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Massachusetts Institute of Technology

The role of AsH_3 partial pressure on anti-phase boundary in GaAs-on-Ge grown by MOCVD – application to a 200 mm GaAs virtual substrate

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Abstract

We demonstrate the influence of the arsine partial pressure (*p(AsH_3)*) on the quality of a GaAs layer grown on Ge substrate by metal organic chemical vapor deposition. The GaAs quality improves with *p(AsH_3)* used during the 100 nm thick GaAs buffer layer. By growing a GaAs buffer layer at 630°C with *p(AsH_3)* of 5 mbar, we obtain a smooth GaAs layer with a root mean square roughness of 4.7 Å. This GaAs layer does not contain anti-phase boundaries. With these optimized growth parameters, we fabricate a virtual GaAs substrate on a 200 mm silicon wafer as a first step towards the integration of III-V devices on silicon.

Keywords

A3. Metalorganic chemical vapor deposition, A1. roughening, A3. Metalorganic vapor phase epitaxy, B1. Gallium compounds, B2. Semiconducting III-V materials

1 Introduction

Although the lattice mismatch (<0.1%) and thermal expansion coefficient mismatch (<1.6% at room temperature) between GaAs and Ge are small, the polar nature of GaAs makes it difficult to obtain high quality GaAs on Ge. GaAs can be deposited in two different orientations on the non-polar Ge lattice, with one orientation being rotated relative to the other by 90° along the growing axis[1]. When two different GaAs orientations are deposited on the same surface, As-As and Ga-Ga bonds form at the domains boundary and propagate in the growing GaAs layer, creating an anti-phase boundary (APB)[1].

Anti-phase boundaries (APB) result in surface roughening in the form of long crack-like structures[2], depressions in the surface[3] or even stacking faults formation[4,5]. APB also act as recombination centers, thereby reducing the photoluminescence (PL) efficiency of the GaAs layer[6]. While surface roughening is detrimental to majority carrier devices because surface scattering decreases channel mobility, a high recombination rate decreases the performances of minority carrier devices such as solar cells or light-emitting diodes. Therefore, the optimization of the GaAs on Ge growth is a first step towards performance improvements of III-V devices on Ge (or Si).

Different techniques have been proposed and experimentally demonstrated to either suppress or reduce APB in GaAs on Ge. An early proposal was to use a non-polar GaAs growing axis (e.g. on {111} or {211} Ge surface)[7,8]. However, <100> orientated Ge wafers are preferred due to their lower cost, greater availability, and more importantly they open a pathway towards integration of III-V devices on Si (100) wafers that are used in CMOS processing. Although the selective area growth of GaAs inside Silicon V-grooves[9,10] or trenches[11] has been demonstrated to prevent the APB formation, the growth of APB-free blanket GaAs on Ge (or Si) by MOCVD still remains challenging.

50 Because of the polar nature of the <100> GaAs growth axis, starting on a double-step
51 Ge surface is required[12]. One way to obtain a double step Ge surface is to use a slightly
52 misorientated Ge wafer (typically between 2 and 10°). Single-domain GaAs growth on such
53 offcut Ge wafers has been demonstrated previously[13]. However, the use of misorientated
54 substrates is an essential but insufficient condition to obtain APB-free GaAs layers. A two-
55 step growth, with a thin GaAs buffer layer with optimized growth parameters, followed by
56 growth of GaAs under more conventional growth conditions, is necessary.

57 Two temperature ranges have been reported for the GaAs buffer layer that allows for
58 the growth of APB-free GaAs layers. One is in the [350-550°C] range[4,14–17] and the
59 second one is in the [600-725°C range][7,17–20]. Between these two temperature ranges,
60 growth of a mixed distribution of GaAs domains occurs, leading to the formation of
61 numerous APB[17]. Although the lower temperature regime reduces the diffusion of Ge into
62 the GaAs layer[14], the higher temperature regime reduces the carbon contamination in the
63 GaAs layer[21]. Furthermore, it is frequent to observe diamond-shape APB-related defects at
64 the GaAs/Ge interface with the low-temperature growth regime[3,15,22]. In addition, using
65 the higher temperature regime, devices grown on Ge substrates such as lasers and solar cells
66 have shown comparable and even better performances than on GaAs substrate[18,21]. This
67 has motivated us to use the higher temperature regime for the GaAs buffer layer.

68 Arsenic atoms play an important role at the Ge surface by creating As dimers with
69 two possible orientations[1] that can lead to two GaAs domains. In addition, the Ge surface
70 exposed to arsine will be covered by a self-limiting As monolayer. Since arsenic has a high
71 vapor pressure, care must be taken to ensure the complete coverage of the Ge surface in order
72 to prevent the formation of APB during the GaAs growth.

73 There are contradictory reports in the literature about the optimized V/III ratio for the
74 GaAs buffer layer growth[13,19,20,23]. Values ranging from 12 up to 120 have been
75 reported. All the cited studies used MOCVD with AsH_3 as the group V precursor, so it is
76 surprising that such a large range of "optimized V/III ratios" was reported.

77 This paper investigates the discrepancies in the reported values for the optimized V/III
78 ratio for APB-free growth of GaAs on Ge. We show that it is the AsH_3 partial pressure
79 ($p(AsH_3)$) during the GaAs buffer layer, and not the V/III ratio, that influences the appearance
80 of anti-phase boundaries (APB). We demonstrate the growth of GaAs on a Ge substrate with
81 a RMS roughness below 5 Å on a 10 × 10 μm^2 scan, with excellent crystalline and optical
82 quality by using an optimized $p(AsH_3)$ of 5 mbar. These optimized growth parameters are
83 used to fabricate a virtual 200 mm GaAs substrate on silicon.

84

85 # 2 Experimental details

86 Epi-ready <100> orientated Ge and GaAs wafers with a 6° offcut towards the nearest
87 (111) plane were used as starting substrates. The growth of GaAs layers was performed in an
88 AIXTRON Crius MOCVD reactor using TMGa and AsH_3 as precursors and 32 standard
89 liters per minute (slm) of H_2 as carrier gas. An optical pyrometer array measured the
90 temperature at the surface of the wafer. GaAs was grown on Ge substrates using a two-step
91 growth process, which consists of a thinner GaAs buffer layer grown with one set of process
92 conditions, followed by a thicker GaAs epi-layer using a different set of growth conditions
93 (Figure 1).

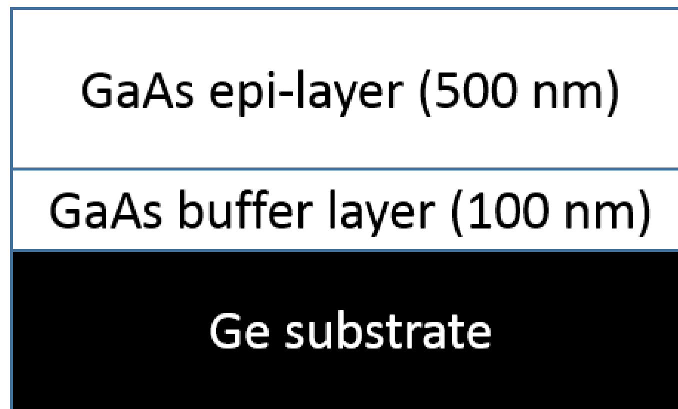


Figure 1: Schematics of the two-step GaAs growth on Ge. A 100 nm GaAs buffer layer is grown with varying growth parameters. Then a 500 nm thick GaAs epi-layer is grown under conventional GaAs growth parameters.

Each growth began with the wafer baked at 650°C under H_2 for 5 minutes in order to initiate a double-step surface. This was followed by the 100 nm thick GaAs buffer layer, which was initiated with a 5-second pre-flow of AsH_3 followed by the introduction of TMGa at a fixed flow rate of 19 µmol/min or 38 µmol/min. The surface temperature, reactor pressure and V/III ratio were varied for the GaAs buffer layer growth of different samples, as listed in Table 1. Following the GaAs buffer layer, a 500 nm thick GaAs epi-layer was deposited. For all samples, growth of the GaAs epi-layer was carried out at 630°C under a reactor pressure of 100 mbar, with a TMGa flow of 96 µmol/min and a V/III ratio of 46.

AFM in tapping mode was used to measure the root mean square (RMS) surface roughness. The interface between GaAs and Ge was observed using cross-sectional TEM at 200kV in a FEI Tecnai tool and a FEI scanning electron microscope (SEM). A 488 nm blue laser coupled to a silicon photo-detector probed the light emission properties of the GaAs layer and the GaAs QW structure at room temperature. The GaAs layer thickness was measured using spectroscopic ellipsometry at 65°, 70° and 75° incidence angle over a [0.7-5] eV energy range. To analyze the crystalline quality of the layers, we used a PANalytical

113 high-resolution X-ray diffractometer equipped with a hybrid 4-bounce Ge(400)
114 monochromator that only let the Cu $K_{\alpha 1}$ radiation pass through. The detector was used in the
115 channel mode configuration for the fast reciprocal space mapping (RSM) or equipped with a
116 symmetric 3xGe (220) triple-axis analyzer to measure the high resolution RSM.

Sample name	Temperature (°C)	V/III ratio	AsH_3 partial pressure (mbar)	TMGa flow (µmol/min)	Reactor Pressure (mbar)	Growth Time (minutes)	Visual inspection of surface
A	630	234	0.3	19	100	21	Cloudy
B	680	234	0.3	19	100	21	Cloudy
C	630	936	1.25	19	100	21	Slightly cloudy
D	630	936	2.5	38	100	10.5	Specular
E	630	936	5	38	200	10.5	Specular
F	630	468	5	38	400	10.5	Specular

117 Table 1: *Process parameters used during the 100 nm thick GaAs buffer layer. All samples are then*
118 *capped by a 500 nm thick GaAs epi-layer grown at 630°C with a V/III ratio of 46.*

119

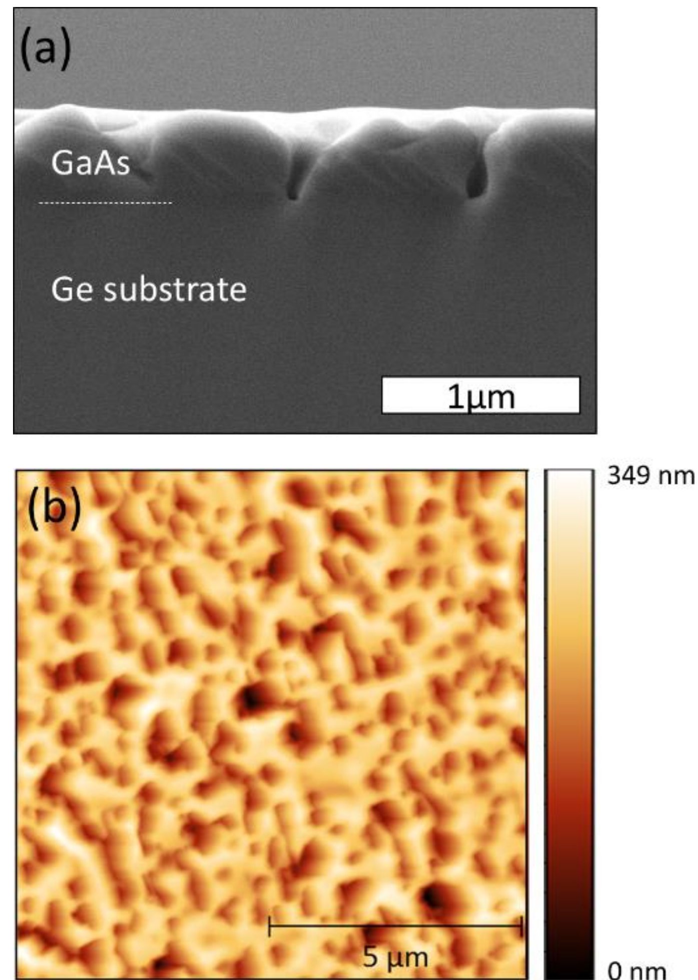
120 # 3 Results

121 ## 3.1 Optimization of GaAs on Ge

122 Sample A, grown with a V/III ratio of 234 at 630°C exhibits a cloudy surface, which
123 is a characteristic of a very rough surface. Indeed, the atomic force microscope (AFM) scan
124 of the surface (Figure 2b) shows numerous pits in the GaAs layer, with a feature size ranging
125 from 100 to 500 nm in both width and length. This leads to a root mean square (RMS)
126 roughness value of 46 nm in a 10 × 10 µm^2 scan. A closer inspection by cross-sectional SEM
127 shows that these pits extend deep into the GaAs layer (Figure 2a). Consequently, the GaAs
128 layer is not continuous but it is composed of islands around 1 µm in length. The measured
129 roughness in this case is likely to be an underestimate of the true RMS roughness,

130 considering the fact that the AFM tip is not able to probe the bottom of the high aspect ratio

131 pits.



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133 *Figure 2: Sample A, the GaAs buffer layer was grown at 630°C with an AsH_3 partial pressure of 0.3*

134 *mbar, a V/III gas phase ratio of 234. (a) Cross-sectional scanning electron micrograph of sample A.*

135 *(b) $10 \times 10\ \mu m^2$ AFM scan of the GaAs surface. The surface is very rough (with a RMS roughness of*

136 *46 nm) and holes (or pits) are observed in the GaAs layer.*

137 Sample B was grown at a 50°C higher growth temperature compared to sample A.

138 The growth resulted in a hazy (or cloudy) surface as well. Microscope inspection revealed the

139 presence of surface pits, which is the characteristic of anti-phase boundaries (APB). The

140 surface pits of sample A (Figure 2b) and B look similar to the results of Wu et al[23].

141 However, unlike their results, we were unable to obtain APB-free GaAs on Ge growth solely

142 by varying the growth temperature. This was despite the fact that sample A and sample B
143 were grown with a V/III ratio of 234, which is higher than the recommended minimum values
144 found in the literature[13,19]

145 Instead, we have found that the large range of optimized V/III ratio in the literature
146 can be explained by the different reactor pressures used in these studies. Indeed, according to
147 equation 1, the arsine partial pressure *p(AsH₃)* is proportional to the reactor pressure.

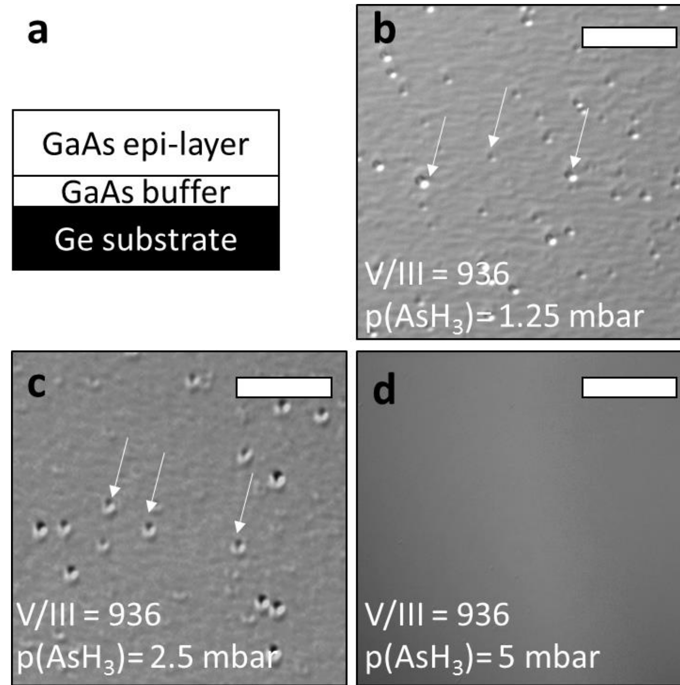
148 $$p(AsH_3) = p(reactor) * \frac{flow(AsH_3)}{total\ gas\ flow} \qquad (1)$$

149 where *p(reactor)* is the reactor pressure, and *total gas flow* includes the carrier gas, TMGa
150 and AsH_3 flow.

151 Therefore, under similar carrier gas and AsH_3 flow, $p(AsH_3)$ can vary by one order of
152 magnitude between an atmospheric pressure (AP) MOCVD and a reduced pressure MOCVD.
153 For instance, Tyagi et al. mention a carrier gas flow of 4 slm[19] (a typical value for an AP-
154 CVD reactor). Assuming a similar AsH_3 flow to ours (800 sccm), Tyagi's $p(AsH_3)$ would be
155 more than 15 times higher than ours, even though the V/III ratio might be approximately the
156 same. This demonstrates that the V/III ratio alone does not completely specify the reactor
157 environment under which the growth is carried out.

158 From our experiments, we found that it was not the V/III ratio but the arsine partial
159 pressure $p(AsH_3)$ that had the most influence on the surface morphology in our set of
160 experiments. As an example, Figure 3 shows Nomarski microscope images of three different
161 GaAs growth conditions, corresponding to sample C, D and E. The only difference was
162 $p(AsH_3)$ during the 100 nm thick buffer layer. The V/III ratio and growth temperature were
163 the same for all three samples. For sample E, the reactor pressure was raised from 100 mbar
164 to 200 mbar in order to increase $p(AsH_3)$ without changing the AsH_3 mass flow (and
165 accordingly V/III ratio), according to equation 1.

166



167 *Figure 3: (a) Schematic of the grown samples. The 100 nm thick GaAs buffer is grown under a V/III*
168 *ratio of 936 and with varying arsine partial pressure. (b-d) Nomarski microscope image of the*
169 *samples C, D and E respectively with the GaAs buffer layer grown under an arsine partial pressure of*
170 *(b) 1.25 mbar, (c) 2.5 mbar and (d) 5 mbar. Numerous surface pits are observed for sample C and D*
171 *(some are highlighted by an arrow) whereas no pits are detected for the sample E. The scale bar is 10*
172 *µm for all Nomarski images.*

173 With $p(AsH_3)$ of 1.25 and 2.5 mbar, although specular to the eye, the GaAs surface is
174 not smooth and contains pits with a density in the order of $10^5/cm^2$ (Figure 3b and 3c).
175 Whereas the sample grown at $p(AsH_3)$ of 5 mbar is free of surface defects and appears
176 smooth when viewed under a Nomarski microscope (Figure 3d). The surface was further
177 analyzed by plan-view SEM (not shown here) and no pits or crack-like structure were
178 detected.

179 The surface of the GaAs (sample E) consists of elongated terraces orientated along the
180 <110> direction (Figure 4) with an average width of 27 nm and a height of 4.4 nm. A similar
181 surface morphology has been observed previously[4,15]. Given that the double atomic steps

182 of the Ge surface are 2.7 nm apart, this suggests that step bunching occurs during the growth

183 of GaAs[15,24]. A larger AFM scan was taken and an RMS roughness value of 4.7 Å was

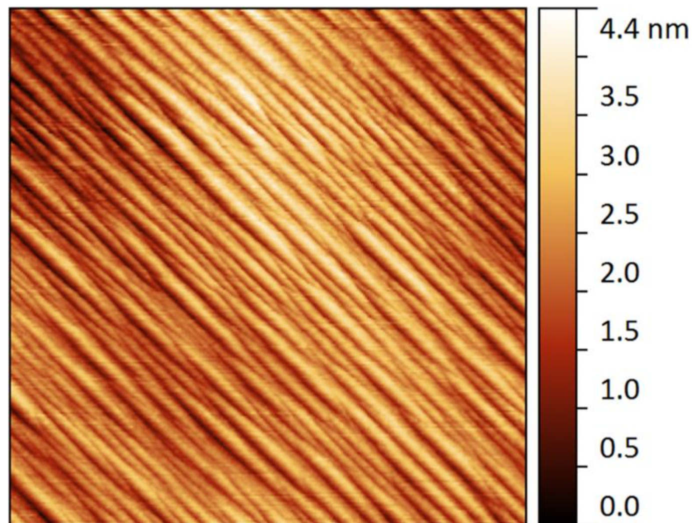
184 measured on a 10 × 10 μm^2 scan. This roughness is more than two times lower than the

185 previously reported roughness of GaAs on Ge using an intermediate quantum dot layer to

186 block the propagation of APB-related defects[2]. Thus, together with the crystalline quality

187 improvement, the surface roughness also decreases when $p(AsH_3)$ increases.

188



189 *Figure 4: 1 × 1 μm^2 AFM image of the GaAs on Ge substrate (sample E). Elongated terraces are*

190 *observed along <110> with an average width of 27 nm.*

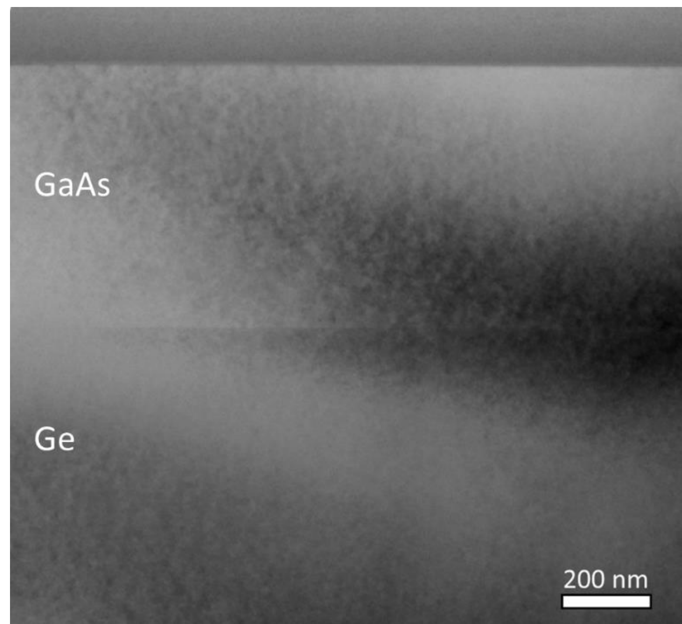
191

192 Sample E was further analyzed by observing the cross-section under TEM (Figure 5).

193 The interface between the Ge substrate and the GaAs layer is abrupt, without any signs of

194 APB features at the interface or in the GaAs layer.

195

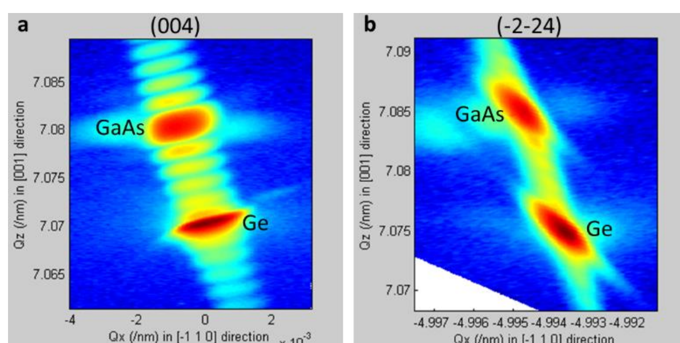


196 *Figure 5: Cross-sectional transmission electron micrograph of the GaAs on Ge using optimized AsH_3*
197 *partial pressure for the initiation layer (sample E), in double beam condition with a <220>*
198 *diffraction vector. No anti-phase boundary or dislocations are detected.*

199 The tilt and strain state of the GaAs layer were calculated using two reciprocal space
200 mapping measured by XRD (Figure 6), according to the method developed by Chauveau[25].
201 The tilt of the GaAs layer in reference to the Ge substrate is 0.0071° in the [-110] direction,
202 which is in the opposite direction of the substrate offcut. This tilt value is comparable to the
203 one reported by Knuuttila for a GaAs grown at 620°C[15]. A tensile strain value of 0.078% is
204 found for the GaAs layer, meaning that the 600 nm GaAs layer is almost fully strained to the
205 Ge substrate, but the relaxation process has started to occur by the formation of misfit
206 dislocations[1].

207

208



209 *Figure 6: Reciprocal space map of the GaAs on Ge sample E taken at the (a) (004) and (b) (-2-24)*

210 *diffraction plane. The interference fringes can be observed in the (004) RSM.*

211 Our experiments clearly shows that the V/III ratio alone does not determine whether

212 APBs form. Indeed, the samples D and E were grown under the same V/III ratio but only

213 sample E shows a smooth APB-free GaAs layer. Rather, we demonstrated that $p(AsH_3)$ is the

214 main factor influencing the formation of APB. Samples E and sample F were grown under

215 the same $p(AsH_3)$ but with different V/III ratios. Both show smooth surfaces without pits. The

216 analysis of sample E confirmed that no APB are observed in the GaAs layer.

217 There are several hypotheses for the dependence of the GaAs layer morphology and

218 crystalline quality on the arsine partial pressure $p(AsH_3)$. First, a low V/III ratio (and

219 consequently a low $p(AsH_3)$) can induce three dimensional growth when initiating

220 heterovalent epitaxy on non-polar surfaces, as demonstrated for GaP on Si growth by Suzuki

221 et al.[26]. Second, the As adsorption at the [-110] step is dependent on $p(AsH_3)$ and

222 temperature[27]. Below a critical $p(AsH_3)$, there might be incomplete surface coverage of the

223 Ge by As, leading to surface sites where Ga atoms might adsorb once TMGa is introduced

224 into the reactor for GaAs growth, thus leading to the formation of APB. Brammertz et al

225 already mentioned that a high As partial pressure is needed in order to prevent the As

226 desorption from the Ge surface[28]. Under our growth conditions, the critical $p(AsH_3)$ lies

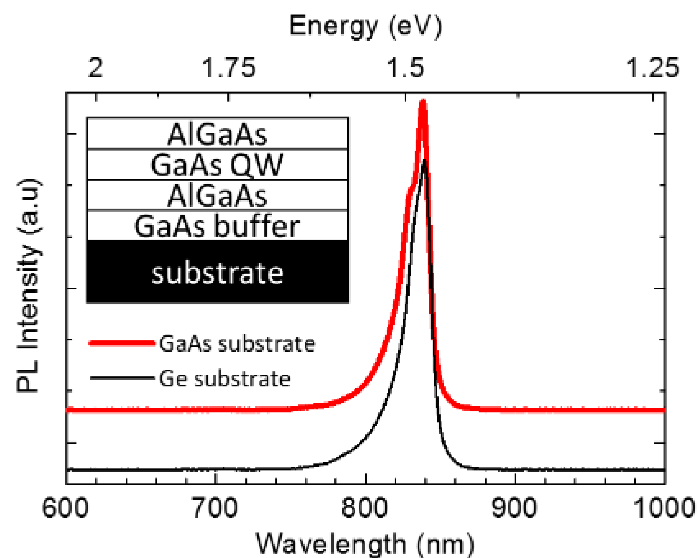
227 between 2.5 and 5 mbar. We expect this critical $p(AsH_3)$ to be lower at reduced growth

228 temperature because the As desorption at the step edges reduces with temperature[27]. A
229 complete mapping of the process conditions (temperature and $p(AsH_3)$) that are necessary to
230 obtain smooth and APB-free GaAs can be performed if epitaxy at different temperatures is
231 desired, but is not the focus of this paper.

232 3.2 GaAs quantum well

233 To further investigate the suitability of the GaAs on Ge layer as a template for further
234 III-V growth, a GaAs QW, cladded by two AlGaAs layers, was grown on another GaAs on
235 Ge sample obtained using the optimized GaAs growth conditions (corresponding to sample
236 E). The AlGaAs was deposited using a TMAl/TMGa molar flow ratio of 0.3, resulting in an
237 AlGaAs composition of 24% Al, as measured by XRD and photoluminescence (PL). The
238 GaAs QW had a nominal thickness of 10 nm.

239 Figure 7 depicts the PL spectra of the QW structure grown both on GaAs and Ge
240 substrates. The PL spectra are similar in shape, with a FWHM of 18 nm, proving the high
241 optical quality of the GaAs layers on both substrates. In the presence of APB, the GaAs PL
242 linewidth has previously been reported to be doubled compared to single domain GaAs[29].
243 This therefore confirms that our optimized GaAs on Ge growth conditions result in the
244 formation of high quality single-domain GaAs on Ge.



245

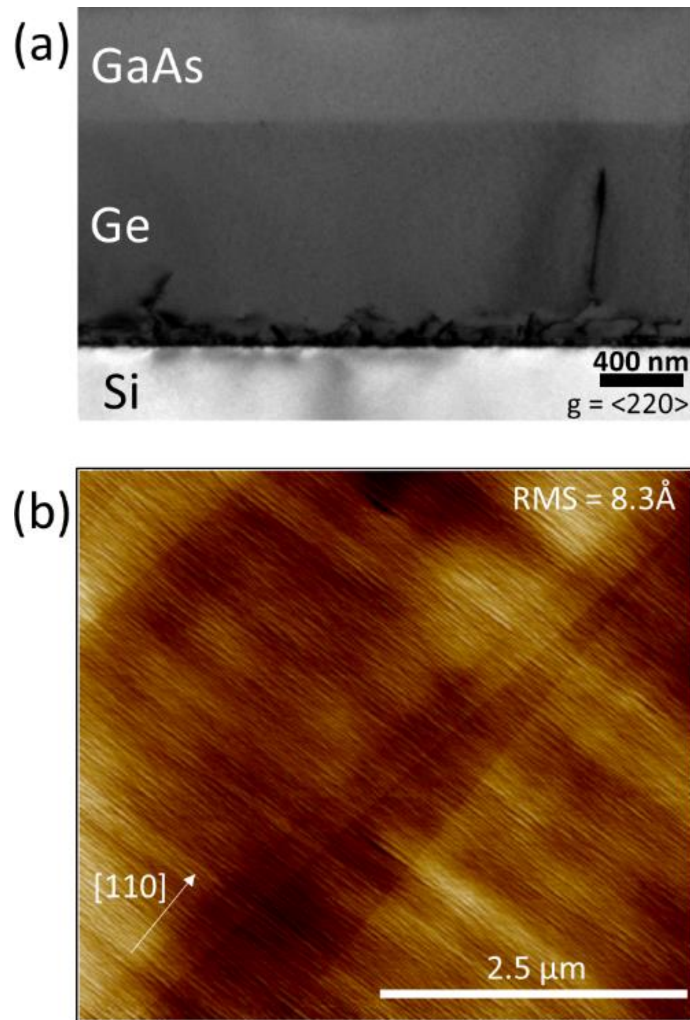
246 *Figure 7: Room temperature PL spectrum of a 10 nm thick GaAs quantum well (QW) cladded by*
247 *$Al_{0.24}Ga_{0.76}As$ layers on Ge and GaAs substrate. Both spectra were taken under the same PL*
248 *conditions with a 488 nm blue laser diode operating at 30mW. The curves are shifted vertically for*
249 *clarity. The peak wavelength is 838.4 nm on GaAs substrate and 839.2 nm on Ge substrate. The*
250 *FWHM for both samples is 18 nm and the intensity are comparable, demonstrating a comparable*
251 *optical quality.*

252

253 ### 3.3 Application to a 200 mm GaAs on silicon substrate

254 To extend our study, the optimized growth conditions of GaAs on Ge were used to
255 fabricate a 200 mm GaAs virtual substrate on a starting Si wafer. Using our previous
256 knowledge on the two-step growth of Ge on Si[30], 1 µm of Ge was deposited on a 200 mm
257 Si (100) wafer, followed by 1 µm of GaAs (100 nm of buffer and 900 nm of epi-layer) and a
258 thin capping layer of AlGaAs. The AlGaAs capping helps in passivating the GaAs surface so
259 that room temperature PL can be measured[31].

260 As shown in the cross-sectional TEM image (Figure 8), the interface between GaAs
261 and Ge is free of crystalline defects, and no sign of anti-phase boundaries (APB) are detected
262 in the GaAs layer. This compares favorably with a report of the latter structure grown by
263 MBE, in which APB were detected at the GaAs/Ge interface[32]. The contrast at the Si/Ge
264 interface is due to the abrupt relaxation of the 4.2% lattice mismatch creating an array of
265 misfit dislocations. Our previous work[30] has shown that the threading dislocation density
266 (TDD) in the Ge layer is in the range of low-10^7 cm^{-2}, and we expect a similar TDD to be
267 propagated in the GaAs layer.



268

269 *Figure 8: (a) Cross-sectional transmission electron microscope image of the GaAs on Ge on Si*
270 *sample, observed under the <022> two-beam diffraction condition. The interface between GaAs and*
271 *Ge is abrupt and free of crystalline defects. No anti-phase boundaries were detected in the GaAs*
272 *layer. Misfit dislocations are visible at the Ge/Si interface with one threading dislocation segment*
273 *extending in the Ge layer. (b) 5 × 5 μm² atomic force microscope image of the surface of the*
274 *GaAs/Ge/Si sample. The root mean square roughness is 8.3Å. The cross-hatch pattern is due to the*
275 *strain field generated by the misfit dislocations at the Ge/Si interface along the <110> direction.*

276 The GaAs surface is smooth with an 8.3Å RMS roughness measured on a 5 × 5 µm^2
277 scan area, as shown in Figure 8b. The surface morphology is very similar to the GaAs layer
278 on Ge substrate, with steps visible in the [1-10] direction. However, the roughness is higher

279 than the GaAs on Ge substrate. This is due to the underlying roughness of the Ge layer on Si,

280 measured at 7.5Å RMS in our previous study[30].

281 Two important observations can be made of our results. First, the roughness of the

282 GaAs layer is similar to the roughness of the underlying Ge layer, as opposed to the work

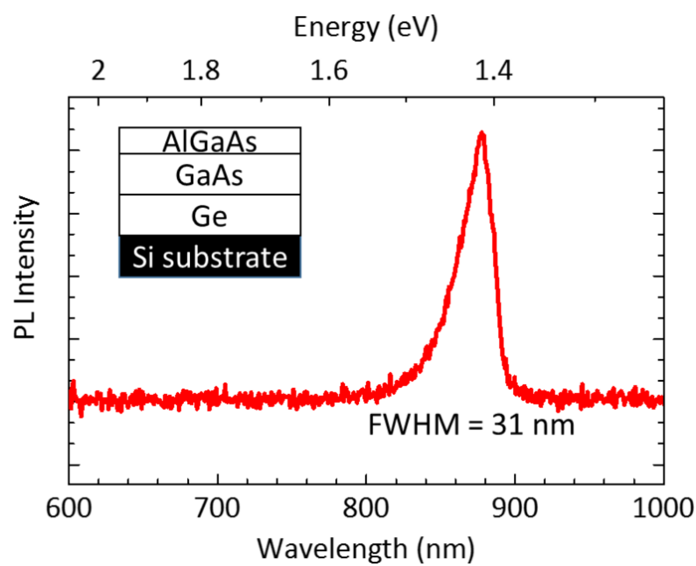
283 from Waldron et al. in which the roughness doubled between the GaAs and the Ge layer[33].

284 Second, a low RMS roughness value (below 1 nm, see Figure 8), similar to the work of Zhou

285 et al can be achieved, without using an intermediate polishing step and a GaAs regrowth[4],

286 therefore simplifying the growth process.

287



288

289 *Figure 9: Room-temperature photoluminescence spectrum of the GaAs layer showing the GaAs peak*

290 *energy at 1.415 eV with a FWHM of 31 nm*

291 The high optical quality of the resulting GaAs layer is demonstrated by the low

292 FWHM value of the room temperature PL spectra (Figure 9). The GaAs peak wavelength is at

293 1.415 eV with a linewidth of around 31 nm, a typical value corresponding to the parabolic

294 band-to-band recombination. This FWHM value is similar to the recently published results of

295 GaAs on Silicon using aspect ratio trapping technique[11] and confirms the high optical

296 quality of the grown layer. The peak wavelength is red shifted by 15 meV compared to a
297 GaAs reference film measured under the same conditions in our PL system. This red shift can
298 be explained by the strain state of the GaAs layer.

299 The strain state of the GaAs layer has been measured by XRD (Figure 10). We found
300 that the GaAs layer has an in-plane lattice constant of 5.6621 Å and an out-of-plane lattice
301 constant of 5.6435 Å. Compared to the unstrained GaAs lattice constant of 5.6532 Å, the
302 GaAs layer grown on the Si-on-Ge template is 0.16% strained (tensile strain). This tensile
303 strain, originated from the thermal expansion mismatch between the silicon substrate (2.6
304 ppm/°C) and the GaAs layer (5.7 ppm/°C), will produce an up-shift of the light holes valence
305 band and a down-shift of the conduction band at the Γ point[34] according to the following
306 equations:

307 $$\Delta E_c = 2a_c\left(1 - \frac{C_{12}}{C_{11}}\right)\varepsilon \quad (2)$$

308 $$\Delta E_{lh} = \left[-2a_v\left(1 - \frac{C_{12}}{C_{11}}\right) - b\left(1 + 2\frac{C_{12}}{C_{11}}\right)\right]\varepsilon \quad (3)$$

309 With C_{11} and C_{12} are the stiffness constant of GaAs, a_c and a_v are the conduction band
310 and valence band hydrostatic deformation potential respectively, b is the shear deformation
311 potential and ε is the biaxial strain. The numerical application is shown in Table 2. The
312 calculated bandgap reduction is 20 meV which agrees with the experimental value of 15
313 meV. The large range of reported for of a_c and a_v[35] can explain the small difference.

Parameter	Value	Units
a_c	-7.17	eV
a_v	-1.16	eV
b	-2	eV
C_{11}	1221	GPa
C_{12}	566	GPa
ε	0.16	%

ΔE_c	-12	meV
ΔE_{lh}	8	meV
ΔE	20	meV

Table 2: *Parameters used in the calculations of the bandgap lowering due to the strain in the GaAs layer and the resulting conduction band downshift, light hole valence band upshift and the net resulting bandgap reduction. The 20 meV value matches the 15 meV red shift measured experimentally.*

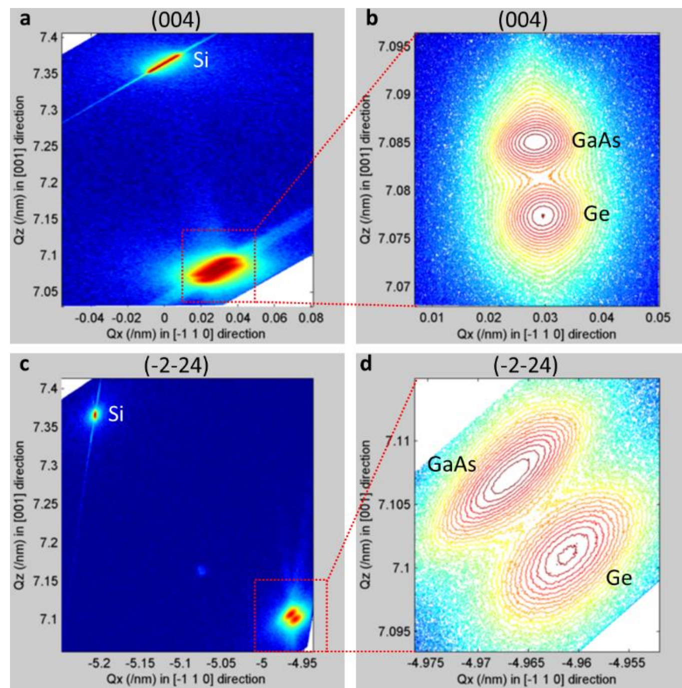
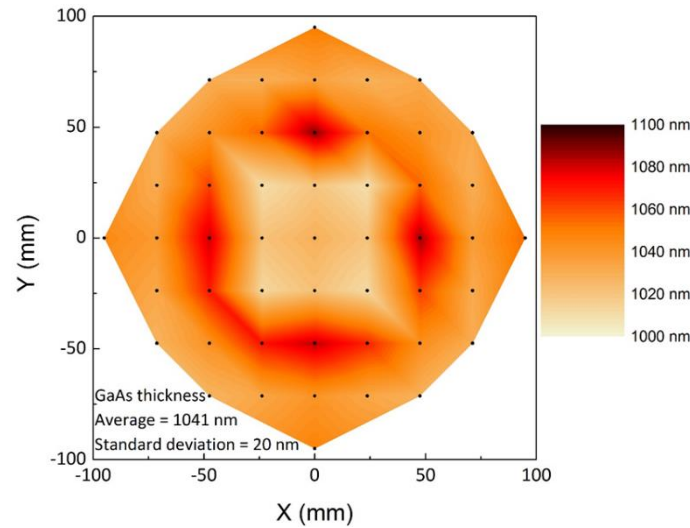


Figure 10: Reciprocal space map of the GaAs on Ge-on-Si sample taken along the (004) and (-2-24) diffraction plane. The large RSM (a) and (c) were taken using an array detector while the zoomed-in RSM (b) and (d) were measured using an analyzer crystal placed in front of the detector. The GaAs layer is under 0.16% tensile strain. This tensile strain is accumulated during the cooldown from growth temperature, due to the thermal lattice mismatch between the silicon substrate.

326 The GaAs thickness uniformity has been measured by spectroscopic ellipsometry
327 (Figure 11). The average GaAs thickness is 1041 nm with a standard deviation of 20 nm,
328 proving the high uniformity of the growth process.

329



330

331 *Figure 11: GaAs layer thickness mapping on the 200 mm wafer measured with spectroscopic*
332 *ellipsometry. The average GaAs layer thickness is 1041 nm and the standard deviation is 20 nm.*

333 # 4 Conclusion

334 In conclusion, we have demonstrated that the arsine partial pressure $p(AsH_3)$, and not
335 the V/III ratio, is the key factor influencing the heteroepitaxy of GaAs on Ge in the high
336 temperature regime. We have shown that below a critical $p(AsH_3)$, the GaAs layer contained
337 surface pits extending down in the GaAs layer. The crystalline quality of the GaAs layer
338 increases together with $p(AsH_3)$. By using a $p(AsH_3)$ of 5 mbar, we have obtained very
339 smooth GaAs layers without anti-phase boundaries and that are of a high crystalline and
340 optical quality.

341 We have also demonstrated the feasibility of 200 mm GaAs virtual substrate
342 fabrication on Si, by employing an intermediate Ge layer. The surface roughness (below 1

nm) was low and comparable to the underlying Ge layer, without requiring any polishing step. We have demonstrated the high optical quality of the GaAs layer with the narrow lineshape obtained by photoluminescence. This GaAs-on-Si virtual substrate can be used as a starting wafer for the growth of III-V electronic and optical devices.

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