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Growth of InGaAs-Channel Transistor Layers on Large-Scale Si Wafers for Hetero-Integration with Si CMOS

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Abstract

We report on the growth of In$_{0.30}$Ga$_{0.70}$As channel high-electron mobility transistor (HEMT) epi-layers on a 200 mm silicon wafer by metal organic chemical vapor deposition (MOCVD). The device epi-layers were grown on a silicon substrate by using a ~ 3 μm thick buffer comprising a Ge layer, a GaAs layer and an InAlAs compositionally graded, strain relaxation layer. The achieved epitaxy has a threading dislocation density of (1 – 2) × 10^7 cm^{-2} and a root mean square surface roughness of 6-7 nm. The device active layers include a delta-doped InAlAs bottom barrier, a 15 nm thick InGaAs channel, a 15 nm InGaP top barrier layer and a heavily doped InGaAs contact layer. Long channel MOS-HEMT devices (L_G ~ 20 μm), were fabricated achieving a peak effective electron mobility of ~ 3700 cm^2/V·s.

INTRODUCTION

New kinds of hybrid circuit can be enabled by integrating InGaAs based analog devices with Si CMOS based digital devices, which draw benefits from both technologies. The first benefit is the computing power and device density of the Si CMOS logic. The second benefit is the high frequency capabilities of the InGaAs high electron mobility transistors (HEMTs) [1, 2].

To enable this integration, both the InGaAs and Si platform have to use compatible substrate sizes. Most Si CMOS manufacturers use silicon substrates of 200 - 450 mm in diameter. This size wafer is expensive or not even available for GaAs or InP, which are the suitable and commonly utilized substrate materials for growth of InGaAs HEMT layers. This makes integration of these substrates with silicon a challenging hurdle.

At SMART LEES, to overcome this draw-back, we address this integration issue by growing InGaAs HEMTs on 200 mm silicon substrates. Such III-V HEMTs will
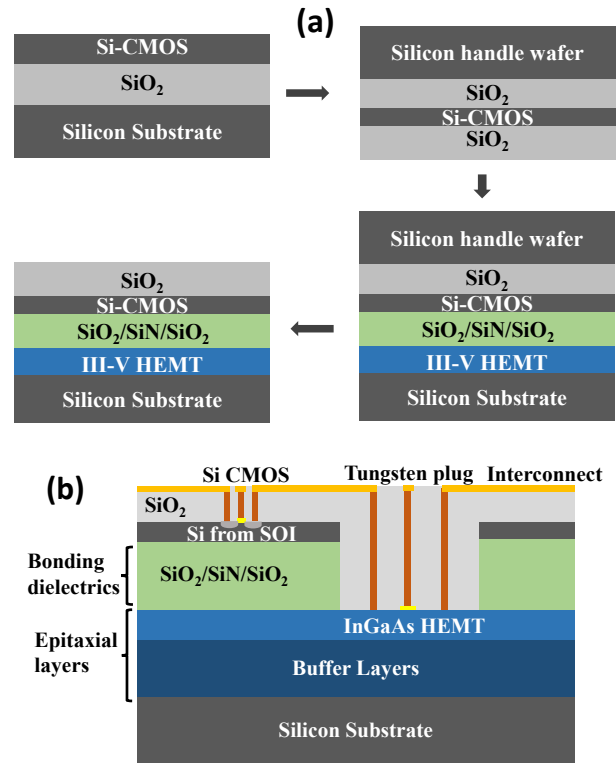

Fig. 1. (a) Schematic flow of the double layer bond and transfer process. (b) InGaAs HEMT integration with Si CMOS on large diameter wafers.

ultimately be integrated with a Si CMOS layer directly at the wafer level through wafer bonding steps, as shown in Fig. 1 (a). Details of process steps are as follows: on the silicon substrate with silicon-on-insulator (SOI) including front-end CMOS foundry fabrication of circuit design first growth of

SiO$_2$ is established on top with this layer subsequently bonded to a Si handle wafer. This is followed by the removal of the Si substrate from the SOI wafer. On a separate Si wafer, an InGaAs HEMT is grown and then attached to the SOI surface of the CMOS – SOI by using SiO$_2$/SiN/SiO$_2$ bonding dielectrics. Following the removal of the Si handle wafer, etching through the SOI wafer enables access to the surface of the InGaAs HEMT. Next, the InGaAs HEMT is processed by a CMOS compatible processing flow. Via-through channels are etched to allow the CMOS as well as HEMT to be wire connected. Interconnects between both devices are established at the wafer surface using back-end CMOS foundry fabrication. The final structure of the stacked CMOS and III-V devices is depicted in Fig. 1 (b).

MOCVD is the preferred III-V-on-Si growth method due to its high throughput, which is suitable for mass production. In 2011, Mukherjee et al. (Intel corp.) reported that InGaAs HEMTs on Si obtained by MOCVD are comparable with those from MBE growth [7]. Therefore, MOCVD was selected in our work.

There are two common approaches to produce buffer layers for InGaAs HEMTs on Si. The first one is low temperature growth of InAlAs compositional graded buffer on GaAs as virtual substrate on Si [5]. The second one is direct growth of InP buffer layer on GaAs on Si. [6, 7]. The advantages of these approaches are (1) higher electron mobility with high Indium content (52% - 70%) and (2) relatively smoother surface. However, they result in very high threading dislocation densities (TDD) ($>10^9$ cm^{-2}) which may result in poor device reliability and yield.

Our approach focuses on using Ge and GaAs intermediate layers and an InAlAs compositionally graded buffer layer grown at high temperatures to achieve a TDD of $(1\text{-}2) \times 10^7$ cm^{-2} [10 - 12].

EXPERIMENTAL PROCEDURE

The starting substrates were 200 mm <100> orientated Si wafer with a 6° offcut towards the nearest (111) plane. Prior to their loading into the AIXTRON Crius MOCVD reactor, wafers were chemically cleaned by SC1 and SC2 solutions and followed by a HF dip. The Si wafers were baked at 1050 °C under 400 mbar of H$_2$ for 10 minutes to desorb any native oxide and contaminants before growth. The Ge buffer layer was grown in a two-step sequence; 100 nm Ge was grown at 400°C and 700-900 nm Ge was grown at 650°C. In order to decrease the dislocation density to $\sim 1 \times 10^7$ cm^{-2}, the wafer was subsequently annealed in reactor chamber at temperatures of 850°C and then 680°C, in both cases for 10 minutes [13, 14].

For the III-V growth, the Ge-on-Si wafers were baked for 5 minutes at 650°C under H$_2$ ambient to remove the Ge native oxide. Then a two-step GaAs layer was grown at 630°C to ensure an anti-phase boundary (APB) free layer, as described in our previous work [15].

The InAlAs graded buffer was grown by keeping the V/III ratio constant at 50, maintaining a constant group III

flow of 44.8 μmol/min, and varying both the TMIn and TMAl flows linearly. The composition of the graded buffer was varied linearly from AlAs to In$_{0.30}$Al$_{0.70}$As [11].

The HEMT stack, shown in Fig. 2, was grown at 630°C and was targeted to be lattice matched to the graded buffer
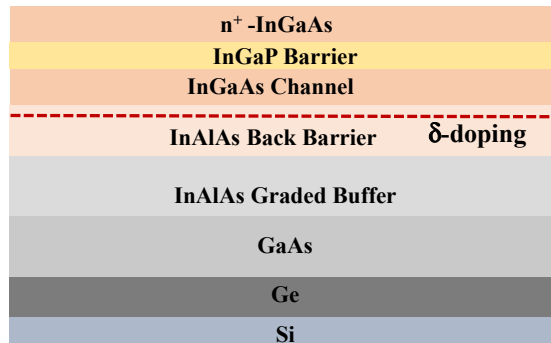

Fig. 2. Structure of InGaAs device epi-layer grown on Si substrate.

capping layer. A bottom Si δ-doping layer was introduced a few nanometers below the InGaAs channel. To achieve this, the growth was paused by switching off the group III flow and SiH$_4$ was flowed for 10 s into the reactor. A 15 nm thick In$_{0.30}$Ga$_{0.70}$As channel was grown using TMIn and TMGa. The top barrier layer was In$_{0.80}$Ga$_{0.20}$P grown under PH$_3$ ambient with a thickness of 15 nm. The n-type doped InGaAs contact layer was grown using SiH$_4$ and DETe as doping sources.

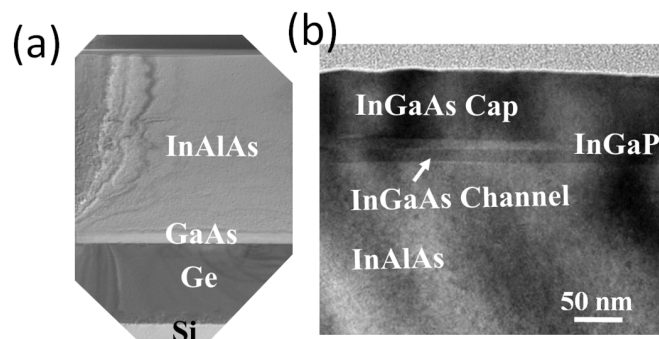RESULTS AND DISCUSSION

1) InGaAs channel device layers

Fig. 3. Cross-section TEM images of epi-stack. (a) Ge, GaAs and InAlAs buffer layer and (b) InGaAs device layer.

TEM images of the InGaAs device layer and buffer layers are shown in Fig. 3. As seen in the TEM images, misfit dislocations were mainly confined to the Ge, GaAs and InAlAs graded buffer layer. The HEMT stack layer is virtually free of dislocations. A zoomed-in image of the device layers is shown in Fig. 3 (b). No dislocations are

observed in this image, which indicates that the threading dislocation density is lower than 1×10^8 cm^{-2}.
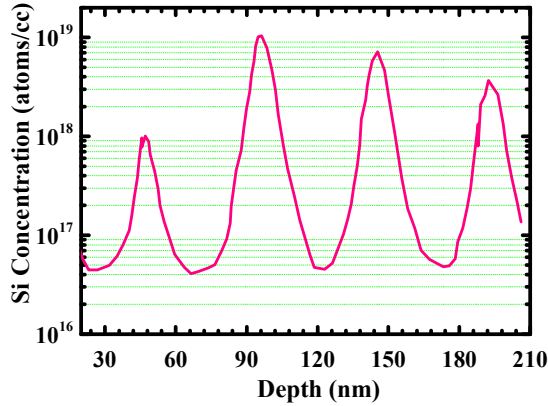
2) Si delta doping profile

Fig. 4. Doping profile with four SiH$_4$ flow conditions for Si delta doping in the InAlAs layer measured by SIMS.

In the HEMT structure, delta doping in the InAlAs buffer layer provides carriers while maintaining high electron mobility in the InGaAs channel. In HEMT layer growth using MBE, the control of delta doping can be within ~ 1 nm. However, during MOCVD growth, delta doping at the InAlAs layer may diffuse into the channel layer due to higher growth temperatures. Fig. 4 shows the SIMS profile of the silicon δ-doping achieved with four different SiH$_4$ flow conditions. The doping level is controllable by changing the flow of SiH$_4$ gas. The FWHM of the doping profile is ~15 nm and the InAlAs back barrier thickness was chosen accordingly, to minimize the dopant diffusion into the channel layer.

3) Doping of the InGaAs contact layer

A highly doped InGaAs capping layer is critical to reduce external series resistance of the devices. We introduced a co-doping technique with Te and Si dopants to maximize the doping level in the layer. There is a delay in time between the start of flowing DeTe and the onset of Te incorporation in an epitaxial layer [16], and therefore the use of Si in the InGaAs contact layer solves that issue to provide highly doped InGaAs throughout the entire layer. By using Si and Te co-doping technique, a reduction of series resistance, R$_{SD}$ from 2.40 kΩ·μm to 1.08 kΩ·μm was obtained in the InGaAs HEMT devices [12]. We achieved a carrier concentration of ~2.5×10^{19} cm^{-3} (obtained via Hall Effect measurement) in an In$_{0.30}$Ga$_{0.70}$As cap layer grown at 550°C.

4) Device fabrication and results
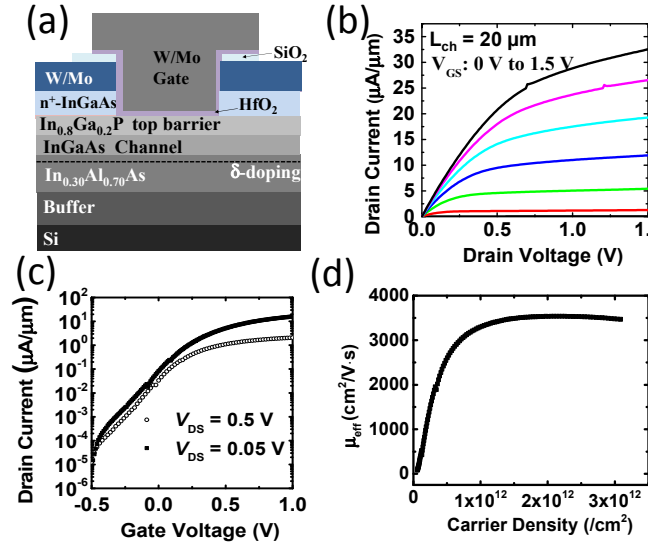
Long channel MOS-HEMT devices were fabricated on

Fig. 5. (a) Cross-section schematic of the HEMT device; (b) I_D-V_{DS} and (c) I_D-V_{GS} characteristics of a device with L_{CH} of 20 μm; (d) effective channel mobility of the device.

samples from the above described wafers with the structure as shown in Fig. 5 (a). I_D-V_{DS} characteristics of a device with L_G of 20 μm are shown in Fig. 5 (b) with V_{GS} varying from 0 V to 1.5 V, indicating good pinch-off characteristics and absence of negative differential resistance. The I_D-V_{GS} curve shows high I_{ON}/I_{OFF} of larger than 5 orders of magnitude (in Fig. 5 (c)) with low off-state leakage current. Electron mobility in the 2-DEG channel extracted using C-V and I-V data of a 20 μm long channel device, and corrected for series resistance, peaks at 3700 cm^2/V·s, as shown in Fig. 5 (d).

CONCLUSIONS

We have reported on the growth of an In$_{0.30}$Ga$_{0.70}$As HEMT on 200 mm silicon substrate. Long-channel HEMTs were fabricated from the material using CMOS-compatible processing. By using a buffer layer stack comprising Ge, GaAs and InAlAs graded buffer layers, a TDD of (1 - 2) ×10^7 cm^2 was achieved. Long-channel HEMT revealed an electron mobility of 3700 cm^2/V·s in the 2-DEG of the device, showing the potential of this approach for low power and high frequency analog devices grown on silicon.

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ACRONYMS

MOCVD: Metal organic chemical vapor deposition
MBE: Molecular Beam Epitaxy
CMOS: Complementary Metal-Oxide Semiconductor
MOS-HEMT: Metal Oxide Semiconductor - High electron mobility transistor
TDD: Threading dislocation density

TEM: Transmission Electron Microscopy
2-DEG: 2 dimentional electron gas
TMIn: Trimethylindium
TMAl: Trimethylaluminium
TMGa: Trimethylgallium
DETe: Diethyltelluride
SC1: Standard clean for particles and chemical impurities removal
SC2: Standard clean for alkali residue and any residual trace metal