Body Coupled Communication: The Channel and Implementation
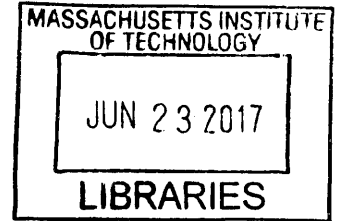
by

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B.S., University of Utah (2009)
M.S., University of Utah (2009)

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Abstract

To achieve comfortable form factors for wearable wireless medical devices, battery size, and thus power consumption, must be curtailed. Often the largest power consumption for wireless medical devices is storing or transmitting acquired data. Body area networks (BAN) can alleviate power budgets by using low power transmitters to send data locally around the body to receivers that are on areas of the body that allow for larger form factors, like the wrist or the waist. Body coupled communication (BCC) has been shown to have great potential in forming a BAN. This work expands the potential of BCC BANs by showing that BCC can include implanted nodes. Implants being able to implement BCC is an impactful discovery as previous BCC channel models have implicitly stated that BCC cannot work with implants. This discovery will allow BANs that include implants, such as pacemakers, to utilize the power efficiency of BCC.

This thesis will give an introduction to BANs and BCC. It will further detail three contributions to BCC and its implementation. The three contributions are: 1) an excellent understanding of the BCC channel, that is verified by careful measurements, 2) a new amplifier circuit that improves the signal to interferer ratio, and 3) an asynchronous digital communication scheme that offers a high data rate and low power implementation. An integrated transmitter and receiver were fabricated in a 0.18 μm CMOS process. The results of the three contributions as implemented in the integrated chips are also presented and discussed. The integrated receiver was able to receive information at 16 Mbps, while consuming 5.9 mW, yielding an energy use of 367 pJ/bit. The integrated transmitter was able to transmit information at 30 Mbps, while consuming 4.32 mW, yielding an energy use of 114 pJ/bit.

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Acknowledgments

Contents

List of Figures

10

11

List of Tables

Chapter 1

Motivation and Background

Biological signals, such as the electrocardiogram (ECG) and electroencephalogram (EEG), are often recorded in areas of the human body where attaching sensors with large form factors would not be comfortable and therefore are not compatible with long-term recording. Making sensors with small form factors places limits on battery size, requiring the sensors to have low power budgets if long-term use is desired. Due to the low frequency bandwidth of most biological signals and advances in low power circuitry, the circuits that detect and amplify biological signals are quite low power. The largest power consumption for medical sensors usually comes from storing the captured data to memory or wirelessly transmitting the information off the body. Body area networks (BAN) alleviate power budgets for medical sensors by providing a low power localized network around the human body in which the sensors can send data to a base station that is on the body. The on-body base station can then retransmit the data off the body, or store it to memory. Most existing commercial BANs utilize radio, such as Bluetooth low energy, as the network channel. A potential alternative to radio-based BANs is body coupled communication (BCC).

1.1 Body Area Networks

While sensor nodes are usually in areas of the body that patients desire small form factors, there are areas of the body that can support larger form factors for longer periods of time, such as the waist and wrist. Placing a base station on an area of the body that can

comfortably support a larger form factor enables the base station to have a larger battery. With greater power capacity, the base station can then perform the higher power functions of storing data to memory or transmitting the information off the body. Having such a base station can alleviate the power budget of the sensor node if the power required to send data to the base station is lower than the power required for the sensor node to store the data in memory or transmit it off the body. For some applications, processing can be done at the sensor node to reduce the amount of information sent over the BAN. Such a BAN can be seen in figure 1-1.

BANs have been implemented using a variety of channels, including: textiles embedded with wires [1], low power radio [2], and body coupled communication (BCC) [3]. The eTextiles have the lowest amount of signal attenuation in the channel, as the channel is simply wires, and as such the receiver doesn't need to amplify the signal and therefore energy requirements are reduced. The drawback of eTextiles is the user is required to wear specialized clothing and the sensor must be located in areas covered by the eTextiles. Forming a BAN using radio or BCC allows for greater flexibility for sensor locations, at the price of higher attenuation in the channel and hence higher power dissipation for equivalent data transmission compared to wired. BCC and ultra-wide band (UWB) radio have been shown to have similar energy per bit efficiencies, while BCC outperforms narrow band radio (NB), as seen in figure 1-2 [3].
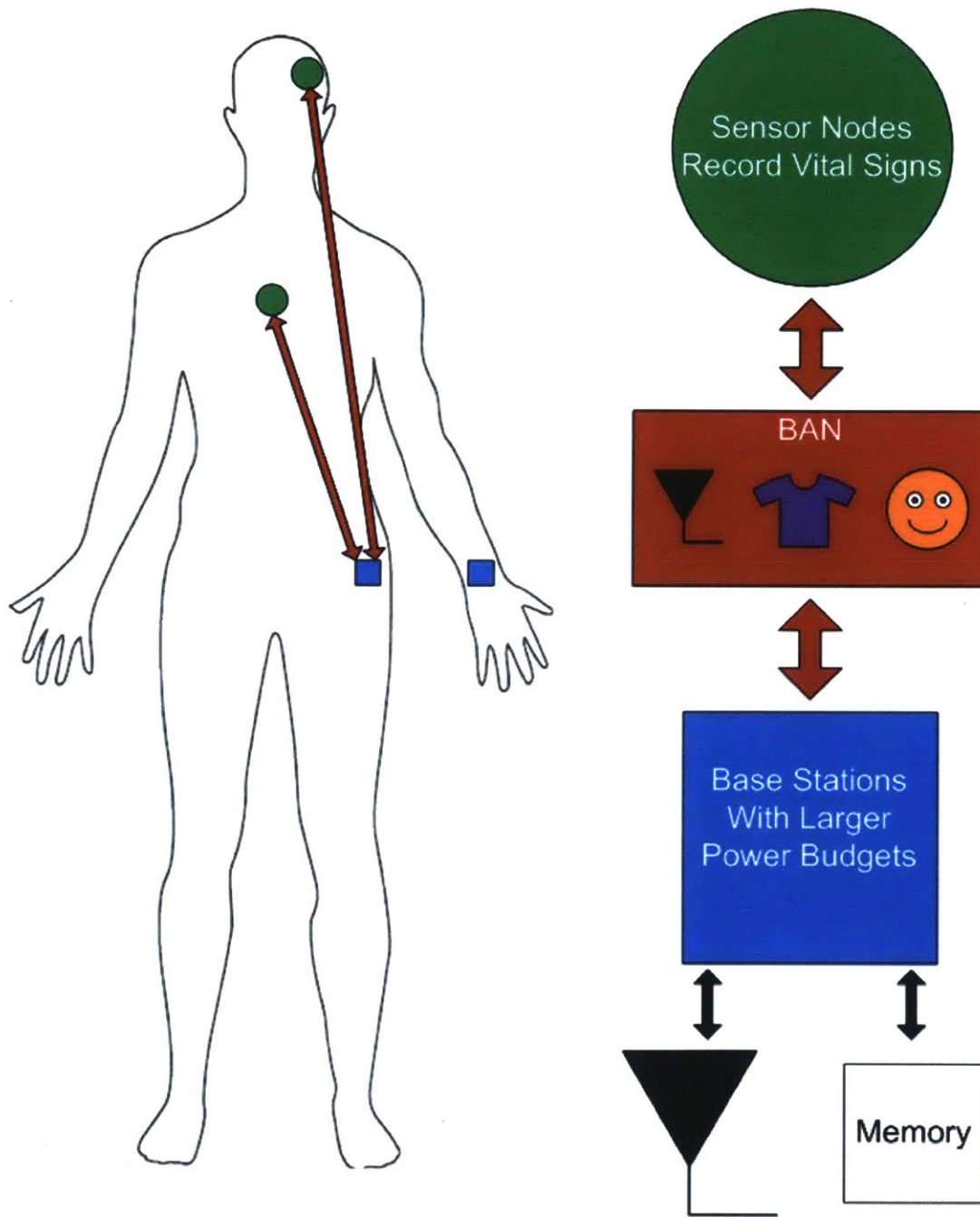
Figure 1-1: Body area network diagram. There are various ways to implement body area networks including eTextiles, radio, and BCC.
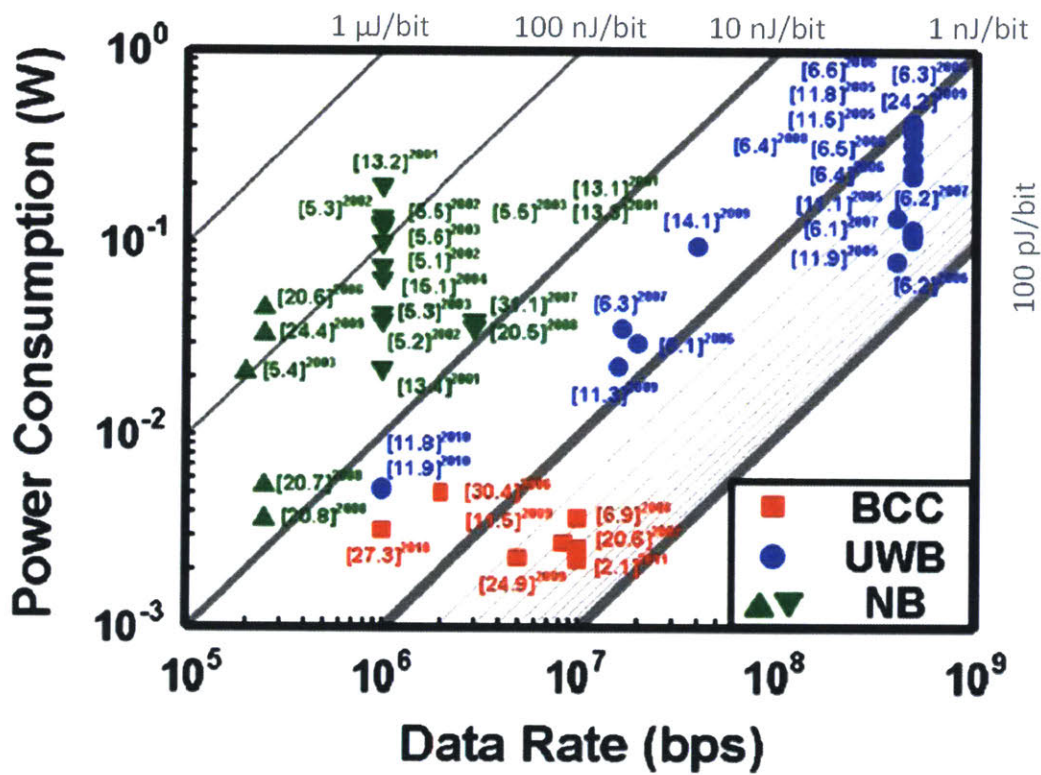
Figure 1-2: Energy efficiency of UWB and NB radio, and BCC transceivers as found in [3].

1.2 Use Models for BCC

There are two properties of BCC that make it highly attractive to form BANs. Both result from BCC using the electric near-field which attenuates proportional to the distance cubed [4]. Because the power in the near-field signal attenuates so quickly this inherently allows for greater security than radio, because conspicuously close proximity to the body is required to connect to the network. The rapid attenuation of the signal also reduces interference from other BCC networks, which allows for reusable bandwidth.

The base station for many sensor applications could use a smartphone equipped with a BCC transceiver. As the smartphone would have to be in close proximity to the body to receive the data, the phone could be in a pocket or a case attached to the belt. If the use model for the sensor network were to render a smartphone base station impractical, a wrist watch BCC transceiver may work.

In addition to BCC replacing radio in BAN use models, like Bluetooth, BCC opens up a new use model known as "touch-to-connect". This use model utilizes the fact that devices using BCC have to be close to the body to communicate to each other; so BCC devices can assume that if two BCC nodes can talk to each other, then the nodes should automatically perform a digital hand shake and see if further communication is desired. This alleviates the step of pairing devices before they'll communicate with each other that Bluetooth requires. Touch-to-connect would allow for such use models as touching a computer to log-in, touching your home's door knob to unlock the door, sitting in a car seat and having your car link with your cell phone, etc.

BCC can also work with implants. This functionality means that devices such as pacemakers can use the same leads they use to regulate the heart as BCC electrodes, allowing the pacemaker to communicate with devices that are outside of the body — a much better alternative than the current method of getting signals in/out of the pacemaker's Faraday cage-like titanium can.

21

1.3   Contributions

There have been previous publications that have characterized the BCC channel, BCC tranmitters, and BCC receivers [3–18]. Many of these publications have proposed channel models that disagree with each other. This work builds off these publications and develops an accurate electrical channel model, validated by a custom battery-powered channel measurement system and through careful measurements. Once an accurate channel model is established, the work details two improvements to BCC communication that will aide in BCC commercialization.

This work makes three contributions to BCC technology:

1. A better understanding of the BCC channel, that is verified by careful measurements in chapter 2.

2. A new amplifier circuit has been designed and characterized, that can improve the signal to interferer ratio and detailed in chapter 3.

3. An asynchronous digital communication scheme that offers a high data rate and low power implementation. The scheme is explained in chapter 4, and an implementation of it is characterized in chapter 5.

Chapter 2

Introduction to Body Coupled Communication

BCC makes capacitive links with the human body and the environment to form a channel in which AC current can be transmitted. Both the transmitter and the receiver have two electrodes that capacitively couple with the body and the environment. The electrodes make the capacitive links with the body and the environment by forming one plate of a parallel plate capacitor, while the other plate is formed either by the conductive tissues in the human body or the environment (figure 2-1). These capacitive links, as well as the capacitive link between the human body and the environment, form the circuit shown in figure 2-2. The environment can be anything that is conductive in the area around the human body, from a chair or table, to the physical ground itself.
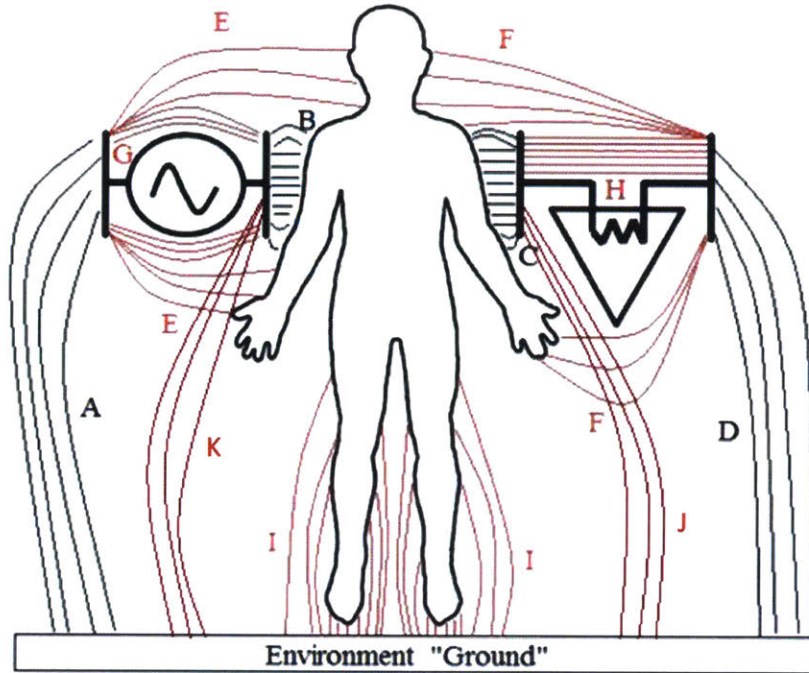
Figure 2-1: The BCC channel. The electrodes on the transmitter and receiver form capacitive links A-K.
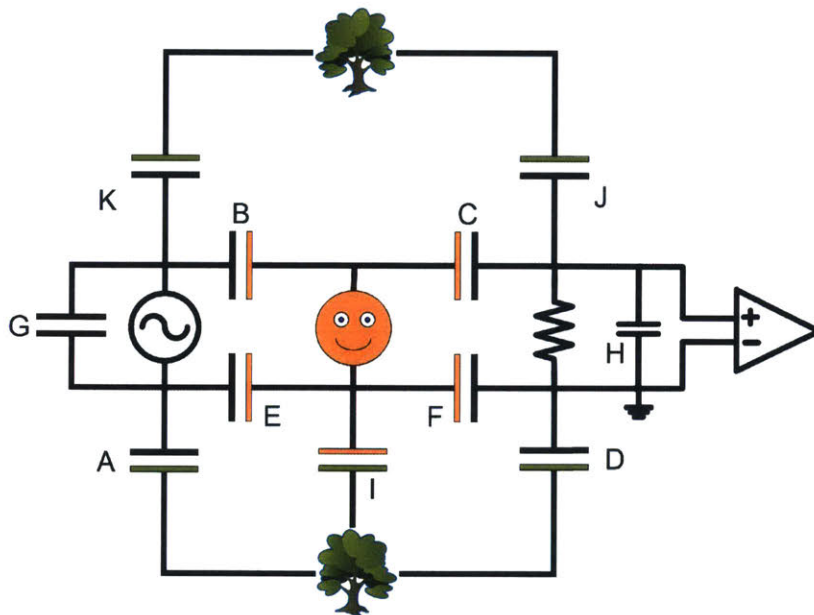
Figure 2-2: The circuit diagram from figure 2-1 where the color of the capacitor plates are color coded with black to be electrodes, green the environment, and peach the body. The resistor is the input impedance of the receiver.

Most published BCC channel models neglect to show the capacitances 'J' and 'K' between the environment and the electrode as seen in figure 2-3. While it is not clear why others omit these capacitors, to keep diagrams in this work consistent with other publications, this work will also omit them. This is reasonable for at least two reasons. First, the electrodes can be shielded, preventing the electrode from making such capacitive links. Second, the final BCC channel model that will be set forth in this work will show that the capacitive links 'A', 'I', 'D', 'J', and 'K' can all be ignored.

From this starting model of the BCC channel there have been opposing views on the dominant current path of the body and how the body should be modeled electrically in the BCC channel. Some of these differences can be attributed to different frequency ranges used in testing. As an example, the first BCC publication used frequencies in the kilo-hertz range [4], while more recent publications have used frequencies over 100 MHz. However, publications that use the same frequency range have reported different results and as such have developed different electrical models for the BCC channel. A big reason for this is the measurements methods. This work will put forth another model for the BCC channel that has been validated with multiple experiments and measured with a battery powered measurement system isolated from the environment.
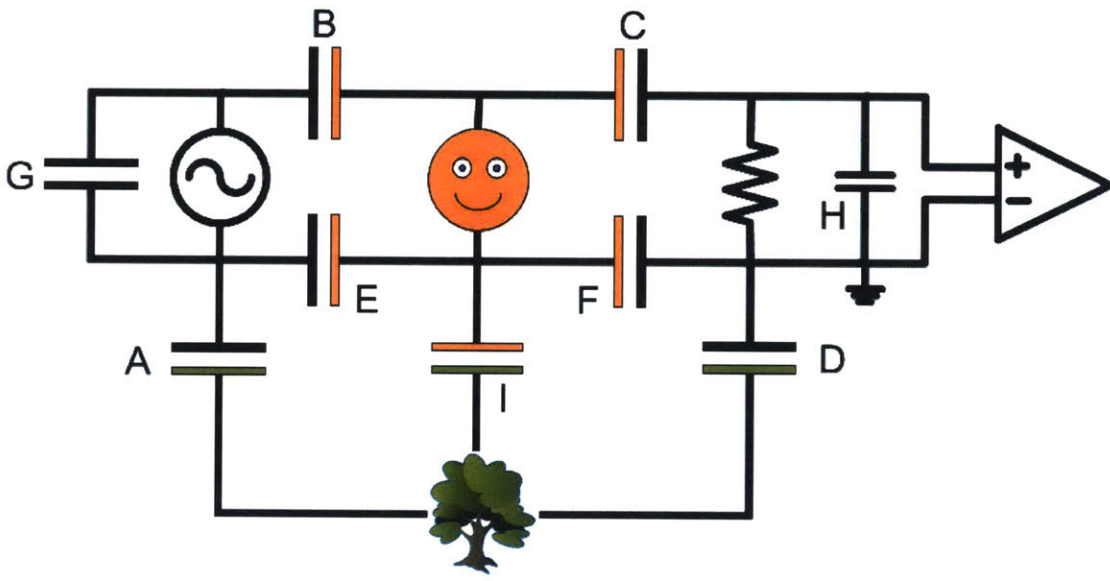
Figure 2-3: Traditional BCC circuit diagram.
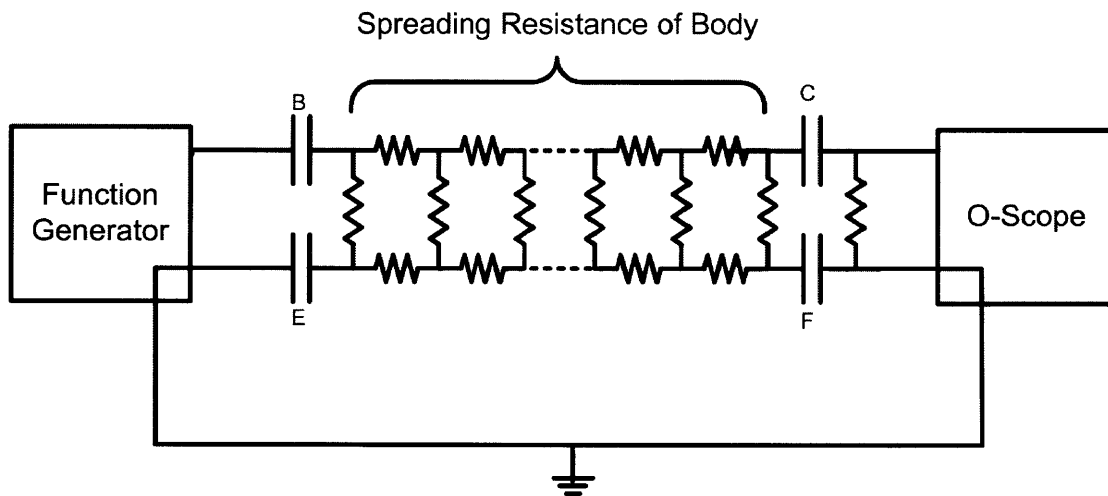
Figure 2-4: Using equipment that shares a common node will significantly change the current paths in BCC, resulting in inaccurate measurements.

2.1 Measuring BCC Channel

Discrete battery-powered signal sources and receivers are critical to measure the BCC channel. If measurement devices that are connected to an "earth ground" are used to measure the channel, such as a function generator and oscilloscope, then because these two instruments share the common "earth ground" between them, one electrode on the transmitter and one electrode on the receiver will be tied to the same voltage (see figure 2-4). Discrete BCC network devices will not share such a connection with each other so what will be measured with a transmitter and receiver that share a common reference will not remotely resemble the true BCC channel.

By shorting the nodes, current that travels through the receiver (the oscilloscope) now has an extremely low impedance path back to the transmitter (the function generator), which will result in an inflated amount of current to run through the receiver, producing measurements that will reveal the BCC channel to have more gain than it truly does. This disparity is shown in figure 2-5, which shows the difference in the channel gain when measured with an oscilloscope and a function generator, versus with the battery-powered transmitter and receiver that will be detailed in this section. Any measurement apparatus that provides a lower impedance path from transmitter to receiver than would otherwise appear, will yield less accurate measurement results. This includes using baluns or trans-
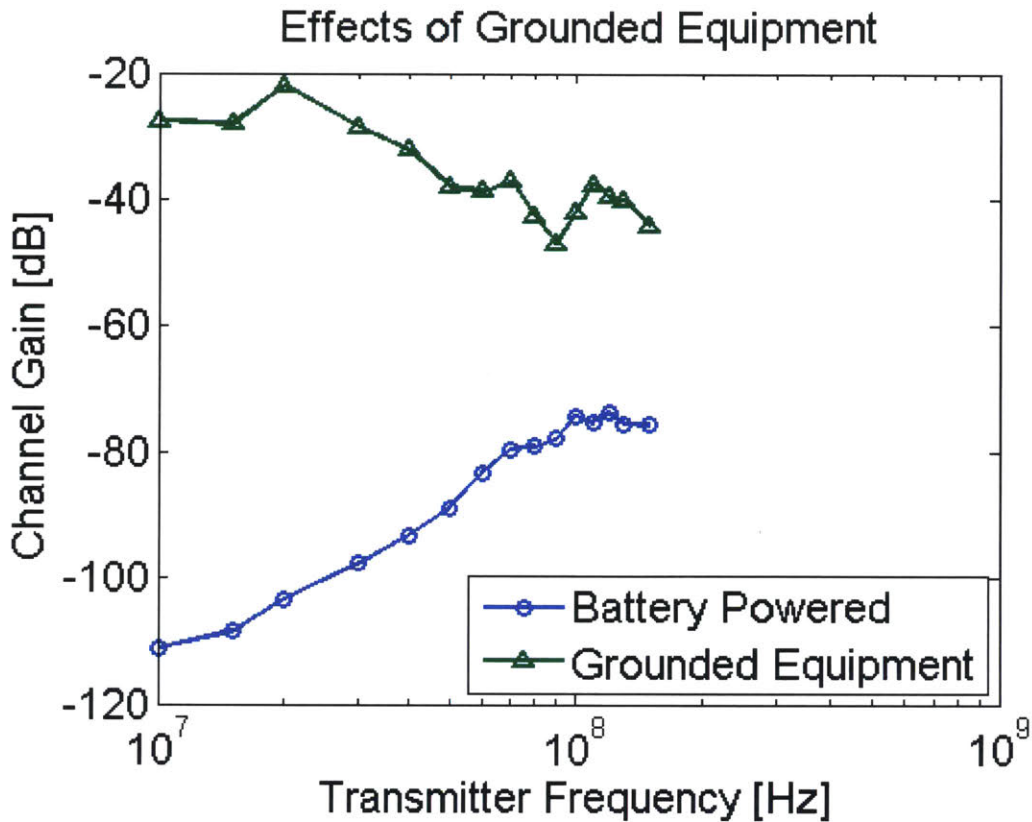
Figure 2-5: Both grounded equipment and discrete battery powered boards were used to measure the gain in the channel. The comparison of the two measurements show contrasting channel gains.

formers to isolate grounded equipment as the capacitance to the common node they provide may be significantly greater than that which appears in the natural BCC channel.

2.1.1 Channel Measurment Equipment

To make accurate measurements of the BCC channel, a discrete transmitter and receiver were fabricated with commercially available parts. These nodes are powered by battery and are not connected in any way, other than through the BCC channel. The transmitter design is shown in figure 2-6 and the receiver design is shown in figure 2-7.

The transmitter consists of an EZ430, a micro-controller radio combination that receives instructions and sets the frequency output of the AD9910 direct digital synthesizer (DDS). The output of the DDS is amplified by the LMH6552, a fully differential amplifier.
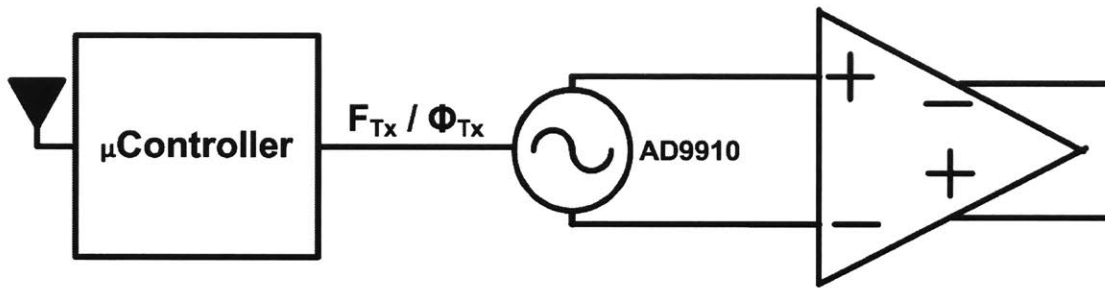
Figure 2-6: Functional schematic of the transmitter.
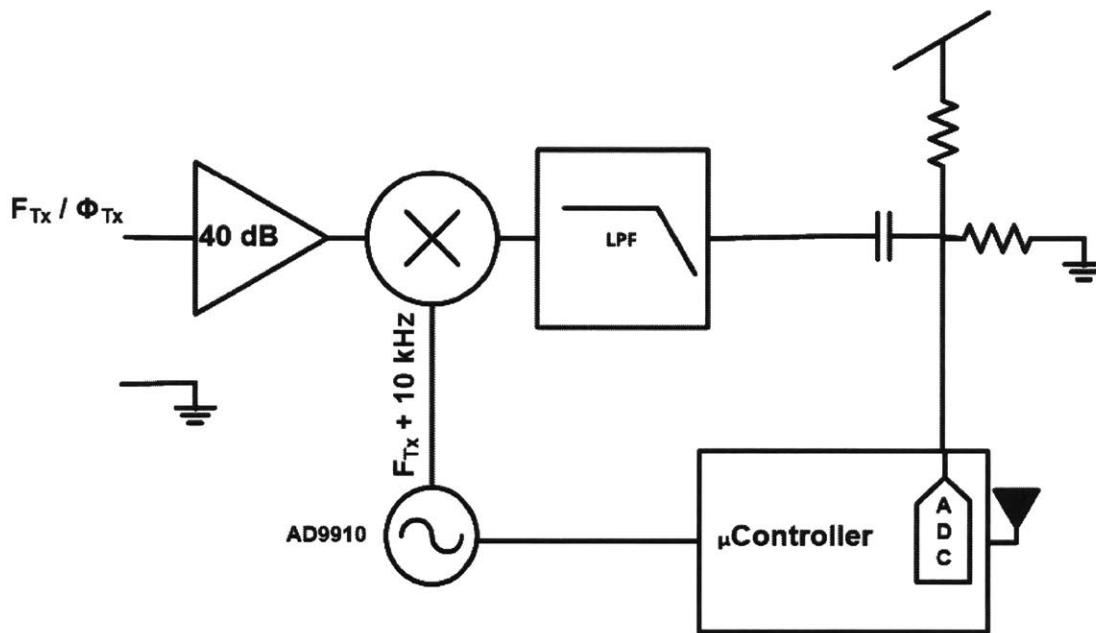
Figure 2-7: Functional schematic of the receiver.

The outputs of this amplifier are connected to the electrodes.

The receiver consists of an amplification block made up of an ADA4817 op-amp as a unity gain buffer (for body buffered return — see Chapter 3), followed by two THS4022 op-amps set for gains of 20 dB each for a total of 40 dB of initial gain. One of the receiver's electrodes is connected to the input of the amplification block. The other electrode can be connected to either the receiver's ground, or the output of the unity gain buffer. The output of the amplification block is then multiplied with a signal from the receiver's AD9910 DDS. The AD835 multiplier's output is then low-pass filtered by an LTC1563. The filtered output is then digitized with the ADC on the receiver's EZ430 micro-controller radio combination.

29

The EZ430 also sets the frequency output of the AD9910.

The receiver's DDS is set to output a sine wave that is 10 kHz higher than the frequency being measured. If the incoming signal is F_{Tx} then it will be multiplied with a sine wave with frequency F_{Tx} + 10 kHz. The output of the multiplier will be a signal with a low frequency component at 10 kHz as well as a high frequency component. After being filtered the amplitude of the 10 kHz signal will be proportional to the input amplitude of F_{Tx}. The relationship of the amplitude of the 10 kHz signal to the amplitude of F_{Tx} can be thought of as a transfer function. This relationship was measured for a range of F_{Tx} frequencies between 10 MHz-150 MHz and will be referred to as the receiver's transfer function.

To measure the frequency response of the BCC channel the transmitter is controlled using radio to output a sine wave with a frequency of F_{Tx}. The receiver is also controlled by radio to receive a sine wave of frequency F_{Tx}. The 10 kHz output of the receiver is digitized and sent off the receiver, using radio, to be analyzed. Using the transfer function of the receiver, the magnitude of the 10 kHz signal can be input-referred, revealing the amplitude of the received signal at frequency F_{Tx}, which is the same as the output signal of the channel. Measuring the output voltage of the transmitter, using a high impedance probe and oscilloscope, the amplitude of the signal to the input of the channel can be captured. The channel's magnitude frequency response can then be calculated as both the amplitude of the input and output of the channel are known. Figure 2-8 shows the full test configuration.
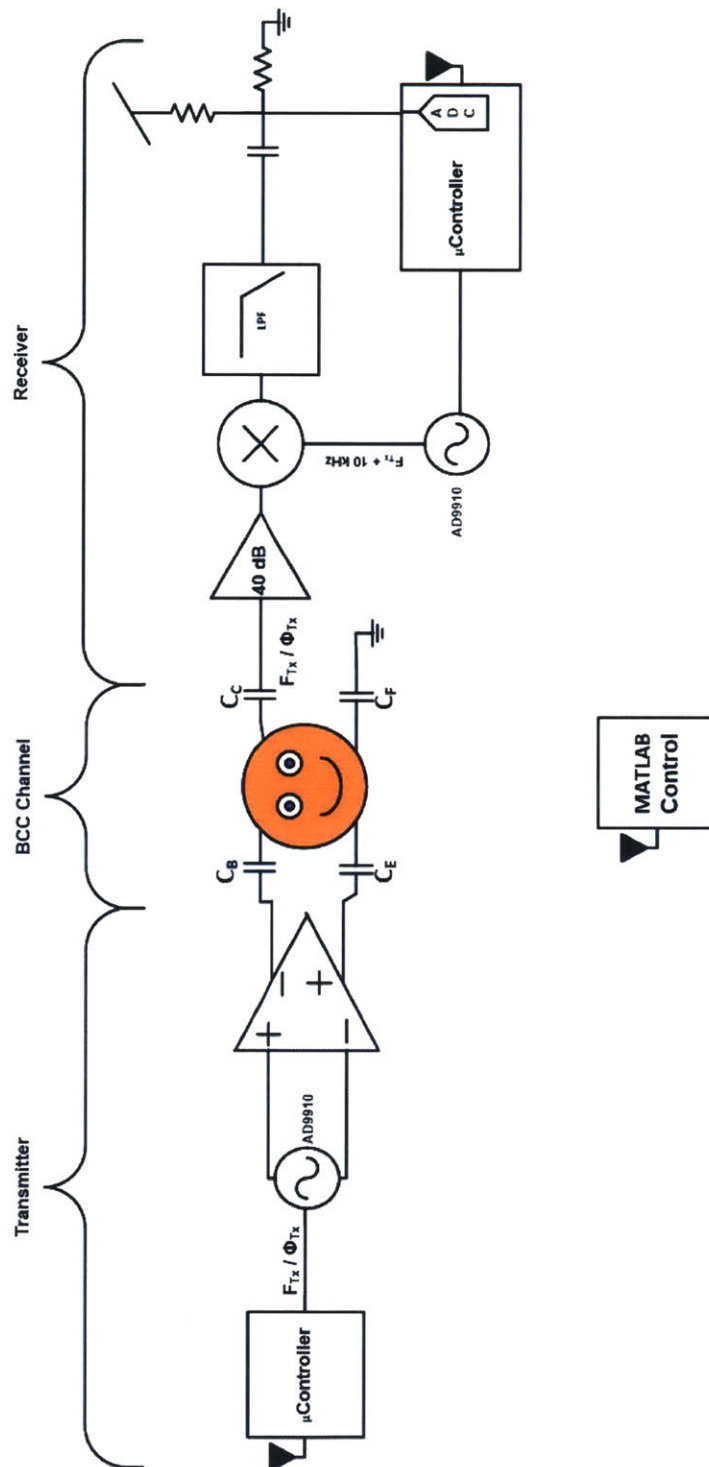
Figure 2-8: The full test configuration to measure the BCC channel. The BCC channel is measured as the output of the transmiter, and input of the receiver. The channel includes all four capacitive links.
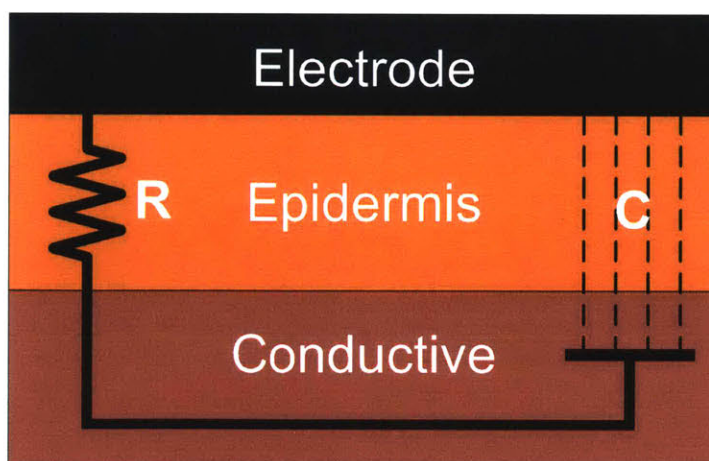
Figure 2-9: While there is a resistive element to the BCC link, the link is dominated by the capacitance at frequencies 10 MHz and above.

2.1.2   Electrodes used for Measurements

All BCC channel measurements were made using the transmitter and receiver detailed in section 2.1.1, unless otherwise specified. The electrodes used were the "3M 2560 Red Dot Electrodes". By placing them on the skin a galvanic and capacitive connection is made as modeled in Figure 2-9. The resistance through the epidermis to the conductive tissue was found to be 1.5 MΩ, while the capacitance to the conductive tissue was found to be 10 pF. The total impedance of this connection at frequencies of 10 MHz and above is dominated by the capacitance. Thus despite being attached to the body, these electrodes still make a capacitive link with the body.

The resistance and capacitance values for the electrodes were found by placing multiple electrodes on various and diverse places on a human body, such as arms, legs, torso, etc. A multimeter was used to measure the DC resistance between each pair of these electrodes, and an LCR meter was used to measure the capacitance between the two electrodes at 10 MHz. Regardless of the distance or position on the body of any pair of electrodes, their capacitive and resistive values were measured to be the same.

To be clear, the purpose of this measurement was not to rigorously characterize the electrode–body parameters. The purpose was solely to verify that using such electrodes would produce a capacitive coupling and not a galvanic coupling. It should be stated that

other electrodes and other human body combinations may have different parameters.

2.2 Return Path

There have been conflicting publications on what the dominant current path is in the BCC channel. The dominant current path is the current loop in the BCC channel that has most of the current flowing through it. Think of the loop as a forward path and return path[1]. The forward path of the dominant current path will be defined as leaving the transmitter, entering the body, then flowing into the receiver. The return path will be defined as the path the current takes in getting back to the transmitter from the receiver. Some publications [4, 6,8–10,14] have concluded that the dominant current path is through both the body and the environment, see Figure 2-10(a). While others [9, 12, 13, 19]concluded that the dominant current path is solely through the body as shown in Figure 2-10(b).

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[1]As an AC current will be sent, which designation is which is arbitrary.
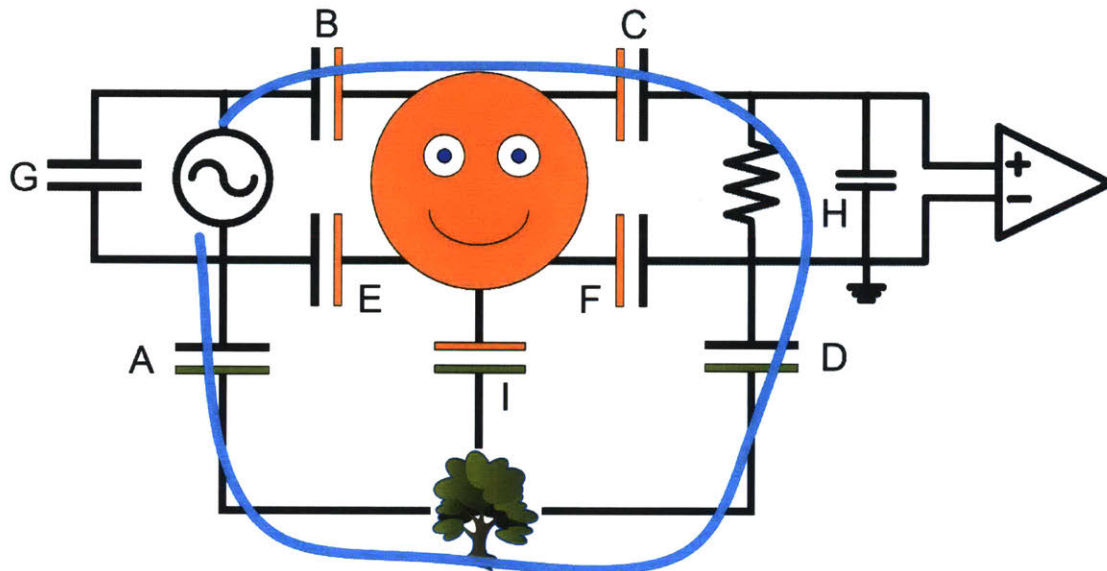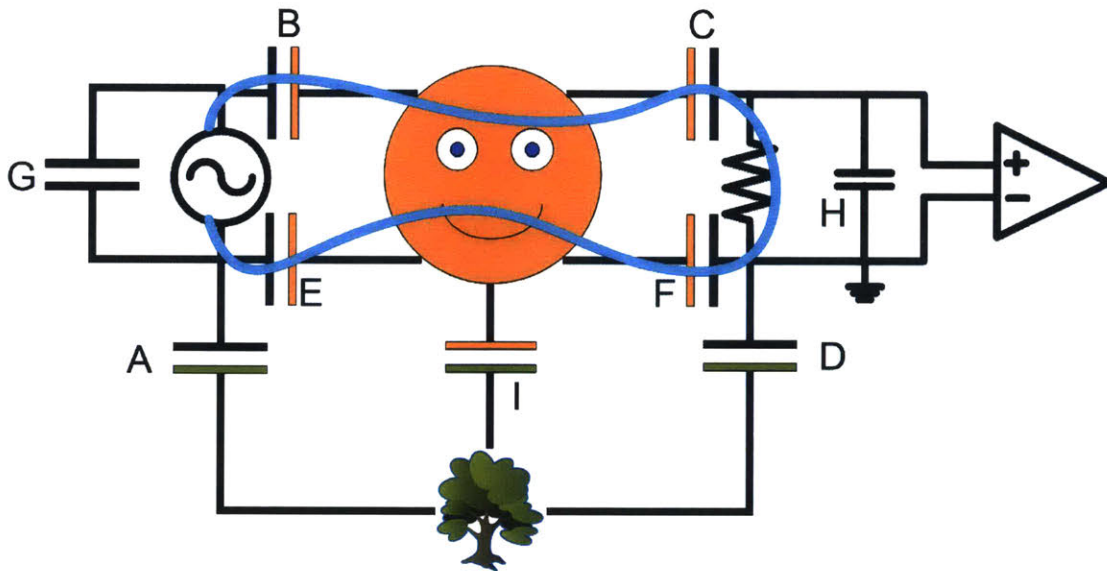
Figure 2-10: Two possibilities for the dominant current path; the dominant current path is shown with the blue loop. (a) The dominant current path as through both the body and the environment. (b) The dominant current path as solely through the body.

Knowing the return path of the channel is important because in practice the positioning of the electrodes can be engineered to enhance the dominant current path. Note that there is no difference in the circuit models in Figure 2-10(a) and 2-10(b), just the dominant path for the current. If the return path is through the environment, then the desire is to maximize the impedance of capacitors 'E' and 'F' to force the current to flow through the environment via capacitors 'A' and 'D', as capacitors 'E' and 'F' would shunt current away from the environment. If the return path is through the body then the capacitive links 'E' and 'F' are not parasitic but are part of the desired current path and as such their impedance should be minimized.

Increasing the impedance of a capacitive link between an electrode and the body is done by increasing the distance between the electrode and the body[2], or preventing the electrode from coupling with the body by shielding the electrode. This means that if the dominant current path is through the environment one electrode, from both the transmitter and receiver, should be placed as close to the body as possible, to form capacitors 'B' and 'C', while the remaining two electrodes should be placed as far away as possible from the body to minimize the impedance of capacitors 'E' and 'F'. If the dominant current path is through the body then the best implementation would be to minimize the impedance of capacitors 'B', 'C', 'E', and 'F' by attaching both electrodes on both the receiver and transmitter as close to the body as possible [12]. Figure 2-11 depicts the differences in the ideal electrode placement for the environmental return verse the body return.

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[2]If a material is used as a spacer to create the distance between the body and the electrode, the material's dielectric constant should be low to further decrease the capacitive coupling between the body and the electrode.
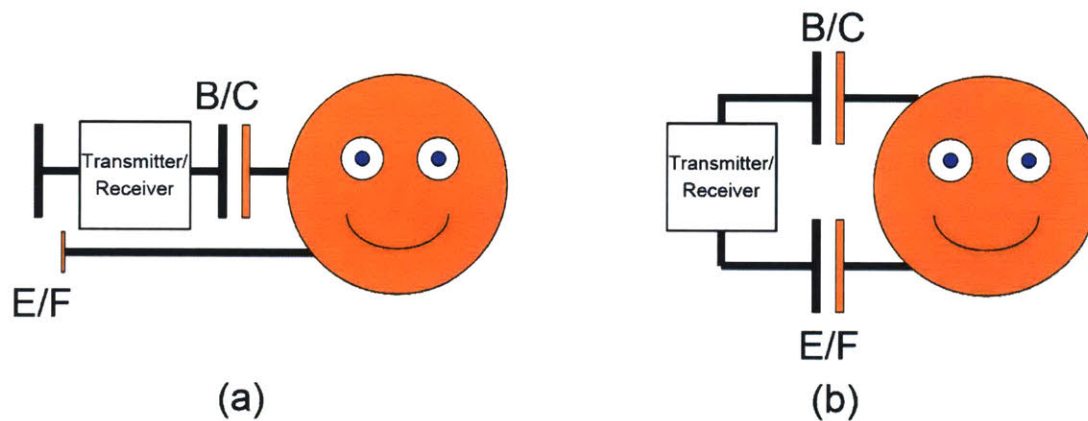
Figure 2-11: The differences in the ideal electrode placement for the environmental return verse the body return. (a) depicts how the transmitter's/receiver's electrodes should be placed if the dominant current path is through the environment: one electrode as close to the body as possible, and the other as far away as possible. While (b) depicts how the electrodes should be placed if the dominant current path is through the body: both electrodes are as close to the body as possible.

2.2.1 Measurments to Determine Dominant Current Path

To determine whether or not the dominant current path includes the environment return path an experiment was set up. In this experiment the channel measurement system described in section 2.1 was used. The transmitters electrodes were placed on the waist, while the receiver's electrodes were attached to the ankle of the right leg. Both electrodes on the transmitter were fixed in position on the body to keep capacitors 'A', 'B', 'E', and 'G' constant (refer to figures 2-1 and 2-2). One electrode on the receiver was also fixed in position on the body to keep capacitor 'C' constant. The distance to the body of the receiver's other electrode, which forms capacitor 'F', was varied using cardboard spacers. The frequency of the signal sent for the experiment was 60 MHz. The channel gain was measured as a function of the distance between the electrode and the skin, this distance being the thickness of the cardboard spacers. This test was run twice with about 10 minutes in between test runs. The results of these measurements, as seen in figure 2-12 are normalized such that the channel gain when the electrode is attached directly to the body has a gain of '1' or 0 dB.

However, the slope of the relationship isn't strictly decreasing, there is a point of inflection where the relationship does increase, though the increase is modest. To simulate what the electrode's capacitance would be at an infinite distance away from the body, that electrode was disconnected from the receiver. The channel gain was measured at this configuration and is the horizontal line beneath each respective curve in figure 2-12. This shows that at some distance away from the body the gain channel gain would again decrease.
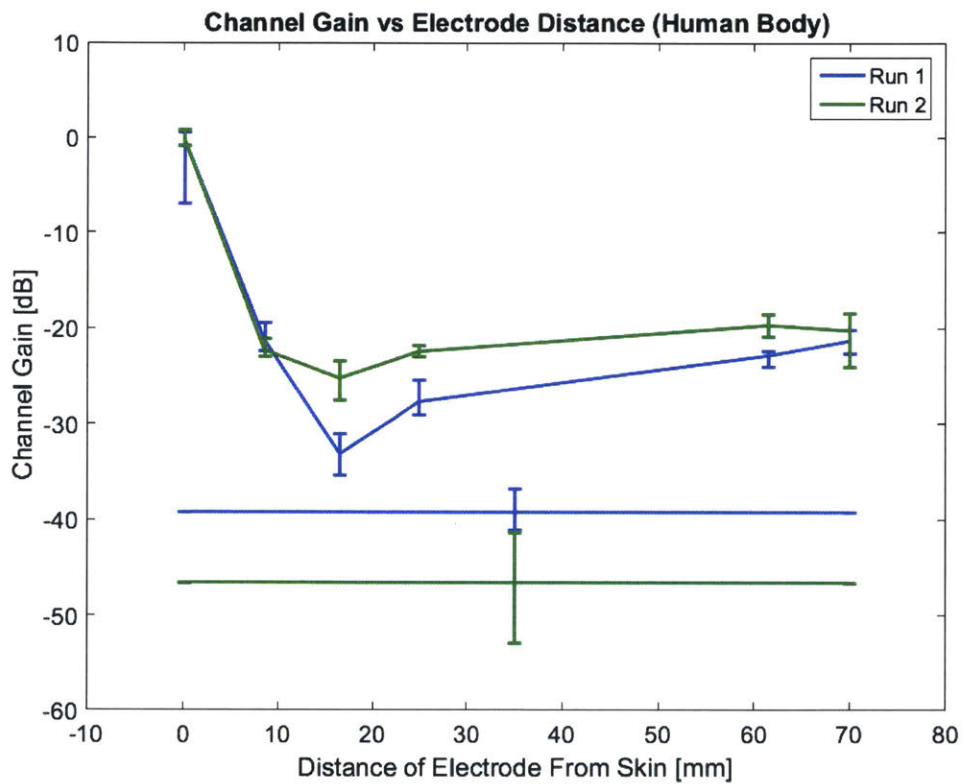
Figure 2-12: The channel gain as a function of the distance between an electrode and the body; normalized when the electrode is attached directly to the body. The bottom horizontal lines are the channel gain when the electrode was disconnected from the receiver.

The reason for this inflection is not well understood. Perhaps there is something in the environment that the electrode starts to couple to, as it moves away from the body, that provides the increase in channel gain. To model this idea the circuit in figure 2-13 was simulated with the two variable capacitors C_{Var1} and C_{Var2}. C_{Var1} represents the capacitive link of an electrode to the body, and C_{Var2} represents the capacitive link between the same electrode to the environment. As the electrode moves away from the body it will get closer to the environment. Thus the value of C_{Var1} decreases as the distance increases and the value of C_{Var2} increases as the electrodes moves away from the body.
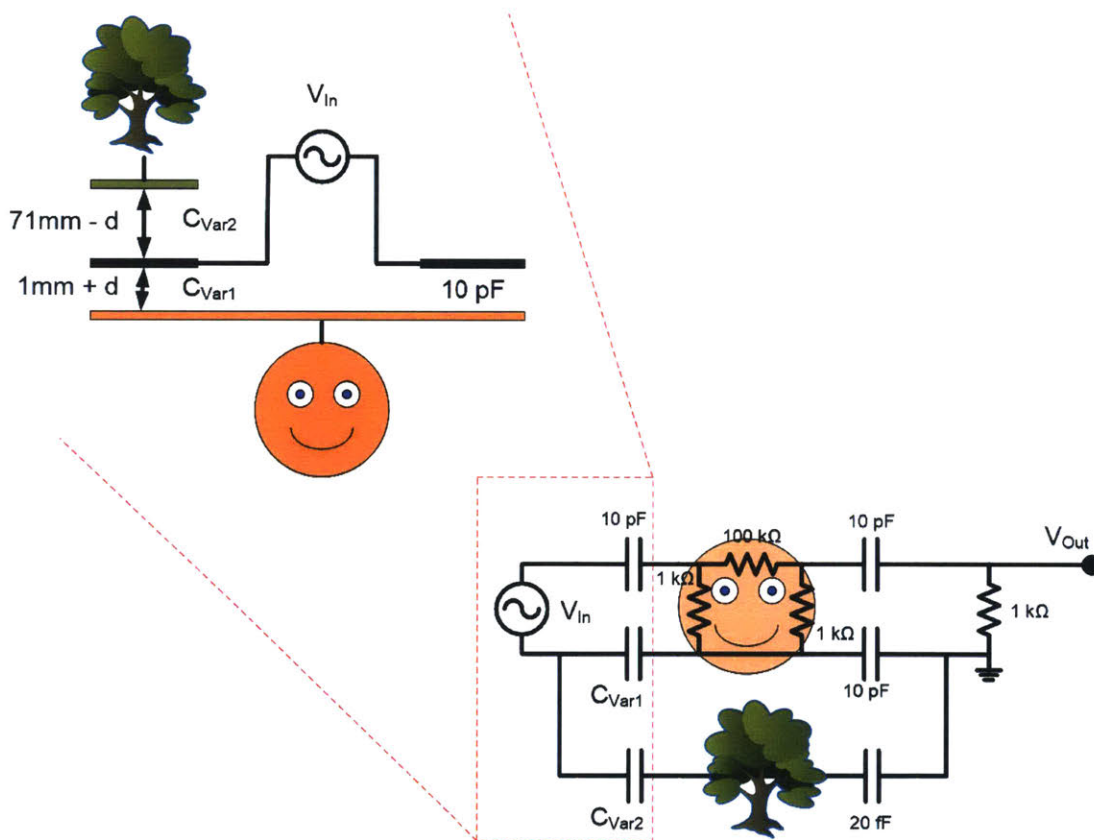
Figure 2-13: A circuit model to give a possible explanation of the inflection in figure 2-12. The voltage source, V_{In}, models the transmitter, the capacitors attached to the transmitter represent the capacitive links made by the electrodes and body, and one of the electrodes and environment (see figure 2-10), the three resistors (making the pi-network) model some fixed attenuation due to the body, while the resistor between V_{Out} and ground model the input resistance of the receiver.

40

Mathematically the two variable capacitors were modeled as:

$$C_{Var1} = \frac{A_1 * \epsilon_0}{d + 1\,\text{mm}}$$

$$C_{Var2} = \frac{A_2 * \epsilon_0}{71\,\text{mm} - d}$$

where d is the distance in millimeters the electrode is away from the body. C_{Var1} was set to be 10 pF, when d was set to 0 mm, and C_{Var2} was set to be 2 pF when d was set to be 70 mm. The variable d was swept from 0 mm – 70 mm. The simulated gain, from V_{In} to V_{Out}, as a function of the distance between the electrode and the body is shown in figure 2-14 and shows an inflection in the channel gain, similar to that in figure 2-12. This simulation shows that indeed the inflection could be due to the electrode coupling to something in the environment. Note that this simulation is only meant to show that the channel gain can have a point of inflection as the electrode moves away from the body. The specific values and trends of the channel gain curve are greatly dependent on the other values of the circuit elements. The simulation is only meant to show that the inflection in the gain from figure 2-12 **could** be attributed to the electrode starting to couple to something in the environment more strongly as it moves away from the body.
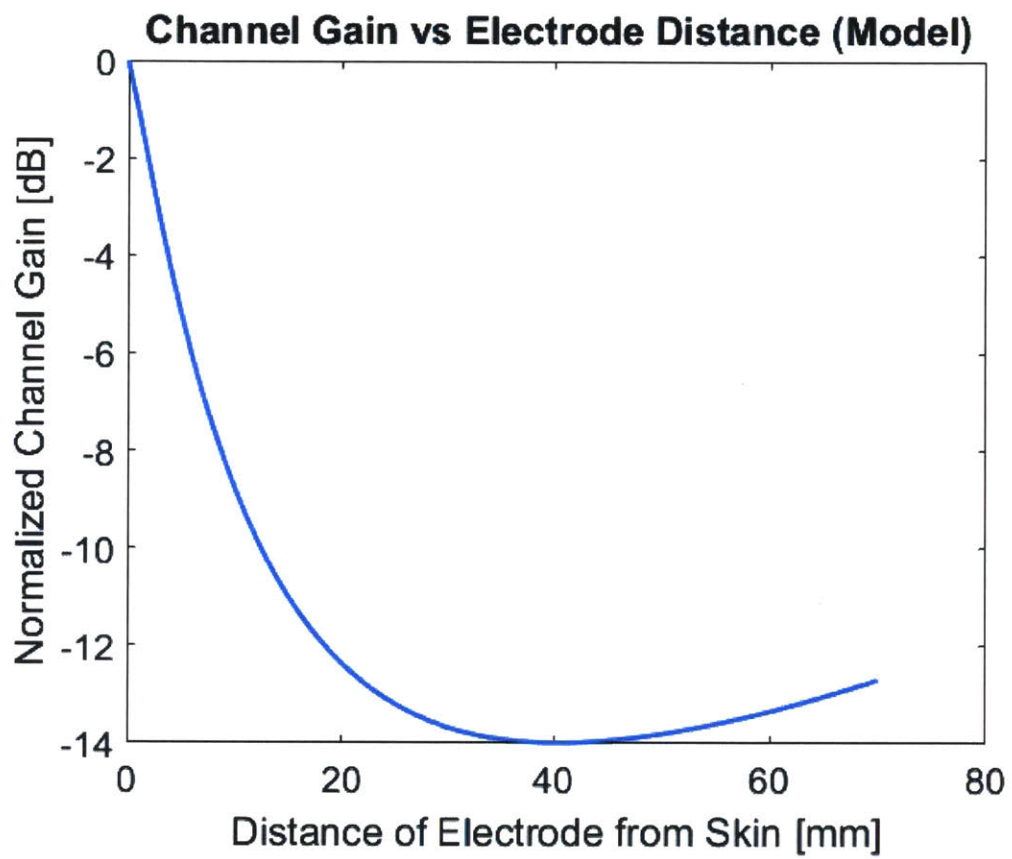
Figure 2-14: Simulated results from the circuit diagrammed in figure 2-13.

Figure 2-13 models the electrode coupling to something conductive in the environment as the distance between the electrode and the body gets bigger. However, it could also be that as the electrode moves away from the body fringe capacitance between the electrode and the body develops on areas of the body that are closer to the receiver's electrodes (see figure 2-15). The change of where fringe capacitance is coupling to on the body would be modeled by the electrode coupling to something with a lower impedance path to the receiver's electrodes as the distance between the body and the electrode increases. If the impedance of the lower impedance path to the receiver's electrodes was set to zero, then this model would reduce to that shown in figure 2-14, and thus would yield the same results as seen in figure 2-14.

(a)

(b)
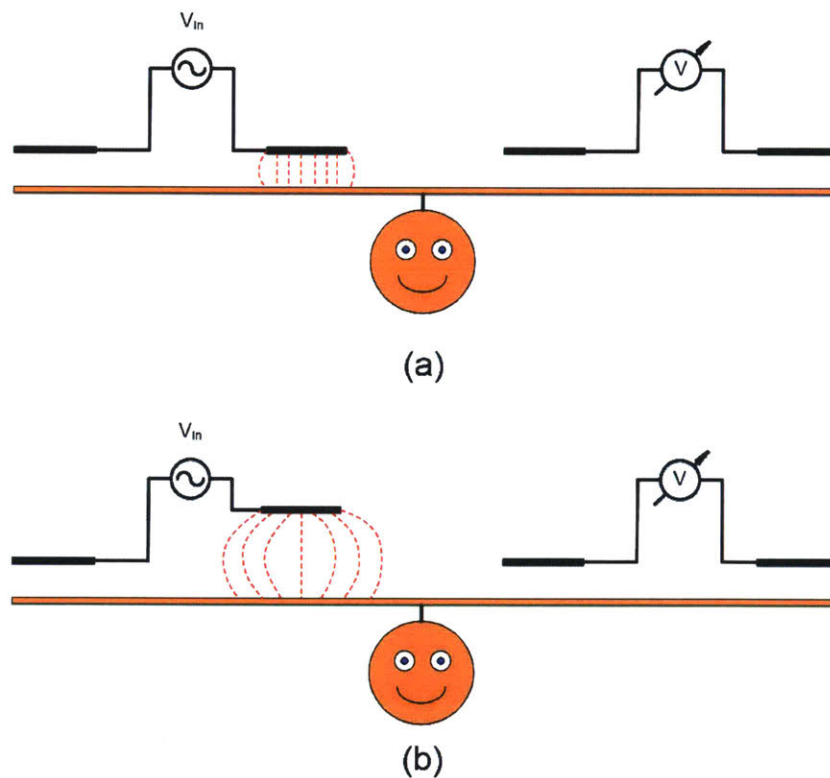
Figure 2-15: On the left, of both (a) and (b), is a transmitter using two electrodes to couple to the body. A receiver is coupling to the same body with electrodes some distance away. (a) Both of the transmitter's electrodes are close to the body. (b) By moving an electrode farther away from the body, the fringe capacitance made by this electrode couples to areas on the body that are closer to the receiver's electrodes.

To ensure that the inflection wasn't a source of experimental setup a similar experiment was performed. This time instead of doing the testing on a human body, the measurement was performed on a pork loin, and instead of cardboard spacers which can become conductive when wet, plexiglass was used to control the distance. The results of the pork loin measurement were similar to the human body measurement and are shown in figure 2-16.
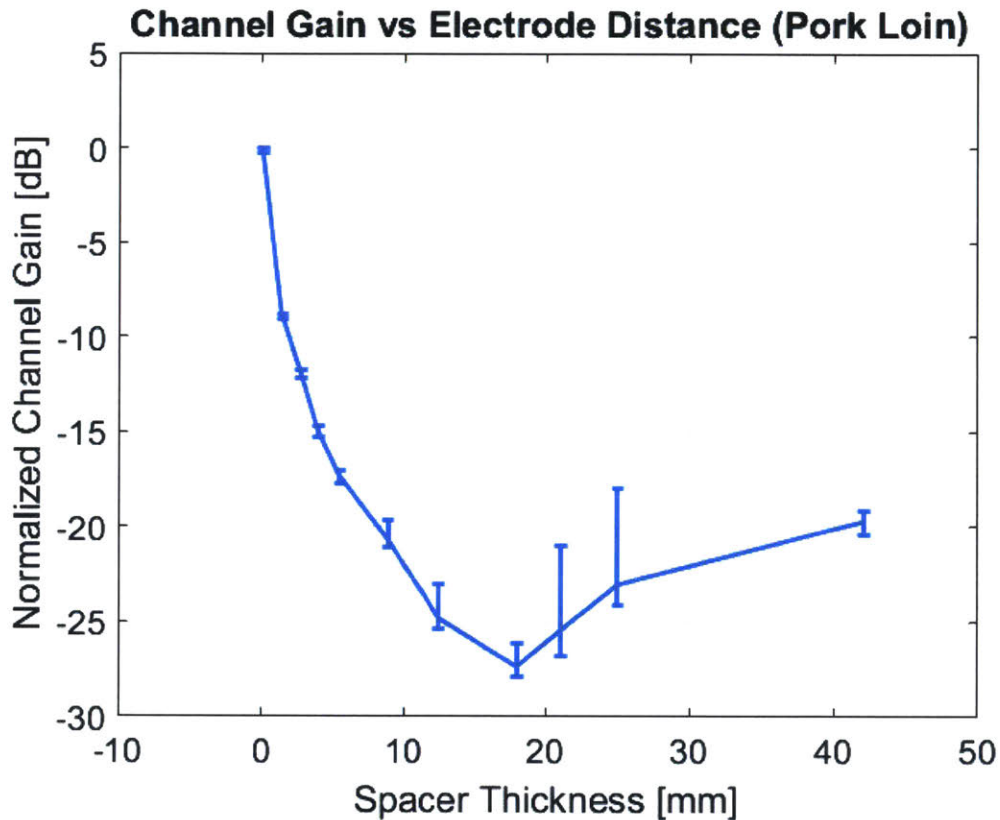
Figure 2-16: The channel gain as a function of the distance between an electrode and the pork loin; normalized when the electrode is attached directly to the pork loin.

These measurements show that as the electrode was moved farther away from the body/pork loin there was a decrease in channel gain. This means that it is better to have all the electrodes close to the body, and that the dominant return path is through the body. This is good for practical applications as it would be hard to shield and minimize the capacitive link of one of the electrodes with the body. This fact also will allow for implants inside the body to communicate with devices that are outside the body, as will be shown in section 2.4.1.

2.3 Body Model

Because the dominant current path in BCC is through the body it is important to have a model for and understand how the body's conductive tissues behave electrically. Many of the BCC papers that have thought the dominant current path is through the environment, have used electrical models for the body that aren't compatible with the dominant current path through the body. Some of the most extensive work on modeling the electrical characteristics of human tissue is found in [18]. Before that work will be discussed and expanded upon, the theory of how electric potentials flow through the conductive tissues of the body will be reviewed.

2.3.1 The Physical Theory

The basics of how signals can be sent through the conductive tissues of the body can be explained through a simplified example [3].

Consider an infinite medium with a uniform conductivity σ. Now cut this medium in half and disregard one of the halves. The medium now spans infinity in five directions, but is bounded in the sixth direction by the cut surface. Now add hemispherical conductive electrodes E_1 and E_2, each with a radius 'a', into the medium such that the flat side of the hemisphere aligns with the surface of the medium, as seen in figure 2-17. When a voltage 'V' is applied between these electrodes a current 'I' will flow. The goal is to find the voltage, V_p, at any point in the medium due to the voltage between the electrodes. The use of super position will be used to calculate the voltage V_P.

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[3]A similar example, emphasizing different details, can be found in [20]

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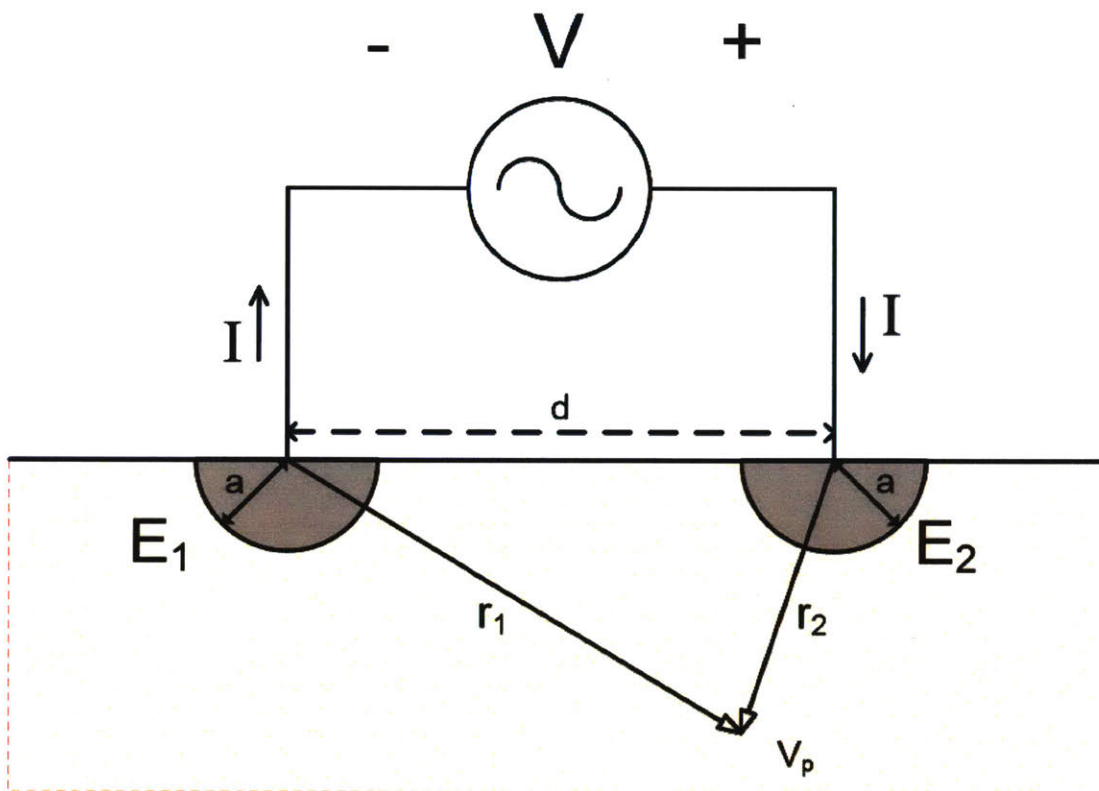
Figure 2-17: A cross section of hemispherical electrodes placed into a medium. The medium is infinite along five directions, and bounded by an infinite plane on the sixth.

Consider one of the hemispherical electrodes in the medium with a current 'I' being injected into the medium from the electrode as seen in figure 2-18.
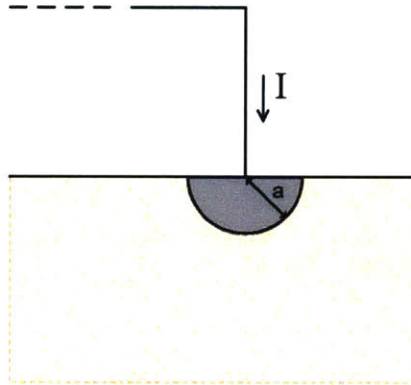
Figure 2-18: Hemispherical electrode placed into an infinite medium.

The reference electrode for both electrodes will be placed at infinity within the medium. Having the reference at infinity will force the current to disperse uniformly[4] throughout the medium as shown in figure 2-19. Thus the current density at any point in the medium due to the injected current is:

$$J = \frac{I}{2\pi r^2} = \sigma \vec{E} \tag{2.1}$$

where 'r' is the distance from the center of the electrode to the point 'P' (where the current density is being measured), $\vec{E}$ is the electric field at 'P', and σ is the conductivity of the medium.

By rearranging equation 2.1 the relationship between the electric field and the current is:

$$\vec{E} = \frac{I}{2\pi r^2 \sigma} = \frac{I\rho}{2\pi r^2} \tag{2.2}$$

The change in voltage from the electrode to point 'P', due to the current flowing from the electrode, can be found by integrating the electric field along the path from from the electrode to point 'P' (see figure 2-20).

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[4]This is also assuming that the effects of the second electrode on the current dispersion is negligible.
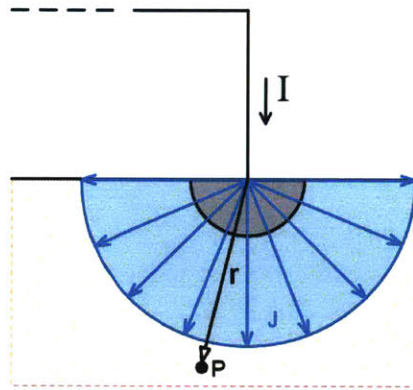
Figure 2-19: The current injected into the medium will produce a uniform current density.

$$\Delta V = -\int_s \vec{E} \, ds = -\int_a^r \vec{E} \, dr = \frac{I\rho}{2\pi} \left[\frac{1}{r} - \frac{1}{a} \right] \qquad (2.3)$$
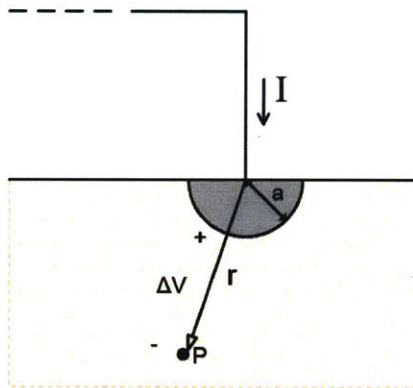
Figure 2-20: The voltage difference between the electrode and the point 'P'.

This is the voltage for injecting current from an electrode into the body. To find the voltage due to an electrode extracting current from the body, the polarity of the current must be changed, such that:

$$\Delta V' = -\frac{I\rho}{2\pi} \left[\frac{1}{r} - \frac{1}{a} \right] \qquad (2.4)$$

where $\Delta V'$ is the voltage at point 'P' due to an electrode drawing current from the body.

The solution to the goal, which is to find the voltage V_p at any point in the medium — as diagrammed in figure 2-17, is simply the super position of the voltages ΔV and $\Delta V'$. Following from the fact that E_2 will inject current 'I' into the medium, and E_1 will extract

that same current. Thus the equation for the voltage at any point in the medium is:

$$V_P = \Delta V + \Delta V' = \frac{I\rho}{2\pi}\left[\frac{1}{r_2} - \frac{1}{r_1}\right] \tag{2.5}$$

where r_2 is the distance from E_2 to the point 'P', r_1 is the distance from E_1 to the point 'P', and V_p is the voltage at point 'P'.

While equation 2.5 provides the relationship between the voltage at point 'P' and the current, it is more useful to have the relationship of V_p as a function of the voltage between the two electrodes. To do this, we will use the boundary conditions at each electrode. It also needs to be stated that in our super position analysis from above, the voltage at E_1 must be equal and opposite to the voltage at E_2 to have the same current injected into the medium as the current extracted from the medium. Thus the two boundary condition equations are:

$$V_{E_2} = \frac{I\rho}{2\pi}\left[\frac{1}{a} - \frac{1}{d-a}\right] \tag{2.6}$$

$$V_{E_1} = -V_{E_2} = \frac{I\rho}{2\pi}\left[\frac{1}{d-a} - \frac{1}{a}\right] \tag{2.7}$$

where d is the distance between the electrodes as seen in figure 2-17.

The voltage difference between the electrodes is $V = V_{E_2} - V_{E_1}$. And thus:

$$I = \frac{V\pi}{\rho\left(\frac{1}{a} - \frac{1}{d-a}\right)} \tag{2.8}$$

By plugging equation 2.8 into equation 2.5, it follows that the voltage at any point in the medium is:

$$V_P = \frac{V}{2\left(\frac{1}{a} - \frac{1}{d-a}\right)}\left[\frac{1}{r_2} - \frac{1}{r_1}\right] \tag{2.9}$$

where V is the voltage between the electrodes.

Equation 2.9 gives the relationship of the voltage at any point in the medium with respect to the the geometry/placement of two electrodes and the voltage between the electrodes. Now consider figure 2-21 that depicts an aerial view from above the medium's sur-
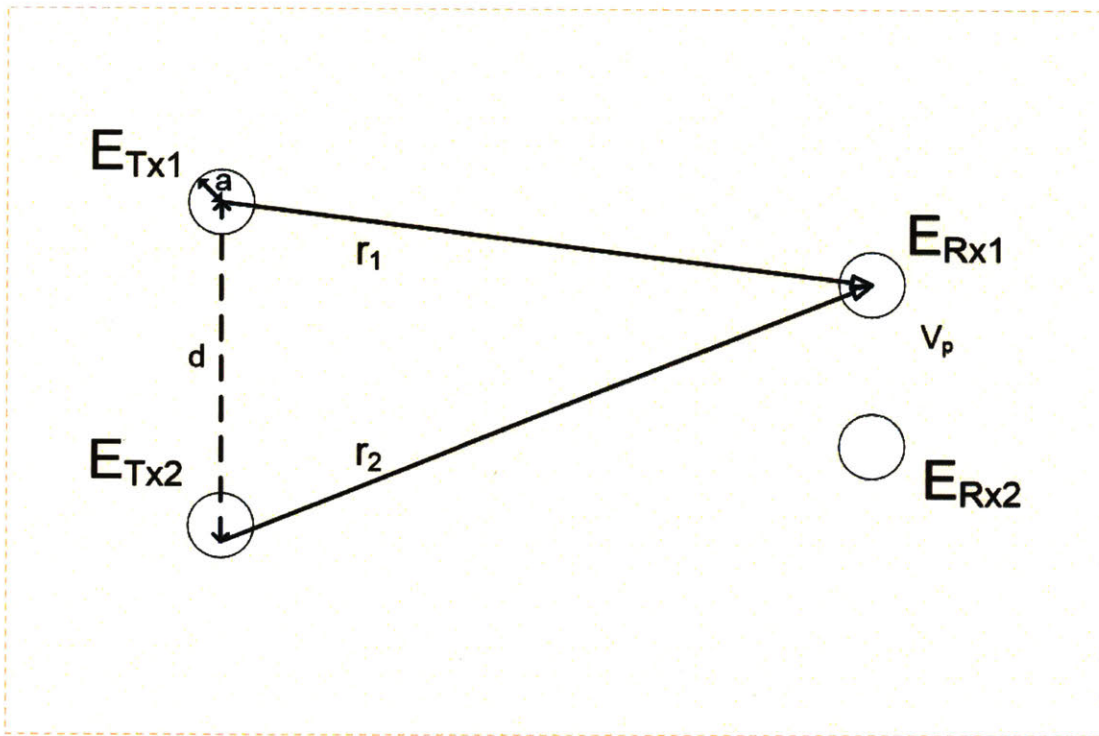
Figure 2-21: An aerial view of four Hemispherical electrodes placed on the medium's surface.

face, looking down at the surface. Two transmitting electrodes, E_{Tx1} and E_{Tx2}, are placed on the surface of the medium. Some distance away from the transmitting electrodes, two receiving electrodes E_{Rx1} and E_{Rx2} are placed on the same surface. If a voltage is applied between E_{Tx1} and E_{Tx2}, then the voltage difference measured between E_{Rx1} and E_{Rx2} can be solved using equation 2.9. The voltage will be a scaled voltage of the input voltage between E_{Tx1} and E_{Tx2}. The scaling factor is a function of the electrodes placement. Thus as long as the positions of the electrodes stay constant, then there is a linear relationship between the transmitting electrodes and the receiving electrodes, allowing signals to be sent across the medium.

This exercise has shown how a voltage generated by two electrodes in one area of the medium will produce a scaled voltage that can be measured between two electrodes in another area of the medium. This medium is analogous to the conductive tissues in the human body, with the surface of the medium being the epidermis. While the human body

is a more complex shape[5], and as such will morph the boundary conditions and affect the details of how voltages will travel through the body, this basic model shows how a potential created in one area of the body, will be able to be measured at another area of the body. It is this fact, that a potential created in one area of the body - can be measured at another area, that allows BCC to work without having current flow through the environment. This exercise also shows how the position of electrodes can affect the channel gain (for more detailed experiments on the effects of electrode placement see [16]).

[5]Obviously not infinite.

2.3.2 Spreading Resistance

Applying finite element approach to the conductive tissues, we can imagine the tissue as a lattice network of impedances, such as that shown in Figure 2-22. In [17] it is shown that at frequencies between 10 kHz and 10 MHz each impedance block can be electrically modeled with the circuit found in Figure 2-23 [18]. The capacitance in the impedance models the cell membranes within the tissue, while the resistors model the resistance of the extra-cellular and intra-cellular fluid in the tissue. At some frequency the capacitive impedance of the cell membrane will become negligible, leaving only the pure resistances to impeded an electrical signal [19]. At that frequency and higher frequencies the conductive tissue of the body will act as a spreading resistance. Replacing the body 'element' in Figure 2-2 with a spreading resistnace, yields the circuit in Figure 2-24.
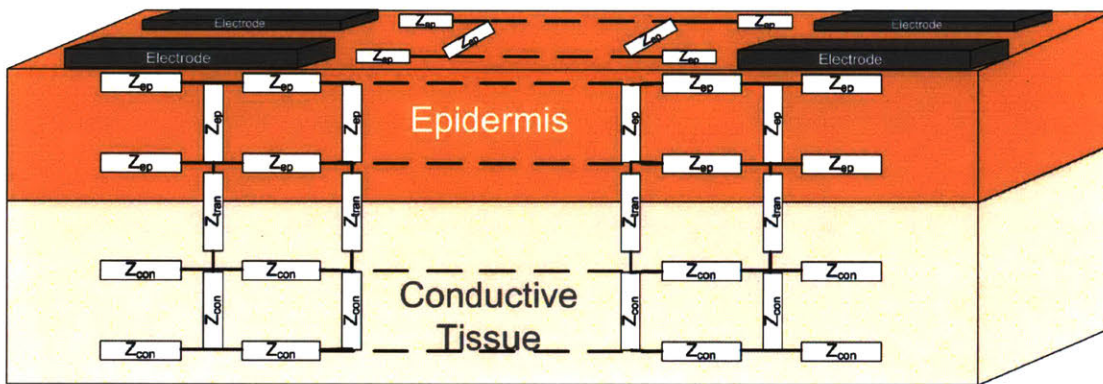
Figure 2-22: The body can be modeled as a lattice work of impedances. Different types of tissues will have different impedances and there will be transition impedances between different tissues.

Modeling the body purely as a spreading resistance at frequencies in the range of 10 MHz – 150 MHz will be validated in section 2.4. This model also allows for the dominant current path to be through the body, and is the finite element analysis model of the physical model discussed in section 2.3.1.
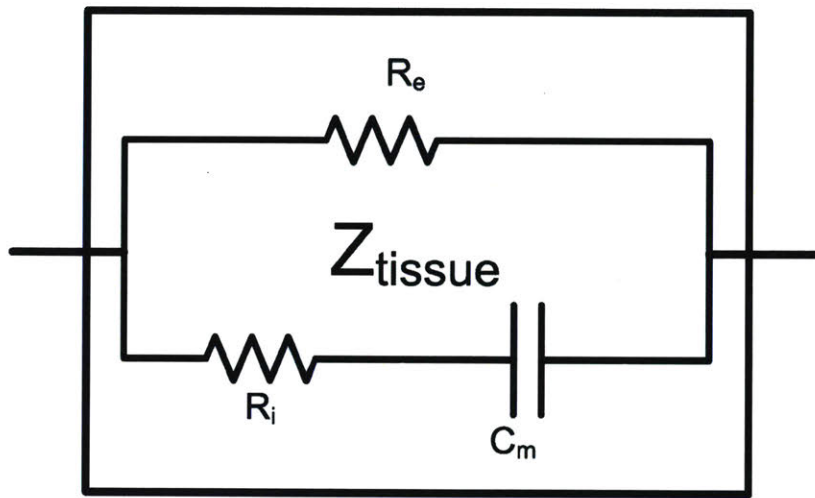
Figure 2-23: The detailed model of the impedances in Figure 2-22.
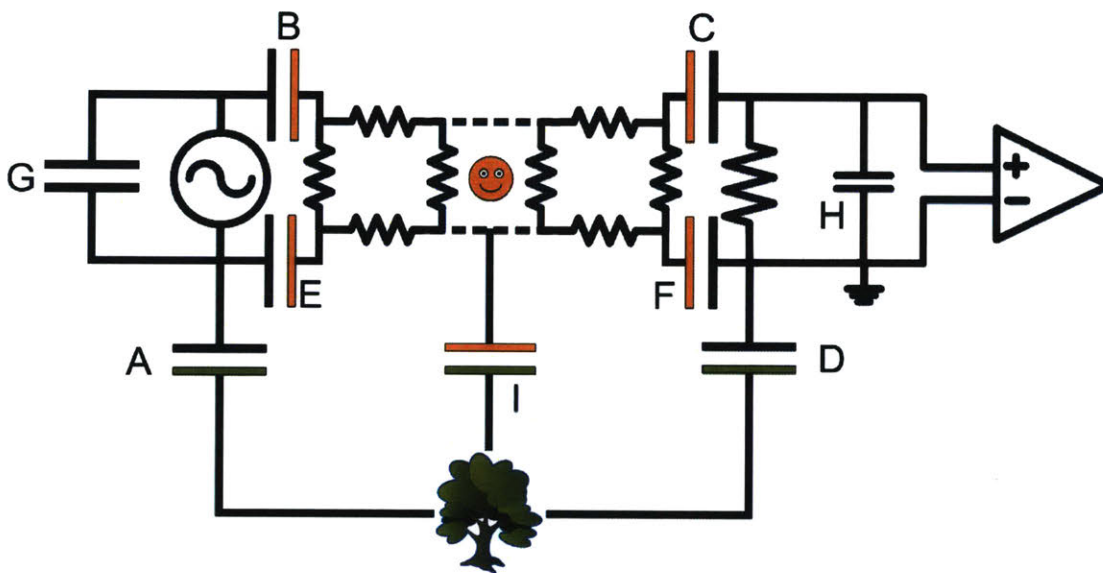
Figure 2-24: The circuit model for the BCC channel, with the body modeled as a spreading resistance. Validated for frequencies from 10 MHz – 150 MHz.
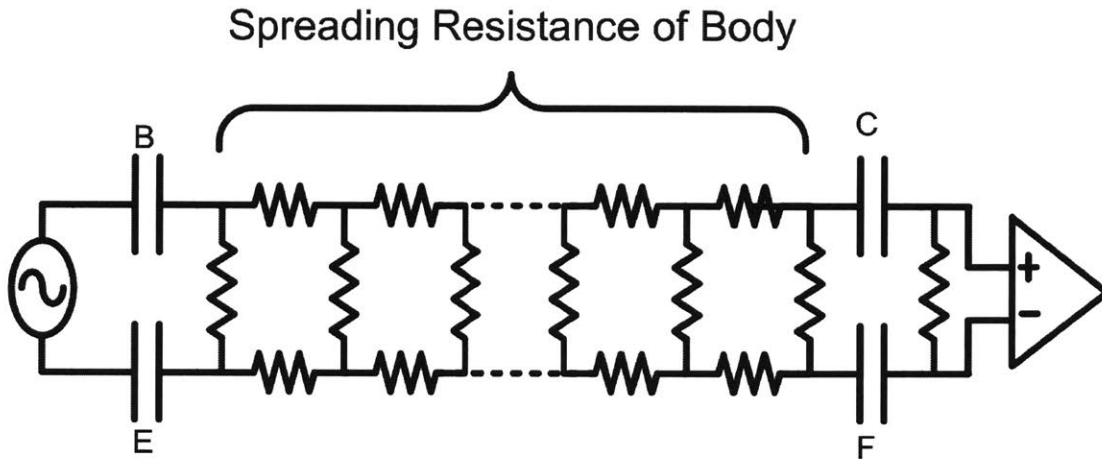
Figure 2-25: The proposed BCC channel model. The body is modeled as a spreading resistance. This model is valid from 10 MHz - 150 MHz

2.4 Proposed BCC Channel Model

Section 2.2.1 showed that the dominant current path for BCC is through the body, and that little current is transmitted through the environment. Because little current flows through the environment, the environment, and the capacitive links to it, may be abstracted away and removed from the model in Figure 2-24. Further, by shielding the electrodes or engineering their placement, capacitors 'G' and 'H' can be minimized and abstracted away. The resulting simplified BCC model is found in Figure 2-25. This is the proposed BCC channel model.

The BCC channel gain will be defined as the transfer function from the output of the transmitter, to the input of the receiver. This definition includes the capacitive links as part of the channel. The proposed model shows that the BCC channel can be characterized as two high-pass filters. One formed by the capacitive links from the transmitter and the spreading resistance of the body, the second by the receiver's capacitive links and the receiver's input resistance. The corner frequencies of the filters are dependent upon the capacitance of the links, the resistivity of the body, and the input resistance of the receiver.

This model predicts that if the input resistance of the receiver is increased, then the mid-band gain would increase, and the associated corner frequency would move to a lower frequency. To validate this model the testing equipment from section 2.1 was used. To

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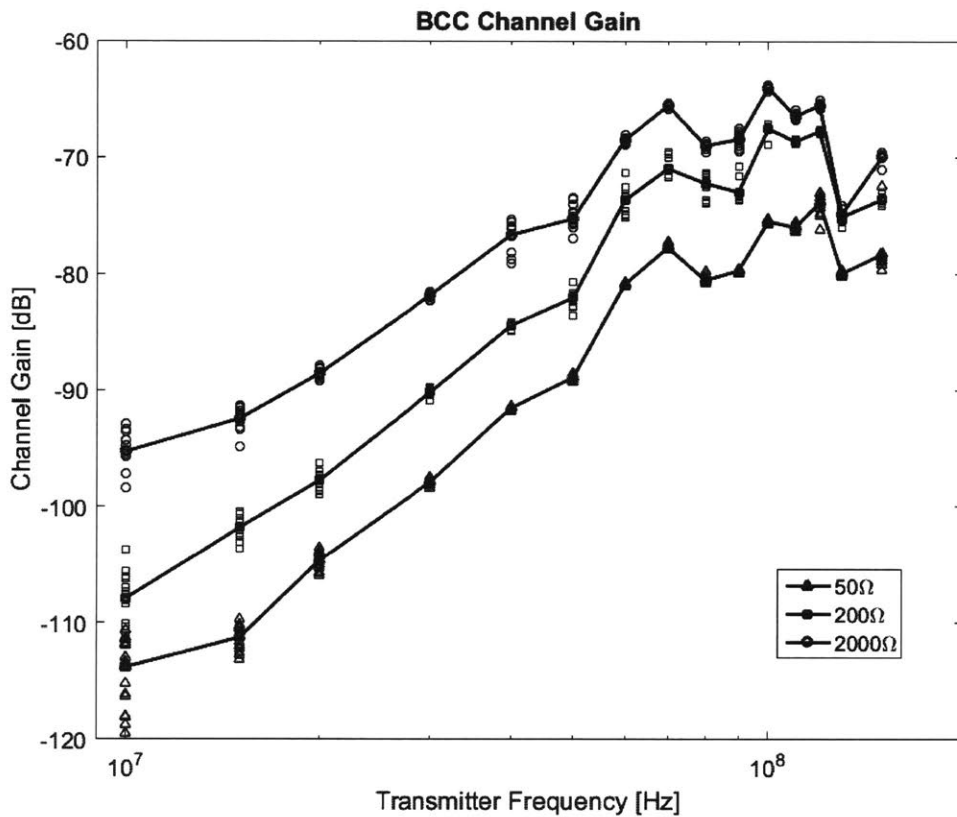
Figure 2-26: BCC channel measurements with the input resistance to the receiver varied.

measure the BCC's channel gain the transmitter was placed on the head with one electrode on the forehead and the other on the mastoid behind the ear. The receiver was placed on the waist with the electrodes attached near the belt line. The frequency was swept over the 10 MHz-150 MHz range [6]. Three different resistance values were tested for the input resistance of the receiver: 50 Ω, 200 Ω, and 2,000 Ω. The results of this experiment are shown in figure 2-26.

Notice that with a 50 Ω input resistance there is about a 40 dB/dec increase in channel gain between 10 and 100 MHz due the channel acting like two high-pass filters. The slope decreases with the increase in resistance, which suggests that the corner frequency of one of the high-pass filters is moving to a lower frequency. In addition, an increase in the input resistance results in an increase in the flat-band gain. Both results are predicted by the

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[6]The frequency band of interest for BCC is 10 MHz - 150 MHz. The lower frequency is set by the desire for high data rates, while the high frequency is limited by the body acting as an antenna for the signal [8].

proposed model, strengthening the validity of the proposed BCC channel model.

2.4.1 Implantable Channel

Further validation of the proposed channel comes from the fact that implants can work with body coupled communication. In other models of the BCC channel, specifically those that hypothesis that the dominant current path is through the environment, implants would not be able to use the BCC channel because they can not make a capacitive link with the environment that wouldn't be shorted by a link with the body. This has lead to proposals of using a combination of radio and BCC for BANs that include implants [11]. But every day the BCC channel is used to detect electrical signals from implanted electrical 'devices'. Think of the heart, or the brain, as an implant that creates a voltage between two points inside the body. These potential differences can be measured outside the body by placing electrodes on the body; these received signals are called ECG and EEG respectively. In essence, recording ECG is body coupled communication: the monitor is the receiver of the signals sent by the heart. Further, it has been shown in [21] that the electrodes don't have to be directly over the heart to measure the potential difference of the heart. The electrodes can be placed near the ear and still measure the potential difference made by the heart. This shows that implants in one area of the body can transmit information to a receiver that is outside, and on a different area of, the body.

The proposed channel model was validated experimentally by simulating an implanted channel using a pork loin. First, both the transmitter's and receiver's (detailed in section 2.1) 3M electrodes were connected to the pork loin taking care to ensure that both the transmitter and receiver would be capacitively coupled to the conductive tissue in the pork loin. In this configuration (see figure 2-27(a)) the purposed body model predicts that there will be two high-pass filters with the channel gain exhibiting a 40 dB/dec slope. Next the transmitter's output was connected to two alligator clips that were inserted into the pork loin, while the receiver was still capacitively coupled as before. This configuration (see figure 2-27(b)) simulates an implanted transmitter in the pork loin that is connected to the BCC channel galvanically. The proposed body model would predict that the channel would
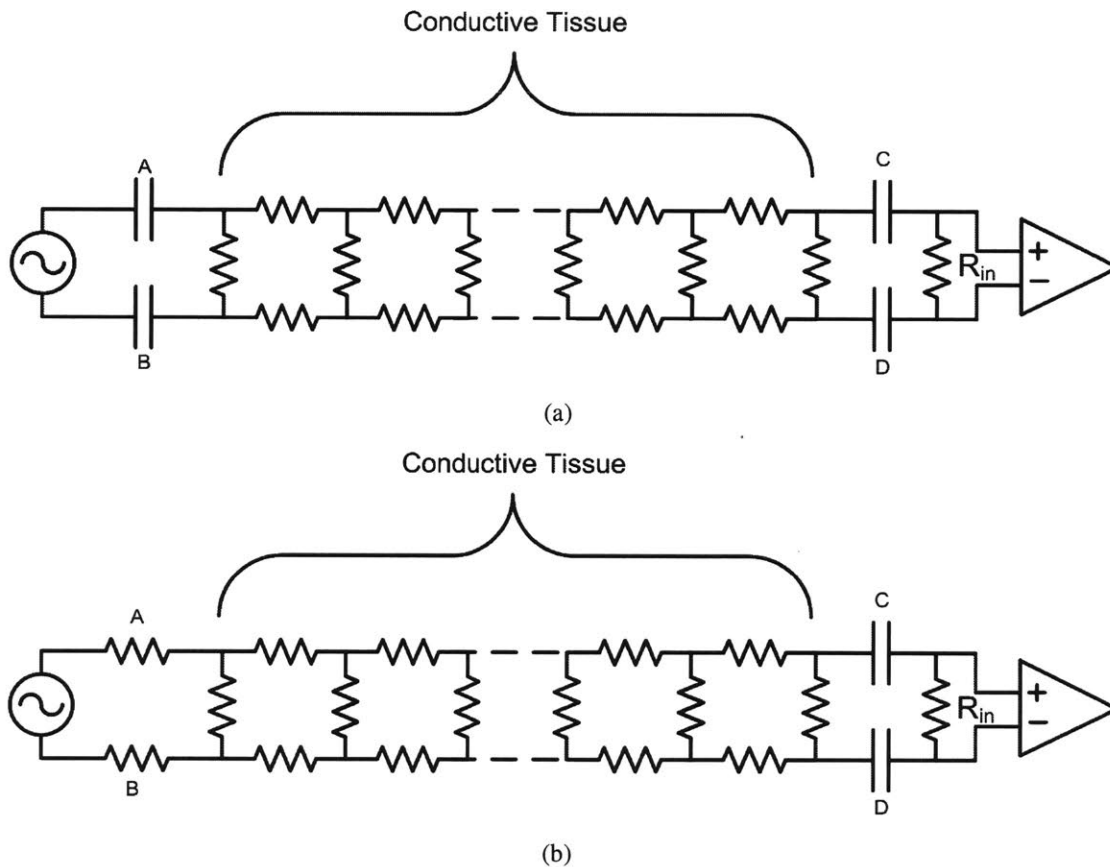
Figure 2-27: (a) The proposed BCC channel model when both transmitter and receiver are connected by capacitive links to the body. (b) The proposed BCC channel model when the transmitter is an implant in the body that is galvanically connected to the BCC channel, and the receiver is outside the body connected to the channel by the capacitive links.

now consist of only one high-pass filter and the gain would exhibit a 20 dB/dec slope. The results, that validate the predictions of the proposed BCC channel model, are shown in figure 2-28.

2.4.2 Implications of the Proposed Channel

The proposed BCC channel model, when both the transmitter and receiver are capacitively coupled, is two high-pass filters. The corner frequencies of the high-pass filters cannot be well controlled as they are dependent on the capacitive links and properties of the body being coupled to. Because the capacitive links can change with body movement, the corner frequency can change during transmission, meaning the channel's attenuation is not
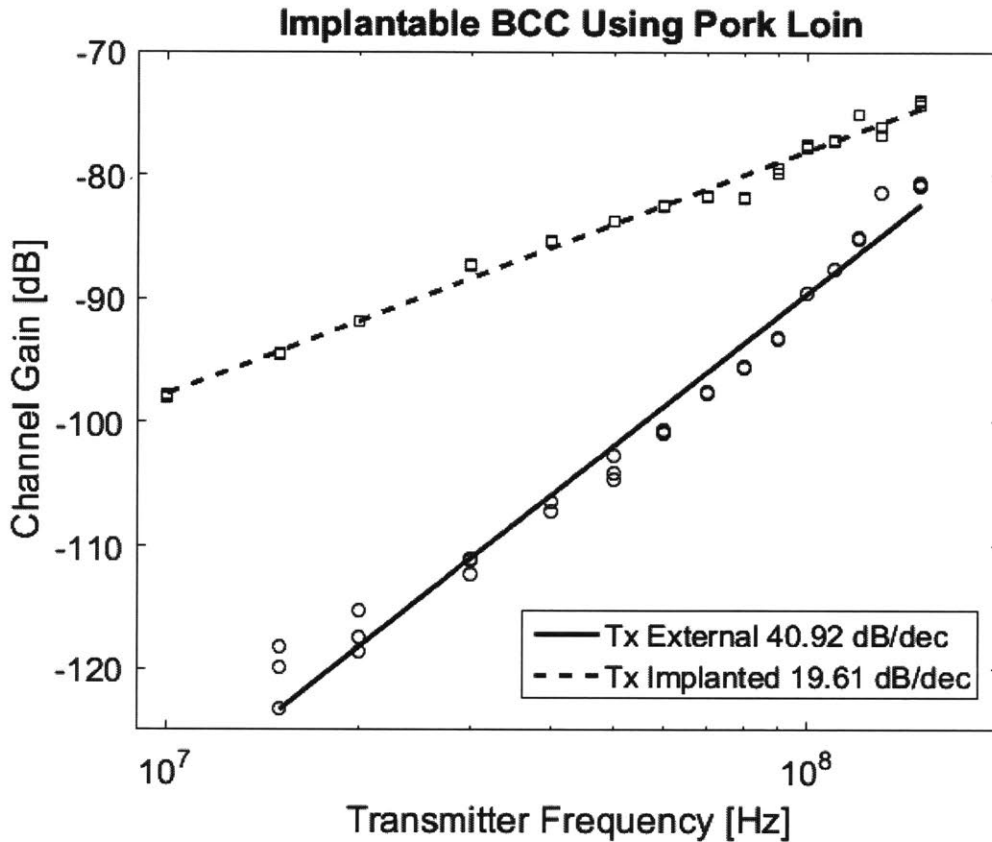
Figure 2-28: The channel gain measurements showing the difference between an external transmitter, that is capacitively coupled, and an implanted transmitter that is galvanically coupled.

constant. Likewise the phase change in the channel is also not constant. Due to the inconsistency of the attenuation and phase change in the channel, data encoded with amplitude and phase are not as robust as frequency. The changing gain of the channel will also modulate any transmitted frequency, causing it to spread. Unless a frequency scheme is sensitive enough to be ruined by the change in frequency due to movement, which is unlikely due to the low frequencies of body movement, data will be most robust encoded with schemes that rely on change of frequencies[7], like FSK. The inverse of frequency, timing, is also a robust way to transmit data using BCC as demonstrated in [15].

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[7]While encoding data with phase and amplitude aren't as robust as frequency, due to the BCC channel, added circuitry such as automatic gain control may be used to ameliorate the problem.

2.5 Summary

This chapter showed the importance and need to use battery-powered, and electrically isolated equipment when making measurements of the BCC channel. An example of a battery-powered, wireless test system was put forth and used to make several measurements of the BCC channel. Using the measurement system an experiment was done to show that the dominant current path is through the body, and that very little current flows through the environment[8]. As the body is the dominant current path for BCC, it is important to understand how how to model the body. This chapter explained, and validated with experiments, modeling the body as a spreading resistance. Previous BCC models excluded implants from being compatible with BCC. In this chapter implants were also shown to be able to use the BCC channel, by 'implanting' the measurement systems electrodes into a pork loin. The most important take away from this chapter is the proposed BCC channel model, shown in figure 2-25, that models the body as a spreading resistance to which electrodes capacitively (galvanically if implanted) couple to.

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[8]An exception for the return path not being through the body would be when something in the environment presents a significantly lower impedance path between the transmitter and receiver, as seen when using grounded measuring equipment (see figure 2-4 and figure 2-5).

Chapter 3

Optimizing the Receiver for BCC: Body Buffered Return

It is possible to design and configure the receiver's amplifier in such a way to increase the gain in the channel. The channel will be defined as the transfer function from the output of the transmitter, to the input of the receiver, including the capacitive links. The channel is a combination of two high-pass filters (see section 2.4). The input resistance of the receiver sets the corner frequency of one of the high-pass filters. As the input resistance increases, the channel's pass band gain will increase and its corner frequency will decrease. Both effects will provide higher gain in the BCC channel over the frequency band of interest, and therefore the receiver should be designed to have a large input resistance. However, as the input resistance increases, it is easier for any stray signals to couple into the input of the receiver, including the receiver's own amplified signal which can cause positive feedback. The coupling of these unwanted signals will limit how large the input resistance can be and is discussed in section 3.2.

3.1 Optimizing the Receiver for BCC

In past implementations of BCC receivers, the electrodes were connected to the input of the receiver's amplifier, with the other electrode connected to ground as shown in figure 3-1. In this configuration the current flowing through the receiver's input resistance creates a po-
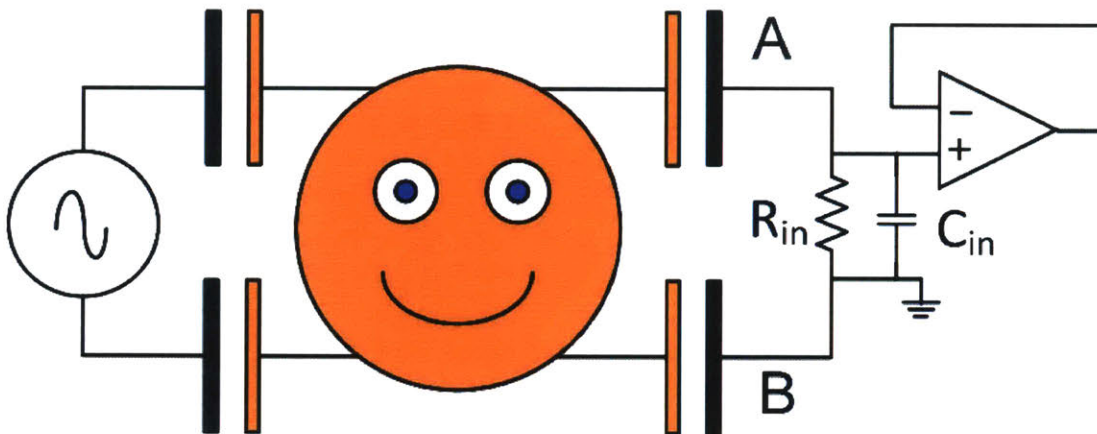
Figure 3-1: The receiver is connected with its local ground being coupled back through the body.
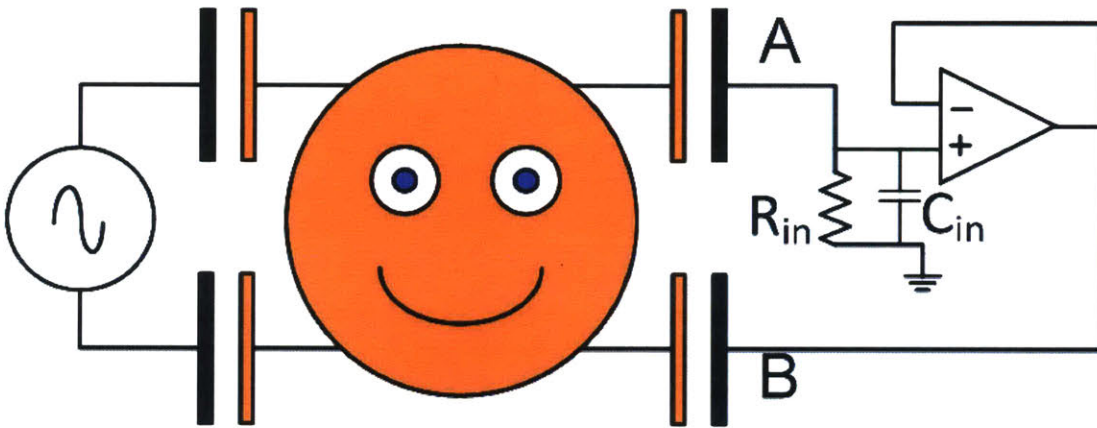
Figure 3-2: The receiver is connected with the output of a buffer being coupled back through the body.

tential difference between nodes 'A' and 'B' which means the resistance directly loads the transmitter. Because the input resistor loads the transmitter, and acts as a voltage divider, as the chosen resistive value of the resistor increases, the voltage drop between 'A' and 'B' will increase, though not proportional to the increase in resistance.

If the electrodes are connected to the receiver as shown in figure 3-2, then the buffer will ensure that nodes 'A' and 'B' are at the same potential which means the input resistance no longer loads the transmitter. This means the same current will flow through the input resistor regardless of its size. Because the current stays the same regardless of resistor size, then the larger the resistor is, the larger the voltage drop will be across it. Because the

voltage across the input resistor increases, without an increase of output-voltage from the transmitter, there is an increase of gain in the channel. Thus by changing the configuration of how the receiver returns current back through the body, the gain in the BCC channel increases. This circuit configuration is called body buffered return, or BBR, as the signal is buffered before returning through the body.

At this point a further in-depth analysis of BBR, its various configurations, and its benefits will be explored. The reader may skip to section 3.3 for the validation of the technique.

3.2 Body Buffered Return

The body buffered technique may be used to amplify any signal that has its own electrically isolated power source, such as a piezoelectric transducer. A piezoelectric transducer produces its own power and does not have to be tied to the same reference as an amplifier, and as such is electrically isolated from the amplifier's power source. A BCC transmitter is also electrically isolated from a BCC receiver, in that the transmitter's and receiver's respective power supplies do not share any reference nodes. As BBR can be used in applications outside of BCC this section will cover the technique generally, but examples will mostly be given with a BCC implementation.

The first step is to take the thevenin equivalent of the BCC channel as shown in figure 3-3. This will be the source to the BCC receiver's amplifier. Note that the capacitive links made by the receiver are included in the thevenin equivalent.
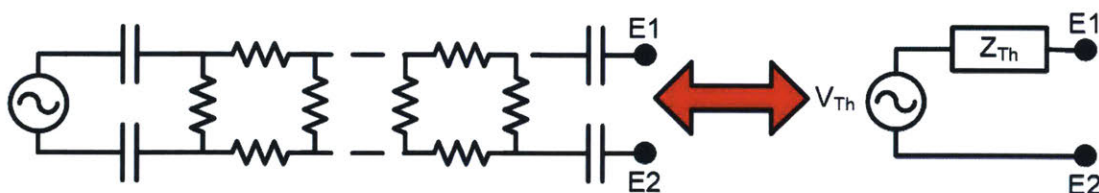
Figure 3-3: The thevenin equivalent of the transmitter and the BCC channel.

Traditionally the BCC receiver will be connected as shown in figure 3-4, with one electrode connected to the input of the amplifier and the second electrode connected to
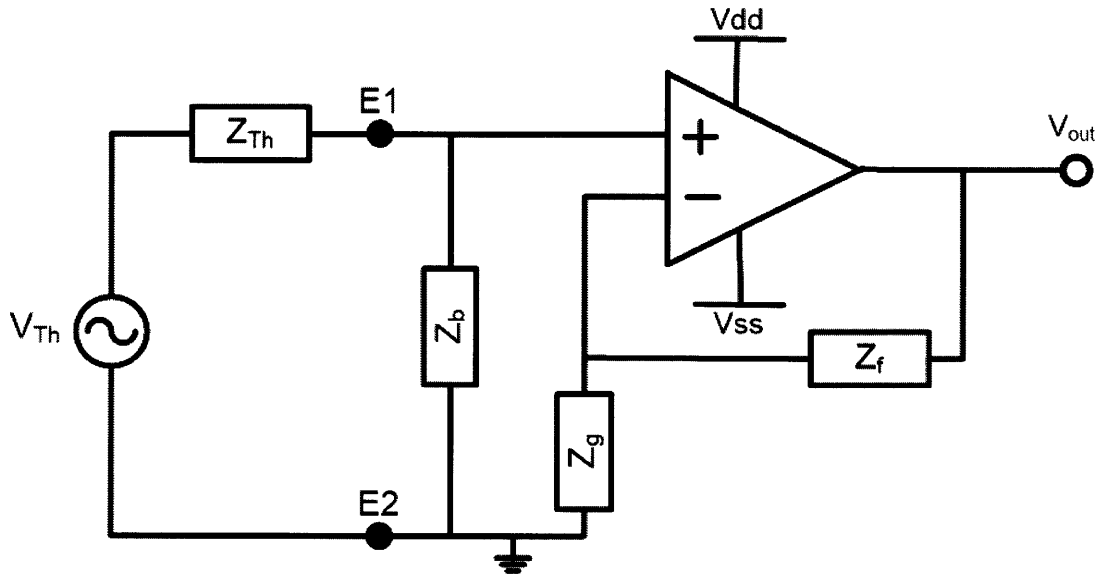
Figure 3-4: The amplifier connected in the traditional way.

the ground plane, or reference, of the receiver. The input impedance between the two electrodes, Z_b, will load the BCC channel and as such will affect the gain ratio of V_{out}/V_{Th}, where V_{out} is the output voltage of the amplifier with respect to the receiver's ground. Mathematically, the gain is expressed as:

$$Gain = \frac{Z_b}{Z_{Th} + Z_b} \left(1 + \frac{Z_f}{Z_g}\right) = \frac{Z_b}{Z_{Th} + Z_b} A \tag{3.1}$$

where A is the gain of the amplifier. Note that the loading effects of Z_b will scale the gain of entire system, with Z_b. This is because the value Z_b will affect the current that flows through it, because it loads the source.

Compare this with the BBR configuration seen in figure 3-5. Here the amplifier is used as a unity gain buffer. One electrode is connected to the non-inverting terminal of the amplifier, and the second electrode is connected to the output of the amplifier. Again the gain will be defined as the ratio of V_{out}/V_{Th}, where V_{out} is the output voltage of the amplifier with respect to the receiver's ground.

To solve for the gain, we assume that no current flows into the non-inverting terminal of the amplifier and that the amplifier forces both electrodes to have the same voltage. Because the electrodes are at the same voltage, the voltage drop across Z_{Th} is V_{Th}. Because no
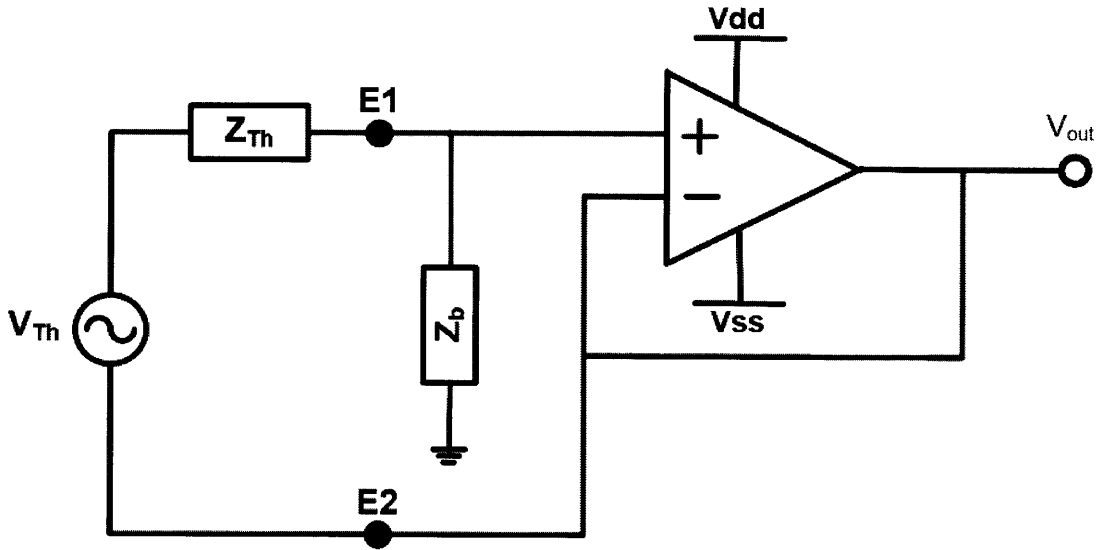
Figure 3-5: The amplifier connected in the BBR configuration.

current flows into the amplifier, all the current that flows through Z_{Th}, which is V_{Th}/Z_{Th}, also flows through Z_b. Thus the voltage at the non-inverting terminal of the amplifier is $Z_b \frac{V_{Th}}{Z_{Th}}$. This is the same voltage as the output of the amplifier, thus the gain of the amplifier is:

$$Gain = \frac{Z_b}{Z_{Th}}$$ (3.2)

Note here that Z_b does not load the source. This is because the amplifier forces both electrodes to be at the same voltage. This decouples the value of Z_b affecting the current that flows from the source. Regardless of the value of Z_b the current flowing through Z_b will always be V_{Th}/Z_{Th}.

Comparing the gain for the traditional configuration, equation 3.1, and the gain for the BBR configuration, equation 3.2, both will increase as Z_b increase. However, traditional configuration will get diminishing returns as Z_b increases, where the BBR configuration will not taper off[1]. Because of this, the signal to interferer ratio can often be better for BBR than for the traditional configuration. Thus the BBR configuration will have a higher gain when:

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[1]This is true as long as the amplifier can keep both electrodes at the same voltage.

$$Z_b \geq Z_{Th}(A - 1)$$

If there is an interferer that is also coupling to the input of the traditional configuration, as seen in figure 3-6, then the output of the signal and interferer are respectively:

$$S_T = \frac{Z_b}{Z_S + Z_b}A, \quad I_T = \frac{Z_b}{Z_I + Z_b}A \tag{3.3}$$

where S_T is the gain the signal receives in the traditional configuration, I_T is the gain the interferer receives in the traditional configuration, Z_S is the thevenin impedance the source uses to couple to the amplifier, and Z_I is the thevenin impedance the interferer uses to couple to the amplifier.

Using the same values for Z_I and Z_S, the respecitve gains for the BBR configuration are:

$$S_{BBR} = \frac{Z_b}{Z_S}, \quad I_{BBR} = \frac{Z_b}{Z_I} \tag{3.4}$$

Taking the ratio of the signal gain to the interferer gain for both BBR and traditional configuration:

$$\frac{S_{BBR}}{I_{BBR}} = \frac{Z_I}{Z_S} \quad > \quad \frac{Z_I + Z_b}{Z_S + Z_b} = \frac{S_T}{I_T} \tag{3.5}$$

Thus when $Z_I > Z_S$ and $Z_b > 0$, the ratio of the signal gain to the interferer gain is larger for the BBR configuration. Thus the signal to interferer ratio will be greater for the BBR configuration given the same conditions.
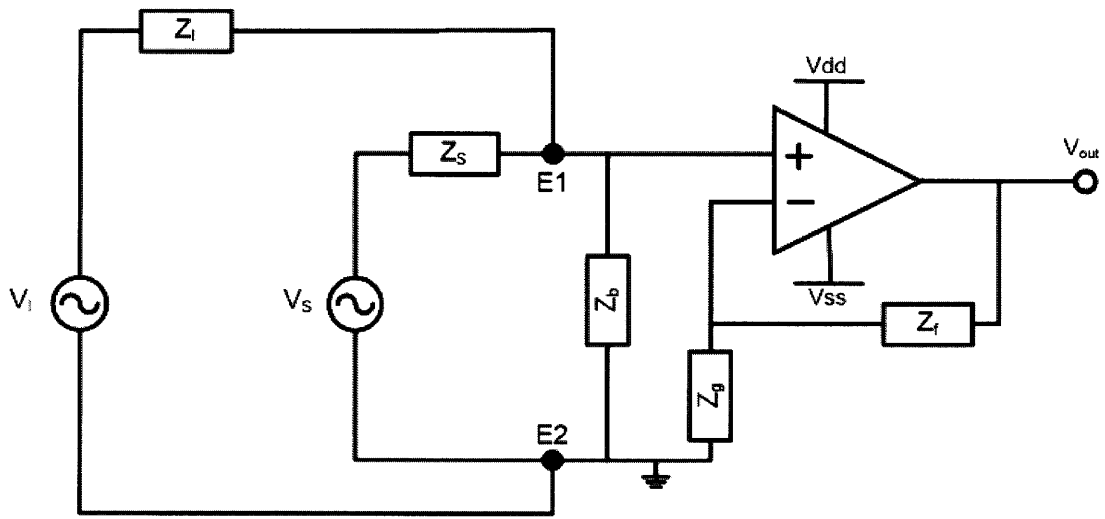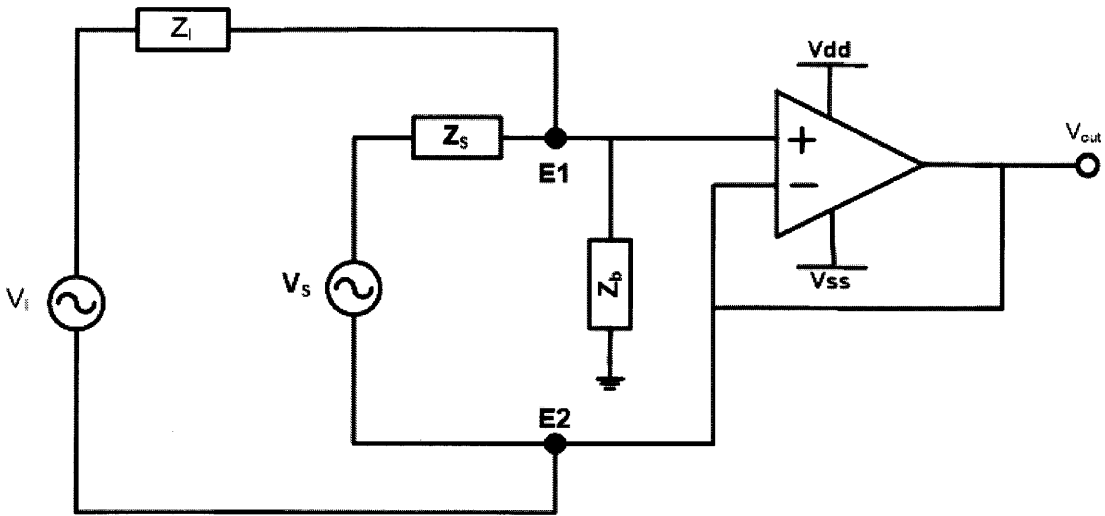
Figure 3-6: Interferers can also couple to the electrodes. (a) shows an interferer coupling to the traditional amplifier, and (b) shows an interferer coupling to a BBR amplifier. Such interferes could be other devices polluting the spectrum, or even the gained up signal of the receiver coupling back to its own input. BBR can provide a higher signal to interferer ratio.

3.2.1 More Amplifier Topologies in a BBR Configuration

Up to this point BBR has been presented using single ended amplifiers. BBR is not limited to single ended and can implemented using differential and fully differential amplifiers. Using such amplifiers could be used when a higher CMRR is required that a single ended amplifier can't provide.

The key to apply BBR to other amplifier topologies, is to make sure that the amplifier is configured in such away that feedback from the amplifier presents a virtual short to the body at the electrode interface. Creating the virtual short in essence 'buffers' the signal present at the body. Thus to apply the BBR configuration to the standard differential amplifier topology, shown in figure 3-7(a), impedances Z_1 and Z_2 are eliminated to create a virtual short across the electrodes. The result is the BBR configuration of a differential amplifier topology shown in figure 3-7(b).

The gain for the differential BBR amplifier will be defined as the ratio of V_{out}/V_{Th}, where V_{out} is the output voltage of the amplifier with respect to the receiver's ground. The gain of this configuration is:

$$Gain = \frac{Z_f + Z_b}{Z_{Th}} \tag{3.6}$$

for high CMRR Z_b should equal Z_f.
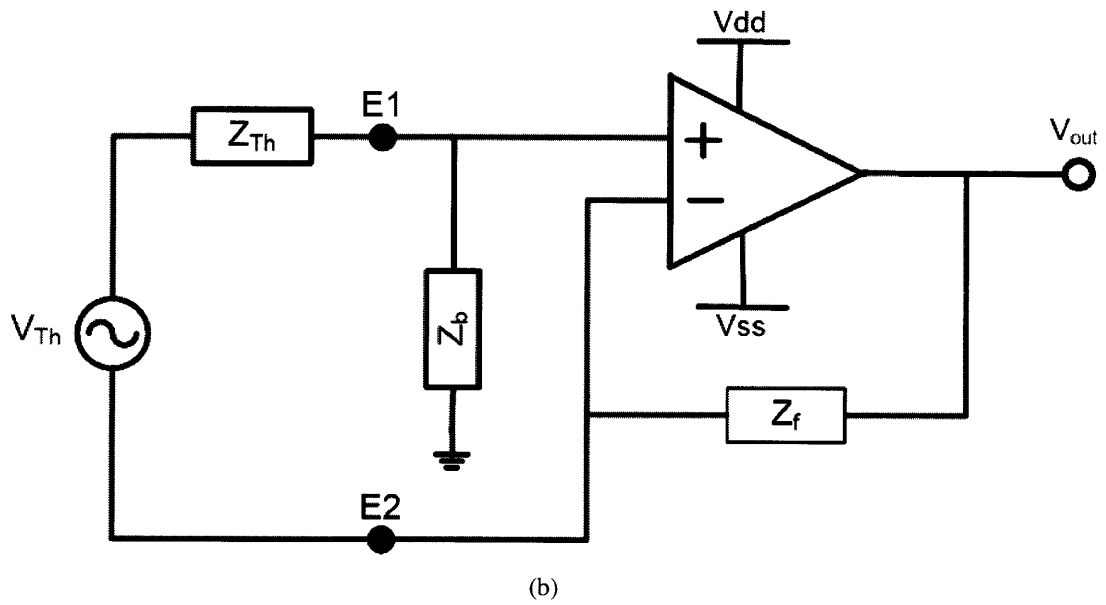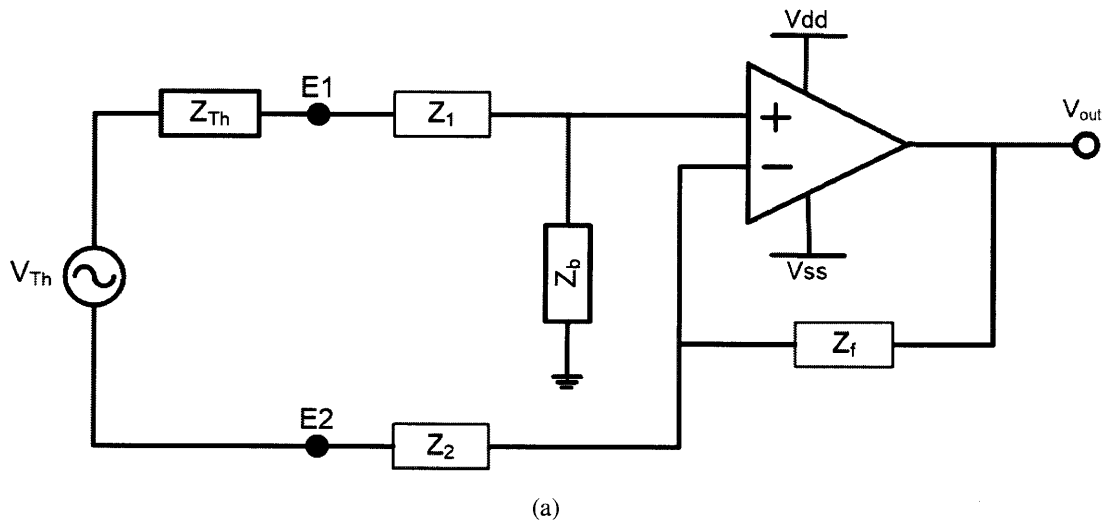
Figure 3-7: Applying BBR to a differential amplifier. (a) A standard differential amplifier. (b) By removing the impedances Z_1 and Z_2 from (a) a virtual short is created between the electrodes, making this a differential BBR amplfier.

The BBR configuration using a fully differential amplifier topology is shown in figure 3-8. The gain will be defined as the ratio of V_{out}/V_{Th}, where V_{out} is the output voltage difference measured between the amplifier's two outputs. The gain of this configuration is:

$$Gain = \frac{2Z_f}{Z_{Th}}$$ (3.7)
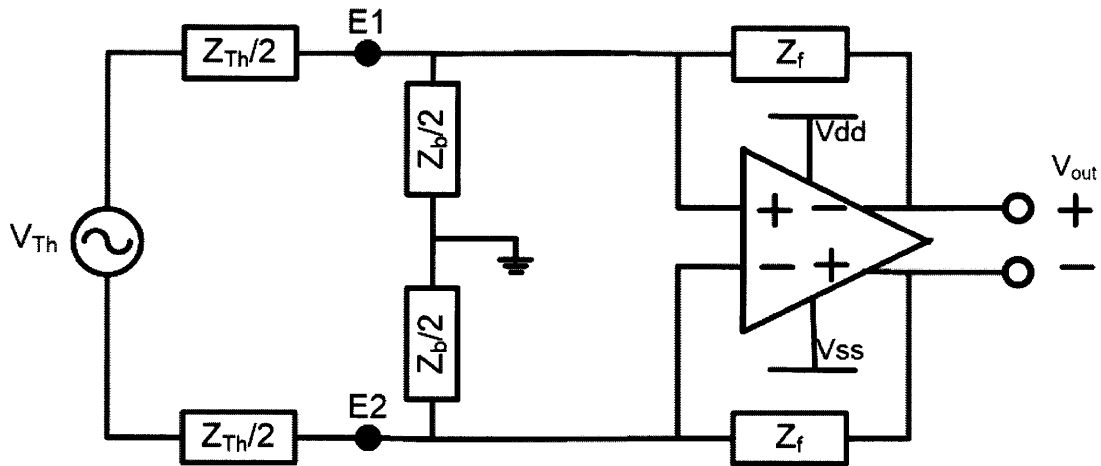
Figure 3-8: A fully differential amplifier topology connected in the BBR configuration. Notice the amplifier creates a virtual short between the two electrodes.

3.3 Validation of BBR

To prove BBR, the BCC's channel gain was measured by placing the transmitter on the head with one electrode on the forehead and the other on the mastoid behind the ear. The receiver was placed on the waist with the electrodes attached near the belt line. The frequency was swept over the 10 MHz-150 MHz range. Three different resistance values were tested for the input resistance of the receiver: 50 Ω, 200 Ω, and 2,000 Ω. This is the same set up, and done at the same time, as the test in section 2.2.1. For each resistance the test was run twice: once with one electrode connected to the receiver's mid-rail voltage, or "ground" (for theses test results see section 2.2.1), and once with the electrode connected to the buffered output[2]. The second electrode was always connected to the input of the receiver. By connecting the one electrode to the buffered output, the receiver was configured to use BBR. By varying the input resistance the effects that BBR predicted were validated and are shown in figure 3-9.

When BBR is used, the same current will flow through the input resistance of the receiver regardless of its impedance. So as the input resistance increases, the gain in the channel should also increase by the same factor. With the resistance values used in the test there should be a gain increase of 12 dB and 20 dB between the increase from 50 Ω to 200 Ω and 200 Ω to 2,000 Ω respectively. At lower frequencies the gain increase for BBR between 50 Ω and 200 Ω is 12 dB. At higher frequencies the gain increase from BBR decreases. There are two reasons for this. First, the buffer has to produce the same voltages at nodes 'A' and 'B', from figure 3-2, or the receiver will load the transmitter causing the BBR effect to taper. This means the output of the buffer has to have the same magnitude and phase as the input. At higher frequencies the buffer's phase response between the input and output is no longer 0 degrees, and therefore nodes 'A' and 'B' are not at the same potential, causing the effect of BBR to diminish. Second, the input impedance to the receiver has some capacitance that is in parallel with the input resistor. This means as the frequency increases, the total input impedance decreases, leading the gain increase from BBR to diminish. The receiver's input capacitance is also responsible for the BBR gain

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[2]The buffered output is explained in the context of the measurment equipment in section 2.1.1.
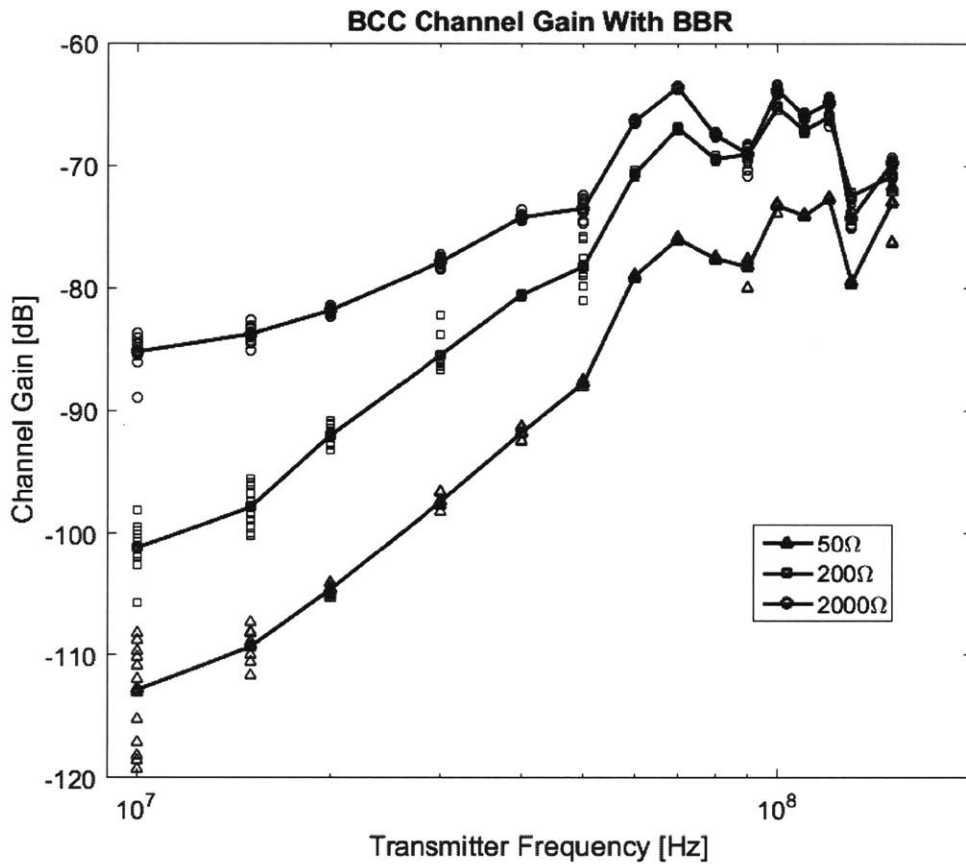
Figure 3-9: The magnitude frequency response for BCC channel using BBR.

increase, from 200 Ω to 2,000 Ω, being smaller than 20 dB even in the lower frequencies.

Despite these non-ideal characteristics of the commercial parts, the gain is still higher with BBR than using the ground return for any given input resistance. The difference in the gains can be seen in figure 3-10, which displays a comparison of both the traditional amplifier connection (as seen in section 2.2.1) and the BBR amplifier connection. These results show that the channel gain is higher when BBR is implemented than when BBR is not implemented, verifying that it is possible to design and configure the receiver's amplifier in such a way to increase the gain in the channel.
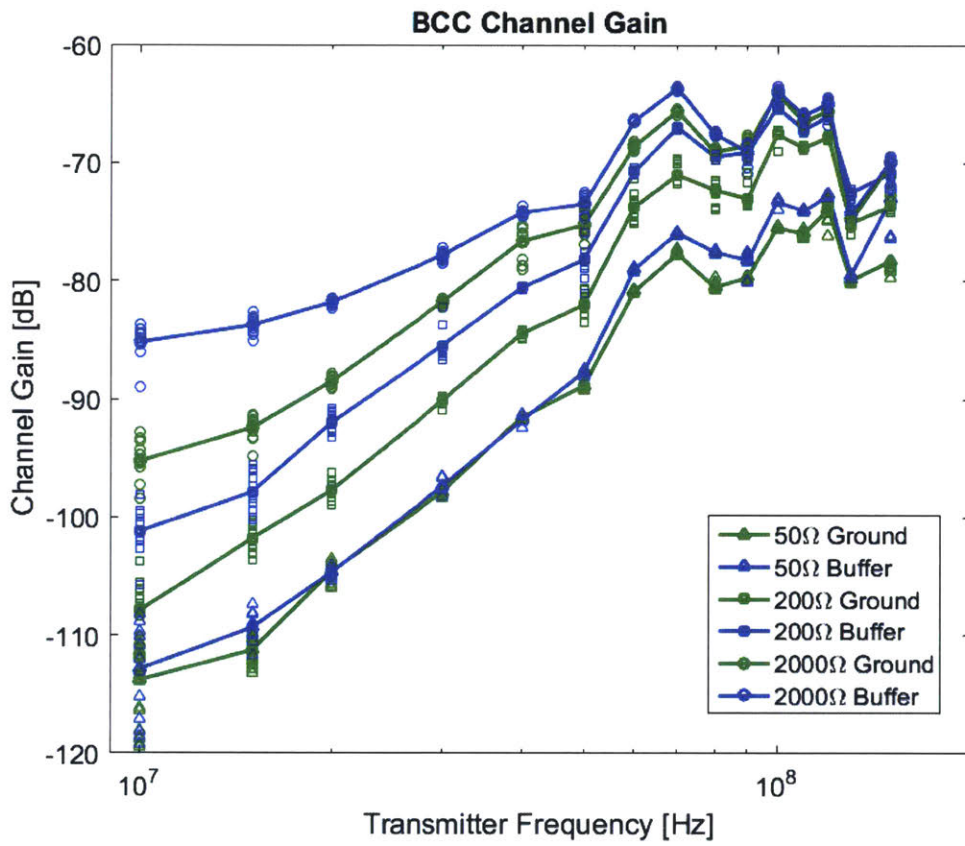
Figure 3-10: The magnitude frequency response for BCC channel, comparing both traditional and BBR.

3.3.1 BBR Using a Source-Follower MOSFET

An amplifier must keep both electrodes at the same voltage for BBR to work. While an op-amp configured as a unity gain buffer was used to prove the technique in section 3.3, it would be preferable if a source-follower could be used. The source-follower can have a faster frequency response for the same amount of power, at the expense of having a DC offset from the input. In general a DC offset would not allow BBR to work because the amplifier cannot produce a virtual short. However, using a coupling capacitor to block the DC offset would allow BBR to be used for high frequency applications. As BCC uses capacitive links they can be used as the coupling capacitor, or an explicit coupling capacitor may be used.

An integrated source-follower amplifier was fabricated in a TSMC 180 nm process . The source-follower, depicted in figure 3-11, is an nMOS transistor made using a deep n-well process so that the source of the transistor could be connected to its body. This allowed for the the gain of the amplifier to be closer to unity by having the high trans-conductance of an nMOS source-follower, without the body effect diminishing the gain. Having the gain be as close to unity as possible is important, because if the gain is not exactly one, the amplification produced by BBR will not be as high.
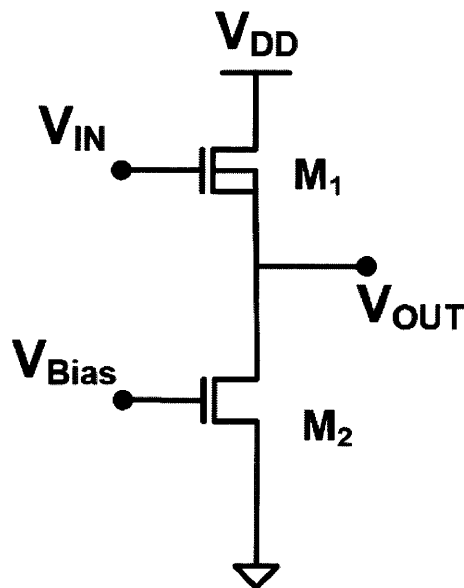
Figure 3-11: An nMOS source-follower.

To test the effectiveness of the source-follower in a BBR configuration, it was connected as shown in figure 3-12. Here the bias resistor for the source-follower is attached to V_{dd}. This was done so that the output of the source-follower would be biased at $V_{dd} - V_{tn}$, where V_{tn} is the threshold voltage of the source-follower. This gives the source-follower's current mirror, M_2, the maximum amount of head room to stay in saturation. The balun is used to present a voltage source that is electrically isolated from the power supply of the amplifier, as required in BBR (see section 3.2). Capacitors C_{E1} and C_{E2} represent the capacitive links made by the electrodes. The capacitors also double as blocking capacitors of the DC offset from the source-follower. The source-follower drives further amplification and circuitry that is used to process the signal for frequency detection. For further details of this circuitry see section 5.2.4. Suffice it to say here that this circuitry will take a sinusoid input and make it a square wave with the same frequency as the sinusoidal input.
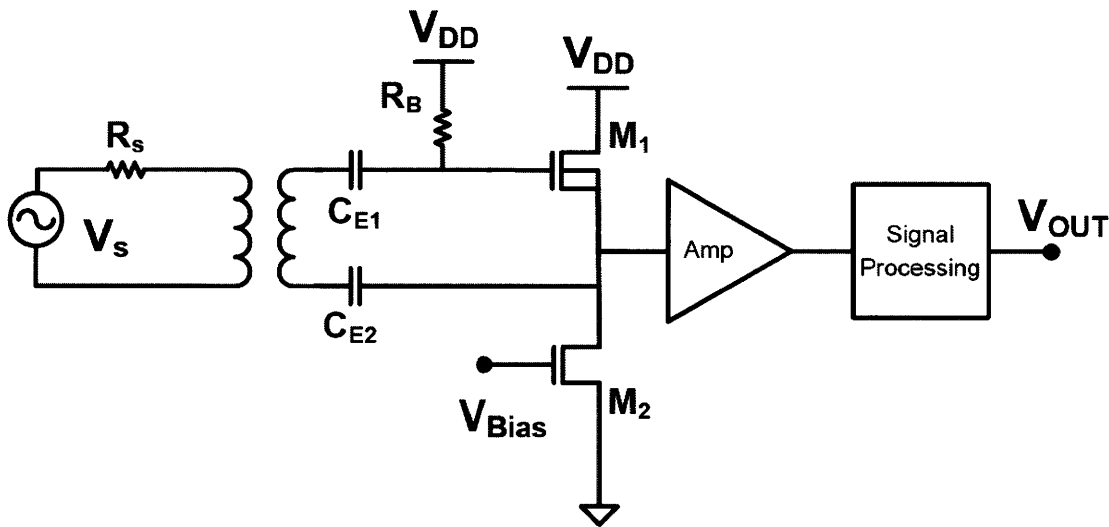
Figure 3-12: The testing circuit for the nMOS source-follower.

To test if the source-follower can be used to implement BBR, an input sinusoid was applied at the input of the balun and the square wave output was recorded. Three different experiments were performed. First, the BBR was turned off. Second, the BBR was turned on and the value of the bias resistor, R_B, was set to 10 kΩ. Third, the BBR was turned on and the value of the bias resistor, R_B, was set to 100 kΩ. The output for the three tests are shown in figure 3-13(a), with a zoomed in version in figure 3-13(b). The output is a square

75

wave because the BBR source-follower was the first amplifier in a chain of amplifiers that ends with a comparator that digitizes the input frequency into a square-wave[3]. With the BBR turned off, there is some interference that causes the signal to not trip the comparator, causing the gaps in the output. As the signal experiences higher gain with BBR turned on, and again with the increase of R_B, the signal strength overcomes the interference so that the comparator trips at the same frequency as the input. These results show that BBR can indeed work with a source-follower.

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[3]The full chain can be seen in figure 5-10, where the square wave output is labeled 'Off Chip Output (Test)'. The BBR source-follower is part of the LNA.
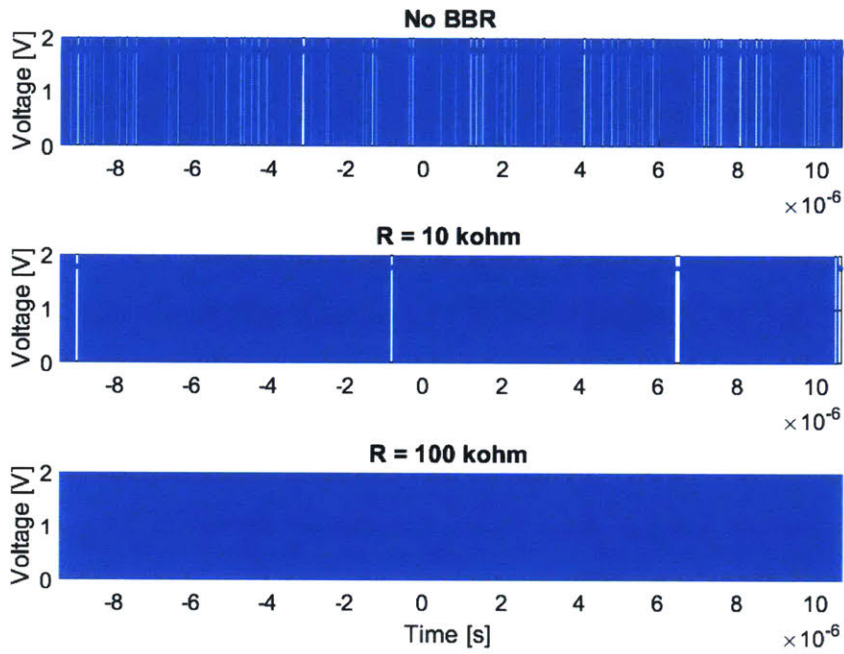
(a)
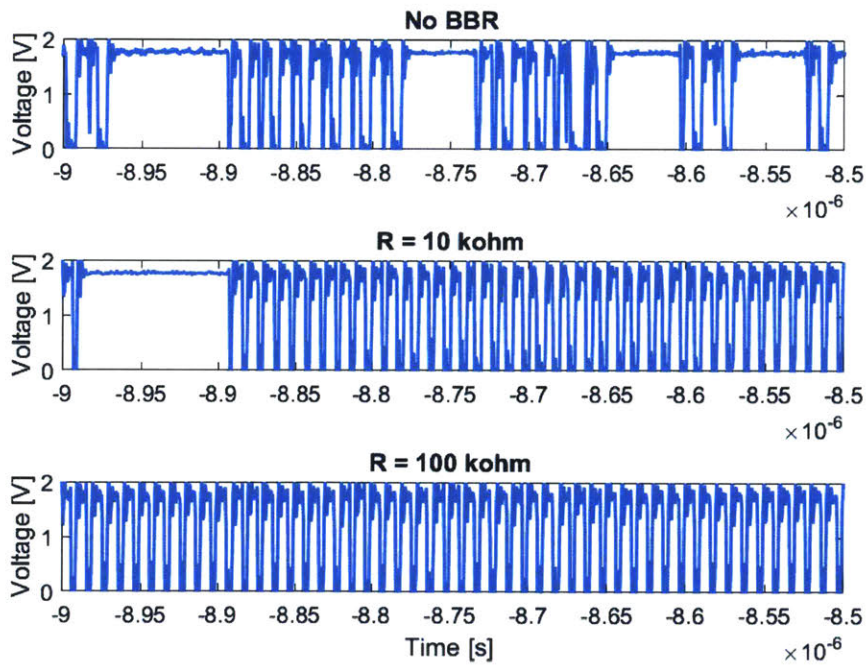
(b)

Figure 3-13: (a) BBR using a source-follower. (b) Zoomed in to see detail..

3.4 Summary

This chapter showed that the BBR amplifier topology can increase the BCC channel gain by changing the transfer function of the channel. The unique feature of BBR is that a virtual short is created between the two receiving electrodes, by the means of an amplifier. Creating this short allows the maximum amount of current to flow into the receiver, and this current is independent of the input impedance of the amplifier. By choosing a large input impedance the gain can be made arbitrarily large; with the input impedance usually being limited by parasitic capacitance. The gain was shown to be the ratio of the input impedance and the impedance seen looking back into the channel from the input of the receiver. It was shown that this ratio allows BBR to have a larger signal to interfere ratio than traditional amplification.

BBR was further explored to not just 'buffer' the incoming voltage signal between the electrodes, but to amplify the signal as well. While this technique can yield larger channel gain, the feedback can create positive feedback and cause oscillations. BBR was also shown to be able to be implemented using differential and fully differential amplifiers, thereby gaining the benefits of BBR and the CMRR of the amplifier topology. Further, BBR was shown to be able to work with a source-follower and coupling capacitors to block the DC offset, while still providing the virtual short between the electrodes at higher frequencies.

Chapter 4

Asynchronous Digital Communication

There are multiple schemes that dictate how digital data can be encoded using electromagnetic waves. The data can be encoded either in amplitude, phase, timing, frequency, or a combination of the four. Such schemes include amplitude shift keying (ASK), phase shift keying (PSK), pulse position modulation (PPM), frequency shift keying (FSK), and quadrature amplitude modulation (QAM). All of these schemes, except PPM, require the receiver's clock to be synchronized to the transmitters. Having synchronized clocks between the transmitter and receiver is critical to knowing when a symbol is valid as new data; without synchronization it would be impossible to know if the same symbol was being sent more than once. While PPM doesn't require synchronization between the clocks on the Tx and Rx, the precision and speed of the clocks become critical at higher data rates as the detectable time difference between pulses become smaller.

In an effort to reduce overhead that is used for clock synchronization and eliminate power consumption of circuits that perform the synchronization, an asynchronous digital communication scheme was developed for the BCC receiver. This Chapter will: explain a scheme for asynchronous digital communication, survey a few ways to practically implement the scheme, and detail the implementation used in the integrated BCC receiver.

4.1 Synchronous Digital Communication

Before explaining an asynchronous communication scheme, it will be useful to review how synchronous communication schemes are defined, and how they are implemented. The review of synchronous communication will help to highlight the differences between synchronous and asynchronous communication. Throughout this text the definitions in table 4.1 will be used. Table 4.1 also gives examples of typical ways to implement these definitions.

Table 4.1: Communication Definitions and Examples

Symbol	A defined characteristic of a signal that has meaning and is distinguishable	FSK ASK PSK QAM	Frequency Amplitude Phase Phase & Amplitude
Codeword	The digital bits being transmitted	$n = 1$ $n = 2$	$1, 0$ $11, 10, 01, 00$

In a typical synchronous communication system, the symbol and codeword are synonymous with each other. Meaning the symbol being transmitted encodes the bit value of the codeword, and the clock marks when a given symbol is a valid codeword. As an example, consider frequency shift keying (FSK) where the communication symbols are encoded in the frequency. If two frequencies, F_0 and F_1, are used then symbol F_0 will encode the codeword '0', and F_1 the codeword '1'. When the clock edge tells the receiver that a new codeword is valid, the receiver will determine which symbol/frequency is being sent. If it is F_1, then the bit received is a '1', and '0' is received if it was F_0. If the bit-stream '11' is desired to be sent, then the transmitter would send F_1 for two consecutive clock cycles. The necessity of a synchronized clock between transmitter and receiver is illustrated in figure 4-1. Figure 4-1 shows that both frequency and phase of a clock can affect which bits are received, highlighting the need of synchronized clocks between transmitter and receiver.

There are various ways to synchronize the transmitter's clock with the receiver's clock. One way is before actual data is sent a preamble of two symbols will be sent at the clock rate. This allows the receiver to feed the timing of the detected symbols into a phased lock loop (PLL) that once locked will then be used as the receiver's clock to validate symbols.
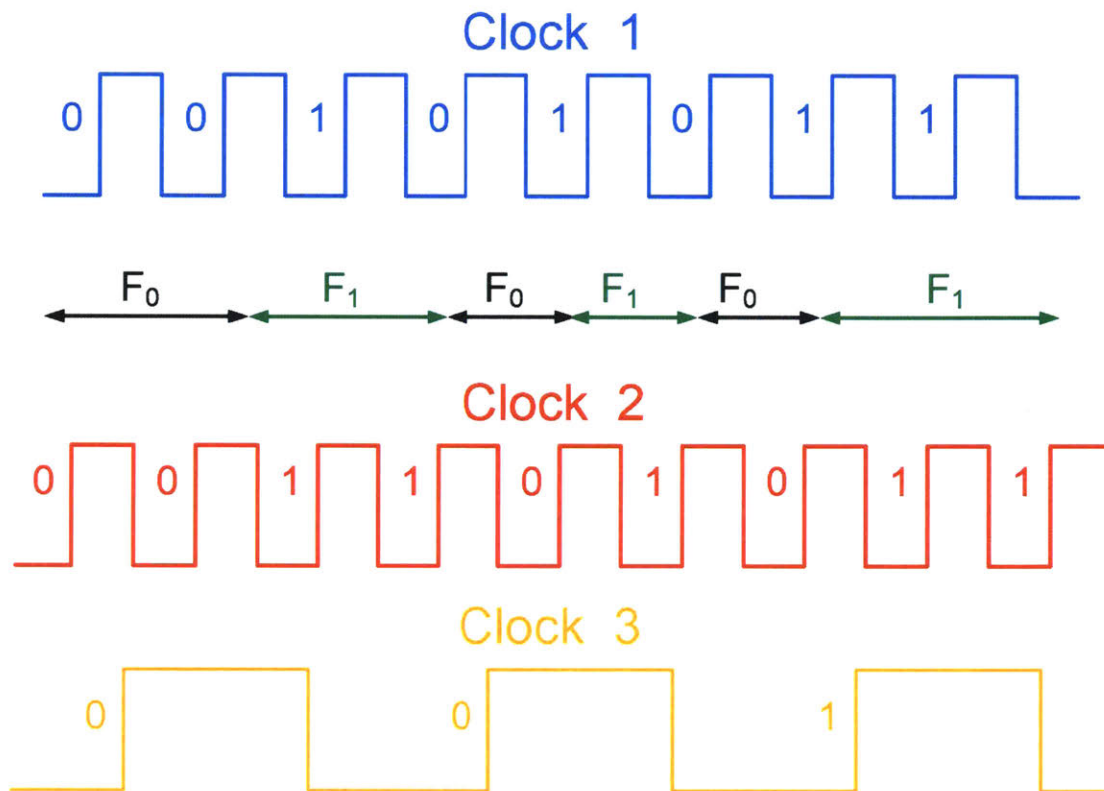
Figure 4-1: Frequencies/symbols being interpreted with different clocks. Each clock validates a frequency/symbol on its rising edge. Clocks 1 and 2 are the same frequency but with different phase, while clock 3 is a different frequency.

Another way is to Manchester encode the data being sent, which effectively embeds the clock within the transmitted data itself, a clock and data recovery circuit will then separate the two and decode the received data. Both of these add overhead in time and/or circuitry to accurately decode a bit-stream.

4.2 Asynchronous Digital Communication

Asynchronous digital communication can relieve the overhead in synchronous communication by removing the need of a synchronized clock to validate when a symbol's codeword is valid. In the asynchronous communication scheme the validity of a new code word is when the symbol changes, and the value of the code word is contained in the relationship between the two symbols. Here, unlike in the typical synchronous scheme, the symbol and

the code word are **NOT** synonymous.

Continuing the example of FSK from section 4.1, we'll define the codeword '0' to be the change from F_0 to F_1, and the codeword '1' to be the change from F_1 to F_0. Using this relationship and applying it to the same received signal as in figure 4-1, the receiver would have received the bit stream '01010'. Because the validity of the codeword happens when the received symbol changes, there is no need for a clock.

Problems arrive in this example however. Using only F_1 and F_0 as symbols there is no way to send a '1' if currently sending symbol F_0 as F_1 is the only other symbol to change to which will signify a valid codeword, and a transition from F_0 to F_1 is already defined as the codeword '0'. Similarly there is no way to send a '0' if currently sending symbol F_1.

A solution is to add another symbol, in this case the frequency F_2. Figure 4-2 shows the defined relationship between each frequency transition. Using this relationship, to send the bit stream '0100', the transmitter would start by sending F_0. The transmitter would then stop sending F_0 and transmit F_1. The transition from F_0 to F_1 signifies a new codeword was sent, and that codeword is defined to be '0'. Now the transmitter is currently sending F_1 it would stop sending F_1 and send F_0. The transition from F_1 to F_0 signifies a new codeword was sent, and that codeword is defined to be '1'; the total bit-stream sent so far is now '01'. Now the transmitter is currently sending F_0 it would stop sending F_0 and send F_1. The transition from F_0 to F_1 signifies a new codeword was sent, and that codeword is defined to be '0'; the total bit-stream sent so far is now '010'. Now the transmitter is currently sending F_1 it would stop sending F_1 and send F_2. The transition from F_1 to F_2 signifies a new codeword was sent, and that codeword is defined to be '0'; the total bit-stream sent so far is now '0100'. This data transmission example is shown in figure 4-3. Please note that the duration each frequency is sent in this figure is arbitrary, as the duration of the symbol being sent does not contain any information. Only the transition from one frequency to the other, and the relationship between those frequencies contain information.

The solution to be able to encode 1 bit of information for each symbol hop in the example above was to have 3 symbols. Having 3 symbols allowed 2 unique symbols to be transitioned to – for every symbol. In general if a codeword of n bits is desired to be sent, per symbol transition, there will need to be 2^n unique symbols to transition to for every
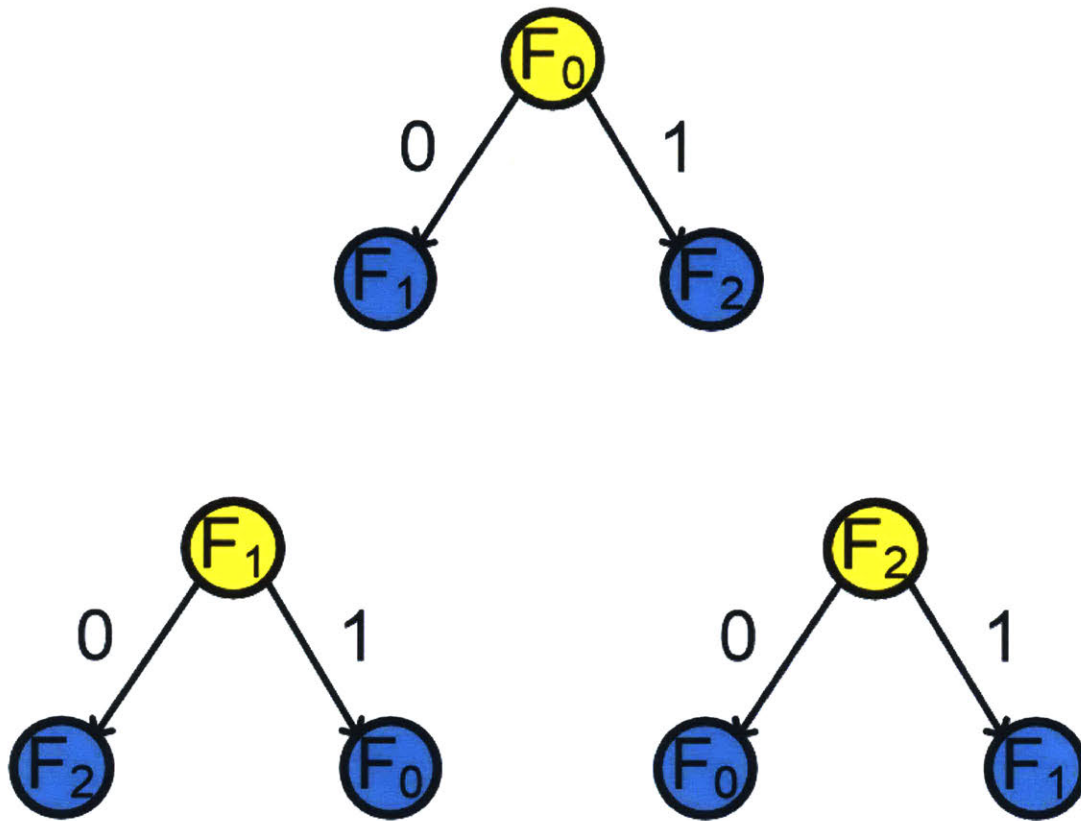
Figure 4-2: One way to define the codeword relationship between three frequency transitions.

symbol. Therefore, including the current symbol being transmitted and the 2^n symbols to transition to, there will need to be a total of $2^n + 1$ symbols.

This scheme to achieve asynchronous communication can be applied to any form of digital communication. The need to add an additional symbol is true regardless of which communication scheme is used to encode the symbols. To help illustrate a larger n asynchronous communication scheme consider the following example of $n = 3$. To encode 3-bits per symbol hop, nine unique symbols will be needed 'A' – 'I'. The nine symbols and their codeword relationships are found in the top left of figure 4-4. The nine symbols are placed on a circle. The number of segments between each symbol, while moving clockwise around the circle, is the codeword relationship between the two symbols. As an example the hop from 'A' to 'B' is '000' and from 'A' to 'C' is '001', as there are '1' and '2' segments between each respective symbol pair. The chosen relationship between the symbols in this

$$F_0 \qquad F_1 \qquad F_0 \qquad F_1 \qquad F_2$$

$$0 \qquad\qquad 1 \qquad\qquad 0 \qquad\qquad 0$$
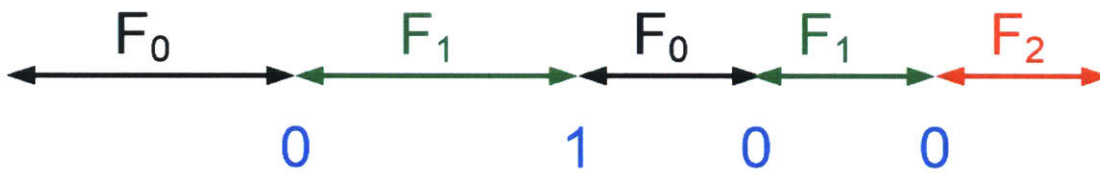
Figure 4-3: Sent codewords, as a function of the frequency changing. The codeword relationship between frequencies used are found in figure 4-2.

example was chosen to be easy to show in an example, while a detailed explanation on how to choose a relationship can be found in section 4.3.2. Using this symbol relationship the following example shows how to send the bit stream '1000 0000 0111'. The initial state of the system is when the transmitter is off and no frequency-symbols are being transmitted. The transmitter then starts by transmitting symbol 'A'. When the transmitter quits sending symbol 'A' and transmits symbol 'F' instead, the transition, or hop, indicates that a new codeword is valid. Because there are five segments between symbols 'A' and 'F' the code word that was sent was '100'. Next whenever the transmitter hops and transmits symbol 'G', instead of 'F', this indicates that a new code word has been sent. Because there is one segment between symbol 'F' and 'G' the code word '000' was sent. As seen in the rest of figure 4-4 the third hop also sends the code word '000', and the fourth hop sends '111'.
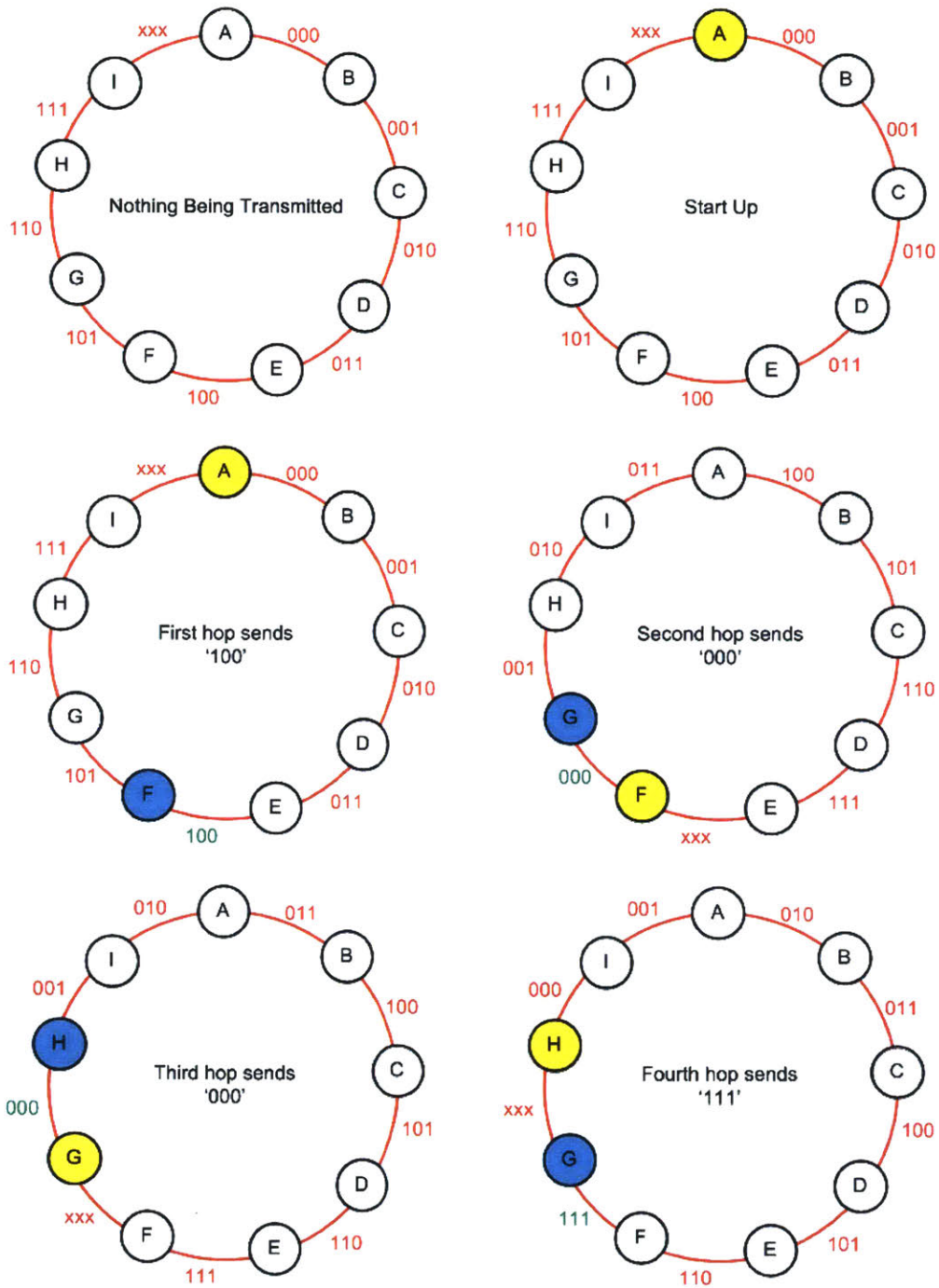
Figure 4-4: Sending the bit stream '100 000 000 111' with 3-bit asynchronous digital communication. The yellow-colored symbol identifies the frequency before the hop, while the blue designates the frequency after the hop.

85
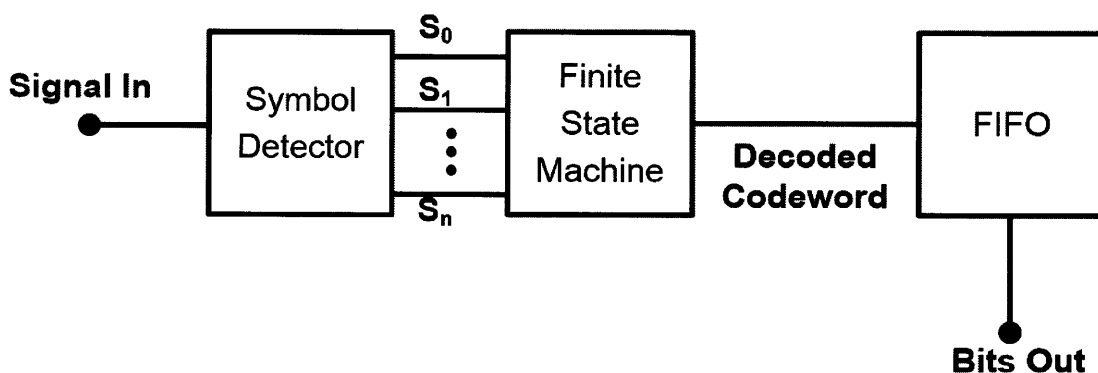
Figure 4-5: The signal path for an asynchronous digital communication receiver.

4.3 Implementation of Asynchronous Digital Communication

The implementation of asynchronous digital communication is actually quite straight forward. The transmitter needs to be able to generate all the symbols necessary, and the receiver must be able to detect each symbol. Each time a new symbol is detected the receiver can use that to change the state of a finite state machine (FSM). The current state of the FSM and the detection of a new symbol, would feed a FIFO the next codeword. The FIFO can then be used to buffer data and send it out — synchronously if needed (see figure 4-5).

4.3.1 Start Up

In asynchronous digital communication bits of data, or codewords, are conveyed in transitions from one symbol to another. This means that the first codeword sent needs two symbols so that there can be one transition between the two symbols. The first symbol sent is called the start up symbol, a transition to it does not convey a codeword, but puts the FSM in a known state. Choosing a start up symbol is arbitrary and is implementation-dependent, but judicious choices can reap benefits.

One implementation may call for an additional symbol that is only used as a start up symbol. Another implementation may require that after a certain number of codewords have been received the receiver's FSM will enter an idle state waiting for the start up symbol

to be sent before processing more codewords. Still another implementation may require that if a codeword hasn't been received in the last 't' amount of time, then the receiver will go into an idle state waiting for the start up symbol to be sent before processing more codewords. This is not an exhaustive list of implementations, and each implementation has its tradeoffs. Many of the tradeoffs in these examples are dependent on, and affect, the specific network implementations; this work will not go into those tradeoffs as the goal here is to describe just the physical layer of asynchronous digital communication. Suffice it to say the physical layer requires a start up symbol and a good way to choose a start up symbol, regardless of the implementation, is to choose the symbol that is least likely to be erroneously detected by the receiver.

4.3.2 Optimizing Data Rate

While this communication scheme is asynchronous, the data rate is not infinite. As in traditional digital communication, the speed at which the symbol's change is the baud rate, BR. The data rate is the number of bits per baud multiplied by the baud rate $n * BR$. However in asynchronous digital communication, the baud rate:

1. Does **not** need to be constant

2. Can be symbol dependent

Because there is no clock, the length of time a symbol is sent does not corrupt the data being sent. However there is a lower bound on the time period a symbol needs to be sent. It will take some finite amount of time for the receiver to detect a symbol and change the FSM, and we will call this time period T_{det}. For proper and error resistant data transmission, T_{det} will be the minimum amount of time the transmitter will need to send that symbol, otherwise the receiver may miss detecting a symbol. While the minimum time a symbol must be sent is T_{det}, the transmitter can transmit and hold that symbol for longer. While there is no upper bound for how long a symbol may be transmitted, no new data is being sent during that time as data is sent as a transition between symbols.

It does not necessarily take the same time to detect all the symbols. Consider an asynchronous frequency shift keying (AFSK) scheme that uses three frequencies, where

$F_0 < F_1 < F_2$. Now assume it takes one full cycle to detect any given frequency, meaning $T_{det} = 1/F_x = T_x$. This means that it takes less time to detect F_2 as it does to detect F_1, and less time to detect F_1 as it does F_0, as $T_0 > T_1 > T_2$. It follows then that transmitter need not transmit each symbol for the same amount of time, and that by sending each symbol for T_x the data rate is:

1. Maximized

2. Non-constant

3. Data dependent

4. Scheme dependent

To illustrate the more non-intuitive points consider the following examples. Take the three frequencies $F_0 = 60\,\mathrm{MHz}$, $F_1 = 100\,\mathrm{MHz}$, and $F_2 = 150\,\mathrm{MHz}$. Assume each symbol has the same probability of being sent, meaning for a given data stream each symbol is transmitted $1/3$ of the time. If it takes one full cycle to detect each frequency, then the maximized data rate is given by:

$$\frac{3}{\frac{1}{60\,\mathrm{MHz}} + \frac{1}{100\,\mathrm{MHz}} + \frac{1}{150\,\mathrm{MHz}}} = 90\,\mathrm{MHz}$$

Now consider a data stream '0000' when it is encoded using the 3-symbol AFSK scheme shown in Figure 4-6. We will choose F_2 as our start up frequency, as it is the fastest frequency to detect. To send this data stream the symbols, including the start up, would be $F_2 F_1 F_0 F_2 F_1$. If each symbol was sent for 1 cycle for the symbol the total time spent would be: 56 ns. As 4 bits of data were sent this would have a data rate of 70 Mbps [1].

If you know a priori that for a given application certain codewords are more likely to be sent, then a better asynchronous scheme may be chosen. Consider the data stream '0000' when it is encoded using the scheme shown in Figure 4-7. Because we know that the data stream is heavily 0's we engineer the scheme so that the '0' codeword is always represented as the transition to the fastest detectable available symbol. With this scheme the symbols,

[1]Note that the start up symbol's detection time was taken into account in this example. As the data stream has more codewords, the start up symbols effect on the data rate will approach 0.

including the start up, would be $F_2F_1F_2F_1F_2$. If each symbol was sent for 1 cycle for the symbol the total time spent would be: 40 ns. As 4 bits of data were sent this would have a data rate of 100 Mbps, 30 Mbps faster than the non-enginered scheme.
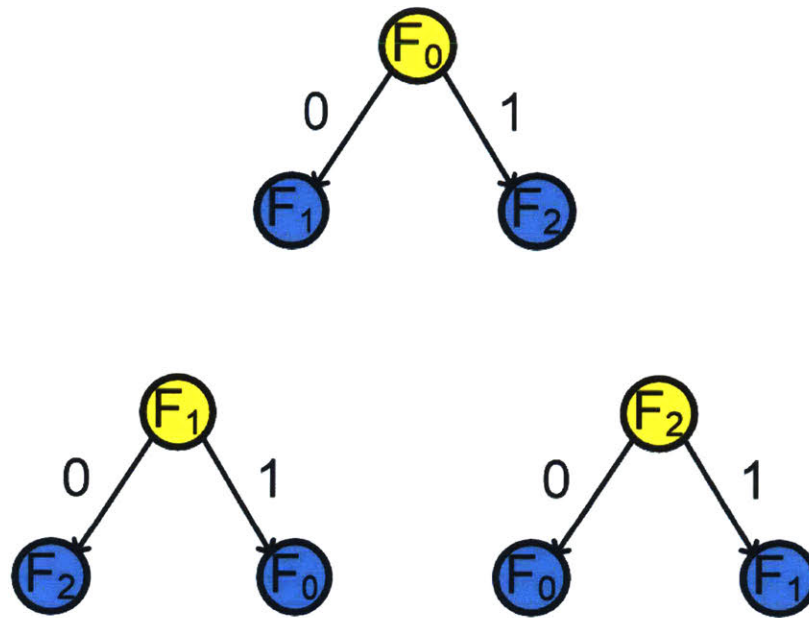
Figure 4-6: An AFSK scheme with an arbitrary code-word relationship between the 3 symbols/frequencies.
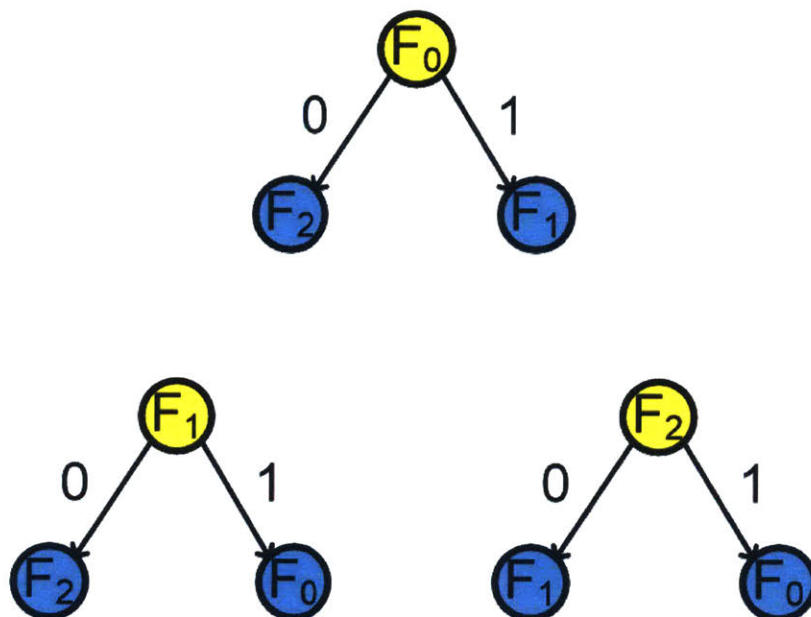
Figure 4-7: An AFSK scheme with the code-word relationship between the 3 symbols/frequencies optimized to send the codeword '0' quickly.

90

4.4 Symbol Transitions

It is near, if not, impossible to transition instantaneously from one symbol to another. Worse, oftentimes when transitioning from one symbol to another, a third valid symbol may be sent for a finite amount of time. If the communication scheme is not set up properly it is possible to have data errors because of symbol transitions. Symbol transition errors happen because in asynchronous communication a codeword is valid when there is a symbol transition, and if during the transition between two purposefully sent symbols a third symbol was sent while transitioning, there would be no way for the receiver know that the extra symbol sent while transitioning was not meant to be sent. To the receiver every symbol received, regardless when that symbol was sent, is valid

As a demonstration of this effect consider the asynchronous amplitude shift keying (AASK) communication signal found in figure 4-8. Here there are three valid voltage levels, V_0 shown in red, V_1 shown in green, and V_2 shown in blue. With the time scale in figure 4-8 it appears as if the transition between these voltage levels is instantaneous. However we know that a real circuit would have some slew rate associated with changing the voltage. If the codeword associated between V_0 and V_2 wanted to be transmitted, this slewing would take the voltage through V_1, as seen in figure 4-9. If the slewing through V_1 was longer than the T_{det} for V_1, then in the process of trying to send the symbol stream $V_0 V_2$ there would be a symbol transition error, and the symbol stream would be $V_0 V_1 V_2$ instead of $V_0 V_2$.

A symbol transition error is not unique to AASK, but will be present in all forms of asynchronous digital communication. A solution to this problem is to design a system that ensures that the time of a transition T_{tran} is less than T_{det}. This will ensure that any unintentional symbol transitions through a valid symbol will not be detected by the receiver. An example of designing T_{det} to be greater than T_{tran} is found in chapter 5.
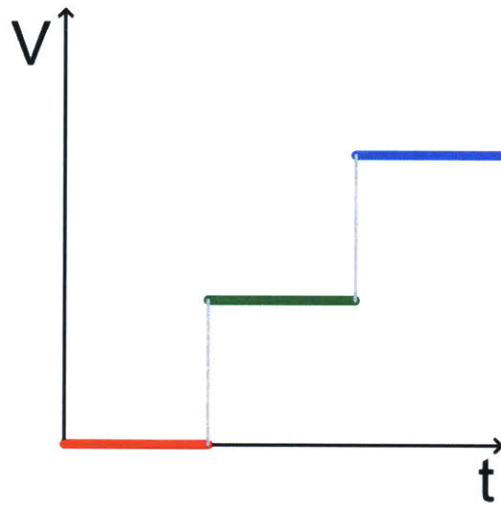
Figure 4-8: The three valid voltage levels of an AASK scheme.
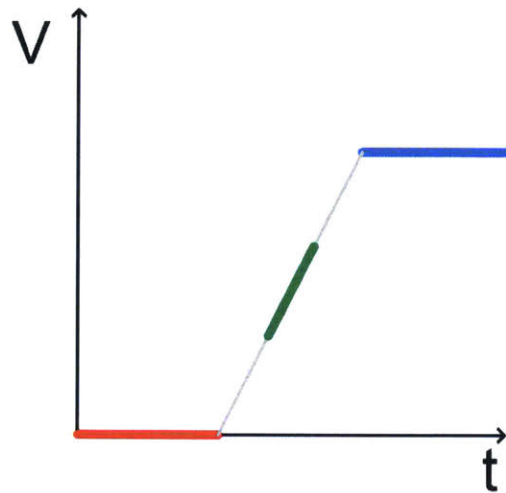
Figure 4-9: If a transmitter transitions from V_0 to V_2, it will have to slew through V_1. If the slewing voltage is in the region that will be recognized as V_1 long enough to be detected by the receiver, a symbol transition error will occur.

4.5 Baud Error Rate & Bit Error Rate

Baud error rate, also known as symbol error rate, is the probability that a transmitted symbol will be corrupted or changed such that the codeword received is not the same as the codeword that was transmitted. In traditional digital communication, the bit error rate is found by multiplying the baud error rate by how many bits are sent per symbol (or baud). In asynchronous digital communication calculating bit error rate from baud error rate is not as straight forward; indeed the relationship between the baud error rate and the bit error rate is so complicated that it isn't really valuable to consider the bit error rate.

With asynchronous digital communication there are the following categories of possible errors:

1. Detecting a symbol that was never sent

2. Not detecting a symbol that was sent

3. Misinterpreting the sent symbol

Each of these may cause one or more codeword errors. Take the error of detecting a symbol that was never sent. If the symbol data stream sent was $S_0 S_1 S_2$ but there was an error in the reception such that the received symbol data stream was $S_0 S_2 S_1 S_2$, there would be two codeword errors because there would be an error in decoding one codeword for the hop from S_0 to the erroneous S_2. In addition to this error there is an extra codeword for the hop from the erroneous S_2 to S_1. This idea of an additional codeword being sent because of a symbol error is not something we see in synchronous communication because a clock will only validate a set number of symbols in a given amount of time. In asynchronous communication there is no clock to say when a symbol hop is valid or not. This is one reason why it is not valuable to think of the bit error rate, as it is not well-correlated with the baud error rate. In the rest of this text BaudER will be used as meaning 'baud error rate'.

While doing baud or bit error correction on an asynchronous scheme is out of the scope of this work, it will be suggested that because of the additional erroneous codewords that can be decoded from the symbol stream, it is better to run error correction on the symbol

93

stream rather than doing error correction on the decoded bit stream. It also may be helpful to packetize transmitted data such that the receiver will know how many symbols it should have detected per packet.

4.6 Summary

This chapter started by explaining the difference between synchronous and asynchronous digital communication. A basic high level understanding of how to implement an asynchronous digital communication scheme was given. The chapter included how to take an existing synchronous communication scheme and enable it to be asynchronous by adding an additional symbol. It detailed the importance of having a start up symbol, how to optimize the data rate of asynchronous communication by not sending each symbol for the same time period. Further it showed how to choose the relationship of symbols to encode the most frequently used codewords to further increase the data rate for a given data patern.

The chapter concluded with some unique challenges asynchronous communication brings. These challenges include symbol transition errors and a bit error rate that does not have a linear relationship with the baud rate. The chapter also included ideas on how to overcome these challenges.

Chapter 5

Integrated Asynchronous Transmitter and Receiver

As stated in section 2.4.2, data encoded with phase and/or amplitude, and transmitted using BCC, will not be as robust as data encoded with frequency. Thus a type of asynchronous FSK (AFSK) was used in the integrated BCC transmitter and receiver. The AFSK scheme used is the same in figure 4-6, where $F_0 = 60$ MHz, $F_1 = 100$ MHz, and $F_2 = 150$ MHz, with F_2 being chosen as the start up symbol; F_2 was chosen as it is the highest frequency and therefore would have the lowest probability of being detected erroneously. This implementation will also require T_{det} to be one full cycle of the frequency being sent.

5.1 Transmitter

Recall that for a device to connect to the BCC channel, it must be close to the body. This requirement makes it difficult for one BAN using BCC, to interfere with another BCC BAN. The AFSK transmitter utilized this BCC channel property by transmitting the frequency symbols as square waves, because in this application the square wave's harmonics will not interfere with other BCC BANs. Transmitting square waves allows the transmitter to be quite simple and comprised of mostly digital logic.

The block diagram for the transmitter is shown in figure 5-1. The input reference frequency was 30 MHz. The PLL locks to 30 MHz when the output of the PLL is a
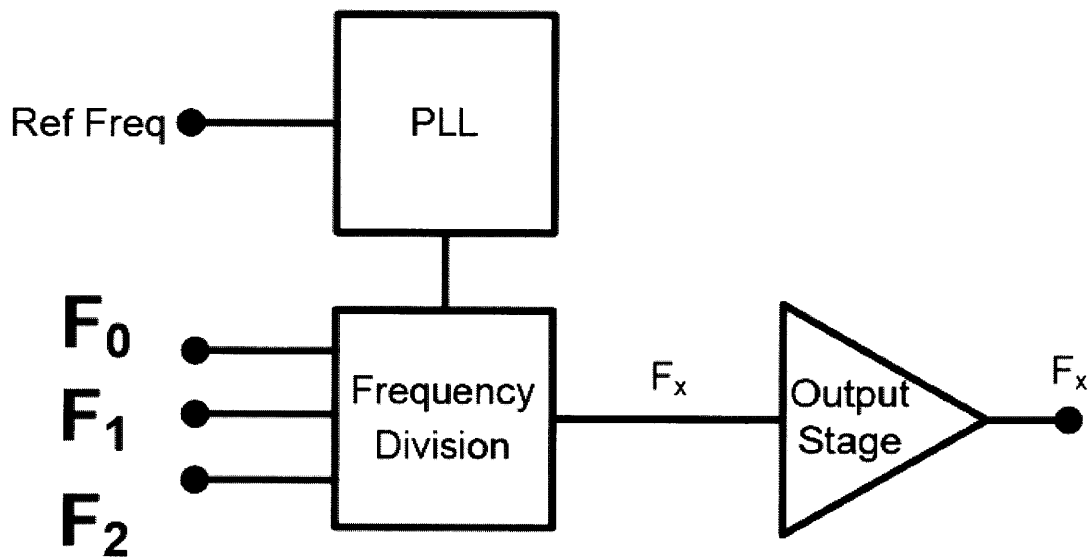
Figure 5-1: The block diagram of the AFSK transmitter.

600 MHz. The PLL was chosen to generate a 600 MHz clock as its factors include 150 MHz, 100 MHz, and 60 MHz — allowing the frequency divider to easily generate every symbol needed for the scheme. With this implementation, generating the "extra" frequency symbol for AFSK, as compared to FSK, was trivial. After the correct frequency is generated it is buffed by the output stage.

The transmitter's output, F_x, toggles from high to low at the appropriate frequency as dictated by the frequency divider. The frequency divider divides the 600 MHZ as determined by which input F_0, F_1, or F_2 is high. That is, if F_0 is high then the 600 MHz signal is divided by ten such that F_x will be toggled with a frequency of 60 MHz.

While 300 MHz also has factors that include 150 MHz, 100 MHz, and 60 MHz — a 600 MHz clock was chosen to prevent symbol transition errors (see section 4.4). For this scheme each frequency takes one complete cycle to be detected. To prevent symbol transition errors, the transmitter was designed to ensure that the output, F_x will not have two consecutive toggle periods that correspond to an erroneous frequency. For any given frequency, the toggle period is half the period of the frequency. By having the clock be 600 MHz we have control over one half the period of every frequency that needs to be generated, something that can't be achieved with a 300 MHz clock. As an example, if

F_0 is being asserted, then there should be 5 clock cycles of the 600 MHz clock between every toggle of the output to generate an output frequency of 60 MHz. If there have only been 3 clock cycles since the last toggle, when F_0 is deasserted and F_2 is asserted, then the output will toggle. This toggle has a period of 3 clock cycles which corresponds to F_1 (which is 100 MHz), and if the next toggle also has a period of 3 clock cycles then a symbol transition error will occur, as F_1 was never meant to be sent. But because F_2 is asserted now, the next toggle will only have a period of 2 clock cyles. By having control over the half period of every frequency in the scheme, symbol transition errors are avoided as an erroneous frequency will ever be sent for a full cycle.

5.1.1 Transmitter Results

To test the integrated transmitter, the control inputs F_0, F_1, and F_2 were toggled in a sequence to test every frequency transition possible. The transitions from not sending any frequency to sending a frequency, and from sending a frequency to not sending any frequency, were also tested. Each frequency was transmitted for 33.3 ns, which equates to a data rate of 30 Mbps. The output of the transmitter sending every frequency transition can be seen in figure 5-2.
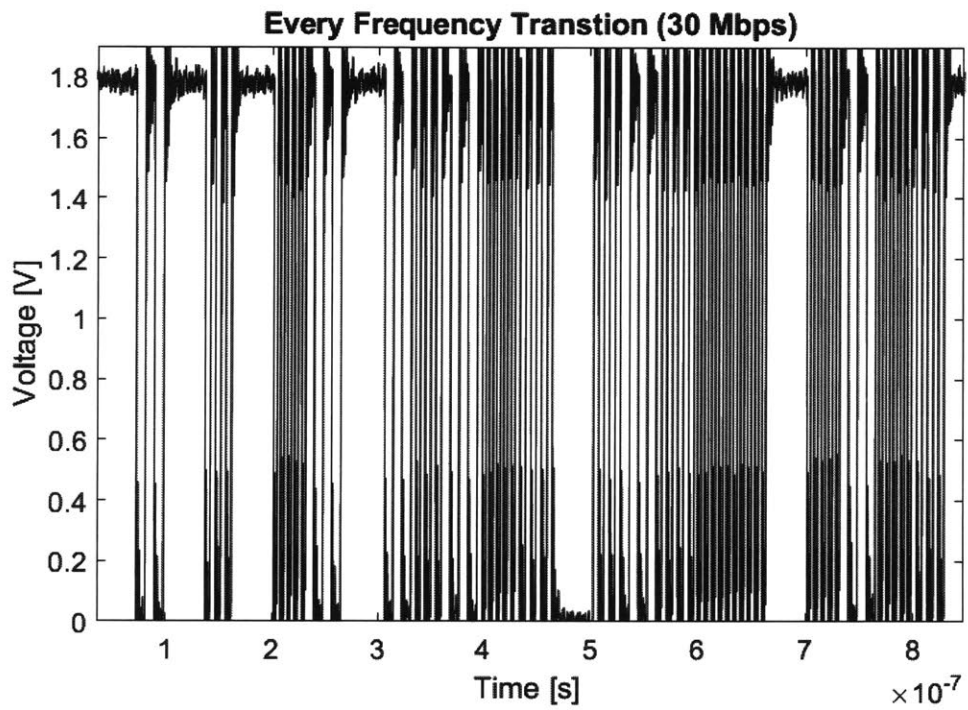
Figure 5-2: The transmitter sending every possible transition. The pattern that was sent was n0n1n20n01021n10122n2021, where 'n' is no frequency and 0 is F_0 etc.

The power used in the transmitter can be divided into two parts: the power for the frequency generation (which includes the PLL and frequency divider from figure 5-1), and the power for the output stage. Because the output of the transmitter is a digital square wave, the output amplifier doesn't need to be anything more than an inverter. Though to save power the inverter should use a break-before-make implementation, so as to avoid wasting power in shoot through current. The lower bound for the output power will be:

$$P_{Output} = \frac{1}{2}CV^2f \tag{5.1}$$

Where C is the capacitance the output has to drive, f is the frequency of the output, and V is the amplitude of the output voltage. The output power equation assumes that the resistance of the body's conductive tissue is negligible, so that the output only has to drive a capacitive load.

To further develop the theoretical minimum amount of power the output stage has to draw, assume that the only capacitance being driven by the output stage is the capacitive links the transmitter makes with the body. This simplification removes any parasitic capacitance in the packaging of the transmitter and the traces on the printed circuit board. The electrodes used in this work each make a capacitive link with the body measuring 10 pF. The transmitter drives two such links that are in series, yielding a total capacitance of 5 pF. Using equation 5.1, the amount of power required for the transmitter's output to drive 5 pF, assuming that the three frequencies (60, 100, and 150 MHz) are each driven one third of the time, is shown in table 5.1. The table has two calculations for the theoretical power needed: one for the output driving an amplitude of 1.8 V, and one for driving an amplitude of 1 V.

Table 5.1: Transmitter Power Consumed for a Data Rate of 30 Mbps

Parameter	Measured Result
Theoretical minimum output (1.8 V Square Wave)	837 μW
Theoretical minimum output (1 V Square Wave)	258 μW
Integrated frequency generation (1.3V supply)	897 μW
Integrated non-optomized output stage (1.8 V Square Wave)	3.42 mW

Table 5.1 also shows how much power the fabricated transmitter's frequency generation

circuit consumed (when operated with a 1.3V supply), and how much power the transmitter's output stage consumed. The power consumption was measured while sending data at 30 Mbps. Attention should be brought to the fact that the frequency generation power of the integrated transmitter, is close to the theoretical minimum power needed for the transmitter to drive the capacitive links with an amplitude of 1.8 V. This comparison shows that if the desired transmission output voltage is 1.8 V, any further optimization to lower the power of the frequency generation will never cut the total power consumed by the transmitter by more than half.

The power was also measured for the transmitter's output stage and is shown in table 5.1. The output stage was not optimized in any way and was implemented with progressively larger inverters to be able to drive the output. This design decision was made because such optimization of the output stage wasn't needed show how low the frequency generation power could be. The design of efficient digital I/O is well known and can be found, in part, in [22].

One of the most important figures of merit (FOM) for a low power communication system, is the number of joules it takes to send one bit of information. This is calculated by dividing the power it takes to operate the device by the data rate.

$$FOM = \frac{Power}{Data\ Rate}$$

Using the data rate of 30 Mbps, the FOM was calculated for the values in table 5.1 and is shown in table 5.2. The total power consumed for the integrated transmitter was 4.32 mW, yielding an FOM of 144 pJ/bit. This FOM could of course be better with an optimized power output, but even an FOM of 144 pJ/bit is very good when compared with the transceivers found in figure 1-2.

Table 5.2: Transmitter FOM for a Data Rate of 30 Mbps

FOM theoretical minimum output (1.8 V Square Wave)	27.9 pJ/bit
FOM theoretical minimum output (1 V Square Wave)	8.6 pJ/bit
FOM integrated frequency generation (1.3V supply)	29.9 pJ/bit
FOM integrated non-optomized output stage (1.8 V Square Wave)	114 pJ/bit

100
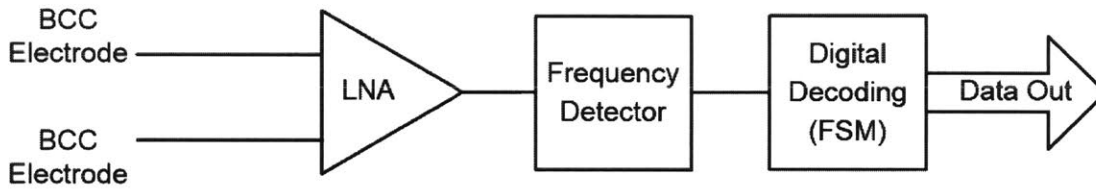
Figure 5-3: The block diagram of the AFSK receiver.

5.2 Receiver

In section 4.3 a very high-level design for an asynchronous digital communication receiver was given. This section will discuss the tradeoffs of designing an AFSK receiver, and design choices made in the integrated receiver that was fabricated in a 180 nm TSMC process. A generic high-level block diagram is shown in figure 5-3 and includes a low-noise amplifier, a frequency detector, and an FSM[1].

5.2.1 Frequency Detection

The receiver needs to be able to detect all the symbols, in this case frequencies, that are part of the communication scheme. Three ways to detect frequency were considered for this design (see figure 5-4): passive filtering, digital filtering, and counting. Passive filtering has a big benefit of using little power consumption in detecting frequency; power is only used in comparing the output of the passive filters to determine which filter output has appreciable power to say that frequency is being detected. Despite this advantage, in this design, passive filtering wasn't used. The frequencies that need to be detected were very close together on the log-scale, such that precise high-order filtering would have needed to be used, and wasn't practical on an integrated chip.

Digital filtering has the benefit of being robust and straight-forward to implement. An added bonus is that the frequencies are spaced out enough that a 1-bit precision digital filter is all that would be needed. Correlation filters are the least complex and work great as shown in [23]. However it was found that in simulation the 180 nm process could not do the

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[1]The FIFO is omitted here as it is not necessary for receiving and decoding bits, and wasn't implemented on the integrated receiver. The FIFO was implemented off chip.
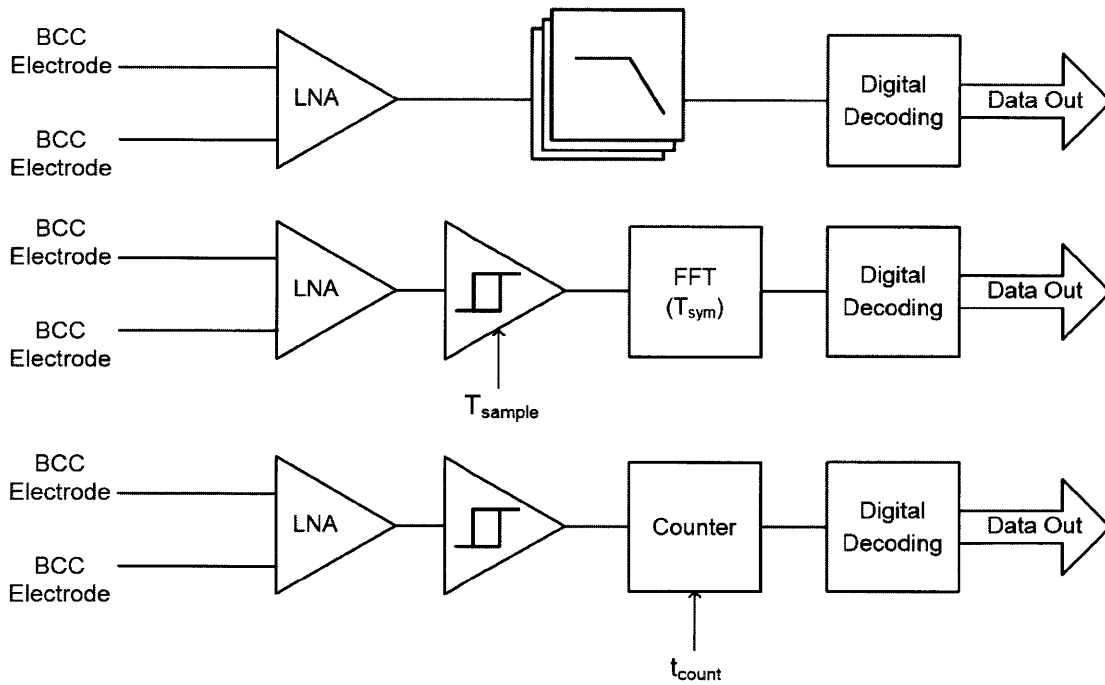
Figure 5-4: Three ways in which to detect a frequency. 1) Passive Filter 2) FFT/Digital Filter/Corrilation Filter 3) Counting

computation fast enough to have a comparable data rate to counting. Thus this integrated circuit used counting to detect the different frequencies.

5.2.2 Frequency Detection using Counting

In the general case of using counting to determine a frequency it is important to digitize the input frequency. This will make a square wave at the same frequency with nice sharp edges that can be used to control digital logic. The now digitized input frequency is then used to create a count period. The count period will be a function of the input frequencies period:

$$T_{count} = c * \frac{1}{F_x}$$

where T_{count} is the count period and F_x is the input frequency. The values of c must be $(1/2) * n$, where n is a positive whole number. The values of c are limited to these numbers because c must be forced to correspond with the rising and falling edges of the input frequency, as the edges are the only events that can be used in the digital logic.

102

Once a count period is generated, a clock is used to increment a counter. At the end of the count period, the count on the counter will then be a function of the clock's frequency and the count period. The choice of how fast the clock is and the length of the count period (or how many half-cycles of the input frequency are counted over) will determine the precision of the frequency detection.

For the integrated receiver to function properly with the integrated transmitter there are two constraints:

1. Determine the difference between the three frequencies — 60 MHz, 100 MHz, and 150 MHz.

2. Have a detection T_{det} time of one cycle for each frequency.

Constraint 1 sets the precision needed for the frequency detection. Constraint 2 limits the count period for the frequency detection. From these constraints the clock frequency for the counter can be determined.

From the design of the transmitter in section 5.1 we know that up to half a cycle of the incoming signal may be erroneous due to symbol transitions. This, along with constraint 2, requires a count period of half a cycle for each incoming signal. Constraint 1 requires that each count period for the three frequencies have a unique count, and will set the counter's clock frequency. To determine what the count could be for each count period consider figure 5-5 where the count period is not a factor of the clock's period. The figure shows how the phase of the clock in relation to the phase of the count period can affect the count. The count is the number of rising edges of the clock over the counter period. Depending on the phase relation between the clock and the count period, the number of rising edges of the clock that overlap with the count period can either be the ceiling or floor of the ratio of the counter's clock and the count period.

$$Count_{nonFactor} = \left\{ \left\lfloor \frac{T_{count}}{T_{clock}} \right\rfloor, \left\lceil \frac{T_{count}}{T_{clock}} \right\rceil \right\} \tag{5.2}$$

Figure 5-6 depicts a scenario where the count period is a factor of the clock's period. With zero phase difference between the count period and clock's period a rising edge of the

103
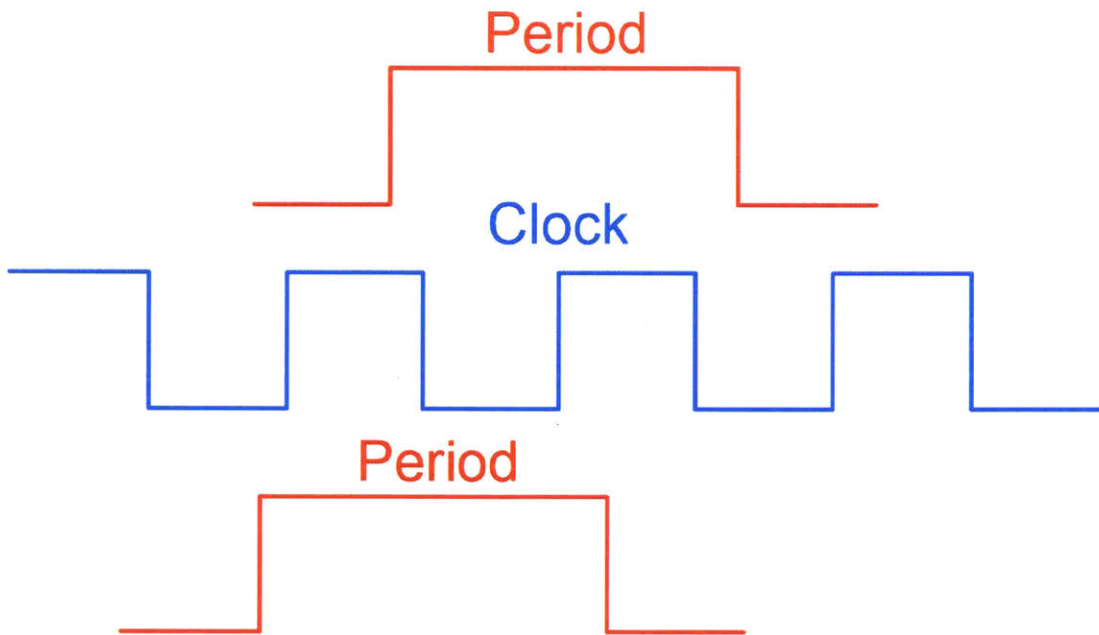
Figure 5-5: Possible counts when the counter's period is not a factor of the count period.

clock can be at the same time the count period starts and ends. The philosophical debate of whether the counter should be incremented at the start, end, or both, of the counter period is meaningless as the hardware will determine whether or not the counter increments or not. The implementation of the counter will most likely be some sort of flip-flop and as such the set up and hold times of the device will matter. As it is not a robust design to have a dependency on set up and hold times[2], it is best to allow all scenarios of the final count be valid for that frequency, thus when the count period is a factor of the clock's period, the possible counts will be:

$$Count_{Factor} = \left\{ \left\lfloor \frac{T_{count}}{T_{clock}} - 1 \right\rfloor, \frac{T_{count}}{T_{clock}}, \left\lfloor \frac{T_{count}}{T_{clock}} + 1 \right\rfloor \right\}$$ (5.3)

5.2.3 Integrated Circuit Counter

The block diagram for the integrated counter can be seen in figure 5-7. The input to the counter-based frequency detection is a square-wave at the frequency which needs to be

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[2]It should be mentioned that any ratio that is close to a whole number, can have the same problems with set up and hold time, and the same solution should be implemented.
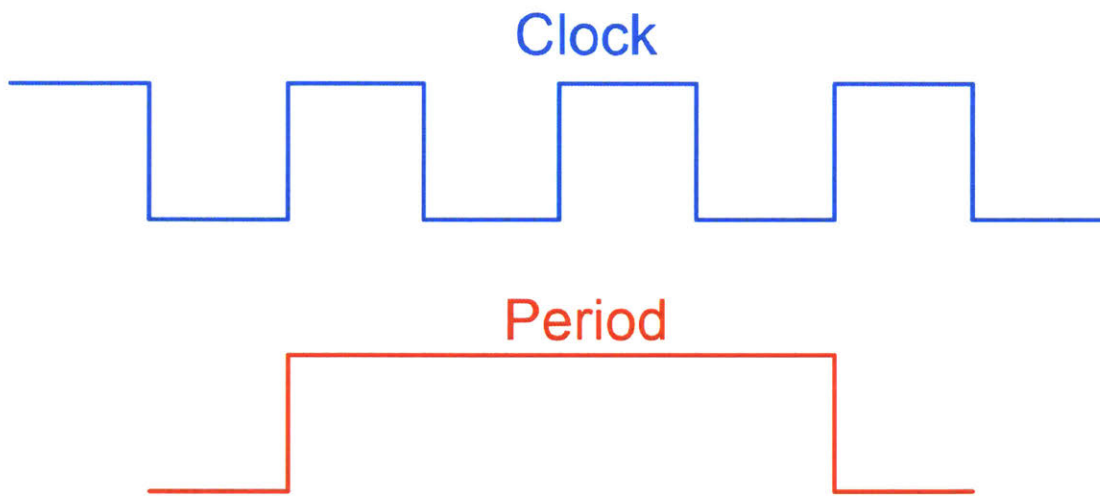
Figure 5-6: Possible counts when the counter's period is not a factor of the count period.

detected with a 50% duty cycle. The counter generates a count for how long the input is high, and generates a count for how long the input is low. If the high-count and the low-count correspond with the same frequency, then the output for that frequency is brought high, denoting that the frequency has been detected. By counting the high count and the low count, each being a half a cycle of the input, the circuit is able to fulfill both constraints found in 5.2.2.

The integrated circuit uses a counter that increments with a frequency of 840 MHz. Using equations 5.2 and 5.3, the three frequencies needing to be detected will have the following possible counts, over the count period which is half of each respective cycle.

$$150\,\mathrm{MHz} = \{1, 2\}$$

$$100\,\mathrm{MHz} = \{3, 4\}$$

$$60\,\mathrm{MHz} = \{5, 6, 7\}$$

5.2.4   Analog Front End

The analog front end (AFE) will need to amplify an incoming signal and condition it to meet the requirements of the frequency detector. The minimum amount of gain the ampli-

105
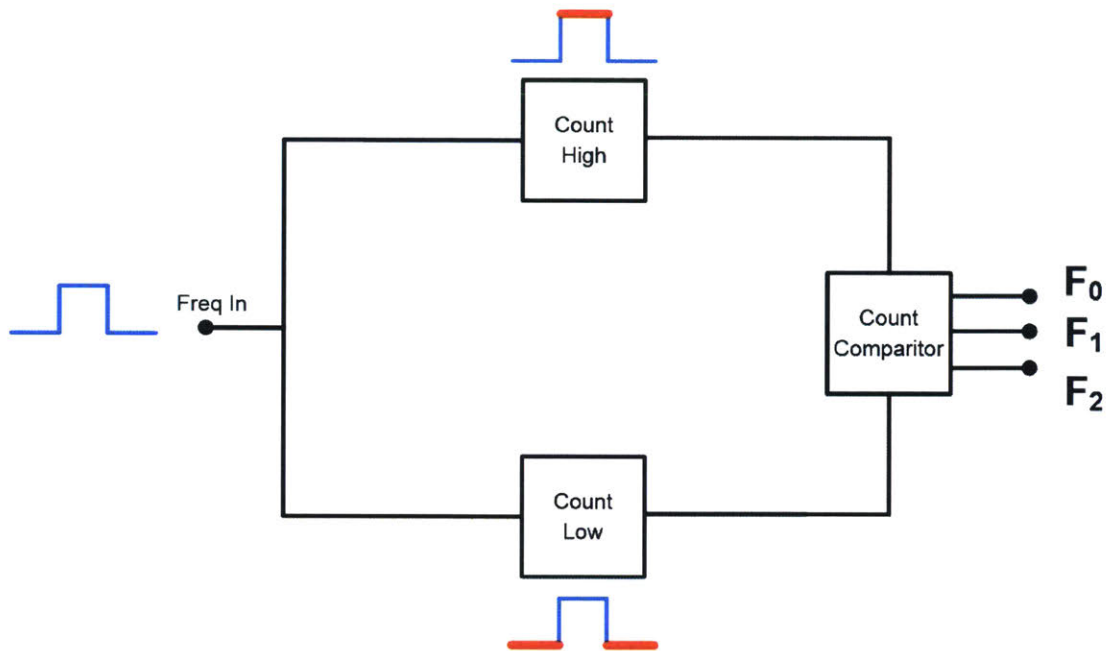
Figure 5-7: Block diagram of integrated counter.

fier will need will depend on signal voltage generated by the transmitter, and the amount of attenuation in the channel. In many receivers and communication schemes there is a constraint on the gain to prevent the recovered signal from clipping. In this system the input to the frequency detector is a square-wave of the input frequency. This is the same as saying it is a digitized version of the frequency; which means that it doesn't matter if the amplifiers clip the signal, because it will be digitized anyway to condition the signal for the frequency detector. Because we don't need to worry about clipping the signal while amplifying, there is no maximum gain requirement and a variable gain amplifier is not needed.

After the amplification the signal will need to be conditioned to fit the input for the counter. The counter expects a square wave with fast transitions to run the digital logic. Thus the amplified signal is passed through a comparator to digitize the signal. The comparator is basically acting like a 1-bit ADC. If there is enough noise on the input of a comparator, then when the signals input is near the switching point of the comparator, the output of the comparator can switch states a few times due to this noise. To avoid this, a schmidt trigger can be used.

The integrated analog front end's block diagram can be seen in figure 5-8. The low-
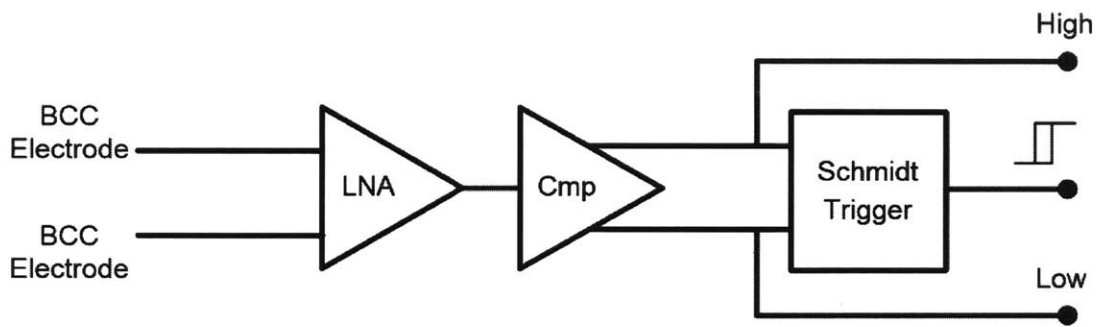
Figure 5-8: Receiver's analog front end.

noise amplifier stage is made up of four common source amplifiers. Each stage has about 20 dB of gain, giving the entire amplification block around 80 dB of gain. As the BCC channel can have upwards of 80 dB of attenuation, as shown in section 2.4, this will allow the recovery of the original signal sent. If a transmitter is generating its transmission with a 1–2 V swing, this would mean a receiver needs to be able to detect a 100–200 μV swing. To ensure a good signal to noise ratio the integrated AFE has an input refereed noise of less than 30 μV$_{rms}$. The integrated AFE has two comparators, one with an nMOS input, one with a pMOS, these comparators feed some digital logic. Using two comparators with complementary inputs allow for a high input dynamic range, and the digital logic allows the two comparators outputs to act like a schmidt trigger.

Common source amplifiers were used, because for a given amount of power and bandwidth, they have the lowest amount of input referred voltage noise. Because we don't have to worry about saturation, precise gain is not needed, which allows us run the amplification open loop; meaning the amplifier stages can just be cascaded together. The circuit used for the common source amplifier can be seen in figure 5-9. Each amplifier's input is capacitively coupled, creating a high pass filter, while its output is low pass filtered and fed back to the input. At low frequencies there is no input due to the high-pass filter, and the amplifier is essentially a diode-connected transistor which allows each transistor to be self biased based on the pMOS current source transistor. The high-pass filter also helps to cut out unwanted noise/interferers at lower frequencies. The low-pass cutoff of the common source amplifiers is a function of the load capacitance and the bias current. Four of these amplifiers, cascaded, make up the amplifier.

107
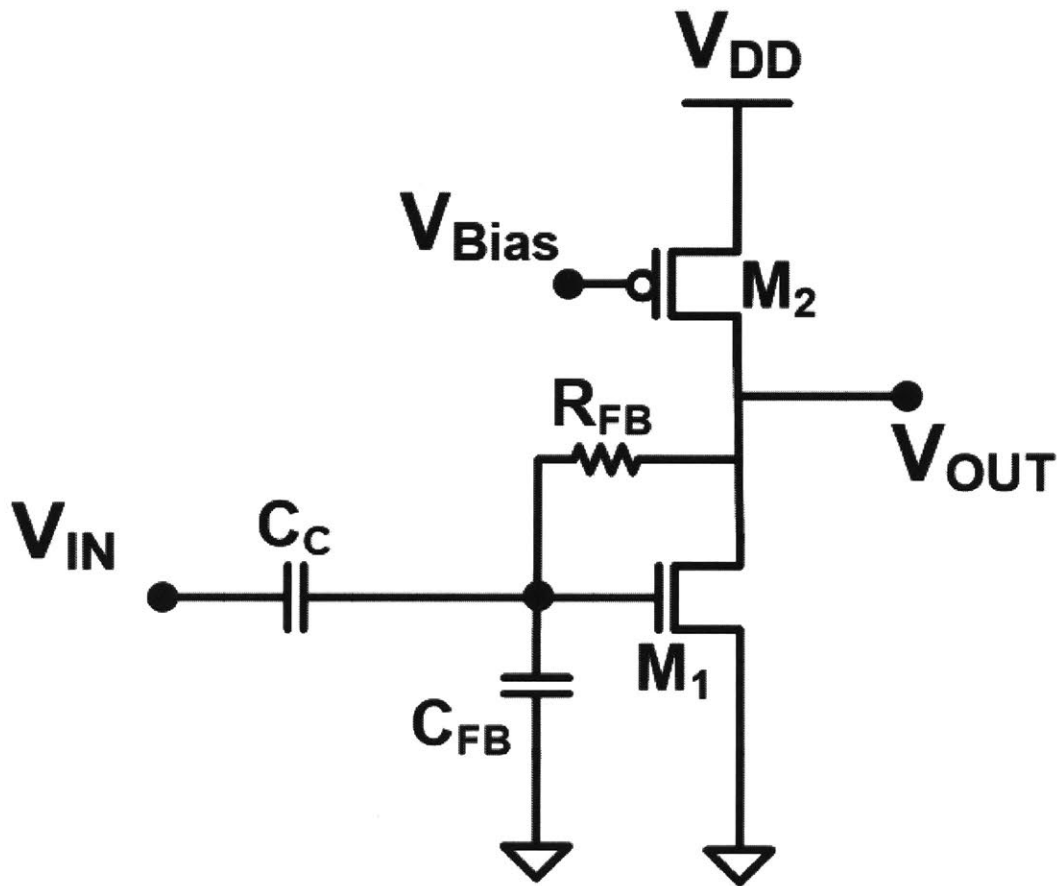
Figure 5-9: Common source amplifier as used in receiver's LNA.

5.2.5 Full Integrated Receiver

The block diagram for the integrated receiver can be seen in figure 5-10. It consists of the amplifier and a high and low comparator as discussed in section 5.2.4. For testing purpose there is some digital logic so that the AFE can feed the frequency detection block either: the schmidt trigger output, the high comparator output only, the low comparator output only, or an off chip signal.

Figure 5-10: The full integrated receiver's block diagram.
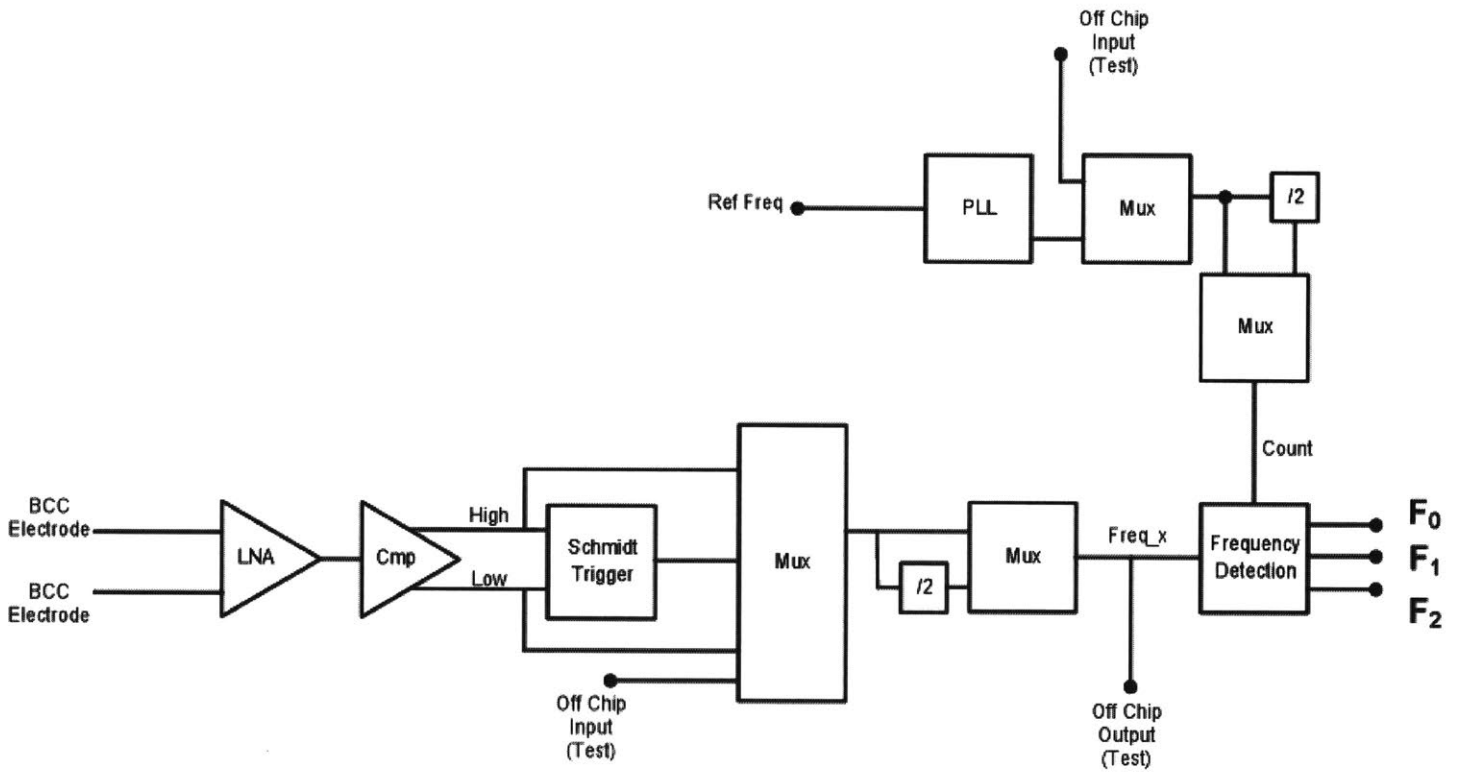
The frequency detector is supported by a PLL to generate the clock for the counter. For testing purpose an off chip counter clock can be utilized instead of the on chip PLL. Note in figure 5-10 the divide by two blocks that appear both after the AFE and the PLL. By dividing both the counter's clock and the input by two, the logic will produce the same count for each frequency as both the count period (coming from the AFE) and the counter (coming from the PLL) will be scaled by the same amount. The divide by two circuit allows for a more robust circuit in two ways. First, the timing requirements for the frequency detector digital logic are relaxed as the fastest frequency, the counter's clock, would run at half the speed. Second, if the output of the AFE does not have a 50% duty cycle, then the output after the divider will have a 50% duty cycle, though the signal will have half the frequency, as illustrated in figure 5-11.

Input 1
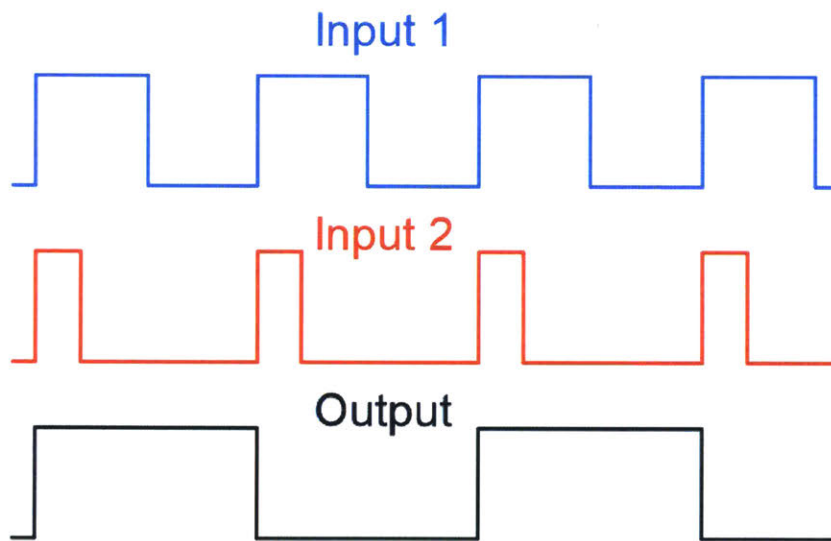
Input 2

Output

Figure 5-11: The output of the frequency divider (black), will be a 50% duty cycle at 1/2 the frequency of the input.

The outputs of the receiver are three lines, each representing one of the frequencies being transmitted. When the frequency detector identifies one of these frequencies, that frequency's respective line is brought high, as shown in figure 5-12.
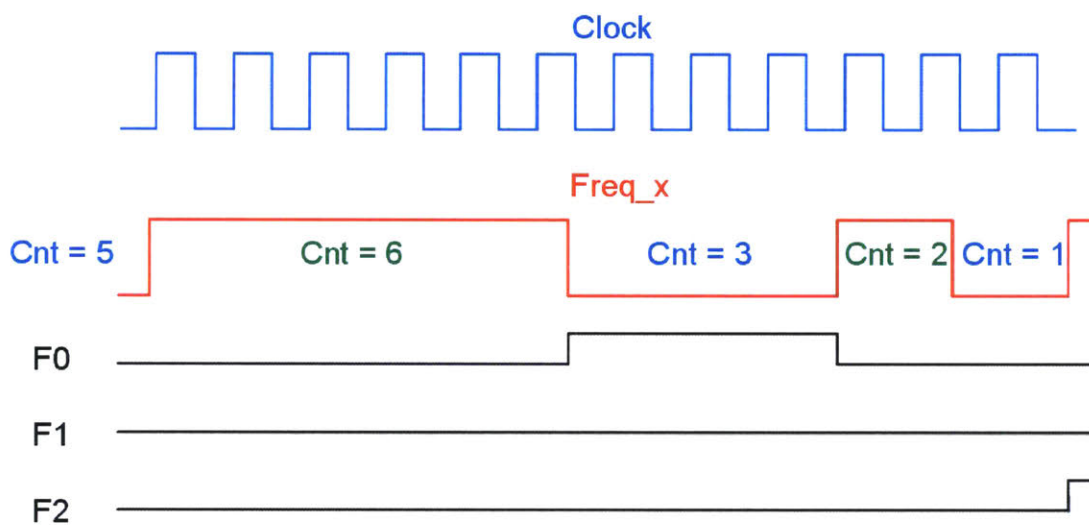
Figure 5-12: Diagram of when the receiver detects a valid frequency. There are two count registers, one stores the count when the input frequency was high (green) and one when it was low (blue). The clock's rising edge increments the counter during the respective phase. When both count registers correlate with the same frequency as found in section 5.2.3, the corresponding 'frequency detected' line will be brought high.

111

Table 5.3: BCC Integrated Receiver Performance

Parameter	Measured Result
Amplifier Power	2.8 mW
Comparator Power	72 μW
Frequency Detector Power	3 mW
Total Power	5.9 mW
Figure of Merit	367 pJ/bit

5.2.6 Receiver Measured Results

The power of the integrated receiver was measured. It was found that the amplifiers drew 2.8 mA of current while being powered by 1 V rails. The comparators drew 40 μA at 1.8 V. And the frequency detector, including the PLL, drew 1.67 mA at 1.8V. This means the total power being drawn by the receiver during operation was 5.9 mW. The data rate while drawing this much power was 16 Mbps. This yields an FOM of 367 pJ/bit. This data is summarized in table 5.3

The baud error rate (BaudER) was also measured during operation. While it is typical in communication systems to display the BaudER as a function of received power, it doesn't makes sense to do this in BCC. In typical radio communication systems the input impedance of the amplifier is 50 Ω, to match the output impedance of an antenna. Because there is a standardized input impedance using power as the specification for BaudER has meaning. With BCC there is no reason to match the input impedance with the output impedance of the channel. In fact in section 2.4 it was shown that the input impedance of the amplifier loads the system, so a larger input impedance would be valuable. Because there isn't a standard input impedance for BCC amplifiers, it doesn't make sense to use input power the variable for BaudER without also giving the input impedance of the amplifier. It makes more sense to plot the BaudER verse the input voltage of the amplifier. Figure 5-13 shows the BaudER vs the input voltage for this system. Because the system is asynchronous it should be said that the BaudER was measured when the symbol length for every symbol was 62.5 ns, which equates to 16 Mbps.

While the integrated receiver was functional, the receiver didn't function as well as hoped when it was designed. Particularly the high gain in the LNA was a source of prob-
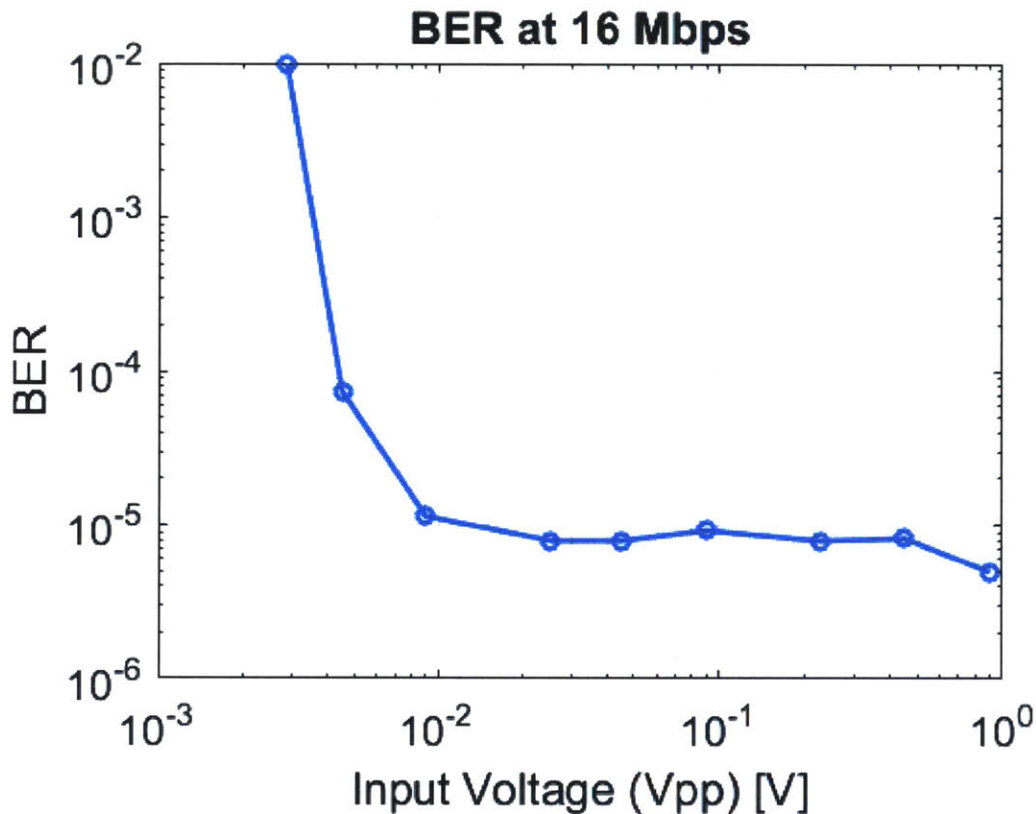
Figure 5-13: The BaudER for the AFSK receiver.

lems. If redesigned the gain should be dropped by at least 20 dB, which should still provide enough signal for the comparators when the received signal is at its minimum of 100 μV. Furthermore the receiver should be implemented in a smaller process node. Getting good analog gain at 150 MHz, with low input referred noise, used a significant amount of power in the LNA in the 180 nm process. Going to a smaller node would allow faster and higher gain amplifiers with lower power. At the same time the smaller processing node would allow for faster logic at lower power points, ideally the counting method to detect frequency could be replaced with correlation filters. The correlation filters will be more robust in detecting frequencies than the counting method and decrease the bit error rate. Designing a receiver in a smaller process node with less amplification and a correlation filter for frequency detection, could easily get the receiver power dissipation down to 3 mW, and possibly down to 1 mW, while achieving a data rate of 30-90 Mbps. This would put the FOM at 100 pJ/bit or lower.

However as is, this receiver is very competitive with Bluetooth low energy (BTLE) which typically has 8 mW of power consumption with a 1 Mbps data rate yielding an FOM of 8 nJ/bit, which is over 10x higher than this BCC receiver.

5.3 Transmitter and Receiver Performance Comparison

This works transmitter and receiver designs are comprised of analog circuits that scale well, and digital logic. As these circuits were designed in a 180 nm process, moving to a smaller processing technology would dramatically reduce the power consumption of both the transmitter and the receiver. A comparison of the FOM performance of both the transmitter and receiver, in relation to those found in figure 1-2, can be found in figure 5-14. It should be noted when comparing BCC transmitters and receivers to be aware of what is being reported. As an example receiver sensitivity is often reported in 'dBm'. In RF communications 'dBm' is a perfectly good way to report the sensitivity as all inputs are 50 Ω. But in BCC where the input resistance does not have to be 50 Ω, reporting the sensitivity in 'dBm' without also reporting the input resistance does not provide enough information to deduce the actual voltage sensitivity the receiver provides.
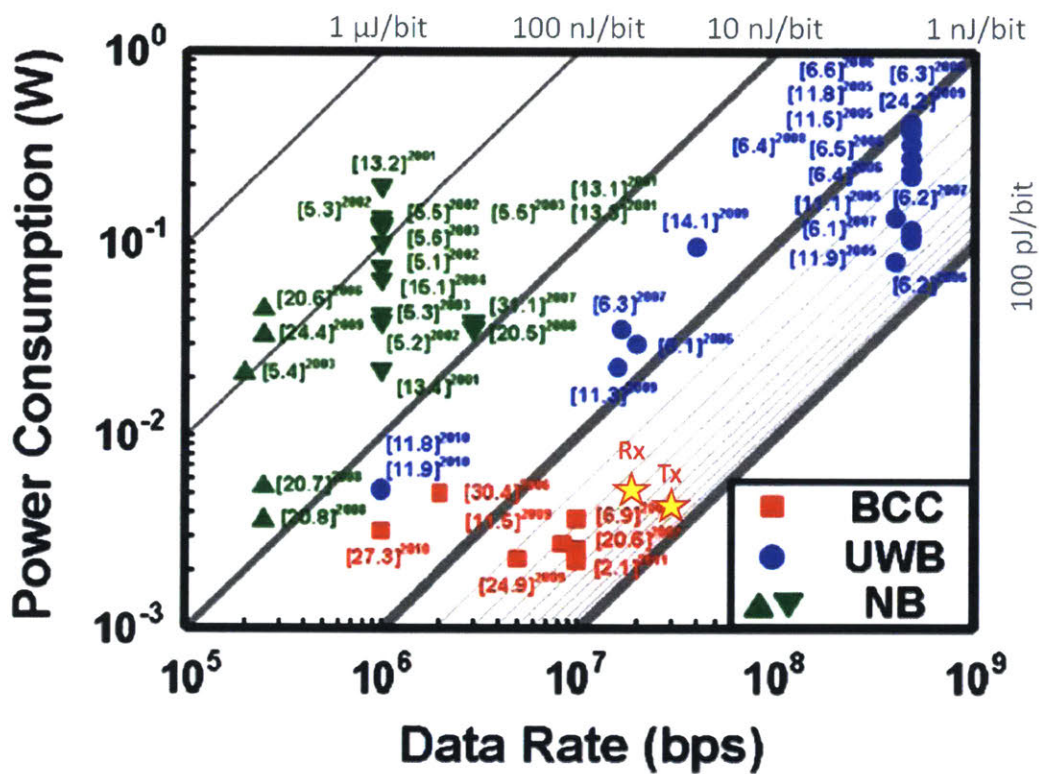
Figure 5-14: This work's transmitter and receiver performance (the respective stars) as compared to figure 1-2.

5.4 Summary

This chapter took the asynchronous communication scheme discussed in chapter 4 and detailed the design decisions in implementing an ASFK scheme in an integrated transmitter and receiver. The section on the transmitter included how symbol transition errors were eliminated and gave the power measurements of the transmitter. The FOM for the transmitter was very competitive. It was shown that further optimization of the power used in generating the frequency, can at most, only result in reducing the total power used in the transmitter by half; as the power to generate frequencies is on par with the theoretical minimum power needed to transmit the frequencies into the body.

The design of the receiver included a section on different ways to detect frequencies. While correlation filters may be the most robust way to detect frequencies on an integrated circuit, a counting solution was determined to be best in the 180 nm fabrication process used. The pitfalls in using counting to determine frequencies were discussed and it was shown how the circuit design overcame them. The section on the receiver design also covered the design of the analog front end of integrated receiver, and suggested that if made again the total gain in the AFE should be reduced; as the total gain was so high that the small parasitic capacitances that couple the output of the amplifier to the input caused oscillations. The full receiver chip was explained and the measured results of the BaudER and the power specs were given.

Chapter 6

Conclusion

A body area network is simply a network for devices on a human body. The main motivation for BANs comes from the fact that certain sensors need to be in areas of the body where a large form factor cannot be tolerated. Thus the battery size, and therefore the power, of these nodes needs to be minimized. Often the highest power consumption comes from storing acquired data to memory or transmitting it off the body. By providing a BAN with a base station on an area of the body that can support the larger form factor, the small sensor nodes can transmit their data to the base station instead of storing it to memory or transmitting it off the body. For a BAN to be successful the power used by the sensor node to send data to the base station must be smaller than the power it would have used to store the data to local memory, or the power used to send the data off the body.

Using body coupled communication is a very promising way to form a BAN, because there is little interference between BCC BANS. This property allows for higher security in the physical layer and for each BCC BAN to use large bandwidths to send information which can lead to large data rates. This thesis made three main contributions in the development of BCC.

The first contribution made to BCC was an accurate and carefully verified model of the BCC channel. Chapter 2 showed the importance of using battery powered, and electrically isolated, measurement equipment when performing BCC channel measurements. The chapter covered the design of custom measurement equipment that met these requirements. With this equipment it was shown that the dominant current path for BCC is through the

body, and that little current is transmitted through the environment. Because the body is the dominant path, the chapter explains how the body acts as a spreading resistance and verifies this model through careful measurements. The end result is a model for the BCC channel, where the body is a spreading resistance and the transmitter and receiver make capacitive links that couple into the spreading resistance. Further it was shown that instead of capacitively coupling into the spreading resistance, a node may galvanically connect to the spreading resistance. Being able to galvanically connect to the BCC channel means implanted devices may use a BCC BAN.

The second contribution was discussed in chapter 3. This chapter showed how buffering the input of the receiver and feeding it back into the body increases the gain in the channel. This technique was termed body buffered return, or BBR. By creating a virtual short between the receiver's electrodes, the BBR technique is able to decouple the amount of current entering the receiver and the value of the input impedance of the receiver. Thus by increasing the input impedance of the receiver the gain of the channel will increase, and the signal to interferer ratio (as compared to traditional receiver amplifiers) will increase. The chapter detailed multiple ways to implement BBR, including using differential amplifiers. The chapter ends by showing how a source-follower can be used to implement the BBR technique.

The third contribution was the development of asynchronous digital communication. This contribution utilizes the large bandwidth inherent in BCC. By transmitting data asynchronously the transmitter and the receiver can do away with synchronization circuitry. Asynchronous communication works by encoding codewords as the relationship between symbols, instead of in the symbol itself, as explained in chapter 4. This chapter explains the key difference between synchronous and asynchronous digital communication. The chapter also provides the framework to take an existing synchronous scheme and make it asynchronous. In addition, the chapter warns of potential problems, such as symbol transition errors, that are unique to asynchronous communication and explains how to design an asynchronous communication system around them.

The three contributions were integral in making the integrated BCC transmitter and receiver that is detailed in chapter 5. This chapter expands the teachings of chapter 4 as

118

it details how the design of an integrated transmitter and receiver overcame the potential pitfalls of implementing asynchronous digital communication. The chapter shows the operation of data communication of both the transmitter and receiver and their power dissipation measurements. It was found that the transmitter was able to transmit data asynchronously at 30 Mbps while drawing 4.32 mW. The receiver was able to receive data asynchronously at 16 Mbps while drawing 5.9 mW. The integrated transmitter and receiver embody the three contributions to BCC, and indeed show the viability of BBR and AFSK.

6.1 This Work's Impact

One of the biggest impacts of this work is the BCC channel model from section 2.4, that was carefully measured and validated. This channel model lead to the discovery that implants can use BCC, and was validated with experiments on a pork loin. Implants using BCC are not limited to communication with other implanted nodes, but can be controlled by and communicate with nodes that are outside the body. Because implants can use BCC directly, a radio/BCC hybrid BAN, such as that proposed in [24], is no longer needed. Implants will be able to achieve the energy savings that BCC can achieve. The power savings for implants, like pace-makers, will be especially large as pace-makers currently have to power radio transmission through the Farady cage like cans that encase the electronics.

The energy savings BCC provides for systems are not trivial as illustrated in the following example. A custom integrated circuit designed to acquire ECG signals can be found in [25]. In this publication the integrated chip uses 1.2 nJ/bit to acquire ECG data. Storing the ECG data to an SD card takes 11 nJ/bit[1]. While sending the data to a base station using Bluetooth low energy (BTLE) takes at least[2] 8 nJ/bit. These performance numbers are summarized in table 6.1 and show that if an ECG system consisting of the integrated acquisition chip was combined with an SD card, then 90% of the system energy is being used for data storage. If Bluetooth is used to transmit the data of the node, then 88% of the energy used in the system would be going to Bluetooth. If instead the ECG system used the

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[1]if it is assumed that it runs with 100 mA at 3.3 V and has a write speed of 30 Mbps

[2]Considering the overhead BTLE requires, BTLE usually achieves 150 nJ/bit.

BCC transmitter (0.14 nJ/bit) from this work, then only 10% of the system energy would be used for data transmission. Using BCC instead of BTLE or an SD card gives a power savings of up to 10x! By using BCC, the batteries for such sensor nodes can be one-tenth the size while maintaining the same operation time, or maintain their current sizes while increasing the operation time by ten.

Table 6.1: The Energy-per-Bit Requirements for an ECG Recorder

ECG System Block	Energy-per-Bit
Integrated ECG Acquisition System	1.2 nJ/bit
Storing to SD card	> 11 nJ/bit
Using BTLE	> 8 nJ/bit
BCC Transmitter	0.144 nJ/bit
BCC Receiver	0.367 nJ/bit

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