Fabrication of a Nanoporous Membrane Device for High Heat Flux Evaporative Cooling

by

Jay D. Sircar

Submitted to the
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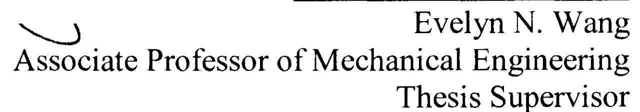
Certified by: 

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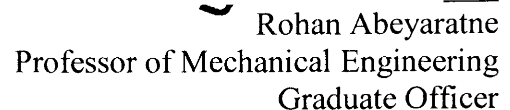
Accepted by: 

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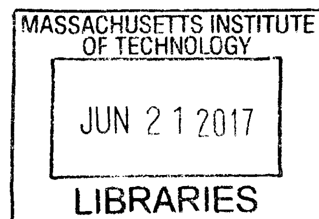

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Abstract

We investigated the experimental performance of a nanoporous membrane for ultra-high heat flux dissipation from high performance integrated circuits. The biporous evaporation device utilizes thermally-connected, mechanically-supported, high capillarity membranes that maximize thin film evaporation and high permeability liquid supply channels that allow for lower viscous pressure losses. The 600 nm thick membrane was fabricated on a silicon on insulator (SOI) wafer, fusion-bonded to a separate wafer with larger liquid channels. Spreading effects and overall device performance arising from non-uniform heating and evaporation of methanol was captured experimentally. Heat fluxes up to 412 W/cm^2, over an area of 0.4×5 mm, and with a temperature rise of 24.1 K from the heated substrate to ambient vapor, were obtained. These results are in good agreement with a high-fidelity, coupled fluid convection and solid conduction compact model, which was necessitated by computational feasibility, which incorporates non-equilibrium and sub-continuum effects at the liquid-vapor interface. This work provides a proof-of-concept demonstration of our biporous evaporation device. Simulations from the validated model, at optimized operating conditions and with improved working fluids, predict heat dissipation in excess of 1 kW/cm^2 with a device temperature rise below 30 K, for this scalable cooling approach.

Thesis Supervisor: Evelyn N. Wang
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Nomenclature

A	area, cm^2
P	pressure, MPa
T	temperature, °C or K
c_p	specific heat, J/kg·K
d	diameter, μm
h	heat transfer coefficient, W/cm^2K
k	thermal conductivity, W/m·K
l	length, μm
m	mass flow rate, kg/s
q''	heat flux, W/m^2
r	radius, nm
t	thickness, μm
w	width, μm

Greek symbols

α	permeability, $1/m^2$
γ	scaling factor, -
η_f	fin efficiency, -
μ	viscosity, Pa·s
ϕ	porosity, -

Subscript

c	capillary
i	interface
l	liquid
l	liquid channel
m	membrane
p	pore
r	ridge
rc	ridge channel
v	vapor
x	far-field, bulk

Chapter 1- Introduction

1.1 Background

At a given footprint, the number of transistors within integrated circuits (ICs) has increased six orders of magnitude over the last four decades, and the resulting power densities have continued to climb [1],[2]. The heat fluxes generated by these devices, particularly those in military-grade electronics operating at high power or high frequency, are expected to surpass 1 kW/cm^2 [3]. With the performance and longevity of ICs deteriorating at elevated temperatures, cutting-edge and future ICs require cooling strategies that can efficiently remove these heat fluxes without excessive heating [3].

Wide band-gap semiconductors, smaller linewidths features, thinner substrates, and higher dimensional architectures allow for continued device compaction and increased energy generation density [4], [5]. Semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN) have increased thermal conductivity, higher breakdown voltages, and lower on-state resistances [6]. Devices on these semiconductors can sustainably operate at higher temperatures and voltages. Leveraging these improved material properties, GaN components in such high electron mobility transistors (HEMT), allow for higher operating efficiencies. For high frequency/high power applications, such as wireless communications and radar, GaN devices have shown improved performance (faster clock speed and increased sensitivity), while reducing size, weight, and power (SWaP) by as much as 90% [7].

Moore's Law which pretty accurately predicted the exponential increase in transistor packing for four decades, has resulted in increased computational power [5]. Having nearly reached the limits of resolvable linewidths for components, recent computational performance improvements have taken advantage of multiple cores for parallel processing and architectures that integrate discrete semiconductor devices into a single system-on-chip. Next generation improvements will go even further with 3-dimesional architectures that shorten interconnect lengths through vertical integration in order to increase computation speeds and

power efficiencies. Compaction at this scale can quickly increase the power densities by an order of magnitude and magnify thermal gradients across devices, even as overall power efficiencies improve [7]. 3D stacked devices heat volumetrically and require novel cooling strategies [5].

The miniaturization and integration of disparate electronic components also magnify the non-uniformities in heat generation. Submillimeter regions at transistor junctions can reach fluxes as high as 1,000 $\mathrm{kW/cm^2}$, significantly more than the background heat flux, and the resulting temperatures, such as those adjacent to transistor gates, can exceed 300°C [8], [9]. Large thermal gradient across devices can result in further performance degradation and/or device failure. Leakage currents within a hot spot can create positive feedback in temperature and result in thermal runaway and device burnout [10]. Mismatches in coefficients of thermal expansion can lead to mechanical failure. GaN-based MMICs can also fail due to thermally induced-clock skew caused by local temperature changes reducing clock speeds at different rates. Conventional thermal management strategies provide uniform cooling, which if implemented on ICs with hot spots may result in over-cooling and wasted power [4].

1.2 Thermal management literature review

Traditional strategies for cooling electronics have relied on conducting heat away from the transistor junction, through the substrate, across thermal-interface materials, to a heat spreader, where it is ultimately dissipated to a remote working fluid in the ambient environment, as shown in Figure 1(a) [1]. Chip-level embedded cooling, shown in Figure 1(b), removes many of the interface and conduction resistances of the conventional heat rejection pathway mentioned above, and offers a way to reduce the size, weight, and power (SWaP) of the thermal management solution. Heat conducts directly into the working fluid which flows within the substrate of the ICs, or, in the case of a stacked, vertically integrated device, flows around individual device layers.

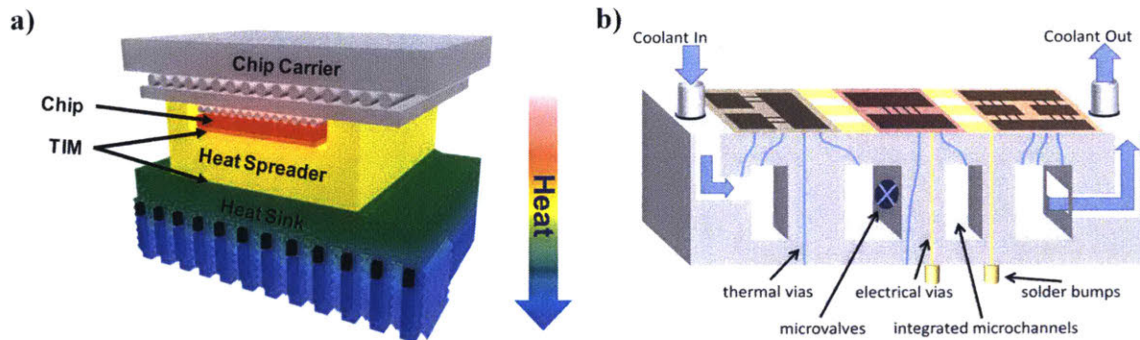


Figure 1- Cooling paradigms for integrated circuit. a) Traditional remote cooling: heat generated at the chip conducts and spreads through multiple materials and interfaces before being removed by a remote working fluid. Adapted from "Thermal Packaging - The Inward Migration," by A. Bar-Cohen in *Technical Symposium on Thermal Management*, 2012. b) Embedded cooling: heat generated at the chip conducts directly into a working fluid that is integrated into the substrate of the IC (or in between substrates, for 3D stacked IC's). Adapted from "Micro and Nano Technologies for Enhanced Thermal Management of Electronic Components," by A. Bar-Cohen, K. Matin, and *J. Maurer, Micro/Nano Manuf. Work.* - Michigan, 2013.

Single-phase and two-phase microfluidic cooling have been researched and implemented in embedded cooling approaches [1], [10], [11]. By taking advantage of the latent heat of vaporization, phase-change cooling has received significant interest in addressing the heat flux requirements of high ($\sim 10^3\ \mathrm{W/cm^2}$) and ultra-high performance ($\sim 10^4\ \mathrm{W/cm^2}$) systems while significantly reducing SWaP [3]. Specifically, flow boiling in microchannels has become an active area of research [10], [12]–[15]. Heat dissipation, q'', ~$200\ \mathrm{W/cm^2}$ with heat transfer coefficients, h, of $\sim 5\ \mathrm{W/cm^2K}$ using water, with exit qualities of up to 90% have been reported [16]–[18]. Two-phase flows experience higher pressure drops and may necessitate higher power requirements and lower the coefficient of performance (CoP, defined as the ratio of the heat removal rate to the rate of work entering the system, primarily the required pumping power). Flow boiling in micro/minichannels cooling has been improved by altering surface wettability using surface modification or nanoparticle fluid mixtures [19]–[21], enhancing vapor removal, and/or intensifying bubble nucleation. Mitigating flow instabilities in order to delay critical heat flux is a continuous barrier to large enhancements of cooling rates [18], [22], [23].

Passive capillary-pumped thermal ground planes take advantage of phase-change cooling, with near unity exit vapor qualities and high heat flux dissipation. These systems operate on capillary pressures, P_c, generated by surface tension at the liquid-vapor interface at the end of small passages of a wick, and is governed by the Young-Laplace Equation:

$$P_c = \frac{2\sigma \cos\theta}{d_p} \tag{2}$$

where d_p is the pore diameter, σ is the surface tension, and θ is the contract angle between the liquid and the solid wick. Examples include micro/nano-structures such as sintered copper mesh coated with carbon nanotubes [24], titanium nanopillars [25], silicon micropillars [26], and oxidized copper microposts [27]. Values of $q'' \cong 500\ \text{W/cm}^2$ and $h = {\sim}12\ \text{W/cm}^2\text{K}$ have been reported for heated area of $5{\times}5\ \text{mm}^2$, however in many cases they represent mixed mode evaporation and boiling. The capillary pressure generated at the liquid-vapor interface competes with the viscous pressure drop of the liquid transport through the wick. Once viscous losses exceed the capillary pressure budget in these systems, the meniscus of the working fluid recedes, dry out of the wick ensues, and the device temperature spikes. Hierarchical fluid supply networks aim to reduce viscous losses, which limit performance while preserving the driving capillarity. Flow architectures such as supply arteries [28], bi-porosity [29]–[31], and fractal-like biomimetic networks [32], [33] have been able to reach thermal dissipation around $q'' = 990\ \text{W/cm}^2$ with $h = 6.7\ \text{W/cm}^2\ \text{K}$ [34].

Evaporation has been studied theoretically and experimentally [35], [36] for dissipating high heat fluxes. The heat transfer coefficient of a two-phase system with efficient vapor transport depends largely on the heat conduction characteristics between the substrate and the liquid-vapor interface. The thin film region, depicted in Figure 2, found between the absorbed liquid on the substrate and the bulk meniscus, exists beyond the effects of adhesion forces. This area provides the maximum interface curvature, has the smallest thermal resistance, and accounts for as much as half of the interfacial flux from a macro-sized liquid menisci [22],[36]. High heat transfer coefficients and ultra-high heat fluxes can be sustained across the entire

interface area, by evaporating liquid from pores that are smaller in diameter than the thickness of the thin film region (~0.5 μm).

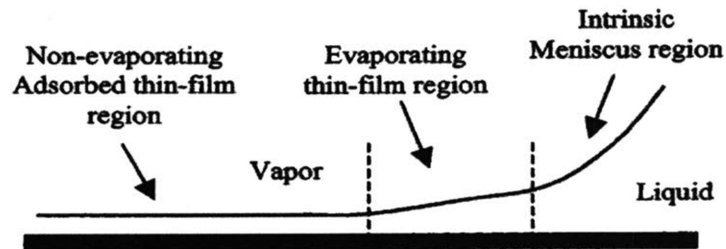


Figure 2- Regions of an evaporating extended meniscus. Adapted from "Characteristics of an evaporating thin film in a microchannel," by H. Wang, S. V. Garimella, and J. Y. Murthy, Heat Mass Transf., vol. 50, no. 19–20, pp. 3933–3942, 2007.

1.3 Thesis Overview

The focus of this thesis is to fabricate the designed high heat flux evaporative intrachip cooling strategy using a silicon nanoporous membrane. Operation of this device was used to characterize performance and validate a multi-scale compact model of the device used to predict its performance. Chapter 1 introduces the necessity for novel, ultra-high heat flux, embedded cooling strategies. Chapter 2 describes the requirements of a thin film evaporator, performance targets for this particular cooling solution, and explains how this nanoporous embedded evaporator operates. Chapter 3 details the evolution of the device fabrication process plan, and highlights key challenges that were encountered. Chapter 4 describes the device performance and compares it to the computational model. Finally, Chapter 5 concludes with recommendations for fabrication improvements and operating conditions for peak performance, and suggestions for future work.

Chapter 2- Nanoporous Evaporative Cooling

2.1 Design objectives & constraints

In order to maximize continuous thin-film evaporation, an efficient ultra-high performance evaporator device must meet the following criteria: (1) a low conduction resistance layer between the substrate and liquid-vapor interface, (2) ability to generate large capillary pressures to supply sufficient working fluid to the interface, (3) a liquid channel architecture that minimizes viscous pressure losses, and (4) an effective vapor transport at the liquid-vapor interface. Using a thin nanoporous membrane (which addresses criteria (2) and (3)), Narayanan et. al. obtained dissipation rates in excess of $600\ \mathrm{W/cm^2}$ [37] and predicted heat fluxes of over $5\ \mathrm{kW/cm^2}$, from a device which relied on conduction through a continuous liquid layer, supplied with actively pumped working fluid, and whose vapor was advected using dry air [38]. These latter aspects needed improvement [39].

Previous work have reported the design for a 1 $\mathrm{cm^2}$ intrachip, two-phase evaporative cooling device, which was parametrically optimized to be capable of dissipating an average heat flux of $1\ \mathrm{kW/cm^2}$ [1], [40]. The modeled device maintained favorable conditions for cutting-edge IC performance by holding the junction temperature within 40°C above the ambient vapor temperature, and cooling a submillimeter hot-spot generating $5\ \mathrm{kW/cm^2}$ with a maximum temperature difference of less than 10°C across the substrate. The monolithic thermal management strategy used evaporative phase change to reach higher fluxes than single phase sensible cooling due to the additional latent heat of evaporation, and provided better temperature uniformity from the isothermal process [41]. Using a supported nanoporous membrane to conduct heat to the phase change interface, and limiting the evaporative process to within the thin film region, ultra-high heat fluxes approaching the kinetic limit were predicted [36], [42]. Hierarchical flow channels within the device helped minimize the hydrodynamic resistance to flow.

2.2 Description of the system

A 1 cm^2 intrachip evaporative cooling device capable of dissipating an average heat flux of 1 kW/cm^2, was previously designed with parametrically optimized geometries [1], [40]. Based on that design, the device fabricated in this study, used nanoporous membranes to restrict the evaporative process entirely within the thin film region. Hierarchical flow channels implemented within the device minimized the hydrodynamic resistance. Cross sections of the device are presented schematically in Figure 3 below.

Heat generated in the active layer of an IC device, proxied by high resistance thin film heaters, conducts through the substrate, up the ridge structures and into the membrane. The membrane dissipates heat by evaporating the working fluid, which is constantly resupplied and drawn in by negative capillary pressures generated by ~100 nm pores. The membrane thickness is minimized to prevent excessive pressure losses through a channel with nanometer scale hydraulic diameter. The liquid and gas phases are completely separated by the membrane, thereby eliminating the high-pressure drops associated with pumping two-phase flow.

Each nanopore self-regulates mass flux by changing the meniscus shape or position. The curvature at the meniscus generates an interfacial pressure difference which drives the fluid flow, overcoming viscous losses along the nanopore. At lower interfacial pressure differences, the meniscus is pinned at the top of the pore. The curvature of the meniscus changes in response to different working conditions, which included the pore wall temperature and liquid supply pressure, as depicted in Figure 4(a). Curvature increases until the contact angle reaches the local receding contact angle beyond which the meniscus recedes within the pore.

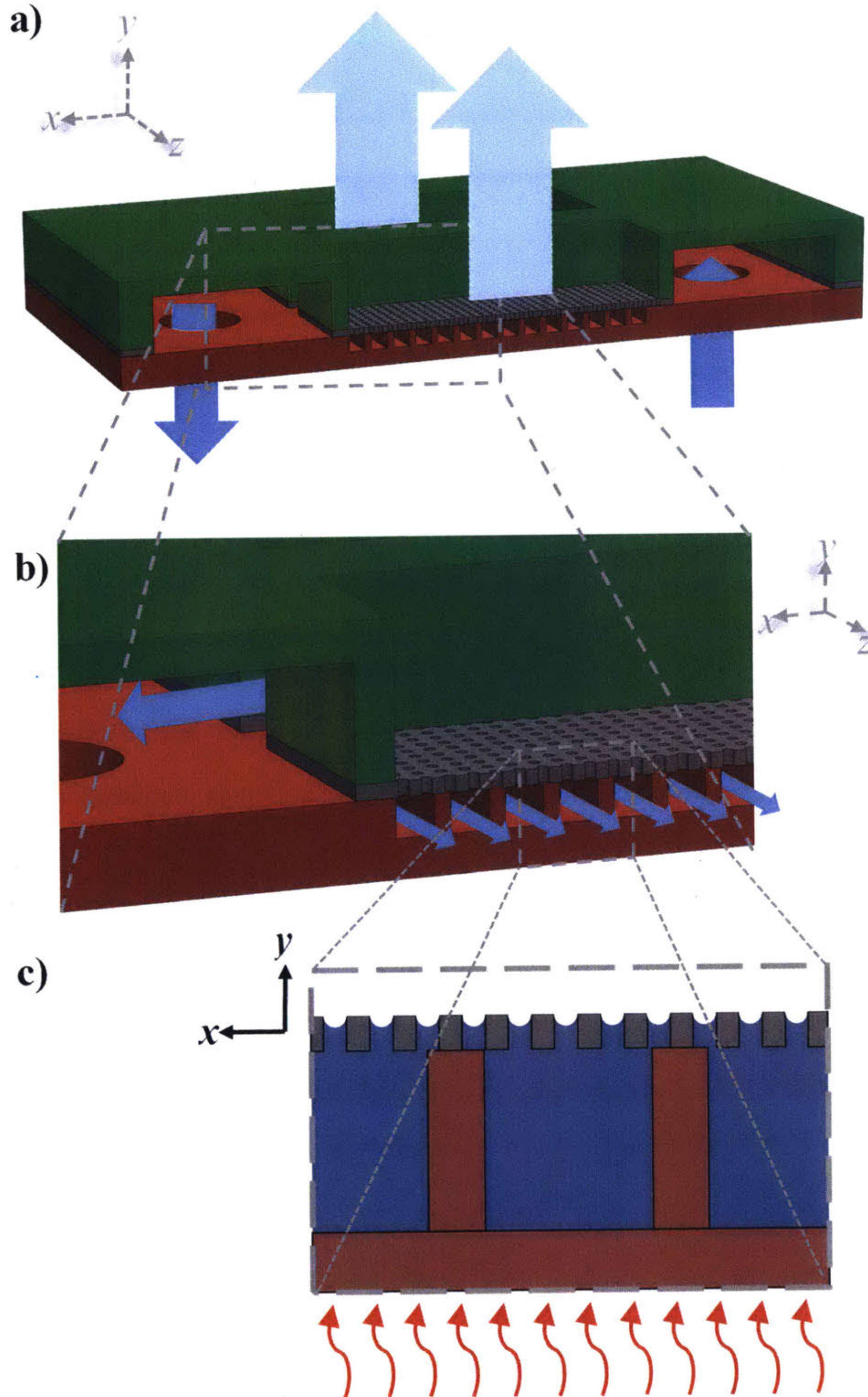


Figure 3- Cross sectional schematic of an intrachip, nanoporous, membrane-enhanced evaporative cooling device. a) Pure liquid enters the device and either exists via a bypass or is evaporated. b) Liquid is supplied across the length of the device through a series of manifold channels (shown in green) and is wicked into shorter and narrower, ridge microchannels (shown in red). c) Heat generated at the base of the device is conducted through the substrate, up the ridges, and across the membrane (shown in grey), and is dissipated by continuously evaporating working fluid.

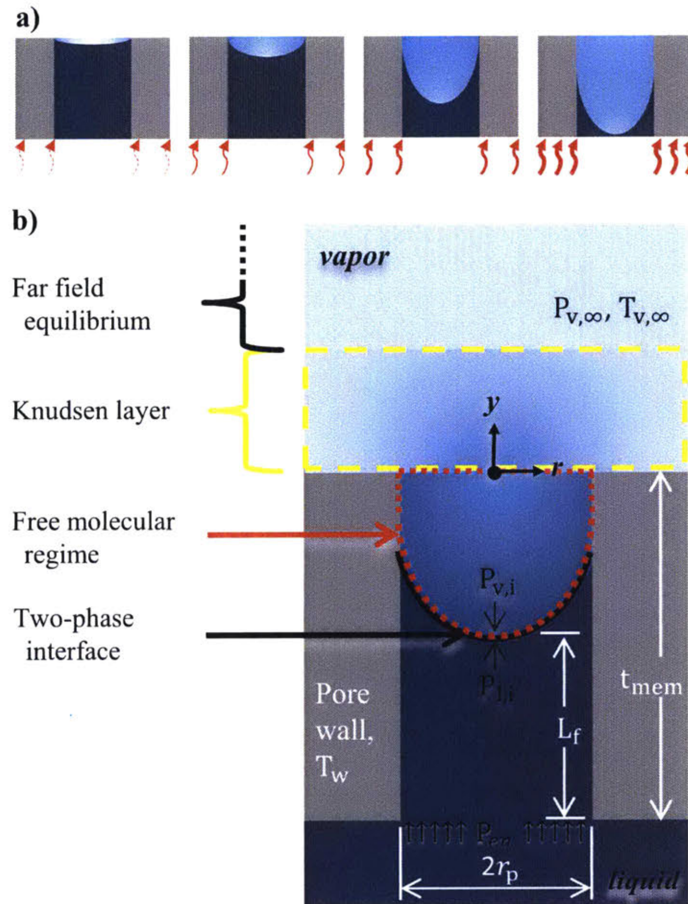


Figure 4- Schematic of evaporation from a nanopore. a) progression of increasing evaporation until dry out from a nanopore: the liquid-vapor interface can change its shape or position in response to different working conditions. and b) vapor transport from the free molecular regime inside the pore, across the Knudsen layer, to the far field equilibrium regime.

Our device concept offers several advantages. Nanopores constrain the evaporation process entirely within the thin-film regime, where there is reduced conduction resistance of the liquid. The architecture leverages nanoporous membranes to decouple the heat dissipation from the pressure drop of the device. Excess flow in the liquid manifold channels and capillary-driven self-regulated flow in the microchannels and pores eliminates the requirement to match the inlet flow rate to the evaporating mass flow rate and reduces the need for additional fluidic valves and active control. The overall pressure drop of the device is composed of the viscous losses in each of the three flow hierarchies. The manifold channels are the only section to require active pumping; the resulting viscous loss is ~15% of the total pressure requirements [40]. With the bulk of the pumping power provided by capillary, an evaporator thermo-fluidic CoP ≫ 100 is possible.

2.3 Modeling

The designed nanoporous evaporative device with a total membrane area of up to 10×10 mm can have a large number of pores and microchannels, thus making computational modeling of the exact physical representation unfeasible. Figure 5 below demonstrates two levels of simplifications that are used to make the computation more tractable. The nonequilibrium and nonlocal evaporation effects are first captured at the pore level and then fed into device level compact models that remove the fine details, while predicting with good agreement the overall performance.

2.3.1 Pore-level model

Lu et al. incorporated nano-scale heat and mass transport into a conjugate conduction-convection compact model used to predict pore level heat transfer coefficients for performance parameterization and optimization [43]. Pore level heat flux was calculated by predicting the behavior of the liquid-vapor interface by conserving energy, mass, and momentum across the different physical fluid regimes of the nanopores, as shown in Figure 4(b). The different layers are i) the liquid permeating through the membrane operating under continuum mechanics, ii) the non-equilibrium, evaporation generated vapor trying to escape the pore which operating as free molecular flow, iii) the Knudsen layer of vapor just above the membrane, where the relative magnitude of vapor mean free path indicates the presence of slip flow, and iv) the far field vapor of the environment with bulk thermodynamic properties where flow is governed by the Navier-Stokes equation.

The effective pore heat transfer coefficient, h_p, was calculated and tabulated into a lookup table for device level modeling as a function of pore wall temperature (T_w), pressure at the base of the pore (P_{in}), and the equilibrium vapor pressure, $(P_{v,\infty})$.For further reference, please refer to Lu et. al. [43], [44].

2.3.2 Compact models

Multiphysics modeling in COMSOL was used to predict device performance with a simplified compact hydrodynamic and thermal modeling.

Hydrodynamic modeling. Pressure drops within microchannels and nanopores were calculated using the Darcy-Weisbach equation for fully-developed laminar internal flow [45]:

$$\frac{dP_l}{dx} = -\mu_l \overline{\vec{u_l}} \frac{f\,Re}{4D_H^2} \tag{2}$$

where P_l was the pressure in the liquid phase, x is the flow length, μ_l is the viscosity on the liquid, $\overline{\vec{u_l}}$ is the mean liquid velocity, D_h is the hydraulic diameter of the channel, and $f\ Re$ is the Poiseuille number (value was obtained from correlations given by Liu *et al.* [12]).

The momentum and mass transport within the liquid channels and membrane were modeled using Darcy's law for laminar flow through porous media with anisotropic permeabilities:

$$\overrightarrow{u_{sup}} = \frac{\phi}{\mu_l} \vec{\alpha} \cdot \overrightarrow{\nabla P} \tag{3}$$

where, $\overrightarrow{u_{sup}}$ is the fluid superficial velocity across the membrane or ridge channels, $\overrightarrow{\nabla P}$ is the pressure gradient, and ϕ is the porosity, and $\vec{\alpha}$ is the permeability vector for the channel.

For a cylindrical nanopore oriented across the membrane (y-direction) with radius r_p and pitch l_p, the permeability, $\overrightarrow{\alpha_{mem}}$, is given by:

$$\overrightarrow{\alpha_{mem}} = \langle 0, \frac{\pi r_p^4}{8 l_p^2}, 0 \rangle \tag{4}$$

For rectangular ridge channels oriented in the x-direction, the permeability, $\overrightarrow{\alpha_{ridge}}$, is given by:

$$\overrightarrow{\alpha_{ridge}} = \langle \frac{2D_{h,r}^2}{f\,Re}, \gamma \frac{2D_{h,r}^2}{f\,Re}, 0 \rangle \tag{5}$$

where $D_{h,r}$ is hydraulic diameter of the ridge channel and γ is a scaling factor chosen such that the flow resistance in the y-direction is small relative to the flow direction. Assuming a uniform evaporative mass flux, Darcy's law was integrated to yield the pressure drop across and underneath the membrane. Simulations in ANSYS Fluent showed agreement to be within 1%-3% for overall pressure drops in the porous media compared to a fully detailed model. Discrepancies are attributed to wall effects associated with the no-slip boundary condition.

Thermal modeling. To assess the validity of the porous media approximations, a fully detailed base case model for a slice of the ridge, channel and substrate, shown in Figure 5, with the following parameters was simulated: $q''_{base} = 1\ \mathrm{kW/cm^2}$, $T_w = 300$ K, $h_p = 7\ \mathrm{W/cm^2}$ K, and water as the working fluid. The first approximation, compact model #1, replaced the porous membrane with solid silicon with an effective lateral thermal conductivity predicted using ballistic phonon transport. Heat conduction along the x-direction resulted in a temperature distribution, $T_{mem,1}(x)$. Heat transfer to the ambient, $q''_{mem,1}$, was assumed to occur at the top surface of the membrane above the ridge channels w_{rc}, but not above the ridges, w_r.

$$q''_{mem,1} = h_1\left(T_{mem,1}(x) - T_{v,\infty}\right) \tag{6}$$

where $h_1 \equiv \phi h_p\, w_{rc}/(w_{rc} - 2w_r)$ is the area weighed effective heat transfer coefficient from the membrane not over the ridge.

In compact model #2, energy transport through the membrane was modeled by treating the membrane as a finite, constant cross-section fin with an adiabatic tip. The resulting heat transfer from the membrane surface, $q''_{mem,2}$, was:

$$q''_{mem,2} = h_2\left(T_{mem,r} - T_{v,\infty}\right) \tag{7}$$

where $T_{m,r}$ is the temperature of the membrane directly over the ridge (the "base" of the fin), and $h_2 \equiv h_1\,(w_{rc} - 2w_r)/w_c$ is the area weighed effective heat transfer coefficient for the membrane above both the ridge and the channel.

In compact model #2, the entire surface of the membrane dissipated heat to the ambient, and not just the portion of the membrane over the channel. Modeled as a fin, the temperature predicted at the surface of the membrane was expected to be representative of the temperature at the junction of the membrane and ridge structures. This was made explicit by solving the fin equation for the membrane, where the temperature drop across the membrane, ΔT_{mem}, is given by:

$$\Delta T_{mem} \equiv \left(T_{mem,r} - T_{m,rc}\right) = \frac{q''_{base}}{h_2}\frac{(1+w_r/w_{rc})}{\eta_{fin}} \quad (8)$$

where $T_{m,rc}$ is the membrane temperature above the middle of the ridge channel (the "adiabatic tip" of the fin) and η_{fin} is the fin efficiency. It shows temperature distribution for the different cases, and highlights the very good agreement for the minimum temperature (at the membrane) for the base case and compact model #1, with the temperatures agreeing to within less than 1%. Deviation for compact model #2, where the minimum temperature was approximately 0.8 K larger, corresponds well to the conductive temperature drop across the membrane when modeled as a fin, which was 0.83 K, and was captured in the computationally expensive base model and compact model #1.

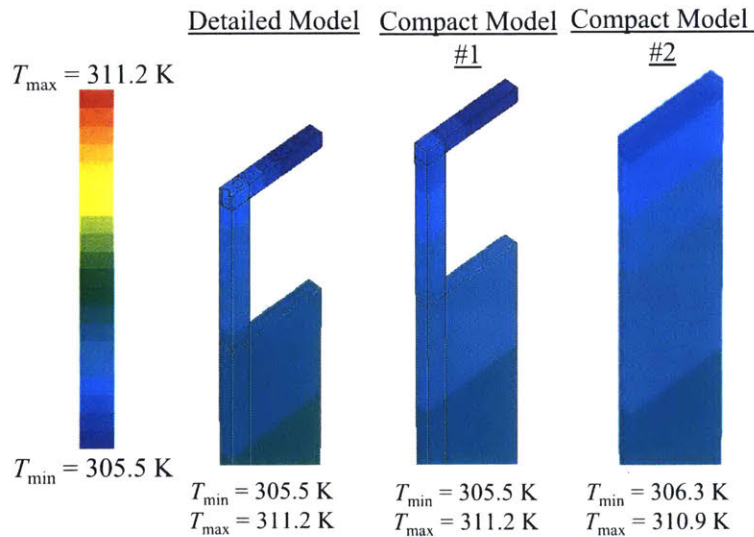


Figure 5- Temperature distribution for a set of models for a 1 kW/cm^2 heat flux at the base of the device and 300 K ambient temperature. $\boldsymbol{T_{max}}$, is located at the bottom of the substrate (not shown).

2.3.3 Parameter optimization and selection

Lu et al. modeled heat transfer performance from pore level evaporation and performed a global parametric optimization over geometric parameters (porosity, pore diameter, membrane thickness, and microchannel width, pitch, and depth), for select working fluids (water, methanol, pentane, R245fa, and R134a) operating at ambient temperature [46]. Heat transfer performance for each of the working fluids at fixed temperature differences between the liquid-vapor interface and far-field ambient were simulated. Listed by increasing heat transfer coefficients was: water, methanol, pentane, R245fa, and R134a. The higher vapor density of solvents and refrigerants more than compensated for the lower latent heat of vaporization when compared to water. Furthermore, the dielectric properties of these fluids make them more readily adoptable by the electronic thermal management industry. The low surface tensions of these dielectric fluids, however, generate lower capillary pressures, thereby requiring smaller pore diameters. This makes using them more likely to dry-out than operating with water.

Target microchannel, ridge, nanopore, and membrane geometric parameters were identified from the parametric optimizations of nanoporous membrane enhanced system level evaporation, with heat dissipation constrained to $1\ \mathrm{kW/cm^2}$ and a viscous device-level pressure drop no greater than 40% of the capillary pressure generated by the nanopores. This latter constraint mitigated the risk of dry-out and provided a safety factor to accommodate additional pressure losses from non-idealities and variations during fabrication. Optimized geometries for R-134 and pentane are presented below in Table 1. Target dimensions for fabrication were selected to bracket the performance of these working fluids, and are also presented.

Table 1- Parametric optimizations of device gemeoteries and fabrication targets

	Optimized performance		Fabrication targets
	R-134* [46]	Pentane** [40]	
Porosity, ϕ, -	0.4	0.5	**0.1 –0 .5**
Pore Diameter, d_p, nm	120	200	**60 - 130**
Membrane thickness, t_m, nm	450	200	**200 - 400**
Ridge width, w_r, µm	1.33	0.2	**0.3 - 2**
Ridge channel width, w_{rc}, µm	4	2	**2 - 5**
Ridge channel height, h_{rc}, µm	10	2	**2 - 4**
Ridge channel length, l_{rc}, mm	0.7***	0.1***	**0.2 – 1**
Manifold channel width, w_{mc}, µm		100***	**100**
Manifold channel height, h_{mc}, µm		100***	**100**
Manifold channel length, l_{mc}, cm		1***	**1**

* Optimization neglected liquid manifold channels and assumed negligible pressure drop

** Added constraint $w_{rc} = h_{rc}$

*** Constrained parameter

Chapter 3- Nanoporous Evaporator Fabrication

A monolithic test device was fabricated with micro and nano-channels using MEMS lithography, chemical etching, thin film deposition, and packaging in a class-100 clean room environment. Facilities used include the Microsystems Technology Laboratories (MTL), the Center for Materials Science and Engineering (CMSE), and the Nanostructures Laboratory (NSL) at MIT, and the Center for Nanoscale Systems (CNS) at Harvard.

3.1 Substrate selection

Materials common to nanofabrication industry were considered for this nanoporous evaporative cooling test device. High power IC devices that may require novel high flux cooling solution, tend to be fabricated on GaN and SiC substrates, for reasons alluded to earlier. However, silicon, with its historic and wide-scale usage, and library of well-developed processes, was selected for this proof of concept study.

In order to maintain a membrane with precise and uniform thickness, a wafer with a thin film of silicon atop of an etch stop of silicon oxide was used for the membrane. This type of substrate is commercially available as silicon on insulator (SOI). Due to sourcing limitations for wafers with the desired thickness, the nanoporous membrane was initially fabricated on SOI-like wafers, fabricated in-house. A prime 4" Si wafer (525 ± 25 μm thick, double side polished (DSP), < 1 0 0 > oriented, p-doped), referred to as the "handle" layer, was oxidized in a Thermco Atmospheric 10K Furnace tube at 1050°C for 6 hours, to form a buried oxide (BOX) layer 1 μm thick. To complete the substrate, a "device layer" of polysilicon (α-Si) 0.325 μm thick was thermally deposited at 650 °C using silane, SiH_4, as the precursor. This substrate will be referred to as a "pSOI" wafer. A separate DSP Si wafer was used to create a ridge channel array and had ohmic heaters deposited to proxy ultra-high thermal loads.

3.2 Initial fabrication process plan

The initial process flow for fabricating the test device with micro and nano-channels is shown schematically in Figure 6.

Nanopores were etched into a 325 nm polysilicon device layer of the pSOI wafer (shown in green in Figure 6), stopping at the 1 μm SiO_2 (BOX) layer. The cleaned pSOI wafer were patterned with liquid channels that run the length of the device, and plenums, liquid inlet and outlet reservoirs. These features were etched through the device and box layer, and partially (140 μm) into the silicon handle.

A separate 6" DSP Si wafer (shown as maroon in Figure 6) had smaller hydraulic diameter liquid channels created by etching an array of 4 μm wide and 4 μm deep square channels with a pitch of 5 μm. Both wafers were cleaned and bonded so that large liquid channels and small ridge channels ran perpendicular to one another. The bonded wafer stack had ohmic platinum heaters and resistance temperature detectors (RTDs) deposited on the back side of the ridge wafer.

Liquid ports were etched into the plenum from the metalized side of the wafer, allowing access to the previously hermetically sealed fluidic device. To complete to flow paths of the device, vapor channels were etched through the handle of the pSOI, interspersed along the z-axis between the positions of the liquid channels, in order to expose the nanoporous membrane and provide an exit for the pure vapor generated from evaporative cooling. The wafer stack was then cut in a die saw and suitable devices were thoroughly cleaned wire bonded.

Process changes and refinement throughout the fabrication were necessary in order to produce test devices that were free of critical defects and could be characterized for their evaporative cooling performance. The most significant process refinements and revisions for each device feature and/or step, will be discussed below.

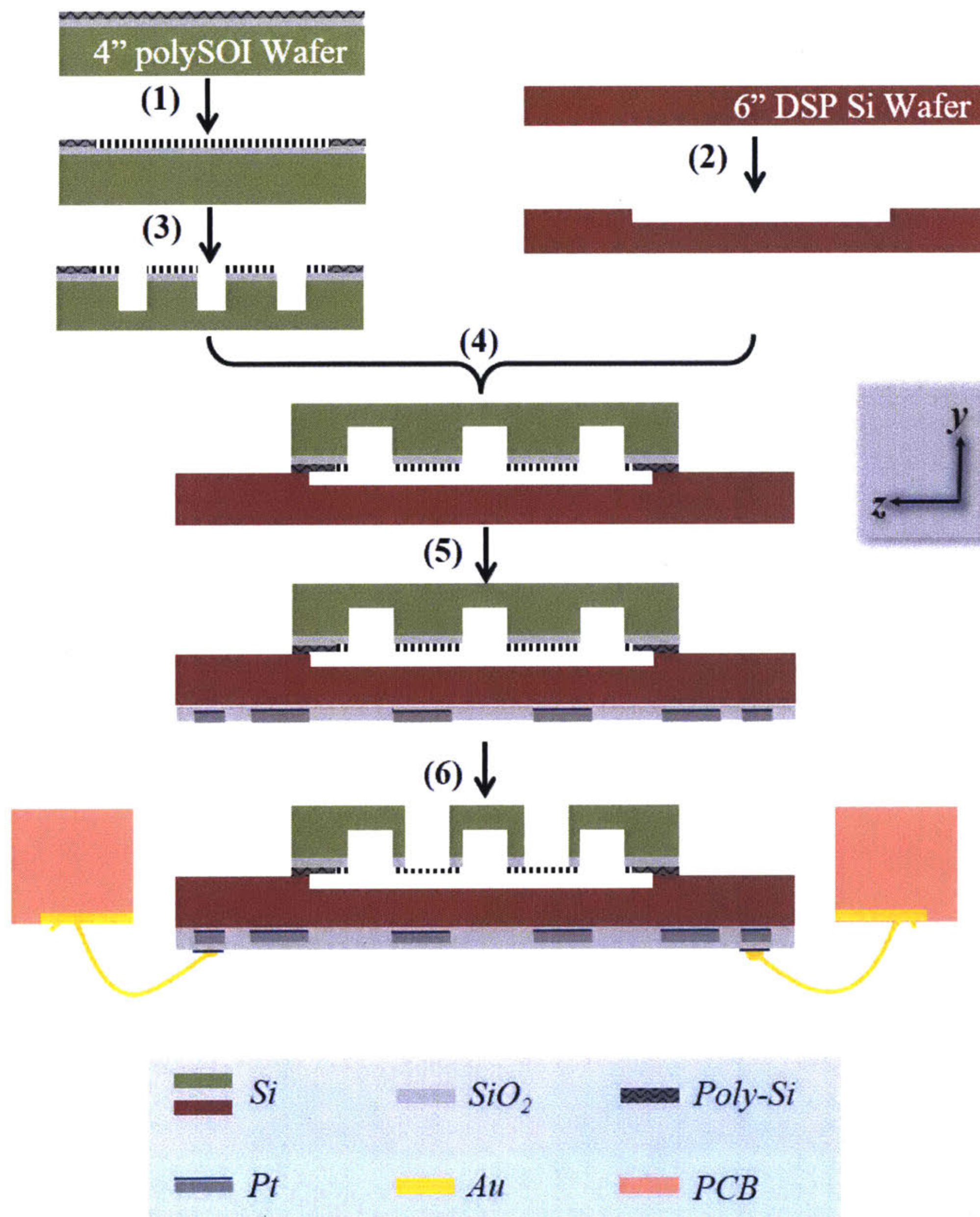


Figure 6- Schematic of the intitial micro-fabrication process. Cross section taken parallel to the ridge channels, along the xy-plane. Ridge channels, which mechanically support the membrane and provide a thermal conduction pathway from the heated substrate to the membrane, were etched in step (1). In parallel, nanopores were etched into the device layer of the pSOI substrate, shown in step (2), and then the larger manifold channels were etched through the (membrane) device layer and partially into the Si handle in step (3). The two wafers were then aligned and bonded to form a hermetically sealed fluidic network, step (4). To enable testing, during step (5), devices had proxy resistive heaters and temperature detectors (RTDs) deposited. In step (6), vapor channels were etched into the Si wafer, and inlet/outlet ports were etched into the "pSOI" wafer (not shown), to complete the open loop system. The wafer stack was then cut into individual dies (not shown) and then Au wire bonded as part of the packaging.

3.3 Nanopore definition

Interference lithography was selected to pattern the vast array of nanopores shown in Figure 6-step (1). Processes capable of meeting the $10^1 - 10^2$ nm resolution with non-negligible porosities required prohibitively expensive/time consuming mask/master stamp fabrication (e-beam lithography & nanoimprints lithography) or had defect densities (block co-polymer self-assembly) capable of diminishing the nanopore generated capillary budget required to prevent dry out and device failure. Interference lithography was selected for pore patterning. Interference lithography uses two or more coherent light waves constructively and destructively interfere to create a fringe pattern within the exposed photoresist. This fringe pattern repeats on the order of the wavelength of monochromatic light used for exposure. Controlling the power dosage during each exposure, a wafer with a fringe pattern exposed once can be re-exposed with the same pattern after a 90° rotation in order to generate a square area of pores. A 325 nm wavelength He-Cd laser used for this process can repeatedly resolve features at up to 54° angle of incidence with high fidelity. This allowed a maximum 200 nm pitch for a square array of pores and pore modulation from 80 nm to 150 nm. The membrane pores were successfully etched using a HBr and O_2 –chemistry, inductively couple plasma (ICP) reactive ion etch (RIE) through the silicon device layer, stopping selectively at BOX layer. Various etching tools and chemistries were tested before a suitably selective and anisotropic etch recipe was developed.

Due to the nature of having a multilayer substrate, a pre-exposure stack of 4 different coatings, including hard and soft masks, were applied in order to transfer the pore pattern onto the device layer to accurately maintain defined pores and to control internal reflections which could result in over/under exposure of the resist. Transferring the pattern through these layers required a number of different reactive ion etches (CCP RIE) with different chemistries. An added challenge of removing remnants of these masks, in order to return the wafer to a prime-smooth bond ready status, required tailored cleaning steps to ensure the integrity of the thin membrane. Detailed summary of the pre-exposure stack, sequential etching, and wet cleaning was developed by collaborator Dr. Daniel Hanks [47].

Figure 7 demonstrates nanoporous membrane fabrication capabilities and the challenges of wafer-scale repeatability. Non-idealities in the interference lithographic process resulted in inconsistent definition of the nanoporous membrane. The Lloyd's Mirror Interferometry used is a type of "One Beam Interferometer"; it is designed primarily for high fidelity patterning over a few square centimeters [48]. The mirror used to create the second beam needed for interference, is susceptible to uncontrolled optical path length differences which can result in a gradient of exposure dosing. Factors such as alignment accuracy, hyperbolic phase distortion, and airflow variations between the mirror and the sample, lower the size of the area accurately patterned. The 4" wafer in Figure 7(a) highlights the variation in pore definition that remained after recipe optimization on the available IL setup. In one region of the wafer, the pores are properly defined and circular, albeit a little undersized (~80 nm), Figure 7(b). With increasing dosage, moving across the wafer pores initial increase in diameter and then start to lose their circular appearance, Figure 7(c). Eventually, the pores widen unevenly along a major semi-axis, elongating into elliptical cross-section pores that start to merge Figure 7(d & e). When enough pores merge sequentially, the undulating Si pore walls that remain, lose structural stability, topple over, and lie on top of the buried oxide layer if they are held strongly enough with stiction forces not to be washed off, Figure 7(f). Deteriorating and destroyed regions of the nanoporous membrane can be detected from the optical changes at the wafer scale, *e.g.* the location where the SEM image of Figure 7(f). 1 μm of thermally grown SiO_2 of a BOX layer should appear carnation pink, which agrees with the SEM identified destruction of the device layer.

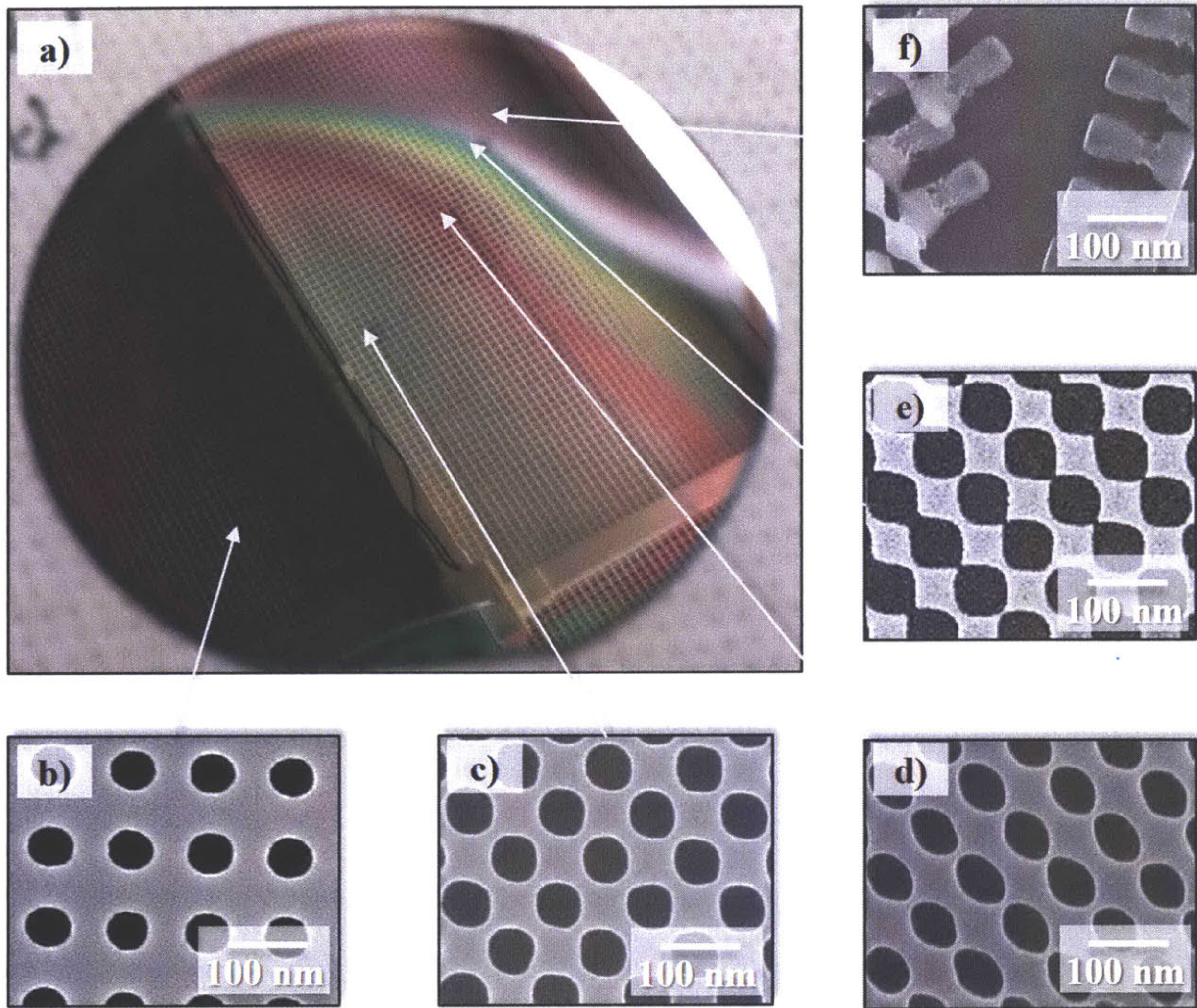


Figure 7- Spatial pattern uniformity challenge of the IL nanopore etch recipe. a) Optical image of a 4 inch polySOI wafer with etched nanoporous membrane. b-f) represent SEM images taken along the diagonal vector across the wafer, which generally followed the largest gradient in bulk optical properties of the wafer. Rough SEM locations are marked along the wafer (a). Scale bars in (b-f) represent 200 nm.

3.4 Liquid channels etching

The 100 μm wide liquid manifold channels were then etched into the same pSOI wafers, through the membrane and buried oxide layers, and partway through silicon handle, Figure 6-step (2). The wafer was primed with ~6 nm of hexamethyldisilizane (HMDS) to promote adhesion of 9 μm of spin-coated positive-tone thick resist (AZ-P4620 from MicroChemicals). The mask was patterned using contact photolithography under a mercury vapor lamp mask aligner (Electronic Visions Model EV620). Each layer of the SOI was etched selectively in order to maintain a sharp etch profile. The silicon membrane was etched using an inductively coupled plasma Deep Reactive Ion Etching (DRIE) tool (ST Systems Multiplex ICP), operating a modified Bosch process for shallow etching. The buried oxide layer was etched with an Electron Cyclotron Resonance Reactive Ion Etcher (ECR/RIE) using an O_2/CF_4 chemistry. A buffered oxide etch (BOE), allowed for enhanced uniformity, and as alluded to above (and depicted in Appendix B), wet etching resulted in 100 nm pores excellent uniformity. The liquid manifolds were etched into Si handle using a DRIE etch tuned for minimal surface roughness.

Key challenges in fabricating the liquid manifold channels were 1) preserving the prime (bondable) status of the pSOI wafer, 2) minimizing surface roughness of the side walls, and 3) adhering to the tight tolerances required, ensuring each future step is not compromised. Cross sections of liquid channels are shown in Figure 8. Failures included the complete destruction of the device layer and rough side walls (a-c), lithography challenges where the photoresist had reflowed (b), and receding photoresist at the mask edges that caused removal of ~10-5 μm of the device layer (c).

Most of the failures experienced were due to overheating of the wafer during etches, which was attributed to having to mount the 4" pSOI wafers to a 6" silicon carrier, due to tool availability. Having a photoresist layer and a full 600 um thick wafer resulted in overheating. Mounting techniques, show in Figure 9 helped better thermally ground the pSOI during etch processes. Figure 10 depicts samples fabricated with the final process, which resulted in smoother side walls and minimal device layer loss, ~ 2 μm.

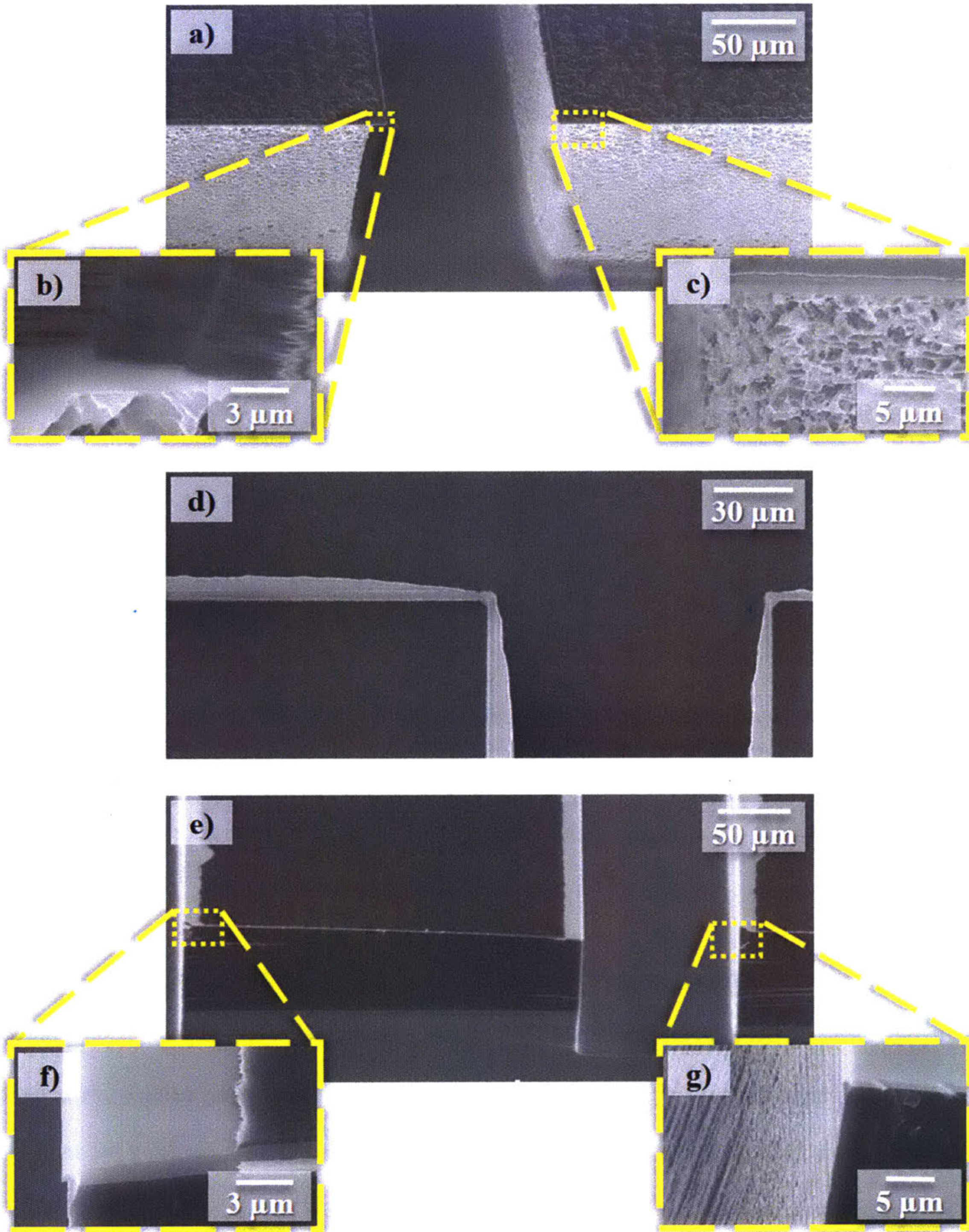


Figure 8- Common liquid manifold channel etch defects. a) Degradation of the Si device layer. b) Loss of etch definition. Device layer, BOX layer, and Si handle etched back creating progressive steps. c) Excessively highly roughness and loss of characteristic Bosch etch scalloping of the sidewalls. d) Loss of etch definition due to photoresist reflow. e-g) Tens of microns of device layer silicon were lost at the pattern edges. All images are of 4" pSOI wafers. a-c) Resulted from poor mounting technique and overheating during oxide etching during RIE. b) Resulted from insufficient post-baking of the resist. e-f) Improved process using wet etching techniques for the BOX, with room for improvement for thermally grounding wafer.

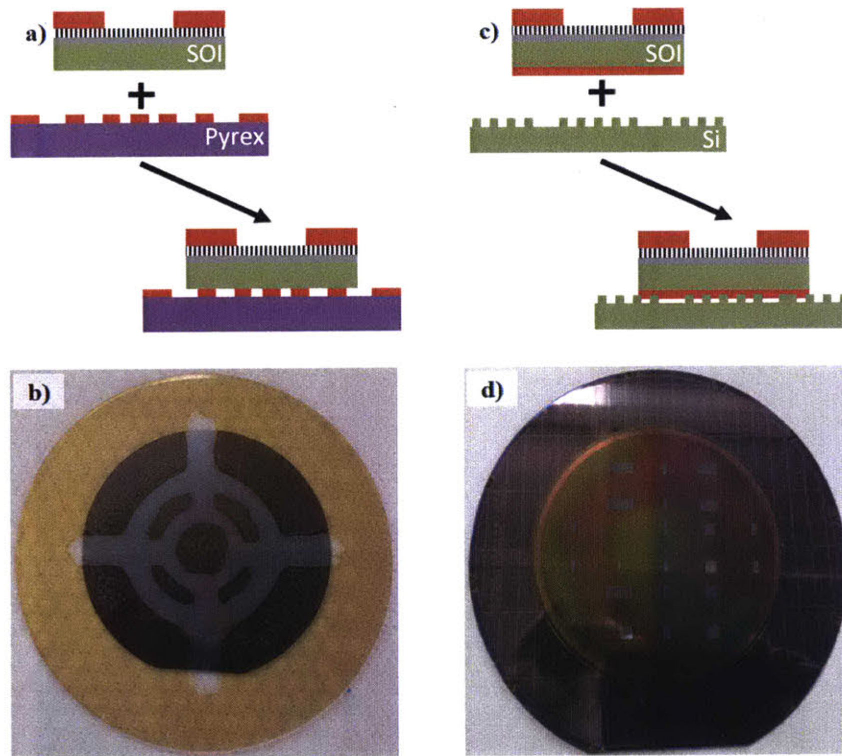


Figure 9- 4" wafer mounting techniques. a-b) Target mounting using a 6" Pyrex carrier. Using acetone and a clean-room swab, a target was hand drawn into resist layer, shown in red in schematics a and c, and appears yellow in optical image (b). Sample 4" wafer is pressed into the design and baked. c-d) The sample is blanket coated with resist and pressed into a pre-etched channel wafer. The latter configuration improved temperature uniformity of the substrate during etches, without hindering the vapor transport of resist off gassing.

The 2 μm wide ridge channel arrays were patterned with projection photolithography on an i-line Scan Field Stepper (Nikon NSR-2005i9) onto a new DSP Si wafer coated with 1 μm of positive-tone photoresist (SPR700-1 from Megaposit), which was spin coated, baked, and later developed using a coater/developer track (SSI-150 from Surface Science Integration). Ridges were etched 2 μm deep using the same shallow etch DRIE recipe mentioned above, Figure 6-step (3). Figure 11 (a & b) shows two cases of failed ridge channel etches. Figure 11 (c) shows an alternative channel configuration while d & e show two views of the final ridge structures.

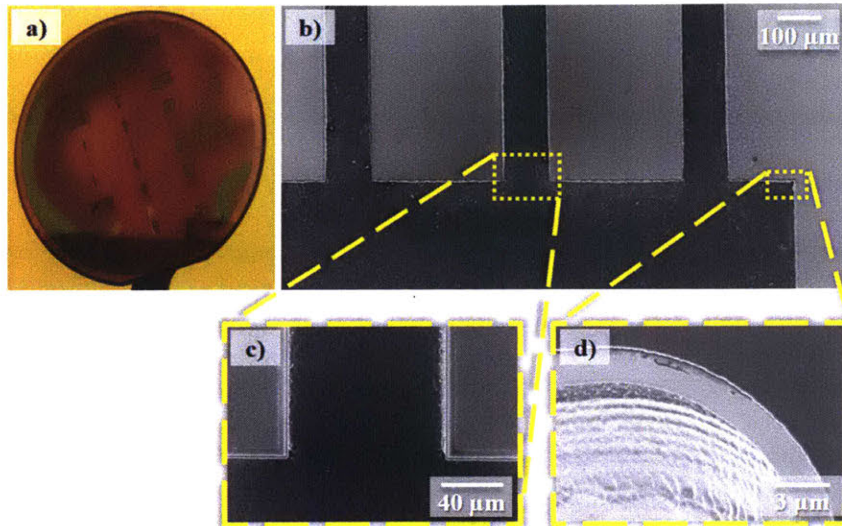


Figure 10- Final liquid manifold channels etch results. a) Optical image of the manifold pattern etched into a 4" pSOI wafer. b) Top view SEM image of a section of the manifold channels (a part of one of the plenums of a single device). Insert c) displays a magnified image of the inlet of a single liquid manifold channel and inset d) highlights the reduction in device layer loss at the pattern edges to below a couple of microns.

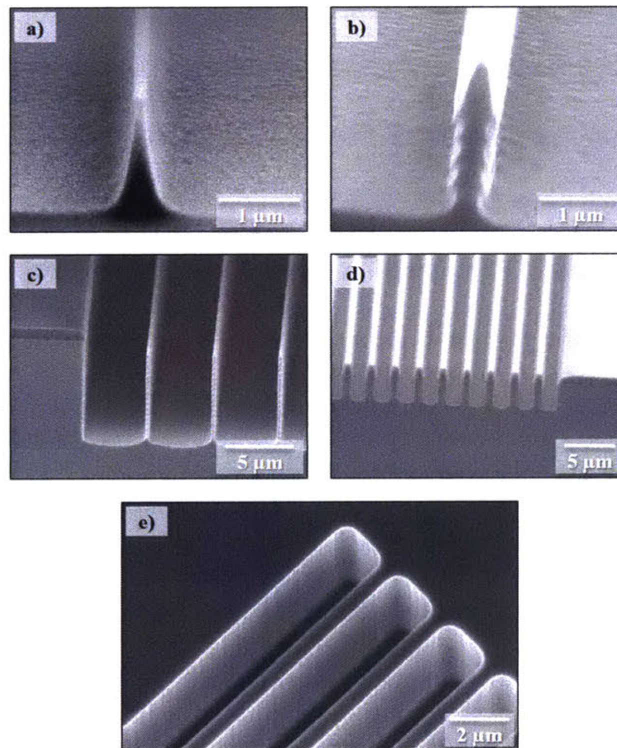
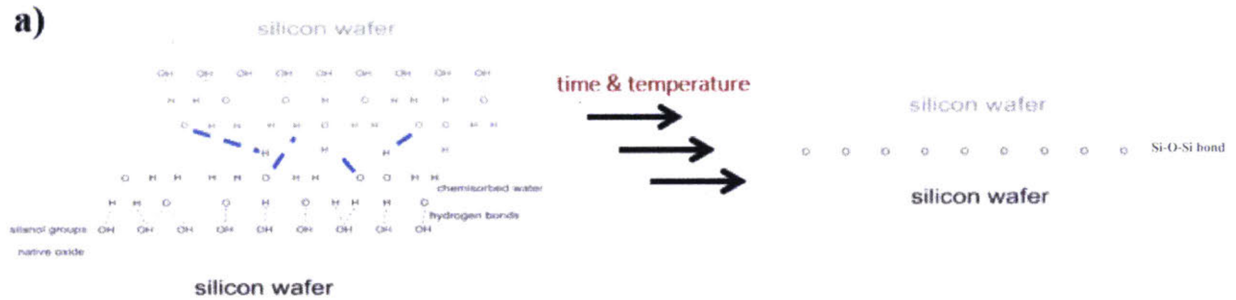
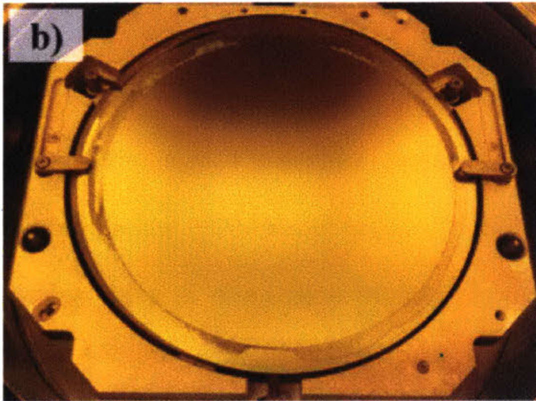


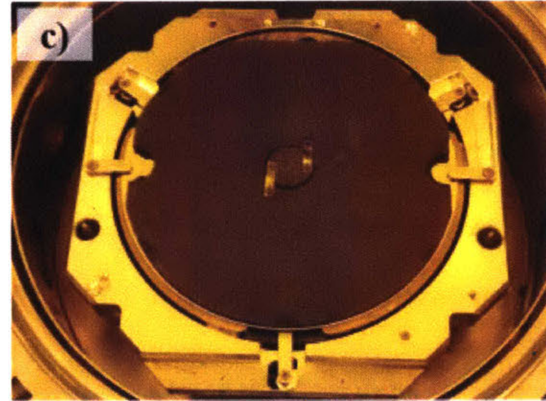
Figure 11- Ridge channel etches. Common ridge etch defects (a & b). a) Severely positive etch profile/loss of anisotropy/hindering etch depth limit, effects possibly due to: too short of an etch cycle, insufficient bias voltage, chamber pressure too high, SF6 flowrate too high. b) High sidewall roughness/excessive scalloping, which may promote bubble nucleation and cavitation. c & d) SEM cross section images of the optimized ridge etch recipes, producing two different geometries of high aspect ratio ridges/ridge channels. e) Oblique top view SEM image of the tested ridge array geometry.

3.5 Wafer bonding

The most critical fabrication step was bonding the membrane of the pSOI wafer to the etched ridge channels to form a suspended membrane structure with good strength, low thermal interfacial resistance, and a hermetic seal. Anodic bonding and intermediate layer bonding, commonly used techniques in the MEMS field, where not possible, due to the prior technique requiring that the bond interface hold a large voltage differential across the two wafers and the latter technique resulting in the introduction of a large thermal resistance from an adhesive layer material which would have to be etched through at a high aspect ratio at each of the nanopores. Silicon fusion bonding, in particular, Plasma Activated Bonding, PAB, as shown in Figure 12, was the selected method for bonding. PAB occurs at the atomic scale, does not introduce a low thermal resistive binder, and results in a Si-O-Si bond which has a bond energy that is greater than the Si-Si bond found throughout the two wafers. The chemical process for the bond involves the activation of the two native oxide layers on the Si of both of the wafers by oxygen plasma bombardment. Surface absorbed water molecules form strong hydrogen bonds that hold the wafers together once they are brought close enough to one another. A high temperature annealing process dehydrates the bond interface, and eventually all that remains are Si-O-Si bonds. This process is schematically summarized in Figure 12(a). Figure 12(b & c) highlights key aspects of the physical bonding process. Aligned wafers were kept from making contact with one another by three flags that were equally spaced around the circumference of the wafers. Contact was initiated at the center of the wafer, where the graphite pressure plate had a hinged center piece. As the bonded-not bonded interface propagated outward, a piston pressed the two wafers together, before the spacer flags were pulled out. Silicon wafers were optically opaque, but were transparent in the infrared spectrum. Figure 12(d) shows how the bond propagated radially outward from the center.







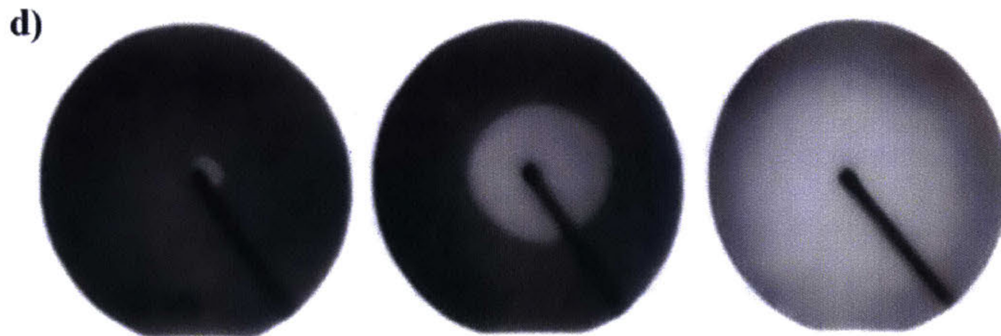


Figure 12- Fusion bonding chemistry & process. a) Schematic of the atomic interactions that occur during fusion bonding. Initial hydrogen bonding and Van der Waal forces are replaced with strong covalent Si-O-Si bonds during a high temperature anneal, during which water molecules must diffuse out of the bond interface. b) Aligned wafers are physically separated at three locations (top left and right and bottom center) by thin metal flags at the start of the bonding process. c) Bonding is initiated at the center of the wafers by a pin that pushes against the hinged center of the graphite pressure plate before a piston clamps down on the whole stack. d) IR images of two clean, smooth, and flat dummy wafers, shows bond propagation that occurs once contact is initiated at the center of the wafer. (Light regions represent IR transparent silicon without any voids/defects larger than 1/4th the light source wavelength. Dark regions represent where the wafers are not in contact.)

Direct fusion bonding is extremely sensitive to cleanliness, surface chemistry, surface roughness and wafer flatness. In preparation for bonding, the wafers were stripped of any remaining photoresist in a Piranha clean (a 3:1 solution of $H_2SO_4 + H_2O_2$) and then processed through a standard RCA clean, in order to ensure the removal of particles and prepare the wafers for bonding. This involved a 10 minute clean in a 5:1:1 solution of H_2O:NH_4OH:H_2O_2 at 80°C which removed any remaining organic residues, then a dip in 50:1 solution of H_2O:HF to remove the native oxide layer, and finally a 10 minute clean in a 6:1:1 solution of H_2O:HCl:H_2O_2 at 80°C which removed any remaining ionic contaminants.

After the wet clean, the bond surfaces were exposed to oxygen plasma to enhance Van der Waals adhesion. It also slightly damaged the new native oxide layer, in order to facilitate the diffusion and removal of the water molecules during the anneal. Finally, the wafers were cleaned once again in a 3:1 solution of H_2SO_4:H_2O_2, rinsed in water at 80°C and dried in a spin-rinse-dryer.

The wafers were mounted into an alignment tool (EVG620, EV Group) with the spacer flags, and transferred into a wafer bonding chamber (EVG501, EV Group). The chamber was evacuated to 10^{-3} torr using a turbomolecular pump for the bonding process in order to prevent expansion of trapped gases inside pores and liquid channels during the anneal step. If there were no defects by IR camera, the wafers were annealed in a tube furnace at 900°C for 4 hours in N_2 gas. Commonly identifiable defects that were identified from the IR camera included a) particle contamination, b) bond propagation obstruction at etched features, and c) pockets of non-bonding near cavities after the anneal step, which may be attributed to the expansion of un-evacuated gas or the generation of gas due to thermal breakdown/off gassing of some contaminant. Examples of qualitative proof of bond failures are presented in Figure 14.

pSOI nanoporous membranes failed to result in complete testable devices. Wafers exiting the wafer bonding chamber could be separated by trying to lift the wafer stack using a vacuum wafer handling tool. These initial failures were attributed to the roughness of the poly-crystalline surface. Fusion bonding generally required that bond surfaces have a root mean square roughness, R_{RMS}, of less than 2 μm. The process of

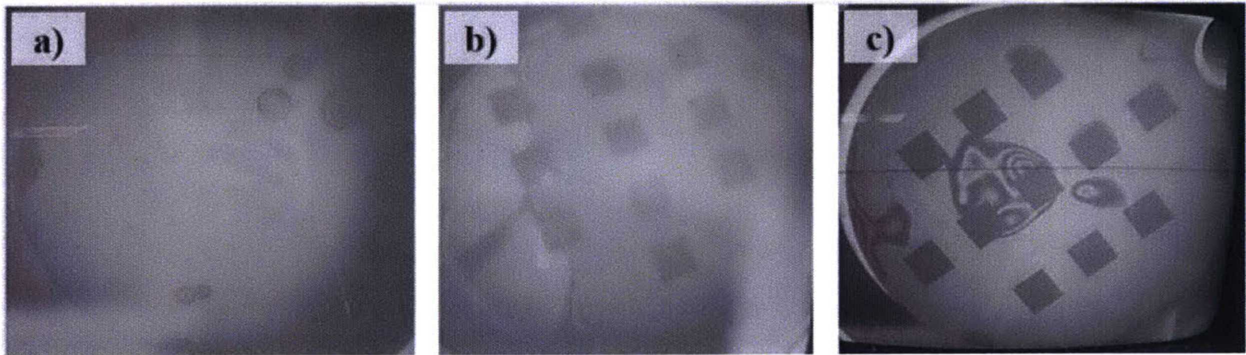


Figure 13- Common bonding defects. Nondestructive IR imaging highlight a) particle contamination, b) incomplete bonding due to pinning of the bond front, and c) gas entrapment during bonding. (a & b) defects were noticed prior to the annealing process. However, small volumes of gas may be hard to visualize until after their expansion during the anneal step.

bonding nanoporous membranes to ridge structures is even more challenging due to the loss of almost 50% of the bondable surface area due to the material removal on each wafer; 32% area loss due to the porosity of the membrane wafer (~40% when incorporating the device layer removal by the liquid channel and plenum etches) and 7% global, 75% local (at each device) area loss due to the etch of the ridge structures. The low contact area for bonding demanded surface cleanliness, smoothness, and waviness, even more stringent.

Surface roughness was measured by Atomic Force Microscopy (Dimension 3100, Veeco) and surface profilometry (Dektak II, Sloan Technologies). The pSOI wafer, created using LPCVD, was found to have a surface roughness of 14 µm which prevented sufficient amounts of Van der Waals attractive forces to be generated upon contact to result in bonding. In-house chemical mechanical polishing (Poli-400L, G & P Technologies) and outsourcing to an external vendor for servicing (Entrepix Inc.) was used to bring the roughness of the poly-silicon membrane down, to $R_{RMS} < 1\ nm$. Table 2 provides surface measurements of the pSOI device layer.

Table 2- pSOI Surface characterization

Surface Treatment	Δz [nm]	R_{RMS} [nm]	R_a [nm]
None	-	14.6	11.3
Poli-400L in-house CMP	18.9	3.35	2.62
Entrepix® CMP service	6.8	0.8	0.97

Polished pSOI wafers exhibited some local regions of bonding, as shown in Figure 14, these wafer stacks were not robust enough to yield any testable samples. Non-destructive IR images show multiple small regions of local bonding. The destructive analysis shown in Figure 14 (b - d) shows regions where the Si device layer bonded strongly in certain regions and remained adhered to the ridge wafer after the two wafers were separated. Figure 14 (e & d) shows the cross section of a membrane suspended on an array of ridges. With weak bonding at the contacts along the ridges, stresses in the device layer and box layer caused the membrane to ripple and periodically detach. The capillary pressure generated by the nanopores and a liquid interface resulted in the membrane completely ripping off on a device such as this.

Wafer bow and surface waviness were the likely obstacles to full bonding. Switching to a true single crystal Silicon on Insulator (SOI) substrate for the membrane improved bonding yield (purchased commercially from Soitec; 6" diameter, 1 μm polished Si on a 1 μm SiO_2 (BOX) layer, on a 625 μm handle, fabricated using the Smart Cut® process). Due to sourcing limitations, both substrates were switched to 6" wafers. The size increased allowed for the incorporation of more devices per wafer after a mask revision. Figure 15 portrays successful bonds using 6" SOI wafers for the nanoporous membranes that arrive with a prime surface.

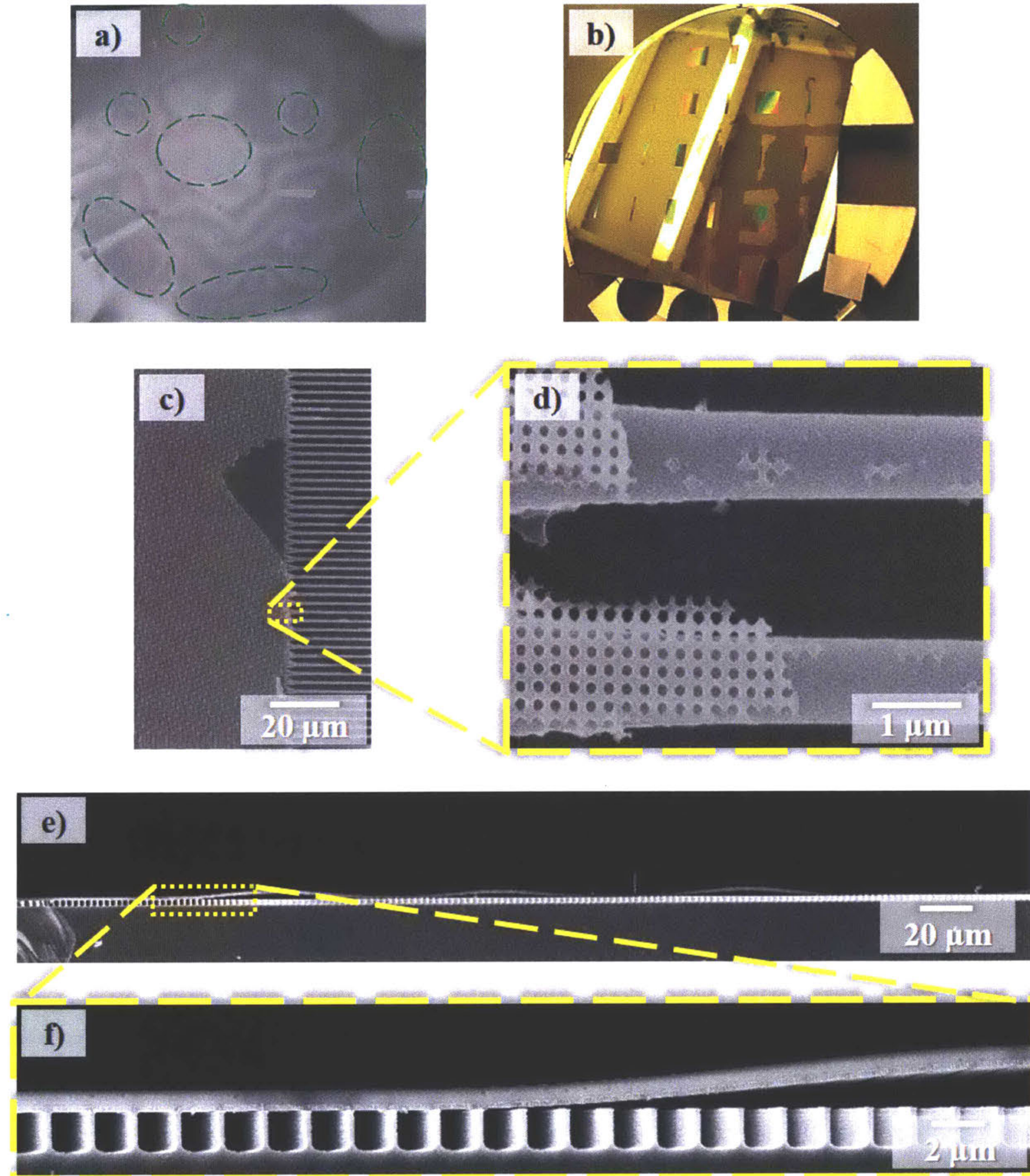
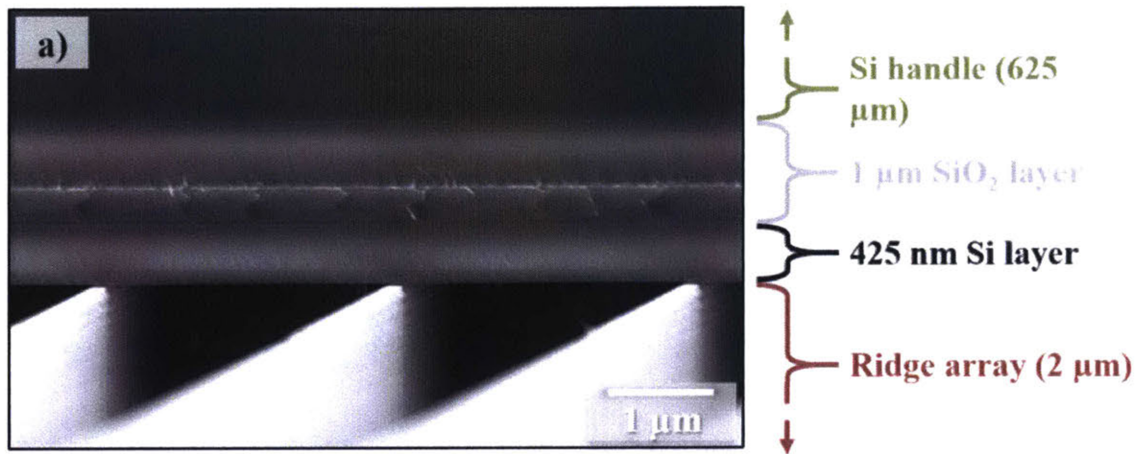
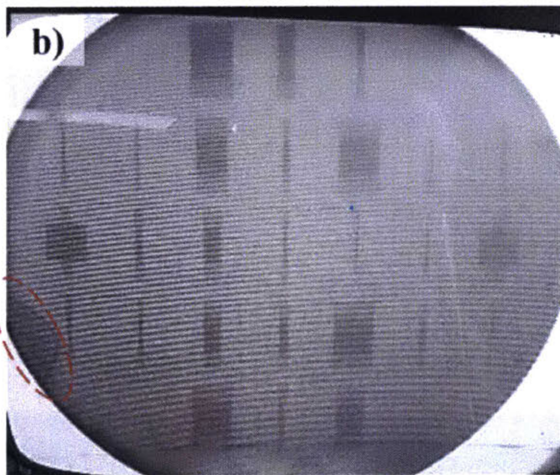


Figure 14- Partial pSOI membrane bonding. a) IR image of unetched 4" pSOI wafer bonded to a 4" prime DSP Si wafer. Due to the topology of the pSOI, only local maxima of the wafer could get close enough to the nominally flat DSP wafer. Outside of these small regions of contact, the concentric pattern highlighted in the image represent the gap between the wafers. b - d) After bond failure and separation of the two wafers, regions of strong bonding were identified, under optical and SEM micrography, due to sections of the membrane ripping off of the pSOI and transferring to the ridge wafer.





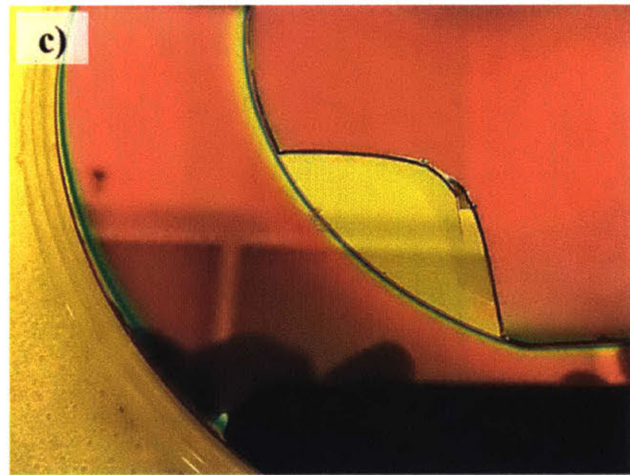


Figure 15- Examples of SOI bonded wafers. a) SEM image after destructive cleaving of a bonded SOI wafer (shown as a cross-section) without pores to a ridge wafer (shown as an oblique top view). b) IR image of a bonded 6" SOI wafer stack. The fringing pattern selected in the bottom left is only IR- resolvable non-bonding region (Note: the fringe pattern predominant at the bottom of the image is just an artifact from the IR station's CRT screen). c) 4" SOI wafers had some success in bonding to 6" SI ridge wafers, but were more likely to chip at the edges due to bending moments from the clamping of the disparately sized wafers together. (Note: the right angle visible in the missing section 4" wafer is the SI device layer that border's a single plenum.)

3.6 Residual stresses & thin-film dielectric deposition

Successfully bonded wafer stacks were found to be highly stressed. Figure 16 (a & b) shows the onset of fracturing in one of the two wafers during downstream processing of the bonded stacks. Figure 16 (a) shows a wafer stack after the anneal step where the DSP Silicon ridge wafer had fractured down the entire length.

Figure 16(b) shows a fracture that appeared in a die after wafer scale vapor channel etching. A mismatch in wafer bow is believed to be the likely cause. The Si ridge wafers remained nominally flat, with ~ 0 μm wafer bow throughout its individual processing. The Soitec SOI arrived with (+40) – (+100) μm bow on the device layer side. This bow is a result of the thermally grown 1 μm SiO_2 BOX layer.

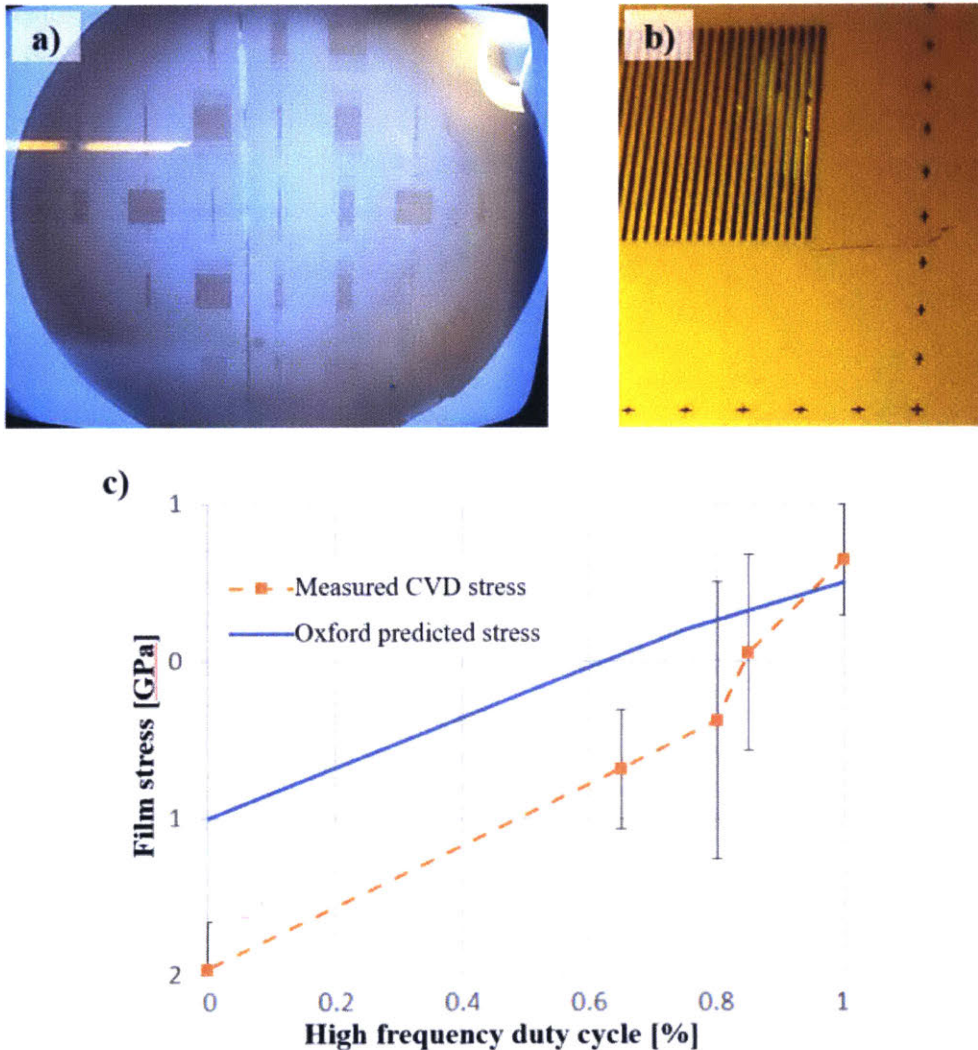


Figure 16- Stress related issues for the bonded wafer stack. a) Silicon wafer, likely under tension, fractured into two pieces after the fusing bonding process and anneal step for this 6" stack. b) Crack development on the order of 1 cm on the backside of the SOI wafer, likely under compression, during later processing (vapor channel etch).

After bonding, the final process called for metalizing the backside of the ridge wafer; depositing the heater and the sensing RTDs. The ridge wafer being a single crystal of electrically conductive Si required the deposition of a dielectric layer. This layer was originally designed to be Plasma Enhanced Chemical Vapor Deposited (PECVD) SiO_2. Silicon nitride, SiN_X (note the subscript x indicates that PECVD nitride is not sociometrically balanced- Si_3N_4), was found to be the preferred thin film dielectric layer. A summary of key properties for the PECVD dielectric layer materials is shown in Table 3.

Table 3- PECVD dielectric thin-film properties

		PECVD SiO_2	PECVD SiN_x
Breakdown voltage	[V/μm]	600 – 1,060	300 – 1,050
Thermal conductivity	$[W/m\ °C]$	1.1	2.2 – 4.5
Coefficient of thermal expansion	$[\mu m/m\ °C]$	2.2 – 2.6	3.3
Film stress	[MPa]	(−500) – (−250) always compressive	(−1,000) – (+500) compressive or tensile

SiO_2 has coefficient thermal expansion (CTE) value close to that of the Si substrate, 2.6 $\mu m/m$ °C, which reduces the likelihood of mechanical failure of the device due to a reduced CTE mismatch. SiN was found to have roughly the same breakdown voltage, but the ability to control the film stress by varying the high frequency duty cycle of the PECVD deposition process was key to relieving the stress issues alluded to earlier. SiN was deposited using a PECVD process selected on a case by case basis for each wafer stack based on the initial wafer bow of the stack. This allowed for the deposition of stress-free or stress-relieving dielectric layer. Figure 16 (c) presents the stress-deposition process relationship used in this study, shown in orange. The Silicon Turnkey Solutions PECVD tool was found to have a relation slightly different from

that described in literature by tool manufacturers. The relation was calibrated empirically using the Stoney Equation shown below, to calculate the deposited thin-film stress, σ_f, from the change in wafer bow (FLX-2320, KLA-Tencor Corporation) attributed to a thin film.

$$\sigma_f = \frac{E_s}{6(1-\nu)} \frac{(t_s)^2}{t_f} \kappa \tag{9}$$

where $E_s$and ν are the Young's modulus and poison ratio of the substrate, t_s and t_f are the thicknesses of the substrate and the deposited film respectively, and κ the curvature of the wafer.

3.7 Bimetallic proxy heaters metallization

Thin film heaters were deposited on the backside of the silicon wafer as a proxy for high heat flux generating integrated circuitry. In order to generate high heat fluxes, relatively high electrical resistance platinum was deposited as serpentine patterned heaters. High resistance can have the undesired effect of heating up the connections to the heaters, leading to heat generation outside the target area of the device. During the 7" mask redesign process, a second metal layer over the connectors was introduced to the process plan in order to reduce the resistances of these connections. Relatively low electrical resistance gold was chosen for this layer. A gold top layer on the contact pads offered the additional benefit of facilitating gold wire-bonding, which is extremely difficult with Pt contact pads. Schematics of a section of the heaters and temperature probes of the original and bimetallic are shown in Figure 17(a & c). The heaters were patterned as 50 μm wide serpentine traces. The RTDs were interspersed over across the heated section of the dies. The original RTDs were all 2 μm serpentine features. Wafer wide uniformity of the 2 μm RTDs tended to be less than 50% due to the variations in the photolithographic tooling (light intensity, hot plate temperature/contact uniformity). Half the RTDs in the redesign where changed to have 3 μm serpentine traces, which had 100% yield, however they were less local as their footprint had to be increased to maintain the same resistance. Figure 17(a - d) highlights the changes described.

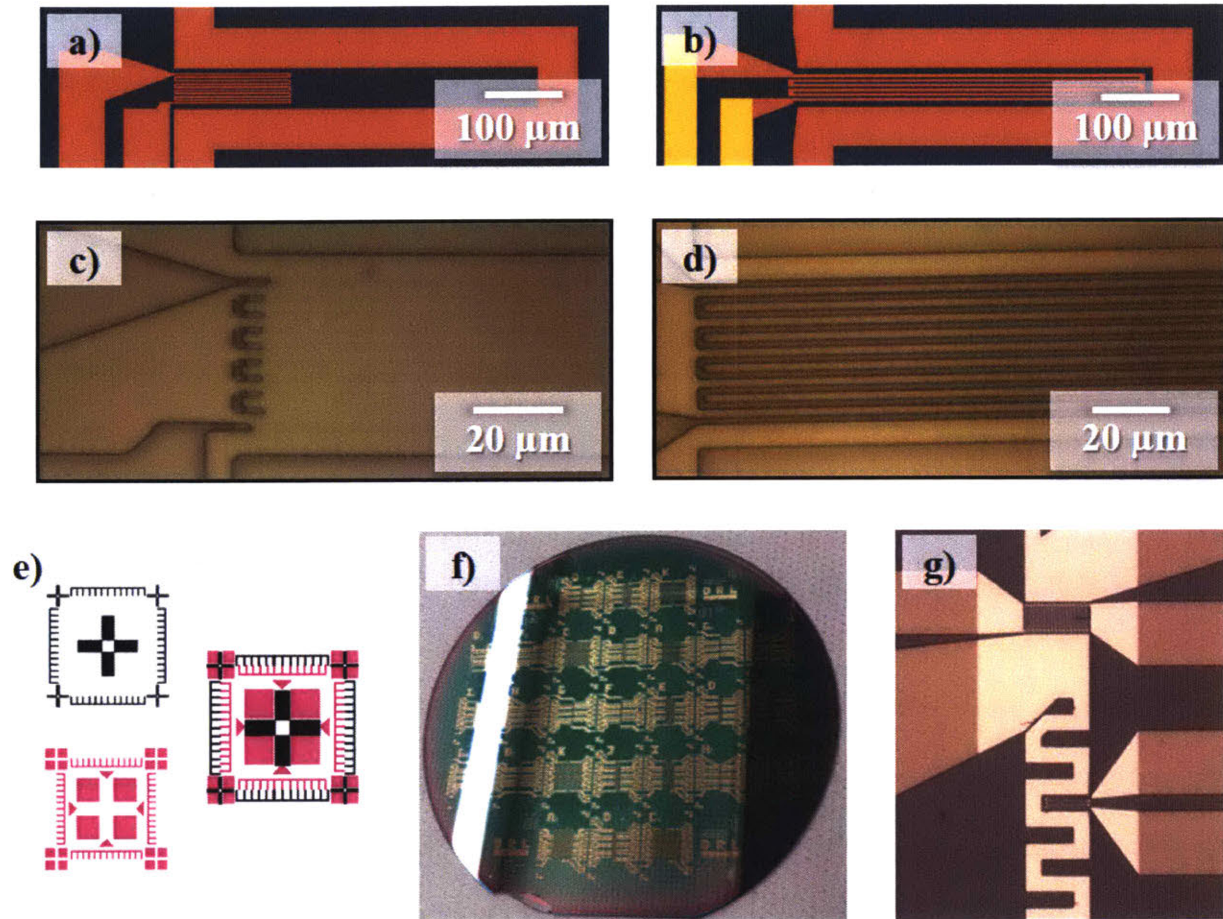


Figure 17- RTD design modification. a & b) Schematics showing the original platinum (shown in red) RTD design and the bimetallic approach, which has a layer of gold (shown in gold) deposited on the heater and probe lead wiring. c) Original platinum thin film design had only 2 µm wide traces for the RTDs, which due to wafer scale variably had low yield. d) Half of the platinum RTDs in the updated design had 3 µm wide traces which had a 100% yield with a slight loss in spatial resolution. e) The two thin film deposition layer masks incorporated Vernier markings to achieve higher alignment accuracy to safeguard against rotational misalignments which could result in short circuiting even when very small. f & e) Wafer and die scale optical images of the final metallization.

The negative tone mask set for the metallization process incorporated a number of beneficial design changes. The proportion of the resistance of each RTD, compared to the completed circuit was kept above 92%, in order to have a strong signal to noise ratio. Tapers and fillets were introduced to eliminate all sharp angles within the metal thin films in order to reduce constriction resistance in the current flow and to increase uniform heat generation in the desired locations, i.e., directly near the exposed membranes under the vapor channels. Finally, in order to ensure the gold leads would not short out the Pt heaters, due to

misalignment, an improved alignment mark was incorporated, shown in Figure 17(e). This pattern relied on Vernier marks and allowed for less than 1 μm misalignment.

The bonded and annealed wafers stack had 500 nm thick SiN dielectric layer deposited on the backside of the Si wafer. Next, 3 μm of negative-tone resist (NR71-1500PY, Futurrex) was spin coated on to the SiN layer. The NR7100-PY series of resist was used due to its characteristic undercut sidewalls, which are tailored for the lift-off process, and because of its high temperature stability. After a 30 min prebake at 150 °C, the wafer was exposed with the overall circuitry pattern, which included heaters, resistance temperature detectors (RTDs), and the connecting leads and contact pads. The resist was then developed in RD6 developer from Futurrex. To promote adhesion of the metals to the nitride layer, the patterned wafer was briefly exposed to oxygen plasma to remove any residual photoresist scum.

Electron beam physical vapor deposition (EBPVD) was used to deposit 25 nm Ti as an adhesion layer and 200 nm of platinum (VES 2550, Temescal Semiconductor). The lift off was completed by removing the non-patterned metal and photoresist in heated resist remover (RR41, Futurrex). To reduce noise and drift in the platinum RTDs thermal response, the piranha-cleaned and O_2 plasma-cleaned wafers were annealed for 3 hours in N_2 at 300 °C. NR71-1500PY was then spun on again, and the process was repeated for the deposition of 40 nm of Ti as an adhesion layer for 400 nm of gold over just the contact pads and leads. Another 500 nm of SiN was blanket deposited over the whole metalized wafer for insulation. Figure 17(f & g) shows a top view of the final metallization scheme. A not-to-scale representation of the dielectric and metal deposition thicknesses is provided as a cross-sectional schematic in Figure 18(a). Figure 18(h & i) provides an SEM cross-section of the leads.

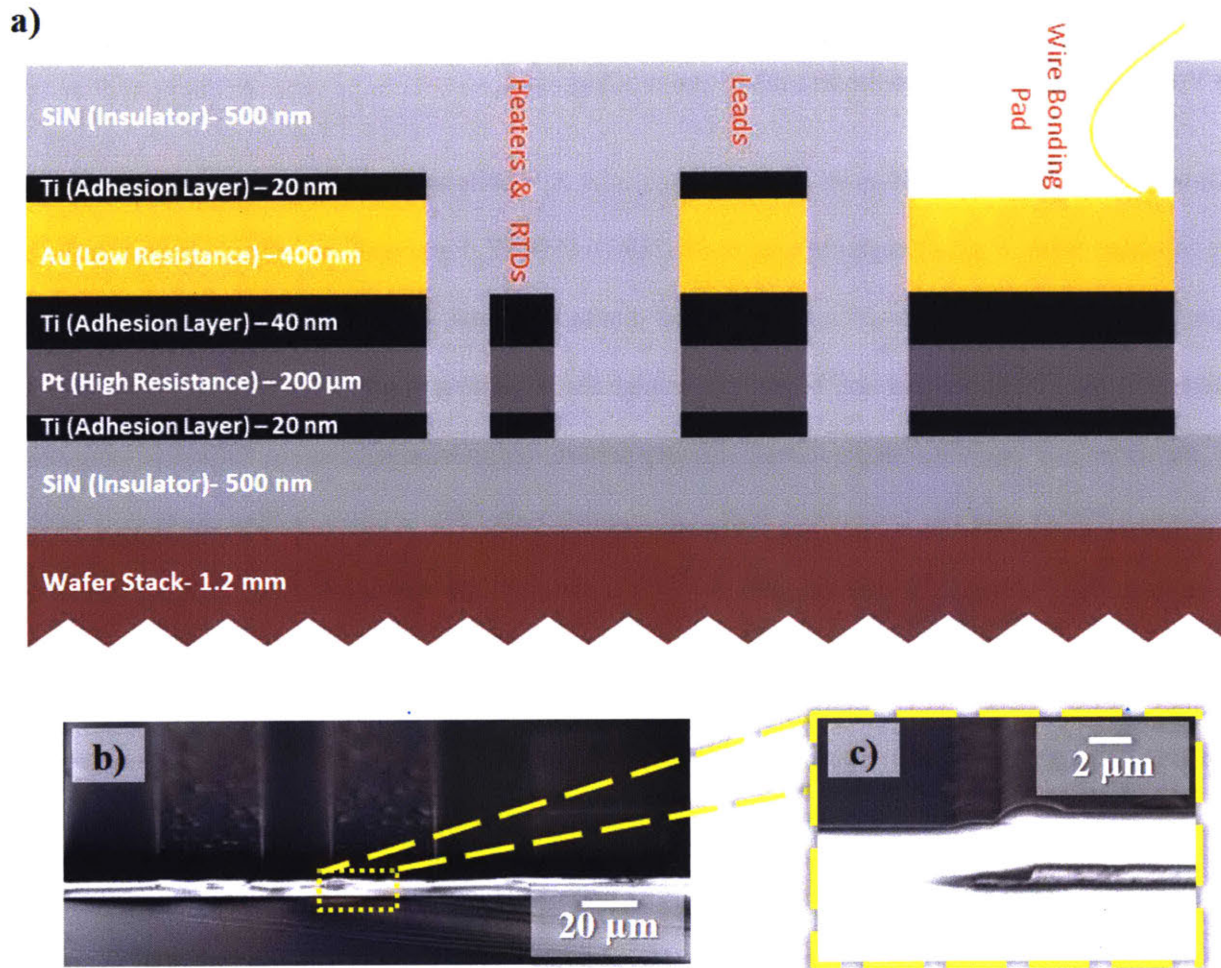


Figure 18- Cross-section of the final metallization depositions. a) Schematic diagram of the proxy heaters sandwiched within SiN for electrical insulation. A base layer of platinum was used for heating and sensing the device. A second layer of gold, was selectively deposited on top of the connectors to ensure that heat flux was generated in targeted locations, and in order to maintain a good signal to noise ratio on the RTDs. b & c) SEM cross-sections of the bimetallic leads.

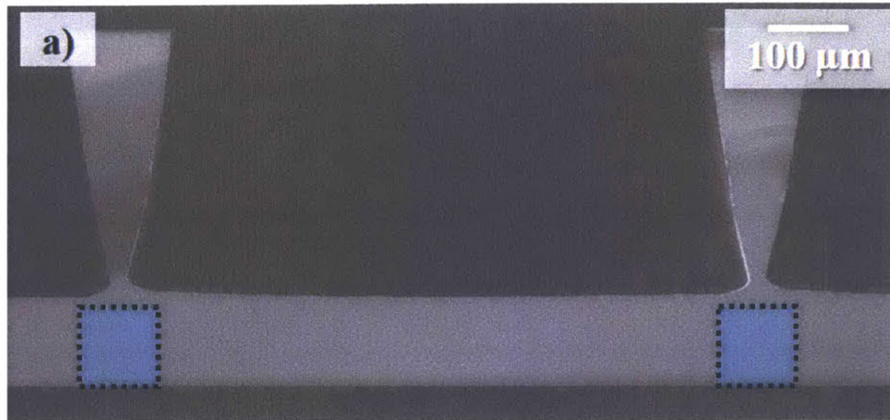
3.8 Vapor channel etching

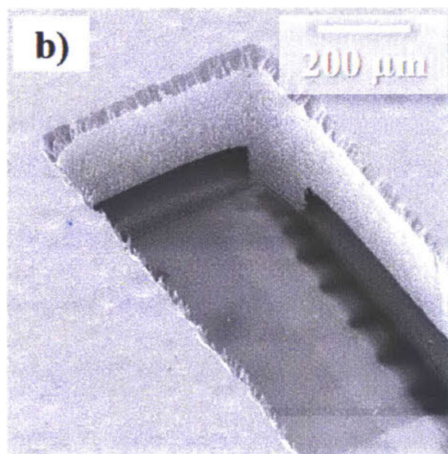
With the liquid pathways of the device fabricated and the thin film proxy heaters and sensors well defined, the final crucial step was to expose to supported nanoporous membrane and provide the generated vapor an exit path from the device, i.e., the vapor channels. Given the high aspect ratio of the membrane (length/width of an unsupported section of membrane versus thickness of the membrane), the membrane itself was very fragile. Using the BOX layer again as an etch stop, the process of exposing the membrane was broken into two distinct steps.

First, the handle of the SOI (silicon-on-insulator) wafer was etched down. The process for this step was very similar to that of the liquid manifold etch, on the other side of the SOI. The sample was coated in thick resist and etched with DRIE. The vapor etch was four times deeper than the liquid, as it had to go through the entire thickness of the 675 μm SOI handle. The extended depth of this etch, coupled with charge and thermal effects resulting from having multiple wafers between the platen holding the wafer and the etch plane, made this process very sensitive to a number of parameters, and can easily over etch laterally, as shown in Figure 19(a). The blue overlaid rectangles roughly highlight the location and size of the liquid channels, not present in this trial. This wafer was etched using the same process as that used to etch the liquid manifold channels.

The designed wall thickness between the vapor channels and the liquid channels was 50 μm. This provided a maximum negative etch profile angle of 4.58° before a lateral breach was formed connecting the liquid and vapor channels. Although deep reactive ion etching was designed to remove large amounts of Si, it is rare that the vertical etch is perfectly normal to the surface of the wafer. As the etch gets deeper, the availability of the reactants at the bottom of the features started to vary, especially if there were large variations in the feature sizes being etched. The progressive widening of etch feature results from the reactive ions etching the lateral side walls.

If the side barrier was breached, the pressure differential between the two channels would guarantee that the working fluid would leak out and flood the membrane. Therefore, lateral etching more than 50 μm would be a critical device failure. Figure 19 (b & c) shows two different refinements that reduced the lateral etching, but still resulted in a breached side wall.





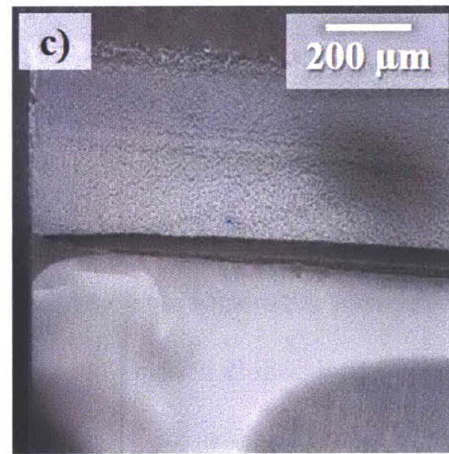


Figure 19- Vapor channels etch defects. Lateral breach of the side wall that separates the liquid manifold channels and the vapor channels would result in critical device failure. a) Schematic overlay of liquid channels on a SEM cross-section of vapor channels with excessive lateral etching. b & c) SEM image looking down into etched vapor channels using various etch tools. The 50 μm dividing wall between the vapor and liquid channels is etched away.

A successful etch process was developed by lowering the pressure and reducing the length of the pulsing etch step during the Bosch process, and by improving the thermal ground during the etching process. Figure 20 provides an example of a vapor channel etch without detrimental lateral etching.

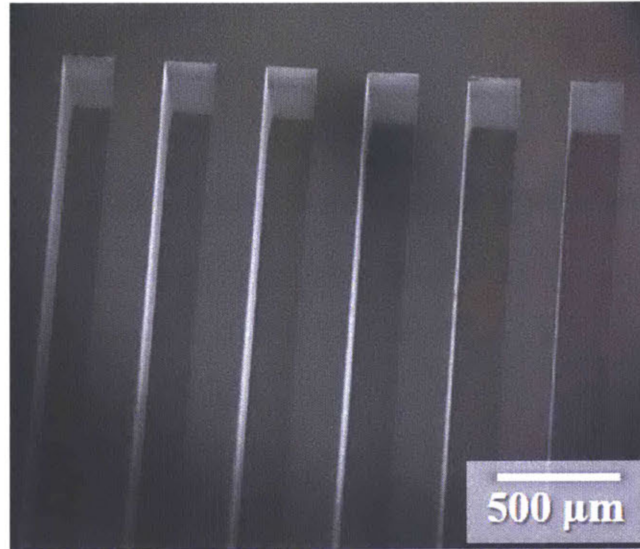


Figure 20- Final vapor channel etch. Oblique top view SEM image of a multi vapor channel device showing no critical breach between the liquid supply and the vapor outlet.

The buried oxide layer protecting the device layer was dry etched using CHF_3 plasma. This etch was very non-uniform and initially over-etched the vapor channel, shown in Figure 21(a). Even though CHF_3 plasma exhibited good selectivity for etching oxide over Si, the non-uniformity across the width of the vapor channel was still able to etch through the 1 um of silicon, destroying sections of the membrane Figure 21(b & c).

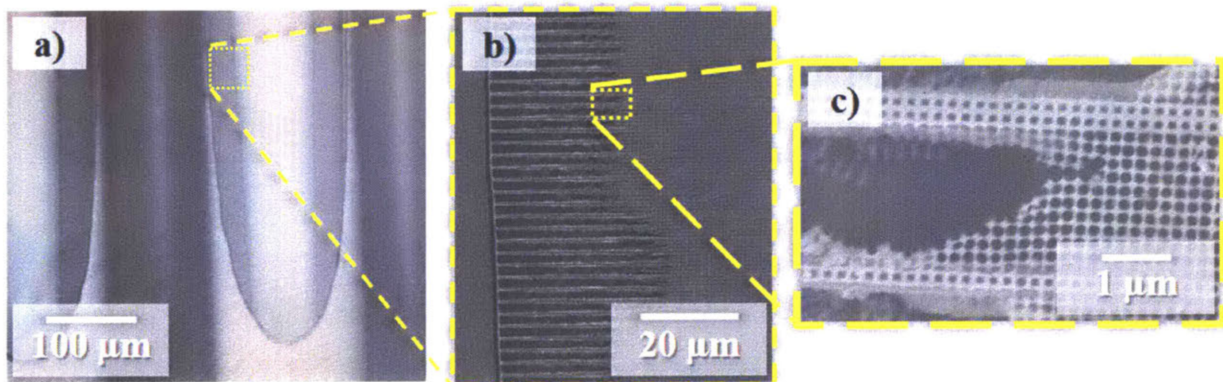


Figure 21- Buried oxide layer etch rate non-uniformity. Etch rate of preliminary process for oxide removal of mounted devices was slower in the center of the channel than the edges. This resulted in oxide remaining in the center of the channel, while the membrane underneath was completely etched away, even though the etch selectivity for silicon dioxide was orders of magnitude higher than silicon.

Once etched through the oxide, it was discovered that this particular sample did not have the pores etched through the entire thickness of the silicon device layer. An additional Si dry plasma etch was developed using SF_4 RIE etching. This etch, shown in Figure 22, exhibited the inverse etch non-uniformity. The center of the vapor channel etched faster than the sides. Inserts (b - d) show the resulting surface of the membrane. Pores showed a gradient in diameters, with completed closed pores at the edges of the channel, and at the center of the channel pores were fully open and about 110 nm in diameter.

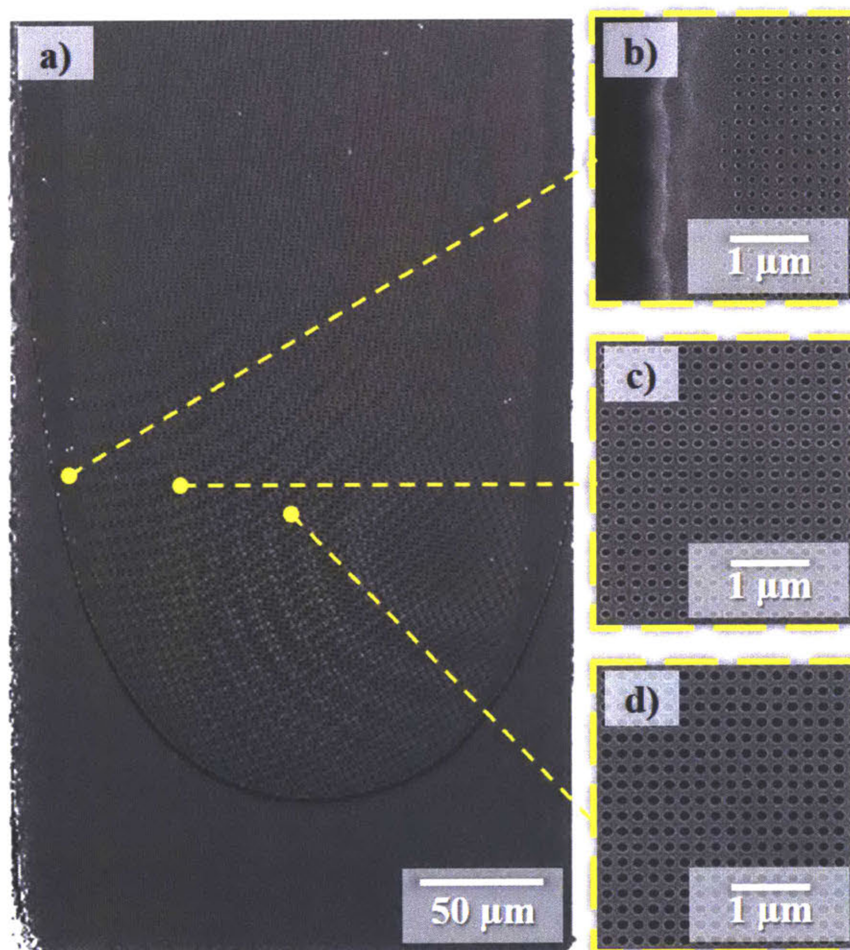


Figure 22- Exposed membrane with pore geometry variance. a) SEM top view of a single vapor channel. Etch rate disparities for the Si etched used to thin the nanoporous membrane down, created blocked pores and a gradient of pore sizes from the edge of the device to the center.

3.9 Final process plan

Iterative revisions, starting from the initial process plan presented in Figure 6, eventually resulted in a positive yield of completed devices. The final process incorporating all changes is shown schematically in Figure 23. The most drastic changes include: shifting to a higher quality substrate, selection of a stress-tunable dielectric material, revising metallization for improved localized heating and lower noise while sensing temperature, and reordering steps to preserve the integrity of the membrane and the hermeticity of the device until as late in the process as possible.

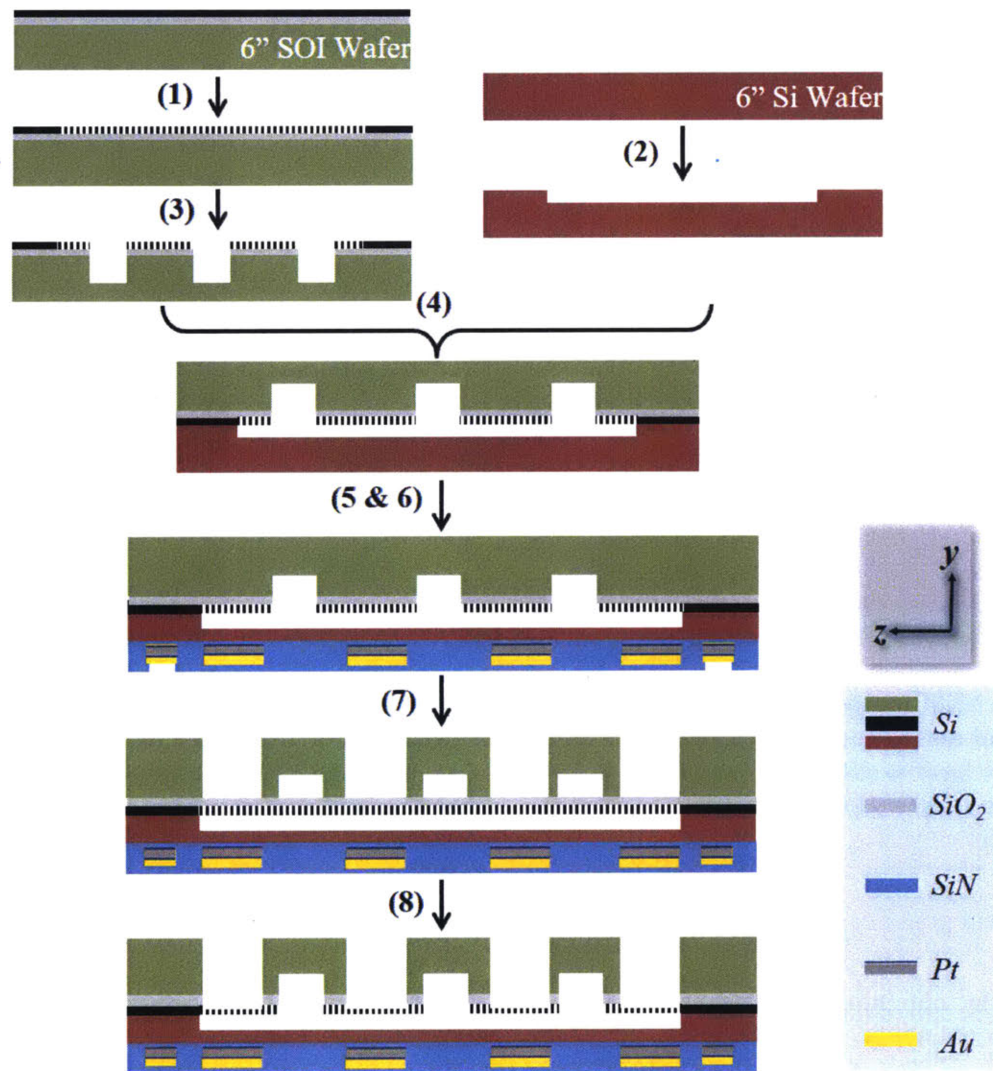


Figure 23- Schematic of the final micro-fabrication process. Cross section taken parallel to the ridge channels, along the xy-plane.

Examples of the fabricated hierarchical fluidic channels that help define this device features are shown in Figure 24.

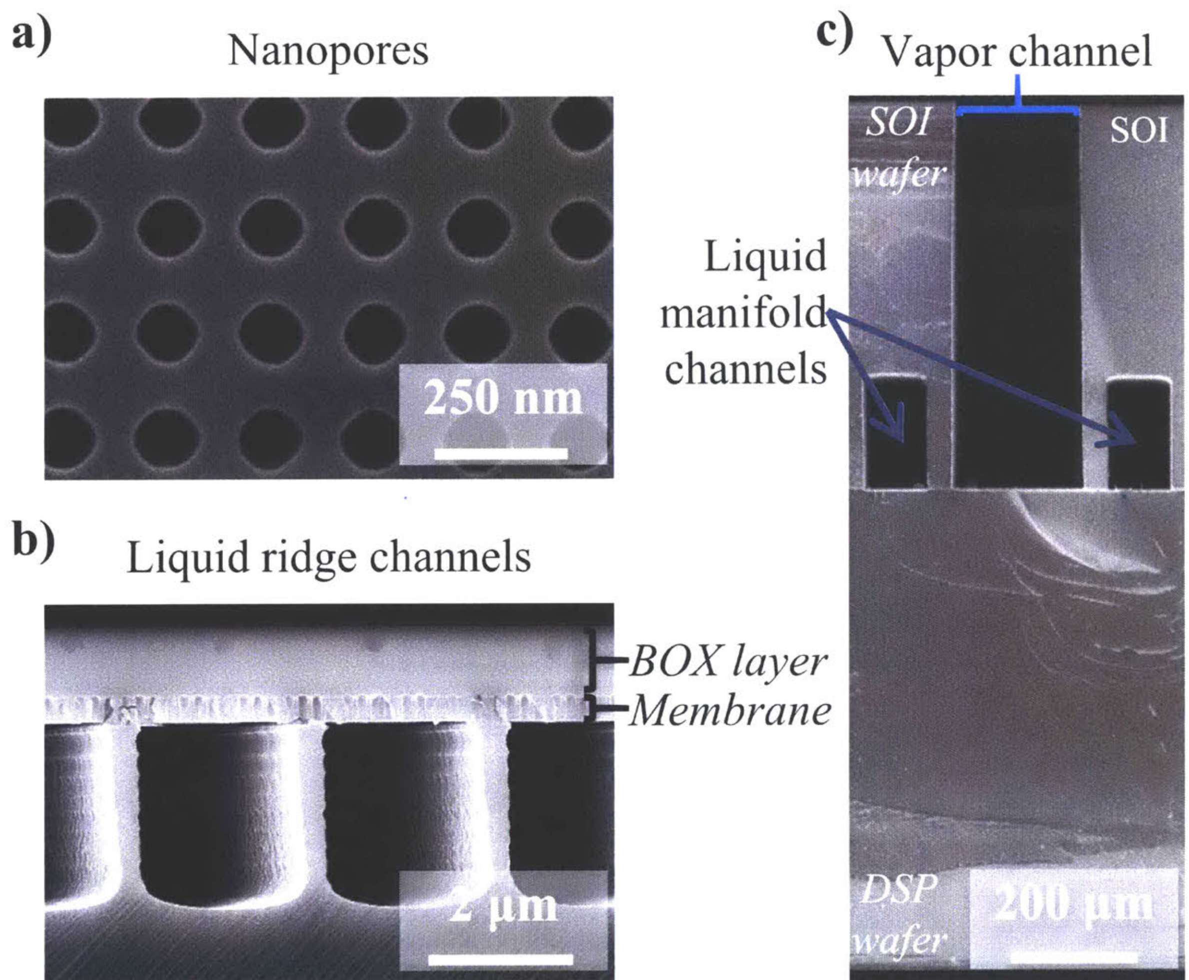


Figure 24- SEM images depicting successfully fabricated nano, micro, and macro- scale channels. a) Top view of nanopores, b) cross-section of a supported nanoporous membrane on liquid ridge channels (note: BOX layer is still intact), and c) cross-section of an entire device with a single 200 µm wide vapor channel between two liquid channels.

Chapter 4- Experimental Characterization & Analysis

Based upon the final process plan described in Chapter 3, samples from three wafers were fabricated to completion, and three more wafers were prepared for packaging. The experimental characterization described below, is for a single device; one of the first to be fabricated with the necessary components for testing. Hanks [47] performed an in-depth performance characterization and robustness assessment of nanoporous membrane enhanced evaporative cooling devices with varying geometries and operating with varying working fluids. The following device characterization was done in collaboration with him.

4.1 Device characterization

The test sample had two vapor channels, each 1 cm long × 200 μm wide, as shown in Figure 25 (a-b). The supported membrane had 130 nm pores (seen in Figure 25c). Upon removing the buried oxide layer, the nanopores were found not to have been etched all the way through the 1 μm thick silicon device layer. Reactive Ion Etching was used to remove ~350 μm, based on a timed etch, using a recipe calibrated on a new, prime, single side polished, silicon wafer, and the same vapor channel pattern.

Figure 25(d-f) shows the back side of the test device. Inlet and outlet liquid ports, and metalized proxy heaters and sensors can be seen.

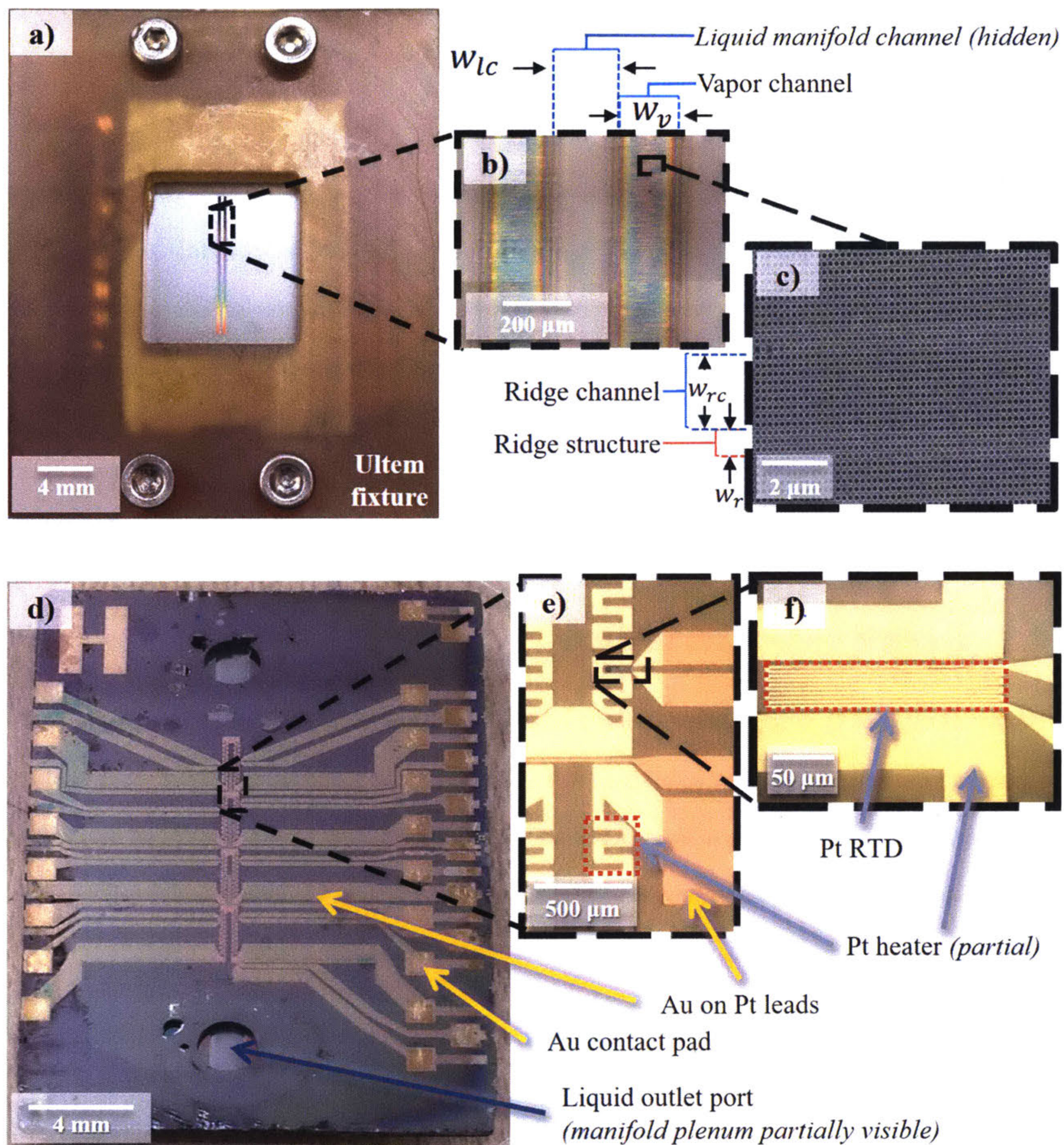


Figure 25- Optical and SEM images of tested device. a) Top view (vapor channel side) of the test device, mounted in an Ultem test fixture. b) Micrograph showing a partial section of the two vapor channels. c) SEM image of the supported membrane. Pores (160 nm) are visible and locations of the ridges discernable through the membrane. d) Bottom side view of the test device. Fluidic I/O, Pt heaters and RTD sensors, and bimetallic leads and contact pads all visible. e) & f) Micrographs at higher magnifications highlighting the different metalized features located underneath the microfluidic channels.

4.2 Device operation

The sample tested in this report suffered a mechanical failure during the die singulation process. Figure 25 (a & d) highlight a missing section of leads and contact pads for the device. In the top view, Figure 25 (a), six exposed gold pogo pins are barely visible underneath the top of the Ultem fixture. The bottom view, Figure 25 (d), shows a single row of contact pads one side off the device, instead of the designed two row of contact pads, as found on the right side of the device. This mechanical failure did not compromise the sealed open fluidic loop of the cooling device. However, it did prevent powering the heaters on half the device, and eliminated a majority of the RTD's. As an initial prototype the device was still characterized with a non-uniform heating pattern, shown in Figure 26. The bottom half of the device, with a total area of 0.2 cm^2, directly downstream of the inlet was powered, but the top half of the device did not have resistive heating directly below the nanoporous membrane.

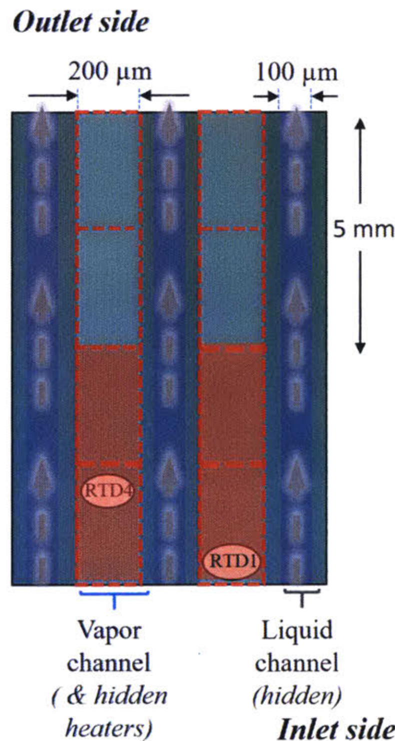


Figure 26- Non-uniform device operation. The bottom two heater zones were active during this experiment. Each heat zone comprised of two areas with 200 μm width and 2.5 mm length for a total area of 0.02 cm^2.

In order to account for heat spreading effects arising from the non-uniform heating and evaporation, the compact level model was rerun with test samples geometries and operating conditions described above. A computational solution of device performance at one operating condition is shown in Figure 27. Temperature and temperature gradients calculated from this static solution provided heat dissipation, and junction temperature rose (which together represent the heat transfer coefficient) for a particular operating condition.

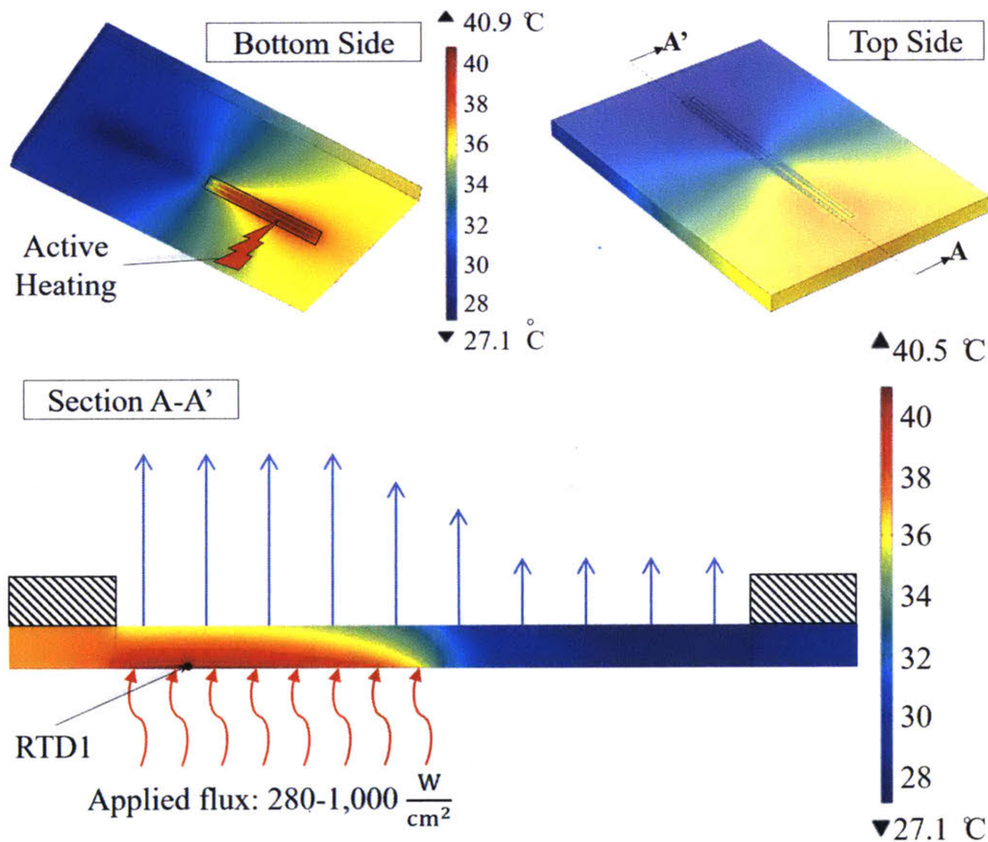


Figure 27- Compact model temperature profile for this non-uniform heating case. Compact model predictions for methanol were calculated across a range of applied heat flux under this non-uniform heating condition to verify and validate the model.

4.3 Methodology

4.3.1 Experimental apparatus

A custom designed experimental apparatus was manufactured for testing the prototype device in pure methanol vapor conditions. A schematic diagram of the test setup is provided in Figure 28.

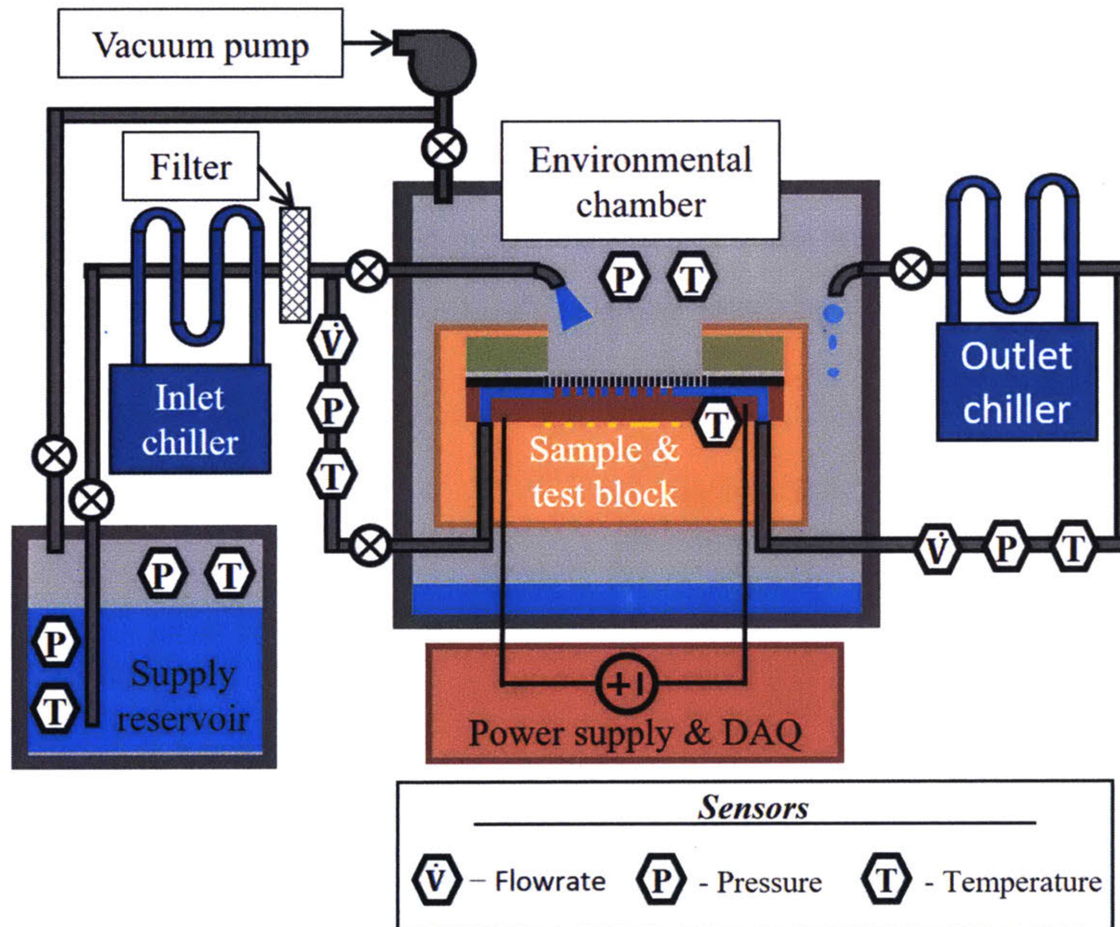


Figure 28- Schematic diagram of test setup. Slightly pressurized liquid from a reservoir tank was conditioned and pumped through the test device in a pure vapor environment. A portion of the liquid evaporated from the device with excess liquid flowing by and out of the chamber. Only a subset of sensors is presented.

Prior to any data collection, the sample was cleaned in O_2 plasma. The cleaned sample was mounted into a custom Ultem fixture with an array of pogo pins along with inlet and outlet tubing. Indium wire gaskets were used to create gas-tight seals, and tested with a helium leak detector.

4.3.2 Calibration

The functioning RTDs were calibrated to a thermocouple probe from room temperature to above 75°C inside the sealed and dry vacuum chamber. The chamber temperature was regulated using PID controllers and resistive band heaters fixed to the outside of the environmental chamber. Data was sampled at 1 kHz for 2 minutes at each temperature set-point after the camber reached steady state. Figure 29 below shows the linear least squared error fit used to calibrate one of the two RTDs. RTDs for raw data and adjusted data were in good agreement with one another, and had coefficients of determination greater than 0.995.

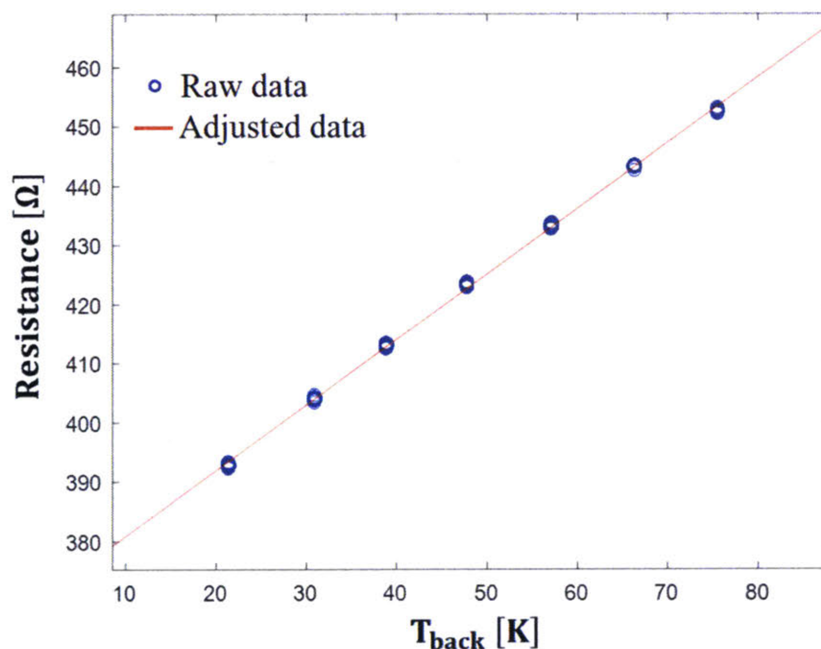


Figure 29- Sample resistance temperature detector (RTD) calibration.

4.3.3 Experimental procedure

Methanol was initially distilled and collected into the supply reservoir to improve purity. The supply reservoir was intermittently placed under vacuum until the vapor pressure reached the saturation pressure of methanol in order to degas the system of non-condensable gases. Each section of the system was then brought under vacuum, and the environmental chamber was filed with pure methanol. The reservoir was heated to 39°C to maintain a slight pressure head above the test chamber; this allowed saturated liquid to flow into the test device and eliminated the need for an external pump, which could have been a possible source of contamination. The liquid was then sieved through a 0.5 μm metal filter and subcooled using a chiller to prevent downstream nucleation. Temperature and pressure were measured prior to the liquid entering the chamber and the test device inlet. A portion of the liquid flow evaporated from the device and eventually condensed on the chamber walls. The remaining bypass liquid flowed out of the device. The outlet flowrate, temperature, and pressure were also measured. The liquid passed through a throttle valve used to control pressure in the liquid manifold, and was discharged back into the chamber. Control of liquid pressure in the manifold channels was critical to device operation: high pressures resulted in membrane flooding, and low pressures could potentially have resulted in nucleate boiling. To purge the membrane of residues left behind during evaporation between tests, the membrane surface was flushed with methanol from the reservoir using a mounted nozzle. Pressure and temperature measurements were taken within the liquid supply reservoir and in the pure-vapor filled chamber. The environmental chamber was kept in quasi-steady state by using the resistive band heaters to match the exterior of the chamber to the interior temperature, in order to minimize the effects of heterogenous condensation on the internal walls.

4.4 Data processing for heat loss characterization

For comparison to the model, evaporative heat transfer of the device was extracted from the overall power input to the heaters. The two major sources of non-evaporative heat dissipation were sensible cooling from the working fluid and conduction losses to the sample holder.

Sensible cooling. The heat transfer contribution of sensible cooling was measured and recorded as a lookup function given a measured inlet temperature (T_{in}), outlet mass flow rate ($\dot{m}_{out}$), and thermal heat capacity (c_p). The inlet flow rate ($\dot{m}_{in}$) was the sum of the outlet flow rate and evaporative flow rate. The outlet liquid temperature (T_{out}) was approximately equal to the substrate temperature due to a large internal heat transfer coefficient (~800 W/m^{2}K) in the manifold channels. The heat transfer by sensible cooling, normalized by the heat input area is:

$$q''_{sensible} = \frac{\dot{m}_{in} c_p (T_{out} - T_{in})}{A} \quad (6)$$

where A is the area of heat input. Typically, sensible cooling accounted for approximately 5% of total heat dissipation. The adjusted data for evaporation heat transfer is plotted and shown in Figure 30 (in blue markers).

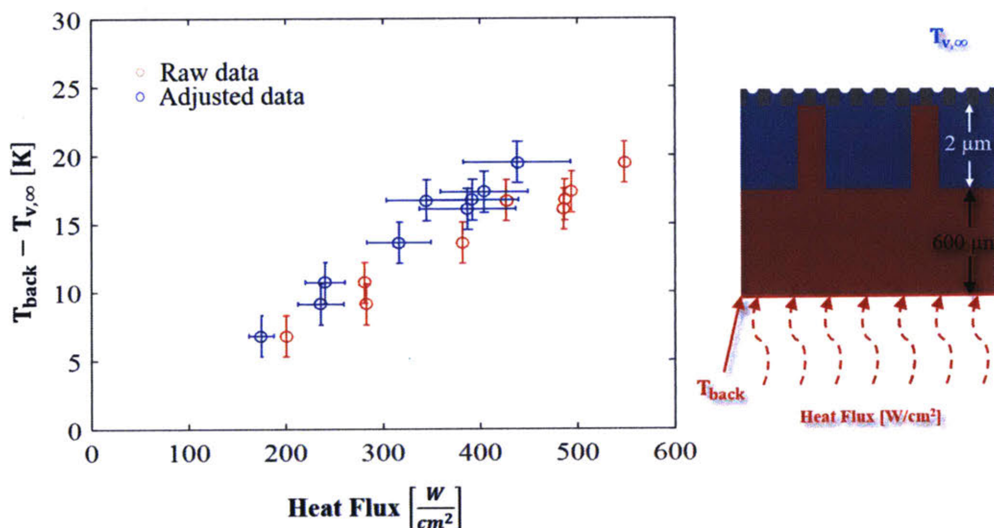


Figure 30- Data corrected for sensible cooling.

Conduction losses. Since the heater resistance is dependent on temperature, as thermal equilibrium is reached the input power changes slightly (~0.4% per degree). While the characteristic time to heat the sample was small (~1 s) the characteristic time to thermally saturate the test block was longer (~1000 s) since the test block was more massive and made from low thermal diffusivity Ultem polyetherimide. Therefore, the parasitic heat loss to the test block decreased over a period of several minutes, as shown in Figure 31. These data were generated by heating the sample during dry conditions, so that parasitic heat loss by conduction in to the test block could be estimated. For any given point of time and substrate temperature, the fraction of input heat that was conducted away from the sample could be estimated. For example, after a sample had been heated with 5.6 W for 180 s during evaporation, and reached ΔT=10 K above ambient, the conduction loss was 0.06 W/K meaning that 0.6 W of the input heat was conducted into the test block and only 5.0 W was dissipated by evaporation and sensible cooling. At $t \rightarrow \infty$, heat loss decayed to a steady state value (0.03 W/K).

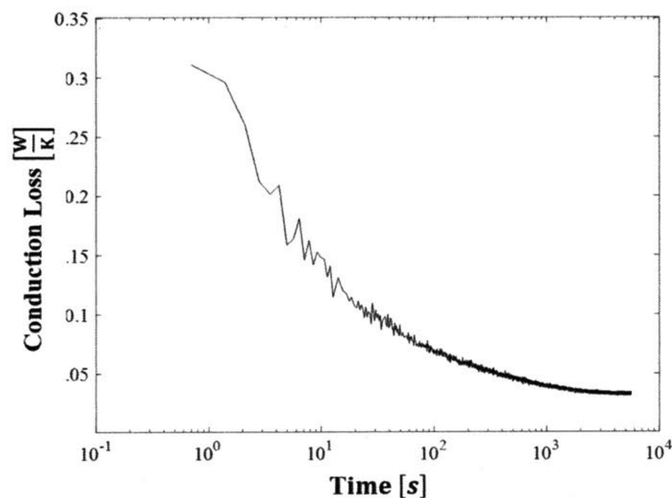


Figure 31- Transient parasitic conductive heat loss.

4.5 Results

The backside device temperature over a range of evaporative cooling of methanol at different corrected heat fluxes is plotted in Figure 32. A maximum evaporative heat flux using methanol as a working fluid of 412 W/cm^2, over 0.02 cm^2, at $\Delta T = 24.1$ K was recorded before nucleate boiling began in the manifold channels. The highest overall heat transfer coefficient of 20.1 W/cm^{2}K occurred at 168.8 W/cm^2 and $\Delta T = 8.4$ K, which includes an unnecessary conduction resistance in the substrate.

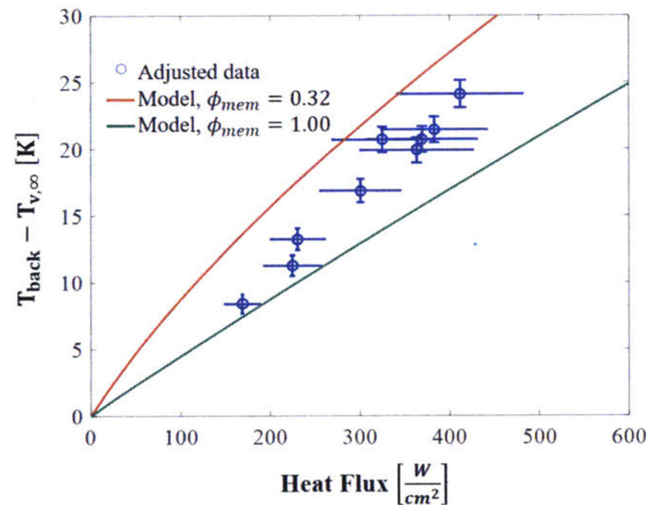


Figure 32- Evaporative heat removal performance. Experimental data for temperature rise plotted against input heat flux over 0.01 cm^2 compared to our model. The model is shown with two porosities at the liquid-vapor interface.

4.6 Discussion

From Figure 32, it is clear that there is some disagreement with the model developed. At high heat flux, there is better agreement with the predicted performance (shown in red, representing the exact geometries of the device tested, including a porosity of 0.32). At low heat flux however, the model under predicts the cooling performance. One explanation for this beneficial cooling enhancement may be nonidealities that arose during fabrication. The conjugate heat transfer model assumes a 2-D cylindrical pore, which when

arrayed creates a smooth planar membrane surface. In etching down the membrane to achieve a 600 nm thick membrane with fully open pores, the final nanoporous membrane tested had a 3-D structure. A SEM image comparison of the modeled membrane and the tested surface is shown in Figure 33. From non-uniform etching, conical pillars formed in between the membrane pores. This difference may allow the device to operate at near unity porosity at low heat flux (plotted in green in Figure 32), when the meniscus is stable and pinned at the tops of the pillars. One explanation for the mechanism behind this observation is as follows. During this highly wetting phase at low heat fluxes, higher than model predicted heat transfer coefficients can be obtained due to increased evaporative area (near a porosity of unity) and smaller thermal resistance across the fluid. As the applied heat flux is increased, the meniscus increases in curvature to maintain an adequate supply of methanol. This trend of increasing capillary pressure could not be sustained indefinitely, and eventually the meniscus would unpin and start to recede. During this transition, the fluid recedes to the original pore diameter where it is pinned once more, generating higher meniscus curvature, i.e., a smaller capillary radius. With the meniscus receded into the pore, the interfacial area is reduced to a porosity 0.32 as originally intended and the temperature response starts to migrate towards the dark red line, representing the modeled performance, and true porosity. This transition was observed around 300 W/cm^2 of applied heat flux. Schematics of these two operating regimes are shown in Figure 33.

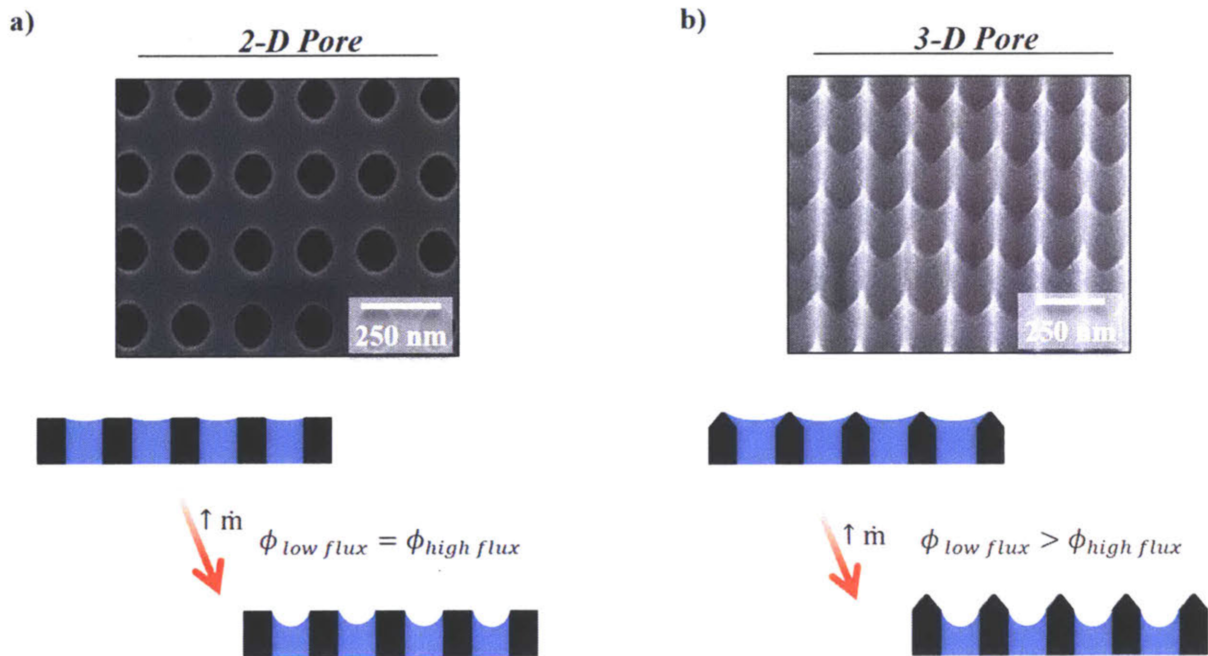


Figure 33- Possible explanation for performance deviation due to fabrication non-idealities. a) Menisci within constant cross-section pores stayed pinned with increasing evaporation until dry out. b) Menisci within narrowing pores at low heat fluxes were able to temporarily pin at artificially high porosities, ~100%, and cool at lower superheats, due to the increased interfacial area. With increasing transport, higher capillary pressures were needed and the effective porosity transitioned back to the nominal value of 32%.

In addition to the change in wetting morphology at the membrane surface, the trend may also be related to the accumulation of non-evaporation residue in the membrane pores. The transition is not uniquely due to contamination because the rise in temperature would be exponential with heat flux, rather than decaying to a linear trend as observed. Further experimentation is needed to elucidate the transitional behavior at high heat flux.

In applications using GaN power amplifiers, the substrate thickness is significantly smaller than the 650 μm of silicon used in the current study. Eliminating the temperature rise associated with the conduction resistance of the substrate, the validated compact model predicts that evaporating methanol can dissipate 1 kW/cm^2 with a temperature rise of 32.4 K, for a corresponding to h = 30.8 W/cm^{2}K. Even higher heat transfer coefficients are predicted when using working fluids with higher surface tension, higher heat

capacity, and lower viscosity. In Figure 34, the predicted backside device temperature over a range of evaporative cooling for different working fluids is shown. Using R245fa, 1.35 kW/cm^2 of heat can be dissipated with a temperature rise of 26.9 K, corresponding to $h = 50.1$ W/cm^{2}K.

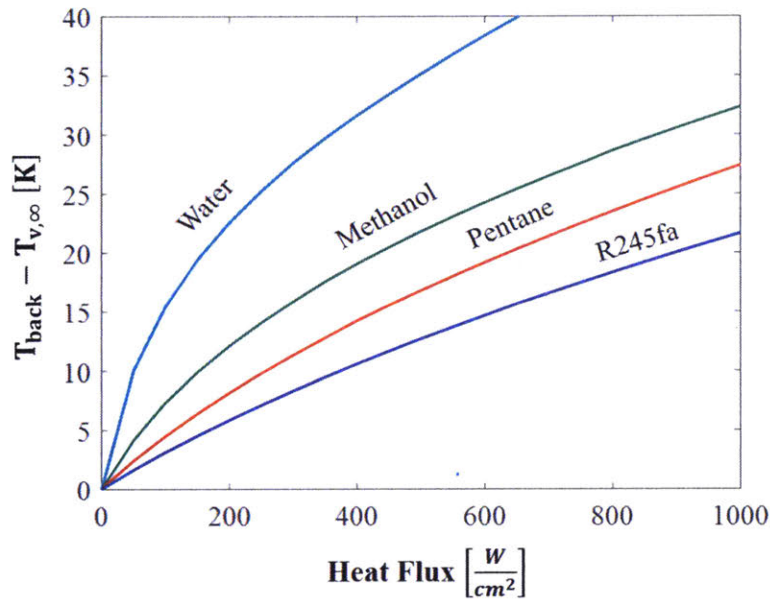


Figure 34- Compact model predicted test sample evaporative cooling for a variety of working fluids. This simulation neglects conduction resistances of a thick substrate, but assumes a supported membrane structure identical to the one that we have fabricated.

Chapter 5- Conclusion & future work

A high-heat flux embedded thermal management device was fabricated and characterized. The monolithic silicon device dissipated heat by evaporating within a thin-film regime supported nanoporous membrane.

Experimental sample fabrication used photolithography, dry chemical etching and fusion bonding. The membrane pores were patterned using interference lithography and etched into an SOI wafer to yield large arrays of highly uniform pores. The SOI wafer was bonded to an array of etched ridge microchannels. Thin film metal heaters and RTDs were deposited by e-beam evaporation and lift-off.

Fabricated samples were characterized in a custom built environmental chamber with methanol as the working fluid. The highest heat dissipation rate achieved was 412 W/cm^2, over 0.02 cm^2, at $\Delta T = 24.1$ K. The highest overall heat transfer coefficient of 20.1 W/cm^{2}K occurred at 168.8 W/cm^2 and $\Delta T=8.4$ K.

A system-level compact model was developed to capture sub-continuum, non-equilibrium physics of evaporation and predicted device performance over changing parameters and operating conditions without the computational expense of simulating every detailed nanoscale feature within the device.

The validated model with optimized parameters predicted other materials and geometric combinations that can further increase heat removal and lower device temperatures. These include reducing the substrate thickness, increasing the membrane porosity, switching to higher conductive semiconductor substrates, and switching to more volatile dielectric working fluids. Lowering the silicon substrate thickness to 100 μm, increasing membrane areas, and evaporating dielectric fluids, such as R245fa, are predicted to increase heat dissipation rates to 1.33 kW/cm^2 with heat transfer coefficients increasing to 50.4 W/cm^{2}K.

This study characterizes a proof of concept device that leverages thin film evaporation and a biporous fluidic supply for high heat flux dissipation. One device, with a specific set of geometries, operating with a single working fluid was characterized, leaving many avenues of future research.

Characterizing a parametric sweep of geometries and working fluids is needed to more robustly validate the model presented. Accurate prediction of suboptimal geometries and working fluids can further confirm that the relevant underlying physics have been captured by the model. Increasing confidence in the model's predictive capabilities and the applying it to optimize across a wider design will allow the maximization of the potential of nanoporous thin film evaporative cooling. Optimal operating conditions, which includes selecting the best working fluid, for a given application, should also be investigated to capture the predicted maximum heat fluxes and heat transfer coefficients that motivate the technology. Metrics beyond pressure drop and heat transfer performance must also be considered as they may limit the implementation- e.g. flammability, toxicity, environmental sustainability, and electrical conductivity may all factor into whether a peak performance reached by a working fluid is meaningful.

Nanoporous evaporative cooling, as demonstrated in this study, still has a low Technology Readiness Level (TRL 2-3). This technology will be of limited use unless it can be shown to handle real world challenges which may include i) non-uniform heating with dramatic thermal gradients, ii) hot-spot mitigation, iii) system size limits that create vapor removal bottlenecks, iv) compatibility/feasibility of incorporating this strategy on actual high power/high performance ICs, and/or v) the need for a closed loop design (the device presented in this study does not have interchip/compact condenser).

Finally, reliability of a system level nanoporous evaporator is a crucial area of study not discussed in this thesis. Preliminary evidence indicates that, for the current design, the mean time to failure (MTTF) is prohibitively short, due to clogging. Even with careful distillation of a working fluid, due to the length scale of the nanopores, ever present, soluble, non-volatile contaminants can eventually accumulate in the evaporating nanopores. Hanks presented a diffusion based model to justify a redesigned flow configuration that takes advantage of concentration gradients to prevent clogging in the nanopores [47]. Experimental demonstration of a sustainably evaporating membrane, such as the one he outlined, should be an immediate research goal.

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