GaN-based Vertical Power Devices

by

Yuhao Zhang

B.S., Peking University (2011)
S. M., Massachusetts Institute of Technology (2013)

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Signature of Author: …………………………………………………………
Department of Electrical Engineering and Computer Science
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Certified by …………………………………………………………………
Tomás Palacios
Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Accepted by …………………………………………………………………..
Leslie A. Kolodziejski
Professor of Electrical Engineering and Computer Science
Chair, Department Committee on Graduate Students

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Abstract:

Power electronics based on Gallium Nitride (GaN) is expected to significantly reduce the losses in power conversion circuits and increase the power density. This makes GaN devices very exciting candidates for next-generation power electronics, for the applications in electric vehicles, data centers, high-power and high-frequency communications.

Currently, both lateral and vertical structures are considered for GaN power devices. In particular, vertical GaN power devices have attracted significant attention recently, due to the potential for achieving high breakdown voltage and current levels without enlarging the chip size. In addition, these vertical devices show superior thermal performance than their lateral counterparts. This PhD thesis addresses several key obstacles in developing vertical GaN power devices.

The commercialization of vertical GaN power devices has been hindered by the high cost of bulk GaN. The first project in this PhD thesis demonstrated the feasibility of making vertical devices on a low-cost silicon (Si) substrate for the first time. The demonstrated high performance shows the great potential of low-cost vertical GaN-on-Si devices for 600-V level high-current and high-power applications.

This thesis has also studied the origin of the off-state leakage current in vertical GaN pn diodes on Si, sapphire and GaN substrates, by experiments, analytical calculations and TCAD simulations. Variable-range-hopping through threading dislocations was identified as the main off-state leakage mechanism in these devices. The design space of leakage current of vertical GaN devices has been subsequently derived.

Thirdly, a novel GaN vertical Schottky rectifier with trench MIS structures and trench field rings was demonstrated. The new structure greatly enhanced the reverse blocking characteristics while maintaining a Schottky-like good forward conduction. This new device shows great potential for using advanced vertical Schottky rectifiers for high-power and high-frequency applications.

Finally, we investigated a fundamental and significant challenge for GaN power devices: the lack of reliable and generally useable patterned pn junctions. Two approaches have been proposed to make lateral patterned pn junctions. Two devices, junction barrier Schottky devices and super-junction devices, have been designed and optimized. Preliminary experimental results were also demonstrated for the feasibility of making patterned pn junctions and fabricating novel power devices.

This Supervisor: Tomás Palacios
Title: Professor of Electrical Engineering and Computer Science

Acknowledgement

The past six years are a very important period in my life. The trainings I received at Palacios' group at MIT not only makes me a better academic researcher, but also makes me mature as a person with better personality, insights and ambitions. During these years, many people have helped me along the way and I would like to express my deepest gratitude to them:

First, I would like to thank my advisor Prof. Tomás Palacios. I am very lucky to be his student and have the opportunity to work with him. His insights, encouragement, patience, optimism and trust always motivate me to work on new ideas and approaches, and to tackle the most important and fundamental problems. He creates many opportunities for me to attend conferences, gain industrial experiences and establish collaborations with other groups. Outside technical world, I also learnt a lot from him in many other aspects. I learnt a lot from him on how to be an impactful researcher in academia and how to combine research and entrepreneurship. All these learnings from him are invaluable in my life.

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Finally, I am very grateful to my parents for their endless love and support. My lovely girlfriend Binggege Guo has always been supportive and understanding. I owe so much to you all. This thesis is dedicated to you.

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Chapter 1 Introduction

1.1 GaN Power Devices

Power electronics is the application of solid-state electronics to the control and conversion of electric power. Power electronics has very diverse applications, from the basic infrastructure in a country, such as power plants and solar farms, to people's daily life, such as electrical vehicles and consumer electronics. Its market size is increasingly large, reaching about $40 billion in 2010. Power electronic devices, such as power transistors or diodes, determine the ultimate performance of power electronics systems and therefore are core component and differentiators of power electronic systems. Ideal switching devices should be able to pass any amount of current with no voltage drop when they are in the ON state and withstand an applied voltage with no current passing when they are in the OFF state. In real power electronic devices, low on-resistance (R_{on}) and high breakdown voltage (BV) are desired to provide high-power and low-loss operation for switching applications.

Medium and high-voltage power electronics is used in a wide variety of energy applications, such as data center, electrical grid, electric vehicles, etc. Central to improving the efficiency of power switching in these applications is the availability of low-cost, efficient, small and reliable power devices that work at high-frequencies, high-voltage and high-power levels. For example, in the application of hybrid automobiles, power devices with 600-1200 V blocking voltages are critical to convert the DC power from batteries to the AC power needed to operate the electric motor [1].

Nowadays, power devices are mainly made of silicon (Si). However, the limited critical electric field of Si and its relatively poor transport properties make many of the

commercial devices and circuits currently available bulky, heavy and inappropriate for future power applications. On the other hand, III-N semiconductors, especially gallium nitride (GaN), are quickly becoming the materials of choice for high-power RF electronics, as well as for low power (<10 kW) power electronics due to a variety of intrinsic materials properties such as high electron saturation velocity ($\times 3$ higher than Si), high breakdown field ($\times 10$ higher than Si) and very high charge density ($\times 3$ higher than Si) available through polarization engineering. All these properties allow GaN-based power switches to show much lower R_{on} than Si and SiC devices for the same BV. Table 1-1 summarizes the physical properties of GaN compared to other semiconductors used for power devices, where the Baliga's figure of merit (BFOM) is a widely adopted metric regarding the suitability of a given semiconductor to power electronics [2]. As can be seen in Table 1-1, GaN is superior to other semiconductors, especially Si, for power devices operating under high-power, high-temperature and high-frequency conditions.

Table 1-1 Physics Properties of GaN compared with Si, GaAs, SiC

Materials	E_g (eV)	ε	μ_n (cm^2/Vs)	E_c (MV/cm)	V_{sat} (10^{7}cm/s)	BFOM
Si	1.12	11.8	1350	0.3	1.0	1
GaAs	1.42	13.1	8500	0.4	2.0	17
4H-SiC	3.26	10	720	2.0	2.0	134
6H-SiC	2.86	9.7	370	2.4	2.0	115
GaN	3.44	9.5	900	3.3	2.5	537

E_g, bandgap; ε, dielectric constant; μ_n, electron mobility; E_c, critical electrical field; V_{sat}, saturation velocity; BFOM, normalized by that of Silicon.

1.2 Lateral and Vertical GaN Power Devices

Currently, two types of structures are being considered for GaN-based power transistors: lateral and vertical. The most distinctive GaN lateral device is the AlGaN/GaN high-electron-mobility transistor (HEMT), which utilizes a two-dimensional electron gas (2DEG) generated at the interface of an AlGaN/GaN heterostructure. Due to piezo- and spontaneous polarization, the 2DEG has high electron mobility and high carrier density, which enable the device to achieve a superior combination of high BV and low R_{on} in comparison with Si and SiC devices. Though GaN-based HEMTs have been studied extensively, it is still very difficult to simultaneously achieve high current (>50 A), high breakdown voltage (>1 kV) with lateral structures because the gate-to-drain distance must be extended proportionally to increasing the BV, and all the current flows through a very confined layer of semiconductor, which increases self-heating in the device and reduces device reliability. Although low-cost substrates, such as Si and sapphire, have been used to grow GaN power devices, the epitaxial material cost of GaN is still high, especially for high-voltage devices. For GaN lateral HEMTs with >1200 V BV, a source-to-drain length above 16 μm is typically needed, which significantly increases the area of these devices. Therefore high-voltage HEMTs require a large area to lower the device on-resistance as well as thick buffer layers to sustain the BV. These issues presently limit the wide deployment of GaN lateral HEMTs in high-voltage and high-power applications.

A GaN-based vertical structure is also effective for realizing low R_{on} and high BV, in comparison with conventional Si- and SiC-based power devices as well as GaN lateral devices. GaN vertical devices have attracted increased attention recently, due to several

potential advantages over GaN lateral devices: (a) higher *BV* capacity without enlarging chip size; (b) superior reliability due to a less-crowded field distribution and moving away of the peak electrical field from the surface into the bulk semiconductor devices [3]; (c) higher current capability due to a much more spread current distribution; (d) superior thermal performance [4]. In fact, vertical structures have been regarded as necessary to achieve the device current (> 100 A) and voltage levels (> 600 V) required for many applications, such as electric vehicles and renewable energy processing [5].

In his MSc Thesis, the author performed electrothermal simulation and thermal performance study of GaN vertical and lateral power transistors [4][6]. In that work, self-consistent electrothermal simulation models have been established for single-finger and multi-finger GaN vertical and lateral power transistors, and were calibrated by experimental data. Then the simulation models were utilized to derive the maximum achievable power density of the transistors without the peak temperature exceeding a safe operation limit of 150 $^{\mathrm{o}}$C ($P_{150\,\mathrm{C}}$). This maximum power density, $P_{150\,\mathrm{C}}$, was utilized as a figure of merit to compare the thermal and power performance of the vertical and lateral GaN transistors with various voltage classes and scaling levels. It was found that vertical GaN devices could achieve a higher $P_{150\,\mathrm{C}}$ than lateral GaN HEMTs, especially for the devices with higher *BV* classes and higher scaling level designs. These work suggested an advantage of vertical GaN power devices *v.s.* lateral in heat dissipation and power handling.

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1.3 Status and Challenges of Vertical GaN Power Devices

Figure 1-1 summarizes the device types, key research groups and voltage classes of the main vertical power devices reported in recent years. The first demonstrations of vertical GaN diodes dates back to over 15 years ago [7]. Recent demonstrations of high-performance vertical GaN diodes and transistor have renewed the interest in these devices. Since 2010, extensive work has been done to demonstrate high-performance vertical GaN devices on free-standing GaN substrates. In 2014, we first demonstrated the vertical GaN devices on low-cost Si substrates, with more followed works on vertical GaN-on-Si diodes in the past years.
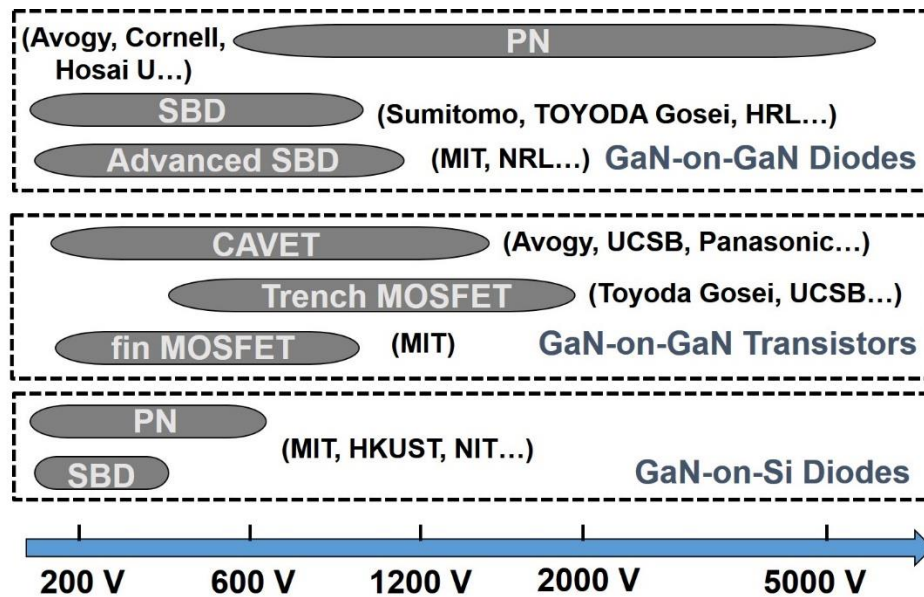
Figure 1-1 Overview of the device types, reporters and voltage classes of main vertical GaN power devices reported in recent years.

For GaN vertical pn diodes, Avogy Inc. has demonstrated a specific R_{on} of 2 mΩ cm^2 for a BV of 2.6 kV and 2.9 mΩ cm^2 for a BV of 3.7 kV [8]. Researchers at

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Cornell University have shown GaN vertical pn diodes with specific R_{on} of 0.95 mΩ cm^2 for a *BV* of 3.48 kV [9]. For vertical GaN Schottky barrier diodes (SBDs), HRL has demonstrated GaN vertical Schottky diodes with a *BV* over 800 V [10]. Mitsubishi has obtained a record performance with R_{on} of 0.71 mΩ cm^2 and a *BV* over 1100 V [11]. To combine the good forward characteristics of Schottky barrier diodes (e.g. low turn-on voltage) and reverse characteristics of pn diodes (e.g. low leakage current and high *BV*), we first demonstrated vertical GaN SBDs with advanced structures. This related work will be described in Chapter 4.
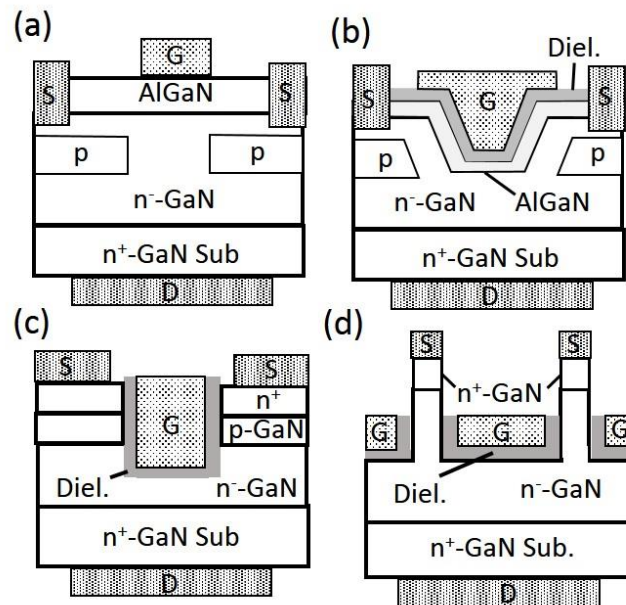
Figure 1-2 Schematic of vertical GaN transistors: (a) CAVET; (b) Trench CAVET; (c) Trench MOSFET; (d) fin MOSFET.

For GaN vertical transistors, four main device structures have been developed by various groups, as shown in Figure 1-2. UCSB has developed a current aperture vertical electron transistor (CAVET) which combines the high conductivity of 2DEG channel at

the AlGaN/GaN heterojunction with the better field distribution in a vertical structure [3] (Figure 1-2 (a)). Avogy Inc. demonstrated a CAVET with a R_{on} of 2.2 mΩ cm^2 for a BV of 1.5 kV [12]. Panasonic introduced the trench structures into the CAVET to allow for a normally-off semi-polar gate structure (Figure 1-2 (b)), and demonstrated a R_{on} of 1 mΩ cm^2, a BV of 1.7 kV and a threshold voltage of 2.5 V [13]. Vertical GaN MOSFETs have also been demonstrated with similar structures to conventional Si and SiC vertical MOSFETs, as shown in Figure 1-2 (c). Compared to CAVET, vertical MOSFETs do not need the regrowth of AlGaN/GaN channels and are intrinsically normally-off. TOYODA GOSEI demonstrated a trench MOSFET with a R_{on} of 1.8 mΩ cm^2 for a BV of 1.2 kV [14]. Finally, our group recently demonstrated a vertical GaN fin MOSFET [15], as shown in Figure 1-2 (d). The fin MOSFETs have sub-micron GaN fins with all-around gates, and achieved a R_{on} of 0.36 mΩ cm^2, a BV of 800 V and normally-off operation without the need for p-type GaN materials or epitaxial regrowth.
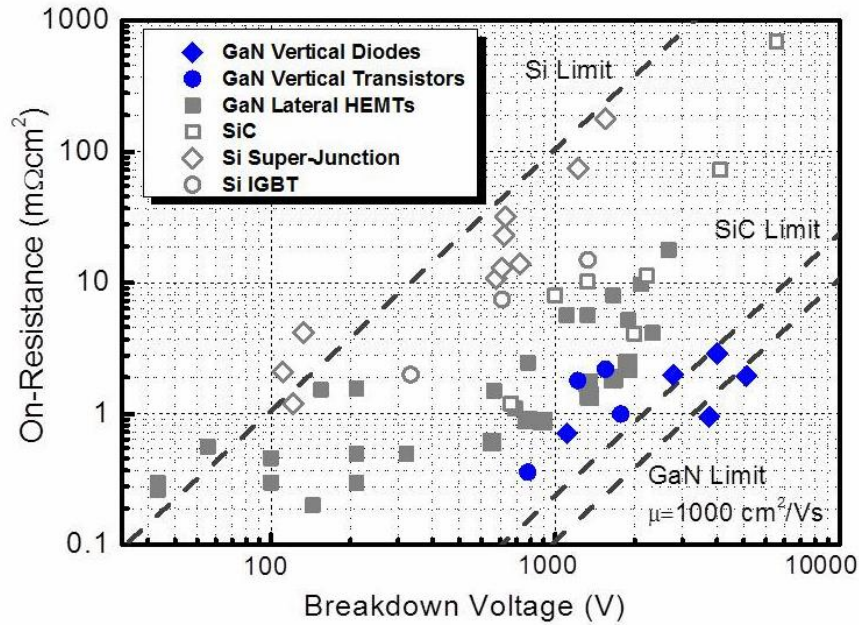
Figure 1-3 On-resistance v.s. breakdown voltage trade-off for the recently demonstrated vertical GaN

devices, in comparison with lateral GaN devices, SiC and Si power devices.

Fig. 1-3 summarizes the *BV v.s. R*$_{on}$ trade-off for the recently demonstrated GaN

vertical diodes and transistors, in comparison with that of GaN lateral HEMTs, SiC

power devices, Si super-junction devices and Si IGBT. As shown, the state-of-the-art

performance of vertical GaN devices has surpassed that of lateral GaN devices, and is

close to or even beyond the GaN theoretical limit (for a channel mobility of 1000

cm^2/Vs).

Despite the promising performance of vertical GaN power devices, several

challenges have hindered the fast commercialization of vertical GaN power devices:

(a) High cost and small diameter of GaN substrates. Currently, almost all vertical

GaN power devices have been demonstrated on free-standing GaN substrates.

As shown in Table 1-2, the cost per area of GaN substrates is over 1000 times

higher than Si substrates. In addition, the small diameter of GaN substrates will

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also greatly increase the cost per area of epitaxial material growth and device fabrications. Thus, low-cost solutions have been greatly desired for the development of vertical GaN power devices.

Table 1-2 Available Substrate and Cost for Different Power Devices

Device Structure	GaN-on-GaN vertical devices	GaN lateral HEMTs	SiC Power Devices	Si Power Devices
Available Substrate	50 mm GaN	200 mm Si / 75 mm SiC	75 mm SiC	200 mm Si
Substrate cost per cm^2	$50~ $100	~ $0.08 / ~ $6	~$6	~$0.08

(b) Lack of a viable selective area doping or selective area epitaxial regrowth process that yields high-quality p-n junction on patterned GaN surfaces. The full potential of vertical power devices requires the development of selective area p-type doping. For example, merged pn/Schottky diodes could allow for a low turn-on voltage and high BV. Junction termination extension structures (p-type GaN rings surrounding the device perimeter) are essential to demonstrated high-voltage vertical devices. However, most of the current approaches, laterally patterned ion implantation and activation or selective area diffusion of p-type dopants (e.g. Mg, Be, Zn) has not produced p-type regions or good-quality (i.e. equivalent to as-grown) p-n junctions.

(c) Complete understanding of BV and leakage current mechanisms. Despite the high BV demonstrated in vertical GaN pn diodes, the microscopic mechanistic understanding for the leakage current and its correlation of dislocation/defect densities is incomplete or non-existent.

1.4 Thesis Outline

This thesis aims to understand and overcome the challenges outlined above, by developing novel device structures and making systematic physical analyses. In particular, extensive studies will be presented to optimize the three main components of a vertical GaN device: channel region, drift region, transitional regions & substrates (Figure 1-4). The remainder of this thesis is organized as follows:

Chapter 2 describes the device design, fabrication, optimization and measurement results of vertical GaN diodes on low-cost Si substrates. Device physics for R_{on} and BV will be also quantitatively analyzed with simulation. The high performance of our optimized devices shows the great potential of low-cost vertical GaN-on-Si devices for 600-V level high-current and high-power applications [16]–[18].

Top Electrodes

Channel Region

Drift Region

Transition Layers and Substrate

Bottom Electrodes
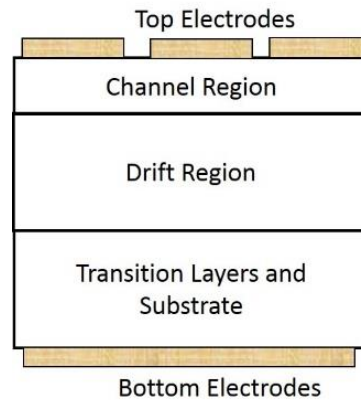
Figure 1-4 Schematics of the main components in a vertical GaN device.

Chapter 3 elucidates the design space and origin of off-state leakage in GaN vertical power diodes on GaN, sapphire and Si substrates. The behavior of leakage current for vertical GaN devices as a function of dislocation density and electric field was derived by TCAD simulations, after careful calibration with experiments and literature data. The

design space of leakage current in vertical GaN devices was derived and benchmarked with that in lateral GaN, Si and SiC devices [19].

Chapter 4 demonstrates the device design, simulation, fabrication and characterization of a novel vertical GaN advanced SBDs: Trench MIS barrier Schottky rectifiers with field rings. Compared to Chapter 2 and 3, where extensive studies have been made for drift regions and substrates, Chapter 4 will focus on the novel structures in top channel regions. The demonstrated devices can achieve a combination of Schottky-like forward characteristics and pn-like reverse characteristics [20].

Chapter 5 presents the concepts and designs for the formation of patterned pn junction structures. The formation of pn junctions in patterned GaN structures is a fundamental and key challenge to enable >1200 V power devices. This chapter will first introduce two basic methods for the formation of these pn junctions, including their concepts and challenges. This vertical pn pillar structure could allow for the realization of two power devices: (a) Junction-barrier Schottky rectifiers, which is an advanced Schottky rectifiers widely used by the SiC industry; (b) GaN super-junction devices, which could break the theoretical limit of R_{on} v.s. BV trade-offs for conventional vertical GaN power devices. Preliminary experimental results of the fabrication and characterization of the vertical pn pillar structures and the two enabled devices will also be presented.

Chapter 6 concludes and summarizes this thesis and presents some future work.

Chapter 2   Vertical GaN Diodes on Si Substrates

This chapter presents the demonstration and optimization of vertical GaN diodes on Si substrates. The motivation and challenges of developing vertical GaN-on-Si devices are elucidated in section 2.1. The first demonstration of vertical GaN-on-Si pn and Schottky diodes is presented in section 2.2. Based on the first-generation devices, physical analyses and engineering optimization for the device reverse characteristics and forward characteristics are discussed in sections 2.3 and 2.4, respectively. The first-generation GaN-on-Si diodes employ a quasi-vertical structure, i.e. anode and cathode locate on the same side of the wafer. Fully-vertical GaN-on-Si diodes, i.e. anode and cathode locate on the different sides of the wafer, are also demonstrated, as shown in sections 2.5. Section 2.6 presents the DC and switching characteristics of the second-generation quasi-vertical and fully-vertical GaN-on-Si diodes. Finally, section 2.7 benchmarks the vertical GaN-on-Si diodes fabricated in this thesis with other competing devices, and provides prospects for future work.

2.1 Introduction

As discussed in Chapter 1, despite of the excellent performance demonstrated by GaN vertical devices, the high cost ($>1000\times$ higher than Si substrates) and small diameter of GaN substrates have become one of the main challenges for the commercialization of GaN vertical power devices. Thus, lower cost substrates, in particular Si substrates, for GaN vertical devices would be greatly preferred to make their market insertion easier.

However, the demonstration of GaN vertical power devices on low-cost Si substrates is extremely challenging mainly due to two reasons: (a) the high dislocation

density in GaN-on-Si structures, and (b) the relatively thin GaN drift regions that can be grown on Si substrates and transition layers. Typical dislocation density in GaN-on-Si structures is above 10^9 cm^{-2}, which is at least three orders of magnitude higher than that in GaN-on-GaN structures (10^3-10^6 cm^{-2}). The high dislocation density typically induces a larger off-state leakage, lower *BV* and inferior reliability. In addition, due to lattice mismatching and subsequent bowing effect, the total GaN epitaxial layer that can be grown on Si substrates and transition layers is typically below 3~4 μm. This thickness is much smaller than the epitaxial GaN layer thickness on GaN substrates (easily above 20~30 μm). The thin GaN drift regions on Si substrates brings great challenges to achieve high *BV* in GaN-on-Si vertical power devices.

To explore the feasibility of using vertical GaN structures on Si substrates, vertical GaN-on-Si diodes need to be studied first. In addition, most of advanced vertical Schottky barrier diodes and vertical transistors contain pn junctions, which determines the device blocking characteristics. To understand the limits of advanced vertical GaN-on-Si power devices, e.g. MOSFETs and junction barrier Schottky rectifiers, GaN-on-Si vertical pn diodes on Si need to be demonstrated and studied.

2.2 First-generation Vertical GaN-on-Si Diodes

The schematics of the first-generation GaN-on-Si vertical SBD and p-n diode are shown in Figure 2-1 (a) and (b). Figure 2-1 (c) shows the net donor/acceptor concentrations profile of the GaN-on-Si pn wafers measured by electrochemical *C-V* measurements. The drift regions consist of 1.5 μm n$^-$-GaN (N_D~6×10^{16} cm^{-3}) drift region for SBD, or 0.5 μm p-GaN (Mg: 1×10^{19} cm^{-3}, N_A~1.5×10^{17} cm^{-3}) and 1.0 μm n$^-$-GaN (Si:

$N_D \sim 6 \times 10^{16}$ cm^{-3}) for p-n diodes. The drift regions were grown on 0.3 μm n$^+$-GaN (Si:

2×10^{18} cm^{-3}) current spreading layer, 0.2 μm semi-insulating GaN, 2.4 μm GaN/AlN

transition layers, on a 3-inch (111) Si substrate. The wafers were grown by metalorganic

chemical vapor deposition (MOCVD) and the estimated dislocation density in the GaN

epilayers is $\sim 10^9$ cm^{-3}. The wafers were purchased from DOWA Inc.
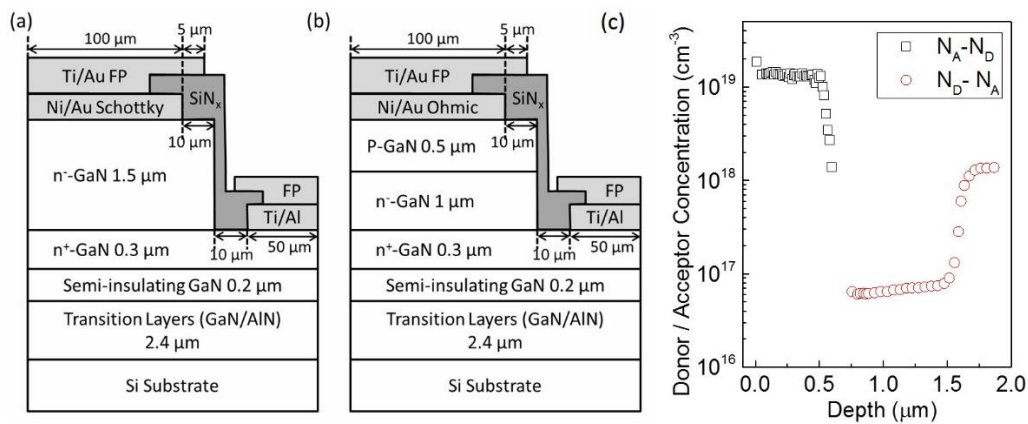
Figure 2-1 Schematic cross sections of vertical GaN-on-Si (a) Schottky and (b) pn diodes. (c) Net

donor/acceptor profile in the wafer measured by electrochemical C-V measurements.

The device fabrication starts with the mesa isolation and GaN deep etching (~1.6 μm)

to access the cathode region. A Ti/Al Ohmic contact ring with a width of 50 μm was

formed on n$^+$-GaN cathode region. Ni (30 nm) / Au (200nm) was then deposited on n$^-$-

GaN as the circular Schottky barrier electrode for SBD, and Ni (15 nm) / Au (50 nm)

was deposited on p-GaN followed by thermal annealing in a mixture of N$_2$ and O$_2$ at 550

^{o}C for 10 min to form the circular Ohmic contact for p-n diodes. The diameter of the

anode electrode is 200 μm. A SiN$_x$ passivation layer (~ 200 nm) and Ti (20 nm) / Au

(300 nm) bilayer formed the field plate (FP) structure.

The inset of Figure 2-2 (a) shows forward *I-V* characteristics of GaN vertical SBDs and p-n diodes. The ideality factor, specific R_{on} and V_{on} (extracted at $I = 1$ A/cm^2) of the SBD and p-n diodes is 1.5, 6 mΩ·cm^2, 0.5 V and 2.0, 10 mΩ·cm^2, 3.5 V, respectively. The V_{on} in p-n diode, 3.5 V, is expected due to the large bandgap of GaN. However, if the V_{on} is extracted by extrapolation of the *I-V* curve in the linear plots, it is 4~5 V, due to the slower diode turn-on. This slow turn-on and higher ideality factor is attributable to the high Ohmic resistance on p-GaN at low current levels, which will be elaborated in Chapter 2.4.
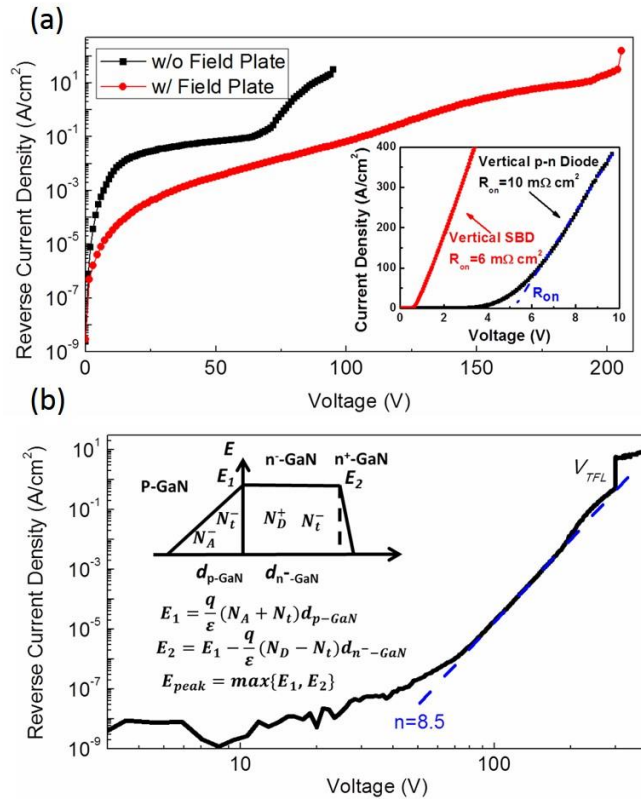
Figure 2-2 (a) Reverse *I-V* characteristics of vertical GaN-on-Si SBDs with and without FP structures. (Inset) Forward *I-V* characteristics of vertical GaN-on-Si Schottky and pn diodes. (b) Reverse *I-V* characteristics and (inset) schematic electric field distribution of vertical GaN-on-Si pn diodes.

Figure 2-2 (a) shows reverse *I-V* characteristics of the GaN vertical SBD. The destructive *BV* of the SBD without and with a FP structure is 90 V and 205 V, respectively, both occurring at the Schottky-electrode edges. This demonstrates that the FP structure is effective in spreading the electric field at electrode edges, reducing the reverse leakage current and improving the reverse *BV*.

Figure 2-2 (b) shows reverse *I-V* characteristics of the GaN vertical p-n diode with an FP structure, demonstrating a soft *BV* higher than 300 V. The leakage current density of the vertical p-n diode at -200 V is ~10^{-2} A/cm^2, which is lower than that of the vertical SBD by three orders of magnitude. The logarithmic *I-V* curve shows that the current *I* is proportional to V^n ($n \approx 8.5$ in our diodes) until a hump (sharp transition in *I-V* curve) at $V_{\text{TFL}} = 300$ V. Such behavior can be modeled by a space-charge-limited current (SCLC) conduction mechanism with traps [21]. Under reverse bias and below V_{TFL}, electrons injected into the p-n junction partly contribute to conduction current and are partly captured by acceptor traps. The hump V_{TFL} represents the traps-filled-limited voltage of the acceptor traps, suggesting the applied voltage overcomes the negative potential formed by the unneutralized electrons in traps and the ionized acceptors (N_{A}) and donors (N_{D}) in p-GaN and n-GaN. Given this mechanism, we could define the soft *BV* for the GaN-on-Si vertical p-n diode by the onset of V_{TFL}. If we define N_{t} as the average density of acceptor traps distributed in p-GaN and n$^-$-GaN, based on the electric field distribution shown in the inset of Figure 2-2 (b), the V_{TFL} is given by

$$V_{TFL} = \frac{q}{2\varepsilon}(N_A + N_t)d_{p-GaN}^2 +$$

$$\frac{q}{2\varepsilon}[2(N_A + N_t)d_{p-GaN} - (N_D - N_t)d_{n^--GaN}]d_{n^--GaN} \tag{2-1}$$

where ε is the permittivity of GaN, d_{p-GaN} and d_{n^--GaN} are the thickness of p-GaN and n⁻-GaN. Given $V_{TFL} = 300$ V and $N_A \sim 1.5 \times 10^{17}$ cm⁻³, we can estimate the N_t to be 6.69×10^{16} cm⁻³ and the peak electric field in GaN to be 2.25 MV/cm. Also, according to [22], the ionized acceptor density N_A could possibly be increased under the high electric field in the p-n junction. Considering this effect, the peak electric field was estimated to be slightly higher, as the reverse voltage would be mainly sustained by the 1-μm n⁻-GaN layer in that case. To our knowledge, the ~2.3 MV/cm peak electric field in our vertical p-n junction is among the highest in all reported GaN-on-Si device, though still lower than the 3.0~3.2 MV/cm reported in GaN-on-GaN [8] and the theoretically predicted critical field 3.4~3.6 MV/cm for GaN.

2.3 Leakage Current and Breakdown Voltage Optimization

2.3.1 Leakage Current Analyses
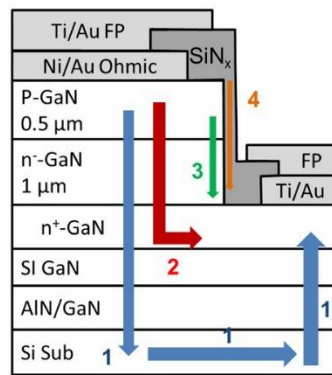
Figure 2-3 Schematics of four possible leakage paths in vertical GaN-on-Si diodes.

Vertical p-n diodes are utilized for the leakage analysis of GaN-on-Si vertical devices, as shown in Figure 2-3. Four possible leakage paths exist in the GaN-on-Si vertical structures: (1) through the transition layers and Si substrate; (2) through the drift layer; (3) along the etch sidewall; (4) through the passivation layer.
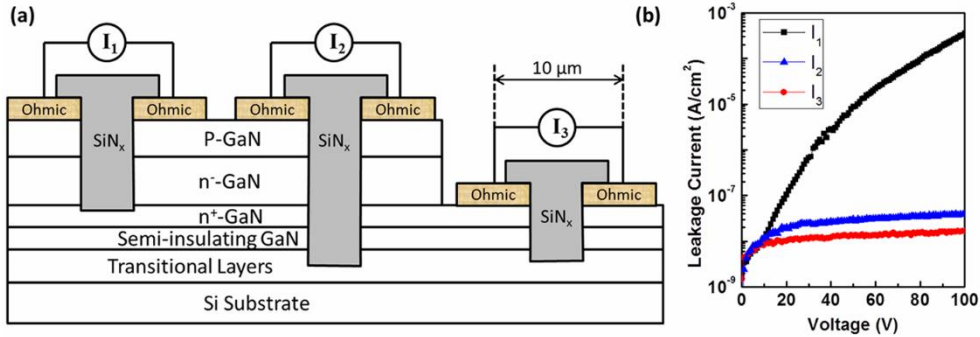
Figure 2-4 (a) Trench structures with different etching depths and the schematic structures for I_1, I_2 and I_3 measurements. The I_1 measures the leakage current of trench structure down to n^+-GaN. The I_2 and I_3 measures the leakage current of trench structures down to the transition layers. (b) The I_1, I_2 and I_3 as a function of reverse biases.

The contribution of leakage path #1 (through transition layers and Si substrate) could be determined by measuring the leakage of trench structures with different etching depths, as shown in Figure 2-4. The I_1 measures the leakage current in a trench structure etched down to the n^+-GaN layer, containing all leakage paths #1-4 shown in Figure 2-3. The I_2 and I_3 measures the leakage current in a trench structure etched down to the transition layers. In I_2 and I_3, the current path #2 and #3 were greatly reduced or eliminated, as they go through the insulated GaN and transition layers. As shown in Figure 2-4 (b), when the trench is etched down to transition layers, I_2 and I_3 are more than 3 orders of magnitude lower compared to I_1, indicating: (a) leakage path #2 and #3 are

the main contribution to the total lekage current; (b) leakage path #1 and #4 are negligible to the diode's total leakage. The small leakage path #1 demonstrates a good vertical insulating property of GaN-on-Si wafers.
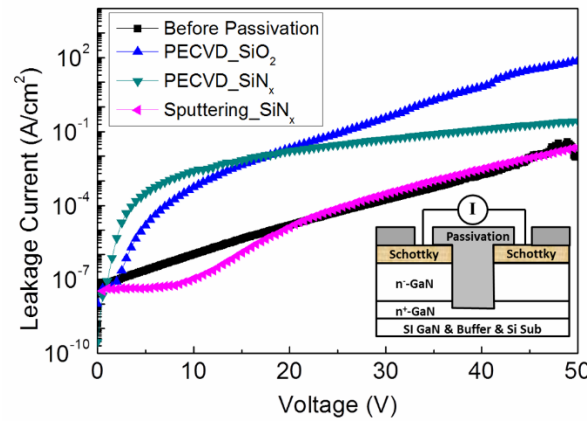
Figure 2-5 Leakage current in trench structure before and after passivation by PECVD SiO_2, PECVD SiN_x and sputtering SiN_x.

The leakage path #4 (through passivation layer) has been further eliminated by a new GaN passivation technology based on a sputtering deposition system [16]. This technology is able to effectively reduce the leakage increase widely reported for traditional passivation using plasma-enhanced chemical vapor deposition (PECVD) systems, as shown in Figure 2-5.

In summary, the leakage paths #1 and #4 have been identified as minor contributors to the total device leakage current in this section. In the next sections, etching sidewall treatment and edge termination technologies are developed to reduce the leakage path #3.

2.3.2 Advanced Edge Termination Technologies

The leakage path #3 (along etch sidewall) is typically due to etch-induced damage or defects (e.g. nitrogen vacancies) created by high-energy dry etching for GaN. It was reported that the surface of p-GaN sidewall could be changed to a depleted or an n^--GaN layer by inductively coupled plasma (ICP) reactive-ion etching (RIE), which would induce a large leakage under high reverse bias [23].
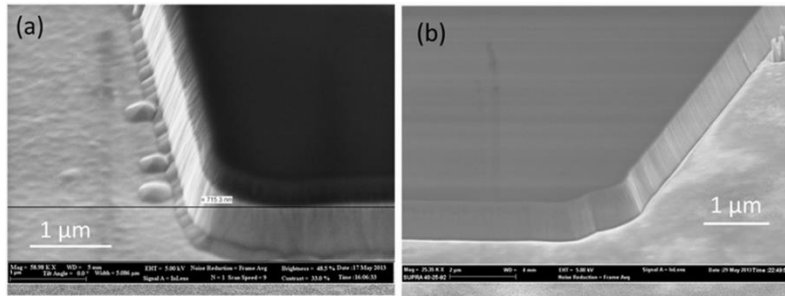
Figure 2-6 Scanning electron microscope (SEM) images of GaN etching sidewalls by using (a) SiO_2 and (b) Ni hard mask.

Two technologies have been developed to reduce leakage path #3: (a) GaN deep etching technology and (b) advanced edge termination technology. The GaN deep etching technology was developed in an ICP-RIE system by using a Cl_2/BCl_3 gas combination and metal hard mask. The optimized etching condition was achieved at an ICP power of 150 W, a bias power of 75 W, a chamber temperature of 40 ^{o}C, pressure of 0.6 Pa and a flow rate of 20/5 sccm for the Cl_2/BCl_3 gas combination. This etching condition would typically give an etching rate of 200~250 nm/min for GaN layers. The selection of etching masks is critical to achieving high quality etching sidewalls and low parasitic leakage currents. As shown in Figure 2-6, compared to traditional oxide hard mask, the

use of metal hard mask could enable a much smoother etch sidewall, due to the lack of oxide edge erosion under high plasma energies. Also, as shown in Figure 2-7, an Ar pre-treatment before the Cl_2/BCl_3 was found to increase the leakage current, probably due to the physical damage by Ar plasmas. The Cl_2/BCl_3 etching with Ni hard mask and without Ar pre-treatment allows for the smallest leakage current.
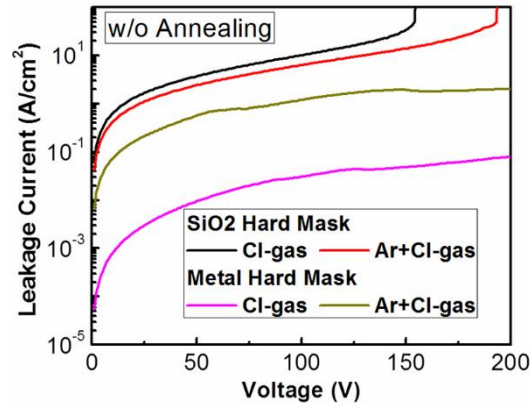
Figure 2-7 Sidewall leakage current for the ICP-RIE etching with SiO_2/Ni hard mask and with/without Ar pre-treatment.

The advanced edge termination technology for GaN-on-Si vertical device has been developed by combining plasma treatment, tetra-methylammonium hydroxide (TMAH) wet etching and ion implantation. As shown in Figure 2-8, various plasma treatments were studied to heal the damage of ICP-RIE. CF_4 and N_2 plasma treatment could effectively passivate the nitrogen vacancies and reduce the sidewall leakage. It is also worth noting that the CF_4 plasma was also applied in GaN-based lateral devices to passivate interface defects [24]. In contrast, H_2 plasma, reported as able to create nitrogen vacancies [25], induces a large sidewall leakage increase, indicating a strong correlation between sidewall leakage and nitrogen vacancies in GaN-on-Si vertical devices.

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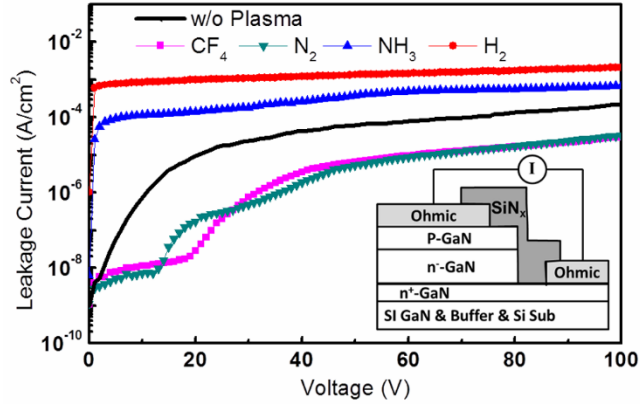
Figure 2-8 Leakage current of the structure with different sidewall plasma treatments (CF_4, N_2, NH_3 and H_2) after ICP-RIE. (inset) Structure for leakage current measurements.

TMAH is widely used as a basic solvent in the development of acidic photoresist in the photolithography process and also used as an anisotropic etchant of Si. It has been reported that TMAH etches any planes of GaN except for the (0001) plane [26]. Due to its anisotropic etching properties, TMAH preferentially etches the side slopes and therefore could eliminate the surface damage caused by the dry etching without increasing the etching depth. As shown in Figure 2-9 (a), we have found that TMAH wet etching (25% concentration) at 85 $^\circ$C could effectively remove the low-quality surface layers at etch sidewall, especially near the p/n-GaN interface. As shown in Figure 2-9 (b), a TMAH treatment for 60 minutes could also induce more than $50\times$ reduction of sidewall leakage. In addition, forward characteristics of GaN-on-Si vertical diodes were also enhanced by TMAH treatment, as shown in Figure 2-10, due to a reduction of sidewall defects and a reduction of current crowding with a more vertical sidewall.
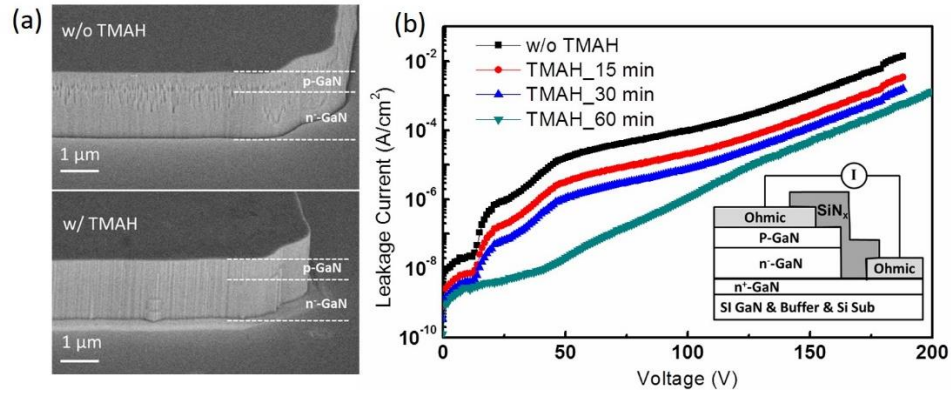
Figure 2-9 (a) Cross-sectional SEM images of the etched GaN sidewalls before and after TMAH treatment for 60 minutes. (b) Leakage current for the quasi-vertical structures after TMAH treatment with different time. (Inset) Device structure for leakage current measurements.
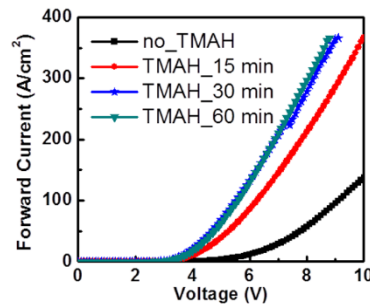
Figure 2-10 Diode forward characteristics by TMAH wet etching for different time.

An ion implantation ring was introduced to isolate the main current from the etch sidewall, as shown in Figure 2-11. Ar was used for implantation [27]. As shown in Figure 2-12, the ion implantation reduces the leakage at high reverse bias, due to a significant mitigation of leakage along the etch sidewall. However, the implantation slightly increases the device leakage at low bias due to parasitic leakage through implanted region. Different Ar dose and energy were also studied for implantation (Figure 2-12). Ion dose mainly determines the insulating properties of implant region and the device leakage current at low reverse bias. Ion energy determines the depth of implant region, with 150

keV for a depth of ~ 0.3 μm and 300 keV for ~ 0.6 μm. High ion energy is needed to extend the implantation region beyond the p/n-GaN junction, in order to prevent the leakage from flowing towards the depleted p-GaN sidewall at high bias.
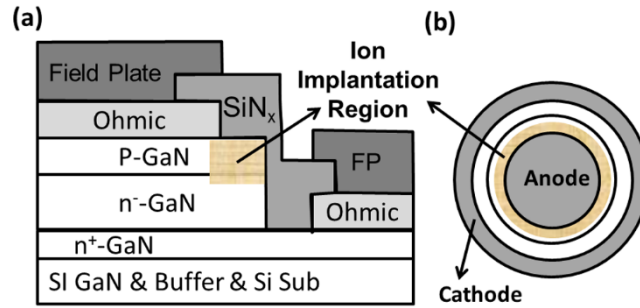
Figure 2-11 (a) Cross sectional and (b) top-view schematics of GaN-on-Si vertical pn diodes with ion implantation edge terminations.
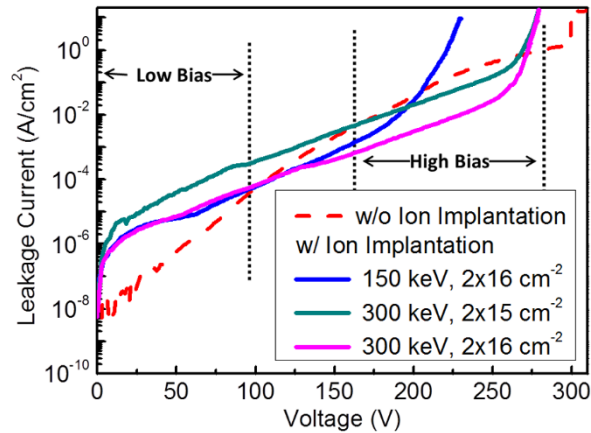
Figure 2-12 Reverse characteristics of vertical GaN-on-Si pn diodes without and with ion implantion edge terminations, as a function of ion doses and energies.

After the development of three main edge termination technologies, a new bunch of vertical GaN-on-Si pn diodes were fabricated. Figure 2-13 presents the reverse characteristics of vertical GaN-on-Si diodes with and without the advanced edge

termination. As can be seen, the leakage current reduced by almost two orders of magnitude at high reverse biases.
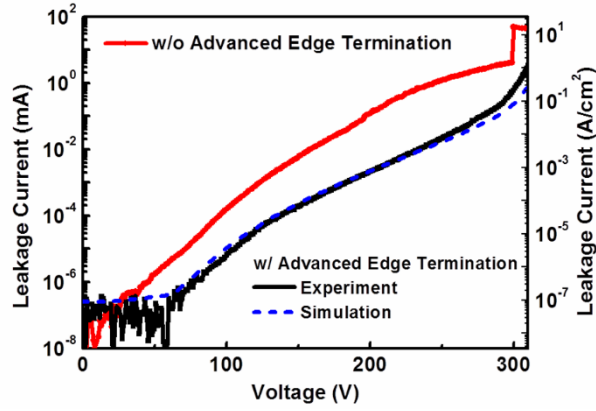
Figure 2-13 Experimental and simulated leakage current of GaN-on-Si vertical p-n diodes with advanced edge termination, and experimental leakage of vertical diodes without edge termination.

To further understand the leakage current in the devices with edge termination, the dependence of leakage current density on diode periphery was investigated. The total leakage density of vertical diodes with a radius (R) of 50, 100, 150 and 300 μm were measured and plotted in Figure 2-14. The total reverse leakage current density J_{total} can be expressed as following:

$$J_{total} = J_2 + J_3 \times P/A = J_2 + 2J_3 \times d \times 1/R \qquad (2\text{-}2)$$

where J_2 and J_3 are the bulk leakage current density (leakage path #2) and perimeter leakage current density (leakage path #3). P and A are the perimeter and area of vertical diodes, with d and R as the etching depth and anode radius. As shown in Figure 2-13, the total leakage current exhibits almost no linear dependence on $1/R$, indicating that the sidewall leakage has been effectively suppressed by edge terminations and the bulk component (leakage path #2) is the main contributor to the total device leakage current.

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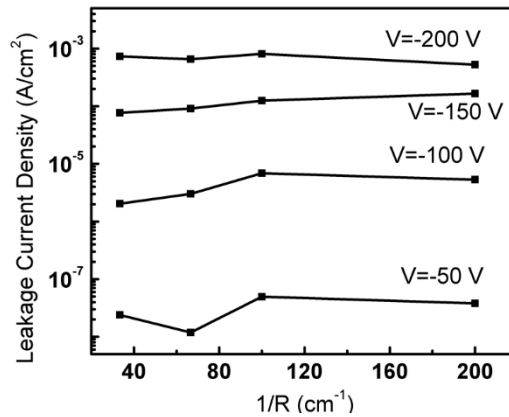
Figure 2-14 Total leakage current density of vertical p-n diodes with different anode radius R (R=50, 100, 150 and 300 μm), as a function of 1/R at a reverse voltage of 50, 100, 150 and 200 V.

The leakage mechanism of the bulk component (leakage path #2) was further studied using analytical modeling and TCAD simulation. The simulated reverse characteristics presented in Figure 2-13 was based on a variable-range hopping model, and exhibits a good agreement with the experimental data. The analyses and simulation details will be presented in Chapter 3.

2.3.3 Epitaxial Layers Optimization

With the optimized edge termination and filed management structures, the key limiting factor for the *BV* of vertical GaN-on-Si diodes is the epitaxial structures, in particular, the drift region, as the drift region is the main part for sustaining reverse biases. With proper electrical field management, the ionized donor level (N_D) and the thickness of drift regions typically determined the device *BV*.

For GaN-on-Si vertical devices, total thickness of GaN epitaxial layers is limited due to the lattice mismatch of Si and GaN. In order to achieve high *BV*, the thickness

distribution into different GaN layers (e.g. p-GaN, n⁻-GaN, n⁺-GaN, etc.) needs to be carefully optimized.

To understand the impact of epi-structures on device performance, we collaborated with Prof. Armin Dadgar's group at Otto-von-Guericke-University Magdeburg (OVGU), Germany. The GaN-on-Si wafers grown by Prof. Dadgar's group have similar layer structure with the first batch of wafers purchased from DOWA, but with various doping levels and thicknesses for each GaN layers. The GaN layers were all grown by MOCVD on 2-inch (111) Si substrates by using AlGaN-based transition layers. We fabricated and characterized vertical GaN-on-Si diodes on these wafers. In order to distinguish this batch of devices from the first batch of devices based on the DOWA wafers, we named this batch of devices as "second-generation" vertical GaN-on-Si diodes. A representative device structure and a cross-sectional SEM image of GaN-on-Si wafers are shown in Figure 2-15.
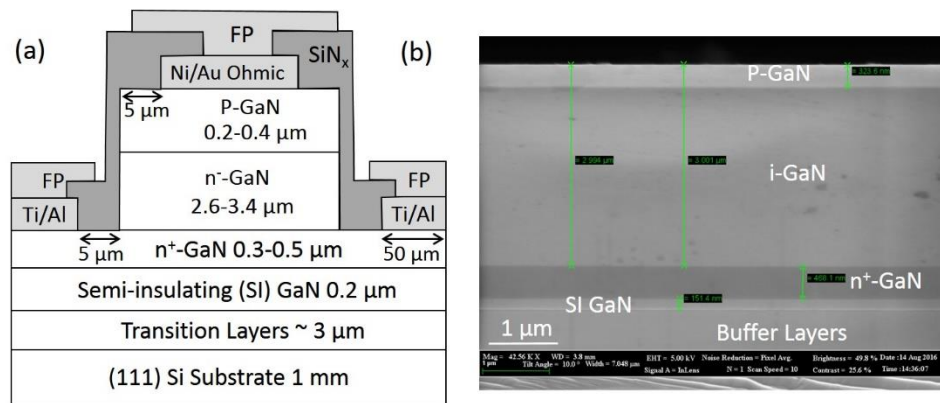
Figure 2-15 (a) Schematics of the second-generation vertical GaN-on-Si pn diodes. (b) Cross-sectional SEM image of the wafer structures.

In the second batch of wafers, we have studied three parameters to increase the device *BV*:

(a) carrier concentration in the n⁻-GaN drift region. The n⁻-GaN was lightly carbon (C) doped by using propane as C-source, to introduce deep acceptors in GaN to compensate the non-intentional-doping introduced by point-defects and other impurities in GaN. The carrier concentration as a function of depth was revealed by the electrochemical *C-V* measurement performed in Prof. Nicolas Grandjeans' group at EPFL (Figure 2-16). The [C] concentration was estimated to be ~1×10^{16} cm⁻³. As shown in Figure 2-16, the net donor concentration in the n⁻-GaN drift layer was reduced from 3×10^{16} cm⁻³ to 1×10^{16} cm⁻³ with the [C] compensation.

(b) n⁻-GaN drift layer thickness. By utilizing a thicker Si substrate and better stress engineering within the transition layers, the n⁻-GaN drift layer thickness was able to increase from 1.5 μm to 2.7~3.5 μm, without inducing any cracks in the wafer.

(c) p-GaN layer thickness. With a high doping level in p-GaN (Mg: $>1 \times 10^{19}$ cm⁻³, $N_A > 6 \times 10^{17}$ cm⁻³), we also studied the effect of reducing p-GaN thickness to enable an even thicker n⁻-GaN drift layer.
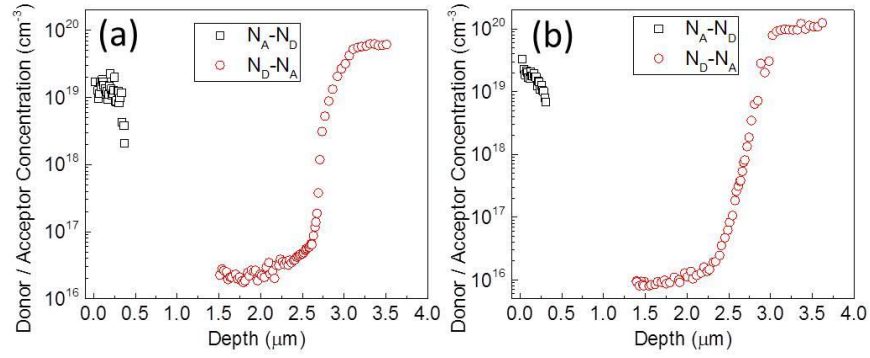
Figure 2-16 Donor/acceptor concentration profiles in the GaN wafers (a) without and (b) with C

doping in the drift region, measured by electrochemical *C-V* measurements.

Table 2-1 summarizes the wafer information and the *BV* of 10 devices fabricated on each wafer. Four 2nd-generation wafers were utilized in the *BV* study. Compared to wafer #1, wafer #2 increases n⁻-GaN thickness with similar p-GaN thickness and N_D-N_A in n⁻-GaN; wafer #3 further increases n⁻-GaN thickness at a cost of reduced p-GaN thickness; wafer #4 reduces the N_D-N_A in n⁻-GaN by [C] doping, with similar p-GaN and n⁻-GaN thickness to wafer #1. As shown, at a N_D-N_A level of 3×10^{16} cm⁻³, the increase of *BV* resulted from an increased n⁻-GaN thickness is quite limited. However, a N_D-N_A reduction from 3×10^{16} cm⁻³ to 1×10^{16} cm⁻³ sees a *BV* increase of about 100 V. This result demonstrates the importance of having low N_D-N_A in the drift region.

The measured *BV* can be well understood by the classical analytical model of pn diodes. By modifying the Equation (2-1) and assuming a strong depletion in p-GaN layer to support the peak electric field, E_{peak}, we can derive Equation (2-2):

$$BV = \frac{1}{2}E_{peak}d_{p-GaN} + \frac{1}{2}(2E_{peak} - \frac{q}{\varepsilon}N_D d_{n^--GaN})d_{n^--GaN} \qquad (2\text{-}2)$$

From the equation above, the E_{peak} derived for the 2nd-generation GaN-on-Si devices is 2.2-2.4 MV/cm, which is similar to that in our 1st-generation devices and still has room

for further improvement. On the other hand, by further reducing the edge type dislocation density, we expect to be able to increase the n$^-$-GaN layer thickness by at least 1.2 μm (reaching 4 μm) without requiring an additional AlN interlayer. Given the current E_{peak} and N_D (1×10^{16} cm^{-3}), this thickness increase would enable a *BV* of ~800 V. A combination of higher material quality (higher E_{peak} to 2.8-2.9 MV/cm [16]), thicker n$^-$-GaN layer (4-5 μm) and lower N_D (below 1×10^{16} cm^{-3}) could potentially push the *BV* of vertical GaN-on-Si devices to above 1000-1200 V.

Table 2-1 Information for the 1st-generation and 2nd-generation wafers, and the high value, low value and average value of the *BV* of 10 devices fabricated on each wafer.

Wafer #	1st-Generation	2nd-Generation			
		#1	#2	#3	#4
p-GaN Thickness (μm)	0.5	0.35	0.35	0.25	0.35
n$^-$-GaN Thickness (μm)	1	2.7	3.0	3.4	2.7
N_D-N_A in n$^-$-GaN (cm^{-3})	6×10^{16}	3×10^{16}	3×10^{16}	3×10^{16}	1×10^{16}
*BV*_High (V)	300	380	404	484	530
*BV*_Low (V)	220	340	350	364	385
*BV*_Average (V)	265	366	372	418	465

2.4 Forward On-resistance Modeling and Optimization

In our demonstrated GaN-on-Si vertical diodes, as shown in Figure 2-17 (a), a mesa structure is formed by deep etching and two electrodes located on the same side of the

wafer. This structure is named as a 'quasi-vertical' structure. In contrast, the structure is named as a 'fully-vertical' structure if the two electrodes are located on different sides of the wafer (e.g. top side and bottom side). Typically, it is easy to make fully-vertical GaN devices on free-standing GaN layers and extremely difficult on foreign substrates, such as Si and sapphire, due to the insulated transition layers.

In quasi-vertical structures, although the current flows dominantly in the vertical direction, it would typically have non-uniform distribution in the lateral direction. This indicates that the device R_{on} is not only dependent on the resistivity of each epitaxial layer, but also on the current distribution in the drift region. To understand the device R_{on}, we fabricated quasi-vertical GaN-on-Si diodes on several different wafers, calibrated a TCAD simulation model and utilized the simulation model to unveil the key factors determining R_{on}.
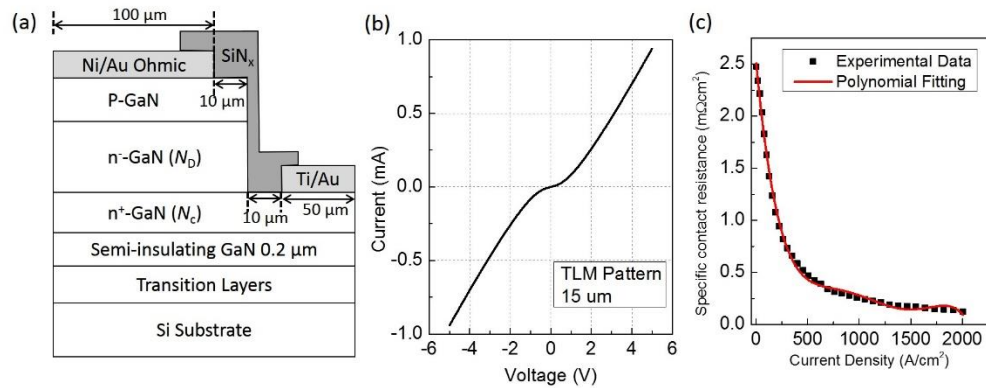
Figure 2-17 (a) Schematic of GaN-on-Si quasi-vertical diodes; (b) *I-V* characteristics measured on two p-GaN Ohmic contacts separated by 10 um; (c) Dependence of specific contact resistance on current density, extracted from the TLM measurements and from fitting.

To improve the accuracy of our R_{on} model, the contact resistance of p-GaN is measured as a function of current density. The specific contact resistance and current density are measured by the transfer length method (TLM) and calculated by using the effective contact area (the contact width times the transfer length). As shown in Figure 2-17 (b) and (c), due to a slight non-linearity in the *I-V* characteristics of the p-GaN contacts, the extracted specific contact resistance shows a strong dependence on the current density at low current density levels. This dependence was fitted by a polynomial fitting expression, which was incorporated into the TCAD simulation model for contact resistance.

Four GaN-on-Si wafers were used for understanding and optimizing the R_{on}, with their information listed in Table 2-2. Compared to the wafer IV (1st-generation wafer), the doping level of n[+]-GaN layer is increased from 10^{18} cm[-3] to 10^{20} cm[-3] in wafer I-III. The high n-type doping level in GaN, 10^{20} cm[-3], was enabled by utilizing Ge doping. In addition, wafers I and II have larger n[+]-GaN thickness than wafer III. The sheet resistance (R_s) of n[+]-GaN layer was measured by etching down to the interface of n[-]-GaN/n[+]-GaN and fabricating TLM patterns. As shown in Table 2-2, the wafers I and II have the smallest R_s of n[+]-GaN layer, followed by the wafer III (due to smaller thickness), and the wafer IV has the largest of R_s due to lower doping level. The specific R_{on} of quasi-vertical GaN-on-Si diodes fabricated on the four wafers is also listed in Table 2-2. The specific R_{on} are all extracted as a differential R_{on} at a forward bias of 7 V. The extraction at this relatively large forward bias is to eliminate the impact of non-ideal contact resistance.

Table 2-2 Wafer composition information, measured n^+-GaN sheet resistance and total device R_{on} for the four wafers used for on-resistance study.

	2nd-Generation			1st-Generation
Wafer #	I	II	III	IV
n^--GaN Thickness (μm)	2.7	2.7	2.7	1
N_D-N_A in n^--GaN (cm^{-3})	3×10^{16}	1×10^{16}	3×10^{16}	6×10^{16}
n^+-GaN Thickness (μm)	0.5	0.5	0.3	0.3
N_D-N_A in n^+-GaN (cm^{-3})	10^{20}	10^{20}	10^{20}	10^{18}
Sheet resistance of n^+-GaN (Ω/sq)	20	20	35	620
Diode specific differential R_{on} (mΩ·cm^2)	1	1.05	1.42	10

TCAD simulations were performed using the Silvaco ATLAS simulator, based on the simulation models previously developed for GaN lateral and vertical power devices by the author [4], [28]. In our simulation model, the doping level dependence of the electron mobility at room temperature was described by the following expression [29], on the base of the well-known Caughey-Thomas approximation:

$$\mu(N) = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \frac{N}{N_g}} \qquad (2\text{-}3)$$

Based on the Hall and TLM measurements for n^--GaN and n^+-GaN layers, the values of the parameters μ_{min}, μ_{max} and N_g of 55 cm^2/Vs, 1000 cm^2/Vs and 2×10^{17} cm^{-3} provided the best fitting for the experimental results. The mobility and free hole concentration of the p-GaN was determined as 10 cm^2/Vs and 6×10^{17} cm^{-3} (wafer I and II), 12 cm^2/Vs and 3×10^{17} cm^{-3} (wafer III), 14 cm^2/Vs and 1.5×10^{17} cm^{-3} (wafer IV), respectively, as revealed by the Hall measurement.

Figure 2-18 shows the simulated and experimental forward *I-V* characteristics for the quasi-vertical GaN-on-Si diodes fabricated on the four wafers. A good agreement was achieved between simulation and experiment, justifying the validity of the developed simulation models in describing the forward *I-V* characteristics.
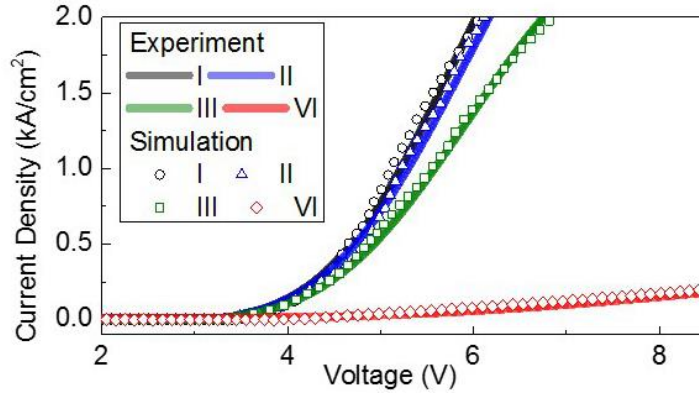
Figure 2-18 Forward *I-V* characteristics of quasi-vertical GaN-on-Si wafers fabricated on four wafers from experiment and simulation.

Figure 2-19 (a)-(c) shows the simulated current density distribution in the quasi-vertical pn diodes on the wafers with different n^+-GaN layer doping levels and thicknesses. The n^+-GaN layers in the structure (a) and (b) have the same n^+-GaN thickness (t_c) but different doping levels (N_c). As shown, in the device (b), the current distribution is much more spread in n^--GaN and n^+-GaN, while the current in the device A is crowded in the regions below the anode edge. The n^+-GaN layers in the structure (b) and (c) have different t_c and N_c, but the same R_s (=$1/q\mu_c t_c N_c$). As shown, the current distribution in the diode B and C is identical in n^--GaN, p-GaN and n^+-GaN. This identical distribution is confirmed by extracting the normalized current density distribution along the cutline #1 and cutline #2 (the cutline locations are illustrated Figure

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2-19 (a)), as plotted in Figure 2-19 (d) and (e). This indicates that in a quasi-vertical diode with the same p-GaN and n$^-$-GaN layers, the sheet resistance of n$^+$-GaN determines the current distribution in the drift region and therefore the diode total R_{on}. This dependence is not difficult to understand physically, as all the current in the drift region will enter the n$^+$-GaN layer and flow laterally towards the cathode. If the R_s of n$^+$-GaN layer is small enough, there is not much difference of resistance for the current paths close to or far away from the anode edge. As a result, the current tends to be more spread into the regions far away from the anode edge. It is interesting that this lateral current spreading in the drift region can be approximated by an exponential distribution, as shown in Figure 2-19 (f). From the exponential fitting, we can define a current spreading length, which increases for the reduced R_s of the n$^+$-GaN. For example, the current spreading length is ~9.1 μm for the device A and ~20 μm for the device B or C.
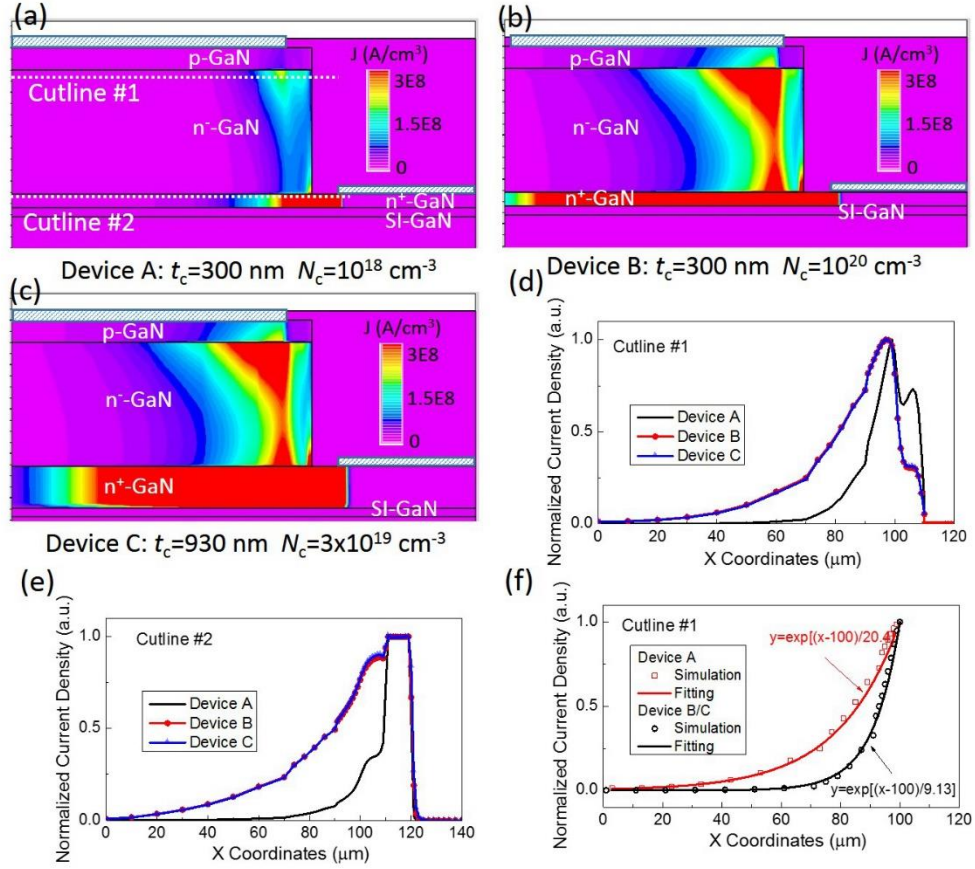
Figure 2-19 (a)-(c) Simulated current density distribution in the pn diodes with different n$^+$-GaN doping level and thickness; (d)-(e) Current density along the cutline #1 and #2 in the simulation results presented in (a)-(c). (f) Exponential fitting for the lateral current distribution along the cutline #1.

After finding out the importance of the R_s of n$^+$-GaN layer, it is also important to see the impact of the drift region (n$^-$-GaN) doping level. The dependence of diode R_{on} on the R_s of n$^+$-GaN is simulated for three doping levels of the drift region, $N_D=2\times10^{15}$ cm^{-3}, 1×10^{16} cm^{-3} and 5×10^{16} cm^{-3}. As shown in Figure 2-20, the device R_{on} is almost independent of the drift region doping level in this N_D range (10^{15}~10^{17} cm^{-3}). This indicates that in this doping range, the diode R_{on} would be mainly determined by the current distribution in the drift region, and therefore by the R_s of n$^+$-GaN layer, regardless

of the drift region doping level. A reduction of the R_s of n$^+$-GaN layer by two orders of magnitude can roughly lead to a reduction of the diode R_{on} by one order of magnitude.
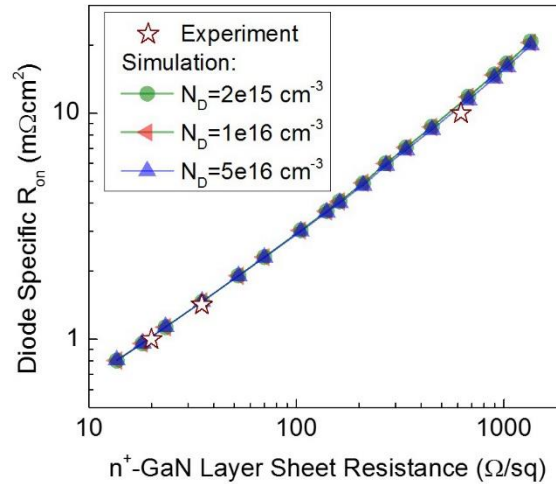
Figure 2-20 Dependence of diode specific R_{on} on n$^+$-GaN layer sheet resistance, for three drift region doping levels, from simulation and experiment.

Another parameter determining the diode specific R_{on} is the anode radius. Ideally, if the current distributes uniformly in the drift region, the specific R_{on} is independent on diode radius; if the current aggregates near the anode edges, the current would scale up with the diode perimeter and the specific R_{on} would then be proportional to the diode radius. Figure 2-21 shows the simulated and measured specific R_{on} for diodes on different wafers. The good agreement between simulation and experiment has confirmed the validity of our simulation models. As shown, the diode specific R_{on} is linearly proportional to the diode radius when the diode radius is larger than the current spreading length. When the diode radius is reduced to be equivalent to or below the current spreading length, the current distribute much more uniform in the total diode region and the specific R_{on} is almost independent of diode radius. Also, the current spreading length

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decreases with the increased R_s of n$^+$-GaN layer. As a result, in the wafer IV with highest R_s of n$^+$-GaN layer, the linear relationship between diode R_{on} and diode radius still applies for a small diode radius of 10 μm.
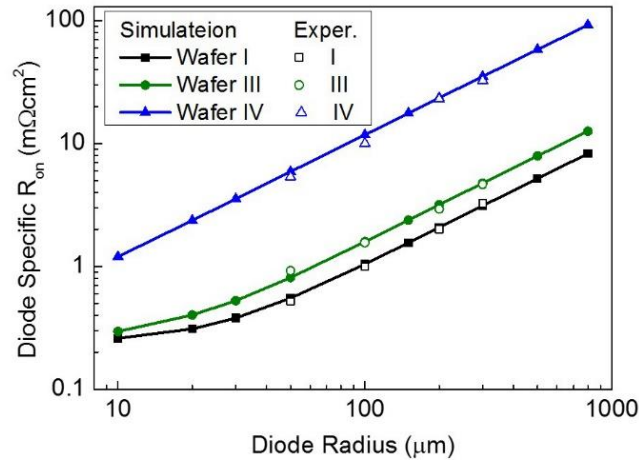
Figure 2-21 Dependence of diode specific R_{on} on the diode anode radius, from simulation and

experiment.

In summary, in section 2.4 we developed and calibrated a simulation model which could well describe the forward characteristics of quasi-vertical GaN-on-Si diodes. Based on the simulation model, we found that the diode R_{on} is mainly dependent on two parameters: (a) R_s of n$^+$-GaN layer, which determines the current distribution in the drift region; and (b) diode radius. This simulation model enabled the understanding of the design space of diode R_{on}. By reducing the R_s of n$^+$-GaN layer in the wafer, we successfully reduced the diode R_{on} from ~10 mΩ cm^2 to ~1 mΩ cm^2.

2.5 Fully-vertical GaN-on-Si Diodes

In section 2.4, we presented the forward current density and on-resistance modulation for quasi-vertical GaN-on-Si diodes. As can be seen, an issue with the quasi-vertical GaN-on-Si diodes is the limited capability in current scaling. From Figure 2-21, it is shown that for quasi-vertical GaN-on-Si diodes, even with the low-R_s current spreading layer (e.g. wafer I), the R_{on} increases with the diode radius, which makes it challenging to get large current from quasi-vertical diodes. A fundamental solution to this issue is the adoption of a fully-vertical structure. However, the highly insulating and defective transition layers between the Si substrate and GaN epi-layers prevents directly making fully-vertical devices on the original GaN-on-Si wafer.
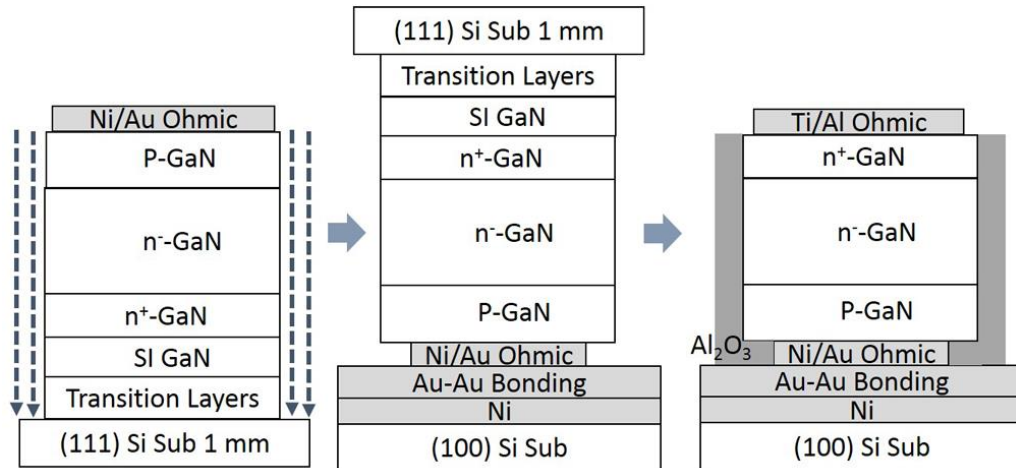
Figure 2-22 Main fabrication steps for fully-vertical GaN-on-Si pn diodes.

In this chapter, we demonstrated the fabrication of fully-vertical GaN-on-Si diodes based on a layer transfer technology. The schematic of main fabrication steps is shown in Figure 2-22. The GaN mesa isolation etch was extended down to the Si substrate. A Ni (15 nm) / Au (50 nm) bilayer was deposited on p-GaN followed by annealing in a N_2/O_2

mixture at 550 $^{\circ}$C. A low Ohmic contact resistance of 10^{-5}-10^{-4} $\Omega \cdot cm^2$ was achieved. After the p-GaN Ohmic formation, an additional Au layer (350 nm) was deposited to enable the bonding to an Au (350 nm)/Ni (200 nm)-coated Si (100) substrate. The bonding was performed through thermal compression at 300 $^{\circ}$C for 20 minutes. The Ni layer was used to protect the Si substrate from potential high-energy etching in the following steps. After the bonding, the original Si (111) substrate was completely removed by dry etching in a deep dry etch system using an SF_6-based plasma [30]. Figure 2-23 shows a photo of a sample piece after original Si substrate removal. As shown, almost 100% of the devices (circular and rectangular patterns) in all the four dies succeeded in this layer transfer process, exhibiting a high process yield.

The transition layers and semi-insulating GaN layers were then etched to reach the N-face of n$^+$-GaN layer. Ti/Al-based Ohmic contact was then formed on top of the n$^+$-GaN layer. A 20 nm Al_2O_3 passivation layer was deposited by atomic layer deposition.
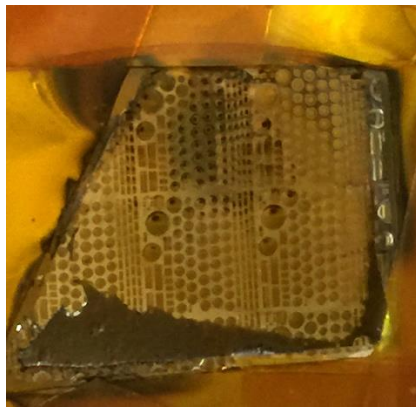
Figure 2-23 Photo (taken by iPhone) of a sample piece of the fully-vertical GaN-on-Si pn diodes after

original Si substrate removal.

Despite of the high yield for the bonding and Si substrate removal processes, the following etching step for removing the transitional layers needs to be further optimized. In the current Cl_2/BCl_3-based dry etching, etching residues have been observed and the surface roughness was measured as up to ~100 nm. In addition, this etching was mainly controlled by the etching time, which might have uniformity problems for wafer-level processes. Optimization of the etching recipes and the insertion of an etching stop layer should be performed in the future to increase device uniformity.

2.6 Electrical Characteristics of Quasi- and Fully-Vertical pn Diodes

After the study and optimization of the reverse and forward characteristics in sections 2.3 and 2.4, we fabricated quasi- and fully-vertical pn diodes based on the wafer structure consisting of 0.3 μm p-GaN (Mg: $>1 \times 10^{19}$ cm^{-3}, $N_A > 6 \times 10^{17}$ cm^{-3}), 2.7 μm n$^-$-GaN drift layer ($N_D \sim 1 \times 10^{16}$ cm^{-3} with [C] compensation), 0.5 μm n$^+$-GaN current collecting layer (Ge: $>1 \times 10^{20}$ cm^{-3}, $N_c \sim 10^{20}$ cm^{-3}) and 0.2 μm iron-doped semi-insulating GaN. The GaN layers were all grown by metal-organic chemical vapor deposition (MOCVD) on 2-inch (111) Si substrates by using AlGaN-based transition layers, by Prof. Armin Dadgar's group.
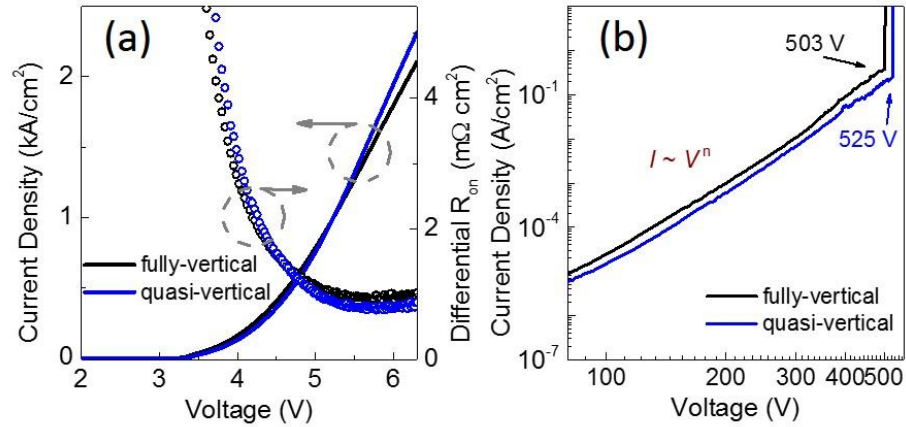
Figure 2-24 (a) Forward *I-V* and differential R_{on} characteristics and (b) reverse *I-V* characteristics for the quasi- and fully-vertical GaN-on-Si pn diodes.

Figure 2-24(a) shows the representative forward *I-V* characteristics and the extracted differential R_{on} for quasi- and fully-vertical GaN-on-Si pn diodes. The forward current is normalized with respect to the anode area (anode diameter 200 μm). The turn-on voltage (V_{on}) is 3.4 V for both pn diodes, close to the bandgap of GaN. A differential R_{on} of 0.8 mΩ·cm^2 and 1 mΩ·cm^2 is extracted for quasi- and fully-vertical diodes, respectively, at a current density over ~kA/cm^2 and a forward bias of 5.3 V. This high forward current level is comparable to state-of-the-art GaN-on-GaN vertical diodes. The R_{on} for the quasi-vertical devices is 10× lower than our first-generation devices, even with a thicker drift layer, which shows the importance of the low-R_s n$^+$-GaN layer used in the second-generation devices.

The R_{on} of fully-vertical GaN-on-Si pn diodes is similar to quasi-vertical diodes. According to TCAD simulation, if the resistance of Si substrate is not considered, the R_{on} of fully-vertical GaN-on-Si pn diodes should be at least ~40% lower than quasi-vertical diodes, due to the more uniform current distribution. The higher R_{on} than the simulation

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results in fully-vertical pn diodes could be attributed to the resistance of Si substrate and the etching-induced defects in the top n[+]-GaN layers. Thinning the Si substrate before bonding and the optimization of etching recipes are expected to further reduce the R_{on} of fully-vertical GaN-on-Si pn diodes.

Despite of the higher experimental R_{on} than in simulations, the advantages of fully-vertical structure have been demonstrated by the R_{on} dependence on anode radius. As shown in Figure 2-21, the specific R_{on} increases with diode radius for quasi-vertical diodes due to the non-uniform current distribution. From the measurement, the fully-vertical diodes with anode radiuses of 50 μm, 100 μm, 150 μm, 200 μm and 300 μm shows similar specific R_{on}. This indicates that fully-vertical diodes require much smaller chip area than quasi-vertical diodes to achieve the high current rate (e.g. 50 A or 100 A).

Figure 2-24 (b) shows the representative reverse *I-V* characteristics of quasi- and fully-vertical diodes. A *BV* over 500 V was demonstrated in both diodes, with a leakage current density ~5×10^{-3} A/cm^2 at -300 V and below 10^{-2} A/cm^2 at -400 V, which is about two orders of magnitude lower than the leakage in our first-generation devices. To our knowledge, this leakage current density is the lowest among all the reported GaN vertical diodes on foreign substrates (references in the next chapter), lower than the leakage of GaN lateral diodes, and comparable to commercial SiC diodes. Similar to our first-generation devices, the off-state leakage mechanism was dominated by the trap-assisted space charge limited current (SCLC). For both fully- and quasi-vertical diodes, reverse current increases with V^n, until a voltage hump, the trap-filled-limited voltage (V_{TFL}), at over 500 V. It should be noted that the trap-filling-induced V_{TFL} is a soft *BV* and has strong ruggedness. Zou *et al.* recently demonstrated that this SCLC-dominated reverse

current mechanism can enable the GaN-on-Si vertical diodes to survive the repetitive avalanche tests with a surge current at a surge voltage much higher than the V_{TFL} [31].

It should be noted that we have observed different device leakage mechanisms in different GaN-on-Si wafers. As shown in Figure 2-13 and discussed in section 2.3.2, after introducing a series of advanced edge termination processes, our first-generation vertical GaN-on-Si diodes based on the DOWA wafers exhibited a change in the leakage mechanism from SCLC to variable-range hopping. In our second-generation devices based on the wafers grown by Prof. Dadgar's group, we found the trap-assisted SCLC is still the dominant leakage mechanism for most of the devices. The similar leakage mechanisms in fully-vertical diodes indicated these traps locate in the bulk GaN and are probably related to dislocations or defects. The leakage mechanism will be discussed in more details in Chapter 3.

Figure 2-25 (a) and (b) shows representative forward and reverse *I-V* characteristics of quasi-vertical diode at high temperatures up to 300 $^{\circ}$C. The fully-vertical diode exhibited almost identical behavior at high temperatures. As shown, a low R_{on} of 1.35 mΩ·cm^2 is extracted at 300 $^{\circ}$C, presenting small degradation compared to the R_{on} at room temperature. The R_{on} and current density are expected to be further improved by enhancing the heat dissipation of the diode structure (e.g. thinning Si substrates). The *BV* and leakage current at high reverse bias show little dependence with temperature. This is consistent with previous reports on trap-assisted SCLC mechanism [16].
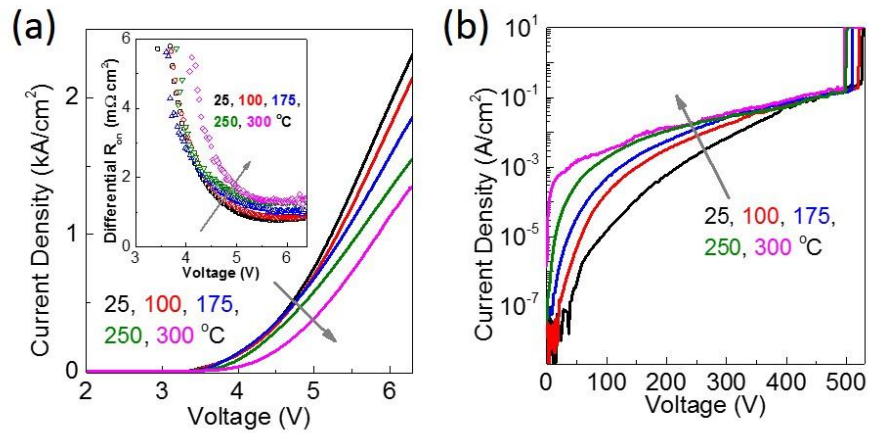
Figure 2-25 (c) Forward *I-V* and differential R_{on} characteristics and (b) reverse *I-V* characteristics of the quasi-vertical GaN-on-Si pn diodes at 25-300 ^{o}C. Similar high-temperature forward and reverse characteristics was observed for the fully-vertical pn diodes.

Figure 2-26 shows the reverse recovery characteristics of the quasi- and fully-vertical pn diodes, measured by an on-wafer pulser setup. The device was switched from a forward current of ~400 A/cm^2 to pinch off with reverse voltage of 200 V (setup limits). A reverse recovery time of 50 ns was extracted in our GaN-on-Si diodes, which is comparable to the best reports for GaN-on-GaN pn diodes [32][33].
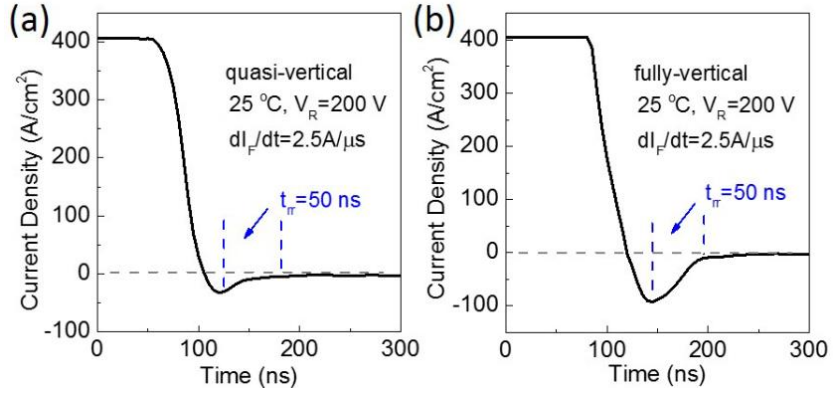
Figure 2-26 Reverse recovery characteristics of (a) quasi-vertical and (b) fully-vertical GaN-on-Si pn diodes, measured by an on-wafer pulser setup. The reverse recovery time (t_{rr}) was extracted between the 90% and 10% of the peak reverse current.

From the measured reverse recovery characteristics, the minority carrier lifetime in GaN-on-Si structure can be extracted by using a simplified method based on the one reported in [34]. Figure 2-27 shows the schematic of a reverse recovery curve.
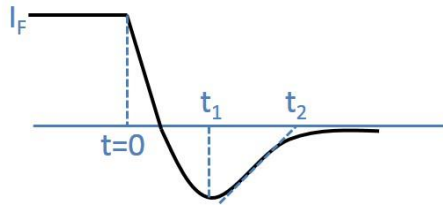
Figure 2-27 Schematic of a reverse recovery curve.

Based on a triangular approximation, the total minority charge $Q(t)$ can be written as

$$\frac{dQ(t)}{dt} + \frac{Q(t)}{\tau_{hl}} = i(t) \approx I_F - \beta t \qquad (2\text{-}4)$$

where $\beta = \frac{dI}{dt}$ is the current ramp rate and τ_{hl} is the high-level minority charge lifetime. Solve the above differential equations with the initial condition $Q(0) = I_F\tau_{hl}$:

$$Q(t_1^-) = \beta\tau_{hl}^2(1 - e^{-\frac{t_1}{\tau_{hl}}}) - \beta\tau_{hl}t_1 + I_F\tau_{hl} \qquad (2\text{-}5)$$

On the other hand, the charge continuity requires $Q(t_1^-)=Q(t_1^+)$, where the $Q(t_1^+)$ is the remaining charge in the device at t_1 and is determined by numerical integration of the measured I(t) waveform in the $t_1<t<t_2$ region.

By utilizing the method above, a minority carrier time of ~9 ns was extracted, which is longer than the reported lifetime in GaN-on-sapphire [35] (2~3 ns) and close to the one in GaN-on-GaN [36] (~13 ns), indicating the high quality of our GaN-on-Si epi-structures.

2.7 Benchmarking and Prospect

To benchmark our GaN-on-Si vertical diodes, Figure 2-28 presents the R_{on} *v.s.* *BV* of GaN vertical diodes on different substrates [11][22][37][38][39][40][41][42]. Our latest results present a record performance for vertical GaN-on-Si diodes, with the Baliga's Figure of Merit (BV^2/R_{on}) of 0.32 GW/cm^2. Considering the large diameter (8-inch) and low cost (~$0.08/cm^2) of Si substrate, comparing to the diameter and cost of sapphire and GaN substrates (sapphire: 4-inch, ~$2.2/cm^2; GaN: 2-inch, ~$100/cm^2) [17], our 500-V class GaN-on-Si vertical diodes have remarkable cost advantages, while maintaining the key advantages of GaN vertical devices (e.g. high current, high-temperature operation, small device area, etc.).

Also, the high *BV*, low R_{on}, high forward current and short reverse recovery time of our GaN-on-Si vertical pn diodes indicates great potential to demonstrate high-performance and low-cost GaN-on-Si vertical power transistors and advanced rectifiers. These devices could further improve the power switching performance by eliminating the adverse effects of the relatively large turn-on voltage in the GaN-on-Si vertical pn diodes, and therefore provide competitive low-cost devices for 200-600 V power switching applications.
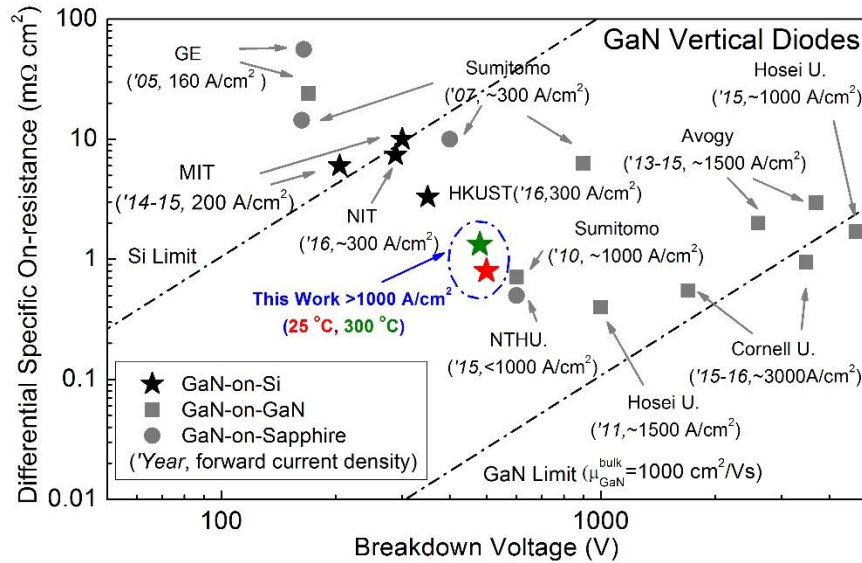
Figure 2-28 R_{on} v.s. *BV* of GaN-on-Si vertical diodes demonstrated in this work and the ones in previous reports. The forward current density is extracted at the bias for differential R_{on} extraction.

Looking forward, further work is needed in the following three aspects to push the limit of vertical GaN-on-Si devices and make them competitive for commercialization:

(a) Demonstrate higher *BV* capability. As discussed in section 2.3.3, thicker n⁻-GaN layer (4-5 μm) and lower N_D (below 1×10^{16} cm⁻³) could potentially push the *BV* of vertical GaN-on-Si devices to above 1000-1200 V.

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(b) Demonstrate novel fully-vertical GaN-on-Si device structures. As discussed in section 2.4, fully-vertical structure has remarkable advantages than quasi-vertical structure in obtaining low on-resistance and high current. The approach to demonstrate fully-vertical devices, as demonstrated in section 2.5, requires complicated bonding and etching processes, which may be particularly difficult to achieve high-yield wafer-level processes. A recent report demonstrated fully-vertical GaN-on-Si diodes by doping the transition layers [41]. However, the on-resistance for the doped transition layers is high. Also, there may be concerns on the dynamic switching performance of the device due to the high defect/dislocation densities in the transition layers. In this regard, novel fully-vertical GaN-on-Si device structures need to be designed and optimized.

(c) Demonstrate 600-1200 V high-current and low-cost GaN-on-Si vertical power transistors and advanced rectifiers. Compared to vertical pn diodes, these devices could further improve the power switching performance and make it easier for the market insertion of vertical GaN-on-Si power devices.

Chapter 3 Design Space and Origin of Leakage Current in Vertical GaN Devices

3.1 Introduction

Off-state leakage current is a key factor determining the device *BV*, power circuit loss and, potentially, device and circuit reliability. As discussed in Chapter 1, if a vertical power device is well designed with good edge termination and electric field management, drift region will typically determine the device *BV* and off-state leakage current at high reverse biases. In particular, in many power transistors and advanced Schottky barrier rectifiers, the peak electric field locates in the p-n junction within the device structure. Thus, it is important to understand the origin and mechanism of the leakage current in vertical pn diodes.

Table 3-1 lists the leakage current, on/off ratio and substrate cost for state-of-the-art vertical GaN pn diodes on different substrates. As shown, vertical GaN diodes on free-standing GaN substrates can offer the best performance with the highest cost. Vertical GaN diodes on Si and sapphire substrates have 2~3 orders of magnitude higher leakage current but 2~3 orders of magnitude substrate costs. For the commercialization of vertical GaN power devices, it is essential to understand the design space and the performance *v.s.* cost trade-off for the devices on different substrates.

In the work presented in this chapter, we fabricated GaN vertical diodes on different substrates, and then unveiled the leakage mechanism of GaN vertical devices by analytical calculations and TCAD simulation. Finally, the design space of leakage current in GaN vertical devices was derived and benchmarked with GaN lateral, Si and SiC devices.

Table 3-1 Leakage current, on/off ratio and substrate cost for lateral and vertical GaN diodes on different substrates.

Diode Structure		Leakage at -200 V (A/cm^2)	I_{on}/I_{off} ratio (I_{off} @-200 V)	Available Substrate	Substrate Cost per CM^2
Vertical GaN Diodes	GaN-on-Si	10^{-4}	$\sim 10^7$	200 mm Si	~$0.08
	GaN-on-sapphire	10^{-3}	$\sim 10^6$	100 mm sapphire	~$2.2
	GaN-on-GaN	10^{-6}	$\sim 10^9$	50 mm GaN	~$50-100
AlGaN/GaN Lateral Diodes		$10^{-3} \sim 10^{-2}$	$10^5 \sim 10^6$	200 mm Si	~$0.08

3.2 Device Fabrication and Material Characterizations

As shown in Figure 3-1, GaN vertical p-n diodes were fabricated on GaN, sapphire and Si substrates with similar doping levels in p-GaN. The GaN-on-GaN and GaN-on-sapphire wafers were provided by IQE with 9.5 µm and 4 µm n$^-$-GaN drift region ($N_D \sim 2 \times 10^{16}$ cm^{-3}) epitaxial grown on 2-inch GaN and sapphire wafers by MOCVD, respectively. The GaN-on-Si wafers used in this work are the wafers provided by DOWA with 1 µm n$^-$-GaN drift region ($N_D \sim 6 \times 10^{16}$ cm^{-3}). The detailed wafer compositions were described in section 2.2. GaN-on-GaN vertical diodes have a fully-vertical structure. GaN-on-Si and GaN-on-sapphire diodes have a quasi-vertical structure due to insulating buffer/transistion layers. Similar passivation and field plate processes were applied to all three diodes. The advanced edge termination technologies, as demonstrated in section 2.3.2, were applied to the quasi-vertical GaN-on-Si and GaN-on-sapphire diodes.
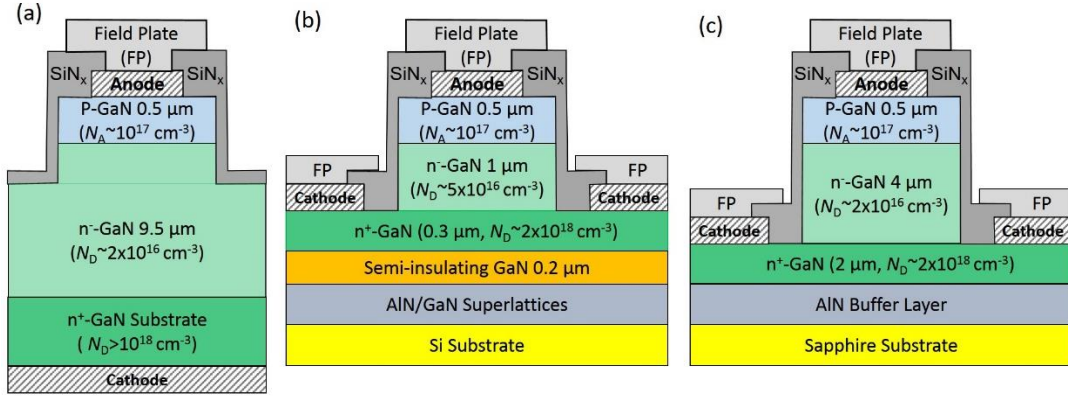
Figure 3-1 Schematic of the fabricated GaN vertical p-n diodes on (a) GaN, (b) Si and (c) Sapphire

substrates.

The total dislocation density of GaN-on-GaN, GaN-on-sapphire and GaN-on-Si structures are ~10^7, ~10^9 and ~10^9 cm^{-2}, measured by the commercial wafer providers. The total screw dislocation densities of the three structures are ~8×10^6, ~10^8 and ~5×10^8 cm^{-2}, estimated from X-ray rocking curves based on the method reported in [43], as shown in Table 3-2. It has been reported that the pure screw dislocation is directly related to bulk leakage in GaN [44]. The pure screw dislocation density is typically 3%~5% of the total dislocation density and 5%~20% of the total screw dislocation density for GaN epitaxial layers by MOCVD or MBE [43][44]. In this work, we utilized a pure screw dislocation density as 10% of the measured total screw dislocation density as the initial input into TCAD simulation model for fitting iterations. The accurate pure screw dislocation density was determined by the best fitting between simulation and experiments.

Table 3-2 Total screw dislocation density of GaN on different substrates, estimated from the full-width

at half-maximum (FWHM) intensity of X-ray diffraction (XRD) rocking curve.

Substrate	FWHM of rocking curve (deg)		Screw Dislocation Density (cm^{-2})
	(0002)	(0004)	
GaN	0.01784	0.01814	GaN
Sapphire	0.07126	0.05334	Sapphire
Si	0.14473	0.14105	Si

3.3 Analytical Study of the Leakage Current Origin

In general, the off-state leakage current in a semiconductor device can be classified into three main categories: electrode-limit conduction mechanism, surface-limit conduction and bulk-limit conduction [45]. The electrode-limit conduction mechanism typically relates to the metal-semiconductor contact, such as Schottky emission, Fowler-Nordheim tunneling, direct tunneling and thermionic-field emission. However, in a properly-designed vertical power devices, the device leakage current under high reverse electric field is dominated by the surface-limit conduction and bulk-limit conduction, rather than the electrode-limit conduction. This is particularly true for a well-designed vertical pn diode, where the peak electric field located in the pn junction rather than the top or bottom Ohmic contacts.

Figure 3-2 illustrates the main conduction mechanisms in GaN layers under high electric field. The first main category is surface-limit conduction, such as the leakage current along the etching sidewalls as illustrated in section 2.3. As shown in Figure 3-1, this surface-limit conduction is particularly easy to be found in GaN-on-sapphire and GaN-on-Si vertical diodes, where a quasi-vertical structure is adopted. Therefore, a study of the relationship between the leakage current on device periphery/area is important.

Figure 3-3 shows the leakage current density of GaN-on-Si and GaN-on-sapphire quasi-vertical diodes as a function of the anode radius R. As shown, no linear dependence between the current density and 1/ R is found. This indicates that the bulk component rather than the surface leakage is the main contribution to device leakage current.
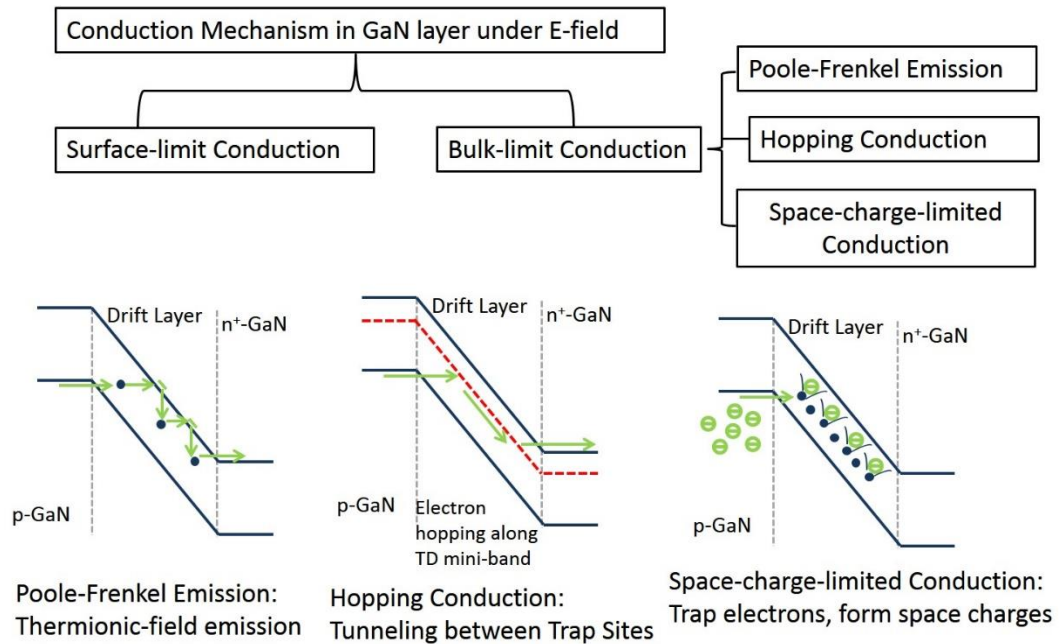
Figure 3-2 Diagram illustrating the classifications of leakage mechanism in GaN layer under high electric field and the concepts of Pool-Frenkel, hopping and space-charge-limited transport models.
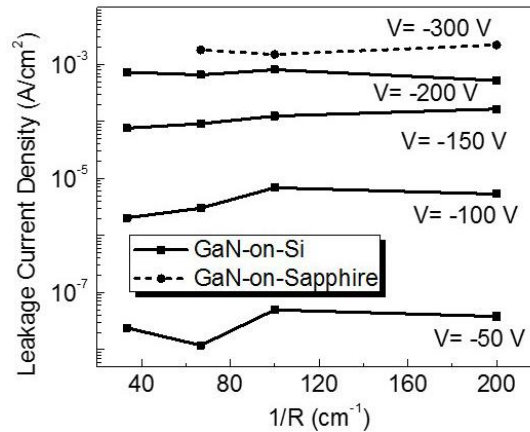
Figure 3-3 Leakage current density of GaN-on-Si and GaN-on-sapphire vertical diodes with different

anode radius *R*.

In a p-n diode under reverse bias, the depletion region can be considered as an insulating layer under a strong electric field [46]. Three bulk-limited conduction processes in GaN epitaxial layers, as revealed by prior researchers, are Poole-Frenkel (P-F) emission, variable-range hopping conduction and space-charge-limited conduction (SCLC), as shown in Figure 3-2. The P-F emission involves the thermal excitation of electrons emitting from traps into the conduction band. The high electric field could greatly reduce the Coulomb potential energy of an electron in a trapping center and facilitate this thermal excitation. Therefore, the P-F emission is often observed at high electric field and high temperature. The hopping conduction is due to the tunneling effect of trapped electrons "hopping" from one trap site to another in dielectric films. In essence, the P-F emission corresponds to the thermionic effect and the hopping conduction corresponds to the tunnel effect. In P-F emission, the carriers can overcome the trap barrier through the thermionic mechanism. In hopping conduction, the carrier energy is lower than the maximum energy of the potential barrier between two trapping sites. In

such case, the carriers can still transit using the tunnel mechanism. The SCLC mechanism has been discussed in Chapter 2. In the trap-assisted SCLC mechanism, the injected free carriers from the pn junction will be captured by acceptors, forming space charges. The leakage current will be modulated by space charges until all acceptors are filled up and the current rapidly jump from a low trap-limited value to a high trap-free SCLC.

Table 3-3 summarizes the conduction processes and the correlation between the leakage current versus electric field and the leakage current versus temperature for each leakage mechanism [46]. In the following paragraphs, we are going to identify the main leakage process of a vertical GaN pn diodes based on the different leakage dependence.

Table 3-3 Summary of conduction mechanisms in insulators under high electric field that can impact the off-state leakage in GaN vertical devices.

Mechanism	Expression	E-field Dependence	Differential Slope
Poole Frenkel (P-F)	$I = I_0 \exp(\frac{\beta_{PF}E^{0.5}}{k_B T})$	$\ln(I) \propto E^{0.5}$	$\frac{d\log(\ln(I))}{d\log(E)} \propto 0.5$
Variable-range hopping (VRH)	$I = I_0 \exp(\frac{CE}{2k_B T}(\frac{T_0}{T})^{\frac{1}{4}})$	$\ln(I) \propto E$	$\frac{d\log(\ln(I))}{d\log(E)} \propto 1$
Surface Leakage	$I \propto E/\rho$	$I \propto E$	$\frac{d\log(I)}{d\log(E)} \propto 1$
Space-charge limited	$I = \frac{9\varepsilon\mu E^n}{8W_d^3}$	$I \propto E^n \ (n \geq 2)$	$\frac{d\log(I)}{d\log(E)} \propto n$

To identify the bulk leakage mechanism, correlation between leakage current I and electric field were studied. The average electric field in the drift layer, E_{av}, was estimated by the equation $E_{av} = (V_{bi} - V_r)/W_d$, where V_{bi} is the built-in voltage of GaN diodes (~3.4 V) and W_d is the drift layer thickness [46]. As shown in Figure 3-4, a linear relationship of $\ln(I) \propto E_{av}$ was found valid for all the GaN vertical diodes, independently of the substrate, that we fabricated and also the ones reported in the literature [8][38][47].

It should be noted that for the plotted leakage current of vertical GaN pn diodes, the reported Avogy's GaN-on-GaN wafer has a 2-3 orders of magnitude lower dislocation density and leakage current probably due to different wafer growth technology. As shown in Figure 3-5, the $\ln(I) \propto E_{av}$ linear relationship is valid at various temperatures for the fabricated and reported devices. Referring to Table 3-3, this $\ln(I) \propto E_{av}$ linearity indicates that the variable-range hopping (VRH) is the dominant leakage mechanisms for GaN vertical diodes.
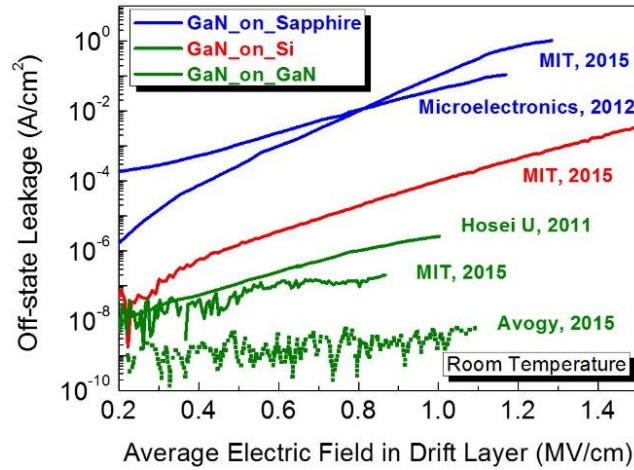
Figure 3-4 The ln (*I*) *v.s. E* characteristics for the GaN-on-GaN, GaN-on-sapphire and GaN-on-Si vertical diodes fabricated at MIT and reported in the literature.
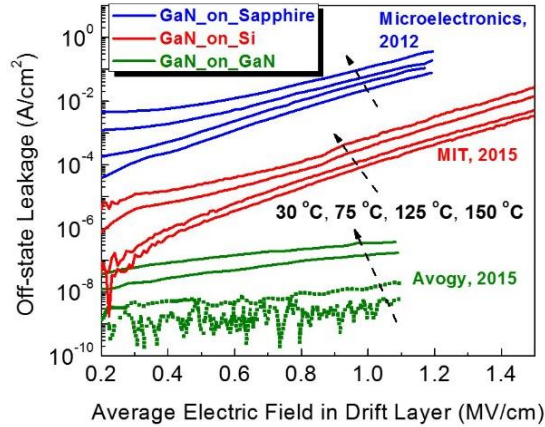
Figure 3-5 The ln (*I*) *v.s. E* characteristics at different temperatures for the GaN-on-GaN, GaN-on-sapphire and GaN-on-Si vertical diodes fabricated at MIT or reported in the literature.

As illustrated in Table 3-3, the differential slopes extracted from the *I~E* characteristics could also assist in identifying the leakage mechanism. As shown in Figure 3-6, the extracted $dlog(\ln(I))/dlog(E)$ has a value around 1.0 in our fabricated GaN-on-Si and GaN-on-sapphire vertical diode. This further confirmed that the VRH is the dominant leakage mechanism. (The GaN-on-GaN *I-V* was too noisy for this derivation, as the leakage is as low as our measurements limits.)
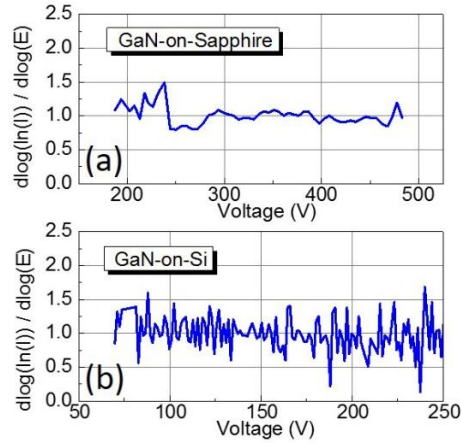
Figure 3-6 d*log*(ln (*I*))/d*log* (*E*) *vs voltage* calculated from *I-V* characteristics of fabricated GaN-on-Si
and GaN-on-sapphire vertical diodes.

3.4 TCAD Simulation of Leakage Current

To build a more precise model for the leakage current in vertical GaN pn diodes on different substrates, we collaborated with Synopsys to conduct TCAD simulation by utilizing the Sentaurus[TM] Device Simulator. TCAD simulations incorporating various leakage mechanisms, namely VRH through threading dislocation (TD), P-F transport and Trap-Assisted Band-to-Band Tunneling (TA-BTBT), were conducted by our collaborators in Synopsys to compare with experimental results. The diagrams illustrating the three models are shown in Figures 3-7 and 3-8.
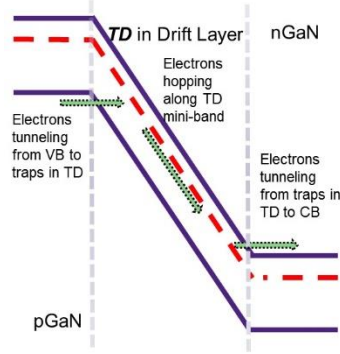
Figure 3-7 Diagram illustrating the concept of VRH and how it is implemented in TCAD simulation.
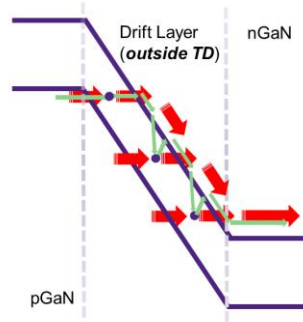
Figure 3-8 Diagram illustrating the concepts of P-F transport (Green thin arrows) and TA-BTBT (Red thick arrows). Both mechanisms are mediated by deep level traps in the band gap.

Cylindrical coordinate system was used in the TCAD simulations (therefore the simulation is essentially 3D) to match the forward current and turn-on voltage. A good agreement has been achieved between the simulated and experimental forward characteristics for vertical GaN pn diodes on sapphire, Si and GaN substrates. Figure 3-9 shows a representative comparison between simulated and experimental data for vertical GaN-on-Si pn diodes.
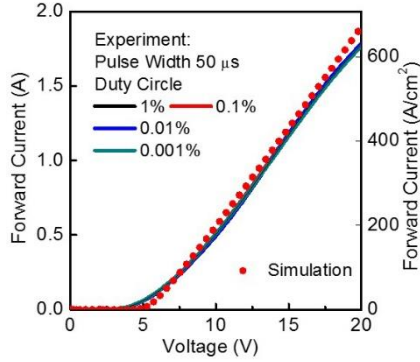
Figure 3-9 The comparison between simulations and experiments shows that the simulation is well-calibrated by experimental on-state forward current (w/ different pulsed modes) for GaN-on-Si vertical diodes.

TD is modeled as a cylindrical line at the center of the structure with an area proportional to the density of TD, from p-GaN/drift-layer interface to drift-layer/n-GaN interface. It is assumed that conduction along the TD is due to carrier hopping between dislocation traps in the "dislocation mini-band" under the VRH framework and is modeled using Gaussian disorder model drift mobility [48] with $\mu=v_0 b/(2F)exp(-(\sigma/kT)^2)[exp(qbF/kT)-1]$, where v_0 (hopping frequency) $= 10^{11}$/s, b (average trap to trap distance) =1.1 nm, σ (energy sigma)=80 meV and F is the electric field. The "dislocation mini-band" is assumed to be coupled perfectly to p-GaN valence band (VB) and n-GaN conduction band (CB) through tunneling but decoupled from VB and CB in the drift layer. Figure 3-10 shows that by assuming the leakage being dominated by VRH along TD and the pure screw dislocation density $\sim 3 \times 10^7$cm^{-2}, the TCAD simulation results match experimental results well with similar field and temperature dependency.

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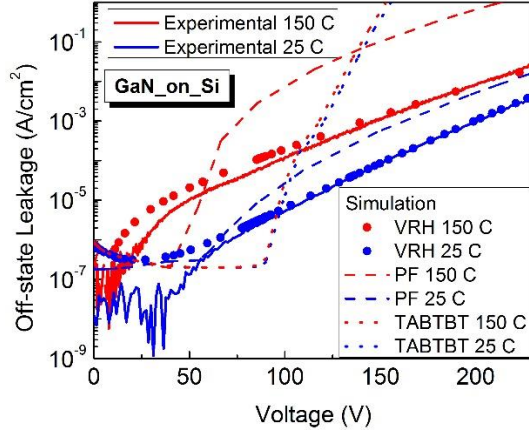
Figure 3-10 Experimental and simulated off-state leakage current of GaN-on-Si vertical diodes, at different temperatures. VRH model gives the best agreement with experiment among various leakage models.

Based on [49] (Chapter 2, page 56), the hopping frequency can be further formulated as $\nu_0 = \boldsymbol{\varGamma}_1 \exp(-2b(2mE_{\mathrm{trap}})^{0.5}/\hbar)$. By setting the attempt-to-escape frequency $\boldsymbol{\varGamma}_1 = 10^{13}$ s^{-1} as in [50] (Chapter 1, page 22), we obtained E_{trap} =1.35eV from the conduction band, which is close to the experimental values summarized in [51]. This consistence further confirms the validity of our TCAD simulation models.

It is also possible that the leakage is due to P-F transport or TA-BTBT in the bulk GaN drift layer (outside TD). However, simulation shows that the field and temperature dependencies are much stronger with P-F and much weaker with TA-BTBT, respectively, than the experimental results, as shown in Figure 3-10.

The VRH simulation model also works well when simulating the performance of the GaN-on-GaN vertical diodes fabricated at MIT or reported by Avogy [8]. As shown in Figure 3-11, good agreement is found over a wide range of temperatures, for a pure screw dislocation density of 6×10^4 cm^{-2} for Avogy's device and 2×10^6 cm^{-2} for MIT's device.

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The slight mismatch between simulation and Avogy's data is probably due to the incomplete information of Avogy's GaN-on-GaN wafers.
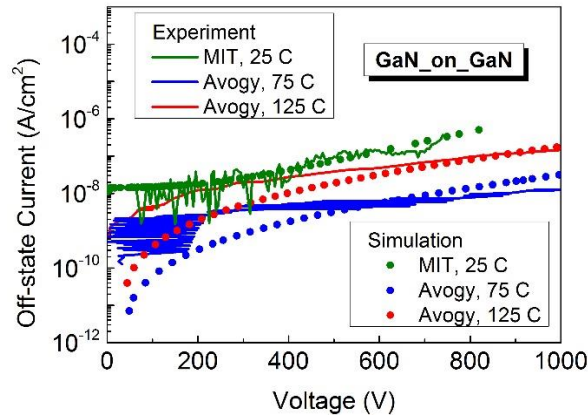
Figure 3-11 Experimental and simulated leakage current of GaN-on-GaN vertical diodes fabricated at MIT or reported by Avogy, at different temperatures.

3.5 Origin of Leakage Current in Defective Structures

After examining the vertical GaN pn diodes fabricated on multiple wafers and the diodes based on different fabrication processes, we found that the optimized material growth and fabrication process are essential to enable the VRH leakage in GaN vertical devices. In contrast, high-power etching process (e.g. the sidewall etching as discussed in Chapter 2) or unsuccessful growth may introduce large amount of defects in device structures. The leakage mechanism in the devices with non-optimized fabrication processes or growth conditions was also studied and compared to that of optimized devices. In these defective structures, trap-assisted space-charge-limited-current rather than VRH is typically the dominant leakage mechanism.
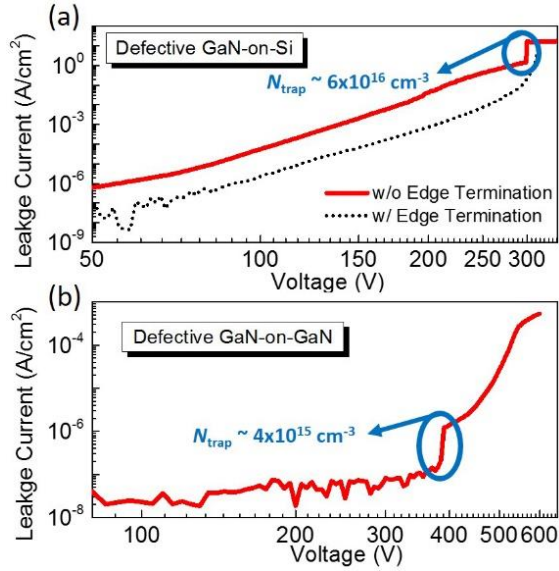
Figure 3-12 Reverse characteristics of (a) GaN-on-Si and (b) GaN-on-GaN vertical diodes in the samples with unsuccessful growth or non-optimized process, where the leakage is dominant by trap-assisted space-charge-limited conduction.

Figure 3-12 shows two examples for the trap-assisted SCLC behavior in defective structures. As shown in Figure 3-12 (a), the GaN-on-Si vertical diodes without advanced edge termination processes show a trap-assisted SCLC behavior while the diodes with optimized edge termination processes show a VRH behavior. This indicates that the traps located near the etching sidewalls determined the SCLC and breakdown behavior in the diodes without optimized processes. Figure 3-12 (b) shows a fully-vertical GaN-on-GaN vertical diode with defective epitaxial layers. The traps results in the current hump at a reverse bias of ~400 V. By utilizing the Equation (2-1), the average density of the trap contributing to the SCLC behavior can be estimated, as shown in Figure 3-12.

3.6 Summary of the Leakage Mechanisms in Vertical GaN Diodes
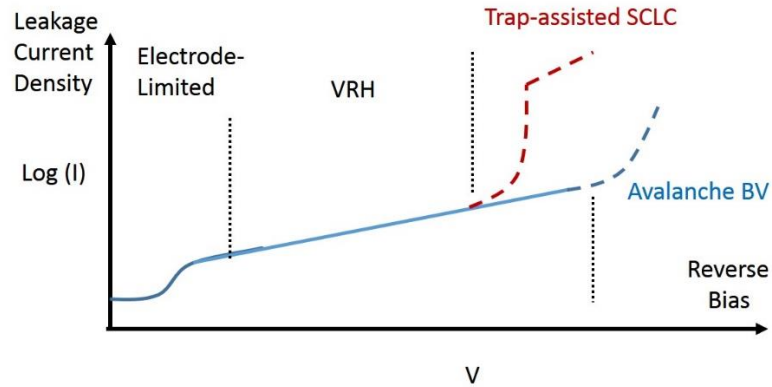
Figure 3-13 Diagram summarizing the typical leakage current behavior in a vertical GaN diode.

After investigating the leakage current mechanism in high-quality and defective vertical GaN devices, we can summarize a generalized leakage current behavior in vertical GaN devices, as shown in Figure 3-13. As mentioned in Section 3.3, the leakage current at low reverse biases is often influenced by the metal-semiconductor contacts, i.e. is electrode-limited. At higher reverse bias levels, in high-quality and well-optimized vertical diodes, the leakage current mechanism is dominant by VRH. If considerable trapping effects exist in the device, the leakage current mechanism is possibly dominant by trap-assisted SCLC, or a combination of SCLC and VRH. In an ideal leakage behavior, VRH leakage would extend until the onset of avalanche breakdown when the device peak electric field reaches the avalanche field of GaN. This ideal behavior has been demonstrated in state-of-the-art vertical GaN-on-GaN pn diodes [32]. However, if there are considerable traps in the device, the trap-assisted SCLC would turn on before the device peak electric field reaches the avalanche electric field of GaN. In this case, the trap-assisted SCLC will determine the device BV, i.e. the trap-filled-limited voltage (V_{TFL})

launching a current jump could be regarded as the device *BV*. This early termination of VRH by the turn-on of SCLC has been reported in many vertical GaN-on-Si diodes [18], [42].

It should be noted that both avalanche breakdown and trap-assisted SCLC are typically 'soft' breakdowns, i.e. non-destructive and repetitive breakdown behavior. A quite interesting work recently demonstrated that the breakdown induced by trap-assisted SCLC is very rugged [31]. This breakdown can survive the repetitive avalanche tests (multiple 50,000 breakdown events) at a frequency of 1 kHz, at a high current (0.73 A) and a peak bias (507 V) higher than the device V_{TFL} (420 V) [31]. These results indicated the rugged breakdown induced by the trap-assisted SCLC may be acceptable for the device applications in power circuits. However, compared to avalanche breakdown, this trap-assisted breakdown behavior is expected to limit the switching frequency due to the need for 'de-trapping' time after each breakdown behavior.

3.7 Design Space of Leakage Current of Vertical GaN Diodes

As illustrated in section 3.4, we have built and calibrated a TCAD simulation model based on VRH leakage mechanism, which well agrees with experimental data. We will use this simulation model to derive the design space of leakage current of vertical GaN diodes on different substrates and at different temperatures.

To derive the leakage current of vertical GaN diodes on different substrates, we simulated the off-state leakage current density I as a function of the total dislocation density N_d in GaN epi-layers at different E_{av} levels, as shown in Figure 3-14. As show in Figure 3-14, the dislocation density below 10^7 cm^{-2} represents the vertical GaN devices

fabricated on GaN substrates, while the dislocation density above 10^7 cm^{-2} represents the devices fabricated on sapphire and Si substrates. It should be noted that the dislocation density shown in Figure 3-14 is the total dislocation density in the epitaxial structure. We assume that 3% of the total dislocation density corresponds to pure screw dislocations, which are directly related to the off-state leakage current. As mentioned in section 3.2, this assumption was based on the percentage of pure screw dislocations typically reported for GaN epitaxial layers grown by MOCVD or MBE. From the simulation results, it can be seen that the dependence between leakage current and dislocation density roughly follows a power law. Thus, an empirical formula can then be derived for an estimation of the leakage current in GaN vertical power diodes at 30 $^{\circ}$C:

$$\ln[I(A/cm^2)] = \ln[N_d(cm^{-2})] + 4.86E_{av}(MV/cm) - 38.0 \qquad (3\text{-}1)$$

In Figure 3-14, the leakage of GaN vertical diodes was also benchmarked with AlGaN/GaN lateral diodes [52][53]. At least 2~3 orders of magnitude lower leakage is seen in GaN vertical diodes compared to lateral diodes with similar average internal electric field and dislocation density.
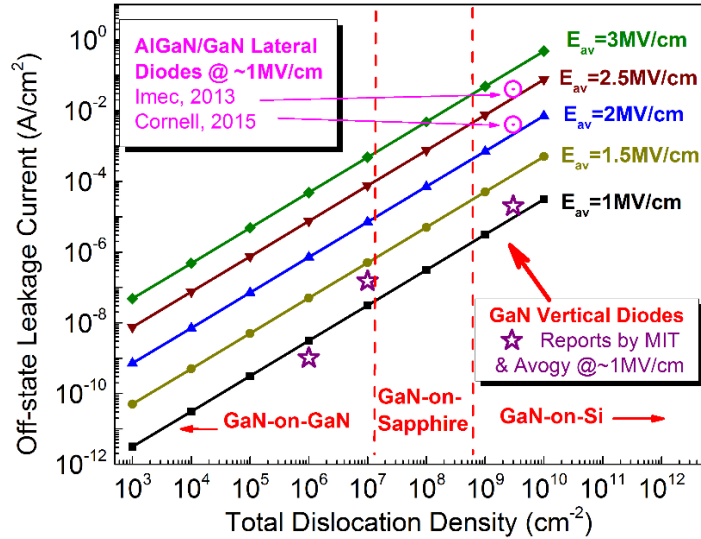
Figure 3-14 Design space of the off-state leakage current of GaN vertical diodes as a function of the total dislocation density level in the structure, and the average electric field in the drift layer (E_{av}=1~3 MV/cm). The different dislocation density represents GaN vertical diodes fabricated on different substrates

With the well-calibrated simulation model based on VRH, we can also derive the design space of leakage at elevated temperature. Off-state leakage current versus temperature was then simulated for GaN-on-GaN vertical diodes and GaN-on-Si vertical diodes, as shown in Figure 3-15. For GaN-on-GaN vertical diodes, we simulated the leakage current at an E_{av} of 2~3 MV/cm, with this E_{av} selected as a target for 600-5000 V applications. A total dislocation density of 2×10^6 cm^{-2} was used, to simulate the worst case of GaN-on-GaN structures (typically 10^4~10^6 cm^{-2}). For GaN-on-Si vertical diodes, we simulated the leakage current at an E_{av} of 2~2.5 MV/cm, with this E_{av} selected as a target for 200-1200 V applications. A total dislocation density of 10^9 cm^{-2} was used for GaN-on-Si structures. It should be noted that lower dislocation density of GaN-on-GaN and GaN-on-Si is experimentally available, which would further increase the outperformance of vertical GaN diodes.

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In Figure 3-15, we benchmarked the leakage performance of vertical GaN diodes with 600 V lateral GaN diodes [53], 600 V SiC diodes [54], 5000 V SiC diodes [55] and 1200 V Si thyristors [56]. In the extracted data of lateral GaN diodes, 5000 V SiC diodes and 1200 V Si thyristors, the leakage current density is normalized by the reported diode junction area. For the 600 V SiC diodes (Infineon 12A 600V SDT12S60), the leakage current density reported in [54] is normalized by the total packaged diode area, which indicates that the real leakage current density normalized by device junction area should be higher than the values shown in Figure 3-15. The average electric field was estimated by utilizing the voltage level and the reported drift region thickness in each devices.

As shown in Figure 3-15, vertical GaN diodes show promising capability for achieving low leakage current and sustaining high temperatures. Low-cost GaN-on-Si vertical diodes can achieve compatible leakage than commercial Si and SiC devices while sustaining 3-5 times higher electric field. This indicates for the same leakage current density level, vertical GaN-on-Si diodes can achieve at least 3 times higher *BV* than Si and SiC devices. GaN-on-GaN vertical diodes can achieve 2-4 orders of magnitude lower leakage while sustaining 5-10 times higher electric field. This shows the great potential of vertical GaN diodes for the applications in low power-loss and high-temperature power switching.
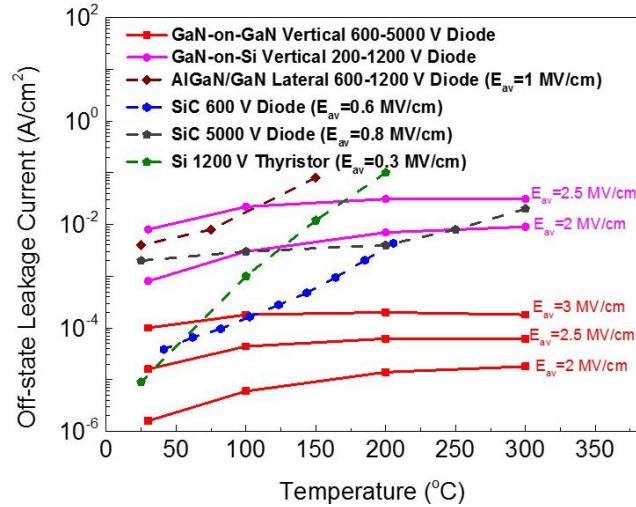
Figure 3-15 Off-state leakage current versus temperature of the designed GaN-on-GaN vertical diodes and GaN-on-Si vertical diodes, and the reported lateral GaN diodes, SiC 600 V and 5000 V diodes and Si 1200 V thyristors.

3.8 Conclusion and Prospect

In this chapter, we fabricated vertical GaN pn diodes on Si, sapphire and GaN substrates and investigated their leakage current mechanism by analytical study and TCAD simulation. From the investigation, we identified VRH through TD as the main off-state leakage mechanism for GaN vertical diodes on different substrates. For defective structures with non-optimized fabrication processes or epitaxial growth, trap-assisted SCLC may become the dominant leakage mechanism and even determine the device *BV*. With a well-calibrated TCAD simulation based VRH leakage mechanism, we derived the design space of leakage current in vertical GaN diodes, as a function of dislocation density and temperature. We demonstrated that the designed GaN vertical diodes can offer 2-4 orders of magnitude lower leakage while supporting 3-5 times higher

electric field than GaN lateral, Si and SiC devices. This demonstrates great potential of GaN vertical devices for high-voltage and low-power-loss applications.

To obtain a more complete understanding into the leakage and breakdown mechanism of vertical GaN devices, future work is needed in the following three aspects:

(a) Microscopic characterization and understanding on the dislocation- or trap-assisted leakage current formation and dynamics.

(b) Understanding the breakdown mechanism, in particular the essential conditions and determining factors for the avalanche breakdown.

(c) Additional investigation into the ruggedness and reliability of the breakdown induced by trap-assisted SCLC, and understanding the trade-off between the trap-assisted breakdown and the avalanche breakdown.

Chapter 4 Advanced Vertical GaN Schottky Diodes

4.1 Introduction

As discussed in Chapter 2 and Chapter 3, low leakage current and high BV have been demonstrated in vertical GaN pn diodes. Despite the high BV and low leakage of GaN pn diodes, the pn diodes have a large turn-on voltage (V_{on}>3 V) due to the large bandgap of GaN. This large turn-on voltage induces large conduction loss in power switching applications. Besides, as the conduction of pn diodes involve minority carrier, the switching frequency of pn diodes is limited by the minority carrier lifetime. GaN vertical Schottky barrier diodes (SBDs) are therefore desired, due to their low V_{on} and fast switching. However, SBDs typically suffer from large reverse leakage current due to Schottky barrier lowering at high bias.

Currently, all the reported vertical GaN SBDs have a BV below 1200 V. One of the earliest high-voltage GaN Schottky rectifiers was reported by University of Florida, with a BV of 550 V, an R_{on} of 6 m$\Omega \cdot$cm^2 and a V_{on} of 3.5 V [7]. Auburn University and Kyma Technologies reported the improved performance in 2006 [57] and 2011[58], demonstrating a BV of 600 V, an R_{on} of 1.3 m$\Omega \cdot$cm^2 and a V_{on} of 0.8 V [58]. In 2010, Sumitomo reduced the drift region carrier concentration to below 10^{16} cm^{-3}, and demonstrated a BV of 1100 V and an R_{on} of 0.71 m$\Omega \cdot$cm^2 [11]. This is still the record performance for vertical GaN Schottky rectifiers. In 2015, TOYODA GOSEI demonstrated a large vertical GaN Schottky rectifier with a forward current of 50 A and a blocking voltage of 790 V [59]. In 2016, HRL demonstrated the leakage current of vertical Schottky diodes can be reduced by [C] doping in the drift region [10].

From the above literature data, it can be seen that the *BV* and leakage current of vertical GaN Schottky rectifiers is far inferior to the ones in vertical GaN pn rectifiers. To suppress the leakage and increase the *BV*, [C] doping can be used to lower the net carrier concentration (N_D-N_A) in the GaN drift layers to ~10^{15} cm^{-3} [10], [60]. However, the [C] doping exhibits complicated roles (a combination of donor and acceptor) in the drift region [60], increases the difficulty of the epitaxial growth and degrades the SBD forward characteristics [10]. In addition, the [C] doping cannot address other issues (e.g. reliability) induced by the high electric field at the surface Schottky contacts.

As an alternative, advanced device structures for leakage reduction are therefore desired for GaN vertical SBD, while there has been no report for advanced vertical GaN Schottky rectifiers so far. When revisiting the Si and SiC power devices, two advanced vertical GaN Schottky rectifiers have been successfully demonstrated and extensively studied. Figure 4-1 shows the schematic of a SiC junction barrier Schottky (JBS) rectifiers [61]. The JBS rectifier consists of a grid of implanted p-wells in the n$^-$-type drift layer, sitting just beneath the Schottky contact. Under reverse bias, the p-n junctions move the peak electrical field from the surface into bulk material, resulting in lower leakage and higher *BV*. Under forward bias, the p-wells are inactive and the V_{on} is determined by the Schottky barrier. Cree has demonstrated high-performance 4H-SiC JBS rectifiers up to 10-kV class [61], which have achieved important commercialization success.
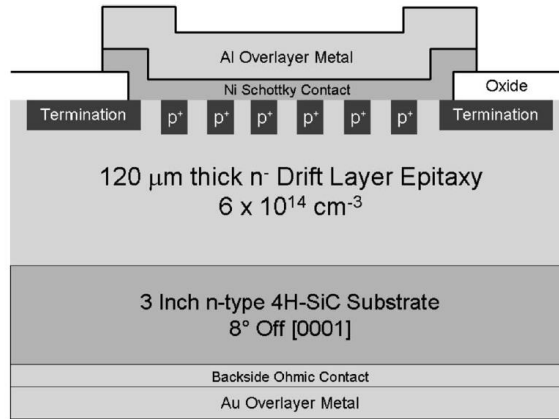
Figure 4-1 Schematic of Cree's SiC Junction Barrier Schottky Rectifiers.

The demonstration of JBS rectifier requires the formation of pn junctions on patterned surfaces. However, as mentioned in Chapter 1, GaN still lacks a selective area doping or selective area epitaxial regrowth process that yields high-quality p-n junction on patterned GaN surfaces. Most of the current approaches, laterally patterned ion implantation and activation or selective area diffusion of p-type dopants (e.g. Mg, Be, Zn) have not produced p-type regions or good-quality (i.e. equivalent to as-grown) p-n junctions. This issue has made it difficult to demonstrate vertical GaN JBS rectifiers. In Chapter 5, we will present some of our preliminary work on developing high-quality p-n junctions on patterned GaN surfaces.

The other successful advanced Schottky barrier rectifier demonstrated in Si and SiC is the trench MOS/MIS barrier Schottky (TMBS) rectifier. The TMBS rectifier consists of multiple trenches and a MIS/MOS structure built into the trench bottoms and sidewalls. Under reverse bias, the depletion effect of MOS/MIS structure moves the peak electrical field from the surface Schottky contact into bulk material, resulting in lower leakage and higher BV. Under forward bias, the V_{on} is determined by the surface Schottky barrier. The

Si TMBS rectifier has been successfully commercialized for 200-V class applications [62]. High-performance SiC TMBS rectifier has also been successfully demonstrated for 600-V class applications [63].
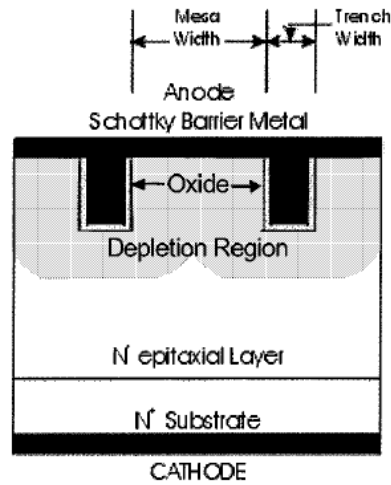
Figure 4-2 Schematic of a fully planarized 4H-SiC trench MOS barrier Schottky rectifier.

Compared to JBS rectifiers, the demonstration of GaN TMBS rectifier does not need selective p-type doping. Although this makes it much more feasible to demonstrate GaN TMBS rectifier, novel fabrication process (e.g. trench formation and corner rounding) and novel structures (e.g. field rings) are needed to enable the electric field management within the TMBS structure. In this Chapter 4, we demonstrate the first GaN TMBS rectifier by combining the TMBS structure and implanted field rings [20]. Novel fabrication process in trench formation and corner rounding was also demonstrated for GaN for the first time. The novel structure enabled a $>10^4\times$ lower leakage current. Improved *BV*, excellent forward characteristics, high-temperature operation and fast switching behavior were also demonstrated.

4.2 Device Design and Simulation

The schematic structure of the developed GaN vertical trench MIS barrier Schotttky rectifier with implanted trench rings (FR-TMBS) is shown in Figure 4-3. A 7 μm-thick n-GaN layer with a N_D-N_A of 2×10^{16} cm^{-3} was grown by MOCVD on free-standing GaN substrates. The device consists of multiple trenches with a depth of 2 μm and a MIS structure built into the trench bottoms and sidewalls. Implanted FRs are below the trench bottom, and the Schottky contact is formed on the top GaN surface. The implanted edge termination was fabricated with the same method to form implanted field rings. Ohmic contact was formed below the ~300 μm thick n$^+$-GaN substrate.
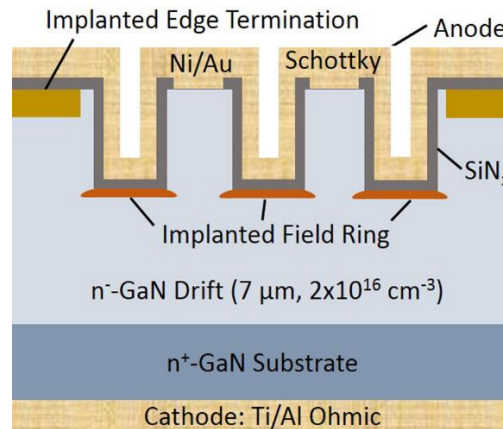
Figure 4-3 Schematic of the developed GaN vertical trench MIS barrier Schotttky rectifier with implanted trench rings (FR-TMBS).

The electric field distribution in a device unit-cell was simulated by *Silvaco Atlas* based on the similar simulation models developed in our previous works [4][28] (also described in Section 2.4). Figure 4-4 shows the simulated electric field distribution in a device unit-cell when the device is at a bias of -1000 V. The electric field distribution

along the vertical cutline in the middle of the GaN mesa is shown in Figure 4-5. As shown in Figure 4-4 and 4-5, four electric field modulation effects can be seen in our designed device:

a) The electric field at the Schottky interface was greatly reduced from 3 MV/cm in conventional Schottky barrier diodes (SBDs) to ~1 MV/cm in our FR-TMBS diodes. This surface electric field reduction would cause an exponential decrease in the leakage current from Schottky contact;

b) The TMBS structure lowers the surface electric field at a cost of creating electric field crowding in the dielectrics near the trench corners, as shown in Figure 4-4 (a). The FRs are effective in smoothing this E-field stress, as shown in Figure 4-5. Here we assume the implanted field ring regions are almost insulated (with extremely low carrier mobility) with deep acceptor traps, such to simulate the Ar implantation into GaN [27].

c) With the TMBS and FR structures, the peak electric field location moves from the upper Schottky surface into the bulk GaN (in the implanted regions below the trench bottom).

d) By comparing the Figure 4-4 (b) and (c) and the extracted electric field along the cutline shown in Figure 4-5, it can be seen that the electric field modulation sees a dependence on mesa width (w_M): a smaller w_M enables a stronger electric field shielding of the Schottky junction and a lower electric field near the FR region
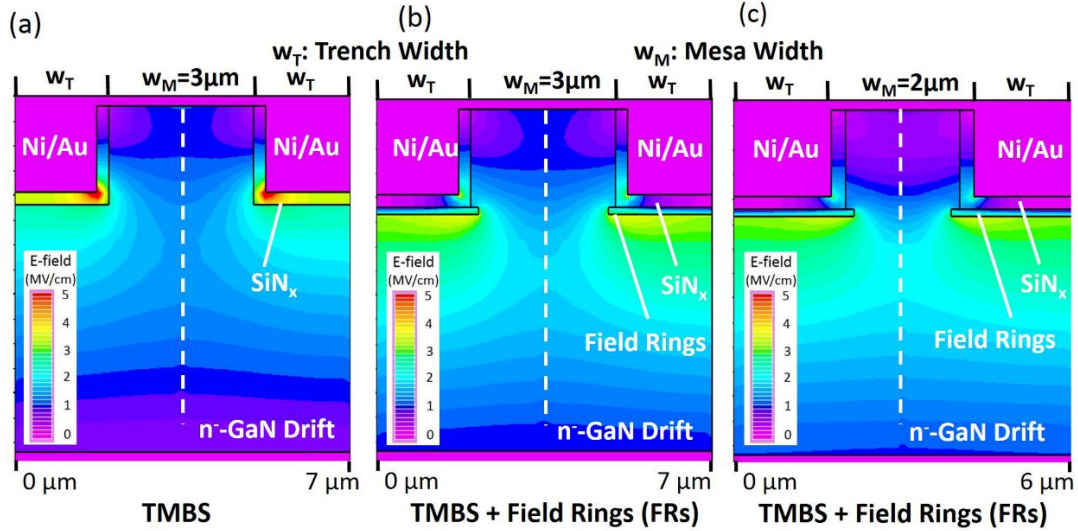
Figure 4-4 Electric field distribution in a device unit-cell at a revers bias of -1000 V by TCAD simulation, for (a) TMBS with a mesa width (w_M) of 3 μm, (b) FR-TMBS with w_M =3 μm and (c) FR-TMBS with w_M =2 μm.
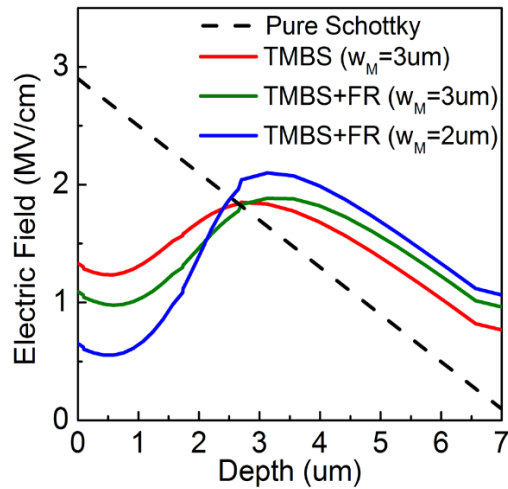
Figure 4-5 Electric field profile along the cutline shown in Figure 4-4 for TMBS, FR-TMBS with w_M =3 μm and 2 μm, in comparison with the electric field for a pure GaN SBD at a reverse bias of 1000 V.

In the TMBS design, there is a fundamental trade-off between MIS depletion and trench corner/bottom regarding electric filed management. To enhance the depletion

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effect of the trench MIS structure and lower the electric field at surface Schottky contacts, high-k dielectrics, thin dielectrics and deep trenches are desired. However, the thin dielectrics and deep trenches will increase the electric field strength in dielectrics and at dielectrics/semiconductor interface near the trench corners and bottoms. This electric field crowding will increase the risk for early breakdown at the trench corners and bottoms. To derive the optimized trench depths, dielectrics materials and dielectrics thickness, TCAD simulation was performed monitoring the peak electric field at dielectrics corner and surface Schottky contact. As shown in Table 4-1, when thick and low-k dielectrics was used, the electric field modulation effect of the TMBS structure is very weak. However, when thin dielectrics and deep trench were used, the peak electric field at dielectrics corner is quite large. Based on this electric field trade-off, we selected the 0.2~0.25 μm SiN_x as dielectrics and a trench depth of ~2 μm.

Table 4-1 Simulated peak electric field at a reverse bias of 1000 V, for the TMBS structures with different trench depths, dielectrics material and dielectrics thickness.

Optimization Parameters	Trench depth (μm)	Diel. Thickness (um)	Diel. Type	E_{peak} @ Diel. Corner (MV/cm)	E_{peak} @ Schottky (MV/cm)
Diel. Type and Thick-ness	2	0.2	SiN_x	3.3	1.2
	2	1	SiN_x	3	2.6
	2	0.2	SiO_2	5	1.6
	2	1	SiO_2	4	3
Trench Depth	1.2	0.2	SiN_x	3	2
	3	0.2	SiN_x	3.8	0.8

Diel.: Dielectrics; E_{peak}: peak electric field;

4.3 Device Fabrication

4.3.1 Cap Layer Removal

The GaN-on-GaN wafer used in this work was originally designed to fabricate vertical fin MOSFETs [15] rather than vertical SBDs. In the wafer structure, there is an additional 300 nm n^+-GaN layer on top of the 7 μm-thick n^--GaN layer and free-standing GaN substrates. Thus, the first step of fabrication is the removal of n^+-GaN cap layer. For vertical SBDs, as the leakage current under high electric fields is quite sensitive to surface roughness [15], it is important to recover all the dry-etching-induced damages and surface roughness on the n^--GaN surface.

The dry etching was performed in an Electron Cyclotron Resonance (ECR)-RIE system by using the Cl_2/BCl_3 gases. The dry etching consists of two steps. In the first step, an etching recipe with RF power of 25 W and etching rate of 15 nm/min was used for 30 minutes. In the second step, another etching recipe with RF power of 10 W and etching rate of ~3 nm/min was used for 30 minutes. The latter etching recipe with smaller RF power and lower etching rate was designed to reduce the etching-induced surface roughness created in the first high-power etching. The ~250 nm over-etch into n^--GaN could guarantee the complete removal of n^+-GaN layer and the top n^--GaN layer with a doping tail of the high Si concentration.

After the dry etching, additional processes are needed to remove the etching-induced surface damages. Various methods have been reported to be able to remove the dry-etching-damages in GaN, including a 700-750 C annealing [64], [65], [66], boiling (~200 C) KOH wet etching [67][68] and KOH treatment under UV environment [69]. In this work, we mainly considered the approaches at relative low temperature (i.e. much lower

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than the epitaxial growth temperature at 800-1000 ^{o}C), including the hot KOH treatment and TMAH treatment (as demonstrated in section 2.3, the TMAH could remove the surface roughness in etching sidewalls).
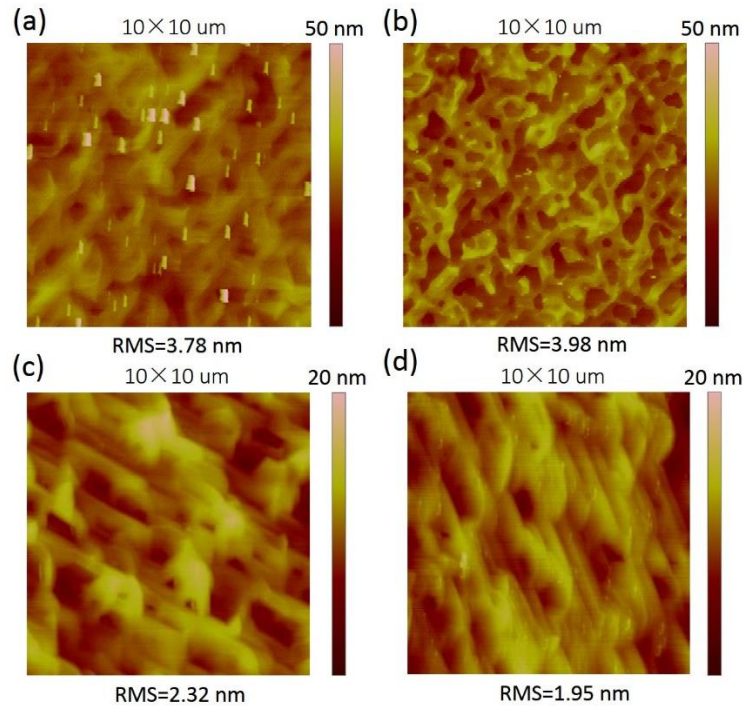
Figure 4-6 Atomic force microscopy images for GaN surface (a) after dry-etching and after (b) an additional boiling KOH treatment for 15 minutes, (c) hot TMAH treatment for 1 hour and (d) hot TMAH treatment for 1 hour and 45 minutes.

Figure 4-6 (a) shows the atomic force microscopy (AFM) image of GaN surface right after dry etching. As shown, the surface is very rough with high density of etching residues (small 'hills' with a height of 10-100 nm). Figure 4-6 (b) shows the AFM image of the GaN sample after a post-dry-etching treatment in 40% boiling KOH (~200 ^{o}C) for 15 minutes. As shown, the dry-etching residues have been completely removed; however, the surface roughness slightly increases and many dislocations/defects expands to

hexagonal pits. Figure 4-6 (c) shows the AFM image of the GaN sample after a post-dry-etching treatment in 25% TMAH at 85 ^{o}C for 1 hour. As shown, the dry-etching residues have been completely removed and the surface roughness was greatly reduced. Figure 4-6 (d) shows the AFM image of the GaN sample after a post-dry-etching treatment in 25% TMAH at 85 ^{o}C for 1 hour and 45 minutes. As shown, with the longer TMAH treatment time, the overall surface treatment further reduces. However, some small 'hills' with a height of 10-20 nm appears on the surface morphology. This is probably due to the slight different etching rates of TMAH on different polarity of GaN (e.g. m-plane and a-plane) [15].

From the studies above, we finally utilized the treatment in 25% TMAH at 85 ^{o}C for 1 hour for all GaN-on-GaN samples after the two-step dry etching processes.

4.3.2 Trench Formation and Corner Rounding

4.3.2.1 Overview

Trench formation and corner rounding are not only the core fabrication process to fabricate vertical GaN TMBS rectifiers, but also the key processes to demonstrate high-voltage trench-based vertical GaN transistors. Figure 4-7 presents the simplified schematics of four trench-based vertical GaN devices. Figure 4-7 (a) shows the vertical GaN TMBS rectifier that we are working on in this work. Figure 4-7 (b) shows the trench fin MOSFETs, which have sub-micron GaN fins with all-around gates, and achieved normally-off operation without the need for p-GaN [15]. Figure 4-7 (c) shows the vertical trench MOSFETs [26][70][71] which combined the trench structure with MOS channel.

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Figure 4-7 (d) shows a trench current aperture vertical electron transistors (CAVETs) [13], [72] which combined the trench structure with 2DEG channels.
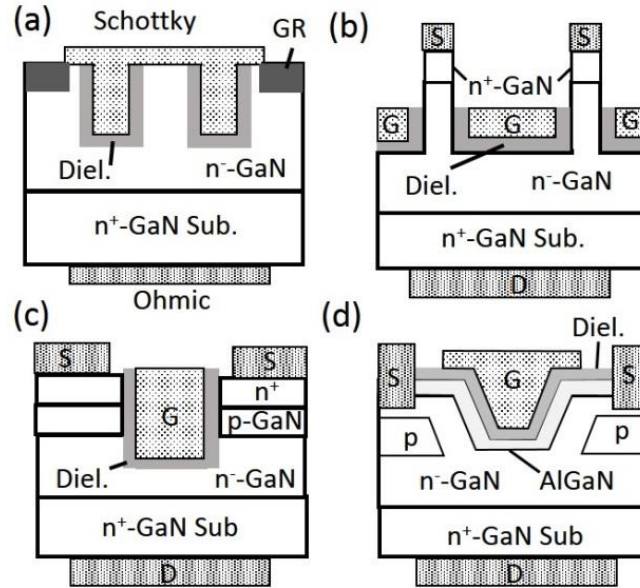
Figure 4-7 Simplified schematics for (a) GaN trench MIS barrier Schottky rectifiers, (b) GaN fin MOSFETs, (c) GaN trench MOSFETs, and (d) GaN trench CAVETs. (GR represents guard ring and Diel. represents dielectrics).

Trench formation and corner rounding are the key technologies to demonstrate these high-voltage trench-based vertical GaN devices. As the device peak electric field is typically located near the trench corners or bottoms, the trench shape and bottom morphology are determining factors for device *BV*. On the other hand, due to the relatively high bond energy (8.92 eV/atom) of GaN, high ion energy is typically required in the dry etching for deep trenches, resulting in rough surfaces and sharp corners in the trench. To prevent surface leakage and electric field crowding, the sidewall smoothening and corner rounding are essential [73][74]. The conventional corner rounding process

technology for Si and SiC devices typically requires high temperature (over 1000 ^{o}C) annealing [73][74] which would deteriorate GaN material quality and device performance. Therefore, the optimization of trench shapes and the development of a damage-free corner rounding process are greatly needed for vertical GaN power devices.

In this section 4.3.2, we developed a novel corner rounding process by utilizing the TMAH wet etching and piranha clean. By varying different dry etching conditions with the corner rounding technology, we demonstrated different bottom morphologies in rounded GaN trenches. TCAD simulations were performed to reveal the impact of these trench shapes on device *BV* and electric field distributions. From the simulation, we selected the rounded flat-bottom trench as an optimized structure for the following fabrication of TMBS rectifier.

4.3.2.2 Corner Rounding and Trench Formation

The trench structures were formed in an inductively coupled plasma (ICP) etching system at an ICP power of 150 W, a bias power of 30-75 W, a chamber temperature of 40 ^{o}C and pressure of 0.6 Pa. Cl_2/BCl_3 gas combination was used for the ICP etching with a flow rate of 20 sccm for Cl_2 and different rates (5-20 sccm) for BCl_3. The etching utilized 50 nm Ni as hard masks. Compared with conventional oxide masks, the use of a metal hard mask allows for a much smoother etch sidewall, due to the lack of oxide edge erosion under high ion energies [17]. The width and depth of the trenches were both around 2 μm.

TMAH wet etching (25% concentration) at 85 ^{o}C for 70 min with a following piranha clean for 10 min was found effective in removing the etch damage and rounding

the trench corners. Figure 4-8 (a)-(c) shows the cross-sectional SEM images of the trench structure right after dry etching [Figure 4-8 (a)], with a following TMAH wet etching [Figure 4-8 (b)], and with an additional piranha clean [Figure 4-8 (c)]. The trench right after the dry etching shows rough surfaces with the sidewall tapered angle being around 70°. As demonstrated in section 2.3, due to its anisotropic etching, TMAH preferentially etches the side slopes and therefore eliminate the surface damage caused by the dry etching. As shown in Figure 4-8 (b) and 4-8 (c), the Ni mask residues produced during the dry etching and TMAH treatment can be effectively removed by piranha clean. A simple ultrasonic clean in acetone was unable to remove these residues. The final rounded trench shows smooth vertical sidewalls and flat bottom, with a corner rounding radius of about 200 nm. It should be also noted that in the formation of sub-micron trenches, we found that the trench structures aligned along the [1120] direction have smoother surface than those in the [1100] direction [15]. However, this orientation dependence of sidewall smoothness is not significant in the formation of micron-sized trenches.

(a) Cl$_2$: 20 sccm; BCl$_3$: 5 sccm; Bias power: 75 W

(b) TMAH 70 min

(c) TMAH 70 min + Piranha 10 min

(d) Cl$_2$: 20 sccm; BCl$_3$: 15 sccm; Bias power: 30 W

(e) TMAH 70 min

(f) TMAH 70 min + Piranha 10 min
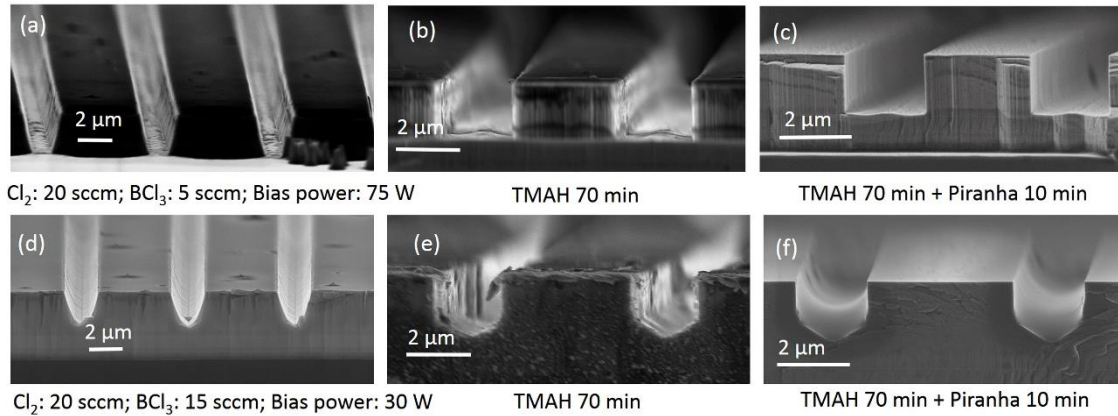
Figure 4-8 Cross-sectional SEM images of the trench structures right after dry etching, with a following TMAH wet etching, and with an additional piranha clean, for two different conditions of initial dry etching.

The trench bottom morphology can be controlled by the dry etching conditions. A less anisotropic dry etching could enhance the lateral etching, reduce the tapered angle of dry etching sidewalls, and produce a tapered trench bottom after the TMAH wet etching. In the Cl$_2$/BCl$_3$ based ICP etching, the less anisotropic etching can be realized by either reducing the bias power or increasing the BCl$_3$/Cl$_2$ ratio [75]. As shown in Figure 4-8 (d)-(f), the dry etching with lower bias power and higher BCl$_3$ flow rate produced a pointed trench bottom; the following TMAH and piranha clean converted the pointed bottom into a tapered bottom (tapered angle ~ 30°) with a rounded bottom corner.

Figure 4-9 summarizes the rounded trench shapes corresponding to different dry etching conditions, i.e. various bias powers and BCl$_3$/Cl$_2$ ratios. From Figure 4-9 (a)-(c), it can be shown that for a high bias power, the rounded trench shape is not sensitive to the BCl$_3$/Cl$_2$ ratio, having flat bottoms for different gas ratios. In contrast, for low bias power, as Figure 4-9 (d)-(f) show, the increase in BCl$_3$/Cl$_2$ ratio could gradually expand the

corner regions and the tapered slopes (tapered angle $\sim 30^{\circ}$), and finally change the flat bottom into a tapered one in the rounded trenches.
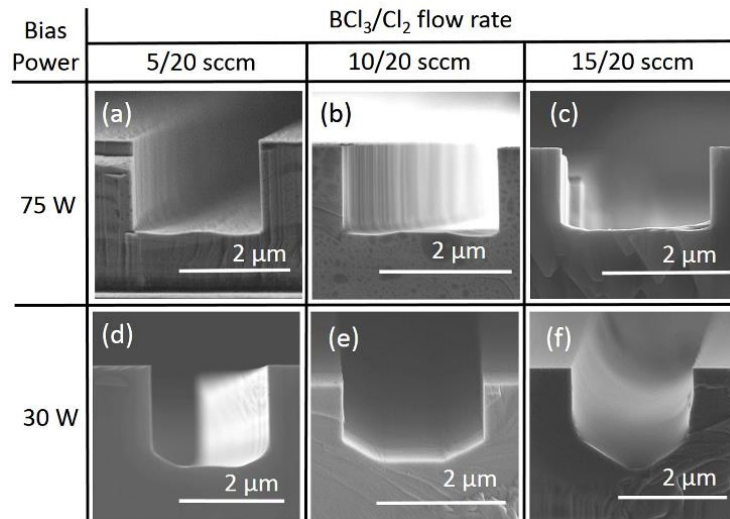
Figure 4-9 Cross-sectional SEM images of the rounded trench structures corresponding to six different conditions of initial dry etching, with various bias power and different BCl_3/Cl_2 flow rate. All the trenches have been rounded by TMAH treatment and piranha clean. All the trenches have a width of 2 μm and a depth of 1~2 μm.

4.3.2.3 TCAD Simulation for Trench Shape Optimization

To study the blocking capability of rounded trenches with different shapes, two-dimensional electric field distribution was simulated for a trench-based device unit-cell using the Silvaco ATLAS simulator. The simulation models are identical the ones described in section 4.2.

The difficulties of the TCAD simulation for trench structures with rounded corners lie in the structure definition and meshing. If the rounded-corner regions are not well defined with fine meshing, it is extremely difficult to reach convergence in electric field simulation. In this work, the structure and meshing were defined in the DEVEDIT

module, and then input into DECBUILD module for the definition of carrier transport models, material and electrode properties. Figure 4-10 (a) and (b) shows the structure definition and meshing for a rounded trench structure in DEVEDIT. As shown, even in areas with the same material, the rounded corner region needs to be defined and meshed separately from the main rectangular regions. This separate and region-to-region meshing could make the simulation much easier to converge. Figure 4-10 (c) and (d) shows the similar structure and meshing definition for another rounded trench structure.
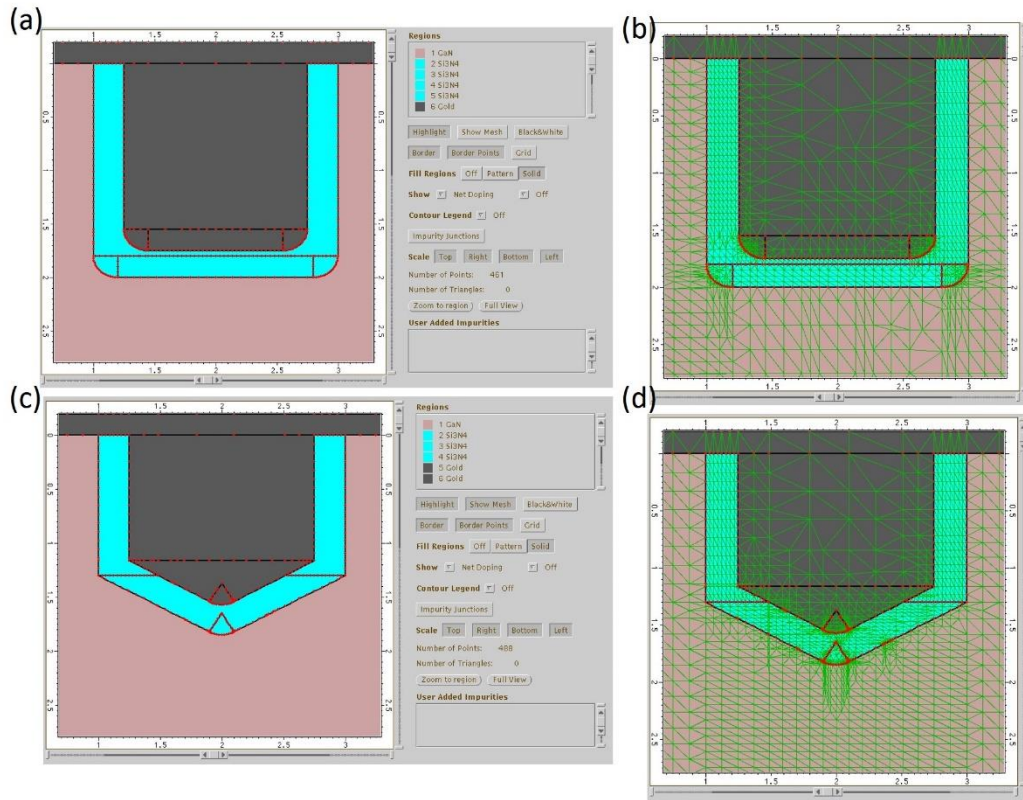
Figure 4-10 Structure definition and meshing for the trench structures with rounded corner in the DEVEDIT module of Silvaco Atlas.

In the simulation for TMBS diodes, the unit-cell consists of a 7 μm n$^-$-GaN (Si: 2×10^{16} cm^{-3}), an n$^+$-GaN substrate, and a 250 nm SiN$_x$ covering the GaN trench. Although the simulated unit cell has only a top and a bottom electrode, the simulated electric field distribution at a high reverse bias also applies to the trench-based normally-off transistors, when they are in the off-state with a zero gate bias and large reverse drain biases. In the unit-cell, three representative trench shapes were simulated: a non-rounded trench [corresponding to Figure 4-8 (a)], a rounded trench with a flat bottom [corresponding to Figure 4-8 (c)] and a rounded trench with a tapered bottom [corresponding to Figure 4-8 (f)], where the rounding radius of all rounded corners was set as 200 nm and the trench depth was set as 2 μm. For simplicity's sake, the trench shapes shown in Figure 4-9 (d) and (e) were not simulated, as they can be regarded as transitional structures between the flat-bottom and tapered-bottom structures. Also, they have more corners than the flat-bottom or tapered-bottom trenches, which would increase the risk of electric field crowding and early breakdown.

Figure 4-11 shows the simulated electric field distribution at a high reverse bias for the three representative trenches. The non-rounded trench shows the highest peak electric fields in GaN and dielectrics located around the sharp corners, while the rounded trench with a flat bottom shows the lowest peak electric fields. The rounded trench with a tapered bottom has an electric field crowding at the bottom rounded corner, indicating an inferior blocking capability to the rounded trench with a flat bottom.
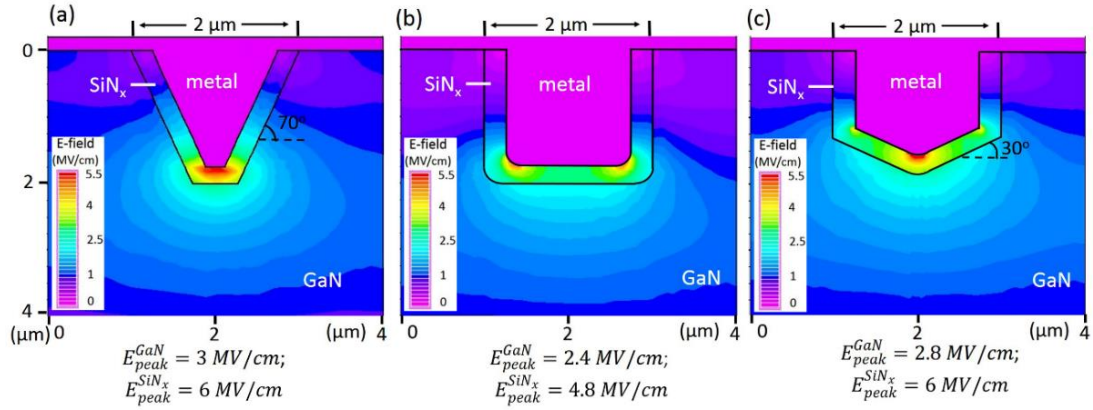
Figure 4-11 Simulated electric field distribution in the top part of a device unit-cell (the bottom electrode, n$^+$-GaN substrate and a part of n$^-$-GaN are not shown), at a reverse bias of 600 V, for three different trench shapes: (a) non-rounded trench, (b) rounded trench with a flat bottom and (c) rounded trench with a tapered bottom.

This simulation results were verified by experimental results. Before fabricating the devices incorporating field rings, TMBS rectifiers with the three representative trench shapes were fabricated. The device without the corner rounding process shows high leakage current and an early breakdown at -150 V, due to the sharp corners and surface damage within the trenches. The device with rounded flat-bottom trenches show the lowest leakage current and highest *BV* (~500 V) among the three trench structures, which agrees well with the simulation results. From the simulation and experimental results, we chose the rounded trench with flat bottoms as the optimized trench structures in the fabrication of the TMBS rectifiers with field rings.

4.3.3 Field Ring, Dielectrics and Electrode Formation

Figure 4-12 shows the main steps to fabricate the vertical GaN TMBS rectifiers with field rings. The rounded trenches with flat bottoms were first formed by using the

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optimized etching processes described in Section 4.3.2. Field rings (FRs) were then formed by Ar ion implantation with the same hard mask. The implantation energy and dose are 100 keV and 1×10^{16} cm^{-2}, respectively. According to Monte Carlo simulation, this implantation has an average depth of ~100 nm into GaN.

After removing the metal masks, a 250 nm PECVD SiN$_x$ was deposited and openings were created on the mesa top surfaces by CF$_4$-based dry etching. A Ni/Au/Ni metal stack then formed the top Schottky contact. The total metal stack is thicker than the SiN$_x$ layer, to guarantee the interconnection between the Schottky metal and the metals deposited on dielectrics. Finally, the bottom Ohmic contact was formed by Ti/Al with a 400 ^{o}C annealing.

As reference devices, conventional SBDs and pure TMBS rectifiers without FRs were also fabricated on the same wafer.
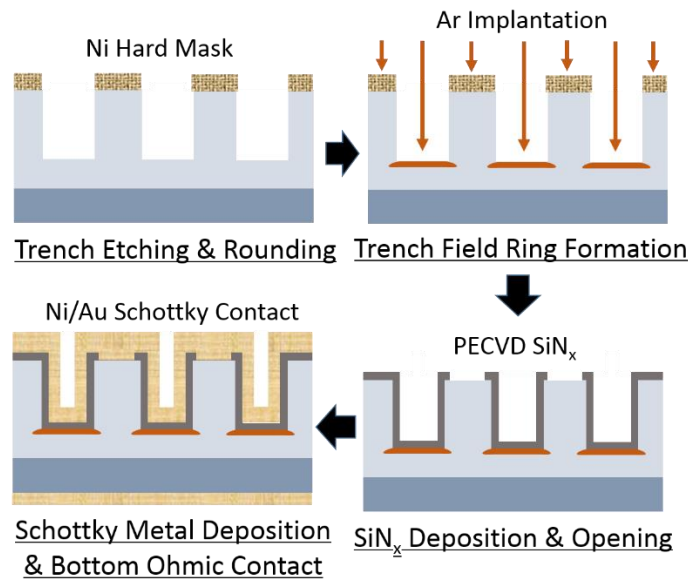
Figure 4-12 Main steps to fabricate the vertical GaN TMBS diodes with field rings.

4.4 DC Electrical Characteristics

Figure 4-13 shows the off-state leakage current and leakage current density of the GaN vertical SBD, TMBS and FR-TMBS. The leakage current density was calculated by using the effective Schottky area of each device. For TMBS and FR-TMBS diodes, only the area of Schottky contact on the top surface of GaN pillars was counted as effective Schottky area. The TMBS and FR-TMBS both have an identical trench width and mesa width of 2 μm. The comparison of leakage current density confirms that the lower leakage current in TMBS and FR-TMBS is not due to reduced effective Schottky area.

As shown in Figure 4-13, the TMBS diode enables a ~$100\times$ lower leakage current density and a slightly higher BV than SBDs (increase from 410 V to 510 V). The FRs further reduce the leakage current by ~$100\times$ and achieve a great improvement of BV (increase from 400 V to a 700 V soft BV).
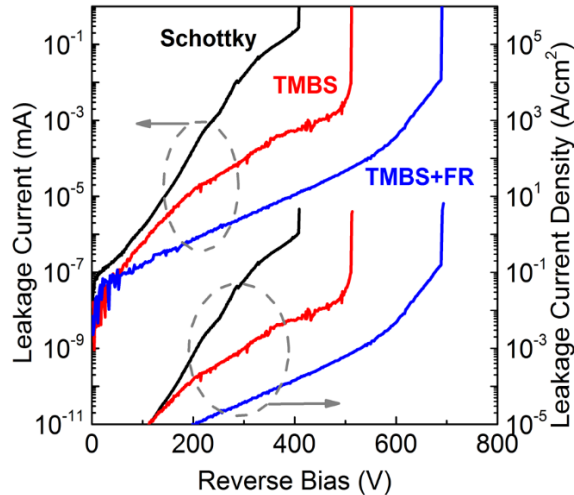
Figure 4-13 The leakage current (left) and leakage current density (right) of the GaN vertical SBD, TMBS and FR-TMBS. The leakage current density was calculated by using the effective Schottky area of each device.

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From the reverse *I-V* characteristics of the three devices, it can be seen that the TMBS and FR-TMBS rectifiers exhibited different leakage mechanisms from SBDs. As shown in Figure 4-14, the leakage current of SBD agrees with the classical thermionic field emission (TFE) model [76], which is based on the tunneling process through a Schottky barrier and can be modeled as the following expression:

$$I = \frac{I_0 E}{(k_B T)^{\frac{1}{2}}} \exp(\frac{-1}{k_B T}(\emptyset_B - C(\frac{E}{k_B T})^2)) \tag{4-1}$$

where E is electric field; T is temperature; k_B is the Boltzmann constant; $\emptyset_B$ is the Schottky barrier height; C is a constant.

For the TMBS rectifiers, the leakage current is mainly determined by TFE model below a reverse bias (V_R) of 200 V, but deviates towards a variable-range-hopping (VRH) model at higher V_R. In Chapter 3, we illustrated that the VRH model is assisted with dislocation hopping in bulk GaN and is featured by a linear relationship between ln (I) and electric field. In Chapter 3, we also showed that this VRH leakage mechanism was typically observed in GaN pn diodes where the peak electric field is in the bulk GaN. This indicates the peak electric field in TMBS has been moved from the Schottky interface to bulk GaN at high V_R, further validating the depletion effects of the trench MIS structures.
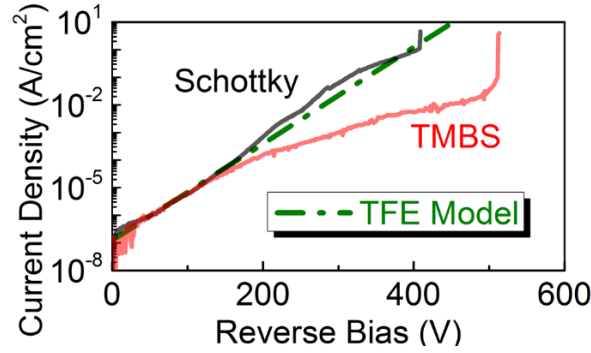
Figure 4-14 Reverse *I-V* characteristics of GaN vertical SBDs and TMBSs, and a theoretical *I-V*

characteristics calculated based on the thermionic field emission (TFE) model.

As shown in Figure 4-15 (a), the leakage mechanism of FR-TMBS diodes is dominant by VRH from low V_R to V_R~600 V. The VRH is further confirmed by having $dlog(\ln(I))/dlog(E)$~1 [19] (as illustrated in Chapter 3) in this bias window, as shown in Figure 4-15 (b). At V_R>600 V, the current increases much faster with the relationship of $I \propto V^n$, until a hump at 700 V. As illustrated in Chapter 3, this behavior indicates a trap-assisted space charge limited current (SCLC) [16][19]. This hump voltage represents the trap-filled-limited voltage (V_{TFL}) and determines the *BV*. If we compare this leakage behavior of FR-TMBS diodes to that the generalized behavior of vertical pn diodes (illustrated in Section 3.6), we can find these two leakage behavior are quite similar. This further validates the success of the design of our FR-TMBS diodes in moving the peak electric field from top Schottky junctions into the bulk GaN.
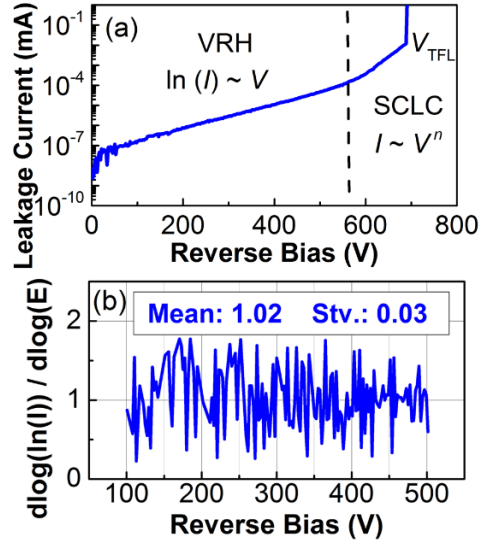
Figure 4-15 (a) Reverse *I-V* characteristics of GaN vertical FR-TMBS and the leakage mechanisms; (b) the *dlog*(ln (*I*))/*dlog* (*E*) derived from the reverse *I-V* data in the reverse bias window of 100-500 V.

Figure 4-16 shows the representative forward *I-V* characteristics of the SBD, TMBS diodes and FR-TMBS diodes. The forward current was normalized by the effective Schottky area of each device. A V_{on} of 0.7 V with a differential specific on-resistance (R_{on}) below 3 mΩ·cm^2 was observed for SBD and TMBS. The device turn-on of FR-TMBS is a little slower, with a V_{on} of 0.8 V and a higher differential specific R_{on} at low forward bias. This is due to the differential R_{on} drops to 2 mΩ·cm^2 at a bias of 4 V. Very high forward current of ~kA/cm^2 was observed in all three devices.
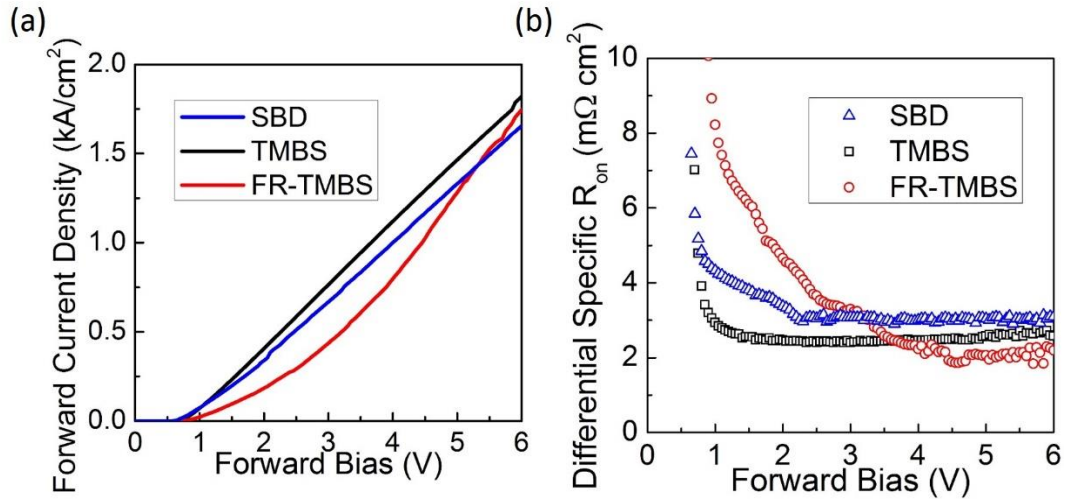
Figure 4-16 (a) The forward *I-V* characteristics and (b) the extracted differential specific on-resistance of the GaN vertical SBD, TMBS diodes and FR-TMBS diodes. The TMBS and FR-TMBS diodes are with an identical trench width and mesa width of 2 μm.

4.5 Geometry Modulation Effects

From the simulation results presented in section 4.2, we know that a smaller mesa width, w_M, enables a stronger electric field shielding of the Schottky junction and a lower electric field near the FR region. It is interesting to experimentally study this geometry modulation effects in the fabricated devices.

Figure 4-17 shows the impact of w_M on the reverse characteristics of the FR-TMBS diodes. Similar leakage current was seen in the VRH region for FR-TMBS diodes with different w_M, but the smaller w_M moves the turn-on of SCLC to a higher V_R, resulting in a larger *BV* and lower leakage at high V_R. This phenomenon is due to the stronger MIS depletion effect in the mesas with smaller w_M, and agrees with simulation.
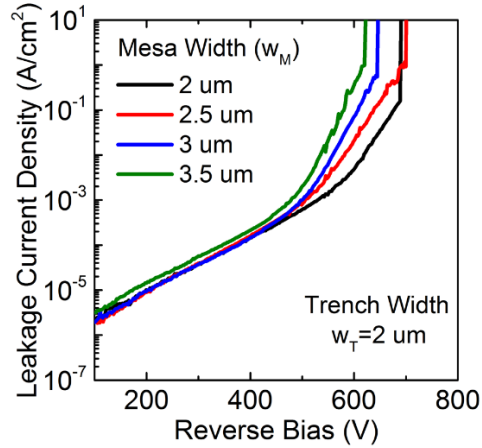
Figure 4-17 The reverse *I-V* characteristics of the GaN vertical FR-TMBS diodes with different mesa widths (2 μm to 3.5 μm). The trench width is 2 μm for all devices.

Figure 4-18 shows the forward *I-V* characteristics of the GaN vertical FR-TMBS diodes with different mesa widths. As shown, similar forward *I-V* were observed for FR-TMBS with different w_M, with the same V_{on} of 0.8 V. Slightly better turn-on was shown for larger w_M due to a more spread forward current.
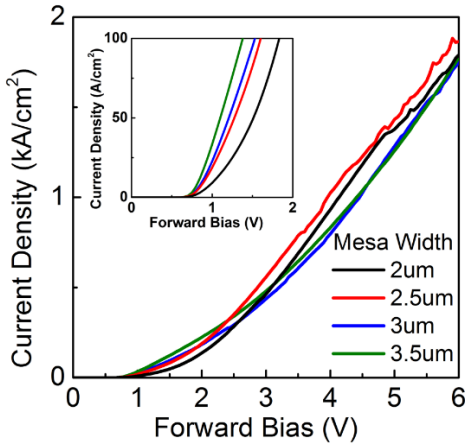
Figure 4-18 The forward *I-V* characteristics of the GaN vertical FR-TMBS diodes with different mesa widths (2 μm to 3.5 μm). The trench width is 2 μm for all devices. (Inset) The zoom-in of the forward *I-V* curve between 0 V and 2 V.

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Figure 4-19 summarizes the on/off current ratio of SBD, TMBS diodes and the FR-TMBS diodes with different w_M. The I(+5V)/I(-400V) represents the ratio of the current at a forward bias of 5 V and the current at a reverse bias of 400 V. The I(+5V)/I(-600V) represents the ratio of the current at a forward bias of 5 V and the current at a reverse bias of 600 V. As can be seen, the FR-TMBS diodes exhibit an on/off ratio $\sim10^4\times$ higher than in the SBD. The FR-TMBS diodes with different w_M has similar $I(+5V)/I(-400V)$ but a dramatically reduced $I(+5V)/I(-600V)$ with increasing w_M. This indicates the importance to have small w_M (<2 μm for the $N_D\sim2\times10^{16}$ cm^{-3} in drift region) in FR-TMBS diodes for 600-V level power applications.
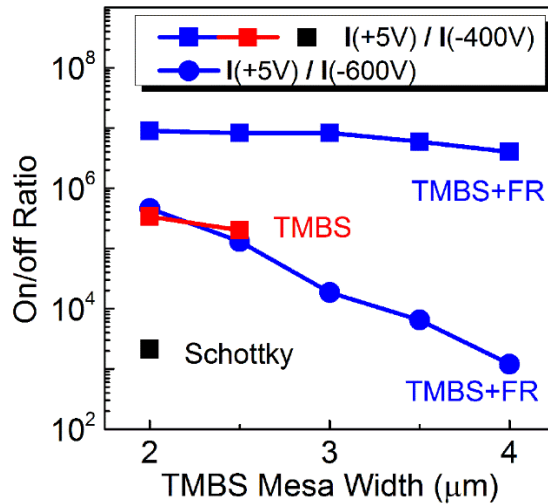
Figure 4-19 The on/off ratio of GaN vertical SBD, TMBS diodes and the FR-TMBS diodes with different mesa widths.

4.6 High-Temperature Behavior and Switching Characteristics

Figure 4-20 shows the high-temperature performance of FR-TMBS diodes. As shown in Figure 4-20 (a), the *BV* drops with increased temperature, but still maintains over 400 V at 250 °C. The increase of leakage current with temperature is slower than in SBD, but faster than in pn diodes [19]. This indicates the leakage current at high temperature is determined by both Schottky barrier and bulk layer. The reduction of *BV* at higher temperature indicates the *BV* is a trap-assisted mechanism, which is consistent with the trap-assisted SCLC mechanism illustrated in section 4.4.
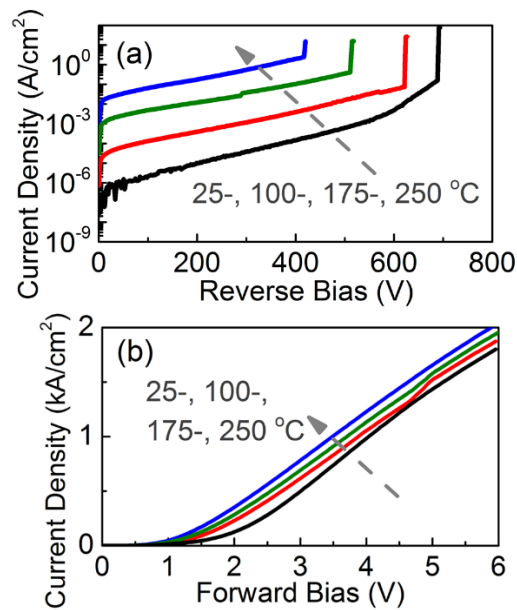
Figure 4-20 The (a) reverse and (b) forward I-V characteristics of the GaN vertical FR-TMBS diodes at different temperatures. The trench width and mesa width are both 2 μm.

The forward *I-V* of FR-TMBS diodes is shown in Figure 4-20 (b). Interestingly, the forward current of FR-TMBS diodes slightly improves at increased temperature, opposite to SBD and TMBS diodes. The reduced forward current of SBDs and TMBS diodes at

higher temperatures can be explained by the degraded carrier mobility. This carrier mobility degradation at high temperatures would also occur in FR-TMBS diodes, indicating that there is another stronger factor driving the forward current to increase at higher temperatures. We believe this factor may be the filling of the acceptor-like traps created by ion implantation at higher temperature or the degradation of insulating properties of the Ar implanted regions at higher temperature. This 'de-activation' effects of the implanted field rings at higher temperature can also explain the degraded *BV* at higher temperatures. However, additional future work in the characterization of FR-TMBS diodes at higher temperatures is needed to verity this proposed model.

Figure 4-21 shows the reverse recovery characteristics of FR-TMBS diodes, measured by an on-wafer pulser setup. The device was switched from a forward current of 1300 A/cm^2 to pinch off with V_R of 200 V at a rate of 2 A/μs (setup limits). A reverse recovery time of 25 ns was extracted, which is comparable to the best reports for vertical GaN SBDs [57][77].
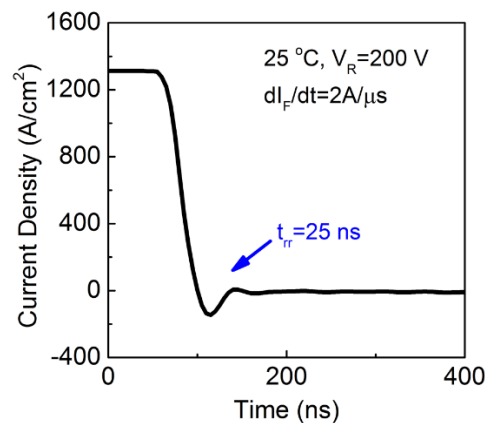
Figure 4-21 Reverse recovery characteristics of the GaN vertical FR-TMBS diodes, measured by an on-wafer pulser setup. The device was measured from a forward current of ~1300 A/cm^2 to a reverse bias of 200 V with a dI$_F$/dt of 2 A/μs (setup limits).

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4.7 Performance Benchmark

Figure 4-22 benchmark the leakage current *v.s.* N_D-N_A and the R_{on} *v.s.* *BV* for our FR-TMBS diodes with the reported GaN vertical SBDs [7], [10], [11], [57]–[59]. In vertical GaN SBDs, many groups have reported a strong dependence of reverse leakage current on the N_D-N_A in drift region [10], [60]. Tanaka *et al.* summarized an empirical model that the leakage current of GaN vertical SBDs is low and stable when N_D-N_A~10^{15} cm^{-3}, but increases exponentially after N_D-N_A exceeds 10^{16} cm^{-3} [60]. As shown in Figure 4-22 (a), this model roughly agrees with the literature data reported by different groups.

The N_D-N_A in the drift region of our GaN-on-GaN wafer is 2×10^{16} cm^{-3}, which is the highest in all the reported vertical GaN SBDs. As shown in Figure 4-22 (a), with a N_D-N_A of 2×10^{16} cm^{-3}, our FR-TMBS diodes showed a leakage current at least 2~3 orders of magnitude lower than the vertical SBDs with similar N_D-N_A concentrations. Our FR-TMBS diodes achieved a low leakage current comparable to the vertical SBDs with N_D-N_A~10^{15} cm^{-3}.

As shown in Figure 4-22 (b), our FR-TMBS diodes exhibit the second best R_{on} *v.s.* *BV* trade-off, with a high on/off ratio of 10^6 at 600-V level. At 125 ^{o}C, our FR-TMBS diodes maintains a high on/off ratio of 5×10^4 at 600-V level. In addition, our FR-TMBS demonstrates the capability of operation at above 200 ^{o}C for the first time in all high-voltage GaN vertical SBDs. Even at 250 ^{o}C, our FR-TMBS diodes maintains a high on/off ratio of 2×10^3 at over 400-V level.
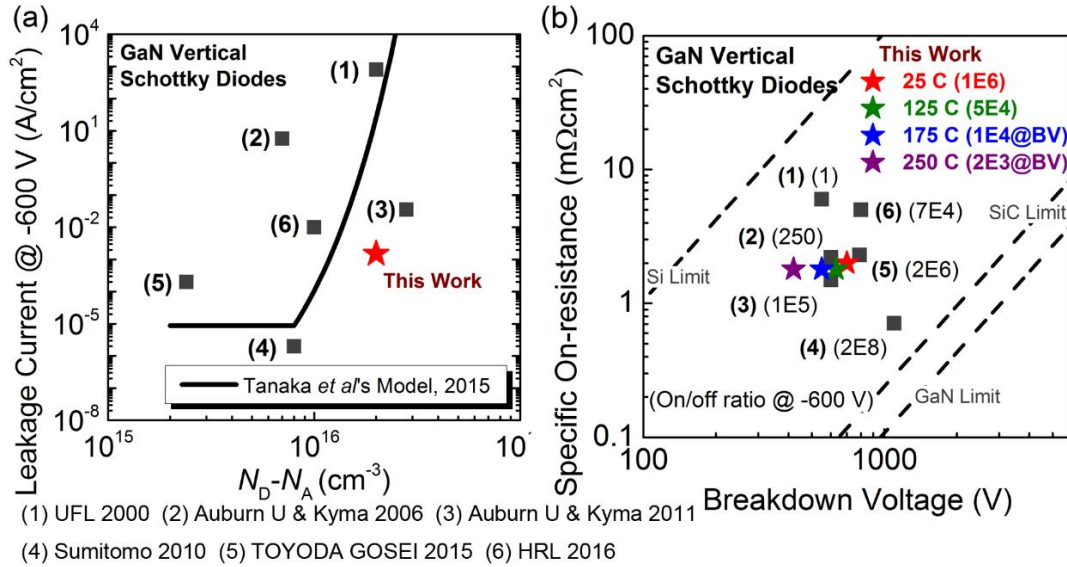
Figure 4-22 (a) leakage current v.s. N_D-N_A and (b) R_{on} v.s. *BV* benchmarking for the reported GaN vertical SBDs with BV higher than 600 V. 600 V-level on-off ratio was also denoted in (b) for the reported GaN vertical SBDs and our vertical FR-TMBS diodes at different temperatures.

Our vertical GaN FR-TMBS diodes were also benchmarked with AlGaN/GaN lateral SBDs, SiC SBDs and Si fast recovery diodes. Table 4-2 shows the forward voltage (V_F), on/off ratio, reverse recovery time (t_{rr}), maximum operation temperature of 600-V level GaN vertical FR-TMBS diodes, AlGaN/GaN lateral SBDs, SiC SBDs and Si Fast Recovery diodes. The V_F of FR-TMBSs was extract at a current level of 100 A/cm^2. The V_F and t_{rr} of AlGaN/GaN lateral SBD, SiC SBD and Si diodes were extracted from [78]. The on/off ratio of GaN lateral SBD was extracted from the state-of-the-art report [52]. From Table 4-2, it can be shown that our first vertical GaN FR-TMBS diodes has similar or even slightly better performance to the extensively studied AlGaN/GaN lateral SBDs and commercial SiC SBDs, and outperformed the commercial Si fast recovery diodes.

Table 4-2 Forward voltage (V_F), on/off ratio, reverse recovery time (t_{rr}), maximum operation temperature of 600-V level GaN vertical FR-TMBS diodes, AlGaN/GaN lateral SBD, SiC SBD and Si Fast Recovery diodes.

	V_F (V)	On/off ratio (-600V)	t_{rr} (ns)	Max Temperature (^{o}C)
This Work (GaN FR-TMBS)	**1.6**	**10^6**	**25**	**>200**
AlGaN/GaN Lateral SBD	1.6	10^5-10^6	20-30	>175
SiC SBD	1.5	10^5-10^6	20-30	175
Si Fast Recovery	2.6	10^5	30-40	150

A further reduction of N_D-N_A in the drift region of our GaN-on-GaN wafers could further enable a lower leakage and better R_{on} *v.s.* *BV* for our vertical GaN TMBS. This is due to two reasons: (a) a lower N_D-N_A could enable a stronger MIS depletion in the mesa structures. For example, if N_D-N_A reduces by a factor of three, the new FR-TMBS diodes with a mesa width of 5~10 μm could have similar depletion effects to the current FR-TMBS diodes with a mesa width of 2 μm. The new FR-TMBS diodes with a mesa width below 2 μm could enable a much more enhanced depletion effects, resulting in an even higher *BV* and lower leakage current. (b) Similar to conventional SBDs, a lower N_D-N_A could lower the leakage current through thermionic emission over the Schottky barrier and the leakage current tunneling directly through the Schottky barrier from the metal to the conduction band of GaN. This would also help reduce the total leakage current in vertical GaN FR-TMBS rectifiers, especially at higher temperatures.

4.8 Conclusion and Prospect

In this Chapter 4, we demonstrate a novel GaN vertical Schottky rectifier with trench MIS structures and trench field rings. This vertical GaN FR-TMBS rectifier is an advanced Schottky diode that greatly enhances the reverse blocking characteristics while maintaining a Schottky-like good forward conduction. The reverse leakage current improved beyond 10^4-fold and the BV increased from 400 V to 700 V, while the low turn-on voltage (0.8 V) and R_{on} (2 m$\Omega \cdot$cm^2) were retained. High-temperature operation up to 250 ^{o}C and fast switching performance were also demonstrated. This new device shows great potential for high-power and high-frequency applications.

In the fabrication of this novel device, we developed an optimized trench formation and corner rounding processes, which are the key processes to demonstrate high-voltage trench-based vertical GaN devices. We developed a novel damage-free corner rounding technology combining TMAH wet etching and piranha clean. By optimizing the ICP dry etching conditions and applying the rounding technology, two main trench shapes were demonstrated: flat-bottom rounded trench and tapered-bottom rounded trench. TCAD simulations were then performed to investigate the impact of trench shapes and round corners on device blocking capability. GaN trench metal-insulator-semiconductor (MIS) barrier Schottky rectifiers with different trench shapes were fabricated and characterized. Both experimental and simulation results support the use of rounded flat-bottom trenches to fabricate high-voltage GaN trench-based power devices.

To obtain a more complete understanding into the developed novel GaN FR-TMBS diodes, future work is needed in the following aspects:

(a) Microscopic characterization and understanding on the location and energy levels of the traps determining the device *BV*;

(b) Demonstrating FR-TMBS diodes on the wafers with N_D-N_A~10^{15} cm^{-3}, and further scaled down the mesa width to sub-micron scales;

(c) Understanding in depth the device reverse and forward characteristics at high temperatures;

(d) Exploring other technologies to make field rings, e.g. p-type doping and activation, other implantation ions, introduction of fixed charges, etc.

Chapter 5 Patterned GaN pn Junctions and Junction-based Power Devices

5.1 Introduction

As demonstrated in Chapters 2, 3 and 4, thanks to the efforts world-wide, GaN vertical devices have recently shown better *BV* and current capability than GaN lateral devices, especially above 600 V. However, besides vertical pn diodes, the full potential of GaN vertical Schottky diodes and transistors beyond 1200 V applications has not been fully exploited yet. For vertical Schottky rectifiers, although advanced structures have enabled high-performance 600-1200 V devices, there is no SBDs demonstrated for beyond 1200 V applications. For vertical transistors, although a high *BV* of 1600-1700 V has been demonstrated [13], there is no avalanche breakdown reported, which will greatly harm the reliability and robustness of these devices in real power switching applications.

The bottleneck for this situation lies in proper electric field management and in the lack of selective area doping, reliable and generally useable pn junction regions. Compared to Si and SiC power device, this bottleneck becomes a fundamental limitation for high-voltage vertical GaN devices. GaN still lacks a viable selective area doping or selective area epitaxial regrowth technologies that yield material of sufficiently high quality to enable a defect-free p-n junction on patterned surfaces. Success in this area will allow further development of a revolutionary and powerful class of vertical GaN power electronic devices suitable for 1200 V to 10 kV broad range of applications (consumer electronics, power supplies, solar inverters, wind power, automotive, motor drives, ship propulsion, rail, and the grid). (Reference: ARPA-E PNDIODES full FOA; https://arpa-e.energy.gov/?q=pdfs/pndiodes-de-foa-0001691)

In this chapter, we will first introduce the concepts and challenges of two approaches to make patterned pn junctions: (a) laterally patterned ion implantation and activation, and (b) selective area etch and regrowth. Then we will discuss two device structures that can be enabled by patterned pn junctions, including: (a) junction-barrier Schottky diodes / merged pn/Shottky diodes; and (b) super-junction devices.

5.2 Formation of Patterned pn Junctions

5.2.1 Patterned Ion Implantation and Activation

Generally, there are two approaches to form patterned pn junctions by patterned ion implantation and activation: (a) p-type dopant implantation and activation in epitaxially grown n-type GaN, and (b) n-type dopant implantation and activation in epitaxially grown p-type GaN.

For the first approach, Mg is typically used as the p-type implanted ion. The main challenge for this approach lies in the activation of Mg in GaN, due to the high temperatures required (over 1300 $^{\circ}$C) for the activation annealing [79]. This activation temperature is much higher than the decomposition temperature of GaN at atmospheric pressure (800-900 $^{\circ}$C) [80]. The decomposition of GaN will typically induce the loss of nitrogen at surface and formation of N vacancies.

To avoid the GaN decomposition at high annealing temperatures, two methods have been proposed. The first method is to do the annealing in high pressure environments. It has been reported that GaN can be successfully annealed at ~1500 $^{\circ}$C at a 1.5 GPa overpressure of N_2 [81]. However, such high gas pressures need complicated experimental set-up and are not generally available.

The other method for GaN annealing at high temperatures relies on using non-equilibrium annealing conditions and a carefully-chosen capping layer. The Naval Research Laboratories is the main research institute developing this method, and has published a series of papers demonstrating the capability to activate the implanted Mg in GaN [80][83] [84]. Figure 5-1 shows the schematic of the temperature profiles for the (a) multicycle rapid thermal annealing (MRTA) technique and (b) symmetric multicycle rapid thermal annealing (SMRTA) technique. The key concept for the MRTA or SMRTA technique is to utilize repetition of heating pulses to get a long aggregate time above 1300 $^{\circ}$C while preserving the integrity of GaN [83]. The SMRTA has been demonstrated to be superior to the MRTA technique in terms of improvement of the crystalline quality of implanted GaN [83]. In addition, an AlN cap layer is used in these processes to prevent the N loss at GaN surfaces [79]. The activation ratio between the ionized acceptor concentration and total implanted Mg density is typically around 1%, with the best reported value above 8% [82]. However, the conductivity of the implanted p-type regions is still very low. Although the best resistivity extracted from the TLM measurements is low than 1 Ω cm [83], the forward current density of Mg-implanted vertical GaN pin diodes is below 1 A/cm^2 [84][85], indicating an average resistivity of Mg-implanted GaN region in the vertical direction is higher than 10^4 Ω cm^2. This large difference between the extracted resistivity in the lateral direction (from TLM measurements) and in the vertical direction (from R_{on} of vertical pin diodes) has not been explained in the literature. We believe this difference may be due to the incomplete activation of Mg ions into free holes in the relative deep regions. This non-activated region may form a highly insulated

inter-layer between the top activated p-type regions and the bottom conductive n⁻-GaN region in a p-i-n structure.
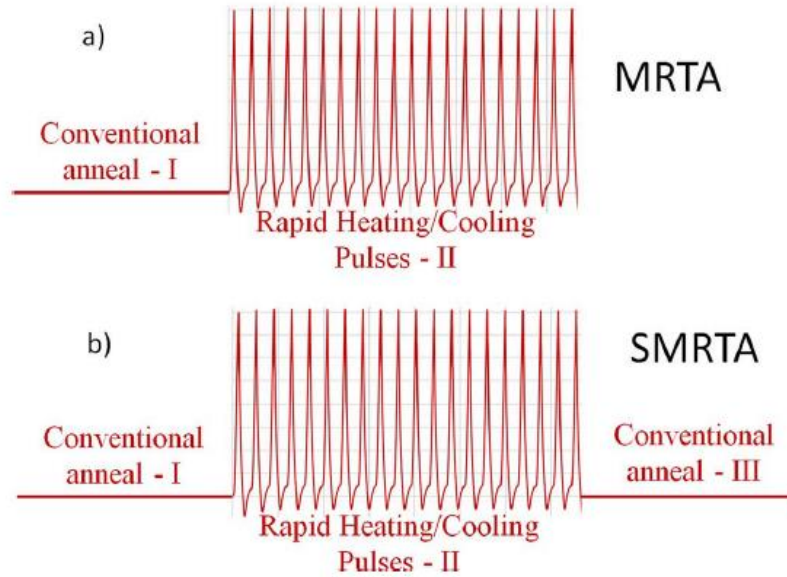
Figure 5-1 Schematic of the temperature profiles for the (a) multicycle rapid thermal annealing technique and (b) symmetric multicycle rapid thermal annealing technique, extracted from [83].
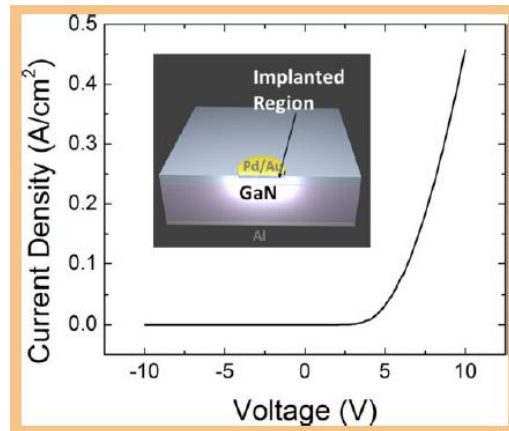
Figure 5-2 Forward *I-V* characteristics of a Mg-implanted pin diode, (inset) schematic of the Mg-implanted pn diode, extracted from [84].

From the above discussion, we can see that the p-type implantation into n-GaN or n⁻-GaN requires complicated activation schemes and has very low average resistivity in the vertical direction. Another approach to create patterned pn junctions by selective ion implantation is to do the n-type implantation into p-GaN. The successful conversion of p-GaN into n-GaN by Si implantation has been reported by several groups [85]–[88]. Table 5-1 summarizes the implantation dose, activation condition and activation efficiency of the Si implantation into p-GaN. From this table, it can be seen that the activation of the implanted Si in p-GaN just requires a single activation at 1000-1200 $^{\circ}$C. This activation is much easier and controllable compared to the p-type activation in n-GaN. The activation temperature is also lower than that in the p-type activation.

Table 5-1 Implantation dose, activation condition and activation efficiency of the Si-implanted p-GaN, reported in the paper I [85], II [86], III [87] and IV [88].

Paper	Year	Cap Layer	p-GaN doping (cm^{-3})	Implantation Dose (cm^{-2})	Annealing temperature, time	Activation Efficiency
I	2002	GaN	Hole: 3E17	1E15, 1E16	1000-1200 C, 60 s	1E15:1.3-30% (1000-1150 C) 1E16: 6.23-11.7% (1000-1150 C)
II	2002	GaN	Hole: 3E17	2E15 (40keV) 5E15 (100keV) 5E15 (200keV)	750-1000 C, 30 min	0.4% to 27% (750 C-1000 C)
III	2008	SiO$_2$	[Mg]~1E17	3E14-3E15	1000-1260 C (mostly at 1260 C), 10-30 s	0.01%-10% (1200 C) 20%-100% (1260 C)
IV	2010	SiO$_2$	Hole: 5E18	1E15, 1E16	1100 C, 5 min	1.4%, 11.3%
		GaN	Hole: 5E18	1E16	1100 C, 5 min	4.8%

From the discussion above, it can be seen that the Si implantation into p-GaN seems to be an easier and more controllable approach compared to the Mg implantation into n-GaN, for the fabrication of patterned pn junctions based on ion implantation. However, in most of vertical devices, such as junction-barrier Schottky rectifiers and superjunction devices, as only n-type regions contribute to the device forward conduction and the p-type regions only impact the device reverse characteristics, the requirement of n-GaN mobility, carrier density and resistivity is much higher than that of p-GaN. If the Si implantation into p-GaN is used to create vertical pn pillars, the implanted ion profile and mobility needs to be accurately calibrated and the implanted region needs to be high-quality with few defects.

5.2.2 Selective Area Etch and Regrowth

In section 5.2.1, we discussed the feasibility of making vertical GaN pn junctions by using ion implantation. However, there are three fundamental challenges regarding ion implantation: (a) relatively small implantation depth (typically less than 500 nm for a high implantation energy level of 500 keV), (b) the need for extremely high temperature activation (typically over 1300 $^{\circ}$C for p-GaN activation and over 1000 $^{\circ}$C for n-GaN activation), and (c) the difficulties to achieve uniform dopants concentration profile in the vertical direction.

In this chapter, we propose to use selective epitaxial regrowth to develop a GaN vertical-pn-pillar technology for power electronics. We will perform GaN epitaxy on n^{+}-GaN substrates, create deep trenches into n^{-}-GaN drift regions, and fill the trenches with regrown p-GaN. In an alternative approach, we will create deep trenches into p-GaN and

then fill the trenches with n⁻-GaN growth. Figure 5-3 shows schematic of a process flow to make patterned pn junctions by using selective epitaxial regrowth.
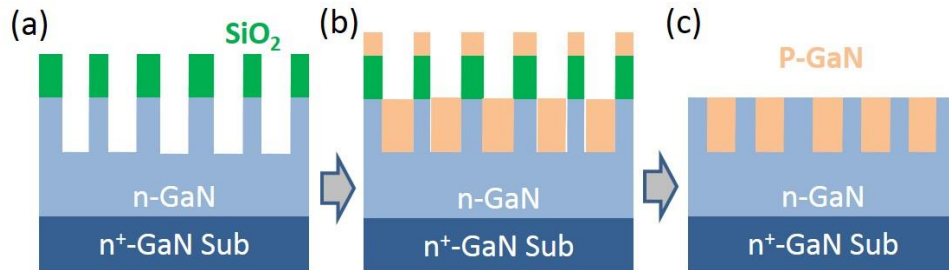
Figure 5-3 Schematic of a process flow to make patterned pn junctions by using selective epitaxial regrowth.

From Figure 5-3, it can be seen that there are two key processes for fabricating patterned pn junctions: (a) trench etching and sidewall treatment; (b) selective epitaxial regrowth. In section 4.3.2, we have developed optimized processes for trench formation, corner rounding and sidewall treatment. Although a trench depth of 2 μm was shown in the processes developed in section 4.3.2, we are able to increase the depth/width aspect ratio to over 4 μm/1.5 μm with further optimization in the etching processes. The details will be shown in section 5.4.2.

The selective regrowth of both n- and p-type GaN has recently been demonstrated by using MBE and MOCVD [3]. This selective regrowth methods have been used and optimized in the fabrication of GaN vertical electron transistors. In order to make this method succeed in making patterned pn junctions, where the trenches with a much higher aspect ratio need to be filled, several kay challenges need to be addressed simultaneously:

(a) Complete filling of the n-GaN trenches with high aspect ratio. During the selective regrowth of p-GaN, the possible GaN deposition at the edge of hard mask may shield the growth inside the n-GaN trenches, making it difficult to fully fill those trenches. This shielding effect may be a serious issue especially for the filling of narrow and deep trenches required for the demonstration of super-junction devices. A potential solution for this problem will be proposed in section 5.3.3.3.

(b) Regrowth Selectivity. As shown in Figure 5-3 (b), ideally, there should be no p-GaN deposition on the top of each n-GaN pillars, so that a perfectly flat surface will be created after removing the masks (Figure 5-3 (c)). However, this ideal selective regrowth is quite difficult, even by utilizing dielectric masks (e.g. SiO_2 and SiN_x) on top of n-GaN pillars. As shown in Figure 5-4, morphological spikes are likely to appear at the edge of the sidewall once the mask is removed; these spikes might induce large device leakage current and early breakdown [3]. A novel method to remove the over-growth p-GaN has been demonstrated in section 5.4.2.

(c) Interface quality control. A great challenge relate to the incorporation of impurities such as [C], [O], and [Si] at the regrowth interfaces, which provides leakage paths leading to the early breakdown of fabricated devices. Regrowth processes are needed to reduce such impurity incorporation through *ex situ* and *in situ* surface treatments as well as special growth strategies. It has been reported in [89] that the pre-growth surface treatments include a series of 15 minute ozone cleaning, followed by 5 minute buffered HF (BHF) dips repeated 3

times, can remove the majority of impurities ([C], [O] and [Si]) from the growth surface.

(d) Activation of p-GaN in deep regions. The p-GaN is preferred to be grown by MBE rather than MOCVD, for a regrowth depth above 1 μm. The p-GaN grown by MOCVD requires a post-growth annealing to break the Mg-H bonds and activate the Mg acceptors. This activation is difficult to reach a depth above 1 μm. On the other hand, the MBE p-GaN regrowth does not need post-growth activation, and is therefore preferred for deep p-GaN regrowth.
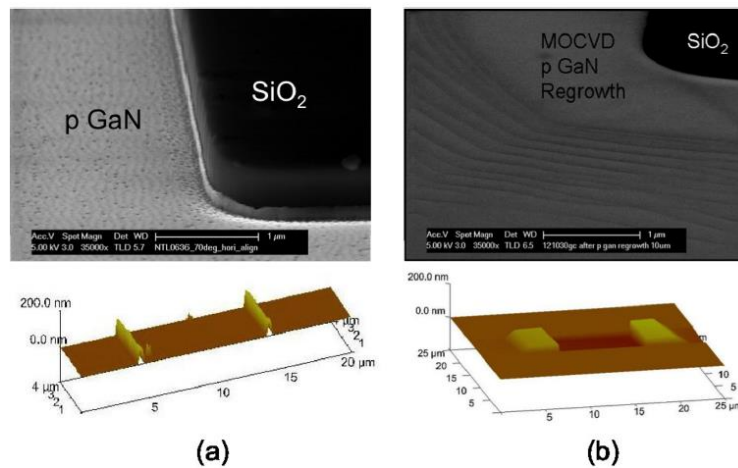
Figure 5-4 p-GaN regrown in n-GaN trenches with SiO_2 mask by (a) NH_3-MBE and (b) MOCVD, and the AFM images for the surfaces after removing SiO_2, as extracted from [3].

5.3 Patterned-Junction-based Power Devices

5.3.1 Junction-Barrier Schottky Diodes / Merged pn-Schottky Diodes

In section 5.2, we introduced two main approaches to form patterned pn junctions. In this section 5.3, we will introduce the power devices that can be demonstrated with the patterned pn junctions. In the section 5.3.1, we will introduce the junction-barrier

Schottky (JBS) diodes / merged pn-Schottky diodes, which has been briefly mentioned in section 4.1.

As mentioned in Chapter 4, despite the high *BV* and low leakage of GaN pn diodes, their large turn-on voltage (V_{on}>3 V) induces large conduction loss in power switching. On the other hand, GaN vertical Schottky barrier diodes (SBDs) have low V_{on} and fast switching, but suffer from large leakage due to the high electric field at the Schottky contact. Thus, advanced GaN rectifiers combining the Schottky-like forward and pn-like reverse characteristics are desired.

As shown in Figure 5-5, the proposed GaN JBS diode consists of a grid of patterned pn junctions, sitting just beneath the Schottky contact (Fig. 2). Under reverse bias, the p-n junctions move the peak electrical field from the surface into bulk GaN, resulting in lower leakage and higher *BV*. Under forward bias, the p-wells are inactive and the V_{on} is determined by the Schottky barrier. The SiC JBS diode has achieved a tremendous success up to 10 kV applications [61].

Figure 5-5 Schematics of a vertical GaN JBS diode.

In a similar structure, we can also make another power device called merged pn-Schottky (MPS) diodes [61]. Both JBS diodes and MPS diodes consist of similar

patterned pn junctions below the top electrode, however, in the former, the Schottky metal does not form a low-resistance contact to the p-type regions. Thus, under forward bias, no minority carriers are injected across the pn junctions. Since there is no minority carrier injection, the JBS diode commutates to the reverse blocking state with a minimal reverse recovery current, enabling a fast switching. In contrast, in MPS diodes, the metallization does form an Ohmic contact to the p-type grid (by either doping the p-type grid very heavily or by annealing the contacts to the p-type grid), allowing for minority carrier injection during forward biasing. This merged pn structures can enable the device to survive a large reverse surge current [61]; however, it will significantly increase the reverse recovery stored charge and induce a much slower switching [61].

The first GaN JBS diode was demonstrated by Naval Research Lab in early 2017 [90] by using Mg implantation into n-GaN, with a BV of 600 V but a high R_{on} over 100 $m\Omega$ cm^2. We have collaborated with Naval Research Lab and demonstrated JBS diodes by using two approaches: Mg implantation into n-GaN and Si implantation into p-GaN. Our preliminary results have shown significantly improved performance compared to the first demonstration. We will show our preliminary results in section 5.4.1.

5.3.2 Super-Junction Devices

5.3.3.1 Super-Junction Device Concepts

Conventional unipolar GaN power devices are limited by a theoretical trade-off between V_B and R_{on}, where R_{on} is proportional to $V_B^{2.4-2.6}$ [91]. This trade-off can be broken by a super-junction (SJ) structure. As shown in Figure 5-6, SJ structures consist of multiple highly-doped thin p-n junctions. The p-n junctions cause full depletion of the

device channel at a small reverse bias. Further reverse voltages are supported by the fully depleted SJ with almost uniform distribution of electric field, regardless of doping concentration. Therefore, a higher doping concentration in the channel can be adopted, compared to conventional structures, to sustain the same V_B, yielding a much lower R_{on}. The R_{on} shows a linear dependence on the V_B for vertical SJ devices ($R_{on} \sim V_B$) (Figure 5-6 (b)), and a square dependence for lateral SJ devices ($R_{on} \sim V_B{}^2$) (Figure 5-6 (a)) [92][93].
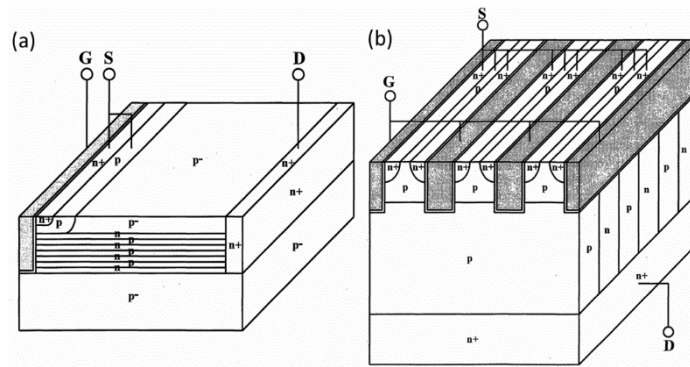
Figure 5-6 Schematics of (a) lateral and (b) vertical SJ power device, as extracted from [94].

SJ devices can enable remarkable improvement for power device performance, but are not easy to fabricate. After over 10 years' development, Si SJ devices have been successfully commercialized. The CoolMOS^{TM} devices based on Si SJ structures have achieved huge success in the current power electronic market. Although SiC power devices have been developed for over 20 years, the first SiC SJ diodes were just demonstrated experimentally in 2014 [95]. For GaN devices, there has been no experimental demonstration of vertical SJ devices reported so far.

5.3.3.2 Design Space for GaN Super-Junction Devices

The initial structure for the proposed GaN vertical SJ diode is shown in Figure 5-7. consists of a n^+-GaN substrate (~300 μm, Si doping > 10^{18} cm^{-3}), multiple p-n GaN pillars (n: 7~8 μm for 1200 V design, Si doping 5×10^{16}~1×10^{18} cm^{-3}) (p: 5~7 μm for 1200 V design, Mg doping level to enable $N_A = N_D$) and p^+-GaN layer (~0.4 μm, Mg doping > 10^{19} cm^{-3}). The anode and cathode are both Ohmic contacts on the top surface and bottom surface of the wafer structure.
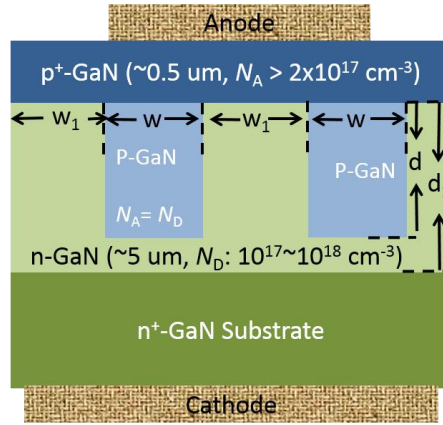
Figure 5-7 Schematics of a proposed GaN vertical SJ diode.

In SJ structures it is important that the ionized acceptor concentration N_A in p-GaN equals to the ionized donor N_D concentration in n-GaN. Under reverse bias, we expect all the acceptors and donors in the depleted regions to be ionized, independently of their ionization energy [22]. Thus, the acceptor concentration N_A equals the uncompensated Mg concentration for the p-GaN pillars under reverse bias.

In GaN vertical SJ devices, an optimum combination of geometry and doping parameters, including pillar width d, ionized donor and acceptor concentration N_A (=N_D),

would allow the best trade-off between V_B and R_{on}. In this section, analytical analysis will be performed to find the optimum combination for the d, N_D and N_A.
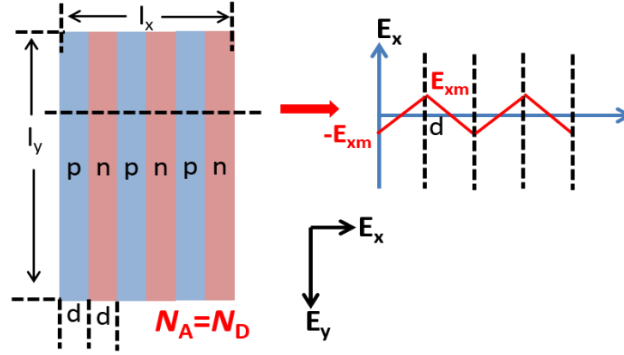
Figure 5-8 Schematics of electric field distribution in vertical SJ structures.

A schematic of the electric field distribution in vertical SJ structures is shown in Figure 5-8. The p-n junctions form a periodic electric field along the x-axis and a uniform electric field E_y along y-axis. The maximum electric field along x direction and y direction at device breakdown is

$$E_{xm} = \frac{qN_A d}{2\varepsilon_{GaN}} = \alpha E_c \qquad (5\text{-}1)$$

$$E_{ym} = \sqrt{1 - \alpha^2} E_c \qquad (5\text{-}2)$$

where E_c is the critical electric field of GaN, ε_{GaN} is the dielectric constant of GaN and $\alpha = \frac{qN_A d}{2\varepsilon_{GaN} E_c}$ is a parameter denoting the ratio between E_{xm} and E_{ym}.

The SJ forward specific on-resistance $R_{on-specific}$ and reverse breakdown voltage is then given by

$$R_{on-specific} = \frac{2}{qN_D\mu_e} l_y = \frac{d l_y}{\alpha \mu_e E_c \varepsilon_{GaN}} \qquad (5\text{-}3)$$

$$V_B = l_y\sqrt{1 - \alpha^2} E_c = \frac{\alpha\sqrt{1-\alpha^2}}{d}\mu_e \varepsilon_{GaN} E_c^2 R_{on-specific} \qquad (5\text{-}4)$$

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After solving the optimum for Equation (5-4), we can get the relationship between optimum pillar width d_{opt} and optimum donor (acceptor) level (N_{Dopt}):

$$\frac{1}{\sqrt{2}d_{opt}} = \frac{qN_{Dopt}}{2\varepsilon_{GaN}E_c} \qquad (5-5)$$

Equation (5-5) shows that we could increase the doping level in the p-n junction to reduce the on-resistance, at the expense of the increased difficulty associated with the fabrication of narrower p-n pillars. The optimum pillar width has been calculated as a function of N_A, N_D levels in p-n pillars, as summarized in Table 5-2. Table 5-2 also shows the design space of BV and R_{on} for vertical SJ diodes corresponding to each N_A, N_D and d combinations.

Considering the process limitations of optical lithography accuracies and deep etching width/depth ratios, a d_{opt} of ~2.5 µm with a N_A, N_D of ~10^{17} cm^{-3} can be selected for the design of the first demonstrator. More advanced processing technologies (e.g. electron-beam lithography) could be developed in the future to enable a smaller d_{opt} with an even higher N_A, N_D.

Table 5-2 Calculated optimum p-n pillar width as a function of the N_A, N_D levels in p-n junction, and

the corresponding design space of BV and R_{on} for vertical SJ diodes.

N_A, N_D (cm^{-3})	5×10^{16}	10^{17}	5×10^{17}	10^{18}
d_{opt} (μm)	5	2.5	0.5	0.25
V_B (V)	1270	1270	1270	1270
$R_{on\text{-}SJ}$ (mΩcm^2)	0.3	0.15	0.03	0.015
$R_{on\text{-}Device}$	< 0.5	< 0.35	<0.25	<0.2

Assume: SJ structure thickness: 6 μm, μ_e=500 cm^2/Vs, E_c=3 MV/cm

$R_{on\text{-}Device}= R_{SJ} + R_{Anode}$ (<10^{-2} mΩcm^2) + $R_{Cathode}$ (<10^{-3} mΩcm^2) + $R_{p\text{-}GaN}$ (~0.1 mΩcm^2 for μ_p=20 cm^2/Vs and N_A=2×10^{17} cm^{-3}) + $R_{substrate}$ (<10^{-2} mΩcm^2)
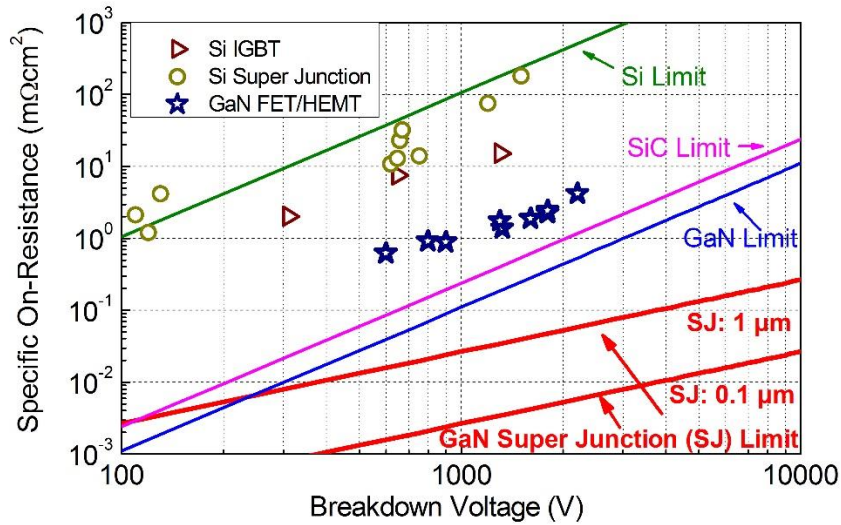
Figure 5-9 Theoretical limits of specific on-resistance as function of breakdown voltage for Si, SiC,

conventional GaN and GaN vertical super junction device (with a p-n pillar width of 0.1 μm and 1 μm).

The theoretical limits of BV vesus R_{on} for vertical GaN SJ devices with the feature p-

n pillar width of 0.1 μm and 1 μm were calculated and plotted in Figure 5-9. As shown,

vertical GaN SJ devices can achieve a 5 to 10× lower R_{on} than the theoretical limit of

conventional unipolar GaN power devices for a V_B range of 1000-3000 V, when the

feature length of SJ device (pillar width of p-n pillars) is ~ 1 μm. If we can make vertical

SJ device with a feature length of ~0.1 μm, then a $50\times$ to $100\times$ lower R_{on} than the

theoretical limit of conventional unipolar GaN power devices can be achieved. Therefore,

the area of conventional devices can be reduced by between 80% and 90% while keeping

the same on-resistance. At the same time, the uniform reverse electric field in vertical SJ

device can reduce the drift layer thickness by ~ 30% while still achieving the same V_B of

conventional power devices. Considering these two factors, we estimate that vertical GaN

SJ devices would save more than 80% of the material cost compared to conventional

GaN devices. In comparison to the best vertical GaN power devices reported, the vertical

GaN SJ devices would achieve at least $8\times$-$10\times$ lower R_{on} and at least 50%-60% lower

epitaxial material cost for 1200 V power device. This performance would create

tremendous new opportunities for GaN power electronics.

It should be noted that the calculation above does not consider conductivity

modulation. Conductivity modulation could further reduce R_{on}, however it is not a key

aim of the proposed SJ structure, due to the uncertainty that exists in the GaN literature

with respect to the lifetime of minority carriers in GaN [35][36][96].

5.3.3.3 Fabrication Considerations

The proposed SJ diode fabrication process is shown in Figure 5-10. There are key

issues regarding the proposed fabrication process:

(a) As the required pn pillar depth is above 5 μm, trench etching and selective

epitaxial regrowth are needed for making these patterned pn junctions. The approach

based on ion implantation is not suitable as it will greatly enhance the fabrication

complexity and costs. Due to the limited depth for pn junctions by ion implantation (~500 nm for an activation energy of ~500 keV), at least 5~10 multiple cycles of ion implantation and epitaxial regrowth are needed for the approach, which is not quite feasible.

(b) The selective epitaxial regrowth of p-GaN needs to satisfy three targets simultaneously: (i) complete trench filling for trenches with high aspect ratios; (ii) a N_A accurately matching the N_D in n-GaN; (iii) a good selectivity with no GaN deposition on the SiO$_2$ masks on top of n-GaN pillars.

(c) After the p-GaN regrowth, an additional p$^+$-GaN layer (300-500 nm, free hole concentration over 5×10^{17} cm^{-3}) should be regrown on top of SJ drift region, with Ohmic contact formed at the top p$^+$-GaN and bottom n$^+$-GaN layer, respectively.
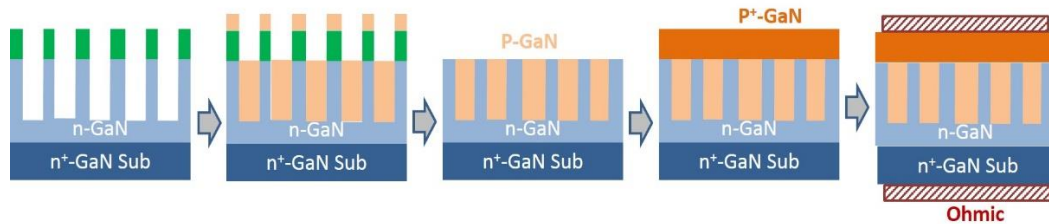
Figure 5-10 Main fabrication steps for a GaN vertical SJ diode. (The green regions represent SiO$_2$ masks for selective regrowth).

From the discussion above, it can be seen that the key process for the experimental demonstration lies in the p-GaN epitaxial regrowth. Especially, during the filling of deep trenches, possible GaN deposition at the edge of hard mask may shield the growth inside the n-GaN trenches, making it difficult to fully fill those trenches. This shielding effect

may be a serious issue especially for the filling of narrow and deep trenches required for the demonstration of SJ devices.

To solve this problem, we also propose to change the trench shape from rectangles to isosceles trapezoid, as shown in Figure 5-11. The trapezoid-shaped trenches are wider on the top, which could greatly mitigate the shielding effect. In order to keep a fully lateral charge depletion required for SJ devices, we would gradually increase the doping concentration in n-GaN while keeping a constant doping concentration in the regrown p-GaN. The donor concentration $N_D(y)$ in n-GaN at the depth y is designed following the relationship:

$$N_D(y) = \frac{w_p(y)}{w_n(y)} N_A \qquad (6)$$

where $w_p(y)$ and $w_n(y)$ are the designed width of n-GaN trench and n-GaN mesa at the depth y, as shown in Figure 5-11.
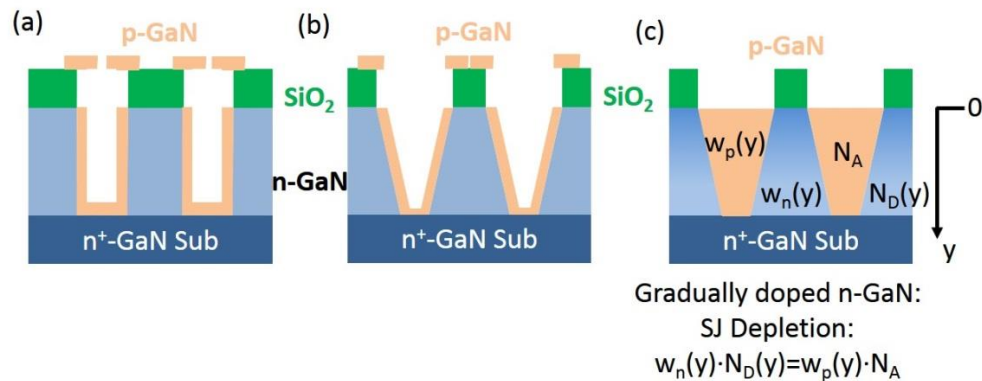
Figure 5-11 Schematics of (a) the shielding effect in narrow trenches, (b) p-GaN regrowth in trapezoid-shaped trenches and (c) design of SJ structures based on trapezoid-shaped trenches and gradually doped n-GaN mesas.

Based on all the fabrication considerations illustrated in this section 5, we are currently working on the experimental demonstration of patterned pn junctions by selective area etch and regrowth. Some of our preliminary experimental results will be discussed in section 5.4.2.

5.4 Preliminary Experimental Results

5.4.1 Patterned Ion Implantation and Junction-Barrier Schottky Diodes

In this section, we will present our preliminary experimental results for demonstrating JBS diodes based on two methods to form lateral pn grids. In the first method, p-wells were formed by Mg implantation into n-GaN, followed by symmetrical multi-cycle rapid thermal annealing (SMRTA) [83][90] for Mg activation at Naval Research Lab. In the second method, n-wells were formed by Si implantation into an epitaxial p-GaN layer. This approach allows for a single annealing at lower temperature for ion activation. In the preliminary results for the JBS rectifiers fabricated by the two methods, a *BV* of 500-600 V with low leakage current has been demonstrated, with a R_{on} of 1.5~2.5 m$\Omega\cdot$cm^2 for the Mg-implanted JBS rectifiers and 7~9 m$\Omega\cdot$cm^2 obtained for the Si-implanted JBS rectifiers.

Figure 5-12 (a) and (b) shows the structure of JBS rectifiers fabricated by Mg and Si implantation, respectively. A 7 μm-thick n-GaN layer with a N_{D} of 2×10^{16} cm^{-3} was grown by MOCVD on n$^+$-GaN substrates. In the structure shown in Figure 5-12 (b), a 0.5 μm-thick p-GaN layer with a doping concentration of 2×10^{18} cm^{-3} was grown on top of the n-GaN layer.

The device fabrication starts with a 1 μm-deep mesa isolation etch. Then a 1.5-μm-thick SiO_2 mask was selectively etched to define the implanted regions with widths ranging from 2 μm to 6.5 μm. Based on Monte Carlo simulations, four and five energies were designed for the Mg and Si implantation, respectively, to create a 0.6 μm-deep box-like profile with a total ion concentration of ~10^{19} cm^{-3}, as shown in Figure 5-12 (c) and (d).
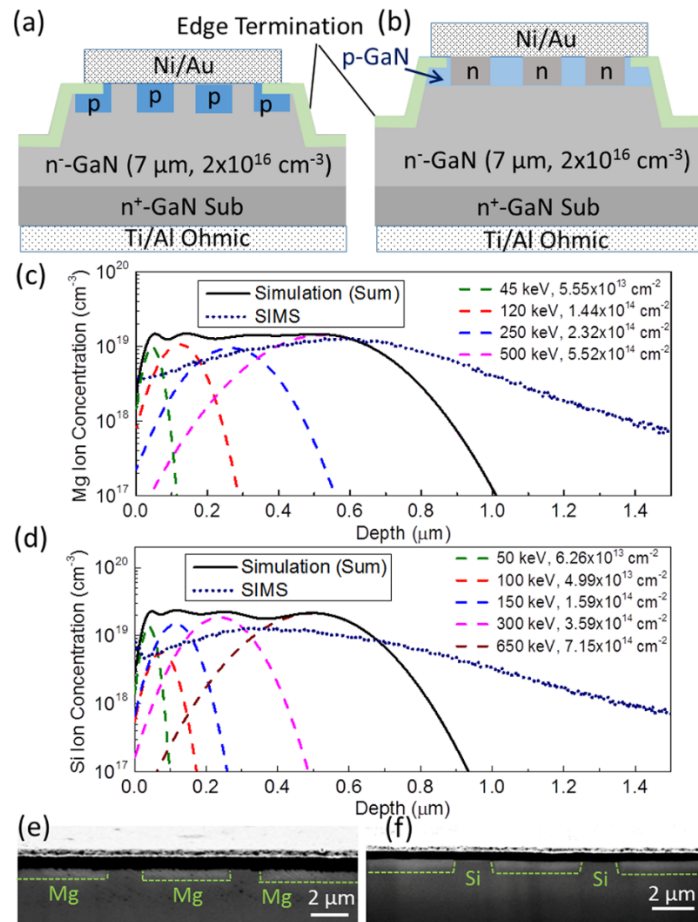
Figure 5-12 Schematic cross sections of the JBS rectifiers by (a) Mg implantation and (b) Si implantation. The simulated (c) Mg and (d) Si ion profiles as a function of depth, and the ion profiles after high-temperature activation measured by SIMS. The cross-sectional SEM images of the (e) Mg-implanted JBS structure and the (f) Si-implanted JBS structure.

After the implantation and SiO_2 removal, the Mg activation was performed by utilizing the SMRTA process with a sputtered AlN protection layer [83][97]. The annealing profile consisted of a 1000 ^{o}C anneal for 30 minutes, followed by 40 pulses of 20 seconds up to 1350 ^{o}C each, and another 1000 ^{o}C anneal for 30 minutes. The Si activation in a second wafer was performed by a standard RTA at 1050 ^{o}C for 2 minutes with a 100 nm SiO_2 cap layer. After activation and cap layer removal, the Si and Mg concentration profiles were measured by secondary ion mass spectrometry (SIMS). As shown in Figure 5-12 (c) and (d), the ion profiles form a long tail into n-GaN due to the ion diffusion at high temperatures, with a concentration of $5 \times 10^{18} \sim 10^{19}$ cm^{-3} within the 1-µm depth. This long tail and difference between experiment and simulation are believed to be due to the channeling effects. In the next batch of samples, the samples will be tilted during implantation, to reduce this channel effects.

The cross-sectional scanning electron microscopy (SEM) images of the Mg-implanted and Si-implanted JBS rectifiers are shown in Figure 5-12 (e) and (f), respectively. As shown, clear n-type and p-type grids have formed in both wafers. After ion activation, an edge termination was formed by Ar implantation with a dose of 1×10^{16} cm^{-2} and an energy of 150 keV, similar to our previous work [17][20]. The bottom Ohmic contact was formed by Ti/Al with a 550 ^{o}C annealing. Finally, a Ni/Au metal stack formed the top Schottky contact.

Besides JBS structures, vertical pn diodes and SBDs on non-implanted, Mg-implanted and Si-implanted areas, are also fabricated for references. The Ohmic contact

on p-GaN was formed by using Ni/Au metal stack followed by an annealing in N_2/O_2 gases, similarly to the fabrication processes described in Chapter 2.

In Mg-implanted wafers, rectifying behavior with a V_{on} of ~3.5 V was shown in Mg-implanted vertical pn diodes, as shown in Figure 5-13 (a). The formation of the rectifying behavior and the similar turn-on voltage to that in epitaxial pn diodes [18] demonstrate the successful p-type implant activation. In addition, these I-V curves are consistent to the best Mg-implanted pn diodes previously demonstrated by NRL by using the same annealing processes [83], [84]. The transmission line measurement (TLM) reveal a measureable hole conductivity, as shown in Figure 5-13 (b). A hole resistivity of ~290 $\Omega \cdot cm$ was extracted by utilizing the average R_{on} in the forward bias range of 2-5 V for the TLM patterns with different distances. The existence of a small turn-on voltage and imperfect linear I-V curves are due to the difficulties of forming perfect Ohmic contact on the p-GaN regions with low acceptor density. This hole resistivity value is also consistent with the reported values by NRL with similar annealing processes [83]. Electrochemical C-V measurements reveal a N_A concentration of ~5×10^{16} cm^{-3}. These results demonstrated the successful p-type implant activation.

Figure 5-13 (c) shows representative forward I-V characteristics and the extracted differential R_{on} for a conventional SBD and Mg-implanted JBS rectifier. The forward current is normalized by the total active device area (185×185 μm^2). A R_{on} of 0.65 $m\Omega \cdot cm^2$ and 1.7 $m\Omega \cdot cm^2$ is extracted for SBDs and Mg-implanted JBS rectifiers, respectively, at a forward bias of 2 V. The larger R_{on} of JBS rectifiers is due to two factor, as shown in the schematic of R_{on} components in Figure 5-13 (e): (i) larger channel

resistance (R_{ch}) due to the reduced n-GaN area for forward conduction; (ii) additional

spread resistance (R_{spread}) due to non-uniform current distribution.
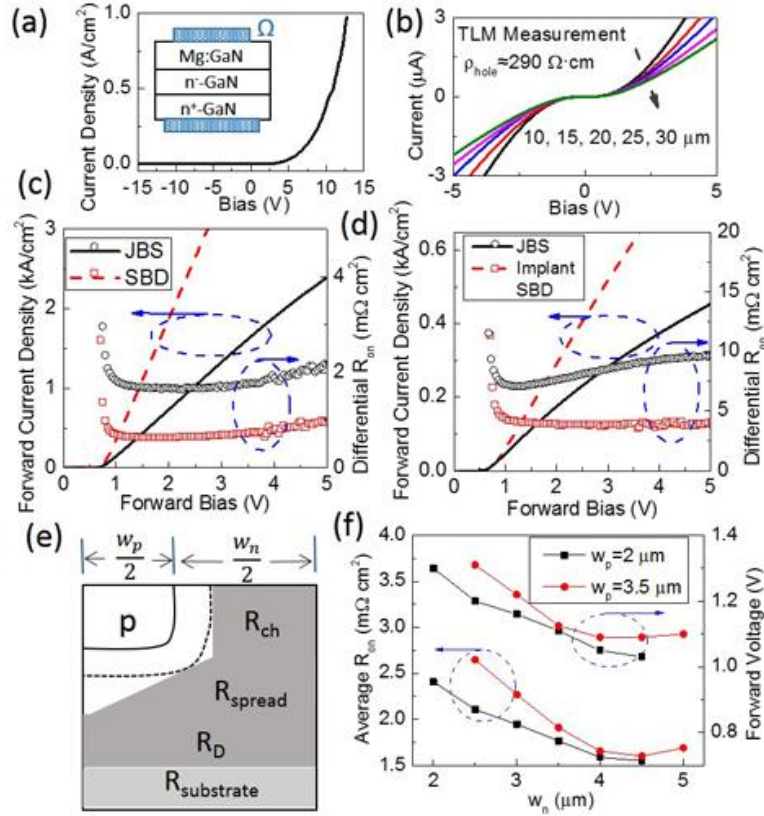
Figure 5-13 (a) *I-V* curve for the Mg-implanted pn diodes and (b) TLM measurements for the Ohmic

contacts formed on Mg-implanted regions. Forward *I-V* and differential R_{on} of (c) SBDs and Mg-implanted

JBS rectifiers, and of (d) Si-implanted SBDs and JBS rectifiers. The n-well and p-well widths are both 3

μm. (e) Schematic of R_{on} components in a JBS unit-cell. (f) The dependence of average R_{on} (in the bias

region from 0.7 to 5 V) and forward voltage (extracted at 100 A/cm^2) as a function of n-well and p-well

widths in Mg-implanted JBS rectifiers.

In Si-implanted wafers, electrochemical *C-V* measurements reveal a N_D

concentration of 5×10^{16}~10^{17} cm^{-3}, indicating the successful conversion from p-GaN into

n-GaN with an activation ratio of ~1%. This ratio is lower than other reports [85], [87],

[88], indicating room for further improvement. The atomic force microscope (AFM) images of the surface of as-grown p-GaN and Si-implanted p-GaN are shown in Figure 5-14 (a) and (b), respectively. As shown, the roughness is almost identical, indicating negligible surface damage by Si implantation.
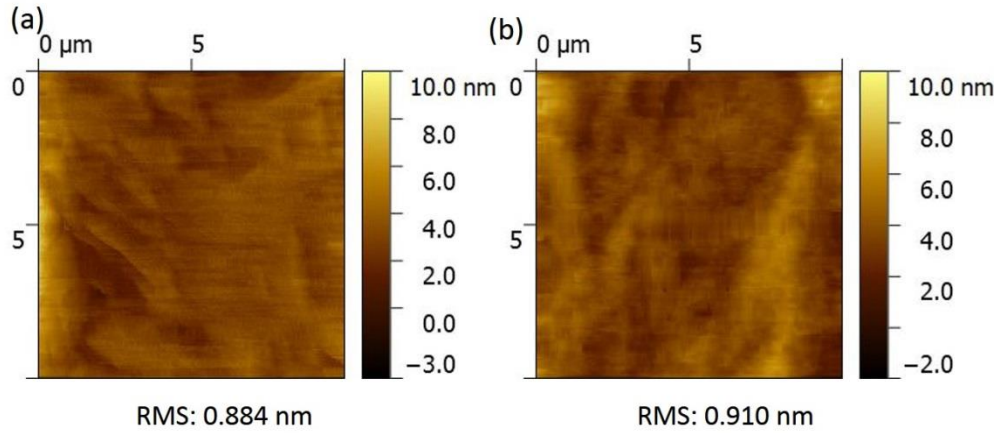
Figure 5-14 AFM images of a 10x10 μm^2 area of (a) p-GaN and (b) Si-implanted p-GaN.

Figure 5-13 (d) shows the forward characteristics of Si-implanted SBD and JBS rectifiers. The low V_{on}, 0.7 V, confirms the successful conversion of the Si implanted p-GaN into n-GaN. A R_{on} of 4 $m\Omega \cdot cm^2$ and 7.6 $m\Omega \cdot cm^2$ is extracted for Si-implanted SBDs and JBS rectifiers, respectively, at a forward bias of 2 V. The high R_{on} is due to the low mobility in the implanted region. An average vertical mobility of ~10 cm^2/Vs was estimated from the comparison of R_{on} of the Si-implanted SBDs and epitaxial SBDs, which can be further improved by reducing the channel effect as well as optimizing the implant dose and activation temperature [85]. Furthermore, a high I_{on}/I_{off} ratio of ~10^{10} was revealed for all the Si- and Mg-implanted JBS rectifiers.

As shown in Figure 5-13 (f), the R_{on} of JBS rectifiers was found to increase by decreasing the n-well width (w_n) and p-well width (w_p). w_n determines the R_{ch} and R_{spread}, as the n-wells contribute to forward conduction. w_p impacts the R_{on} mainly by changing the percentage of n-GaN region in the total device area. The forward voltage (V_F, extracted at a current of 100 A/cm^2) is 1.0~1.3 V for the Mg-implanted JBS rectifiers, which is lower than the GaN TMBS diodes and SiC SBDs [20].

Figure 5-14 (a) and (b) shows representative reverse *I-V* characteristics of SBDs, JBS rectifiers and p-SBDs (i.e. SBDs formed on a pn structure) in the Mg-implanted and Si-implanted wafers, respectively. In JBS rectifiers, the depletion layers from the lateral pn grids merge at relative low reverse voltage. Before this channel pinch-off, the leakage current behaves similarly to SBDs, dominated by thermionic field emission current of Schottky contacts (as illustrated in Section 4.4). After the pinch-off, a potential barrier is formed in the pn grids and the peak E-field moves away from the surface contact into the bulk GaN [98]. The leakage current deviates towards the bulk-limited behavior similar to that in pn diodes [19] and p-SBDs. Compared to SBDs, the JBS rectifiers have higher *BV*, from 300-400 V to 500-600 V, with $100\times$ lower leakage current at high bias.
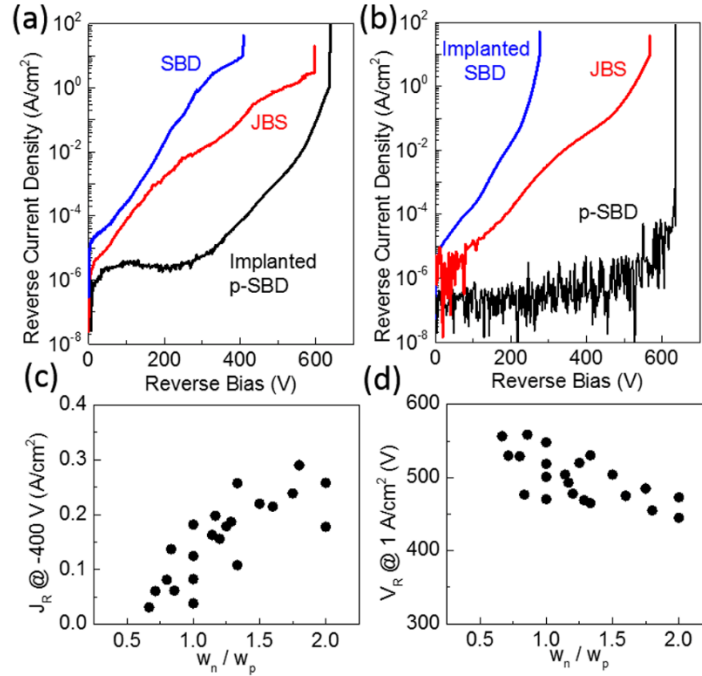
Figure 5-15 Reverse *I-V* characteristics of n-GaN SBDs, JBS and p-GaN SBDs in the (a) Mg-implanted wafer and (b) Si-implanted wafer. The w_n and w_p are both 3 μm. Dependence of the (c) reverse current density at -400 V and the (d) reverse bias reaching a leakage of 1 A/cm^2 on the w_n/w_p ratio, for 22 Mg-implanted JBS rectifiers with different w_n and w_p.

In JBS rectifiers, the extent of pn depletion and channel pinch-off is dependent on the relative amount of total acceptors and donors. For a given donor/acceptor concentration, this pinch-off extent would be dependent on the w_n/w_p ratio. As shown in Figure 5-14 (c) and (d), for a smaller w_n/w_p ratio, the leakage current at high reverse bias is statistically lower, and the soft '*BV*' extracted at a current compliance (1A/cm^2) is statistically higher (Most of the real device destructive *BVs* occur at higher biases at the Schottky contact edges). It should be noted that this modulation effect due to the w_n/w_p ratio is only valid when the p-type doping and n-type doping are in the similar levels. If the p-well is highly doped, like in Si and SiC JBS, the depletion is dominated by w_n [98].

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Figure 5-16 shows the reverse recovery characteristics of JBS diodes, SBDs and pn diodes The devices were switched from a forward current of ~400 A/cm^2 to pinch off with reverse voltages of 200 V (setup limits). As shown, the JBS diodes recovered equally fast as SBDs, much faster than pn diodes. This confirms that there is no minority carrier injection in our JBS diodes [61].
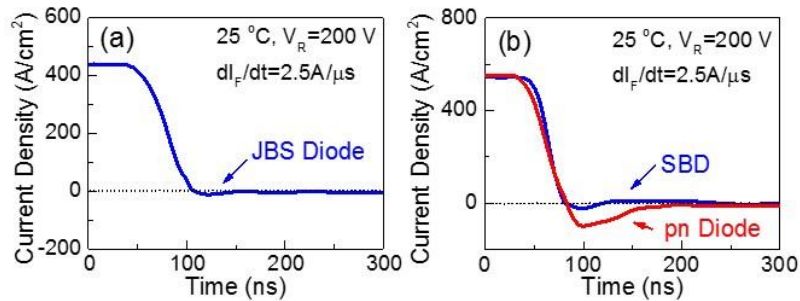
Figure 5-16 Representative reverse recovery characteristics of (a) JBS diodes as well as (b) SBDs and pn diodes, measured by an on-wafer pulser setup.

To benchmark the preliminary results of our JBS rectifiers, Figure 5-17 presents the R_{on} *v.s.* *BV* of GaN-based vertical Schottky diodes [7], [10], [11], [57]–[59], [99] [100]. The performance of our Mg-implanted JBS rectifiers is among the best in all vertical GaN Schottky diodes with $N_D > 10^{16}$ cm^{-3} in the drift region. A further reduction of N_D to ~10^{15} cm^{-3}, increase in p-GaN doping and the scaling of w_n and w_p could enhance the lateral depletion in pn grids, and therefore enable a better R_{on} *v.s.* *BV* trade-off in GaN JBS rectifiers.
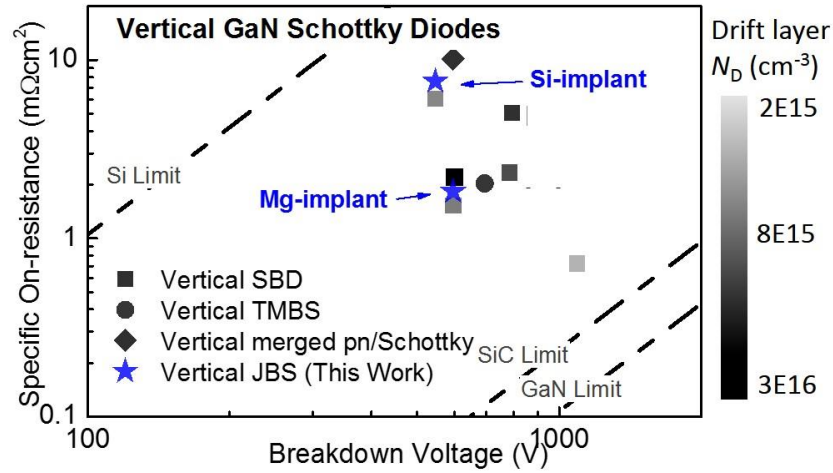
Figure 5-17 R_{on} *v.s.* *BV* of vertical GaN Schottky diodes demonstrated in this work and the ones in previous reports. The right bar shows the scale of N_D in the drift layers in the each benchmark device.

In summary, our vertical GaN JBS diodes have achieved significantly higher performance than the first demonstration reported in [90]. Specific R_{on} of 1.5-2.5 $m\Omega \cdot cm^2$ and 7-9 $m\Omega \cdot cm^2$ was obtained in the Mg-implanted and Si-implanted JBS rectifiers, respectively. A *BV* of 500-600 V was achieved in both devices, with a leakage current at high reverse biases at least 100-fold lower than conventional vertical GaN Schottky barrier diodes.

We are currently improving the fabrication of vertical GaN JBS diodes in several aspects:

(a) Optimize the implantation and activation conditions for Si-implanted JBS diodes, to reduce the channeling effects and improve the conductivity of Si-implanted regions in the vertical direction.

(b) Explore the possibilities of enhancing the p-type ion densities for Mg-implanted JBS diodes. Currently, the Mg-implanted p-wells are still lightly p$^-$-type. If p$^+$-

type is enabled, like in Si and SiC JBS diodes, a much stronger electric field modulation effect would be expected, resulting in further improvement in leakage current and *BV*.

(c) Lower the drift region carrier density from $N_D \sim 2 \times 10^{16}$ cm^{-3} to $10^{15} \sim 10^{16}$ cm^{-3}. This reduction of N_D could further reduce the total donors in a lateral pn junction and therefore enhance the depletion effects of p-wells. Meanwhile, the lower N_D could reduce the leakage current at the Schottky contact and increase the total sustained voltage in drift regions, resulting a further improvement in leakage current and *BV*.

5.4.2 Selective Area Etch and Regrowth

In last section, we introduced our preliminary results for making vertical pn junction based on ion implantation. Although successful demonstrations have been made, but it also shows the limitations of the ion implantation approaches, such as limited implanted depth, the need for high-temperature and complicated annealing schemes, etc.

In parallel to our works regarding ion implantation, we have been experimentally exploring the feasibility of utilizing the selective area etch and regrowth to demonstrate patterned pn junctions. In this section, we will describe our preliminary experimental results for selective area etch and regrowth.

The selective area etch was based on our optimized trench formation and corner rounding processes (discussed in detail in section 4.3). Before the deposition of Ni hard mask, a 40~50 nm SiO$_2$ was deposited by PECVD. This layer of SiO$_2$ will be selectively etched in the same mask for GaN etching, and the remaining SiO$_2$ on top of n-GaN pillars

will be used as the regrowth mask. A thicker Ni layer or a Ni/Au/Ni sandwich metal stack were used as the hard mask. The Ni/Au/Ni sandwich metal stack could reduce the intrinsic stress in the single Ni layer, enable a total thickness of Ni, and therefore sustain a longer dry etching. With this improvement of hard mask, the total etching depth can be increased from 2~3 μm to 6~7 μm (or even thicker) without any problems. After the optimized dry etching in an ICP-RIE system by using the Cl_2/BCl_3 gas combinations, the sample was treated in hot TMAH in an hour. It has been confirmed experimentally that the hot TMAH will not attack the SiO_2 layers on top of n-GaN pillars. Figure 5-18 shows the top-view optical microscopic images and SEMs images for the etched structures with an etch depth of ~4 μm. As shown, smooth etching sidewalls with uniform etching depth has been achieved.
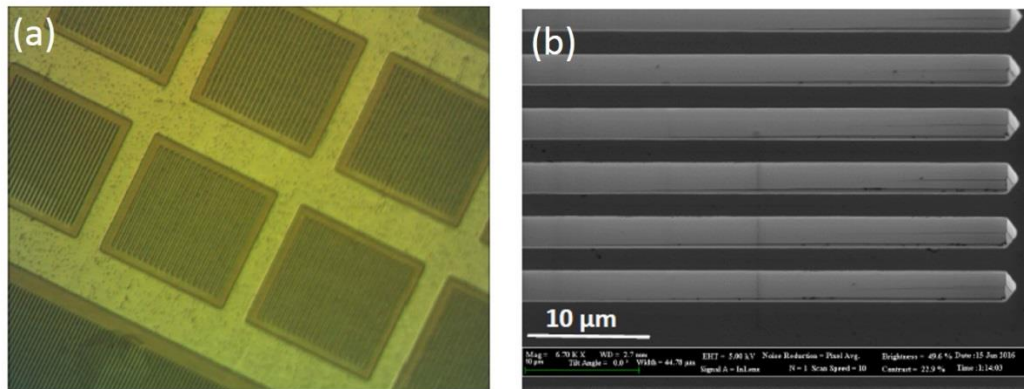
Figure 5-18 Top-view optical microscopic images and SEMs images for the etched structures

In collaboration with Prof. Nicolas Grandjeans' group at EPFL, we have studied p-GaN regrowth techniques by both MOCVD and MBE for over a year. As mentioned in sections 5.2.2 and 5.3.3, our target is to achieve four key properties of the filled p-GaN simultaneously: (a) complete trench filling; (b) significant growth selectivity; (c) a

perfect match of N_A in p-GaN and N_D in n-GaN; (d) no leakage current along the p/n regrowth interfaces. After continuous efforts, we can now fulfill the properties (a) and (b) simultaneously. Figure 5-19 (a) shows a cross-sectional SEM image for a successful p-GaN regrowth by MOCVD. As can be seen, the 2-μm-wide n-GaN trenches have been completely filled by p-GaN with a perfect regrowth selectivity (i.e. no GaN deposition on SiO_2 masks on top of n-GaN pillars). It should be noted that the p-GaN was intentionally overgrown for about ~2 μm, in order to develop processes to remove the overgrown p-GaN. By well-controlling the growth rate and growth time, the p-GaN overgrowth can be well controlled within ~100 nm.

With the demonstrated successful fulling of key properties (a) and (b), we are currently working towards to achieve the properties (c) and (d). In the MOCVD-regrowth shown in Figure 5-19 (a), the N_A was 10^{18}~10^{19} cm^{-3}, which is too high to match the N_D in n-GaN. In a separate non-patterned sample, we have calibrated the growth of p-GaN with a much lower N_A in the range of 10^{17}~10^{18} cm^{-3}. As for the properties (d), we are currently fabricating devices to characterize the leakage current of the structure. We will also characterize the material quality at the pn regrowth interface.
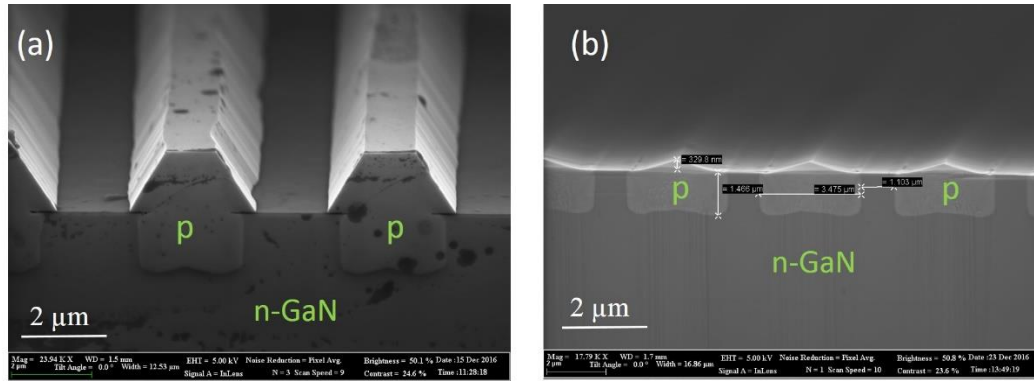
Figure 5-19 Cross-sectional SEM images for (a) vertical pn pillars right after p-GaN regrowth and (b) vertial pn pillars after an additional 6.5 hour hot TMAH treatment to remove the excess p-GaN on the top surface.

As mentioned, in the structure of Figure 5-19, the p-GaN was intentionally overgrown for about ~2 μm. This large overgrowth is to help develop processes to remove the overgrown p-GaN. As illustrated in sections 1.3 and 4.3, TMAH will slowly etch all GaN lattice planes except for the c-plan. Thus, we used TMAH treatment to remove the overgrown p-GaN. Also, as TMAH does not attack SiO_2, the n-GaN pillars will not be attached by TMAH. Figure 5-19 (b) shows the cross-sectional SEM images of the structure shown in Figure 5-19 (a) after 6.5 hour hot TMAH treatment. As shown, the over-growth p-GaN has almost been completely removed. These results demonstrated the validity of using TMAH hot treatment as a damage-free method to remove the overgrown p-GaN.

5.5 Conclusion and Prospect

A fundamental and significant challenge for GaN power devices is the lack of selective area doping, reliable and generally useable pn junction regions. Compared to Si

and SiC power device, this bottleneck becomes a fundamental limitation for high-voltage vertical GaN devices. GaN still lacks a viable selective area doping or selective area epitaxial regrowth process that yields material of sufficiently high quality to enable a defect-free p-n junction on patterned surfaces.

In this chapter, we presented our works towards solving this problem. We proposed and investigated two approaches to make patterned pn junctions: (a) laterally patterned ion implantation and activation, and (b) selective area etch and regrowth. Then we proposed two device structures that can be enabled by patterned pn junctions, including: (a) junction-barrier Schottky diodes / merged pn-Shottky diodes; and (b) super-junction devices. For vertical GaN super-junctions, we analyzed and derived the optimized relationship between the n/p-GaN doping concentration and the pillar width. Based on the optimized relationship, we further derived the design space of vertical GaN super-junction devices, and demonstrated their remarkable outperformance than conventional vertical GaN power devices in the *BV v.s. R_{on}* trade-offs and costs.

Besides designs and calculations, we have presented preliminary experimental results for different key technologies to making patterned pn junctions. For the approach (a), we have demonstrated the feasibility of making patterned pn junctions by two methods: p-type ion implantation into n-GaN and n-type ion implantation into p-GaN. The former method requires complicated annealing schemes for ion activation, but is typically not required to produce high free-hole density with high mobility (as p-GaN is typically not designed to contribute to the forward conduction in GaN power devices). The latter method requires much simpler annealing for ion activation, but is typically required to produce accurate free-electron or donor density with high mobility for free

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electrons. Vertical junction barrier Schottky rectifiers based on these two methods have been successfully demonstrated. A *BV* of 500-600 V was achieved in both devices, with a leakage current at high reverse biases at least 100-fold lower than conventional vertical GaN Schottky barrier diodes.

We also demonstrated our preliminary results for making patterned pn junctions by selective area etch and regrowth. For the selective area etch, we have demonstrated a deep etching process that can produce 5~6-µm-deep trenches with high aspect ratios and good sidewall qualities. With selective regrowth, we have demonstrated the successful p-GaN regrowth which can completely fill the trenches with no GaN deposition on the dielectric masks. We also developed a damage-free process which could remove the over-grown materials for surface planarization.

Looking forward, there is still a need for tremendous efforts to enable selective area doping, reliable and generally useable pn junction regions. The laterally patterned ion implantation and activation has not produced p-type regions or satisfactory pn junctions with high qualities equivalent to as-grown n-GaN or p-GaN. Some potential improvement proposals based on our preliminary results have been listed at the end of section 5.4.1.

For the other approach, there has been no report of successful fabrication of patterned pn junctions by selective area etch and regrowth. As mentioned in section 5.4.2, the key bottleneck is in the selective regrowth in the etched trenches, to achieve three key properties simultaneously: (a) complete trench filling; (b) significant growth selectivity; (c) no leakage current along the p/n regrowth interfaces.

To demonstrated vertical GaN superjunction devices, an additional requirement for the selective are regrowth is to achieve a perfect match of N_A in p-GaN and N_D in n-GaN.

This is challenging, but our preliminary results have revealed promising prospect to make the demonstration of vertical GaN superjunction devices happen. The vertical GaN superjunction devices could achieve at least $8\times$-$10\times$ lower R_{on} and at least 50%-60% lower epitaxial material cost for 1200 V power device. This performance would create tremendous new opportunities and make revolutionary changes for GaN power electronics.

Chapter 6 Conclusion and Future Work

6.1 Thesis Conclusion
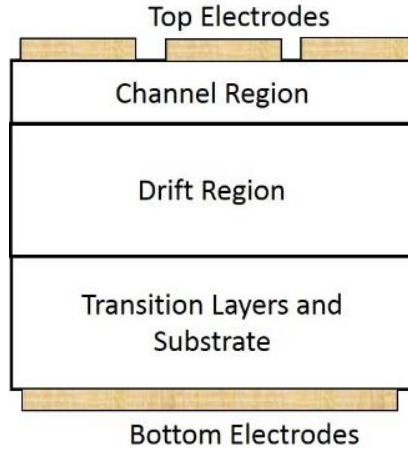
Figure 6-1 Schematics of the main components in a vertical GaN device.

This PhD thesis has tackled several major challenges in developing high-performance and low-cost vertical GaN power devices. The problems investigated in this thesis involve all the three key components in vertical GaN power devices: transition layers & substrate, drift region and channel regions, as shown in Figure 6-1.

First, we showed for the first time the feasibility of making vertical GaN power devices on Si substrates (Chapter 2). Vertical GaN-on-Si diodes have been demonstrated by utilizing either a quasi-vertical structure or a fully-vertical structure. The device physics for R_{on} and BV has been quantitatively studied by experiment and simulation. Key edge termination and sidewall treatment processes have been developed to reduce off-state leakage current. The impact of the doping concentration and thickness of each epitaxial layer on the device R_{on} and BV performance has been revealed. A BV over 500 V, a R_{on} below 1 m$\Omega \cdot$cm^2 with the capability of high-temperature (300 ^{o}C) operation and

fast switching was demonstrated for vertical GaN-on-Si diodes. This high performance shows the great potential of low-cost vertical GaN-on-Si devices for 600-V level high-current and high-power applications

Second, we unveiled the origin and design space of the off-state leakage current for vertical GaN diodes on different substrates (Chapter 3). Vertical GaN pn diodes were fabricated on Si, sapphire and GaN substrates and their leakage current mechanism was investigated by experiments, analytical study and TCAD simulations. We identified variable-range-hopping through threading dislocations as the main off-state leakage mechanism for GaN vertical diodes on different substrates. We also revealed a more general leakage current pattern for device with non-optimized fabrication processes or epitaxial growth. With a well-calibrated TCAD simulation, we derived the design space of leakage current in vertical GaN diodes, as a function of dislocation density and temperature. We demonstrated that the designed GaN vertical diodes can offer 2-4 orders of magnitude lower leakage while supporting 3-5 times higher electric field than GaN lateral, Si and SiC devices. This demonstrates great potential of GaN vertical devices for high-voltage and low-power-loss applications.

After the first two projects focused on the drift region and substrates, we expanded our effort to the channel region. We demonstrated a novel GaN vertical Schottky rectifier with trench MIS structures and trench field rings (Chapter 4). This novel vertical GaN rectifier is an advanced Schottky diodes without the need for p-GaN. The new structure greatly enhanced the reverse blocking characteristics of while maintaining a Schottky-like good forward conduction. The reverse leakage current improved by more than 10^4-fold and the *BV* increased from 400 V to 700 V, while the low turn-on voltage (0.8 V)

and R_{on} (2 m$\Omega\cdot$cm^2) were retained. High-temperature operation up to 250 $^{\text{o}}$C and fast switching performance were also demonstrated. This new device shows great potential for high-power and high-frequency applications. Besides, in the fabrication of this novel device, we developed an optimized trench formation and corner rounding processes, which are the key processes to demonstrate high-voltage trench-based vertical GaN diodes and transistors.

In the last chapter of this thesis, we concentrated on tackling a fundamental and significant challenge for GaN power devices: the lack of reliable and generally useable patterned pn junctions. We proposed and investigated two approaches to make patterned pn junctions: (a) laterally patterned ion implantation and activation, and (b) selective area etch and regrowth. Then we proposed two device structures that can be enabled by patterned pn junctions, including: (a) junction-barrier Schottky diodes / merged pn-Shottky diodes; and (b) super-junction devices. We calculated the optimized structure and derived the design space of vertical GaN super-junction devices, and demonstrated their remarkable outperformance than conventional vertical GaN power devices in the *BV v.s.* R_{on} trade-offs and costs. In addition, we presented our preliminary experimental results for the two approaches for making patterned pn junctions. Vertical junction barrier Schottky rectifiers based on the patterned pn junctions by ion implantation and activation have been successfully demonstrated. A *BV* of 500-600 V was achieved in both devices, with a leakage current at high reverse biases at least 100-fold lower than conventional vertical GaN Schottky barrier diodes. Finally, we demonstrated our preliminary results for making patterned pn junctions by selective area etch and regrowth. The preliminary results show the promising prospect to demonstrate vertical GaN super-junction devices.

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6.2 Future Work

Ideas for future work have been included in the last section of each chapter. Here, we summarize these future works into the three main components of vertical GaN power devices, and briefly listed all the key problems that need to be solved to enable the commercialization of vertical GaN power devices for 1200 V and even higher voltage classes power applications.

- **Channel Regions**:

    (1) For diodes: the *BV* of advanced Schottky diodes needs to be pushed to beyond 1200 V or even higher, in order to compete the SiC Schottky barrier diodes that have been successfully commercialized;

    (2) For transistors: a careful selection needs to be made for the channel structures between 2DEG, MOS channel and bulk-material channel (such as fin structures). The winning channel structure should have high mobility, high carrier density and easy configurations to enable normally-off operation.

    (3) An effective and reliable approach needs to be developed to enable the selective area doping, reliable and generally useable pn junction regions. Viable GaN selective area doping or selective area epitaxial regrowth process need to be improved to yield material of sufficiently high quality and to enable a defect-free p-n junction on patterned surfaces.

    (4) Edge termination structures need to be designed and demonstrated for GaN devices to enable avalanche breakdown in advanced Schottky rectifiers and

vertical transistors. Optimized edge termination structures, such as junction termination extension (JTE) structures and multiple field rings, are the key for SiC power devices to achieve a high BV over 10 kV. However, there has been no good demonstrations for vertical GaN devices. This situation can also be attributed to the lack of usable patterned pn junctions on patterned surfaces.

- **Drift Regions**:

  (1) Dislocation density needs to be further reduced. From our works presented in Chapter 3, it can be seen that the off-state leakage current at high reverse biases are largely dependent on the dislocation density in the drift region. A reduction of dislocation density could greatly reduce the off-state leakage, enhance the robustness of BV and further improve the device reliability. A dislocation density reduction by 2~3 orders of magnitude in GaN-on-Si structures could enable the vertical GaN-on-Si power devices to have a comparable leakage current level to GaN-on-GaN power devices.

  (2) For the demonstration of even higher BV (e.g. above 5000 V), carrier density in the drift regions need to be at least reduced to 10^{14}~10^{15} cm^{-3}. From Chapter 3, we have seen that a reduction of carrier density from 3×10^{16} cm^{-3} to 10^{16} cm^{-3} could bring a significant increase of BV. From the literature data presented in Chapter 5, we have seen that a reduction of carrier density from 2×10^{16} cm^{-3} to 2×10^{15} cm^{-3} could enable a reduction of off-state leakage current by 3~4 orders of magnitude in vertical GaN

Schottky diodes. Thus, the reduction of carrier density to $10^{14} \sim 10^{15}$ cm^{-3}, comparable to the one in state-of-the-art SiC power devices ($10^{13} \sim 10^{15}$ cm^{-3}), is the key to demonstrate vertical GaN devices at 5000-50,000 V voltage classes.

(3) Demonstration of vertical super-junction structures to replace the conventional lightly-doped drift region. As illustrated in Chapter 5, the vertical GaN superjunction drift region could achieve at least $8\times$-$10\times$ lower R_{on} and at least 50%-60% lower epitaxial material cost for 1200 V power device, with even greater outperformance for higher voltage devices. This performance would create tremendous new opportunities and make revolutionary changes for GaN power electronics.

- **Substrates:**

(1) Large diameter GaN substrates with lower costs. Currently, mainstream SiC substrates are 4-inch with a price around $600. 6-inch SiC substrates are also available at much higher prices. The mainstream GaN substrates are 2-inch with the lowest prices around $1000. 4-inch GaN substrates are also available in small volumes. In order to compete the cost of SiC power devices, the larger diameter GaN substrates with similar price to SiC substrates need to be enabled.

(2) High-performance vertical GaN substrates on low-cost Si substrates. The vertical GaN-on-Si power devices for the 600-1200 V applications with high-current and high-power capability need to be demonstrated. These high-

performance 600-1200 V GaN-on-Si power devices, if demonstrated, are expected to have a great cost and performance advantages than SiC power devices and have a higher current and power handling capability than GaN lateral devices.

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