Losses in Polysilicon Waveguides

by

Marcie R. Black

Submitted to the Department of Electrical Engineering and Computer Science in Partial Fulfillment of the Requirements for the degree of Master of Engineering in Electrical Engineering and Computer Science

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Abstract

Polysilicon waveguides are evaluated for optoelectronic interconnection. Losses are found to be the major limitation to the implementation of polysilicon waveguides. The major causes of loss are determined to be grain boundary absorption or scattering and the surface roughness scattering. We have demonstrated experimentally that losses can brought down from 77 dB/cm to 33dB/cm by modifying surface roughness and grain structure. As a consequence of our findings, we predict that losses of less than 10dB/cm can be achieved for small grained, smooth, hydrogenated polysilicon waveguides.

Thesis Supervisor: L. C. Kimerling
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Chapter 1

INTRODUCTION

Integrated Circuit technology is being pushed to its physical limits. Clock frequencies are expected to reach the GHz region by 2007. At that time, RCL delays are required to meet standards of 50 picoseconds. Current electrical technology can not meet the rising clock trends. The propagation delay from one logic element to another is already larger than the gate delay, so decreases in the logic speed alone can not solve the problem. In addition, the interconnection density, if current technologies are used, will be required to reach 2B lines/cm^2. Not only is such high interconnection density challenging to fabricate, but electromigration will cause reliability constraints. High interconnection density also increases the chance of cross talk, signals interfering with each other between wires. Further more, with current technologies, the power per chip is expected to reach 200 W, which will cause problems in cooling and energy conservation[1]. New technologies need to be investigated. Optoelectronic interconnection can help overcome these challenges.

"There is little doubt that as computational-bandwidth demands increase, optical interconnections will replace certain metallic interconnections"[2]. Electronics and photonics are different even on the most fundamental levels. For example, electrons interact strongly with one another while photons interact only weakly. The differences between electrons and photons cause one technology to have applications in which it out performs the other. Because electrons interact strongly, they are very well suited for logic circuits where one signal must control another. Electrical technology is also very well suited to carry power. On the other hand, optical technology has low losses and high bandwidths, and therefore it

is more appropriate for information transfer and interconnection. A system that combines these technologies can have both high bandwidth interconnection and high speed logic.

In order to utilize the advantages of both electronics and photonics, the industry needs a system which takes an electrical signal, converts it to optics for transport, and then converts it back again into an electrical signal when logic is needed. In this way, all logic can be done with electronics, while interconnection is done with photonics. Among other advantages, this system would greatly minimize the problem of skew (registers receiving the clock signal at different times). The design must account for skew, effectively reducing the maximum speed of the clock. Multiplexing (sending many signals down the same wire) can be combined with optical interconnection to ease both the interconnection density and skew problems. The Fanout System combines photonics and electronics by sending one clock signal down a waveguide and then spliting it into many signals. Distributing clock signals in this fashion allows detectors distributed throughout the chip to receive clock signals with minimal skew and less required interconnection.

Not only does optoelectronic interconnection offer high speeds and minimal skew, but it also limits crosstalk. Crosstalk limits the spacing between wires because signals from one wire interfere with signals on other nearby wires. In fact coaxial designs are being proposed to minimize crosstalk. Optical waveguides on the other hand can be placed closer together than parallel conductors without one signal interfering with each other. If communication between waveguides is desired, crosstalk can be increased by modifying the waveguide design.

The advantages of using waveguides to carry signals include the fact that optical waveguide transmission is independent of bandwidth. Therefore, not only can waveguides make use of temporal multiplexing like wires, but they also can incorporate wavelength

division multiplexing. In this way many signals can be sent down the waveguide at different wavelengths and not interfere with each other.

Another advantage of light over electricity, which is often not mentioned, is that the waveguide does not need to touch the detector in order for light to be detected, hence allowing moving parts, or even replaceable parts, in the optoelectronic system[3]. For all these reasons and many others, optoelectronic integration is necessary to eliminate the communication bottleneck on integrated circuits.

Since the majority of integrated circuits are made from silicon, the optoelectronic system requires a detector, emitter, and waveguide compatible with silicon technology. Polysilicon waveguides satisfy these criteria. In addition, since silicon waveguides have a high index contrast, their bending losses are low and sharper turns can be designed. These waveguides also have very little crosstalk with the standard strip design, but can be designed with large crosstalk for applications which desire crosstalk, such as coupling by using the rib design (Section 1.1). In addition, silicon waveguides have a similar index of refraction to the proposed detector and emitter which greatly reduces coupling losses at the beginning and end of the waveguide.

Polysilicon waveguides have these advantages plus others which single crystalline waveguides do not. For polysilicon waveguides, the designer has complete control of where the waveguides go on the wafer. These waveguides can easily be designed to travel up and down layers with as many layers as desired. The designer therefore has the option to work in three dimensions. Furthermore, polysilicon waveguide technology satisfies the important requirement that the technology must be low cost and compact. Polysilicon is a promising waveguide material and therefore is chosen for investigation in this thesis.

Information needed to understand polysilicon waveguides is reviewed in the next section, including waveguide fundamentals, types of waveguides, loss mechanisms, and materials issues. This thesis concentrates on surface roughness as a loss mechanism, and begins exploration of other loss mechanisms.

Chapter 2

BACKGROUND

2.1 Waveguide Fundamentals

2.1.1 Basic Optics:

An optical waveguide consists of a core and a cladding. The core has a higher index of refraction than the cladding, so light remains in the core. The cladding ensures that the light is not scattered to the outside air by reducing the core-air index contrast.

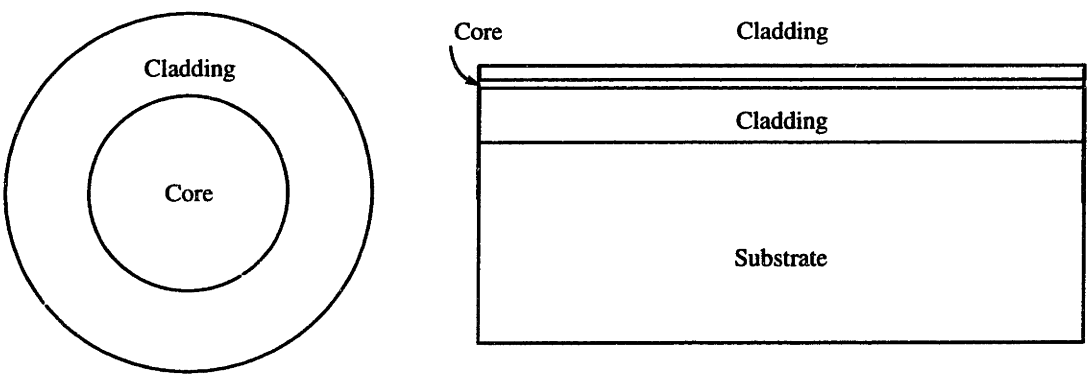


Figure 2.1: Picture of an optical fiber waveguide and a planar optical waveguide. Both structures make use of the index of refraction difference between the core and the cladding to confine light inside the core.

When light in a high index media encounters a border with a lower index media some light is reflected and some is transmitted (Figure 2.2 a). If however the light is incident at an angle smaller than the critical angle, all of the light is reflected, and total internal reflection occurs.

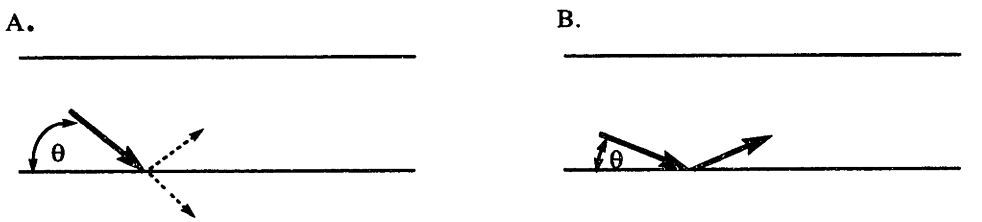


Figure 2.2: A. shows normal reflection. Only some of the light is reflected and some is transmitted. B. shows total internal reflection.

Light in the waveguide is usually confined within the core by total internal reflection between the cladding and the core. The larger the index contrast the larger the critical angle.

Two types of polysilicon waveguides are considered. Figure 2.3 shows the cross sections for a single mode strip and rib guide. These waveguides are designed for the core to be silicon and the cladding to be oxide and air. The waveguide design is based on operation at 1.54μm.

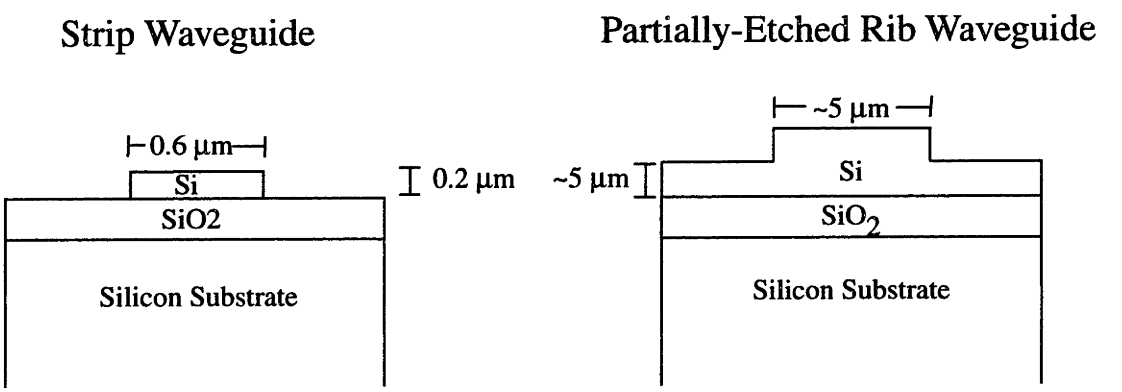


Figure 2.3: The two types of waveguides considered for silicon electric-optic applications is shown. The dimensions for both these waveguides are for single mode operation.

Rib and strip waveguides are optimal for different applications. Strip waveguides are smaller, have lower bending losses, and less crosstalk. Rib waveguides make ideal cou-

plers since waveguides close together interfere with each other. Rib waveguides also have the advantage that they are larger, so coupling light into them is easier. All waveguides tested in this thesis are multimode strip waveguides, but the final system will be single mode either rib or strip.

2.1.2 Solving the Silicon-Silicon Dioxide Waveguide:

For the waveguides used in this thesis, the core is silicon and the cladding is oxide. The index of refraction of silicon and oxide at 1.54μm are 3.5 and 1.5, respectively is a large index contrast allows total internal reflection to occur over a large range of incident angles. Since the index of refraction in silicon is large, the waveguides can be made as small as 0.6μm, but for ease of coupling they have a width of 8μm and a thickness of 1μm.

The field inside the waveguide is a combination of the incident and reflected field. If these fields are out of phase with each other, they will interfere to form a field profile such as the one shown below.

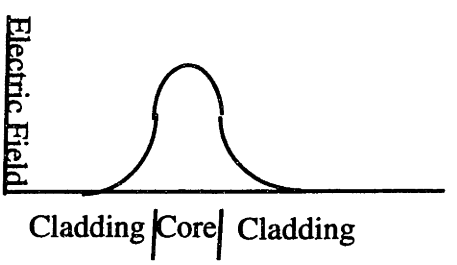


Figure 2.4: The electric field profile for the fundamental mode is shown.

At the boundary between the core and the cladding, Maxwell's equations require the power distribution to be both continuous and smooth. These two requirements allow for only certain field distributions in the waveguide. Each allowed distribution is called a

mode.

For monochromatic light, the photon energy is independent of mode. However, the higher the mode, the less energy in the direction of propagation, so the slower the wave travels. Since the photon's energy in the direction of propagation is less, the energy must be higher in one of the confined directions. Since energy is related to the second derivative of the field, the higher the photon's energy in the confined directions, the greater the number of times the waveguide power distribution passes through zero.

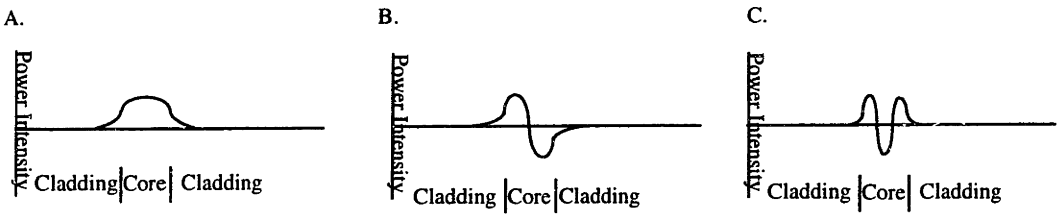


Figure 2.5: Picture of the electric field distribution for the first three modes. The higher the mode, the more zeros occur.

The number of modes can be found by calculating the number of zeros allowed for a given photon energy. First, all the photon energy is placed in a confined dimension. This energy corresponds to a given wavelength. The number of half wavelengths that fit into the thickness of the waveguide is approximately the number of modes allowed. The energy of a photon of wavelength 1.54μm is 0.805 eV, corresponds to a wavelength of 1.54μm/3.5 or 0.44 μm in silicon. For a thickness of 1μm, four half wavelengths are allowed so about four modes are allowed. In the other confined direction for 8μm around 36 modes are allowed.

The number of half wavelengths that fit into the thickness of the waveguide is only an approximation since the calculation does not account for the field slightly extending into

the cladding. (See Figure 2.5). Even with total internal reflection, power is distributed inside the cladding (see Figure 2.4). The field in the cladding forms an evanescent wave where no power travels towards or away from the core. The distance the electric field is distributed into the cladding is referred to as the penetration depth. The larger the index of refraction contrast between the core and cladding, the smaller the penetration depth and the better the confinement of the mode. The higher the mode, the larger the penetration depth.

For the case where z is the direction of propagation, x is the direction of confinement, and the y-direction is unconfined, the TE (transverse electric) field can be defined as:

$$E_y(x) = \begin{cases} A \bullet e^{-qx} & 0 \le x \le \infty \\ B \bullet (\cos(hx) + C \cdot \sin(hx)) & -t_g \le x \le 0 \\ D \bullet e^{p \cdot (x + t_g)} & -\infty \le x \le -t_g \end{cases} \tag{2.1}$$

where t_g is the thickness of the waveguide. q and p are the penetration depths of the top and bottom oxide respectively. h, q, and p can be determined simultaneously by solving the four transcendental equations which relate them to β the propagation coefficient.

$$\begin{aligned} q &= \left(\beta^2 - n_1^2 k^2\right)^{1/2} \\ h &= \left(n_2^2 k^2 - \beta^2\right)^{1/2} \\ p &= \left(\beta^2 - n_2^2 k^2\right)^{1/2} \\ k &\equiv \omega / c \\ \tan(ht_g) &= \frac{p+q}{h(1 - (pq)/h^2)} \end{aligned} \tag{2.2}$$

where n_1, n_3, and n_2 are the index of refraction of the top oxide, bottom oxide, and silicon respectively.

For the waveguides in this thesis, the fundamental mode has a solution of $p = q =$ 13.0031 μm^{-1}, $h = 3.0035\ \mu m^{-1}$, and $\beta = 14.37\ \mu m^{-1}$. Using these values and the relation

$h/\beta = \tan(\Theta)$ Θ_m, the angle shown in Figure 2.6 and 2.2, can be found. Θ_m for the fundamental mode is found to be 11.8°.

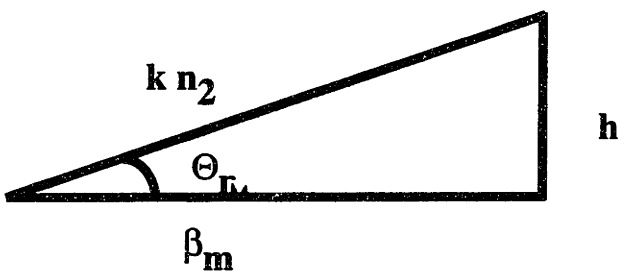


Figure 2.6: The relationships between *h, k,* Θ, and β are shown. $(kn_2)^2$ is proportional to the total energy of the photon, β_m^2 to the energy distributed in the *z* direction, and h^2 in energy in the direction of confinement. Since the total energy must equal the sum of the energy in all directions, a right triangle is a connivent conceptual tool to understanding the relationship between *h, k,* Θ, and β.

2.1.3 A Measure of Loss

Waveguides have many types of loss. Most of these losses result in an exponential decay of the power in the waveguide and can therefore be lumped together with one characteristic length.

$$P(z) = P_o e^{-x\alpha}$$
$$P(z) = P_o 10^{-Ax} \qquad (2.3)$$

The effective length can be expressed by either on a natural base or base 10 function. In equation 2.3 both of the common ways of expressing the exponential loss are shown. *P* is the power in the waveguide as a function of the direction of propagation. P_o is the power of the waveguide when $z = 0$. α and *A* are the time constants when natural base and base 10 are used respectively. α is commonly referred to as the absorption constant. *A* is in

units of 0.1 * dB/distance. From equation 2.3, α is related to A by a factor of ln(10). Therefore α is converted into dB/cm by multiplying by 1n(10)/10. Different waveguides have different measures of absorption (dB/cm). Some of the more common waveguides are investigated in the next section.

2.2 Waveguide Types

Many research groups work on optical waveguides. Below are some of the types of waveguides investigated.

2.2.1 Single Crystal Silicon Waveguides Fabricated Using Bond and Etch Back Silicon on Insulator Technology:

Bond and Etch Back Silicon on Insulator (BESOI) is a technique that allows a Si-SiO_2-Si structure. This process takes two wafers. On one wafer an oxide is grown. On the second wafer, boron is implanted in a buried layer. These two wafers are then bonded together and the back side of the second wafer is grounded and then chemically etched. The p+ silicon layer acts as an etch stop to control the thickness of the silicon layer.

BESOI waveguides have the advantage that they made from silicon of high perfection and that the losses are lower than 1 dB/cm[4]. However, BESOI has many disadvantages: BESOI is costly and fabrication of more than one layer is difficult. In addition, these waveguides take up valuable active area of the silicon. In BESOI, the thickness of the top silicon layer is limited to about 5000A with the uniformity across the wafer determined by the etch back process.

2.2.2 Single Crystal Silicon Waveguides Fabricated Using Separation by Implantation of Oxygen Technology:

Separation by Implantation of Oxygen (SIMOX) is a candidate for future integrated circuit technology, and therefore for silicon waveguides. This process is cheaper than BESOI, but more expensive than polysilicon waveguides. SIMOX implants oxygen at very high doses into a silicon wafer. The wafer is then annealed and a buried layer of oxide is formed underneath a thin single crystalline region. SIMOX waveguides have similar disadvantages to BESOI waveguides. These waveguides are costly, take up valuable active area, are limited to one layer, and these dimensions limit critical waveguide parameters. In SIMOX waveguides the oxide layer is very thin and is may not to prevent losses to the substrate.

2.2.3 Silicon Nitride/SiO_2

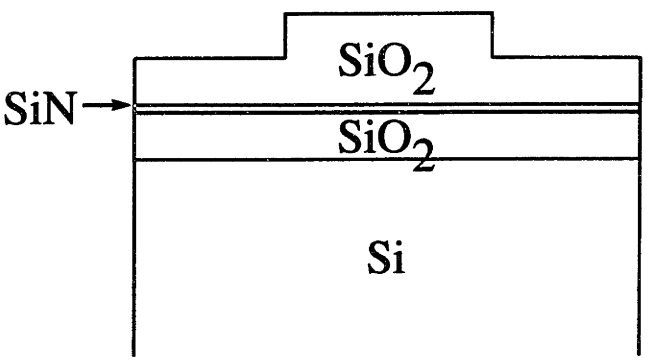


Figure 2.7: Type of waveguide used by others. Light is confined inside the oxide.

Some waveguides are made with a silicon nitride core. The silicon nitride has a different index of refraction than the silicon dioxide, so optical confinement occurs. This type of waveguide has the advantages that it is compatible with silicon technology and has low losses, but may not be ideal for optoelectronic interconnections. Since the detector proba-

bly will be made from silicon and/or germanium and the emitter from silicon, the index contrast between these components and the waveguide is large. (Silicon's index of refraction is 3.5 and silicon oxynitride has an index of refraction around 1.7 [5].) This large index of refraction contrast creates extra reflections at the ends of the waveguide, which will then require a lower detection limit of the detector or a higher emitter power. Also in these waveguides, since the core and the cladding have only slightly different indexes of refraction, the cladding must be thick in order to prevent loss to the substrate. Cladding layers of 15 μm are often used for this purpose[1]. In addition, these waveguides have weak lateral confinement requiring wider waveguides.Waveguides of this type have been fabricated with losses less than 0.1 dB/cm at 0.633μm[5].

2.2.4 Doping to Modify the Effective Index:

The free carrier effect can modify the index of refraction of silicon. The change in index of refraction is related to the increased electron concentration by the equation 2.4 and increased hole concentration by equation 2.5.

$$\Delta n = -3.499 \cdot 10^{-21} \Delta N_e^{\,1.0228} \tag{2.4}$$

$$\Delta n = -5.369 \cdot 10^{-18} \Delta N_h^{\,0.80866} \tag{2.5}$$

Δn is the change in the index of refraction and ΔN_e and ΔN_h are the change in electron and hole concentrations respectively. Doped silicon can be combined with silicon to create a waveguide. These waveguides have low index contrast and therefore have high bending

losses. In addition, they can't be placed close together because of the large penetration depth. Doping not only changes the index of refraction, but it also causes free carrier absorption. Waveguide losses of 5-13 dB/cm have been measured at 1.3 μm on doped silicon waveguides[6].

2.2.5 Arrow (Anti-Resonant Reflecting Optical Waveguide (Si-oxide-Polysilicon-oxide-air:)

The cross section of an arrow waveguide is shown below:

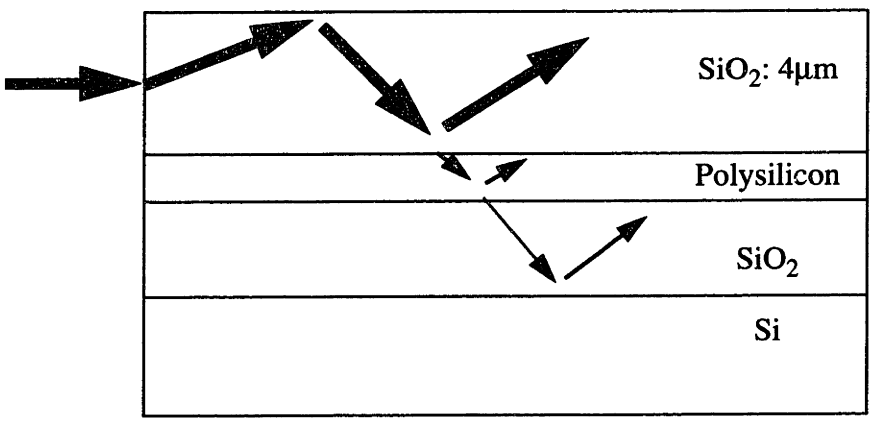


Figure 2.8: Arrow waveguide. Light is confined by total internal reflection from the top interface and interference from the lower surfaces.

In this waveguide, the light is confined in the top oxide. The oxide-air interface provides total internal reflection while the oxide-polysilicon-oxide interference provides confinement through interference. This method has losses as low as 0.4 dB/cm for the TE mode and losses of 60 dB/cm for the TM mode[7]. This waveguide therefore, offers good polarization selectivity. Since ARROW waveguides require an oxide - air interface, more than one layer may not be possible. Another challenge is to make non-planar ARROW waveguides since they would require layers at arbitrary angles.

2.2.6 Si 1-x Gex/Si

Germanium is sometimes mixed with silicon to increase the index of refraction. The engineering challenge here is to lattice match the materials. Lattice mismatch induced strain limits the layer thickness and introduces defects. If the defect density is large enough, the structure no longer is single cyrstalline.

2.2.7 Polysilicon Waveguides:

All waveguides fabricated for this thesis are polysilicon waveguides. The structure for these waveguides is very similar to the BESOI and SIMOX waveguides, except the guiding layer is polysilicon instead of single crystalline silicon.

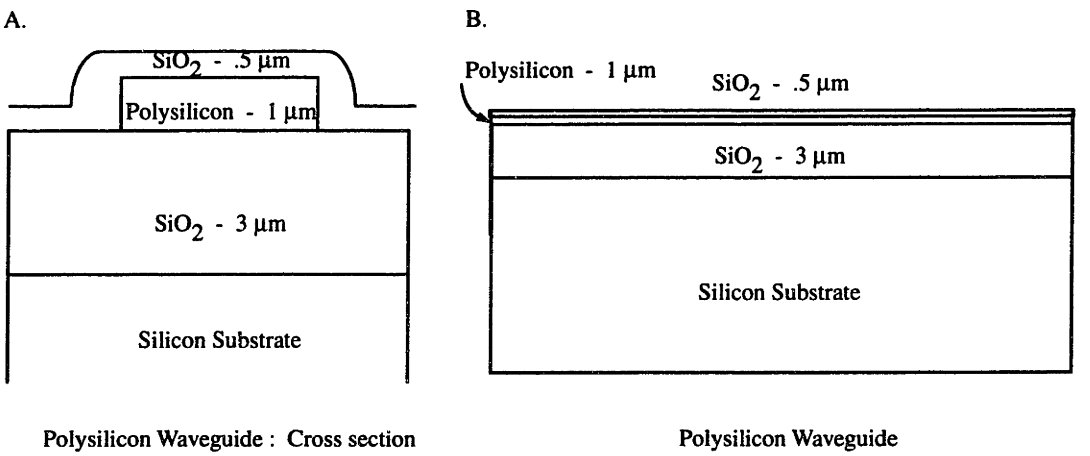


Figure 2.9: A. The cross section of the polysilicon waveguides fabricated in this thesis. B. The sideview of a polysilicon waveguide.

If these waveguides were to be made usable, optoelectronic interconnection will have made a great jump forward. Like BESOI and SIMOX, polysilicon waveguides are com-

patible with current silicon technology. However, polysilicon is easier and less expensive to manufacture than both these types of waveguides. To make these waveguides the oxide is grown and the polysilicon is deposited on top. Oxide growth and polysilicon deposition are common and comparably cheap processes. Unlike BESOI and SIMOX, the designer has complete control over all the critical parameters of the polysilicon waveguides. In BESOI waveguides the top layer of silicon can only reach a minimum thickness of about 5000A and in SIMOX waveguides the oxide is very thin so light is lost to the substrate.

Many advantages to polysilicon waveguides are unique. Since oxide can be grown or deposited at varying thickness, the waveguides can easily be fabricated in three dimensions allowing for layers of waveguides that can communicate together. BESOI and SIMOX would only allow for waveguides along one plane. Secondly, the complete freedom to place these waveguides anywhere on the wafer allows the designer to maintain valuable active area for electronics. Lastly, if polysilicon is determined to be an ideal waveguide material, a key factor to its successes will be the similarities to existing interconnection technology. Designers, therefore, will not need to modify their way of thinking.

Polysilicon does have a disadvantage. Measures of the losses in polysilicon can be as high as 1000 dB/cm[8], and our original measured losses were 80 dB/cm. This loss is equivalently 10^{-6}% of the original power after one centimeter. BESOI waveguides, on the other hand have losses of 1 dB/cm, or an equivalent of 80% of the original power after one centimeter. This thesis begins to bring the losses closer to a usable value required for optoelectronic integration.

2.3 Isolating the losses

As mentioned our first measured polysilicon waveguides had losses of 80 dB/cm compared to the BESOI waveguides which had losses lower than 1 dB/cm. In order for polysilicon waveguides to be usable for optoelectronic interconnection, the main causes for losses must be determined and then minimized. Many possible causes of losses in a waveguide exist. Of these causes of loss, scattering from roughness is determined and grain boundary related losses are investigated. Of the remaining loss mechanisms, some can be easily eliminated as a major cause of loss in polysilicon. while the rest are left for future work to explore.

2.3.1 Scattering Due to Surface Roughness

The surface on top of the waveguide which is either an interface between polysilicon and air or polysilicon and the overlaying oxide layer is often rough in polysilicon waveguides.

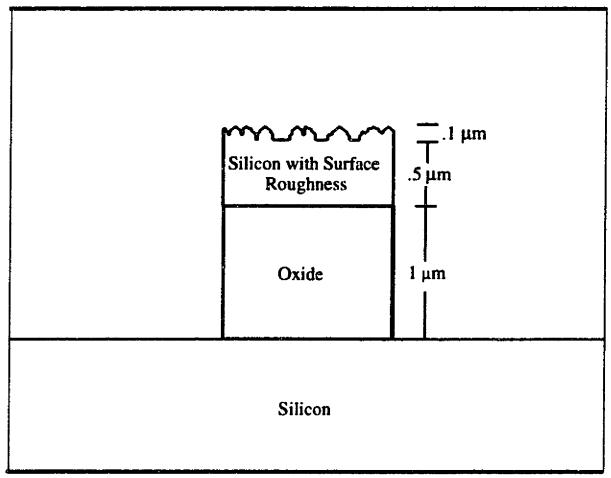


Figure 2.10: The cross section of a polysilicon waveguide is shown. The Interface between the polysilicon and the overlaying oxide or the polysilicon and air is often rough. The surface roughness is a possibility for the high losses in polysilicon waveguides.

This roughness can cause losses in several ways. Scattering of light off the rough surface is probably the major cause of loss in polysilicon waveguides. If a scattering site is modeled as a site where light is absorbed and then re-emitted equally in all directions, then the amount of light scattered out of the waveguide can be calculated by finding the critical angle using Snell's law.

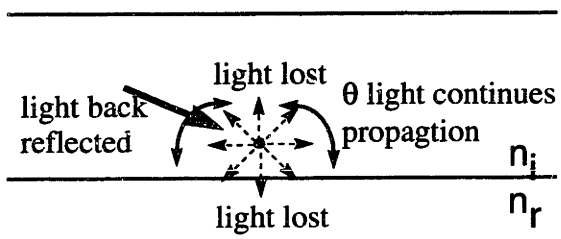


Figure 2.11: Light traveling down the waveguide encounters a scattering site. This site is assumed to scatter light equally in all directions. Only a small fraction of that light remains confined in the waveguide. This light is distributed among the allowed modes.

$$\theta = \text{asin}\left((n_r) / (n_i) \right) \tag{2.6}$$

Θ is the critical angle, above which total internal reflection occurs. For the silicon-oxide interface, n_i is 3.5 and n_r is 1.5 so the critical angle is 23°. With the above assumptions 87% of the light from a point scatter is not totally internally reflected. Of this light part is reflected from normal refections. However, even the light that remains in the waveguide after scattering is not completely unaffected by scattering. The light that remains in the waveguide after scattering is distributed in various modes allowing lower order modes to couple into higher order modes. The higher the order of the mode, the higher the losses, since both surface and bulk losses are amplified in these modes. In some modes the losses are so high no light from that mode makes it to the output.

It is also possible that since the surface area goes up with surface roughness, the losses from surface defects are larger. Amorphous silicon films of thickness around 1 μm have a "strong surface related absorption which dominates" at the wavelength used in this thesis[9]. Since amorphous films have surface absorption, polysilicon may also have such absorption. It is expected that this loss goes up with surface area and therefore with roughness. This loss may be caused by dangling bonds or impurities at the surface.

If surface roughness is of the right periodicity in the direction of propagation, it can also cause back reflection. The periodicity that gives large losses at 1.54μm for silicon waveguides is about 0.5μm. AFM can help determine the periodicity of the roughness by taking the fast Fourier transform of the spectra.

2.3.2 Grain Boundary Absorption and Scattering

Since a grain boundary is the interface between two different crystal orientations, at the grain boundary some silicon outer electrons are left unbound. These electrons are known as dangling bonds. The dangling bonds create defect states in the energy gap which then contribute to sub band gap absorption. The dangling bond defect state is found to be 0.65 +/- 0.15 eV below the conduction band minimum, creating a grain boundary band gap equal to 1.0 eV. "Evidence for exponential tailing of the band edges," is observed and may lead to losses at 0.8 eV (the energy looked at in this thesis)[10].

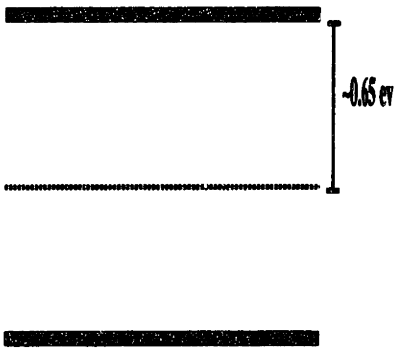


Figure 2.12: The dangling bonds at the grain boundaries creates a defect state in the band-gap

The defect states can trap electrons, which in turn form a bump in the potential seen by the photon. This bump can cause a localized change in the index of refraction which in turn causes scattering of light. The scattering then contributes to the measured losses. If a change in index does occur at the grain boundaries reflections from periodic changes of index may occur. The periodicity required for reflection to be considered is around 0.5μm. Tien reports "It can be seen that the average grain size is on the order of 0.5μ. This grain size is comparable to the optical wavelength used in the experiment and thus causes excessive scattering to the propagating light wave in the film."[11]

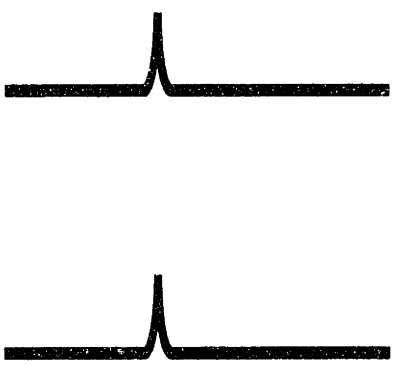


Figure 2.13: Some believe that the grain boundaries create a small "bump" in the band gap which contributes to scattering.

Grain boundaries not only may cause scattering, but probably also cause absorption. The defect state at the grain boundaries can act as an absorption site. In other words, a photon's energy transfers to an electron by exciting the electron to the defect state or from the defect state to the conduction band. The excited electron can decay to the valence band.

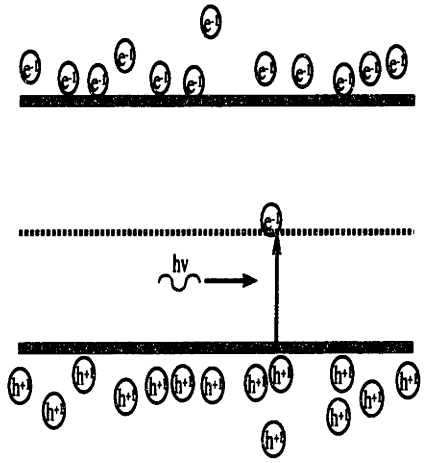


Figure 2.14: Photons can transfer their energy to electrons and holes through the defect site.

Most of the high losses measured for polysilicon are often assumed to be inherent in the grain boundaries. Such high losses are quoted that no work on polysilicon core waveguides has been reported. For example Jones finds the absorption coefficient in poly-silicon to be over 400 cm-1, which is around 1,700 dB/cm[12]. The method however, includes both scattering and absorption. Transmission and reflectance measurements are used to determine absorption. The transmission and reflectance measurements do have absorption information hidden in them, but the information is mixed with losses from scattering.

High losses in polysilicon are reported by others. Similar results were found for sili-con-on sapphire and silicon-on-spinel films reported by Kuhl[13]. Others measured the

losses of undoped polysilicon at 0.75μm. They find losses of several thousand cm^{-1}[14]. From the measurements on polysilicon waveguides done in this thesis, these values are known to be much higher than the actual absorption.

Harbeke measured absorption of both annealed samples and as deposited polysilicon. His results are shown in Figure 2.15.

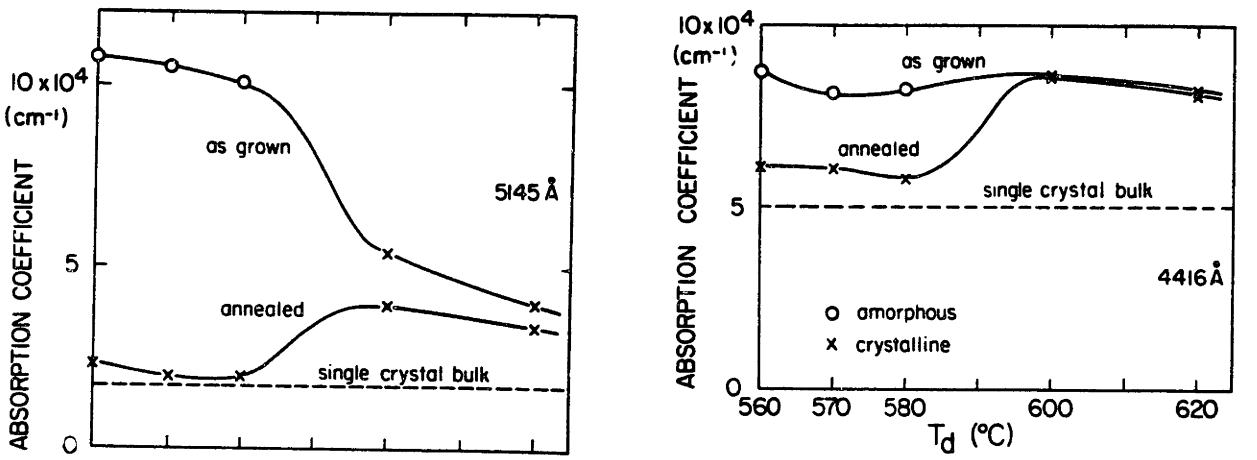


Fig. 11. Absorption coefficient of polysilicon vs. deposition temperature, as-grown and annealed (900°-1000°C), at 5145Å (top) as pertinent for Raman and elastic using spectrometer method and at 4416Å (bottom) as pertinent for scanner method.

Figure 2.15: Harbeke's measurements on polysilicon. Both as deposited polysilicon and annealed amorphous silicon into polysilicon are shown. The annealed into polysilicon shows measured absorption very close to that of single crystalline silicon. Harbeke attributes much of the measured losses to be from scattering.

Harbeke attributes the large differences between samples to "internal scattering which seemingly reduces the transmitted light and thus increases the apparent absorption coefficient." One should note that the lowest absorption in the annealed waveguides is very close to that of single crystalline silicon[15].

For all the reasons above, one can see that grain boundaries may cause some of the losses in polysilicon waveguides. This loss can be either scattering losses or absorption

losses. Research of the effect of grain boundaries on losses is investigated, but further work is needed.

2.3.3 Scattering From Sidewalls

The sidewalls are not perfectly smooth. Just as in the case for the surface, roughness can be a cause of losses in the waveguides. However, SEM pictures show sidewall roughness, but this roughness is smaller than the surface roughness. Therefore, sidewall roughness does not cause as much loss as surface roughness. (Once the losses are brought down further, sidewall roughness should be investigated as a possible loss mechanism, possibly by changing the etch chemistry and masking technique.)

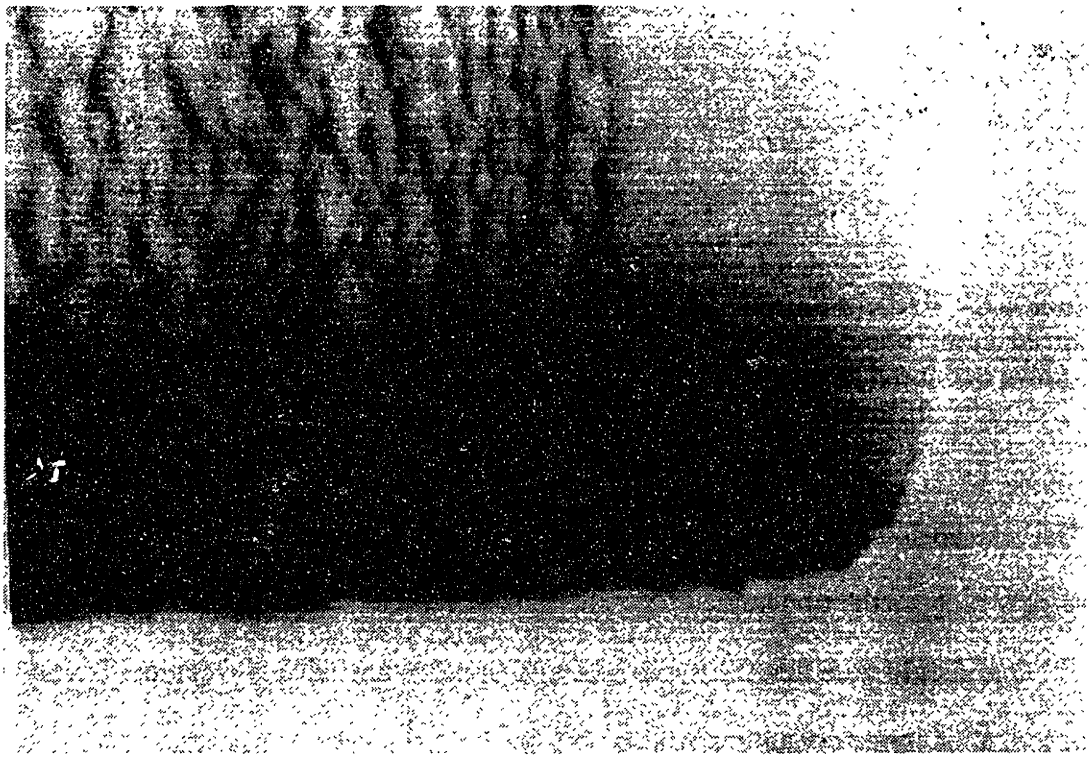


Figure 2.16: SEM picture of waveguides made from silicon deposited at 625°C. Both the surface and edge roughness can be observed.

The sidewall roughness is expected to improve with the elimination of surface roughness. A rough surface causes the photoresist to lay unevenly which then causes the sidewalls to be etched roughly. The effect of uneven photoresist on the sidewall roughness can be seen from the SEM picture since the sidewall roughness appears to be only varying in the z direction. Once the surface roughness is smoothed, it is expected that the sidewall roughness will be negligible. The work done in this thesis therefore, lessens sidewall roughness, but does not determine the amount lost from this roughness.

2.3.4 Other Loss Mechanisms Not Investigated:

Scattering from Interface Roughness

The scattering from the roughness of the interface between the underlying oxide and the polysilicon (see Figure 2.10) results in identical scattering as that due to surface roughness. However, TEM pictures indicate that the interface is not as rough as the surface. The losses due to interface roughness are therefore expected not to be as large as those due to surface roughness, so interface roughness is not investigated.

Tunneling From Waveguide to Substrate

The field traveling down the waveguide has an evanescent wave that extends into the oxide. If the oxide is thinner than the penetration depth of this field then the energy can leak into the substrate.

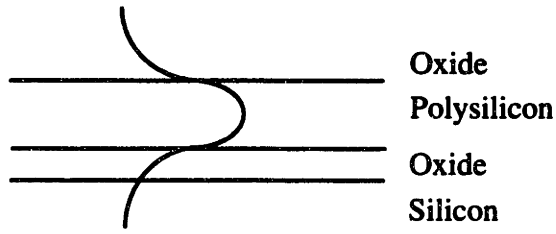


Figure 2.17: The power in the waveguide is shown. If the oxide is not thick enough, the field will penetrate into the silicon. In this Figure, a small exponential tail exists at the silicon oxide interface.

Power leakage into the substrate shows up in the loss of the waveguide. SIMOX waveguides may have high losses from this mechanism since the oxides are thin. Well designed polysilicon waveguides do not have this problem, since the oxide can be grown very thick. The oxide only needs to be 0.7μm thick[16]. The waveguides fabricated in this thesis have an oxide of 3μm, so this loss is negligible.

Absorption Within a Grain

Between the grains are patches of single crystalline material. From the low losses in single crystalline material we know that these patches of single crystalline material can not be a cause of the high losses in polysilicon waveguides. This loss can therefore be eliminated as a major cause of loss

2.4 Polysilicon Materials Issues

Polycrystalline silicon (polysilicon) consists of many single crystalline regions with different orientations. The boundary between single crystalline regions is a grain bound-

ary. All polysilicon materials are not created equal. The grain size, grain structure, defect states, grain orientation, surface roughness, doping, and crystalline quality are among the variables that can change depending on the fabrication technique.

All polysilicon materials in this thesis are undoped. Since doped polysilicon is commonly used in semiconductor processing, most of the research on polysilicon is on doped polysilicon. Fortunately the trends for grain size, grain structure, and surface roughness are expected to remain the same for doped and undoped samples. One must be careful, though, to directly compare exact numbers. For example, doping gives enhanced grain sizes[17, 18].

2.4.1 Grain Size vs. Deposition Temperature

For some applications the grain size needs to be as large as possible, so many people are working on ways to increase the grain size. Doping is one method of fabricating large grains, but is not utilized for this work. Another method of getting large grains is by depositing amorphous silicon instead of polysilicon and then annealing the silicon into polysilicon. Deposition temperatures are often chosen to be between the required temperatures for polysilicon and amorphous deposition (between 600 and 550 ^{o}C) In this temperature region neither pure amorphous or pure polysilicon is grown. Instead, some grains are nucleated which in the annealing stage, can grow with a head start over the new grains sites. Tsai grew 1 micron diameter grains when using this method compared to 0.1 micron diameter grains that she obtained using the traditional method[17]. The grain size is found to increase with decreasing deposition temperature [19] and not depend much on annealing temperature. The grain size dramatically falls off when the deposition temperature is high enough to deposit polysilicon[15].

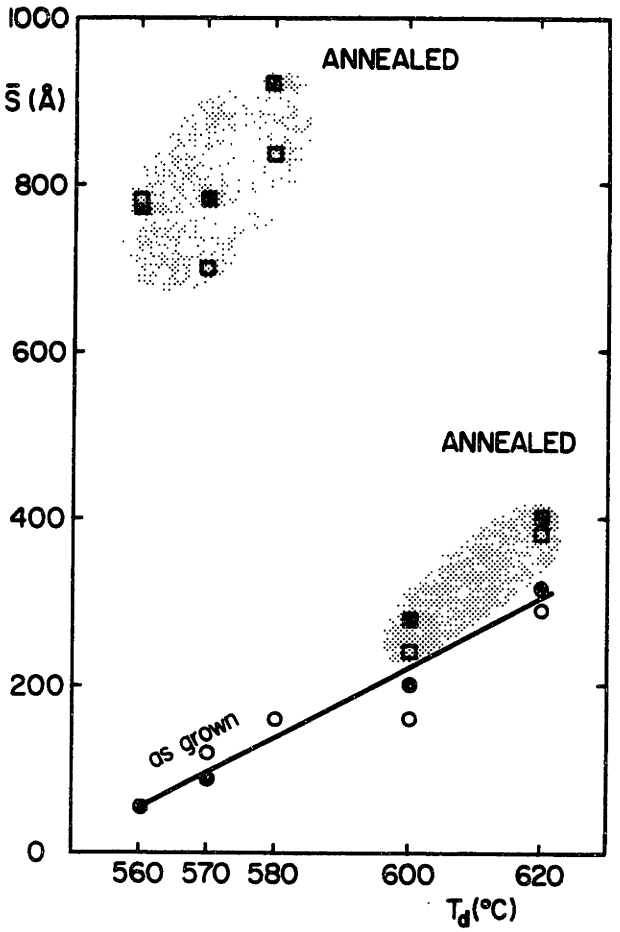


Fig. 4. Average crystallite size $\bar{S}$ for LPCVD Si-layers, as-grown (○ : interface, ● surface) and annealed at 1000°C (□ : interface, ■ surface) as a function of T_d.

Figure 2.18: Harbeke's graph of grains size vs. temperature. The temperatures used in this thesis are 625°C, 580°C, and 560°C. [15].

Small grains can be reached by deposition systems with deposition rates around 1500A/ min. This method deposits silicon so rapidly very small grains are formed.

2.4.2 Surface Roughness vs. Deposition Temperature

Since surface roughness is important in integrated circuit technology, much work is done on it. One method commonly used to minimize surface roughness is to transform

amorphous silicon into polysilicon. Using this method the lower the amorphous silicon deposition temperature, the smoother the surface. The annealing temperature has little effect on surface roughness[15]. Surface roughness have been measured to be around 20A [17] and 30A[20] by annealing doped silicon into polysilicon.

Annealing not only gives smother surfaces for an air polysilicon interface but also for an oxide polysilicon interface. The surface roughness of a polysilicon/oxide interface is measured to be 120A in one study [21]. Some have attributed the polysilicon-polyoxide smoother surface to the poor crystalline quality[22]. However, others find the crystalline quality to be better in these samples[15]

2.4.3 Hydrogenation

Hydrogenation is a standard technique used in the electronics industry to passivate defects, for example, to satisfy dangling bonds at the Si/SiO_2 interface for improved MOS gate oxide integrity. Since the presence of defects and dangling bonds, both, at the surface and in the bulk, can possibly be a source of optical absorption and scattering losses, polysilicon waveguides are exposed to a hydrogen plasma at temperatures which allow the atomic hydrogen in the plasma to diffuse to the defects and then passivate them. In this process, hydrogen atoms attach to the dangling bonds or defects making them less probable to act as a generation center where photons can transfer their energy to electrons. One study found hydrogenation of polysilicon reduced losses at around 0.8eV by about 30dB/cm[23].

The degree of hydrogen absorption can be measured by using photoluminesnce(PL). The PL peak at 0.9 eV is found to shift an amount depending on the degree of hydrogenation. The luminescence peak shifts from 0.90eV to about 0.92eV with hydrogenation[24].

Chapter 3

EXPERIMENTAL PROCEDURE

The waveguides are fabricated using many different processing sequences. For each process the surface roughness, power loss at 1.54μm, and degree of hydrogenation are measured. Before the loss measurements, the waveguide facets are polished and the sample is cleaned to ensure the waveguide facets are clear. We then determine the loss of the waveguide using a cutback technique. Atomic Force Microscopy (AFM) and reflectance measurements are used to determine the surface roughness, and Photoluminescence (PL) is used to determine the degree of hydrogen absorption. Transmission Electron Microscopy (TEM) is used to investigate the grain structure of the samples. The following sections discuss the details of the experimental techniques.

3.1 General Recipe

All experiments begin with a p-type, boron doped, 4 inch, 0.5-2 ohm-cm resistivity, CZ, <100> silicon wafer. Following an RCA clean, a 3μm low temperature thermal oxide is grown on top of the wafer. Then either polysilicon or amorphous silicon is deposited. Half the wafers are left unpatterned. The others are patterned with a mask with 4 sets of 20 waveguides and test patterns on it. The patterned wafers are then silicon plasma etched (CCl_4/O_2/He:: 130/20/70 sccm at 300W and 0.19 Torr). All wafers then go through an RCA clean and a low temperature oxidation. The wafers are then annealed at 600°C for 16 hours. During this anneal the amorphous films crystallize into polysilicon. All wafers are made from the same lot.

After processing, the unpatterened wafers are cleaved into quarters for reflectance measurements and AFM (and for future work using an Fourier Transform infrared Spectrograph (FTIR) or Photothermal Deflection Spectroscopy (PDS)). The patterned wafers are die sawed so that each sample contains waveguides with different lengths. Usually these lengths are 2mm, 1.5mm, and 1.0mm. Two of these samples are polished, cleaned, and measured for transmittance. Other samples are used for TEM and SEM. Several dies are selected from each patterned wafer for hydrogenation.[1]

3.2 Hydrogenation

In our hydrogenation experiment, the re-crystallized amorphous silicon samples deposited at 560°C and 580°C, as well as the as-deposited polysilicon (625°C deposition temperature) sample were hydrogenated at 200°C with 40 watts power and 370-400 milli-Torr pressure in a plasma chamber. The samples were cooled to 68°C (1 hour) in the presence of the plasma to prevent out-diffusion of hydrogen during the cool-down process. The level of hydrogenation was subsequently investigated by comparing the differences in the band-tail photoluminescence of the hydrogenated and unhydrogenated samples[24].

3.3 Sets of Wafers:

3.3.1 Deposited as Polysilicon:

Prior to this thesis polysilicon waveguides were fabricated and tested. These waveguides were deposited at 625°C. This experiment is repeated to ensure equal compar-

1. Processing is done by Anu Agarwal.

ison with other experiments. Four wafers are fabricated by depositing polysilicon at 625°C and annealing for 16 hours. These wafers are referred to as "625". 625°C is a high enough temperature so that the silicon is deposited in polysilicon form.

3.3.2 Annealed Amorphous Silicon into Polysilicon:

If the deposition temperature is less than a critical temperature, amorphous silicon is deposited instead of polysilicon. Twelve wafers less than the critical temperature are fabricated. After silicon deposition, all twelve wafers are annealed to crystallize the silicon into a polycrystalline film. The only variable among these wafers is the deposition temperature of the amorphous silicon. Four wafers at each of the three temperatures 560°C, 580°C, and 600°C, are fabricated. No data is presented for the wafers deposited at 600°C, since a haze formed on the surface of these wafers. The wafers deposited as amorphous are referred to as "560" and "580".

3.3.3 Polysilicon Polished:

Two wafers are chemically mechanically polished (CMP). These wafers contain polysilicon deposited at 625°C. The surface of the wafers are polished. One wafer is then cleaved for surface roughness and other measurements. The other wafers is patterned, annealed, and then die sawed for cutback measurements. These wafers are referred to as "CMP".

3.3.4 Hydrogenated Polysilicon:

Hydrogenation passivates the dangling bonds at the grain boundaries, therefore decreasing the generation-recombination centers, and hence decreasing the absorption at the grain boundaries. In order to investigate the effect of grain boundaries, after the 560, 580, and 625 wafers are completely fabricated, a die from each is selected for hydrogenation. After hydrogenation, these dies are polished, cleaned, and measured as the unhydrogenated samples. The hydrogenated samples are referred to as 560h, 580h, 625h.

3.4 Sample Preparation: Polishing and Cleaning

Before all loss measurements samples are polished and then cleaned. Polishing creates new waveguide facets and ensures that they are not broken. Cleaning then removes residue from the waveguides and in particular from the facets.

3.4.1 Polishing

When measuring the output power from the waveguides, the facets of the waveguides must be well polished in order to reduce coupling losses and to ensure reproducible measurements. Variations in coupling losses lead to increased error in the measurements and a large variation in output power measured across waveguides on the same sample. The standard deviation of the measured output power for 20 waveguides from the same sample therefore reflects the quality of polishing and cleaning and is found to be around 3%.

The polishing technique is adapted from TEM preparation.[1] First the waveguides are mounted onto a sample holder using hot wax. The sample is aligned so that it is polished evenly across the sample edge. Once the sample is aligned, 1μm and then 0.3μm grit alumina impregnated polishing pads are used to polish the facets. Both sides of the waveguide are polished before testing.

3.4.2 Cleaning

The sample cleaning is also adapted from TEM preparation. First the wafer is placed in trichloroethylene (TCE) and put in an ultrasonic bath for 5 minutes which removes most of the wax and organic contaminants on the sample. In order to protect the waveguides from breaking during the clean, a cleanroom safe towel is placed inside the container. After TCE, the sample is placed in acetone and then in methanol for the same 5 minute ultrasonic bath. At the completion of the clean, the waveguides and their facets are checked under a 100X microscope to determine if residue remains on the waveguides. Often the clean is repeated until clean samples are achieved.

3.5 Optical Loss Measurements

Since 1.54μm light is at the dispersion minimum for optical fiber and is the wavelength of emission of the erbium doped silicon LED, all loss measurements are done at this wavelength. The output power of each waveguide is measured using the setup shown in Figure 3.1.

1. The polishing technique is developed by James Foresi.

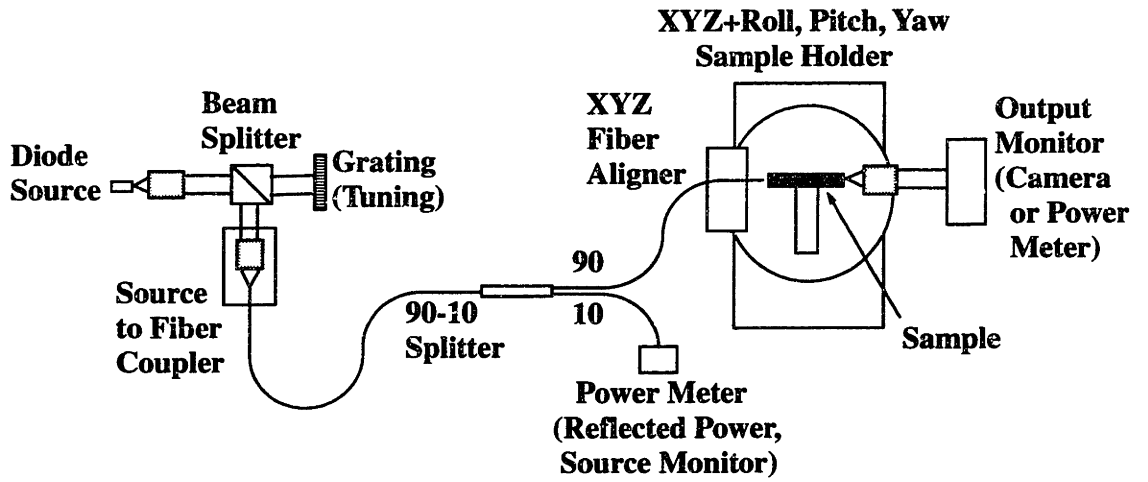


Figure 3.1: Waveguide loss measurement setup. The light is emitted from a laser. 10%of the light is used to keep the input power constant. The rest is coupled into the waveguide using an optical fiber to butt couple the light in. The light is then either observed on a camera or measured using a IR detector.

Light at 1.54μm is emitted from a laser diode. The light is then coupled into an optical fiber. The light in the fiber is split using a 90-10 splitter. 10% of the light goes to a light meter which is measured with either an oscilloscope or a multimeter. Throughout the measurement, the 10% signal is monitored to ensure that the power entering the waveguide is constant. The remaining 90% of the light is coupled into the waveguide using a standard butt-coupling configuration. The optical fiber has a pointed tip to focus the beam from the 9μm optical fiber core into a spot approximately 4μm in diameter. The light coming out of the waveguide can either be observed through a camera or measured by an infrared detector. The light output is optimized by adjusting piezoelectric translators on which the optical fiber is mounted.

3.6 Cutback Analysis

One sample consists of 20 waveguides with a width of 8 μm. For these 20 waveguides the output power is divided by the input power. An average is then taken by excluding waveguides which only have a fraction of the output power, indicating a broken facet.

Since the measured loss is a combination of both the coupling losses and the loss per length, two measurements of different lengths are needed to factor out coupling losses. Once two different sets of waveguides with different lengths and the same width are measured, the loss per centimeter is found by the following cutback equation:

$$\frac{dB}{cm} = \frac{10}{l_1 - l_2}\log\frac{P_1}{P_2} \tag{3.1}$$

where l_1 and l_2 are the lengths of the waveguides in cm and P_1 and P_2 is the ratio of the input power divided by the output power. The lengths of the waveguides are obtained using a calibrated microscope. The coupling losses can then be calculated from the dB/cm by multiplying by the length and then subtracting from the total losses.

3.7 Atomic Force Microscopy (AFM)

AFM is used to find the RMS surface roughness of the samples. A Digital Instrument Nanoscope III with a dimension 3,000 stage was operated in tapping mode to examine the surface of the samples. A resolution of 256 x 256 is used for all diagrams. The RMS roughness is calculated from height of the sample at each location with the equation:

$$RMS = \sqrt{\frac{\sum (Z_i - Z_{ave})^2}{N}} \tag{3.2}$$

where Z is the height of the sample, Z_{ave} is the average height, and N is the number of samples.One should note that RMS contains no information on size and shape of roughness. RMS is only a measure of how far the heights at different locations deviate from the average height and is not obviously meaningful for scattering.

3.8 Surface Reflectance

Surface Reflectance is using along with TEM to find the RMS surface roughness. All reflectance measurements reported in this thesis are specular reflectance as described below. The instrument used is a Cary 5E Spectrophotometer.

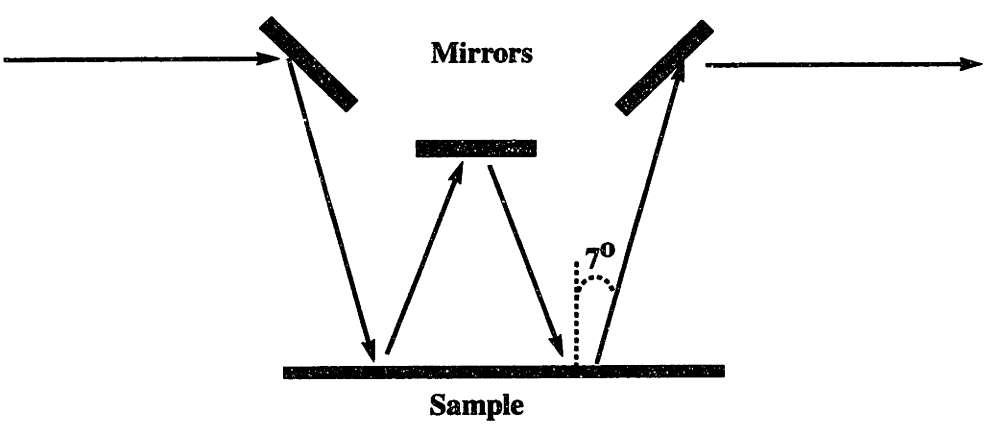


Figure 3.2: Specular reflectance is done with the light reflecting off the sample twice at an angle of 7°. The reflectance is then calculated from the measured output.

The specular reflectometer measures the light reflecting off of a surface versus wavelength. The system dependence on wavelength is factored out by taking a baseline (a mea-

surement with a mirror in place of a sample). All spectra are divided by this baseline. The spectroreflectometer operated with an angle of incident of 7^{o} (Figure 3.2) and spans a spectrum of $3{,}030cm^{-1}$ to $57{,}142cm^{-1}$ wavenumbers.

Surface roughness can be calculated from the reflectance measurements. A single crystalline sample is used as a smooth surface reference. The reflectance, R, of the poly-crystalline material is related to the reflectance, R_0, of the single crystalline smoother surface by the following equation:

$$R/R_o = \exp-\left(4\pi\cos\Phi\frac{\sigma}{\lambda}\right)^2 + 32\pi^2(\cos\Phi)^3\Delta W\frac{(\sigma/\lambda)^4}{M^2} \tag{3.3}$$

where λ, Φ, and ΔW represent the wavelength, angle, and the solid angle of observance respectively. σ is the rms height of the surface roughness, and M is the slope of this roughness[26].

Fortunately if the wavelength is much larger than the root mean square of the roughness, a more simple equation can be used which assumes that the diffuse reflection term can be neglected. "The result is specular reflectance from a surface with an 'effective' refractive index" [26] ; with such approximation we get:

$$R/R_o = \exp-\left(4\pi\cos\Phi\frac{\sigma}{\lambda}\right)^2 \tag{3.4}$$

Since our roughness is on the order of 10nm and the wavelengths used are greater than or equal to 200nm, equation 3.4 is used[26].

The reflectance measurements can also be used to determine the crystallinity of the silicon. If the sample is single crystalline, maxima of reflection should appear in the reflectance spectra around 26,000 and 37,000 cm^{-1}. "These maxima arise from optical transitions at the X point and along the Γ-L axis of the Brillouin zone, respectively, and are strongly affected by distortions in the crystal structure." [27] The maxima are largest in single crystalline material, observable in polycrystalline material, and non-existent in amorphous material.

3.9 Calculation of Loss from Surface Roughness

Tien did an estimate of the effect of surface roughness on the loss of a waveguide. He stresses that the analysis is only an estimate of loses, since several assumptions are made that are not completely justified. This method, however, gives losses that correlate well to the experimental results.

The Tien loss estimate is found by the equation: [28]

$$\alpha = A^2 \frac{(\cos\theta')^3}{2\sin\theta'} \frac{1}{t_g + 1/p + 1/q} \tag{3.5}$$

α is the exponential decay constant. $\theta' = 90-\theta$, is found to be 78.2° for the fundamental mode (section 2.1.2). p and q are the penetration depths into the top and bottom oxide. p and q are calculated in section 2.1.2. to be 13.0031μm^{-1} and 13.0031μm^{-1} for the fundamental mode. A is a measure of the surface roughness and can be found by the equation:

$$A = \frac{4\pi}{\lambda}\langle \sigma_{12}^{\ 2} + \sigma_{21}^{\ 2} \rangle^{1/2} \tag{3.6}$$

λ is the wavelength in the core, which in the case of polysilicon waveguides is 1.54μm/ 3.5. σ_{12} and σ_{21} are the RMS roughness of the two Si-SiO_2 surfaces[28].

3.10 TEM

TEM cross section is used to determine the exact grain structures and sizes. Using TEM, we can tell if the polysilicon is deposited as amorphous or as polysilicon and can get a qualitative estimate of the grain size. TEM plane view can be done in the future to analytically determine the size of the grains. Both light and dark field are used at a magnification of 50KX.[1]

3.11 Chemical Mechanical Polishing (CMP)

CMP polishing is used to deconvolve the effects of surface scattering and bulk scattering. CMP polishes the sample surface and maintains its grain structure. CMP is performed at Lincoln Laboratory on a WESTECH 372 machine. This system has a uniformity of 1%. A touch down method is used where the polish time is only 30 seconds. The other important polishing parameters are listed in Table 3.1. [2]

1. TEM samples are prepared and taken by Anu Agarwal.
2. James Reinold from Lincoln Labs chemically mechanically polished all CMP samples.

Parameter	Setting
polish time	30 seconds
pressure	2 psi
temperature	30 °C
polish pad type	IC-60 on a SUBA-IV
carrier head curvature	50μm
slurry flow rate	200ml/min
slurry flow	200 ILD 1300 by Rodel
platen RPM	15
carrier RPM	15

Table 3.1: Polishing Parameters

Before and after the polish, the thickness of the polysilicon is measured on a Prometrix system.

3.12 Photoluminescence (PL)

PL is used in this thesis to help determine the degree of hydrogen absorption. In PL, 488nm wavelength light excites electron hole pairs. When the electrons hole pairs recombine phonons are emitted, some of which are collected by a detector. The light collected is passed through a monochromomoneter so a power vs. wavelength plot can be obtained. The power used is 1.0 watt, and the slit width is 2mm. All measurements are taken at 42K with a 0.5 optical density filter at the detector.[1]

1. Photoluminescence spectra are taken by Anu Agarwal.

3.13 Surface Roughness Computer Simulations

A finite-difference waveguide simulation is used to aid in our understanding of the light scattering, which occurs due to surface roughness. This beam propagation method solves the paraxial wave equation for the given input field and index profile. The program obtains the fields in a cross-sectional plane and then iterates to obtain the third dimension, the direction of propagation. The simulation does not account for back reflections.

The effective index is found by using imaginary distance beam propagation. This method simulates the light traveling down an imaginary axis of propagation. Normally a mode is characterized by e^{-jkz}. When z is an imaginary number the new wave is e^{kz}, and the wave amplitude exponentially grows with a propagation constant of k. Since the fundamental mode has a much larger propagation constant than other modes, after a short time the fundamental wave function can be found. By averaging the propagation constant, the effective index can be found[29]. The effective index is then used in the real waveguide propagation simulation.

As part of this thesis, the user interface was modified to account for surface roughness. Cells are created on the surface of the waveguide where the interface between the silicon and silicon dioxide is higher. The user specificizes the smooth waveguide index profile, the wavelength, the number of cells across the window, the average width of the cell (nrandx), the height of the cells (hrand), and the variation of the cells (sigma).

Variable	Description
hrandx	The height of the cells in x-dimensions.

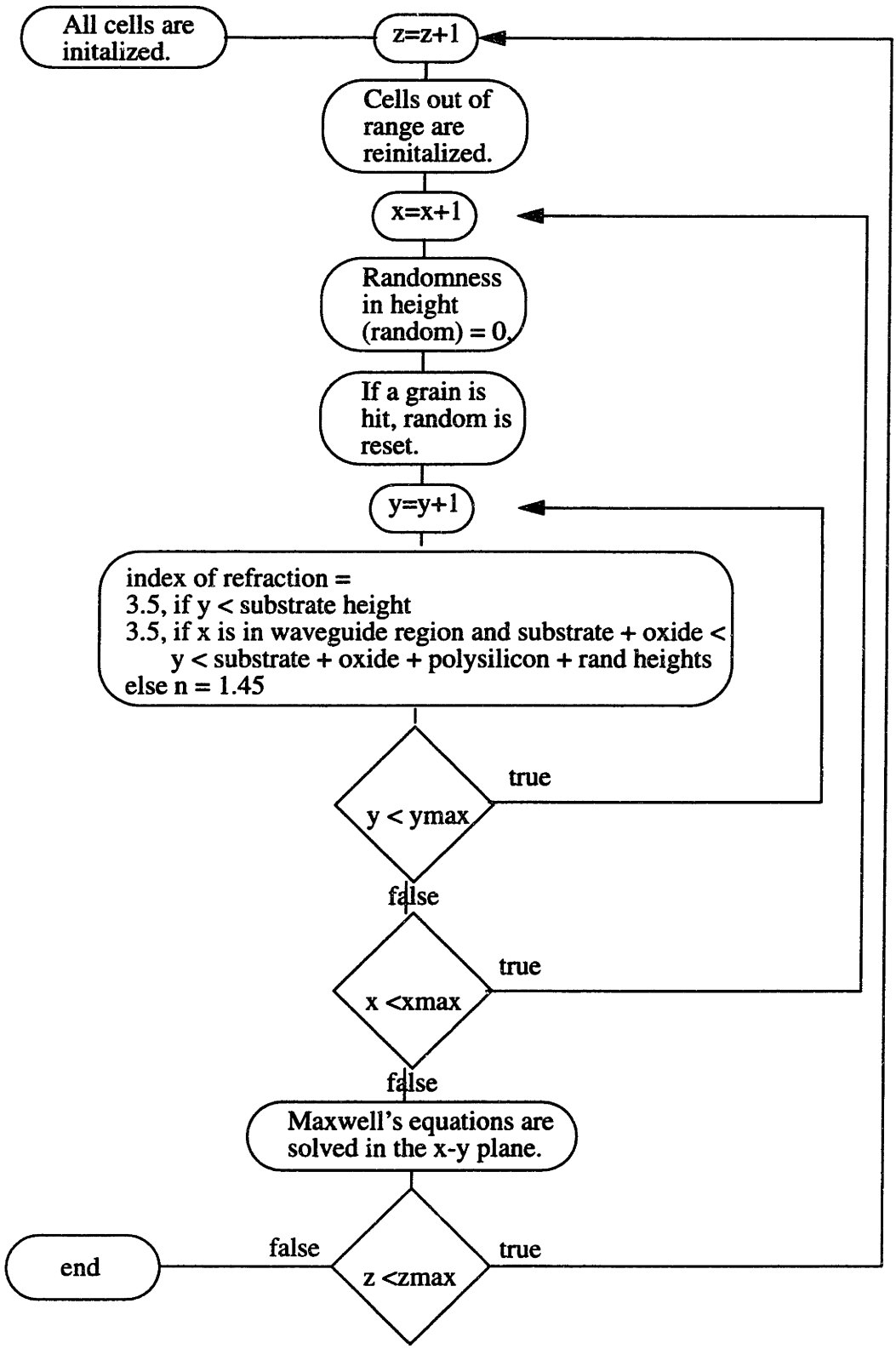
Table 3.2: The input surface roughness parameters are shown. The four variables together completely describe the roughness of the waveguide simulated.

Variable	Description
nrandx	The average width of the cells in x-dimensions
sigma	The variation in the cells' widths in x-dimension
grains	The number of grains in the simulation window

Table 3.2: The input surface roughness parameters are shown. The four variables together completely describe the roughness of the waveguide simulated.

The cells are parabolic in the cross section plane as well as in the direction of propagation. The cells are assumed to be as wide in the x direction as in the z direction. In order to avoid anaphasic reflections due to periodic grains, randomness is incorporated. The grain width is random across the range of the average width +/- the variation in cell width entered by the user.

On start up the initial cells are formed. For each cell, the width in the x dimension in units of x resolutions (widthx), a width in the z dimension in units of z resolutions (widthz), the x position (xdir), and the z position (zdir) are determined. Widthx is randomly selected to be between nrandx - sigma and nrandx + sigma. The probability over this range is constant. Widthz is calculated from widthx so that the cell has the same width in the z and x directions. Xdir is randomly selected so the center of the grain is in the simulation window. Zdir is set to be equal to the largest grain width possible, nrandx + sigma (except in units of z resolution. For each iteration in the z dimension, the index profile is calculated, and Mawell's equations are solved. After each iteration, one is subtracted from widthz. If widthz is less than the negative of the radius of the grain (the grain is no longer in range) the grain is reset just as in the start-up procedure.


All cells are initalized.
z=z+1
Cells out of range are reinitalized.
x=x+1
Randomness in height (random) = 0.
If a grain is hit, random is reset.
y=y+1
index of refraction =
3.5, if y < substrate height
3.5, if x is in waveguide region and substrate + oxide < y < substrate + oxide + polysilicon + rand heights
else n = 1.45
y < ymax
true
false
x <xmax
true
false
Maxwell's equations are solved in the x-y plane.
z <zmax
false
true
end

In order to obtain better results only part of the interface between the polysilicon and the overlaying oxide is simulated. The full waveguide and the section simulated are shown below.

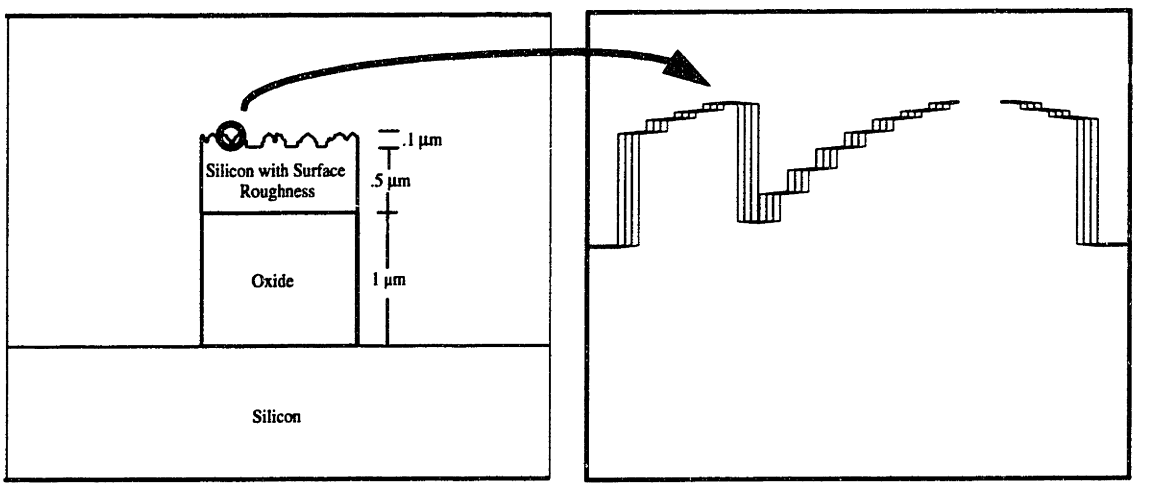


Figure 3.3: The complete and partially simulated waveguide. The Figure on the left is a cross section of a rough waveguide constructed from the waveguide simulation program. The Figure on the right is the interface between the polysilicon and the overlaying oxide constructed from the simulation program. Cross sections such as that shown on the right are simulated in this work.

Chapter 4

EXPERIMENTAL RESULTS

4.1 Cutback Power Loss Measurements at 1.54μm

Cutback measurements factor out the effects of coupling loss and determine the dB/cm of the polysilicon waveguides. The values obtained from cutback measurements are shown in table 4.1 and 4.2. Error bars of 1 sigma are obtained by measurements on 40 samples, 20 at two different lengths.

waveguide type	dB/cm-unhydrogenated	dB/cm-hydrogenated
560	37 +/- 6	42 +/- 4
580	71 +/- 7	71 +/- 3
625	75 +/- 19	64 +/- 8
CMP	34 +/- 4	----------

Table 4.1: Cutback Measurement Losses.

Table 4.1 shows the measured loss in dB/cm at 1.54μm. The 625 wafers have losses of 75 dB/cm, which agrees with the losses measured prior to this thesis of 77 +/- 5 dB/cm[4]. Even though the error bars are large on the 625 sample, this number can be trusted since previous experiments correlate well. For the rest of the thesis, the 625 loss obtained prior to this thesis are used since the error bars are considerably smaller.

As can be seen from Table 4.1, the 580 and 625 unhydrogenated samples have a much larger loss than the CMP and the 560 unhydrogenated samples. In addition, the reader

should note hydrogenation has no measurable effect, within error bars, on the 560 and 580 samples, but decreases the 625 losses slightly. Three loss measurements instead of two are preformed on the 580H sample. A curve fit is done on these points to obtain the result in Tables 4.1.

4.2 AFM

Atomic Force Microscopy Measurements are shown in Figure 4.1, 4.2, 4.3, 4.4 for 560, 580, 625, and CMP wafers respectively.

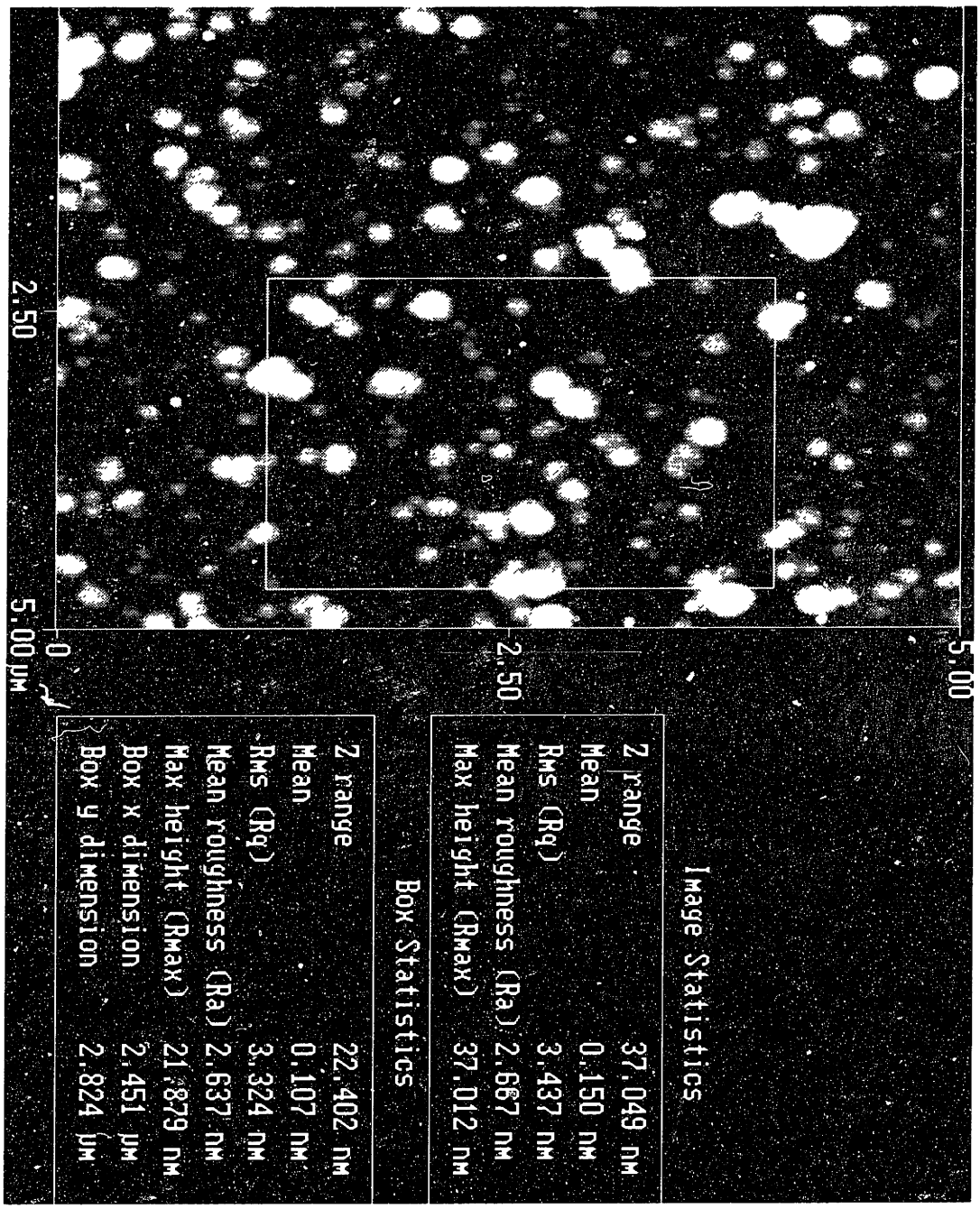


Figure 4.1: AFM surface plot is shown for polysilicon deposited on oxide at 560^0C and then annealed into polysilicon.

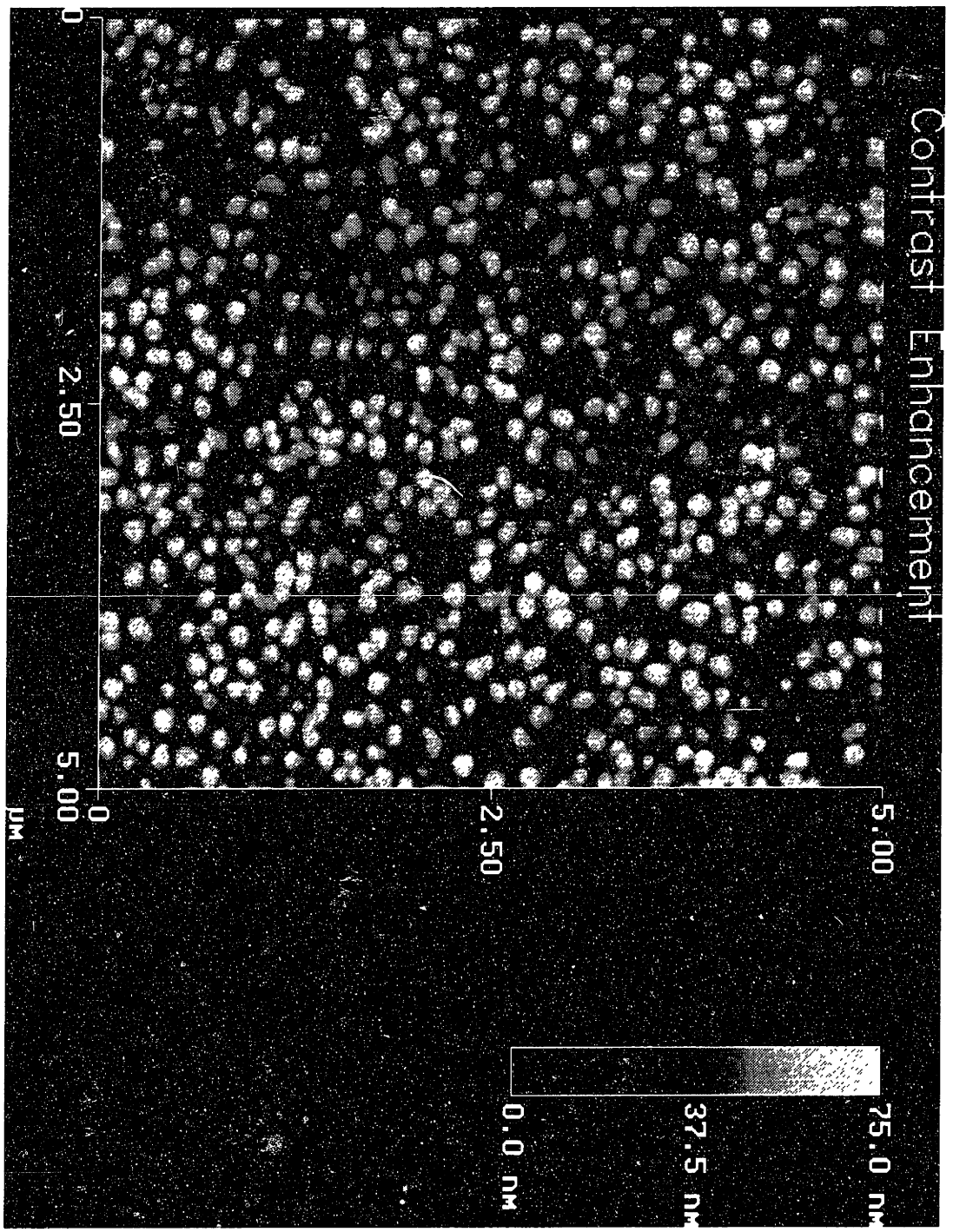


Figure 4.2: AFM surface plot is shown for polysilicon deposited on oxide at 580^0C and then annealed into polysilicon.

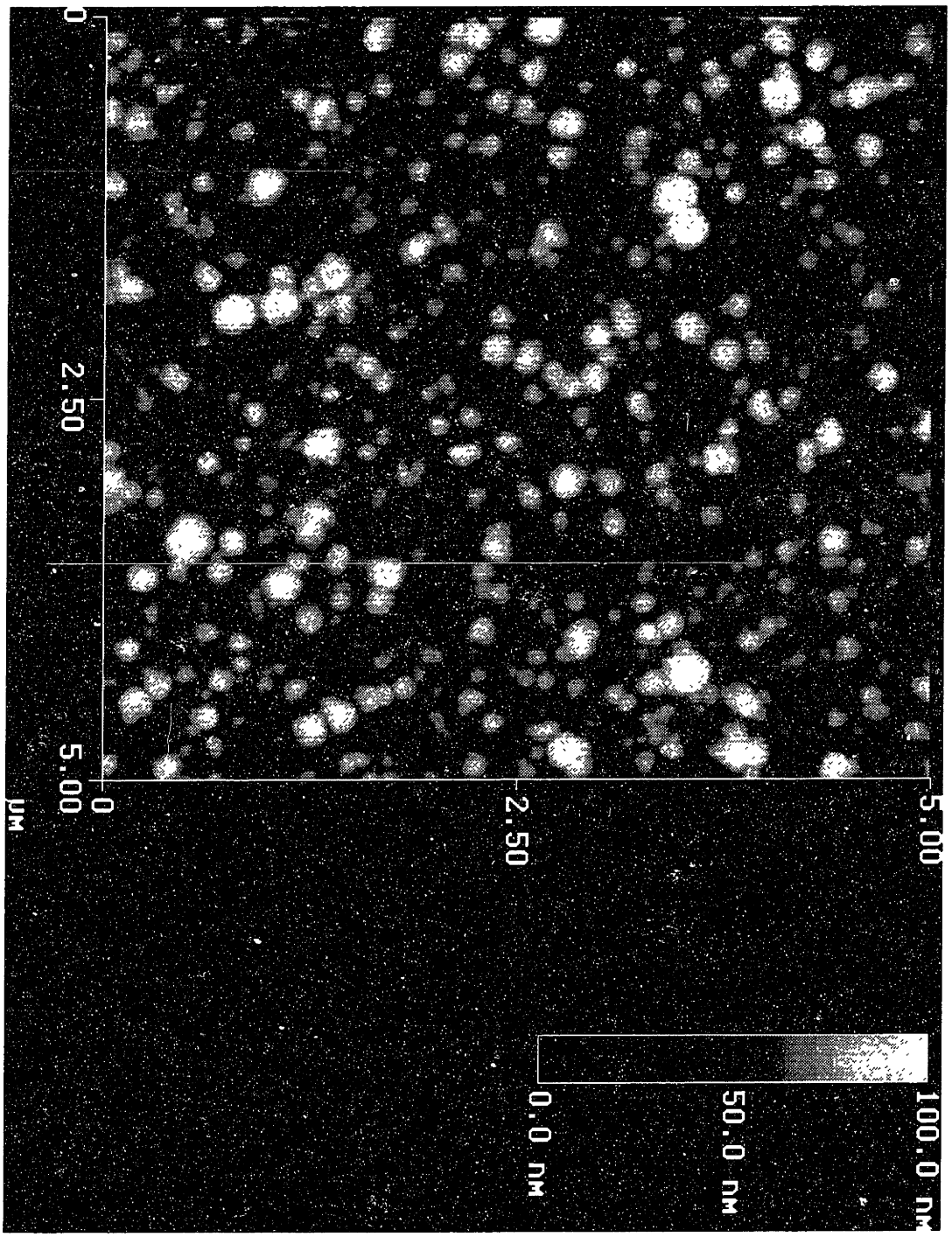


Figure 4.3: AFM surface plot is shown for polysilicon deposited on oxide at 625^0C and then annealed.

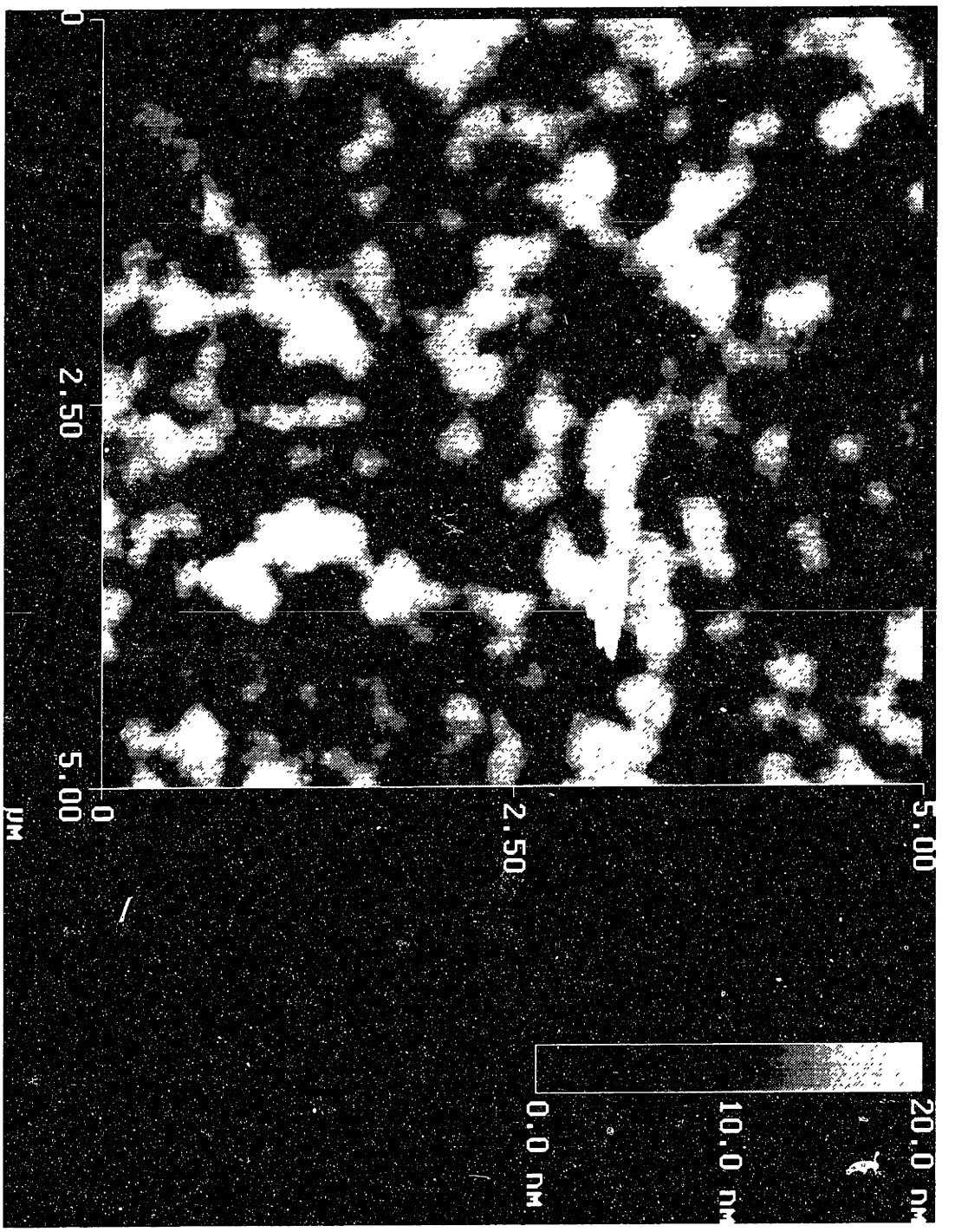


Figure 4.4: AFM surface plot is shown for the CMP wafer is shown.

The RMS values are found to be 3.7nm, 14.9nm, 20.0nm and 6.8nm. for the 560, 580,

625, and CMP wafers respectively.

Sample Type	RMS from AFM (nm)
625 annealed	20.0
580 annealed	14.9
580 unannealed	15.6
560 annealed	3.7
CMP 30 seconds	6.8
CMP 60 seconds	1.9

Table 4.2: Roughness RMS From AFM Measurements

The Fourier transform of the roughness of the 625 wafer is shown in Figure4.5.

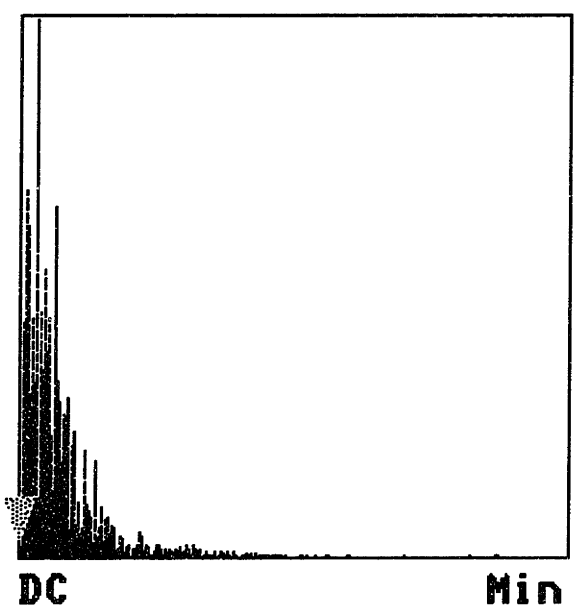


Figure 4.5: The Fourier transform of the surface height of the 625 sample. No strong periodicity exists.

The Fourier transform of the roughness indicates the roughness is nonperiodic.

4.3 Reflectance

The reflectance vs. wavelength measurements are shown for all the annealed samples and single crystalline silicon (560A, 580A, 625A, CMP, and single Si).

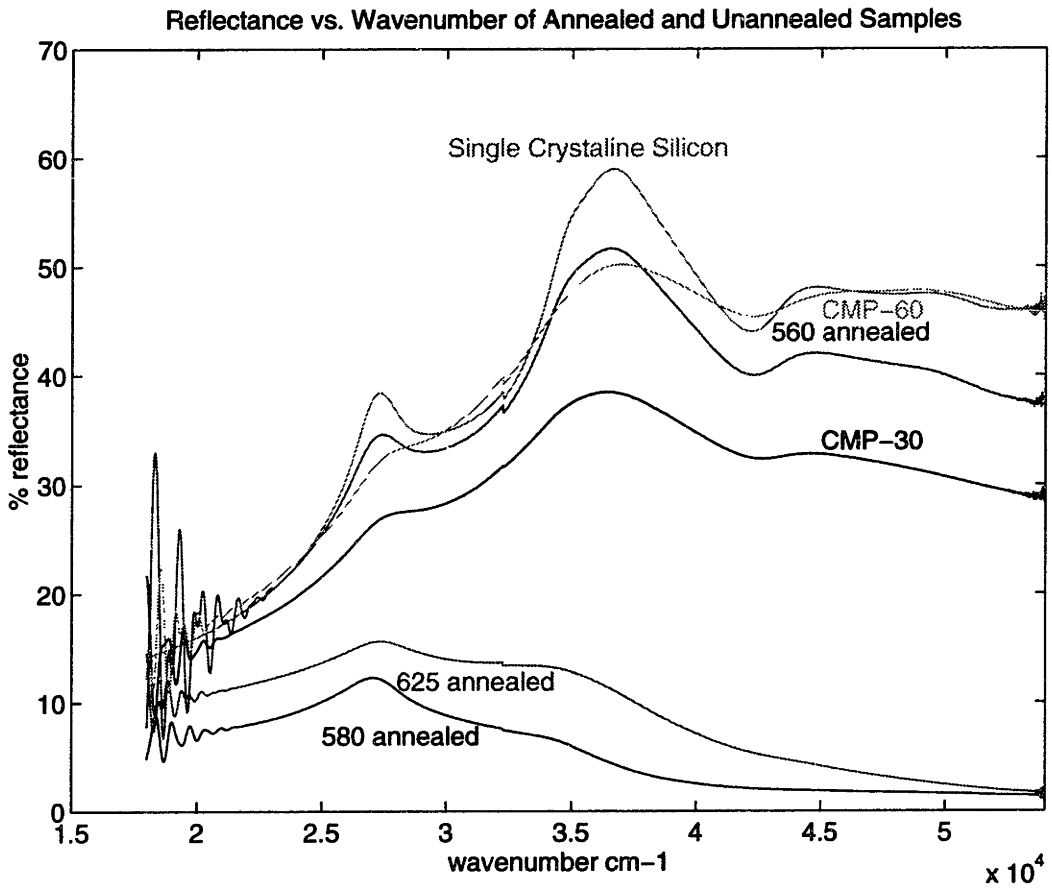


Figure 4.6: The reflectance measurements for samples with silicon deposited at three temperatures and then annealed are shown. A single crystalline sample and a chemically mechanically polished sample are also shown. The CMP wafer is deposited at 625°C.

One should observe the large reflectance of the single crystalline, 560, and CMP wafers relative to the 625 and 580 wafers, indicating a smoother surface. The large reflections of

the 560A and single crystalline silicon at 26,000 and 37,000 cm^{-1} indicate the larger degree or crystallinity as explained in section 3.8. The peaks are also observable in the 580, 625, CMP-30, and CMP-60, but are not as large as in the single crystalline silicon, thus indicating polycrystalline material. The 560 unannealed has no peaks and is therefore amorphous silicon.

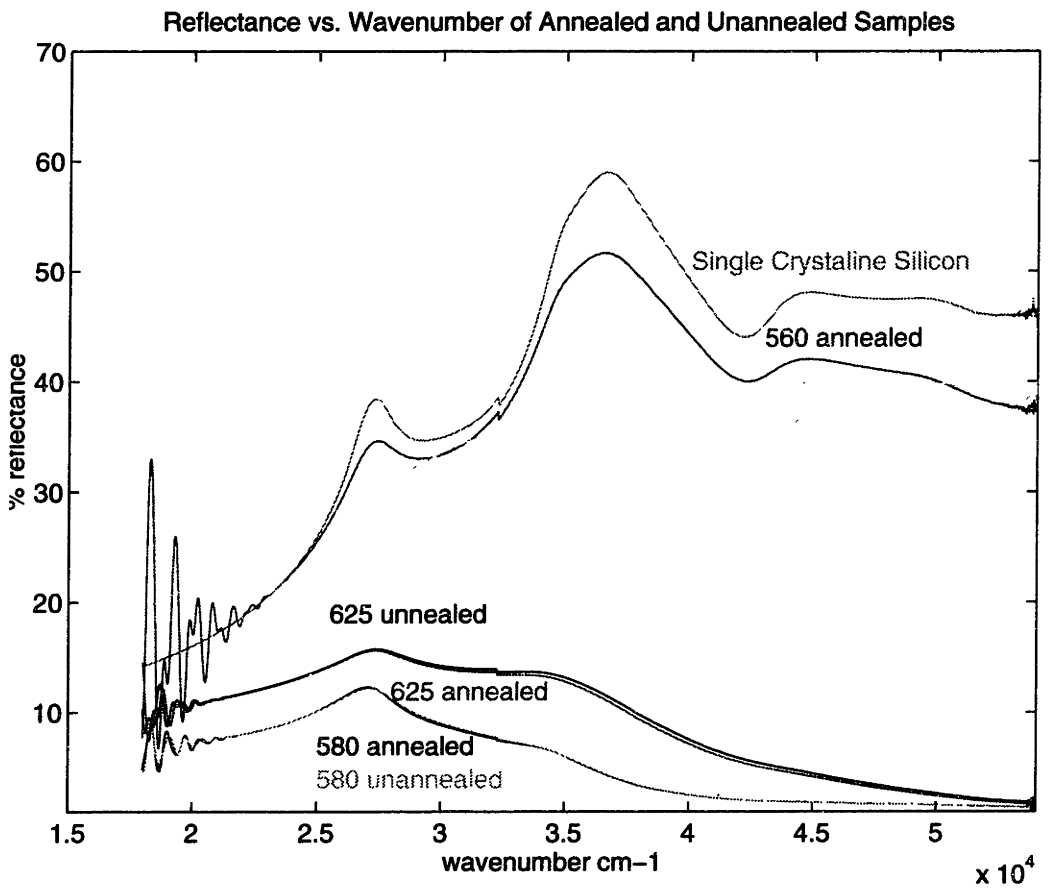


Figure 4.7: The reflectance measurements for the annealed and unannealed samples are shown. For each deposition temperature, the annealing has little effect on the reflectance and hence the surface. The 560 does show slight variations.

The reflectance of the unannealed samples is identical to the annealed samples for both 625 and 580 °C deposition temperatures (see Figure 4.7). The 560 samples, have minimal differences between the annealed and the unannealed samples. These differences are

mainly at around 36,000 cm-1 and 28,500 cm-1. The small variations between annelaed and unanealed samples indicate annealing does not vary the surface profile considerably.

4.4 TEM

TEM is used to determine the grain structure of the samples. We assume hydrogenation has no effect on grain structure, and therefore did not preform TEM on hydrogenated samples. The TEM cross-sections and top view of the 560 and 625 samples are shown below. The differences in grain size and grain structure can be seen. Since the 625 is deposited as polysilicon while the 560 is annealed into polysilicon, the 625 has columnar grains while the 560 does not. The as deposited polysilicon forms grains at the beginning of deposition and these grains grow during the entire growth process (surface nucleation). Bulk nucleation occurs in the deposited amorphous silicon and these sites are grow during the anneal.

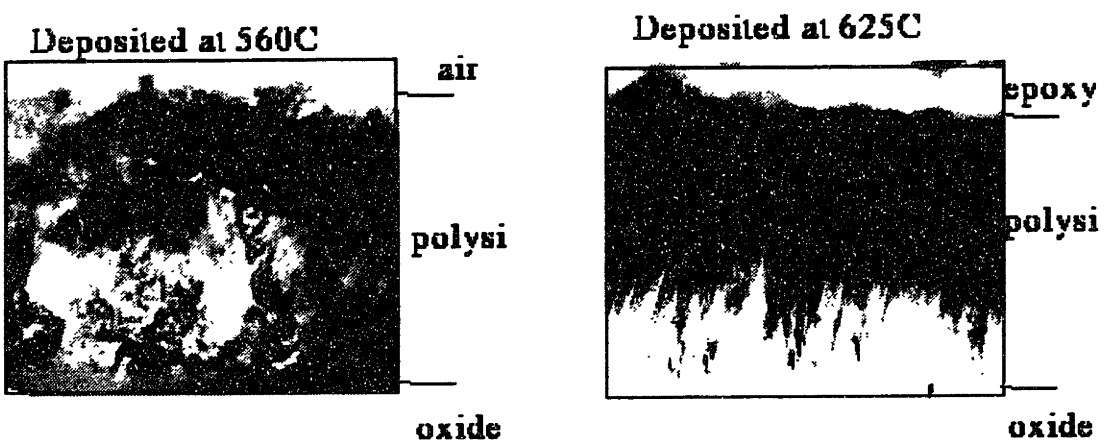


Figure 4.8: The cross-sectional TEM the 625 sample is shown on the left. The cross-sectional TEM of the 625 is on the right. The difference in grain structure can be seen as well as the surface roughness.

4.5 Photoluminescenec

The PL spectra for the 560, 625, 560H, and 625H are shown below.

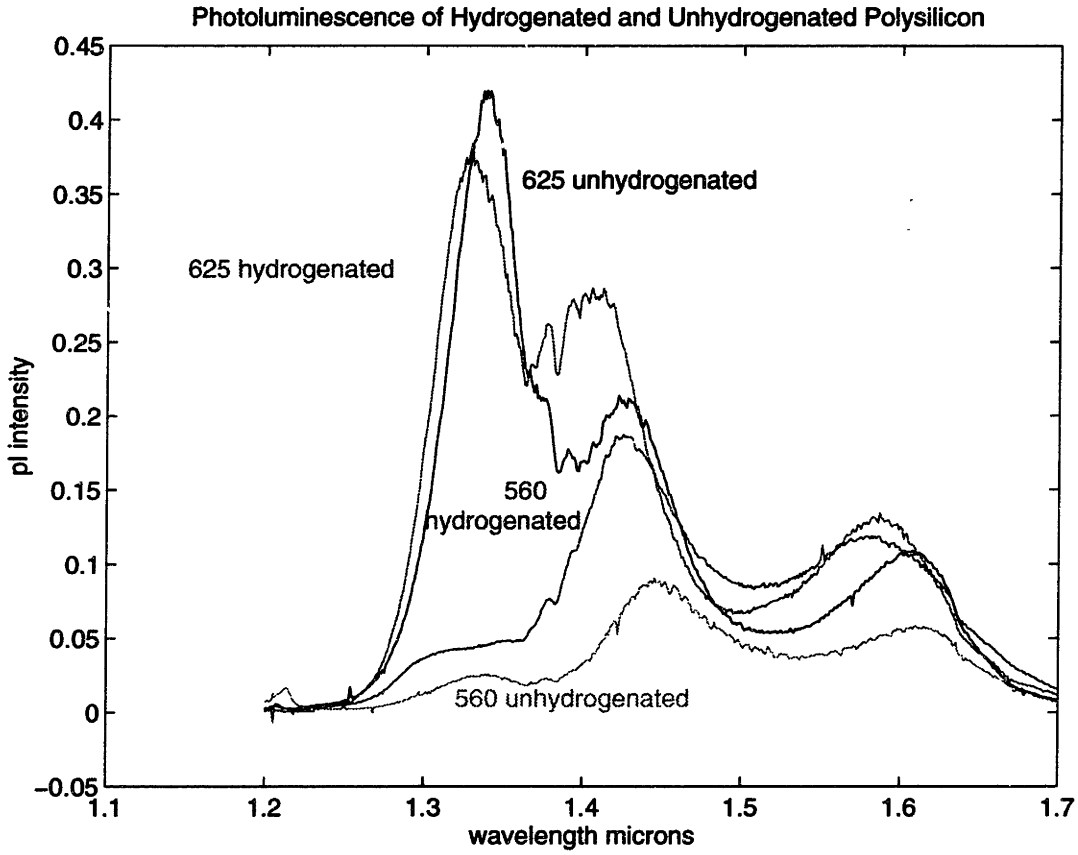


Figure 4.9: The Photoluminescence (PL) spectra for 560 and 625 hydrogenated and unhydrogenated are shown. No peak at 1.38μm is observed. (When analyzing the PL spectra, one should keep in mind that the relative amplitude between samples is arbitrary since it is sensitive to sample angle, temperature, laser alignment, ect.)

Several peaks measured have not been reported previously. Savchouk observes a peak at 0.9eV (1.38μm)[24]. The difference in peaks are attributed to the difference in substrates and humidity in the air. (Our polysilicon is deposited on oxide which is on silicon. His pol-

ysilicon is on glass.) The peak observed by Savchouk appears to be over shadowed by the larger peaks in our samples. Savchouk finds the shift luminescence peak to indicate the degree of hydrogenation. The peaks shift slightly, but since the peak at 1.38μm is not observed, no conclusions can be drawn from this data.

4.6 Waveguide Simulation Results

The waveguide simulator is used to investigate the effect of surface roughness and in particular the effect of the roughness height and width. For all simulated waveguides the x-y cross section of the incident field is that shown in Figure 4.10.

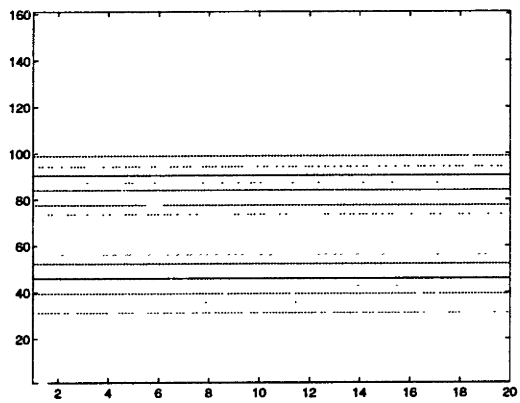


Figure 4.10: The input electric field used for simulating rough waveguides.

All waveguides are simulated in a 0.3 by 0.3μm window. The axes shown are the resolution in the x and y directions. All simulations have a resolution of 0.015μm (0.3μm/20) in the x direction and 0.0018μm (0.3μm/161) in the y direction.

The electric field profiles for a smooth surface and a rough surface after 1.5μm of propagation in the z direction are shown in Figure 4.11.

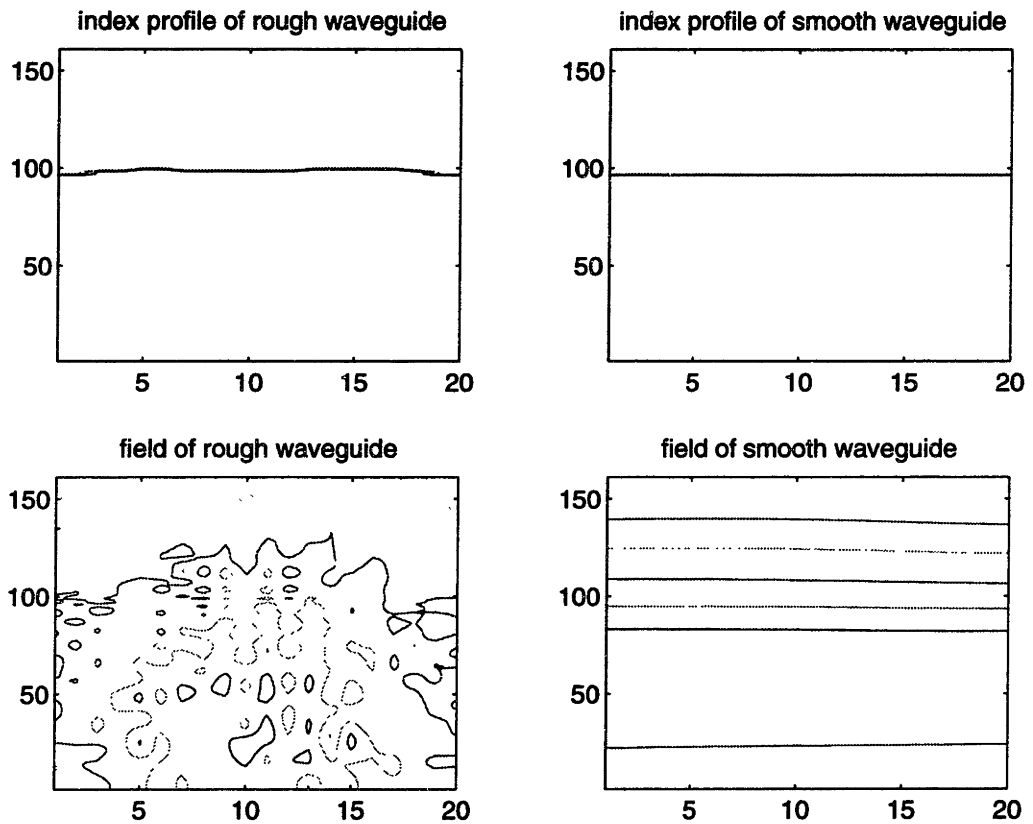


Figure 4.11: The top pictures shows the index profile cross section of the simulated smooth and rough surfaces at z = 1.5μm. The bottom graphs are the electric field profiles of these waveguides after propagation to z = 1.5μm.

The surface has 5 cells in the simulated window, a cell height of 4nm, and a maximum grain width of 0.3μm. Figure 4.11 shows that the smooth waveguide has an insignificant effect on the shape of the field. However, with the introduction of minor surface roughness, the electric field profile changes dramatically.

A power vs. distance curve can be found by integrating the power over the simulation window for different values of z. The power vs. distance of the simulated waveguides in Figure 4.10 are shown in Figure 4.12

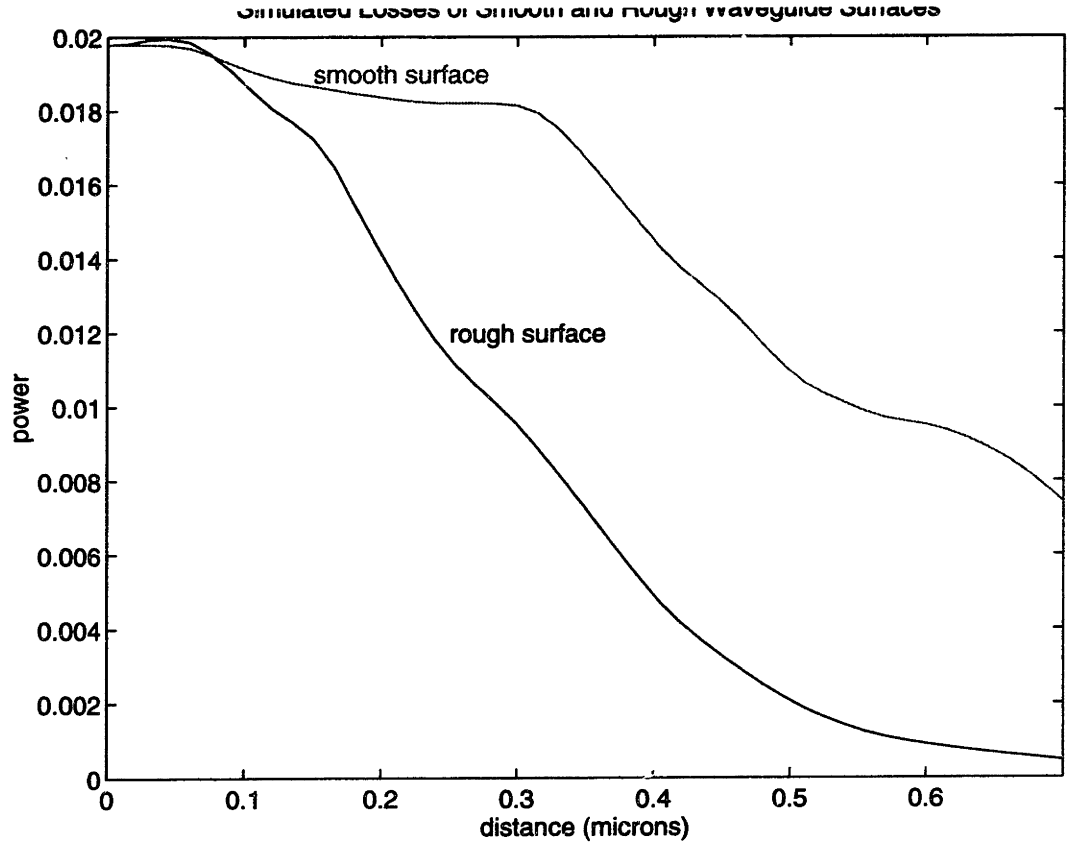


Figure 4.12: The power verses distance of the simulated waveguides in Figure 4.1. The red is the waveguide with peak to peak roughness of 4nm. The blue is the smooth waveguide.

Figure 4.12 shows that the rough surface causes the waveguide to lose light more rapidly than the smooth waveguide. The increase in loss is attributed to surface scattering.

We investigated effect of the waveguide height by holding all variables including cell width constant while varying the height of the cell. The cross sectional index of refraction profiles are shown below.

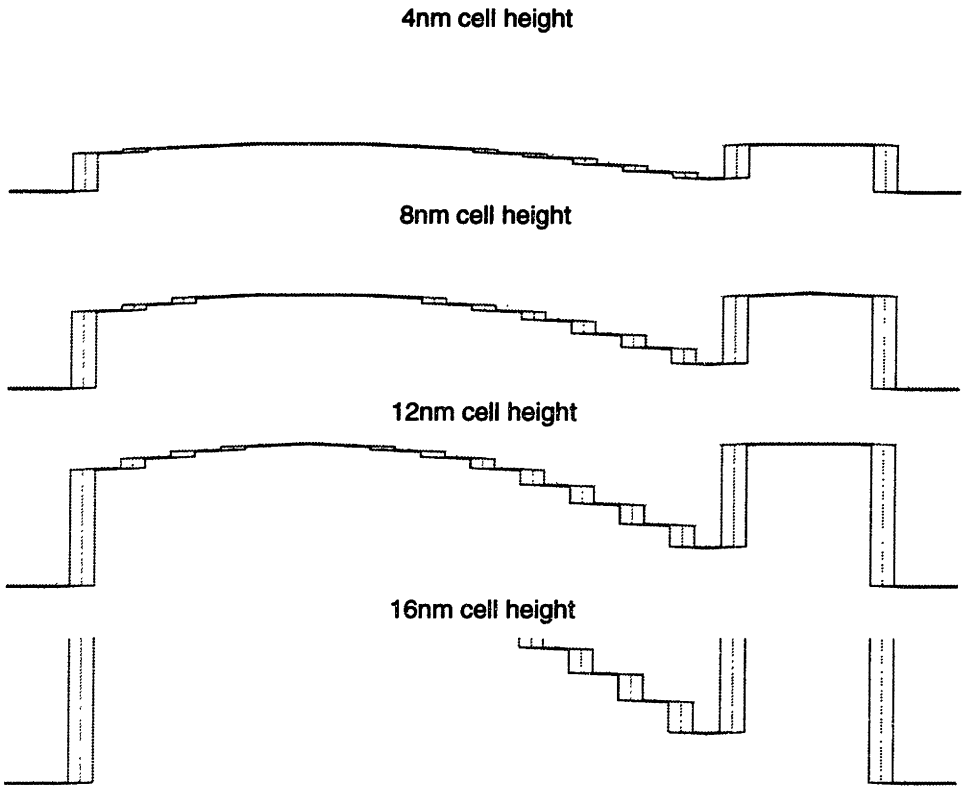


Figure 4.13: The index of refraction cross sections of the simulated waveguides with varying surface roughness height.

Cell heights of 4nm, 8nm, 12nm, and 16nm are simulated. The 16nm cells began to extend outside of the simulation window.

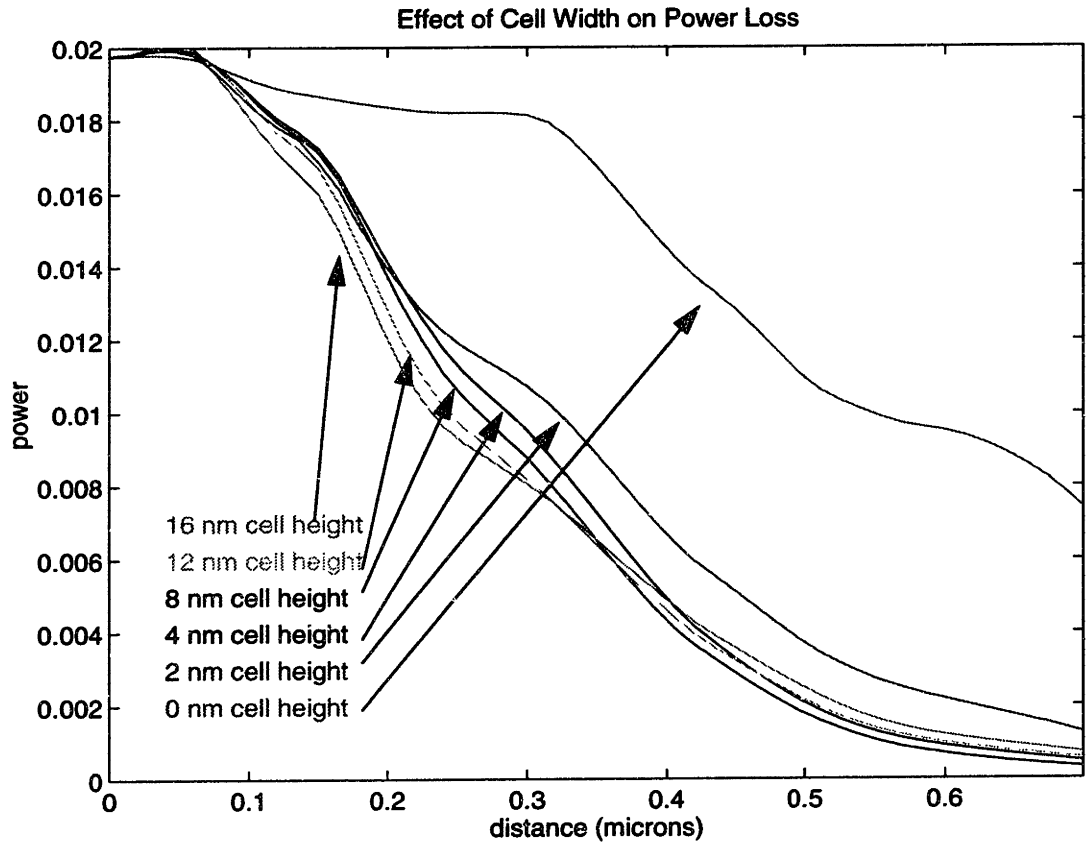


Figure 4.14: Simulated power vs. propagation distance is shown with varying the surface roughness cell height.

The power vs. distance for the simulated cell heights of 0, 4, 8, 12, and 16 nm are shown in Figure 4.14. The smooth waveguide is shown as a reference. All rough waveguides have similar losses, which are much larger than the losses in a smooth waveguide. As the cell height increases, the losses increase.

In addition to cell width, well height is investigated. In this experiment, all variables except the cell width are held constant.

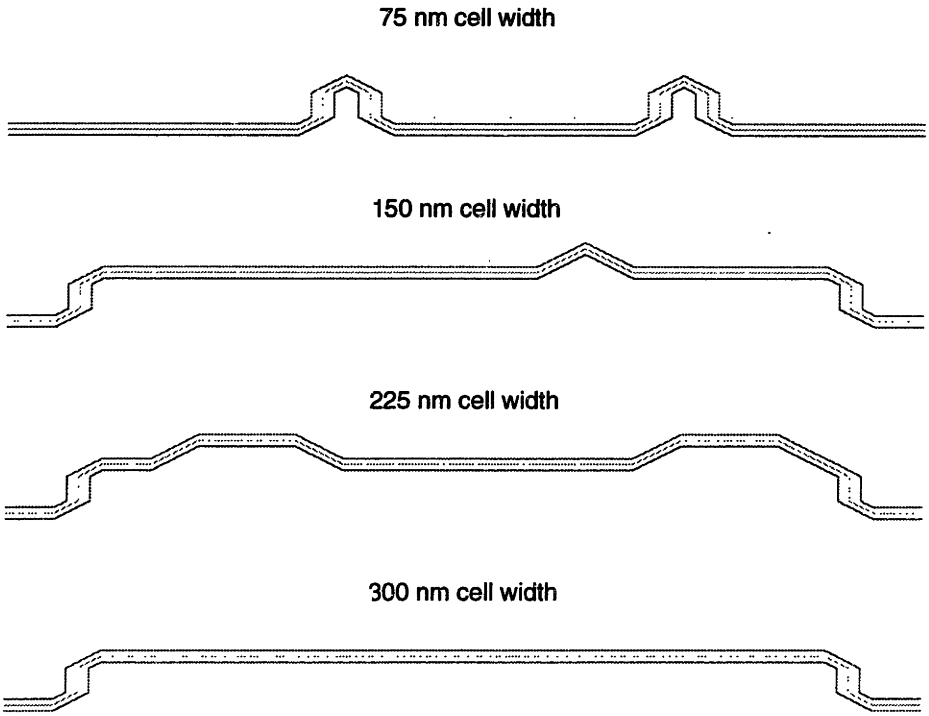


Figure 4.15: The effect of cell width is investigated. The widths of 75nm, 150nm, 225nm, and 300nm are shown. Each profile is 300nm long.

Figure 4.15 shows the four rough surfaces with varying cell width simulated. The height is selected to be 4nm with five cells per simulation. The cell widths simulated are close to the cell widths observed using AFM which were on the order of 300nm.

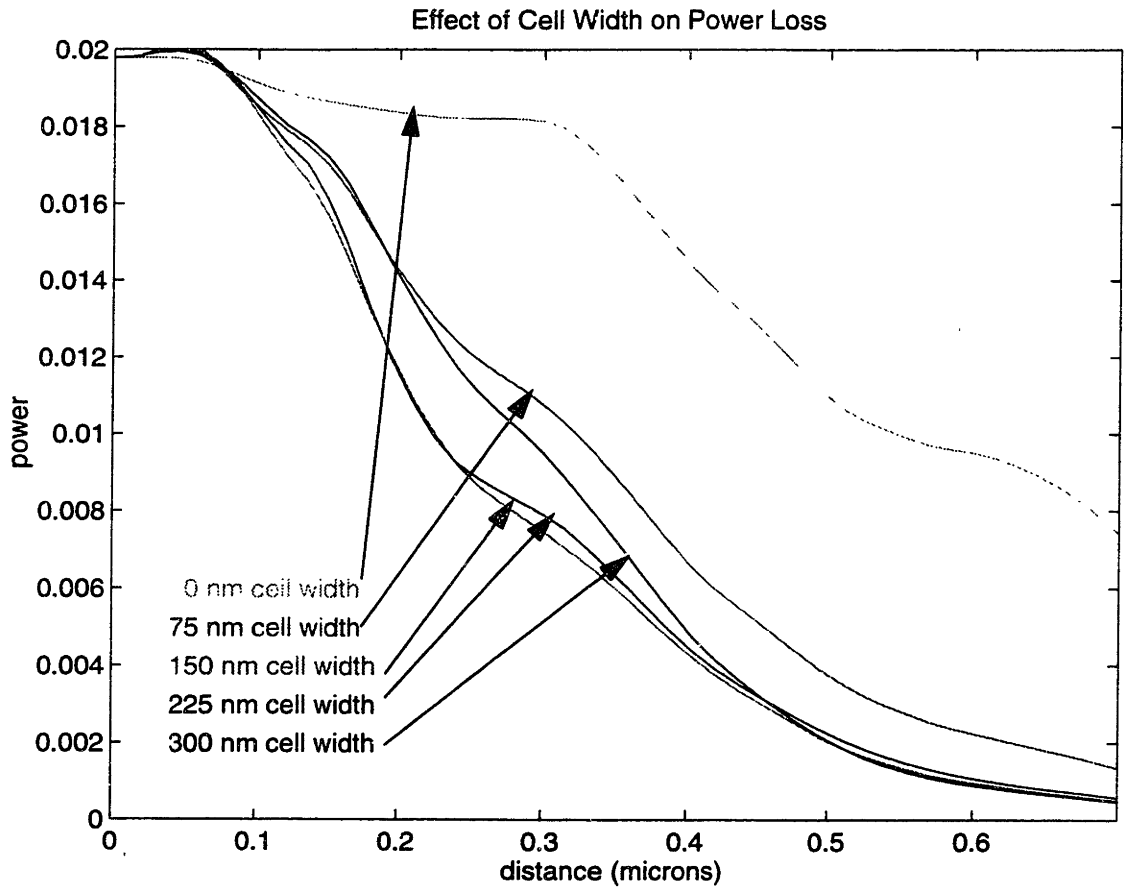


Figure 4.16: The power vs. distance of the simulated waveguides in Figure 4.4 are shown. The rough waveguides have varying surface widths and have a cell height of 4 nm.

The power vs. distance is shown for the surfaces with varying cell width. The power radiates out of the waveguide faster as roughness increases from 0nm to about 150nm. The rate of power loss decreases as the cell width is increased beyond 150nm. The increase with larger grains is seen because the simulation window is close to the cell width in this region. The cell then takes up the full window and so very little roughness is observed. This effect can be seen at the bottom of Figure 4.15 where the cell width equals the window. In this case the only roughness seen is at the edges where the roughness is forced to be 0.

Chapter 5

DISCUSSION

5.1 Surface Roughness

Surface roughness can be determined using reflectance and AFM. The loss due to surface roughness can then be estimated using Tien analysis. The calculated and measured losses and simulations are used to determine the effect of surface roughness to a polysilicon waveguide.

5.1.1 Surface Roughness from Reflectance Measurements

Using equation 3.4 the surface roughness vs. wavelength of the 560, 580, 625, CMP - 30, CMP - 60, and the hydrogenated samples are calculated.

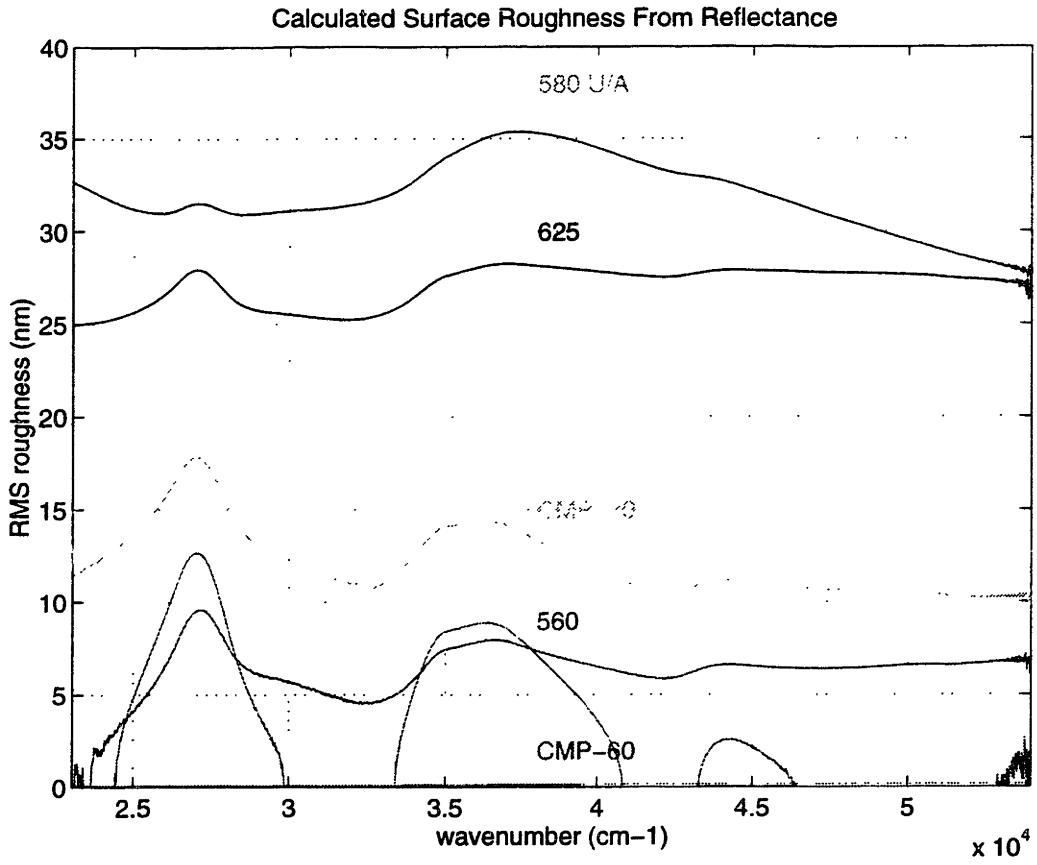


Figure 5.1: The RMS roughness is calculated from the reflectance measurements using equation 3.4.

Figure 5.1 shows the calculated roughness for the 560, 580, CMP, and 625 wafers vs. wavenumber. The region past 54,000 cm-1 is not shown since interference dominates this region. Slight variations in the calculated surface roughness are observed over wavelength. The increase in the calculated roughness around $2.7 * 10^4$ cm^{-1} and $3.6 * 10^4$ cm^{-1} is a result of the difference in crystallinity of the samples and the silicon wafer used as comparison. These increases are therefore not a reflection of the surface, but the result of the crystallinity in the bulk. Since the CMP-60 is almost as smooth as the reference sample, the calculated roughness is dominated by the peaks at $2.7 * 10^4$ cm^{-1} and $3.6 * 10^4$ cm^{-1}. The calculated roughness for the CMP-60 therefore could not be determined.

For the 580, the calculated roughness at wavelengths greater than $4 * 10^4$ cm^{-1} are very wavelength dependent. For the 625 at wavelengths greater than $4 * 10^4$ cm^{-1}, the surface roughness is greater than that predicted at smaller wavenumbers. The discrepancy at larger wavenumbers may be a result of the wavelength of light approaching of either the surface roughness height or the surface roughness width.

5.1.2 AFM vs. Reflectance Analysis

The route mean square roughness values obtained by AFM and estimated from reflectometry are repeated in Table 5.1.

Sample Type	RMS from AFM (nm)	RMS from reflectance(nm)	difference
625 annealed	20	27	7
580 annealed	15	31	16
580 unannealed	16	31	15
560 annealed	4	7	3
CMP 30 sec.	7	11	4
CMP 60 sec.	2	?	----------

Table 5.1: Comparison of Roughness Techniques

The AFM and reflectance measurements show consistency over the relative roughness of the samples; namely: 625 is the roughness, followed by CMP-30, followed by 560, and CMP-60 is the least rough. The 580 RMS roughness determined by the AFM and the reflectance algorithm differ considerably. Further more, the 560, CMP-30, and 625 RMS measurements differ between 4 and 7nm with the reflectance RMS always the greater. The

differences may be caused by the reflectance algorithm. In addition, if the "surface roughness is large and if the irregularities are closely spaced", the AFM might not have been able to follow the contours of the surface and underestimate the roughness.Since the reflectance measurements give RMS readings that vary according to the wavenumber used, the AFM measurements are judged to be the more reliable.

5.1.3 Tien Analysis and Comparison With Experimental Results

An estimate of power loss due to surface roughness can be preformed using equations 3.5 and 3.6 and assuming the bottom interface roughness to be zero. For the RMS surface roughness of 1.9, 3.7, 6.8, 14.9, and 20.1nm, A is calculated to be 0.054, 0.105, 0.194, 0.425, and 0.574 respectively. We can then calculate α from A and the values in section 2.1.b. The dB/cm is found by multiplying α by 10/(ln10). These values are shown in Table 5.2. The grain sizes are estimated from Figure 2.18 and are included on Table 5.2.

sample	AFM roughness (nm)	Calculated Tien loss (dB/cm)	Measured loss (dB/cm)	Bulk loss (dB/cm)	Estimated grain size (A)
625	20.1	54	77 +/- 5	23 +/- 5	400
580	14.9	30	71 +/- 7	41 +/- 7	800
560	3.7	2	37 +/- 6	35+/- 6	700
CMP-30	6.8	6	34 +/- 4	28+/- 4	400
CMP-60	1.9	0.5	----------	----------	400

Table 5.2: Comparison of Tien Analysis and Measured Losses.

Only the fundamental mode calculated losses are shown. The higher modes have dramati-

cally increased losses since their transmission occurs mostly close to the surface and they have a smaller θ'. Since the output of the optical fiber is about 4μm wide and the waveguides are 8μm wide, the light couples into many modes. We, therefore, expect a much higher loss than calculated. However, reflection at the end of the waveguide allows only the first few modes to be measured at the output while the higher order modes are reflected. Just as total internal reflection confines the light inside the waveguide while it is propagating, total internal reflection can confine light when the end of the waveguide is reached. Using the calculated critical angle of 23^{o} (see section 2.3.a.) and solving equation 2.2 for higher order modes we can show that even the first excited mode has an angle greater than the critical angle (25^{o}) and therefore, only the fundamental mode is measured at the output[31].

Even though Tien analysis is meant to be an approximation, it correlates well with the experimental results. The difference in the actual losses and the losses due to surface roughness are the losses from the bulk. One way of checking the accuracy of the Tien analysis is to compare the calculated bulk effect from two wafers with the same bulk and different surfaces. The CMP-30 and 625 have polysilicon deposited at the same temperature, but have different surface conditions. When the Tien loss of these samples is subtracted from the measured loss, the bulk losses are found to be equal to within 5 dB/cm. This accuracy validates the use of Tien analysis.

5.1.4 Simulation

Surface roughness has many different variables. The cell height, width, and density can all vary. Tien analysis and RMS readings lump all these degrees of freedom into one

variable thus limiting the accuracy of the results. Simulations have been written to take into account all these parameters.

The surface roughness simulations conclusively show that losses are greatly effected by surface roughness. In addition, the electric field profile is greatly modified when even very small roughness is incorporated into the simulation. The width and height variation simulations show that both the width and the height of the cells are important in determining losses. The losses increase with both the width and the height of the cells.

One could theoretically calculate the losses seen in the simulations. This loss can then be converted into the loss across the total waveguide by performing an overlap integration. In other words, the percentage of power located at the region simulated is multiplied by the losses from that region. This calculation could theoretically give an estimate of the losses due to surface roughness. However, a quantitative prediction of the losses is difficult. For one, the simulation program does not take into account back reflections. Any reflection outside of the x-y plane is not accounted for. For surface roughness, all scattering is extremely important. Secondly, the losses in the simulated window are so high that not enough cells are encountered to make the simulation statistically rigorous. Most importantly, the power vs. distance results change with resolution. The cause of the dependence on resolution was not determined, and by itself invalidates any numbers obtained by simulations. It should be emphasized, however that all these factors do not change the trends of increased losses with increasing cell height and cell width.

5.1.5 The dB/cm Caused by Surface Roughness in the 625 Sample:

By comparing the CMP-30 and the 625 wafer the surface roughness is shown to cause a loss of 43 +/- 9. In addition, the CMP-30 sample is not completely smooth so Tien anal-

ysis is used to estimate a further loss of 6 dB/cm due to surface roughness. The total estimated loss due to surface roughness on the 625 wafer is 49 dB/cm. Using this number, a perfectly smooth waveguide with same grain structure and dimensions as the 625 wafer is expected to have losses of 28 dB/cm. The 28 dB/cm not from surface roughness is probably loss from the grain boundaries in the polysilicon. Grain boundaries and grain structure are investigated in the next section.

5.2 Grain Boundaries

Absorption and scattering at the grain boundaries may result in the 28 dB/cm not accountable for by surface roughness. Tien analysis is used to factor out surface roughness from the measured losses. The difference between the measured and the surface roughness losses are assumed to be the bulk losses. Hydrogenation is performed to lessen these losses. Grain boundaries are found to cause waveguide loss, but further investigation is needed in this area.

5.2.1 Calculated Bulk Losses

The bulk losses can be calculated by subtracting the calculated losses from surface roughness from the measured total losses.

	unhydrogenated	hydrogenated	estimated grain size (A)
625	23 +/- 5*	10 +/- 8*	400

Table 5.3: Bulk Losses of Hydrogenated and Unhydrogenated Waveguides.

	unhydrogenated	hydrogenated	estimated grain size (A)
580	41 +/- 7	41 +/- 3	800
560	35+/-6	40 +/- 4	700
CMP	28 +/- 4	----------	400

Table 5.3: Bulk Losses of Hydrogenated and Unhydrogenated Waveguides.

Since the RMS from AFM and reflectance differed considerably for the 580 sample, the bulk losses may not be accurate. However, since the surface roughness is the same for the 580 hydrogenated and unhydrogenated, a comparison between these samples is accurate. The grain sizes are estimated from Figure 2.18. The bulk losses of the unhydrogenated samples are inversely related to the grain size.

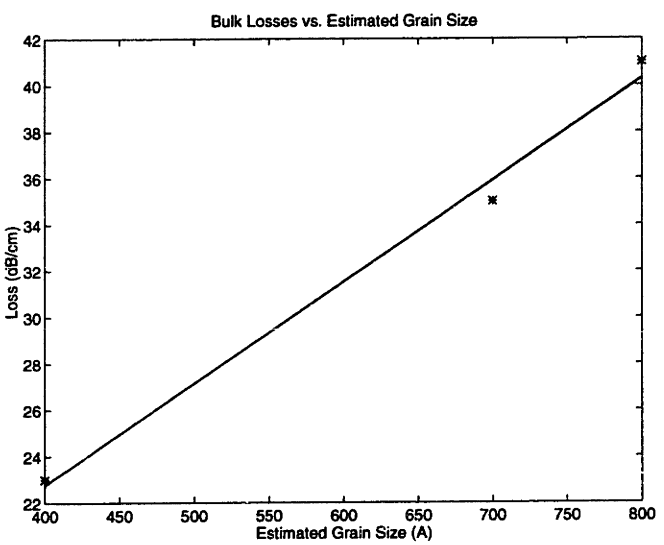


Figure 5.2: The bulk losses are shown to be inversely proportional to the grain size.

5.2.2 Hydrogenation

Hydrogenation improves the optical transmission of the 625 sample, indicating that the dangling bonds are partially passivated. The 580 and 560 samples show no conclusive change in the measured loss. The improvement in the transmission of the 625 and not the 560 or the 580 after hydrogenation is consistent with the samples grain boundary density. Since the 625 samples have smaller grains, they have a higher density of grain boundaries and hence dangling bonds. Hydrogenation should therefore have a larger effect on the 625 samples.

The hydrogenation could also passivate the dangling bonds at the surface. Since the 625 samples are rougher than the 560 samples, hydrogenation makes a larger difference. However, passivation of the surface of the 580, since the surface is rough, would decrease the losses, but no measurable effect is observed. The 560 losses hint at an increase in absorption.

The hydrogenation process used is found optimal for single crystalline silicon, but was later realized to be not ideal for polysilicon. In addition, hydrogenation is usually used to improve electrical characteristics which are surface dominated. The optical transmission properties are bulk dependent. This hydrogenation process is therefore not optimal for the purposes of this thesis and should be further optimized.

5.2.3 Optimal Grain Structure

Both the samples deposited at 625°C (625 and CMP) have lower bulk losses than the 560, indicating that either the different grain structure or the grain size plays a role in bulk losses. Since the 580 is expected to have similar grain structure to the 625 but larger

grains, the larger absorption of the 580 indicates the importance of grain size. If the grains are on the order of the wavelength of light in the material (0.44μm), a resonance can form. Low loss Ta_2O_3 waveguides require grain widths less than 0.5μm since this grain size probably causes excess scattering. Polysilicon 560 waveguides indicate a similar trend.

5.2.4 The dB/cm Caused by Dangling Bonds in the 625 Sample:

By comparing the 625 hydrogenated and unhydrogenated, around 10 dB/cm is shown to be eliminated by hydrogenation. By optimizing the hydrogenation process another 10 dB/cm improvement is expected. A total improvement of 20 dB/cm is expected by improving the bulk properties through hydrogenation.

5.3 Material Results

In the exploration of waveguide loss, some material results are also obtained. Since doped polysilicon is used in IC technology, it has been the focus of most of the research in polysilicon. This thesis however is only on undoped polysilicon. However, the trends observed for doped polysilicon appear to occur in undoped polysilicon as well.

5.3.1 Grain Size and Structure vs. Temperature

The TEM pictures in Figure 4.8 show the different grain structure of the as deposited polysilicon and transformed from amorphous polysilicon silicon. The columnar structure of the 625 confirms that the polysilicon formed at deposition. The 560 TEM shows the polysilicon crystallized during the anneal. The TEM pictures also give a qualitative esti-

mate of the grain sizes. 625 is shown to have much smaller grains than 560. In addition, assuming bulk losses are inversely proportional to grain size, the grain sizes vs. temperature correlates well with past work.

5.3.2 Polycrystalline vs. Amorphous Deposition:

Since the reflectance of the 560 before and after annealing changes only by the appearance of reflectance spectra around 26,000 and 37,000 cm^{-1}, we determine that the 560 is deposited as amorphous and then annealed into polysilicon just as the TEM pictures suggests. The 625 and 580 reflectance graphs change only slightly after the anneal indicating that both are deposited as polysilicon. For both the 580 and 625, small maxima are observed. Even though other research suggests the transition deposition temperature between polysilicon and amorphous silicon is around 600, the transition temperature is very dependent on temperature and impurities. 580 was expected to be deposited as amorphous, but not surprisingly is deposited as polysilicon.

5.3.3 Surface Roughness vs. Temperature

Our results show that surface roughness decreases greatly when depositing at low enough temperatures for amorphous deposition. The surface roughness dropped from 20nm to 4nm. The decrease in surface roughness corresponds with others' work on doped polysilicon[17, 20].

The surface roughness for the 580 is undetermined. The surface roughness calculated from reflectance is dependent on wavenumber and disagrees with the AFM measurement. Possibly an unusual shape of roughness occurs in this sample that invalidates the calculation of surface roughness from reflectance.

Chapter 6

CONCLUSION

The different types of losses in polysilicon waveguides are isolated in order to maximize transmission. Our polysilicon waveguides prior to this work had losses of 77 dB/cm. 43 dB/cm of the 77 dB/cm is shown to be from surface roughness. An additional 6 dB/cm is expected to be from surface roughness.

Grain structure is found to play an important role in waveguide loss as well. Experimental results indicate smaller grains are desirable. In addition, the grain boundaries can be passivated by hydrogenation. This hydrogen passivation reduces the losses by 10dB/cm and is expected reduce losses even further by another 10dB/cm. Further research in this area is needed to improve the hydrogenation process.

The trends of grain size, grain structure, and surface roughness with process conditions is shown to be the same for undoped polysilicon as for doped polysilicon. Grains are columnar in as deposited polysilicon and randomly orientated in transformed polysilicon. The grain size of the silicon deposited as amorphous and then annealed into polysilicon is much larger than the as deposited polysilicon. In addition the transformed polysilicon is smoother than the as deposited polysilicon.

A polysilicon waveguide with small grains, smooth surface, and passivated dangling bonds is found to be ideal. A waveguide of this type can be obtained by a fast deposition system which deposits smooth polysilicon with small grains. The waveguides can then be hydrogenated using a technique optimized for bulk polysilicon. A polysilicon waveguide fabricated using this technique is expected to have losses less than 10dB/cm [77 (deposited at 625oC) - 43 (losses shown to be from surface roughness) - 6(losses expected to be

from surface roughness) - 10(losses shown to be eliminated by hydrogenation) - 10(losses predicted to be eliminated by hydrogenation)]. In addition to providing low loss waveguides, the fast deposition system allows for high throughput, which is valuable on the production line.

Chapter 7

FUTURE WORK

1. Smooth Surface, Small Grains, and Hydrogenated Dangling Bonds

As mentioned in the conclusion, I believe that the lowest losses can be achieved by a structure with small grains, smooth surface, and hydrogenated dangling bonds. Smooth surfaces are shown to be obtainable from CMP, but many layers of smooth surfaces may be difficult to be achieved using CMP. In view of this challenge, other methods of obtaining smooth surfaces need to be investigated. One particular method that we believe is viable is a fast polysilicon deposition system which gives smooth surfaces and, in addition, small grains.Using a fast polysilicon deposition system followed by a hydrogenation step, we should be able to get waveguides with low losses.

2.Optimizing Hydrogenation

The hydrogenation method used in this work is found to be inefficient for the passivation of dangling bonds in polysilicon. By optimizing the hydrogenation, we expect to minimize the bulk losses. A promising method for polysilicon hydrogenation is using a high density plasma.

3. Cutback Loss Measurements vs. Wavelength

A loss vs. wavelength measurement could reveal more information on the polysilicon waveguides. For example, if the periodicity in the grain structure causes reflections, the loss vs. wavelength measurement will show an increase in loss at the wavelength which matches the periodicity of the grain structure.

4. Loss vs. Wavelength

The bulk losses may be either due to absorption or scattering. The measurements described in this thesis do not distinguish between these types of losses. However, Photo-ThermalDeflection Spectroscopy or FTIR measurements of absorption vs. wavelength could separate absorption from scattering.

5. TEM of 580

Reflection measurements lead us to believe that 580 is deposited as polysilicon which means that 580 is comprised of small grains. However, if 580 does indeed have small grain structure, the hydrogenation should reduce the losses as had occurred for the 625. In reality, when hydrogenation is performed, we see no observable reduction in the losses of 580. The conflicting experimental data prevent us from arriving on a consistent conclusion about the grain size and structure of 580. One possible way to clear up this would be to perform a TEM measurement on 580.

6.Explanation of 580 Roughness

Not only is the grain structure of the 580 undetermined, its roughness remains uncertain as well. The AFM and reflectance measurements of roughness differ greatly. In addition, the reflectance calculations, which would have been able to point us in the right direction, vary strongly with wavelength. Understanding these phenomena may provide further understanding of the roughness measurements.

7. Etch Chemistry

Once other loss mechanisms are eliminated, edge roughness may be a major cause of loss. If edge roughness does cause high losses, the etch chemistry can be modified to lessen edge roughness.

8. Polarization of Output Light

Further work should include measuring the polarizaion of the output light for several reasons. Polarization experiments may reveal information on the effect of grain structure and on the edge vs. surface roughness. In addition, if the detector in the optoelectronic system is polarization dependent, the polarization properties of the waveguide must be determined.

9.Electrical and Optical Properties

Investigate the correspondence between the electrical and optical properties as well as application of knowledge learned from polysilicon waveguides to other areas, such as solar cells.

10. Coupling Losses

Coupling losses may have information not obtained by other methods. Maybe coupling losses should be looked into.

11. Simulation Work

Since RMS measurements do not take into account the size and shape of surface roughness, simulations may reveal information that they do not. Simulations of bulk and surface scattering have been done for normal incidence.[31] Possibly a similar simulation can be done to model polysilicon waveguides.

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"Knowledge is as wings to man's life, and a ladder for his ascent."

-Baha'u'llah, Compilation on Baha'i Education

Appendix A

A.1 Code from simulator:

global variables:

```
      dimension widthx(100), widthz(100), xdir(100), zdir(100)
      common/poly/ widthx,widthz, xdir, zdir
      real*4 ran1
      integer xdir, widthx, widthz, zdir
```

reading in parameters:
and setting up inital grains

```
       else if (gtype.eq.'POLY') then
c    POLY:  to model Marcie's Poly waveguides with rough surface.
c
c                n0      effective index
c      gpar(1..3) = h1..h3   height in microns
c      gpar(4)    = hrand    height of rougness bump boundary
c      gpar(5)    = w        width of waveguide
c      gpar(6)    = nrandx   the roughness bump will be n points long
c        where n is a random number centered around
c        nrand.
c      gpar(7)    = sigma    the distribution of n (see above)
c      gpar(8)    = grains   number of grains across the whole xdirection
         read(22,*) n0
         do 345 iz= 1,8
           read(22,*) gpar(iz)
 345       continue
c      setting up inital grain points and widths
c      grains < 100 make error detection here to ensure this
          do 169 iz = 1,(gpar(8))
            widthx(iz) = ran1(iz - 101)*2*gpar(7)+gpar(6)-gpar(7)
            widthz(iz) = widthx(iz) * dx/cabs(dz)
            xdir(iz) = ran1(iz - 150) * nx +1
            zdir(iz) = (gpar(6)+gpar(7))*dx/(cabs(dz)*2)
```

```
 169      continue
      else if (gtype.eq.'JAY2') then
```

calling main poly procedure

```
      else if (gtype.eq.'POLY') then
        call gpoly(gpar(1),gpar(2),gpar(3),gpar(4),gpar(5),gpar(6),
     $      gpar(7),gpar(8))
```

main polyprocedure. This procedure is called for every z itteration

```
c*******************************************************
      subroutine gpoly(h1,h2,h3,hrand,w,nrandx,sigma,grains)
c*******************************************************
      include '3d.com'
      real*4 h1,h2,h3,w,hrand,nrandx,grains,sigma
c     sigma is the variation in grain width in dimensions of xresolution
      real*4 ran1,x,y,n,wi,rand,ratiozx
c     ran1 is the random procedure I coppied from a book.
c     ratiozx is used to convert zdim to xdim so width is the same.
c     I'm not sure if ratiozx works, since I always made it = 1 by setting
c     xres = zres.
      integer ix,iy,grain,widthx,widthz, xdir, zdir
      dimension widthx(100), widthz(100), xdir(100), zdir(100)
c     For each grain, a widthx is found randomly, the widthz is then calculated
c     The xdir is also selected randomly. And the zdir is set to half the
c     largest grain possible (nrandx + sigma) is terms of zresolution.
c     For each iteration in the zdimension, zdir subtracts one.  The grain
c     is at its maximum when zdir = 0.  Once the grain is completely passed
c     (zdir = -widthz/2) then the grain is erased and a new one is formed.
c     Periodicty is avoided by setting sigma > 0.  If sigma = 0, all grains
c     are the same width and therefore reset at the same time.
c     The grains are assumed to be parabolic all with the same height.
      common/poly/ widthx, widthz, xdir, zdir
ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
c                                                              c
c                3-D Semivectorial BPM                         c
```

```
c                                                                       c
c    Ridge waveguide, an example for uniform structurre                 c
c                                                                       c
c                      <----- w ----->                                  c
c                                                                       c
c                    ^^^^^^^^^^^^          | hrand                      c
c                  |                  |          !                    c
c        PolySi    |                  |          ! h3                  c
c                  |------------------|                                c
c        oxide     |                  |          | h2                  c
c          ---------------------------------------                      c
c      y ^  Si                                  !                      c
c        |                                      ! h1                   c
c        |------------------------------>-------                       c
c                                    x                                  c
c                                                                       c
ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc
      wi = (wx)/2.
      ratiozx = dx/cabs(dz)
c     update the grain points if they need to be. ie grain no longer is used
      print*,'widthz, zdir',widthz(2),zdir(2)
      do 240 grain=1,int(grains)
        if (widthz(grain)/2 + zdir(grain).lt.0) then
          zdir(grain) = (nrandx+sigma)*ratiozx/2
          widthx(grain) = ran1(grain-101- z*10)*2*sigma+nrandx-sigma
          widthz(grain) = widthx(grain) * ratiozx
c          print*,'widthx zdir',widthx(grain), zdir(grain),grain
          xdir(grain) = ran1(grain - 150 - z*10) * nx +1
        else
          zdir(grain) = zdir(grain) -1
        endif
 240  continue
      x= -dx
c     first grid point always no bump
      do 10 ix=1,nx
      x= x+dx
      rand = 0
c     calculating the rand value for this x and z
      do 239 grain=1,int(grains)
        if (((ix-xdir(grain))**2+(zdir(grain)/ratiozx)**2).lt.
```

```
     $       (widthx(grain)/2)**2) then
             rand =(((ix-xdir(grain))**2+(zdir(grain)/ratiozx)**2)*
     $          hrand*(-4)/widthx(grain)**2)+hrand
c    If the height is less than a resolutionin the y dir.  set it eyual to zres
             if (rand.lt.dy) then
               rand = dy*1.1
c    the 1.1 instead of 1 is just a hack because I don't know how to do
c    less than or equal.  This will make the less than only work.
             endif
             print*,'grain, rand',grain,rand
           endif
 239  continue
      if (ix.eq.1.or.ix.eq.nx.or.ix.eq.2.or.ix.eq.(nx-1)) then
        rand = 0
      endif
      y= -dy
      do 10 iy=1,ny
        y=y+dy
        if (y.lt.0.) then
          stop
        else if (y.lt.h1) then
          n = 3.5
        else if (y.lt.h1+h2) then
          if (abs(x-wi).lt.w/2) then
            n = 1.45
          else
            n = 1.45
          endif
        else if (y.lt.h1+h2+h3+rand) then
          if (abs(x-wi).lt.w/2) then
            n = 3.5
          else
            n = 1.45
          endif
        else
          n = 1.45
        endif
        dex2(ix,iy)=n*n*(1.,0.)
 10   continue
      return
```

```
end
```

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