A new architecture for high-frequency variable-load inverters

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A New Architecture for High-Frequency Variable-Load Inverters

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***Abstract*—Efficient generation and delivery of high-frequency (HF, 3-30 MHz) power into variable load impedances is difficult, resulting in HF inverter (or power amplifier) systems that are bulky, expensive and inefficient. This paper introduces a new inverter architecture and control approach that directly addresses this challenge, enabling radio-frequency power delivery into widely variable loads while maintaining efficient zero-voltage switching operation. We model the proposed architecture, develop design and control guidelines for it and analyze the range of load admittances over which it can efficiently operate and deliver a specified output power. The opportunities posed by the proposed approach are illustrated through time-domain simulations of an example HF inverter system.**

Keywords—antenna tuning unit; tunable matching network; HF; VHF; immittance converter; switched-mode power amplifier

I. INTRODUCTION

Many applications – ranging from industrial plasma generation to wireless power transfer – require inverters (or power amplifiers) that can deliver power at high frequency (HF, 3-30 MHz). Such applications often utilize ISM-band frequencies (e.g., 6.78 MHz, 13.56 MHz, 27.12 MHz), and can exhibit load impedances that vary over a wide range, including both inductive and capacitive components.

Addressing these applications at high efficiency is challenging owing to the constraints imposed by the combination of high-frequency operation and variable loading. Inverter designs at HF generally utilize fundamental-frequency inductive loading of the inverter transistor(s) to achieve the zero-voltage switching transitions necessary for high efficiency. For efficiency reasons, it is desirable to provide only the minimum amount of inductive loading necessary to support zero-voltage switching (along with the current needed to support the load.) Operating into a highly-variable load impedance (especially with both inductive and capacitive variations) makes it difficult to maintain this desired inductive transistor loading without requiring a large inductive circulating current, which itself can induce substantial loss. Loading variation can directly limit the achievable operating range and efficiency of an inverter system (e.g., [1]), and these constraints become increasingly severe as frequency and power rating increase.

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A commonly-used approach to addressing load impedance variations in such applications is to augment an inverter designed for a single load impedance (e.g., 50 Ohms) with a tunable matching network (TMN) that dynamically matches the variable load impedance to the fixed value desired for the inverter (e.g., [2,3]). Such TMNs realize the adaptive tuning using variable passive components, such as motor-driven mechanically-variable capacitors, switched capacitor banks, or high-power varactors. While this approach is very effective, allowing the inverter to operate at its designed operating point for all loads within the tuning range of the TMN, the TMNs themselves are generally expensive, bulky, slow and inefficient. An alternative to a tunable matching network is to design the load (e.g., including the plasma coils and matching system) such that a degree of self-compensation is provided; this can be accomplished with a set of matched loads and a resistance compression network, for example [4,5], but requires a specially-designed load network (e.g., a special set of plasma coils) which may not be practical in many cases. It would be much more desirable to have a high-frequency inverter system that can directly support a wide range of load impedances.

Here we propose a power delivery architecture and associated control approach that addresses this issue. It comprises a pair of inverters connected together and controlled in a way that each inverter always sees resistive / inductive loading, with the inductive loading component limited to that necessary for supplying any reactive component of the load current and realizing zero-voltage switching of both inverters. This new approach enables inverter systems that can directly provide efficient power delivery into highly variable load impedances. Section II of the paper introduces the proposed architecture and the basic operating method. Section III of the paper provides an analysis of the achievable load admittance range that can be driven as a function of inverter VA rating and desired output power. Section IV of the paper considers design and control for the proposed architecture, including inverter selection. Simulation results illustrating the operation of the proposed architecture are presented in Section V. Finally, Section VI concludes the paper.

II. THE HF VARIABLE-LOAD INVERTER ARCHITECTURE

The proposed architecture, illustrated in Fig. 1, comprises two inverters, with one directly coupled to the load and the other coupled to the load via an immittance converter [6]. We

focus on the variant in Fig. 1(a), although the alternative connection of Fig. 1(b) can be used to provide the same advantages in terms of inverter loading. (A difference between these dual implementations is that the variant of Fig. 1(a) is more suitable for supplying loads requiring large transient currents at limited voltage, while the variant of Fig. 1(b) is advantageous for supplying loads requiring large transient voltages at limited current.) In either case, one inverter (inverter "A") is directly connected to the load (with an output in series or parallel with the load), while the other inverter (inverter "B") is coupled to the load via an immittance converter (with one port of the immittance converter in parallel or series with the load). For modeling purposes and to explain the operation of the proposed architecture, we treat the inverters as ideal ac voltage sources having controllable amplitude and phase. In practice, one can utilize any type inverter suitable for HF operation under resistive/inductive loading; amplitude control of the individual inverters can be realized through any suitable means (e.g., supply voltage modulation, phase-shift or outphasing control, pulse-width modulation, etc.). The immittance converter serves to losslessly transform the voltage (current) delivered by inverter B at the first port of the immittance converter into an appropriately-scaled and phase-shifted current (voltage) at the second port of the immittance converter and vice versa, according to the following rule:

$$\begin{bmatrix} V_A \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & -j \cdot Z_0 \\ -j/Z_0 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_B \\ I_B \end{bmatrix} \qquad (1)$$

The characteristic of the immittance converter of swapping voltages and currents between its ports and consequently transforming between capacitive and inductive impedances is central to the operation of the proposed architecture. In practice, the immittance converter can be realized with a variety of passive lumped networks [4], and at sufficiently high frequencies can be realized with a quarter-wave transmission line.

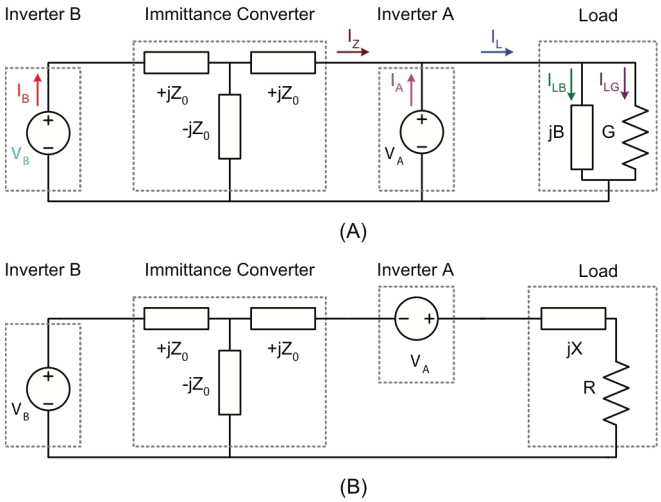

Fig. 1. (A) Structure of the proposed architecture. (B) An alternative connection having the same capabilities. Note that in the version with inverter A in series with the load, the location of inverter A and the load may be exchanged to make the inverter ground referenced.

The amplitudes and relative phase of the two inverters are used to control both the total output power and the effective loading admittance seen by each of the two inverters. (By effective loading admittance, we mean the complex ratio of current to voltage at an inverter output port with both inverters active.) In particular, we control the relative phases and amplitudes of the two inverters in a manner such that each inverter sees a resistive/inductive effective load regardless of the nature of the actual system load, facilitating zero-voltage switching (ZVS) of the inverters. It is noted that the classical Doherty rf power amplifier [7,8] also utilizes an immittance converter to combine power from two sources into a single output. However, whereas the Doherty architecture provides in-phase combining of power from linear power amplifiers into a specified resistive load (yielding resistive load modulation of the amplifiers), the present architecture utilizes both amplitude and phase shift control among switched-mode inverters to achieve both power control and desirable resistive / inductive loading of the constituent inverters across a wide range of load impedances.

For simplicity of explanation, we treat how the inverters are controlled in terms of the conductive and susceptive components of the load admittance. Which inverter supplies the susceptive component of the load current depends upon whether the susceptive component is inductive or capacitive. In the case where the load is inductive, the susceptive portion of the load current I_{LB} is provided by inverter A, while the conductive portion of the load current I_{LG} is split between inverters A and B. By contrast, when the load is capacitive, the susceptive portion of the load current is provided by inverter B (after processing through the immittance converter), while the conductive portion of the load current I_{LG} is split between inverters A and B. In each case, the relative phases of inverters A and B can also be set to ensure a degree of inductive loading for each inverter to provide soft switching. We treat each of these cases in turn.

The phasor relationship for the case where the load is conductive/inductive is shown in Fig. 2. The load voltage is directly set by the voltage of inverter A, with amplitude V_A set to a level sufficient to drive the desired average load power. (We arbitrarily assume a zero-phase reference for voltage V_A.) The phase of inverter B voltage V_B is set to an angle ($\theta_B + 90°$) ahead of V_A; owing to the action of the immittance converter, the current I_B lags V_B by θ_B, providing a degree of inductive loading for inverter B. We choose angle θ_B to be as small as possible commensurate with providing both inverters A and B with desirable operating waveforms (e.g., providing sufficient inductive currents to each for ZVS switching.) In the case where the inverters are designed such that they can achieve ZVS with a purely resistive load, θ_B can be set to zero. Owing to the action of the immittance converter, current I_Z leads V_A by θ_B. The amplitude V_B is selected such that the sum of the real components of I_Z and I_A are sufficient to support the necessary load conductance current I_{LG}. The imaginary component of I_A is negative, representing the difference between the susceptive component of the load current I_{LB} and the imaginary component of current I_Z. I_A thus lags V_A, providing inverter A with a degree of inductive loading. While the detailed achievable operating range will be established in the following

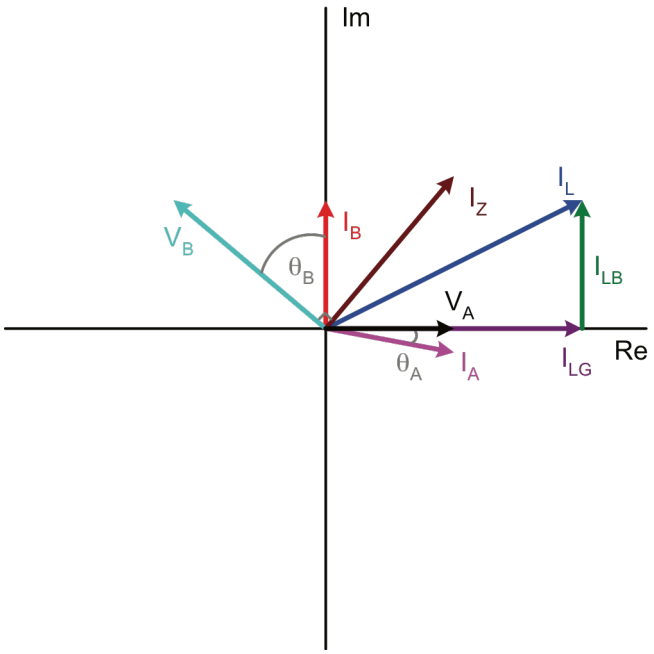

Fig. 2. Phasor diagram illustrating the voltage and current relationships in the network of Fig. 1(A) for a load having inductive susceptance.

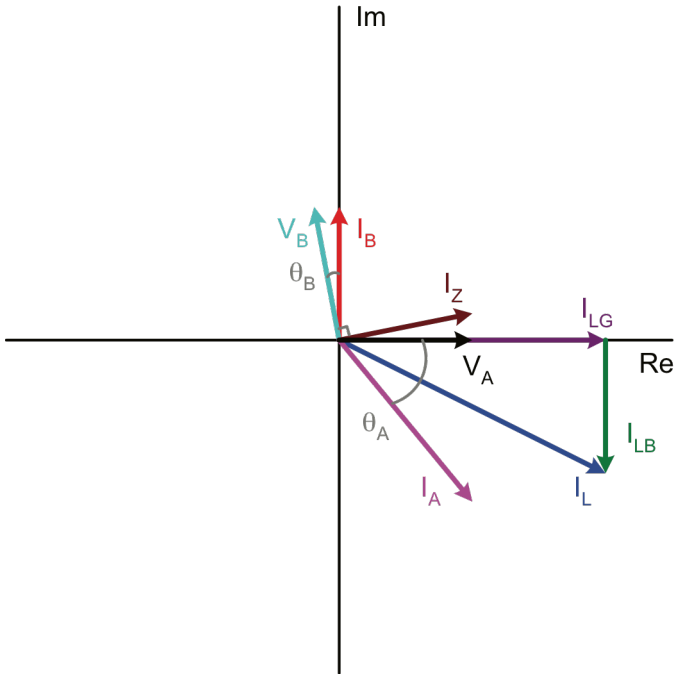

Fig. 3. Phasor diagram illustrating the voltage and current relationships in the network of Fig. 1(A) for a load having capacitive susceptance.

section, it can be seen that for any conductive or conductive/inductive load admittance, each of the two inverters can be provided with desirable loading conditions (e.g., for ZVS soft switching).

The case where the load is conductive/capacitive is shown in Fig. 3. The load voltage and output power are again set by the voltage of inverter A, and the phase of inverter B voltage V_B is likewise set to an angle (θ_B + 90°) ahead of V_A. In this case, however, the phase θ_B is selected in conjunction with the amplitude of V_B such that the imaginary component of related current I_Z provides the susceptive portion of the load current I_{LB} along with any necessary additional current to enable soft switching of the two inverters. Owing to this additional (imaginary axis) current, the phase of current I_A lags V_A by a small amount (θ_A), providing an inductive loading component to inverter A. Likewise, phase θ_B provides a sufficient inductive loading component for inverter B. (If the inverters are designed to achieve desired operation into a resistive load, θ_B can be selected such that θ_A is zero, making current I_A in phase with V_A.) As can be seen from Figs. 2 & 3, by utilizing the appropriate controls, loads with either capacitive or inductive susceptive components can be supplied with the proposed system while maintaining resistive/inductive loading of each inverter (e.g., for ZVS soft switching). Section IV introduces a more detailed control strategy by which the above goals can be realized.

III. Achievable Operating Range and System Design

Of interest in the proposed architecture is the achievable load admittance range that can be driven as a function of inverter VA rating and specified output power. Here we focus on the symmetric case in which the two inverters are identical, each with an ac output current amplitude rating I_M and ac output voltage amplitude rating V_M, and with a characteristic impedance of the immittance converter of $Z_0 = V_M/I_M = 1/Y_0$. Each inverter thus has an ideal rated output power of $P_{r,i} = ½ \cdot V_M \cdot I_M$, though this output power is only achievable into a single effective load impedance. (Consequently, we typically operate at system power levels well below $P_{r,i}$.)

Here we develop an analytical treatment of the range of load admittances that can be driven within inverter operating limits as a function of the desired output power (normalized to the power rating of a single inverter $P_{r,i}$). We start by establishing the load conductance range over which a single inverter can drive a desired average power P assuming zero susceptance. Equations 2 and 3 show the required load voltage amplitude $|V_{OUT}|$ and conductive load current amplitude $|I_G|$ necessary to drive power P as a function of conductance G.

$$|V_{OUT}| = \frac{\sqrt{2P}}{\sqrt{G}} \tag{2}$$

$$|I_G| = \sqrt{2P} \cdot \sqrt{G} \tag{3}$$

These relationships are illustrated in Fig. 4, along with constraints on inverter voltage and current. G_{MIN} denotes the *minimum* load conductance for which power P can be delivered within the specified inverter voltage rating V_M. For lower conductances, power P cannot be delivered without exceeding the inverter voltage limit. Likewise, G_{MAX1} is the maximum load conductance for which a single inverter can deliver sufficient current to drive power P within inverter current rating I_M. Given that two inverters are available to deliver power, there is an extended load conductance range over which a specified power P could be delivered by the system. G_{MAX2} shows the maximum conductance for which both inverters

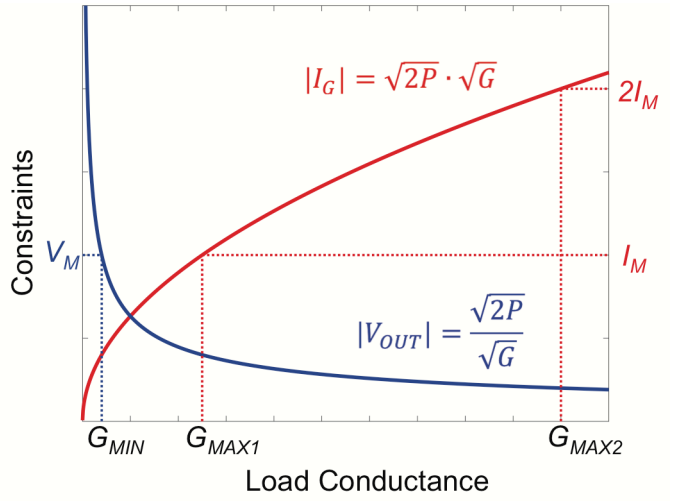

Fig. 4. Voltage and current constraints determining allowable inverter operating range as a function of load conductance. The left vertical axis (blue curve) shows the voltage constraint, and the right vertical axis (red curve) shows current constraints.

operating together could deliver the current required to provide power P (at zero susceptance). These load conductance values can be found to be:

$$G_{MIN} = \frac{2P}{V_M^2} \qquad G_{MAX1} = \frac{I_M^2}{2P} \qquad G_{MAX2} = 4\frac{I_M^2}{2P} \tag{4}$$

Evidently, the real part of the load admittance range that can be supported is defined by G_{MIN}, G_{MAX1} *and* G_{MAX2}. To find the complete admittance range that is supportable, we first consider the typical case of power levels $P \le P_{r,i}$, for which $G_{MIN} \le G_{MAX1} < G_{MAX2}$. For operation between G_{MIN} and G_{MAX1}, we are not constrained by voltage, and the real (conductive portion) of load current can be completely supported by one of the two inverters. This leaves the second inverter to support the susceptive portion of load current up to its maximum rated current I_M. Based on the current delivery constraint of the second inverter, we can provide the necessary current for susceptances having magnitudes up to a value B_{MAX}:

$$|B_{MAX}| = \frac{I_M}{\sqrt{2P}} \cdot \sqrt{G} \tag{5}$$

At G_{MIN}, we find that $|B_{MAX}| = Y_0 = 1/Z_0$.

Operating between G_{MAX1} and G_{MAX2}, current contributions from both inverters are needed to support the conductive component of the load current; this leaves a portion of current from one of the inverters remaining to support susceptive load components, which may be shown to yield a maximum susceptance amplitude for this range of conductances:

$$|B_{MAX}| = \sqrt{\frac{G}{2P} \cdot (2I_M\sqrt{2PG} - 2PG)} \tag{6}$$

When load conductance G reaches G_{MAX2}, all available current is being delivered to the load conductance, and the achievable susceptance is zero. These results are plotted in Fig. 5.

To further delineate the achievable operating range, we find the largest susceptance magnitude that can be driven while providing power P to the load conductance. We denote this susceptance magnitude as B_{BP}, and the load conductance (between G_{MAX1} and G_{MAX2}) at which this peak susceptive drive capability is reached as G_{BP}. Differentiating (6) with respect to G and setting this derivative to zero yields:

$$B_{BP} = \frac{3\sqrt{3}I_M^2}{8P} \qquad G_{BP} = \frac{9I_M^2}{8P} \tag{7}$$

This boundary result is likewise indicated in Fig. 5.

It will be appreciated that the range of load admittances that can be driven is a function of average power P, with lower power corresponding to a wider region of admittances. The achievable operating range of load admittances that can be driven (normalized to Y_0) is illustrated in Fig. 6 for specified output powers of 0.5, 1 and 1.5 times $P_{r,i}$. It can be seen that the load admittance range that can be driven increases rapidly with reductions in commanded power (or, equivalently, with increases in the volt-ampere ratings of the inverters relative to a desired output power). The boundaries of the operating region are directly linked to inverter constraints; for example, the vertical boundary of a minimum load conductance directly expresses the voltage output limit of inverter A and current output limit of inverter B, while the boundaries to the right reflect complementary constraints. At power levels below $P_{r,i}$, $G_{MIN} < G_{MAX1}$, and the region is delineated just as illustrated in Fig. 5, with the area encompassed diminishing as P increases. At $P = P_{ri}$, $G_{MIN} = G_{MAX1}$, while for higher values of P, $G_{MIN} > G_{MAX1}$, such that the inverter voltage limit increasingly constrains the achievable admittance region. The area of allowable admittances continues to decrease with increasing power, collapsing to a single point $Y = 2Y_0$ at $P = 2P_{r,i}$. These same constraints on allowable load range as a function of power can be expressed as regions of the load impedance plane

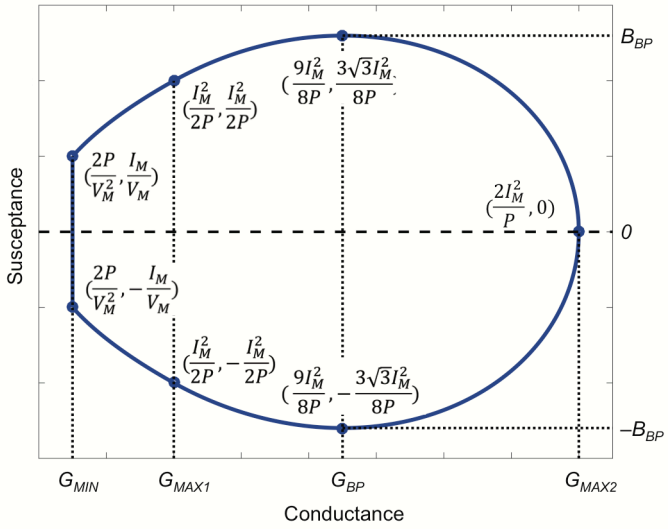

Fig. 5. The region of the load admittance plane that can be driven by the system of Fig. 1(a) for resistive/inductive loading of each inverter, assuming an output power level $P \le P_{ri}$.

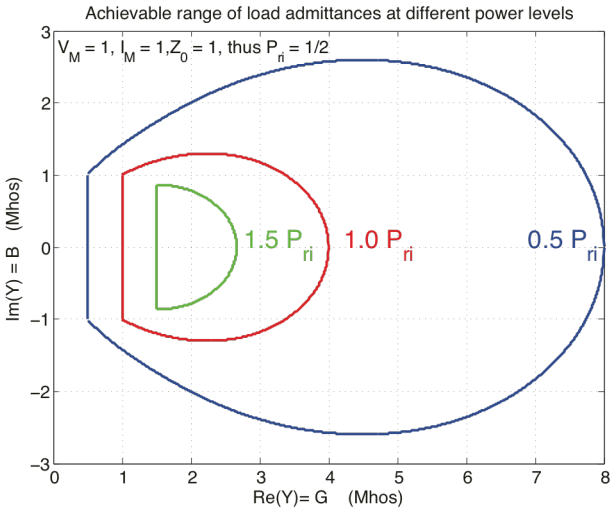

Fig. 6. The regions of the load admittance plane that can be driven by the system of Fig. 1(a) for different normalized output power levels. Results are shown normalized to a characteristic admittance $Y_0 = 1$.

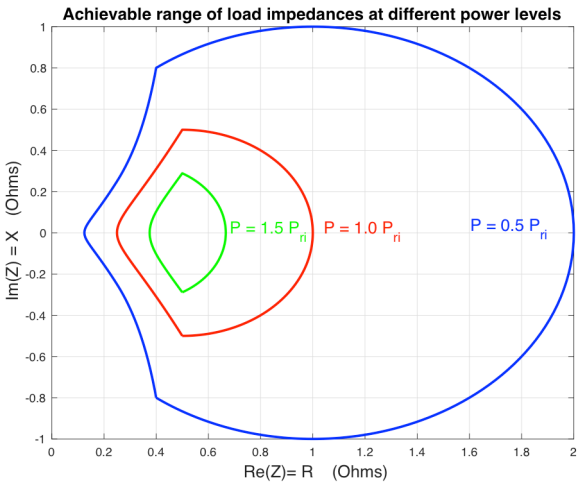

Fig. 7. The regions of the load impedance plane that can be driven by the system of Fig. 1(a) for different normalized output power levels. Results are shown normalized to a characteristic impedance $Z_0 = 1$. This plot reflects the same operating boundaries as Fig. 6.

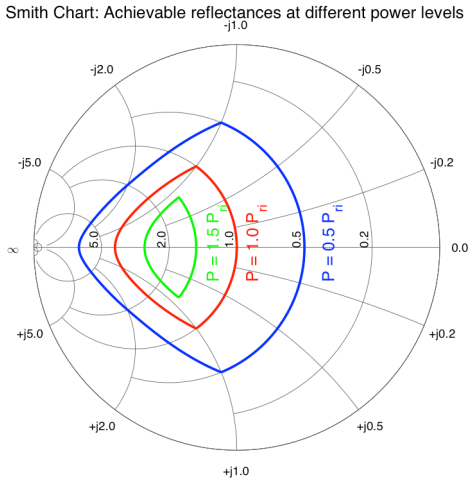

Fig. 8. Achievable operating ranges for the system of Fig. 1(a) for different normalized output power levels as expressed in a Smith chart (illustrating reflectance and admittance). Results are shown normalized to a characteristic admittance $Y_0 = 1$. This plot reflects the same operating boundaries as Figs. 6 and 7.

(Fig. 7), or in a Smith chart (Fig. 8).

It can be observed that the admittance regions encompassed in Figs. 5, 6 and 8 are symmetric about zero susceptance, and the impedance regions in Figs. 7 are symmetric about zero reactance. The operating ranges can made nonsymmetric by inclusion of "offset" reactance(s) in shunt and/or series with the load, though we do not treat the details here. It should be noted that the operating boundaries indicated in Figs. 5-8 assume the use of inverters which operate well under all of pure resistive, pure inductive, and combination resistive/inductive loading. Thus, to meet these boundaries, the inverters must be able to efficiently supply a purely resistive load; inverters requiring external inductive loading can be accommodated by adjusting the relative inverter phases such that each inverter sees a sufficient inductive load through action of the immittance converter (as illustrated in Figs. 2 and 3), while incurring a degree of reduction in the operating boundaries. In the remainder of the paper, we assume that the inverters are designed to operate with any combination of resistive and inductive loading within their voltage and current ratings.

IV. System Design and Control

There are many high-frequency inverter designs that can operate well within the constraints of resistive / inductive loading described above. One option is a ZVS class D or class DE inverter [9,10] having either a matching network or inductive pre-load network such that it can operate with soft switching into a variable resistive/inductive load. Another option is an appropriately-designed single-switch inverter (e.g., class E, class Φ_2, etc.). While "classical" Class-E inverter designs impose significant constraints on loading to maintain ZVS operation (e.g., [11-13]), some single-switch inverters are suitable for variable-load operation. In particular, the variable-load class E design introduced [14] can operate with low loss across a wide range of resistive, resistive/inductive and inductive loads. (While [14] only explicitly treats design for variable load resistance, the resulting inverter designs can maintain ZVS and low loss for resistive/inductive and pure inductive loads as well, so long as the active switch has an antiparallel diode or equivalently provides reverse conduction.) Modulation of the individual inverter output amplitudes (as necessary for the proposed architecture) is most easily realized by modulating the inverter supply voltages (i.e., using dc-dc converters to vary the inverter dc supplies, also known as "drain modulation"), though other means are also possible.

The operating points on the boundaries of Figs. 5-8 reflect the most extreme loads that can be driven at the specified power levels by inverters operating within maximum peak ac voltage and current ratings V_M and I_M. As such, there is typically only one set of control commands (inverter amplitudes and phases) that can support these operating points. By contrast, there are many combinations of amplitudes and phases that can support many interior points (as one could divide power between the two inverters in various ways for

these interior points.) This, in turn, means that there are multiple ways the system can be controlled to achieve the desired output. Here we propose one possible control strategy.

We express the proposed control strategy based on in-phase and quadrature components of the inverter A and inverter B voltage commands; this I/Q representation carries the same information as the magnitudes and phases of the inverter voltages. We define the I/Q relationships such that the quadrature component for each inverter leads its in-phase component by 90°, and the in-phase component of inverter B leads that of inverter A by 90°. We arbitrarily define the in-phase component of inverter A (V_{AI}) to be the desired output voltage phase reference such that the voltage of inverter A is defined by its in-phase component and has zero quadrature component ($V_{AQ} = 0$). We define the in-phase component of inverter B (V_{BI}) as leading the in-phase component of inverter A by 90°. Thus, in terms of phasors, $\boldsymbol{V_A} = V_{AI}$ and $\boldsymbol{V_B} = -V_{BQ} + jV_{BI}$. To achieve the desired control goals, we select the in-phase and quadrature components of the two inverters as shown in Table I. This control algorithm (supported by appropriate measurements and feedback compensators) can provide the desired output and inverter loading characteristics across the operating range.

Fig. 9 shows the resulting inverter voltages and current phasors with this control algorithm for six of the boundary operating points indicated in Fig. 5 (six load admittances at $P = 0.5 \cdot P_{ri}$ with normalized inverter ratings $V_M = 1$, $I_M = 1$ and $Z_0 = 1$). The relationships between inverter A voltage (V_A) and inverter B current (I_B), and inverter B voltage (V_B) and immittance converter output current (I_Z) are apparent. It can be seen that both Inverters A and B maintain resistive/inductive loading for all operating points. Moreover, it can be seen that any capacitive component of load current is provided by inverter B through the immittance converter, while any inductive component of load current is provided directly by inverter A.

TABLE I. CONTROL METHOD BASED ON SETTING IN-PHASE AND QUADRATURE COMPONENTS OF THE INVERTER VOLTAGES TO ACHIEVE THE DESIRED OUTPUT POWER AND INVERTER LOADING CHARACTERISTICS

V_{AI}	Set amplitude (within $0 \le V_{AI} \le V_M$) to achieve desired reference output power $P_{o,ref}$. (V_{AI} is thus used to set output power.)
V_{AQ}	Set to zero (by definition of the desired phase of V_A)
V_{BQ}	Set within $0 \le V_{BQ} \le V_M$ to drive I_{AQ} to zero. (V_{BQ} is thus used to drive any capacitive component of inverter A loading to zero, and becomes zero when the load is inductive.)
V_{BI}	Set within $0 \le V_{BI} \le (V_M^2 - V_{BQ}^2)^{1/2}$ to drive I_{AI} towards 0^+ limited by the requirement on V_{BQ} above and by the allowed total operating voltage of inverter B. (V_{BI} is thus set such that inverter B will deliver as much of the real component of the output power as possible within the voltage rating of inverter B and while maintaining the current sourced by inverter A to be zero or positive.)

V. DEMONSTRATION

Here we present LTSPICE simulation results illustrating the proposed approach. Figure 10 shows the simulated 13.56 MHz inverter system; component values are shown in Table II. The ZVS class D inverters (operated with 11 ns switching deadtime) utilize an inductive preload network to provide ZVS soft switching under resistive or resistive/inductive loading. The immittance converter has a characteristic impedance of 10 Ω and is realized as a T network. (Notional values for V_M and I_M are 100 V and 10 A, respectively, though these are only

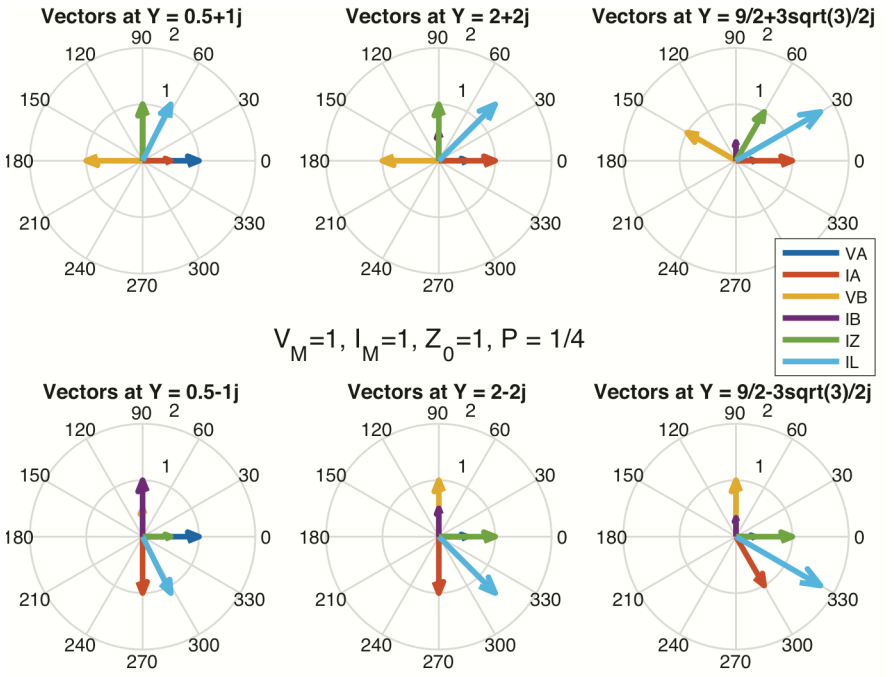

Fig. 9. Phasor representations of system voltages and currents for different load admittances with $V_M = 1$, $I_M = 1$, $Z_0 = 1$ and $P = 0.5 \cdot P_{ri} = 0.25$ using the control approach specified in Table I. The load admittances correspond to some of the boundary operating points specified in Fig. 5.

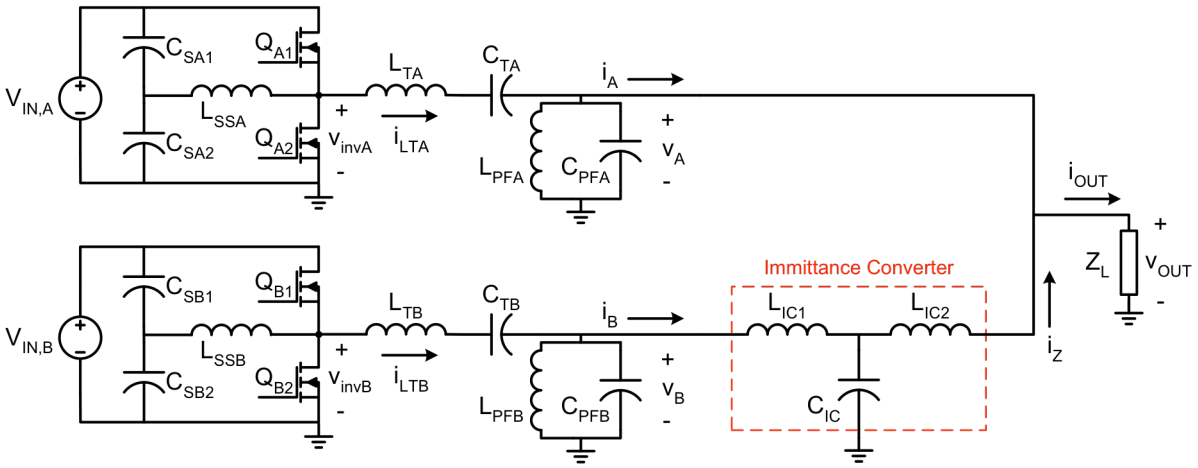

Fig. 10. An example implementation of the proposed architecture based on ZVS class D inverters with inductive preload networks and a lumped "T" implementation of the immittance converter. Component values for operation at a switching frequency of 13.56 MHz are shown in Table II.

approximate in practice.) The inverter devices are modeled as having 50 mΩ on-state resistance and 400 pF output capacitance, commensurate with available devices. The inverters are each provided with series and parallel filter networks tuned at the switching frequency for harmonic reduction. The dc input voltages and relative switching phases of the two inverters are dynamically varied to control the system.

Figure 11 shows example simulation results for this system; the black and cyan traces are the unfiltered outputs of the ZVS soft-switched inverters A and B, and the magenta and red traces are their respective currents (providing resistive and/or inductive loading of the inverters). The output (load) voltage is shown in dark gray. The top plot shows operation with a resistive/capacitive load comprising a 5 Ω resistor in parallel with a 2.34 nF capacitor (representing an admittance of approximately 0.2 +0.2j). This operating point is achieved with dc input voltages $V_{IN,A}$ = 80 V and $V_{IN,B}$ = 160 V, with the fundamental output voltage component of inverter B leading that of inverter A by ~180°. The bottom plot shows operation for a resistive/inductive load comprising a 5 Ω resistor in parallel with a 58.7 nH inductor (representing an admittance of approximately 0.2-0.2j). This operating point also utilizes dc input voltages $V_{IN,A}$ = 80 V and $V_{IN,B}$ = 160 V, but with the fundamental output voltage component of inverter B leading that of inverter A by ~90°. These two operating points correspond approximately to those of the middle column in Fig. 9 (with values appropriately renormalized for V_M, I_M and Z_0).

TABLE II. COMPONENT VALUES FOR THE EXAMPLE INVERTER SYSTEM OF FIG. 10

$V_{IN,A}$, $V_{IN,B}$	0-160 V_{DC}
C_{SA1}, C_{SA2}, C_{SB1}, C_{SB2}	1μF
L_{SSA}, L_{SSB}	100 nH
Q_{A1}, Q_{A2}, Q_{B1}, Q_{B2}	R_{ON}=50mΩ C_{OSS}=400pf
L_{TA}, L_{TB}, L_{PFA}, L_{PFB}	470nH
C_{TA}, C_{TB}, C_{PFA}, C_{PFB}	294pF
L_{IC1}, L_{IC2}	117nH
C_{IC}	1.17nF

It can be seen that zero-voltage switching of each inverter is maintained for both the resistive/capacitive and resistive/inductive load cases. Moreover, the output waveforms match well with the underlying theory. For the resistive/capacitive case, the ac output voltage has a peak value of 48.6 V and the system delivers 234 W, while in the resistive/inductive case the peak ac output voltage is 48.8 V, and the system delivers 238 W. These simulation results illustrate the ability of the proposed architecture to operate with a wide range of load impedances including both capacitive and inductive loads, and show how such a system might work with practical inverter designs.

VI. CONCLUSION

This paper introduces an inverter architecture and associated control approach for providing efficient delivery of high-frequency power into variable load impedances while maintaining resistive/inductive loading of the constituent inverters for ZVS soft switching. The proposed architecture is analyzed, and the region of load admittances over which it can efficiently operate within inverter constraints is determined as a function of output power. A control algorithm is proposed that achieves the output control goals (delivering the specified output power while preserving desired inverter loading characteristics) for loads within the achievable range. The opportunities posed by the proposed approach are illustrated through time-domain simulation of an example HF inverter system. It is hoped that the proposed approach will enable more compact and efficient generation of high-frequency power for applications in which load admittance varies over a wide range.

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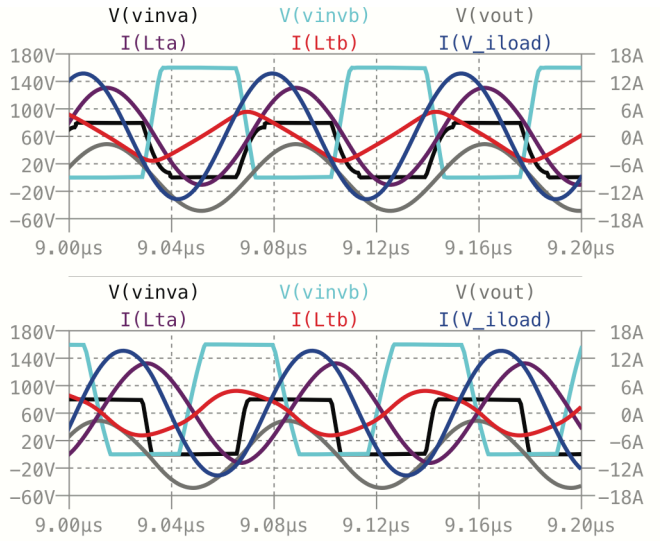

Fig. 11. LTSPICE Simulations showing the behavior of the inverter system of Fig. 10 and Table II. This system operates at 13.56 MHz with a system characteristic admittance of Y_0=0.1. The top plot shows operation for a resistive/capacitive load comprising a 5 Ω resistor in parallel with a 2.34 nF capacitor (representing an admittance of approximately 0.2 +0.2j). The bottom plot shows operation for a resistive/inductive load comprising a 5 Ω resistor in parallel with a 58.7 nH inductor (representing an admittance of approximately 0.2-0.2j).

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