Design and Evaluation of a Reconfigurable Stacked Active Bridge dc/dc Converter for Efficient Wide Load-Range Operation

by

Rose Abramson

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Abstract

This thesis presents the design and implementation of a step-down soft-switched dc-dc converter based on an active bridge topology which overcomes some of the limitations of the conventional dual-active bridge (DAB). The topology comprises a double-stacked bridge inverter, coupled to a reconfigurable rectifier through a special three-winding leakage transformer. The converter can run in a low power mode that greatly increases light-load efficiency by reducing core loss and extending the zero-voltage switching (ZVS) range. The converter is implemented with a single compact magnetic component, providing power combining, isolation, and energy transfer inductance.

The theory of the converter and its various operating modes, referred to in this thesis as the Double-Stacked Active Bridge converter, is also explored, and a magnetic model of the special three-winding transformer and leakage inductance is presented. The target application is for 380 V dc distribution systems for data centers, where the converter operates for the majority of the time at the nominal input voltage, but must have high efficiency over a wide load range. A 175 kHz, 300 W, 380 V to 12 V prototype converter achieves 95.9% efficiency at full load, a peak efficiency of 97.0%, an efficiency above 92.7% down to 10% load and an efficiency above 79.8% down to 3.3% load.

Thesis Supervisor: David J. Perreault
Title: Professor of Electrical Engineering and Computer Science

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Chapter 1

Introduction

This thesis presents the design and implementation of a step-down soft-switched dc-dc converter, using a double-stacked active bridge inverter coupled to a reconfigurable rectifier through a special three-winding leakage transformer. The Double-Stacked Active Bridge topology (or DSAB topology, as it is referred to in this thesis), is designed to address some of the challenges of the traditional full-bridge dual-active-bridge (DAB) converter, such as its decreased efficiency at low loads due to the loss of ZVS. The DSAB converter can run in a low power mode that greatly increases light-load efficiency by reducing core loss and extending the ZVS range.

A single compact magnetic component is used to implement the three-winding transformer and leakage inductance required for the DSAB topology. This single component provides power combining, isolation, voltage transformation, and energy transfer inductance. This thesis presents magnetic models for this transformer structure, for operation in both the full-power and low-power modes. Additionally, this work details the general benefits of stacking in high-voltage converters, and investigates the performance benefits of using this topology over a more traditional DAB architecture. Simulations of several topologies and implementations, using different voltage-rated devices as well as different semiconductor technologies (such as vertical Si MOSFETs, Si Superjunction MOSFETs, and GaN FETs), are presented, as are experimental results for multiple 175 kHz, 300 W, 380 V to 12 V prototype converters. The GaN-FET-based DSAB prototype achieves 95.9% efficiency at full load, a peak

efficiency of 97.0%, an efficiency above 92.7% down to 10% load and an efficiency above 79.8% down to 3.3% load.

1.1 Thesis Motivation

The dual-active-bridge (DAB) converter has many characteristics that make it attractive for high-voltage dc-dc converter applications, such as bidirectional power flow, high power density, soft-switching capability, isolation, and high efficiency [1] [2]. Additionally, the transformer leakage inductance can be used as the energy transfer inductance, while the switch parasitic output capacitance can be used as the capacitance required for the resonant transitions required for ZVS. This allows the DAB converter to be implemented with a small number of components, which helps decrease converter size and increase power density [1].

Resonant-transition or pseudo-resonant converters such as the DAB are also attractive for high power applications because of their lower device and component VA stress compared to resonant converters [1]. DAB converters have become a popular topology for dc distribution systems, electric vehicles, and grid interfaces.

This thesis presents a 380 V to 12 V dc-dc converter that could be used in such a dc distribution system for data centers, where a bus of 380 V (that can range from 260 V - 410 V) needs to be converted to 12 V to power individual servers, and proposes a new converter topology that is optimized for efficiency across the entire load range. This is especially desirable for data center applications, as the converter's load can quickly change based on the server computation demands.

1.2 Thesis Objectives and Contributions

The goal of this thesis is to design and build a high-efficiency dc-dc converter with the following specifications:

- Input Voltage: 260 V - 410 V
- Output Voltage: 12 V

- Output Power Rating: 300 W

The converter is able to achieve high efficiencies at low loads due to its stacked-inverter structure, which allows for the use of lower-voltage rated devices that can more easily achieve ZVS at low currents, in addition to its low-power operating mode that decreases core loss and switching loss, and greatly extends the ZVS range.

1.3 Organization

This thesis is organized into the following chapters:

- Chapter 2 gives an overview of the traditional DAB topology, and describes some of its typical limitations, such as the loss of ZVS at low powers or when the voltage transformation ratio deviates substantially from the transformer turns ratio. Existing methodology for improving the ZVS performance of the DAB is explored, and is briefly compared to the techniques proposed in this thesis.

- Chapter 3 develops the theory behind the operation of the DSAB converter, and provides an overview of the benefits of stacking devices in high-voltage converters. The double stacked-inverter, reconfigurable rectifier, and full-power and low-power mode operation are explored, and magnetic circuit models are presented for the magnetics in both operating modes.

- Chapter 4 details the selection of the semiconductor devices for use in the simulated and assembled prototypes, and gives an analysis of the benefits of low-voltage semiconductor devices. Devices for use in the DSAB, a traditional full-bridge DAB, and a DAB with a stacked full-bridge are compared. A figure-of-merit is also presented to aid in this comparison.

- Chapter 5 details the design of the DSAB's magnetic structure, and discusses the methods used to decrease winding loss and implement the internal leakage inductance. An overview of the benefits of planar magnetics is also presented,

followed by a description of the physical realization of the magnetic component using a printed circuit board structure.

- Chapter 6 presents simulation results using the devices chosen in Chapter 4 for the DSAB converter, as well as for some more traditional DAB topologies. The full-power and low-power modes of the DSAB are also simulated. Efficiency curves are presented showing the DSAB's high efficiency over the entire load range, which exceeds that of the DAB designs.

- Chapter 7 presents experimental data collected from the assembled prototypes, including the DSAB converter with both GaN and Si inverters, as well as a stacked full-bridge DAB converter using Si Superjunction devices. Operating waveforms for the full-power and low-power modes are also presented, as is a discussion of the ZVS performance of the DSAB.

- Chapter 8 summarizes the thesis contributions, and explores possible areas for future research in relation to the proposed topology.

Chapter 2

Large Conversion Ratio Step-Down dc-dc Converters

2.1 Typical Applications

There is a growing need for high-efficiency dc-dc converters providing large step-down voltage transformations, as dc loads and distribution systems become more common. Dc-dc converters allow easier integration of inherently dc systems, such as solar panels and microgrid interfaces, batteries, LED lighting, and battery chargers or interfaces for hybrid and electric vehicles (which often require bi-directional converters) [3] [4].

Dc distribution systems, such as for data centers, are one such application where a high voltage (e.g., 380 V) must be converted down to a much lower voltage (e.g., 12 V) to power server racks, while still maintaining high efficiency across a wide load range. Dc distribution is attractive as it requires fewer conversion stages (including UPS systems) which increases efficiency, better manages power factor, and makes it easier to connect to renewable energy sources such as PV panels or battery back-up systems [5]. The converter topology presented here is designed to meet the emerging voltage input and output specifications for data center dc distribution systems. It is especially attractive for such an application due to its high efficiency even at low powers, as servers may remain connected to the dc bus while not actively drawing large amounts of current, as in standby or low-demand conditions.

However, high-voltage, large conversion-ratio converters such as these applications require face several challenges, such as large device switching loss and magnetic core loss. Soft switching techniques (such as zero-voltage switching (ZVS) or zero-current switching (ZCS)), where the switch voltage or current are made to be zero at the switching transition to reduce overlap loss, $P_{overlap} = VI$), are often used in these types of converters to minimize switching losses. As switching loss is proportional to the converter switching frequency, reducing switching loss can allow the converters to operate at higher frequencies, resulting in smaller passive components and increasing the power density of the converter. This can be especially beneficial for converters designed for low-space or low-weight applications, such as electric vehicles. However, for many soft-switched converters, soft-switching is only achievable under certain operating conditions, and the converters will often lose soft-switching when operating too far away from the nominal voltage conditions or at light loads.

Some topologies, such as resonant dc-dc converters, use variable frequency to extend their soft-switching ranges to efficiently operate over a wider region; however, this means that magnetic components cannot be optimized for a given frequency and increases the difficulty of filter design.

Instead, a very popular topology for these types of applications is the dual-active-bridge (DAB) converter, which consists of two phase-shifted bridges connected across a transformer and energy transfer inductance, operating at a fixed switching frequency. It has become very popular since its introduction in [1] due to its simple topology and straightforward control scheme. Additionally, while not a resonant converter, it uses resonant switching transitions to achieve ZVS, and can achieve very high efficiency operation.

2.2 The Dual-Active-Bridge Topology

The DAB topology is often used where high efficiency or power density is required. It is also capable of buck-boost operation and bi-directional power flow, which is often desirable for electric vehicle or battery charging applications. Additionally, the DAB

offers isolation due to its transformer stage and is capable of soft-switching all the bridge devices (under certain operating conditions) [2].

The DAB has a very simple structure that consists of two bridges phase-shifted across a transformer with some amount of energy transfer inductance. This inductance can often be implemented with the transformer leakage inductance, reducing the number of reactive components needed and allowing the size of the converter to be decreased. In its most basic configuration, the DAB requires a single transformer and eight semiconductor switches [1], giving it a low number of components compared to other isolated bi-directional dc-dc converters [4]. Because the device output capacitance can be used as the snubber capacitance for soft-switching, no additional passive components are necessary to achieve ZVS.

The DAB can achieve very high efficiencies around its nominal operating point, where the devices can be soft-switched. Additionally, the control strategy for the standard DAB is very simple, as the output power is modulated by controlling the phase-shift between the two bridges, for a given frequency and transformer voltages. Additionally, the DAB can be designed to operate at a single frequency, which allows the magnetic core material and winding structure to be optimized for the operating frequency and corresponding skin depth, and also simplifies filter design. The converter's modular design also lends itself well to bi-directional or multi-port operation [6].

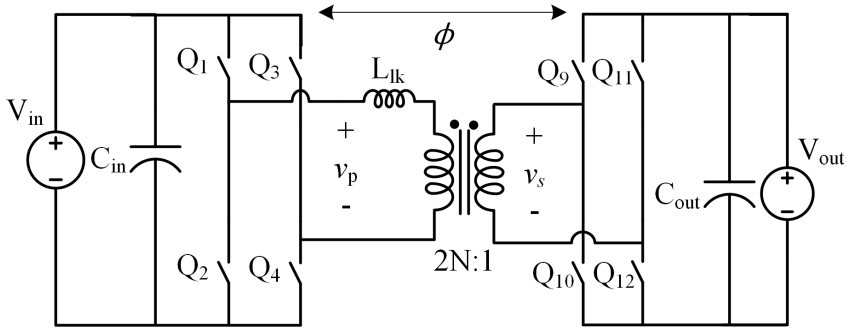


Figure 2-1: Circuit diagram for a DAB using a full-bridge input and output. The two bridges are phase-shifted from each other across a transformer and an inductance, L_{lk}.

Fig. 2-1 shows a circuit diagram for the conventional DAB converter which consists

of two full-bridges that are phase shifted from each other across a transformer with some leakage inductance, L_{lk}, by a phase shift ϕ. The transformer primary and secondary voltages are square-waves with 50% duty cycles. Under phase shift control, the output power can be given by [1]:

$$P_{out} = \frac{v_p v_s N}{2\pi f_s L_{lk}} \phi (1 - \frac{\phi}{\pi}) \tag{2.1}$$

where L_{lk} is the leakage inductance of the transformer v_p is the primary voltage, v_s is the secondary voltage, N is the transformer turns ratio, f_s is the switching frequency in Hz, and ϕ is the phase shift between the the two bridges in radians.

Here, positive ϕ represents power flow from V_{in} to V_{out}, so that the input voltage leads the output voltage. The direction of power flow can be reversed by making the input voltage lag the output voltage, so that ϕ is negative according to the conventions in Eqn. (2.1). The maximum power transfer is achieved at a ϕ of $\frac{\pi}{2}$ or 90° which places a limit on the achievable output power for a given set of voltages, inductance, and operating frequency.

2.2.1 Drawbacks of the Dual-Active-Bridge Topology

Although the DAB converter is capable of achieving high efficiency and ZVS around its nominal operating point, the converter can lose ZVS when the voltage ratio deviates substantially from the condition $V_{out} = NV_{in}$, or at light loads where the output current decreases [2]. There can also be high circulating currents at light loads, or when the converter is operating outside of its nominal voltage region. Many of the standard applications of the DAB, such as battery charging, energy storage, fuel cells, photovoltaics, or dc distribution systems, have inherently varying voltage or load conditions, making it hard to achieve high efficiency over all operating points when using the traditional DAB topology.

There has been a significant amount of work done to extend the soft-switching range of the DAB and increase efficiency at light-loads, including alternative control schemes, variable inductance or frequency techniques, and deadtime optimization. A

selection of these are summarized below, and compared to the methodology proposed here.

Alternate Control Schemes: Three-Level and PWM Patterns

Standard phase shift control can result in high conduction and switching losses when operating away from the nominal conditions [4]. Additionally, it is not possible to directly shape the current waveform, which is set by the leakage inductance, the phase shift, and the transformer voltages. Current waveform shaping, however, may be desirable to achieve ZVS at low loads, where the operating current may not be enough to generate the required voltage transitions on the switch output capacitance in the given deadtime.

The Triangular and Trapezoidal control methods presented in [4] and [7] involve generating three-level transformer voltages with arbitrary duty cycles, and are named for the voltage and current waveforms they produce. These methods are designed to reduce reactive power in the transformer and decrease switching loss. The control strategies also introduce switching states where the inductor current is zero in order to create ZCS transitions. However, triangular control is only applicable when the primary and secondary voltages satisfy the constraint $v_p \ll v_s N$, while trapezoidal control is applicable for the condition $v_p \approx v_s N$ and provides near-ZCS transitions.

These modes are combined in [4] to produce a control scheme that can be used over the full operating range. However, this involves sensing the power level and input and output voltages, which adds control complexity. Additionally, although the soft-switching range is extended, it is done through the use of ZCS transitions, which get rid of overlap losses but do not necessarily decrease the losses associated with the charging and dischaging of the switch output capacitances.

Another control technique is the use of PWM control on the DAB full-bridges. These modulation sequences are designed to minimize conduction losses and circulating transformer currents and extend the soft-switching range. They often require sensing circuitry for various circuit parameters, and can involve continuously calculating optimal variables, such as the duty-cycle or phase shift angle [6]-[8]. This can

greatly increase the control complexity of the DAB, which diminishes one of the main attractions of the DAB architecture.

Additionally, these control schemes are designed for full-bridge topologies, which may prevent the use of stacked-bridge architectures designed to reduce switch stress and allow for the use of lower-voltage rated devices with more desirable parasitic resistance and capacitance characteristics.

Dead-time Control

As described in [9]-[10], the actual value of the switch deadtimes can have a large impact on efficiency, especially at low loads or where the voltage transfer ratio is far from the transformer turns ratio. This is because the deadtime can effectively act as an additional part of the phase shift, and at low powers, can dramatically affect the actual output power delivered.

Additionally, if the deadtime is too long (namely, longer than a quarter cycle of the period set by the resonating leakage inductance and switch capacitance), the sinusoidal voltage waveform across the switch capacitance will start to ring down. This can lead to increased switching losses due to partial hard-switching at the end of the transition, as the voltage is no longer reaches the full blocking voltage of the switch. Additionally, too large of a deadtime can lead to losses due to body diode conduction.

Therefore, several methods have been introduced to adaptively control the dead-time to minimize switching losses. [9], for example, senses the switch drain-to-source voltage, V_{ds}, to detect if it has started to ring down, signifying too long of a deadtime. In that case, the deadtime for the next switching cycle is decreased, and the V_{ds} value is checked again.

However, these methods require additional control complexity, such as feedback control loops and additional sensing of circuit parameters.

Variable Inductance and Frequency Control

The value of the leakage inductance in the DAB heavily influences the ZVS capability of the converter, as achieving ZVS requires that the stored energy in the leakage inductance at the switching transition must be equal or higher to the stored energy in the output parasitic capacitances of the devices being switched [11].

In order to achieve ZVS across a wider operation range, the leakage inductance should be high so that it can store more energy and have high enough current to charge and discharge the switch capacitances. On the other hand, higher RMS currents in the leakage inductor result in higher conduction losses, and therefore lower efficiency at full load where ZVS is already achievable. Therefore, there is a trade-off between optimizing for high efficiency at full-load versus high efficiency over a wide power range. To maximize full-load efficiency, the phase shift should be as low as possible; however, this would result in the phase shifts at low load being further reduced, which would restrict the ZVS range even more.

Therefore, work has been done to try to vary the leakage inductance and current as a function of the load to allow the DAB converter to be optimized for both high-efficiency at full load and high efficiency over a wide operation range. As described in [11], using different leakage inductance values for different power levels can help increase the converter's efficiency over the entire operating range. One method is to physically reconfigure the leakage inductance in the converter [11] [12], but these can require additional control and physical components. Another option is to vary the switching frequency depending on the power levels to appropriately scale the leakage inductance current. Lower frequencies can be used at higher powers, which reduces the phase shift required to obtain the desired power, thereby reducing RMS currents and conduction losses [11].

However, as with variable frequency resonant converters, this makes it harder to optimize the transformer design, especially with respect to core and skin effect losses. As described in [13], the upper end of the frequency range is limited by the core and skin effect losses for the magnetics, and by the switching losses for the semiconductors.

The lower end of the frequency range is limited by the core saturation characteristics.

Burst

Another method to increase the current at the switch transition for light-load conditions is the burst control scheme. In burst mode, the converter is turned on and off at a burst frequency much lower than the switching frequency of the converter. In its most basic form, the converter is kept on for a duty cycle proportional to the percentage of the full-load power required, so that 10% load would require the converter to be on for 10% of the burst period. Burst mode for the DAB converter is explored in [11] and [14].

By running the converter in this manner, the converter is made to operate in its full-load condition during the on-time, so that the leakage inductor current is high enough to provide the necessary switch voltage transitions to achieve ZVS. This increases the efficiency of the converter at low loads.

One drawback of burst mode control is that there can be significant transient events when the converter turns on and off. These startup and shutdown waveforms can deviate from the ideal operating waveforms, and at very low powers where the converter is only on for a small percentage of the burst period, these transients can represent a significant portion of the converter on time, resulting in decreased efficiency.

2.3 The Double Stacked-Active Bridge Converter

The proposed DSAB topology attempts to address several of the drawbacks of the methods explored above. Like the variable frequency and leakage inductance method, this converter aims to optimize efficiency both at full-load as well as under light-load conditions. This is achieved through the use of a stacked inverter topology and operating modes for both high-power and low-power conditions. The converter operates at the same fixed frequency for both modes, allowing for optimization of the magnetic components and simplifying filter design.

The efficiency at full-load is increased by using a double stacked-bridge topology that reduces the voltage stress on each inverter device, allowing for the use of lower-voltage rated devices that have more favorable switching characteristics, such as lower parasitic resistance and capacitance. A fixed deadtime is used for the entire operation range, simplifying control (though adaptive deadtime techniques could be applied to this technology if desired).

High efficiency is achieved over a wide operation range due to 1) the lower device parasitic capacitances achievable with a stacked inverter design, which allows for ZVS at lower currents, and 2) the low-power operating mode which reduces core loss and switching loss in light-load operation.

The DSAB converter consists of two stacked full-bridges that each feed into one of the transformer's two primary windings. Both primary windings are coupled to a single secondary winding which feeds into a reconfigurable rectifier. When the converter is operating in the full-power mode, the two primaries are energized with in-phase square-waves and the rectifier is configured as a full-bridge rectifier. When the converter is operating in the low-power mode, the primaries are alternately energized or held at zero voltage, by switching one inverter as a stacked full-bridge and shorting the other. The rectifier is also configured as a half-bridge rectifier. The end result of this is to halve both the total primary and secondary voltages, resulting in decreased core loss and a converter that now nominally operates at a quarter of the full-load power for the same phase shift ϕ.

This has a similar effect as varying the leakage inductance or switching frequency, as this operating scheme allows large enough values of ϕ at low loads to allow for ZVS, without similarly scaling up the values of ϕ at full-load and subsequently increasing RMS currents and conduction losses. The leakage inductor current is increased in this low-power mode, allowing the converter to achieve ZVS down to a much lower power level. The control complexity is not dramatically increased, as the rectifier is reconfigured with a single auxiliary switch, which transitions a single time for a mode-switch, while the inverter gate signals are simply switched between two pre-programmed patterns depending on the operating mode.

Because the stacked inverters are alternately switched, the low-power mode also effective reduces the number of switching events per cycle, reducing switching loss. Additionally, all soft-switched transitions are ZVS, so the power loss from the charging and discharging of the switch output capacitance is removed or significantly reduced.

The converter only needs to undergo a mode-switch when the load changes significantly, as the efficiency of the converter is relatively flat for a range of powers around the intersection points of the two modes. This means there are not the repeated transient events characteristic of burst-mode control. While this topology does require additional switches due to the double stacked-bridge inverter architecture, this 1) reduces the device stress on each inverter switch and helps decrease switching loss and extend the ZVS range, and 2) allows for alternate switching patterns to implement the low-power mode.

The benefits of the DSAB converter are summarized below:

- Fixed frequency allowing for optimization of magnetics and filters
- Capable of achieving high efficiency with a fixed deadtime over the entire load range
- Stacked inverter bridge topology that allows the use of lower-voltage rated devices with more favorable parasitic resistance and capacitance characteristics, decreasing switching and conduction losses and extending the ZVS range
- Low-power mode that reduces core loss, switching loss, and extends the ZVS range
- No repeated transients; the converter only mode-switches if the load conditions change significantly, and does so with only a single auxiliary switch

The DSAB converter is therefore able to achieve high-efficiency at full-load while also maintaining excellent performance across a wide load range. The results presented here do not use any sort of feedback control as this was a prototype design, but a more advanced version could use a simple hysteretic control scheme to switch between modes based on the measured output power.

Chapter 3

Double-Stacked Active Bridge Topology and Theory

The Double-Stacked Active Bridge (DSAB) topology uses the active bridge technique, but is designed in a way so as to overcome some of the limitations of the conventional dual-active-bridge (DAB) design. One such limitation is the DAB's tendency to lose zero-voltage switching (ZVS) in light-load conditions when the current is not high enough at the switching transitions to provide the required voltage transitions on the device output capacitance. This work extends the ZVS range of the converter by both decreasing the device output capacitance, as well as enabling a low-power mode that both extends the ZVS switching range in power and reduces core loss. The architecture is made up of a double stacked-bridge inverter coupled to a reconfigurable rectifier via a special three-winding leakage transformer. The transformer provides power combining and energy storage, as well as isolation and voltage transformation. The details of the design of the inverter, rectifier, and magnetics stages are provided below.

3.1 Inverter Stage

As discussed in Chapter 2, the conventional DAB converter uses a full-bridge for both the input and output bridges (see Fig. 3-1). This converter, however, uses a dou-

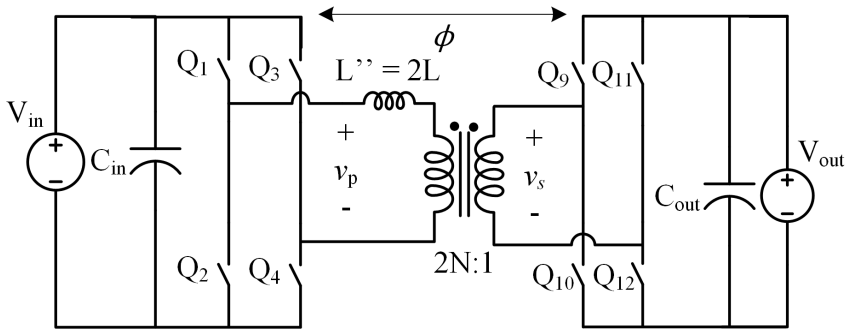


Figure 3-1: Circuit diagram for a DAB using a full-bridge input and output. The two bridges are phase-shifted from each other across a transformer and an inductance, $2L$. (Note that leakage inductance here is shown as $2L$ so that the total primary-referred leakage is the same as that shown in the DSAB converter in Fig. 3-3). The turns ratio is $2N$:1 because the voltage on the primary waveform is double that of the DSAB converter.

ble stacked-bridge inverter topology for high-efficiency, high-voltage conversion. By stacking two stacked-full-bridge inverters (hence, a double stacked-bridge inverter), the converter takes advantage of multiple benefits:

- Stacking decreases the individual inverter device voltage ratings, which provides favorable tradeoffs in overall device performance, and decreases energy stored in the device parasitic capacitance (specifically the output capacitance, C_{oss}), which makes it easier to achieve ZVS for lower inductor currents.

- Having two inverters (e.g. as in a double stack) enables additional switching patterns between individual stacked bridges, allowing for a low-power mode that reduces core loss and device switching loss to further extend the ZVS range.

3.1.1 Device Rating

The devices $Q_1 - Q_4$ in Fig. 3-1 must be rated for the full input voltage, V_{in}. For high input voltage applications, this switch stress is very high, and the conventional DAB suffers from losses due to poor switch characteristics. By comparison, $Q_1 - Q_4$ for the single stacked-bridge topology shown in Fig. 3-2 are only rated for $\frac{V_{in}}{2}$, while $Q_1 - Q_8$ for the proposed double-stacked topology in Fig. 3-3 are only rated for $\frac{V_{in}}{4}$.

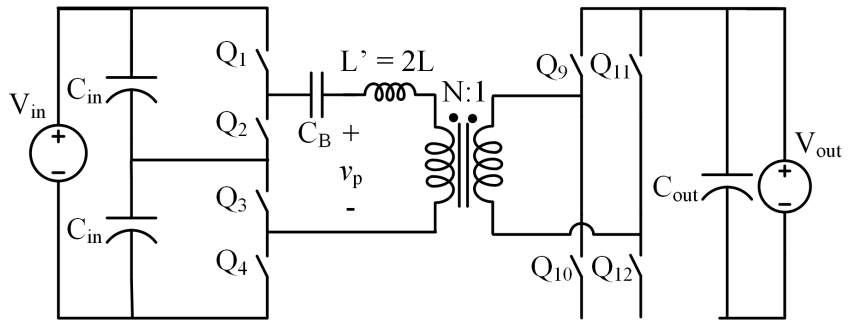


Figure 3-2: Circuit diagram for a DAB using a stacked full-bridge on the input and a full bridge on the output. A blocking cap, C_B, is used to remove the DC component in the square-wave output of the stacked bridge. (Note that leakage inductance here is shown as $2L$ so that the total primary-referred leakage is the same as that shown in the DSAB converter in Fig. 3-3)

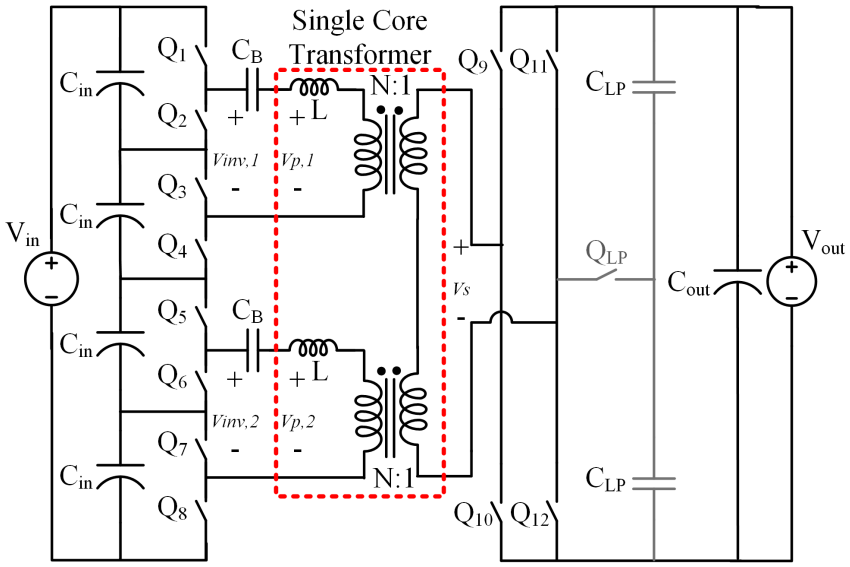


Figure 3-3: Circuit diagram for the proposed system. The dashed red box contains an equivalent circuit model for the single magnetic component. Each of the stacked bridges feeds the primary winding of a single-core, three-winding transformer. An auxiliary switch, Q_{LP}, in the rectifier allows for a mode switch into a low power mode. A blocking cap, C_B, is used to remove the DC component in the square-wave output of each stacked bridge. Each primary winding is assigned half of the total primary-referred leakage inductance, $2L$.

These lower-voltage rated devices can have much better switching performance with lower parasitic resistance, capacitance or both. This is often represented through a figure-of-merit (in this case $R_{ds,on}C_{oss}$), due to the fact that the figure-of-merit offers a convenient way to compare switches of similar voltage ratings despite different die sizes or technologies. The figure-of-merit chosen here was $R_{ds,on}C_{oss}$, as this product represents the two main loss mechanisms in the switches for this topology:

- Higher $R_{ds,on}$ means more conduction loss when the switch is conducting current, as shown in the equation for conduction loss in a switch ($P_{COND} = I_{RMS}^2 R_{ds,on}$).

- Higher C_{oss} means that more energy will be stored in the parasitic output capacitance of the device. For hard-switched applications, this will require more power to be dissipated to charge and discharge C_{oss} during switch transitions. For soft-switched applications (such as the proposed topology), since C_{oss} is charged / discharged by the resonant tank (or some inductance resonating with the output capacitance), this will not contribute to power loss in the switch; however, a higher C_{oss} will require a greater amount of current to complete the necessary voltage transitions on the output capacitance in the given amount of deadtime. This can mean that switches with too high of C_{oss} can lose ZVS sooner than switches with lower C_{oss}, as the current decreases in light-load conditions.

More detail about switch characteristics and figure-of-merit will be given in Chapter 4, but a rule-of-thumb for the relationship between figure-of-merit and breakdown voltage, BV_{DSS} (in effect, the rated voltage) for common device technologies is given below:

$$R_{ds,on}C_{oss} \propto BV_{DSS}^k, \quad where \quad k > 2 \tag{3.1}$$

Because this relationship grows faster than a linear relationship, adding more devices (though adding more parasitic resistance and capacitance) can still have lower loss associated with the switches because of the much better switching performance

of lower-voltage rated devices. This effect becomes more beneficial at higher voltages, where a doubling of the rated voltage can drastically impact the switch characteristics. Because of this, stacked topologies are especially attractive at higher input voltages, such as in this 380 V input application. By stacking, one can use lower-voltage devices to decrease conduction losses and maintain ZVS over a wider range.

Comparisons between the proposed topology and a single-stacked DAB converter will be presented in Chapters 4, 6, and 7. Chapter 4 will compare the devices possible for each design, highlighting the figures-of-merit for different voltage-rated devices; Chapter 6 will present simulated efficiency data for the Double-Stacked Active Bridge (the proposed topology), the single-stacked DAB, and the full-bridge DAB; and Chapter 7 will present experimental data from the proposed topology and a single stacked-inverter DAB. A prototype of the full-bridge DAB topology of Fig. 3-1 was not built, but would be expected to have significantly worse performance than the single stacked-inverter DAB topology.

3.1.2 Additional Switching Patterns

An additional benefit of the double-stacked architecture is the ability to operate in a low-power mode, which will be more fully detailed in Section 3.4. The low-power mode takes advantage of the two-primary magnetic structure by energizing the primaries at different times, which could not be achieved with a single full-bridge inverter with one primary winding.

3.1.3 Balancing

A common concern with stacked topologies is how to maintain balanced operation between all of the stacked devices. To address this, a switched-capacitor balancer network is used to internally balance each stacked full-bridge inverter; active balancing is not used between the two inverters in the double-stacked topology. Experimental waveforms presented in Chapter 7 show that the two inverter voltages remain balanced, which we attribute in part to the compact, single-component magnetic

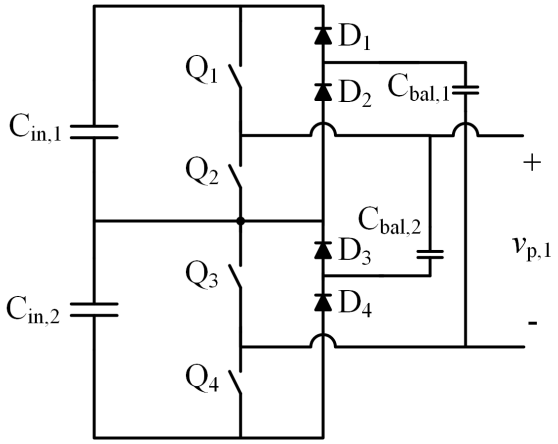


Figure 3-4: Circuit diagram of the balancer used to balance the input capacitors in one stacked full-bridge inverter. $C_{in,1}$ and $C_{in,2}$ are balanced with respect to each other using the balancing capacitors $C_{bal,1}$ and $C_{bal,2}$. Only the top inverter, connected to the primary winding, $v_{p,1}$, is shown here; the same circuit is used on the bottom inverter.

structure and the repeatability and symmetry of the planar windings design.

A circuit diagram for the balancer is shown in Fig. 3-4, while Fig. 3-5 shows the behavior of the balancer depending on whether $v_x > v_y$ or $v_x < v_y$. Fig. 3-5 (a) shows the balancer circuit operation for the case where $C_{in,2}$ has more charge than $C_{in,1}$, and therefore $v_y > v_x$. The balancer capacitors are nominally at $\frac{V_{in}}{4}$, which is the desired voltage across $C_{in,1}$ and $C_{in,2}$. In (a), when Q_4 is on, if $C_{in,2}$ has more charge than $C_{bal,1}$, then D_2 will be forward biased and current will flow from $C_{in,2}$ to $C_{bal,1}$. This current path is shown in red. When Q_3 is then closed, the excess charge now on $C_{bal,1}$ will be shunted over to $C_{in,1}$. This current path is shown in blue. In this manner, the circuit segment on the right will balance out $C_{in,1}$ and $C_{in,2}$ in the case that $C_{in,2}$ has more charge.

Fig. 3-5 (b) shows the balancer circuit operation for the case where $C_{in,1}$ has more charge than $C_{in,2}$, and therefore $v_x > v_y$. If Q_1 is on (which occurs at the same time as Q_4 being on), if $C_{in,1}$ has more charge than $C_{bal,2}$, current will flow from $C_{in,1}$ to $C_{bal,2}$. This current path is shown in red. When Q_2 is on (which occurs at the same time as Q_3 being on), the excess charge shunted from $C_{in,1}$ to $C_{bal,2}$ will then be moved over to $C_{in,2}$. This current path is shown in blue. The balancer capacitors and diodes required for the system are quite small and process very little power, and

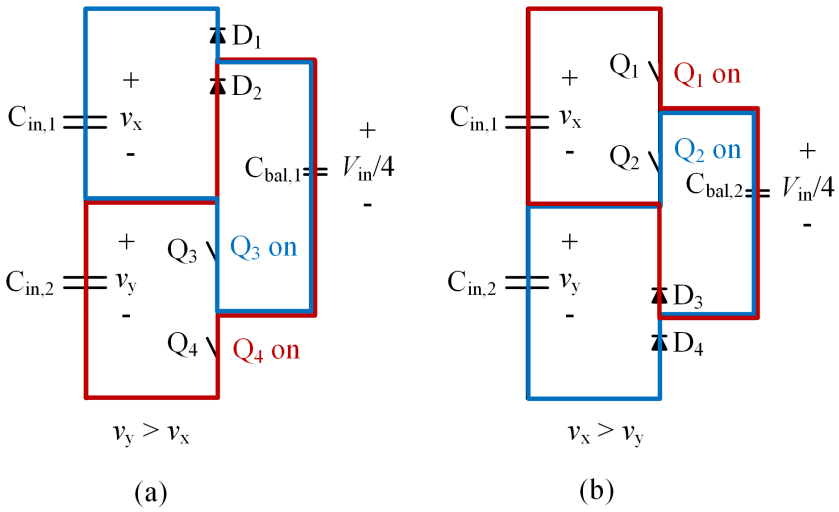


Figure 3-5: Balancer circuit operation for (a) the case where $v_y > v_x$, and (b) the case where $v_x > v_y$. The red loops represent the current paths when Q_1 and Q_4 are on, and are the states where charge is being shunted from the over-charged input capacitors to the corresponding balancer capacitor. The blue loops represent the current paths when Q_2 and Q_3 are on, and are the states where the excess charge now on the balancer capacitors is shunted to the under-charged input capacitors.

so do not heavily influence system size and efficiency.

3.2 Rectifier Stage

The rectifier in Fig. 3-3 can be reconfigured using an auxiliary low-power switch, Q_{LP}, to allow for different operating modes. In one operating mode (designated as the full-power mode), Q_{LP} is held off, and the rectifier acts as a full-bridge rectifier. In the second operating mode (designated as the low-power mode), Q_{LP} is held on, and the rectifier acts as a half-bridge (or voltage-doubler) rectifier. More details on converter operation in the different modes is given in Section 3.4.

Since Q_{LP} must block voltage in both directions in the full-power mode (when held off), a single FET device cannot be used because the body diode will allow some amount of current conduction even if the gate of the transistor is held at zero. Therefore, Q_{LP} is implemented with two back-to-back FETs that are source-connected. A single gate driver is used to turn the devices on and off.

Fig. 3-6 shows how the low-power auxiliary switch is implemented using FET

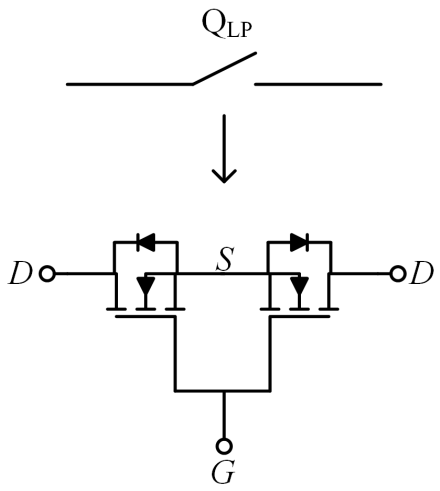


Figure 3-6: Implementation of the low-power auxiliary switch, Q_{LP}, using two source-connected FET devices with their gates tied together. The two internal body diodes block bidirectional current in the off state. A single gate driver is used to turn the devices on and off, and is referenced to the source.

devices that are source-connected with their gates tied together. In this configurations, the internal body diode of the FETs will block current from flowing when in the off state. More detailed schematics of the low-power switch will be presented in Appendix C.

3.3 Transformer and Leakage Inductance

The transformer is a three-winding, three-core-leg structure composed of two primary windings, both of which are coupled to the same secondary winding. This can be physically constructed in a single magnetic structure by winding each primary around the outer leg of an E-I core, and winding the secondary around the middle leg. The leakage inductances, L (see Figs. 3-1 - 3-3), are also realized by this physical structure, yielding an equivalent circuit model as shown in the dashed red box in Fig. 3-3. In this model, each primary winding is assigned an identical leakage inductance; in general, a more complicated model of a multi-winding transformer is needed (e.g., see the cantilever model in [15]), but the symmetric structure and drive of the transformer make this model adequate. For SPICE modeling, the structure is modeled as

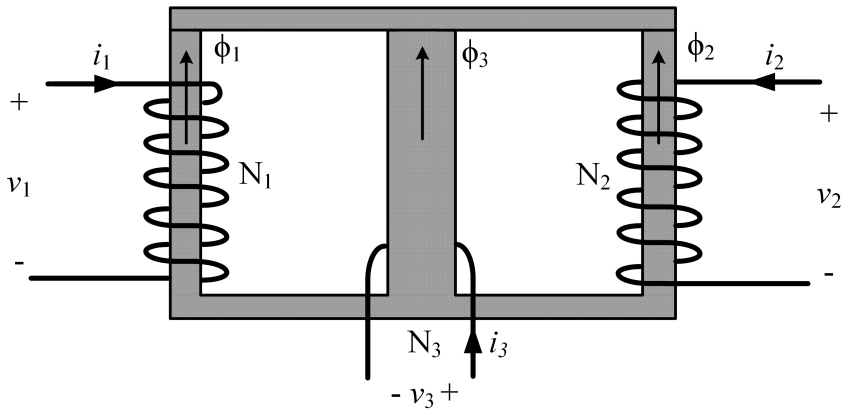


Figure 3-7: A winding diagram of the three-winding transformer. The primary windings are wound around the outer legs (windings 1 and 2), while the secondary is wound around the middle leg (winding 3) of an E-I core.

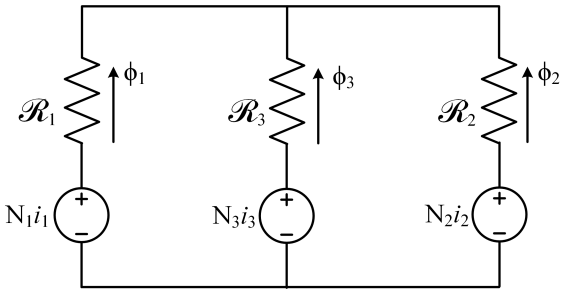


Figure 3-8: Magnetic circuit model for the three-winding transformer. Let $v_1 = v_2 = v_p, v_3 = -v_s, N_1 = N_2 = N$, and $N_3 = 1$.

two transformers with a single primary and secondary, with the secondary windings connected in series (as shown in Fig. 3-3). Chapter 6 will give more detail about the SPICE model methodology.

The physical winding structure of the transformer is shown in Fig 3-7. The primary windings (windings 1 and 2) are wound on the outer legs of an E-I core, while the secondary (winding 3) is wound around the middle leg. The transformer windings are shown to have a turns ratio of $N_1 : N_2 : N_3$ where $N_1 = N_2$. The winding direction is such that the flux directions are all upwards.

A simplified magnetic circuit model is shown in Fig. 3-8 (neglecting reluctance paths outside of the core). $N_1 i_i - N_3 i_3$ represent the magnetomotive forces of each winding. $\mathscr{R}_1$-$\mathscr{R}_3$ represent the reluctances of the core for the corresponding legs. Making the assumption that for a high μ material ($\mu \to \infty$), $\mathscr{R}_1 \approx \mathscr{R}_2 \approx \mathscr{R}_3 \approx 0$,

one can use the magnetic equivalent of KVL and KCL to show the following

$$KVL: \quad N_1 i_i \approx N_2 i_2 \approx N_3 i_3. \tag{3.2}$$

where N_i is the number of turns on winding i and i_i is the current through winding i. Similarly,

$$\begin{aligned} KCL: &\quad \Phi_1 + \Phi_2 + \Phi_3 = 0 \\ Take \quad derivative: &\quad \frac{d}{dt}\Phi_1 + \frac{d}{dt}\Phi_2 + \frac{d}{dt}\Phi_3 = 0 \end{aligned} \tag{3.3}$$

where Φ_i is the flux through winding i, and the second line is obtained by taking the time derivative of the first.

Using the equation $\frac{v}{N} = \frac{d}{dt}\Phi$, where v is the winding voltage, we can substitute this into Eqn. (3.3) in order to get a relationship between the primary and secondary winding voltages, as shown below

$$\begin{aligned} \frac{v_1}{N_1} + \frac{v_2}{N_2} + \frac{v_3}{N_3} = 0 \\ \frac{v_p}{N} + \frac{v_p}{N} + \frac{-v_s}{1} = 0 \end{aligned} \tag{3.4}$$

where the second equation was found by letting $v_1 = v_2 = v_p, v_3 = -v_s, N_1 = N_2 = N$, and $N_3 = 1$. This can be rearranged to get the following relationship between the voltages of the two primaries and secondary

$$\frac{2v_p}{N} = v_s \rightarrow \frac{2v_p}{v_s} = N \tag{3.5}$$

where v_p is the voltage on each primary. A more sophisticated model (including flux paths outside of the core) would be necessary to fully capture the leakage inductances present in this system.

3.4 Operating Modes

3.4.1 Full-Power Mode

From Eqn. (3.5), it is evident that the effective primary voltage is the sum of the voltages applied to each primary winding. The effective secondary voltage is that applied by the rectifier. Eqn. (3.5), which is in terms of the primary and secondary voltages, can be expressed in terms of the converter input and output voltages for normal operation (full-power mode), as follows: for a system input voltage, V_{in}, each stacked full-bridge inverter output ($V_{inv,1}$ and $V_{inv,2}$, before the blocking capacitor, C_B) will swing from 0 to $\frac{V_{in}}{2}$, assuming the two stacked-bridges have evenly balanced input voltages. After the dc offset is blocked by the blocking capacitor, the voltage on each primary ($V_{p,1}$ and $V_{p,2}$) will swing between $-\frac{V_{in}}{4}$ and $+\frac{V_{in}}{4}$. Therefore, the relationship between the peak value of each primary voltage and the system input voltage is $V_p = \frac{V_{in}}{4}$. For a full-bridge rectifier, the ac voltage at the rectifier input will swing between $-V_{out}$ and $+V_{out}$, so that the rectifier input is a square wave of amplitude $v_s = V_{out}$. Under full-power mode operation at the nominal operating point, with each of the stacked bridge inverters operating in square-wave mode and the rectifier operating as a full-bridge rectifier, the output power characteristic is then given as

$$P_{out,FP} = \frac{(\frac{V_{in}}{4} + \frac{V_{in}}{4})V_{out}N}{2\pi f_s 2L}\phi(1 - \frac{\phi}{\pi}) \tag{3.6}$$

Here, $2L$ is the total primary-referred leakage inductance of the transformer (e.g., as illustrated in the model of Fig. 3-3), V_{in} is the dc input voltage, f_s is the switching frequency in Hz and ϕ is the phase shift between the inverter and rectifier in radians.

Fig. 3-9 shows waveforms for the inverter's operation while in the full-power mode. $V_{gate,1} - V_{gate,8}$ show the gate drive signals for switches $Q_1 - Q_8$. $V_{p,1}$ and $V_{p,2}$ are the top primary voltage and bottom primary voltage, as shown in Fig. 3-3. As can be seen in the figure, $V_{p,1}$ and $V_{p,2}$ are energized with in-phase square waves of the same amplitude; these individual primary voltages are summed to produce a total effective primary voltage that swings between $+\frac{V_{in}}{2}$ and $-\frac{V_{in}}{2}$. The deadtime

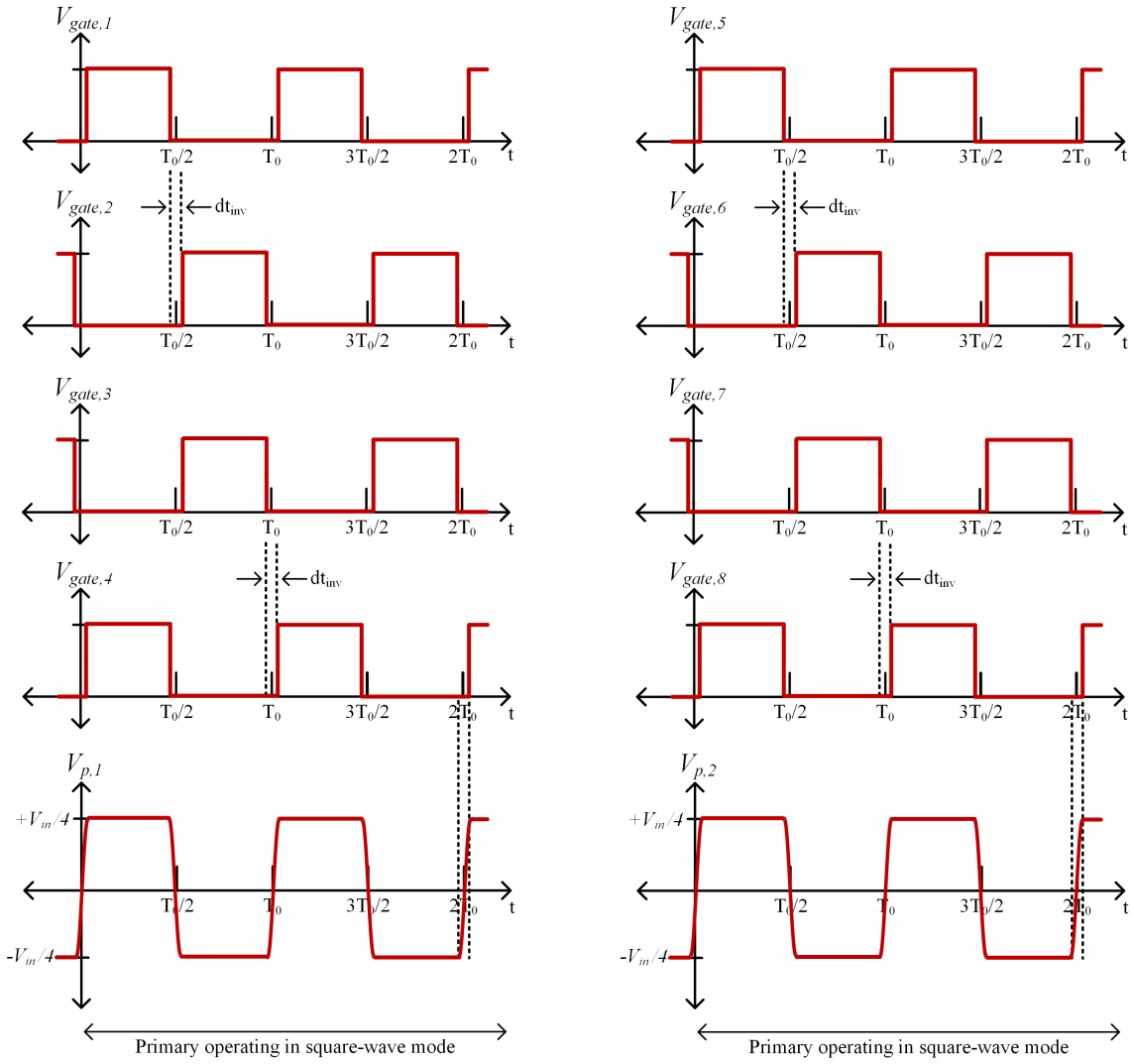


Figure 3-9: Switching diagram for the inverter and primary windings shown in Fig. 3-3. $V_{gate,1} - V_{gate,8}$ are the gate signals driving the inverter switches $Q_1 - Q_8$, which are switched as a stacked full-bridge. $V_{p,1}$ and $V_{p,2}$ are the resulting top and bottom primary voltages. The timing diagram is shown for two switching cycles ($2T_0$). Note that the two primaries have the same waveform, which sums to an effective primary voltage that is twice the amplitude of each individual primary voltage. Deadtime between the on-times for the top and bottom switches in each half-bridge are shown by dashed lines, labeled dt_{inv} for the inverter.

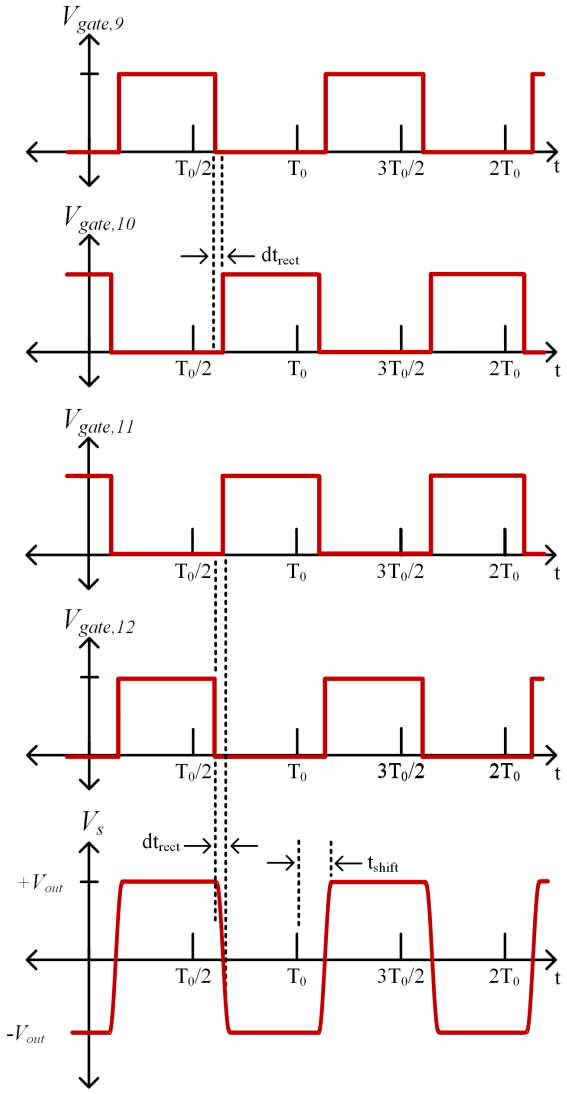


Figure 3-10: Switching diagram for the rectifier and secondary winding shown in Fig. 3-3. $V_{gate,9} - V_{gate,12}$ are the gate signals driving the rectifier switches $Q_9 - Q_{12}$, which are switched as a full-bridge. V_s is the secondary voltage. t_{shift} is the amount the rectifier is phase-shifted from the inverter in seconds.

between the top and bottom switches' on-times is illustrated by dashed lines, and the duration is labeled dt_{inv} for the inverter. The deadtime prevents shoot-through and allows time for ZVS transitions (i.e. for the voltage across the device capacitance to either fully transition). Under ZVS conditions, the device output capacitances will resonate with the leakage inductance, producing sinusoidal transitions between $+\frac{V_{in}}{4}$ and $-\frac{V_{in}}{4}$ on each primary.

Fig. 3-10 shows waveforms for the rectifier's operation while in the full-power mode. $V_{gate,9} - V_{gate,12}$ show the gate drive signals for switches $Q_9 - Q_{12}$. The rectifier is configured as a full-bridge, so that Q_9 and Q_{12} are driven with the same gate signals, and Q_{10} and Q_{11} are driven with complementary signals. Q_{LP} is held open (off) while in full-power mode, as well. The resulting secondary waveform swings between $+V_{out}$ and $-V_{out}$. The rectifier waveforms are shifted from the inverter waveforms by a time t_{shift}, which can be expressed as an electrical angle ϕ by the following: $\phi = 2\pi\frac{t_{shift}}{T_0}$, where T_0 is the switching period. Again, the deadtimes between top and bottom switches in a half-bridge are illustrated by dashed lines, labeled dt_{rect} for the rectifier. Deadtime duration and phase shift duration are not drawn to scale with each other.

3.4.2 Low-Power Mode

The converter can also be configured in a low power mode that naturally delivers a quarter of the power of the fully rated converter for a given phase shift, while reducing transformer core loss, providing increased current at the switching transition to extend the power range for which ZVS is achieved, and reducing switch gating loss. Power reduction is achieved by effectively halving the net voltages at the transformer primary and secondary. To do this, the inverter is configured to only energize one primary at a time while holding zero voltage on the other primary (such that their sum inducing on the secondary is halved). To maintain charge balance on the input capacitors, C_{in}, as well as to fully utilize the transformer core, the two primaries alternate between being energized or held at zero voltage every other switching period (though this could be done on a longer time basis). To maintain a proper voltage transformation ratio, the rectifier is reconfigured to operate as a half bridge (or voltage-doubler) rectifier.

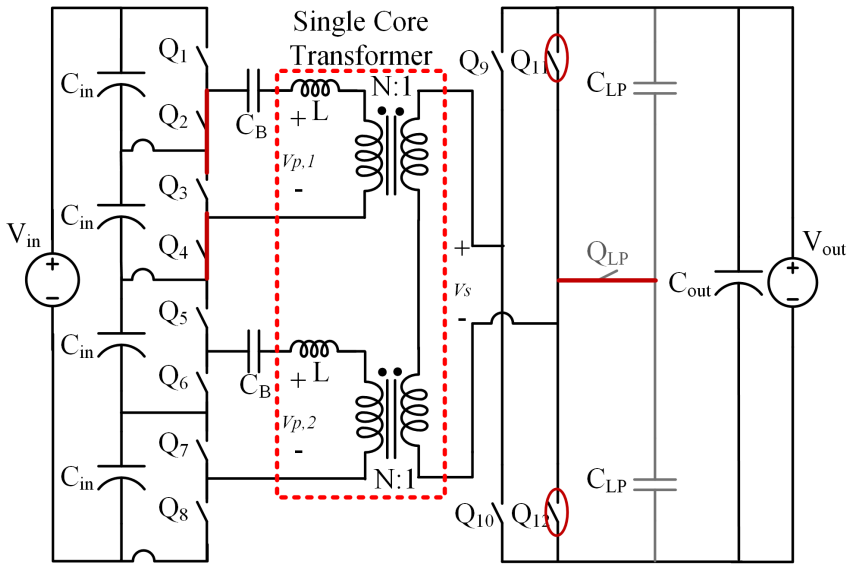


Figure 3-11: The proposed converter configured for low-power mode operation. Here, the converter is shown with the top primary held at zero voltage. Q_2 and Q_4 are held on as $Q_5 - Q_8$ are switched as in a normal stacked full-bridge inverter. In alternate half cycles, Q_6 and Q_8 would be held on, and the top stacked bridge would be operated as usual. The rectifier is configured as a half-bridge rectifier in the low-power mode, by closing Q_{LP} and leaving Q_{11} and Q_{12} open.

The converter configured in low-power mode is shown in Fig. 3-11. Here, the converter is shown with the top primary held at zero voltage, by leaving Q_2 and Q_4 closed while $Q_5 - Q_8$ are switched in normal stacked full-bridge fashion. To hold zero voltage on the bottom primary, Q_6 and Q_8 are held closed while $Q_1 - Q_4$ are switched. Since one primary is always held at zero voltage, the total primary voltage is half that of the full-power mode.

Fig. 3-12 shows waveforms for the inverter's operation while in the low-power mode. $V_{gate,1} - V_{gate,8}$ show the gate drive signals for switches $Q_1 - Q_8$. $V_{p,1}$ and $V_{p,2}$ are the top primary voltage and bottom primary voltage, respectively. As can be seen in the figure, while $V_{p,1}$ is held at zero voltage, $V_{p,2}$ is being energized with a square-wave voltage; after one switching cycle (T_0), the primaries switch behavior. The deadtime between each half-bridges' top and bottom switches is shown by dashed lines and labeled dt_{inv}.

Fig. 3-13 shows waveforms for the rectifier's operation while in the low-power mode. $V_{gate,9} - V_{gate,12}$ show the gate drive signals for switches $Q_9 - Q_{12}$. In order

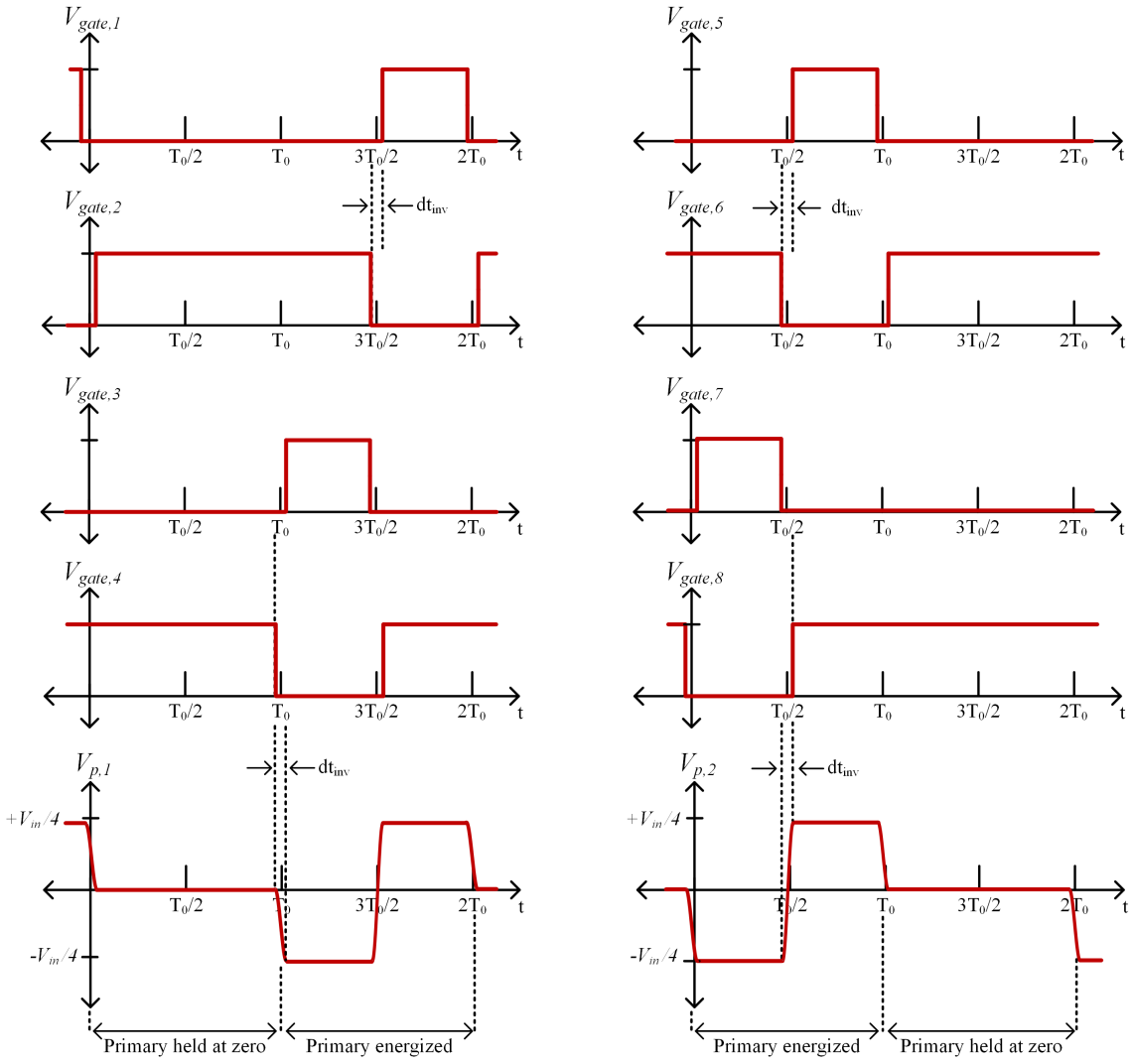


Figure 3-12: Switching diagram for the inverter and primary windings shown in Fig. 3-11. $V_{gate,1} - V_{gate,8}$ are the gate signals driving the inverter switches $Q_1 - Q_8$. $V_{p,1}$ and $V_{p,2}$ are the top and bottom primary voltages. The timing diagram is shown for two switching cycles ($2T_0$), during which each primary winding alternates between operating in a square wave mode and holding zero voltage. T_0 represents one period for the given switching frequency. Deadtime between the on-times for the top and bottom switches in each half-bridge are shown by dashed lines, labeled dt_{inv} for the inverter.

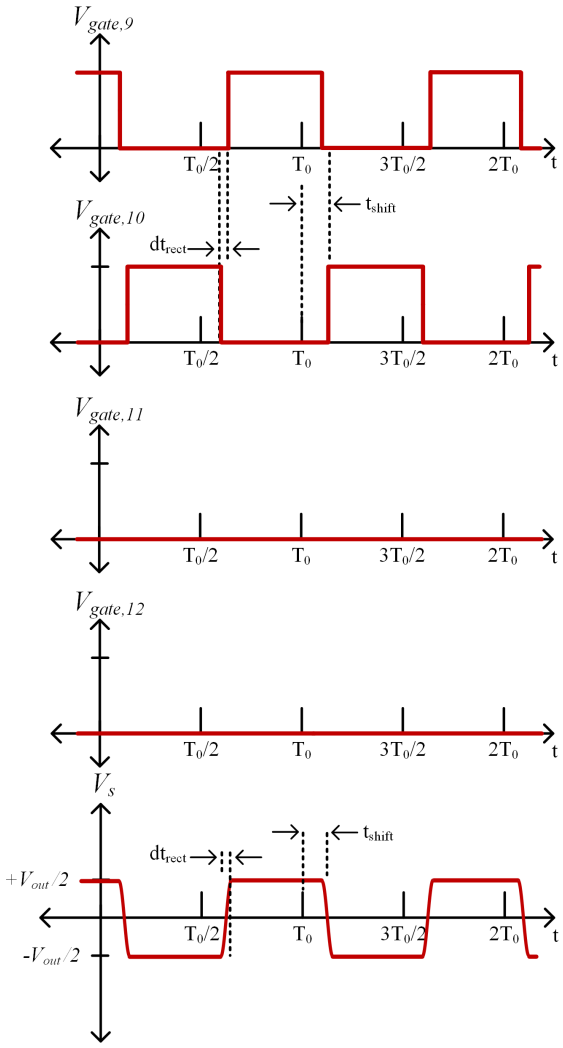


Figure 3-13: Switching diagram for the rectifier and secondary winding shown in Fig. 3-11. $V_{gate,9} - V_{gate,12}$ are the gate signals driving the rectifier switches $Q_9 - Q_{12}$. V_s is the secondary voltage. Note that Q_{11} and Q_{12} are held open.

to configure the rectifier as a half-bridge, Q_{11} and Q_{12} are held open while in the low-power mode, while Q_9 and Q_{10} switch in an alternating manner. Q_{LP} is held closed (on) while in low-power mode, as well. The resulting secondary waveform is therefore half the amplitude of the full-power mode secondary waveform. The rectifier waveforms are shifted from the inverter waveforms by a time t_{shift}, which corresponds to an electrical angle ϕ. The deadtime between each half-bridges' top and bottom switches is shown by dashed lines and labeled dt_{rect}.

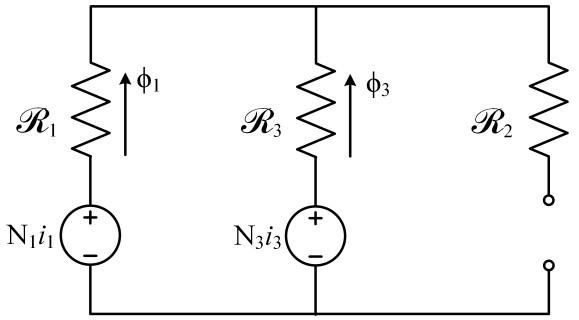
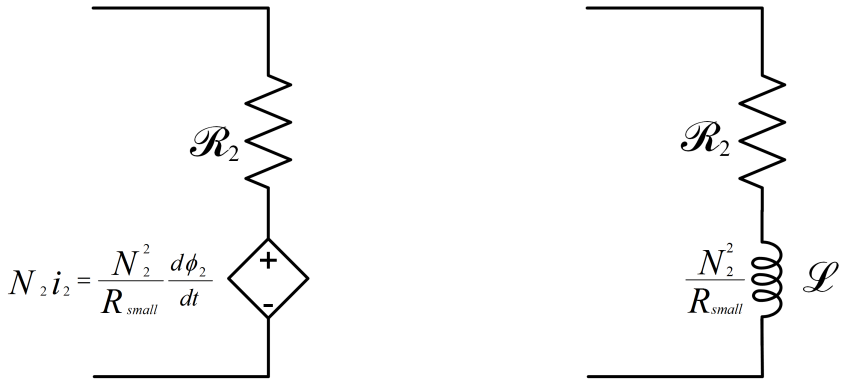


Figure 3-14: Magnetic circuit model for the three-winding transformer in the low-power mode, where one primary is held at zero voltage by shorting the corresponding winding. This is modeled as an open circuit in that winding's flux path. Let $v_1 = v_p, v_2 = 0, v_3 = -v_s, N_1 = N_2 = N$, and $N_3 = 1$. This simplified model does not show flux paths going outside the core. These flux paths do provide leakage inductance which is utilized in the converter.



(a) dependent source $N_2 i_2$ (b) transferance, $\mathscr{L}$

Figure 3-15: (a) A model of the shorted winding as a dependent source that produces a current i_2 to effectively cancel all flux in this leg. Note that nonidealities in the winding path are represented by the small resistance R_{small}. (b) Equivalent transferance model, showing the shorted winding as having a transferance $\mathscr{L} = \frac{N_2^2}{R_{small}}$

A simplified magnetic circuit model for the transformer in the low-power mode is shown in Fig. 3-14. For simplicity of description, we neglect leakage flux outside of the core. Winding 2 is (ideally) shorted, and carries whatever current is necessary to keep flux from flowing through it, ideally resulting in an effective open circuit for the flux path in the magnetic circuit model. Nonidealities - such as small resistance in the shorting winding - appear as a large transferance (the magnetic equivalent of inductance) in the magnetic circuit model [16].

Fig. 3-15 shows a more detailed model of the open-circuited flux path in Fig. 3-14. Although the total flux in the right-most leg (winding 2) is zero, there is a current $N_2 i_2$ in the leg. The shorted winding, however, acts as a dependent source, as shown in Fig. 3-15 (a), that generates whatever current is necessary to cancel the flux flowing through that leg. Assuming some small resistance R_{small} in the flux path, the result can be modeled as a large transferance of value $\mathscr{L} = \frac{N_2^2}{R_{small}}$.

For purposes of simplified modeling, we treat the shorted winding as providing an open-circuit to flux and yielding zero voltage on the winding. Then, substituting $v_2 = 0$ into (3.4), the following relationship is found

$$\begin{aligned} \frac{v_1}{N_1} + \frac{0}{N_2} + \frac{v_3}{N_3} &= 0 \\ \frac{v_p}{N} + \frac{0}{N} + \frac{-v_s}{1} &= 0 \end{aligned} \tag{3.7}$$

This can be arranged to get the following relationship between the voltages of the two primaries and secondary for low-power mode operation

$$\frac{v_p}{N} = v_s \rightarrow \frac{v_p}{v_s} = N \tag{3.8}$$

Notice that this is different from the relationship obtained for full-power mode in Eqn. (3.5) by a factor of 2. To compensate for this mismatch, the rectifier is configured as a half-bridge by closing Q_{LP}. Since the two capacitors labeled C_{LP} in Fig. 3-11 are in series and connected across the output, they will each be charged to $\frac{V_{out}}{2}$. Therefore, when Q_{LP} is activated, the secondary voltage will swing from $+\frac{V_{out}}{2}$ to $-\frac{V_{out}}{2}$. The

secondary voltage in the low-power mode is then effectively half that of the full-power mode. Substituting $\frac{v_s}{2}$ for v_s in Eqn. (3.8), we can see that the correct transformer ratio can be maintained the same as in the full-power mode.

$$\frac{v_p}{\frac{v_s}{2}} = \frac{2v_p}{v_s} = N \tag{3.9}$$

Therefore, the power characteristic for the low-power mode can be found by substituting in the new primary and secondary voltages in terms of the dc input and output voltages

$$P_{out,LP} = \frac{(\frac{V_{in}}{4} + 0)\frac{V_{out}}{2}N}{2\pi f_s 2L}\phi(1 - \frac{\phi}{\pi}) \tag{3.10}$$

In this low power mode, the converter thus naturally delivers a quarter of the normal mode power for a given phase shift ϕ.

In addition to changing the operating space of the converter, the low-power mode also helps to decrease switching loss and core loss. The higher currents for a given output power compared to the full-power mode also help to maintain ZVS over a wider range of loads. Since the winding is relatively underutilized at low power, this is a good trade-off. Core loss and switching loss savings in the low-power mode are detailed below.

Core Loss

Using the Steinmetz equation, the core loss for the three winding transformer can be compared for the full-power and low-power modes. The peak magnetic flux density, looking at a single core leg having a primary winding, can be expressed as

$$B_{pk,1} = \frac{V_{pk}\frac{T}{2}}{N\frac{A_e}{2}} = \frac{\frac{V_{in}}{4}}{NfA_e} = B_{pk,2} \tag{3.11}$$

where $B_{pk,1}$ and $B_{pk,2}$ here are the peak magnetic flux densities in the core leg sections for each primary winding, V_{pk} is the magnitude of the voltage excitation on the primary, T is the period of the voltage excitation on the primary, N is the turns ratio from primary to secondary, A_e is the area of the core (specifically the core centerpost),

and f is the frequency of the voltage excitation on the primary. The magnitude of the primary voltage waveform can be expressed in terms of the dc input voltage, and as described above is $\frac{V_{in}}{4}$. The core area is divided by 2 in the above expression, since each primary is would around the outer leg of the E-I core, which has half the area of the center post for the core used.

The power loss in the core while operating in full-power can then be expressed as

$$P_{core,full-power} = K p_{v,sin} \left(\frac{f}{f_0}\right)^{\alpha} \left(\left(\frac{B_{pk,1}}{B_0}\right)^{\beta} + \left(\frac{B_{pk,2}}{B_0}\right)^{\beta}\right) \frac{V_c}{2} \tag{3.12}$$

where f is the actual operating frequency; $B_{pk,1}$ and $B_{pk,2}$ are the actual operating peak sinusoidal flux densities at a standard operating temperature T_{op}; K is a multiplication factor for the particular core shape used; $p_{v,sin}$ is the loss density at the standard operating temperature T_0, base frequency f_0 and peak sinusoidal flux density B_0; α is the Steinmetz exponent for frequency; and β is the Steinmetz exponent for flux density for the core material at T_0, and V_c is the magnetic volume of the core. Core volume is divided by two here because there are two primaries each contributing flux, but their individual fluxes can be imagined as only traveling through half the volume of the core. It is also noted that to use typical Steinmetz loss data, the loss for a triangular flux waveform (as in the double stacked-bridge converter) is being modeled the same as for a sinusoid of the same peak flux value. This is only a rough approximation, but is sufficient for illustrating how loss scales.

For the low-power mode, the peak magnetic flux density remains the same, but now there is only one primary that is energized at a time. As can be seen in Fig. 3-12, the amplitude of the primary voltage waveform is the same as that of the full-power mode, but there is also a period where the voltage is zero. If we assume no flux in the outer leg that corresponds to the shorted winding, the center leg will have reduced flux density due to the one-primary drive. A overestimation of the core loss can be found by letting one of the B_{pk} terms go to zero, as shown in:

$$P_{core,low-power} = K \left(\frac{f}{f_0}\right)^{\alpha} \left(\left(\frac{B_{pk,1}}{B_0}\right)^{\beta} + 0\right) \frac{V_c}{2} \tag{3.13}$$

which, given the exponent β, is much lower than the core loss in the full-power mode. Note that because the center leg flux is reduced due to only one primary driving flux into it at a time, the actual core loss will be a little bit lower.

Switching Loss

Because the low-power mode naturally increases the converter currents for a given output power, it maintains ZVS down to a lower power level than compared to the full-power mode, as there is more current available to charge and discharge the device parasitic output capacitances. Too little current can mean that the voltage across the switch can only partially charge or discharge, and then hard-switches for the rest of the voltage transition. In addition to loss, there can be severe ringing in these hard transitions, resulting in high EMI. Losing soft-switching can rapidly reduce the efficiency of the converter, so extending the ZVS range is of great importance for maintaining high efficiency at light-load. Additionally, as can be seen by comparing Fig. 3-9 and 3-12, the low-power mode has fewer switch transitions, which can further help reduce switching loss at very low powers once ZVS is no longer possible (as hard-switching loss is roughly $\propto CV^2f$). Chapter 7 will provide experimental waveforms showing the loads at which the different modes and topologies lose ZVS.

The low-power mode offers a way to reduce switching loss and extend the range of output powers for which ZVS is achieved, thereby greatly increasing the light-load efficiency of the converter. Additionally, it also allows for switching patterns that reduce core loss by only energizing half the transformer core at a time to further boost efficiency, and because relatively low power is being delivered, conduction loss in this mode is not severe.

Chapter 4

Semiconductor Selection for the Converter Prototype

As one of the major goals of this work is to produce a converter that performs with high efficiency over the entire load range, the device selection for the inverter and rectifier bridges is of great importance. Additionally, since this converter is designed for a high-voltage input of 380 V, finding switches rated for that voltage that still maintain good switch characteristics is non-trivial, and is a strong motivation for using a stacked topology, as described in Chapter 3.

This chapter presents a comparison of different available transistors for use in the Double-Stacked Active Bridge (DSAB), as well as for use in a modified Single-Stacked Dual Active Bridge (DAB) and a more traditional Full-Bridge DAB. This includes exploration of several different device technologies, such as GaN FETs, Si MOSFETs, and Superjunction MOSFETs.

The efficiency of dc-dc power converters is strongly dependent on the on-state resistance, $R_{ds,on}$, of the devices. Higher $R_{ds,on}$ corresponds to higher conduction losses, which decrease overall efficiency. Many modern switch technologies can achieve very low $R_{ds,on}$, but at the expense of higher parasitic capacitances. For soft-switched converters, such as this converter, the parasitic output capacitance, C_{oss}, is of particular importance, as its value impacts the ability of the switches to achieve zero-voltage transitions. A heavily simplified figure of MOSFET parasitic resistances and capac-

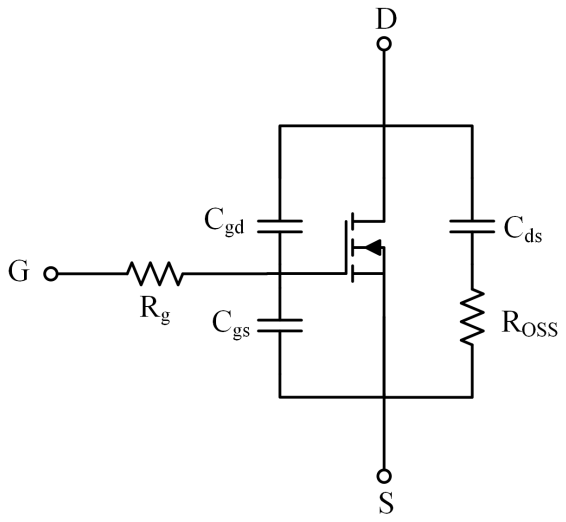


Figure 4-1: Equivalent circuit parasitic model for a power MOSFET, incorporating parasitic resistances and capacitances.

itances is shown in Fig. 4-1. $R_{ds,on}$ represents the resistance of the drain to source path when the MOSFET is conducting, and is not shown as an external discrete resistance. Note that this model does not include any parasitic inductances of bond-wires or other packaging and internal routing.

R_g is the parasitic gate (G) resistance, and R_{oss} is the equivalent series resistance (ESR) of the parasitic capacitance C_{ds} between the drain (D) and source (S) terminals [17] [18]. The parasitic resistance of the parasitic capacitance C_{gd} between the gate and drain terminals is not shown here. Often, the parasitic capacitances of the devices are listed in terms of C_{iss}, C_{oss}, and C_{rss} in device datasheets. The relationship between these parameters and the device model parasitic capacitances are given below:

$$C_{iss} = C_{gs} + C_{gd} \quad C_{oss} = C_{ds} + C_{gd} \quad C_{rss} = C_{gd} \tag{4.1}$$

4.1 Soft-Switching Figure-of-Merit

In order to compare various device technologies, as well as to compare topologies that require different voltage ratings, the following figure-of-merit was used to determine

device performance:

$$FOM = R_{ds,on}C_{oss} \tag{4.2}$$

This figure-of-merit precisely relates to the conduction loss in some high-frequency inverters, such as the classical Class E inverter [19], and is a useful qualitative metric for the ZVS bridge inverters and rectifiers considered here. As described in Chapter 3, $R_{ds,on}$ and C_{oss} are related to the two main loss mechanisms in the switches: conduction loss, and the ability to maintain zero-voltage switching (ZVS) over a wide load range and minimize switching loss.

Conduction losses due to the on-state resistance of the transistor can be expressed as:

$$P_{cond} = I_{RMS}^2 R_{ds,on} \tag{4.3}$$

where I_{RMS} is the RMS current flowing through the switch while it is on.

In a hard-switched converter, the energy needed to charge and discharge the output capacitances is dissipated each cycle. Assuming a linear output capacitor for simplicity, this switching loss can be expressed in terms of dissipated power as follows:

$$P_{sw} = C_{oss}V_{in}^2 f \tag{4.4}$$

where C_{oss} is the parasitic output capacitance described above, V_{in} is the voltage the switch must block in the off state, and f is the switching frequency of the devices. This accounts for the capacitive turn on loss in each device in a half-bridge for complete charging / discharging of the two device capacitances in the half-bridge. This loss (or a portion of it) will be present in a ZVS converter if the converter ever loses soft switching.

In a converter operating with ZVS, however, this energy used to charge and discharge the output capacitances is either delivered to the load or is shuttled between devices. In the DSAB described here, the inductor current is used to charge and discharge the capacitances on the stacked bridges. Because the inductor current is bidirectional, both turn-on and turn-off transitions can be soft-switched. However, the amount of current necessary to complete the required voltage transitions on the

switch capacitances is dependent on the value of that capacitance.

As described in [2], the snubber capacitance C_{oss} affects the minimum leakage inductor current required for the inverter devices to achieve ZVS. Assuming Q_1 is the high-side device in a half-bridge and Q_2 is the corresponding low-side device, let Q_1 currently be on and Q_2 be off. When Q_1 turns off, the current through the leakage inductor L will resonantly charge the voltage of the output capacitance of Q_1 (previously on) and discharge the voltage of the output capacitance of Q_2 (previously off). A minimum current $i_{l,min}$ is required to ensure that the voltage transitions are fully completed within the given transition time (i.e. the deadtime). At t_0 when Q_1 turns off, $i_l = i_{l,min}$, $v_{c,Q1} = 0$, and $v_{c,Q2} = V_i$, where V_i is the voltage the switch blocks when off (the exact value depends on whether the switch is in a full-bridge or half-bridge / stacked-full-bridge topology) and v_c is the voltage on the switch output capacitance. At t_1 (the end of the deadtime period), $i_l = 0$ and ZVS conditions require that $v_{c,Q1} = V_i$, $v_{c,Q2} = 0$. Therefore, the minimum current required to charge and discharge the capacitors can be found in the form of $i_c = C\frac{dV_c}{dt}$, as given below:

$$i_{l,min} = 2C_{oss}\left(\frac{dV_c}{dt}\right) = 2C_{oss}\left(\frac{\frac{V_{in}}{2}}{dt_{sw}}\right) \tag{4.5}$$

where dV_c is the change in voltage on the switch capacitance and dt_{sw} is the deadtime, which is the maximum time the voltage transition can take while still achieving ZVS. ZVS also requires that $dV_c = \frac{V_{in}}{2}$ for the DSAB converter, as each stacked full-bridge swings from 0 to $\frac{V_{in}}{2}$. Note that the above analysis neglects the device turn-off time and assumes that the switch capacitance voltage changes very little during this turn-off time.

From this, it can be seen that larger values of C_{oss} require higher minimum currents through the leakage inductance for a given deadtime to achieve ZVS. This means that during light-load conditions, when the current is much lower than at the nominal operating point, the converter can lose ZVS. The deadtime can be lengthened to allow the current through the inductor to ramp for a longer period of time, but this increases conduction losses, and there is a current level below which no amount of

deadtime is sufficient to provide ZVS, as there is not enough energy in the leakage inductance to fully transition the device voltages. Additionally, if the converter loses soft-switching, it will experience switching losses as described above, and may also exhibit higher EMI.

Devices that have very low values of $R_{ds,on}$ typically have higher values of C_{oss} due to the semiconductor construction. Therefore, a reasonable metric would be to minimize the product of $R_{ds,on}$ and C_{oss} in order to find the most compatible devices. In addition, because one of the main goals of this thesis was to demonstrate a topology with high efficiency even at light loads, devices with low values of C_{oss} are preferentially valued in order to allow the converter to achieve ZVS at as low loads as possible. A plot of $R_{ds,on}C_{oss}$ vs. C_{oss} is therefore valuable to determine the best devices for this application.

4.2 Device Technologies

Three main technologies were looked at when selecting devices, listed below:

- GaN FET devices
- Si vertical power MOSFET devices
- Si Superjunction MOSFET devices

4.2.1 GaN FET vs. Si MOSFET

Emerging GaN-on-Si power transistors offer several benefits over traditional Si MOSFETs, including lower $R_{ds,on}$, gate charge Q_g, gate resistance R_g, and output capacitance C_{oss}. Lower $R_{ds,on}$ helps increase efficiency overall by decreasing conduction losses, and lower Q_g and R_g allows devices to be switched much faster. The low C_{gd} and C_{gs} values in GaN also leads to lower values of C_{oss} compared to Si devices for a given $R_{ds,on}$ value. The $R_{ds,on}$ of GaN devices is also lower for a given breakdown voltage compared to Si due to the different semiconductor properties and manufacturing process. Additionally, GaN devices lack the parasitic bipolar junction present

in Si MOSFETs, responsible for the "body diode" of the MOSFET and the associated reverse recovery losses [20]. At the same time, GaN-on-Si FETs are in their relative infancy, so the voltage ratings available at the time of writing are still limited to relatively low values, typically up to a few hundred volts, but with very few 600/650 V devices starting to become available.

Because of these many benefits, the DSAB converter was designed with GaN FETs in mind, in order to increase efficiency and extend the ZVS range as much as possible. However, a DSAB prototype using Si MOSFETs was also assembled and tested, and comparisons of the respective efficiency curves are given in Chapter 7.

4.2.2 MOSFET vs. Superjunction MOSFET

As the voltage rating of traditional Si MOSFETs increases, the $R_{ds,on}$ values can dramatically increase as well. For traditional vertical MOSFETs, lower $R_{ds,on}$ values can be achieved with larger die sizes, but at the price of increased gate and output capacitances. In an application where wide-range ZVS operation is necessary, this can result in many challenges in trying to balance conduction and switching losses. The overall $R_{ds,on}$ is related to three components: the resistance of the channel, the epitaxial layer, and the substrate. For low voltage devices, the resistance is somewhat evenly divided between all three.

However, as the voltage rating is increased, the epitaxial layer thickness must also be increased to provide a high enough breakdown voltage for the device. This results in the epitaxial resistance contributing to a much higher percentage of the overall resistance, as well as leading to a much higher overall $R_{ds,on}$. By some metrics [21], for every doubling of the voltage rating, the area required to maintain a constant $R_{ds,on}$ increases by a factor of five; or, for every doubling of the voltage rating while maintaining constant die size, $R_{ds,on}$ can increase by a factor of three to five. Superjunction MOSFETs seek to alleviate this problem by using a MOSFET structure that can greatly reduce the thickness of the epitaxial layer for a given voltage rating. Superjunction devices can have a linear relationship between the on-resistance and the voltage rating, rather than the exponential one typical of traditional MOSFET

designs ($R_{DS,ON} \propto BV_{DSS}^{k}$, where $k > 2$).

Additionally, Superjunction MOSFETs can have reduced gate and output capacitances due to smaller die areas, so the technology can decrease the $R_{ds,on}$ and C_{oss} values in the figure-of-merit expression. However, Superjunction devices are most effect for, and hence commercially available in, voltages above 500 V, so they are not typically used in low voltage applications.

4.3 Inverter

Two prototypes of the DSAB topology were built: one populated with GaN FETs and one populated with traditional Si power MOSFETs. For the DSAB, as explained in Chapter 3, each switch must be able to block $\frac{V_{in}}{4}$. For the high end of the input voltage range, this voltage is $\frac{410}{2} = 102.5$ V. A 200 V EPC GaN device was chosen for the GaN prototype, and a 200 V Si MOSFET was chosen for the Si prototype. Two printed circuit boards (PCBs) were laid out: one with an EPC GaN device package, and one with a DPAK package that was able to be used for both the DSAB Si board and a modified single-stacked dual-active-bridge (DAB).

Devices for a single-stacked DAB consisting of one stacked full-bridge inverter were also selected. The singe-stacked DAB was constructed using the same PCB as for the double-stacked, but with only the top and bottom half-bridge inverters populated to create a single stacked full-bridge inverter. The two primaries of the three-winding transofrmer were connected in series in order to form one single primary winding. For the single-stacked DAB, the switches must be able to block $\frac{V_{in}}{2}$, which for the high end of the voltage range is $\frac{410}{2} = 205$ V. Traditional 250 V Si MOSFETs, 300 V GaN devices, and 550 V Si Superjunction devices were explored and a selected subset were simulated. However, only a Si Superjunction prototype was built, due to the layout and footprint constraints of the modified PCB.

Finally, devices for a more traditional full-bridge DAB were also selected. For this design, 650 V GaN devices and the same 550 V Si Superjunction devices as used in the single-stacked DAB were used in simulation. These switches must be able to

block the full input voltage V_{in}, or 410 V. Simulation results of all three topologies with both Si and GaN devices and their calculated $R_{ds,on}$ and C_{oss} are presented in Chapter 6.

For the input stage, preliminary simulation of the devices showed an average RMS current through the switches of 2 A or less. All the devices presented here meet this current rating.

4.3.1 Selection of Devices for Double-Stacked Active Bridge (DSAB)

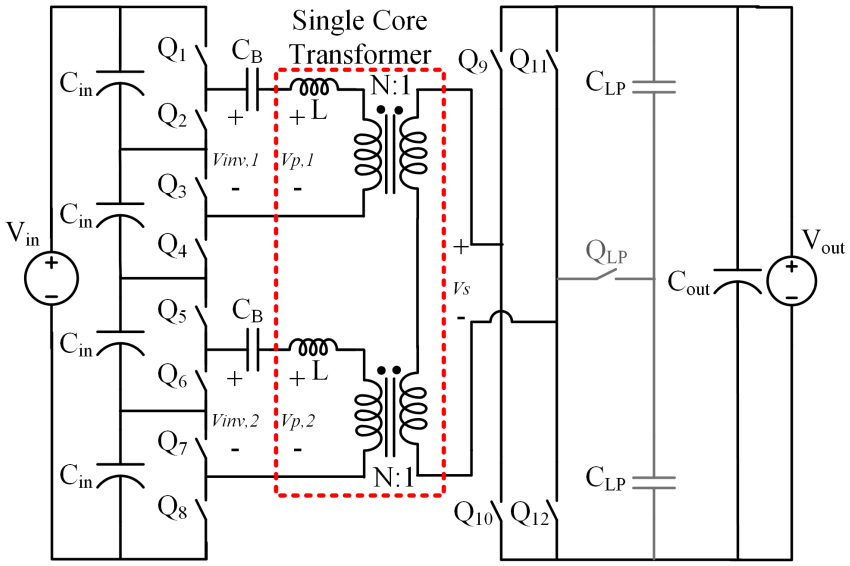


Figure 4-2: Circuit diagram of the proposed double stacked active bridge topology. Inverter devices must be rated for $\frac{V_{in}}{4}$.

In order to evaluate the actual efficiency increase from using GaN devices over Si devices for the DSAB topology, shown again in Fig. 4-2, both GaN and Si devices were chosen for the inverter bridges. As GaN devices cannot be driven with a higher gate drive voltage than 6 V, drivers designed for enhancement mode GaN FETs were chosen. The complete Bill-of-Materials for all prototypes is included in Appendix D. In order to minimize drive circuit layout changes between the boards, Si devices that were capable of being logic-level driven were preferred. Additionally, low Q_g and R_g values were preferred in order to minimize gating loss.

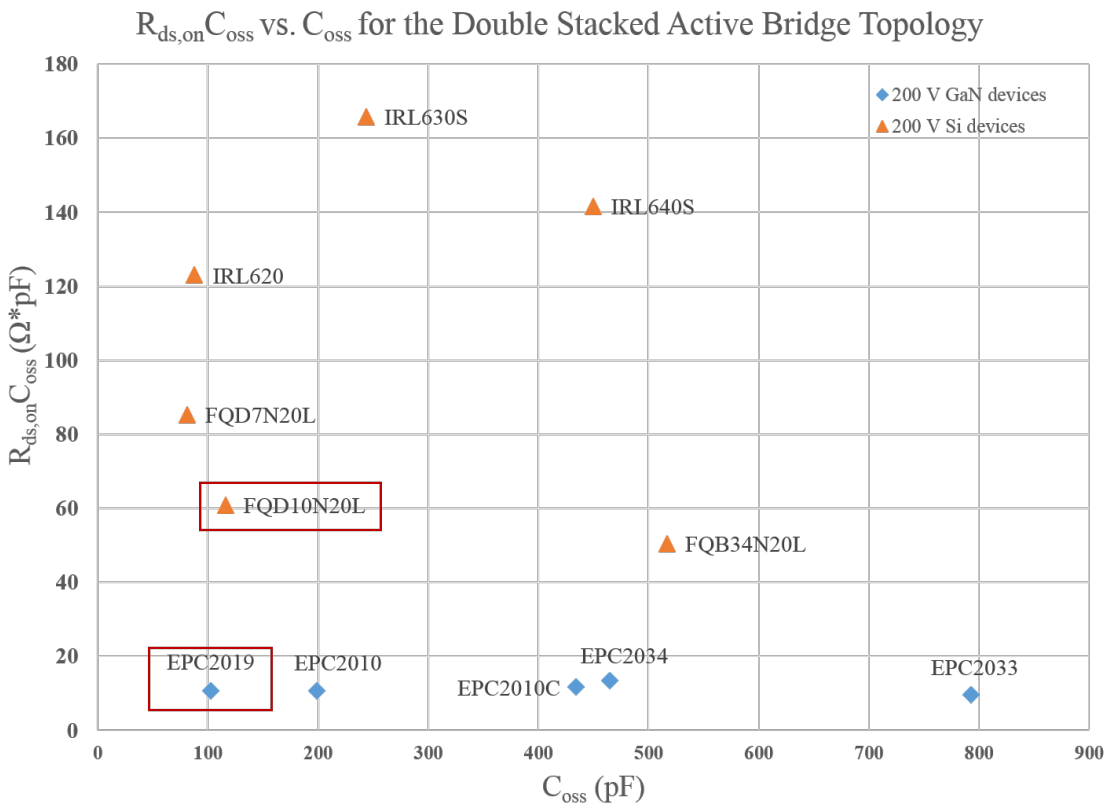


Figure 4-3: A plot of the figure-of-merit $R_{ds,on}C_{oss}$ vs. C_{oss} for 200 V GaN and Si devices for use in the DSAB topology. The selected GaN and Si devices are shown boxed in red.

In order to evaluate the devices, the figure-of-merit $R_{ds,on}C_{oss}$ was calculated as follows: the value of $R_{ds,on}$ was taken at a V_{gs} of 5 V, as close to the rated current as possible given the datasheet values presented, and then de-rated for a junction temperature T_j of 100° C; the value of C_{oss} was calculated using the curve of C_{oss} vs. V_{ds} by hand-calculating the area under the curve up to the blocking voltage that the switch would see in the circuit (roughly 100 V for double-stacked, 200 V for single-stacked, and 400 V for full-bridge), and using an equivalent "chordal" capacitance $C_{eff} = \frac{Q}{V}$. The product $R_{ds,on}C_{oss}$ was then graphed against C_{oss}, as too high a value of C_{oss} can severely limit the ZVS range and result in low efficiency, even if the overall figure-of-merit is low.

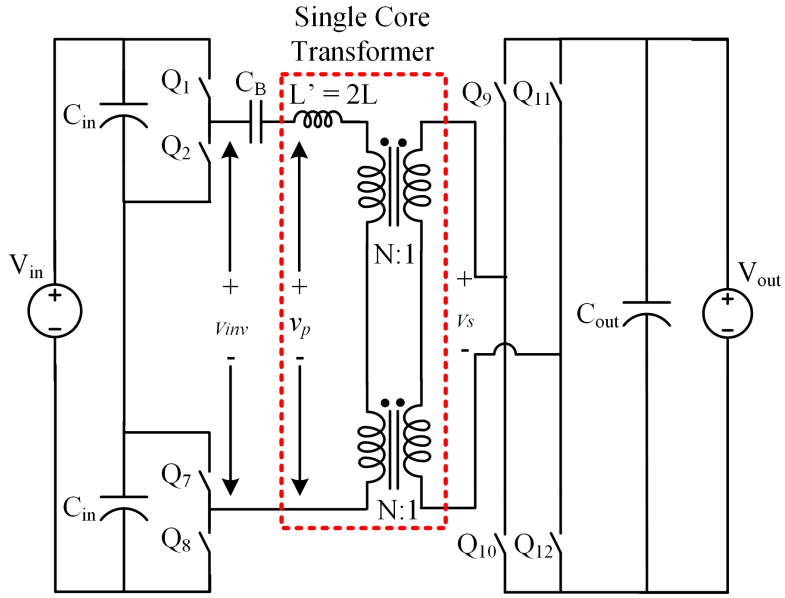
A plot of $R_{ds,on}C_{oss}$ vs. C_{oss} is shown in Fig. 4-3 for both GaN and Si devices for the DSAB topology. As can be seen in the plot, the figure-of-merit for GaN devices

is much lower than that of Si devices for the same voltage rating. Based on this plot, the EPC2012C device was chosen for the GaN double-stacked inverter, while the FQD10N20L was chosen for the Si double-stacked inverter. Although the EPC2034 device had a better overall figure-of-merit, it has a much higher C_{oss} than desired ($\sim$800 pF), while the EPC2012C device has $\sim$100 pF. This lower capacitance means the switches can maintain ZVS over a wider load range. Similarly, FQD10N20L was chosen for the Si device even though FQB34N20L had lower overall figure-of-merit, because it has lower C_{oss}.

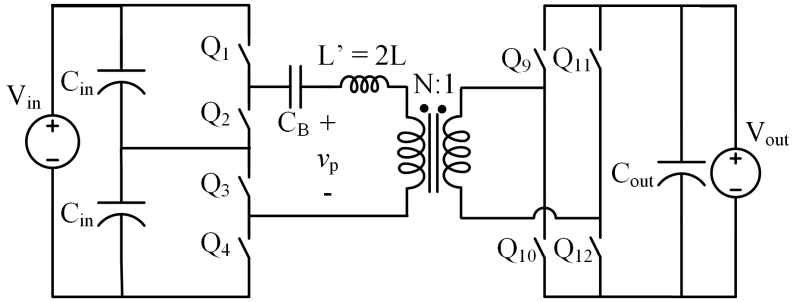
4.3.2 Selection of Devices for Single-Stacked Dual Active Bridge (DAB)

To compare the proposed DSAB topology and its two-primary transformer with a more traditional DAB structure, a single-stacked DAB was also simulated and built. A circuit diagram of the single-stacked DAB is shown in Fig. 4-4. Three different device technologies were looked at for the single-stacked DAB. The switches in the single-stacked DAB must block $\frac{V_{in}}{2}$, or at least 205 V. Therefore, 250 V Si MOSFETs and 300 V GaN FETs were explored. Note that EPC only offers FETs at 200 V or 300 V, so there are no intermediate range options. Si Superjunction MOSFETs were also explored, as they offer decreased $R_{ds,on}$ while still maintaining reasonable C_{oss}. However, the device technology for Superjunction is only applicable in higher-voltage rated devices, such as above 500 V.

A plot of $R_{ds,on}C_{oss}$ vs. C_{oss} is shown in Fig. 4-5 for devices for use in the single-stacked DAB topology. The Infineon 550 V Superjunction IPD50R280CE was chosen, as it had a resonably low figure-of-merit $R_{ds,on}C_{oss}$ for a low amount of C_{oss}. Although the 250 V Si MOSFET STL52N25M5 has a lower figure-of-merit and a lower C_{oss}, it comes in a PowerFLAT (5x6) footprint while the IPD50R280CE comes in a DPAK footprint, the same footprint as the selected Si MOSFET for the DSAB topology. This would allow the same PCB to be used for both prototypes, saving on prototyping costs. Additionally, the STL52N25M has a maximum gate threshold voltage, $V_{gs,th}$,



(a)



(b)

Figure 4-4: (a) Implementation of a DAB converter that uses a stacked full-bridge rather than a traditional full-bridge on the high-voltage side. The same magnetic component (again boxed with a dashed red line) was used as in the DSAB design, with the two primary windings connected electrically in series. There is thus only one primary winding, as opposed to the two-primary winding structure of the DSAB. (b). Equivalent circuit for this single-stacked DAB converter. The total leakage inductance is now $L' = 2L$, as the total primary-referred leakage inductance is now modeled as a single element.

of 5 V, meaning that it could have trouble being driven with logic-level gate drivers, while the IPD50R280CE has a maximum gate threshold voltage of 3.5 V and is

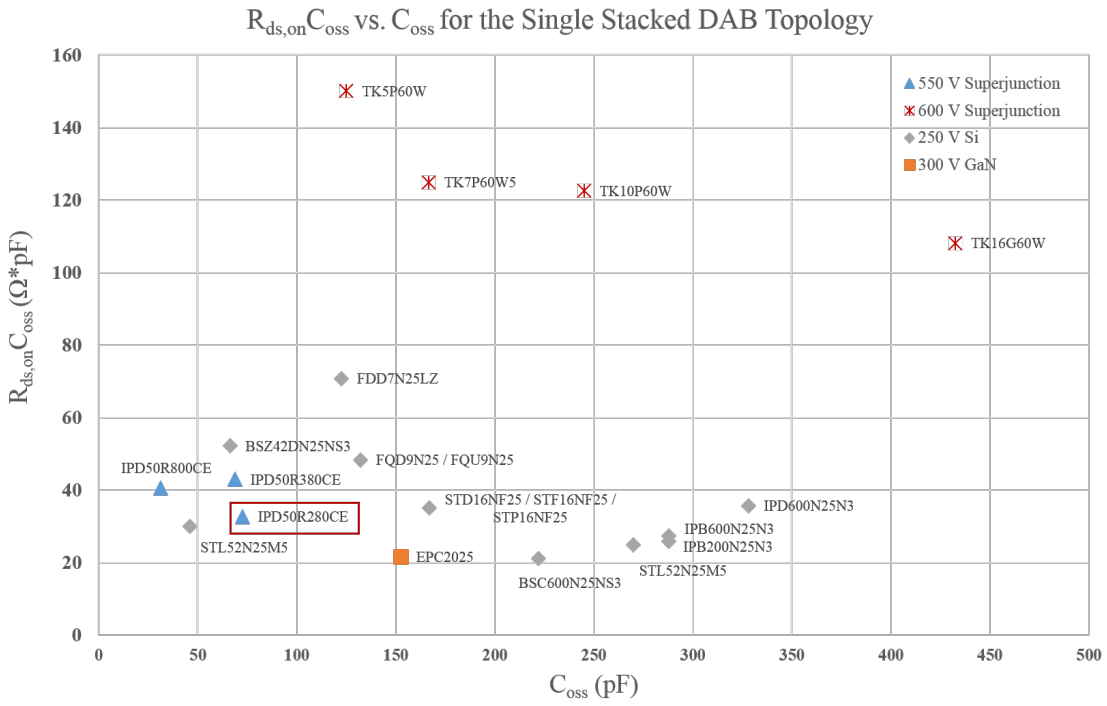


Figure 4-5: A plot of the figure-of-merit $R_{ds,on}C_{oss}$ vs. C_{oss} for 250 V Si MOSFETs, 300 V GaN FETs, and 550 V and 600 V Si Superjunction MOSFETs. The selected device for the single-stacked DAB prototype is shown boxed in red.

capable of being driven with logic-level gate drives. The GaN device available from EPC, the EPC2025, does have an overall lower figure-of-merit, but at a higher C_{oss}. A prototype was not made for a GaN single-stacked DAB because it would require a new inverter switch layout, resulting in an additional set of PCBs manufactured. While only a prototype using the Si Superjunction device was experimentally tested, simulations were done using both the IPD50R280CE and the EPC2025, to compare Si vs. GaN devices for a single-stacked DAB topology.

4.3.3 Selection of Devices for Full-Bridge Dual Active Bridge (DAB)

Simulations were also done to compare the traditional full-bridge DAB topology (repeated here in Fig. 4-6) to the single-stacked DAB and the DSAB converter topologies. The inverter switches in the full-bridge topology must be able to block the full

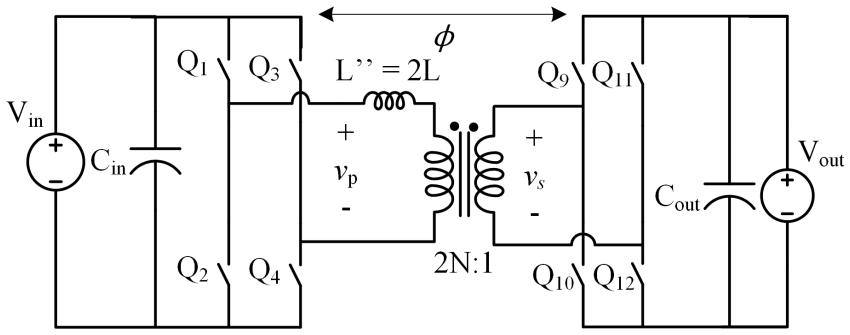


Figure 4-6: A traditional DAB converter with a full-bridge on both the input and output bridges. There is only one primary winding, as opposed to the two-primary winding structure of the DSAB. The total leakage inductance $L'' = 2L$ and the turns ratio is now $2N : 1$ due to the fact that the primary voltage is twice that in the DSAB or the Single-Stacked DAB.

input voltage, V_{in}, which is 410 V at the high end of the input voltage range. While this voltage range is above that offered by the EPC GaN devices, high-voltage devices from GaN Systems are available at the 650 V level.

A plot of $R_{ds,on}C_{oss}$ vs. C_{oss} is shown in Fig. 4-7 for devices capable of being used in the full-bridge DAB. As can be seen in the plot, the 650 V GSS6516T from GaN Systems has a much lower overall figure-of-merit, but does have higher C_{oss} than the Superjunction FETs. Simulations of the full-bridge DAB topology using both the GSS6516T and the IPD50R280CE are presented in Chapter 6, and both show less optimal performance compared to the DSAB and single-stacked DAB.

A plot of $R_{ds,on}C_{oss}$ vs. the breakdown voltage BV_{DSS} (effectively the voltage rating) of the devices explored above is shown in Fig. 4-8. The selected GaN and Si devices for the DSAB topology are shown boxed in red. The devices are color-coded by device technology and the topology they would be applicable for, as shown in the legend. As can be seen in the figure, the DSAB GaN and Si devices have some of the lowest (best) figures-of-merit. Although the 650 V GaN device also has a low figure-of-merit, a full-bridge DAB will experience much greater switching losses due to the $C_{oss}V_{in}^2 f$ losses in the case where it loses soft-switching, as the V_{in} term is four times that of the DSAB topology (380 V vs. 95 V at the nominal operating point), and is then squared.

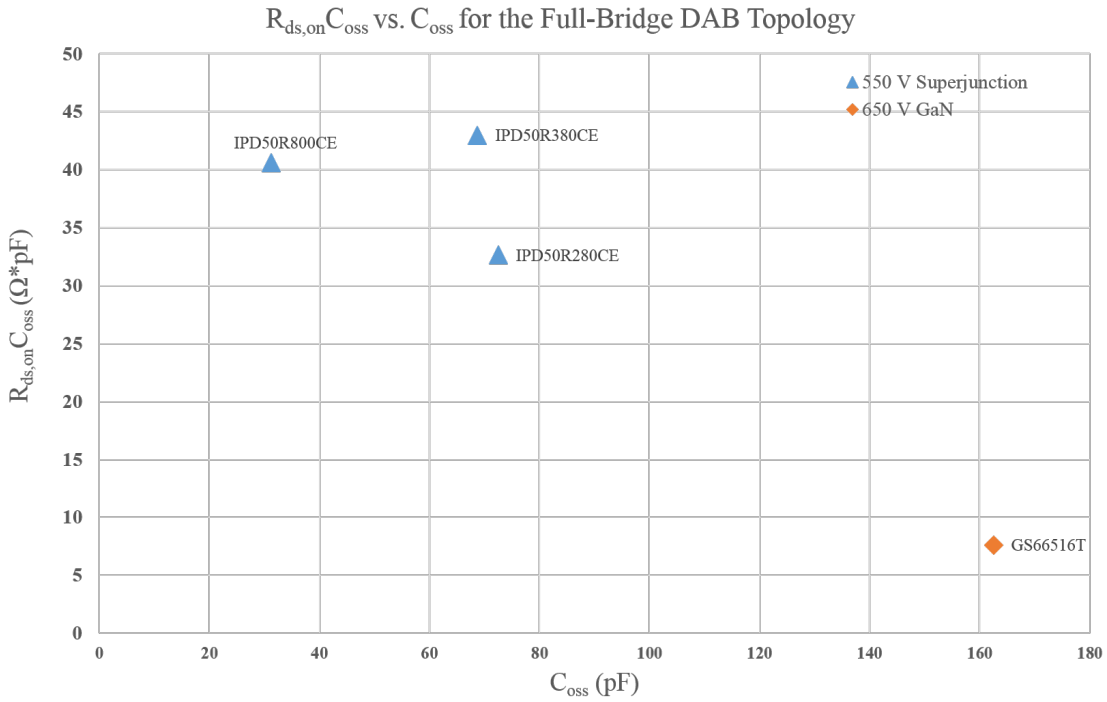


Figure 4-7: A plot of the figure-of-merit $R_{ds,on}C_{oss}$ vs. C_{oss} for 550 V Si Superjunction MOSFETs and a 650 V GaN FET.

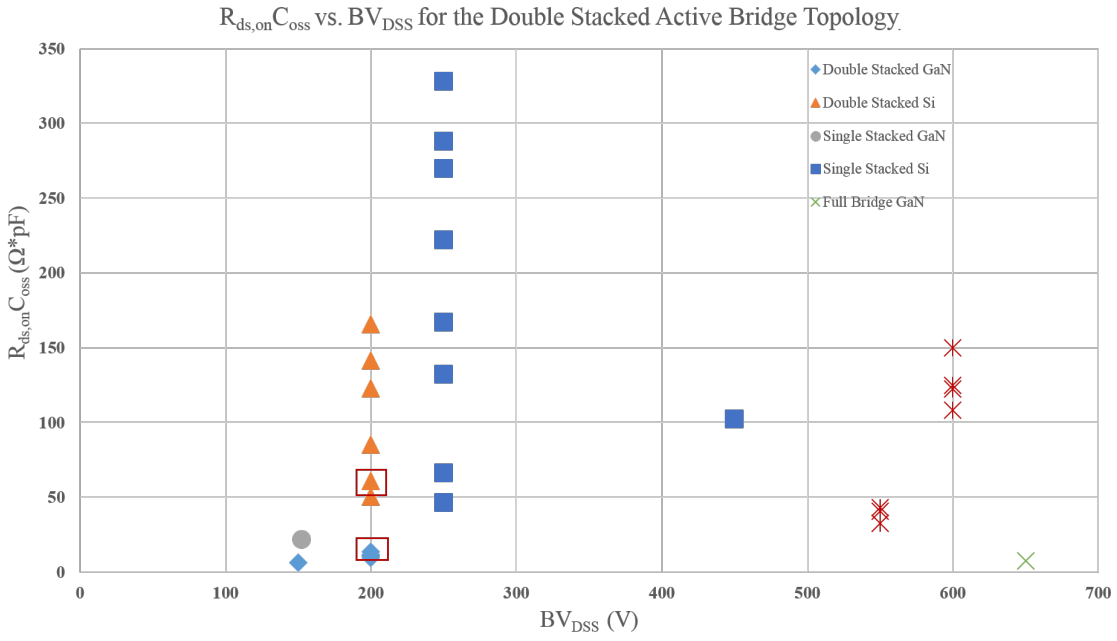


Figure 4-8: A plot of the figure-of-merit $R_{ds,on}C_{oss}$ vs. the device breakdown voltage BV_{DSS} for all the devices explored. The selected GaN and Si devices for the DSAB topology are shown boxed in red.

Fig. 4-8 showcases the benefits of using lower-voltage devices, which is achievable using a stacked topology. Simulation data presented in Chapter 6 will further validate the efficiency gains of the DSAB compared to both the single stacked DAB and the full-bridge DAB.

A summary of the devices chosen for each topology is presented in Table 4.1.

Topology	GaN	Si	Superjunction
DSAB	EPC2012C	FQD10N20L	N/A
Single-Stacked DAB	EPC2025*	N/A	IPD50R280CE
Full-Bridge DAB	GS66516T*	N/A	IPD50R280CE*

Table 4.1: Table of the devices selected for simulation and PCB layout for the DSAB, Single-Stacked DAB, and Full-Bridge DAB topologies. An (*) denotes that the device was only simulated, not experimentally tested.

4.4 Rectifier

All prototypes were designed with the same rectifier layout and populated with the same devices. Because the output side of the DSAB, and the single-stacked DAB, and the full-bridge DAB is at a low voltage (12 V), a non-stacked full-bridge rectifier is used (the rectifier is capable of being reconfigured as a half-bridge for operation in the DSAB's low-power mode). Stacking devices at sub-100 V breakdown voltages adds little to no benefit in efficiency because switch characteristics across such a narrow range of breakdown voltages are not very different.

Additionally, because the output bridge carries high current (∼30 A at full load), minimizing $R_{ds,on}$ is more important than minimizing C_{oss} in the rectifier, for two reasons: 1) $I_{RMS}^2 R_{ds,on}$ losses are a major source of loss overall, and 2) since the current is so high, even relatively high C_{oss} values can be charged or discharged very quickly, allowing for the switches to achieve ZVS. Additionally, even if the switches do not achieve ZVS, their switching losses will be low, as the output bridge switches' blocking voltage is very low, decreasing the V_{in} term in the switching loss expression, $C_{oss} V_{in}^2 f$. Because of these reasons, the rectifier (low-voltage-side bridge) was designed with only GaN devices in order to maximize efficiency, as comparing device technologies

at such a low rated-voltage was not a focus of this work.

Table 4.2 presents the available EPC GaN devices up to a rated voltage of 60 V and 30 A, and gives their corresponding max $R_{ds,on}$ at $T_j = 25°$ C and typical $R_{ds,on}$ derated to a junction temperature $T_j = 100°$ C. The devices are ordered from lowest $R_{ds,on}$ to highest.

Part Number	$V_{ds,max}$ (V)	Max $R_{ds,on}$ at $T_j = 25°$ C (mΩ)	Typical $R_{ds,on}$ at $T_j = 100°$ C (mΩ)
EPC2023	30	1.3	1.5
EPC2024	40	1.5	1.77
EPC2020	60	2.2	2.25
EPC2030	40	2.4	2.61
EPC2031	60	2.6	2.9
EPC2015	40	4	4.54
EPC2015C	40	4	4.64

Table 4.2: Table of available EPC GaN devices for the rectifier full-bridge. Devices up to a voltage rating of 60 V and capable of carrying greater than 30 A were looked at. The table is sorted in order of increasing $R_{ds,on}$.

Using this, EPC2023 devices were chosen for the rectifier bridge, as they had the lowest $R_{ds,on}$.

4.4.1 Paralleling of Devices

In order to further decrease conduction losses, each switch in the full-bridge rectifier was implemented as three parallel devices each controlled by their own driver, but receiving the same gate drive signals. By paralleling devices, the overall resistance is ideally decreased as $R_{eq} = \frac{R_{ds,on}}{3}$ (neglecting interconnect resistance). However, each device's C_{oss} is now in parallel with two other devices' C_{oss}, leading to increased output capacitance. At full-load, this is outweighed by the savings in conduction loss because there is already very high current available for the ZVS transitions. However, at light-loads where the current is lower, the increased parasitic capacitance could have a more significant effect. In this case, switching losses could possibly be decreased by turning off one or two of the paralleled FETs (i.e. as in phase shedding

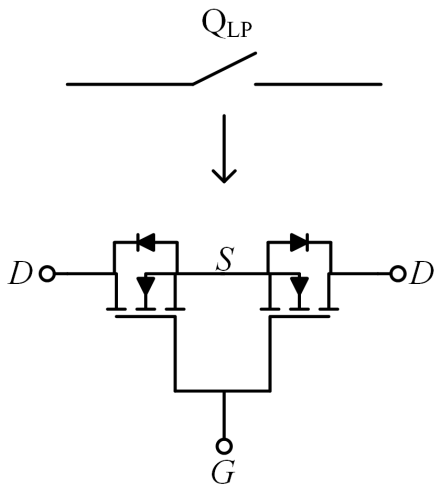


Figure 4-9: Implementation of the low-power auxiliary switch, Q_{LP}, using two source-connected FET devices with their gates tied together.

or gate-width switching). However, the prototypes presented here were not designed with the ability to selectively turn off paralleled devices while running.

4.4.2 Low-Power Switch Implementation

As described in Chapter 3, an auxiliary switch Q_{LP} (see Fig. 4-2) is included in the converter to allow for a mode switch into a low-power mode that reduces core loss, switching loss, and extends the ZVS range. The low-power switch is implemented with two FET devices that are source connected, as illustrated in Fig. 4-9. EPC2023 devices were again chosen due to their low $R_{ds,on}$. The low-power switch experiences an RMS current that is greater than the RMS current going through each rectifier switch, as Q_9 and Q_{10} in Fig. 4-2 conduct for only half the the switching cycle, while Q_{LP} conducts positive current for half of the switching cycle and negative current for the other half. However, because the converter will only be operating at low powers, the currents through Q_{LP} are well within the rated current for the device.

However, as will be shown in Chapters 6 and 7, minimizing the overall resistance of the low-power switch path, including board parasitics, is of great importance to increasing the efficiency of the DSAB converter while operating in the low-power mode. If the resistance is too high, the transformer current waveforms will have too

large a slope due to the resistive voltage drop on the low-power switch path resistance, which can increase conduction losses and affect the converter's ability to achieve ZVS.

Chapter 6 will present simulated efficiency curves and operating waveforms for the DSAB converter, the single-stacked DAB converter and the full-bridge DAB converter using the devices selected here, and Chapter 7 will present experimental efficiency curves and operating waveforms for the GaN and Si DSAB prototypes and a modified Si Superjunction single-stacked DAB prototype.

Chapter 5

Magnetics Design

The Double-Stacked Active Bridge (DSAB) topology uses a special three-winding leakage transformer that provides isolation, voltage transformation, power combining, and energy storage all in a single magnetic component. A single core is used to implement both a three-winding transformer consisting of two primary windings coupled to a single secondary winding, as well as the leakage inductance necessary for energy transfer. The magnetic component is implemented as a planar magnetic structure, as planar magnetics offer several benefits that can help improve power density and efficiency. An overview of the benefits of planar magnetics is given, followed by details of the physical realization of the transformer structure as well as loss modeling for it.

5.1 Benefits of Planar Magnetics

As described in [22], planar magnetics have several advantages over traditional wire-wound magnetic components. Planar magnetic structures use the printed circuit board (PCB) process to implement the windings as copper traces that have been etched to the correct geometry, rather than using discrete wires or foil sheets. Holes in the PCB can be routed out to allow for core legs or posts to fit around the windings, so as to completely encase them in magnetically permeable material. Some of the benefits of planar structures are summarized below:

- **Low profile components** - because the windings are only as thick as the PCB thickness (usually on the order of 62 mils), very low profile cores can be used to encase the windings. This helps to reduce the size and profile of magnetic components - which often take up a large amount of space in power converters - and to increase power density.
- **Good thermal characteristics** - planar magnetic cores have a higher surface area to volume ratio than typical wirewound designs, which can help achieve better heat conduction, resulting in lower temperatures.
- **Precision dimensioning and repeatability** - planar windings are laid out as PCB traces and will therefore have very precisely defined dimensions that can be easily reproduced. Additionally, PCB layout software allows for precise placement and duplication of windings, allowing for multi-winding or multilayer structures to have very good symmetry. This is especially beneficial in the two-primary transformer used in the DSAB, as symmetric primaries can help to ensure the inverters are loaded equally.
- **Reduction in interconnect and other resistive losses** - the planar structure is already internal to the PCB, meaning connections to other passives or semiconductors can be implemented with short, low resistance paths, and on multiple layers. This can help decrease losses due to parasitic interconnect resistances in the converter. Additionally, traces can easily be customized to completely take up the core window width, which can help decrease dc resistance and increase current handling capabilities. Windings can also be connected in parallel to further increase the current handling of the windings.
- **Ease of winding interleaving** - since PCBs are naturally multilayer, it is very easy to precisely define which layers should correspond to which traces. Therefore, it makes it very easy to interleave primary and secondary windings in transformers in order to reduce high-frequency winding losses due to ac resistance. This can also reduce leakage inductance, which may or may not be beneficial depending on the converter topology.

- **Parasitic modeling** - because the trace dimensions, layer spacings, and material makeup of the copper and dielectric layers used in the PCB are very well defined, it is reasonably straightforward to create or use models to predict the parasitic resistance, inductance, and capacitance of windings. [23] provides a detailed description of one such planar magnetics modeling tool.

In particular, the magnetic component in the DSAB uses interleaved and paralleled windings to reduce dc and ac resistance losses, and achieve high-efficiency operation. Section 5.1.1 gives a summary of these loss mechanisms.

5.1.1 Winding Loss

Winding loss results from eddy currents in the windings of the magnetic component, and increases with frequency, hindering the designer's ability to miniaturize magnetic components while still maintaining high-efficiency operation. Skin effect and proximity effect are explored below, as well as methods to reduce the losses caused by them.

Skin Effect

Skin effect is the tendency of ac current flowing through a conductor to be concentrated along the surface of the conductor [24] [25]. This is due to eddy currents induced by the alternating magnetic field, which then produce a field in a direction to oppose the original field. The eddy currents will tend to cancel the original current in the center of the conductor, while adding to it at the edges of the conductor. The result is that more current flows along the surface of the conductor than in the center, which can be seen as an increase in ac resistance. This effect increases with the frequency of the ac current. The skin depth δ refers to the distance the majority of the current can penetrate into the conductor, measured from the surface. If the wire is not sized correctly for the frequency of the ac currents, this distance can be much smaller than the actual diameter of the wire.

The skin depth for a sinusoidal ac wave can be expressed as [25]:

$$\delta = \sqrt{\frac{2}{\omega \mu_0 \mu_r \sigma}} \tag{5.1}$$

where δ is the skin depth in m, ω is the frequency in radians, μ_0 is the permeability of free space, μ_r is the relative permeability of the conductor, and σ is the conductivity of the conductor. As can be seen in Eqn. (5.1), as frequency increases, the skin depth decreases, meaning that there is less effective area for the current to travel through.

In order to mitigate skin effect losses, small diameter wire (or thin foil) may be selected in traditional wire-wound magnetics so that the wire diameter is only slightly larger than the skin depth. However, this can increase dc losses if the winding must carry dc current, as $R_{dc} = \frac{\rho l}{A}$, where A is proportional to the wire diameter. To balance dc resistive and skin effect losses, one can use paralleled wires or litz wire, which consists of bundles of very small diameter wires twisted together in a special transposition pattern.

In planar PCB windings, however, windings are implemented with laminated copper sheets that can be designed with very large widths for low dc resistance and very small heights (on the order of mils) for low ac resistance.

Proximity Effect

Proximity effect is similar to skin depth, but deals with interactions between multiple conductors carrying ac current. Proximity effect is particularly pernicious as - under its influence - not only does a thick conductor not have lower ac resistance than a thin conductor, but it may actually have higher resistance. Proximity effect arises from eddy current losses in one conductor induced by currents in another nearby conductor, and becomes prominent with high-layer-count windings. Ac current in a nearby (second) conductor creates an alternating magnetic field, which induces circulating currents in the first conductor. This results in increased ac resistance. Depending on the winding configuration, proximity effect loss can strongly dominate skin effect loss.

Using thinner copper for a given frequency can lead to lower eddy currents, decreasing ac resistance to a limited extent. The high width-to-thickness ratio of planar windings is very beneficial here, as the trace width can be very large to lower dc resistance, while the trace height can be very small to minimize skin and proximity loss due to eddy currents. PCB stack-ups can be optimized by selecting a copper weight (usually measured in ounces) that satisfies the desired conductor height to skin depth ratio. A large amount of research has been done to derive analytical expressions for the optimum ratio between the conductor height and the skin depth in order to minimize winding losses overall [22]. [25] gives a method for selecting the optimal ratio of conductor height to skin depth for various excitation waveforms, rather than just sinusoids.

5.1.2 Interleaving of Windings

One method to reduce ac resistance in a transformer is to interleave the primary and secondary windings in the PCB winding stack-up. Fig. 5-1 shows (a) a non-interleaved transformer design, and (b) an interleaved transformer design, in both cases shown as planar PCB windings. The PCB stack is shown surrounded by a core oriented on its side, with a core material for which we have approximated $\mu \to \infty$. The core has a window width w and a core height h. The primary and secondary winding layers for this transformer are shown as copper sheets whose width take up the entire core window. The primary layers are shown in red and the secondary layers are shown in yellow. The direction of the current in the windings is represented as a ($\bullet$) for current out of the page or a ($\times$) for current into the page, and the primary and secondary windings have opposite net current directions. The magnetic field lines, labeled H, are shown in the spacings between winding layers, and underneath each winding configuration is a graph of the H field as a function of the distance x along the core height h. The primary windings are labeled p_i where i represents the i^{th} layer of the primary layers, and the secondary windings are similarly labeled as s_i where i represents the i^{th} layer of the secondary layers. The spacing between the layers is shown in green and represents the PCB dielectric layers.

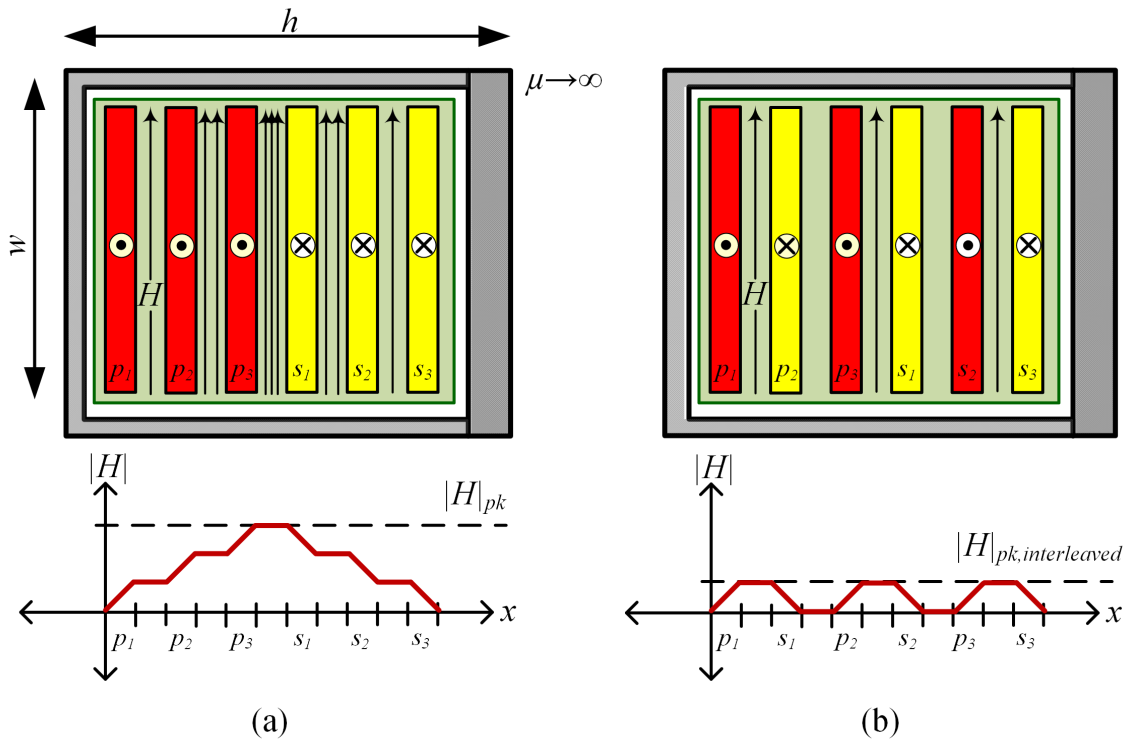


Figure 5-1: Effect of interleaving on peak H field in a transformer. (a) shows a non-interleaved design with a plot of the H field magnitude as a function of distance x along the core height h below it. The H field magnitude grows with each primary layer, and then reaches a peak value, $|H|_{pk}$, before decreasing with each secondary layer. (b) shows an interleaved design with alternating primary and secondary layers, where the H field returns to zero after every pair of primary and secondary layers. The interleaved design reaches a much lower peak value, $|H|_{pk,interleaved}$, reducing proximity effect loss.

The H field is assumed to be zero in the core, and the magnitude between PCB layers is found using Ampere's Law, so that $H = \frac{I_{enc}}{w}$ where I_{enc} is the enclosed current in the amperian loop. The density of H field lines between layers represents the magnitude of the H field. In the non-interleaved design in (a), as one travels across the winding window (in the direction x), the H field increases with each primary turn (shown as an increase in H field lines between layers). This is because the enclosed current has increased, as all primary layers have current flowing in the same direction. The H field then starts to decrease as each secondary layer is included in the amperian loop. If the magnitude of the H field is plotted versus position in the layer stack, the result is a stepped waveform with a peak value of H_{pk}.

In the interleaved design in (b), the H field increases across each primary winding, but as the current is integrated along the x direction, each secondary winding cancels the current of the previous primary winding, resulting in zero enclosed current and zero H field (assuming the current in each primary and secondary layer is exactly matched). As can be seen in the figure, after every primary and secondary winding pair, the H field is zero, shown here as no field lines. Additionally, if one plots the magnitude of the H field as function of position, the H field is trapezoidal and returns to zero after every secondary. The non-interleaved peak H field is greater than that of the interleaved design ($|H|_{pk} > |H|_{pk,interleaved}$), which results in higher eddy currents within the conductors. By interleaving, one can reduce the proximity loss in the transformer.

Interleaving is very easy to achieve in a planar PCB structure, which inherently consists of stacked layers that can be electrical connected to different ports internally. Vias can also allow for connections between multiple layers; however the resistance of the vias may be important at high frequency. Additionally, interleaving can lead to increased primary-to-secondary capacitance, which could be detrimental.

Interleaving can also decrease leakage inductance due to a decrease in the leakage fields around the transformer, which may or may not be desirable for a given converter topology. The leakage inductance of a transformer represents the fact that not all the magnetic flux follows the core path and that the flux linkage between windings is not perfect. Leakage energy can also be stored between windings, and is a function of the winding geometry, core geometry and number of turns [22]. For example, as illustrated by the magnetic energy storage in Fig. 5-1, a non-interleaved design may be expected to have higher leakage inductance than a fully interleaved design for similar spacings.

In some cases, such as phase-shifted dc-dc converters, leakage inductance is desirable as it can be used as the energy transfer element. If the transformer does not have enough leakage inductance, external inductance will have to be added, adding interconnect losses and additional magnetic losses. The DSAB converter does require some amount of leakage inductance to act as an energy transfer inductance between the

phase shifted input and output bridges. Additionally, the magnitude of the leakage inductance affects the current magnitude at the switching transitions, and therefore affects the converter's ability to achieve zero-voltage-switching (ZVS).

Through a special winding configuration detailed in Section 5.2.2, the transformer structure used in the DSAB is able to interleave the primary and secondary windings to reduce ac resistance, while still creating enough leakage inductance. This is due to the fact that the primary windings are wound around the outer legs of an E-I core so that some of the winding area is outside the core, resulting in high leakage fields in that area. Section 5.2.3 will give a more detailed description of the source of the leakage inductance.

5.1.3 Paralleled Windings

Another advantage of planar magnetic structures is the ease in implementing parallel windings to decrease dc resistance and increase current carrying capability. However, the currents do not necessarily split evenly over the PCB layers, and depending on the winding and core configuration, paralleled windings can have circulating currents, adding to winding loss [23] [26]. M2Spice, a tool developed in [23], generates a lumped model SPICE netlist from a customizable winding configuration and PCB layer stack, allowing one to visualize each layer's currents in the time domain. The model can also be included in the converter netlist to simulate the magnetic component's in-circuit behavior for a variety of operating points. While it was not used to model the DSAB transformer, the transformer did follow lessons learned from M2Spice models of previous phase-shifted dc-dc converters [26].

The design of the DSAB's magnetic component took advantage of the benefits of interleaving and paralleled windings to reduce ac and dc resistance and increase efficiency. The winding configuration and layer stack is detailed in Section 5.2.2.

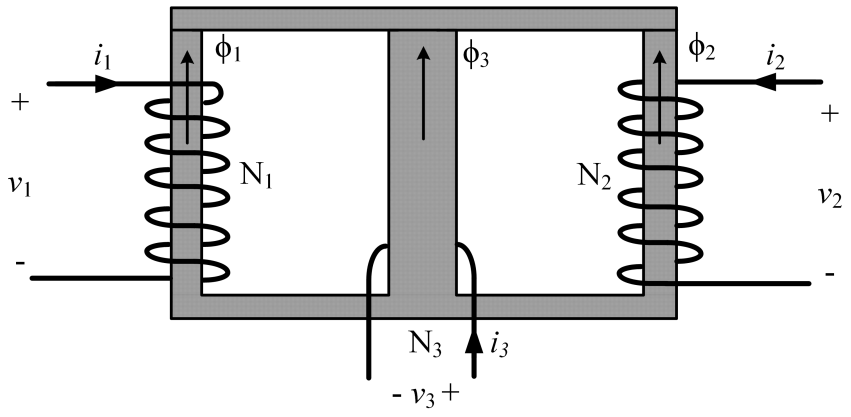


Figure 5-2: A winding diagram of the three-winding transformer on an E-I core. The primary windings are wound around the outer legs (windings 1 and 2), while the secondary is wound around the middle leg (winding 3).

5.2 Transformer Structure

The DSAB converter uses a three-winding transformer structure, with two primaries coupled to a single secondary. A planar magnetic structure with a single core was used to implement both the proposed transformer structure and the energy transfer leakage inductance. Each primary winding is wound around the outer leg of an E-I core, while the single secondary is wound around the middle leg. This winding configuration is shown in Fig. 5-2, where windings 1 and 2 represent the primary windings and winding 3 represents the secondary winding. The diagram shows the transformer with a turns ratio of $N_1 : N_2 : N_3$, in which $N_1 = N_2$.

5.2.1 Turns Ratio

The nominal operating point of the DSAB converter was chosen to satisfy the system requirements for a 380 V bus for a data center application. A 380 V nominal input voltage and a constant 12 V output was chosen, with a wide-input voltage range of 260 V to 410 V (the Electric Power Research Institute (EPRI) has defined a 380 Vdc Voltage Tolerance Curve requiring standard operation from 360 V to 410 V, and operation at 260 V for 1000 seconds [5]). As discussed in Chapter 3, the total primary voltage is $v_{p,tot} = \frac{V_{in,dc}}{2} = 190$ V at the nominal operating point of 380 V.

The secondary voltage is simply $v_s = V_{out,dc} = 12$ V.

As described in [2], the converter has the largest achievable ZVS range when the input and output voltages satisfy the constraint:

$$NV_s = V_p \tag{5.2}$$

where V_s is the secondary voltage, V_p is the primary voltage, and N is the primary-to-secondary turns ratio for a secondary of one turn. This condition represents a flat-topped leakage inductor current waveform, where the voltage across the inductor is exactly zero outside of the phase shift time period (i.e. when the input and output bridges' voltage is both high or both low). If the trapezoidal current waveform instead had sloped tops rather than flat tops, the current at the switch transitions would be decreased, making it harder for the converter to achieve ZVS [2].

Designing for this condition, the turns ratio was found to be:

$$N = \frac{v_{p,tot}}{v_s} = \frac{190\,V}{12\,V} = 15.833 \approx 16 \tag{5.3}$$

where 16 was chosen as the closest integer value. The primary-to-secondary turns ratio is then 16:1 (or an overall ratio of 16:16:1).

5.2.2 PCB Winding Stack-up

Fig. 5-3 shows hows the windings are arranged in each layer of the PCB for the DSAB magnetic component. An 8-layer stack-up was used to allow for interleaving and paralleled windings; the PCB stack-up dimensions are given in Appendix C.2.1. The primaries are shown in red and blue, and are each wound around an outer leg of an E-I core. The secondary winding is shown in yellow, and is wound around the center leg. The primary and secondary windings are interleaved inside the core window. However, the primary windings on the outside of the core are not interleaved, as there are no secondary windings in that area.

Each primary winding has a 16:1 turns ratio to the secondary. Because the primary

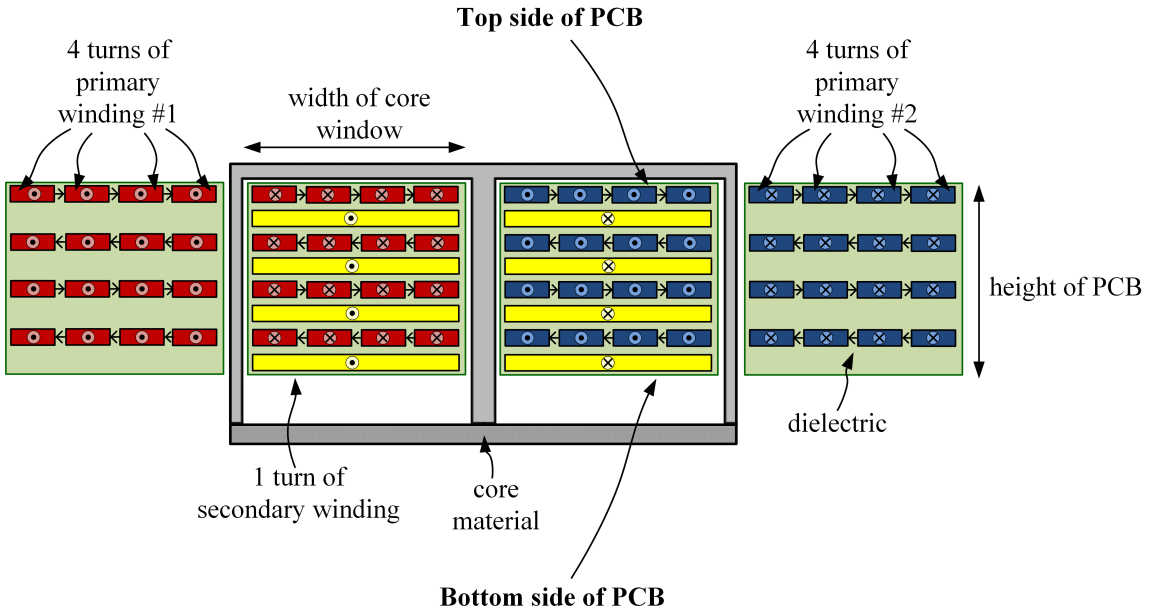


Figure 5-3: Cross section view of the magnetic core and PCB layer stack for the three-winding transformer. The primary windings are shown in red and blue and have four turns on each layer. The secondary winding only has one turn per layer, and is shown in yellow. The primary winding is the top layer of the PCB.

is the low-current, high-voltage side, primary winding traces do not need to be very wide. There are four layers for each primary winding that each contain four turns (shown in Fig. 5-3 as four different segments in blue or red) that together take up the entire window space, minus the dielectric spacing between each turn. The layers are connected in series, resulting in $4 \cdot 4 = 16$ total turns, as required.

The full load output current is approximately 25 A ($\frac{300\,W}{12\,V}$), so the traces must be designed to carry high current. As the secondary winding has only one turn, the trace can be made almost as wide as the core window. The four secondary layers are connected in parallel to further decrease dc resistance by increasing trace cross-sectional area, and to decrease ac resistance by allowing for interleaving with the primary windings. It is presumed that this approach leads to good current sharing among the layers of the secondary, but while excellent performance was achieved, this has not been validated, and is deemed a good topic for future study.

The PCB layout is shown in Fig. 5-4. Layers 1 (top side of PCB), 3, 5, and 7 are primary winding layers, and layers 2, 4, 6, and 8 (bottom side of PCB) are secondary

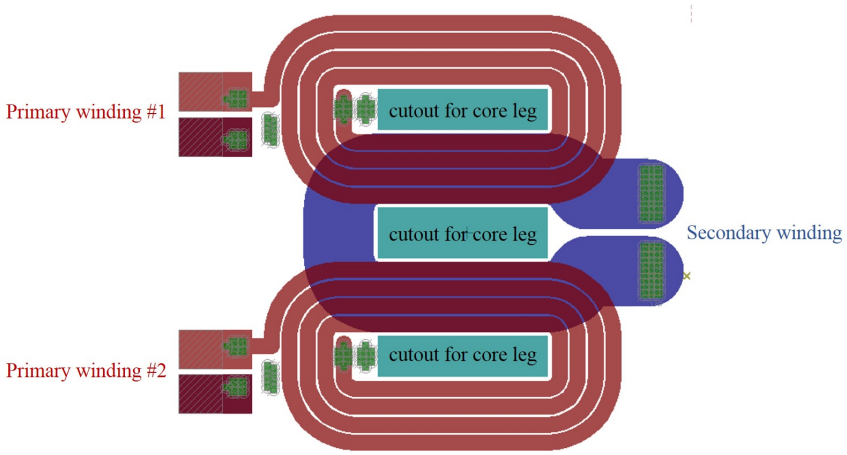


Figure 5-4: PCB layout of the magnetic component. The red traces are the two primary windings, and the blue trace is the secondary winding. Each primary winding is series-connected between layers 1, 3, 5, and 7, where layer 1 is the top side of the PCB. The secondary winding is parallel-connected across layers 2, 4, 6 and 8, where layer 8 is the bottom side of the PCB.

winding layers. PCB layout and Gerber files showing the trace layout are included in Appendix C. The two primaries are symmetric with respect to each other. The core lies directly on top of layer 1, so that the empty window space not taken up by the PCB is next to bottom layer, which is a secondary winding layer. There are three cutouts in the PCB so that the three core legs can fit through. Layers are connected through large arrays of vias to decrease resistance. The via configuration is presented in more detail in Appendix C.2.2.

4 oz copper was used in the six internal PCB layers (layers 2-7) to mitigate skin effects, decrease dc resistance, and increase current handling capability. While higher-ounce copper could be used to more closely match the optimal conductor height to skin depth ratio, weights above 4 oz are often not standard or are much more expensive. The top and bottom layers of the PCB (layers 1 and 8) used 2 oz copper, as 4 oz copper did not offer high enough resolution for the small pitch GaN devices used. Table 5.1 summarizes the winding configuration and copper ounce for each winding layer in the planar magnetic component.

Layer	Winding	Copper Oz.
1 (top)	P	2
2	S	4
3	P	4
4	S	4
5	P	4
6	S	4
7	P	4
8 (bottom)	S	2

Table 5.1: Summary of PCB layer stack. P stands for primary and S stands for secondary.

5.2.3 Leakage Inductance

Since the primary windings are wound around the outer legs, there is a substantial amount of winding that is not enclosed by the core. This leads to high primary-side leakage inductance due to leakage fields around the windings outside the core. Additionally, since the PCB height is approximately 90 mils while the core window height is approximately 213 mils, there is a significant portion of the core window that is empty. This is responsible for additional leakage fields. Fig. 5-5 shows the main flux paths for the transformer, while Fig. 5-6 (a) shows the corresponding magnetic circuit model, including the leakage paths shown in Fig. 5-5. ϕ_1 and ϕ_2 are the total fluxes in each outer core leg, and are shown in red. The flux $-\phi_3$ is the total flux in the center leg of the core, and is shown in orange; it is negative in Fig. 5-5 to match the notation used in Fig. 5-6 (a). The relationship between ϕ_1, ϕ_2, and ϕ_3 is $\phi_1 + \phi_2 = -\phi_3$. Due to the symmetry of the primary windings, $\phi_1 = \phi_2$. The secondary is shown connected to a load resistance, R_{load}. Due to the alternating magnetic field in the middle core leg, the secondary winding will generate current in the direction illustrated in Fig. 5-5 in order to oppose this field, as described by Lenz's law.

The leakage flux paths $\phi_{lk,1}$ and $\phi_{lk,2}$ on the primary windings represent the flux generated by the primary windings that does not link to the secondary, and are shown in blue. There are also similar leakage fields on the secondary winding that

do not couple to the primary windings, as well as leakage fields between layers of the PCB; these are left out for simplicity. Also note that this drawing is only shows a single 2-D slice of a 3-D field distribution - there are also leakage fields coming out of and into the page. Since the main sources of leakage for this transformer are the primary windings, the magnetic circuit model in Fig. 5-6 (a) only shows the primary-side leakage elements, modeling them as additional reluctances in parallel with the primary winding MMFs and outer core leg reluctances.

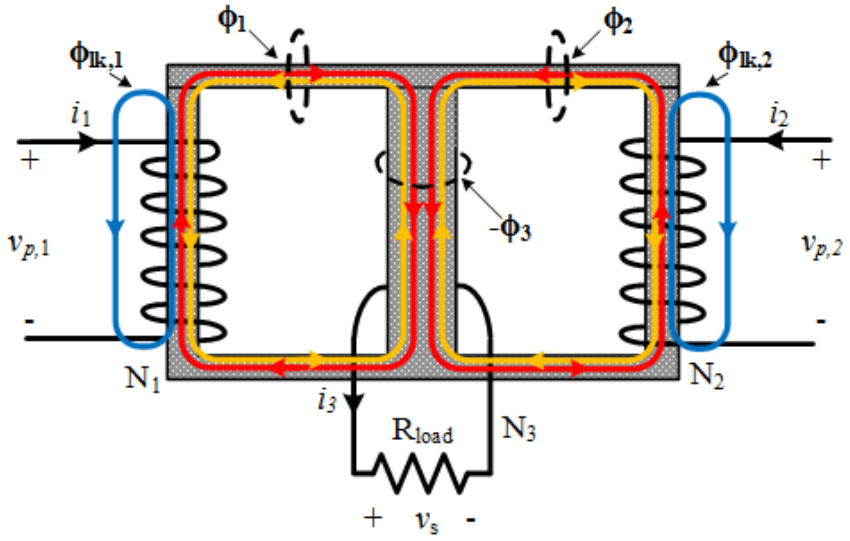
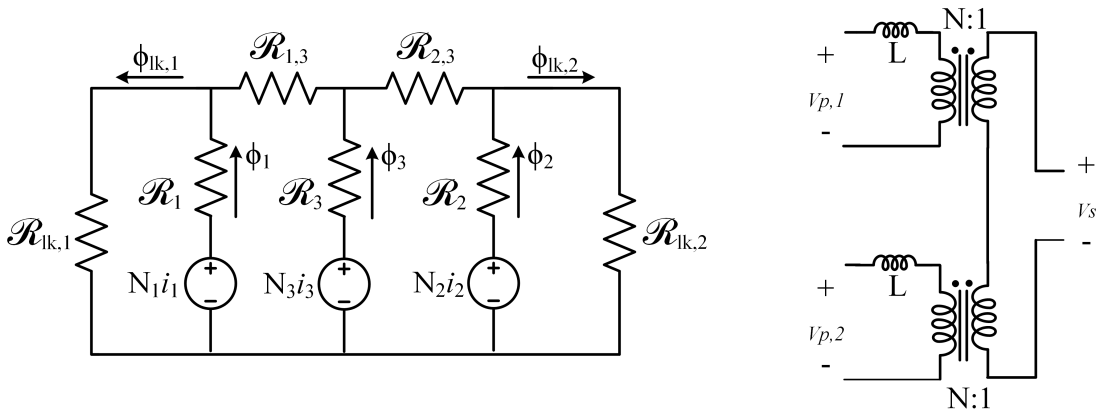


Figure 5-5: A diagram of the flux paths in the three-winding transformer. The fluxes in each outer leg that link the secondary, ϕ_1 and ϕ_2, are shown in red. The primary winding leakage fluxes, $\phi_{lk,1}$ and $\phi_{lk,2}$ are shown in blue. $-\phi_3$ is the flux through the center leg, and is negative to be consistent with the magnetic circuit model in Fig. 5-6 (a). The direction of the flux paths are shown by the arrows. Note that the fluxes are time-varying, so the direction of the arrows represents the relationships between the different fluxes at a given time, rather than a constant direction.

Fig. 5-6 (b) shows the corresponding simplified electrical circuit model. As discussed in Chapter 3, the total primary-referred leakage inductance is shown as two equal leakage inductances on each primary winding, with a value of L. The total primary-referred leakage inductance measured for this transformer was $2L = 32\mu$H as inferred by experiments with the converter. No extra discrete inductance was used in the DSAB converter prototypes presented in Chapter 7.

The value of the total leakage inductance was found by using the power charac-



(a) Magnetic Circuit Model (b) Electric Circuit Model

Figure 5-6: (a) A magnetic circuit model that includes the primary-side leakage paths, modeled as additional reluctances $\mathscr{R}_{lk,1}$ and $\mathscr{R}_{lk,2}$ in parallel with the main primary branches. $\mathscr{R}_{1,3}$ and $\mathscr{R}_{2,3}$ represent the reluctances of the horizontal core pieces between the outer legs and the center leg. (b) A corresponding electrical circuit model, showing the primary-referred leakage as two leakage inductors of value $\frac{L}{2}$ each, where L is the total primary-referred leakage inductance.

teristic of the DSAB to solve for L, given an operating frequency f_s, total primary voltage $v_{p,tot} = \frac{V_{in}}{4} + \frac{V_{in}}{4}$, secondary voltage $v_s = V_{out}$, output power P_{out}, and phase shift ϕ, as shown in Eqn. (5.4).

$$L_{tot} = 2L = \frac{(\frac{V_{in}}{4} + \frac{V_{in}}{4})V_{out}N}{2\pi f_s P_{out}}\phi(1 - \frac{\phi}{\pi}) \tag{5.4}$$

Initial testing was done at 400 kHz and 500 kHz with a dc system input voltage of 40 V - 120 V, and the average total leakage was found to be approximately 32 μH. This inductance value was then used to generate phase shifts for various operating points. As described in Section 5.3, the actual operating frequency was finalized at 175 kHz in order to achieve higher output power and efficiency for the given leakage inductance, as the effective leakage was higher than expected.

By configuring the windings in the manner described in 5.2.2, a single core magnetic component can create a two-primary, single-secondary transformer with sufficient leakage inductance on each primary. In this way, a single magnetic component can implement isolation, voltage transformation, power combining, and energy trans-

fer. Additionally, since the magnetic component is realized with a planar design, the core profile can be kept small, resulting in a compact magnetic structure with low loss.

5.2.4 Transformer Loss Analysis

Several transformer designs were analyzed in order to find a low-loss design to increase overall efficiency. The transformer losses consist of core loss and winding loss. An overview of these losses are given, followed by a description of the methodology used to estimate them for the DSAB magnetic structure. The following analysis as well as the MATLAB code used to calculate transformer loss are presented in more detail in [27].

Core Loss Calculations

Core loss in the transformer mainly consists of eddy current loss due to the core bulk material conductivity, hysteresis loss, or other "excess" losses that are not well-defined analytically. Due to the difficulty in deriving analytical expressions for core loss, the core loss for this transformer was estimated using the Steinmetz equation, repeated in a general form in Eqn. (5.5):

$$P_v = K f^{\alpha} B_{ac}^{\beta} \tag{5.5}$$

where P_v is the power loss density, f is the frequency of the sinusoidal excitation, and B_{ac} is the peak amplitude of the magnetic flux density. K, α, and β are provided by the core manufacturer and are calculated empirically using curve-fitting techniques. They are therefore only valid over certain frequency and B field ranges.

Eqn (5.6) gives a version of Eqn. (5.5) as presented by the core manufacturer EPCOS. The loss P_c represents the core loss in units of W / core set for a soft ferrite core, and is calculated as follows:

$$P_c = K_F \, V_e \, p_{v,sin} \left(\frac{f}{f_b}\right)^{\alpha} \left(\frac{B}{B_m}\right)^{\beta} \tag{5.6}$$

where f is the actual operating frequency in kHz; B is the actual operating peak sinusoidal flux density at an operating temperature of T_{op} in °C; $p_{v,sin}$ is the loss density in kW/m^3 at temperature T_{op}, base frequency f_b in kHz and base peak sinusoidal flux density B_m in mT; V_e is the magnetic volume of the core in mm^3; α is the Steinmetz exponent for frequency; β is the Steinmetz exponent for flux density for the given ferrite material at T_{op}; and K_F is a multiplication factor for the core shape used, as $p_{v,sin}$ is measured on standard ring cores [28].

Although the actual flux density in the DSAB is triangular rather than sinusoidal, this equation provides a good reference point to compare different transformer design options. [27] gives the exact values of the Steinmetz parameters used in the core loss calculations for the DSAB converter.

Winding Resistance Calculations

An approximation of the winding loss given the PCB trace dimensions and core geometry is calculated in the MATLAB script included in [27]. The calculation takes into account skin depth limitations, but does not account for proximity losses. Fig. 5-7 shows a simplified view of a standard E core, from the top and side views. The available area for PCB traces is shown by the blue curve, and the average length of the trace is shown by the dashed blue line labeled l. The trace width is the entire window width of the core, and can be defined by an outer diameter OD and an inner diameter ID. The width of the core itself is dimensioned as W in the diagram.

Using these dimensions, the resistance of a single turn with length l is given by:

$$R_{wind} = \frac{\rho l}{A} = \frac{\rho(2ID + 2W + \frac{2\pi(OD-ID)}{4})}{\frac{\delta(OD-ID)}{2}} \tag{5.7}$$

where δ is the skin depth, or the distance the ac current can penetrate into the copper layer. The skin depth is calculated as a function of the frequency, which is input as a parameter to the MATLAB script.

The primary and secondary winding resistances can be calculated in terms of the single-turn winding resistance, R_{wind}. The secondary winding in the transformer is

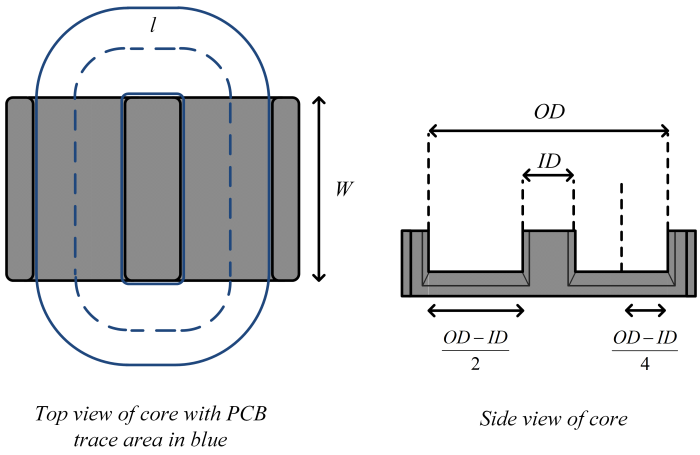


Figure 5-7: Top and side views of the E-core used for the three-winding transformer. The trace area is shown in blue, which represents the area that can be filled with planar windings. The outer diameter OD and inner diameter ID of the core window are dimensioned. $\frac{OD-ID}{2}$ represents the width of one of the core windows, and $\frac{OD-ID}{4}$ represents the radius of the arc defined by the corners of the blue PCB trace area.

split over 4 layers, so a simple approximation is that the secondary winding resistance, R_{sec}, is a fourth of the single-turn R_{wind}:

$$R_{sec} = \frac{R_{wind}}{4} \tag{5.8}$$

The primary winding in the transformer is also split over 4 layers, but these are connected in series, rather than in parallel. There are 16 total turns, so the effective length of the winding is 16 times longer than that of the secondary. Also, since each layer is split into 4 turns, the width is also a fourth of that of the single turn. The primary resistance, R_{pri}, can then be expressed as:

$$R_{pri} = 16 \cdot 4 \cdot R_{wind} = 16 \cdot 4 \cdot (4R_{sec}) = 16^2 R_{sec} \tag{5.9}$$

The winding loss on the secondary is $P_{sec} = I_{sec}^2 R_{sec} = I_{sec}^2 \frac{R_{wind}}{4}$ and the winding loss on the primary is $P_{pri} = I_{pri}^2 R_{pri} = \frac{I_{sec}^2}{16^2} \cdot 16^2 R_{sec} = I_{sec}^2 \frac{R_{wind}}{4}$. Because there are two primaries and one secondary winding, the total winding loss is:

$$P_{wind} = \frac{3}{4} I_{sec}^2 R_{wind} \tag{5.10}$$

Results of Transformer Loss Calculations

More detailed results from the transformer loss script can be found in [27], but a summary of the script's function is presented here. As described in [27], various core materials were investigated to find the optimal material with the lowest core loss for a given peak magnetic flux density. Transformer losses were also calculated for a wide array of core sizes and operating frequencies, for a set operating point. The E core geometry was chosen due to the three-winding transformer configuration. The most optimal design was found to be an EPCOS EILP43 core, using the N49 core material.

Core geometry data, including core area A_e, core volume V_c, the outer diameter of the core window OD, and the inner diameter of the core window ID, was gathered from EPCOS manufacturer data. Steinmetz parameters were found using the EPCOS MDT design tool [28].

The MATLAB script takes a range of frequencies, and at each frequency calculates the peak magnetic flux density B_{pk} for each core type for the estimated operating parameters. If B_{pk} exceeds the maximum allowable magnetic flux density B_{max}, that combination of frequency and core type is discarded, and the script will continue on to the next core until it finds one that satisfies the B field limit. Then, it will calculate the current density in the high-current secondary winding given the core geometry and PCB trace dimensions, as well as the skin depth at the corresponding frequency. If the current density J_{wire} is greater than the maximum allowable current density J_{wire}, that frequency and core type combination is again discarded.

If a core is within both the B_{pk} and J_{wire} limits, the core loss and winding losses are then calculated. The core loss P_{core} is calculated using the previously calculated B_{pk}, the corresponding Steinmetz parameters, and the core volume V_c.

Winding loss, P_{wind}, is calculated using the resistance of a single turn winding R_{wind}, which is a function of the skin depth δ and the core dimensions. The winding loss calculation includes dc resistance and ac resistance due to skin effect, but does not take proximity effect into account.

The winding resistance calculated in the script is then used to calculate the pri-

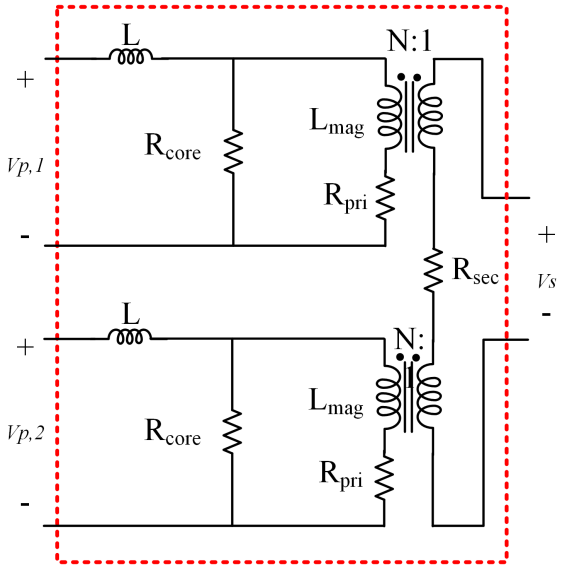


Figure 5-8: Transformer model used in LTSPICE simulations of the DSAB converter. R_{core} is used to model the core loss, while R_{pri} and R_{sec} represent the winding losses on the primary and secondary windings. For the DSAB operating at 380 V input, $R_{core} = 2650\ \Omega$, $R_{pri} = 88.5\ \text{m}\Omega$, and $R_{sec} = 0.346\ \text{m}\Omega$. L is each primary's leakage inductance (16 μH), and L_{mag} is each primary's magnetizing inductance (1.5 mH).

mary and secondary windings' parasitic resistances R_{pri} and R_{sec}, following the expressions given in Sec 5.2.4. This allows the winding loss to be included in LTSPICE simulations of the DSAB converter. The core loss can also be included in the SPICE simulation by adding a parallel resistance across each winding's magnetizing inductance, with a value R_{core}, where R_{core} is given by:

$$R_{core} = \frac{v_p^2}{P_{core}} \tag{5.11}$$

The transformer is modeled in LTSPICE using the electrical circuit model shown in Fig. 5-8, which includes winding loss and core loss in the form of the parasitic resistances R_{pri}, R_{sec} and R_{core}.

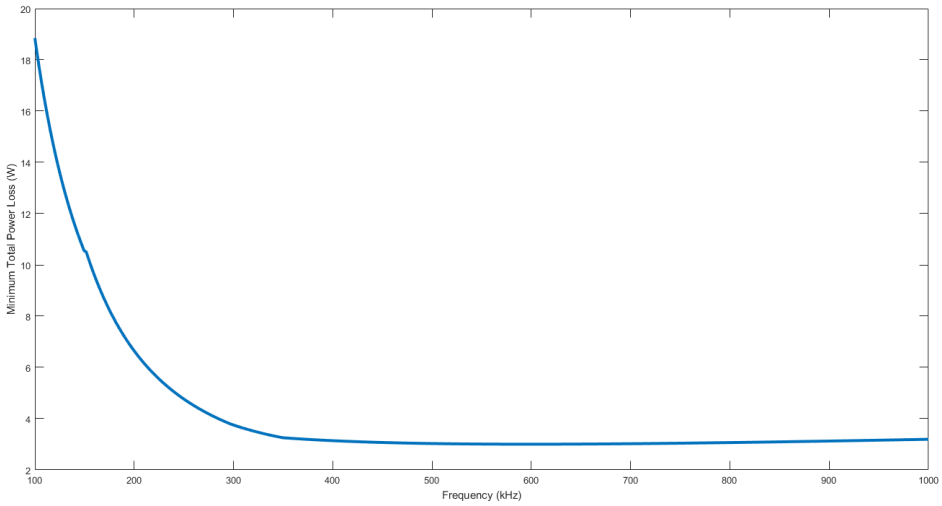


Figure 5-9: Plot of the minimum total power loss for the DSAB transformer over all valid core designs. The loss, given in W, decreases rapidly from 100 kHz to 300 kHz, and then flattens out around 3 W from 350 kHz to 1 MHz.

5.3 Selection of Operating Frequency and Output Power

A plot of the minimum total transformer loss vs. frequency generated from the transformer loss MATLAB script and taken from [27] is presented in Fig. 5-9. The total loss decreases as the frequency increases from 100 kHz. However, after 400 kHz, the total loss remains relatively constant at ∼3 W, until it starts to increase again at 1 MHz. An initial design of the converter was therefore done targeting the 500 kHz range.

However, the final operating frequency and full-load power was changed after simulation and initial experimental testing at several converter operating conditions. The leakage inductance of the transformer was higher than expected at 32 μH, which required the operating frequency to be decreased from the original 500 kHz range. Additionally, looking at the DSAB power characteristic (repeated in Eqn (5.12)), one can see that for a given total inductance $2L$, operating frequency f_s, and input voltage V_{in}, the maximum power P_{out} occurs when the expression $\phi(1-\frac{\phi}{\pi})$ is maximized. This corresponds to a phase shift of $\phi = \frac{\pi}{2}$ radians or 90°. This limits the achievable P_{out}

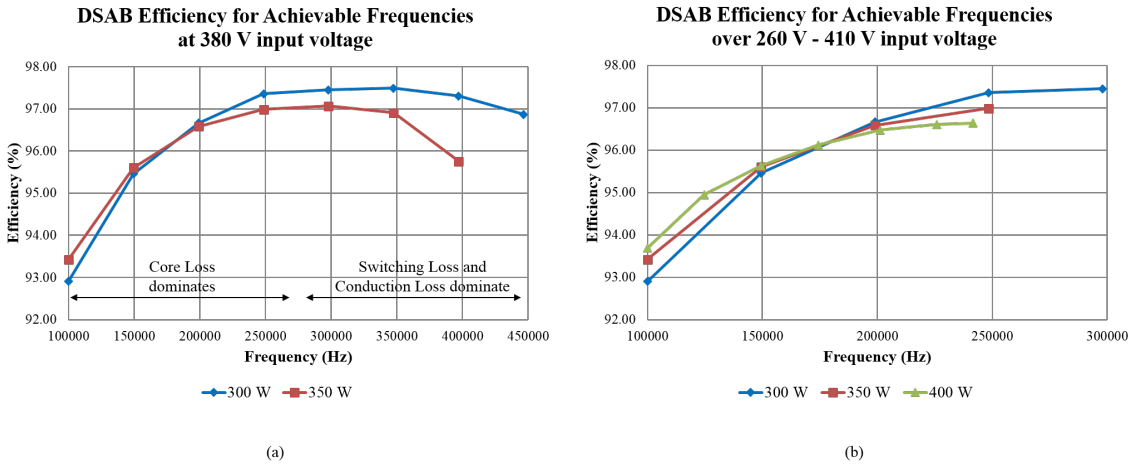


Figure 5-10: (a) A graph of simulated converter efficiency over a range of frequencies for which ϕ is realizable at an input voltage of 380 V and the given power rating. Core loss decreases with frequency while switching and conduction losses increase, causing a peak in the efficiency curve. (b) A graph of simulated converter efficiency over a range of frequencies for which ϕ is realizable over the entire input voltage range of 260 V to 410 V. As can be seen in both graphs, as the power rating increases, the range of possible frequencies decreases.

for a given frequency (e.g. at 500 kHz, 300 W output power was not achievable for the given leakage inductance).

$$P_{out} = \frac{(\frac{V_{in}}{4} + \frac{V_{in}}{4})V_{out}N}{2\pi f_s 2L}\phi(1 - \frac{\phi}{\pi}) \tag{5.12}$$

A MATLAB script (included in Appendix A) was used to calculate the necessary phase shift ϕ for a given frequency, output power rating, and leakage inductance, both at the nominal operating point of 380 V input and 12 V output, and over selected input voltages in the range of 260 V to 410 V. The script checks if ϕ is realizable for the nominal operating point, as the value calculated for ϕ will start to become complex if the desired output power is higher than the output power delivered at the maximum phase shift of $\frac{\pi}{2}$ radians (90°). The script also displays the maximum possible frequency for each output power level, as well as the phase shift at that frequency for 380 V input and the phase shift at that frequency for 260 V input, which corresponds to the maximum phase shift for a given combination of L, f_s, and P_{out}.

Using the phase shift data generated from the script, the DSAB converter operation was simulated in LTSPICE. The core resistances and winding resistances for each frequency point were included in the model for the transformer structure. The efficiency at the full power rating and 380 V input was measured for each simulation. Plots of the converter efficiency for different power levels over a range of frequencies are shown in 5-10. Fig. 5-10 (a) shows efficiency curves at 300 W and 350 W over a frequency range of 100 kHz to 450 kHz. Although the MATLAB script included frequencies up to 500 kHz, the 350 W converter was not able to achieve the desired power above 446500 kHz at an input voltage of 380 V, and the 300 W converter was not able to achieve the desired power above 496000 kHz. As can be seen in the figure, the efficiency increases as the frequency increases from 100 kHz, reaches a peak around 300 kHz, and then starts to decrease again. As the core loss decreases with increasing frequency, while the winding loss increases with increasing frequency, the peak of the efficiency curve is then the point where core loss becomes less dominant than conduction loss (including winding loss in the transformer) and switching loss. As frequency increases, ϕ also increases for a given P_{out}, and conduction losses then increase due to higher RMS currents caused by the leakage inductor current's longer ramp time.

Since the DSAB converter was designed for a wide input voltage range of 260 V to 410 V, the phase shift also had to be achievable for all voltages in this range. This further restricts the maximum possible frequency. The maximum frequency for each power level given the full input voltage range of 260 V to 410 V is shown in Table 5.2, along with the nominal phase shift (at 380 V and f_{max}) and the maximum phase shift (at 260 V and f_{max}). Fig. 5-10 (b) shows a graph of the efficiencies for 300 W, 350 W, and 400 W over the frequencies for which ϕ is realizable for all input voltages. Using this graph, an initial operating point of 300 W and 300 kHz was chosen, as it had the highest efficiency. After additional bench testing and calibration, 175 kHz was found to be the optimal operating frequency for maximizing efficiency.

For the selected operating point of 300 W and 175 kHz, the phase shifts at each input voltage are given in Table 5.3. The phase shifts correspond to between 4.7%

P_{out} (W)	f_{max} (Hz)	ϕ_{nom} at f_{max} (deg)	ϕ_{max} at f_{max} (deg)
300	325000	19.7	45.0
350	277750	19.6	42.6
400	241750	19.5	41.0

Table 5.2: Summary of achievable frequencies at full power ratings of 300 W, 350 W, and 400 W, along with the corresponding nominal phase shift ϕ_{nom} (at 380 V) and maximum phase shift ϕ_{max} (at 260 V). Phase shifts are given in degrees.

and 8% of the total switching period, which is reasonable balance between too high of phase shifts, which result in a high peak value for the leakage inductor current, and too low of phase shifts, where the the deadtime values become non-negligible in calculating correct phase shifts for a given output power.

V_{input} (V)	ϕ (deg)
260	14.4
290	12.6
320	11.3
350	10.1
380	9.2
410	8.5

Table 5.3: List of phase shifts in degrees for input voltages ranging from 260 V to 410 V at 300 W and 175 kHz.

This chapter has described the design and analysis of the three-winding transformer with built-in leakage inductance used in the DSAB converter. This single magnetic component was implemented with planar PCB windings on an EPCOS EILP43-N49 E-I core. The transformer has a primary-to-secondary turns ratio of 16:1 for each primary, and the windings are implemented using an 8-layer stack-up with 2 oz. copper external layers and 4 oz. copper internal layers. The total primary-referred leakage inductance is 32 μH. After analyzing transformer loss, an operating point of 300 W and 175 kHz was selected for the DSAB converter.

Chapter 6

Simulation Results

Simulations of the Double Stacked Active-Bridge (DSAB) topology, a Single-Stacked DAB topology, and a Full-Bridge DAB topology were performed using LTSPICE software. The three topologies were all simulated with GaN and Si inverter devices, and the DSAB was simulated in both the full-power and low-power modes. The converters were simulated over a wide load range, where the output power was controlled by varying the phase shift between the input and output bridges.

Table 6.1 gives a summary of the devices and topologies simulated. An (*) indicates that the device or topology was only simulated, with no prototype built. For all simulations, the rectifier was simulated with 30 V GaN EPC2023 devices.

Topology	GaN	Si	Superjunction
DSAB	EPC2012C	FQD10N20L	N/A
Single-Stacked DAB	EPC2025*	N/A	IPD50R280CE
Full-Bridge DAB	GS66516T*	N/A	IPD50R280CE*

Table 6.1: Table of the devices selected for simulation in the DSAB, Single-Stacked DAB, and Full-Bridge DAB topologies. An (*) indicates that the device was only simulated, not experimentally tested.

The following simulations were performed at the operating point of 300 W and 175 kHz:

1. Simulations of each of the following topologies: 1) DSAB, 2) Single-Stacked DAB, and 3) Full-Bridge DAB. The converter efficiency and ZVS behavior was

characterized over a wide load range by sweeping the phase shift ϕ.

2. Simulations of the same converter topology with different inverter devices (i.e. GaN or Si).

3. Simulations of the DSAB converter for operating under 1) the normal full-power mode, and 2) a low-power mode for operation below 100 W, designed to decrease switching and core loss.

4. Simulations of the DSAB converter with one to three paralleled rectifier devices, to explore the trade-off between decreased path resistance and increased switch node capacitance due to paralleled devices.

5. Simulations of the DSAB converter over a wide-input voltage range of 260 V to 410 V, at 300 W.

(1) - (4) were performed with the nominal system input voltage of 380 V. For all simulations, a single EPC2023 device was used for each rectifier switch, except where explicitly stated that paralleled devices were used, as in Section 6.2.3. Additional simulations performed at the original target design of 500 kHz and 400 W are included in [27].

6.1 LTSPICE Models

This section gives an overview of the methodologies used to model the switch devices and the magnetic structures for each topology. LTSPICE netlists and schematics are included in Appendix B.

6.1.1 Device Models

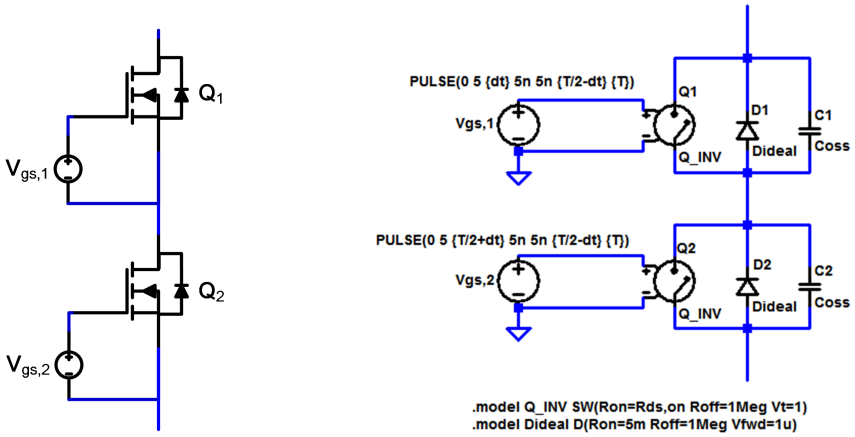
The inverter and rectifier switches were modeled as a voltage-controlled switch with an on-resistance equal to the $R_{ds,on}$ of the device, in parallel with a capacitance equal to the C_{oss} of the device (calculated by the method given in Chapter 4). A diode was also placed in parallel to mimic the parasitic diode of the device (while eGaN

FETs do not have a body diode in the same way as standard Si FETs, there is still effectively an internal parasitic diode [20]). The values of $R_{ds,on}$ and C_{oss} for each device used in the inverter and rectifier bridges are given in Table 6.2.

	Device	$R_{ds,on}$	C_{oss}
Inverter	EPC2012C	105 mΩ	102.5 pF
	FQD10N20L	525 mΩ	116 pF
	EPC2025	141.75 mΩ	108.125 pF
	IPD50R280CE	450 mΩ	72.5 pF
	GS66516T	46.875 mΩ	134 pF
Rectifier	EPC2023	1.5 mΩ	1854 pF

Table 6.2: Table of $R_{ds,on}$ and C_{oss} values used in LTSPICE simulations to model each switch device. $R_{ds,on}$ and C_{oss} were calculated in the same manner as described in Chapter 4.

It is important to note, however, that C_{oss} in a real device depends non-linearly on the drain-to-source voltage of the switch. This effect was not included in the device models, which instead used a constant value for C_{oss}, calculated using the methodology in Chapter 3. This leads to some discrepancy between the simulated efficiency and the experimental efficiency at low power levels.



(a) (b)

Figure 6-1: (a) A schematic diagram of switches Q_1 and Q_2 arranged in a half-bridge and (b) an LTSPICE schematic showing the switches modeled as a voltage-controlled switch with an on-resistance of $R_{ds,on}$ in parallel with a diode and capacitor with a capacitance equal to the C_{oss} of the device, as calculated in Chapter 4.

Fig. 6-1 (a) shows a circuit diagram of two devices, Q_1 and Q_2, configured in a half-bridge. They are each driven by a gate-to-source voltage, V_{gs}. The corresponding LTSPICE schematic is shown in (b). Each device is modeled as an ideal switch Q (with model Q_INV) in parallel with a diode D (with model Dideal) and a capacitor C. Q_1 and Q_2 are driven with two complementary square-waves with an off-voltage of 0 V and an on-voltage of 5 V, with a period T, deadtime dt, rise and fall times of 5 ns, and an on-time of $\frac{T}{2} - dt$. The deadtime insures that both devices are never on at the same time, preventing shoot through.

6.1.2 Transformer

The LTSPICE model for the magnetic structure of each topology consists of an ideal transformer, with turns ratio N:1 (2N:1 for the full-bridge DAB topology), magnetizing inductance L_m, leakage inductance L_{lk}, and parasitic resistances R_{core}, R_{pri}, and R_{sec}, representing core loss and winding loss. As described in Chapter 5, R_{core}, R_{pri} and R_{sec} were calculated at the nominal system input voltage of 380 V.

Double-Stacked Active Bridge

Fig. 6-2 shows the LTSPICE circuit model used to simulate the magnetic component in the DSAB converter. The structure is modeled as two ideal transformers with the secondary windings connected in series. Each primary winding is fed by one of the stacked full-bridge inverters in the DSAB. The coupling statements "K1 L1 L2 1" and "K2 L3 L4 1" each couple the corresponding primary and secondary windings. The coupling factor is 1, representing perfect coupling (and no leakage inductance). The leakage inductance of the transformer is instead modeled externally, and is split across both primary windings, so that $L_{lk1} = L_{lk2} = 16$ μH, where the total primary-referred leakage is 32 μH. This transformer model is simplified as compared to a full cantilever model [15], but this simplification is merited by the symmetry through which the transformer is driven. The turns ratio of each primary is set by the ratio

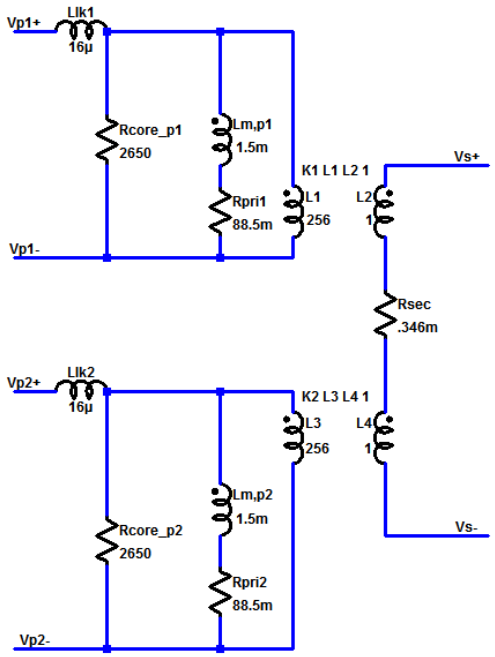


Figure 6-2: The LTSPICE model used for the magnetic structure in the DSAB, with leakage inductances $L_{lk1} = L_{lk2} = 16$ μH, magnetizing inductances $L_{m,p1} = L_{m,p2} = 1.5$ mH, core resistances $R_{core,p1} = R_{core,p2} = 2650$ Ω, primary winding resistances $R_{pri1} = R_{pri2} = 88.5$ mΩ, and secondary winding resistance $R_{sec} = 0.346$ mΩ. Each primary has a turns ratio of 16:1 with respect to the secondary.

of L1 and L2, as given by:

$$L_1 : L_2 = N_1^2 : N_2^2 = 16^2 : 1^2 = 256 : 1 \tag{6.1}$$

The ratio of the inductances $L_1 : L_2$ and $L_3 : L_4$ are set as the exact integer ratios (i.e. $L_1 = L_3 = 256$ and $L_2 = L_4 = 1$), while $L_{m,p1}$ and $L_{m,p2}$ are used to represent the actual magnetizing inductance expected from the given core material and number of primary winding turns. Because L_1 and L_3 are in parallel with $L_{m,p1}$ and $L_{m,p2}$ and are several orders of magnitude larger, they should not have a significant impact on the simulation results. $L_{m,p1}$ and $L_{m,p2}$ were calculated according to the following equation:

$$L_{m,p1} = L_{m,p2} = A_L N^2 = 5900 \, \frac{nH}{turn^2} \cdot (16 \, turns)^2 \approx 1.5 \, mH \tag{6.2}$$

The primary-side magnetizing inductances $L_{m,p1}$ and $L_{m,p2}$ are modeled in series with the parasitic winding resistances R_{pri1} and R_{pri2}. The two secondary windings are modeled with a single parasitic series resistance R_{sec}, as there is only one secondary turn. For the DSAB, $R_{pri1} = R_{pri2} = 88.5$ mΩ and $R_{sec} = 0.346$ mΩ. R_{core} was calculated using the methodology in Chapter 5, and was found to be 2650 Ω for each primary winding in the DSAB, at a system input voltage of 380 V.

Single-Stacked DAB

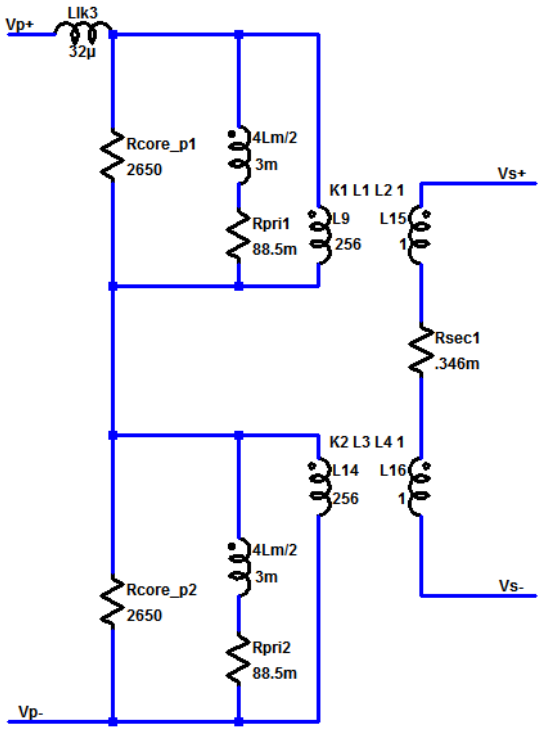


Figure 6-3: The LTSPICE model used for the magnetic structure in the Single-Stacked DAB, complete with a single leakage inductance $L_{lk} = 32$ μH, magnetizing inductances $\frac{4L_m}{2} = 3$ mH, core resistances $R_{core,p1} = R_{core,p2} = 2650$ Ω, primary winding resistances $R_{pri1} = R_{pri2} = 88.5$ mΩ, and secondary winding resistance $R_{sec} = 0.346$ mΩ. Each primary has a turns ratio of 16:1 with respect to the secondary. The primaries are connected in series to form a single effective primary winding.

Fig. 6-3 shows the LTSPICE circuit model used to simulate the magnetic component in the Single-Stacked converter. The secondary windings of the ideal transformers remain connected in series, and the turns ratio between each primary and

secondary pair also remains constant, as do the winding resistances $R_{pri1} = R_{pri2}$ and R_{sec}. However, the two primary windings are now connected in series to form a single effective primary winding. Therefore, the total number of primary turns is 32, so the total magnetizing inductance is now:

$$L_{m,p1} = L_{m,p2} = A_L N^2 = 5900 \frac{nH}{turn^2} \cdot (32\,turns)^2 \approx 6\,mH \tag{6.3}$$

This magnetizing inductance is modeled as being split between each primary, so that each magnetizing inductance equals $\frac{4L_m}{2} = 3$ mH, where $L_m = L_{m,p1} = L_{m,p2}$ from the DSAB. The leakage inductance is modeled as a single leakage inductor with a value of 32 μH.

Full-Bridge DAB

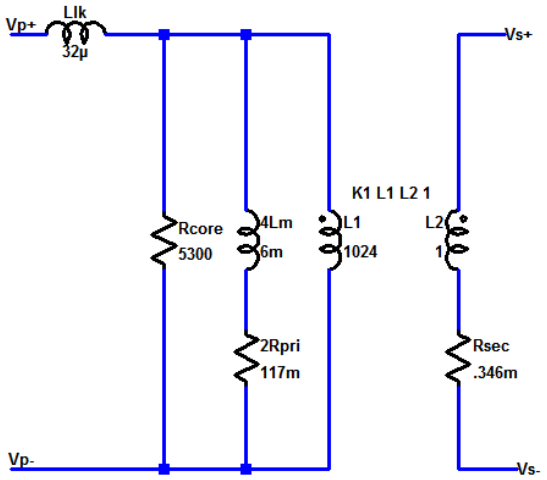


Figure 6-4: The LTSPICE model used for the magnetic structure in the Full-Bridge DAB, complete with a single leakage inductance $L_{lk} = 32$ μH, a single magnetizing inductance $4L_m = 6$ mH, a single core resistance $R_{core} = 5300$ Ω, total primary winding resistance $2R_{pri} = 117$ mΩ, where $R_{pri} = R_{pri1} = R_{pri2}$ from the DSAB, and a secondary winding resistance $R_{sec} = 0.346$ mΩ. The primary has a turns ratio of 32:1 with respect to the secondary.

Fig. 6-4 shows the LTSPICE circuit model used to simulate the magnetic component in the Full-Bridge converter. The transformer consists of a single primary coupled to a single secondary, with a total leakage inductance of 32 μH. Because the

total primary voltage is double that of both the DSAB (where $v_{p,tot} = V_{p1} + V_{p2}$=190 V) and the Single-Stacked DAB (where $v_{p,tot}$ = 190 V), the primary-to-secondary turns ratio must be increased to 32:1. This requires $L_1 : L_2 = 32^2 : 1 = 1024$:1. The total magnetizing inductance is therefore $4L_m = 6$ mH again, but is now modeled as a single inductor in parallel with the primary winding. The total series primary winding resistance is the same as in the other converters, but is now modeled as a single resistor of value $2R_{pri}$. The total series secondary winding resistance stays the same because there is still only one secondary winding. The core resistance R_{core}, however, is doubled because the primary voltage has doubled. This can be seen in Eqns. (6.4) and (6.5), which give expressions for core loss in the DSAB and Full-Bridge converters:

$$P_{core,DSAB} = K\left(\left(\frac{B_{pk}}{C}\right)^y + \left(\frac{B_{pk}}{C}\right)^y\right)\left(\frac{V_c}{2}\right) = K\left(\frac{B_{pk}}{C}\right)^y V_c \tag{6.4}$$

$$P_{core,FB-DAB} = 2K\left(\frac{B_{pk}}{C}\right)^y \frac{V_c}{2} = K\left(\frac{B_{pk}}{C}\right)^y V_c \tag{6.5}$$

C and K are lumped constants representing the Steinmetz parameters. Eqns. (6.5) and (6.5) assume that the same E-I core is being used as in the DSAB, except that the primary and secondary winding are both wound around the center leg for the Full-Bridge topology, and that the volume of the center leg is twice that of the outer legs. B_{pk} is the same for the DSAB and the Full-Bridge DAB even though the total primary voltage is doubled in the Full-Bridge DAB, because the turns ratio is also doubled.

6.2 Simulations

Three different topologies were simulated, using GaN FETs, vertical Si power MOSFETs, and Si Superjunction MOSFETs in the inverter. For all topologies, a single GaN EPC2023 device was used for each rectifier switch (unless explicitly stated to be paralleled, as in Section 6.2.3). The topology and device combinations are as follows:

1. The proposed Double Stacked-Active Bridge (DSAB), with 200 V GaN EPC2012C inverter devices and 200 V Si F1D10N20L inverter devices, labeled in graphs as "DSAB".

2. A dual-active-bridge using a single stacked full-bridge as the input bridge, with 300 V GaN EPC2025 inverter devices and 550 V Si Superjunction IPD50R280CE inverter devices. It is labeled in graphs as "Single-Stacked DAB".

3. A dual-active-bridge using a non-stacked full-bridge as the input bridge, with 650 V GaN GS66516T inverter devices and 550 V Si Superjunction IPD50R280CE inverter devices, labeled in graphs as "Full-Bridge DAB".

Efficiency values over a wide-load range were calculated by sweeping the phase shift for each converter and device combination, and using the LTSPICE .MEAS function to measure the input and output voltage and current.

Under ZVS, the switch voltage transitions sinusoidally from zero to the blocking voltage of the switch or vice versa, so the maximum deadtime is equal to a quarter of the sinusoid period, T_{ZVS}. The maximum deadtime can then be expressed in seconds:

$$dt_{max} = \frac{T_{ZVS}}{4} = \frac{2\pi\sqrt{C_{oss}L_{lk}}}{4} = \frac{\pi}{2}\sqrt{C_{oss}L_{lk}} \tag{6.6}$$

where the period of the sinusoid can be related to the inductance and capacitance that are resonanting together. T_{ZVS} can be expressed as $2\pi\sqrt{LC}$, where L is the branch leakage inductance (equal to half the total primary-referred leakage for the DSAB and the total primary-referred leakage for the Single-Stacked DAB and Full-Bridge DAB) and C is equal to the C_{oss} of the inverter device.

A single deadtime was used over the entire load range for each converter (though the inverter and rectifier deadtimes were selected separately for the DSAB and Single-Stacked simulations), to simplify the simulation process. This deadtime value was chosen so as to allow for ZVS over as wide a load range as possible. For the full-bridge topologies the deadtime was set to the maximum possible value, but even then the inverter switches were not capable of achieving full ZVS, as will be shown in

Section 6.2.1.

Note that too large of deadtimes can causes extra losses due the device drain-to-source voltage starting to resonantly ring down before the end of the switching transition, causing partial hard-switching of the device. In addition, there can also be losses due to body diode conduction in the device before it is turned on by its gate signal. More detailed fine-tuning of deadtimes can be performed (both in simulation and experimental testing) to select the optimal deadtime for the operating conditions.

Table 6.3 gives the maximum deadtimes for the inverter switches for each device. Actual inverter deadtimes dt_{inv} and rectifier deadtimes dt_{rect} used in simulation are given in Table 6.4 for each topology.

Device	dt_{max} (ns)
EPC2012C	64
FQD10N20L	68
EPC2025	92
IPD50R280CE	76
GS66516T	103

Table 6.3: Maximum deadtime dt_{max} for the inverter switches.

Topology	Device	dt_{inv} (ns)	dt_{rect} (ns)
DSAB	all	55	20
Single-Stacked DAB	all	55	20
Full-Bridge DAB	GS66516T	75	75
	IPD50R280CE	100	100

Table 6.4: Inverter and rectifier deadtimes for the converters simulated.

Based on the simulation results, the DSAB converter with EPC2012C inverter devices was found to be the most efficient topology overall, and the DSAB's low-power mode offered significant improvement in efficiency at low loads for both the Si and GaN versions. Fig. 6-5 shows efficiency curves for the three different topologies, for the applicable devices. The two Full-Bridge topologies show a significantly lower efficiency than both the Single-Stacked DAB and DSAB topologies across the entire load range, but especially below 200 W.

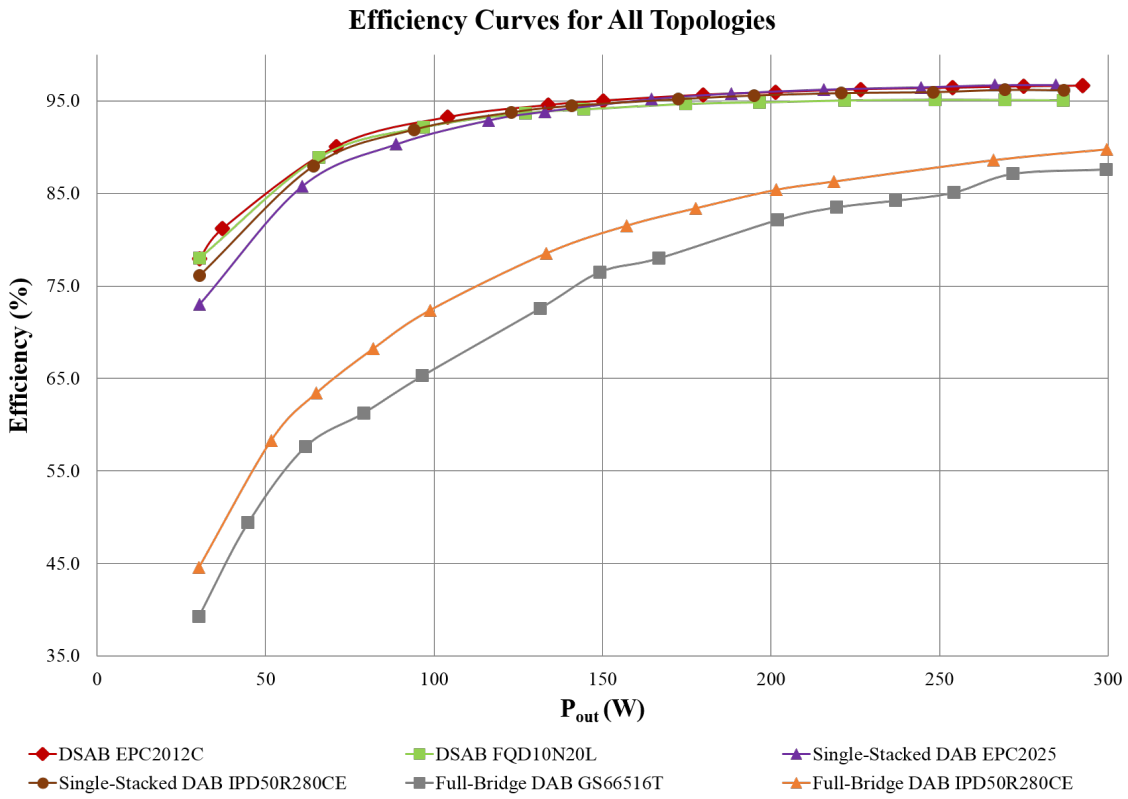


Figure 6-5: Simulated efficiency curves for the DSAB converter, the Single-Stacked DAB converter, and the Full-Bridge DAB. Each topology was simulated with both GaN and Si inverter devices. The converters were simulated over a range of output powers by varying the phase shift between the input and output bridges.

6.2.1 Comparison of Simulated Topologies

Figs. 6-6 shows simulated waveforms for the three topologies at 300 W. ϕ_{FB} is the phase shift for the Full-Bridge topology, ϕ_{DSAB} is the phase shift for the DSAB converter, and ϕ_{SSDAB} is the phase shift for the Single-Stacked DAB converter. ϕ_{FB} is much smaller than ϕ_{DSAB} and ϕ_{SSDAB}, which are approximately the same at 300 W. This is due to the larger primary voltage in the Full-Bridge DAB, as the peak primary voltage is 380 V for the Full-Bridge DAB, 190 V for the Single-Stacked DAB, and 95 V for the DSAB (where it is recognized that the DSAB has two primaries, and we are showing the voltage at each primary). The DSAB and the Single-Stacked DAB have almost identical current waveforms, as the total primary voltage and the phase shift for each converter are very close; however, the Full-Bridge converter has

a much lower inductor current.

The inductor currents are not perfectly flat-topped, as the turns ratio is 16:1 (or 32:1 for the Full-Bridge DAB), while the 380 V to 12 V conversion ratio corresponds to a non-integer turns ratio of 15.83:1 (or 31.67:1). The secondary voltage swings between -12 V and 12 V, with the rectifier operated as a full-bridge. Fig. 6-6 shows only the results for the GaN version of each topology (GS66516T for the Full-Bridge DAB, EPC2025 for the Single-Stacked DAB, and EPC2012C for the DSAB) for simplicity.

Of note is the fact that Full-Bridge DAB cannot achieve ZVS on the inverter devices, even at full load, as shown by the partial charge and discharge on its primary voltage waveform (green curve). This results in the much lower efficiency observed compared to the DSAB and Single-Stacked DAB, both of which are able to achieve full ZVS at 300 W.

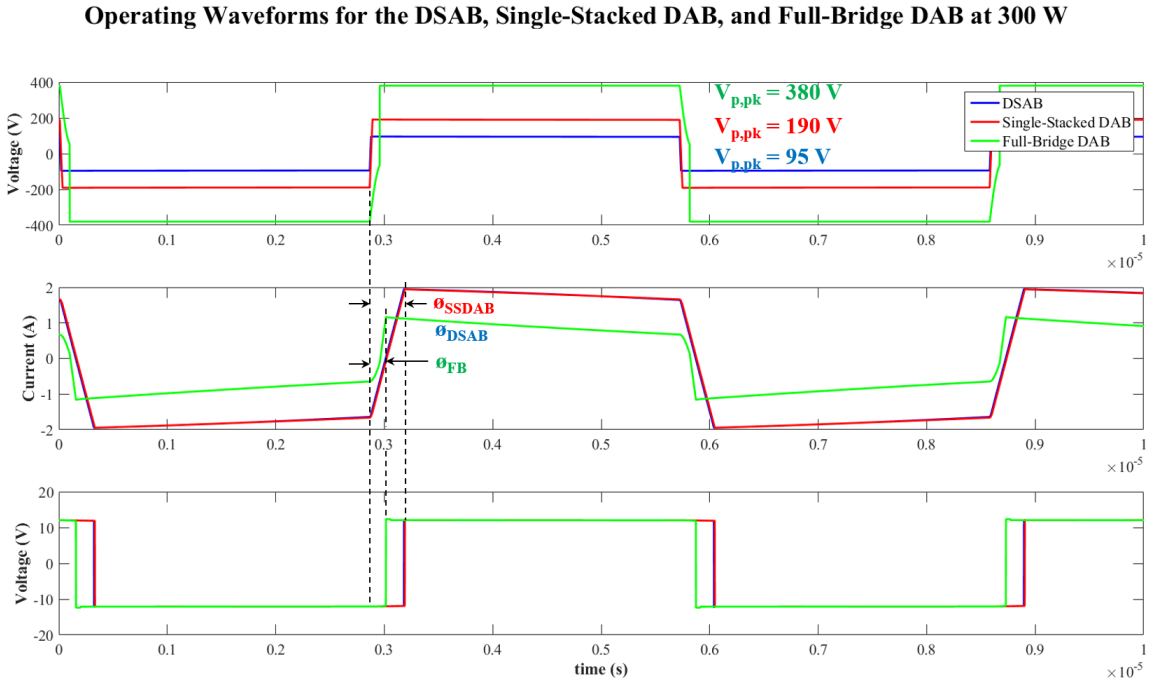


Figure 6-6: Simulated operation waveforms for the DSAB converter (blue curve), the Single-Stacked DAB converter (red curve), and the Full-Bridge DAB (green curve) at 300 W. The peak primary voltage for each topology is labeled in the top plot.

Full-Bridge DAB

As can be seen from Fig. 6-5, the Full-Bridge topology is significantly less efficient than the DSAB and Single-Stacked DAB. This is due to two main reasons:

1. The Full-Bridge DAB cannot achieve full ZVS for either inverter device, even at full load, due to the lower leakage inductor current. Although the C_{oss} of the IPD50R280CE device is lower than that of the EPC2012C and FQD10N20L devices used in the DSAB, the leakage inductor current is not great enough to completely discharge and charge the parasitic device output capacitance during the deadtime between switch transitions

2. The Full-Bridge DAB has higher switching loss, even in the case where all three topologies have lost ZVS, as the voltage across the Full-Bridge devices is two times that of the Single-Stacked DAB and four times that of the DSAB. Since switching losses are proportional to $C_{oss}V_{sw}^2 f$, the higher voltage will contribute to dramatically higher switching losses. In part this arises from the favorable trade-off in $R_{ds,on}C_{oss}$ product for multiple lower-voltage devices as compared to a single high-voltage device as described in Chapter 4.

Fig. 6-7 and Fig. 6-8 show the drain-to-source (V_{ds}) and gate-to-source (V_{gs}) waveforms for the switches in one of the inverter's half-bridges, designated as Q_1 and Q_2. $V_{ds,Q1}$ is the top switch drain-to-source voltage and $V_{ds,Q2}$ is the bottom switch drain-to-source voltage, similar to Fig. 6-1 (a). The V_{ds} waveforms are shown above the corresponding gate signals, $V_{gs,Q1}$ and $V_{gs,Q2}$, zoomed in on the deadtime between the gate signals on-times. The V_{ds} waveforms are not able to sinusoidally ramp up or down to the final switch voltage within the given deadtime, reaching only about 41% of the final switch voltage for the GS66516T devices and 54% of the final switch voltage for the IPD50R280CE devices, before hard-switching the rest of the way. For both Full-Bridge topologies, the deadtime was set as the maximum possible deadtime (75 ns for the IPD50R280CE devices and 100 ns for the GS66516T devices). This behavior highlights the importance of low C_{oss} devices, as even though

the IPD50R280CE device has much higher $R_{ds,on}$ compared to the GS66516T device (450 mΩ vs. 46.875 mΩ), it is able to soft-switch for more of the switch transition due to its lower C_{oss} value, greatly reducing switching losses and increasing efficiency.

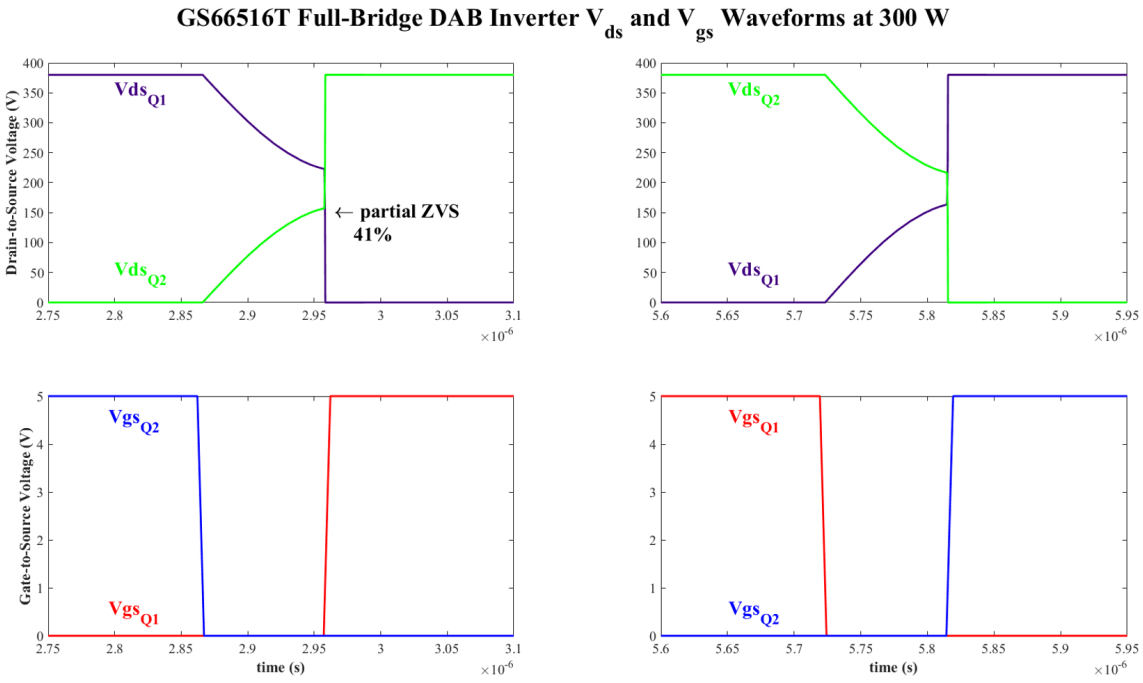


Figure 6-7: Simulated inverter device V_{ds} and V_{gs} waveforms for a Full-Bridge DAB with GS66516T inverter devices at 300W. The available current can only charge or discharge the switch voltage to 41% of its final value.

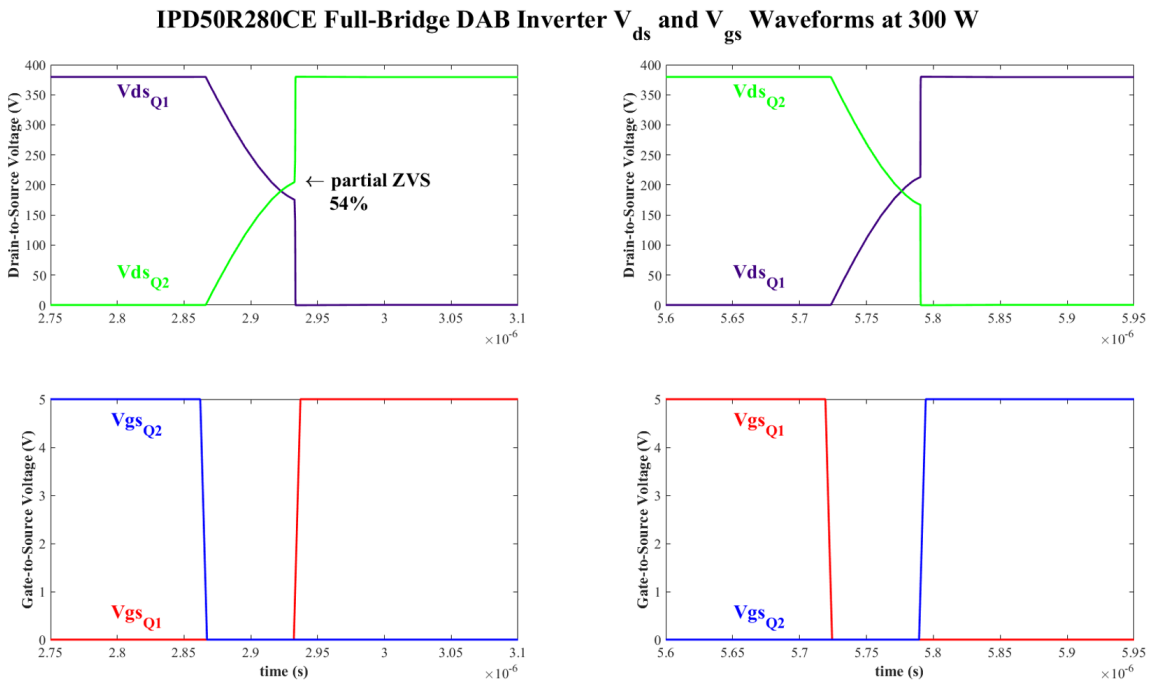


Figure 6-8: Simulated inverter device V_{ds} and V_{gs} waveforms for a Full-Bridge DAB with IPD50R280CE inverter devices at 300W. The available current can only charge or discharge the switch voltage to 54% of its final value.

Single-Stacked DAB

Fig. 6-9 shows zoomed-in simulated efficiency curves for the DSAB and Single-Stacked DAB converter topologies, for both GaN and Si devices. At high powers, the GaN Single-Stacked DAB is close in efficiency to the DSAB GaN, as both have similar $R_{ds,on}$ and C_{oss} (105 mΩ and 102.5 pF, compared to 141.75 mΩ and 108.125 pF, respectively). Interestingly, the Si Single-Stacked DAB has higher efficiency than the Si DSAB at high powers, due to its lower $R_{ds,on}$ and lower C_{oss} (450 mΩ and 72.5 pF, compared to 525 mΩ and 116 pF, respectively). At lower powers both the Si and GaN Single-Stacked DAB start to drop in efficiency more rapidly than the Si and GaN DSAB converters, which have similar performance to each other at low powers because of their similar C_{oss} values.

Additionally, the Single-Stacked DAB converters lose ZVS more quickly than either of the DSAB converters, even given the relatively low C_{oss} values for the Single-Stacked DAB inverter devices. The EPC2025 Single-Stacked converter loses ZVS at

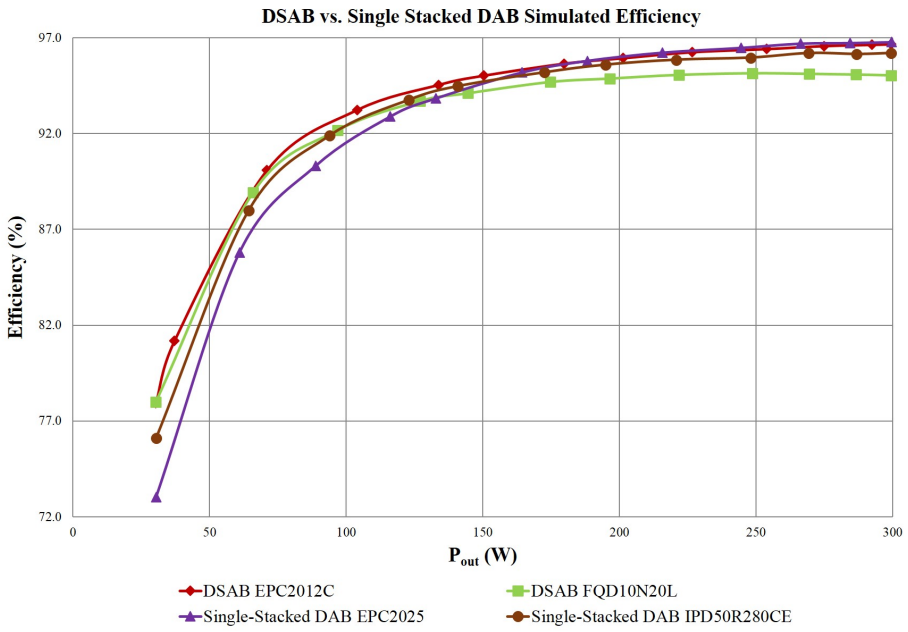


Figure 6-9: Simulated efficiency curves for for the DSAB and Single-Stacked converters with GaN and Si devices.

175 W, while the IPD50R280CE Single-Stacked converter loses ZVS at 136 W. Here, losing ZVS is defined as the point where the converter is only able to charge or discharge the switch capacitance to ∼95% of the final switch voltage. As the converter can still soft-switch during the majority of the switch transition, the efficiency can still be quite high when ZVS is just lost, but rapidly starts to decrease with decreasing output power, as more of the transition is traversed in a lossy manner. Figs. 6-10 and 6-11 show the inverter device V_{ds} and V_{gs} waveforms for the Single-Stacked DAB with EPC2025 and IPD50R280CE inverter devices at the output power where the converters lose ZVS.

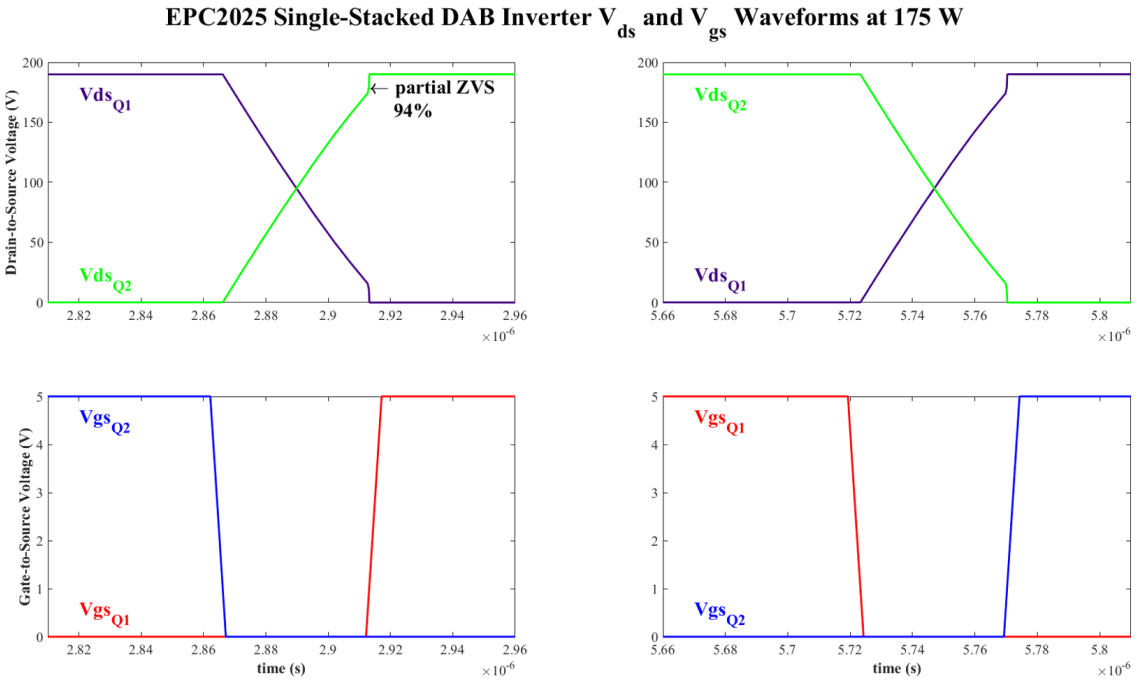


Figure 6-10: Simulated inverter device V_{ds} and V_{gs} waveforms for the Single-Stacked DAB with EPC2025 inverter devices at 175 W, when the converter starts to lose ZVS. The available current can only charge or discharge the switch voltage to 94% of its final value.

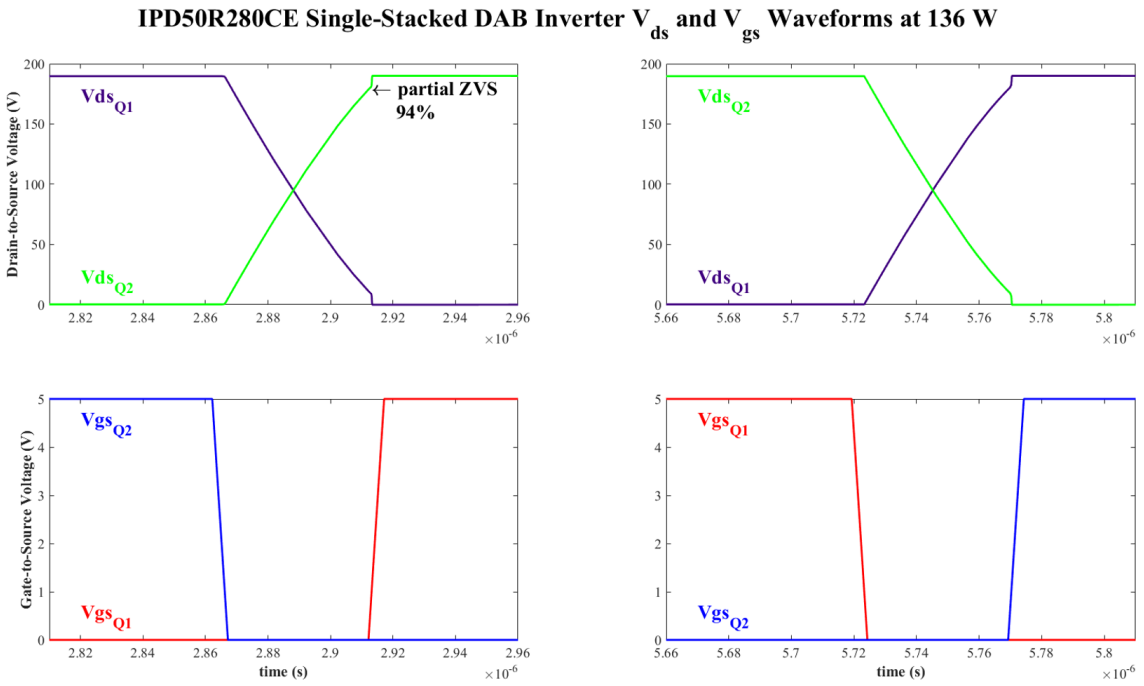


Figure 6-11: Simulated inverter device V_{ds} and V_{gs} waveforms for the Single-Stacked DAB with IPD50R280CE inverter devices at 136 W, when the converter starts to lose ZVS. The available current can only charge or discharge the switch voltage to 94% of its final value.

Double-Stacked Active Bridge

Both the Si and GaN DSAB converters can achieve ZVS at 300 W, and can also maintain ZVS down to a much lower power level than the Single-Stacked DAB converters. The EPC2012C DSAB was able to maintain ZVS down to 104 W in simulation, while the FQD10N20L Double Stacked Active Bridge (which had slightly higher C_{oss}) was able to maintain ZVS down to 120 W, lower than that achieved by either device simulated in the Single-Stacked DAB. Figs. 6-12 and 6-13 show the inverter device V_{ds} and V_{gs} waveforms for the DSAB, at the output power where ZVS is lost.

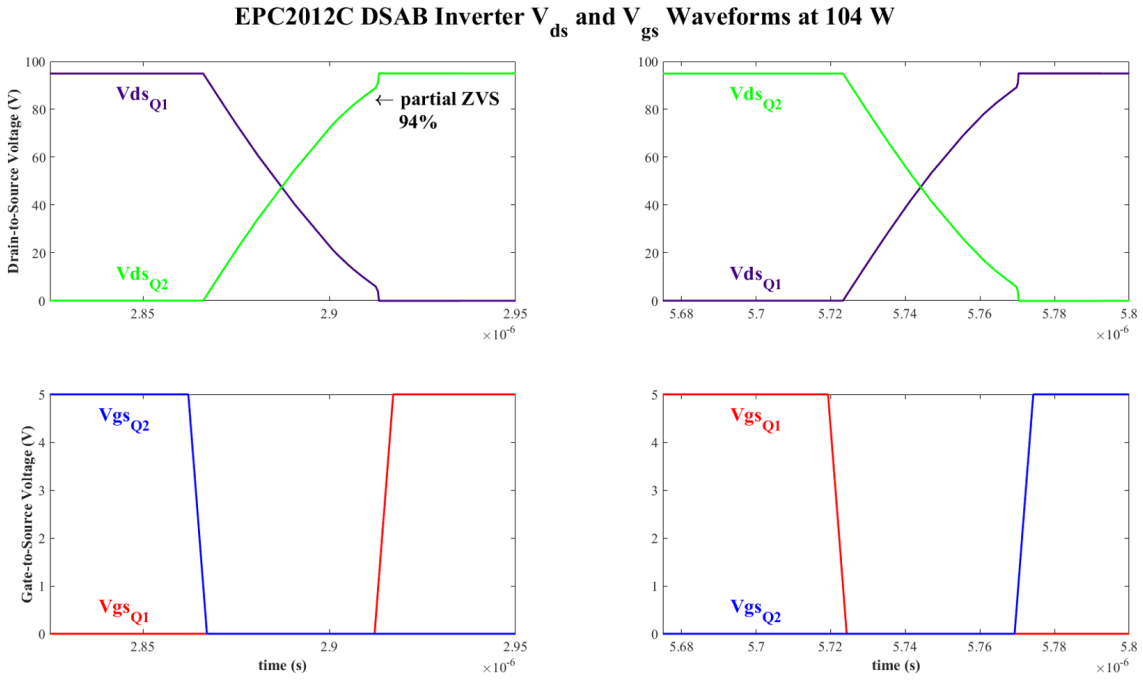


Figure 6-12: Simulated inverter device V_{ds} and V_{gs} waveforms for the DSAB with EPC2012C inverter devices at 104 W, when the converter starts to lose ZVS. The available current can only charge or discharge the switch voltage to 94% of its final value.

Additionally, the DSAB converter offers the opportunity to compare the performance of 200 V Si and GaN devices. The GaN EPC2012C device has a much lower $R_{ds,on}$ than the Si FQD10N20L device (105 mΩ compared to 525 mΩ), resulting in a 1-1.5% increase in efficiency at higher output powers (1.7% at 300 W) compared to the Si device. (Note that 1.5% of output power is a substantial improvement in this situation where the total loss is less than 5% of the output power.) This is due to the

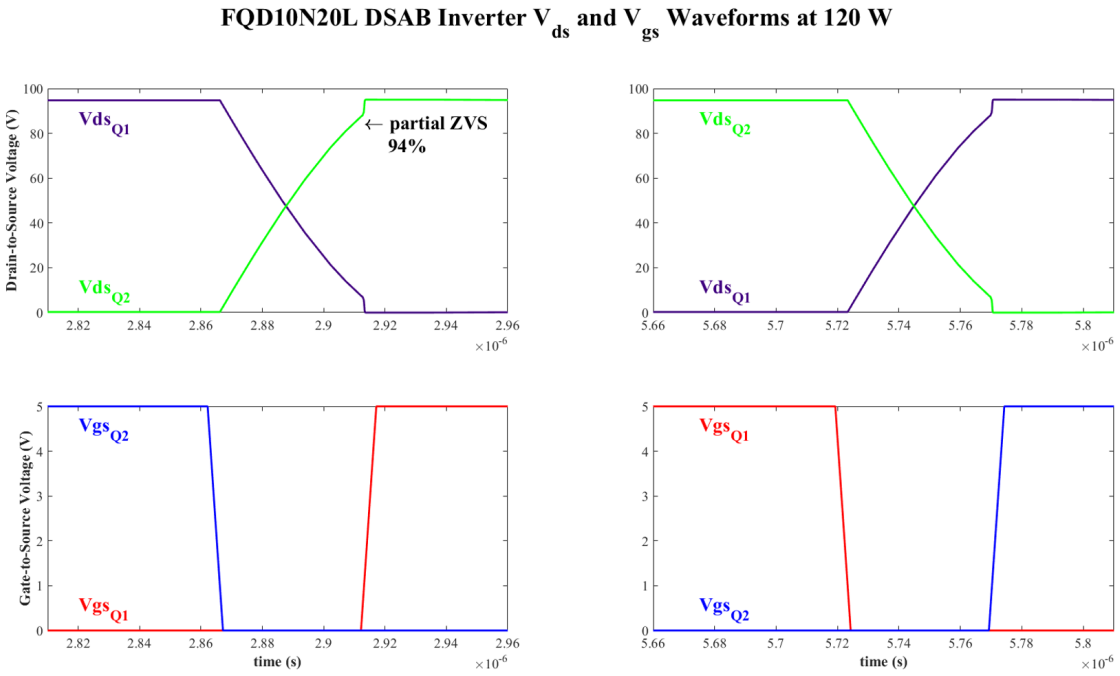


Figure 6-13: Simulated inverter device V_{ds} and V_{gs} waveforms for the DSAB with FQD10N20L inverter devices at 120 W, when the converter starts to lose ZVS. The available current can only charge or discharge the switch voltage to 94% of its final value.

fact that higher output powers correspond to higher RMS currents in the inverter, leading to greater $I_{RMS}^2 R_{ds,on}$ losses. However, as the GaN and Si devices have similar C_{oss} values, they lose ZVS within ∼16 W of each other, and have very similar efficiency characteristics at low power, where the effects of switching loss dominate those of conduction loss due to the presence of hard-switching and lower inverter RMS currents.

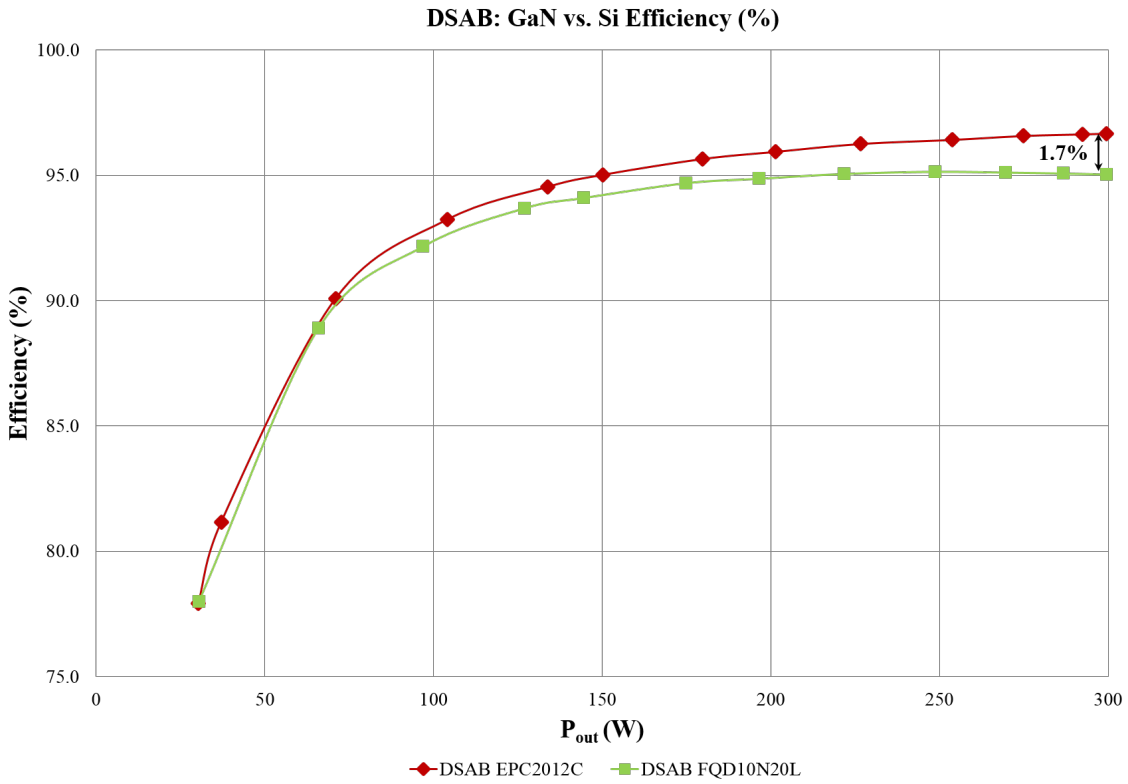


Figure 6-14: Simulated efficiency for the DSAB converter, populated with GaN EPC2012C inverter devices (red curve) and Si FQD10N20L inverter devices (green curve).

6.2.2 Full-Power Mode vs. Low-Power Mode in the DSAB

In addition to its wider ZVS range under normal operation, the DSAB also offers an attractive low-power mode that greatly increases efficiency at low loads by reducing core loss and switching loss. In this low-power mode, only one primary is energized at a time, and the rectifier is configured as a half-bridge or voltage-doubler rectifier through the use of an auxiliary switch. More detailed descriptions of the low-power mode operation can be found in Chapter 3.

Fig. 6-15 shows simulated efficiency curves for the GaN and Si DSAB converters running in full-power mode and low-power mode. The low-power mode is designed for output power levels around a quarter of the rated power and below, and was simulated from around 130 W and below, to show the intersection point of the full-power mode and low-power mode (around 100 W in simulation). The low-power mode

has a simulated efficiency that is 7-10% higher than the full-power mode for output powers lower than 50 W. It can also maintain higher than 90% efficiency down to 35 W, as opposed to ∼70 W for the full-power mode.

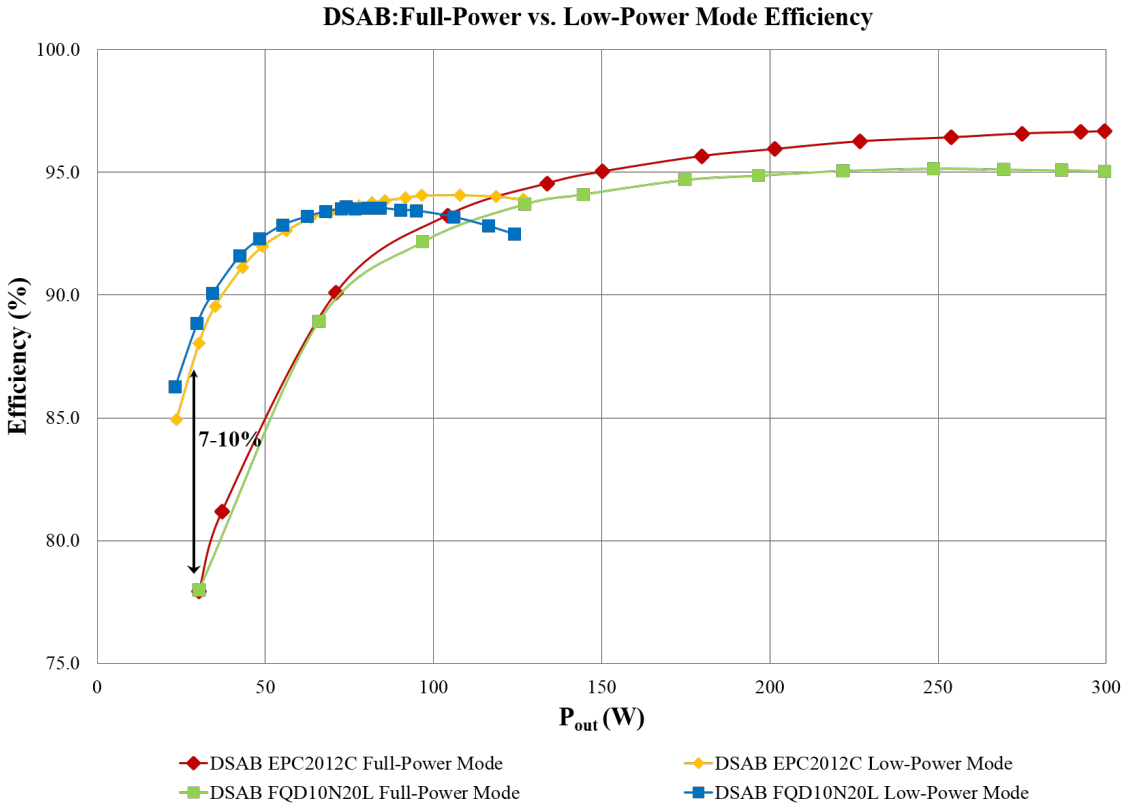


Figure 6-15: Simulated efficiency curves for the DSAB in both low-power and full-power modes, populated with GaN EPC2012C inverter devices (in red and yellow), and Si FQD10N20L inverter devices (in blue and green). The low-power mode enables the DSAB to maintain higher than 90% efficiency down to ∼35 W, and provides an efficiency that is around 7-10% higher than the full-power mode below 50 W.

Table 6.5 summarizes the simulated efficiency at 75 W for the DSAB in the full-power and low-power modes, for both EPC2012C and FQD10N20L inverter devices. It also gives the phase angle ϕ required in simulation for each converter to produce 75 W. At this operating point, the low-power mode has a simulated efficiency that is 2.9% higher than that of the normal mode when using EPC2012C devices, and 3.3% higher when using FQD10N20L devices. Additionally, the low-power mode's larger ϕ means the inductor current at the switch transition will be higher, which allows the low-power mode to maintain ZVS even at 75 W (and substantially below).

Table 6.6 summarizes the simulated efficiency at 30 W for the DSAB in full-power and low-power modes, where the low-power mode provides a much higher efficiency. The low-power mode is able to achieve simulated efficiencies above 88% all the way down to 30 W, while the full-power mode drops to around 78% at 30 W.

Output Power = 75 W

Topology	Device	ϕ (deg)	Efficiency (%)
DSAB Full-Power	EPC2012C	5.94	90.67
	FQD10N20L	6.19	90.23
DSAB Low-Power	EPC2012C	19.08	93.59
	FQD10N20L	19.37	93.55

Table 6.5: Simulated efficiency of full-power mode vs. low-power mode at 75 W

Output Power = 30 W

Topology	Device	ϕ (deg)	Efficiency (%)
DSAB Full-Power	EPC2012C	4.03	77.93
	FQD10N20L	4.14	78.00
DSAB Low-Power	EPC2012C	8.57	88.05
	FQD10N20L	8.64	89.12

Table 6.6: Simulated efficiency of full-power mode vs. low-power mode at 30 W

Fig. 6-16 shows the simulated operating waveforms for both operating modes at 75 W. The low-power primary voltages are shown in blue and purple, the leakage inductance current is shown in green, and the secondary voltage is shown in red. The corresponding full-power mode waveforms are shown with a dashed black line for each plot. In the full-power mode, the primary voltages are the same, while in the low-power mode the primary voltages alternate between holding zero voltage and being driven in a square-wave mode, as described in Chapter 3. The secondary voltage in the low-power mode is also half the amplitude as in the full-power mode, as the rectifier is configured as a half-bridge rectifier in the low-power mode. The inductor current is greatly increased at the switch transition in the low-power mode, which allows it to achieve ZVS at 75 W, whereas the full-power mode has already lost ZVS at 104 W.

Looking at Fig. 6-16, one can also see that there are three distinct switching events:

1. Both primary voltages switch down, with one primary going from positive voltage to 0 V and one primary going from 0 V to negative voltage

2. Both primary voltages switch down, with the opposite primary going from positive voltage to 0 V and vice versa.

3. One primary switching from negative to positive, and the other primary staying at 0 V.

Fig. 6-17 shows the inverter device drain-to-source waveforms for each of three switch transitions for the top primary voltage, or $V_{p,1}$. The low-power primary voltages are again shown in blue and purple, with the full-power mode voltage shown with a dashed black line. All four switch V_{ds} waveforms are shown for each switching transition in the low-power mode in blue, red, green, and cyan. The corresponding V_{ds} waveforms for the full-power mode are shown with a dashed black line. The low-power mode can achieve ZVS on all three transitions, while the full-power mode only achieves partial ZVS.

The simulated double-stacked EPC2012C converter operating in low-power mode is able to achieve full ZVS on all switch transitions down to 51 W. The different switch events lose ZVS at slightly different times, and in simulation the transitions where the primary voltage swings from negative to positive rather than positive to 0 V or 0 V to negative maintain ZVS down to a lower power. Waveforms for the EPC2012C converter operating in the low-power mode at 46 W are given in Figs. 6-18 and 6-19. These waveforms are included to illustrate how different transitions on the two inverters can lose ZVS at different times.

A summary of the simulated ZVS performance of each converter topology and device combination is given in Table 6.7.

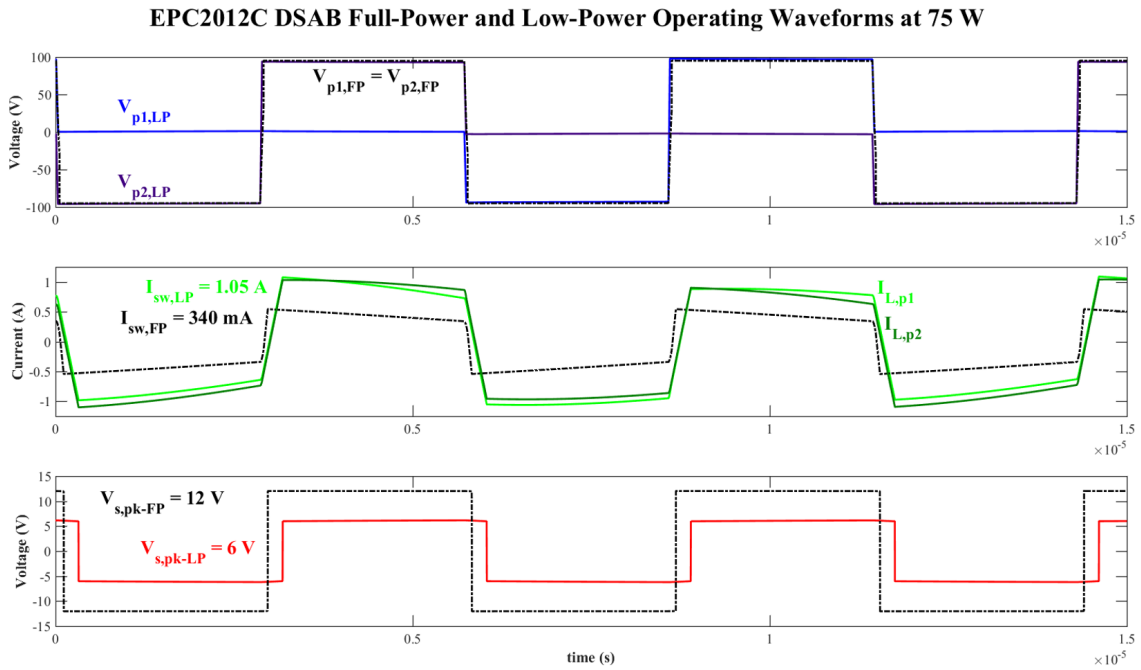


Figure 6-16: Operating waveforms for the DSAB in full-power and low-power modes. Full-power mode waveforms are shown with a dashed black line. The two primary voltages in low-power mode are shown in blue and purple. The two leakage inductor currents in low-power are shown in green and dark green. The low-power secondary voltage is shown in red, and is half that of the full-power secondary voltage, as the rectifier is configured as a half-bridge rectifier in the low-power mode.

Topology	Device	P_{out} where ZVS lost (W)	% ZVS
Full-Bridge DAB	GS66516T	300	43*
	IPD50R280CE	300	56*
Single-Stacked DAB	EPC2025	175	94
	IPD50R280CE	136	94
DSAB Full-Power	EPC2012C	104	94
	FQD10N20L	120	94
DSAB Low-Power	EPC2012C	51	94**
	FQD10N20L	53	94**

Table 6.7: Summary of ZVS range for the converters simulated.
*ZVS not achievable at full-load
**at the output power where at least one transition loses ZVS in the low-power mode

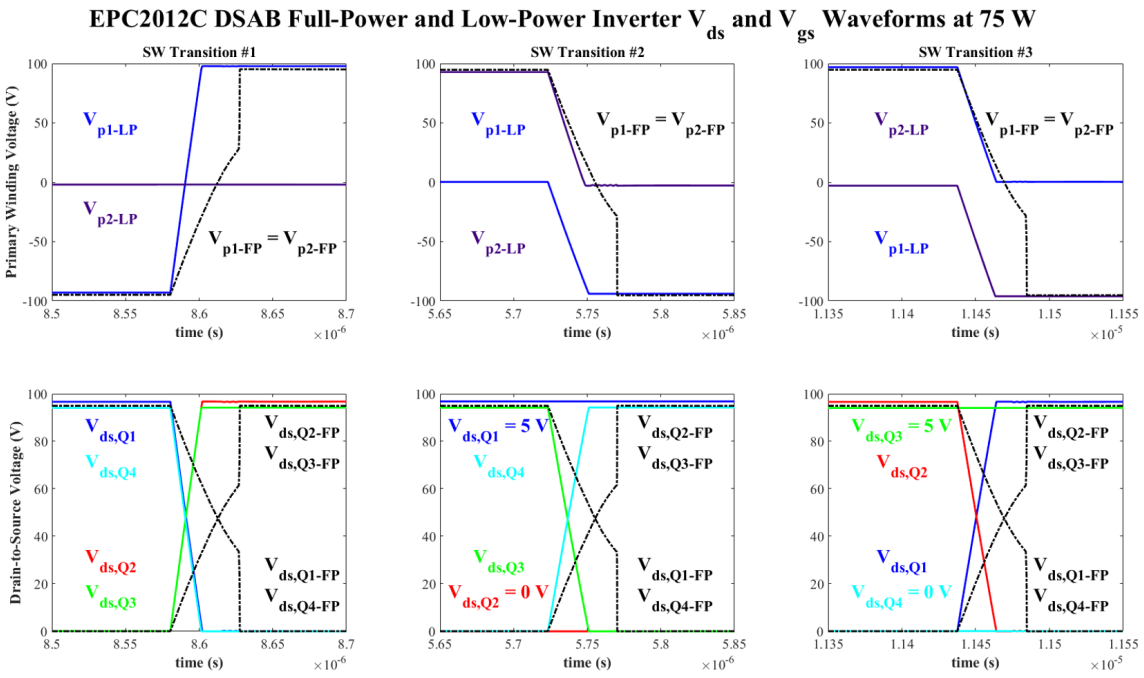


Figure 6-17: The top plots show the simulated primary voltages, in dashed black for the full-power mode and in blue and purple for the low-power mode at 75 W. Each of the three switch transitions for the top primary are shown zoomed in. The bottom plot shows the inverter device V_{ds} and V_{gs} waveforms for the full-power mode at 75 W (in dashed black lines), and for the low-power mode at 75 W (in red, blue, green, and cyan). As can be seen, the inverter devices achieve ZVS in the low-power mode, and can reach their final values much quicker than in the full-power due to the higher inductor current.

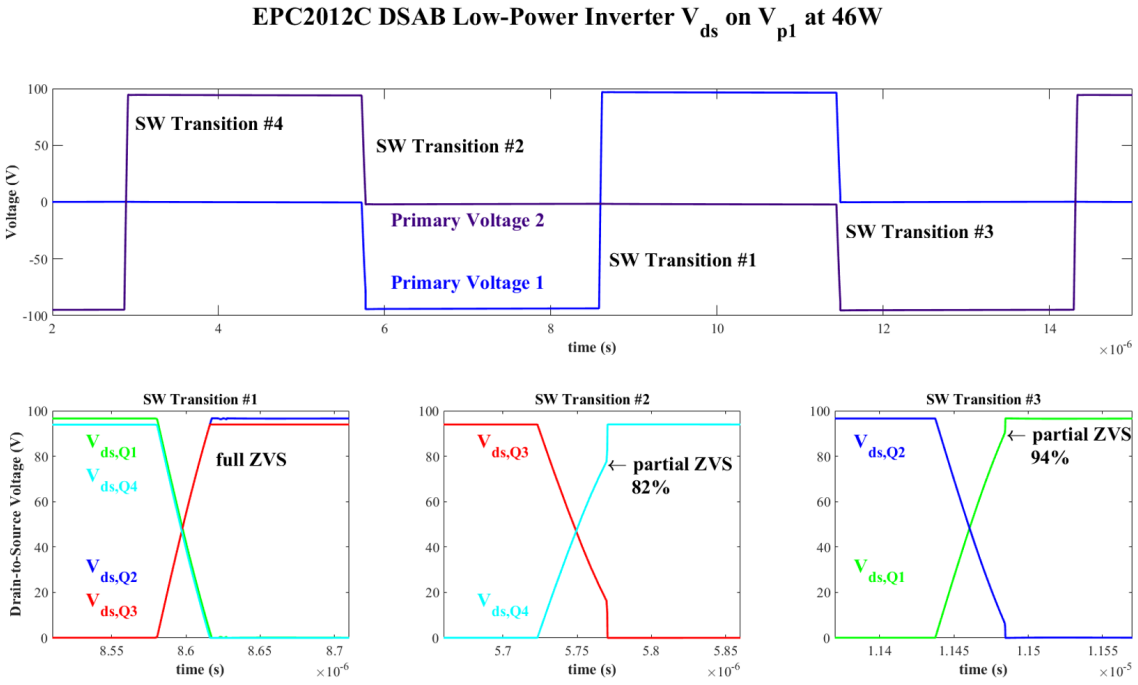


Figure 6-18: EPC2012C device V_{ds} waveforms for each switch transition on $V_{p,1}$ (top primary), at the point where several transitions have lost ZVS (46 W).

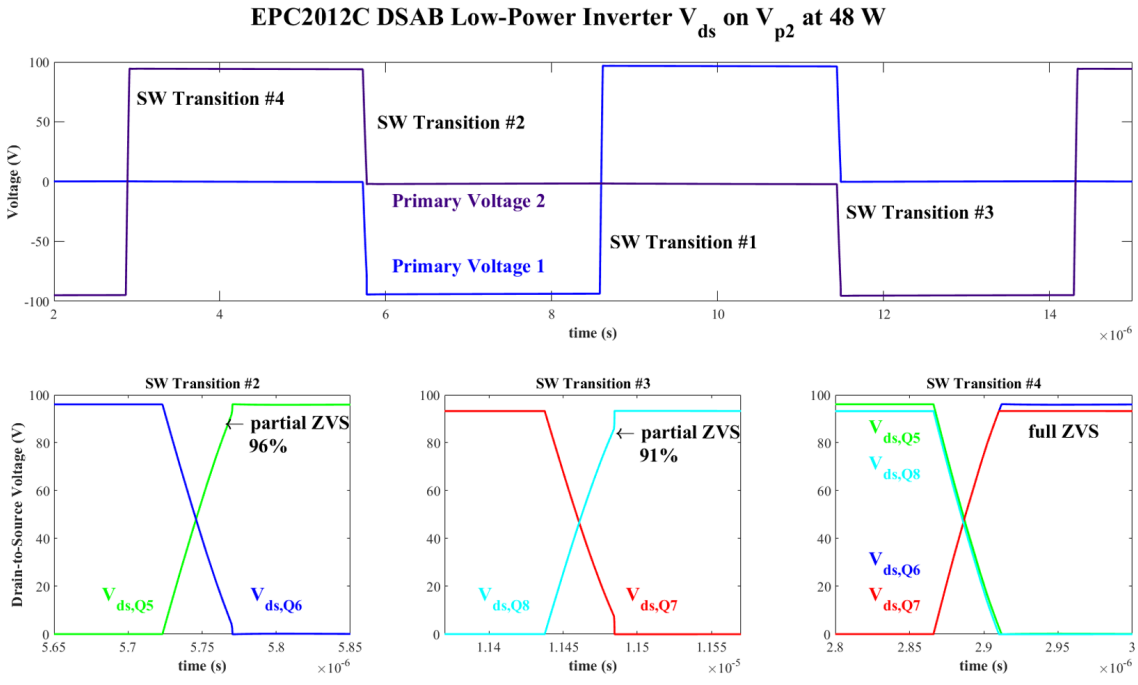


Figure 6-19: EPC2012C device V_{ds} waveforms for each switch transition on $V_{p,2}$ (bottom primary), at the point where several transitions have lost ZVS (48 W).

Effect of Parasitic Resistance in Low-Power Switch Path

One aspect of the low-power mode to note is the importance of creating a very low resistance path through the low-power auxiliary switch, Q_{LP}. Extra resistance in this path, due to high $R_{ds,on}$ devices or high PCB trace resistance, can dramatically decrease the efficiency. Fig. 6-20 shows a graph of the simulated efficiency of the EPC2012C DSAB converter operating in the low-power mode, with and without extra parasitic resistance in the Q_{LP} switch path. The "EPC2012C Low-Power" curve only includes 3 mΩ of resistance, as each of the source-connected EPC2023 devices used to implement Q_{LP} have an $R_{ds,on}$ of 1.5 mΩ. The "EPC2012C Low-Power with added resistance" curve had an additional 5 mΩ of extra resistance added in series with Q_{LP}.

At higher power levels (above 50 W) the efficiency of the converter with the extra resistance starts to decrease dramatically. The difference in efficiency increases as the output power increases, due to the higher currents and therefore higher $I_{RMS}^2 R$ losses from the extra resistance. At 100 W, where the low-power mode efficiency curve intersects the full-power mode efficiency curve in simulations, the difference in efficiency is around 1.7%.

Fig. 6-21 shows the current through the low-power switch Q_{LP}, for the case where only the $R_{ds,on}$ of the devices is included at 102 W, the case where 5 mΩ of extra resistance is added and the original phase-shift is used (resulting in a lower output power of 100 W), and the case where 5 mΩ was added and the phase shift was increased to bring the output power back up to the original value of 102 W. In the case with added resistance, the switch current has a steeper slope, resulting in a higher peak current. The overall efficiency also goes down, as does the output power for a constant ϕ. By increasing ϕ, the output power returns to the original value, but the peak current value also increases.

Table 6.8 gives a summary of the simulated efficiency in the low-power mode with and without added parasitic resistance near 100 W. It can be seen that the extra resistance requires that ϕ be increased in order to deliver a given output power.

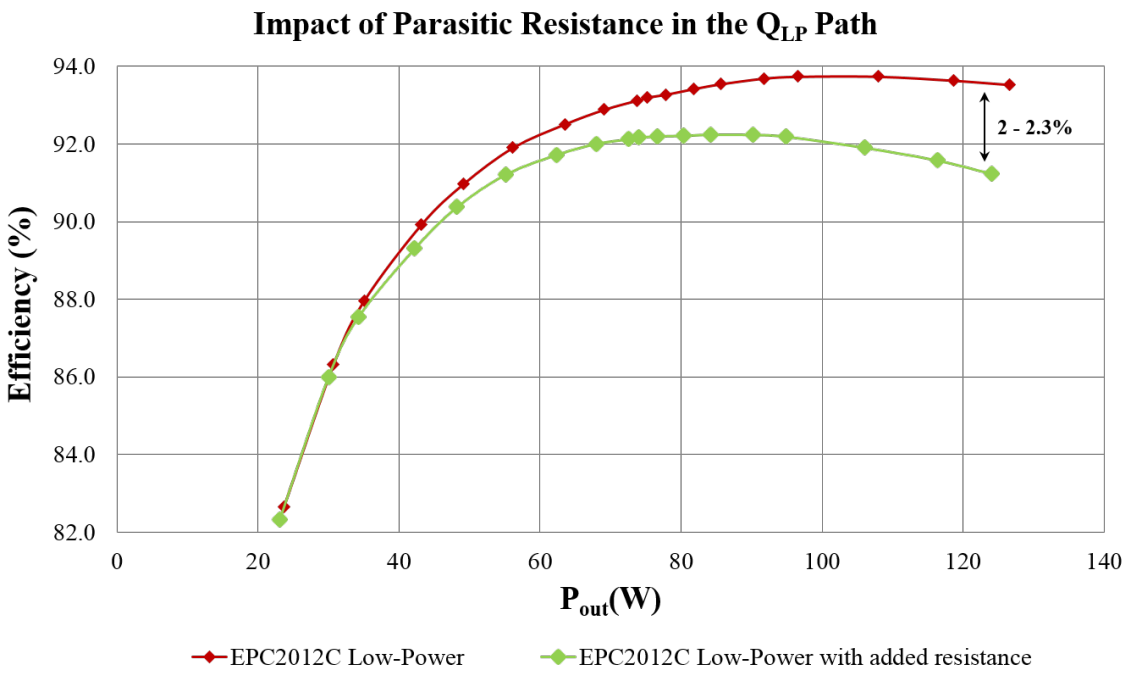


Figure 6-20: Simulated efficiency curves for the DSAB operating in the low-power mode, with and without extra resistance added in the Q_{LP} path.

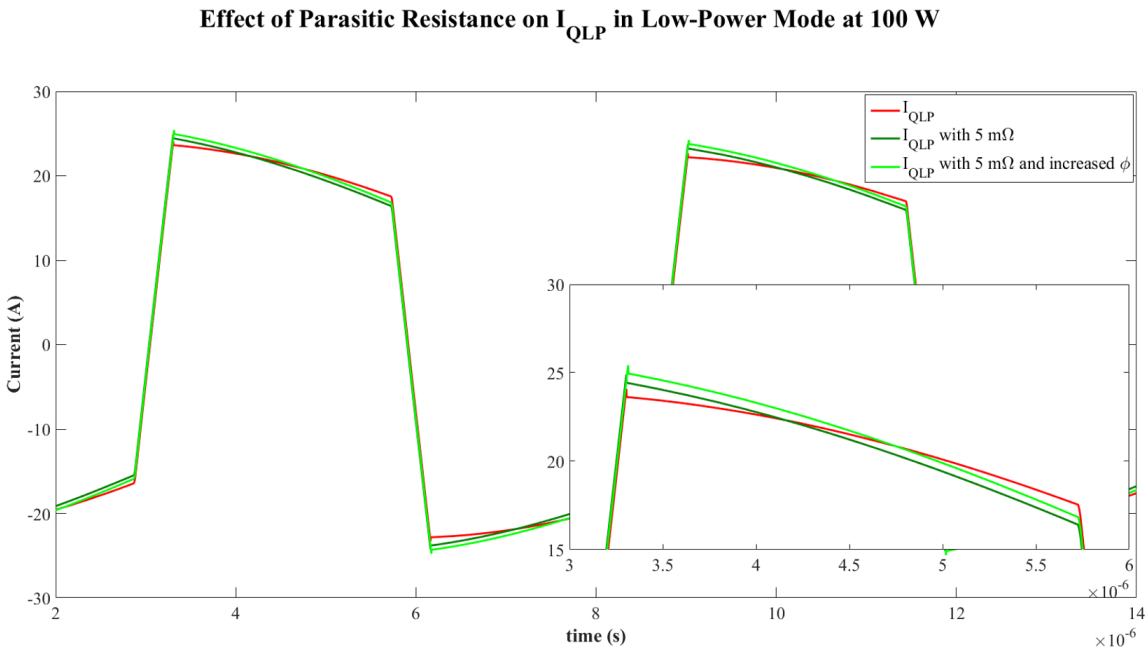


Figure 6-21: Simulated current through Q_{LP} at $phi = 27°$ and P_{out}=102.4 W (red), at $phi = 27°$ and P_{out}=100.6 W (dark green), and at $phi = 27.6°$ and P_{out}=102.4 W (light green). The inset shows the slope of the current waveform zoomed in. Adding resistance to the path causes the slope to become steeper.

Condition	ϕ (deg)	P_{out} (W)	Efficiency (%)
No added resistance	27	102.4	93.73
5 mΩ added, ϕ constant	27	100.6	92.04
5 mΩ added, ϕ increased	27.6	102.4	91.98

Table 6.8: Table of P_{out}, ϕ, and efficiency for the DSAB operating in low-power mode with EPC2012C inverter devices, with and without added resistance in the Q_{LP} path. If the output power is held constant, adding 5 $m\Omega$ of extra resistance decreases the efficiency by 1.75%.

6.2.3 Paralleling Rectifier Devices

Additionally, simulations were done to see how paralleling the rectifier devices affects the efficiency of the converter. By paralleling the devices, one can decrease the total resistance of that path, reducing resistive losses. However, paralleling devices also increases the device parasitic output capacitance, making it harder to charge and discharge the capacitance for a given deadtime and current, which can reduce the ZVS range.

Fig. 6-22 shows simulated efficiency curves for the DSAB using EPC2012C inverter devices, with one to three paralleled EPC2023 rectifier devices. Table 6.9 gives the efficiency at 300 W for the different numbers of paralleled EPC2023 devices. At 300 W, using two paralleled devices has an efficiency that is 0.24% higher than with using a single device, and using three paralleled devices increases efficiency by 0.39% as compared to using a single device. Two and three paralleled sets of EPC2023 devices are very close in efficiency, and are more efficient than using a single EPC2023 device from 100 W to 250 W.

However, below 100 W, the converters with fewer parallel devices become slightly more efficient in simulation. This matches the expectation that at high powers, where low $R_{ds,on}$ is more important, paralleled devices are favorable, while at low powers, where low capacitance is more important, a single device is more favorable. As the low-power mode efficiency curve intersects the full-power mode's around 100 W, the slight decrease in efficiency shown here is not very important, as the low-power mode will naturally increase the currents in the rectifier, extending the rectifier switches'

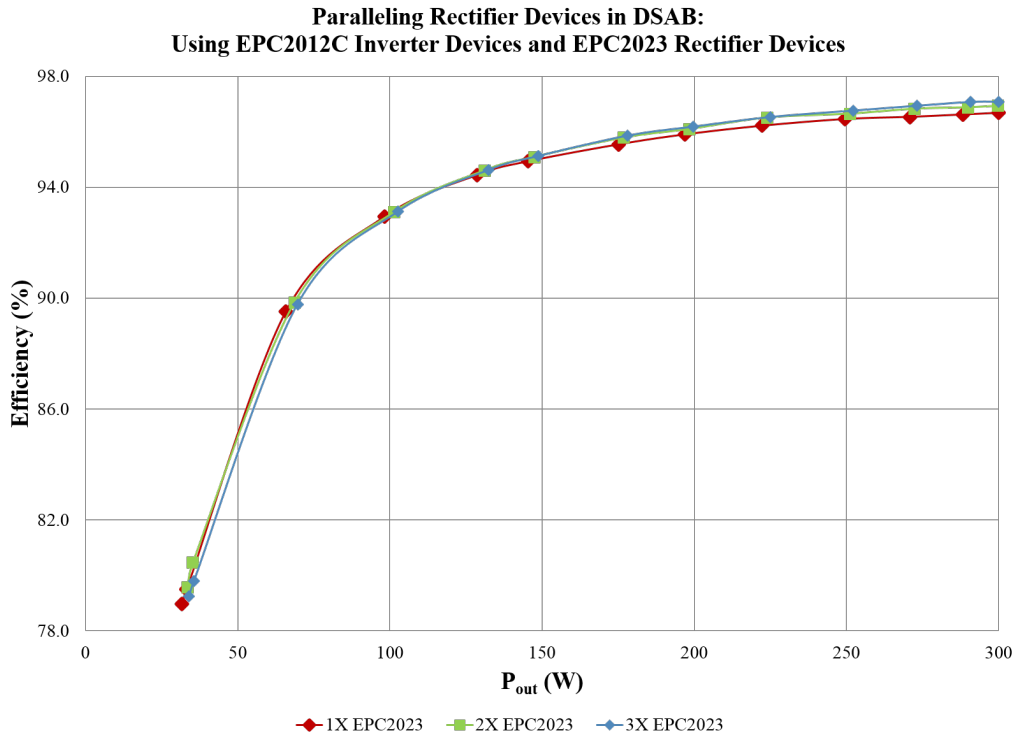


Figure 6-22: Efficiency curves for one to three paralleled EPC2023 devices in the DSAB rectifier stage, using EPC2012C inverter devices. At high powers, paralleled devices are more efficient, while at low powers, one device is the most efficient.

ZVS range.

Although 0.39% is not a huge increase in efficiency, paralleling devices is a relatively easy technique to implement and also helps with current handling (especially at the low-input voltage range of the converter operation, where the phase shift and therefore the peak current is higher than at nominal). Therefore, the prototypes were designed to be used with three paralleled devices, each driven with their own gate driver to minimize high-frequency loops in the layout.

Number of EPC2023 devices	P_{out} (W)	ϕ (deg)	Simulated efficiency (%)
1X	299.99	19.5	96.68
2X	299.74	19.39	96.92
3X	299.93	19.33	97.07

Table 6.9: Table of simulated efficiency at 300 W for the EPC2012C DSAB converter with one to three paralleled EPC2023 devices in the rectifier.

6.2.4 Wide Input Voltage Range

The DSAB converter was designed to also handle a wide input voltage range of 260 V to 410 V. For a typical data center application, the converter must be able to operate continuously at an input voltage range of 360 V to 410 V, and be able to run for short periods of time all the way down to 260 V [5].

The DSAB converter was simulated with an input voltage from 260 V to 410 V at 300 W, and showed good efficiency over the entire input voltage range. Fig. 6-23 shows the simulated efficiency of the DSAB converter using EPC2012C inverter devices and non-paralleled EPC2023 rectifier devices over an input voltage range of 260 V to 410 V.

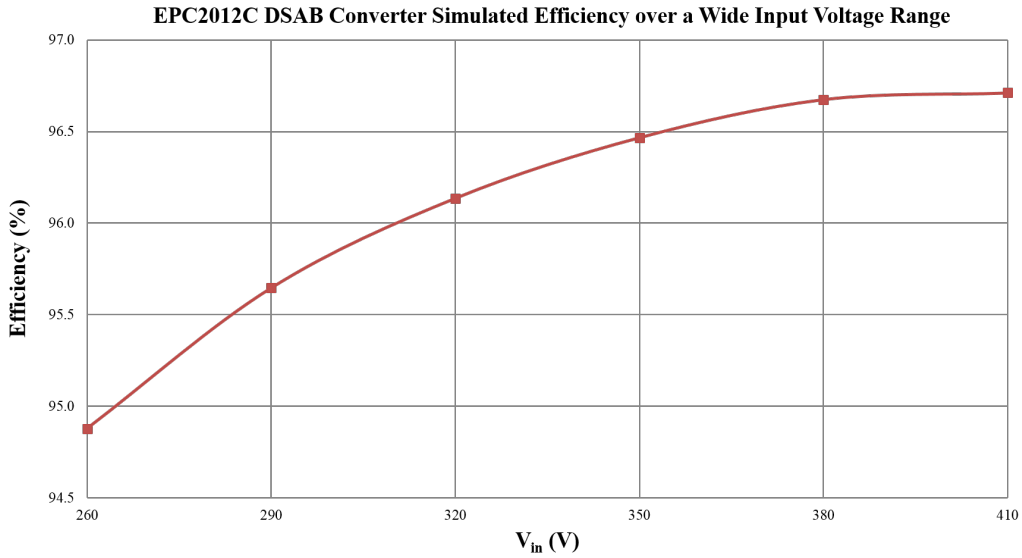


Figure 6-23: Simulated efficiency curve for the DSAB with EPC2012C inverter devices over an input voltage range of 260 V to 410 V. The converter is able to maintain greater than 94% efficiency over the entire input voltage range.

At lower input voltages, the phase shift must be increased to achieve the same output power, which results in increased switch currents in the inverter and rectifier. Additionally, as the input voltage gets further away from nominal, the primary-to-secondary relationship gets farther away from the ideal $\frac{V_p}{V_s} = N$, causing the leakage inductor current to become more peaked, resulting in higher RMS currents. These higher RMS currents can cause greater resistive losses in the circuit, reducing the

overall efficiency. As mentioned previously, paralleling rectifier devices can help to ensure that each device can handle the peak current, especially on the high current rectifier side.

Fig. 6-24 shows the primary voltage V_p and leakage inductor current I_L waveforms for the DSAB with EPC2012C inverter devices for V_{in} = 410 V (top), V_{in} = 380 V (middle), and V_{in} = 260 V (bottom). Because the transformer turns ratio was designed for the nominal operating point of 380 V, the current is fairly flat-topped at an input voltage of 380 V. However, when the input voltage is greater than nominal (e.g., 410 V) the current slopes upwards, and when the input voltage is less than nominal (e.g., 260 V) the current slopes downwards. The slope of the current increases as the input voltage gets farther away from nominal.

The large slope and peaked form of the current for an input of 260 V provides some challenges, as the higher peak current leads to higher loss and device stresses. Additionally, while the peak current is increased at 260 V, the current at the inverter switch transition is decreased due to the more sloped shape of the current waveform. Since the current is now close to zero at the switch transition, the converter does not have ZVS at 260 V, which can also be seen by the partial sinusoidal rise and fall on the primary voltage.

Table 6.10 gives a summary of the ϕ used for each V_{in} point, as well as the RMS current through the rectifier switches, $I_{rect,RMS}$. As V_{in} decreases, the RMS current in the inverter and rectifier switches also increases (only $I_{rect,RMS}$ is listed here, however).

V_{in} (V)	ϕ (deg)	$I_{rect,RMS}$ (A)
410	17.64	13.96
380	19.51	14.71
350	21.74	16.37
320	24.55	18.80
290	28.44	21.87
260	33.70	25.55

Table 6.10: Table of the phase shift ϕ, and RMS current through the rectifier switches $I_{rect,RMS}$ for the simulated EPC2012C DSAB converter for V_{in} = 260 V to 410 V.

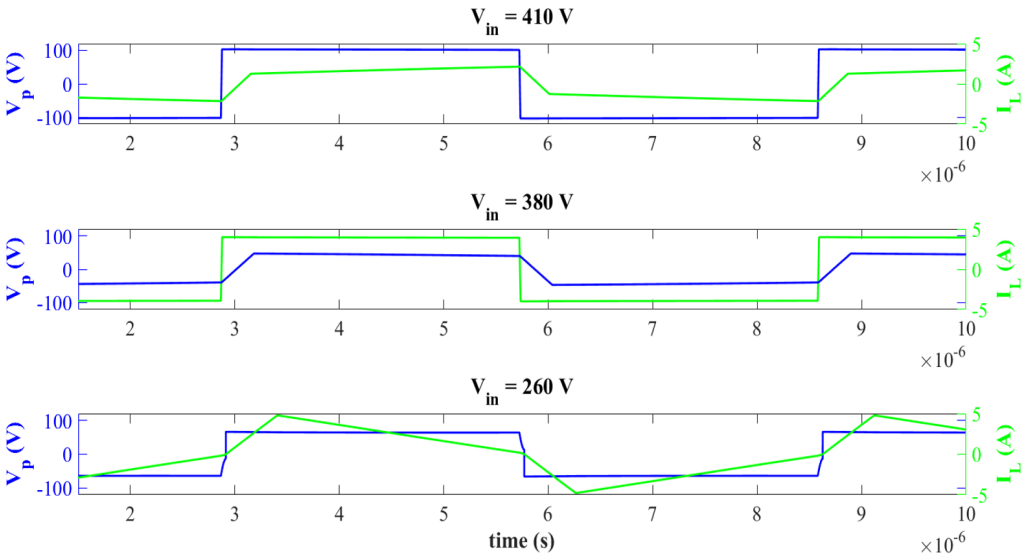


Figure 6-24: Simulated primary voltage V_p and leakage inductor current I_L waveforms for the case where $V_{in} = 410$ V (top), $V_{in} = 380$ V (middle), and $V_{in} = 260$ V (bottom) for the EPC2012C DSAB converter at 300 W.

6.3 Summary

Several techniques were investigated in simulation to improve efficiency and extend the ZVS range over a wide load range. A summary of these techniques and the resulting benefits is summarized here.

- **DSAB Topology:** The DSAB topology was shown to have very favorable efficiency, especially at low powers. The DSAB converter had ∼18-33% lower percent loss for 50% and lower load, compared to a more traditional Full-Bridge DAB structure. The DSAB also had lower percent loss than the comparable Single-Stacked DAB simulated, by about 2-4.5% of input power at 30 W depending on the inverter device.

- **Full-Power vs. Low-Power Modes:** The DSAB topology allows for a low-power mode which increases efficiency under light-load conditions. Compared to the full-power mode, the low-power mode has ∼ 7-10% higher efficiency.

- **GaN vs. Vertical Si Devices:** By using GaN or Superjunction device technologies, the efficiency at high powers where there are high currents can be

increased. For the DSAB, using GaN devices over Si devices results in 0.8-1.6% higher efficiency at high power, depending on the output voltage.

- **Paralleling Devices:** By paralleling the devices on the rectifier (the high-current side), the efficiency can be increased by ∼0.3-0.4% at high powers

The next chapter will present experimental data for the DSAB converter with EPC2012C and FQD10N20L inverter devices, as well as data for the Single-Stacked DAB converter with IPD50R280CE inverter devices. The GaN Single-Stacked DAB and the Full-Bridge DAB converters were not built due to the amount of new layout that would be needed to create the PCBs.

Chapter 7

Experimental Results

Several prototype boards were assembled and experimentally tested to validate the operation of the Double-Stacked Active-Bridge (DSAB) converter. The efficiency of each board was measured over a wide load range, and the efficiency curves and ZVS behavior of the various versions are presented in this chapter, along with oscilloscope captures of the DSAB's operating waveforms.

7.1 Prototype Boards

Three boards were assembled, as listed below:

1. Double Stacked Active-Bridge (DSAB) with GaN EPC2012C inverter devices
2. Double Stacked Active-Bridge (DSAB) with Si FQD10N20L inverter devices
3. Single-Stacked Dual-Active-Bridge (DAB) with Si Superjunction IPD50R280CE inverter devices

Only two printed circuit board (PCB) layouts were fabricated, as the Single-Stacked DAB was assembled by converting the Si DSAB layout, as described below. Pictures of the top and bottom sides of each assembled prototype board are presented here.

7.1.1 DSAB with GaN Inverter Devices

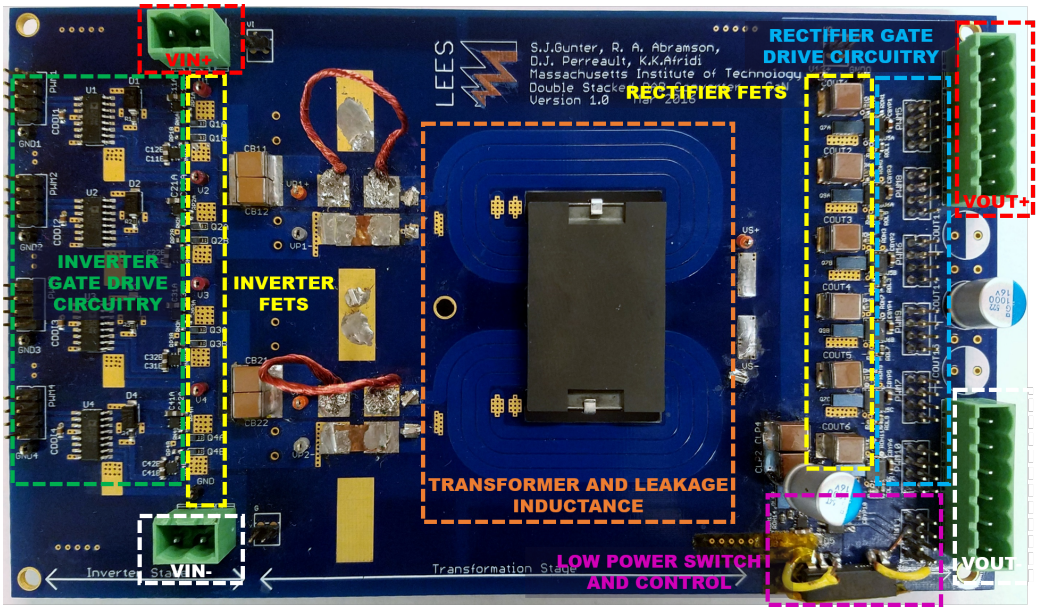


Figure 7-1: Top side of the DSAB board, with GaN inverter devices. The inverter and rectifier devices and control circuitry are shown, as well as the single-core magnetic component.

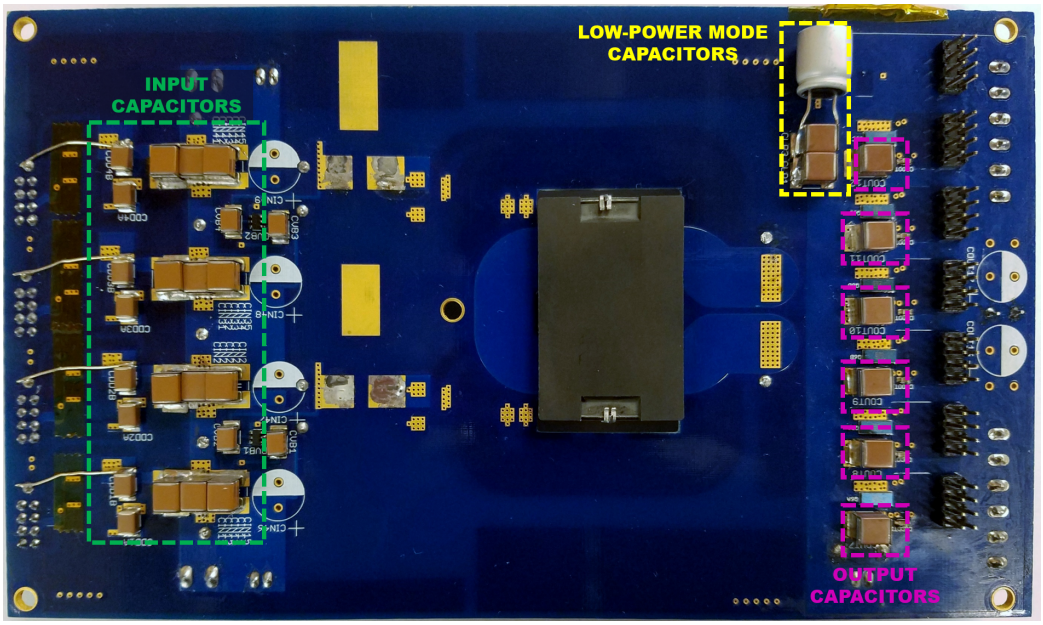


Figure 7-2: Bottom side of the DSAB GaN board, showing the input capacitors C_{in}, output capacitors C_{out}, and capacitors for the low-power mode's reconfigured rectifier, C_{LP}.

7.1.2 DSAB with Si Inverter Devices

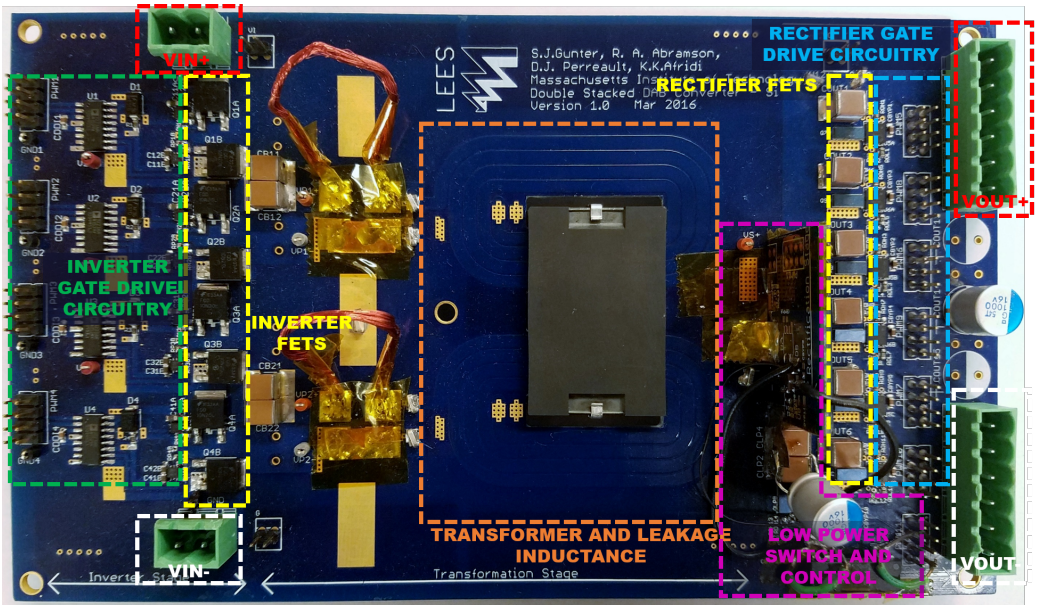


Figure 7-3: Top side of the DSAB board, with Si inverter devices. The inverter and rectifier devices and control circuitry are shown, as well as the single-core magnetic component.

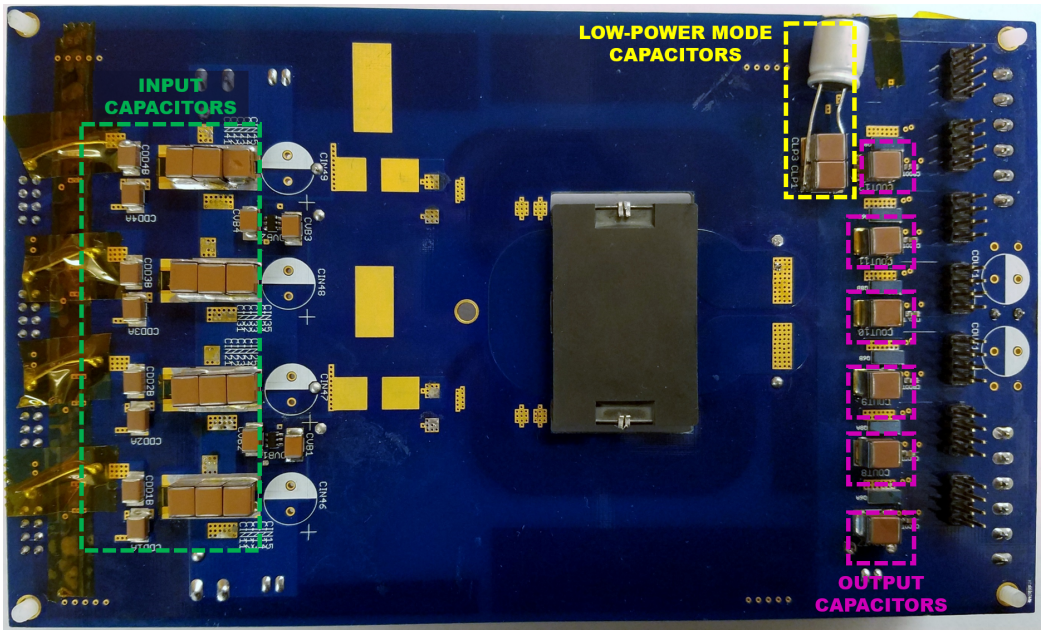


Figure 7-4: Bottom side of the DSAB Si board, showing the input capacitors C_{in}, output capacitors C_{out}, and capacitors for the low-power mode's reconfigured rectifier, C_{LP}.

7.1.3 Single-Stacked DAB with Si Inverter Devices

The Single-Stacked DAB was assembled using the same PCB as the DSAB Si board, as both the FQD10N20L and the IPD50R280CE devices are D-PAK packages. The

DSAB board was converted to a Single-Stack DAB by populating the top-most and bottom-most half-bridges in the double stacked-full-bridge inverter, to create a single-stacked full-bridge inverter, while the two primaries were connected in series with foil, to create one effective primary winding, as shown in Fig. 7-6. Fig. 7-5 shows a schematic illustrating how the DSAB was converted to the Single-Stacked DAB.

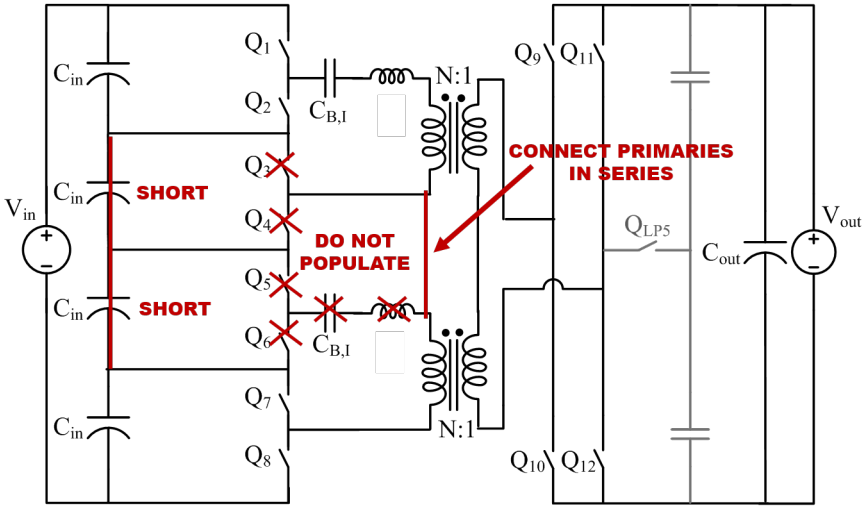


Figure 7-5: Circuit diagram showing how the DSAB topology can be converted to a Single-Stacked DAB topology. Only the top and bottom half-bridges in the inverter are populated. The primaries are connected in series, while the bottom blocking capacitor C_B is left unpopulated. Note that the input capacitors C_{in} and the top blocking capacitor C_B must be increased in voltage rating, as they will now be holding twice the voltage.

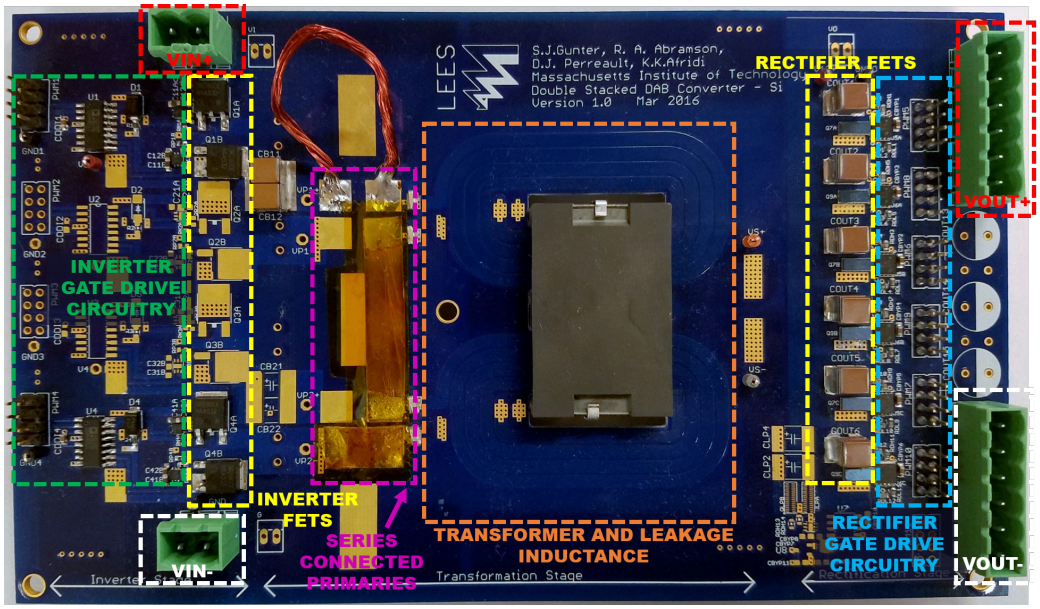


Figure 7-6: Top side of the Single-Stacked DAB board, with Si Superjunction inverter devices. Note that only the top and bottom half-bridges are populated, to create a single-stacked full-bridge inverter. The primaries are also connected in series by a foil sheet to create a single effective primary.

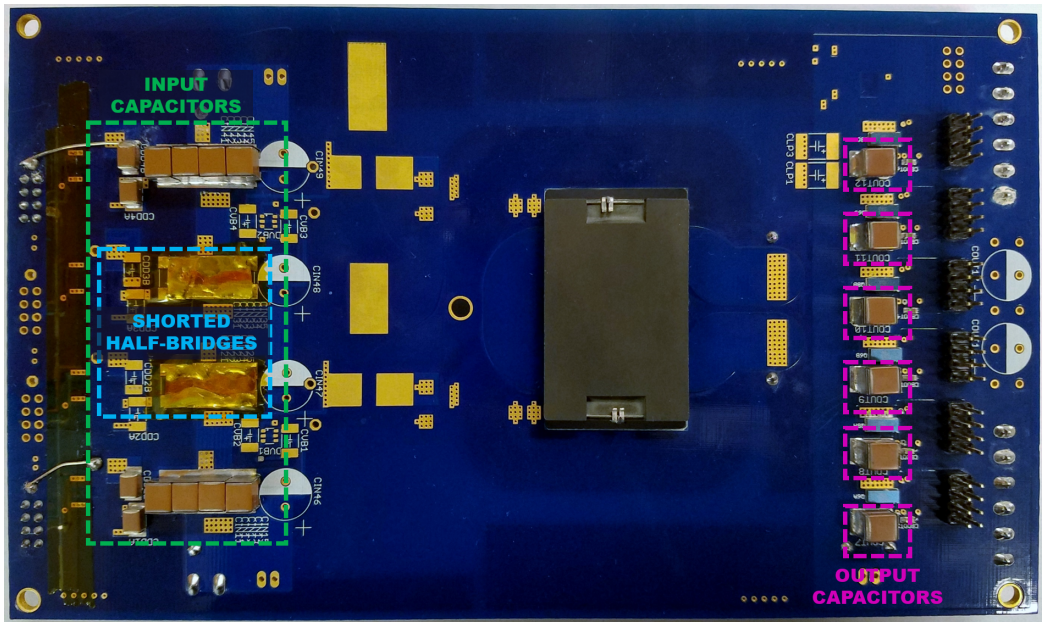


Figure 7-7: Bottom side of the Si Single-Stacked DAB board, showing the input capacitors C_{in} and output capacitors C_{out}. The input capacitors of the two middle half-bridges were also shorted on the backside of the board with foil.The Q_{LP} circuitry is left unpopulated, as the Single-Stacked topology cannot be run in the low-power mode.

Table 7.1 lists the main components used, noting where the various prototype versions differ. Schematics, PCB layouts and Gerber files for each board are included in Appendix C, and Bills-of-Materials are included in Appendix D.

Table 7.1: Prototype Components for All Assembled Boards

Component	Description	Value / Device	
Q_1 - Q_8	Inverter switch	DSAB GaN DSAB Si Single-Stacked DAB Si	EPC2012C FQD10N20L IPD50R280CE
Q_9 - Q_{12}	Rectifier switch	3x EPC2023 (in parallel)	
Q_{LP}	Low-power switch	2x EPC2023, source connected 2 sets in parallel[1]	
N	Transformer turns ratio	16:1	
L	Leakage inductance	32 μH[2], EPCOS EILP43-N49 core 8-layer PCB, 4oz copper internal layers, 2oz copper outer layers	
C_{in}	Input capacitors	DSAB Single-Stacked DAB	3x 3.3 μF 250 V 4x 2.2 μF 450 V all ceramic
C_{out}	Output capacitors	12x 100 μF 16 V ceramic	
C_{LP}	Low-power stacked capacitors[3]	2x 100 μF 16 V ceramic 1x 1000 μF 16 V electrolytic	
C_B	Blocking capacitors	DSAB Single-Stacked DAB	2x 3.3 μF 250 V 2x 2.2 μF 450 V all ceramic

[1] see discussion of the Q_{LP} path resistance effects
[2] total-primary referred leakage inductance
[3] across each switch in the reconfigured half-bridge rectifier

7.2 Experimental Setup

Fig. 7-8 shows the bench setup for testing the prototype boards. The circuit input voltage was provided with a Kepco KLP 600-4 power supply, while a Hewlett Packard 6050A electronic load configured in "voltage-mode" provided a 12 V load. Bench-top multimeters (Agilent 34401A and GWInstek GDM-8341) were used to measure the voltages and currents of the inverter and rectifier gate drive circuitry, in order to measure the gating power. A Yokogawa WT1800 power analyzer was used to

measure the dc input and output voltages and currents for efficiency calculations. An oscilloscope was used to capture waveforms of the converter in various operating regions and modes. The board was fan-cooled, with a 12 V dc-supplied fan running at 9.6 W. The converter gate signals were supplied by an external control board, which was configured through the serial program PuTTY, shown running on the laptop in Fig. 7-8. Table 7.2 gives a more detailed description of the equipment settings.

Fig. 7-9 shows the probe setup for measuring the input and output voltage used in the efficiency calculations. Probes for measuring the gate drive power dissipation are also shown, as are the jumper cables used to supply drive signals for all six of the rectifier half-bridges (each of the switches are actually three paralleled devices). The method used to calculate gating loss is described in Section 7.2.2.

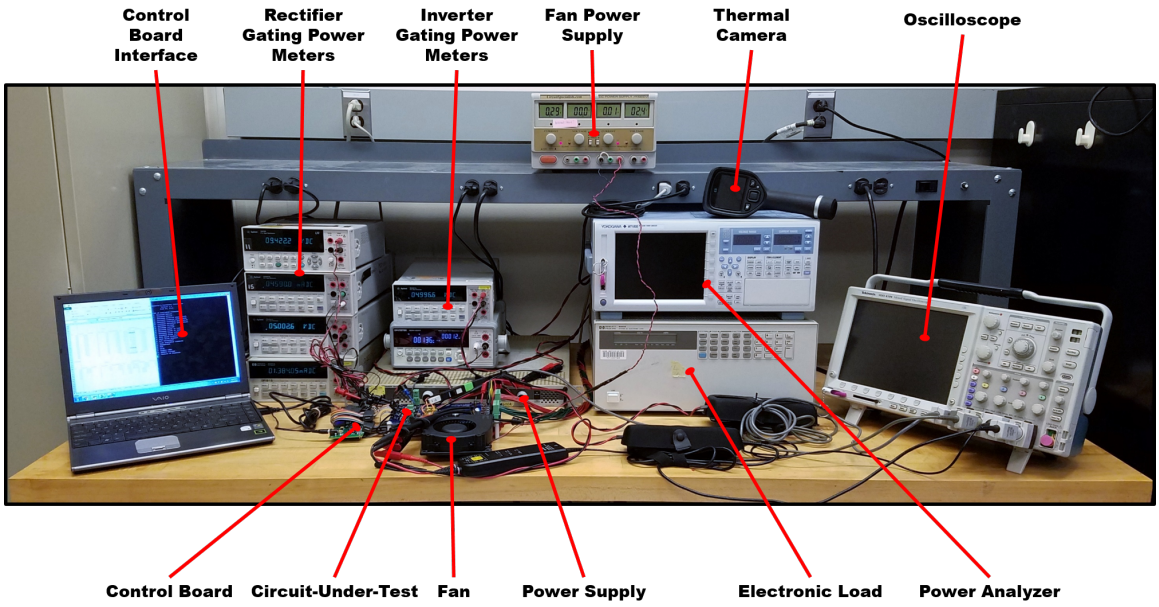


Figure 7-8: Experimental bench setup for testing prototype converters.

Table 7.2: Table of Equipment Used for Experimental Testing

Equipment	Part Number	Settings
Oscilloscope	Tektronix MSO 4054 Mixed Signal Oscilloscope	
Probes	High Voltage Differential Probe Tektronix P5205 100 MHz	500X attenuation
	High Voltage Differential Probe Textronix THDP0200 200 MHz	150 Vpk
	Texktronix TCP202 Current Probe	
Bench-top Multimeters	Agilent 34401A[1] $6\frac{1}{2}$ Digit Multimeter	dc voltage (V)
	Agilent 34401A[2] $6\frac{1}{2}$ Digit Multimeter	dc current (mA)
	GWInstek GDM-8341[3] 50000 Counts Dual Measurement Multimeter	dc current (mA)
Electronic load	Hewlett Packard ELoad 6050A	voltage mode, 12 V
Power Analyzer	Yokogawa WT1800	measuring V_{dc}, I_{dc} on input and output
Power supply	Kepco Inc KLP 600-4 Power Supply	380 V nominal
Fan Power supply	HY3002D-3 DC Power Supply	12 V, 0.8 A
Fan	PMB1212PLB2-A DC12V 9.8 W	12 V, 0.8 A
Thermal Camera	FLIR	FLIR-E63900
Control Board Interface	PuTTY	Serial, 921600 baud rate

[1] for measuring inverter and rectifier gate-drive voltage
[2] for measuring inverter gate-drive current
[3] for measuring rectifier gate-current

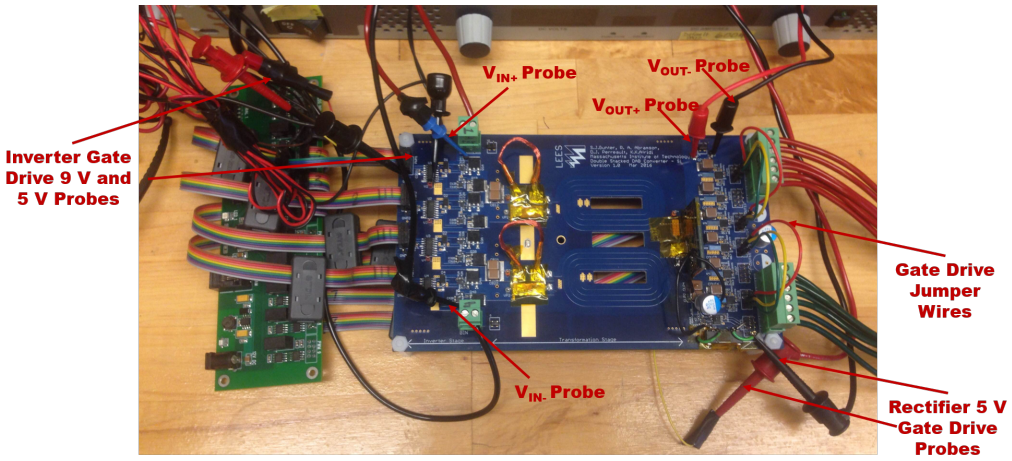


Figure 7-9: Board-Under-Test with probes for measuring input and output voltage, as well as the gate drive voltage and current in order to calculate gating loss.

7.2.1 Control Board

An external control board was used to generate the appropriate gate signals for each converter under test [29]. The control board, shown in Fig. 7-10, is powered by a 12 V dc wall power supply, has nine isolated PWM channels, and is controllable over a serial connection. PuTTY software was used to communicate with the board, and allowed the user to set the PWM frequency/period, duty cycle, deadtime, and phase shift from other PWM signals. The duty cycle, phase shift, and deadtime can be set with 1.04 ns resolution. The control board was also able to generate the necessary gate signals for the low-power mode, and allows the user to switch between the full-power and low-power modes. Fig. 7-11 shows the user interface for the control board, listing the available commands as well as the parameters used for the DSAB converter. The Master Period of 5412 corresponds to a commanded period of 177668 kHz. The Master Duty Cycle 2706 corresponds to a 50% duty cycle for all the gate drive signals. PWM1-PWM4 are the inverter gate drive signals (for each of the four stacked half-bridges), and have a deadtime of $90 \cdot 1.04\text{ns} = 93.6$ ns. PWM5-PWM8 are the rectifier gate drive signals and have a deadtime of $15 \cdot 1.04\text{ns} = 15.6$ ns. Because there are only nine PWM channels, there are not enough to drive all six half-bridges in the rectifier. Therefore, the gate drive signals are jumped over to the last two half-bridge drivers using jumper wires, as shown in Fig. 7-9.

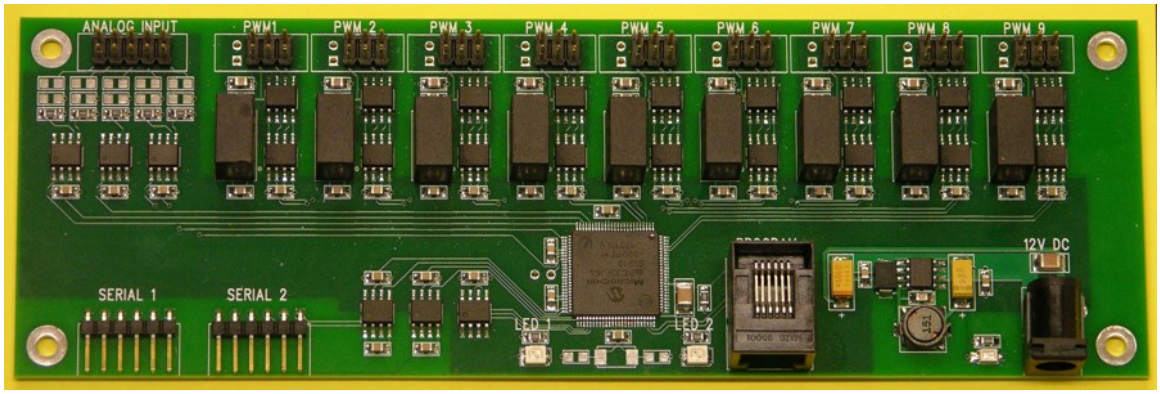


Figure 7-10: Photo of control board, showing the nine PWM channels and their corresponding headers. Ribbon cables are used to connect to the converter under test.

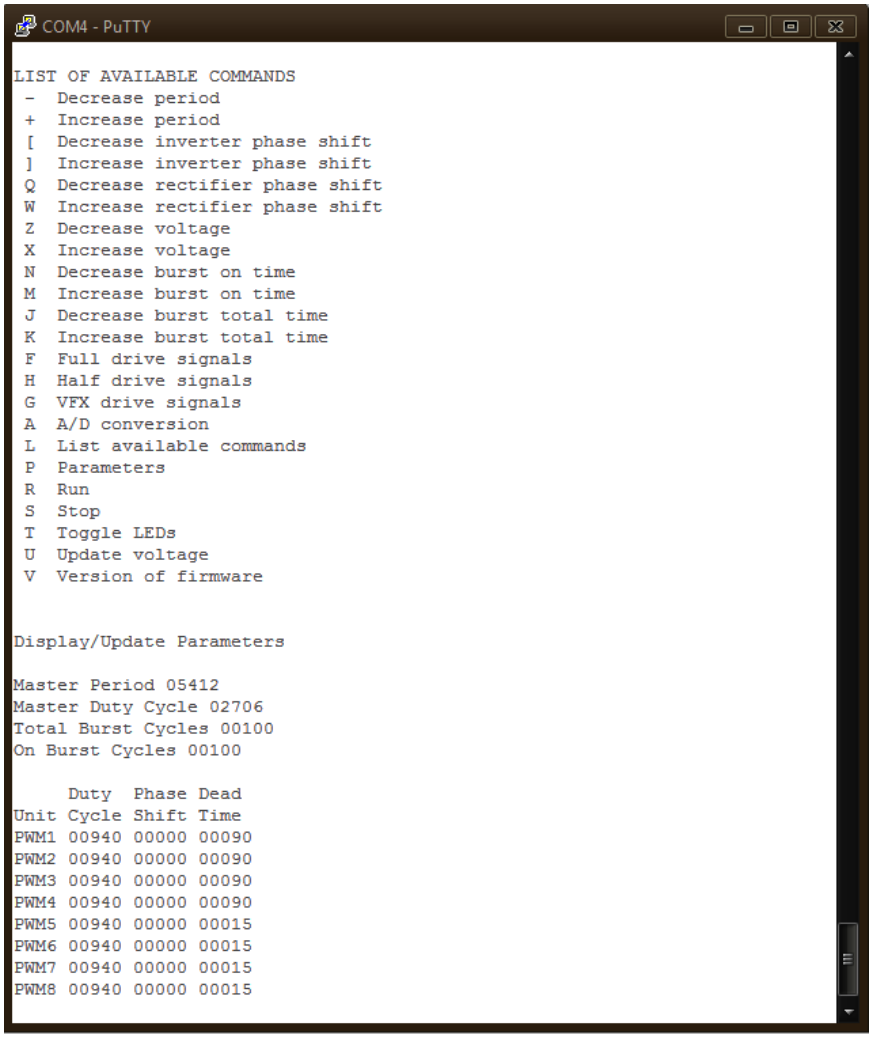


Figure 7-11: Screen capture of the PuTTY terminal program while communicating with the control board. A list of available commands is shown, along with the master parameters used for the converter gate signals, such as period, duty cycle, and deadtime values.

7.2.2 Gate Power Measurement

The gate drive power was measured for the inverter and rectifier switches, and included in the final efficiency calculations. The circuitry for the inverter and rectifier gate drives are shown in Figs. 7-12 and 7-13. The gate signals come from the control board over ribbon cables.

Because the inverter switches are stacked, each one must have an isolated gate drive signal. Therefore, the control signals go through an ADUM3223 signal isolator, and then on to the gate drivers, one for each switch. A bootstrap circuit is used for

the high-side gate drive signal. The isolator is powered from 5 V from the control board ($VDDI$ in the schematic), while an unregulated 9 V is used for the gate-driver power ($VDDB$ in the schematic for the low-side gate driver, and $VDDA$ for the high-side driver, which is referenced to $VDDB$ through a bootstrap circuit). Therefore, to calculate the power dissipation in the inverter circuitry, the power draw from the 5 V and the 9 V buses was measured. This was done by cutting into the ribbon cable and connecting taps to go through a multimeter to measure the current draw, as well as measuring the actual voltage of the 5 V and 9 V buses on the board (with the probes set up as in Fig. 7-9). One half-bridge was measured (in this case, the top-most) on the inverter, and the total inverter gating loss was calculated as four times this for the DSAB topologies, and two times this for the Single-Stacked DAB (as there are only two half-bridges in the single-stacked inverter topology). Eqn (7.1) gives an expression for the total inverter gate loss:

$$\begin{aligned} P_{gating,inv,DSAB} &= 4(V_{5V}I_{5V} + V_{9V}I_{9V}) \\ P_{gating,inv,SSDAB} &= 2(V_{5V}I_{5V} + V_{9V}I_{9V}) \end{aligned} \tag{7.1}$$

where $DSAB$ stands for Double-Stacked Active Bridge and $SSDAB$ stands for Single-Stacked DAB.

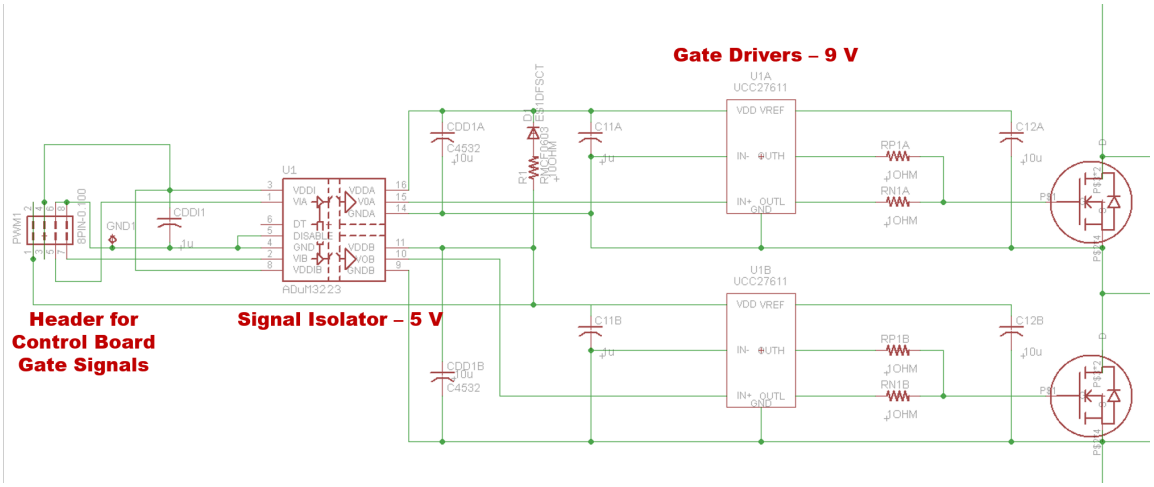


Figure 7-12: Schematic of the inverter gate drive circuitry, showing the header for the control board signals, signal isolator, and gate drivers.

The rectifier devices are not stacked, so there does not need to be extra signal isolation before the gate drive signals go to the gate drivers. Additionally, the gate drivers used drive both the low-side and high-side rectifier devices. As such, all that is needed is the non-inverted gate drive signal from the control board and a 5 V power supply for the gate driver. The gating power was measured in a similar manner using bench-top multimeters to measure the actual voltage at the gate driver as well as cutting into the ribbon cable to measure the current on the 5 V bus. Because the rectifier uses three paralleled devices, there are a total of six half-bridges, each driven with their own half-bridge gate driver. Therefore, the total rectifier gating power is six times that measured on one half-bridge, as expressed in Eqn (7.2).

$$P_{gating,rect} = 6V_{5V}I_{5V} \tag{7.2}$$

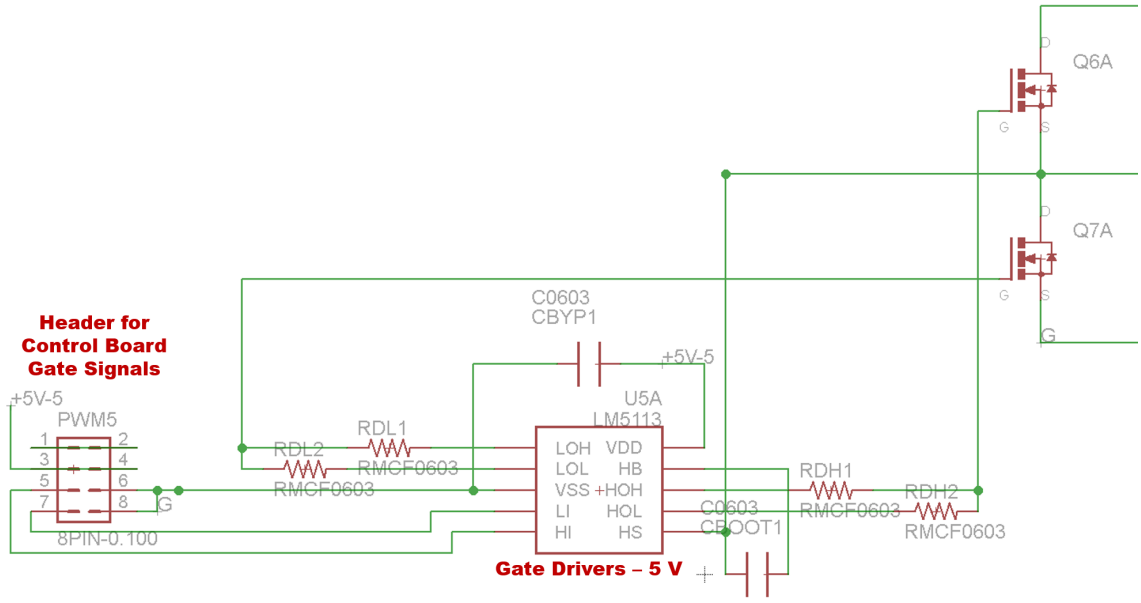


Figure 7-13: Schematic of the rectifier gate drive circuitry, showing the header for the control board signals, and half-bridge gate driver.

The total gating power is then the sum of the total inverter and rectifier gating power, so that $P_{gating,tot} = P_{gating,inv} + P_{gating,rect}$. The efficiency was calculated including this power loss, so that:

$$\eta_{eff} = \frac{P_{out}}{P_{in} + P_{gating,tot}} \tag{7.3}$$

where P_{out} and P_{in} were calculated using the voltage and current values measured by the Yokogawa WT1800 power analyzer.

The gating power over the entire load-range is presented in Section 7.4.1 for the prototypes tested.

7.3 Operating Waveforms

Operating waveforms were taken for each of the prototypes over a wide load range. Oscilloscope screen captures of the primary voltage waveforms, secondary voltage waveform, and primary leakage inductor current waveform are included below, all at the nominal operating point of 380 V in and 12 V out. Both of the DSAB's primaries have the same excitation patterns, and therefore appear one on top of the other in the screen captures, demonstrating good matching between the two stacked inverters.

All of the tested converters were run with 93.6 ns of deadtime on the inverter, and 15.6 ns of deadtime on the rectifier.

7.3.1 DSAB Converter

Fig. 7-14 shows the GaN DSAB converter operating at 300 W (100% load), zoomed out to show several switching periods on the left, and zoomed in to show the inverter switch transition on the right. The top waveform is actually two waveforms, one for each primary and aligned one on top of the other, shown in green and blue. The middle waveform in purple shows the voltage on the secondary, and is phase-shifted from the primary waveforms by a phase shift, ϕ_{300W}. The bottom waveform in blue shows the leakage inductor current. As the waveforms are taken at the nominal input voltage of 380 V, the current waveform is nicely trapezoidal and relatively flat-topped.

The image on the right shows the inverter rising transition zoomed in. As can be seen by the smooth rise of the green curve, the DSAB is able to achieve ZVS at 300

W. Although there is some ringing on the rectifier, it is believed that this is mostly due to probe pickup.

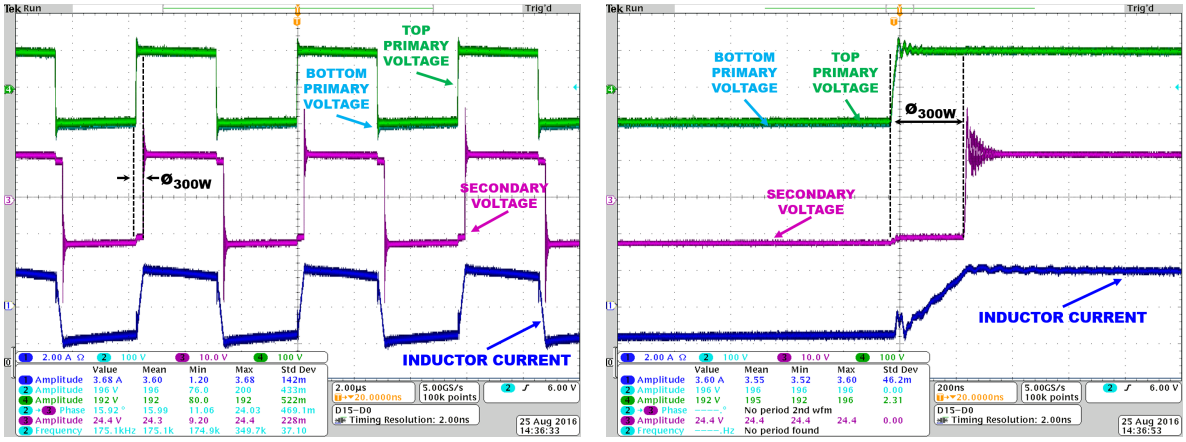


Figure 7-14: Operating waveforms for the GaN DSAB converter operating in full-power mode at 300 W (100% load), for several switching cycles (left) and zoomed in (right). The phase shift between primary and secondary is 17.2°

Fig. 7-15 shows the GaN DSAB converter operating at 150 W (or 50% load). Note that the phase shift has been decreased to achieve the lower output power, and the inductor current has a lower peak value. The inverter waveforms start to show some ringing, signifying that the converter is on the verge of losing ZVS. By the time the converter is operating at 105 W (or 35% load), as shown in Fig. 7-16, the converter is hard-switching in that the top transistor turns on under a significant voltage. The effects of this can be seen in the large amount of ringing on the inverter primary waveforms and the current waveform.

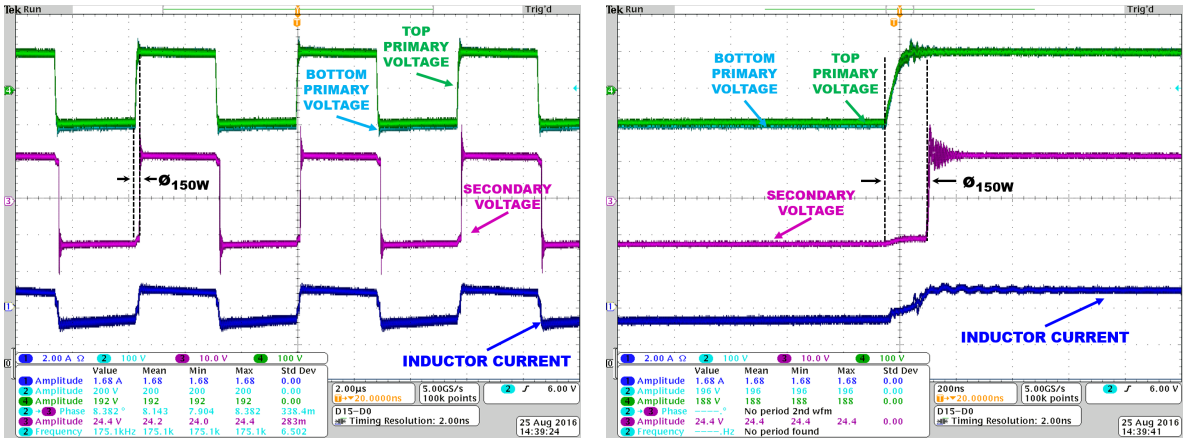


Figure 7-15: Operating waveforms for the GaN DSAB converter operating in full-power mode at 150 W (50% load), for several switching cycles (left) and zoomed in (right). The phase shift between primary and secondary is 10.2°

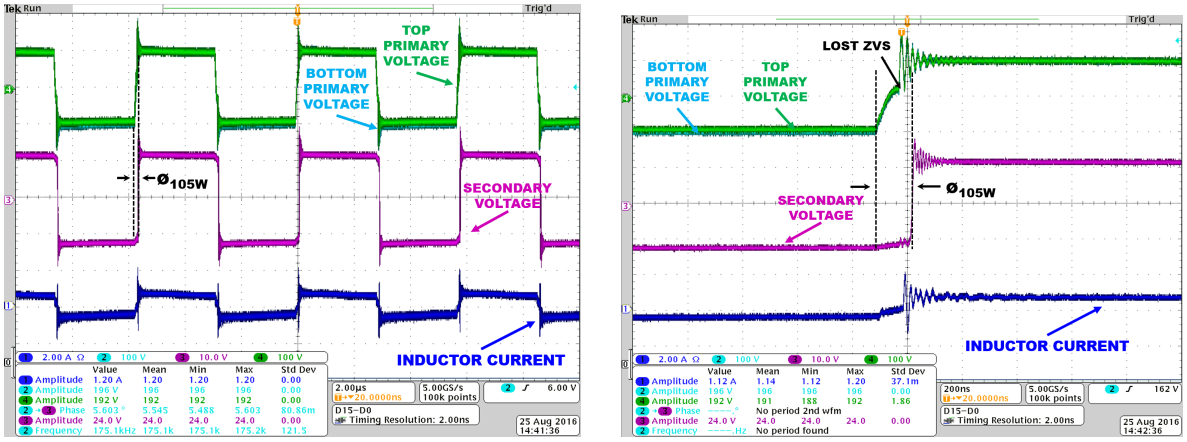


Figure 7-16: Operating waveforms for the GaN DSAB converter operating in full-power mode at 105 W (35% load), for several switching cycles (left) and zoomed in (right). The converter has lost full ZVS, and is hard-switching for part of the switch transition. The phase shift between primary and secondary is 8.8°

Low-Power Mode

As described previously, the DSAB is able to operate in a low-power mode that greatly increases efficiency at low loads, and allows the converter to achieve ZVS over a wide power range. Operating waveforms for the low-power mode of the GaN DSAB converter are shown below. Fig. 7-17 shows a comparison of the converter waveforms operating at 75 W for the full-power mode (left) and the low-power mode (right). In the low-power mode, the primaries are alternately driven in square mode and held at zero voltage. Additionally, the rectifier is configured to operate as a half-bridge (voltage-doubler), so that the peak secondary voltage is now 6 V, as opposed to 12 V in the full-power mode. A benefit of the low-power mode is the increased current relative to that in the full-power mode, especially at the switch transitions, such that ZVS is more easily realized. $\phi_{75W,LP}$ is larger than $\phi_{75W,FP}$, so the inductor current is allowed to ramp longer, and therefore reaches a higher peak value.

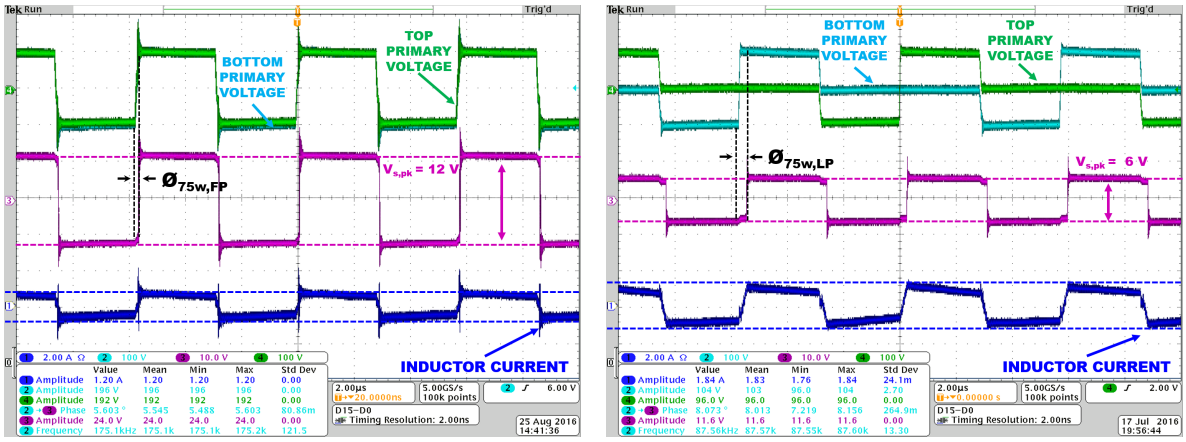


Figure 7-17: GaN DSAB converter operating in full-power mode (left) at a phase shift of 8.1° and low-power mode (right) at a phase shift of 18.0°, both at 75 W.

Fig. 7-18 shows the full-power mode primary voltage transition zoomed in. The turn-on transition is hard-switched, with the transistor turning on under substantial voltage, as the current available for a soft transition of the device capacitor voltage is very low.

Fig. 7-19 shows the zoomed-in rise and fall transitions on the primary voltage waveforms in the low-power mode. As mentioned in Chapter 6, the transition where

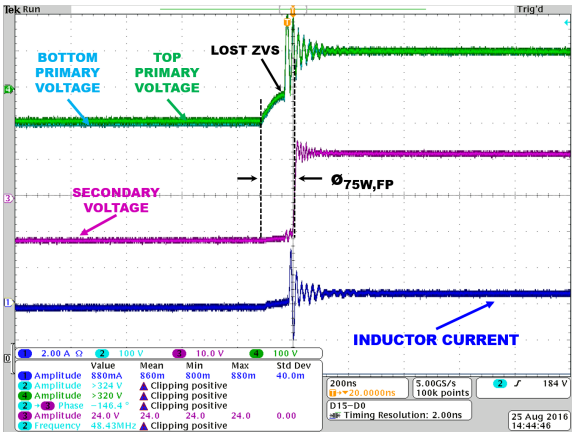


Figure 7-18: GaN DSAB converter operating in full-power mode at 75 W, zoomed in on the primary voltage transition.

the primary voltage changes from negative to positive can maintain ZVS for a wider load range than for a transition from positive to 0 V or 0 V to negative. At 75 W, the rising transition has full ZVS, while the falling transition is starting to lose ZVS.

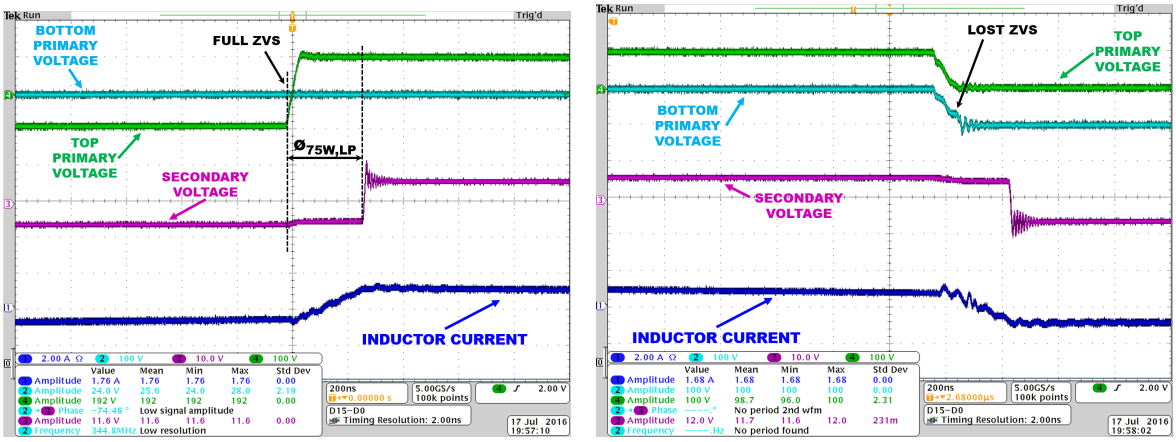


Figure 7-19: GaN DSAB converter operating in low-power mode at 75 W, zoomed in on the rising transition on the primary waveforms (left) and the falling transition on the primary waveforms (right). The falling transition is starting to lose ZVS.

The same waveforms are shown at 38 W in 7-20. The falling transition has a significant amount of hard-switching at this low power level, while the rising transition is just starting to show some ringing on the primary waveform. The Si DSAB converter operating in low-power mode also has similar operating waveforms at these power levels, but oscilloscope captures of its operation are not presented here.

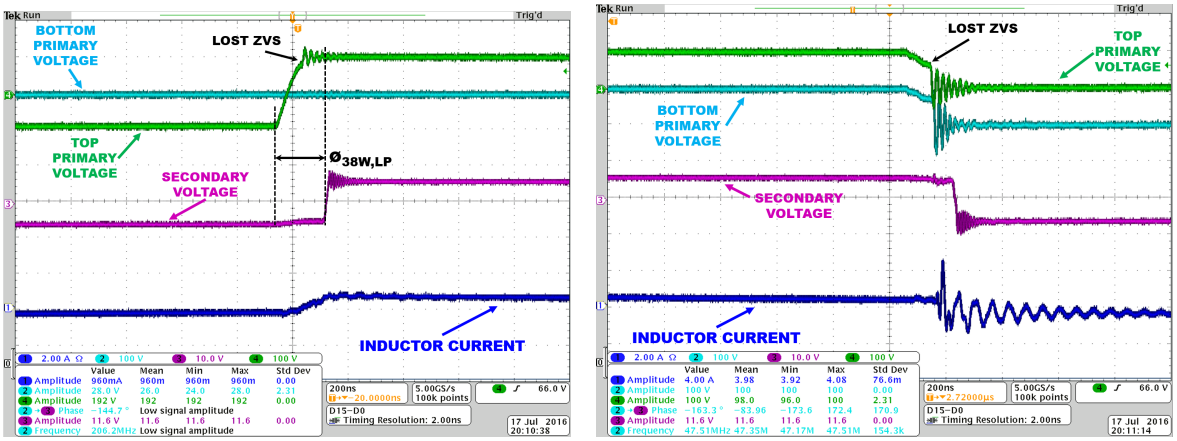


Figure 7-20: GaN DSAB converter operating in low-power mode at 38 W, zoomed in on the rising transition on the primary waveforms (left) and the falling transition on the primary waveforms (right). The rising transition is just starting experiences a small amount ringing, while the falling transition is already hard-switching for a significant portion of the transition.

The low-power mode can still achieve partial ZVS down to very low powers, compared to the full-power mode (i.e., significantly reduced turn-on loss owing to a relatively low voltage across the incoming transistor at turn-on). Fig. 7-21 shows the GaN DSAB converter operating in full-power mode at 30 W (left), and operating in the low-power mode at 28 W (middle and right). The full-power mode has almost no ZVS on the transition, while the low-power can provide a resonant transition of more than 50% of the total switch voltage on the rising transition, and around 50% on the falling transition.

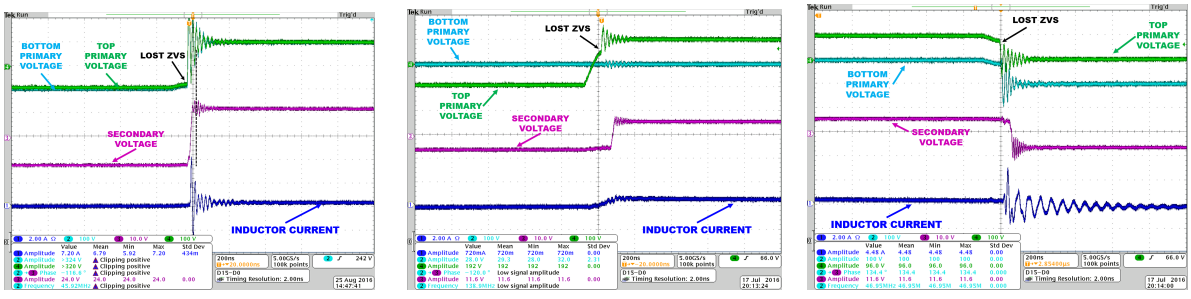


Figure 7-21: GaN DSAB operating in the full-power mode at 30 W (left) and operating in the low-power mode at 28 W (middle and right). The rising and falling transitions are individually zoomed in for the low-power waveforms.

Full-Power Mode		Low-Power Mode	
P_{out} (W)	ϕ_{exp} (deg)	P_{out} (W)	ϕ_{exp} (deg)
300 W	17.2°		
150 W	10.2°		
104 W	8.8°		
75 W	8.1°	75 W	18.0°
30 W	6.7°	28 W	9.8°

Table 7.3: GaN DSAB phase shifts for various output powers

Table 7.3 lists the experimental phase shifts for the above operating points. Note that the phase shift at 75 W for the low-power mode is close to the phase shift at 300 W for the full-power mode, as the low-power mode naturally delivers a quarter of the rated power for the same phase shift.

Full-Power Mode		Low-Power Mode	
P_{out} (W)	ϕ_{exp} (deg)	P_{out} (W)	ϕ_{exp} (deg)
300 W	18.1°		
75 W	8.6°	79 W	20.0°
		70 W	18.1°
30 W	7.1°	30 W	10.9°

Table 7.4: Si DSAB phase shifts for various output powers

7.3.2 Single-Stacked DAB

A Single-Stacked DAB converter was also tested over a wide load range. Fig. 7-22 shows the operating waveforms for the converter at 300W, at the nominal input voltage of 380 V. The total primary voltage, across the two series-connected primaries, is shown in green, and swings from -190 V to 190 V, double the swing of each primary in the DSAB converter. The voltage of one of the two series-connected primaries (forming a single effective primary) is shown in blue. As can be seen from the waveform, there is some ripple in this primary voltage. However, when the two primary voltages are added, or the voltage across the entire effective primary is measured, the resulting waveform is a very sharp-edged square-wave (as shown in green). This suggests that the individual primary voltages may be somewhat unmatched for this version of the Single-Stacked DAB, as the magnetic structure places a constraint on the sum of the

primary voltages with relation to the secondary voltage and turns ratio, rather than a constraint on each individual primary voltage.

The rectifier is again operated as a full-bridge rectifier as in the DSAB full-power mode (note that the scaling of the rectifier voltage is different than that in the screen captures for the DSAB converter). The inductor current is also of a similar value to the DSAB converter at 300 W (the scaling is the same as that of the screen captures for the DSAB converter). The converter is operated at a phase shift of $\phi = 21.3°$ which is larger than the phase shift required for either the GaN or the Si DSAB at 300 W. A larger phase shift implies higher RMS currents, which can add to conduction losses.

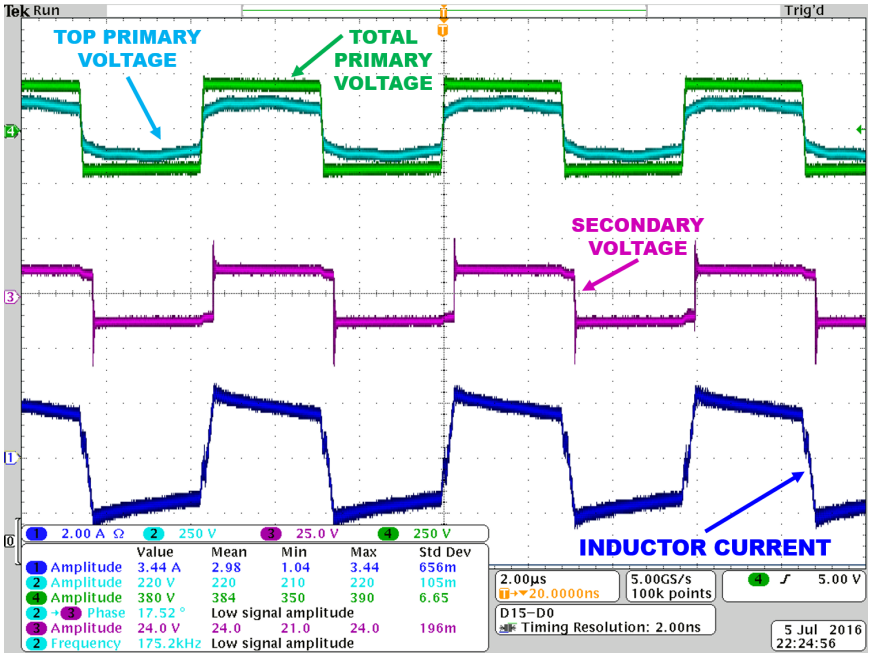


Figure 7-22: Single-Stacked DAB operating waveforms at 300 W

7.3.3 ZVS Performance of Prototypes

Oscilloscope captures were taken of the inverter device V_{ds} and V_{gs} waveforms for the Si and GaN DSAB converter and the Si Single-Stacked DAB converter in order to investigate the ZVS range of each prototype. Note that the gate signals for the DSAB converters were taken at the input to the gate driver, which has a propagation delay

of 10-14 ns. The prototypes' waveforms are presented at several important output power levels.

P_{out} = 300 W, 100% Load

Fig. 7-23 shows the inverter device V_{ds} and V_{gs} waveforms for the Single-Stacked DAB converter operating at 300 W. As shown by the sudden sharp transition on the V_{ds} waveforms, once the second switch turns on, the Si Single Stacked DAB prototype is not able to achieve full ZVS, even at 300 W. The GaN DSAB prototype, shown in Fig. 7-24, is able to achieve ZVS. (Although the V_{ds} waveforms for the GaN DSAB prototype have some ripple on them, one can tell that the inverter devices are in fact achieving ZVS by noting that the switching transition occurs well before the end of the deadtime. We suspect the ripple / ringing on the wave forms is due to some parasitic inductance from the probes). Also, note that the phase shift required for the Single-Stacked DAB converter is higher than that required for the GaN DSAB converter, which implies higher RMS currents and higher conduction loss, in addition to the higher switching loss due to the loss of ZVS.

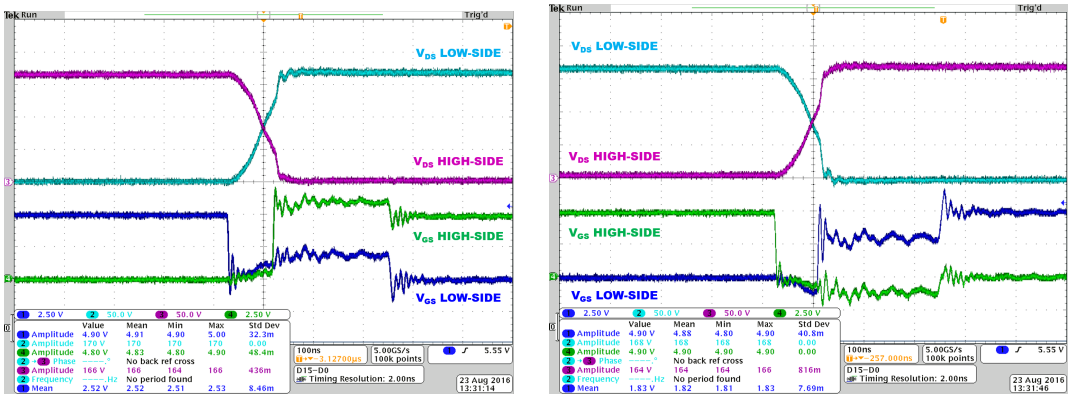


Figure 7-23: Single-Stacked DAB V_{ds} and V_{gs} waveforms for an inverter half-bridge, at 300 W. Turn on and turn off transitions are shown for each device. The phase shift is 21.2°. (Note that the V_{gs} waveforms are at a different scale than those in the GaN DSAB waveforms).

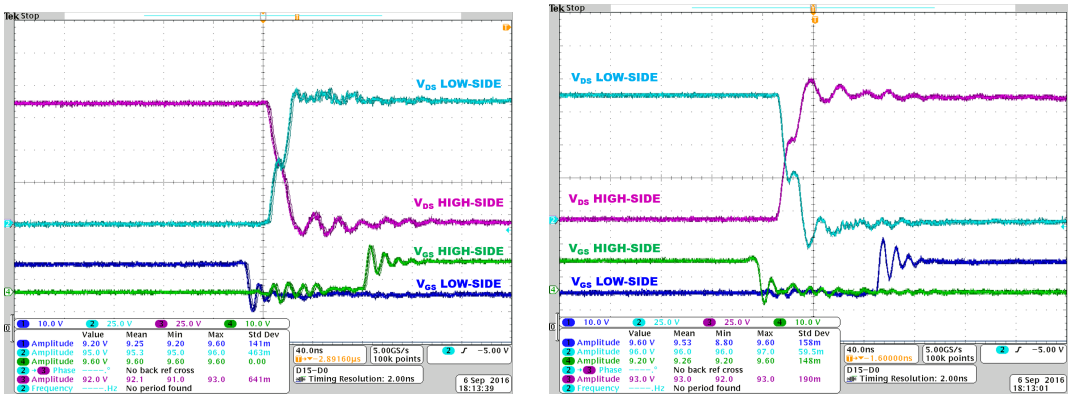


Figure 7-24: GaN DSAB V_{ds} and V_{gs} waveforms for an inverter half-bridge, at 300 W. Turn on and turn off transitions are shown for each device. The phase shift is 17.1°.

P_{out} = 150 W, 50% Load

At 150 W or 50% load, the Single-Stacked DAB converter can only provide a "soft" resonant transition for a very small portion of the switch voltage transition (shown in Fig. 7-25). this is in contrast to the GaN DSAB converter, which is only just beginning to lose ZVS at this power level.

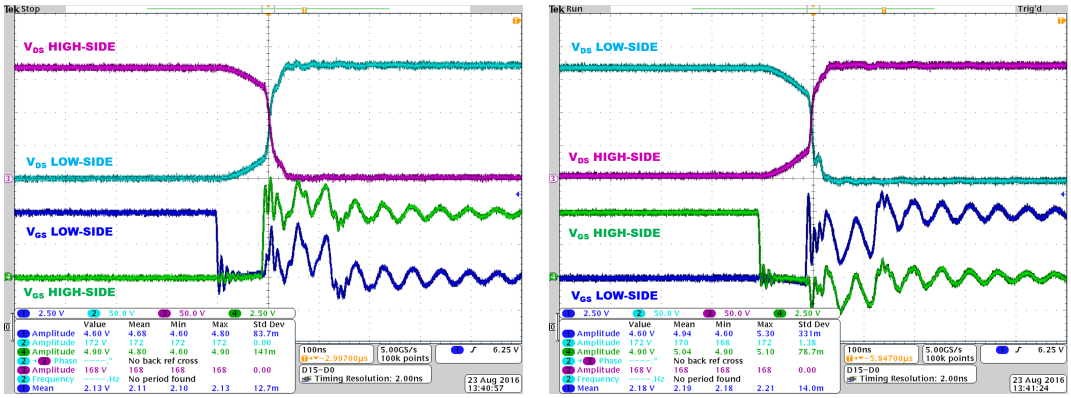


Figure 7-25: Single-Stacked DAB V_{ds} and V_{gs} waveforms for an inverter half-bridge, at 150 W. The switches are hard-switched for most of the switch transition. The phase shift is 14.7°.

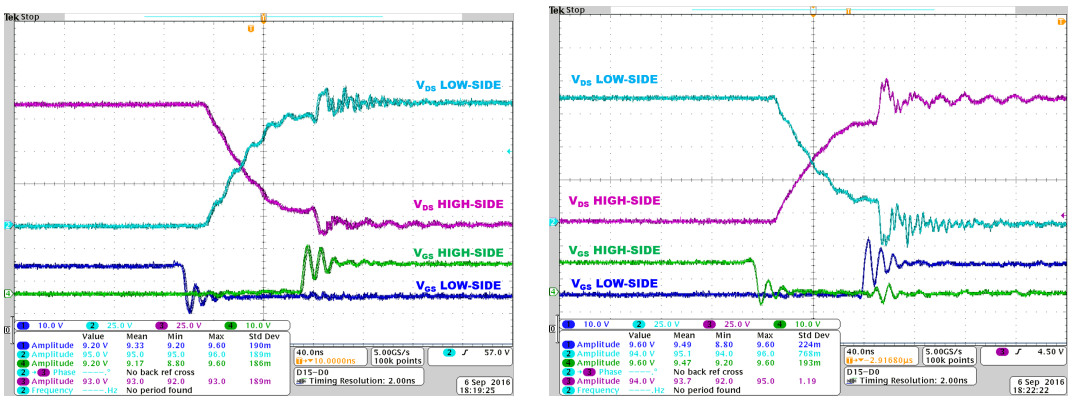


Figure 7-26: GaN DSAB V_{ds} and V_{gs} waveforms for an inverter half-bridge, at 150 W, where the converter starts to lose ZVS. The phase shift is 10.0°.

P_{out} 75 W, 25% Load (Quarter-Power)

Another interesting power level to compare is at 75 W, where the DSAB converter ideally switches operation from the full-power mode to the low-power mode. Fig. 7-27 shows the V_{ds} and V_{gs} waveforms for the GaN DSAB converter operating in the full-power mode at 75 W. As can be seen in the figure, the switches are hard-switched for a significant portion of the switch transition. This is in contrast to the GaN DSAB converter operating in the low-power mode at 75 W, shown in Fig. 7-28, which can fully soft-switch the devices in one transition, and almost completely soft-switch the devices in the other transition.

As discussed in Chapter 3, different transitions in the low-power mode can lose ZVS at different times; specifically the high-side device turn-on and low-side device turn off (shown on the left in Fig. 7-28) has just barely lost ZVS at 75 W, while the high-side device turn-off and low-side device turn-on (shown on the right in Fig. 7-28), easily achieves ZVS.

Fig. 7-29 shows where the switching transition on the left of Fig. 7-28 first loses ZVS, which occurs at 87 W. However, the other transition easily achieves ZVS at this power. Fig. 7-30 shows where this transition eventually loses ZVS, which occurs at 52 W. By this point, the transition on the left is hard-switching a significant portion of the switch voltage transition.

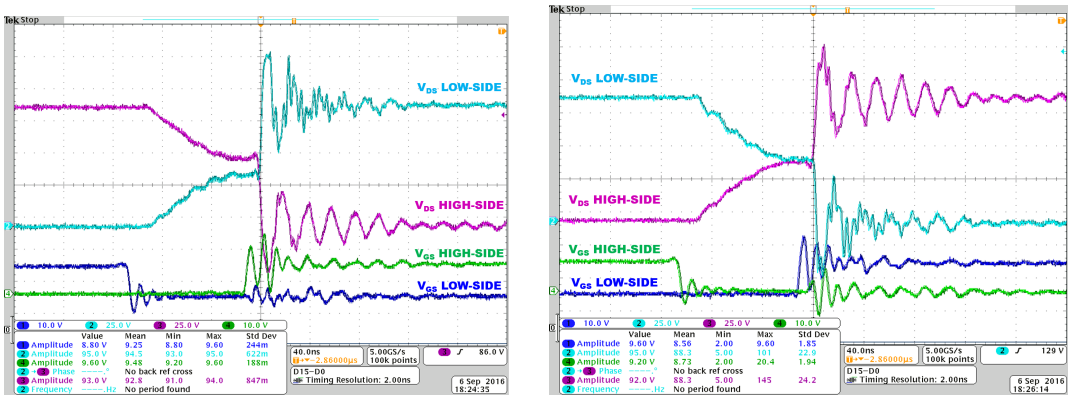


Figure 7-27: V_{ds} and V_{gs} waveforms for an inverter half-bridge in the GaN DSAB converter operating in full-power mode, at 75 W. The switches are hard-switched for most of the switch transition. The phase shift is 8.0°.

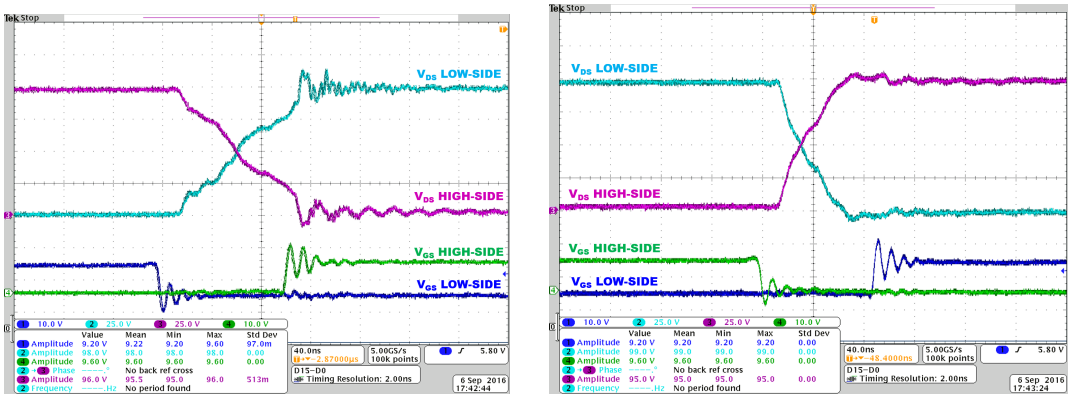


Figure 7-28: V_{ds} and V_{gs} waveforms for an inverter half-bridge in the GaN DSAB converter operating in low-power mode, at 75 W. The switching transition on the left has partially lost ZVS, while the switching transition on the right easily achieves ZVS. The phase shift is 18.3°.

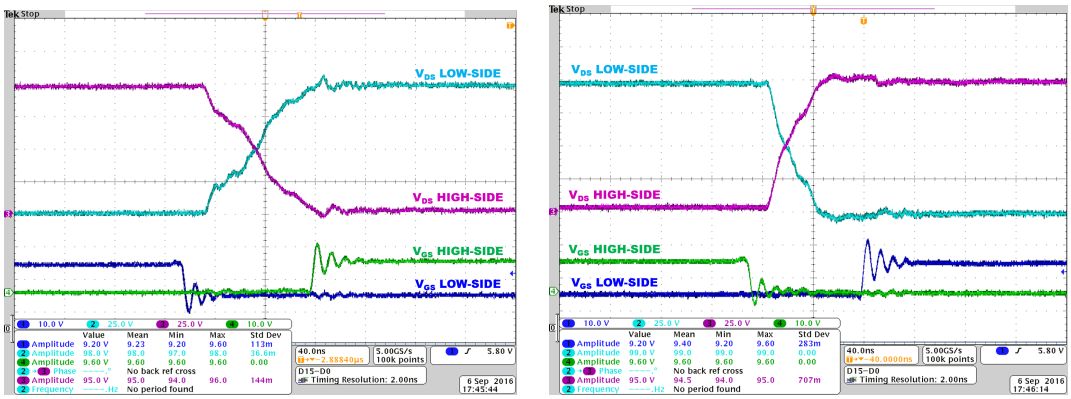


Figure 7-29: V_{ds} and V_{gs} waveforms for an inverter half-bridge in the GaN DSAB converter operating in low-power mode, at 87 W. The switching transition on the left has just barely lost ZVS, while the switching transition on the right easily achieves ZVS. The phase shift is 20.9°.

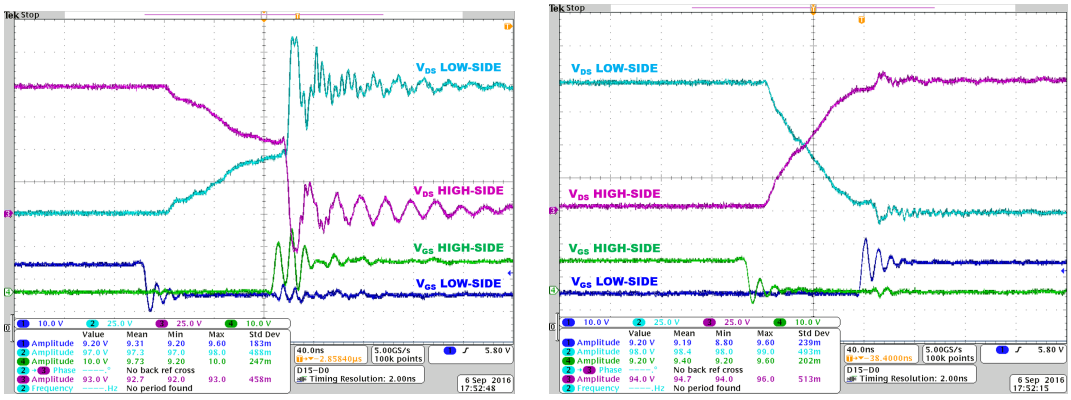


Figure 7-30: V_{ds} and V_{gs} waveforms for an inverter half-bridge in the GaN DSAB converter operating in low-power mode, at 52 W. The phase shift is 14.4°. The switching transition on the left has a significant amount of hard-switching, while transition on the right has just lost ZVS.

P_{out} = 30 W, 10% Load

ZVS waveforms were also taken at 30 W, or 10% load. At this operating point, all prototypes have lost ZVS. However, the GaN low-power mode is able to achieve a "soft" transition for a much larger portion of the switch voltage transition, compared to the full-power mode. Fig. 7-31 shows the V_{ds} and V_{gs} waveforms for the GaN DSAB converter operating in full-power mode at 30 W. The switches are not able to be achieve much of a soft transition on the switch voltages, and the devices are hard-switched for a majority of the switch voltage transition. However, as shown in Fig. 7-32, the GaN DSAB converter is able to softly transition a significant portion of the switch voltage, which helps to reduce switching loss overall.

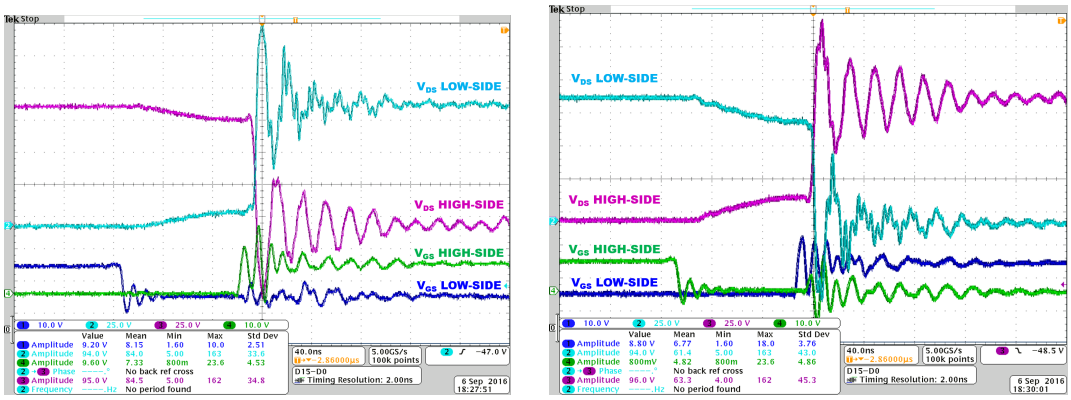


Figure 7-31: GaN DSAB in full-power mode V_{ds} and V_{gs} waveforms for an inverter half-bridge, at 30 W. Turn on and turn off transitions are shown for each device. The switches are hard-switched for most of the switch transition. The phase shift is 6.7°.

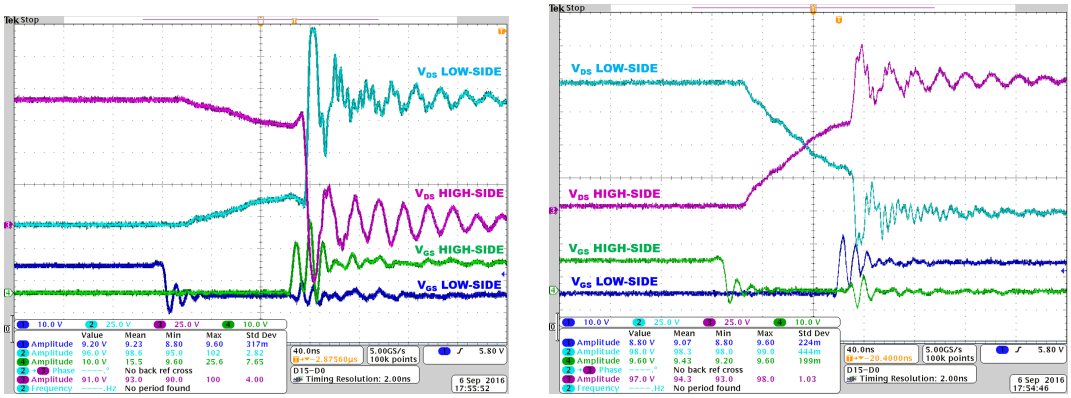


Figure 7-32: GaN DSAB in low-power mode V_{ds} and V_{gs} waveforms for an inverter half-bridge, at 30 W. Turn on and turn off transitions are shown for each device. The switches are hard-switched for most of the switch transition. The phase shift is 10.3°.

7.4 Efficiency Curves

Fig. 7-33 shows experimental efficiency curves for all prototype boards and configurations. The DSAB converter shows much better efficiency than the Single-Stacked DAB, more so than in simulation. The Single-Stacked DAB has similar efficiencies to the DSAB designs above 225 W, but below that begins to dramatically drop in efficiency.

The experimental curves for the low-power mode in the DSAB also show better efficiency than the full-power mode, intersecting the full-power curves around 75 W (as opposed to the 100 W observed in simulation).

Fig. 7-34 shows the same experimental data, zoomed in to the 90-100% efficiency range. As can be seen here, the GaN DSAB prototype was able to achieve a higher efficiency than the Si DSAB prototype at high powers, and significantly higher efficiency than the Si Single-Stacked DAB prototype, especially at low powers. In addition, the low-power mode allows the DSAB converter to maintain greater than 90% efficiency down to a lower power than the full-power mode (and down to a much lower power than the Single-Stacked DAB converter).

Figs. 7-35 and 7-36 show the efficiency and percent loss for the Si DSAB (using 200 V vertical Si devices) and the Si Single-Stacked DAB (using 550 V Si Superjunction devices). The DSAB shows significant improvement over the Single-Stacked DAB

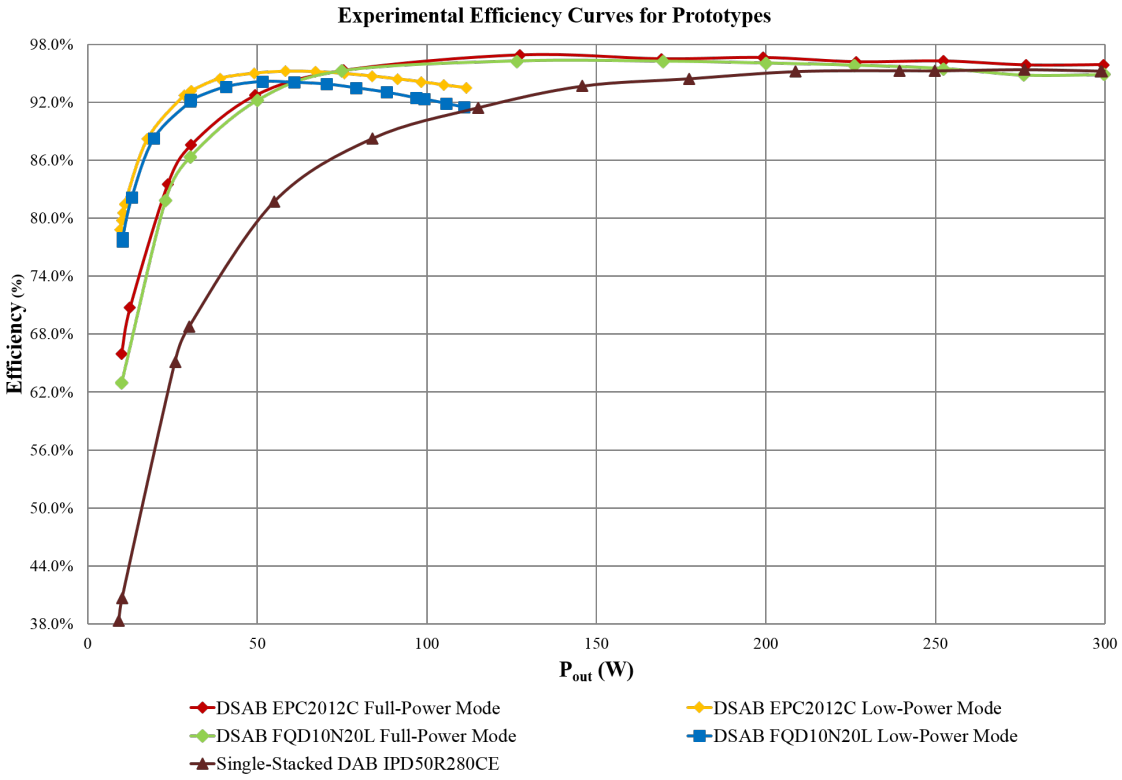


Figure 7-33: Experimental efficiency curves for all topologies and devices tested. The GaN DSAB converter had the best efficiency performance over the entire load-range.

below about two thirds of full load. The DSAB has ∼10% (of input power) lower loss below a quarter power, and at 10 W (3.3% load) has 22% (of input power) lower loss.

Another advantage of the DSAB is its ability to run in a low-power mode, as the two inverters can be run in alternating switch patterns to minimize core and switching loss. The Single-Stacked DAB does not have this ability, as it only has a single inverter driving a single primary winding. Figs. 7-37 and 7-38 show the efficiency and percent loss curves for the DSAB with GaN devices operating in the full-power and low-power modes. The low-power mode is especially beneficial below a quarter power, or 75 W. Between 50 W to 10 W, the low-power mode saves on average 5-6% (of input power) loss. At 10 W, the low-power mode has 14.5% (of input power) less loss than the full-power mode, on top of the gains already added due to the DSAB topology itself.

Finally, the DSAB converter used GaN inverter devices to further optimize effi-

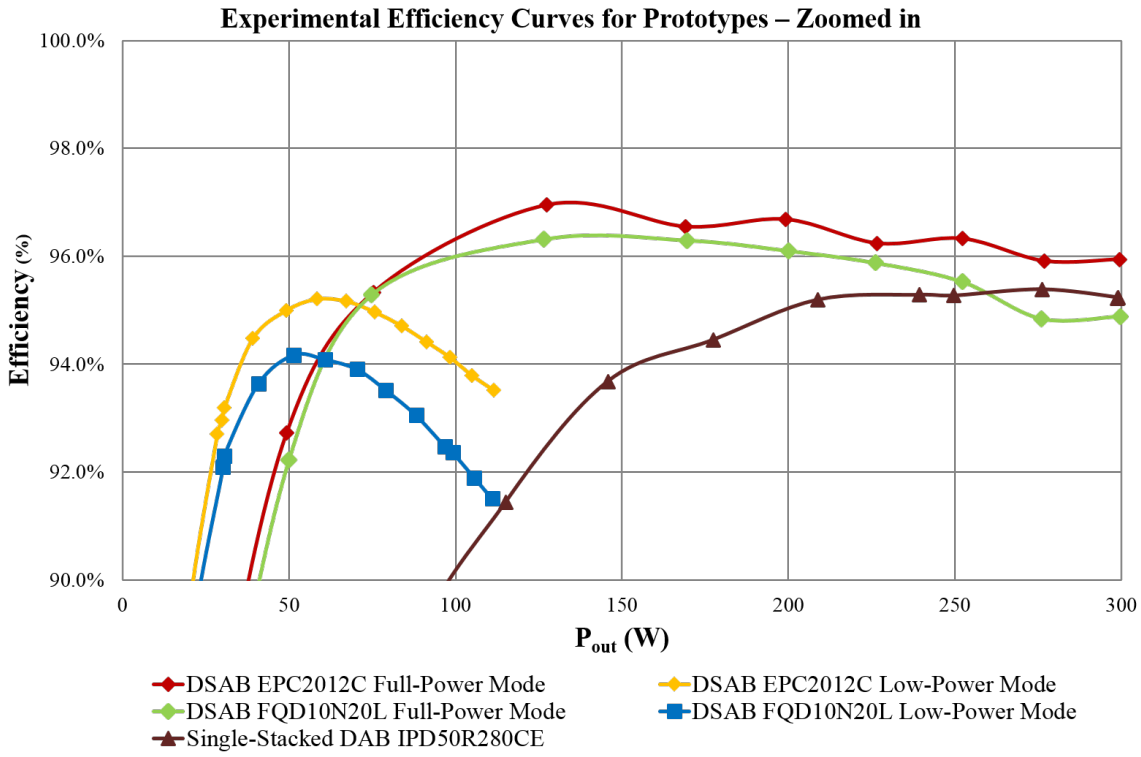


Figure 7-34: Experimental efficiency curves for all topologies and devices tested, zoomed in to the 90-100% efficiency range.

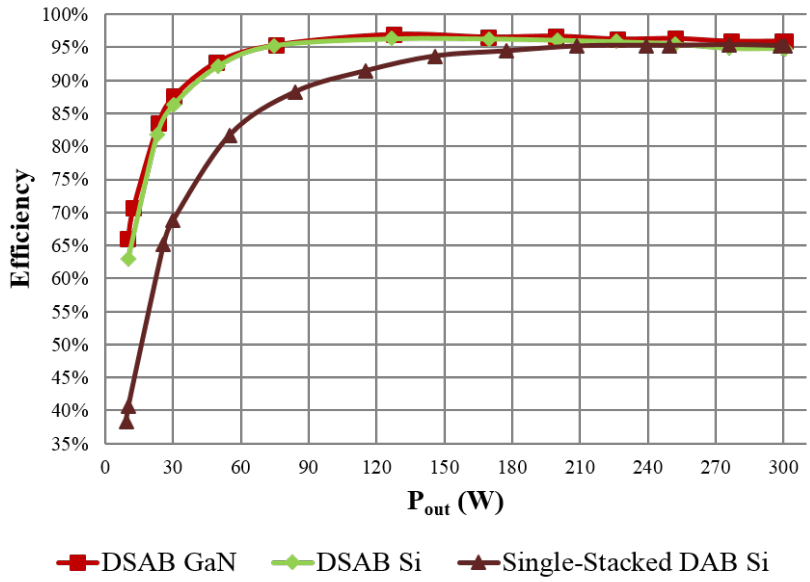


Figure 7-35: Experimental efficiency curves for the Si DSAB and Single-Stacked DAB converters. While both converters have similar efficiencies at high powers, the Single-Stacked DAB's efficiency starts to drop around 200 W.

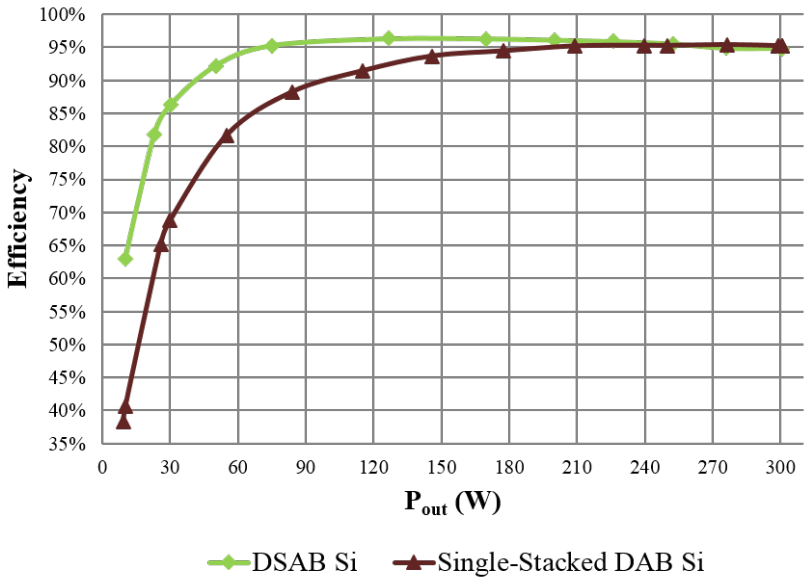


Figure 7-36: Experimental percent loss curves for the Si DSAB and Single-Stacked DAB converters. The DSAB converter has significantly lower percent loss at low powers (below 100 W).

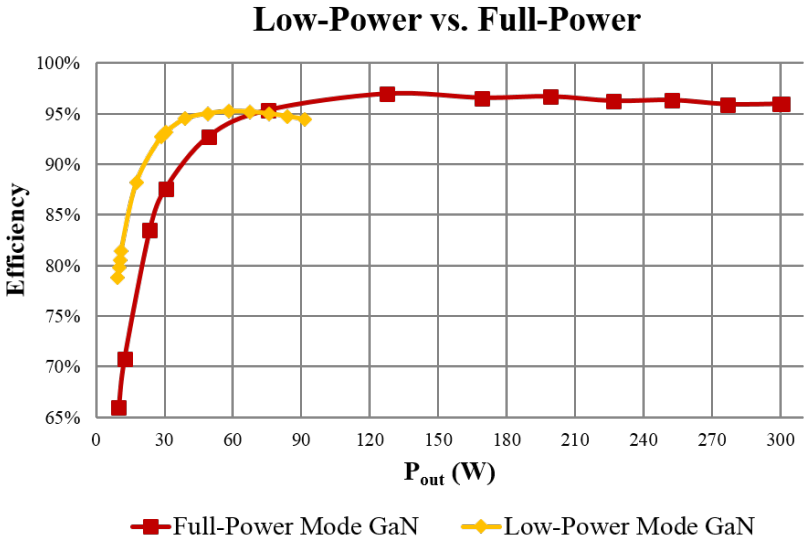


Figure 7-37: Experimental efficiency curves for the GaN DSAB converter operating in full-power mode and low-power mode. The low-power mode is designed for operation at a quarter of the rated power and below.

ciency. As the GaN and Si devices used in the DSAB prototypes had similar C_{oss}, the main benefits come from the GaN devices' lower $R_{ds,on}$, and therefore the efficiency differences are more pronounced at high power. Figs. 7-39 and 7-40 show the

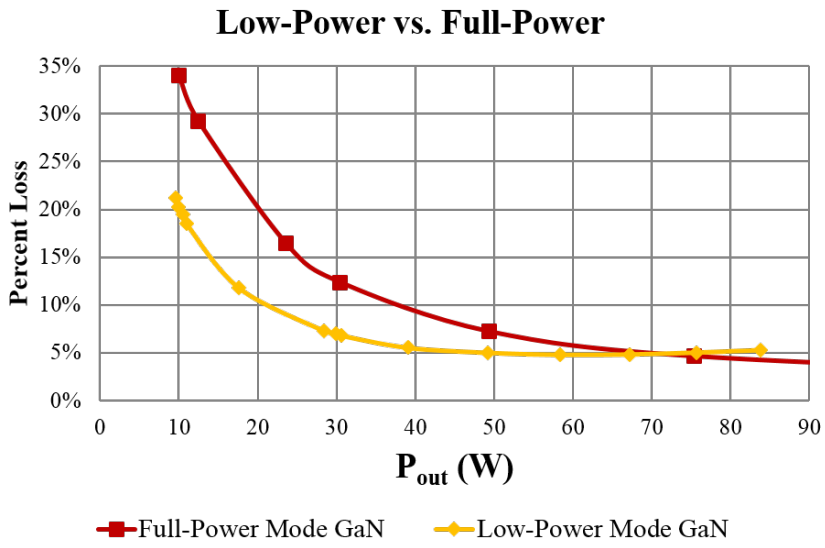


Figure 7-38: Experimental percent loss curves for the GaN DSAB converter operating in full-power mode and low-power mode. The low-power mode has significantly lower percent loss over its operating range compared to the full-power-mode.

efficiency and percent loss curves for the DSAB operating with GaN and Si inverter devices. Fig. 7-40 shows a 0.8-1.2% lower percent of input power loss for the GaN board from 85% load to 100% load.

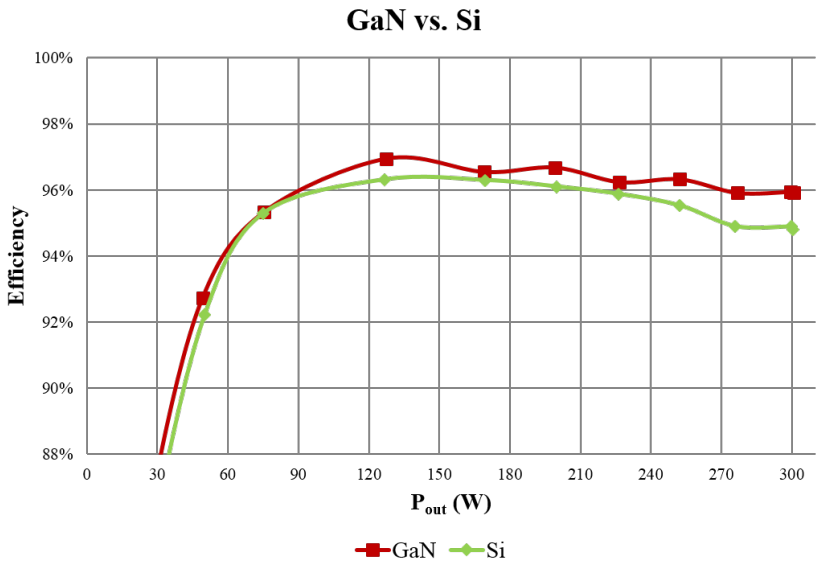


Figure 7-39: Experimental efficiency curves for the GaN and Si DSAB converters. The GaN DSAB converter has higher efficiency, especially at high powers where the lower $R_{ds,on}$ of the GaN devices helps with conduction losses.

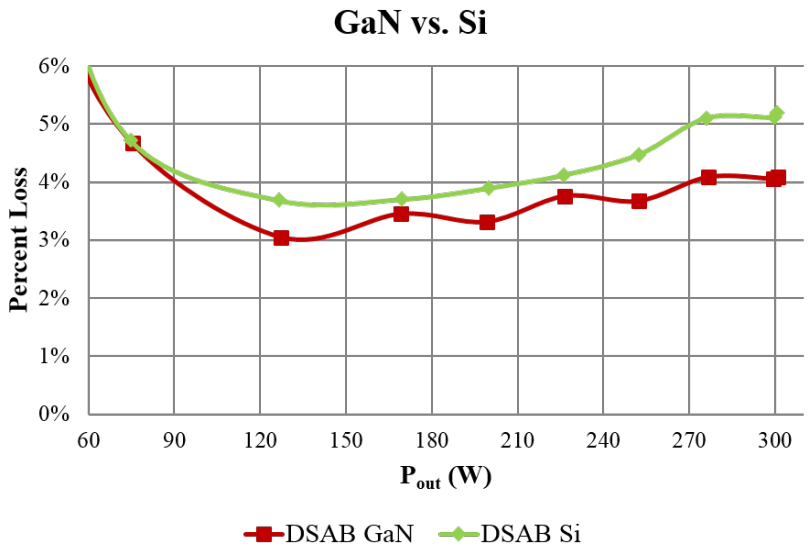


Figure 7-40: Experimental percent loss curves for the GaN and Si DSAB converters.

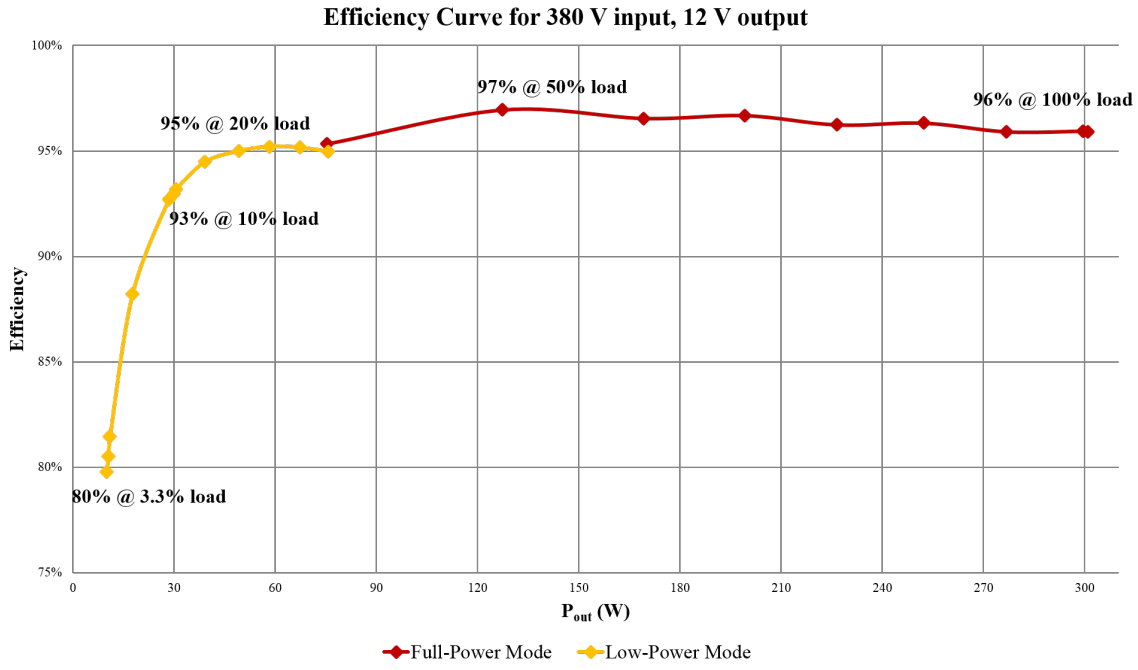


Figure 7-41: Efficiency curve for the DSAB converter using GaN devices and operating in the low-power mode for loads below 75 W.

Fig. 7-41 shows the entire efficiency curve for the DSAB converter, using GaN inverter devices and the low-power mode to optimize efficiency over the entire load range. The converter achieves a peak efficiency of 97%, 96% efficiency at full load,

95% efficiency at 20% load (operating in the low-power mode), 93% efficiency at 10% load, and 80% efficiency at 3.3% load.

The Single-Stacked DAB, however, is only able to maintain greater than 90% efficiency down to ∼100 W or 33% load, and is 69% efficient at 10% load and 41% efficient at 3.3% load.

Tables 7.5 to 7.7 list the efficiencies of the various topologies and operating modes at 300 W (100% load), 30 W (10% load), and 10 W (3.3% load). The most efficient design at each pointed is bolded, which is the DSAB converter populated with GaN inverter devices for all three cases.

Table 7.5: Efficiency at 300 W (100% Load)

Topology	P_{out} (W)	Efficiency (%)
DSAB GaN - Full-Power Mode	**299.6**	**95.9**
DSAB Si - Full-Power Mode	299.7	94.9
Single-Stacked DAB Si	299.1	95.2

Table 7.6: Efficiency at 30 W (10% Load)

Topology	P_{out} (W)	Efficiency (%)
DSAB GaN - Full-Power Mode	30.42	87.6
DSAB GaN - Low-Power Mode	**30.22**	**92.7**
DSAB Si - Full-Power Mode	30.26	86.3
DSAB Si - Low-Power Mode	30.44	92.3
Single-Stacked DAB Si	29.91	68.8

Table 7.7: Efficiency at 10 W (3.3% Load)

Topology	P_{out} (W)	Efficiency (%)
DSAB GaN - Full-Power Mode	9.97	66.0
DSAB GaN - Low-Power Mode	**10.01**	**79.8**
DSAB Si - Full-Power Mode	10.07	62.9
DSAB Si - Low-Power Mode	10.19	77.6
Single-Stacked DAB Si	10.19	40.7

7.4.1 Gating Loss

As mentioned in Section 7.2.2, the gating power for the inverter and rectifier devices was measured and included in efficiency calculations.

Fig. 7-42 shows the total gating power for each of the topologies experimentally tested. Although the Single-Stacked DAB converter had the lowest overall gating loss, the gating loss for the GaN DSAB converter using EPC2012C inverter devices was within 50 mW of the Single-Stacked DAB converter's over the entire load range. The low-power mode for each DSAB converter also had lower overall gating loss compared to the full-power mode's, highlighting its improved switching performance. While the Si DSAB converter with FQD10N20L inverter devices was within 140 mW of the gating loss of the Single-Stacked DAB converter for most of the load range, it is interesting to note that at low powers its gating loss is very high, possibly due to the non-linear device capacitances of that particular device. The GaN And Si Superjunction devices used do not show such an increase at low power.

Even though the Single-Stacked DAB converter had the lowest gating loss for most of the load range, because the total gating loss is very small compared to the rated output power, both the Si and GaN DSAB converters were more efficient overall.

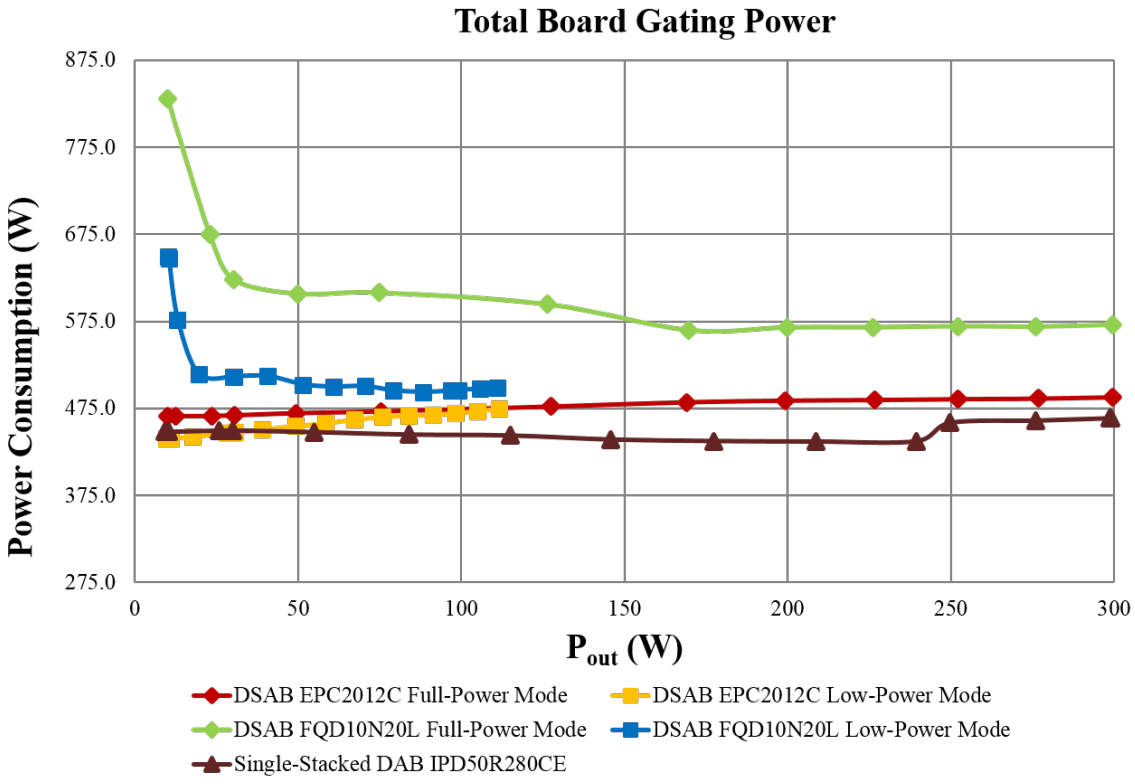


Figure 7-42: Total gating power over a wide load range.

7.4.2 Low-power switch path resistance

As discussed in Chapter 6, the resistance of the low-power switch Q_{LP} path has a large impact on the efficiency. If the resistance is too high, the low-power mode will have lower efficiency, and will also intersect the full-power mode efficiency curve at a lower power, reducing its applicable range.

Fig. 7-43 shows efficiency curves taken from the Si DSAB prototype while in the process of optimizing the Q_{LP} path. The curves show four cases:

1. Q_{LP} implemented with a foil short, so that the board is permanently configured in the low-power mode (red curve).

2. Q_{LP} implemented with the on-board low-power switch circuitry (brown curve).

3. Q_{LP} implemented with the on-board low-power switch circuitry in addition to a daughter board providing a parallel path through two additional source-connected EPC2023 devices, mounted horizontally so that it is parallel to the main PCB surface.

4. implemented with the on-board low-power switch circuitry in addition to a daughter board providing a parallel path through two additional source-connected EPC2023 devices, mounted vertically so that it is perpendicular to the main PCB surface.

The gating loss is not included in any curves in this figure to allow for a fair comparison between the different cases, as the foil short data was collected on a preliminary prototype that did not have the probes for measuring gating power set-up.

As can be seen in the figure, the on-board low-power switch had much lower efficiency than the foil short, which could maintain greater than 94% efficiency over a wide power range. To attempt to reduce the parasitic resistance in the low-power switch path, a daughter board was constructed that contained another set of source-connected EPC2023s. The same gate signal was used to drive both sets of devices, although each device had their own gate drivers.

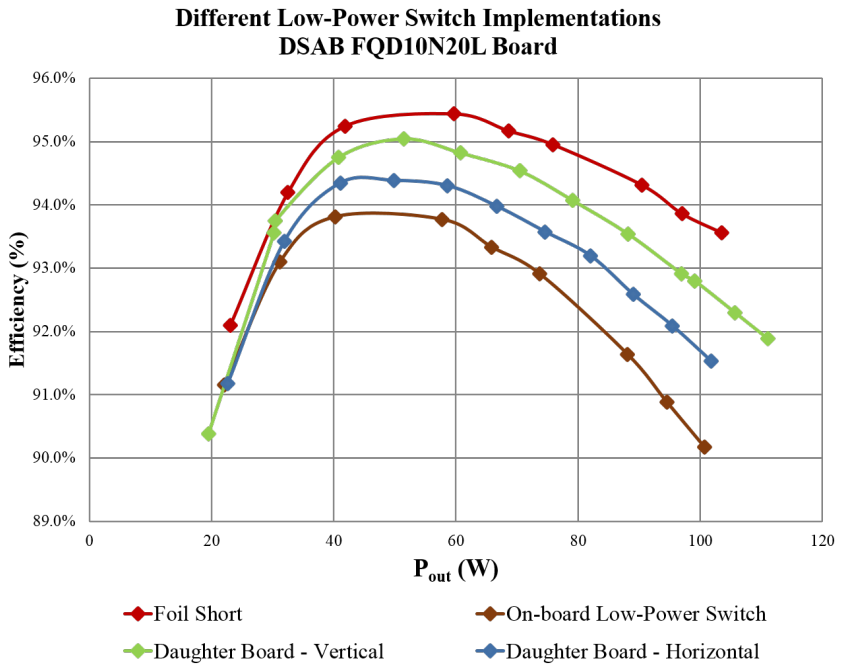


Figure 7-43: Efficiency curves for the Si DSAB for various low-power switch implementations.

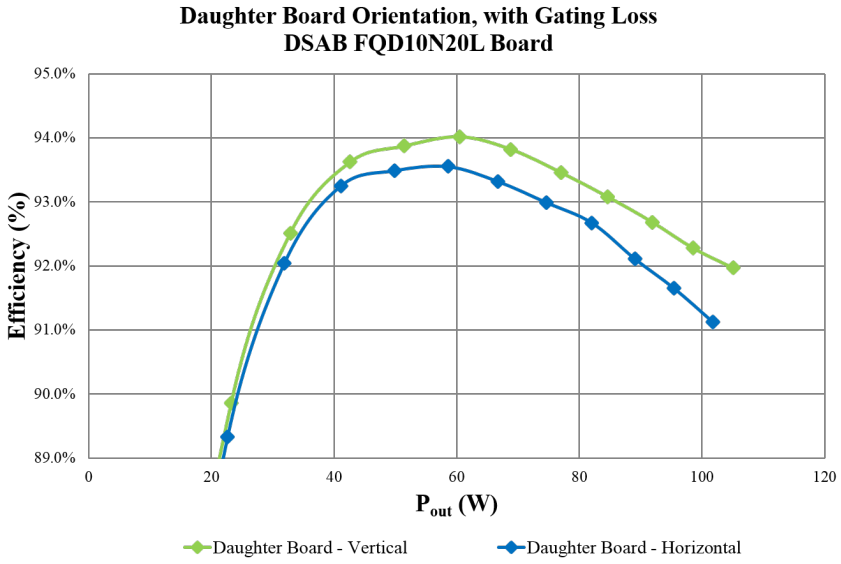


Figure 7-44: Efficiency curves for the Si DSAB for two different orientations of the low-power switch daughter board.

The orientation of the daughter board also proved to be very important, as the vertically mounted board had approximately 0.7% higher efficiency than the horizontally mounted board. Part of the benefit is from the fact that the foil inter-board

connections could be made shorter with the vertically mounted board.

Fig. 7-44 shows the efficiency curves for the vertically mounted and horizontally mounted board orientations, this time including the gating loss. The vertically mounted board can achieve a peak efficiency of 94.0%, while the horizontally mounted board achieves a peak efficiency of 93.6%. At higher powers, the vertically mounted board can achieve 0.7-0.8% higher efficiency than the horizontally mounted board. A vertically mounted daughter board was also mounted on the GaN converter. While not as efficient as an actual short, the vertically mounted board was within ∼0.3% of the permanent copper short efficiency. These efficiency values do not include gating loss, as the permanent copper short efficiency was measured during preliminary testing before the gate power dissipation was measured.

Fig. 7-45 shows the leakage inductor current waveforms for the Si DSAB converter operating in the low-power mode. The waveforms were taken from oscilloscope screen capture data, and plotted and smoothed in MATLAB (to average out some noise from the probe measurement). The figure shows the current for the case where only the on-board low-power switch circuitry is used (green) and for the case where a horizontally-mounted daughter board is used in parallel to the on-board circuitry (red). The slope of the current is much steeper with just the on-board circuitry, as a result of the higher resistance in the Q_{LP} switch path. This behavior matches that predicted by simulation. Additionally, the efficiency for the converter with just the on-board circuitry was 90.2% at 100 W, while the efficiency for the converter with the added the daughter board was 91.5% at 101 W.

The above figures emphasize the importance of making sure the Q_{LP} path is low resistance, even though the switch is operating in a low power mode with low current compared to the full-load current. Fig. 7-46 shows the different mounting positions of the low-power switch daughter board (horizontal on the left, and vertical on the right).

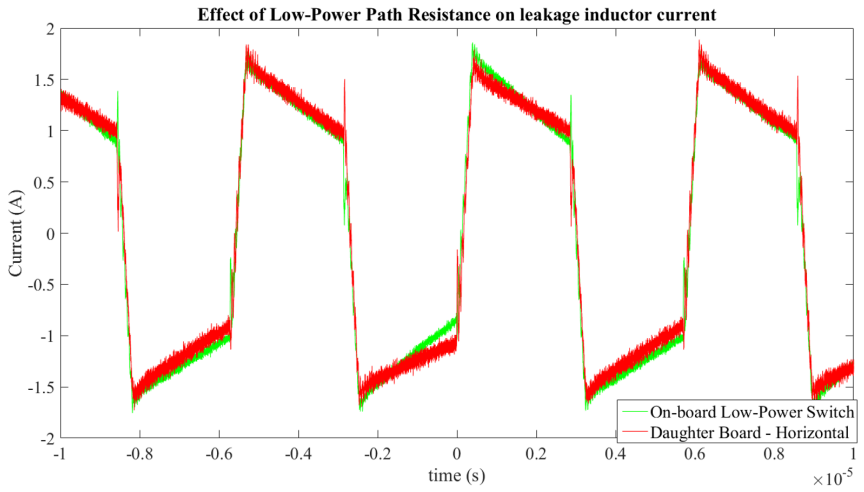


Figure 7-45: Leakage inductor current for the Si DSAB converter with and without a daughter board in parallel with the on-board low-power switch circuitry.

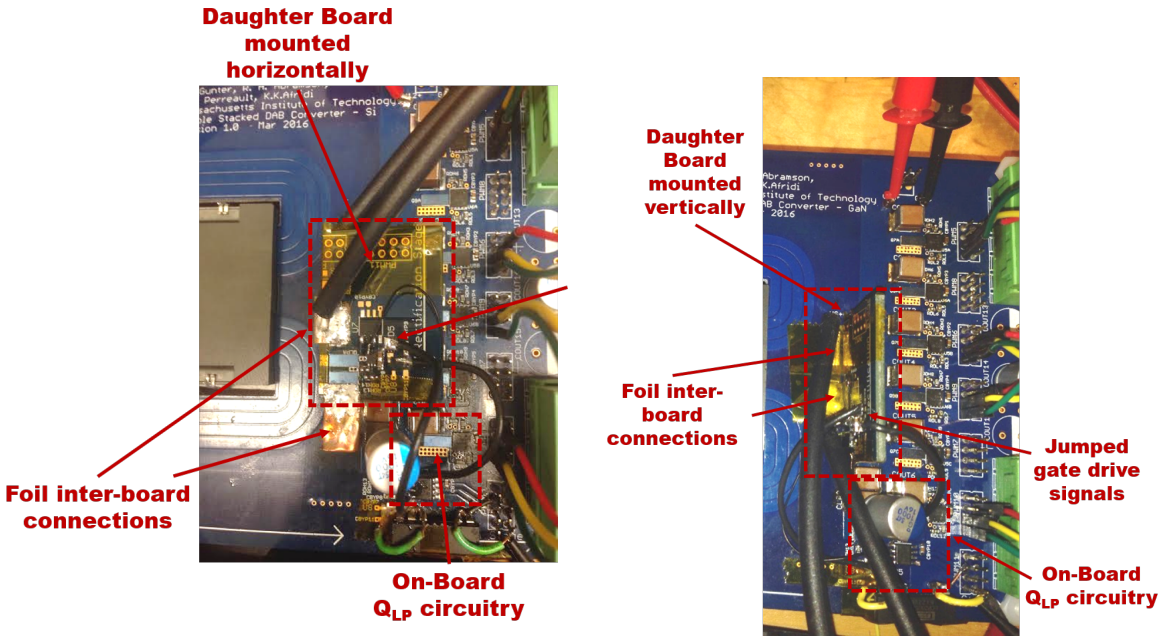


Figure 7-46: Horizontally mounted daughter board (left) and vertically mounted daughter board (right)

7.4.3 Wide Voltage Range Operation

The DSAB converter was also simulated over a wide input voltage range. While the converter was designed to handle a range of 260 V to 410 V, test data is only presented down to 350 V, as the converter had some thermal issues during initial testing at the lower voltages. More investigation is needed to examine the prototypes actual achievable input voltage range, but in the case that the higher currents at the lower input voltage are proving to be too much for the prototype's rectifier switches, which are not provided with any special heat-transfer path, then additional prototypes could be designed to improve the heat-sinking ability of the layout.

Fig. 7-47 shows the experimental efficiency of the Si DSAB converter at three points in the voltage range: 350 V, 380 V, and 410 V. The efficiency increases with input voltage, possibly due to the lower RMS currents at the high end of the input voltage range.

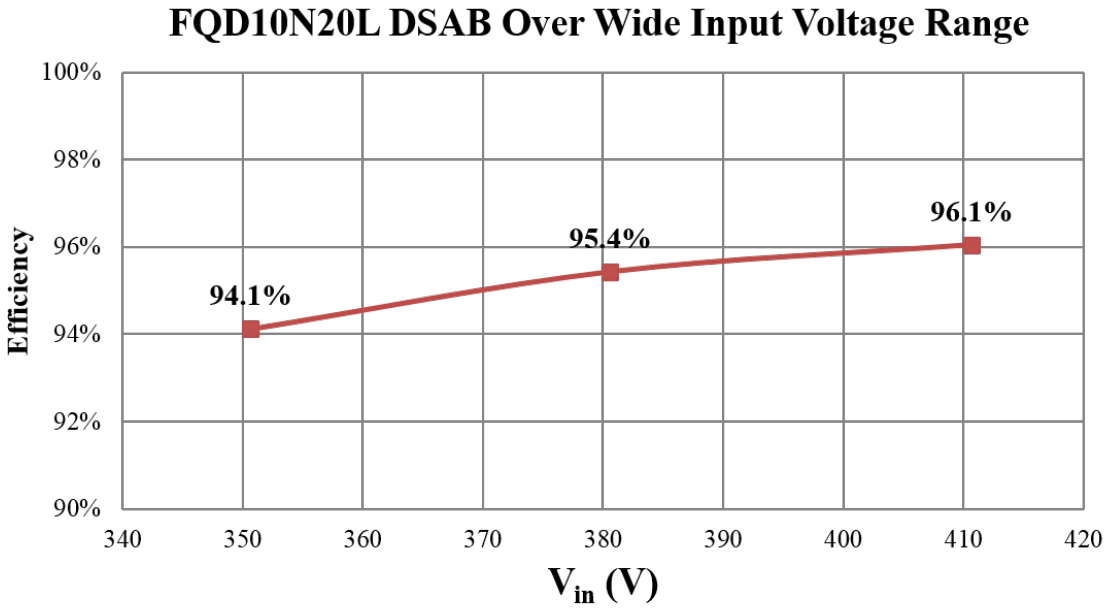


Figure 7-47: Experimental efficiency of the Si DSAB converter over an input voltage range of 350 V to 410 V.

Figs. 7-48 - 7-50 show the operating waveforms for the Si DSAB converter operating at 410 V, 380 V, and 350 V at an output power of 300 W. At 410 V, the inductor current slopes up because the input voltage is higher than the nominal volt-

age, which set the transformer turns ratio. At 350 V, the current slopes downward, and has a steeper slope than either of the other two operating points. Because the current slopes downward, the actual current value at the inverter switch transition has decreased. As the input voltage is further decreased, the converter will start to lose ZVS due to the shape of the current waveform, which creates additional power loss.

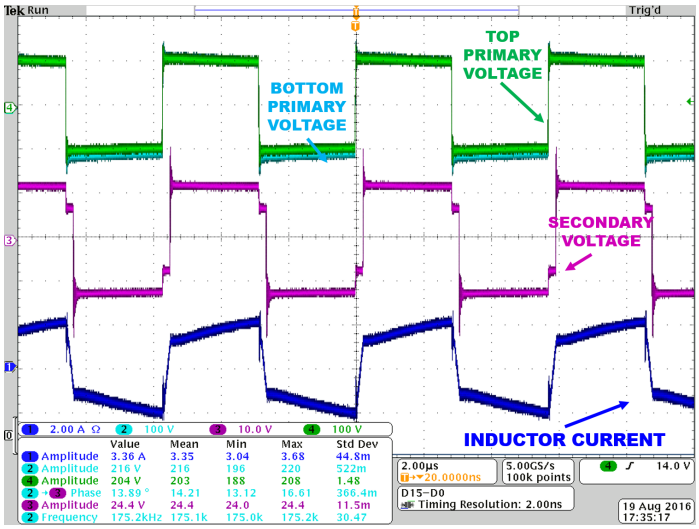


Figure 7-48: Si DSAB converter operating waveforms at an input voltage of 410 V and 300 W.

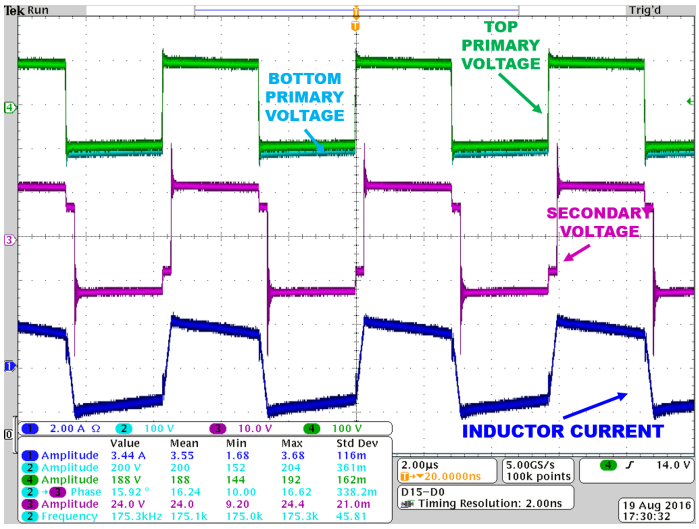


Figure 7-49: Si DSAB converter operating waveforms at an input voltage of 380 V and 300 W.

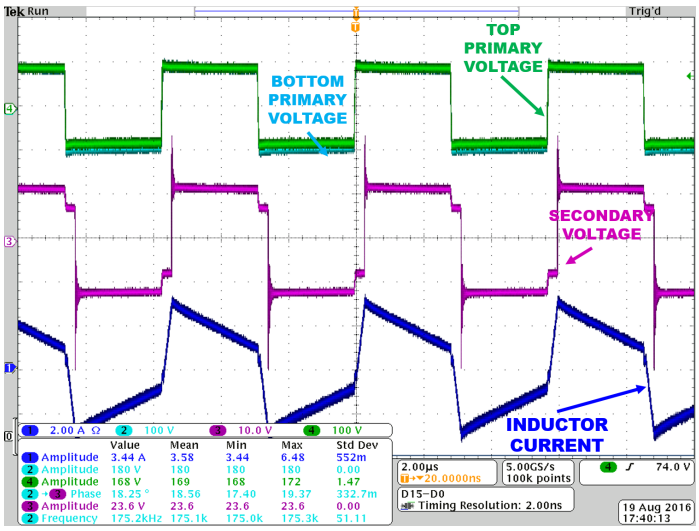


Figure 7-50: Si DSAB converter operating waveforms at an input voltage of 350 V and 300 W.

7.5 Summary

This chapter has presented experimental results from three prototype converters: DSAB converter with GaN inverter devices, DSAB converter with Si inverter devices, and a Single-Stacked DAB converter with Si Superjunction devices. The converters' efficiency was measured over a wide range of loads, and the ZVS performance of each implementation was investigated.

The DSAB converter demonstrated much better performance than the Single-Stacked DAB converter, and was able to achieve ZVS down to a lower power. Additionally, the low-power mode of the DSAB proved to be very effective at maintaining high efficiency down to very low loads. Although the proposed topology requires more devices than the Single-Stacked DAB and Full-Bridge DAB topologies explored here, the gating loss is not significantly higher, nor is the control that much more complex (especially with the addition of a passive balancer network that balances the voltages internal to each stacked full-bridge inverter, as discussed in Chapter 3). The double-stacked topology also allows for operation in the low-power mode, which greatly increases efficiency by decreasing core loss, switching loss, and greatly extends the ZVS range over output power. Using GaN inverter devices, a 175 kHz, 300 W, 380 V to 12 V prototype DSAB converter is able to achieve 95.9% efficiency at full

load, a peak efficiency of 97.0%, an efficiency above 92.7% down to 10% load and an efficiency above 79.8% down to 3.3% load. Using Si devices, the DSAB converter is able to achieve 94.9% efficiency at full load, a peak efficiency of 96.3%, an efficiency above 92.3% down to 10% load, and an efficiency above 77.6% down to 3.3% load.

Chapter 8

Conclusion and Future Work

This chapter provides a summary of the results obtained in this thesis, and also discusses future areas of research that could continue the work presented here. This thesis, and the companion work presented in [27], set out to develop a new topology for high efficiency large step-down dc-dc voltage conversion. A theoretical analysis of the converter was presented, followed by simulation and experimental data for several prototype converters operating at 175 kHz and 300 W.

The main objective of this thesis was to develop a topology that could maintain high efficiency over a very wide load range, by taking advantage of several of the benefits of the traditional dual-active-bridge (DAB) converter, and at the same time overcoming its limitations operating at low load or away from the nominal voltage conversion ratio. The converter operation was also verified with theoretical analysis (with special attention given to the three-winding transformer with built-in leakage inductance), numerous simulations, and experimental testing of several prototypes.

8.1 Summary

The proposed topology as well as two dual-active-bridge topologies were simulated with Si and GaN devices. Of these, three were built as prototypes to be experimentally verified. From simulated and experimental data, we find that the Double-Stacked Active Bridge (DSAB) topology proposed here has several advantages compared to

both a single stacked full-bridge DAB topology and a traditional full-bridge DAB topology, due to its higher efficiency and greater ZVS range over output power.

The main conclusions of this work are listed below:

- The DSAB topology showed higher efficiency compared to the Single-Stacked DAB and Full-Bridge DAB topologies over a wide load range. The Full-Bridge DAB simulations showed significantly lower efficiency over the entire load range, and were not able to achieve zero-voltage-switching (ZVS). While the Single-Stacked DAB simulations and prototype had similar efficiency to those of the DSAB at high powers, the efficiency dropped as the output power decreased. The DSAB simulations and prototypes were able to maintain ZVS down to a much lower power than the Single-Stacked DAB, which helped it maintain such high efficiency at low loads.

- The stacked architecture of the DSAB allowed for the use of lower-voltage rated devices with much more favorable parasitic resistance and capacitance, which decreased conduction and switching losses.

- The low-power mode of the DSAB was very effective at maintaining high efficiencies down to very low powers. The DSAB converter running in this mode was able to achieve greater than 92% efficiency down to 10% load. The low-power mode decreases core loss, switching loss, and extends the ZVS range over output power.

- This work (and that of [27]) presented a compact magnetic design capable of realizing a multi-winding transformer with internal leakage inductance. Two primary windings, a secondary winding, and the requisite leakage for both inverters were implemented with a single-core design. Additionally, by using planar magnetics, the primary and secondary windings were able to be interleaved to reduce ac resistance and proximity effect, while winding the primaries on the outer legs of an E-I core created enough leakage for use as the entire energy transfer inductance in the DSAB topology.

- The benefits of GaN devices in high-voltage (e.g. hundreds of volts) converters was experimentally demonstrated, as the DSAB converter with GaN inverter devices was able to achieve higher efficiency (1-1.5%) compared to the Si DSAB prototype.

8.2 Future Work

As the designs presented in this thesis are prototypes, there are several techniques that could be used to improve performance.

While the prototypes here were run open-loop, a simple control loop could be implemented to handle the phase-shift in the face of load variation. Specifically, the output power could be sensed in order to operate the converter in the corresponding mode (e.g., full-power or low-power), using a simple hysteretic control scheme. The transients on the mode-switch have not yet been evaluated, which is another area to be explored.

Additionally, while the converters presented here used a fixed deadtime and frequency, the deadtime could be adaptively adjusted as a function of the output power to reduce body diode conduction in the devices or prevent ring down on the switch drain-to-source voltages. Frequency modulation schemes could also be implemented on the topology, by modulating the operating frequency and the phase shift together. This could be done to separately optimize the efficiency at both full power and low power.

The magnetic structure presented here could also be used in other topologies where both transformation and energy transfer inductance are needed. As shown with the Single-Stacked DAB converter, the transformer can be configured as a single-primary component, though this does not utilize its full functionality. Multi-port converters, however, could be an area where this compact magnetic component could be used to increase power density or efficiency.

The reconfigurable rectifier in the low-power mode could be used to handle wide input voltage variations, as well as a decrease in output power. Since the auxiliary

switch in the rectifier changes the secondary voltage, it could be used to keep the voltage transformation ratio close to the turns ratio, if a wide enough input voltage range is expected.

The DSAB converter demonstrates several techniques that can be used to increase efficiency, thorough the use of a stacked high-voltage-side inverter and a compact magnetic component. Smaller benefits (though still valuable) come from using GaN technology and paralleling devices. This topology is especially attractive where large step-down voltage conversion and high efficiency across a wide load range is required.

Appendix A

MATLAB: Frequency and Output Power Operating Points

```
%This script takes in a Frequency vector (eg from Core Loss Testing) and
%caculates the phi for the given frequency, L, and Pout combination at the
%nominal operating point for the DAB (380 V in, 12 V out).

%The script also checks if phi is realizable (completely real), and outputs
%the min and max frequencies for the given L and Pout

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Set up excel sheet to write to
filename = 'FrequencySweepOverOperatingPoint.xlsx';

%Set up inputs
L = 32e-6;
Pout = [300 350 400];
Vin_range = [260 290 320 350 380 410];
Vin_nom = 380;

%sample a few values from the Frequency vector (this is designed for a
```

```
%sweep of 100 kHz to 1 MHz. We are only interested in the values from 100
%kHz to 500 kHz however. The frequency step size is 2250 Hz. To sample at
%every 50th kHz, we sample every 22nd entry.

%FrequencyHz is the name of the vector imported in from Transformer
%Resistance.xslx
%If there isn't a vector to import, create FrequencyHz vector here:
%FrequencyHz =

i = 1:1:9;
sampledF = FrequencyHz(22*(i-1)+1);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Calculate value of phi for sampled frequency values

phi_nom = zeros(length(Pout),length(sampledF));

phi_sweep_summary = length(Pout);

%index where phi becomes complex in first loop
stop_k_outer = zeros(1, length(Pout));

%index where phi becomes complex in second loop
stop_k_inner = zeros(1, length(Pout));

%holds max fsw for real phi, phi_nom, and phi_max for all power points
OutputSummary = zeros(length(Pout),4);
OutputSummary(:,1) = Pout;              %first column holds Pout

fprintf('Phi evaluated every 50 kHz at nominal operating point\n')
for n=1:length(Pout);            %for each Pout rating sweep over fsw
       phi_sweep = zeros(length(sampledF), length(Vin_range));
```

```
for k=1:length(sampledF)
        phi_nom(n,k) = phi_calc(sampledF(k),L,Pout(n),Vin_nom);
        fprintf('fsw = %g, Pout = %g, phi = %g + %gi\n', sampledF(k),
             Pout(n), real(phi_nom(n,k)), imag(phi_nom(n,k)));

        if phi_nom(n,k) ~= real(phi_nom(n,k))
                stop_k_outer(n) = k; %sampled frequency at which phi
                    becomes complex
                break;
        end
end

xlRange = strcat('A1:',sprintf('B%d', length(sampledF)));
sheet = strcat('Pout = ',sprintf('%d', Pout(n)));

xlswrite(filename,[sampledF phi_nom(n,:)'],sheet, xlRange)

%Now, check that phi is real from 260 V - 380 V for each frequency
%point

for k=1:length(sampledF)
        for m = 1:length(Vin_range)
                phi_sweep(k,m) = phi_calc(sampledF(k),L,Pout(n),
                    Vin_range(m));
                if phi_sweep(k,m) ~= real(phi_sweep(k,m))
                        if k < stop_k_outer(n)
                                %get rid of frequencies that don't have
                                     real phi for all Vin
                                stop_k_outer(n) = k;
                        end
                        break;
```

```
                end
        end
end

fprintf('\n\tCheck for real phi over entire Vin range...\n')

interF = FrequencyHz(1:22*(stop_k_outer(n)-1)+1);

phi_sweep_inter = zeros(length(interF), length(Vin_range));
data_to_write = [];
max_fsw_index = length(interF);

for j =1:length(interF)

        for m = 1:length(Vin_range)
                phi_sweep_inter(j,m) = phi_calc(interF(j),L,Pout(n),
                    Vin_range(m));

                if phi_sweep_inter(j,m) ~= real(phi_sweep_inter(j,m))
                        if stop_k_inner(n) == 0
                                stop_k_inner(n) = j; %sampled frequency
                                     at which phi becomes complex
                                max_fsw_index = stop_k_inner(n)-1;
                        end
                break;

                end
        end

        if j <= max_fsw_index
                data_temp = [ones(1,length(Vin_range))*interF(j);
                    Vin_range; phi_sweep_inter(j,:)]';
```

```
                data_to_write = [data_to_write; data_temp];
            end
        end

        %write to excel sheet
        xlRange_append = strcat(sprintf('A%d:', length(sampledF)+1),sprintf
            ('C%d', length(data_to_write)+length(sampledF)));
        sheet = strcat('Pout = ',sprintf('%d', Pout(n)));
        xlswrite(filename, data_to_write, sheet, xlRange_append)

        fprintf('\tMax fsw for real phi = %g\n', interF(max_fsw_index));
        fprintf('\n')

        Vin_max_index = 1;    %260 V is where max phi occurs
        Vin_nom_index = 5;    %380 V is nominal o.p.

        phi_nom_val = phi_sweep_inter(max_fsw_index, Vin_nom_index); %eval
            at max freq
        phi_max_val = phi_sweep_inter(max_fsw_index, Vin_max_index);

        OutputSummary(n,2) = interF(max_fsw_index);
        OutputSummary(n,3) = phi_nom_val;
        OutputSummary(n,4) = phi_max_val;

end

fprintf('At Nominal Operating Point: Vin = 380 V, Vout = 12 V\n');
Power = OutputSummary(:,1);
MaxFrequency = OutputSummary(:,2);
PhiNominal = OutputSummary(:,3);
PhiMax = OutputSummary(:,4);
T = table(Power,MaxFrequency,PhiNominal,PhiMax);
```

```
display(T);

%write summary to excel sheet
writetable(T, filename, 'Sheet', 'Summary')

Phi evaluated every 50 kHz at nominal operating point
fsw = 100000, Pout = 300, phi = 2.78692 + 0i
fsw = 149500, Pout = 300, phi = 4.30484 + 0i
fsw = 199000, Pout = 300, phi = 5.9433 + 0i
fsw = 248500, Pout = 300, phi = 7.73656 + 0i
fsw = 298000, Pout = 300, phi = 9.73911 + 0i
fsw = 347500, Pout = 300, phi = 12.0477 + 0i
fsw = 397000, Pout = 300, phi = 14.8693 + 0i
fsw = 446500, Pout = 300, phi = 18.8763 + 0i
fsw = 496000, Pout = 300, phi = 25 + -5.25657i

Check for real phi over entire Vin range...
Max fsw for real phi = 325000

fsw = 100000, Pout = 350, phi = 3.28615 + 0i
fsw = 149500, Pout = 350, phi = 5.11271 + 0i
fsw = 199000, Pout = 350, phi = 7.12495 + 0i
fsw = 248500, Pout = 350, phi = 9.39453 + 0i
fsw = 298000, Pout = 350, phi = 12.0561 + 0i
fsw = 347500, Pout = 350, phi = 15.4315 + 0i
fsw = 397000, Pout = 350, phi = 21.0541 + 0i
fsw = 446500, Pout = 350, phi = 25 + -7.77282i

Check for real phi over entire Vin range...
Max fsw for real phi = 277750

fsw = 100000, Pout = 400, phi = 3.79714 + 0i
```

```
fsw = 149500, Pout = 400, phi = 5.95481 + 0i
fsw = 199000, Pout = 400, phi = 8.39045 + 0i
fsw = 248500, Pout = 400, phi = 11.251 + 0i
fsw = 298000, Pout = 400, phi = 14.8909 + 0i
fsw = 347500, Pout = 400, phi = 21.082 + 0i
fsw = 397000, Pout = 400, phi = 25 + -8.45525i

Check for real phi over entire Vin range...
Max fsw for real phi = 241750

At Nominal Operating Point: Vin = 380 V, Vout = 12 V

T =

Power   MaxFrequency   PhiNominal   PhiMax
-----   ------------   ----------   ------

300       3.25e+05     10.951          25
350     2.7775e+05     10.906       23.642
400     2.4175e+05     10.827       22.735
```

Appendix B

LTSPICE Schematics and Netlists

Schematics and netlists for the simulations performed in Chapter 6 are listed below, grouped by converter topology. Schematics and netlists are presented in the order given below.

Double-Stacked Active Bridge (DSAB) Topology simulations:

- `DoubleStackedDAB_EPC2012C_FP`
  DSAB Converter with GaN EPC2012C inverter devices in Full-Power Mode with a single EPC2023 device for each rectifier switch.
- `DoubleStackedDAB_EPC2012C_FP_2xEPC2023`
  DSAB Converter with GaN EPC2012C inverter devices in Full-Power Mode with two paralleled EPC2023 device for each rectifier switch.
- `DoubleStackedDAB_EPC2012C_FP_3xEPC2023`
  DSAB Converter with GaN EPC2012C inverter devices in Full-Power Mode with three paralleled EPC2023 device for each rectifier switch.
- `DoubleStackedDAB_EPC2012C_LP_alt`
  DSAB Converter with GaN EPC2012C inverter devices in Low-Power Mode with a single EPC2023 device for each rectifier switch.
- `DoubleStackedDAB_FQD10N20L_FP`
  DSAB Converter with Si FQD10N20L inverter devices in Full-Power Mode with a single EPC2023 device for each rectifier switch.

- `DoubleStackedDAB_FQD10N20L_LP_alt`

  DSAB Converter with Si FQD10N20L inverter devices in Low-Power Mode with a single EPC2023 device for each rectifier switch.

Single-Stacked DAB Topology simulations:

- `SingleStackedDAB_EPC2025_series`

  Single-Stacked DAB converter with GaN ECP2025 inverter devices with a single EPC2023 device for each rectifier switch.
- `SingleStackedDAB_IPD50R280CE_series`

  Single-Stacked DAB converter with Si Superjunction IPD50R280CE inverter devices with a single EPC2023 device for each rectifier switch.

Full-Bridge DAB Topology simulations:

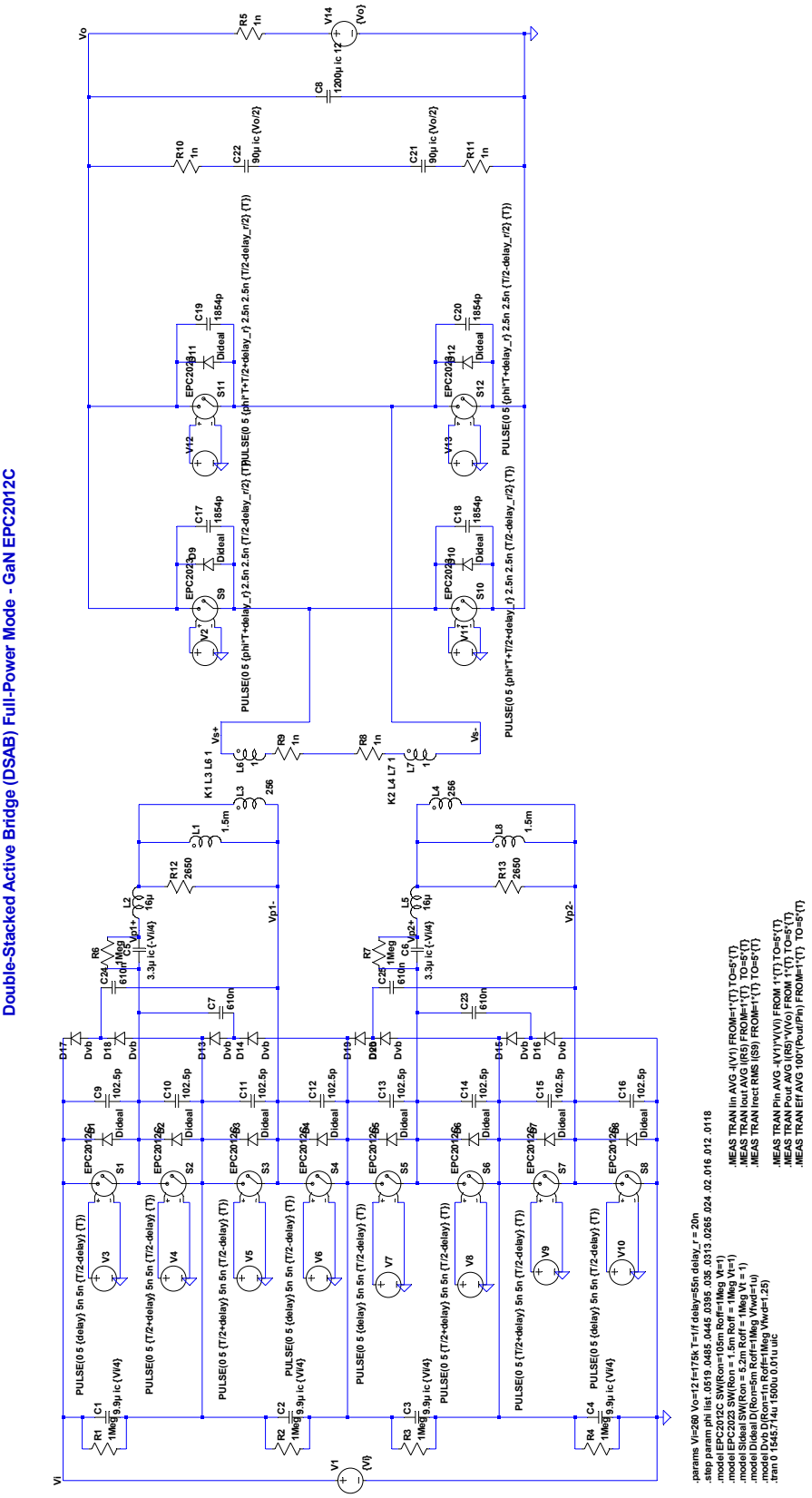
- `FullBridgeDAB_GS66516T`

  Full-Bridge DAB converter with GaN GS66516T inverter devices with a single EPC2023 device for each rectifier switch.
- `FullBridgeDAB_IPD50R280CE`

  Full-Bridge DAB converter with Si Superjunction IPD50R280CE inverter devices with a single EPC2023 device for each rectifier switch.

The following general SPICE settings were used for all simulations:

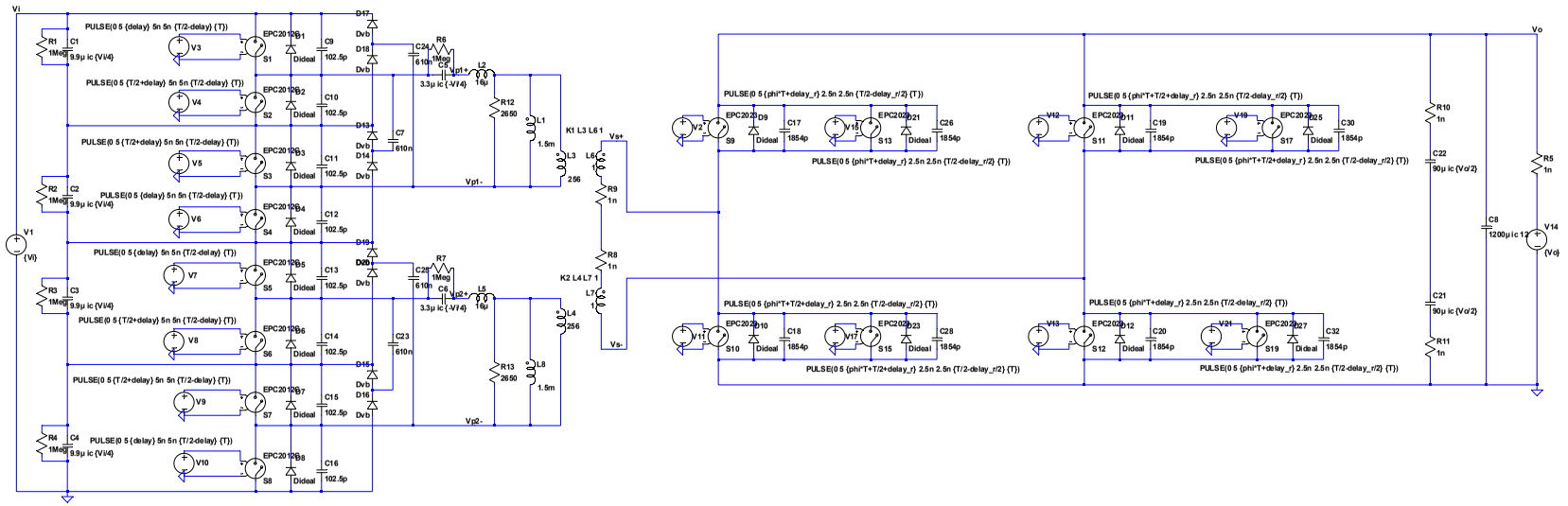
- Default Integration Method: modified trap
- Solver: Alternate
- Gmin: 1e-012
- Abstol: 1e-012
- Reltol: 0.001
- Chgtol: 1e-014
- Trtol: 1
- Volttol: 1e-006
- Sstol: 0.001
- MinDeltaGmin: 0.0001


Double-Stacked Active Bridge (DSAB) Full-Power Mode - GaN EPC2012C
.params Vi=260 Vo=12 f=175k T=1/f delay=55n delay_r = 20n
.step param phi list .0519 .0485 .0445 .0395 .035 .0313 .0265 .024 .02 .016 .012 .0118
.model EPC2012C SW(Ron=105m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 1.5m Roff = 1Meg Vt=1)
.model Sideal SW(Ron = 5.2m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.model DVb D(Ron=1n Roff=1Meg Vfwd=1.25)
.tran 0 1045.714u 1000u 0.01u uic
.MEAS TRAN Iin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T} TO=5*{T}
.MEAS TRAN Irect RMS I(S9) FROM=1*{T} TO=5*{T}
.MEAS TRAN Pin AVG -(V1*V(Vi)) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG (I(R5)*V(Vo)) FROM 1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T} TO=5*{T}

```
* C:\Users\Rose\Dropbox\MIT\MENG\DAB\LTSPICE\Thesis Simulations\Final Versions of
EffCurves\DoubleStackedAB_EPC2012C_FP.asc
V1 Vi 0 {Vi}
V3 N001 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V4 N006 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S1 N004 Vi N001 0 EPC2012C
S2 N003 N004 N006 0 EPC2012C
S3 Vp1- N003 N009 0 EPC2012C
S4 N014 Vp1- N013 0 EPC2012C
V5 N009 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V6 N013 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C1 Vi N003 9.9µ ic {Vi/4}
C2 N003 N014 9.9µ ic {Vi/4}
V7 N017 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V8 N026 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S5 N021 N014 N017 0 EPC2012C
S6 N023 N021 N026 0 EPC2012C
S7 Vp2- N023 N028 0 EPC2012C
S8 0 Vp2- N030 0 EPC2012C
V9 N028 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V10 N030 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C3 N014 N023 9.9µ ic {Vi/4}
C4 N023 0 9.9µ ic {Vi/4}
C5 Vp1+ N004 3.3µ ic {-Vi/4}
C6 Vp2+ N021 3.3µ ic {-Vi/4}
L3 Vp1- N005 256 Rser=1n
L4 Vp2- N022 256 Rser=1n
V2 N007 0 PULSE(0 5 {phi*T+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
V11 N024 0 PULSE(0 5 {phi*T+T/2+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
S9 Vs+ Vo N007 0 EPC2023
S10 0 Vs+ N024 0 EPC2023
V12 N008 0 PULSE(0 5 {phi*T+T/2+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
V13 N025 0 PULSE(0 5 {phi*T+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
S11 Vs- Vo N008 0 EPC2023
S12 0 Vs- N025 0 EPC2023
C8 Vo 0 1200µ ic 12
D1 N004 Vi Dideal
C9 Vi N004 102.5p
D2 N003 N004 Dideal
C10 N004 N003 102.5p
D3 Vp1- N003 Dideal
C11 N003 Vp1- 102.5p
D4 N014 Vp1- Dideal
C12 Vp1- N014 102.5p
D5 N021 N014 Dideal
C13 N014 N021 102.5p
D6 N023 N021 Dideal
C14 N021 N023 102.5p
D7 Vp2- N023 Dideal
C15 N023 Vp2- 102.5p
D8 0 Vp2- Dideal
C16 Vp2- 0 102.5p
D9 Vs+ Vo Dideal
C17 Vo Vs+ 1854p
D10 0 Vs+ Dideal
C18 Vs+ 0 1854p
D11 Vs- Vo Dideal
C19 Vo Vs- 1854p
D12 0 Vs- Dideal
C20 Vs- 0 1854p
R1 Vi N003 1Meg
R2 N003 N014 1Meg
R3 N014 N023 1Meg
```

```
R4 N023 0 1Meg
R5 Vo N015 1n
L2 Vp1+ N005 16µ Rser=1n
L5 Vp2+ N022 16µ Rser=1n
L6 N012 Vs+ 1 Rser=0.346m
L7 Vs- N019 1 Rser=1n
R6 N004 Vp1+ 1Meg
R7 N021 Vp2+ 1Meg
R8 N016 N019 1n
R9 N012 N016 1n
V14 N015 0 {Vo}
C22 N011 N020 90µ ic {Vo/2} Rser=3.93m
C21 N020 N027 90µ ic {Vo/2} Rser=3.93m
R10 Vo N011 1n
R11 N027 0 1n
R12 N005 Vp1- 2650
R13 N022 Vp2- 2650
D13 N010 N003 Dvb
D14 N014 N010 Dvb
C7 N004 N010 610n Rser=10.15m Lser=1.87n
D15 N029 N023 Dvb
D16 0 N029 Dvb
C23 N021 N029 610n Rser=10.15m Lser=1.87n
D17 N002 Vi Dvb
D18 N003 N002 Dvb
C24 N002 Vp1- 610n Rser=10.15m Lser=1.87n
D19 N018 N014 Dvb
D20 N023 N018 Dvb
C25 N018 Vp2- 610n Rser=10.15m Lser=1.87n
L1 Vp1- N005 1.5m Rser=88.5m
L8 Vp2- N022 1.5m Rser=88.5m
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.params Vi=260 Vo=12 f=175k T=1/f delay=55n delay_r = 20n
.model EPC2012C SW(Ron=105m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 1.5m Roff = 1Meg Vt=1)
.model SIdeal SW(Ron = 5.2m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.model Dvb D(Ron=1n Roff=1Meg Vfwd=1.25)
.tran 0 1545.714u 1500u 0.01u uic
K1 L3 L6 1
K2 L4 L7 1
.MEAS TRAN Iin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T}  TO=5*{T}
.MEAS TRAN Irect RMS I(S9) FROM=1*{T} TO=5*{T}

.MEAS TRAN Pin AVG -I(V1)*V(Vi) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG I(R5)*V(Vo) FROM 1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T}  TO=5*{T}
.step param phi list .0519 .0485 .0445 .0395 .035 .0313 .0265 .024 .02 .016 .012 .0118
.backanno
.end
```

Double-Stacked Active Bridge (DSAB) Full-Power Mode - GaN EPC2012C
2 parallel EPC2023 devices

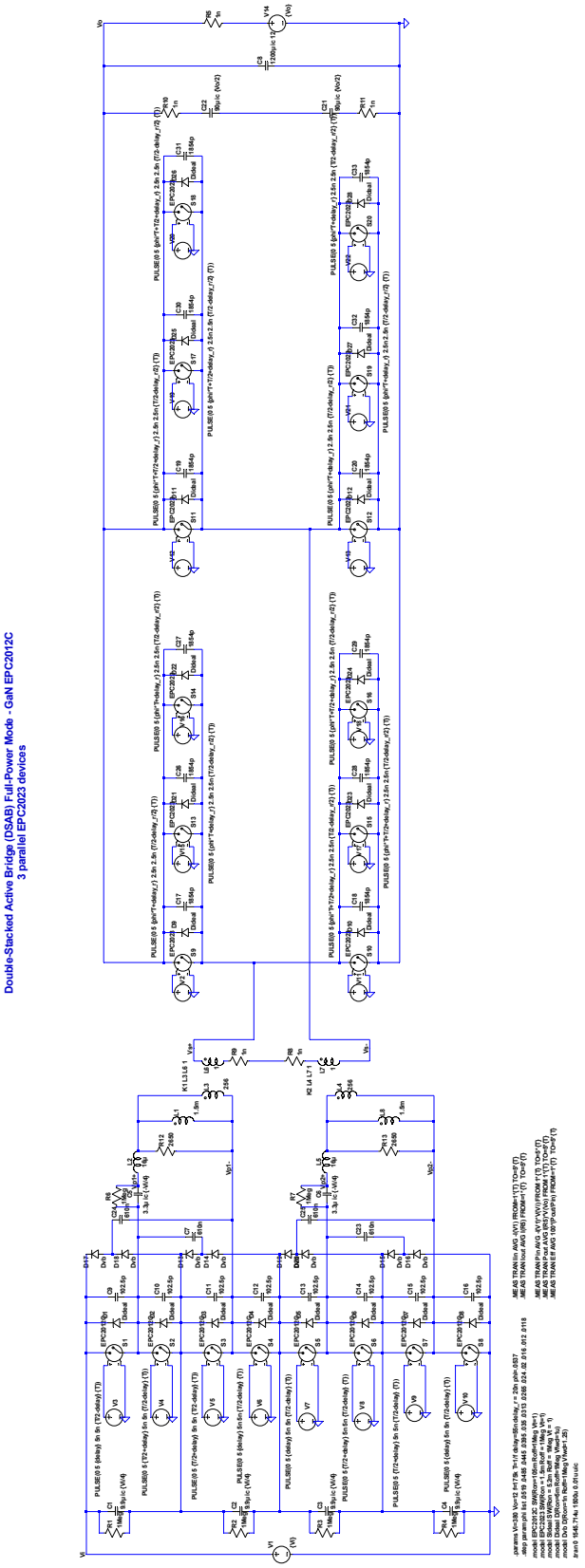



```
.params Vi=380 Vo=12 f=175k T=1/f delay=55n delay_r = 20n phi=.0537
.step param phi list .0519 .0485 .0445 .0395 .035 .0313 .0265 .024 .02 .016 .012 .0118

.model EPC2012C SW(Ron=105m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 1.5m Roff = 1Meg Vt=1)
.model Sideal SW(Ron = 5.2m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.model Dvb D(Ron=1n Roff=1Meg Vfwd=1.25)

.tran 0 1545.714u 1500u 0.01u uic
```

```
.MEAS TRAN Iin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T}  TO=5*{T}

.MEAS TRAN Pin AVG -I(V1)*V(Vi) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG I(R5)*V(Vo) FROM 1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T}  TO=5*{T}
```

```
* C:\Users\Rose\Dropbox (MIT Solar Car Team)\MIT\MENG\DAB\LTSPICE\Thesis Simulations\Final
Versions of EffCurves\DoubleStackedAB_EPC2012C_FP_2xEPC2023.asc
V1 Vi 0 {Vi}
V3 N001 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V4 N006 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S1 N004 Vi N001 0 EPC2012C
S2 N003 N004 N006 0 EPC2012C
S3 Vp1- N003 N011 0 EPC2012C
S4 N016 Vp1- N015 0 EPC2012C
V5 N011 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V6 N015 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C1 Vi N003 9.9µ ic {Vi/4}
C2 N003 N016 9.9µ ic {Vi/4}
V7 N019 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V8 N030 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S5 N023 N016 N019 0 EPC2012C
S6 N025 N023 N030 0 EPC2012C
S7 Vp2- N025 N032 0 EPC2012C
S8 0 Vp2- N034 0 EPC2012C
V9 N032 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V10 N034 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C3 N016 N025 9.9µ ic {Vi/4}
C4 N025 0 9.9µ ic {Vi/4}
C5 Vp1+ N004 3.3µ ic {-Vi/4}
C6 Vp2+ N023 3.3µ ic {-Vi/4}
L3 Vp1- N005 256 Rser=1n
L4 Vp2- N024 256 Rser=1n
V2 N007 0 PULSE(0 5 {phi*T+delay_r} 5n 5n {T/2-delay_r/2} {T})
V11 N026 0 PULSE(0 5 {phi*T+T/2+delay_r} 5n 5n {T/2-delay_r/2} {T})
S9 Vs+ Vo N007 0 EPC2023
S10 0 Vs+ N026 0 EPC2023
V12 N009 0 PULSE(0 5 {phi*T+T/2+delay_r} 5n 5n {T/2-delay_r/2} {T})
V13 N028 0 PULSE(0 5 {phi*T+delay_r} 5n 5n {T/2-delay_r/2} {T})
S11 Vs- Vo N009 0 EPC2023
S12 0 Vs- N028 0 EPC2023
C8 Vo 0 1200µ ic 12
D1 N004 Vi Dideal
C9 Vi N004 102.5p
D2 N003 N004 Dideal
C10 N004 N003 102.5p
D3 Vp1- N003 Dideal
C11 N003 Vp1- 102.5p
D4 N016 Vp1- Dideal
C12 Vp1- N016 102.5p
D5 N023 N016 Dideal
C13 N016 N023 102.5p
D6 N025 N023 Dideal
C14 N023 N025 102.5p
D7 Vp2- N025 Dideal
C15 N025 Vp2- 102.5p
D8 0 Vp2- Dideal
C16 Vp2- 0 102.5p
D9 Vs+ Vo Dideal
C17 Vo Vs+ 1854p
D10 0 Vs+ Dideal
C18 Vs+ 0 1854p
D11 Vs- Vo Dideal
C19 Vo Vs- 1854p
D12 0 Vs- Dideal
C20 Vs- 0 1854p
R1 Vi N003 1Meg
R2 N003 N016 1Meg
R3 N016 N025 1Meg
R4 N025 0 1Meg
R5 Vo N017 1n
L2 Vp1+ N005 16µ Rser=1n
L5 Vp2+ N024 16µ Rser=1n
L6 N014 Vs+ 1 Rser=0.346m
L7 Vs- N021 1 Rser=1n
R6 N004 Vp1+ 1Meg
R7 N023 Vp2+ 1Meg
```

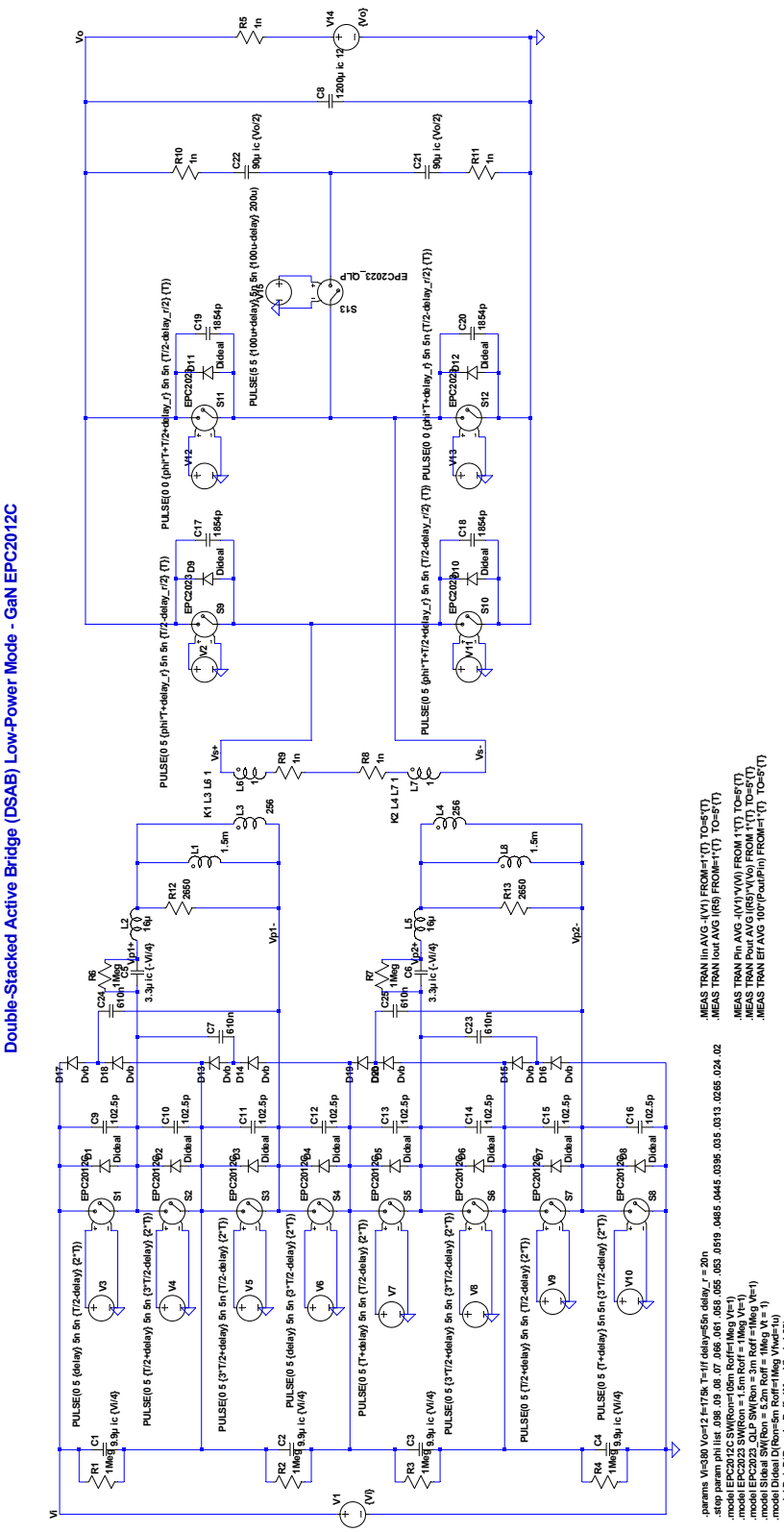
```
R8 N018 N021 1n
R9 N014 N018 1n
V14 N017 0 {Vo}
C22 N013 N022 90µ ic {Vo/2} Rser=3.93m
C21 N022 N031 90µ ic {Vo/2} Rser=3.93m
R10 Vo N013 1n
R11 N031 0 1n
R12 N005 Vp1- 2650
R13 N024 Vp2- 2650
D13 N012 N003 Dvb
D14 N016 N012 Dvb
C7 N004 N012 610n Rser=10.15m Lser=1.87n
D15 N033 N025 Dvb
D16 0 N033 Dvb
C23 N023 N033 610n Rser=10.15m Lser=1.87n
D17 N002 Vi Dvb
D18 N003 N002 Dvb
C24 N002 Vp1- 610n Rser=10.15m Lser=1.87n
D19 N020 N016 Dvb
D20 N025 N020 Dvb
C25 N020 Vp2- 610n Rser=10.15m Lser=1.87n
L1 Vp1- N005 1.5m Rser=88.5m
L8 Vp2- N024 1.5m Rser=88.5m
V15 N008 0 PULSE(0 5 {phi*T+delay_r} 5n 5n {T/2-delay_r/2} {T})
S13 Vs+ Vo N008 0 EPC2023
D21 Vs+ Vo Dideal
C26 Vo Vs+ 1854p
V17 N027 0 PULSE(0 5 {phi*T+T/2+delay_r} 5n 5n {T/2-delay_r/2} {T})
S15 0 Vs+ N027 0 EPC2023
D23 0 Vs+ Dideal
C28 Vs+ 0 1854p
V19 N010 0 PULSE(0 5 {phi*T+T/2+delay_r} 5n 5n {T/2-delay_r/2} {T})
S17 Vs- Vo N010 0 EPC2023
D25 Vs- Vo Dideal
C30 Vo Vs- 1854p
V21 N029 0 PULSE(0 5 {phi*T+delay_r} 5n 5n {T/2-delay_r/2} {T})
S19 0 Vs- N029 0 EPC2023
D27 0 Vs- Dideal
C32 Vs- 0 1854p
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.params Vi=380 Vo=12 f=175k T=1/f delay=55n delay_r = 20n
.step param phi list .0519 .0485 .0445 .0395 .035 .0313 .0265 .024 .02 .016 .012 .0118
.model EPC2012C SW(Ron=105m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 1.5m Roff = 1Meg Vt=1)
.model SIdeal SW(Ron = 5.2m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.model Dvb D(Ron=1n Roff=1Meg Vfwd=1.25)
.tran 0 1545.714u 1500u 0.01u uic
K1 L3 L6 1
K2 L4 L7 1
.MEAS TRAN Iin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T}  TO=5*{T}

.MEAS TRAN Pin AVG -I(V1)*V(Vi) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG I(R5)*V(Vo) FROM 1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T}  TO=5*{T}
* .MEAS TRAN Iin_rms RMS I(V1) FROM=1*{T} TO=5*{T}\n.MEAS TRAN Iout_rms RMS I(R5) FROM=1*{T}
TO=5*{T}
.backanno
.end
```


Double-Stacked Active Bridge (DSAB) Full-Power Mode - GaN EPC2012C
3 parallel EPC2023 devices

```
* C:\Users\Rose\Dropbox\MIT\MENG\DAB\LTSPICE\Thesis Simulations\Final
Versions of EffCurves\DoubleStackedAB_EPC2012C_FP_3xEPC2023.asc
V1 Vi 0 {Vi}
V3 N001 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V4 N006 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S1 N004 Vi N001 0 EPC2012C
S2 N003 N004 N006 0 EPC2012C
S3 Vp1- N003 N013 0 EPC2012C
S4 N018 Vp1- N017 0 EPC2012C
V5 N013 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V6 N017 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C1 Vi N003 9.9µ ic {Vi/4}
C2 N003 N018 9.9µ ic {Vi/4}
V7 N021 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V8 N034 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S5 N025 N018 N021 0 EPC2012C
S6 N027 N025 N034 0 EPC2012C
S7 Vp2- N027 N036 0 EPC2012C
S8 0 Vp2- N038 0 EPC2012C
V9 N036 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V10 N038 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C3 N018 N027 9.9µ ic {Vi/4}
C4 N027 0 9.9µ ic {Vi/4}
C5 Vp1+ N004 3.3µ ic {-Vi/4}
C6 Vp2+ N025 3.3µ ic {-Vi/4}
L3 Vp1- N005 256 Rser=1n
L4 Vp2- N026 256 Rser=1n
V2 N007 0 PULSE(0 5 {phi*T+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
V11 N028 0 PULSE(0 5 {phi*T+T/2+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
S9 Vs+ Vo N007 0 EPC2023
S10 0 Vs+ N028 0 EPC2023
V12 N010 0 PULSE(0 5 {phi*T+T/2+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
V13 N031 0 PULSE(0 5 {phi*T+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
S11 Vs- Vo N010 0 EPC2023
S12 0 Vs- N031 0 EPC2023
C8 Vo 0 1200µ ic 12
D1 N004 Vi Dideal
C9 Vi N004 102.5p
D2 N003 N004 Dideal
C10 N004 N003 102.5p
D3 Vp1- N003 Dideal
C11 N003 Vp1- 102.5p
D4 N018 Vp1- Dideal
C12 Vp1- N018 102.5p
D5 N025 N018 Dideal
C13 N018 N025 102.5p
D6 N027 N025 Dideal
C14 N025 N027 102.5p
D7 Vp2- N027 Dideal
C15 N027 Vp2- 102.5p
D8 0 Vp2- Dideal
C16 Vp2- 0 102.5p
D9 Vs+ Vo Dideal
C17 Vo Vs+ 1854p
D10 0 Vs+ Dideal
C18 Vs+ 0 1854p
D11 Vs- Vo Dideal
```

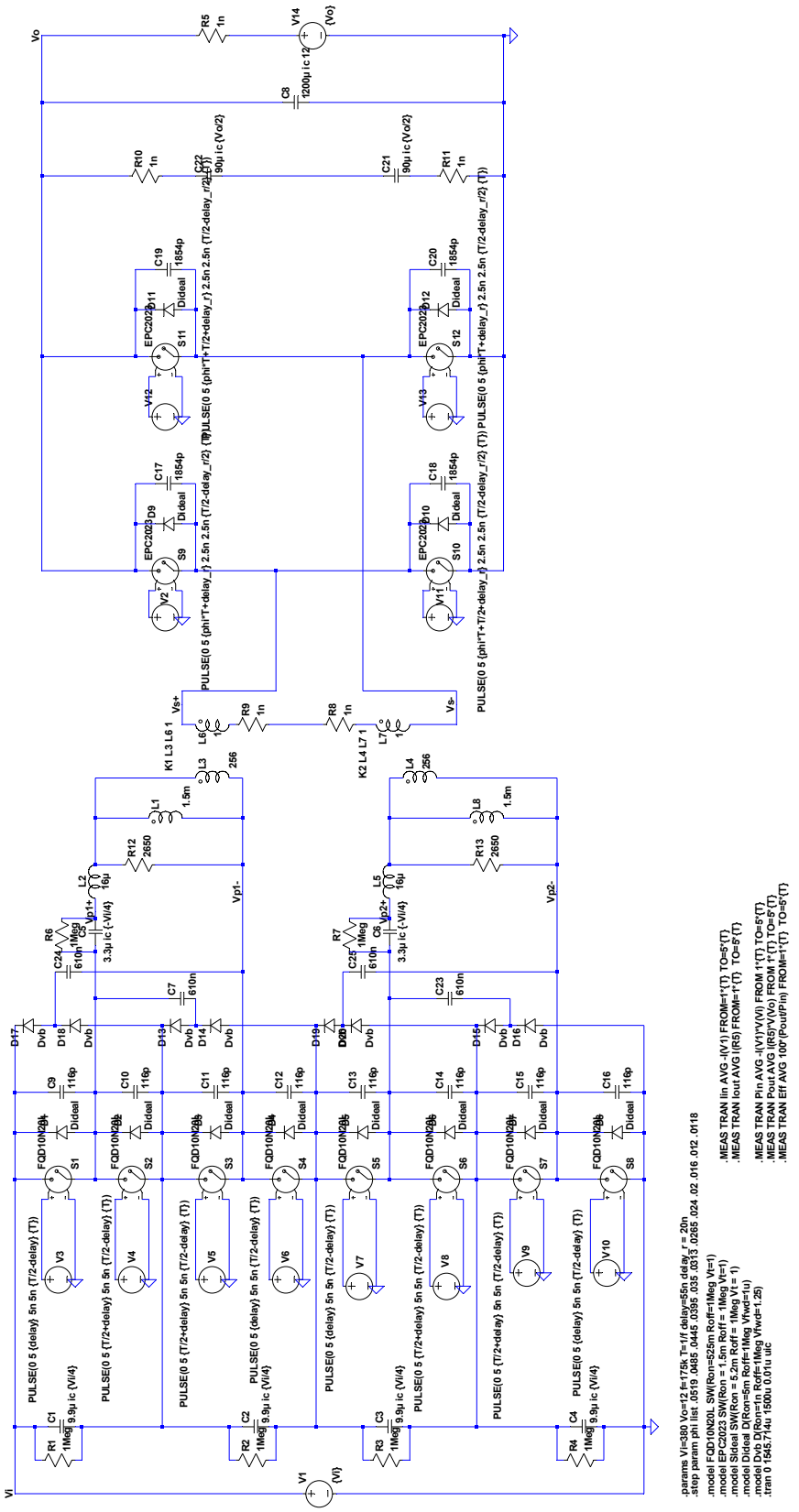
```
C19 Vo Vs- 1854p
D12 0 Vs- Dideal
C20 Vs- 0 1854p
R1 Vi N003 1Meg
R2 N003 N018 1Meg
R3 N018 N027 1Meg
R4 N027 0 1Meg
R5 Vo N019 1n
L2 Vp1+ N005 16µ Rser=1n
L5 Vp2+ N026 16µ Rser=1n
L6 N016 Vs+ 1 Rser=0.346m
L7 Vs- N023 1 Rser=1n
R6 N004 Vp1+ 1Meg
R7 N025 Vp2+ 1Meg
R8 N020 N023 1n
R9 N016 N020 1n
V14 N019 0 {Vo}
C22 N015 N024 90µ ic {Vo/2} Rser=3.93m
C21 N024 N035 90µ ic {Vo/2} Rser=3.93m
R10 Vo N015 1n
R11 N035 0 1n
R12 N005 Vp1- 2650
R13 N026 Vp2- 2650
D13 N014 N003 Dvb
D14 N018 N014 Dvb
C7 N004 N014 610n Rser=10.15m Lser=1.87n
D15 N037 N027 Dvb
D16 0 N037 Dvb
C23 N025 N037 610n Rser=10.15m Lser=1.87n
D17 N002 Vi Dvb
D18 N003 N002 Dvb
C24 N002 Vp1- 610n Rser=10.15m Lser=1.87n
D19 N022 N018 Dvb
D20 N027 N022 Dvb
C25 N022 Vp2- 610n Rser=10.15m Lser=1.87n
L1 Vp1- N005 1.5m Rser=88.5m
L8 Vp2- N026 1.5m Rser=88.5m
V15 N008 0 PULSE(0 5 {phi*T+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
S13 Vs+ Vo N008 0 EPC2023
D21 Vs+ Vo Dideal
C26 Vo Vs+ 1854p
V16 N009 0 PULSE(0 5 {phi*T+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
S14 Vs+ Vo N009 0 EPC2023
D22 Vs+ Vo Dideal
C27 Vo Vs+ 1854p
V17 N029 0 PULSE(0 5 {phi*T+T/2+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
S15 0 Vs+ N029 0 EPC2023
D23 0 Vs+ Dideal
C28 Vs+ 0 1854p
V18 N030 0 PULSE(0 5 {phi*T+T/2+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
S16 0 Vs+ N030 0 EPC2023
D24 0 Vs+ Dideal
C29 Vs+ 0 1854p
V19 N011 0 PULSE(0 5 {phi*T+T/2+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
S17 Vs- Vo N011 0 EPC2023
D25 Vs- Vo Dideal
C30 Vo Vs- 1854p
```

```
V20 N012 0 PULSE(0 5 {phi*T+T/2+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
S18 Vs- Vo N012 0 EPC2023
D26 Vs- Vo Dideal
C31 Vo Vs- 1854p
V21 N032 0 PULSE(0 5 {phi*T+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
S19 0 Vs- N032 0 EPC2023
D27 0 Vs- Dideal
C32 Vs- 0 1854p
V22 N033 0 PULSE(0 5 {phi*T+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
S20 0 Vs- N033 0 EPC2023
D28 0 Vs- Dideal
C33 Vs- 0 1854p
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.params Vi=380 Vo=12 f=175k T=1/f delay=55n delay_r = 20n phi=.0537
.model EPC2012C SW(Ron=105m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 1.5m Roff = 1Meg Vt=1)
.model SIdeal SW(Ron = 5.2m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.model Dvb D(Ron=1n Roff=1Meg Vfwd=1.25)
.tran 0 1545.714u 1500u 0.01u uic
K1 L3 L6 1
K2 L4 L7 1
.MEAS TRAN Iin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T}  TO=5*{T}

.MEAS TRAN Pin AVG -I(V1)*V(Vi) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG I(R5)*V(Vo) FROM 1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T}  TO=5*{T}
.step param phi
list .0519 .0485 .0445 .0395 .035 .0313 .0265 .024 .02 .016 .012 .0118
* Double-Stacked Active Bridge (DSAB) Full-Power Mode - GaN EPC2012C\n3
parallel EPC2023 devices
.backanno
.end
```


Double-Stacked Active Bridge (DSAB) Low-Power Mode - GaN EPC2012C
Vo
Vi
Vp1+
Vp1-
Vp2+
Vp2-
Vs+
Vs-
K1 L3 L6 1
K2 L4 L7 1
EPC2023_OLP
PULSE(0 5 (phi*T+delay_r) 5n 5n (T/2-delay_r) (T)
PULSE(0 5 (phi*T+T/2+delay_r) 5n 5n (T/2-delay_r/2) (T)
PULSE(0 5 (phi*T+T/2-delay_r) 5n 5n (T/2-delay_r/2) (T)
PULSE(0 5 (phi*T+delay_r) 5n 5n (T/2-delay_r) (T)
PULSE(5 5 (100u+delay) 5n 5n (100u-delay) 200u)
.params Vi=380 Vo=12 fs=175k T=1/f delay=55n delay_r = 20n
.step param phi list .098 .09 .08 .07 .066 .061 .058 .055 .053 .0519 .0485 .0445 .0395 .035 .0313 .0265 .024 .02
.model EPC2012C SW(Ron=10m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron=1.5m Roff=1Meg Vt=1)
.model EPC2023_OLP SW(Ron=1.5m Roff=1Meg Vt=1)
.model Sideal SW(Ron = 5.2m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.model Dvb D(Ron=1n Roff=1Meg Vfwd=1.25)
.tran 0 1545.714u 1500u 0.01u uic
.MEAS TRAN Iin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T} TO=5*{T}
.MEAS TRAN Pin AVG -I(V1)*V(Vi) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG I(R5)*V(Vo) FROM 1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T} TO=5*{T}

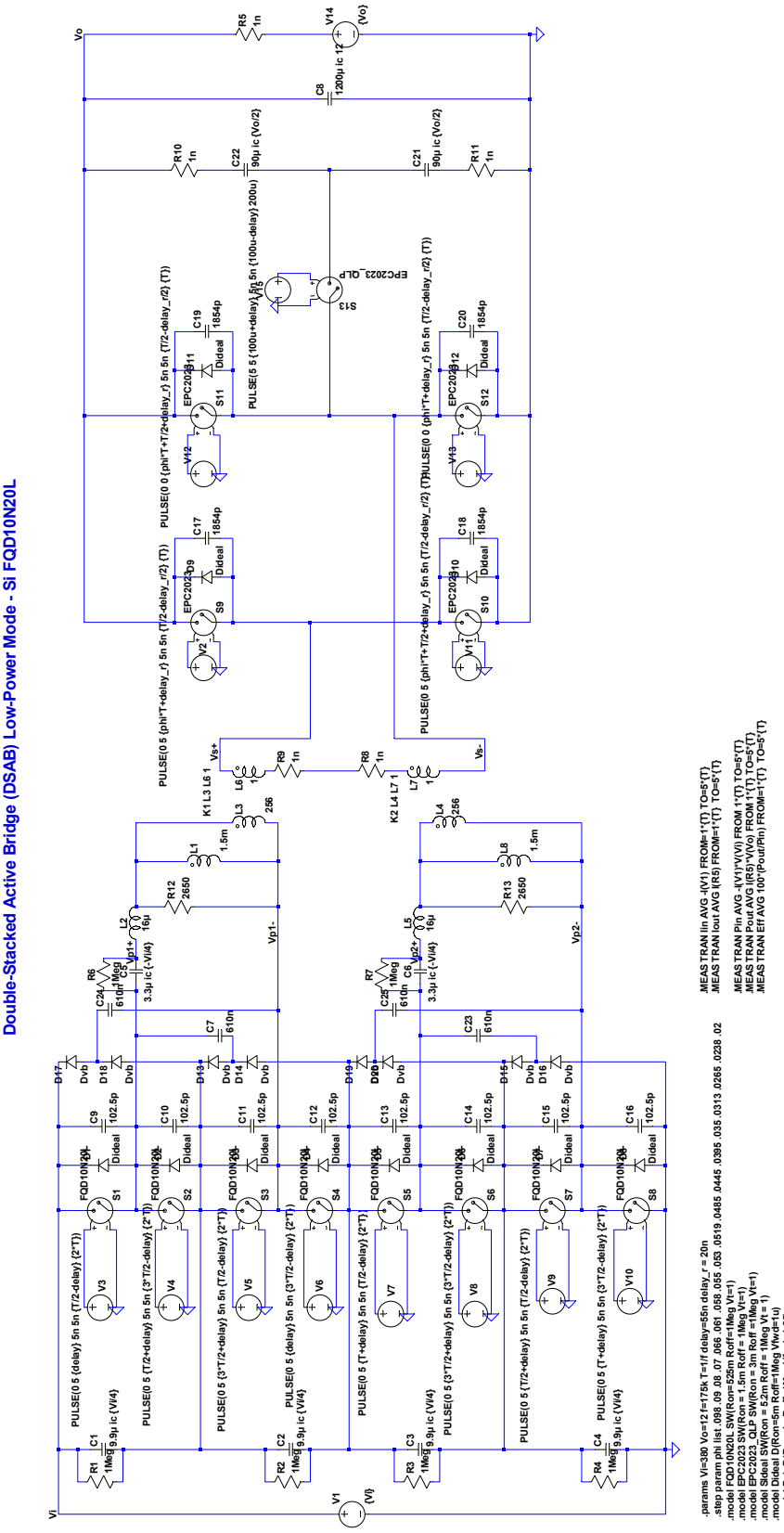
```
* C:\Users\Rose\Dropbox\MIT\MENG\DAB\LTSPICE\Thesis Simulations\Final Versions of
EffCurves\DoubleStackedAB_EPC2012C_LP_alt_pattern.asc
V1 Vi 0 {Vi}
V3 N001 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {2*T})
V4 N006 0 PULSE(0 5 {T/2+delay} 5n 5n {3*T/2-delay} {2*T})
S1 N004 Vi N001 0 EPC2012C
S2 N003 N004 N006 0 EPC2012C
S3 Vp1- N003 N009 0 EPC2012C
S4 N014 Vp1- N013 0 EPC2012C
V5 N009 0 PULSE(0 5 {3*T/2+delay} 5n 5n {T/2-delay} {2*T})
V6 N013 0 PULSE(0 5 {delay} 5n 5n {3*T/2-delay} {2*T})
C1 Vi N003 9.9µ ic {Vi/4}
C2 N003 N014 9.9µ ic {Vi/4}
V7 N019 0 PULSE(0 5 {T+delay} 5n 5n {T/2-delay} {2*T})
V8 N027 0 PULSE(0 5 {3*T/2+delay} 5n 5n {3*T/2-delay} {2*T})
S5 N022 N014 N019 0 EPC2012C
S6 N024 N022 N027 0 EPC2012C
S7 Vp2- N024 N029 0 EPC2012C
S8 0 Vp2- N031 0 EPC2012C
V9 N029 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {2*T})
V10 N031 0 PULSE(0 5 {T+delay} 5n 5n {3*T/2-delay} {2*T})
C3 N014 N024 9.9µ ic {Vi/4}
C4 N024 0 9.9µ ic {Vi/4}
C5 Vp1+ N004 3.3µ ic {-Vi/4}
C6 Vp2+ N022 3.3µ ic {-Vi/4}
L3 Vp1- N005 256 Rser=1n
L4 Vp2- N023 256 Rser=1n
V2 N007 0 PULSE(0 5 {phi*T+delay_r} 5n 5n {T/2-delay_r/2} {T})
V11 N025 0 PULSE(0 5 {phi*T+T/2+delay_r} 5n 5n {T/2-delay_r/2} {T})
S9 Vs+ Vo N007 0 EPC2023
S10 0 Vs+ N025 0 EPC2023
V12 N008 0 PULSE(0 0 {phi*T+T/2+delay_r} 5n 5n {T/2-delay_r/2} {T})
V13 N026 0 PULSE(0 0 {phi*T+delay_r} 5n 5n {T/2-delay_r/2} {T})
S11 Vs- Vo N008 0 EPC2023
S12 0 Vs- N026 0 EPC2023
C8 Vo 0 1200µ ic 12
D1 N004 Vi Dideal
C9 Vi N004 102.5p
D2 N003 N004 Dideal
C10 N004 N003 102.5p
D3 Vp1- N003 Dideal
C11 N003 Vp1- 102.5p
D4 N014 Vp1- Dideal
C12 Vp1- N014 102.5p
D5 N022 N014 Dideal
C13 N014 N022 102.5p
D6 N024 N022 Dideal
C14 N022 N024 102.5p
D7 Vp2- N024 Dideal
C15 N024 Vp2- 102.5p
D8 0 Vp2- Dideal
C16 Vp2- 0 102.5p
D9 Vs+ Vo Dideal
C17 Vo Vs+ 1854p
D10 0 Vs+ Dideal
C18 Vs+ 0 1854p
D11 Vs- Vo Dideal
C19 Vo Vs- 1854p
D12 0 Vs- Dideal
C20 Vs- 0 1854p
R1 Vi N003 1Meg
R2 N003 N014 1Meg
R3 N014 N024 1Meg
```

```
R4 N024 0 1Meg
R5 Vo N017 1n
L2 Vp1+ N005 16µ Rser=1n
L5 Vp2+ N023 16µ Rser=1n
L6 N012 Vs+ 1 Rser=0.346m
L7 Vs- N021 1 Rser=1n
R6 N004 Vp1+ 1Meg
R7 N022 Vp2+ 1Meg
R8 N018 N021 1n
R9 N012 N018 1n
V14 N017 0 {Vo}
C22 N011 N016 90µ ic {Vo/2} Rser=3.93m
C21 N016 N028 90µ ic {Vo/2} Rser=3.93m
R10 Vo N011 1n
R11 N028 0 1n
R12 N005 Vp1- 2650
R13 N023 Vp2- 2650
D13 N010 N003 Dvb
D14 N014 N010 Dvb
C7 N004 N010 610n Rser=10.15m Lser=1.87n
D15 N030 N024 Dvb
D16 0 N030 Dvb
C23 N022 N030 610n Rser=10.15m Lser=1.87n
D17 N002 Vi Dvb
D18 N003 N002 Dvb
C24 N002 Vp1- 610n Rser=10.15m Lser=1.87n
D19 N020 N014 Dvb
D20 N024 N020 Dvb
C25 N020 Vp2- 610n Rser=10.15m Lser=1.87n
L1 Vp1- N005 1.5m Rser=88.5m
L8 Vp2- N023 1.5m Rser=88.5m
V15 N015 0 PULSE(5 5 {100u+delay} 5n 5n {100u-delay} 200u)
S13 Vs- N016 N015 0 EPC2023_QLP
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.params Vi=380 Vo=12 f=175k T=1/f delay=55n delay_r = 20n
.model EPC2012C SW(Ron=105m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 1.5m Roff = 1Meg Vt=1)
.model EPC2023_QLP SW(Ron = 3m Roff =1Meg Vt=1)
.model SIdeal SW(Ron = 5.2m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.model Dvb D(Ron=1n Roff=1Meg Vfwd=1.25)
.tran 0 1545.714u 1500u 0.01u uic
K1 L3 L6 1
K2 L4 L7 1
.MEAS TRAN Iin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T}  TO=5*{T}

.MEAS TRAN Pin AVG -I(V1)*V(Vi) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG I(R5)*V(Vo) FROM 1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T}  TO=5*{T}
.step param phi
list .098 .09 .08 .07 .066 .061 .058 .055 .053 .0519 .0485 .0445 .0395 .035 .0313 .026
5 .024 .02
* Double-Stacked Active Bridge (DSAB) Low-Power Mode - GaN EPC2012C
.backanno
.end
```


Double-Stacked Active Bridge (DSAB) Full-Power Mode - Si FQD10N20L
Vo
Vs+
Vs-
Vp1-
Vp2-
Vi
PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
PULSE(0 5 {phi*T+delay_r} 2.5n 2.5n {T/2-delay_r} {T})
PULSE(0 5 {phi*T+T/2+delay_r} 2.5n 2.5n {T/2-delay_r} {T})
K1 L3 L6 1
K2 L4 L7 1
.params Vi=380 Vo=12 f=175k T=1/f delay=55n delay_r = 20n
.step param phi list .0519 .0485 .0445 .0395 .035 .0313 .0265 .024 .02 .016 .012 .0118
.model FQD10N20L SW(Ron=528m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 1.5m Roff = 1Meg Vt=1)
.model Sideal SW(Ron = 5.2m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.model Dvb D(Ron=1n Roff=1Meg Vfwd=1.25)
.tran 0 1545.714u 1500u 0.01u uic
.MEAS TRAN Iin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T} TO=5*{T}
.MEAS TRAN Pin AVG -I(V1)*V(Vi) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG I(R5)*V(Vo) FROM 1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T} TO=5*{T}

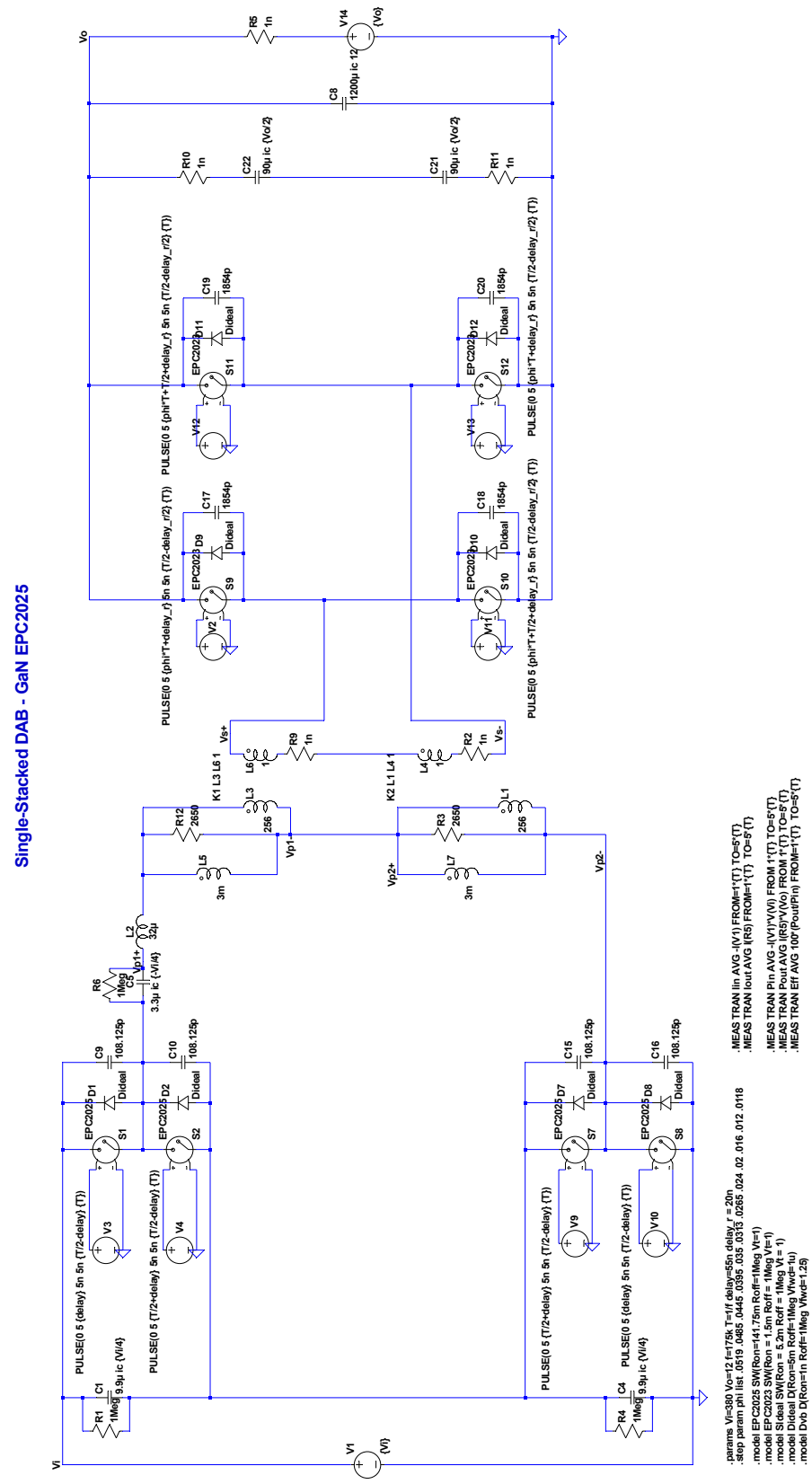
```
* C:\Users\Rose\Dropbox\MIT\MENG\DAB\LTSPICE\Thesis Simulations\Final Versions of
EffCurves\DoubleStackedAB_FQD10N20L_FP.asc
V1 Vi 0 {Vi}
V3 N001 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V4 N006 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S1 N004 Vi N001 0 FQD10N20L
S2 N003 N004 N006 0 FQD10N20L
S3 Vp1- N003 N009 0 FQD10N20L
S4 N014 Vp1- N013 0 FQD10N20L
V5 N009 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V6 N013 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C1 Vi N003 9.9µ ic {Vi/4}
C2 N003 N014 9.9µ ic {Vi/4}
V7 N017 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V8 N026 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S5 N021 N014 N017 0 FQD10N20L
S6 N023 N021 N026 0 FQD10N20L
S7 Vp2- N023 N028 0 FQD10N20L
S8 0 Vp2- N030 0 FQD10N20L
V9 N028 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V10 N030 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C3 N014 N023 9.9µ ic {Vi/4}
C4 N023 0 9.9µ ic {Vi/4}
C5 Vp1+ N004 3.3µ ic {-Vi/4}
C6 Vp2+ N021 3.3µ ic {-Vi/4}
L3 Vp1- N005 256 Rser=1n
L4 Vp2- N022 256 Rser=1n
V2 N007 0 PULSE(0 5 {phi*T+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
V11 N024 0 PULSE(0 5 {phi*T+T/2+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
S9 Vs+ Vo N007 0 EPC2023
S10 0 Vs+ N024 0 EPC2023
V12 N008 0 PULSE(0 5 {phi*T+T/2+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
V13 N025 0 PULSE(0 5 {phi*T+delay_r} 2.5n 2.5n {T/2-delay_r/2} {T})
S11 Vs- Vo N008 0 EPC2023
S12 0 Vs- N025 0 EPC2023
C8 Vo 0 1200µ ic 12
D1 N004 Vi Dideal
C9 Vi N004 116p
D2 N003 N004 Dideal
C10 N004 N003 116p
D3 Vp1- N003 Dideal
C11 N003 Vp1- 116p
D4 N014 Vp1- Dideal
C12 Vp1- N014 116p
D5 N021 N014 Dideal
C13 N014 N021 116p
D6 N023 N021 Dideal
C14 N021 N023 116p
D7 Vp2- N023 Dideal
C15 N023 Vp2- 116p
D8 0 Vp2- Dideal
C16 Vp2- 0 116p
D9 Vs+ Vo Dideal
C17 Vo Vs+ 1854p
D10 0 Vs+ Dideal
C18 Vs+ 0 1854p
D11 Vs- Vo Dideal
C19 Vo Vs- 1854p
D12 0 Vs- Dideal
C20 Vs- 0 1854p
R1 Vi N003 1Meg
R2 N003 N014 1Meg
R3 N014 N023 1Meg
```

```
R4 N023 0 1Meg
R5 Vo N015 1n
L2 Vp1+ N005 16µ Rser=1n
L5 Vp2+ N022 16µ Rser=1n
L6 N012 Vs+ 1 Rser=0.346m
L7 Vs- N019 1 Rser=1n
R6 N004 Vp1+ 1Meg
R7 N021 Vp2+ 1Meg
R8 N016 N019 1n
R9 N012 N016 1n
V14 N015 0 {Vo}
C22 N011 N020 90µ ic {Vo/2} Rser=3.93m
C21 N020 N027 90µ ic {Vo/2} Rser=3.93m
R10 Vo N011 1n
R11 N027 0 1n
R12 N005 Vp1- 2650
R13 N022 Vp2- 2650
D13 N010 N003 Dvb
D14 N014 N010 Dvb
C7 N004 N010 610n Rser=10.15m Lser=1.87n
D15 N029 N023 Dvb
D16 0 N029 Dvb
C23 N021 N029 610n Rser=10.15m Lser=1.87n
D17 N002 Vi Dvb
D18 N003 N002 Dvb
C24 N002 Vp1- 610n Rser=10.15m Lser=1.87n
D19 N018 N014 Dvb
D20 N023 N018 Dvb
C25 N018 Vp2- 610n Rser=10.15m Lser=1.87n
L1 Vp1- N005 1.5m Rser=88.5m
L8 Vp2- N022 1.5m Rser=88.5m
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.params Vi=380 Vo=12 f=175k T=1/f delay=55n delay_r = 20n
.model FQD10N20L SW(Ron=525m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 1.5m Roff = 1Meg Vt=1)
.model SIdeal SW(Ron = 5.2m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.model Dvb D(Ron=1n Roff=1Meg Vfwd=1.25)
.tran 0 1545.714u 1500u 0.01u uic
K1 L3 L6 1
K2 L4 L7 1
.MEAS TRAN Iin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T}  TO=5*{T}

.MEAS TRAN Pin AVG -I(V1)*V(Vi) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG I(R5)*V(Vo) FROM 1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T}  TO=5*{T}
.step param phi list .0519 .0485 .0445 .0395 .035 .0313 .0265 .024 .02 .016 .012 .0118
.backanno
.end
```


Double-Stacked Active Bridge (DSAB) Low-Power Mode - Si FQD10N20L
.params Vi=380 Vo=12 f=175k T=1/f delay=55n delay_r = 20n
.step param phi list .098 .09 .08 .07 .066 .061 .058 .055 .053 .0519 .0485 .0445 .0395 .035 .0313 .0265 .0238 .02
.model FQD10N20L SW(Ron=525m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 1.5m Roff = 1Meg Vt=1)
.model EPC2023_QLP SW(Ron = 3m Roff =1Meg Vt = 1)
.model Sideal SW(Ron = 52m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=10m Roff=1Meg Vfwd=1.1)
.model Dvb D(Ron=1n Roff=1Meg Vfwd=1.25)
.tran 0 1545.714u 1500u 0.01u uic
.MEAS TRAN Iin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T} TO=5*{T}
.MEAS TRAN Pin AVG -I(V1)*V(Vi) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG I(R5)*V(Vo) FROM=1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T} TO=5*{T}

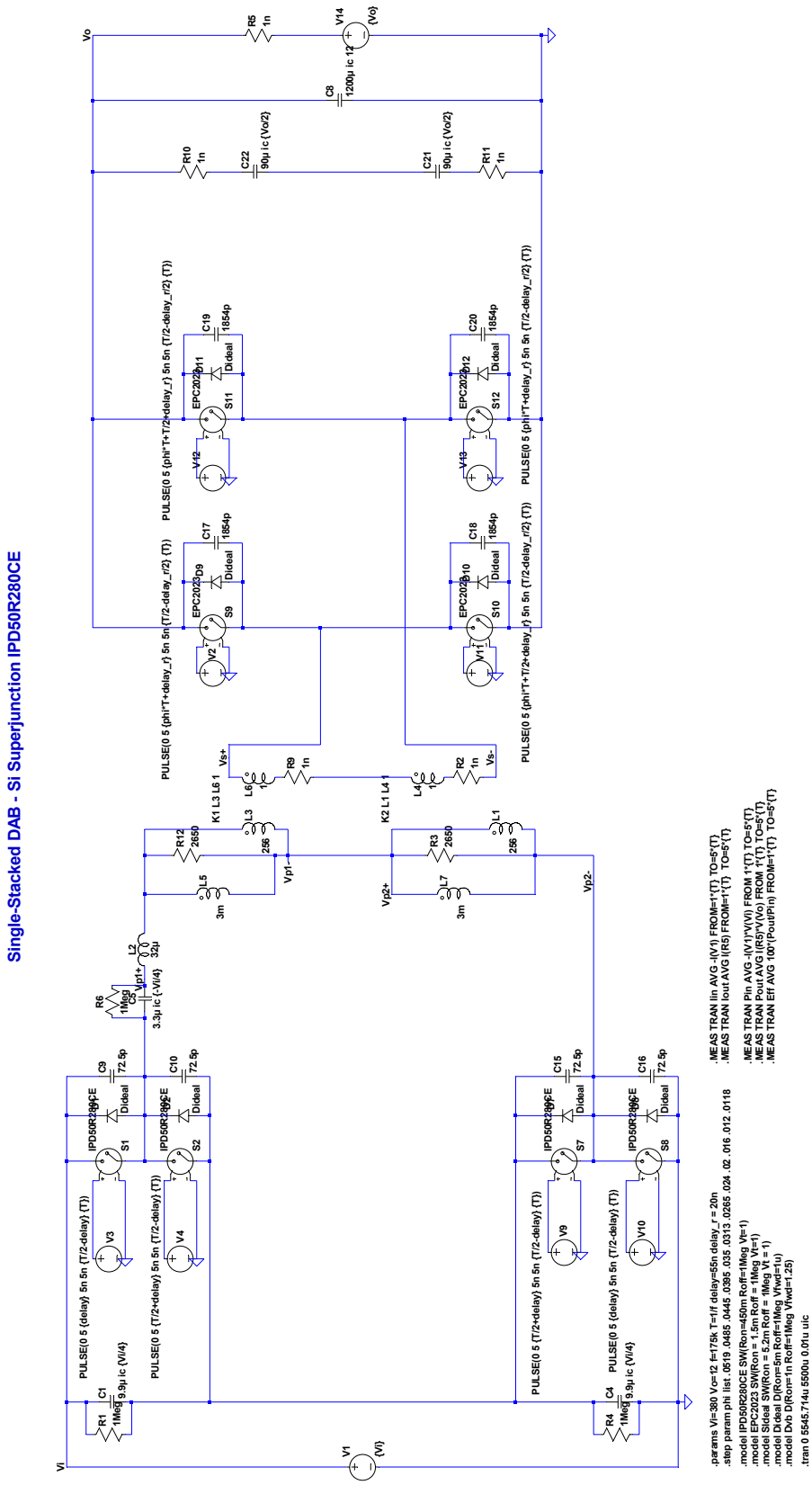
```
* C:\Users\Rose\Dropbox\MIT\MENG\DAB\LTSPICE\Thesis Simulations\Final Versions of
EffCurves\DoubleStackedAB_FQD10N20L_LP_alt_pattern.asc
V1 Vi 0 {Vi}
V3 N001 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {2*T})
V4 N006 0 PULSE(0 5 {T/2+delay} 5n 5n {3*T/2-delay} {2*T})
S1 N004 Vi N001 0 FQD10N20L
S2 N003 N004 N006 0 FQD10N20L
S3 Vp1- N003 N009 0 FQD10N20L
S4 N014 Vp1- N013 0 FQD10N20L
V5 N009 0 PULSE(0 5 {3*T/2+delay} 5n 5n {T/2-delay} {2*T})
V6 N013 0 PULSE(0 5 {delay} 5n 5n {3*T/2-delay} {2*T})
C1 Vi N003 9.9µ ic {Vi/4}
C2 N003 N014 9.9µ ic {Vi/4}
V7 N019 0 PULSE(0 5 {T+delay} 5n 5n {T/2-delay} {2*T})
V8 N027 0 PULSE(0 5 {3*T/2+delay} 5n 5n {3*T/2-delay} {2*T})
S5 N022 N014 N019 0 FQD10N20L
S6 N024 N022 N027 0 FQD10N20L
S7 Vp2- N024 N029 0 FQD10N20L
S8 0 Vp2- N031 0 FQD10N20L
V9 N029 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {2*T})
V10 N031 0 PULSE(0 5 {T+delay} 5n 5n {3*T/2-delay} {2*T})
C3 N014 N024 9.9µ ic {Vi/4}
C4 N024 0 9.9µ ic {Vi/4}
C5 Vp1+ N004 3.3µ ic {-Vi/4}
C6 Vp2+ N022 3.3µ ic {-Vi/4}
L3 Vp1- N005 256 Rser=1n
L4 Vp2- N023 256 Rser=1n
V2 N007 0 PULSE(0 5 {phi*T+delay_r} 5n 5n {T/2-delay_r/2} {T})
V11 N025 0 PULSE(0 5 {phi*T+T/2+delay_r} 5n 5n {T/2-delay_r/2} {T})
S9 Vs+ Vo N007 0 EPC2023
S10 0 Vs+ N025 0 EPC2023
V12 N008 0 PULSE(0 0 {phi*T+T/2+delay_r} 5n 5n {T/2-delay_r/2} {T})
V13 N026 0 PULSE(0 0 {phi*T+delay_r} 5n 5n {T/2-delay_r/2} {T})
S11 Vs- Vo N008 0 EPC2023
S12 0 Vs- N026 0 EPC2023
C8 Vo 0 1200µ ic 12
D1 N004 Vi Dideal
C9 Vi N004 102.5p
D2 N003 N004 Dideal
C10 N004 N003 102.5p
D3 Vp1- N003 Dideal
C11 N003 Vp1- 102.5p
D4 N014 Vp1- Dideal
C12 Vp1- N014 102.5p
D5 N022 N014 Dideal
C13 N014 N022 102.5p
D6 N024 N022 Dideal
C14 N022 N024 102.5p
D7 Vp2- N024 Dideal
C15 N024 Vp2- 102.5p
D8 0 Vp2- Dideal
C16 Vp2- 0 102.5p
D9 Vs+ Vo Dideal
C17 Vo Vs+ 1854p
D10 0 Vs+ Dideal
C18 Vs+ 0 1854p
D11 Vs- Vo Dideal
C19 Vo Vs- 1854p
D12 0 Vs- Dideal
C20 Vs- 0 1854p
R1 Vi N003 1Meg
R2 N003 N014 1Meg
R3 N014 N024 1Meg
```

```
R4 N024 0 1Meg
R5 Vo N017 1n
L2 Vp1+ N005 16µ Rser=1n
L5 Vp2+ N023 16µ Rser=1n
L6 N012 Vs+ 1 Rser=0.346m
L7 Vs- N021 1 Rser=1n
R6 N004 Vp1+ 1Meg
R7 N022 Vp2+ 1Meg
R8 N018 N021 1n
R9 N012 N018 1n
V14 N017 0 {Vo}
C22 N011 N016 90µ ic {Vo/2} Rser=3.93m
C21 N016 N028 90µ ic {Vo/2} Rser=3.93m
R10 Vo N011 1n
R11 N028 0 1n
R12 N005 Vp1- 2650
R13 N023 Vp2- 2650
D13 N010 N003 Dvb
D14 N014 N010 Dvb
C7 N004 N010 610n Rser=10.15m Lser=1.87n
D15 N030 N024 Dvb
D16 0 N030 Dvb
C23 N022 N030 610n Rser=10.15m Lser=1.87n
D17 N002 Vi Dvb
D18 N003 N002 Dvb
C24 N002 Vp1- 610n Rser=10.15m Lser=1.87n
D19 N020 N014 Dvb
D20 N024 N020 Dvb
C25 N020 Vp2- 610n Rser=10.15m Lser=1.87n
L1 Vp1- N005 1.5m Rser=88.5m
L8 Vp2- N023 1.5m Rser=88.5m
V15 N015 0 PULSE(5 5 {100u+delay} 5n 5n {100u-delay} 200u)
S13 Vs- N016 N015 0 EPC2023_QLP
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.params Vi=380 Vo=12 f=175k T=1/f delay=55n delay_r = 20n
.model FQD10N20L SW(Ron=525m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 1.5m Roff = 1Meg Vt=1)
.model EPC2023_QLP SW(Ron = 3m Roff =1Meg Vt=1)
.model SIdeal SW(Ron = 5.2m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.model Dvb D(Ron=1n Roff=1Meg Vfwd=1.25)
.tran 0 1545.714u 1500u 0.01u uic
K1 L3 L6 1
K2 L4 L7 1
.MEAS TRAN Iin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T}  TO=5*{T}

.MEAS TRAN Pin AVG -I(V1)*V(Vi) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG I(R5)*V(Vo) FROM 1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T}  TO=5*{T}
.step param phi
list .098 .09 .08 .07 .066 .061 .058 .055 .053 .0519 .0485 .0445 .0395 .035 .0313 .026
5 .0238 .02
* Double-Stacked Active Bridge (DSAB) Low-Power Mode - Si FQD10N20L
.backanno
.end
```


Single-Stacked DAB - GaN EPC2025
Vi
Vo
Vp1+
Vp1-
Vp2+
Vp2-
Vs+
Vs-
PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
PULSE(0 5 {phi*T+T/2+delay_r} 5n 5n {T/2-delay_r/2} {T})
PULSE(0 5 {phi*T+delay_r} 5n 5n {T/2-delay_r/2} {T})
PULSE(0 5 {phi*T+T/2+delay_r} 5n 5n {T/2-delay_r/2} {T})
PULSE(0 5 {phi*T+delay_r} 5n 5n {T/2-delay_r/2} {T})
EPC2025
Dideal
K1 L3 L6 1
K2 L1 L4 1
.MEAS TRAN lin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T} TO=5*{T}
.MEAS TRAN Pin AVG -I(V1)*V(Vi) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG I(R5)*V(Vo) FROM 1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T} TO=5*{T}
.params Vi=380 Vo=12 f=175k T=1/f delay=55n delay_r = 20n
.step param phi list .0519 .0485 .0445 .0395 .035 .0315 .0265 .024 .02 .016 .012 .0118
.model EPC2025 SW(Ron=141.75m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 1.5m Roff = 1Meg Vt=1)
.model Sideal SW(Ron = 5.2m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.model Dvb D(Ron=1n Roff=1Meg Vfwd=1.29)
.tran 0 5545.714u 5500u 0.01u uic

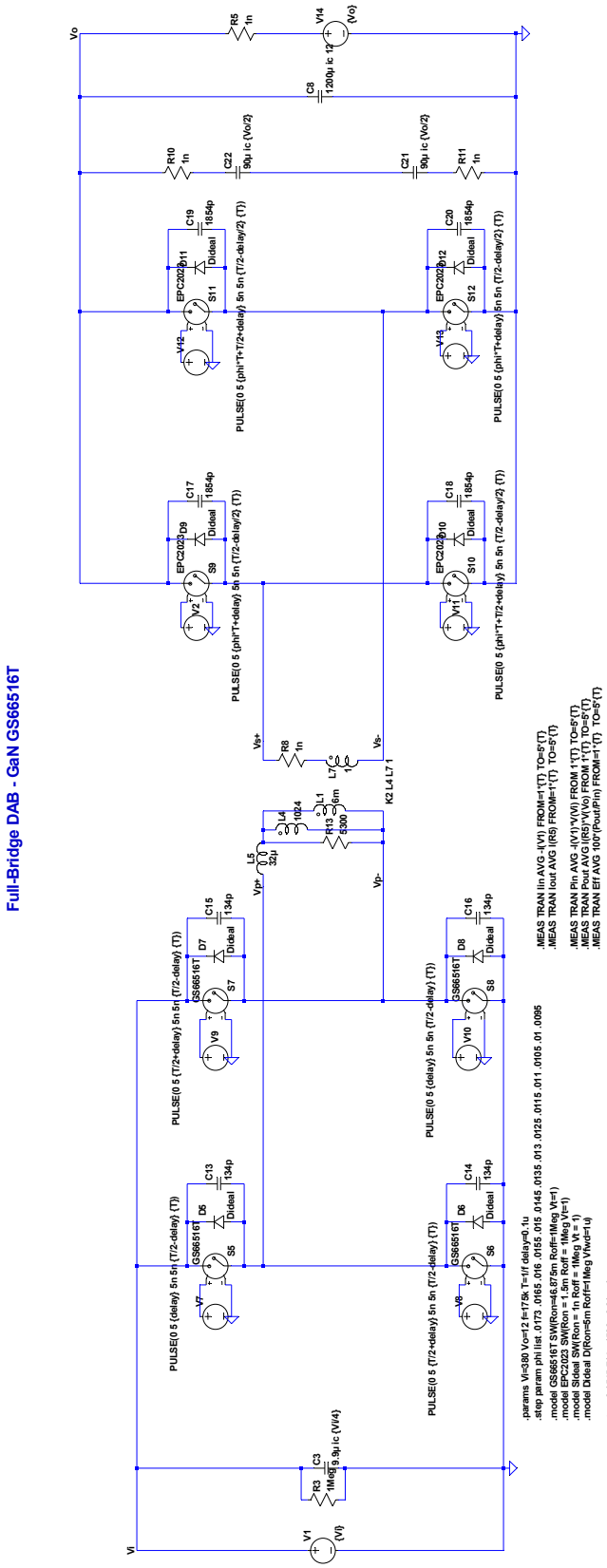
```
* C:\Users\Rose\Dropbox (MIT Solar Car Team)\MIT\MENG\DAB\LTSPICE\Thesis
Simulations\Final Versions of
EffCurves\SingleStackedDAB_EPC2025_series_connected_primaries.asc
V1 Vi 0 {Vi}
V3 N001 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V4 N005 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S1 N003 Vi N001 0 EPC2025
S2 N002 N003 N005 0 EPC2025
C1 Vi N002 9.9µ ic {Vi/4}
S7 Vp2- N002 N017 0 EPC2025
S8 0 Vp2- N018 0 EPC2025
V9 N017 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V10 N018 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C4 N002 0 9.9µ ic {Vi/4}
C5 Vp1+ N003 3.3µ ic {-Vi/4}
L3 Vp2+ N004 256 Rser=1n
V2 N006 0 PULSE(0 5 {phi*T+delay_r} 5n 5n {T/2-delay_r/2} {T})
V11 N014 0 PULSE(0 5 {phi*T+T/2+delay_r} 5n 5n {T/2-delay_r/2} {T})
S9 Vs+ Vo N006 0 EPC2023
S10 0 Vs+ N014 0 EPC2023
V12 N007 0 PULSE(0 5 {phi*T+T/2+delay_r} 5n 5n {T/2-delay_r/2} {T})
V13 N015 0 PULSE(0 5 {phi*T+delay_r} 5n 5n {T/2-delay_r/2} {T})
S11 Vs- Vo N007 0 EPC2023
S12 0 Vs- N015 0 EPC2023
C8 Vo 0 1200µ ic 12
D1 N003 Vi Dideal
C9 Vi N003 108.125p
D2 N002 N003 Dideal
C10 N003 N002 108.125p
D7 Vp2- N002 Dideal
C15 N002 Vp2- 108.125p
D8 0 Vp2- Dideal
C16 Vp2- 0 108.125p
D9 Vs+ Vo Dideal
C17 Vo Vs+ 1854p
D10 0 Vs+ Dideal
C18 Vs+ 0 1854p
D11 Vs- Vo Dideal
C19 Vo Vs- 1854p
D12 0 Vs- Dideal
C20 Vs- 0 1854p
R1 Vi N002 1Meg
R4 N002 0 1Meg
R5 Vo N010 1n
L2 Vp1+ N004 32µ Rser=1n
L6 N009 Vs+ 1 Rser=0.346m
R6 N003 Vp1+ 1Meg
R9 N009 N011 1n
V14 N010 0 {Vo}
C22 N008 N012 90µ ic {Vo/2} Rser=3.93m
C21 N012 N016 90µ ic {Vo/2} Rser=3.93m
R10 Vo N008 1n
R11 N016 0 1n
R12 N004 Vp2+ 2650
L1 Vp2- Vp2+ 256 Rser=1n
L4 N013 N011 1 Rser=1n
R2 N013 Vs- 1n
```

```
R3 Vp2+ Vp2- 2650
L5 Vp2+ N004 3m Rser=88.5m
L7 Vp2- Vp2+ 3m Rser=88.5m
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.params Vi=380 Vo=12 f=175k T=1/f delay=55n delay_r = 20n
.model EPC2025 SW(Ron=141.75m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 1.5m Roff = 1Meg Vt=1)
.model SIdeal SW(Ron = 5.2m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.model Dvb D(Ron=1n Roff=1Meg Vfwd=1.25)
.tran 0 5545.714u 5500u 0.01u uic
K1 L3 L6 1
.MEAS TRAN Iin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T}  TO=5*{T}

.MEAS TRAN Pin AVG -I(V1)*V(Vi) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG I(R5)*V(Vo) FROM 1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T}  TO=5*{T}
K2 L1 L4 1
.step param phi
list .0519 .0485 .0445 .0395 .035 .0313 .0265 .024 .02 .016 .012 .0118
* Single-Stacked DAB - GaN EPC2025
.backanno
.end
```


Single-Stacked DAB - Si Superjunction IPD50R280CE
Vo
Vi
Vs+
Vs-
Vp1+
Vp1-
Vp2+
Vp2-
K1 L3 L6 1
K2 L1 L4 1
R5 1n
V14 {Vo}
C8 1200µ ic 12
R10 1n
C22 90µ ic {Vo/2}
C21 90µ ic {Vo/2}
R11 1n
R9 1n
R2 1n
R12 265Ω
R3 265Ω
L3 25n
L1 25n
L5 3m
L7 3m
L2 32µ
R6 1Meg
3.3µ ic {-Vi/4}
C9 72.5p
C10 72.5p
C15 72.5p
C16 72.5p
C1 9.9µ ic {Vi/4}
C4 9.9µ ic {Vi/4}
R1 1Meg
R4 1Meg
V1 {Vi}
V3 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V4 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V9 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V10 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V2 PULSE(0 5 {phi*T+delay_r} 5n 5n {T/2-delay_r/2} {T})
V11 PULSE(0 5 {phi*T+T/2+delay_r} 5n 5n {T/2-delay_r/2} {T})
V12 PULSE(0 5 {phi*T+T/2+delay_r} 5n 5n {T/2-delay_r/2} {T})
V13 PULSE(0 5 {phi*T+delay_r} 5n 5n {T/2-delay_r/2} {T})
S1 S2 S7 S8 S9 S10 S11 S12
D9 D10 D11 D12
C17 1854p
C18 1854p
C19 1854p
C20 1854p
EPC2023
Dideal
IPD50R280CE
.params Vi=380 Vo=12 f=175k T=1/f delay=55n delay_r = 20n
.step param phi list .0519 .0485 .0445 .0395 .035 .0313 .0265 .024 .02 .016 .012 .0118
.model IPD50R280CE SW(Ron=450m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 1.5m Roff = 1Meg Vt=1)
.model Sideal SW(Ron = 5.2m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=1m Roff=1Meg Vfwd=1u)
.model Dob D(Ron=1n Roff=1Meg Vfwd=1.25)
.tran 0 5545.714u 5500u 0.01u uic
.MEAS TRAN Iin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T} TO=5*{T}
.MEAS TRAN Pin AVG -I(V1)*V(Vi) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG I(R5)*V(Vo) FROM 1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T} TO=5*{T}

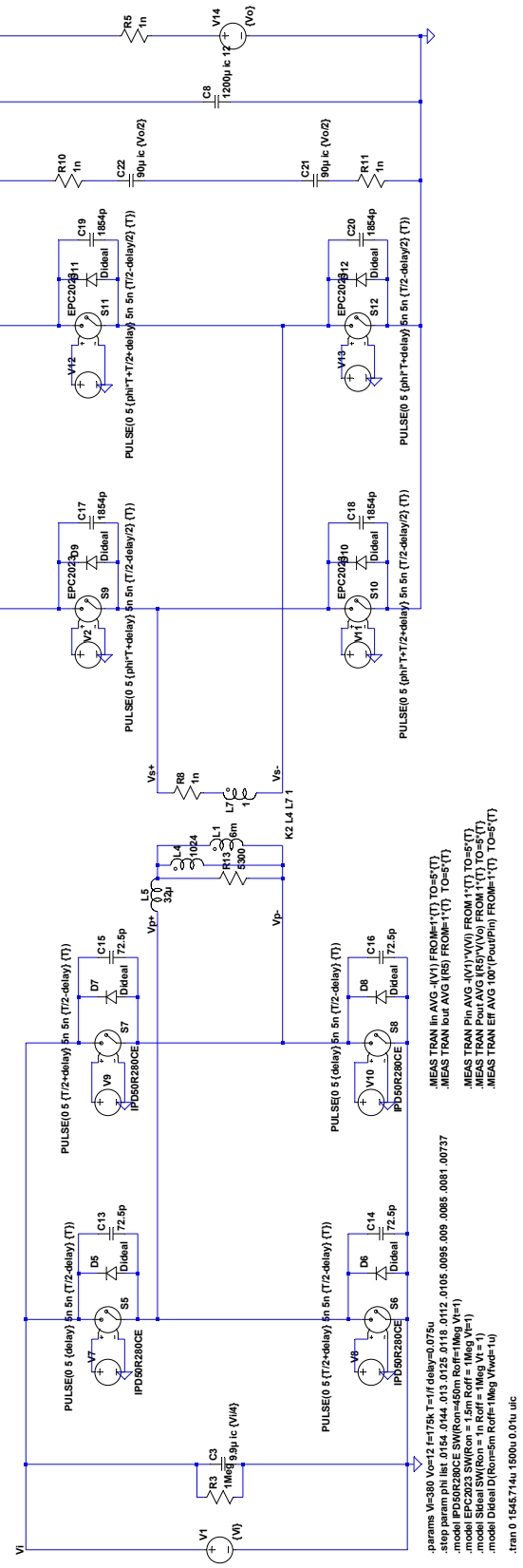
```
* C:\Users\Rose\Dropbox (MIT Solar Car Team)\MIT\MENG\DAB\LTSPICE\Thesis
Simulations\Final Versions of
EffCurves\SingleStackedDAB_IPD50R280CE_series_connected_primaries.asc
V1 Vi 0 {Vi}
V3 N001 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V4 N005 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S1 N003 Vi N001 0 IPD50R280CE
S2 N002 N003 N005 0 IPD50R280CE
C1 Vi N002 9.9µ ic {Vi/4}
S7 Vp2- N002 N017 0 IPD50R280CE
S8 0 Vp2- N018 0 IPD50R280CE
V9 N017 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V10 N018 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C4 N002 0 9.9µ ic {Vi/4}
C5 Vp1+ N003 3.3µ ic {-Vi/4}
L3 Vp2+ N004 256 Rser=1n
V2 N006 0 PULSE(0 5 {phi*T+delay_r} 5n 5n {T/2-delay_r/2} {T})
V11 N014 0 PULSE(0 5 {phi*T+T/2+delay_r} 5n 5n {T/2-delay_r/2} {T})
S9 Vs+ Vo N006 0 EPC2023
S10 0 Vs+ N014 0 EPC2023
V12 N007 0 PULSE(0 5 {phi*T+T/2+delay_r} 5n 5n {T/2-delay_r/2} {T})
V13 N015 0 PULSE(0 5 {phi*T+delay_r} 5n 5n {T/2-delay_r/2} {T})
S11 Vs- Vo N007 0 EPC2023
S12 0 Vs- N015 0 EPC2023
C8 Vo 0 1200µ ic 12
D1 N003 Vi Dideal
C9 Vi N003 72.5p
D2 N002 N003 Dideal
C10 N003 N002 72.5p
D7 Vp2- N002 Dideal
C15 N002 Vp2- 72.5p
D8 0 Vp2- Dideal
C16 Vp2- 0 72.5p
D9 Vs+ Vo Dideal
C17 Vo Vs+ 1854p
D10 0 Vs+ Dideal
C18 Vs+ 0 1854p
D11 Vs- Vo Dideal
C19 Vo Vs- 1854p
D12 0 Vs- Dideal
C20 Vs- 0 1854p
R1 Vi N002 1Meg
R4 N002 0 1Meg
R5 Vo N010 1n
L2 Vp1+ N004 32µ Rser=1n
L6 N009 Vs+ 1 Rser=0.346m
R6 N003 Vp1+ 1Meg
R9 N009 N011 1n
V14 N010 0 {Vo}
C22 N008 N012 90µ ic {Vo/2} Rser=3.93m
C21 N012 N016 90µ ic {Vo/2} Rser=3.93m
R10 Vo N008 1n
R11 N016 0 1n
R12 N004 Vp2+ 2650
L1 Vp2- Vp2+ 256 Rser=1n
L4 N013 N011 1 Rser=1n
R2 N013 Vs- 1n
```

```
R3 Vp2+ Vp2- 2650
L5 Vp2+ N004 3m Rser=88.5m
L7 Vp2- Vp2+ 3m Rser=88.5m
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.params Vi=380 Vo=12 f=175k T=1/f delay=55n delay_r = 20n
.model IPD50R280CE SW(Ron=450m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 1.5m Roff = 1Meg Vt=1)
.model SIdeal SW(Ron = 5.2m Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.model Dvb D(Ron=1n Roff=1Meg Vfwd=1.25)
.tran 0 5545.714u 5500u 0.01u uic
K1 L3 L6 1
.MEAS TRAN Iin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T}  TO=5*{T}

.MEAS TRAN Pin AVG -I(V1)*V(Vi) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG I(R5)*V(Vo) FROM 1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T}  TO=5*{T}
K2 L1 L4 1
.step param phi
list .0519 .0485 .0445 .0395 .035 .0313 .0265 .024 .02 .016 .012 .0118
* Single-Stacked DAB - Si Superjunction IPD50R280CE
.backanno
.end
```


Full-Bridge DAB - GaN GS66516T
Vo
R5 1n
V14 (Vo)
C8 1200µ ic 12
R10 1n
C22 90µ ic {Vo/2}
C21 90µ ic {Vo/2}
R11 1n
C19 1854p
C20 1854p
EPC2023 D11 S11 Dideal
EPC2023 D12 S12 Dideal
V12
V13
PULSE(0 5 {phi*T+T/2+delay} 5n 5n {T/2-delay/2} {T})
C17 1854p
C18 1854p
EPC2023 D9 S9 Dideal
EPC2023 D10 S10 Dideal
V9
V11
PULSE(0 5 {phi*T+delay} 5n 5n {T/2-delay/2} {T})
Vs+
R8 1n
L7 1
Vs-
K2 L4 L7 1
L4 1024
L1 6m
R19 5300
L5 30µ
Vp+
Vp-
C15 134p
C16 134p
GS66516T D7 S7 Dideal
GS66516T D8 S8 Dideal
V7
V8
PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C13 134p
C14 134p
GS66516T D5 S5 Dideal
GS66516T D6 S6 Dideal
V5
V6
PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
Vi
V1 {Vi}
R3 1Meg
C3 9.9µ ic {Vi/4}
.params Vi=380 Vo=12 f=175k T=1/f delay=0.1u
.step param phi list .0173 .0165 .016 .0155 .015 .0145 .0135 .013 .0125 .0115 .011 .0105 .01 .0095
.model GS66516T SW(Ron=46.875m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 1.5m Roff = 1Meg Vt=1)
.model Sideal SW(Ron = 1n Roff = 1Meg Vt = 1)
.model Dideal D(Ron=6m Roff=1Meg Vfwd=1u)
.tran 0 1545.714u 1500u 0.01u uic
.MEAS TRAN Iin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T} TO=5*{T}
.MEAS TRAN Pin AVG -I(V1)*V(Vi) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG I(R5)*V(Vo) FROM 1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T} TO=5*{T}

```
* C:\Users\Rose\Dropbox (MIT Solar Car Team)\MIT\MENG\DAB\LTSPICE\Thesis Simulations\Final
Versions of EffCurves\FullBridgeDAB_GS66516T.asc
V1 Vi 0 {Vi}
V7 N003 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V8 N014 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S5 Vp+ Vi N003 0 GS66516T
S6 0 Vp+ N014 0 GS66516T
S7 Vp- Vi N004 0 GS66516T
S8 0 Vp- N012 0 GS66516T
V9 N004 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V10 N012 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C3 Vi 0 9.9µ ic {Vi/4}
L4 Vp- N006 1024 Rser=1n
V2 N001 0 PULSE(0 5 {phi*T+delay} 5n 5n {T/2-delay/2} {T})
V11 N010 0 PULSE(0 5 {phi*T+T/2+delay} 5n 5n {T/2-delay/2} {T})
S9 Vs+ Vo N001 0 EPC2023
S10 0 Vs+ N010 0 EPC2023
V12 N002 0 PULSE(0 5 {phi*T+T/2+delay} 5n 5n {T/2-delay/2} {T})
V13 N011 0 PULSE(0 5 {phi*T+delay} 5n 5n {T/2-delay/2} {T})
S11 Vs- Vo N002 0 EPC2023
S12 0 Vs- N011 0 EPC2023
C8 Vo 0 1200µ ic 12
D5 Vp+ Vi Dideal
C13 Vi Vp+ 134p
D6 0 Vp+ Dideal
C14 Vp+ 0 134p
D7 Vp- Vi Dideal
C15 Vi Vp- 134p
D8 0 Vp- Dideal
C16 Vp- 0 134p
D9 Vs+ Vo Dideal
C17 Vo Vs+ 1854p
D10 0 Vs+ Dideal
C18 Vs+ 0 1854p
D11 Vs- Vo Dideal
C19 Vo Vs- 1854p
D12 0 Vs- Dideal
C20 Vs- 0 1854p
R3 Vi 0 1Meg
R5 Vo N007 1n
L5 Vp+ N006 32µ Rser=1n
L7 Vs- N008 1 Rser=.346m
R8 Vs+ N008 1n
V14 N007 0 {Vo}
C22 N005 N009 90µ ic {Vo/2}
C21 N009 N013 90µ ic {Vo/2}
R10 Vo N005 1n
R11 N013 0 1n
R13 N006 Vp- 5300
L1 Vp- N006 6m Rser=117m
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.params Vi=380 Vo=12 f=175k T=1/f delay=0.1u
.model GS66516T SW(Ron=46.875m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 1.5m Roff = 1Meg Vt=1)
.model SIdeal SW(Ron = 1n Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.tran 0 1545.714u 1500u 0.01u uic
K2 L4 L7 1
.MEAS TRAN Iin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T}  TO=5*{T}

.MEAS TRAN Pin AVG -I(V1)*V(Vi) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG I(R5)*V(Vo) FROM 1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T}  TO=5*{T}
.step param phi
list .0173 .0165 .016 .0155 .015 .0145 .0135 .013 .0125 .0115 .011 .0105 .01 .0095
* Full-Bridge DAB - GaN GS66516T
.backanno
.end
```

Full-Bridge DAB - Si Superjunction IPD50R280CE



```
* C:\Users\Rose\Dropbox (MIT Solar Car Team)\MIT\MENG\DAB\LTSPICE\Thesis Simulations\Final
Versions of EffCurves\FullBridgeDAB_IPD50R280CE.asc
V1 Vi 0 {Vi}
V7 N003 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
V8 N012 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
S5 Vp+ Vi N003 0 IPD50R280CE
S6 0 Vp+ N012 0 IPD50R280CE
S7 Vp- Vi N004 0 IPD50R280CE
S8 0 Vp- N013 0 IPD50R280CE
V9 N004 0 PULSE(0 5 {T/2+delay} 5n 5n {T/2-delay} {T})
V10 N013 0 PULSE(0 5 {delay} 5n 5n {T/2-delay} {T})
C3 Vi 0 9.9µ ic {Vi/4}
L4 Vp- N006 1024 Rser=1n
V2 N001 0 PULSE(0 5 {phi*T+delay} 5n 5n {T/2-delay/2} {T})
V11 N010 0 PULSE(0 5 {phi*T+T/2+delay} 5n 5n {T/2-delay/2} {T})
S9 Vs+ Vo N001 0 EPC2023
S10 0 Vs+ N010 0 EPC2023
V12 N002 0 PULSE(0 5 {phi*T+T/2+delay} 5n 5n {T/2-delay/2} {T})
V13 N011 0 PULSE(0 5 {phi*T+delay} 5n 5n {T/2-delay/2} {T})
S11 Vs- Vo N002 0 EPC2023
S12 0 Vs- N011 0 EPC2023
C8 Vo 0 1200µ ic 12
D5 Vp+ Vi Dideal
C13 Vi Vp+ 72.5p
D6 0 Vp+ Dideal
C14 Vp+ 0 72.5p
D7 Vp- Vi Dideal
C15 Vi Vp- 72.5p
D8 0 Vp- Dideal
C16 Vp- 0 72.5p
D9 Vs+ Vo Dideal
C17 Vo Vs+ 1854p
D10 0 Vs+ Dideal
C18 Vs+ 0 1854p
D11 Vs- Vo Dideal
C19 Vo Vs- 1854p
D12 0 Vs- Dideal
C20 Vs- 0 1854p
R3 Vi 0 1Meg
R5 Vo N007 1n
L5 Vp+ N006 32µ Rser=1n
L7 Vs- N008 1 Rser=.346m
R8 Vs+ N008 1n
V14 N007 0 {Vo}
C22 N005 N009 90µ ic {Vo/2}
C21 N009 N014 90µ ic {Vo/2}
R10 Vo N005 1n
R11 N014 0 1n
R13 N006 Vp- 5300
L1 Vp- N006 6m Rser=117m
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.params Vi=380 Vo=12 f=175k T=1/f delay=0.075u
.model IPD50R280CE SW(Ron=450m Roff=1Meg Vt=1)
.model EPC2023 SW(Ron = 1.5m Roff = 1Meg Vt=1)
.model SIdeal SW(Ron = 1n Roff = 1Meg Vt = 1)
.model Dideal D(Ron=5m Roff=1Meg Vfwd=1u)
.tran 0 1545.714u 1500u 0.01u uic
K2 L4 L7 1
.MEAS TRAN Iin AVG -I(V1) FROM=1*{T} TO=5*{T}
.MEAS TRAN Iout AVG I(R5) FROM=1*{T}  TO=5*{T}

.MEAS TRAN Pin AVG -I(V1)*V(Vi) FROM 1*{T} TO=5*{T}
.MEAS TRAN Pout AVG I(R5)*V(Vo) FROM 1*{T} TO=5*{T}
.MEAS TRAN Eff AVG 100*(Pout/Pin) FROM=1*{T}  TO=5*{T}
.step param phi list .0154 .0144 .013 .0125 .0118 .0112 .0105 .0095 .009 .0085 .0081 .00737
* Full-Bridge DAB - Si Superjunction IPD50R280CE
.backanno
.end
```

Appendix C

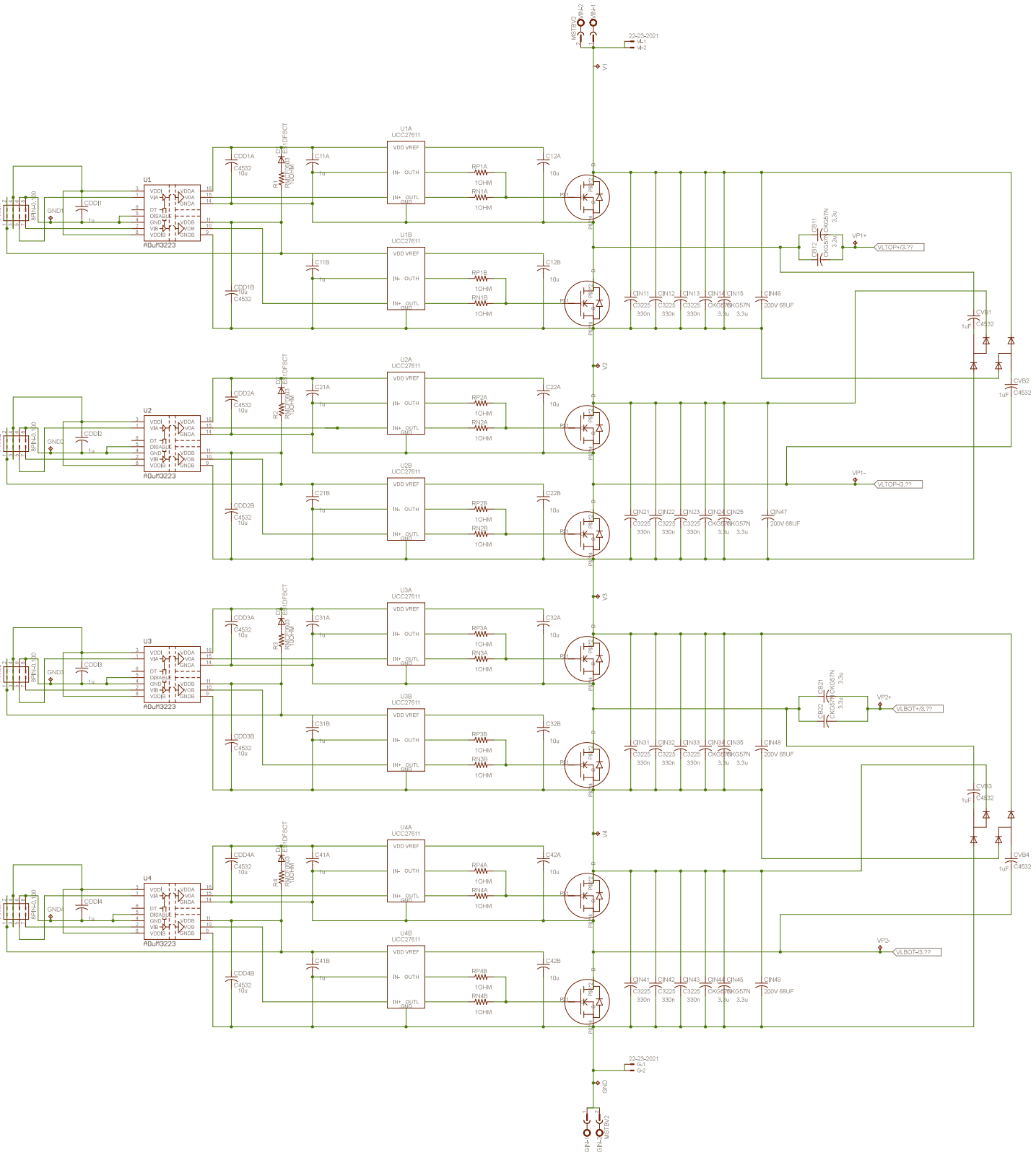
Prototype Schematics, Layout, and Gerber Files

This appendix provides schematics, layouts, and Gerber files for the two prototype printed circuit boards (PCBs) fabricated, namely the Double-Stacked Active Bridge (DSAB) topology. Two layouts were done: one using GaN inverter devices and one using Si inverter devices. While a Single-Stacked Dual-Active-Bridge (DAB) topology was also populated, it used the same PCB as the Si DSAB prototype.

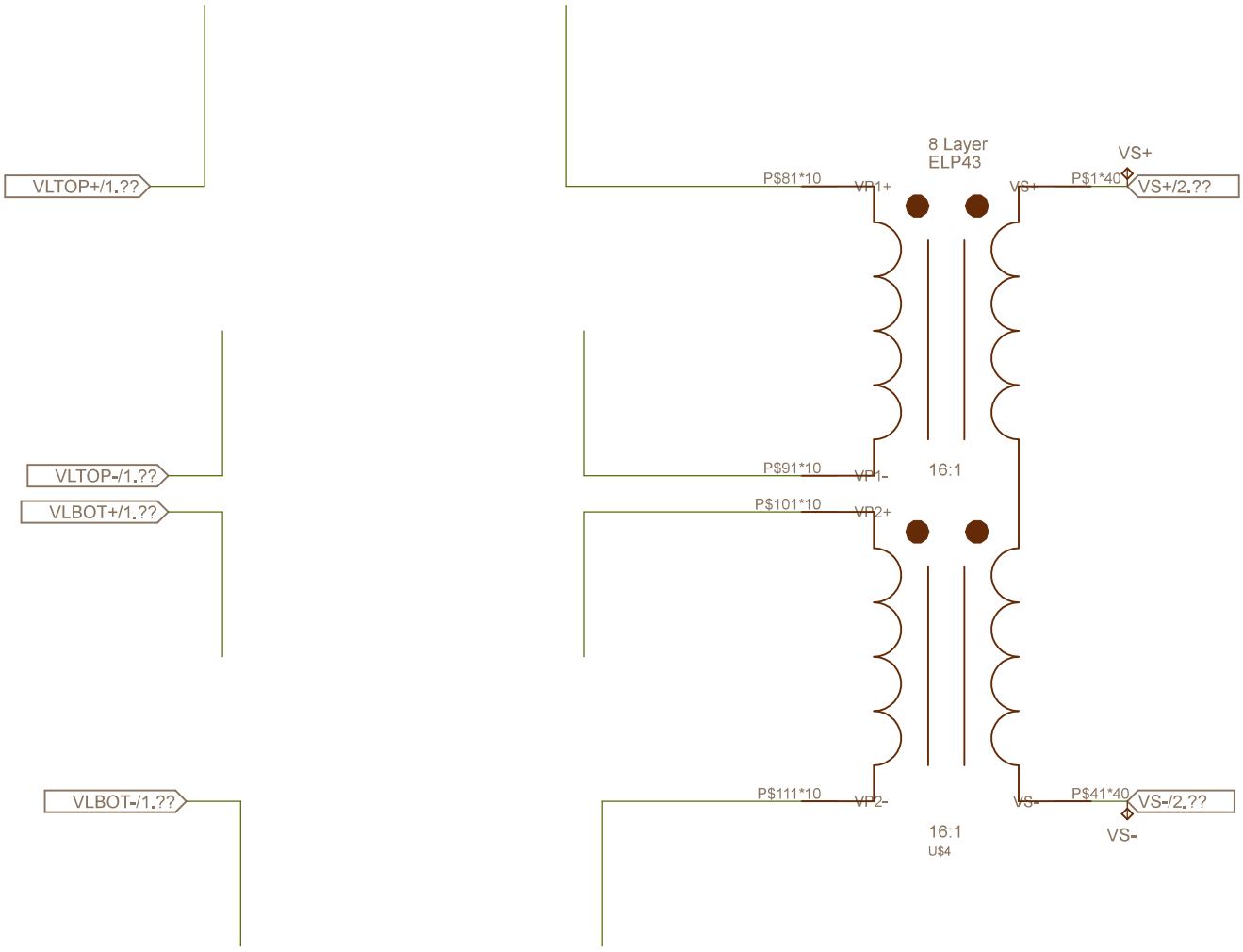
C.1 Schematics

Only one set of schematics is included here, as the only difference between the GaN and Si DSAB prototypes was the inverter device footprint, which is reflected in the layout files rather than the schematic. The schematics show the inverter gate drive and switch circuitry, the transformer structure, the rectifier gate drive and switch circuitry, and the low-power switch circuitry.

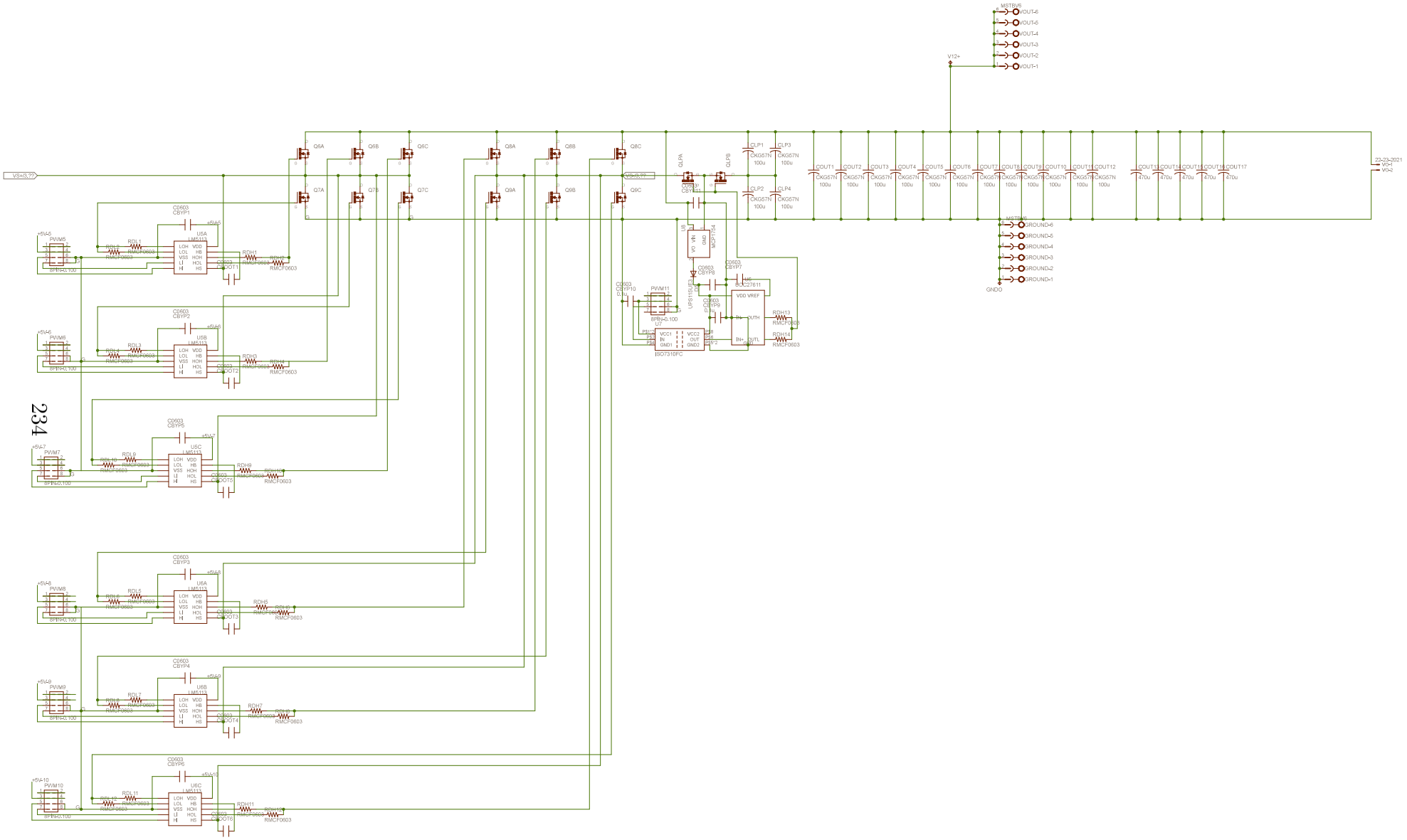
Inverter Gate Drive and Switches



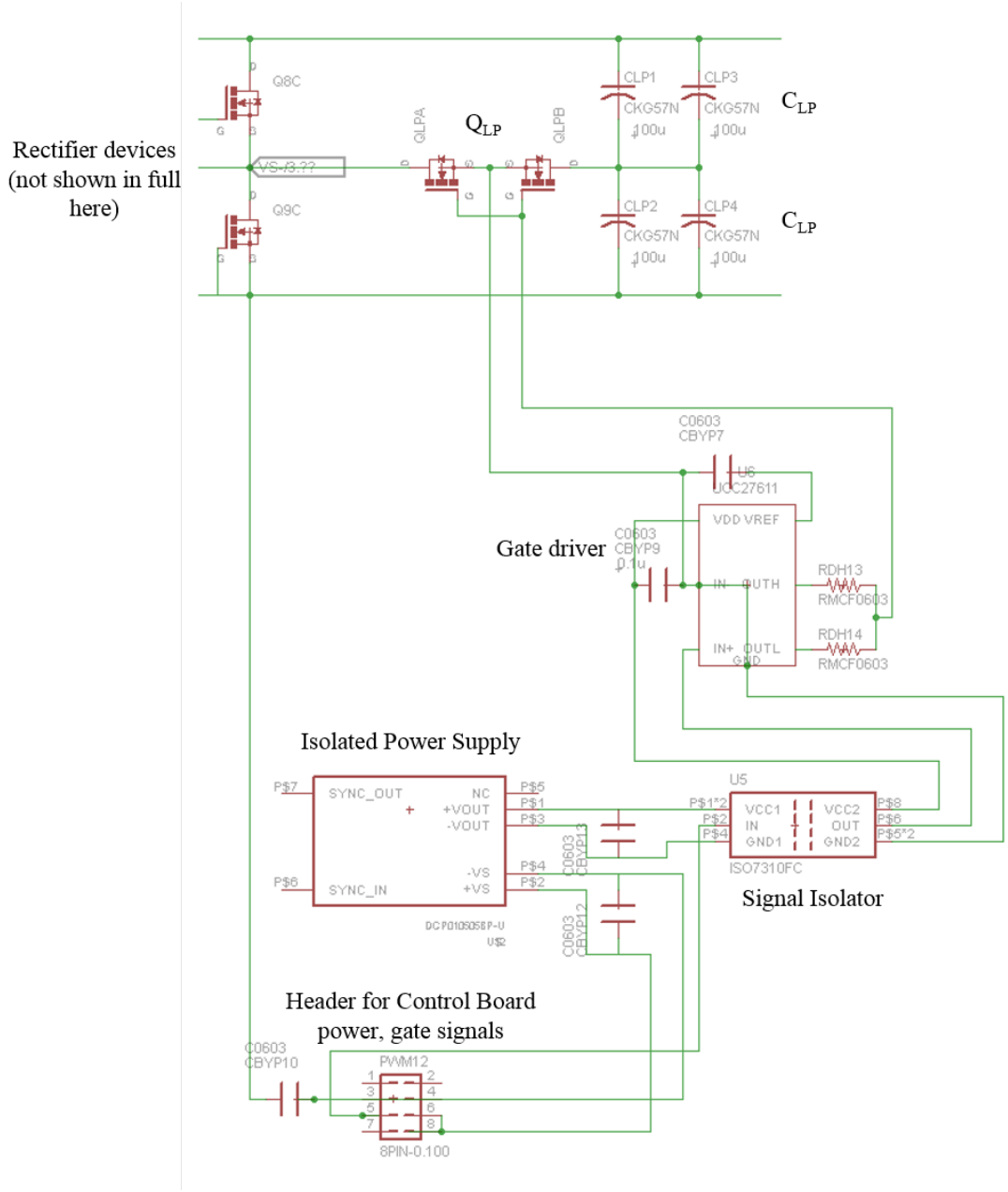
Transformer Structure



Rectifier Gate Drive and Switches



C.1.1 Low-Power Switch Gate Drive Circuitry



The low-power switch was implemented with two source-connected EPC2023 GaN FETs. Each device was controlled by a separate driver (UCC27611), though both drivers received the same gate signal. The drive circuitry was powered from the 5 V bus from the Control Board, which was first passed through an Isolated Power Supply (DCP010505BP-U). The gate signal was also isolated from the Control Board ground through a Signal Isolator (ISO7310FC). As suggested by the DCP010505BP-

U datasheet, a 2.2 μF, low ESR ceramic input capacitor (CBYP12 in the figure) and a 1.0 μF, low ESR ceramic output capacitor (CBYP13 in the figure) were used. The gate drive signal was referenced to the source of the two low-power switches.

C.2 PCB Layout

C.2.1 PCB Stackup

Layer	Copper Oz.	Copper Height
1 (top)	2	70 μm (2.76 mil)
2	4	140 μm (5.51 mil)
3	4	140 μm (5.51 mil)
4	4	140 μm (5.51 mil)
5	4	140 μm (5.51 mil)
6	4	140 μm (5.51 mil)
7	4	140 μm (5.51 mil)
8 (bottom)	2	70 μm (2.76 mil)

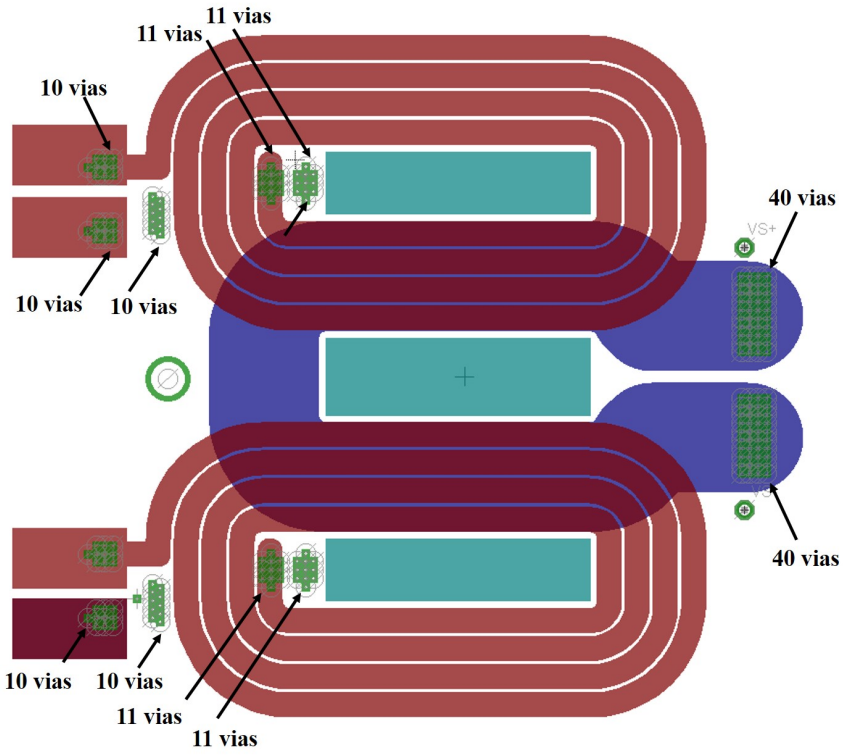
Table C.1: PCB Layer Dimensions

Table C.1 gives the heights of each layer in the PCB stack-up. The total height of the PCB was $\sim$2286 μm or 90 mils. The exact heights of each dielectric layer are not explicitly known, though they can be defined when fabricating the board if necessary for the design.

For a more detailed description of the winding trace widths, see [27].

C.2.2 Transformer Via Layout

Vias were used to connect the primary winding layers in series to implement the primary windings, and to connect the secondary layers in parallel to implement the secondary winding. 10-11 vias were used at each connection point on the primary side, while 40 vias were used at each connection point on the secondary side (due to the high currents present on the secondary side). See [27] for a more detailed description of the transformer layout.



C.2.3 PCB Layouts

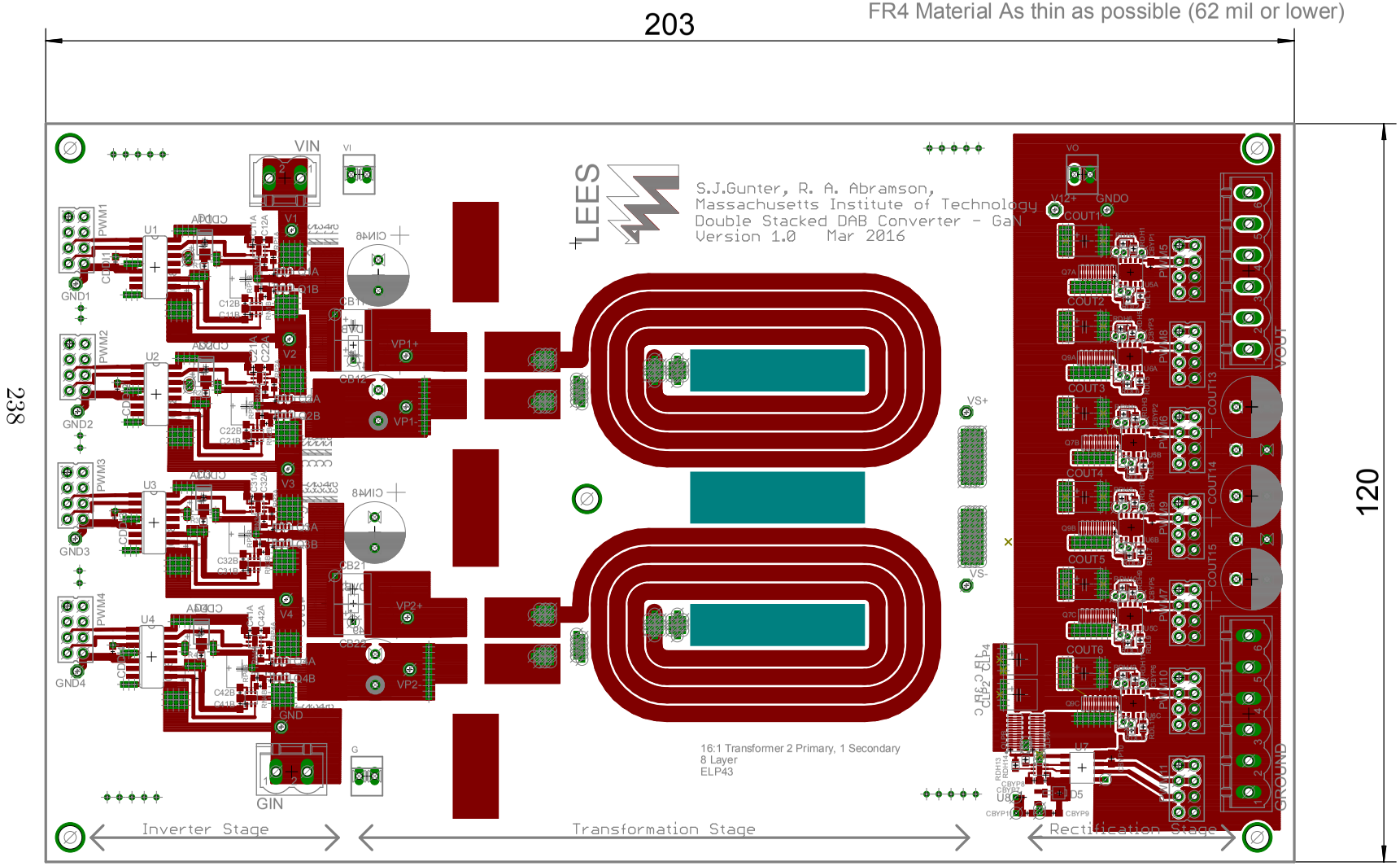
PCB layouts for each board layer are presented here, for both the GaN and Si DSAB prototype boards.

C.2.4 GaN DSAB

The layers are presented from Layer 1 (top layer) to Layer 8 (bottom layer).

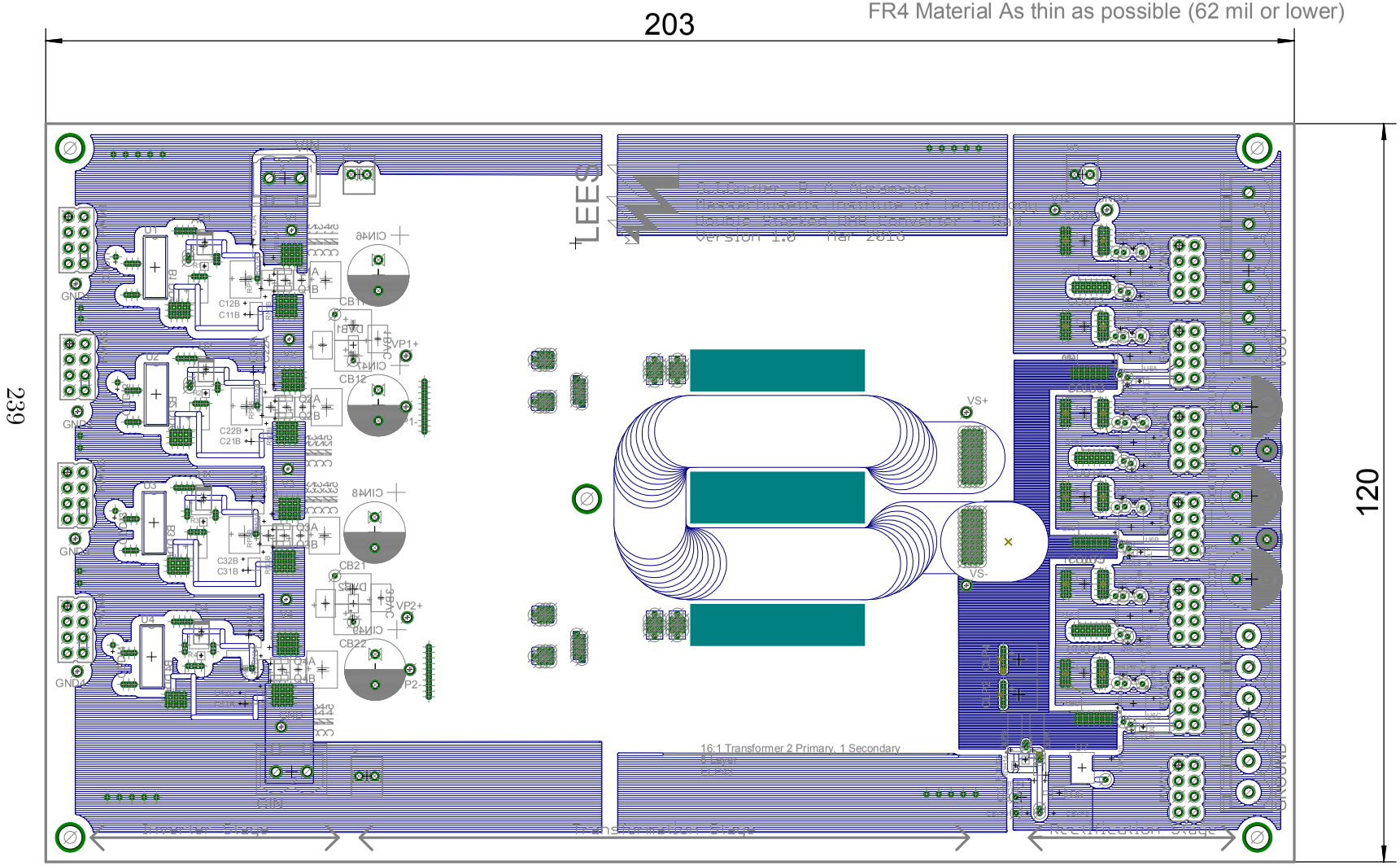
8 layers 2 oz copper for outer layers 4 oz copper for inner layers

FR4 Material As thin as possible (62 mil or lower)



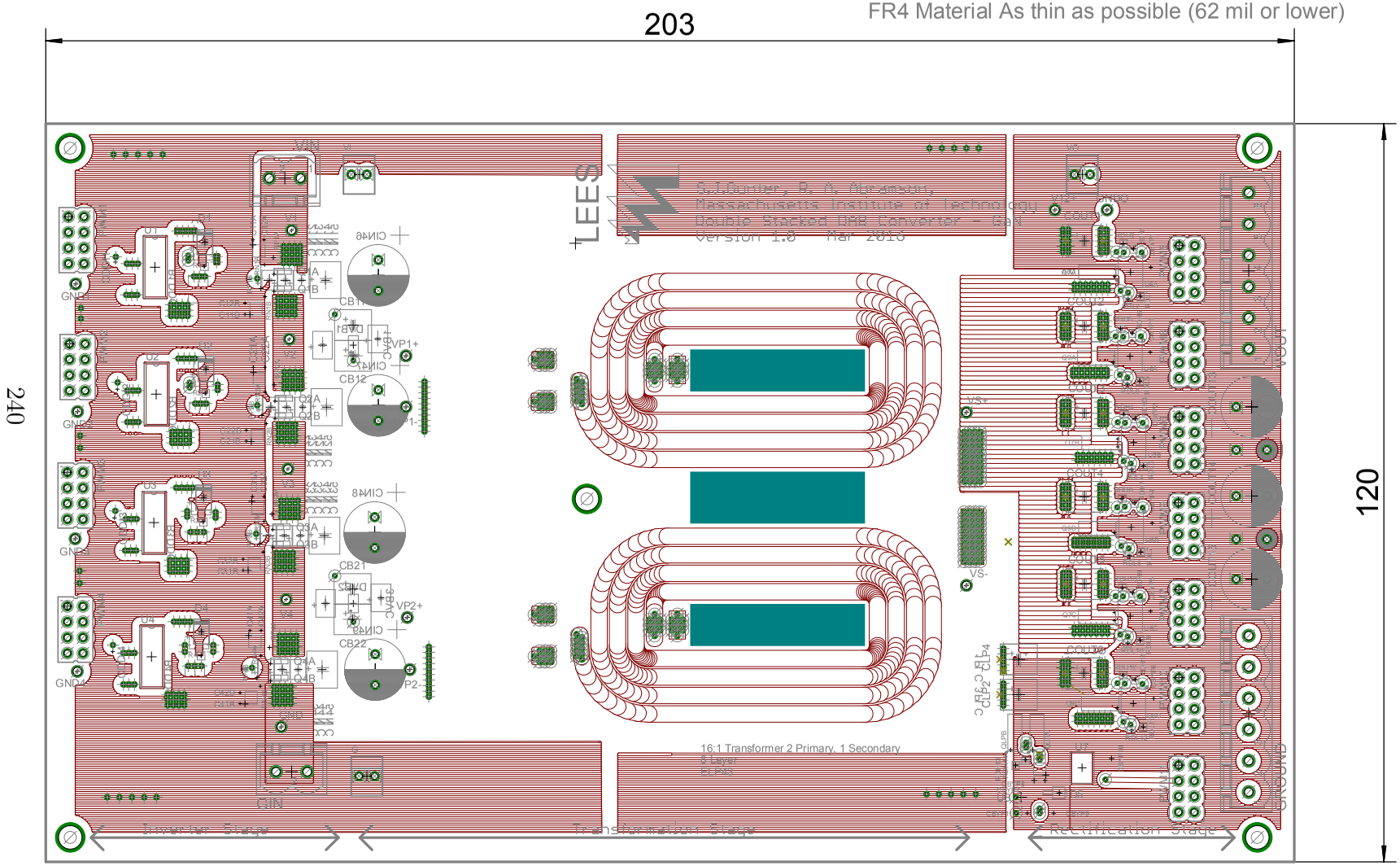
8 layers 2 oz copper for outer layers 4 oz copper for inner layers

FR4 Material As thin as possible (62 mil or lower)



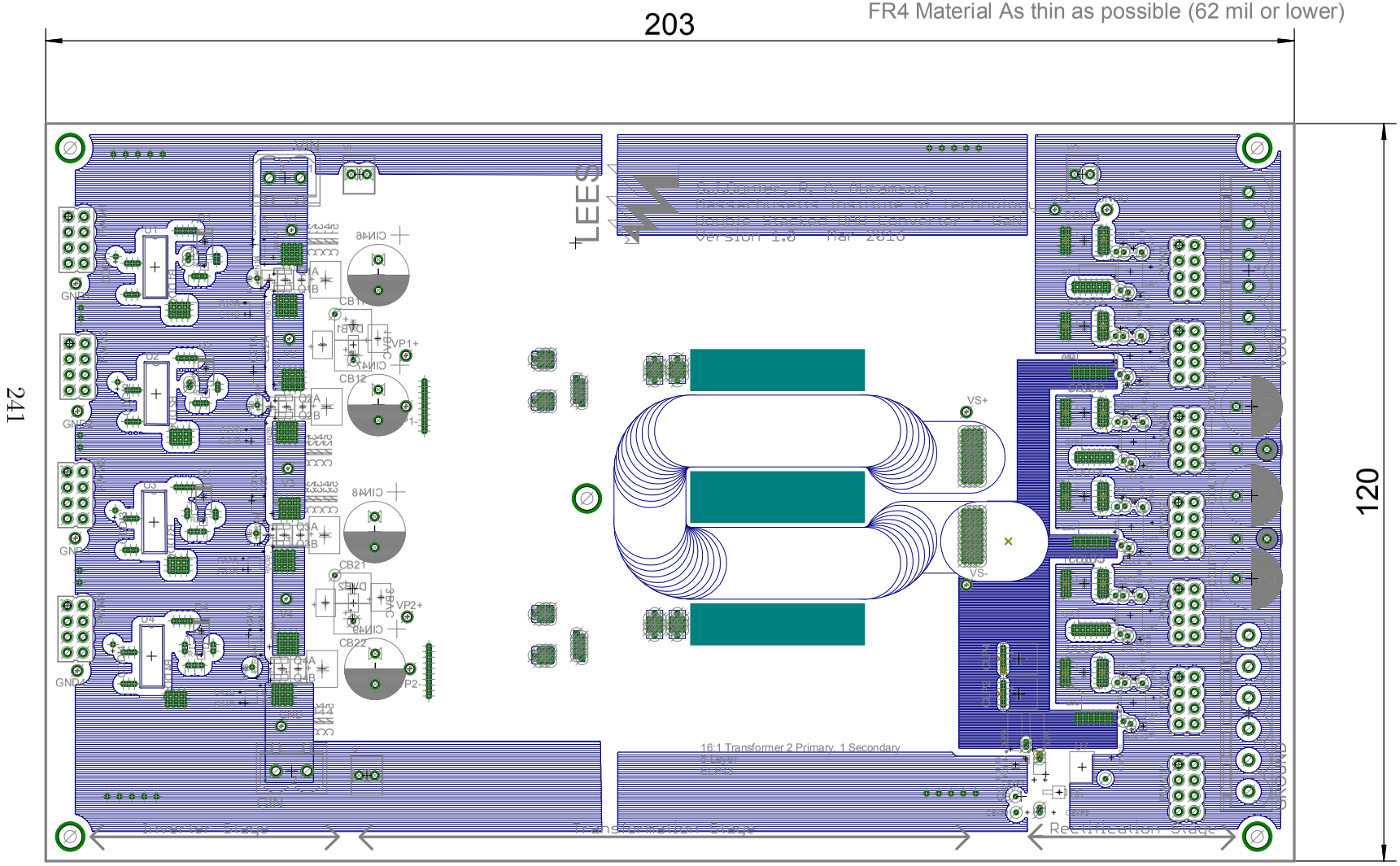
8 layers 2 oz copper for outer layers 4 oz copper for inner layers

FR4 Material As thin as possible (62 mil or lower)



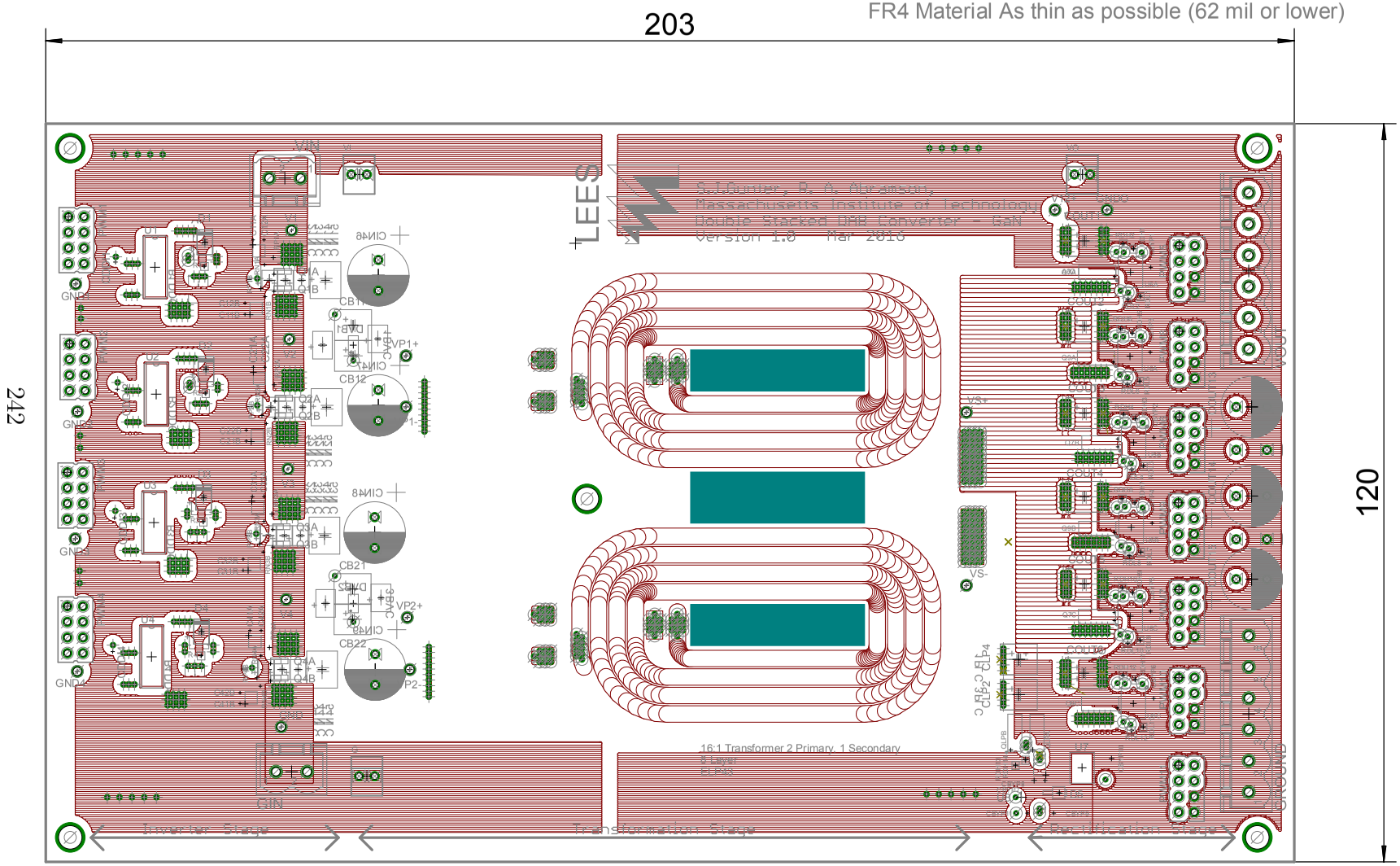
8 layers 2 oz copper for outer layers 4 oz copper for inner layers

FR4 Material As thin as possible (62 mil or lower)



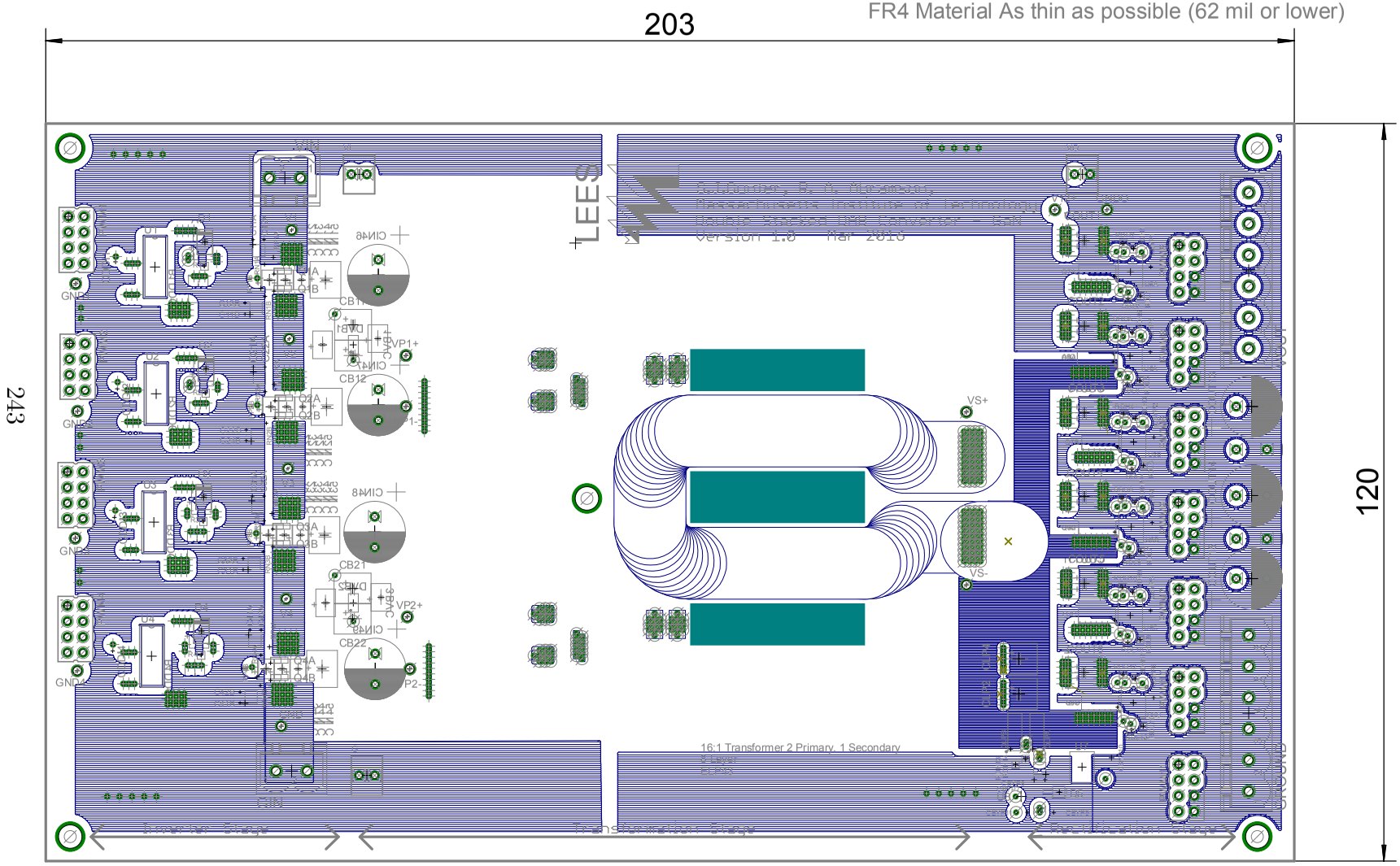
8 layers 2 oz copper for outer layers 4 oz copper for inner layers

FR4 Material As thin as possible (62 mil or lower)



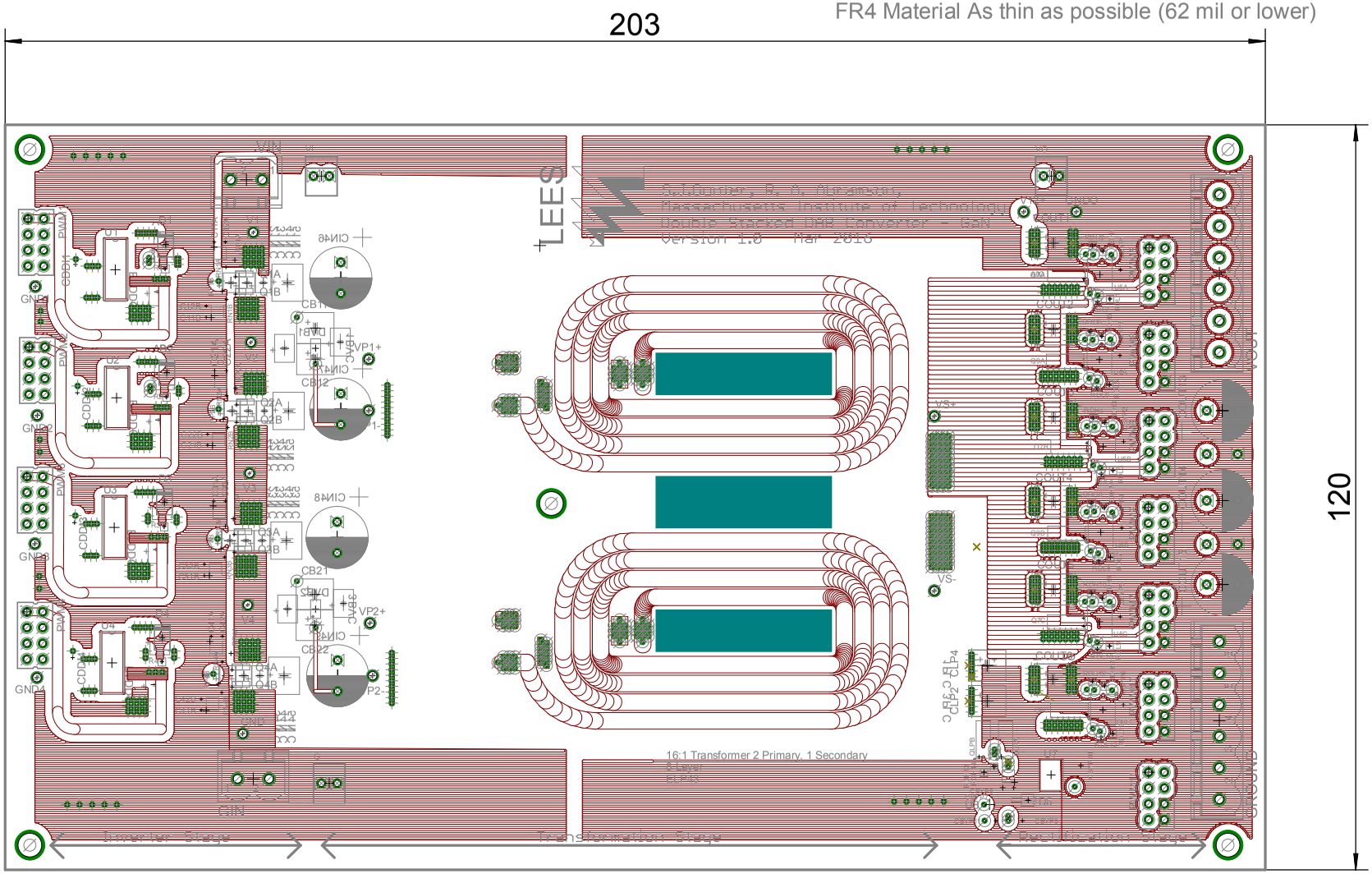
8 layers 2 oz copper for outer layers 4 oz copper for inner layers

FR4 Material As thin as possible (62 mil or lower)



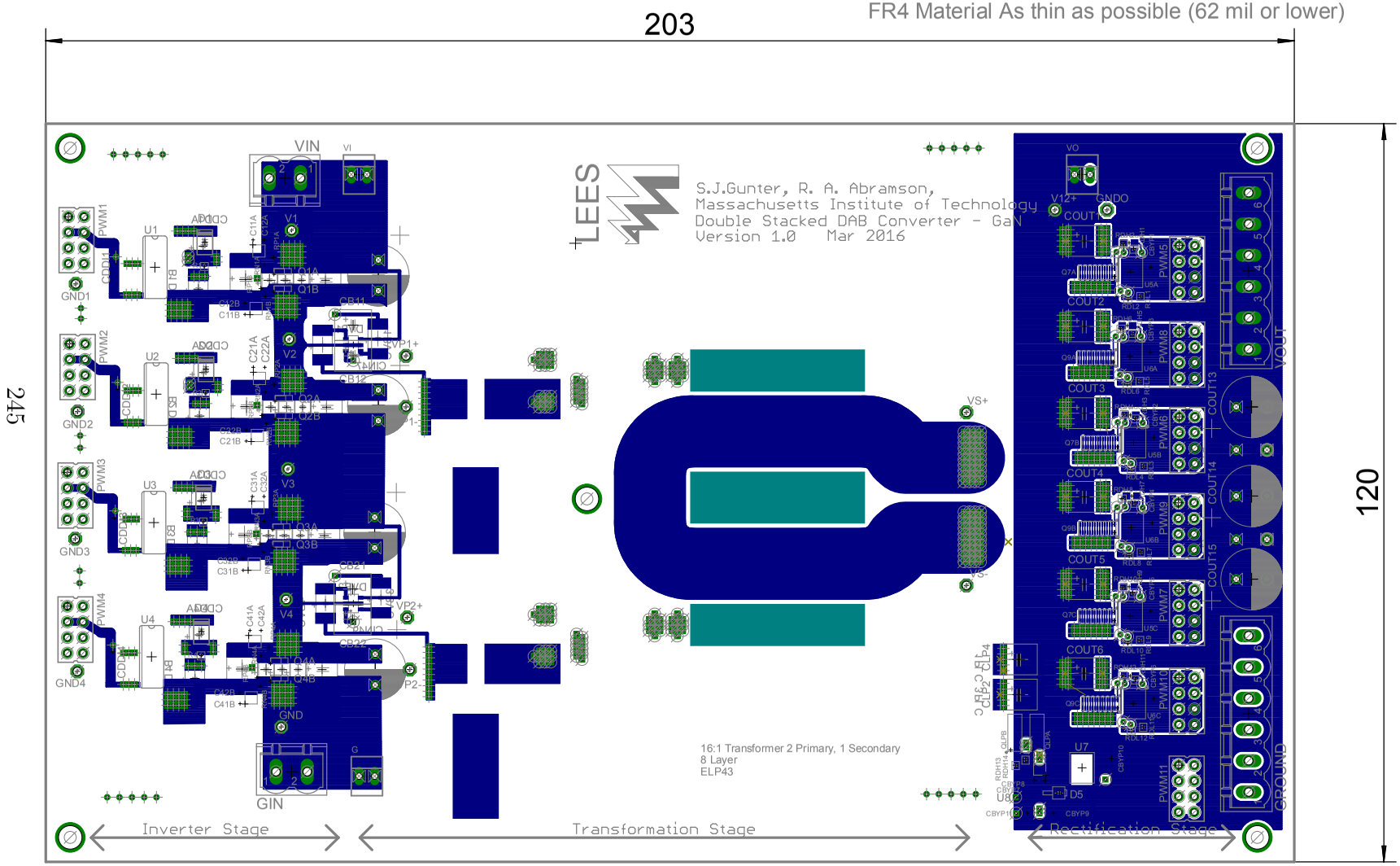
8 layers 2 oz copper for outer layers 4 oz copper for inner layers

FR4 Material As thin as possible (62 mil or lower)



8 layers 2 oz copper for outer layers 4 oz copper for inner layers

FR4 Material As thin as possible (62 mil or lower)

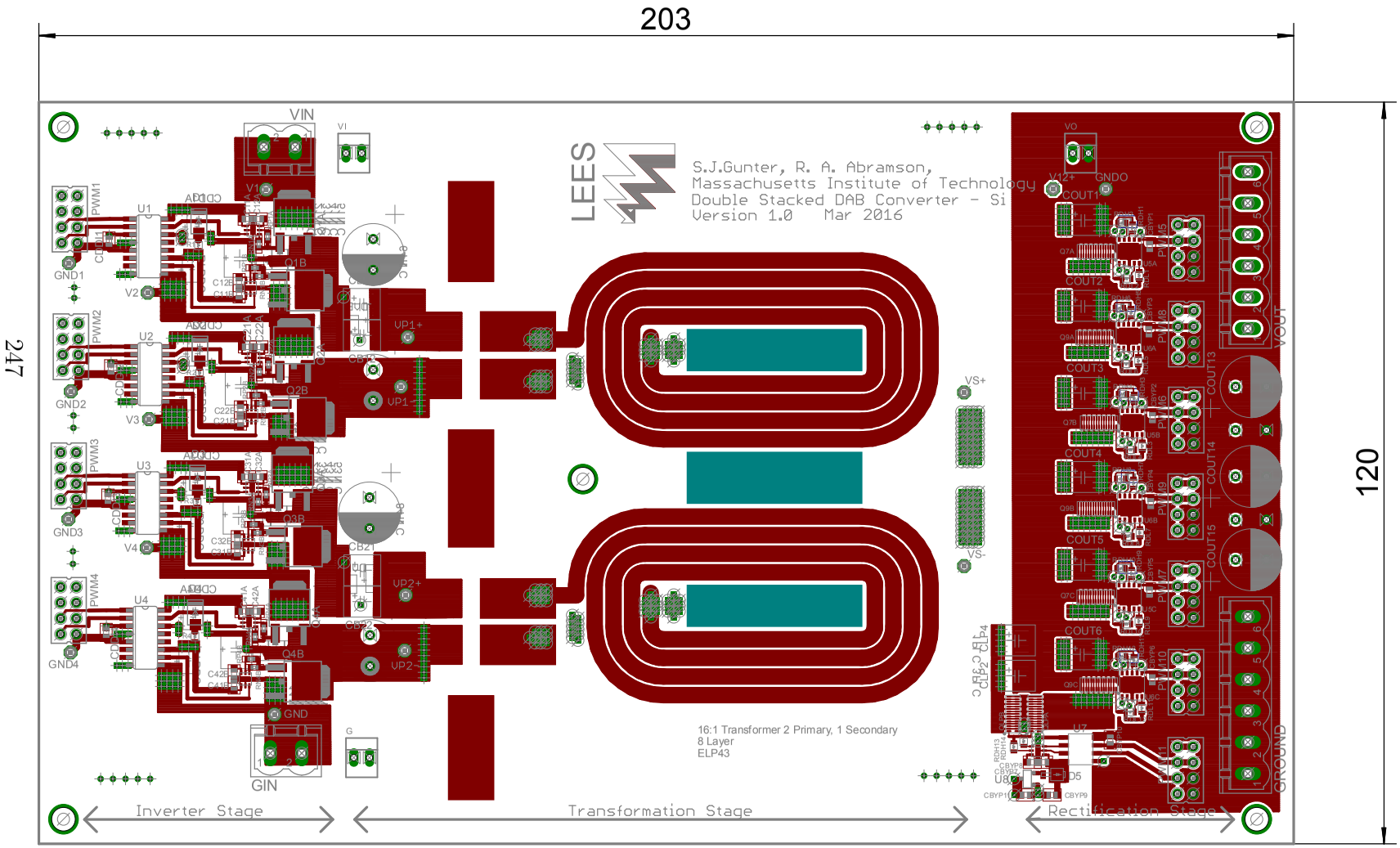


C.2.5 Si DSAB

The layers are presented from Layer 1 (top layer) to Layer 8 (bottom layer).

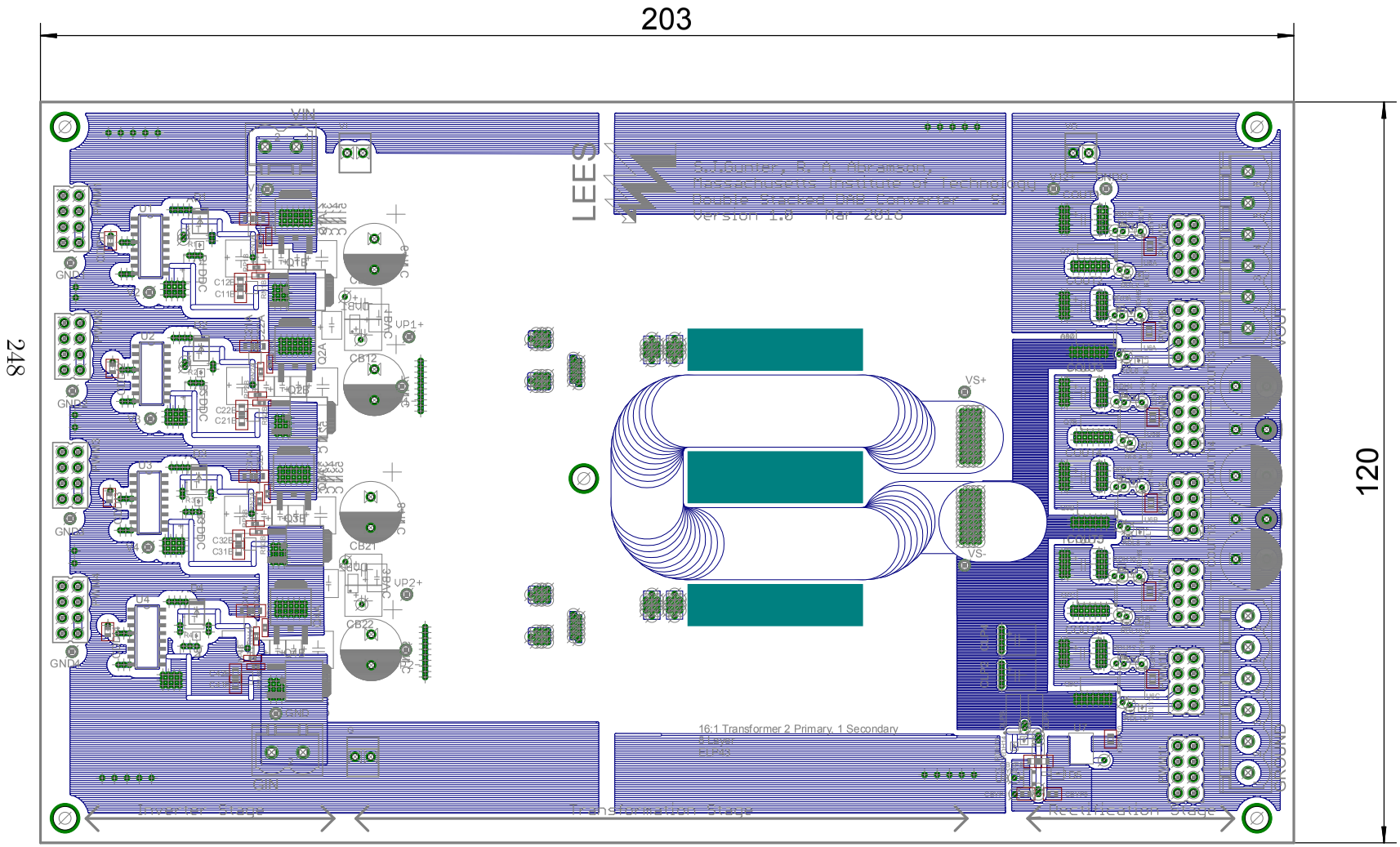
8 layers 2 oz copper for outer layers 4 oz copper for inner layers

FR4 Material As thin as possible (62 mil or lower)



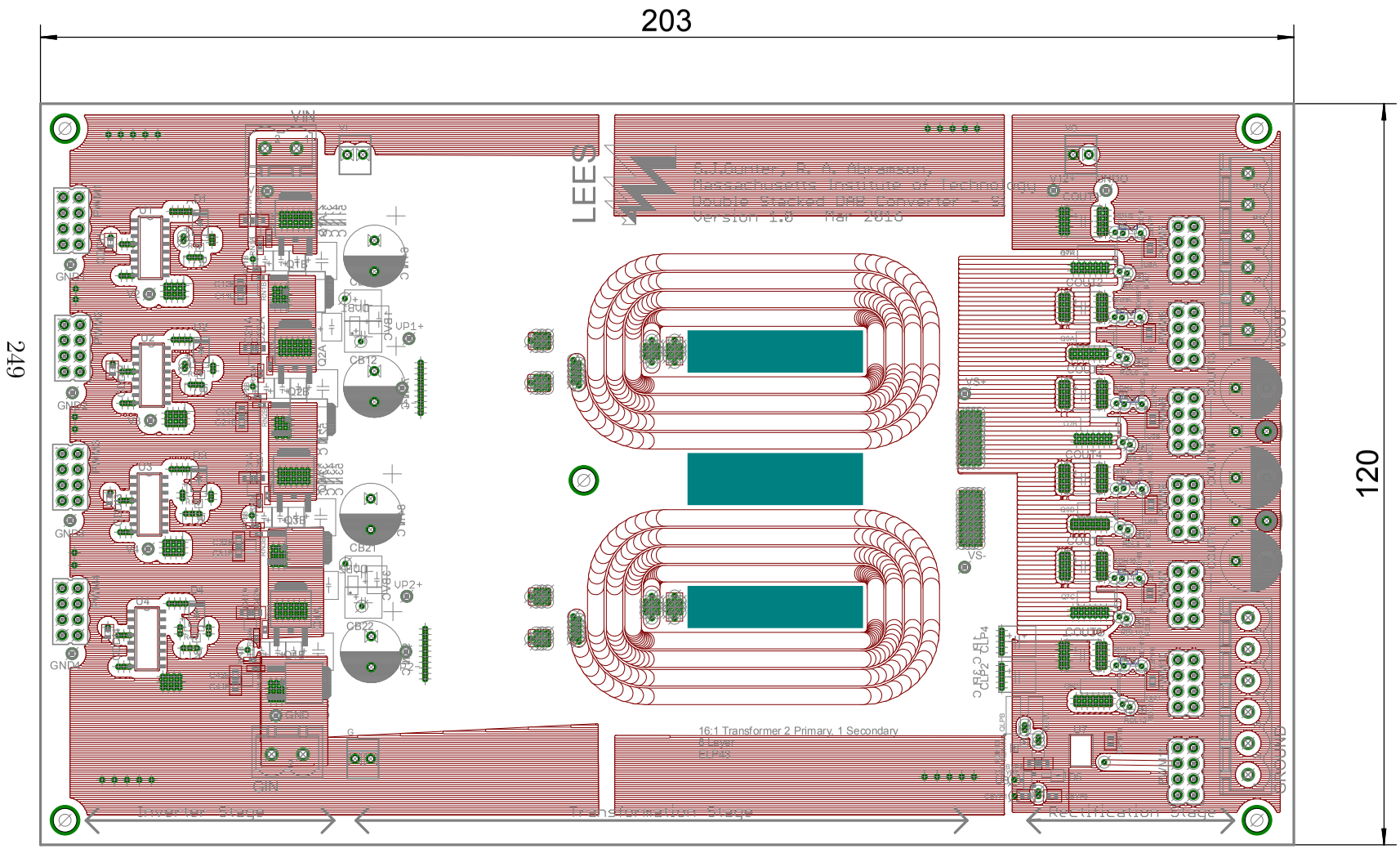
8 layers 2 oz copper for outer layers 4 oz copper for inner layers

FR4 Material As thin as possible (62 mil or lower)



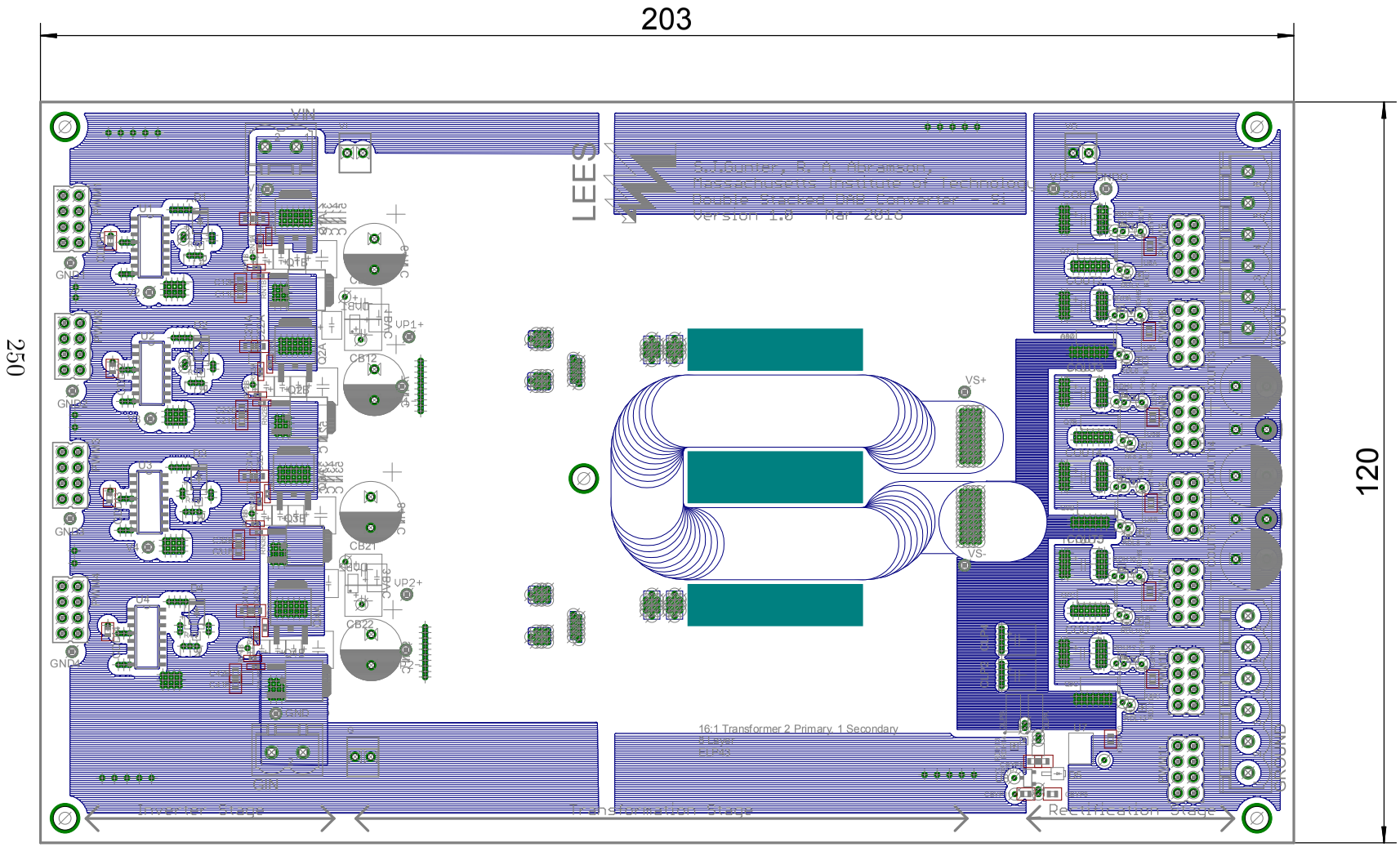
8 layers 2 oz copper for outer layers 4 oz copper for inner layers

FR4 Material As thin as possible (62 mil or lower)



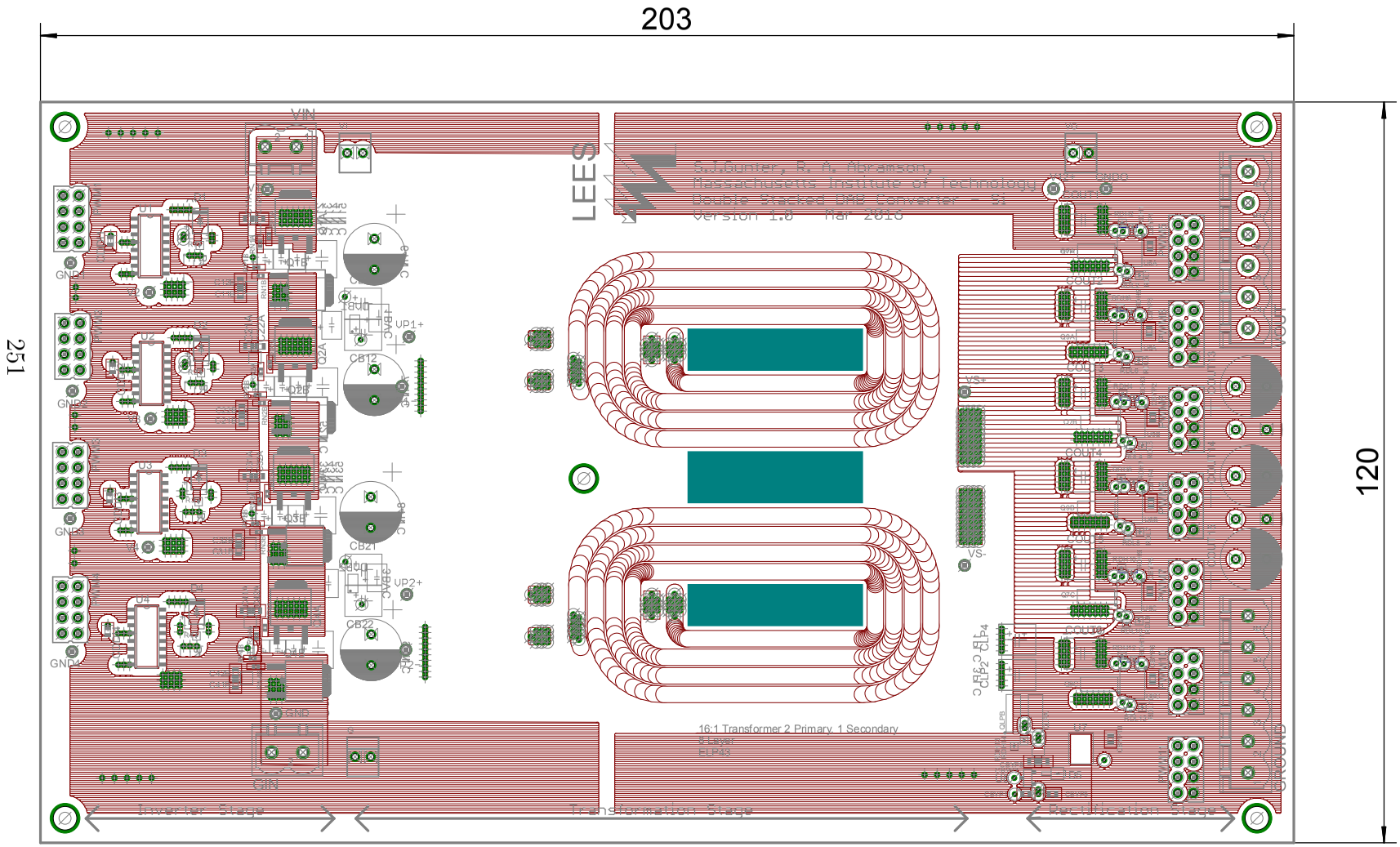
8 layers 2 oz copper for outer layers 4 oz copper for inner layers

FR4 Material As thin as possible (62 mil or lower)



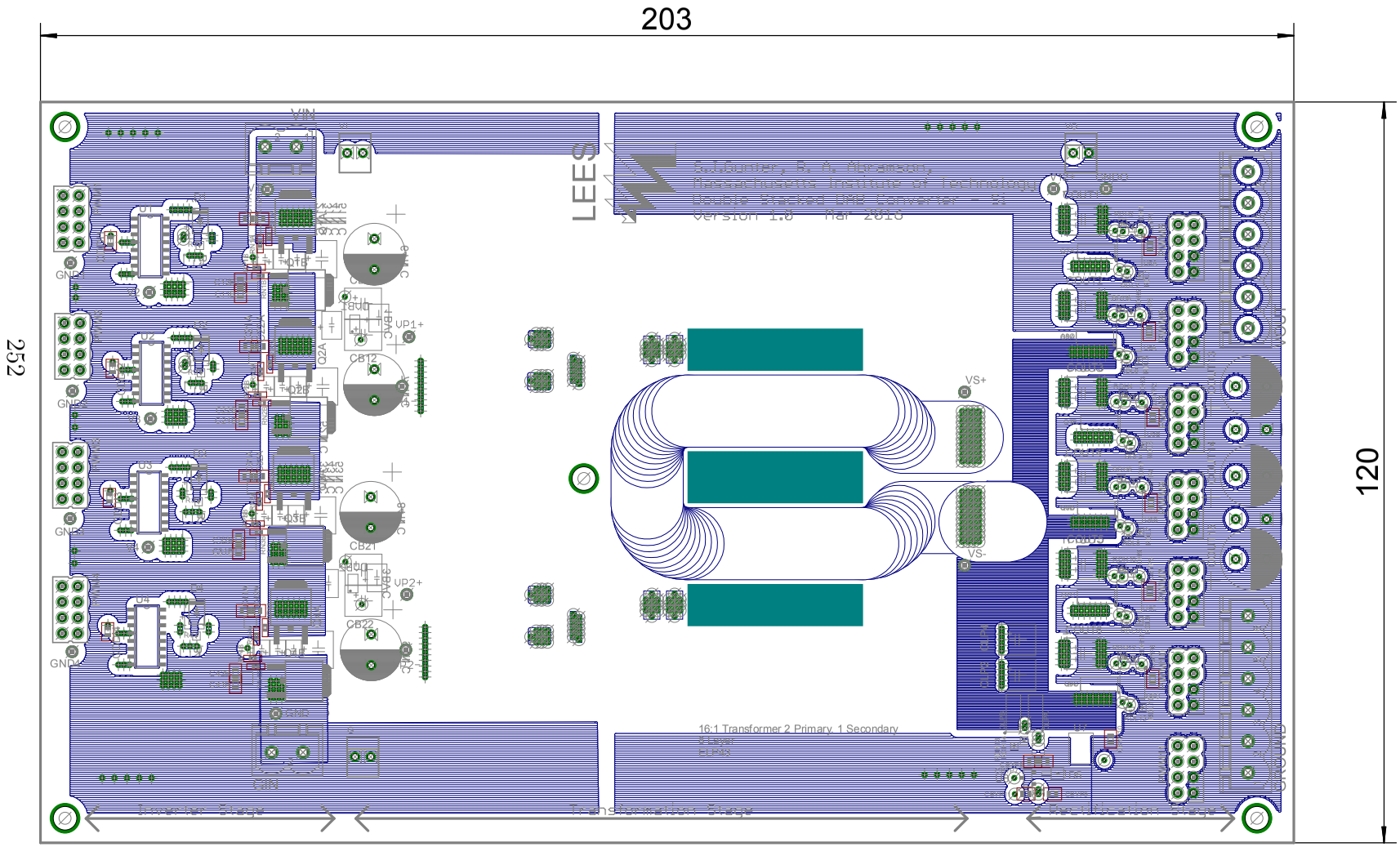
8 layers 2 oz copper for outer layers 4 oz copper for inner layers

FR4 Material As thin as possible (62 mil or lower)



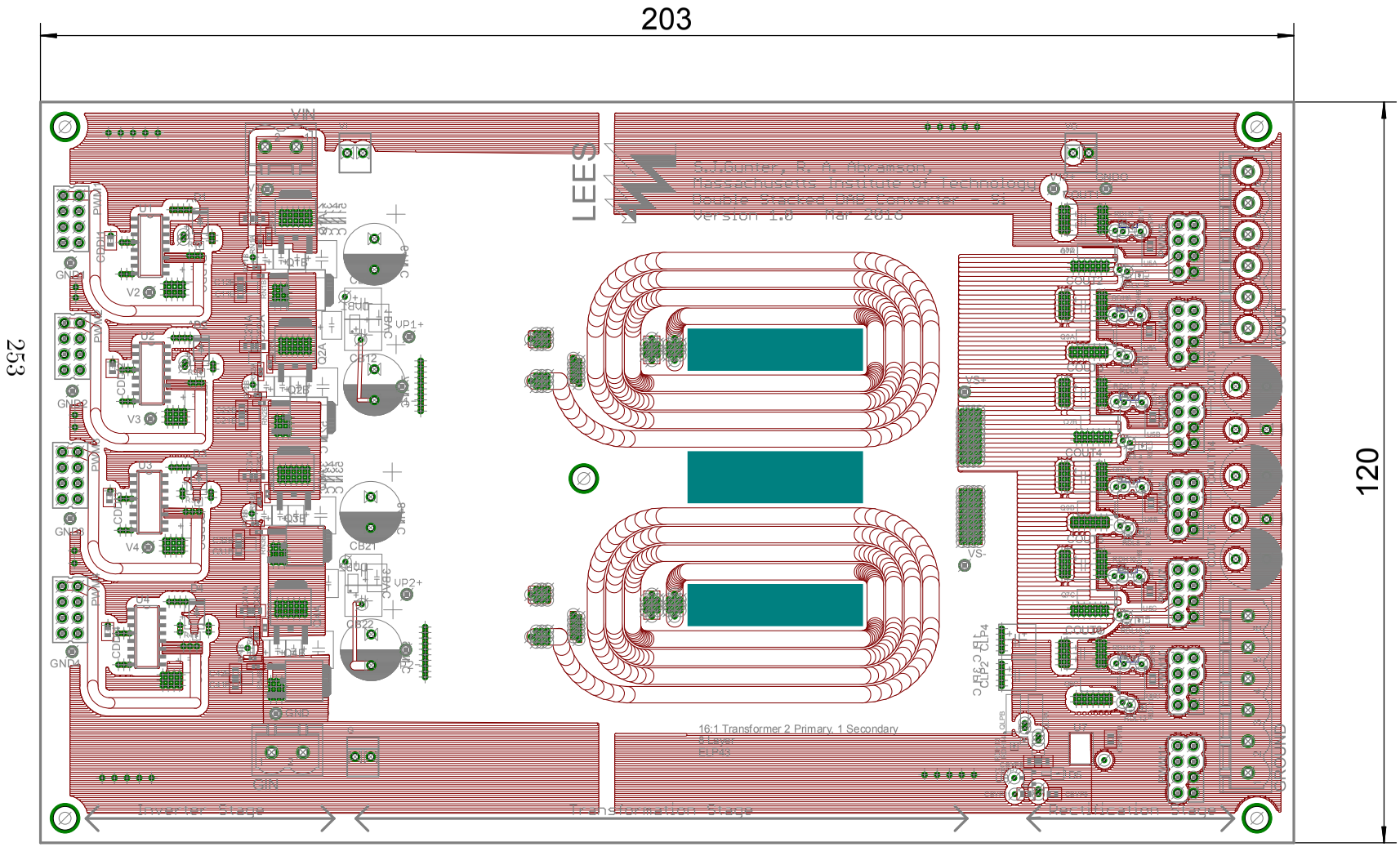
8 layers 2 oz copper for outer layers 4 oz copper for inner layers

FR4 Material As thin as possible (62 mil or lower)



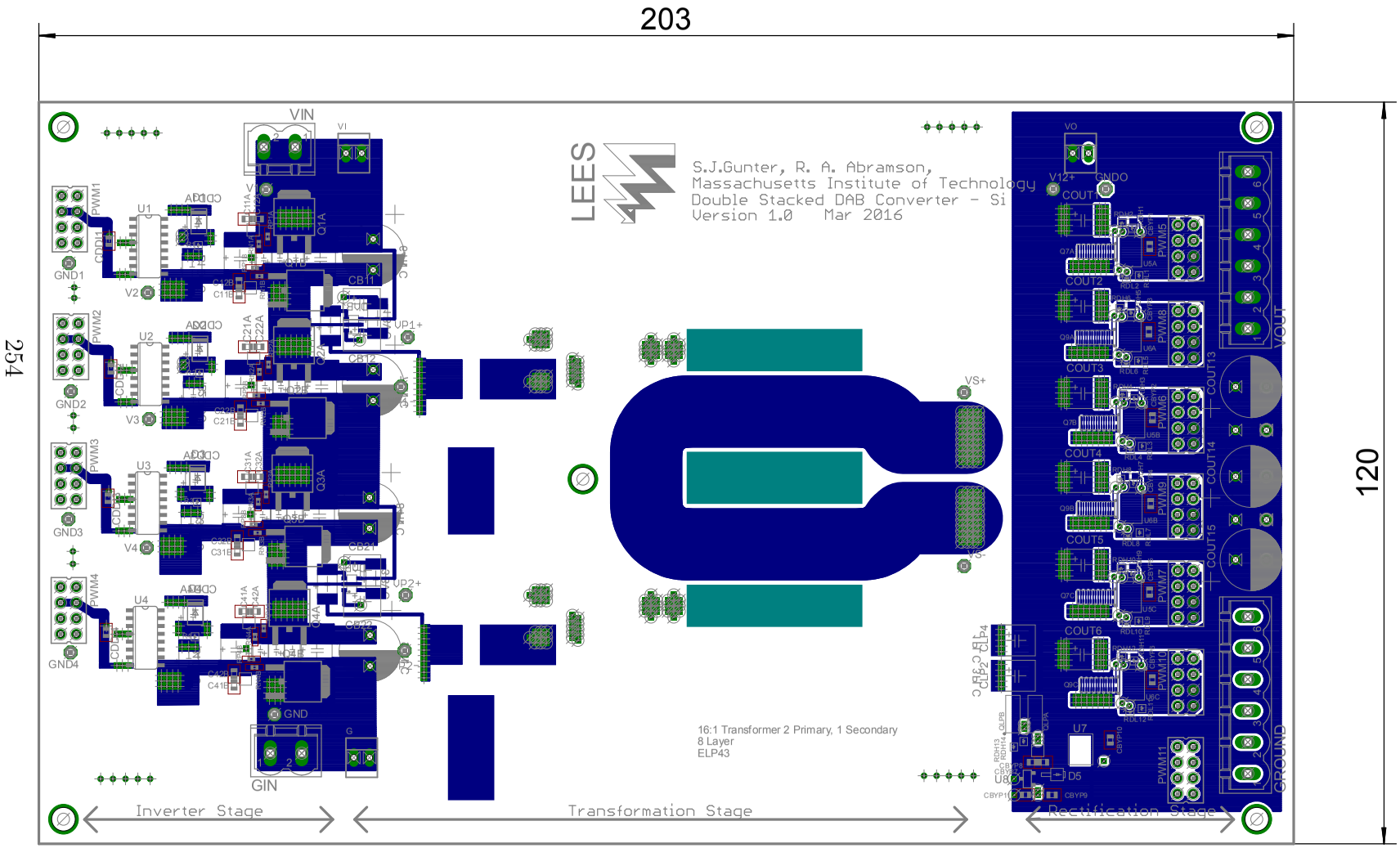
8 layers 2 oz copper for outer layers 4 oz copper for inner layers

FR4 Material As thin as possible (62 mil or lower)



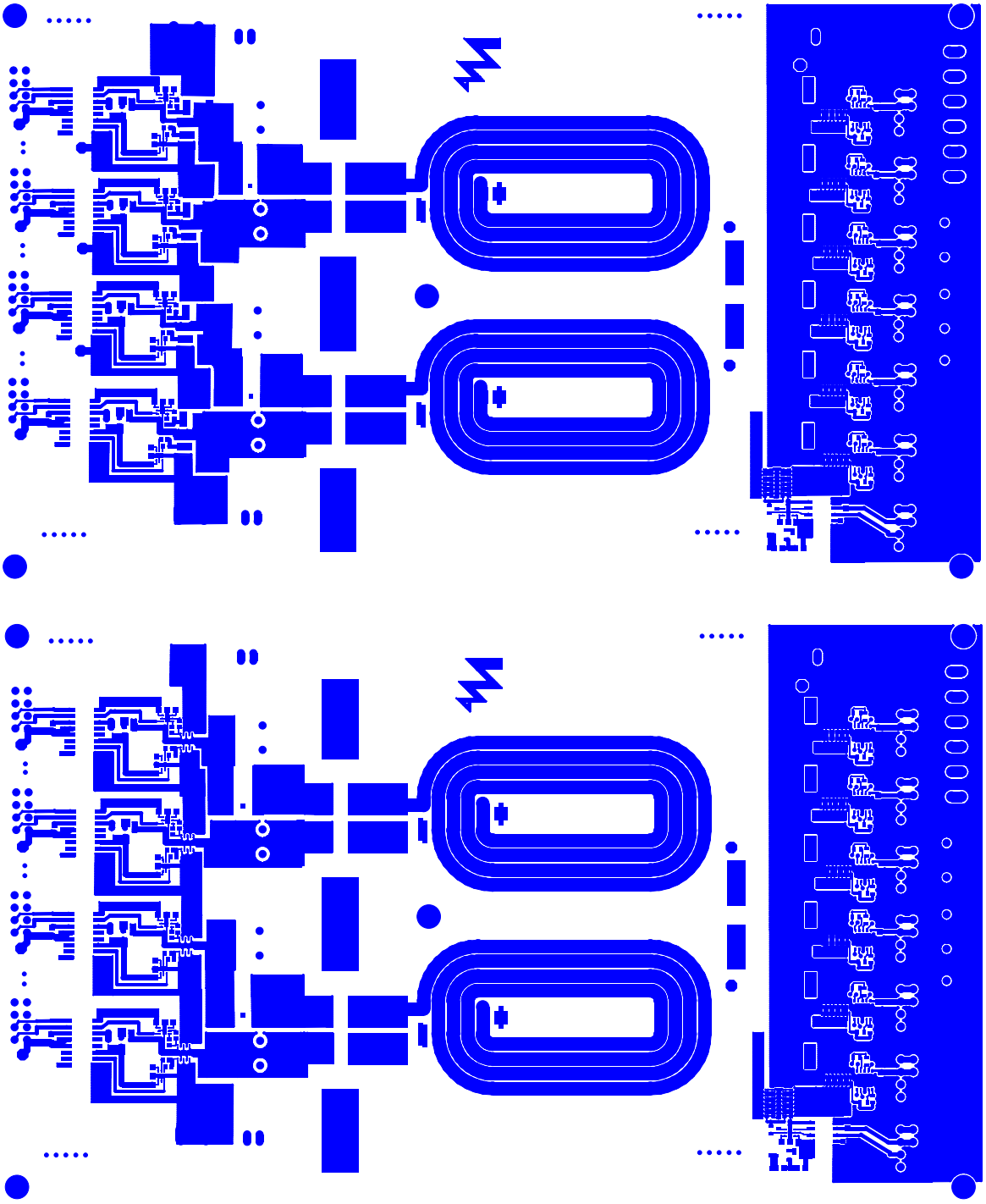
8 layers 2 oz copper for outer layers 4 oz copper for inner layers

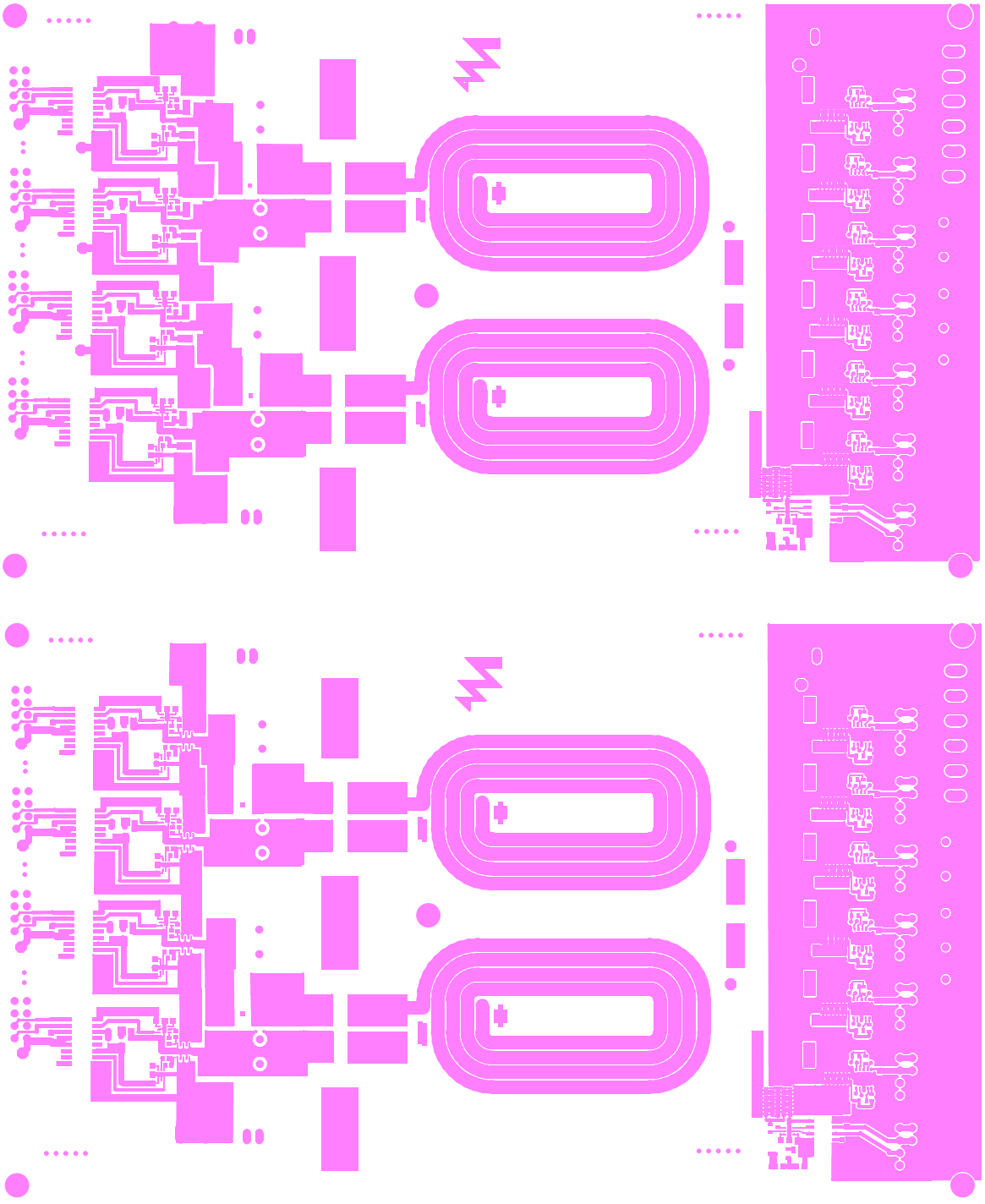
FR4 Material As thin as possible (62 mil or lower)

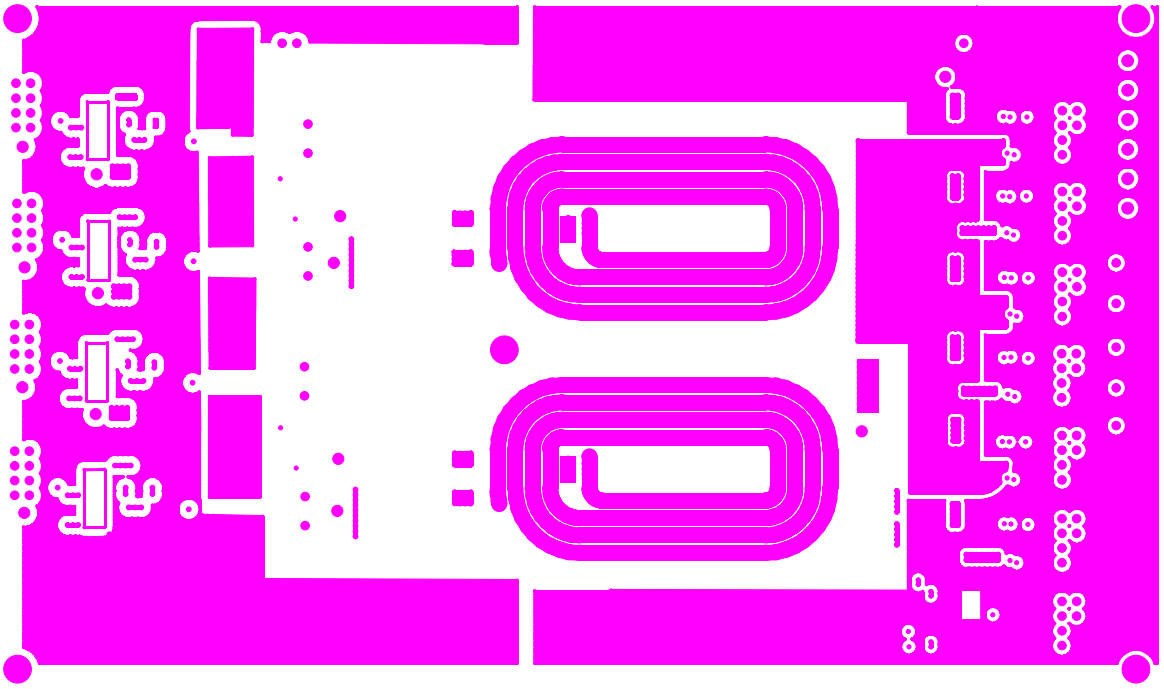


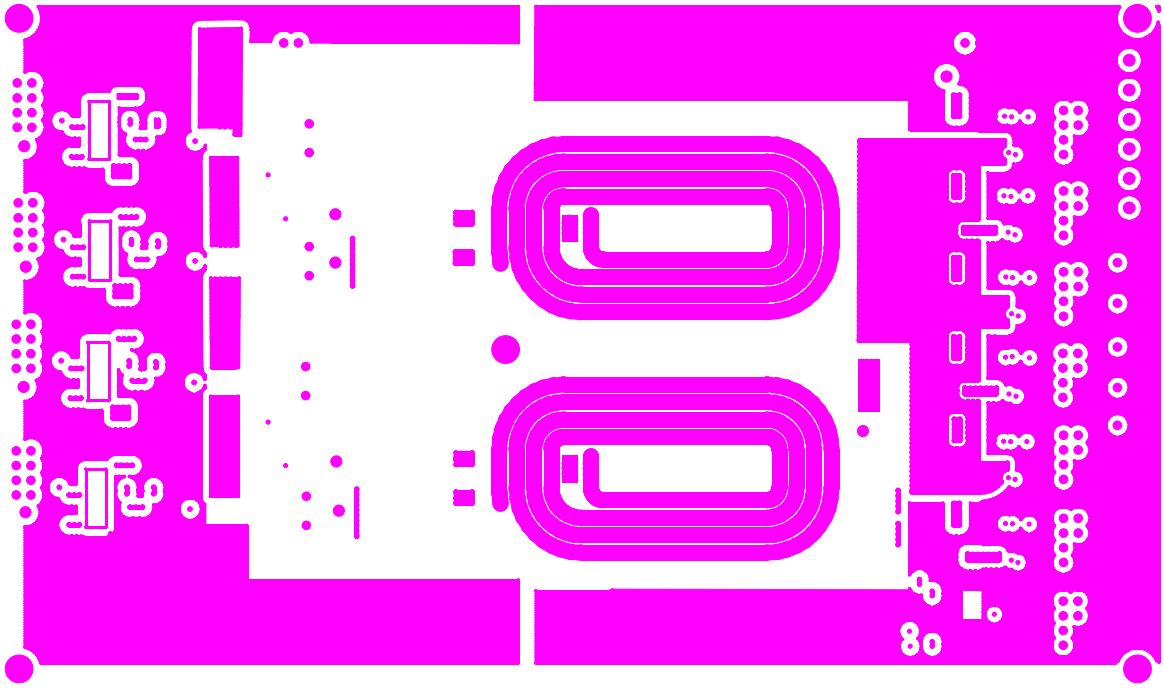
C.3 Gerber Files

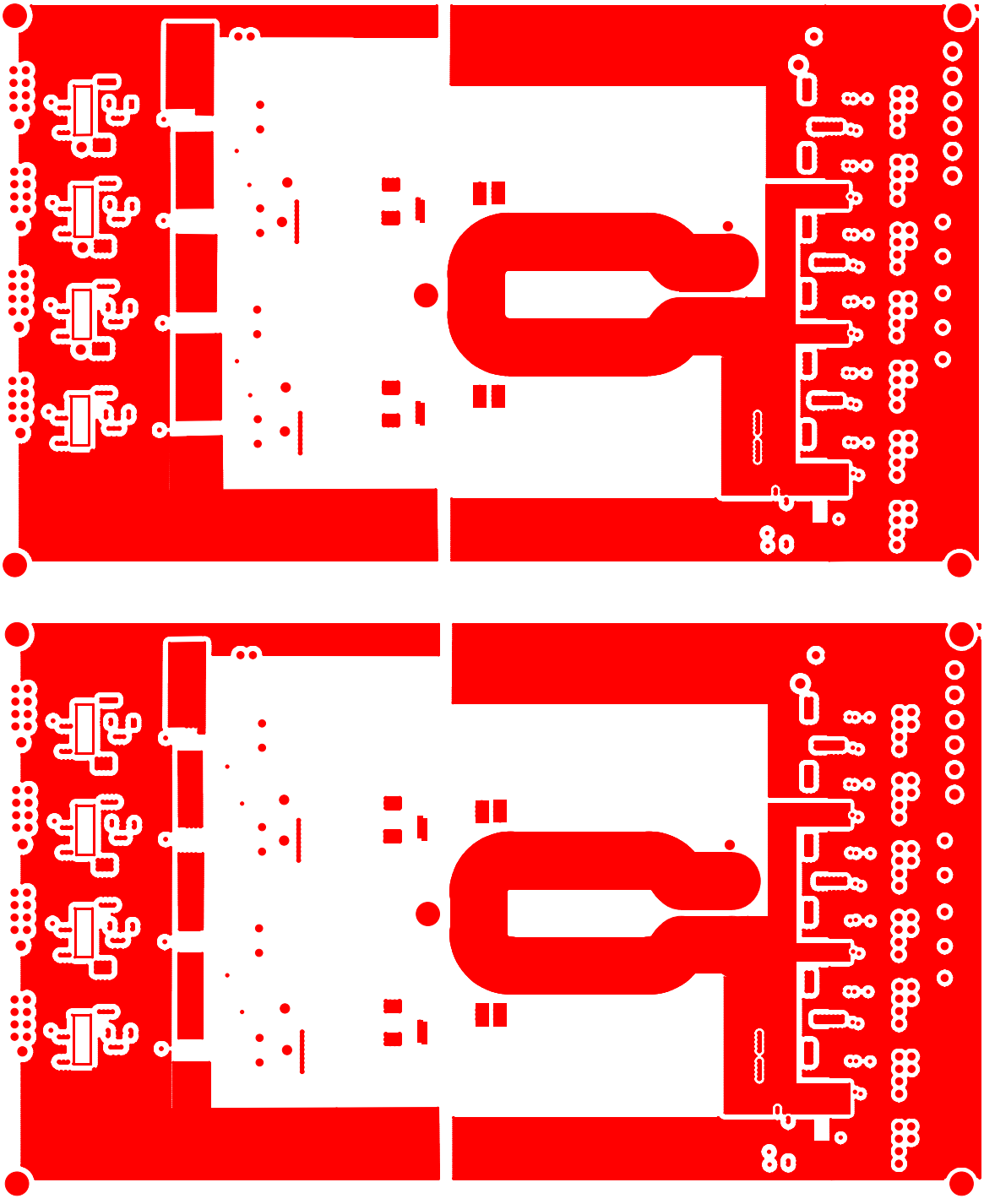
The GaN and Si PCBs were fabricated as an arrayed board to save on production costs. The gerber files for this array are presented here, with the Si DSAB prototype arrayed on top of the GaN DSAB prototype.

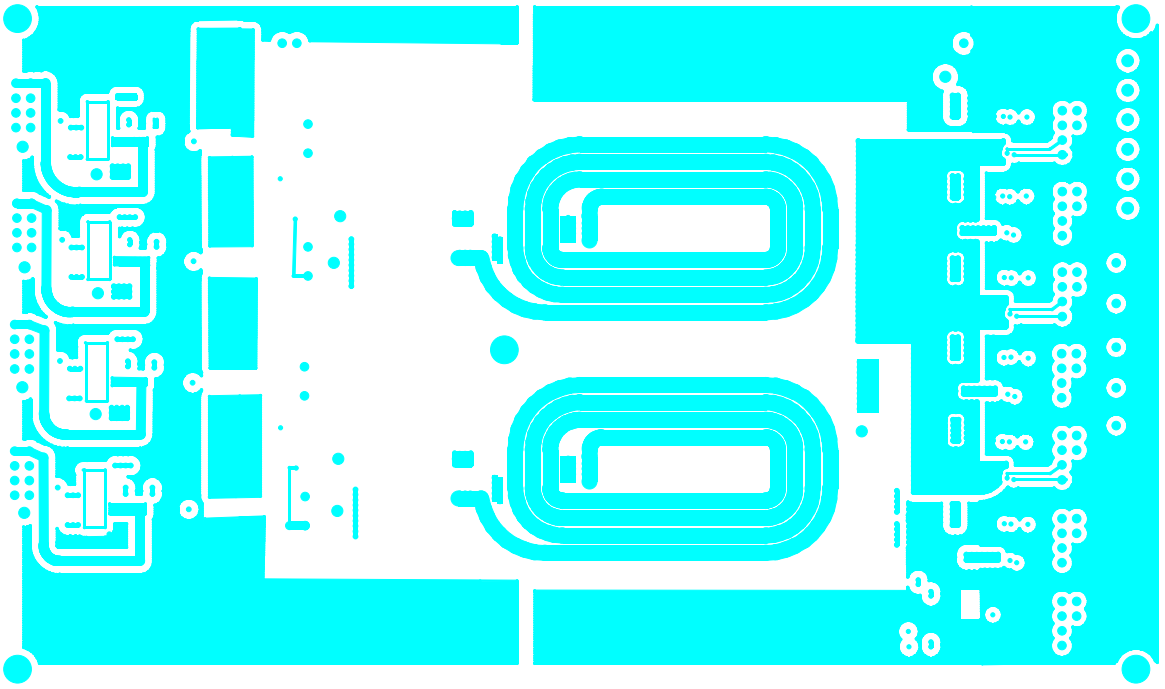


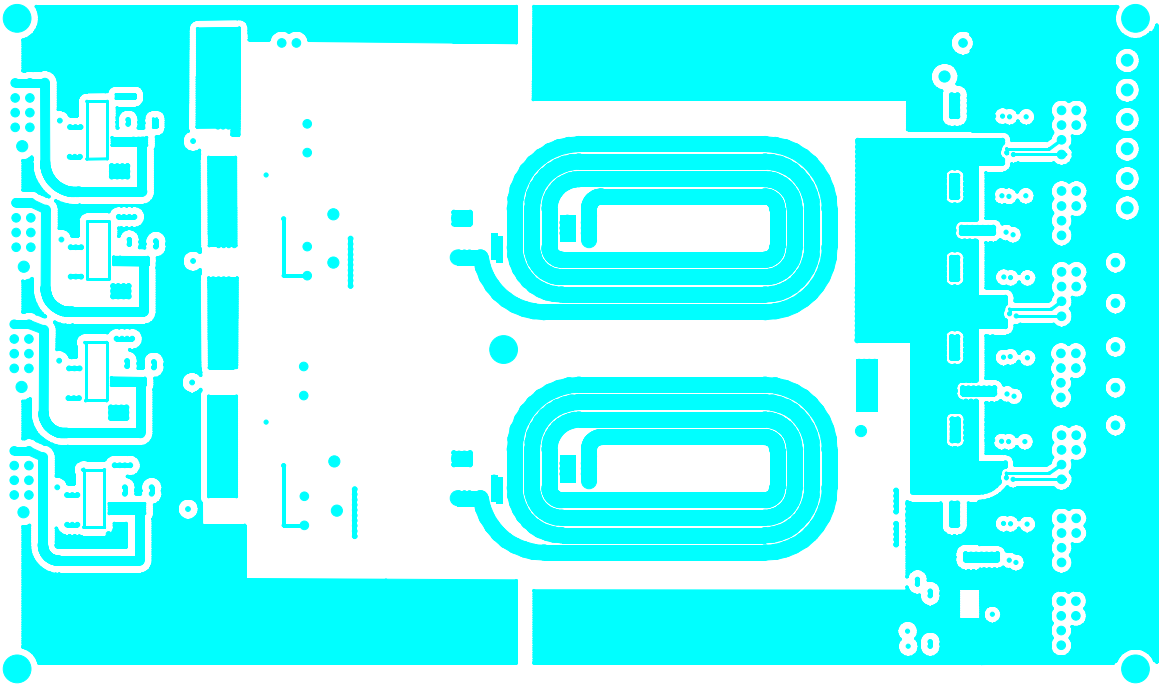


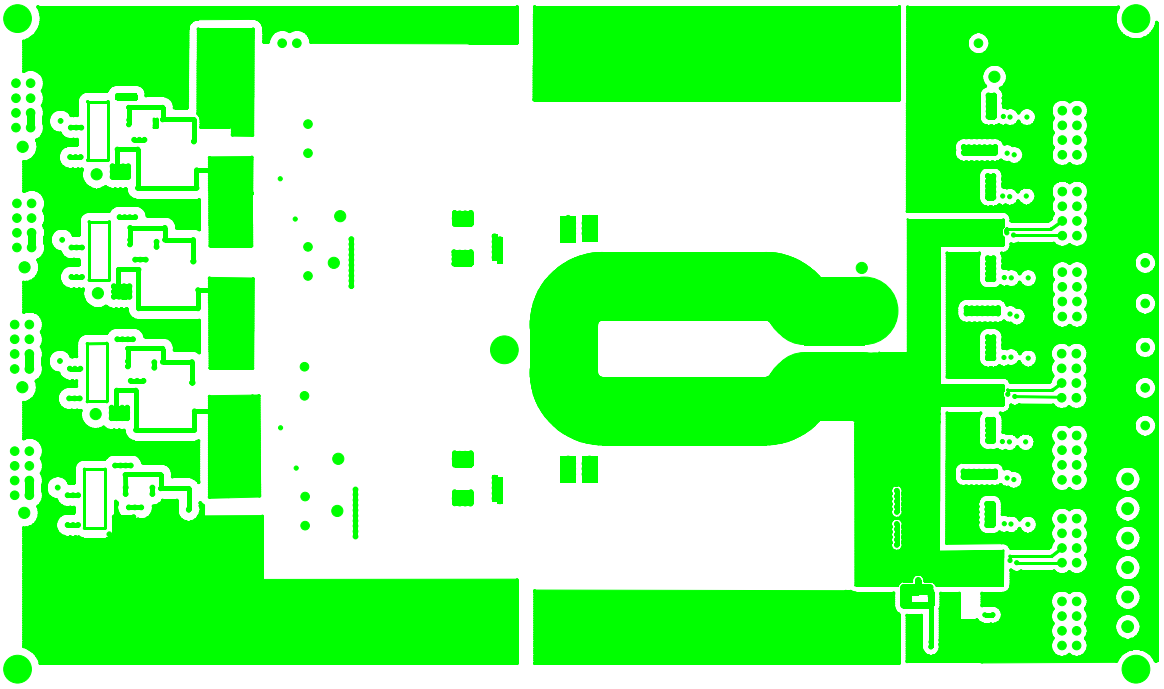


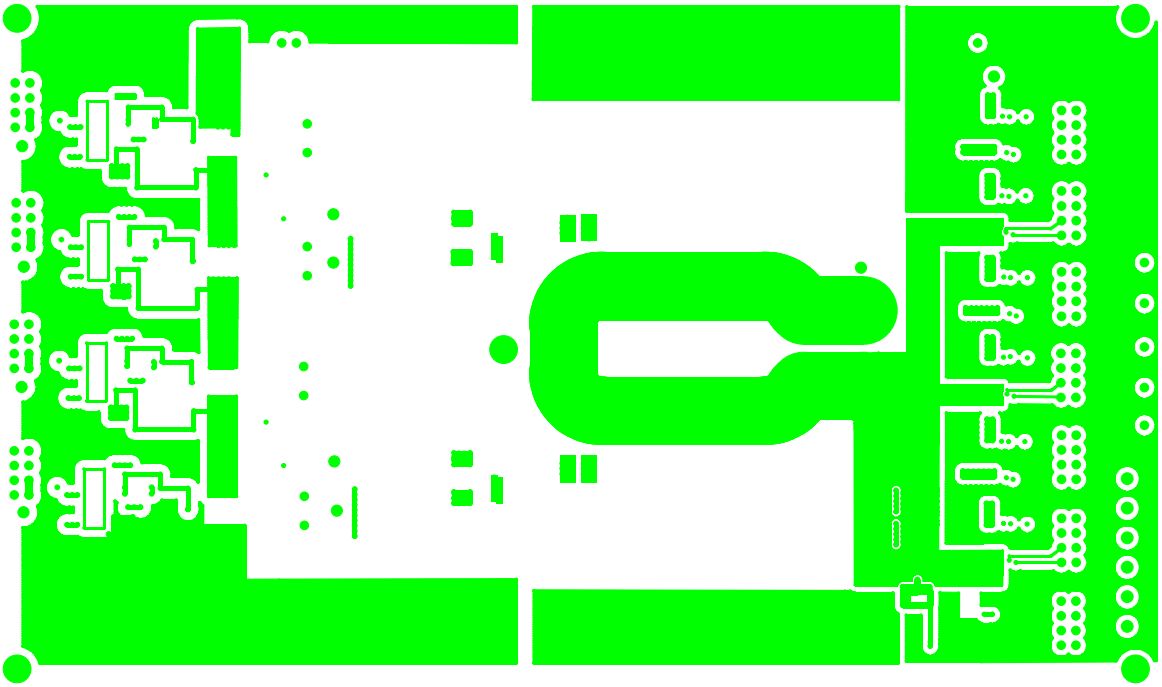


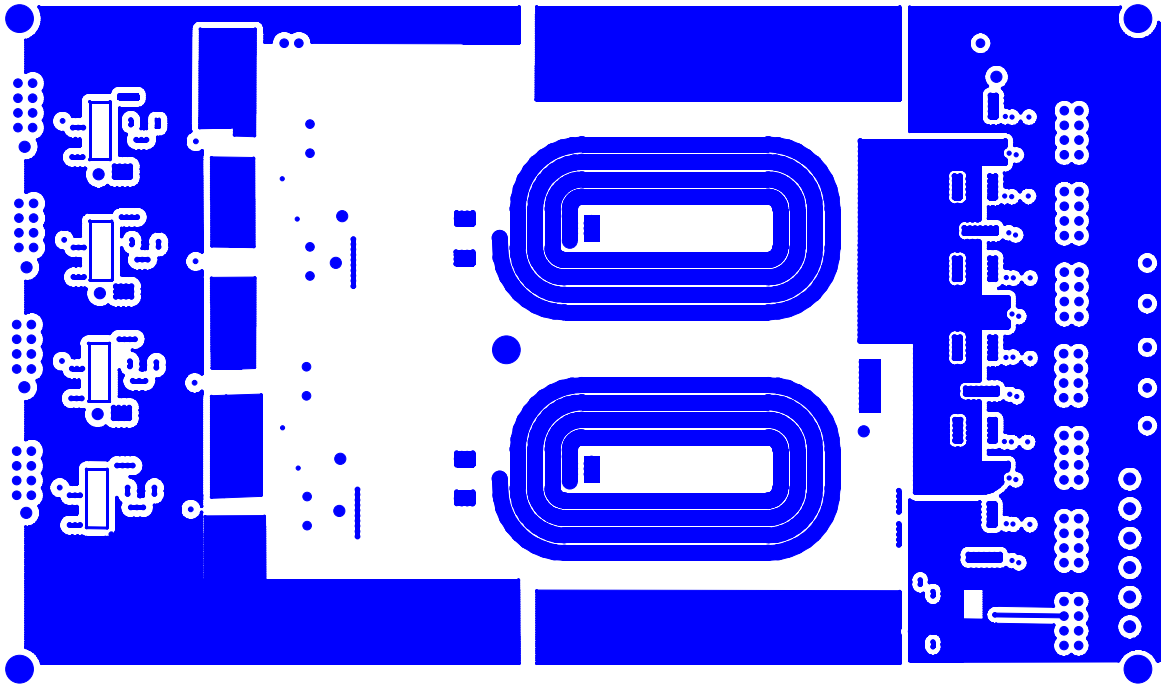


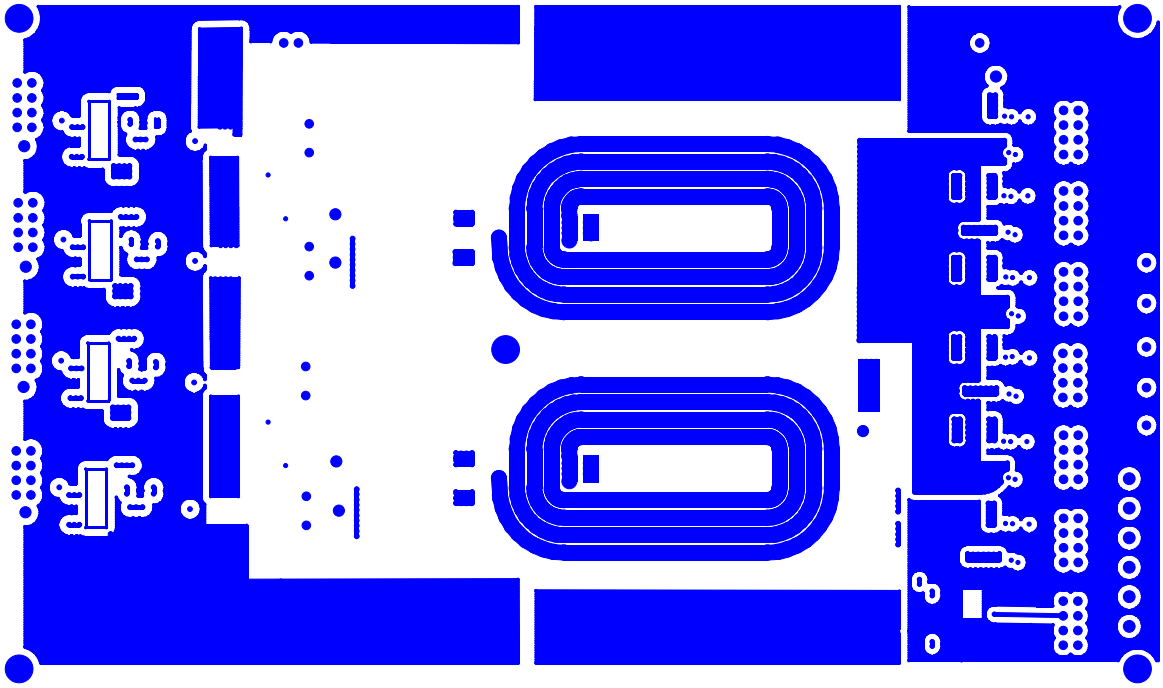


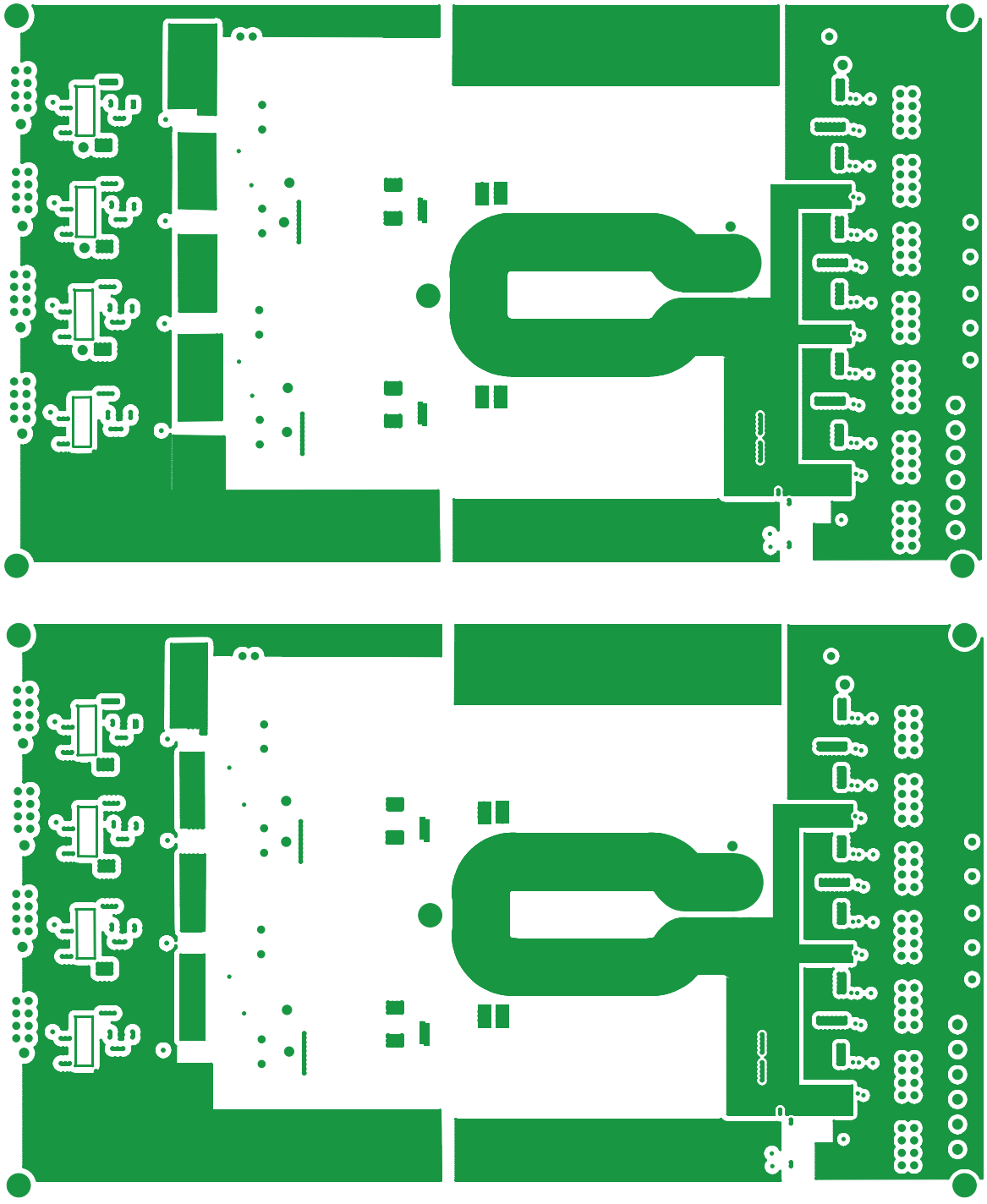


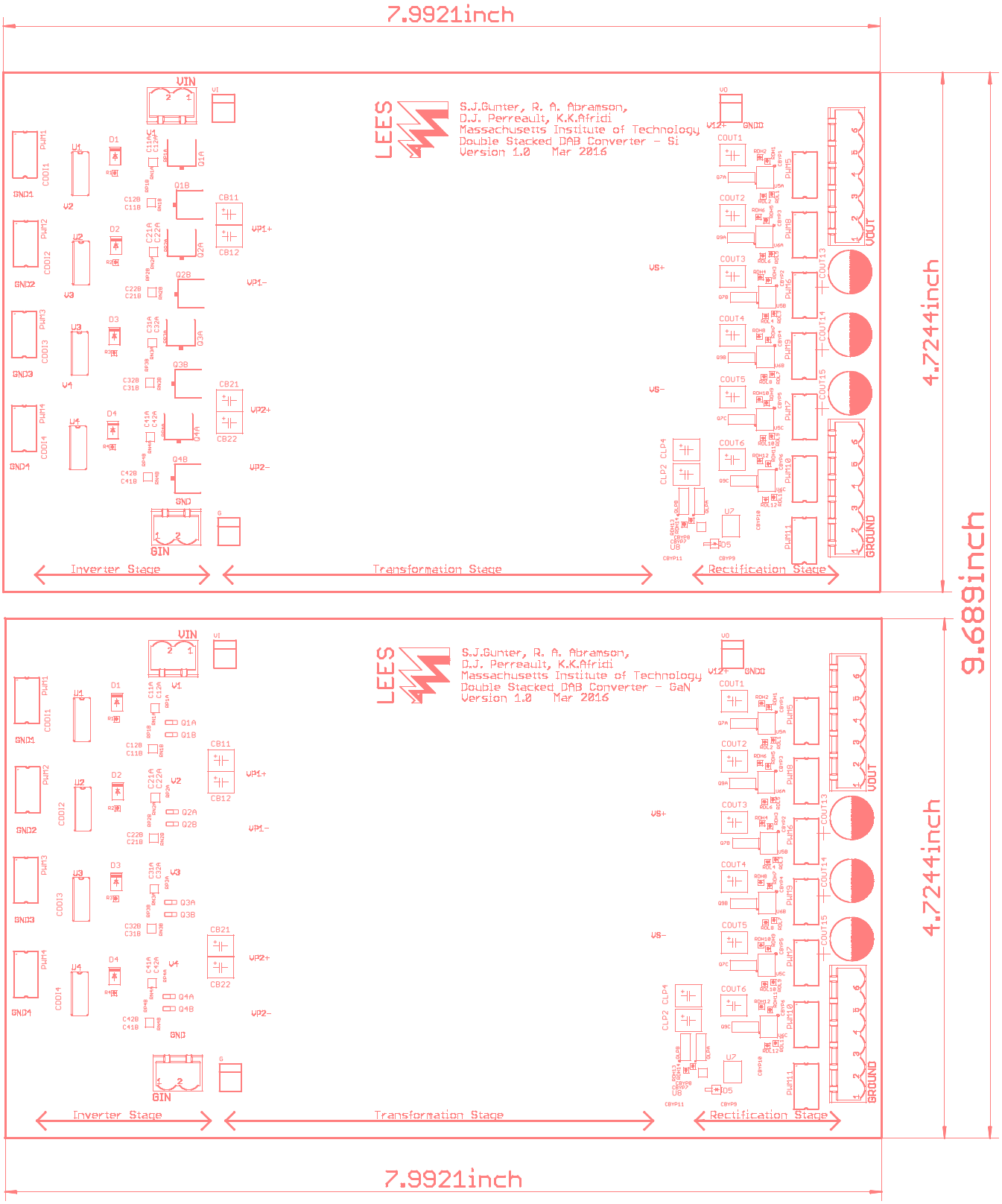








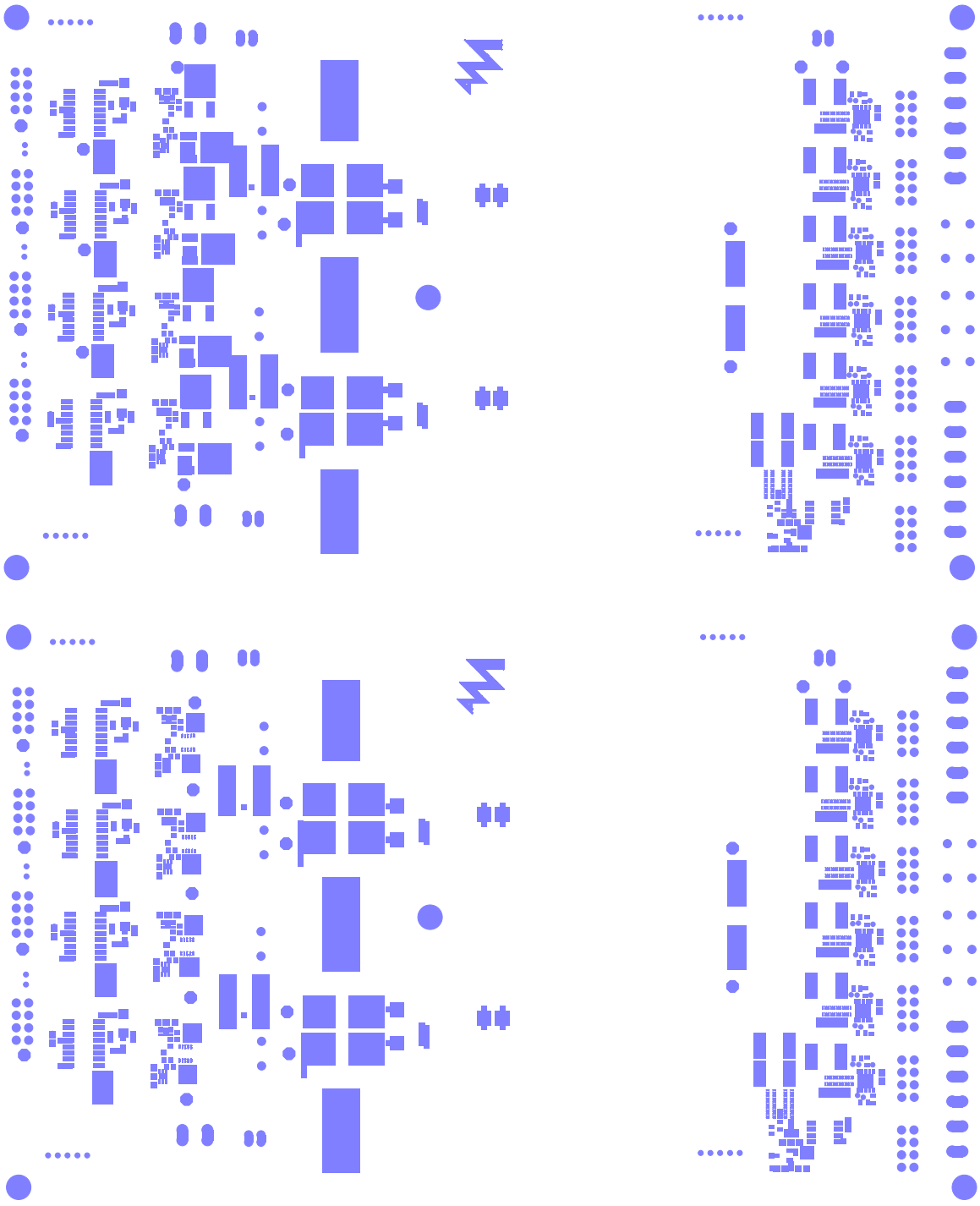


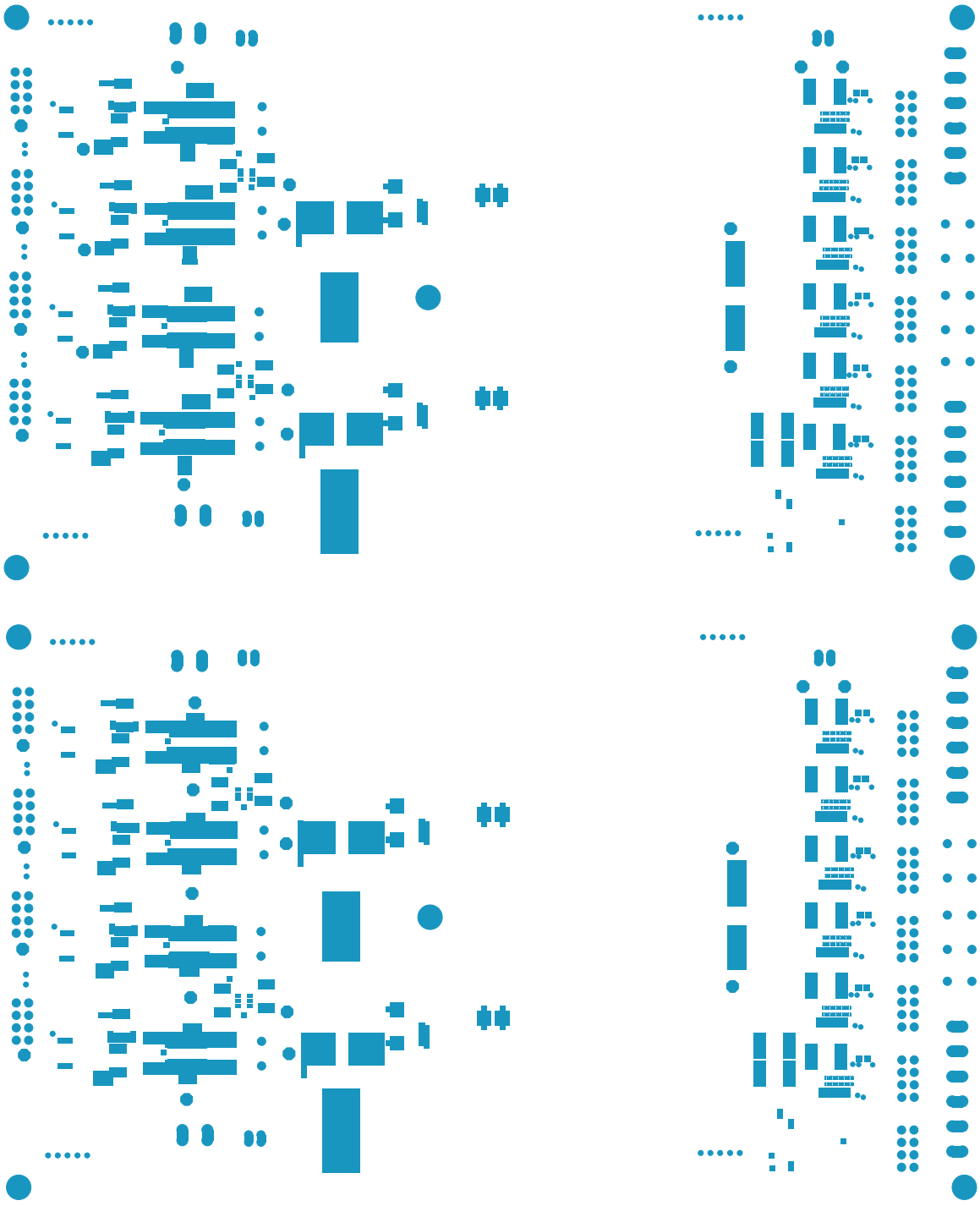


8 layers
2 oz copper for outer layers
4 oz copper for inner layers

FR4 Material
As thin as possible (62 mil or lower)
ENIG Finish
Blue Soldermask
White Silkscreen (both sides)

7.9921inch
4.7244inch
9.689inch
4.7244inch
7.9921inch





Appendix D

Bill-of-Materials for Prototype Converters

The Bill-of-Materials is included here for the GaN and Si Double-Stacked Active Bridge (DSAB) converters, as well as for the Si Superjunction Single-Stacked DAB converter.

As only a few devices differ between the boards, the Bill-of-Materials for the Si DSAB converter and the Si Superjunction Single-Stacked DAB converter simply list where their components differ from the GaN DSAB converter.

Table D.1: Bill of Materials for the GaN-Based Double Stacked Active Bridge Converter

Description	Part Number	Notes
CONN HEADER .100" DUAL STR 8POS	PRPC004DABN-RC	Ribbon connector from control
TERM BLOCK HDR 2POS VERT 5.08MM	1755736	Solder to board power connectors
TERM BLOCK PLUG 2POS 5.08MM	1792757	Plugin power connectors
CAP CER 1UF 50V X6S 0603	C1608X6S1H105K080AC	Maintain voltage - input to ISO
DGTL ISO 3KV 2CH GATE DVR 16SOIC	ADUM3223ARZ	Isolator and H-Bridge Driver, Dual input, 5V UVLO, Narrow
DIODE ULTRA FAST 200V 1A SMA	ES1D	Bootstrap Diode
RES 10 OHM 1/10W 1% 0603	RMCF0603FT10R0	Bootstrap Resistor to limit current
CAP CER 10UF 25V X5R 0603	C1608X5R1E106M080AC	Maintain voltages of driver
CAP CER 10UF 25V 10% X7R 1812	C4532X7R1E106K250KA	Maintain voltage - VDDA, VDDB of isolator/driver
IC GATE DRIVER 6SON	UCC27611DRVT	Single GaN FET Driver with voltage regulator, for inv. and LP switch
RES SMD 10 OHM 5% 1/10W 0402	ERJ-2GEJ100X	Resistor for pull up and pull down gate resistors
DIODE ARRAY GP 300V 225MA SOT26	MMBD3004BRM-7-F	Diodes for voltage balancing circuits
CAP CER 1UF 250V X7T SMD	CKG45KX7T2E105K290JH	Caps for voltage balancing circuits
TRANS GAN 200V 5A BUMPED DIE	EPC2012C	Inverter GaN FETs
TEST POINT PC MINI .040"D	5000, 5001, 5003, 5118	Test Points
CAP CER 0.33UF 250V 10% X7T 1210	C3225X7T2E334K200AA	Small caps across GaN FETs
CAP CER 3.3UF 250V 20% X7T SMD	CKG57NX7T2E335M500JH	Medium caps across GaN FETs, Blocking caps before transformers
CAP ALUM 56UF 200V 20% RADIAL	UCY2D560MPD1TD	Electrolytic input caps
CAP CER 100UF 16V 20% X7S SMD	CKG57NX7S1C107M500JH	Output caps
CAP POLYMER 1000UF 20% 16V T/H	APSG160ELL102MJB5S	Electrolytic output caps
FERRITE CORE	B66291GX149	E core for transformer
Ferrite Cores & Accessories I 43/4/28 N49 5900 +25%-25%	B66291KX149	I core for transformer
TRANS GAN 30V 60A BUMPED DIE	EPC2023ENG	Synchronous rectifier GaNFETs
IC GATE DVR HALF BRIDGE 4A 10LLP	LM5113SD/NOPB	Half-bridge driver for rectifier
CAP CER 6.8UF 10V 10% JB 0603	C1608JB1A685K080AC	Capacitors for LM5113 driver
KIT RES 1% 22 VALUES 50 EA 0603	PHH1-KIT	0603 resistor kit for P_out and N_out resistors of LM5113 (50x 1-7.5 Ohm)
DIODE SCHOTTKY 15V 1A POWERMITE	UPS115UE3/TR7	Bootstrap Diode for LP switch
IC REG LDO 5V 0.15A SOT23A-3	MCP1754ST-5002E/CB	On-board Regulator for LP switch
IC REG ISOLATED 5V 0.2A 7SOP	DCP010505BP-U	External regulator for LP switch
DGTL ISO 3KV 1CH GEN PURP 8SOIC	ISO7310FCQDRQ1	Isolator for LP switch
TERM BLOCK HDR 6POS VERT 5.08MM	1755778	Solder to board output power connectors
TERM BLOCK PLUG 6POS 5.08MM	1792799	Plugin output power connectors
HEX STANDOFF 6-32 NYLON 1-1/4"	4822	Standoffs
HEX NUT 5/16" NYLON 6-32	9606	Nuts for standoffs
WIRE JUMPER FEM-FEM 15CM 10PCS	MIKROE-511	Jumper cables for rectifier signals

Table D.2: Bill of Materials for the Si-Based Double Stacked Active Bridge Converter that differ from those in **Error! Reference source not found.**

Description	Part Number	Notes
RES SMD 0.47 OHM 5% 1/10W 0402	73L1R47J	Resistor for pull up and pull down gate resistors
MOSFET N-CH 200V 7.6A DPAK	FQD10N20LTM	Inverter MOSFETs

Table D.3: Bill of Materials for the Si-Based Single Stacked Active Bridge Converter that were not included in **Error! Reference source not found.**

Description	Part Number	Notes
RES SMD 0.47 OHM 5% 1/10W 0402	73L1R47J	Resistor for pull up and pull down gate resistors
CAP CER 2.2UF 450V X7T SMD	CKG57NX7T2W225M500JH	Medium caps across GaN FETs, Blocking caps before transformers
MOSFET N-CH 500V 13A PG-TO252	IPD50R280CE	Inverter MOSFETs
DIODE GEN PURP 300V 1A SMA	ES1F	Bootstrap Diode

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