A Current-Balancing Control System for Cellular Power Converters

by

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B.S.E.E. Electrical Engineering
Southern University and A & M College, 1993

Submitted to the Department of Electrical Engineering
and Computer Science in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 1996

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Abstract

The use of a cellular power converter architecture offers potential benefits in the construction of high power converters relative to conventional system designs. This cellular architecture is realized by the parallel connection of a large number of autonomous converters, or *cells*, designed for a fraction of the total load rating.

One design challenge is the implementation of a mechanism to control current-balancing among the paralleled converter cells. Current balancing is important in terms of the reliability, dynamics, and efficiency of the overall system. In order to perform current sharing in a distributed manner, the converter cells must be able to compare their output with respect to some average value and take action to achieve load balance.

The objective of this thesis work is to investigate a new approach for current-balance control which results in equal load sharing among the converter cells. A key attribute of the approach is that it uses only locally measured quantities to achieve load balance, without the use of additional inter-cell connections. Functional tests of a proposed design are conducted using a prototype cellular architecture.

Thesis Supervisor: John G. Kassakian
Title: Professor of Electrical Engineering and Computer Science

"I can do all things through Christ who strengthens me." - Phil. 4:13

Acknowledgments

In the midst of all that is to be done, deadlines that must be met, and things that require our immediate attention, I'm glad to know that I can always draw from an Infinite Source which provides constant help at all times. I first give thanks to God for saving and sustaining my life, for this thesis work could not have been completed without Him. He has bestowed upon me so many blessings and has done so many things, that if I had the rest of my life to write them all down, I would never finish. I only pray that He helps me to be *rooted and grounded in love,* that I *may be able to comprehend with all the saints what is the breadth and length and height and depth, and to know the love of Christ which surpasses knowledge, that* I *may be filled up to all the fullness of God.* - Eph. 3:17-19.

I would like to dedicate this thesis to my entire family whose fervent prayers and undying support have encouraged and uplifted me as far back as I can remember, and continue to this day. I love you all very much and I pray that God will continue to abundantly bless your lives. Particularly, to my father, Dr. Robert L. Selders, Sr., and my mother, Devoria H. Selders. Pops...thank you for all of the *swift kicks* and encouraging advice you never hesitated to give me when times got pretty rough here. I thank God that He has provided me with a father who is also my daddy, my role model, and one of my best friends. Moma...thank you for *helping* me during my growth process, it (your *help*) has been very real. I also thank you for your encouraging advice and your calm and humble spirit which continues to help me remain grounded.

To my finance', Keila Monique Legree (I couldn't wait to write that in my thesis). I thank God for who you are, and all that you have done. You have been my best friend, my

girlfriend, and now you are going to be my wife...umh, umh, umh, ain't God good!?! Thank you for prodding and motivating me to get this thesis done, especially during the times that I was straight up trifling! You are truly a gift from God. And to think, a few years ago, who would have ever thought that we would be at this point. I thank you for all of the special times we have shared together; and all those times you let me know that you care and are there for me no matter what. I look forward to spending the rest of my life with you. I'll always love you!

I want to also thank you, Professor John G. Kassakian, for your support during my entire time here at the Institute. God truly blessed me with someone who has been more than just a research advisor or thesis supervisor. I thank you for your encouragement and friendly advice, and helping me learn to think more clearly about different ideas and ways of presenting them. Dave Perreault, what can I say but thanks. You have endured my craziest of questions and you are still standing! Thanks for all of your technical expertise, time, and patience in helping me to complete this thesis. Moreover, thanks for your friendship during my short time in LEES. I wish you and Heidi the best in all that you endeavor to do and may God continue to bless you both.

God has a way of placing people in our lives who help us to grow in ways that are we would never imagine. To those individuals at the 'Tute' who provided support, counseling, and who "schooled" me on a number of things, I say thanks. But to my sisters...particularly Deirdre, Carla, and Robbin (my OME's)...y'all are some strong BWs. Keep your head up and always stay real. I'll just say, "Thank you for everything," and leave it right there 'cause I know you know what I'm talking about. To my brothers in the struggle, especially Ofori, Steve I., Mike, Christ R., James M., James W., and Don. Thanks for all the advice and time you all spent "schooling" me about the 'real deal.' I

also thank you all for providing me with good constructive criticism and a sound wall to bounce a lot of ideas off of.

To various BGSA, NSBE, and BSU members, the Office of the Dean of the Graduate School (particularly, Dean Colbert, Dean Tyler, and Nadine), Ayida, J.J., and Ann Davis Shaw...thanks for listening to all of my issues and offering comforting advice during the times I needed reminding that "trouble doesn't last always."

Thanks to the members of the Laboratory for Electromagnetic and Electronic Systems (LEES)...you all are a great group of people. Keep up the hard work and the 'positive *energy* flow'. To Barbara, Kathy, and Vivian...thanks for all your help, especially during my first few months at the Institute. Special thanks to Deron Jackson whose FrameMaker expertise, among other things, helped me to complete the text formatting for my thesis.

I would also like to thank Delco Electronics Corporation for affording me the opportunity to further my education via the DE Scholarship program. Additional thanks to Glen Hall, Jeanetta Burbridge, Lamar Crowder, Steve Rohr, and the Advanced Body Systems Engineering crew for their encouragement and support during my time away from Delco Electronics.

Finally, I would like to thank those members of the churches I attended in Cambridge (St. Paul A.M.E. Church) and in Kokomo (Mt. Pisgah Baptist Church) for welcoming and praying for and with me during my stay in these places. I also want to thank the Headley and Collins families for 'adopting' me and 'feeding' me while I was away from home.

In writing this thesis, I may have forgotten to mention others who should also be thanked. All I ask is that you charge it to my head and not to my heart, for it was certainly not intentional. A struggle has ended and many others are nascent, so with this, I leave MIT on this untimely adage:

"If there is no struggle, there is no progress." - Frederick Douglass.

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Chapter 1

Introduction

1.1 Background

Technological advances in semiconductor devices and the increased development of integrated control circuits have assisted in meeting the design demands posed by high power energy conversion systems. Such systems can be realized using conventional single large converter designs. However, the design of converter systems using a distributed approach can be useful in applications where high reliability, high switching frequencies, or substantial power levels are required [1]. Such applications include large motor drives and uninterruptible power supplies [2-4]. The design of high power converter systems using a more recent distributed approach, called a cellular architecture, provides several potential benefits compared to those systems designed by conventional methods [5]. A cellular architecture consists of a large number of converter *cells* connected in parallel to form a high power converter system, Fig. 1.1.

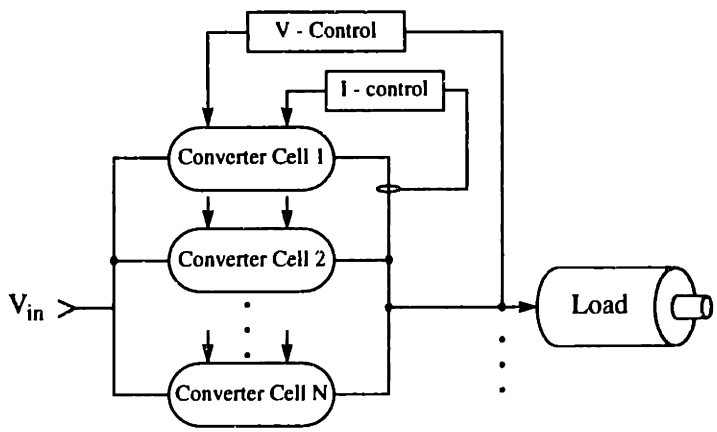


Figure 1.1: Diagram of a cellular converter system supplying a single load.

For many applications, cellular converter systems can offer significant benefits which can be used to enhance the performance characteristics of the overall system. Some areas in which attendant benefits can be realized include:

1) ***Modularity***: For some systems, the ability to adjust the output power level for changes in load requirements is desirable. Unfortunately, most single large converter systems often lack the flexibility for expanding in this manner. Cellular systems allow the user to adjust the number of cells as needed to maintain optimum operating conditions [6-9].

2) ***Thermal Management***: The total power is distributed among the cells, thereby eliminating the single point source of heat usually generated by single power modules. This can result in lower device junction temperatures which, in turn, could simplify and reduce the cost of the thermal management system [1, 5, 9].

3) ***Reliability/Availability*** through ***Redundancy***: When configuring the system using more cells than required by the minimum load, electrical and thermal stresses on the semiconductor devices can be reduced. Although the number of components in the cellular converter are increased, overall system reliability is likely to increase. This increased reliability is due to the degree of redundancy introduced by the distributed system, which is not present in conventionally designed systems [1, 5-7, 9-10].

4) ***Manufacturing processes***: Cellular converter systems can utilize the advantages offered by automated, high volume manufacturing processes in the construction of the cells. Cellular power converter systems designed using large numbers of autonomous cells has remained, for the most part, unexplored. However, it is believed that the use of automated assembly processes may yield superior results compared to the hand assembly processes used in manufacturing single large converter systems [1, 5].

A major design challenge in realizing the cellular system is the implementation of a technique which allows equal current sharing among the paralleled converter cells. In such systems, the cells are controlled in order to distribute the load current equally among them in an efficient, stable, and cost effective manner. Current sharing among paralleled

converter cells may be accomplished by using global control, information-sharing control, or autonomous control techniques. Global control techniques use a common feedback controller to determine and regulate each cell's operation [2, 3, 11-14].

Information-sharing control methods use distributed load-sharing controllers, along with additional circuitry or interconnections, to transfer current sharing information among the cells [15, 16]. Only very little information needs to be shared among the individual converter cells [22]. Therefore, control variables such as the highest cell current [24], rms cell current [23], or cell current stress [16] can be used to regulate the output current of each cell to achieve load balance.

For some applications, the use of a centralized controller, or the addition of interconnections between cells for current sharing may be undesirable for reliability reasons. Autonomous control methods are similar to information-sharing approaches, but implement load balancing without interconnections between cells [15, 17-20, 22]. One such scheme for paralleled constant-frequency inverters, using the fundamental system output voltage and frequency to transfer information among the controllers, is presented in [15, 17]. Unfortunately, this approach can have a high implementation cost and a complex control strategy. Furthermore, this approach only works for constant frequency inverters and cannot be used to parallel dc/dc or ac/dc converters.

This thesis investigates a new autonomous control approach for current sharing in cellular architectures. In this approach, current sharing information is encoded on the converter output bus at frequencies much higher than the fundamental output frequency of the converter system. Each cell injects onto the output bus a signal whose frequency is related to the output cell current. The aggregate frequency information is available to all of the connected cells via the output voltage. Each cell uses a frequency-based estimator to provide the local cell with current-sharing information based on the information

encoded in the output voltage. Different implementations of this new approach are developed and tested in a low power prototype system.

1.2 Thesis Scope

This thesis explores a new frequency-based current-sharing technique which can be used to achieve load balance among paralleled converter cells. It introduces the concept of a cellular architecture and presents several benefits the architecture could offer to high power converter systems.

In Chapter 2, a current-sharing control scheme based on this approach is discussed, in which the converter cells encode current-sharing information onto the output bus using small sinusoidal perturbations. A detailed explanation is presented of one possible implementation of this current-sharing method. The experimental evaluation of a low-power prototype cellular converter system which implements this approach follows in Chapter 3. Here, the static and dynamic current-sharing performance of the converter system is discussed.

Chapter 4 introduces an alternate scheme in which the perturbation signal is the cell's switching frequency ripple instead of a synthesized perturbation. We present the design and experimental evaluation of a frequency-based estimator for this approach and show its limitations. Finally, Chapter 5 presents conclusions and recommendations for future work.

Chapter 2

Injected Perturbation Method

In cellular architectures, it is desired that the converter cells share the load current equally. This chapter presents a technique which can be used to achieve load balance among connected cells using a perturbation source to encode current sharing information onto the output bus voltage. Coupled with a method to process this information, the cell's output voltage can be regulated.

Section 2.1 introduces a current-sharing technique in which sinusoidal perturbations are injected onto the output bus by each converter cell to encode current-sharing information, and describes the main components used to implement this method. Section 2.2 describes the information needed by each cell for current sharing and how it is computed from the aggregate output signal. We discuss the implementation of the perturbation source used in this method in Section 2.3. A description of the converter cell's power circuit follows in Section 2.4. Finally, we discuss the design of closed- loop controllers in Section 2.5.

2.1 Injected Perturbation Method

Figure 2.1 shows the block diagram of a current-sharing control method in which a sinusoidal perturbation is injected into the output (or input) current of the individual cells to encode current-sharing information. The magnitude and frequency of the perturbations generated by each converter cell are a function of the reference current of the cell as shown in Fig. 2.2. The frequency of the perturbations are much higher than the fundamental frequency of the converter system, but much lower than that of the switching

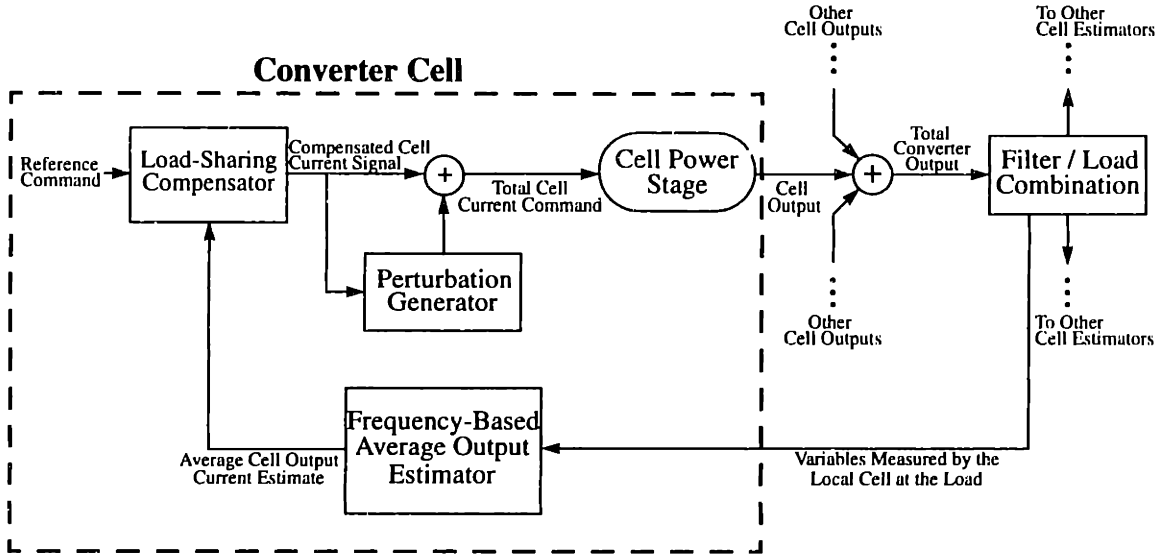


Figure 2.1: Block diagram of current sharing approach for cellular architecture which uses injected perturbations to encode load sharing information.

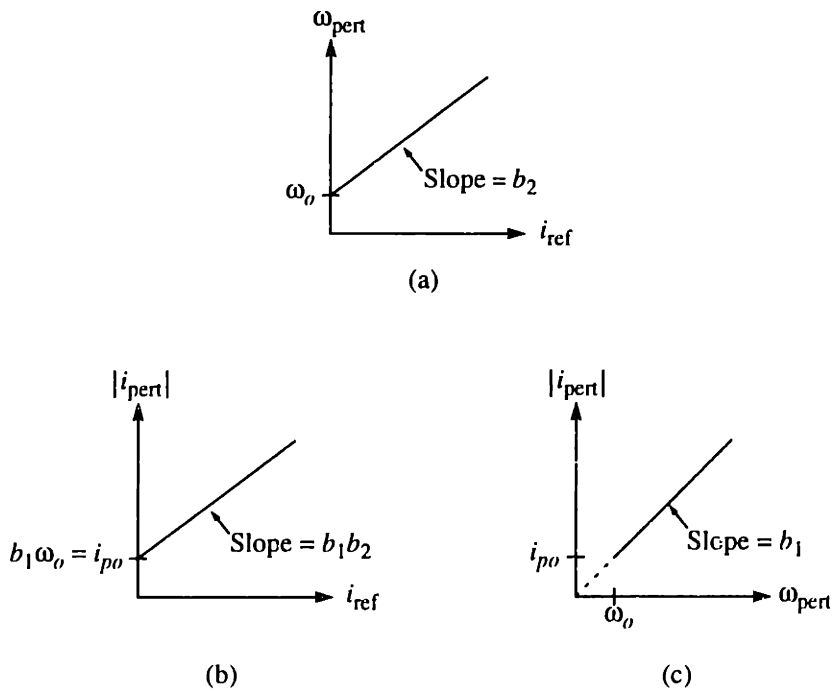


Figure 2.2: Graphs illustrating the relationship between: (a) the perturbation frequency and reference current; (b) the perturbation magnitude and reference current; and (c) the perturbation magnitude and perturbation frequency.

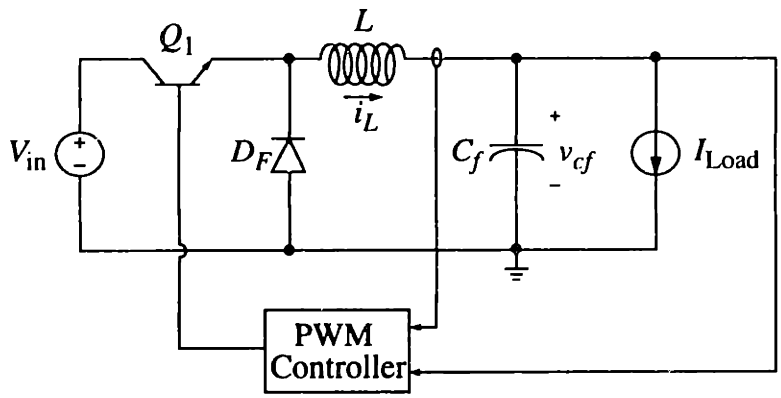


Figure 2.3: Circuit schematic of the buck converter in current-mode control.

frequency of the cell. Because the cell outputs are aggregated, this frequency information is contained in the aggregate output voltage signal and is available to each cell. Since there is frequency information related to the output current of each cell at the converter output, a method for extracting this information and processing it to achieve load-balance is necessary.

Each cell employs a frequency estimator circuit which computes a weighted rms average, ω_{est}, of the frequency content of the output signal. Each converter cell can then compare its generated perturbation frequency, $\omega_{pert,k}$, to the weighted rms average and adjust its output using a current-balancing controller to achieve load balance [12].

The converter cells were implemented as buck converters operating in current-mode control, Fig. 2.3. The converter cell power stage design and operation is described in detail in Section 2.4. The accuracy of the estimator and the performance of the controller determine the accuracy to which the cells equally share the load current. Since both the frequency estimator and current-sharing controller functions are replicated among the converter cells, they must be performed using simple, inexpensive circuitry. Figures 2.4 and 2.5 illustrate the structure of the frequency estimator and current sharing controller. The input to the estimator is the output voltage, v_{cf}. It is worth noting that $v_{\omega,est}$ and $v_{\omega,pert}$

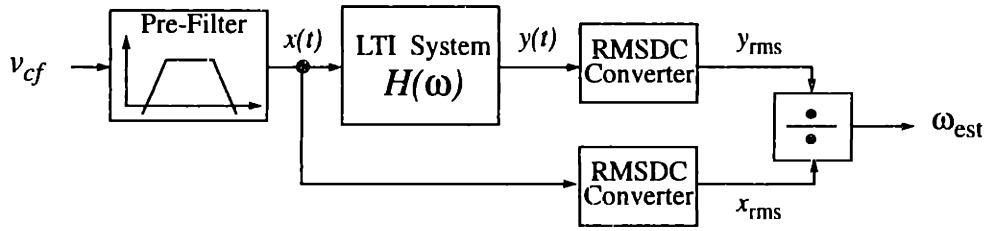


Figure 2.4: Block diagram of the estimator used to compute the weighted rms frequency of the aggregate output signal.

in Fig. 2.5, are voltages which are proportional to the rms frequency estimate and the frequency of the injected perturbation signal, respectively. Load balance can be regulated, for example, by adjusting the local converter voltage references. This is carried out by the reference voltage controller in Fig. 2.5, which adjusts v_{ref} based on the difference between $v_{\omega,est}$ and $v_{\omega,pert}$.

2.2 RMS Frequency Estimator

We have introduced the injected perturbation technique used to achieve load balance. In this section, we show how to compute an estimate of the rms frequency from the aggregated output signal using the estimator structure shown in Fig. 2.4.

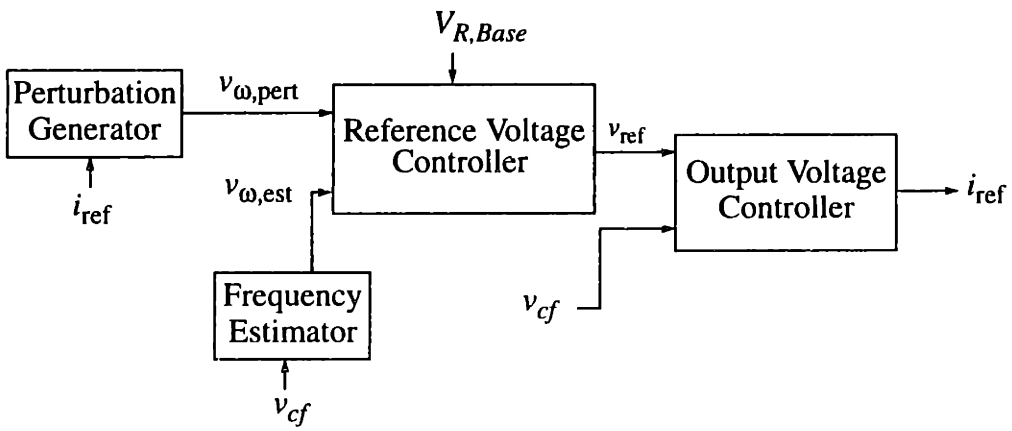


Figure 2.5: Functional block diagram of current sharing controller.

Assume that each cell generates a sinusoidal perturbation signal at a different frequency. For a system of N cells, the sum of these perturbations at the system output, $x(t)$, can be written as:

$$x(t) = \sum_{k=1}^{N} x_k(t) = \sum_{k=1}^{N} X(\omega_k) e^{j\omega_k t} \tag{2.1}$$

where $x_k(t)$ represents the perturbation signal generated by the kth cell and $k = 1, 2, ..., N$. The weighted rms frequency of $x(t)$ can be defined as:

$$\omega_{est} = \frac{\sqrt{\sum_{k=1}^{N} |X(\omega_k)|^2 \omega^2_k}}{\sqrt{\sum_{k=1}^{N} |X(\omega_k)|^2}} \tag{2.2}$$

where ω_k is the perturbation frequency generated by the kth converter cell. Since we only have N perturbation frequencies from the outputs of the N cells, the *power spectral density* (PSD), $S_x(\omega)$, of the aggregate signal and the corresponding rms value of $x(t)$ can be given as:

$$S_x(\omega) \equiv 2\pi \sum_{k=1}^{N} |X_k|^2 \cdot \delta(\omega - \omega_k) \tag{2.3}$$

and

$$x_{rms} \equiv \sqrt{\frac{1}{2\pi} \int_{-\infty}^{\infty} S_x(\omega)\, d\omega} = \sqrt{\sum_{k=1}^{N} |X_k|^2}. \tag{2.4}$$

Consider passing $x(t)$ through an LTI system, with frequency response $H(\omega)$, to obtain a new signal $y(t)$. The PSD of the input and output signals are related by:

$$S_y(\omega) = |H(\omega)|^2 \cdot S_x(\omega) . \qquad (2.5)$$

Therefore,

$$S_y(\omega) = 2\pi \sum_{k=1}^{N} |H(\omega_k)|^2 \cdot |X_k|^2 \cdot \delta(\omega - \omega_k) \qquad (2.6)$$

and

$$y_{rms} \equiv \sqrt{\frac{1}{2\pi} \int_{-\infty}^{\infty} S_y(\omega)\, d\omega} = \sqrt{\sum_{k=1}^{N} |H(\omega_k)|^2 \cdot |X_k|^2} \quad . \qquad (2.7)$$

If the frequency response of the system over the encoding range of interest is an ideal differentiator, $H(\omega) = j\omega$, then the ratio of *(2.7)* to *(2.4)* has the form of the weighted rms frequency estimate shown in *(2.2)*. Here, the magnitude of the perturbation signals correspond to the weighting coefficients.

To implement the result found in *(2.2)* using analog circuitry, we employ: 1) a filtering function to realize the differentiator, 2) a method to compute the rms signals x_{rms} and y_{rms}, and 3) a method to compute the ratio between y_{rms} and x_{rms} to obtain the final ω_{est} signal. This weighted rms frequency can also be computed using digital hardware. If the aggregate signal, *x(t)* is sampled at a high enough rate, a microcontroller or digital signal processor (DSP) integrated circuit may be used to compute the weighted rms estimate value using equations similar to those derived for the analog case.

2.2.1 Implementation of the Frequency Estimator

A frequency estimator is used by each cell to compute the weighted rms frequency of the aggregate output signal. This estimator was designed to implement the result shown by *(2.2)* derived in Section 2.2 using simple, low-cost circuitry. The following describes

the design of the estimator. It should be noted that the detailed circuit schematics can be found in Appendix B, Figs. B.1 and B.2.

Figure 2.6 shows the circuitry used to implement the frequency estimator. It is composed of four sections: 1) pre-amplification and pre-filter stage, 2) gain and differentiation stage, 3) rms to dc conversion stage, and 4) division stage.

The prototype system is designed such that the perturbation frequencies are in the range of 5-10 kHz. This frequency range is much lower than the 200 kHz switching frequency of the converter cells, but much higher than the bandwidth of the output voltage controllers. The resulting maximum output voltage perturbation amplitude is approximately 0.25 mA (50 mV). Since we are only concerned with the perturbation components of the output voltage, a 2nd order high pass Butterworth filter (f_c = 500 Hz) is used to reject the low frequency components of v_{cf}. In order to keep the gain constants in

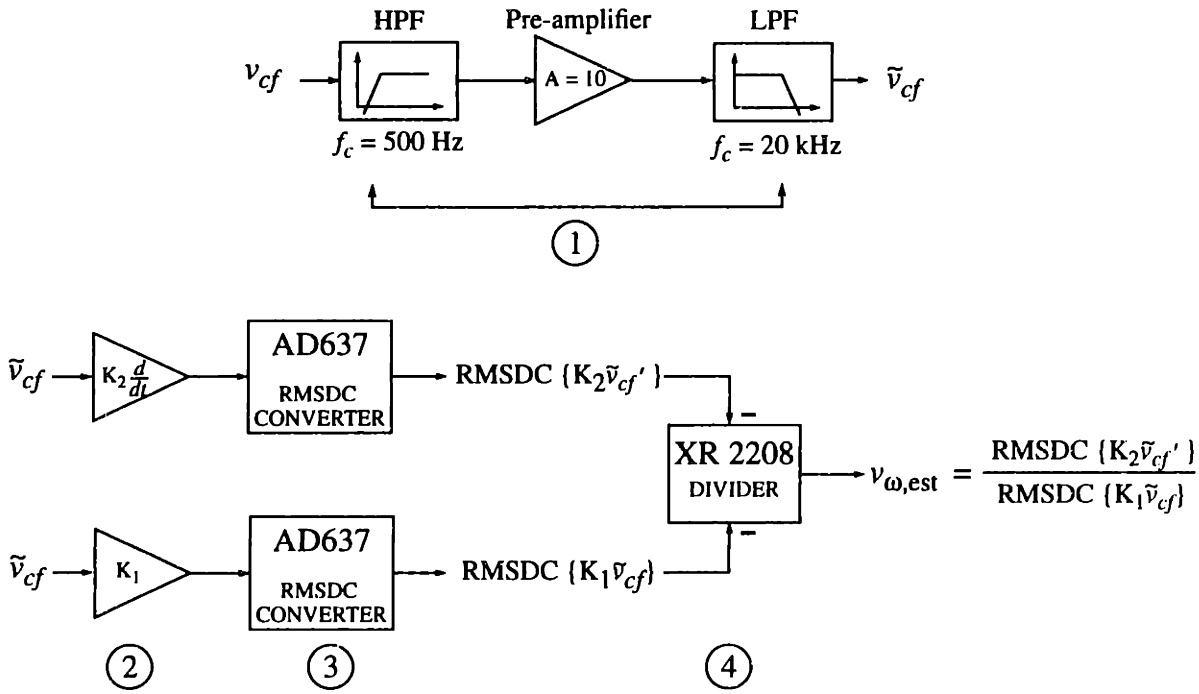


Figure 2.6: Functional block diagram of frequency estimator circuit.

the second stage at reasonable values, we follow this with a gain = 10 pre-amplifier. To reject high frequency components which may corrupt the final result, we pass the pre-amplified perturbation signal through a 2nd order Low Pass Butterworth filter (f_c = 20 kHz).

The rms to dc conversion circuitry allows a maximum continuous rms input of 7 V_{rms} (peak input transient of ±15 V_{pp}). The gain and differentiation stages thus have gain constants such that this maximum rating is not exceeded, while still providing the proper scaling to accurately compute the weighted rms value. We use a band-limited differentiator circuit which generates the derivative of the input signal over the frequencies of interest, but which has limited high frequency gain.

The rms to dc conversion stage uses two Analog Devices, AD637 high precision, wideband rms-to-dc converters. These devices compute a local-time rms value of the output ripple voltage and its derivative. The AD637s are each connected in a two-pole Sallen-Key filter configuration with the capacitors selected to give 1% settling time and averaging error (See Appendix B, Fig. B.1 for details). Using this particular connection allows the use of larger averaging capacitors, C_{av}, which reduce the peak value of the ac ripple component in the averaging error. This helps to maximize the accuracy of the measurement being made.

The divider circuit in the prototype system is implemented by placing a four-quadrant multiplier in the feedback path of an operational amplifier. The XR2208 operational multiplier combines both the multiplier and op-amp plus a high frequency buffer in a single monolithic circuit, and is suitable for the computational requirements of the system. The inputs to the divider must be negative values in order to stabilize the feedback loop. Therefore, we invert the rms to dc outputs before they enter the divider circuit. It is worth noting that this particular device seemed to be very susceptible to potentiometer drift after

trimming the circuit for the divider operation. An output compensation circuit was used to ensure that the final voltage corresponding to the average rms frequency was accurate over the perturbation frequency range. One way to alleviate the trimming problem is to use a computational unit with better stability and accuracy. Logarithmic computational circuits avoid the inherent trimming and stability issues of the approach employed here. The only drawback is that the computational unit alone may significantly increase the overall cost of the current-balance controller.

2.3 Perturbation Generation

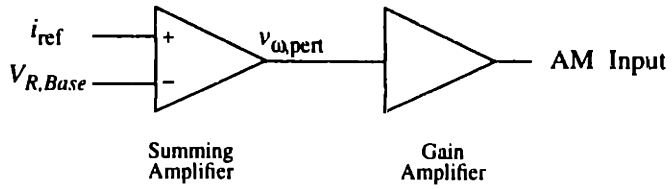
This section describes the operation of the perturbation generator which generates sinusoidal signals whose magnitude and frequency are related to the local reference current. Each converter cell generates its own perturbation signal and injects it onto the output bus. These signals are summed and their frequency content appears in the spectrum of the aggregate output voltage. This frequency information can then be processed by the each cell to regulate load balance.

2.3.1 Implementation of the Perturbation Generator

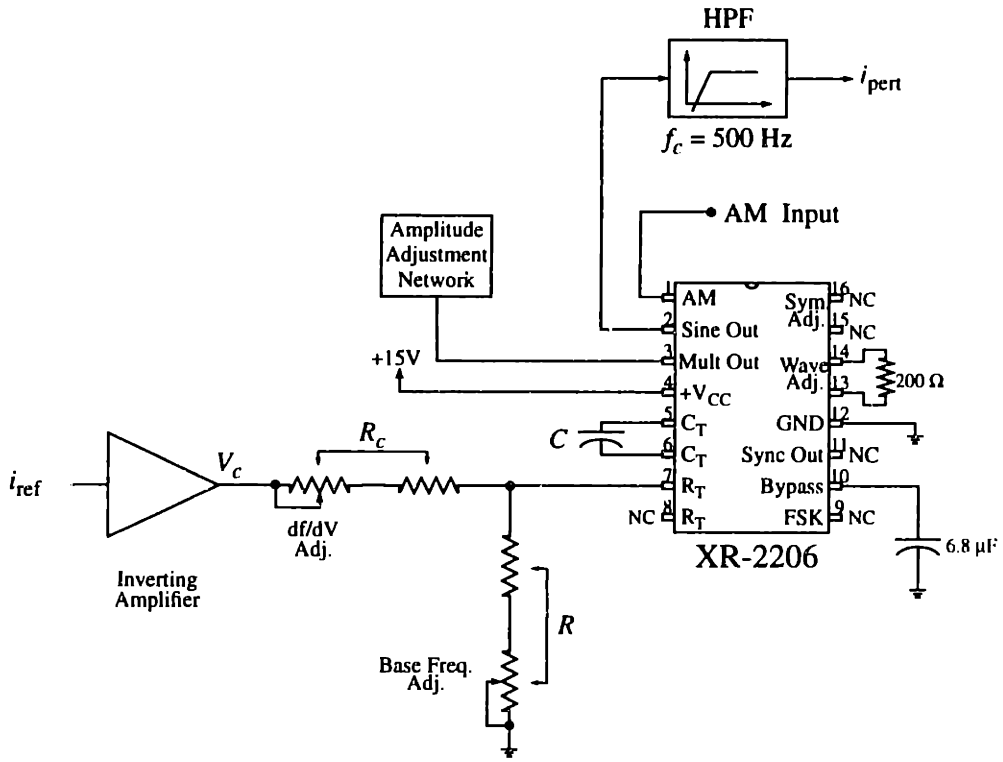
Figure 2.7 shows a functional representation of a perturbation generator which implements the relationships illustrated in Fig. 2.2, and is described as follows:

(1) Base Perturbation Frequency (ω_o) vs. Cell Reference Current (i_{ref}):

For this method, we chose a base perturbation frequency of ω_o = 5 kHz and a perturbation frequency range from 5 - 10 kHz over values of i_{ref} from 0 - 5 V (0 - 25 mA). For a 1 V change in the local i_{ref}, there is a change of 1 kHz in the perturbation frequency. In Fig. 2.7(a), $V_{R,Base}$ is fixed at 5 V to help ensure a base frequency of 5 kHz. By adjusting the df/dV potentiometer in Fig. 2.7(b), the frequency-to-voltage ratio, denoted by b_2 in Fig. 2.2(a), can be set so that the correct relationship between perturbation frequency and reference current is maintained at 1 kHz/V.



(a)



(b)

Figure 2.7: Functional diagram of perturbation generator: (a) Circuits used to generate $v_{\omega,pert}$; and (b) Circuitry needed to maintain the correct frequency to voltage and amplitude relationships between i_{pert} and i_{ref}.

(2) Perturbation Magnitude $|i_{pert}|$ vs. Cell Reference Current (i_{ref}):

For the maximum current reference signal (i_{ref} = 5 V), the amplitude adjustment network is used to set the maximum perturbation magnitude to be approximately 0.25 mA (50 mV) at ω_{pert} = 10 kHz.

If relationships (a) and (b) of Fig. 2.2 are satisfied, then relationship (c) is automatically satisfied.

The XR2206 Monolithic Function Generator, along with the proper amplifiers, allow the base perturbation frequency ω_o, perturbation magnitude $|i_{pert}|$, and the frequency-to-voltage ratio to be adjusted to satisfy the above relationships. As shown in Fig. 2.7(a), 5 V is added to the voltage representation of the reference current signal to obtain $v_{\omega,pert}$, the voltage representation of the perturbation frequency. The gain amplifier is used to bias the XR2206 in a region which modulates the output frequency linearly. The output of the XR2206 is passed through a high pass filter (f_c = 500 Hz) to reject an internally generated dc level present in the output signal. Figure B.3 in Appendix B shows the circuit in its entirety.

Before the converter cells were connected in parallel, each one was tested individually to ensure that the perturbation source generated the proper frequency over the range of i_{ref} values. Table 2.1 shows the perturbation frequency generated by each converter cell for the applied i_{ref} compared to the ideal perturbation frequency for the same i_{ref}.

Table 2.1: Generated perturbation frequencies for i_{ref} values 0 - 5 V (R_{Load} = 200 Ω).

Converter	0 V	1 V	2 V	3 V	4 V	5 V
Ideal	5 kHz	6 kHz	7 kHz	8 kHz	9 kHz	10 kHz
#1	5.08 kHz	5.95 kHz	6.95 kHz	7.95 kHz	8.98 kHz	10.2 kHz
#2	4.98 kHz	5.9 kHz	6.98 kHz	8.06 kHz	9.08 kHz	9.98 kHz
#3	5.03 kHz	5.97 kHz	7.03 kHz	8.08 kHz	9.11 kHz	10.2 kHz

2.4 Converter Cell Power Stage

It has been shown how to generate a perturbation signal whose frequency is related to its local reference current. Each cell can also compute the weighted rms frequency value

of the output signal. Now we look at the design of the converter cell which uses the above components in its controller to regulate the output bus voltage.

Figure 2.8 shows the circuit schematic representation of the current-mode controlled buck converter used for the cell's power stage. The input to output voltage conversion ratio is equal to the duty ratio:

$$D = \frac{V_{out}}{V_{in}}. \tag{2.8}$$

Starting with an input voltage of $V_{in} \cong 15$ V, we regulated the output voltage of the system so that $v_{cf} = V_{out} \cong 5$ V; therefore, $D \approx 0.33$. The LF411 is used to generate the cell current command signal from the perturbation and current reference signals. Since the perturbation magnitudes are small, large amounts of noise can affect the accuracy of the command signals. Before the current command signal is compared to the fedback sensed output cell current, they are both passed through a low pass filter ($f_c \sim 40$ kHz) to eliminate high frequency noise. The comparison is made using a fast, precision comparator, AD790, with maximum propagation delay of 45 ns and maximum input offset of 250 μV. Because high switching speeds are desired to reduce passive component sizes, this section of the converter cell power stage must be very fast to maintain good switching performance and accuracy of the cell.

The switching power stage was implemented using the Unitrode, UC3843 current mode PWM controller, since we were operating at a very low power level per cell (approximately 150 mW/cell maximum). The comparator output was used as the input to the UC3843's current sense pin. The output of the comparator is a 0-5 V PWM signal, with the gate drive provided by the UC3843.

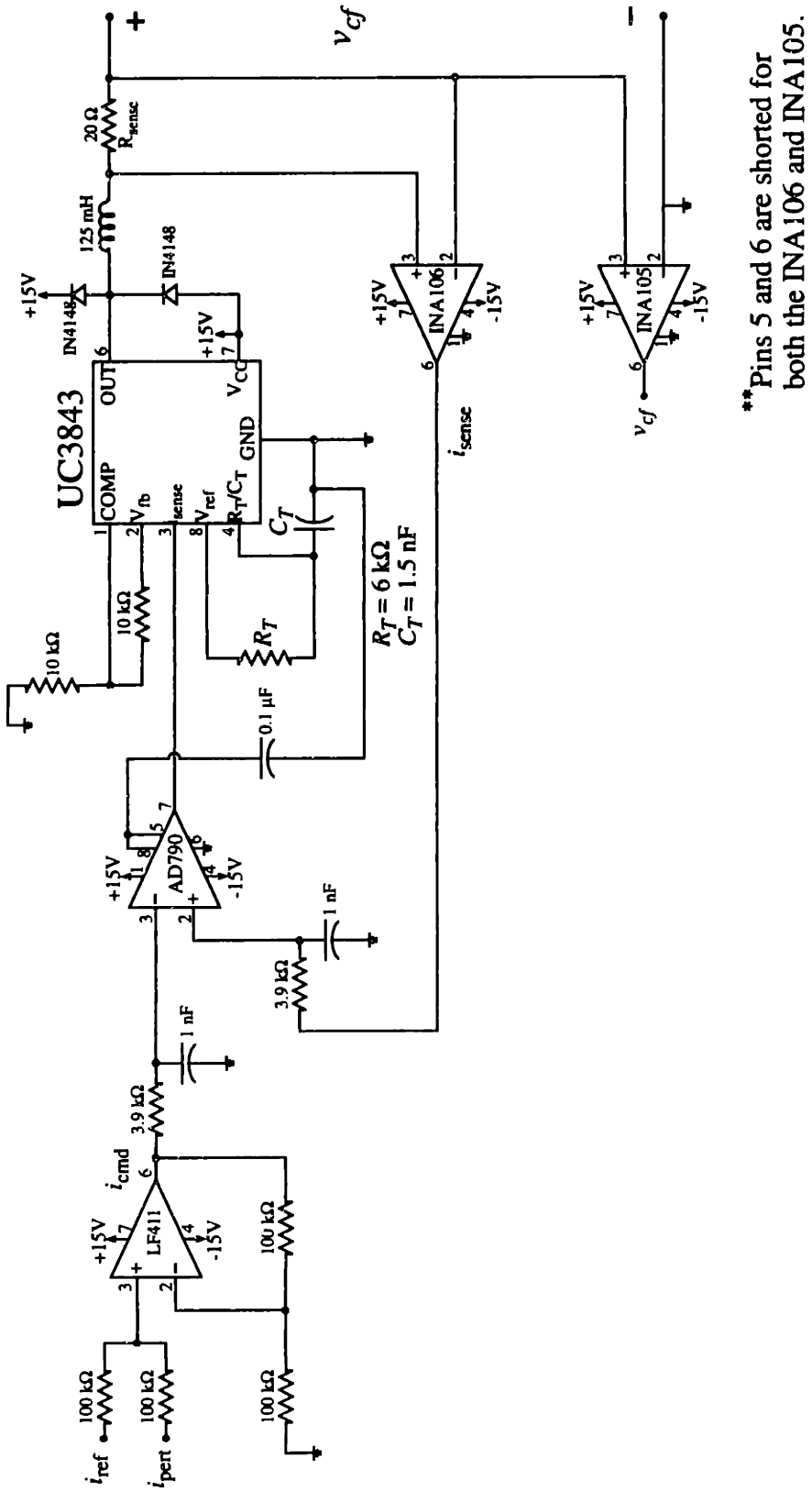


Figure 2.8: Schematic representation of current-mode controlled buck converter cell.

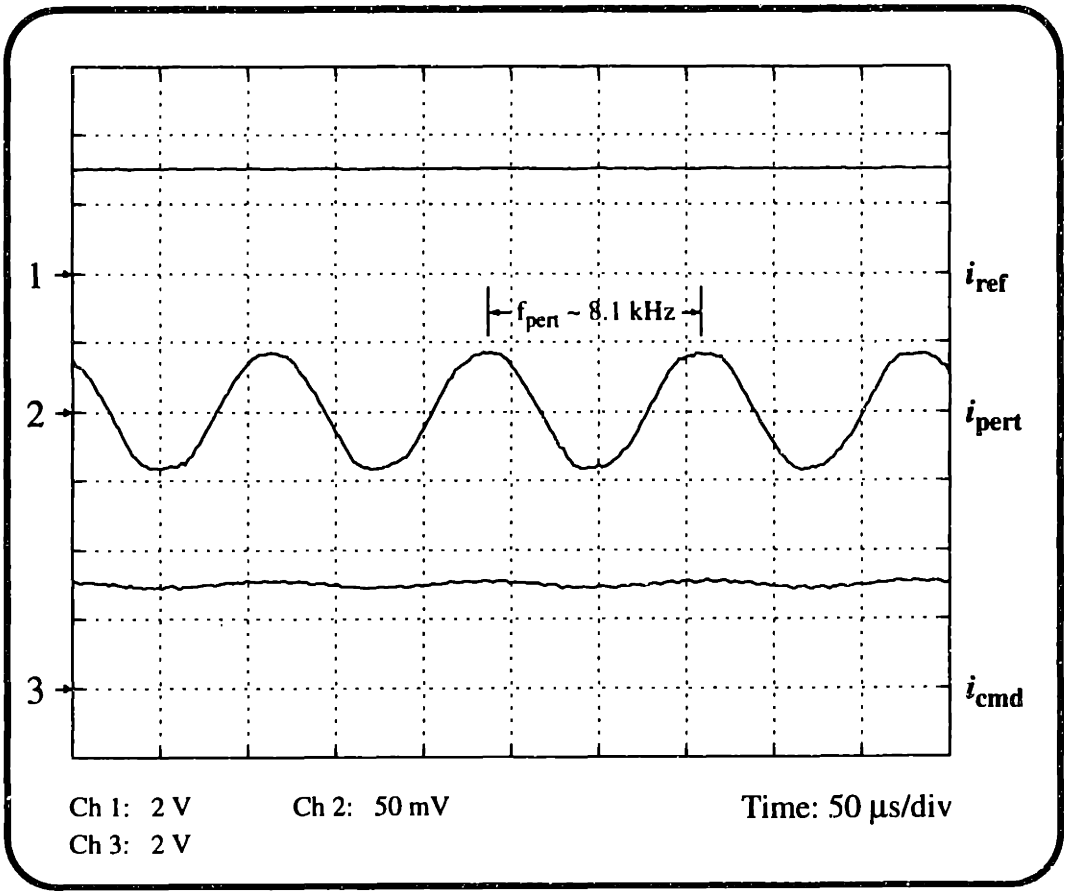


Figure 2.9: Current command (i_{cmd}) signal waveform generated from the reference current and perturbation signals i_{ref} and i_{pert}, respectively.

Operational testing of each converter cell was done by powering it up and operating it in a current feedback mode with an applied reference signal without a voltage control loop. Several test points were then observed to determine the functionality of the cell. The following presents the results from testing one cell since they are all similar.

The reference current signal, i_{ref}, is a 0-5 V signal representing a reference current value of 0-25 mA. During the test, i_{ref} was varied over its full range to verify correct operation of the converter cell. The waveforms in Figs. 2.9 - 2.12 reflect parameter measurements using: $C_f = 0.33$ µF, $R_{Load} = 301$ Ω, and $i_{ref} \approx 3$ V (15 mA). The current perturbation signal shown in Fig. 2.9 has a value of approximately 0.165 mA (33 mV_{pp}) with a frequency of 8.1 kHz. Also shown in this figure is the current command output,

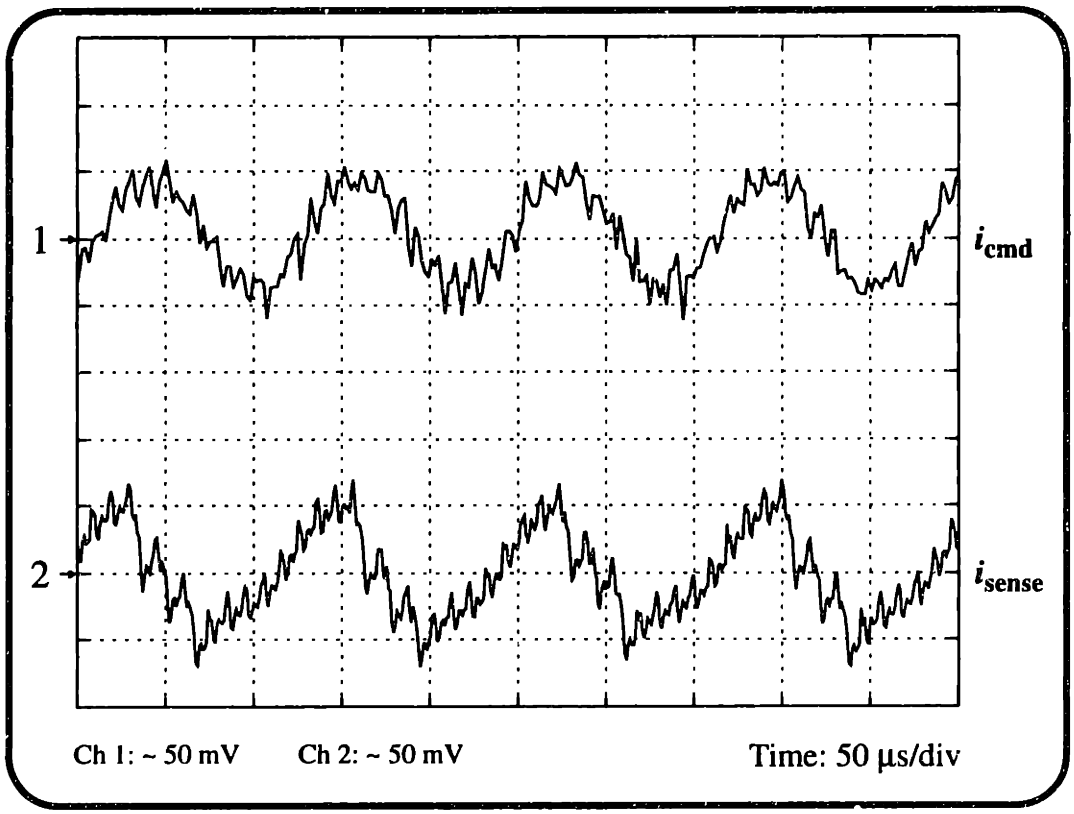


Figure 2.10: Current command and sensed output current signal inputs to the AD790 comparator. The waveforms are AC coupled.

i_{cmd}, of the LF411 from Fig. 2.8. As expected, the command signal has the dc level of the reference signal with the perturbation signal superimposed. Figure 2.10 shows the waveforms of the commanded current and sensed output current signals. The commanded current signal is filtered and compared to the filtered version of the fed back sensed output cell current by the AD790 comparator. The AD790 generates a low voltage signal which commands the power stage driver, UC3843. Figure 2.11 shows the form of the outputs of the AD790 and the UC3843 for the converter cell in open-loop operation. This operation mode is termed open-loop because the reference current signal is constant for all time and is not varied to regulate the output voltage to the desired value. The inner current loop formed by the fed back sensed output current is used to regulate the inductor current, but this feedback loop does not regulate the output bus voltage.

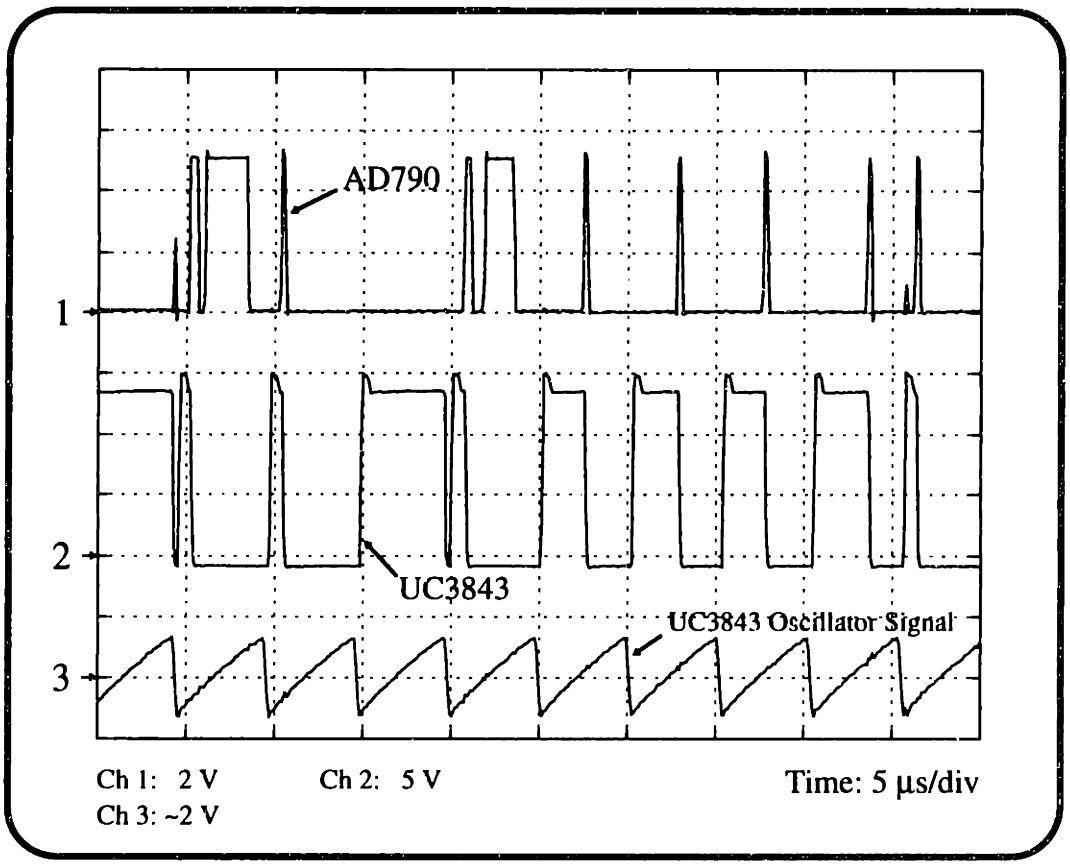


Figure 2.11: Typical PWM output signals of the AD790 and the UC3843. The oscillator signal of the UC3843 is also displayed to show the cell's switching frequency (~200 kHz).

The switching frequency of the cell was set by adjusting the timing resistor, R_T and capacitor, C_T of the oscillator section of the UC3843. From the UC3843 data sheet:

$$f_s \approx \frac{1.72}{R_T C_T}$$

where f_s = 200 kHz if R_T = 6 kΩ and C_T = 1.5 nF.

The output of the comparator is connected to the current sense input of the UC3843. This current sense input signal is the input to the UC3843's internal current sense comparator whose output is high whenever the output of the AD790 is high. The output of this current sense comparator is connected to the reset pin of the UC3843's internal PWM latch. At the peak of the oscillator signal, the internal latch is set high. If the

AD790 output is high ($i_{sense} > i_{cmd}$) at this point, then the output of the UC3843 is low because the latch gets reset. This is analogous to the switch in the power stage being turned off for a period of time and the inductor current discharging as it circulates through the freewheeling diode. A similar scenario occurs when the AD790 output is low at the peak of the oscillator signal.

The current perturbations, scaled by the effective load/filter impedance, show up on the output ripple voltage. The waveforms are shown in Fig. 2.12, and Fig. 2.13 shows the frequency content of the output voltage signal (the dc component is not displayed). The frequency of this perturbation is seen to be approximately 8.1 kHz.

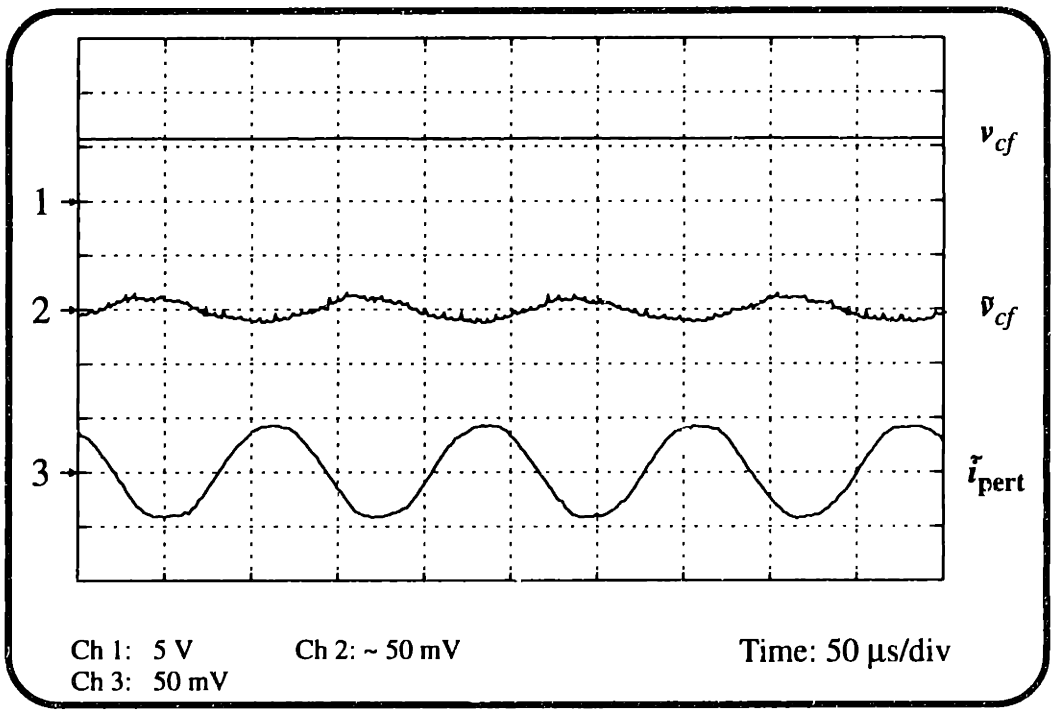


Figure 2.12: Output voltage waveforms and current perturbation signal.

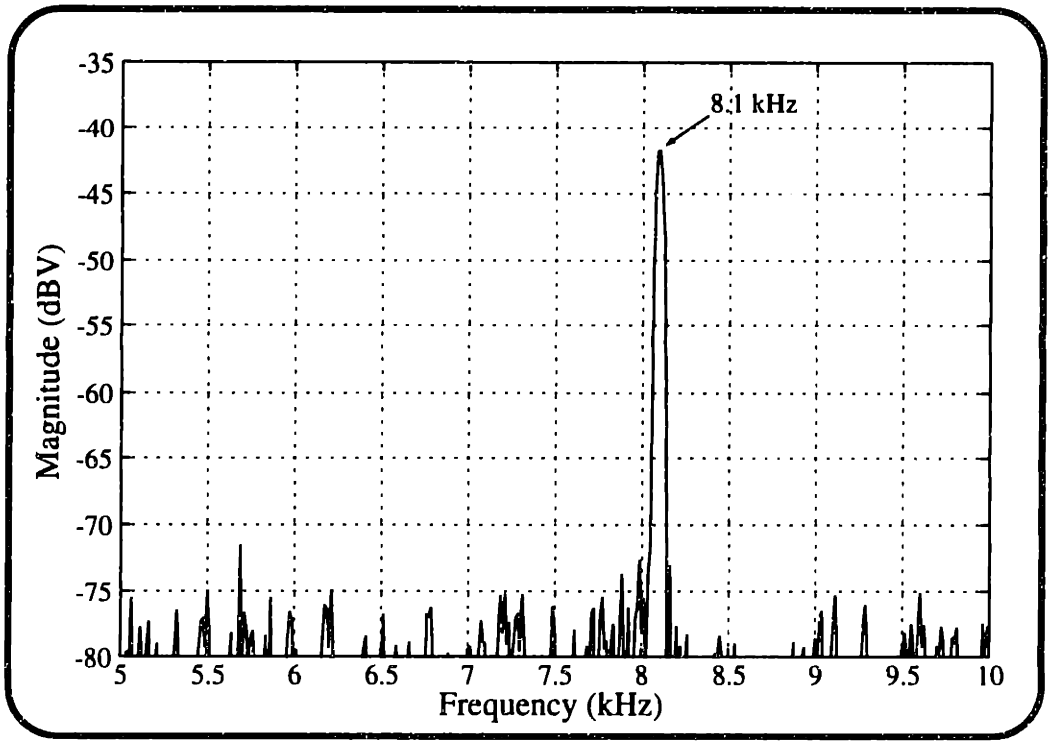


Figure 2.13: Spectrum analyzer plot illustrating frequency content of output voltage signal, v_{cf}.

2.5 Closed-Loop Controllers

One of the goals of this thesis work was to design a simple controller which could be used to achieve load balance among the converter cells in a stable and efficient manner. That is, for small disturbances, or perturbations due to input variations, load changes, etc., the cell should not exhibit oscillatory behavior. These controllers are implemented in a multiloop fashion. Around the innermost current loop, we employ a slower output voltage controller which sets the inner current-loop reference to regulate the output voltage to a voltage reference. Outside of this loop we employ an even lower bandwidth controller which varies the local reference voltages to achieve current balancing among the converter cells. Figure 2.14 shows in more detail how the control signals interact.

In the discussion on the open loop operation of the converter cell, Section 2.4, we presented the results of the large-signal behavior of the cell for a fixed reference current

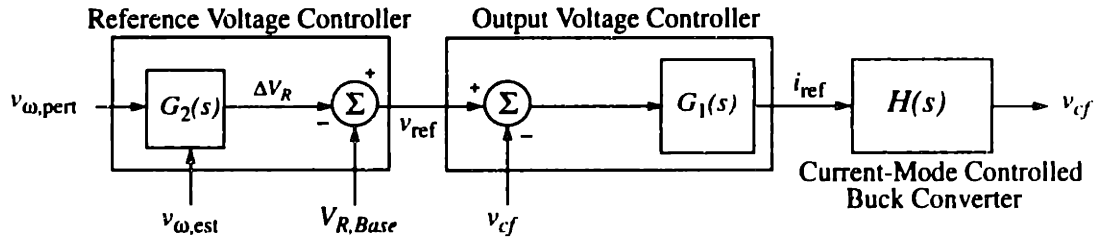


Figure 2.14: Block diagram of injected perturbation control methodology.

value. In the sections that follow, we discuss the basic design of a controller used in the closed-loop operation of the paralleled cells to achieve output voltage control and load balance.

2.5.1 Voltage Loop Controller

To regulate the output voltage to a constant value, we employed a current-mode control scheme. The error between the output voltage and a reference voltage is the input to the output voltage controller, which sets the current reference for the inner current control loop. In this control mode, the buck converter's regulated output voltage becomes fairly insensitive to input voltage variations [25].

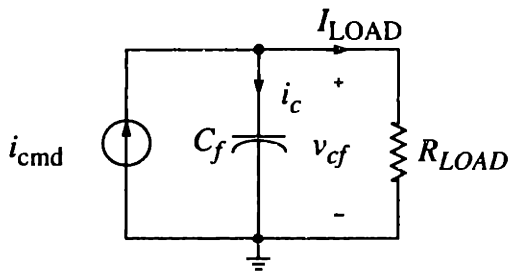


Figure 2.15: Dynamic model approximation of the buck converter in current-mode control where $i_{cmd} = i_{ref} + i_{pert}$.

Since the average inductor current is relatively large compared to the magnitude of the injected perturbation (maximum $|i_{pert}|$ ~ 1% of peak cell current) and switching ripple, the cell output current remains relatively constant over the switching period. Therefore, the converter with its inner current loop can be replaced in the model by a constant current source approximately equal to the command current signal of the converter cell. This model of the current-mode controlled buck converter also follows from a detailed analysis presented in [26] for continuous mode operation. Furthermore, since the switching ripple magnitude is low and the duty ratio in this system remains well below 0.5, no slope compensation is used in the system. The resulting dynamic model is shown in Fig. 2.15, where the total commanded current is the sum of the reference current (from the voltage-loop controller), and a perturbation used by the current-balance control system.

The result of the reference current to output voltage transfer function for the given parameters is:

$$H(s) = \frac{v_{cf}}{i_{cmd}} \cong \frac{R_x}{1 + sR_xC_f}. \qquad (2.9)$$

The voltage loop controller [$G_I(s)$] was designed using a proportional (P) controller, Fig. 2.16. For the P controller shown in Fig. 2.16:

$$R_3 = 1\ \text{k}\Omega,\ R_4 = 25\ \text{k}\Omega$$
$$V_X = v_{cf}$$
$$V_Y = v_{\text{ref}}$$
$$V_Z = i_{\text{ref}}.$$

The proportional controller output varies i_{ref} proportionally to the difference between v_{cf} and v_{ref}. The low pass filter at the output is used to limit the bandwidth of the controller. This controller was chosen due to its simplicity. It yields acceptable control dynamics

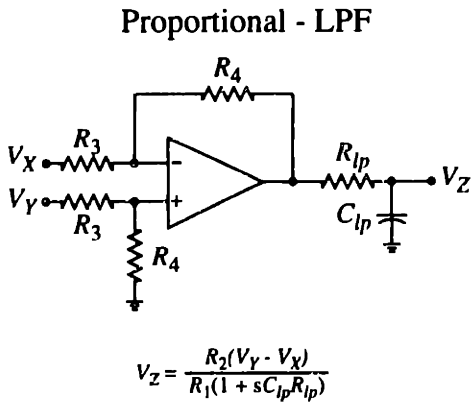


Figure 2.16: Schematic representation of output voltage controller, $G_1(s)$ of Fig. 2.14.

over the entire load range, at the expense of a small steady state error.

2.5.2 Current-Balancing Loop

Section 2.4 discussed the inner current loop which regulates the inductor current. Section 2.5.1 described the voltage loop control circuitry which regulates the output voltage by controlling the reference current. Now we look at an even slower control loop which implements current balancing by adjusting the local reference voltages whenever load imbalances are detected.

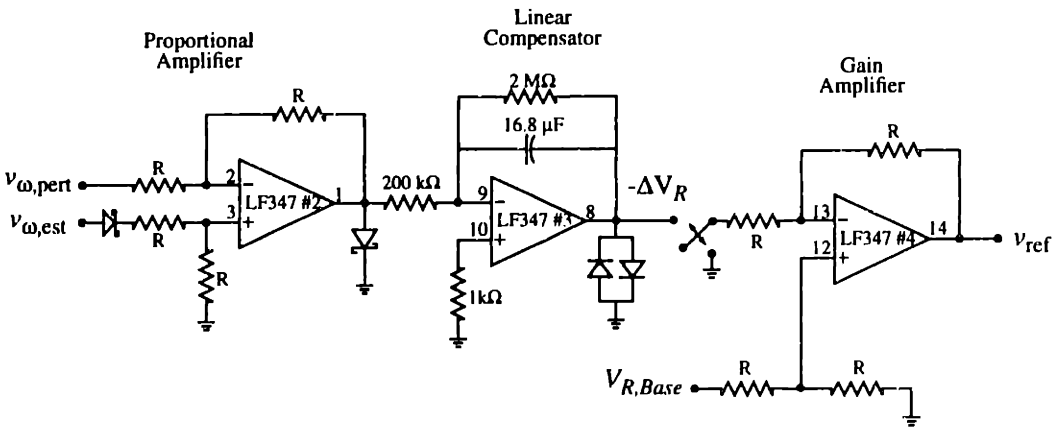
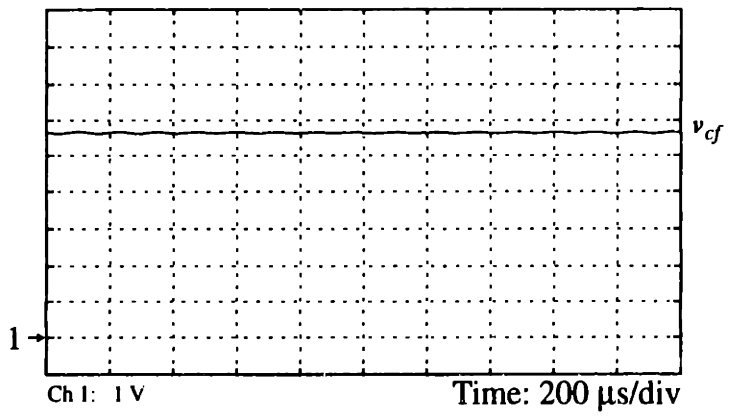


Figure 2.17: Functional schematic of the reference voltage controller, $G_2(s)$ used to adjust v_{ref} to achieve current-balance among converter cells.

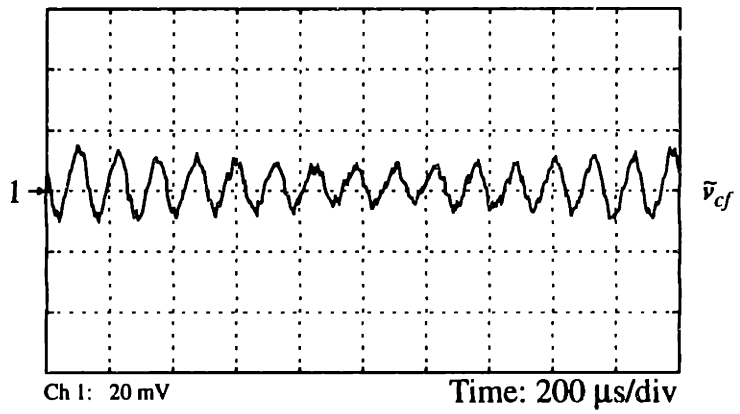
Figure 2.17 illustrates the controller used to regulate the local cell reference voltage using the difference between the perturbation and estimated rms frequency. The controller operates as an integrator, but with a finite low-frequency gain. The output of this compensator, ΔV_R, is added to a constant base reference voltage $V_{R,Base}$ to yield the total reference voltage v_{ref}. There is a switch between the linear compensator and the gain amplifier which allow the cells to operate with or without current-sharing control (i.e. without current-sharing control, the switch is connected to ground).

The operation of this current-balance controller can be understood as follows. If the cell perturbation frequency (and output current) is low compared to the rms frequency estimate, the linear compensator will decrease ΔV_R, which in turn increases the total reference voltage. As v_{ref} is increased, $G_1(s)$ will increase i_{ref} so that the local cell output current is increased. During this time, the currents from all the cells will converge towards a single value. At this point, an equilibrium state will be reached, and v_{ref} will not increase any further.

The converse is true for the situation when the cell perturbation frequency is high compared to the rms frequency estimate. For this case, the total reference voltage is decreased, which drives i_{ref} via $G_1(s)$, to a lower value so that current sharing is achieved among the cells. Eventually, the controllers will regulate the system in such a way that all the output currents (and perturbation frequencies) are close to a single value, and the output voltage is regulated to a fixed value. Figure 2.18(a) shows the output voltage of a three cell system under closed-loop operation, along with the voltage perturbations used to achieve current sharing, Fig. 2.18(b).



(a)



(b)

Figure 2.18: Prototype cellular converter system: (a) output bus voltage; and (b) voltage perturbations.

Chapter 3

Cellular Converter Testing

Functional testing of a prototype cellular converter system was conducted using the proposed design and control scheme for the injected perturbation method.

3.1 Cellular Converter System Setup

The prototype converter system was constructed using three converter cells connected in parallel, along with a load circuit card, assembled in a 19" rack as shown in Fig. 3.1.

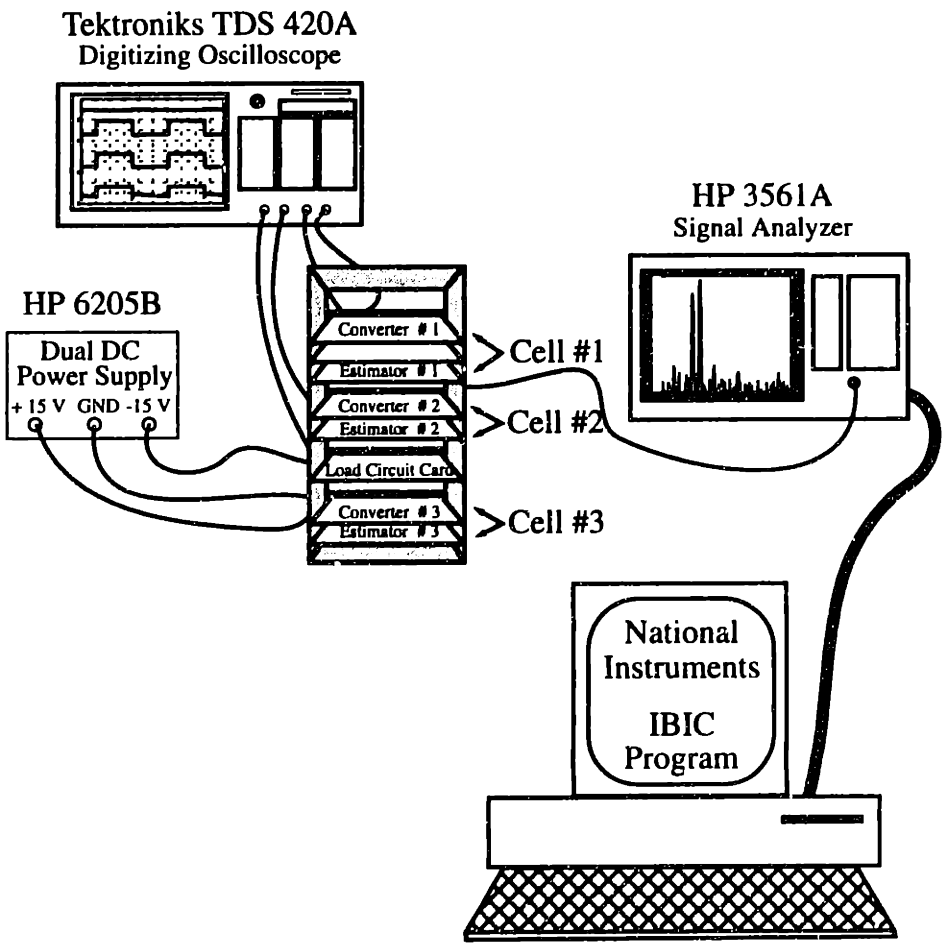


Figure 3.1: Prototype cellular power converter system.

The cells were comprised of a frequency estimator, current-mode controlled converter, and current-sharing controller whose detailed schematics are shown in Figs. B.1 - B.6 of Appendix B. The filter capacitor and an electronically controllable load resistor bank were built on a separate card. This section describes the equipment used in conducting tests to verify system functionality and performance. Section 3.2 discusses the methods and presents the results of the static load-sharing test used to observe the current-sharing capability of the converter cells in steady state operation. We also discuss the dynamic tests which were performed to determine the transient response of the cells for various load steps. Finally, we present the results of the dynamic range tests in Subsection 3.2.3.

3.1.1 Test Equipment

The following describes the various equipment used in testing the prototype cellular system. The system was powered with ±15 V from a HP6205B dual dc power supply. The converter cell input voltage was +15 V; both +15 V and -15 V were used to power the integrated circuits used in each cell. An HP3561A signal analyzer was used to observe the frequency content of the output bus voltage during the operation of the system. National Instruments' Interface Bus Interactive Control (IBIC) program was used to capture data from the spectrum analyzer. The Tektroniks TDS 420A oscilloscope was used to measure the transient responses of the cells.

3.2 Testing the Prototype Cellular System

Converter cells used to construct high power converter systems can be rated for extremely high voltages and currents. In our prototype system, we employ low-power converter cells which are designed to deliver a maximum of 25 mA to a fixed output voltage. Figure 3.2 illustrates waveforms measured while testing the functionality of one converter cell. Testing was done by powering up one converter cell whose voltage and

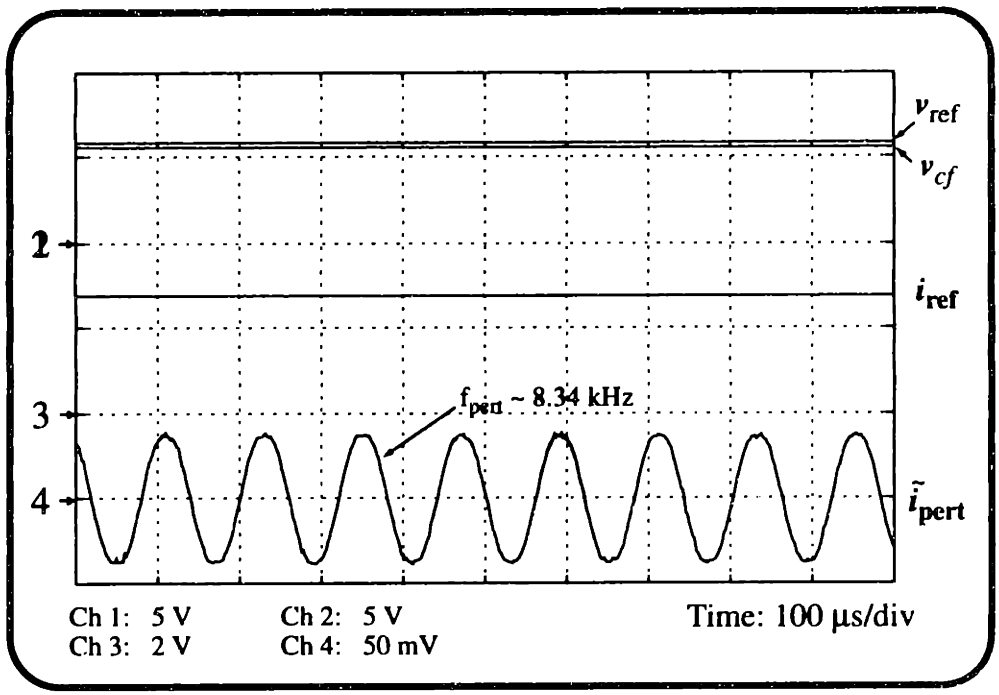


Figure 3.2: Waveforms for converter cell #2 in closed-loop operation.

current- sharing feedback loops were closed. Figure 3.2 reflects measurements taken from one cell with R_{Load} = 301 Ω. For one cell in closed loop operation, the current reference signal should be controlled so that the output voltage is regulated to a reference value of roughly 5.7 V (the value of this voltage can be adjusted by modifying $V_{R,Base}$ of the reference voltage controller). The measurements above show that the controller does regulate the output voltage to approximately 5.7 V and the corresponding reference current signal needed to maintain this output voltage level was i_{ref} ~ 14.2 mA (2.84 V). The perturbation magnitude and frequency were measured as 0.195 mA (39 mV_{pk}) and 8.3 kHz, respectively. Figure 3.3 displays the measurement of the frequency content of the output voltage, v_{cf}, for this cell. Although all the cells are of identical design, component variations exist which make their characteristics differ by small amounts. Table 3.1 lists the results of this test on each of the cells. The converter cells exhibit similar, but not identical, behavior in closed loop operation as can be seen from the values

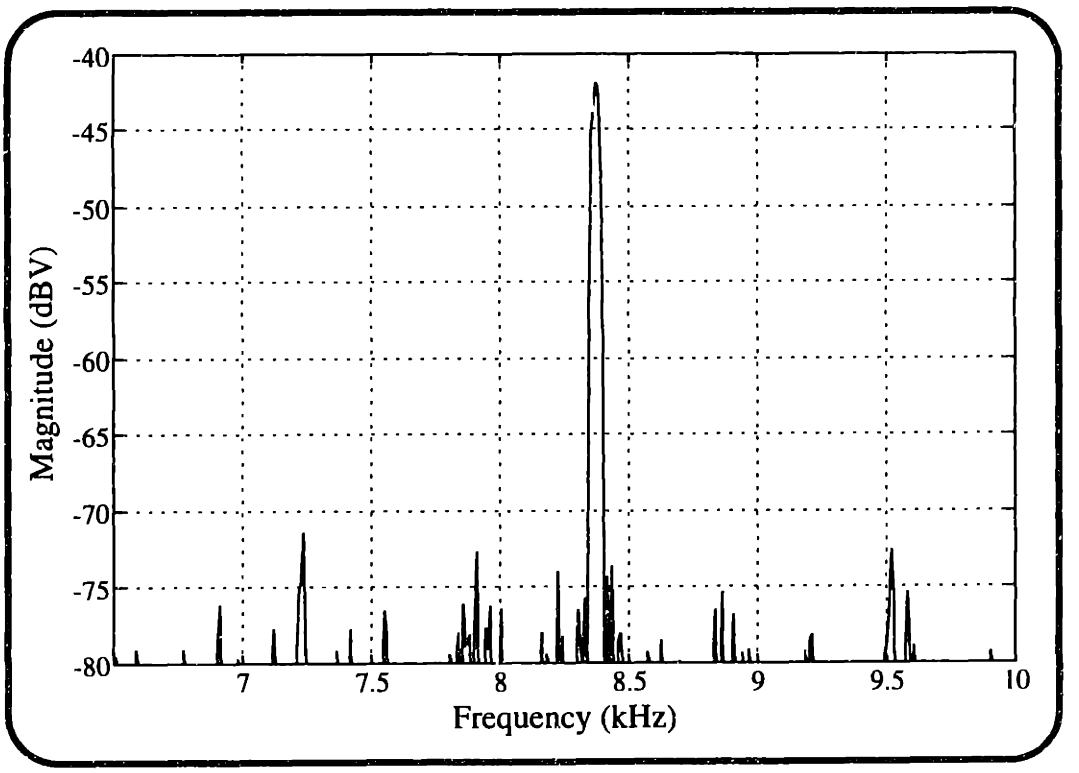


Figure 3.3: Spectrum analyzer plot showing frequency content of output signal for one converter operating in closed loop control.

listed in the table. Their deviation from one another is due to component variations which we did not adjust for. The differences in the reference voltages are primarily due to the amount of adjustment range left for the current-balancing loop and it is possible to regulate these more closely if desired. For this scheme, the converter cells do not have to be identical, as the current-balancing controller will force the cells to share the load current.

The results of all previous testing shows that the converter cells exhibit similar behavior for each of the tests performed. Our main interest is in the performance of the current-balance controllers and how accurately they adjust the local i_{ref} to achieve load balance among the cells. Therefore, the waveforms of all subsequent static and dynamic

tests will reflect measurements of the reference current signals of the local cells. Now we connect the cells in parallel and observe how they behave as a system.

Table 3.1: Measurement results from closed loop operation of individual converter cells.

Converter	v_{cf}	$V_{R,Base}$	i_{ref}	i_{pert}	f_{pert}
#1	4.68 V	4.86 V	2.1 V	43 mV	7.2 kHz
#2	5.7 V	6.0 V	2.84 V	39 mV	8.34 kHz
#3	5.72 V	5.96 V	2.82 V	39 mV	8.14 kHz

3.2.1 Parallel Operation Without Current-Balancing Control

The difference between cell reference currents, or the current-sharing error, can be used as a metric to determine how well the converter cells share current. Without current-sharing control, some degree of load balance exists due to the finite output impedance of the current-mode converter cells under proportional control, Fig. 3.4. For example, at 50% load, (Fig. 3.4), i_{ref3} is approximately 3.03 mA below the average cell current of 3.93

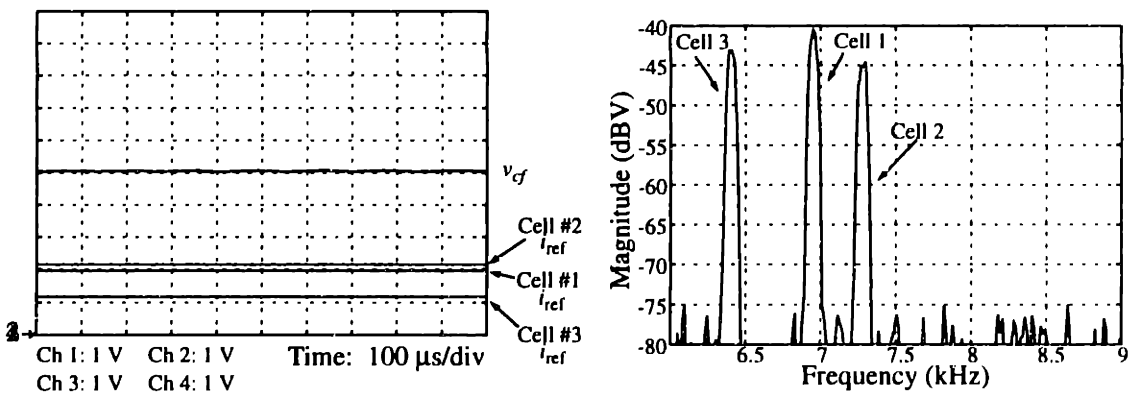
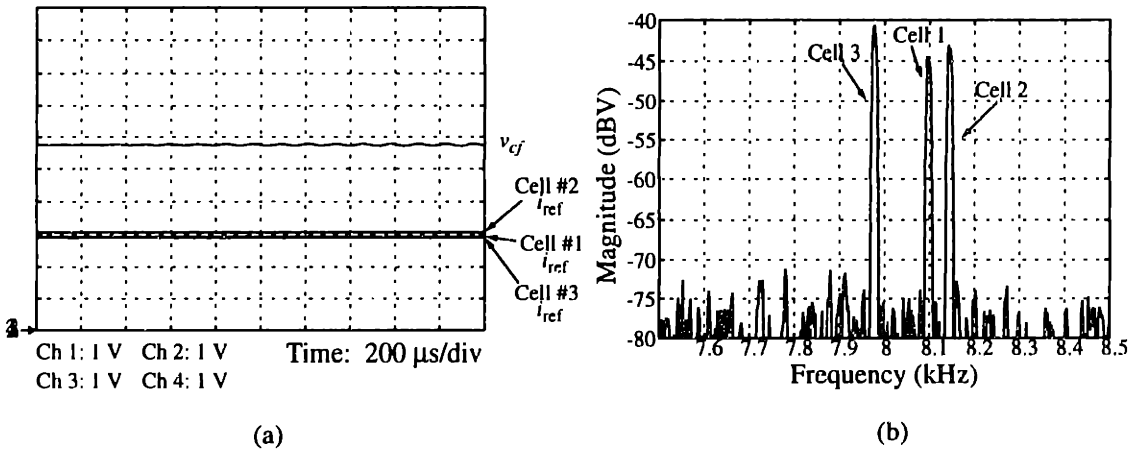


Figure 3.4: Paralleled converter cells without current-balance control at 50% load: (a) Cell reference currents and system output voltage measured from same reference, and (b) the corresponding perturbation signal frequency injected by each converter cell onto output bus.



(a) (b)

Figure 3.5: Paralleled converter cells with current-balance control. Same measurements taken as shown in Fig. 3.4.

mA, yielding a 34% current sharing error. However, for the same load, with current-balancing control, the cells share the load current with less than 3% error, Fig. 3.5. It should be noted that the frequency-based approach will yield accurate current sharing regardless of how the cells share current without current-balance control.

3.2.2 Static Current-Sharing Test

After testing the converter cells in parallel without current-balance control, we observed how the cells shared current, with control, over a wide range of loads. The static current-sharing test was performed by varying the load current over a relatively wide range (5% to 95% rated load current) and observing how the converter cells shared the load current over this range. Figure 3.6 shows a plot of the cell reference currents versus the total converter output current. Here we see that cell #1 and #2 share current more closely to one another than does cell #3 for lighter loads. This is due to the accuracy of the estimators (±4 to 5%) and the perturbation generators. The rms frequency estimators had an absolute accuracy of about ±5% (or ±250Hz) over the 5 - 10 kHz perturbation frequency range. It should be noted that the estimator's absolute accuracy tended to be

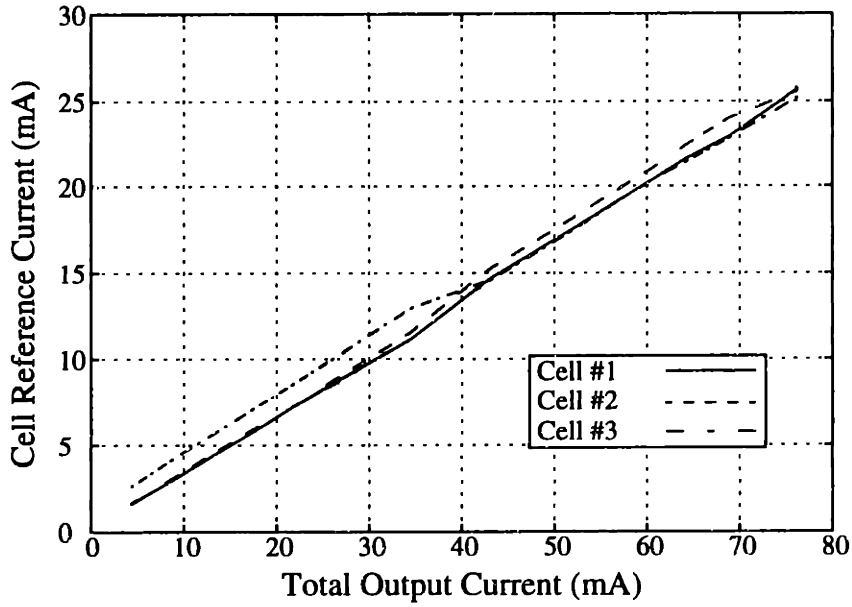


Figure 3.6: Converter cell reference current versus total output current illustrating static current-sharing capability of paralleled cells.

better for frequencies above 8 kHz, than at lower frequencies. This may have introduced some current sharing error at lighter loads. The absolute accuracy corresponds to a maximum absolute current error of 1.25 mA over the full load range. Therefore, at lighter load values, the percent error will tend to be higher for this maximum absolute error because the cell currents are considerably smaller. For heavier loads (or higher cell currents), this maximum absolute error (1.25 mA) has little effect on the overall current sharing error.

It is desirable for the converter cells to equally share the load current even at extremely light loads; however, current sharing at these load levels is not as important as at heavier loads because the cells are under considerably lower amounts of stress. It can be inferred from Fig. 3.6, that more accurate estimators and better tuned perturbation generators could likely render very accurate current-sharing results even at extremely light loads. In obtaining data to shown the cells' static current-sharing ability, we also acquired data which shows how well the output voltage is regulated over the same range of load values.

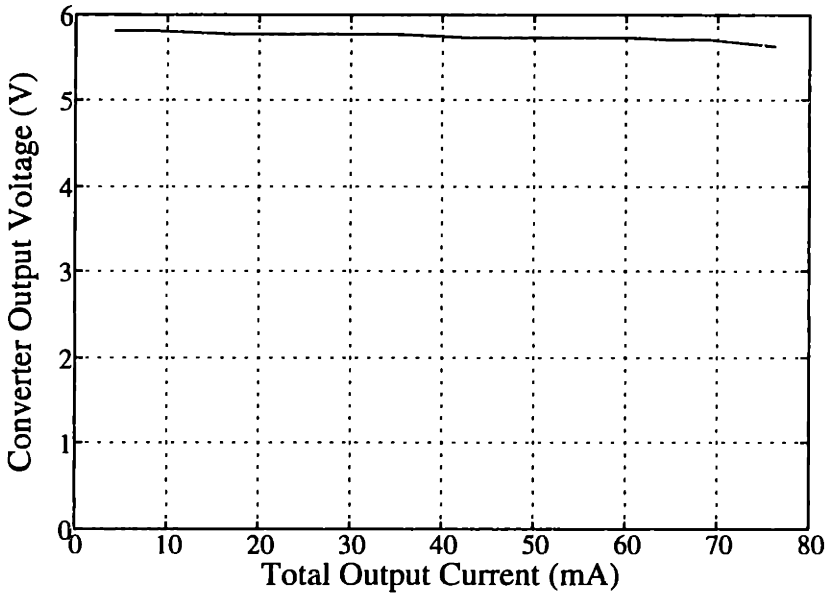


Figure 3.7: Load regulation curve of prototype cellular system output voltage.

Figure 3.7 illustrates a load regulation plot taken from collected data. We see that the output voltage is regulated to well within 5% for a load current up to approximately 76 mA, implying that each cell can carry a little more than its maximum rated current. The heavy regulation appearance of Fig. 3.7 beyond this current value is due to the fact that each cell's reference current is clamped by a Zener diode, to limit its maximum value. We select 5%, 50%, and 95% of this maximum rated load current (76 mA) as our very light, nominal, and heavy load operating points, respectively. The corresponding load resistance needed to obtain these points are roughly 1.33 kΩ, 133 Ω, and 71 Ω, respectively. Table 3.3 lists the data corresponding to the operating point for R_{Load} = 71 Ω and shows the related cell reference currents.

In this table, the values for the reference current (in mA) are inferred from the voltage measurements of the reference current signals of the converter cells. We can infer from this table that the cells share the load current to within ±0.2 % of the average cell current.

Table 3.2: Load sharing data @ 95% Load: $v_{cf} = 5.4$ V, $R_{Load} = 71\ \Omega$

Converter	$V\{i_{ref}\}$(V)	i_{ref} (mA)
Cell #1	5.16 V	25.13 mA
Cell #2	5.12 V	25.10 mA
Cell #3	5.04 V	25.03 mA

From Section 2.3, with a base perturbation frequency of 5 kHz, we show the frequency to voltage relationship between ω_{pert} and i_{ref} to be 1 kHz/V. Figure 3.8 shows a spectrum analyzer plot displaying the frequency content of the output voltage under heavy load conditions. Here we see three distinct frequencies which represent the different perturbation frequencies generated by the converter cells. The following lists and displays a similar table and plot of the prototype system operating under light load (Table 3.3 and Fig. 3.9) conditions. The measured reference current signals and the spectrum analyzer plot for the nominal case were presented in Subsection 3.2.1.

The results of the static current sharing tests illustrate that the converter cells do indeed share current to within ±10 % of the average cell current over a wide load range.

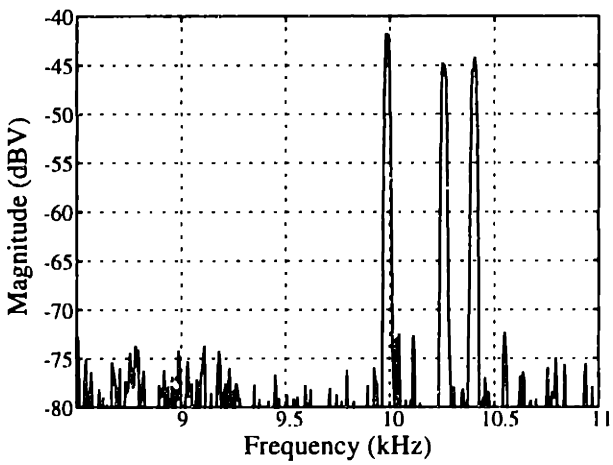


Figure 3.8: Spectrum analyzer plot showing the distinct perturbation frequencies generated by each cell for system operating under heavy load conditions.

Table 3.3: Load sharing data @ 5% Load: v_{cf} = 5.82 V, R_{Load} = 1.33 kΩ

Converter	$V\{i_{ref}\}$ (V)	i_{ref} (mA)
Cell #1	0.316 V	1.58 mA
Cell #2	0.328 V	1.64 mA
Cell #3	0.52 V	2.6 mA

Thus current-sharing performance is much better with the load-balance controller than without as was seen in Subsection 3.2.1.

3.2.3 Dynamic Load Step Test

In Subsection 3.2.2, tests were conducted to prove that the converter cells shared the load current in a static manner. However, to demonstrate the stability of the control system for such occurrences as instantaneous load variations, dynamic testing must be done. The manner in which we chose to perform this test was to change the load resistance by connecting and disconnecting an additional resistor. Figure 3.10 shows a schematic of the load circuit used in performing this test. The resistance R_{fix} represents the value necessary for the cells to operate at the minimum test current level, while R_{eq} is the equivalent

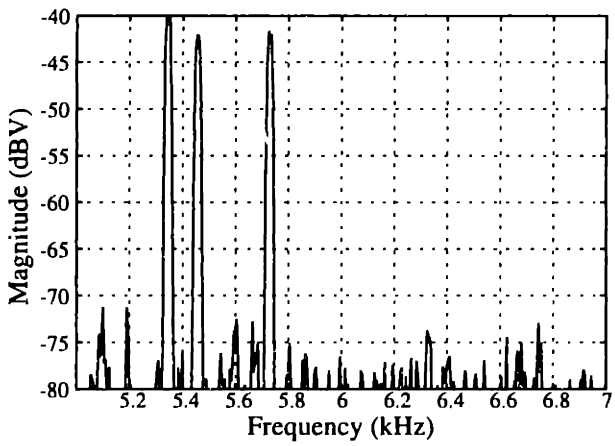


Figure 3.9: Spectrum analyzer plot of prototype system output voltage at very light load: v_{cf} = 5.82 V, R_{Load} = 1.33 kΩ

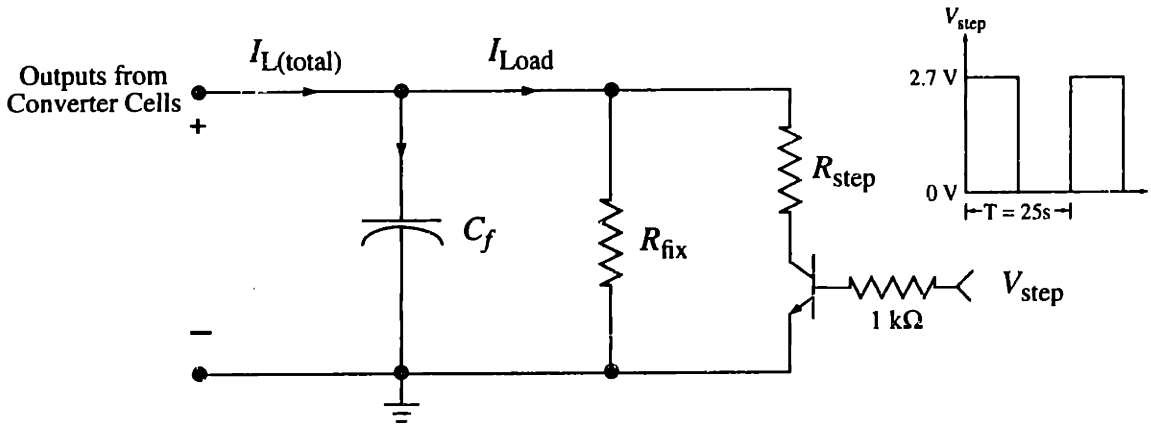


Figure 3.10: Schematic representation of the dynamic load step resistance test.

resistance needed to obtain the maximum test current level.

The resistance R_{eq} was computed for the case when the output voltage is regulated to 5 V:

$$R_{eq} = \frac{5V}{I_{max}}. \qquad (3.1)$$

The resistance R_{step} is a variable resistor whose value is used to reduce the load resistance to R_{eq} so that the load current is increase to I_{max} for the given test:

$$R_{step} = \frac{R_{fix} \cdot R_{eq}}{(R_{fix} - R_{eq})}. \qquad (3.2)$$

Table 3.4: Load step test parameters for determining system dynamic characteristics.

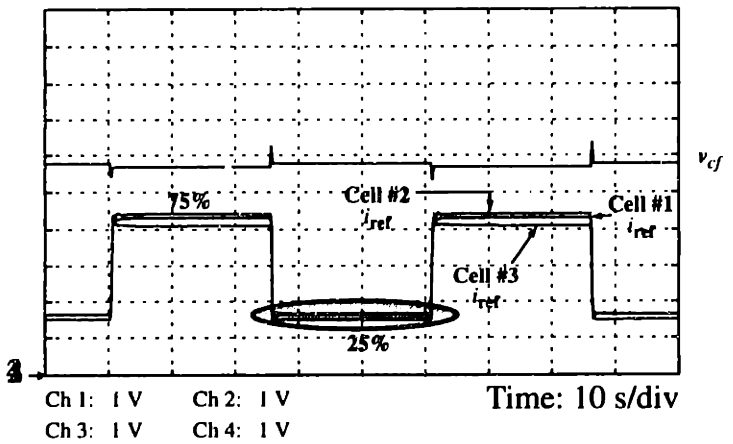
Test	I_{min}	I_{max}	R_{fix}	R_{step}	R_{eq}
25% to 75%	18.75 mA	56.25 mA	261 Ω	134 Ω	88.89 Ω
10% to 90%	7.5 mA	67.5 mA	681 Ω	83 Ω	74.07 Ω

Table 3.4 lists the test parameters used to observe the transient response of the system and cells. The following results reflect the transient responses of the prototype cellular system

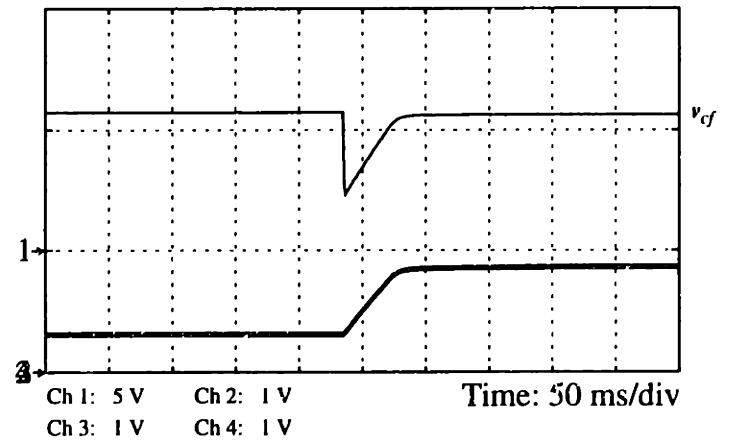
for changes in the load current as outlined in Table 3.4. Shown is an oscilloscope measurement of the cells' reference current waveforms as the load step test was performed. Since the output current tracks the reference current signal very accurately, we can measure the cell reference signals to get an indication of the cell output current behavior as well as the transient behavior of the control variable during the load step.

Depending on the converter system used in a particular application and on the application itself, appreciable load steps can occur. To demonstrate that a cellular converter system can regulate the output bus voltage for wide load fluctuations, we chose to use the case were we test the prototype system with a 25% to 75% load step. Shown in Fig. 3.11 are the results of the 25% to 75% load step test. Here we can see that the controllers do not exhibit oscillatory behavior as the cells undergo the load test, but instead display good damping so that current sharing is achieved, Fig. 3.11(a).

We use this case also to show that the voltage loop discussed in Section 2.5 is much faster than the current sharing loop by orders of magnitude. Here, the voltage loops settle to their final value within approximately 30 ms as can be seen in Figs. 3.11(b),(c). The current sharing loops are much slower (12 - 15 s), Fig. 3.11(a). Also, in Fig. 3.11(a) the system output voltage appears to remain fairly constant during the load steps; however, Figs. 3.11 (b),(c) show that during the transients, the output bus voltage does increase and decrease for a period on the order of the settling time of the voltage control loop. Figure 3.12 shows the same waveforms illustrated in the shaded region of Fig. 3.11(a) displayed from the same measurement reference point to observe more closely the current sharing dynamics for the 25% to 75% load step test. We see in Fig. 3.11(a) that the converter cells share the load current to within a few percent of the average at 75% load. When the load is stepped to 25%, the reference current signals overshoot by a small amount and the current-balancing controller works to stabilize the cells' output current towards a single



(a)



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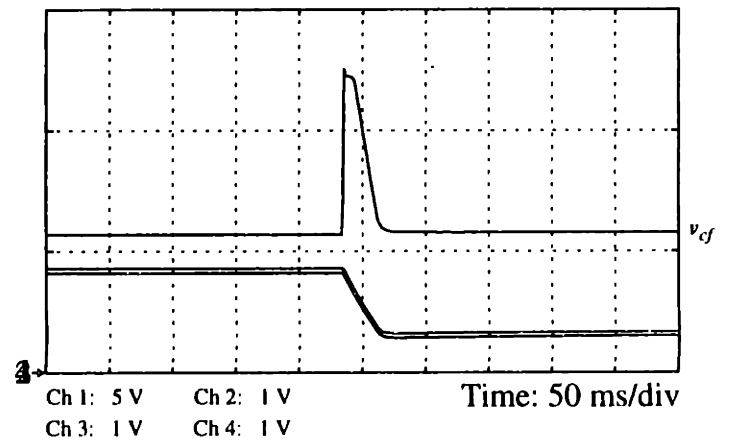


(c)

Figure 3.11: 25% to 75% dynamic load step test showing: (a) the current sharing responses of the converter cells; (b) the transient response of the voltage loop for a 25% to 75% load step; and (c) the transient response of the voltage loop for a 75% to 25% load step. Note that the current-sharing response is on a much slower time scale than the voltage responses.

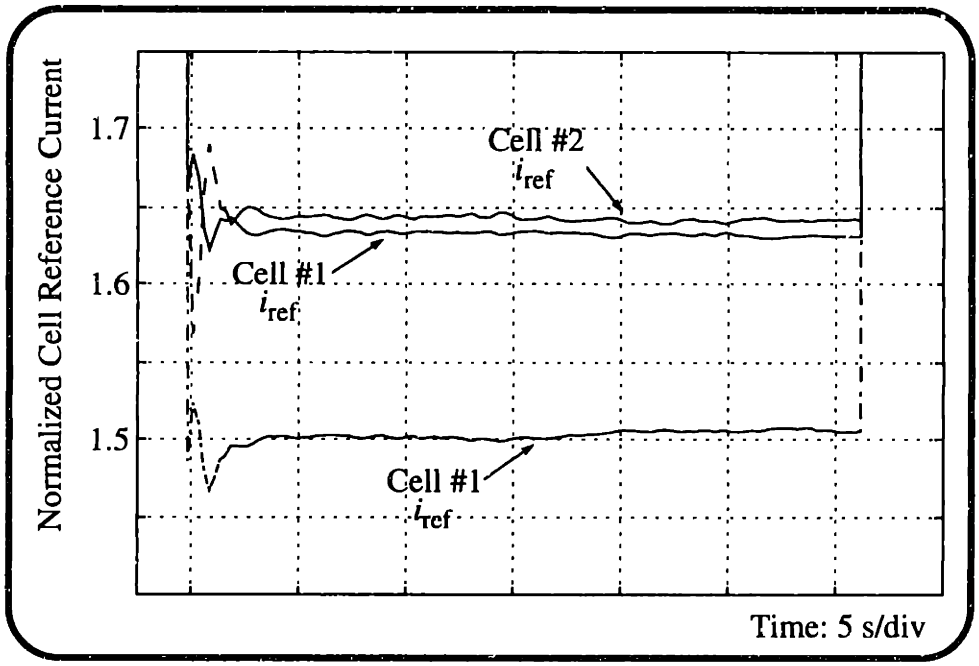


Figure 3.12: Expanded view of shaded region in Fig. 3.11(a) showing transient behavior of the current-sharing controller for 75% to 25% load step.

value. Figure 3.12 shows that after the initial transient overshoot, the converter cells are controlled so that load balance is achieved.

Figure 3.13 shows a spectrum analyzer plot of the frequency content of the output bus voltage corresponding to the perturbation frequencies generated when the converter cells are operating at 25%, Fig. 3.13(a), and 75%, Fig. 3.13(b), of the total load current. This plot shows that each cell has injected current sharing information onto the output bus via its own perturbation generator, so that the other cells can use the aggregated current-sharing information to achieve load balance. In both cases, the proximity of the peaks imply that the converter cells are sharing current at both levels to within their designed value. We only illustrate this spectrum analyzer plot for the 25% to 75% load step test, but similar spectrum analyzer plots can be generated for the other load step tests as well.

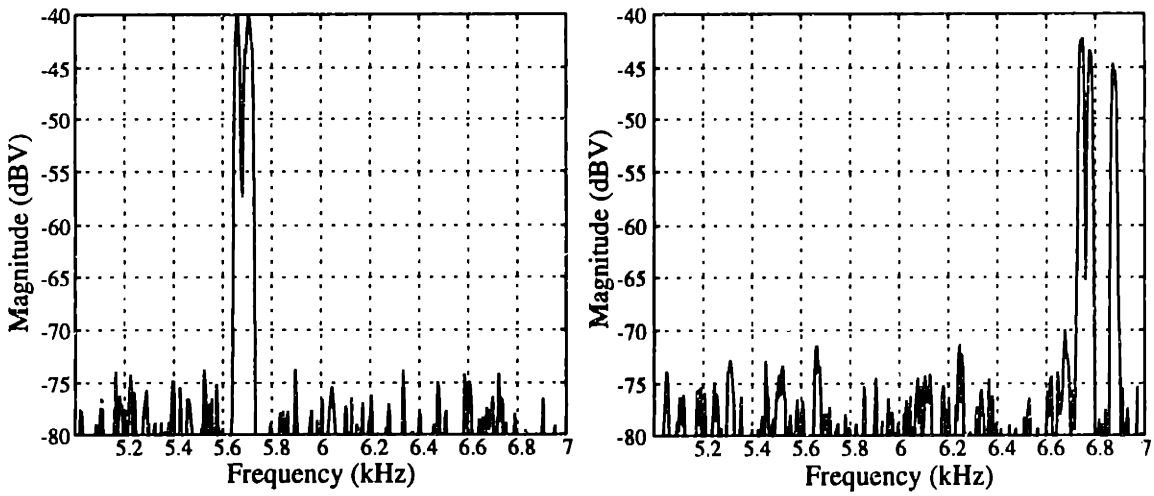


Figure 3.13: Spectrum analyzer plot of system output voltage at (a) 25% Load, and (b) 75% Load Current.

The final dynamic test performed to observe the transient behavior of the cells was a 10% to 90% load step test. This test was performed as an extreme case to determine whether or not the control system would remain stable in the presence of significantly large disturbances. Figure 3.14 shows the oscilloscope measurements taken during this test. We also notice that the load current starts to be distributed among the cell within a few seconds after the transition. Figure 3.15 references waveforms from a similar point as shown in Fig. 3.12, and focuses on the time period immediately after the 90% to 10% to the end of the cycle. It illustrates that the cells begin to take action almost immediately to distribute the load current equally among themselves when this large load imbalance occurs.

The test results illustrate that without a load-balance control, the current sharing error among the paralleled converter cells is substantial. Static load sharing test results show that with current-balancing control our converter cells do share current to within $\pm 10\%$ over a wide range of load values. Further testing of the performance of our prototype

system demonstrates that acceptable system dynamics are obtained even for large load changes.

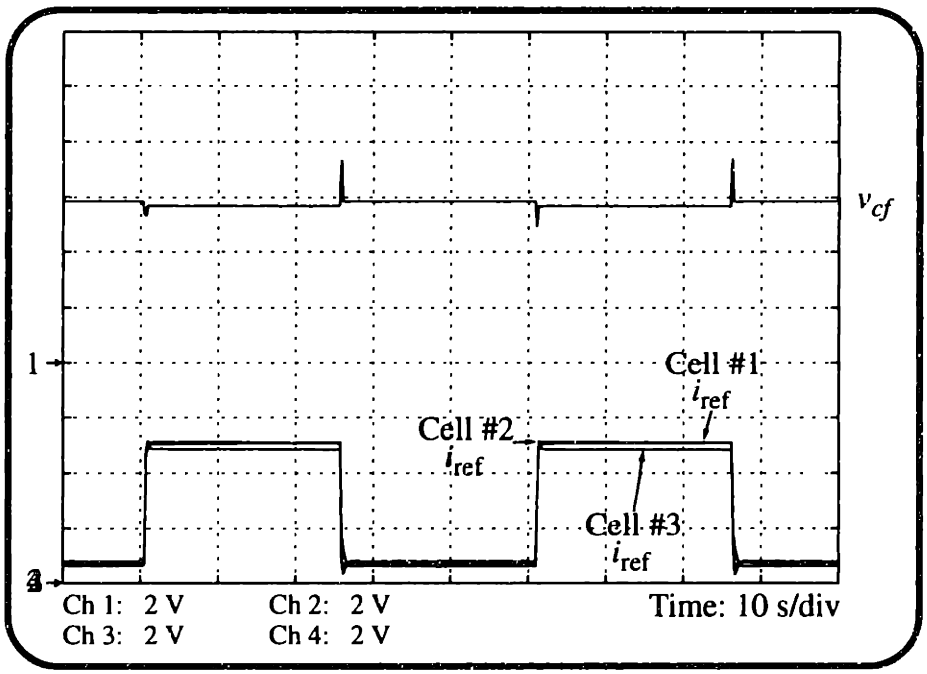


Figure 3.14: Current sharing dynamics: 10% to 90% load step test.

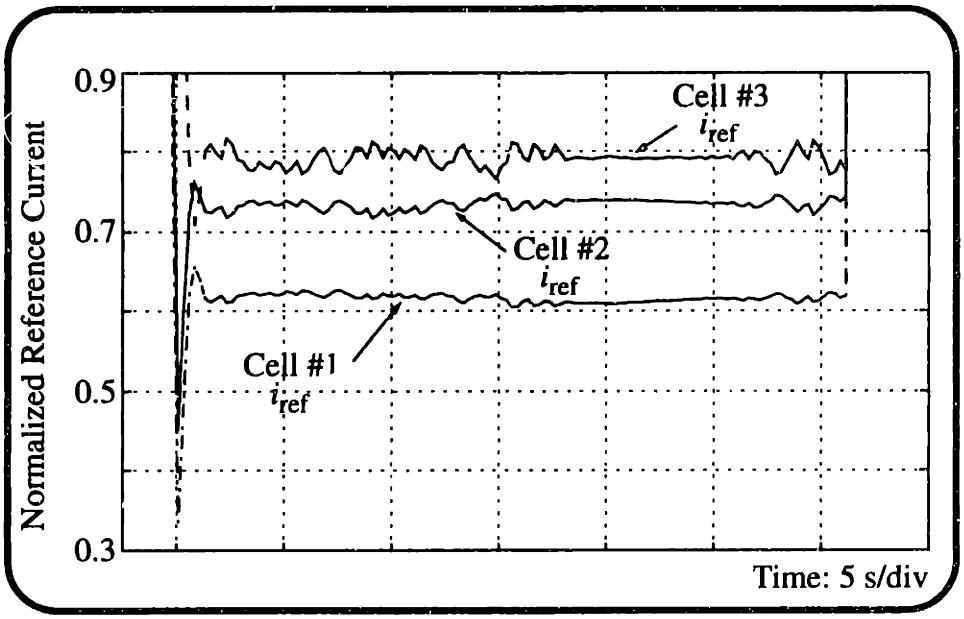


Figure 3.15: Current sharing dynamics: 10% to 90% load step test illustrating the cells taking action when a large load imbalance is introduced during the 90% to 10% load step transition.

Chapter 4

Cell Switching Frequency Ripple Method

In Chapter 2, we discussed the implementation of a current-balancing technique in which the cells encode information about their output current onto the system bus voltage using small perturbations. We now turn our attention to an alternate method which works similarly, but uses the switching frequency ripple of the converter cell as the perturbation source.

4.1 Cell Switching Ripple Method

Fig. 4.1 illustrates a current-sharing approach in which the switching frequency ripple is used to encode current-sharing information in the output bus. In order to implement this method, there must be a relationship between the converter switching frequency and the cell output current (or some other load-sharing variable). To investigate this approach, we exploit the natural relationship between cell output current and switching frequency of a buck converter operating in *edge of discontinuous conduction mode* (EDM). A detailed analysis of the buck converter in EDM operation is given in Appendix A.1.

In the EDM converter, the switching frequency is inversely related to the average output current. Thus, information about the output current of the cells is contained in the aggregate output current (and voltage) ripple, and can be used to estimate the rms output current of the individual cells. As discussed in Section 2.5, it is possible to design a distributed load sharing controller which uses this information to achieve load balance. Section 4.2 presents a technique by which the rms cell output current can be estimated from the output voltage ripple due to the aggregated switching harmonics. We then

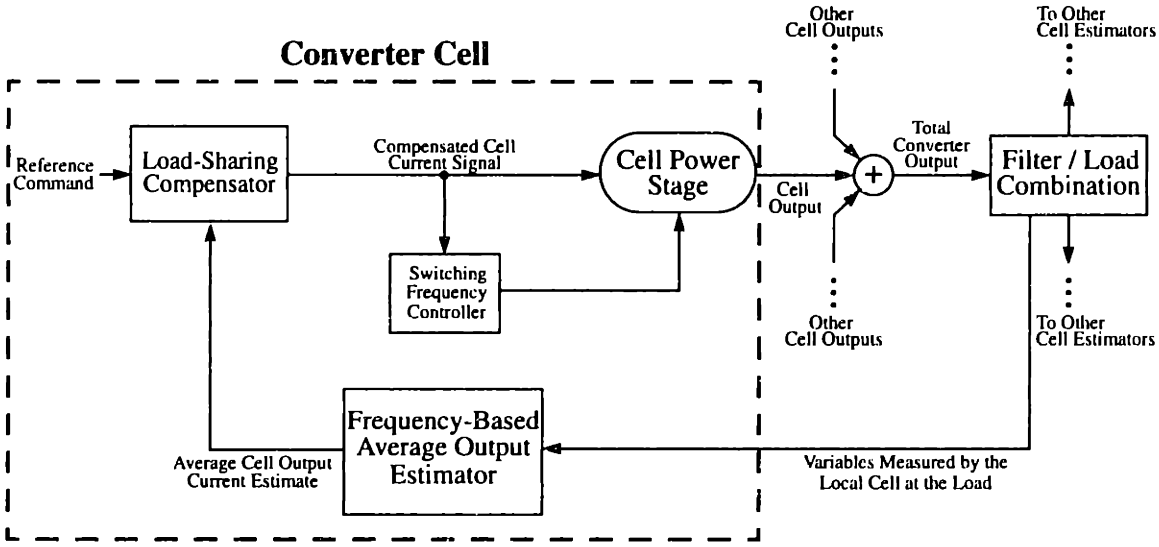


Figure 4.1: Block diagram of current sharing approach for cellular architecture which uses the cell's switching frequency to encode load balance information.

describe a low-power implementation of an EDM converter and current estimator. Limitations of the implemented approach are described, followed by a section which describes possible methods for overcoming these limitations.

4.2 EDM Converter and RMS Current Estimator

The output current of an EDM cell is related to its switching frequency. Since the switching frequency information of the individual cells appear on the aggregate output voltage, an rms cell current estimate is computable from the output voltage ripple. We now present a technique in which the rms cell output current of paralleled EDM converter cells can be estimated from the aggregated switching harmonics in the output voltage. This is accomplished using the estimator structure shown in Fig. 4.2.

The rms cell output current for a set of N paralleled cells is:

$$i_{rms}(t) = \sqrt{\frac{\sum_{k=1}^{N} i^2_{ref,k}}{N}} \qquad (4.1)$$

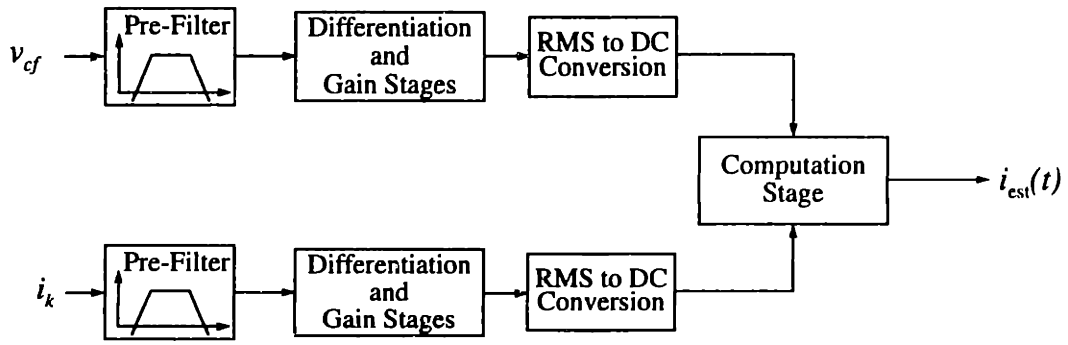


Figure 4.2: Block diagram of the estimator used to compute the rms output current of the aggregated output signal.

where $i_{ref,k}$ is the reference current (or equivalently, the output current) of the kth cell.

To describe the manner in which we obtain an estimate of the rms output current, we begin by elucidating the relationship between the average output current, total output current, and the voltage harmonics of an EDM cell. This information can then be used in the design of the estimator. From Fig. A.2 in Appendix A, for a fixed reference current, the inductor current is periodic, with period T_s, and can be represented as a Fourier series by:

$$i_L(t) = \sum_{n=-\infty}^{\infty} C_n e^{jn\omega_o t} \tag{4.2}$$

where

$$\omega_o = \frac{2\pi}{T_s} = \frac{\pi v_{CF}(V_{in} - v_{CF})}{V_{in} L i_{ref}}$$

and the complex coefficients C_n are given by:

$$C_n = \frac{1}{T}\int_0^T i_L(t)\, e^{-jn\omega_o t}. \tag{4.3}$$

The output current spectrum of the kth converter cell can be written as:

$$I_k(\omega) = 2\pi \sum_{n=-\infty}^{\infty} C_{n,k}\,\delta(\omega - n\omega_k) \tag{4.4}$$

where $\omega_k = \dfrac{\pi v_{CF}(V_{in} - v_{CF})}{V_{in} L i_{ref,k}}$.

C_n is computed in Appendix A.2 and the result for the k[th] cell, taken from *(A.11)*, is:

$$C_{n,k} = \frac{m_2}{2\pi n^2 \omega_k}\left(1 - e^{jn\omega_k \Delta t_2}\right) - \frac{m_2 \Delta t_2}{j2\pi n} e^{jn\omega_k \Delta t_2} + \frac{m_1}{2\pi n^2 \omega_k}\left(e^{jn\omega_k \Delta t_1} - 1\right) - \frac{m_1 \Delta t_1}{j2\pi n} e^{jn\omega_k \Delta t_1}. \qquad (4.5)$$

It can be shown that the values $C_{n,k}$ are proportional to $i_{ref,k}$ through ω_k. This occurs because the shape of the output current waveform is invariant to the value of $i_{ref,k}$ as shown in Fig. 4.3.

The spectrum of the total output current for N cells is given by:

$$I_T(\omega) = I_1(\omega) + I_2(\omega) + \ldots + I_N(\omega)$$

$$I_T(\omega) = \sum_{k=1}^{N} 2\pi \sum_{n} C_{n,k} \delta(\omega - n\omega_k). \qquad (4.6)$$

If we consider a limited switching frequency range and *assume that the load is an open circuit for frequencies* over this range, the ripple components of the output voltage can be determined directly from the output current ripple. The ripple voltage $\tilde{v}_{cf}$ is comprised of

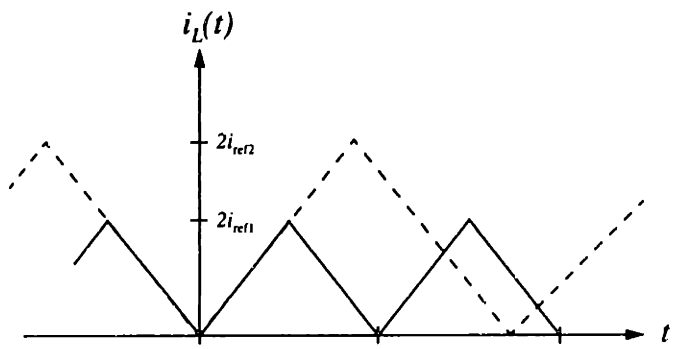


Figure 4.3: Shape of the output inductor current waveform, for EDM converters, showing invariance to the value of $i_{ref,k}$.

all harmonics excluding the component at $\omega = 0$. The ripple voltage spectrum produced by the k^{th} cell is:

$$\tilde{V}_{cf,k}(\omega) = \frac{1}{C_f}\frac{I_k(\omega)}{j\omega} = \frac{2\pi}{jC_f}\sum_{\left(\substack{n \\ n\neq 0}\right)}\frac{C_{n,k}}{n\omega_k}\delta(\omega - n\omega_k)\,. \tag{4.7}$$

Because $C_{n,k} \propto i_{\text{ref},k}$ and $\omega_k \propto \frac{1}{i_{\text{ref},k}}$, then $|\tilde{V}_{cf,k}| \propto i^2_{\text{ref},k}$. The total ripple voltage spectrum is the sum of the ripple voltages contributed by each converter cell at the output filter capacitor:

$$\tilde{V}_{cf,T}(\omega) = \tilde{V}_{cf,1}(\omega) + \tilde{V}_{cf,2}(\omega) + \ldots + \tilde{V}_{cf,N}(\omega)$$

$$\tilde{V}_{cf,T}(\omega) = \sum_{k=1}^{N}\frac{2\pi}{jC_f}\sum_{\left(\substack{n \\ n\neq 0}\right)}\frac{C_{n,k}}{n\omega_k}\delta(\omega - n\omega_k)\,. \tag{4.8}$$

where $\tilde{V}_{cf,T}(\omega)$ is the total output ripple voltage spectrum across C_f.

We can use this information along with Parseval's Theorem to obtain the desired estimate of the rms output current. Parseval's Theorem relates the total energy in time to the total energy in frequency for a given signal, *x(t)*.

$$\int_{-\infty}^{\infty} x^2(t)\,dt = \frac{1}{2\pi}\int_{-\infty}^{\infty}|X(\omega)|^2 d\omega. \tag{4.9}$$

Since the energy in the harmonic components of the ripple voltage for the k^{th} cell is proportional to $|\tilde{V}_{cf,k}(\omega_k)|^2$ and $|\tilde{V}_{cf,k}(\omega_k)| \propto i^2_{\text{ref},k}$, then the energy is proportional to $(i_{\text{ref},k})^4$. Likewise, in the current harmonics, or harmonics of the first derivative of the voltage (which is proportional to $\omega_k \cdot \tilde{V}_{cf,k}(\omega_k)$), the energy is proportional to $(i_{\text{ref},k})^2$. Furthermore, the energy in the harmonics of the second derivative of the voltage is independent of $i_{\text{ref},k}$. This means that the energy in the second derivative of a converter's output voltage harmonic spectrum will be a constant, K_E, regardless of its output current,

i.e.,

$$K_E = \int_{-\infty}^{\infty} \frac{d^2}{dt^2}(\tilde{v}_{cf,k}^2)\,dt = \frac{1}{2\pi}\int_{-\infty}^{\infty} \left|\omega_k \tilde{V}_{cf,k}(\omega)\right|^2 d\omega. \qquad (4.10)$$

So for N cells connected in the parallel structure, the total energy is $E_T = N \cdot K_E$ provided the cells are operating at different frequencies.

While it is beyond the scope of this thesis, it can be shown that similar results occur if the integration is approximated by a low pass filter [28]. Using a (causal) low pass filter yields a "local-time" calculation of these energies which may be employed in a feedback control circuit. The impulses in the spectrum for the previous case are replaced by finite pulses, and the total signal energies become finite. We can make these local-time computations using commercially available rms to dc converters as will be seen in the next section. From the results presented in [28], it can be shown that for the kth converter cell,

$$LPF\{[\tilde{i}_{L,k}(t)]^2\} \cong \sum_{\left(\substack{n \\ n\neq 0}\right)} C_{n,k}^2$$

$$LPF\{[\tilde{i}_{L,k}'(t)]^2\} \cong \omega_k^2 \sum_{\left(\substack{n \\ n\neq 0}\right)} [nC_{n,k}]^2$$

$$LPF\{[\tilde{v}_{cf,k}'(t)]^2\} \cong \frac{1}{C_f^2}\sum_{\left(\substack{n \\ n\neq 0}\right)} C_{n,k}^2$$

$$LPF\{[\tilde{v}_{cf,k}''(t)]^2\} \cong \frac{\omega_k^2}{C_f^2}\sum_{\left(\substack{n \\ n\neq 0}\right)} [nC_{n,k}]^2 \qquad (4.11)$$

We can use the same approach to write similar expressions for other desired quantities. Remembering that $C_{n,k} \propto i_{\text{ref},k}$ and $\omega_k \propto \frac{1}{i_{\text{ref},k}}$, we can define variables $\hat{C}_n$ and $\hat{\omega}$ to be independent of $i_{\text{ref,k}}$:

$$\hat{C}_n = \frac{C_{n,k}}{i_{\text{ref},k}}$$

and

$$\hat{\omega} = \omega_k \cdot i_{\text{ref},k}.$$

Note also that $\hat{C}_n$ and $\hat{\omega}$ are the same for each converter cell. This is possible because the shape of the inductor current waveform is invariant to the value of $i_{\text{ref},k}$ as shown in Fig. 4.3. Therefore, the relative magnitudes of the Fourier coefficients are also invariant to $i_{\text{ref},k}$, that is, they are independent of k. For a single converter cell this substitution yields:

$$LPF\{[\tilde{i}_{L,k}(t)]^2\} \cong i_{\text{ref},k}^2 \sum_{\binom{n}{n\neq 0}} \hat{C}_n^2$$

$$LPF\{[\tilde{i}_{L,k}'(t)]^2\} \cong \hat{\omega}^2 \sum_{\binom{n}{n\neq 0}} [n\hat{C}_n]^2$$

$$LPF\{[\tilde{v}_{cf,k}'(t)]^2\} \cong \frac{i_{\text{ref},k}^2}{C_f^2} \sum_{\binom{n}{n\neq 0}} \hat{C}_n^2$$

$$LPF\{[\tilde{v}_{cf,k}''(t)]^2\} \cong \frac{\hat{\omega}^2}{C_f^2} \sum_{\binom{n}{n\neq 0}} [n\hat{C}_n]^2. \qquad (4.12)$$

For N cells, the mean square of the first derivative of the total output voltage ripple can be written as:

$$LPF\{[\tilde{v}_{cf}'(t)]^2\} \cong \frac{1}{C_f^2} \cdot \sum_{\binom{n}{n\neq 0}} \hat{C}_n^2 \cdot \sum_{k=1}^{N} i_{\text{ref},k}^2 \qquad (4.13)$$

which is proportional to the sum of the squared cell currents. Similarly, the mean square of the second derivative of the total output voltage ripple is:

$$LPF\{[\tilde{v}_{cf}''(t)]^2\} \cong \sum_{k=1}^{N}\left(\frac{\hat{\omega}^2}{C_f^2}\sum_{\binom{n}{n\neq 0}}[n\hat{C}_n]^2\right) = N\cdot\left(\frac{\hat{\omega}^2}{C_f^2}\sum_{\binom{n}{n\neq 0}}[n\hat{C}_n]^2\right) \qquad (4.14)$$

which is proportional to the total number of cells in the system. Therefore, the ratio of *(4.13)* to *(4.14)* is proportional to the mean square cell current, namely

$$\frac{LPF\{[\tilde{v}_{cf}'(t)]^2\}}{LPF\{[\tilde{v}_{cf}''(t)]^2\}} = \left\{\frac{\frac{1}{C_f^2}\cdot\sum_{\binom{n}{n\neq 0}}\hat{C}_n^2}{\frac{\hat{\omega}^2}{C_f^2}\sum_{\binom{n}{n\neq 0}}[n\hat{C}_n]^2}\right\}\cdot\frac{\sum_{k=1}^{N} i_{\mathrm{ref},k}^2}{N}. \qquad (4.15)$$

Additionally, the factors from *(4.12)* for the cell output current ripple and its first derivative can be used to cancel the bracketed proportionality term generated in *(4.15)*. If we multiply the right side of *(4.15)* by the following factors, which equal 1, from *(4.12)*

$$1 = \frac{LPF\{[\tilde{i}_{L,k}(t)]^2\}}{i_{\mathrm{ref},k}^2\sum_{\binom{n}{n\neq 0}}\hat{C}_n^2}\cdot\frac{\hat{\omega}^2\sum_{\binom{n}{n\neq 0}}[n\hat{C}_n]^2}{LPF\{[\tilde{i}_{L,k}'(t)]^2\}} \qquad (4.16)$$

we get

$$\frac{LPF\{[\tilde{v}_{cf}'(t)]^2\}}{LPF\{[\tilde{v}_{cf}''(t)]^2\}} = \left\{\frac{\sum_{k=1}^{N} i_{\mathrm{ref},k}^2}{N}\right\}\cdot\frac{\frac{1}{C_f^2}\cdot\sum_{\binom{n}{n\neq 0}}\hat{C}_n^2}{\frac{\hat{\omega}^2}{C_f^2}\sum_{\binom{n}{n\neq 0}}[n\hat{C}_n]^2}\cdot\frac{LPF\{[\tilde{i}_{L,k}(t)]^2\}}{i_{\mathrm{ref},k}^2\sum_{\binom{n}{n\neq 0}}\hat{C}_n^2}\cdot\frac{\hat{\omega}^2\sum_{\binom{n}{n\neq 0}}[n\hat{C}_n]^2}{LPF\{[\tilde{i}_{L,k}'(t)]^2\}}. \qquad (4.17)$$

Solving *(4.17)* for the mean-square output current (the bracketed term) and taking the square root of both sides, we compute a local-time estimate of the root-mean-square cell output current:

$$i_{est}(t) = \frac{\left(\sqrt{LPF\{[K_3\tilde{i}_{L,k}'(t)]^2\}}\right)\cdot i^2_{ref,k}}{\left(\sqrt{LPF\{[\tilde{i}_{L,k}(t)]^2\}}\right)} \cdot \frac{\left(\sqrt{LPF\{[K_1\tilde{v}_{cf}'(t)]^2\}}\right)}{\left(\sqrt{LPF\{[K_1K_2\tilde{v}_{cf}''(t)]^2\}}\right)} \cong \sqrt{\frac{\sum_{k=1}^{N} i^2_{ref,k}}{N}}. \qquad (4.18)$$

The scale constants K_1, K_2, and K_3 are used to ensure that the intermediate signals remain in the range of the computation circuit. Substituting the proper expressions from *(4.12)* through *(4.14)* into *(4.18)* and letting $K_2 = K_3$, it is easily verified that this calculation forms an estimate of the rms output current,

$$i_{est}(t) \cong \sqrt{\frac{\sum_{k=1}^{N} i^2_{ref,k}}{N}}. \qquad (4.19)$$

Note the this estimate only depends on variables locally measurable by each cell. Also, this estimate can be computed without a priori knowledge of the number of converter cells, since this information is implicitly determined by *(4.14)* using the information contained in the output ripple voltage. The estimate can then be used in turn for current-balancing control.

The implementation of this estimator requires more circuitry than needed in the rms frequency estimator since we use derivatives of the sensed current and output voltage signals. In the design of analog circuitry to perform this estimate derived above, we employed: 1) band-limited differentiator circuits, 2) a method to compute the local-time rms values of the differentiated signals, and 3) a circuit to compute the ratio of these rms values as shown in *(4.18)*. Again, digital hardware can be used to compute the rms current value using equations similar to those derived above.

4.3 Design of Test Circuits

Section A.1 of Appendix A shows that a natural relationship exists between the average output current and switching frequency of the buck converter operated in the edge of discontinuous conduction mode. We have shown that each converter cell can compute an rms cell output current estimate from the information in the output ripple voltage. This section presents one possible design of a converter cell and estimator which may be used to investigate this current-balancing scheme.

4.3.1 Implementation of the Power Stage

Figure 4.4 illustrates the power stage design of the low-power prototype buck converter used for this investigation. The input supply voltage is V_{in} = 10 V, and the output voltage is regulated to 5 V, yielding $D \approx 0.5$. The converter cell was designed to operate over a load range of 1 - 10 mA. The inductor is sized to 125 mH, thus yielding a 1

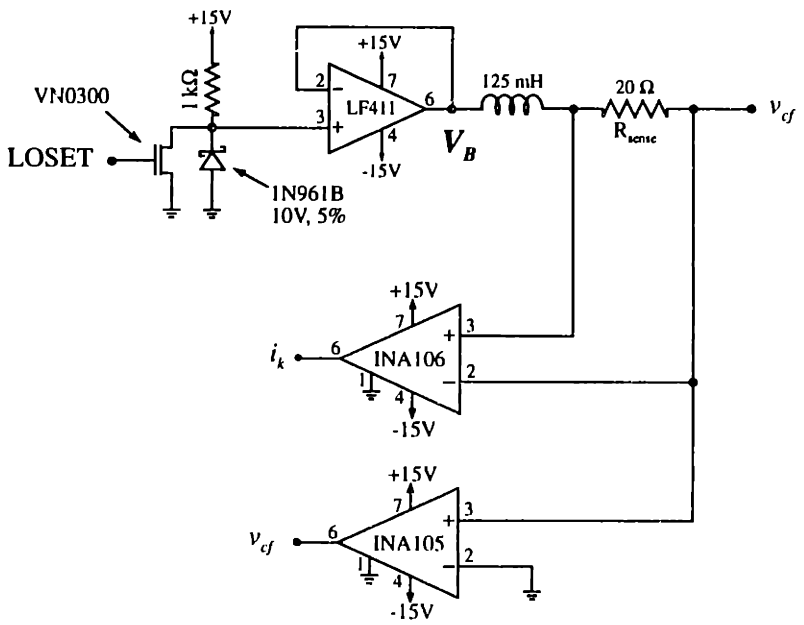


Figure 4.4: Schematic representation of EDM buck converter power stage.

- 10 kHz switching frequency range. To obtain a maximum voltage ripple of 100 mV_{pp}, a 25 μF output filter capacitor was selected.

Figure 4.5 show the implementation of an EDM current controller which drives the power stage, Fig. 4.4. The non-inverting amplifier is used to set the maximum inductor current limit, while the minimum limit is zero. The power stage is controlled by the active-low PWM signal, LOSET.

An explanation of a typical switching cycle, beginning when $i_k(t) = 0$ and LOSET is low, is as follows: While $i_k < 2i_{ref}$, pin 12 of the PM219 is clamped at +5 V through the diode, which means that $\overline{S}_2$ and $\overline{R}_4$ are high. In this state, Q2 (LOSET) is set low, the transistor is turned off, and the output voltage of the power stage buffer is at +10 V (clamped by the zener diode). During this time, the current through the inductor increases linearly until $i_k > 2i_{ref}$. When i_k reaches $2i_{ref}$, or positive limit, Q2 (LOSET) is set high, the transistor turned on, and the buffer output voltage falls to zero. During this time, the current through the inductor decreases. Once the inductor current decreases to the negative limit where ($i_k \cong 0$), Q2 (LOSET) goes low and the cycle starts over. To keep excessive noise from causing the controller to switch inadvertently, hysteresis bands can be set to increase the switching threshold of the comparators.

We selected a single E-L load, shown in Fig. 4.6, since we wanted the load to be effectively an open circuit relative to the filter capacitor over the switching frequency range. The voltage is set by a zener reference, and the load inductor is sized at 125 mH. Figure 4.7 illustrates several associated waveforms of the buck converter operating in the edge of discontinuous conduction mode.

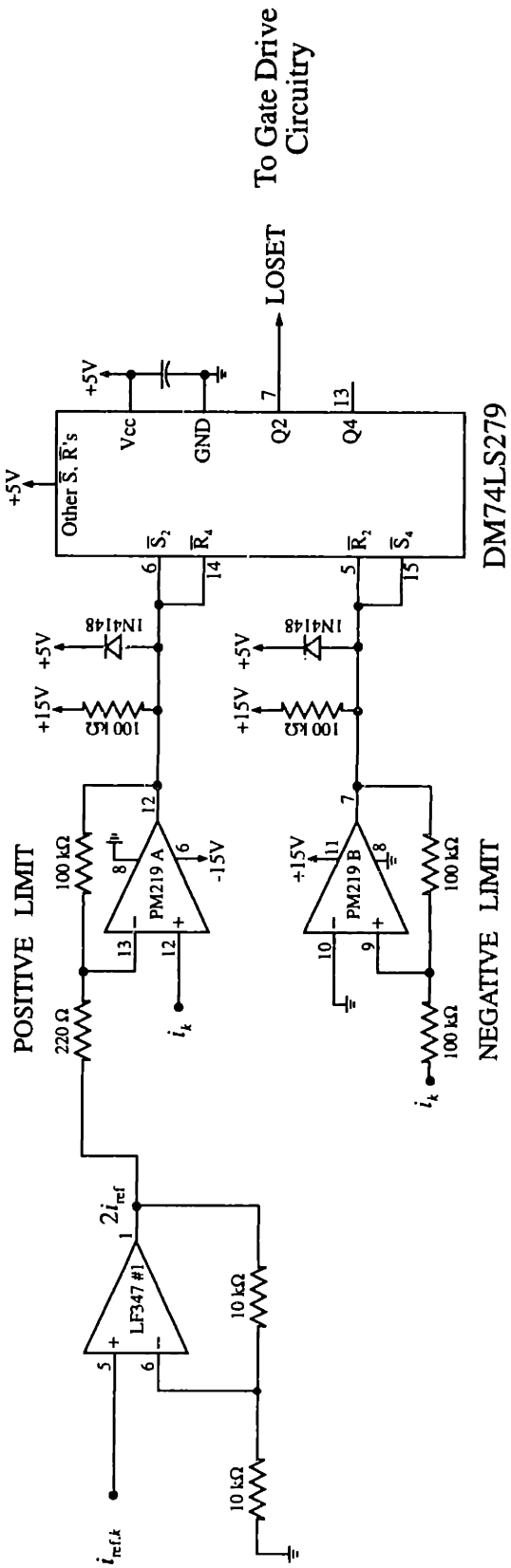


Figure 4.5: Current controller for EDM operation of the buck converter.

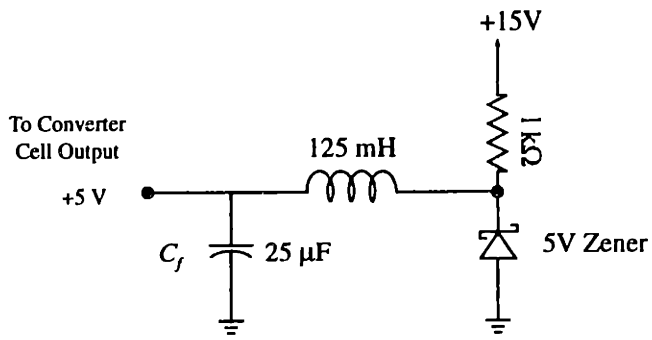


Figure 4.6: E-L load circuit used for EDM buck converter.

4.3.2 Implementation of the RMS Output Current Estimator

A functional circuit representation of the rms output current estimator which implements the result presented in *(4.19)* using simple, inexpensive analog circuitry is shown in Fig. 4.8. It is composed of the following stages: 1) pre-filter stage, 2) differentiation and gain stages, 3) rms to dc conversion stages, and 4) a computational stage which performs the proper multiplications and divisions. The estimator was designed to handle a switching frequency range of approximately 1 to 10 kHz.

The pre-filtering stage rejects the low (dc) and high (noise) frequency components of the sensed current and output voltage signals. This stage is comprised of a 2nd order low pass Butterworth filter with cutoff frequency f_c = 50 Hz and a 2nd order high pass Butterworth filter with f_c = 20 kHz.

The gain of the differentiation stages is set such that the maximum rating of the rms to dc converters is not exceeded. Here, we use band-limited differentiators that generate the derivative of the input signal over a limited frequency range [27]. This differentiator circuit has the property that above a cutoff frequency (f_c = 50 kHz), its gain rolls off like an integrator at -20dB/decade to attenuate any high frequency noise.

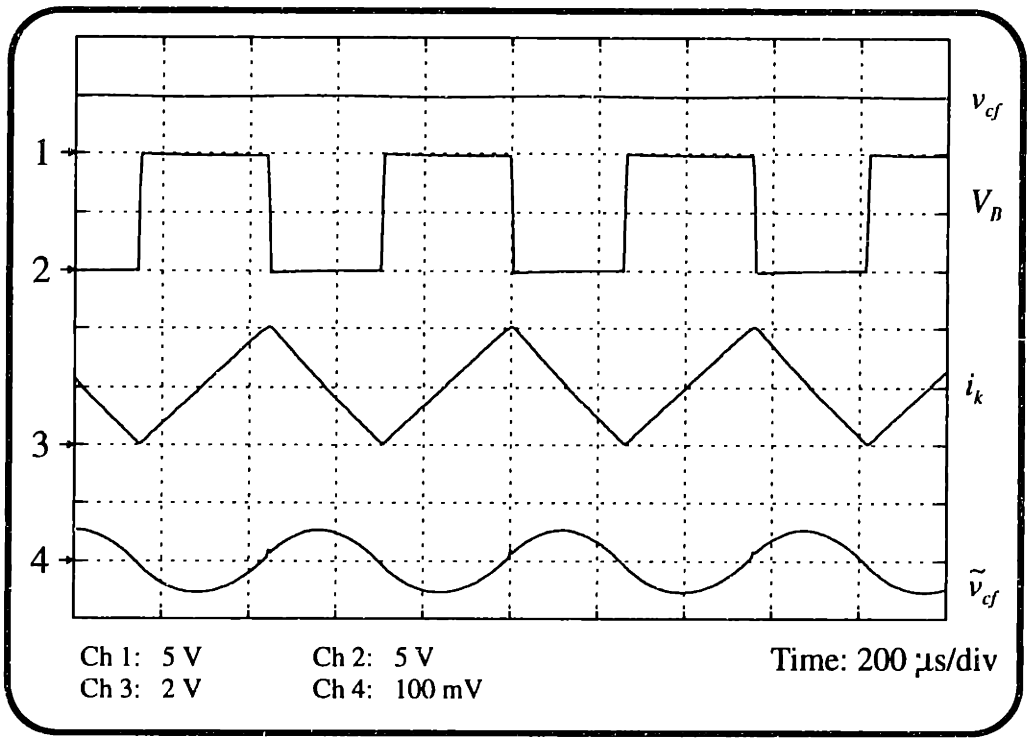


Figure 4.7: Associated waveforms of the EDM operated buck converter.

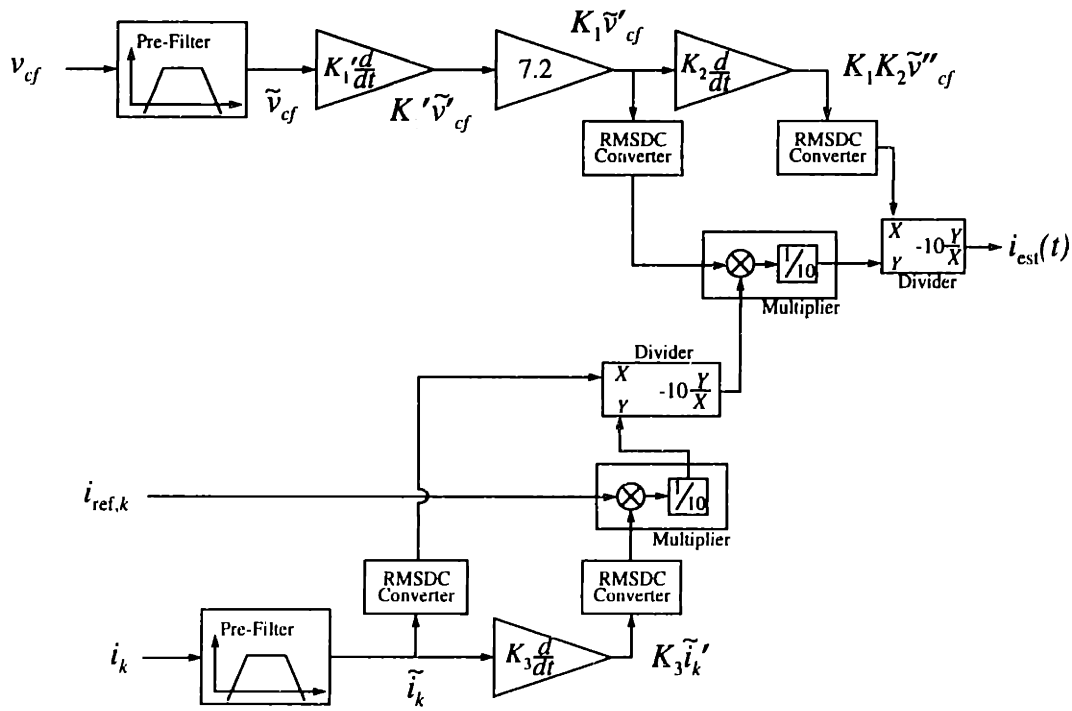


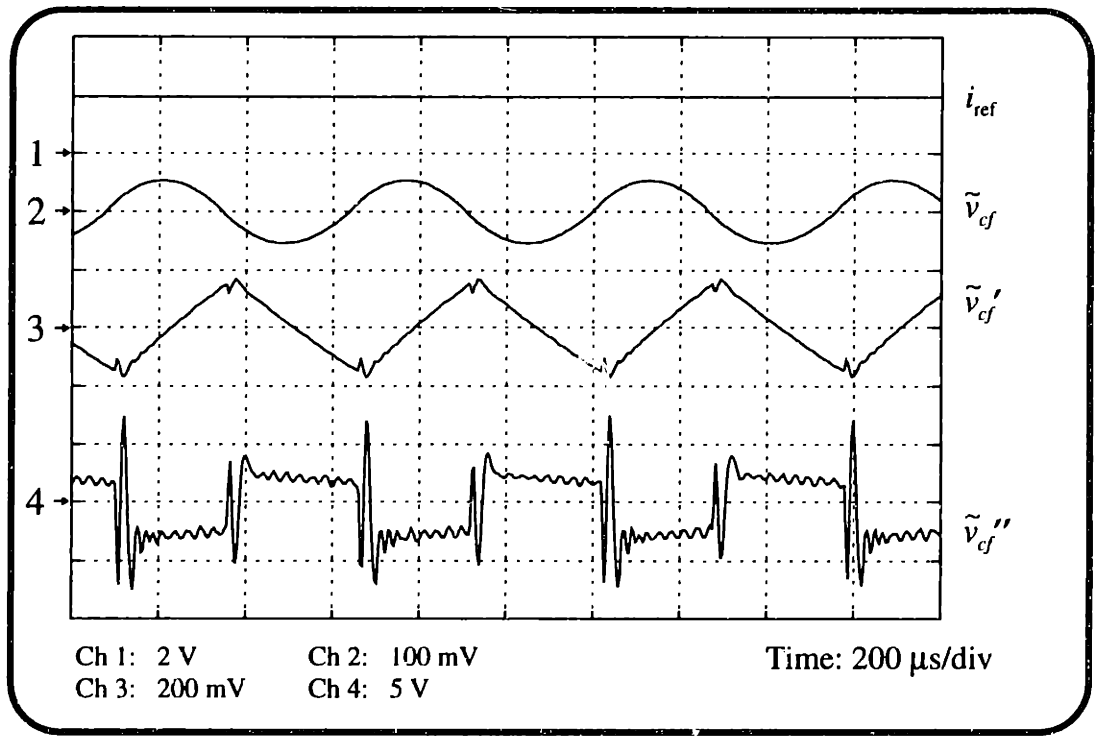
Figure 4.8: Functional circuit representation of the output rms current estimator.

AD637 rms to dc converters were again used to compute the local-time rms values of the various signals. They are connected in the same two pole Sallen-Key configuration as presented in Subsection 2.2.1.

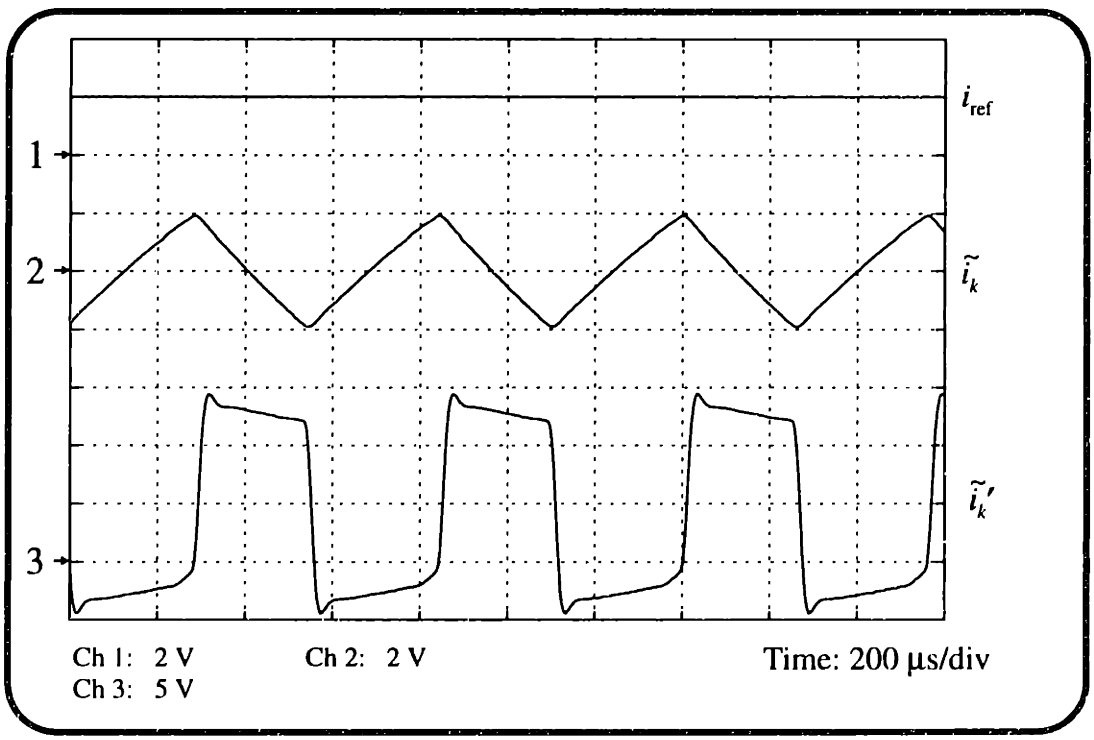
The AD633JN multiplier was used in this estimator implementation. Division was realized by placing this four-quadrant multiplier in the feedback path of an LF347 operational amplifier.

4.3.3 Design Limitations

We present these designs as one possible implementation of the EDM buck converter and rms output current estimator. Figure 4.9 shows the intermediate waveforms used to compute the rms output current estimate. As expected, the first derivative of the output ripple voltage is proportional to the cell output current. The second derivative of the output voltage has the correct form, but has pronounced noise peaks which can affect the final estimate. The performance of this estimator over the range of reference currents is shown in Fig. 4.10. In full power converter systems, the output ripple voltage of the cell is likely to have appreciable noise introduced due to the switching of the converter. Although the signal is pre-filtered, it is differentiated twice to obtain the signals needed in the calculation of the output rms current. This implies that the inherent noise associated with the differentiating signals is likely to affect the results significantly as the power level is raised. Thus, while the concept of the switching ripple method seems viable, the tested implementation is unlikely to be suitable at realistic power levels. For this reason, we decided not to pursue further investigation of this approach.



(a)



(b)

Figure 4.9: Intermediate rms output current estimate waveforms.

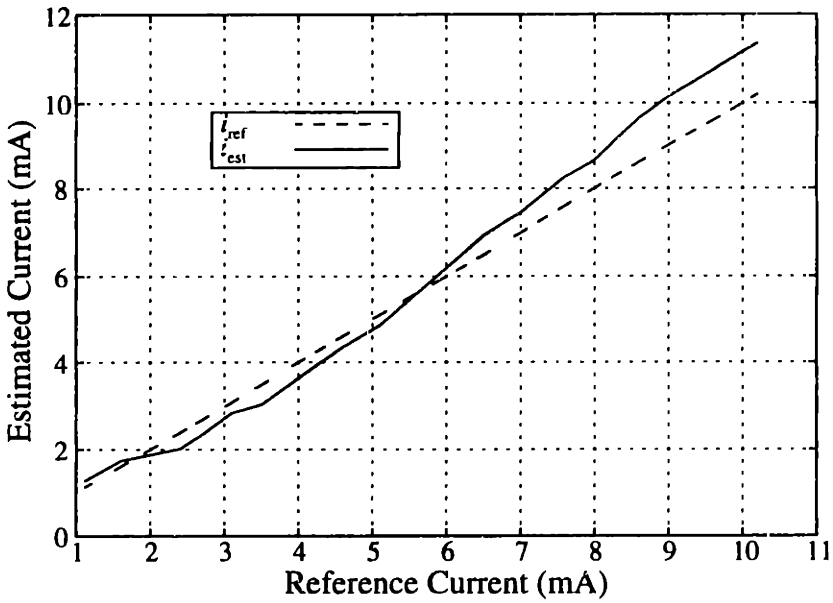


Figure 4.10: RMS output current estimator performance.

Chapter 5

Conclusions and Recommendations

In Chapter 1 we presented the concept of a cellular architecture and possible advantages that may be obtained when using it to construct high power converter systems. One major challenge that must be overcome to realize the potential benefits of the cellular architecture is the design of a control mechanism which enforces equal current sharing among the paralleled cells.

In Chapter 2 and 3, different versions of a new frequency-based approach for current-balance control were presented. These methods operate by frequency-encoding current sharing information onto the output bus at frequencies widely separated from the fundamental output frequency of the system. A key attribute of this control technique is that it achieves current balancing among the converter cells with no additional inter-cell connections.

We introduced one method in which small sinusoidal perturbations, whose magnitude and frequency were related to the cell's reference current, were used to inject current-sharing information onto the output bus. The second method utilized the inherent relationship between the switching frequency and average output current of a converter cell, operating in the edge of discontinuous conduction mode, to encode current-balancing information. In both cases, the converter cells employed a frequency-based estimator which computed necessary control quantities from the information present in the output voltage harmonics.

As shown in Subsection 4.3.3, the implementation of the rms output current estimator for the switching frequency ripple method exhibited a high sensitivity to noise. Hence, we

chose to implement the injected perturbation control method in the current-balance control system for the cells in the prototype cellular converter system. This method uses information locally measurable by the cells to adjust the reference voltages via the reference voltage controllers. Output voltage controllers then use the difference between the adjusted reference voltage and the output voltage to vary the reference current resulting in control of both the output voltage and load balance among the converter cells.

Functional testing of the prototype converter systems showed that only a minor degree of current sharing existed among the cells without current-balance control. However, with current-balance control, the load current is shared by the cells to within 10% of the average over a wide range of load values. Dynamic testing demonstrated that the current-balance controllers exhibited acceptable performance in the presence of large load changes.

Based on the results of this thesis, the following recommendations for future work are provided. The current sharing accuracy among the cells is directly related to the accuracy of the estimators and current-balance controllers. Enhancing the computational accuracy of the estimators will reduce the measurement discrepancies among the converter cells. Further investigating the current-sharing control dynamics for this frequency encoding scheme can result in improved stability, performance, and robustness of the controller design. Together, enhanced estimator and controller can be used to provide even better static and dynamic current-sharing performance of the converter cells.

For the switching frequency ripple method, the rms output current estimator implementation was very susceptible to noise interference. Therefore, it is recommended that, for the EDM converter cell, different control variables, whose computation (estimation) is not as noise sensitive, be used in the control scheme to achieve load balance.

Although we have only presented two possible control methods which feature a zero wire implementation, other methods exist in which current-sharing information can be transferred among the converter cells (e.g., an isolated single wire interconnect approach). These current-balance control methods should be investigated to determine their usefulness in a cellular architecture.

Just as other control methods should be investigated, other implementations of the frequency-based estimator need to be explored as well. We implemented the estimators using analog circuitry. However, the implementation of the frequency-based estimators using other structures or methods such as digital hardware can increase the range of control variables used to improve the accuracy of the overall control system.

Once these issues have been properly addressed, a full power converter system can be constructed using the frequency-based approach for current-sharing to demonstrate the usefulness of this technique at high power levels.

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Appendix A

Derivations

A.1 Buck Converter in Edge of Discontinuous Conduction Mode (EDM)

The basic schematic of the buck converter and its inductor current waveform in the *edge of discontinuous conduction mode* (EDM) operation is illustrated in Figs. A.1 and A.2. In this mode, the inductor current goes to zero at the end of the switching cycle by

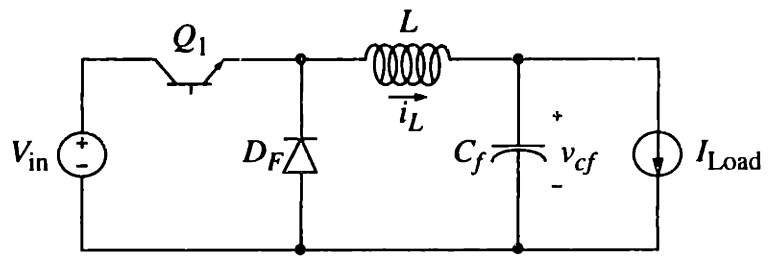


Figure A.1: Circuit schematic of the basic Buck converter

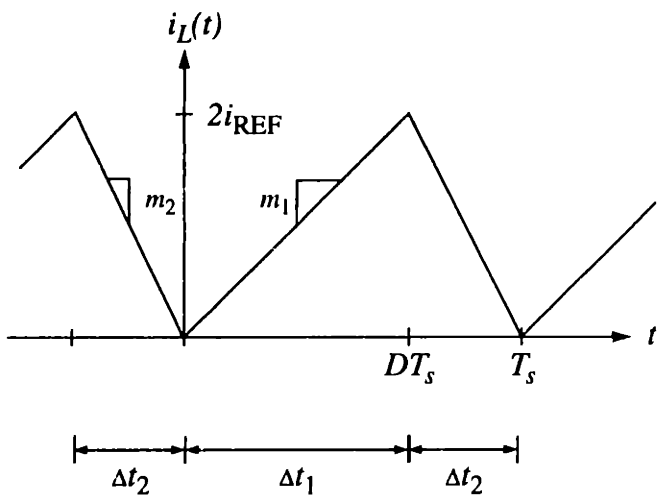


Figure A.2: Waveform of $i_L(t)$ in *edge of discontinuous conduction mode* (EDM).

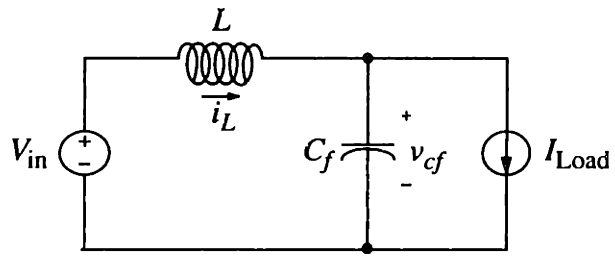


Figure A.3: The equivalent circuit for Fig. A.1 when Q_1 is on for time DT_s.

definition. Here, we assume that the converter is supplying a constant voltage to an output resistive load. This assumption is based on the premise that the output filter capacitor is large enough to clamp the output voltage for the duration of the period.

Figs. A.3 and A.4 show the equivalent circuits of Fig. A.1 for the two switching states. When Q_1 is turned on for a time, DT_s, the inductor current increases linearly from zero to a peak value, $2i_{REF}$ (set by the controller) with a slope:

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t_1} = \frac{V_L}{L} = \frac{V_{in} - v_{cf}}{L} \qquad (A.1)$$

where $\Delta i_L = 2i_{REF}$. The corresponding slope of the capacitor voltage during this time is:

$$\frac{dv_{cf}}{dt} = \frac{I_{Load} - i_L}{C_f}. \qquad (A.2)$$

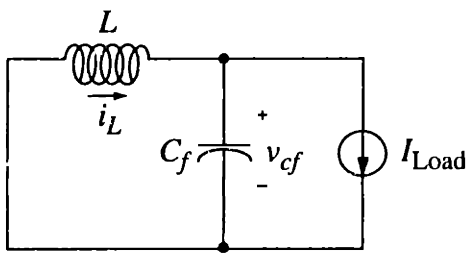


Figure A.4: The equivalent circuit for Fig. A.1 when Q_1 is off for $(1\text{-}D)T_s$.

When the current reaches $2i_{REF}$, Q_1 is turned off and the inductor current decreases linearly for a time $(1\text{-}D)T_s$, as it circulates through the freewheeling diode D_F. The slope of the inductor current and capacitor voltage for this time period is given by:

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t_2} = \frac{V_L}{L} = \frac{-v_{cf}}{L} \qquad (A.3)$$

and

$$\frac{dv_{cf}}{dt} = \frac{I_{Load} - i_L}{C_f}. \qquad (A.4)$$

The inductor charge and discharge times can be computed from *(A.1)* and *(A.3)* and Fig. A.2 as:

$$\Delta t_1 = \frac{2Li_{ref}}{V_{in} - v_{cf}} \qquad (A.5)$$

and

$$\Delta t_2 = \frac{2Li_{ref}}{v_{cf}}. \qquad (A.6)$$

The switching period, T_s, can be expressed in terms of the circuit parameters by summing the inductor charge and discharge times. The result, with reference to Figs. A.1 and A.2, is:

$$T_s = \Delta t_1 + \Delta t_2 = \frac{v_{cf}L(2i_{ref}) + (V_{in} - v_{cf})L(2i_{ref})}{v_{cf}(V_{in} - v_{cf})}$$

$$T_s = \frac{V_{in}L(2i_{ref})}{v_{cf}(V_{in} - v_{cf})}. \qquad (A.7)$$

Equation *(A.7)* and Δi_L, we can deduce that the switching frequency and the peak-to-peak voltage ripple are inversely proportional to i_{ref}.

A.2 Computation of Fourier Series Coefficient, C_n

The Fourier Series coefficient of the inductor current is computed to determine its dependence on the reference current. These coefficients give the magnitude of the inductor current harmonics for the converter cell. From equation *(A.8)*, we see that C_n is the result of performing a complex integral on $i_L(t)$ over the converter switching period, T_s.

From the inductor charge and discharge times shown in Fig. A.2, the expanded equation becomes,

$$C_n = \frac{1}{T_s}\int_{-\Delta t_2}^{0} m_2 t e^{-jn\omega_o t}dt + \frac{1}{T_s}\int_{0}^{\Delta t_1} m_1 t e^{-jn\omega_o t}dt \qquad (A.8)$$

where $T_s = 2\pi/\omega_o$ and m_1, m_2 correspond to the positive and negative slopes of the waveform, respectively.

Using integration by parts to solve this integral, we obtain,

$$C_n = \frac{m_2}{T_s}\left[\frac{1}{n^2\omega_o^2} - \frac{t}{jn\omega_o}\right]e^{-jn\omega_o t}\Bigg|_{-\Delta t_2}^{0} + \frac{m_1}{T_s}\left[\frac{1}{n^2\omega_o^2} - \frac{t}{jn\omega_o}\right]e^{-jn\omega_o t}\Bigg|_{0}^{\Delta t_1}. \qquad (A.9)$$

After applying the limit we find that C_n can be written as:

$$C_n = \frac{m_2}{T_s}\left[\frac{1}{n^2\omega_o^2}\left(1 - e^{jn\omega_o\Delta t_2}\right) - \frac{\Delta t_2}{jn\omega_o}e^{jn\omega_o\Delta t_2}\right] + \frac{m_1}{T_s}\left[\frac{1}{n^2\omega_o^2}\left(e^{-jn\omega_o\Delta t_1} - 1\right) - \frac{\Delta t_1}{jn\omega_o}e^{-jn\omega_o\Delta t_1}\right]. \qquad (A.10)$$

Expanding this equation we see that for the k[th] converter, the Fourier Series coefficients are given by:

$$C_{n,k} = \frac{m_2}{2\pi n^2\omega_k}\left(1 - e^{jn\omega_k\Delta t_2}\right) - \frac{m_2\Delta t_2}{j2\pi n}e^{jn\omega_k\Delta t_2} + \frac{m_1}{2\pi n^2\omega_k}\left(e^{jn\omega_k\Delta t_1} - 1\right) - \frac{m_1\Delta t_1}{j2\pi n}e^{jn\omega_k\Delta t_1} \qquad (A.11)$$

where $\omega_k = 2\pi/T_k$. From *(A.7)* we also know that,

$$T_s = \frac{V_{in} L (2 i_{ref})}{v_{cf} (V_{i.} - v_{cf})} ,$$

and thus, $C_{n,k}$ is proportional to i_{ref} through ω_k.

Appendix B

Circuit Implementations

B.1 Injected Perturbation Method

The following circuits are the actual circuits used in realizing the prototype system which implements the injected perturbation method for current-balance control.

The pre-filter and pre-amplification stage and rms to dc conversion circuitry is shown in Fig. B.1. Figure B.2 illustrates the section of the estimator circuit, also described in Section 2.2, which implements the divider circuit with an output compensation circuit to ensure that the estimate remains correct over the perturbation frequency range. The circuitry which generates the small sinusoidal perturbations is shown in Fig. B.3. The power stage of the buck converter used to realize the cells is shown in Fig. B.4. The circuit which was considered for the voltage controller is shown in Fig. B.5. Figure B.6 illustrates the current-balance controller circuitry.

B.2 Cell Switching Ripple Method

Since the current feedback controller and power stage of the buck converter cell in EDM operation was shown in Section 4.3, the remaining circuitry illustrates the output rms current estimator implementation for the alternate current-balance control approach described in Section 4.2.

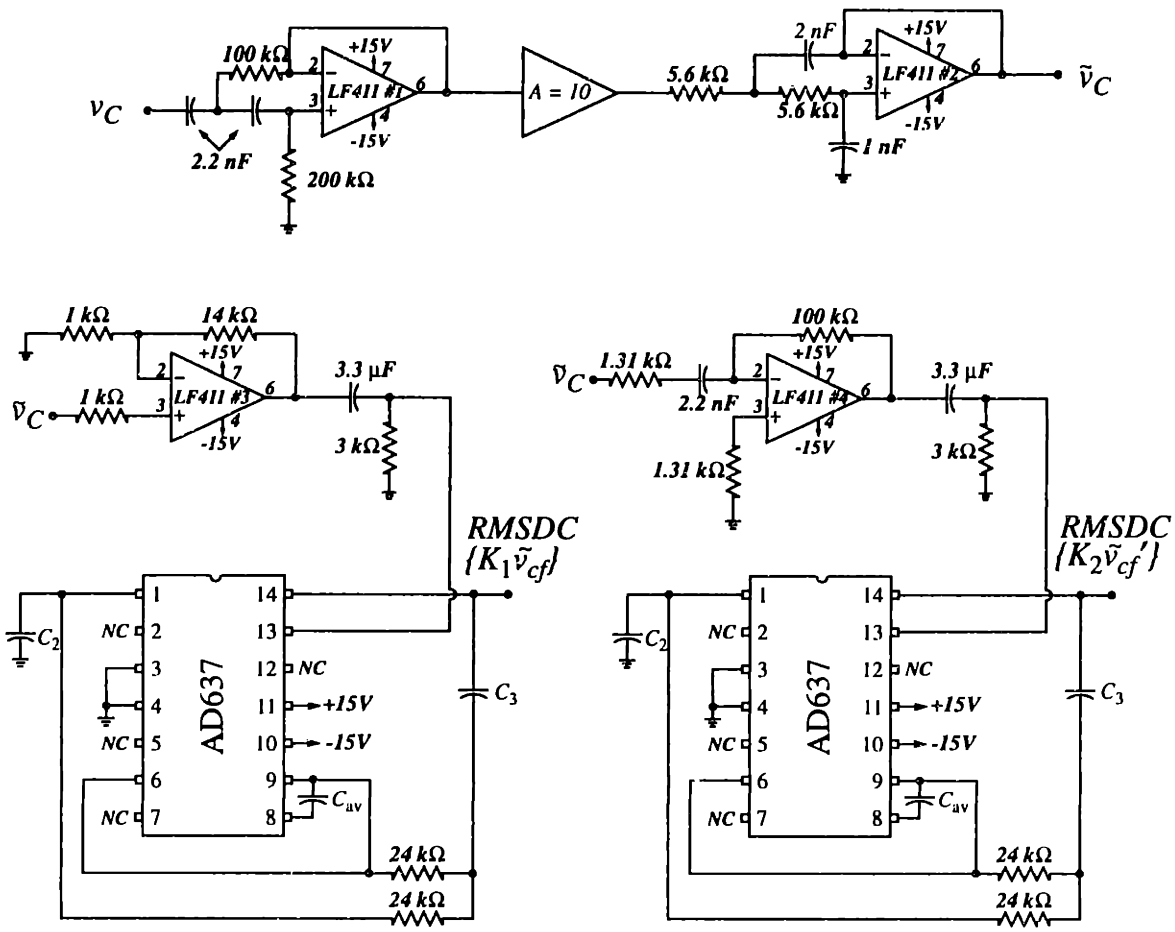


Figure B.1: The section of the RMS Frequency Estimator circuit which performs the pre-filter and pre-amplify, gain and differentiation, and rms to dc conversion functions described in Section 2.2.

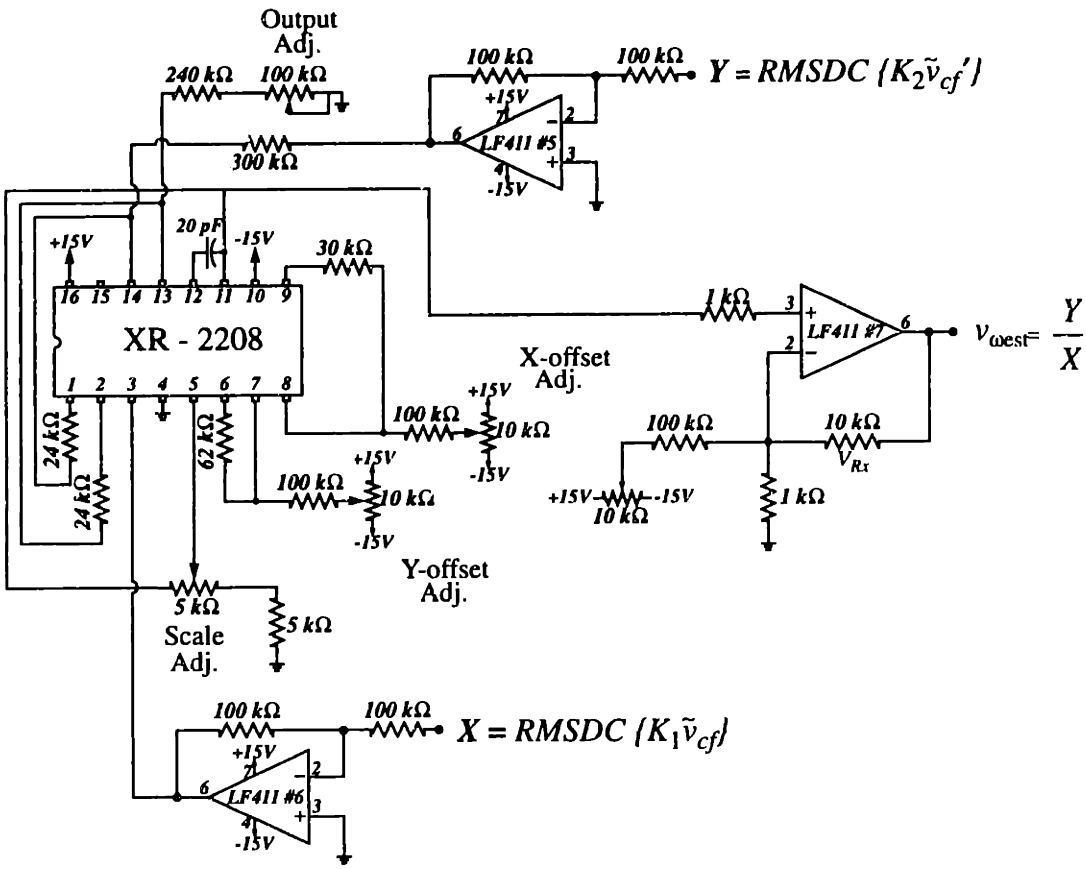


Figure B.2: RMS Frequency Estimator circuit: Division stage with output compensator.

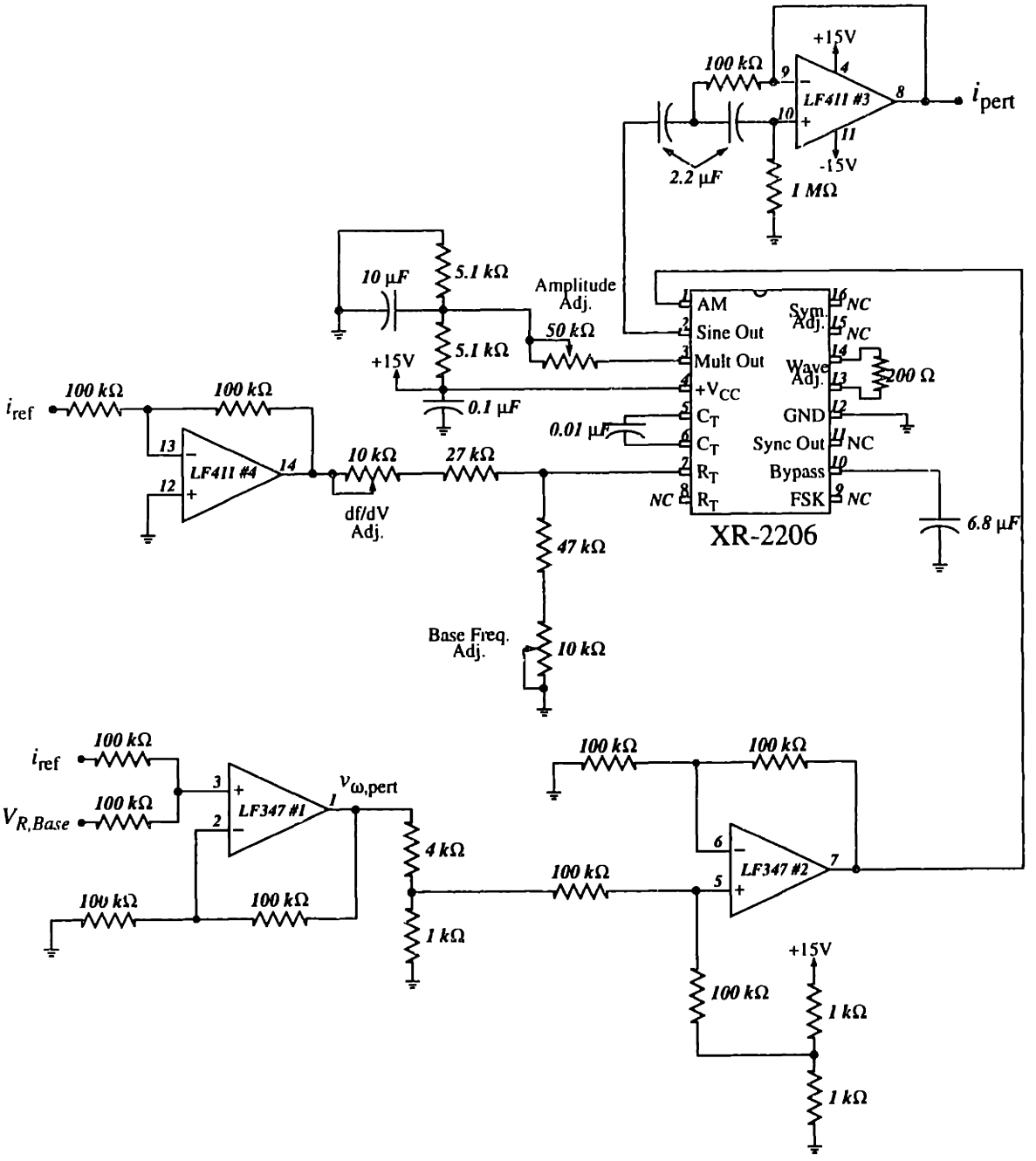


Figure B.3: Perturbation generator which generates a small sinusoidal signal whose magnitude and frequency are proportional to the reference current. This circuit's operation is discussed in Section 2.3.

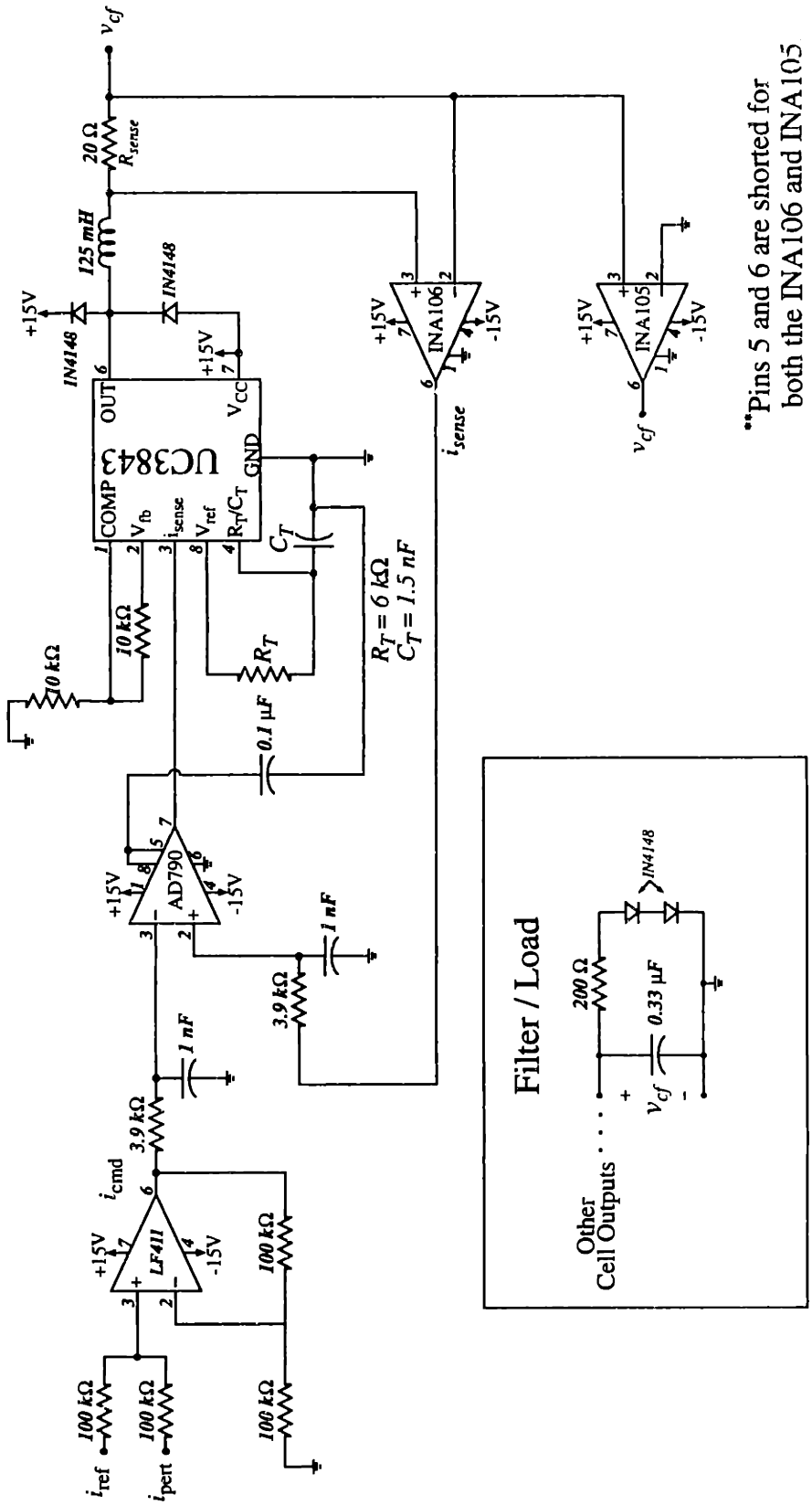


Figure B.4: Converter cell main power stage implementation. The operation of this circuit is presented in Section 2.4.

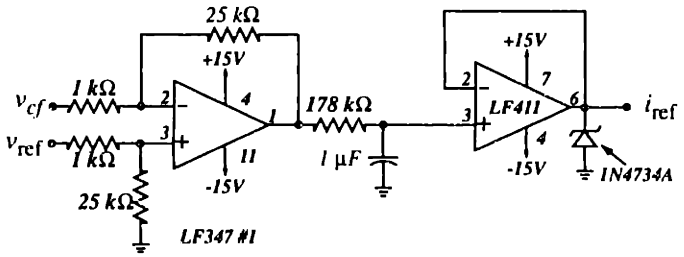


Figure B.5: The proportional (P) controller with output follower to buffer the reference current signal is described in Section 2.5.

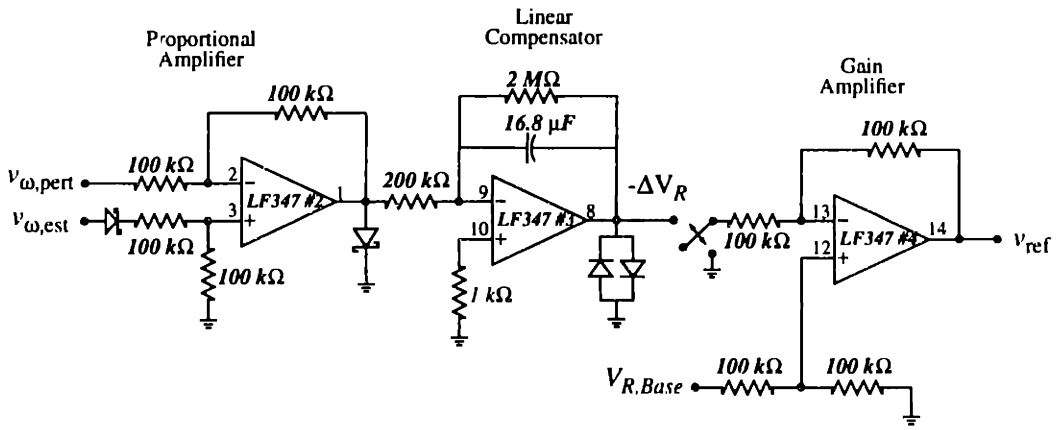


Figure B.6: Section 2.5 discusses the current-balance controller which uses the rms frequency estimate and the voltage representation of the perturbation frequency to adjust v_{ref} so that load balance is achieved.

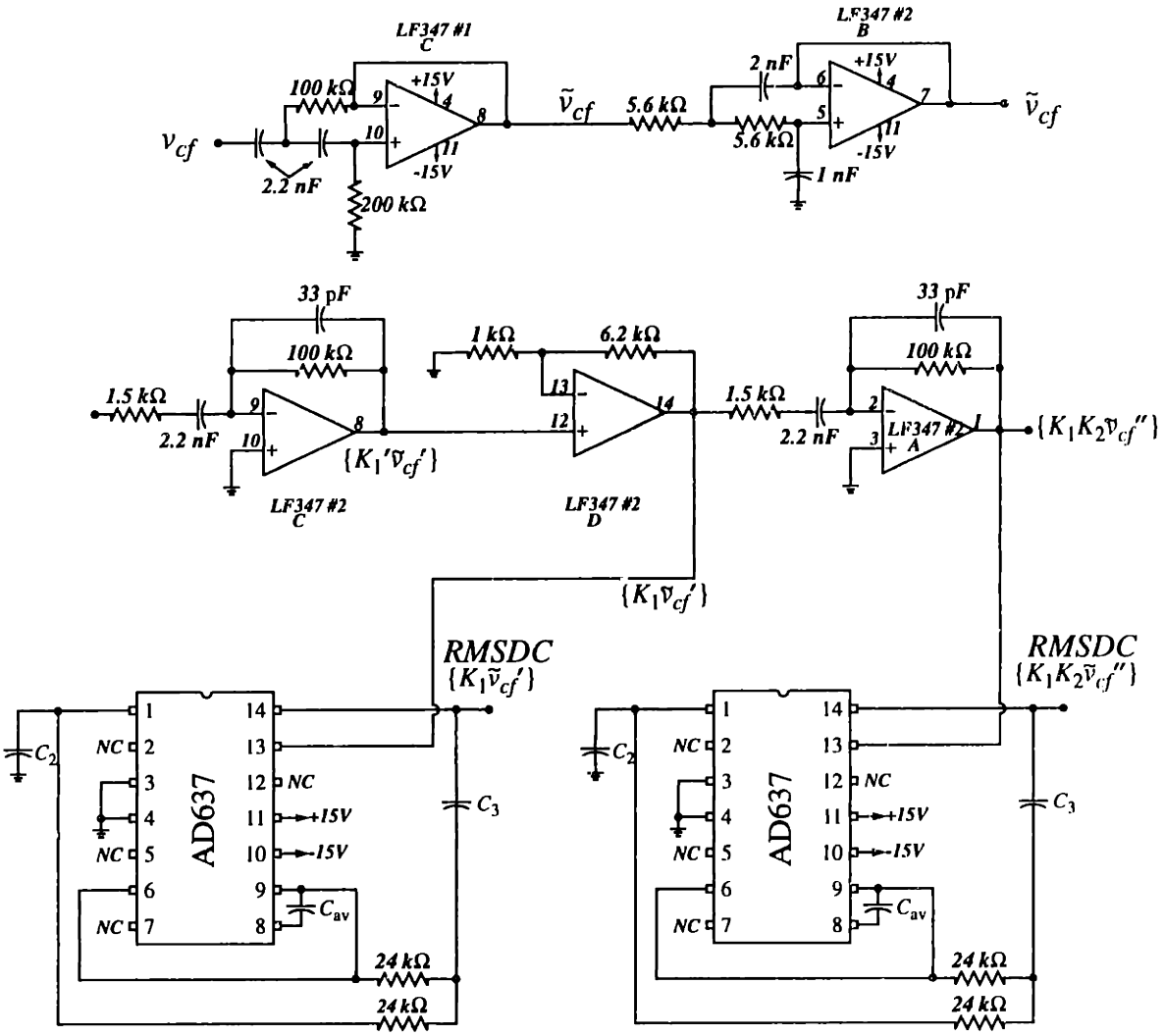


Figure B.7: The circuitry employed to perform the pre-filtering, differentiation, and rms to dc conversion of the output voltage described in Section 4.2.

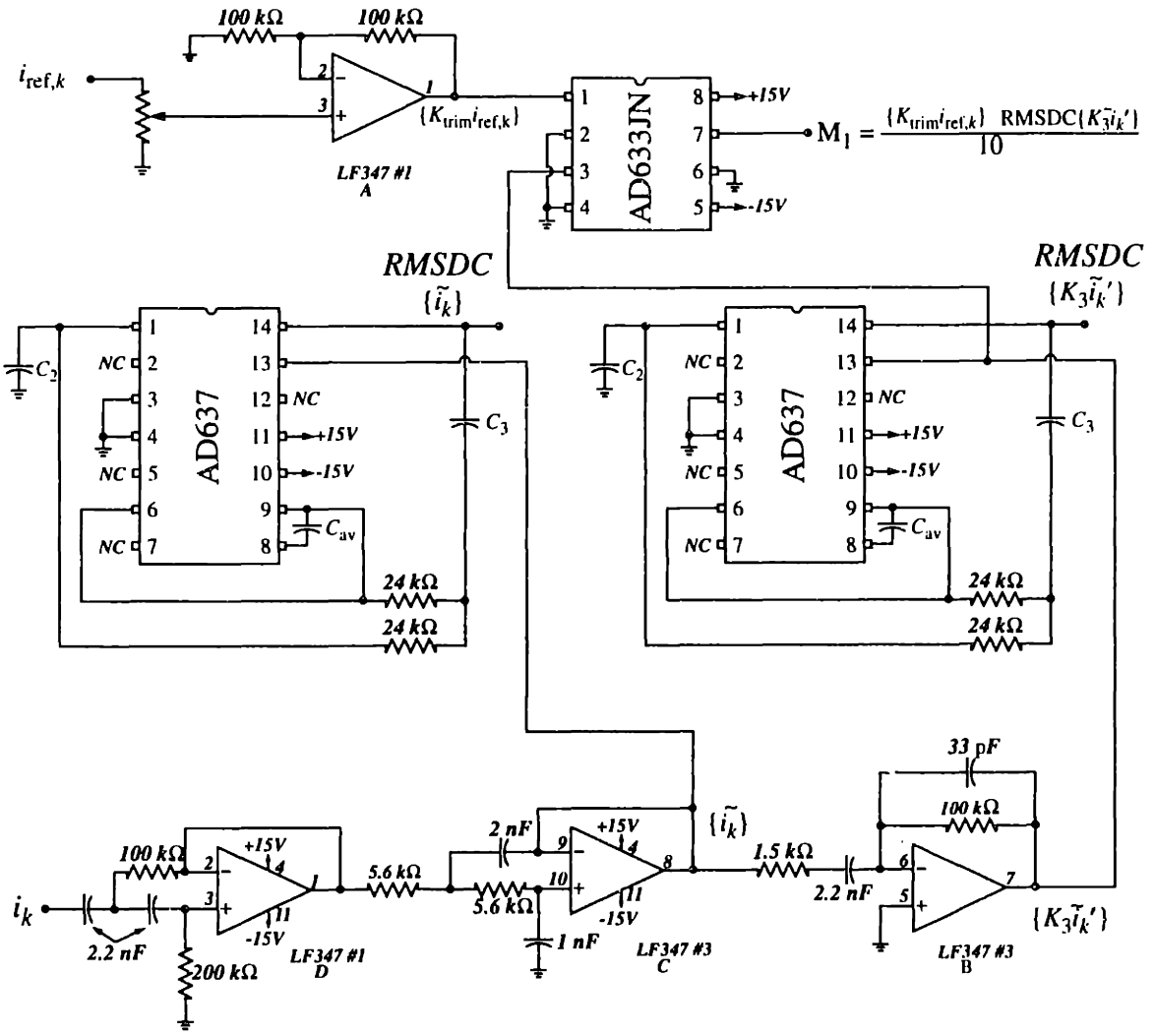
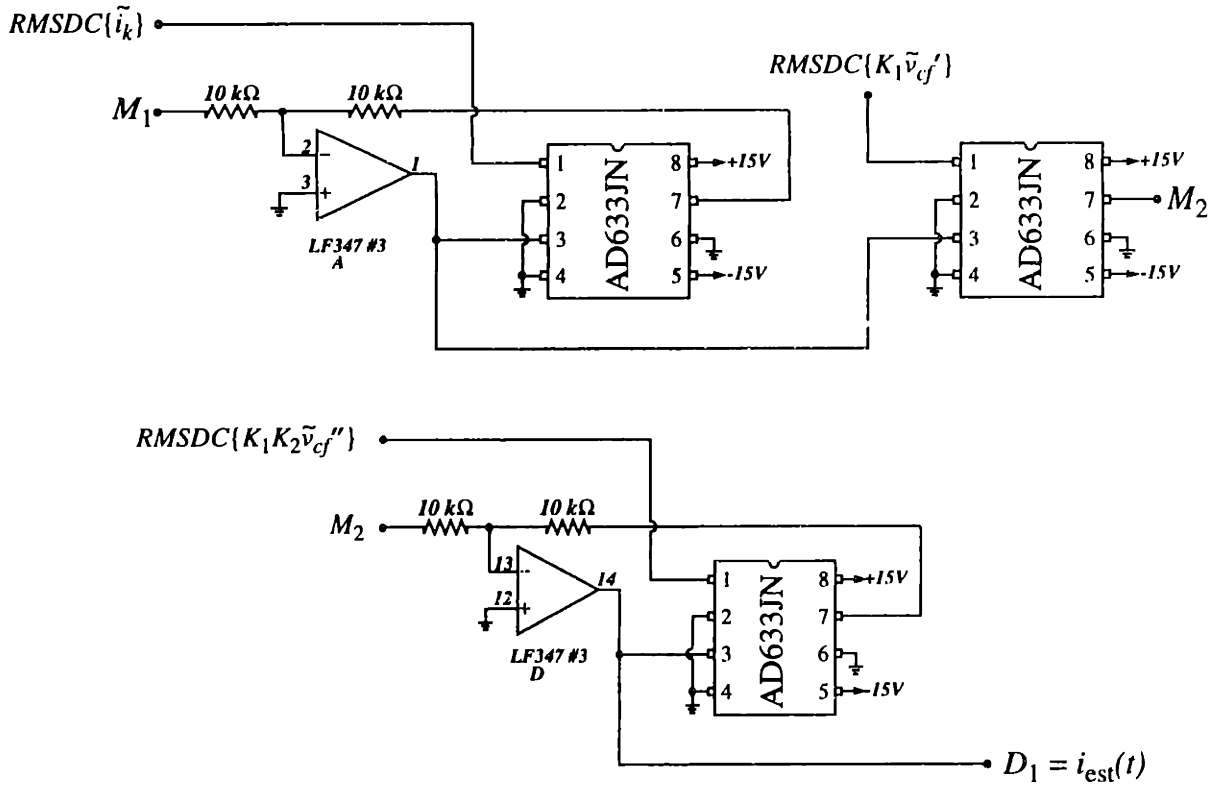


Figure B.8: The circuitry used to perform the pre-filtering, differentiation, and rms to dc conversion of the sensed fed back current, i_k.



$$i_{est}(t) = \frac{(\text{RMSDC}\{K_1\tilde{v}_{cf}'\})\ (\text{RMSDC}\{K_3\tilde{i}_k'\})\ (K_{trim}i_{ref,k})}{(\text{RMSDC}\{\tilde{i}_k\})\ (\text{RMSDC}\{K_1K_2v_{cf}''\})}$$

Figure B.9: Multiply and division circuitry of computational stage.

Appendix C

Alternate Compensator Design

C.1 Alternate Current-Sharing Controller Design

This appendix describes an alternate reference voltage controller containing a nonlinear integrate and hold compensator as shown in Fig. C.1. Integrate and hold approaches have been used for current-sharing compensation in the various applications [24].

This controller, which was tested as an alternate to the linear compensator of Fig. 2.17, operates in the following manner. If $v_{\omega,est} > v_{\omega,pert}$, then the diode D_1 of the integrate and hold compensator is turned on and the voltage to the linear section of this compensator is greater than zero. Like the linear compensator, this linear section acts as an integrator with finite gain. This alternate compensator adjusts the value of v_{ref} upward so that current sharing can be achieved via regulating the cell reference current. If $v_{\omega,est} > v_{\omega,pert}$, then the diode is off and the cell is held in its present state (with ΔV_R decaying very slowly towards zero).

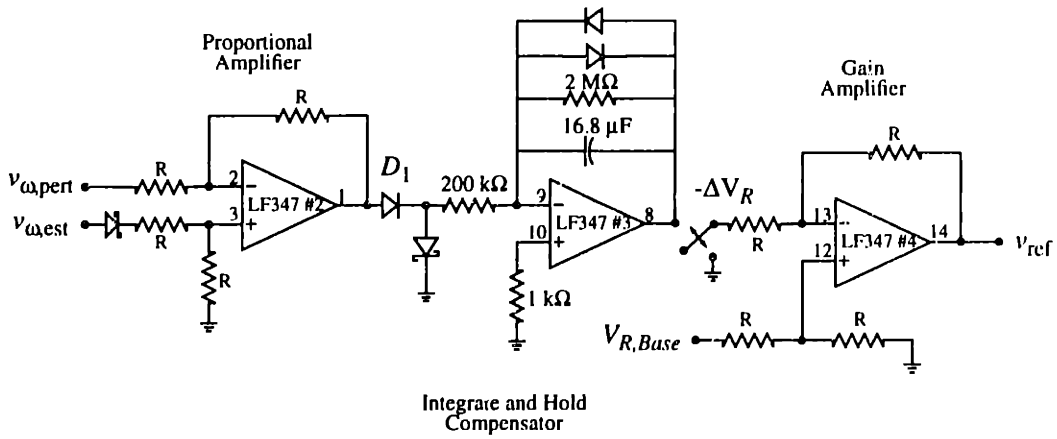


Figure C.1: Functional schematic of the alternate reference voltage controller.

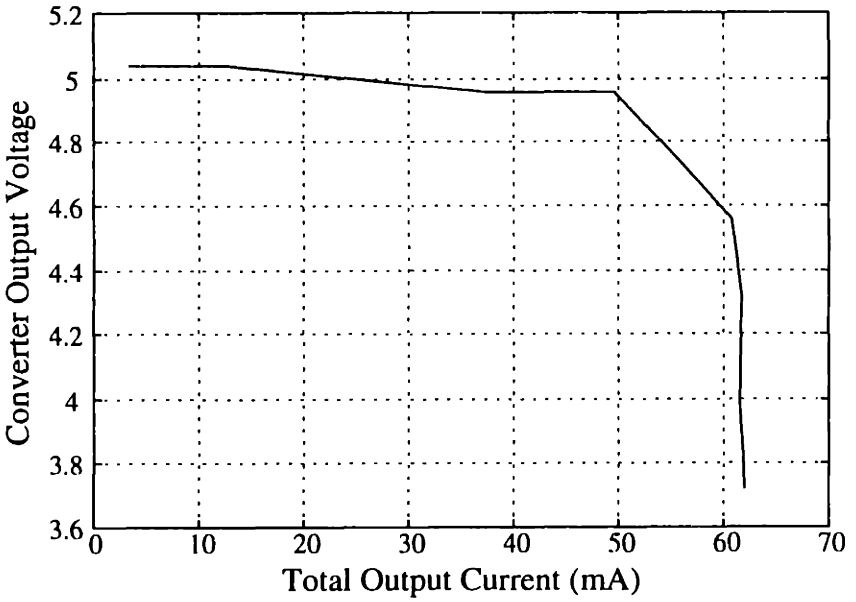


Figure C.2: Load regulation curve of prototype cellular system output voltage.

This alternate controller was tested in the same system as all the previous tests. The only significant difference was that the Zener diode used to clamp the reference current command signal was placed at the input of the voltage follower instead of the output. The major effect of this difference was a lower maximum output current command, resulting in load regulation at lower output currents, Fig. C.2. We see that the output voltage is regulated to within 5% for a load currents up to approximately 50 mA, implying that each cell can carry about 17 mA before heavy regulation occurs. As the load current increases, i_{ref} eventually reaches the limit imposed by the Zener diode and the system output voltage decreases since the current-limited converters can no longer support the load at 5 V.

The static load sharing characteristic for this alternate controller is shown in Fig. C.4, while data for 95% and 5% load are tabulated in Table C.1 and C.1. From Fig. C.3 we see that cell #1 and cell #2 share current more closely than does cell #3. This occurs because the frequency estimator of cell #3 generates an estimate that is slightly lower that the others. The controller of cell #3 thus regulates its output current to a lower value. In spite of this, the converter cells still share current in a reasonable manner over this wide load

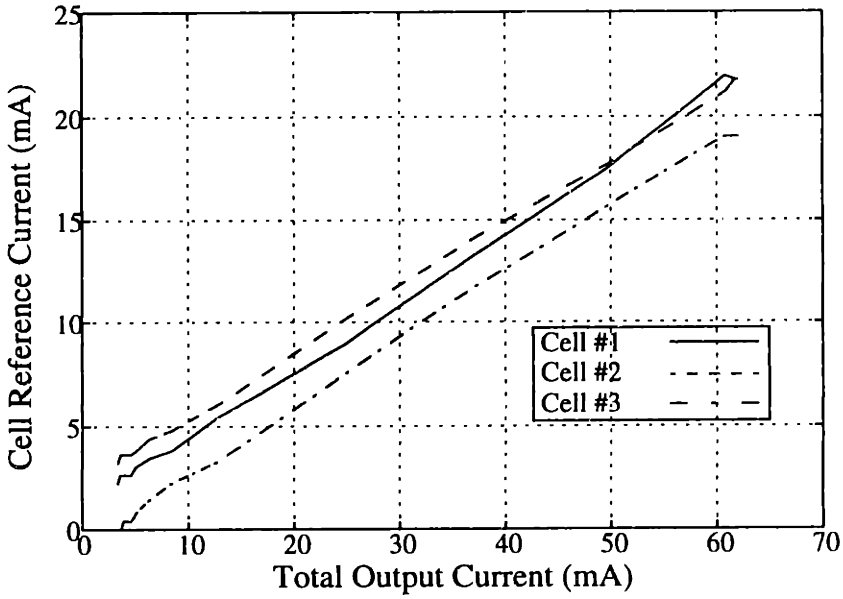


Figure C.3: Converter cell reference current versus total output current.

range. Figure C.4 illustrates an alternate output voltage controller used to vary the reference current so that load-balance is achieved among the converter cells.

Table C.1: Load sharing data @ 95% Load: v_{cf} = 4.4 V, R_{Load} = 75 Ω

Converter	$V\{i_{\text{ref}}\}$ (mV)	i_{ref} (mA)
Cell #1	4.4 V	22.0 mA
Cell #2	4.24 V	21.2 mA
Cell #3	3.8 V	19.0 mA

Table C.2: Load sharing data @ 5% Load: v_{cf} = 5.04 V, R_{Load} = 1.3 kΩ

Converter	$V\{i_{\text{ref}}\}$ (mV)	i_{ref} (mA)
Cell #1	520 mV	2.6 mA
Cell #2	720 mV	3.6 mA
Cell #3	80 mV	0.4 mA

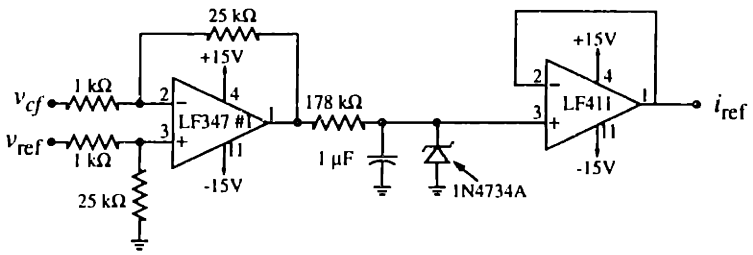
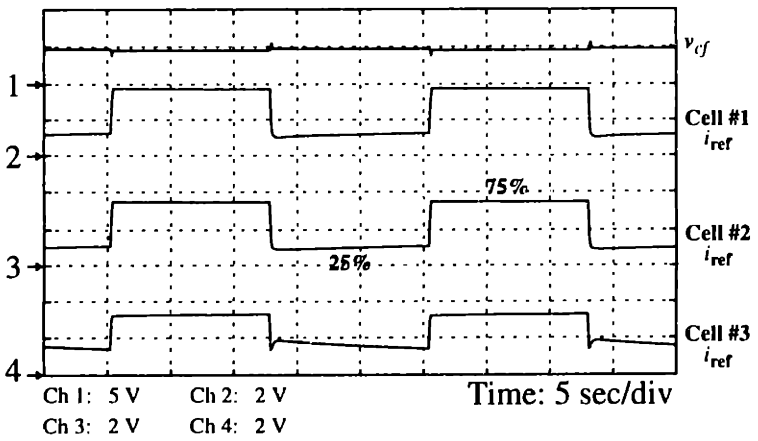


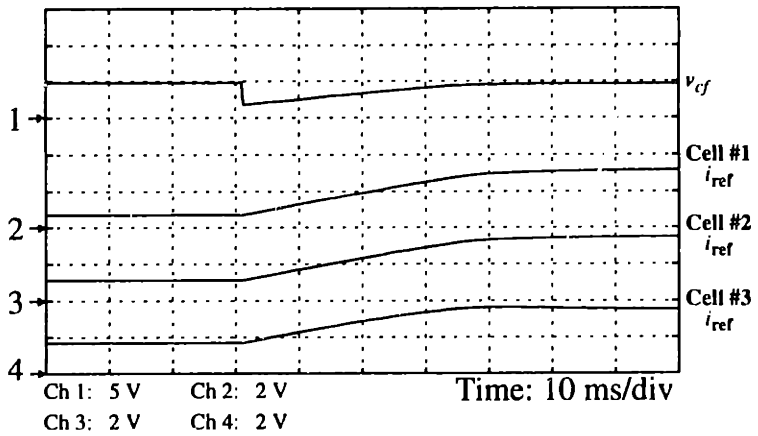
Figure C.4: Alternate output voltage controller.

Table C.1 lists the data corresponding to the operating point for R_{Load} = 75 Ω and shows the related cell reference currents. We can infer from this table that the cells share the load current to within 10% of each other. However at lighter loads (Table C.1), the current sharing performance is not as good as in the case of heavier loads.

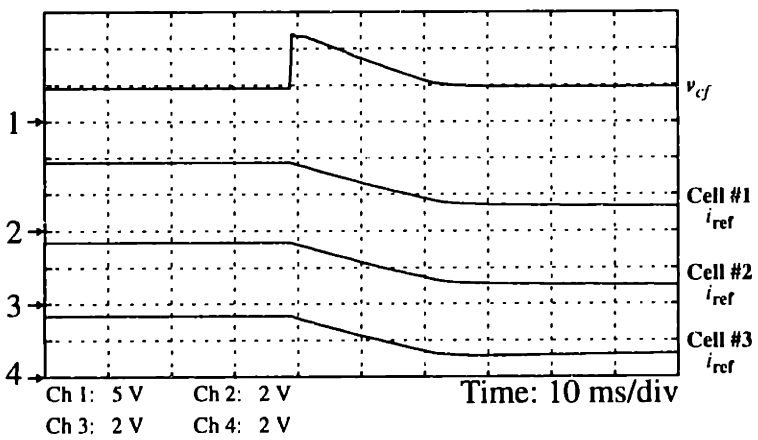
Dynamic load step tests identical to the one described in Subsection 3.2.3 were also performed for the alternate compensator.The results of these tests, shown in Figs. C.5 - C.9), demonstrate that the current-sharing control is stable and well damped over the load range. It may be concluded that this type of "integrate and hold" compensator is also potentially useful in the load-balancing control scheme for some applications.



(a)



(b)



(c)

Figure C.5: 25% to 75% dynamic load step test showing: (a) the current sharing responses of the converter cells; (b) the transient response of the voltage loop for a 25% to 75% load step; and (c) the transient response of the voltage loop for a 75% to 25% load step. Note that the current-sharing response is on a much slower time scale than the voltage loops.

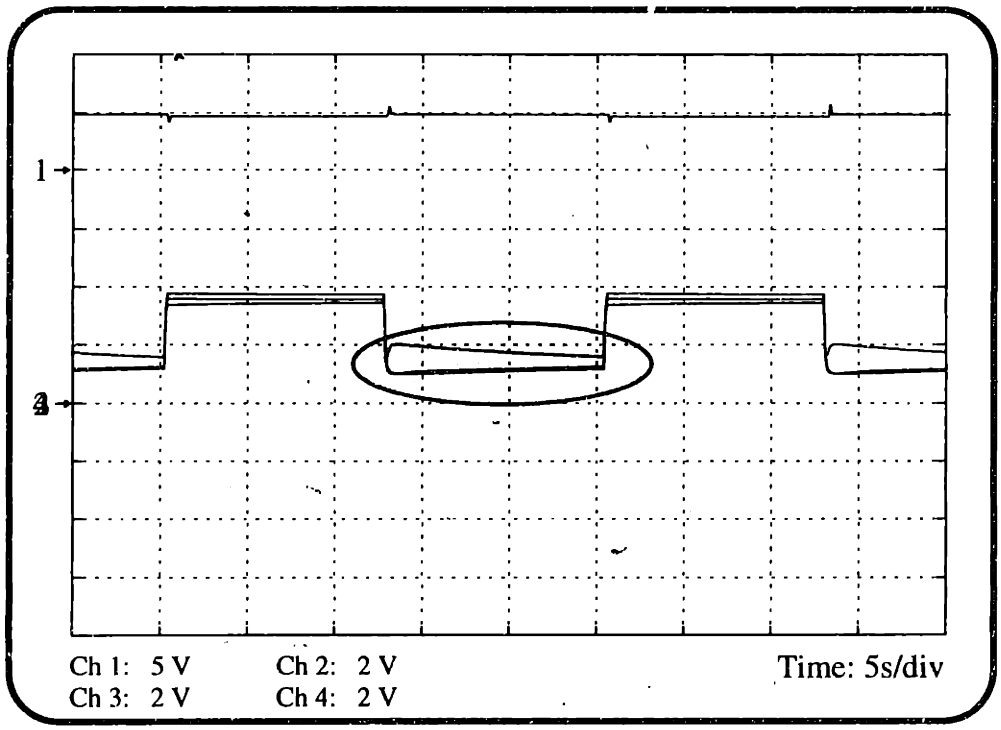


Figure C.6: Current sharing dynamics 75% to 25% to 75%.

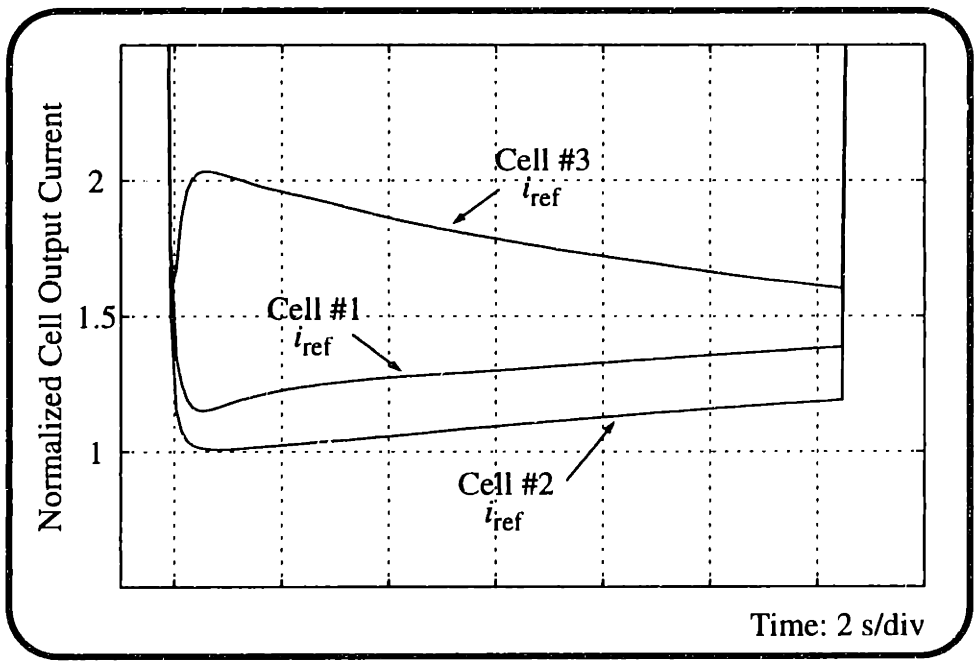


Figure C.7: Illustrates an expanded view of the shaded region in Fig. C.6, showing the transient behavior of the current-sharing controller for 75% to 25% load step.

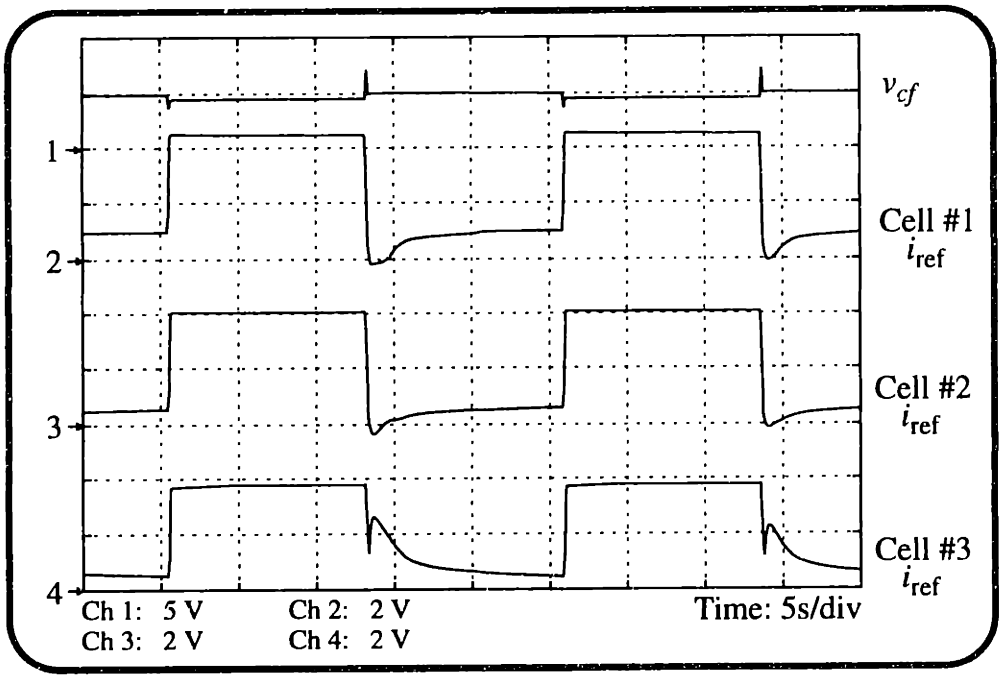


Figure C.8: Current sharing dynamics: 10% to 90% load step test.

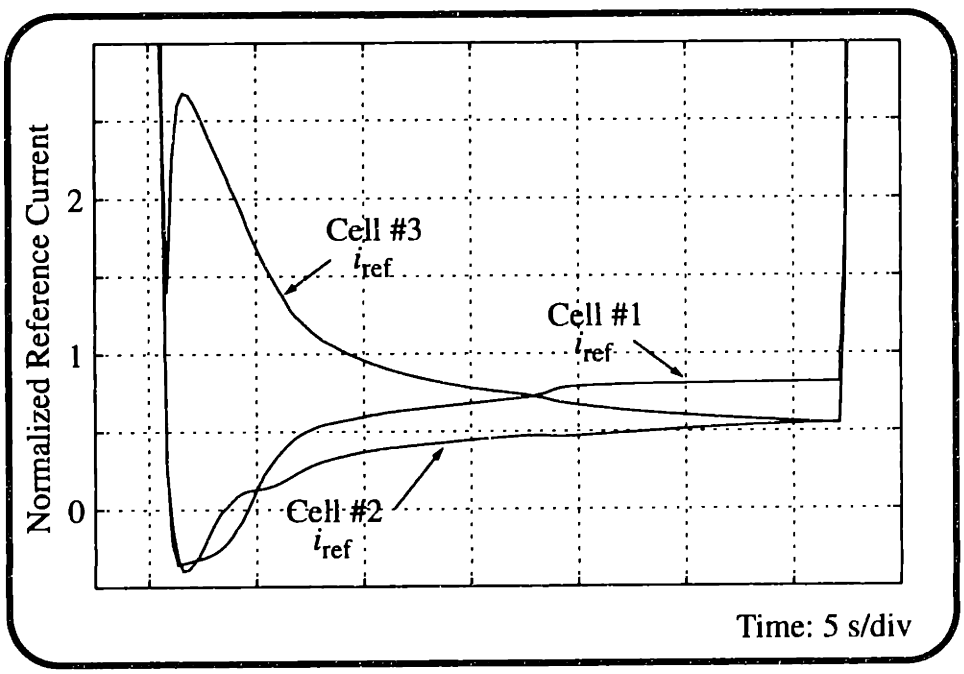


Figure C.9: Current sharing dynamics: 10% to 90% load step test illustrating the cells taking action when a large load imbalance is introduced during the 90% to 10% load step transition.