Near Junction Thermal Management of GaN HEMTs via Wafer Bonding

by Robert M. Radway

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Abstract

Gallium nitride (GaN)-based high electron mobility transistors (HEMTs) offer excellent performance in power conversion and high frequency power amplification. However, device self-heating limits reliable output power to 1/8th of reported maximums. Device-level thermal management is therefore critical for reliable high power operation. This thesis proposes and examines wafer bonded GaN-on-SiC HEMTs as a thermally efficient alternative to growth structures. This work first compares the thermal properties of this novel structure to the state-of-the-art. It then develops suitable wafer bonding techniques to fabricate this structure. In addition, the bonded interface thermal conductivity is measured via time domain thermoreflectance. The results of these measurements are analyzed to determine the thermal performance of the structure. In all, this thesis shows that the proposed bonded technology is a promising method for the fabrication of the next generation of GaN HEMTs. These devices are expected to perform at a level equivalent to GaN-on-diamond devices, although further process development is needed to achieve high bonding yields.

Thesis Supervisor: Tomás Palacios
Title: Professor

Acknowledgments

I would like to acknowledge first and foremost my supervisor, Professor Tomás Palacios, for the insightful discussions we have had, as well as the wonderful opportunity to join his group and pursue this work. Tomás and the rest of his group make excellent colleagues and have made my Master's work very enjoyable.

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Chapter 1

Introduction

Gallium nitride (GaN) is a wide bandgap semiconductor that has many uses in optical, radio, and power applications. GaN high electron mobility transistors (HEMTs) are commonly found in high-frequency power amplifiers (PAs) [1]. These amplifiers are a critical component in many broadcasting technologies including cellular communications and radar applications. GaN HEMTs are a particularly promising technology due to increased power density and efficiency over existing technologies such as silicon (Si) laterally diffused metal oxide semiconductor (LDMOS) transistors, silicon carbide (SiC) metal semiconductor field effect transistors (MESFETs), and gallium arsenide (GaAs) HEMTs [1,2]. This increased power density arises from the excellent material properties of GaN. Particularly, GaN has a wide bandgap, high breakdown field, high electron mobility, excellent charge density, and high thermal conductivity [1,3].

Due to these desirable characteristics, GaN HEMTs and GaN transistors in general have undergone significant academic and commercial development. GaN HEMTs have been reported with a maximum output power of 40 W/mm under active device cooling [4]. Large devices are also possible; CREE, Inc. has produced compact, high-power amplifiers with 521W of output and a record 72.4% efficiency at 3.55GHz [5]. The wide bandgap properties of GaN HEMTs make them particularly well suited for

reliable high temperature operation such as internal engine sensors [6]. GaN HEMTs have also been integrated in monolithic microwave integrated circuits (MMICs) for use in the L thru W-bands. With power outputs of 11W at 34 GHz, these devices meet the high level requirements of next generation radar and communication systems [7].

Overall, GaN HEMT technology has numerous benefits and uses in high power and high frequency regimes. However, commercially available technologies typically operate at reduced power densities of 3-6 W/mm [1,8]. This reduced power density is needed to mitigate device self-heating and thereby improve operational reliability and device lifetime. With the high voltages and high power densities required for efficient, scalable PAs, GaN HEMTs must be engineered with improved thermal dissipation to achieve reliable, widely commercial devices [9]. While both package-level and device level thermal engineering are required, the growth constraints of GaN present several opportunities to improve near junction thermal resistance through novel structures [8].

1.1 GaN HEMTs

The structure of a generic GaN HEMT is shown Figure 1-1. The exact buffer layers depend greatly upon the substrate used, however, for all HEMTs the principal of operation is the same. Sufficient buffer material is needed to achieve a high quality GaN material with a smooth epitaxial surface (see subsection 1.1.1). After this is achieved, an $Al_xGa_{1-x}N$ layer (usually with concentration $x = 0.28$) is grown [1, 2].

Due to a difference in the spontaneous polarization fields of GaN and AlGaN, a two dimensional electron gas (2DEG) forms at the GaN/AlGaN material interface. While both N-face and Ga-face polarities can introduce a 2DEG, the Ga-face has been much more widely investigated [1, 2, 10]. The formation of the 2DEG is shown in the band diagram in Figure 1-1; the mode of operation is apparent as an applied gate voltage can lift the well above the Fermi level thereby turning off the device. However,

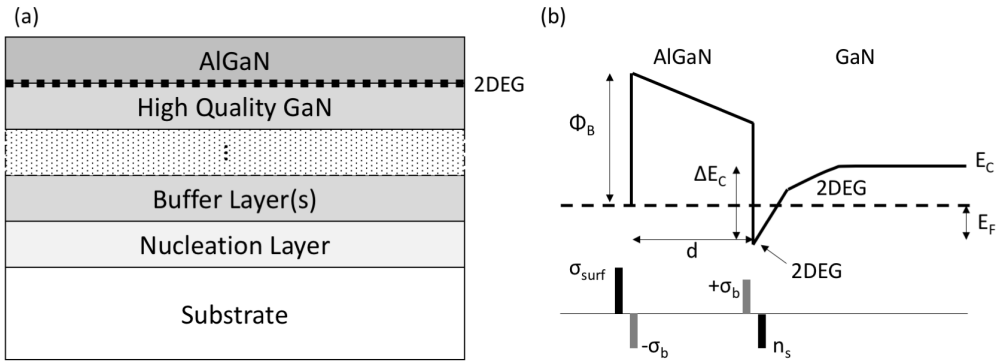

Figure 1-1: (a) Epitaxial structure for a generic HEMT (b) Band diagram around a AlGaN/GaN heterojunction

this means that GaN HEMTs are always-on – a key limitation for use in digital logic. While GaN HEMTs operate much as other HEMT devices, the major benefit is that no doping is needed to populate the 2DEG (as is required for GaAs HEMTs) [11]. Another benefit is that the native 2DEG carrier concentration is extremely high, greater than $1 \times 10^{13} cm^{-2}$ [10], and high quality devices achieve channel mobilities of over $2000 cm^2/Vs$ [1]. The level of confinement and concentration in the 2DEG can be tuned with the alloy concentration, as well as the thickness of the GaN and AlGaN layers. This dependence is described in Equation 1.1, where n_s is the 2DEG charge density, σ_B is the AlGaN polarity induced charge, Φ_B is the gate metal work function, and ΔE_c is the polarity induced band bending.

$$n_s = \frac{\sigma_B}{e} - (\frac{e\epsilon_0}{de^2})[\Phi_B + E_F(n_s) - \Delta E_c] \tag{1.1}$$

To contact the 2DEG, ohmic contacts are formed through multi-layer metal depositions (usually a Ti/Ni/Al/Au stack). The wafer then undergoes a high temperature anneal to diffuse the contact metal through to the 2DEG. A Ni/Au Schottky gate is then deposited to control the channel. Usually, devices are isolated via a mesa etch. There are several other contact and gate methodologies: those that allow CMOS-

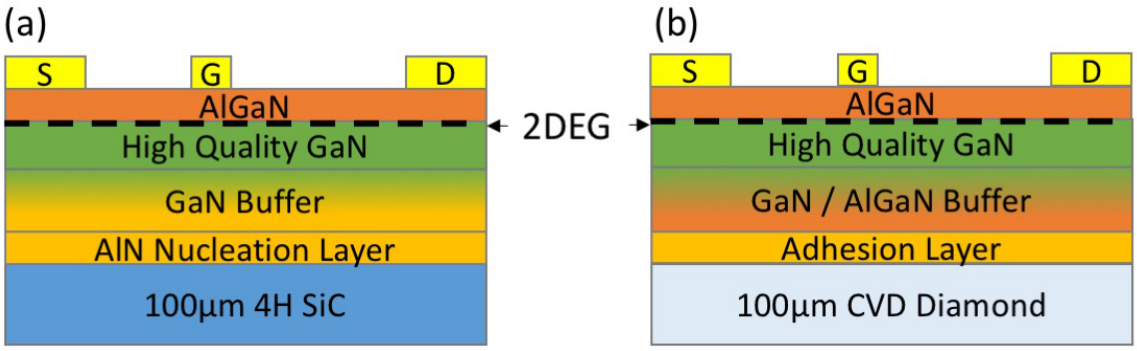

Figure 1-2: Epitaxial structure for (a) GaN-on-SiC and (b) GaN-on-Diamond HEMTs

compatible processing [12], the addition of Si_xN passivation [13, 14], and the use of field plates for increased breakdown voltage [4, 15, 16]. However, these complexities and the circuit design of PAs are beyond the scope of this work, see [1, 2, 17, 18] for in-depth review. Subsequently, this thesis will only consider GaN HEMTs of the basic design outlined above and depicted in Figure 1-1. It is also key to note that GaN RF PAs are usually found in a multi-fingered configuration [1]. This is important to consider in device simulation, and it is this type of mask layout which will be simulated in chapter 3.

While GaN-on-SiC HEMTs have been the dominant structure in commercial applications, there is a growing interest in GaN-on-diamond devices [19–24]. The high thermal conductivity of synthetic diamond improves heat dissipation in the device, allowing for higher power density circuits [25]. Such a GaN-on-diamond structure is shown in Figure 1-2. There are two main processes for fabricating such a device. The first starts with a GaN-on-Si epitaxial wafer; a carrier wafer is then attached to the top surface via an adhesive. The original substrate is etched away, an adhesion interlayer is deposited, and a CVD diamond substrate is subsequently bonded to this interlayer [19, 23]. The second method instead directly grows CVD diamond on the exposed GaN surface (after a nucleation layer is deposited) [21, 22]. In general, GaN-on-diamond devices are state-of-the-art in terms of power density and thermal

performance; however, they are significantly more expensive due to increased materials and processing costs [23,26]. These devices will be used as the point of comparison in chapter 3, as they achieve the highest published thermal performance.

1.1.1 Gallium Nitride Growth

There has been significant work on hydride vapor phase epitaxy (HVPE), ammonothermal, and Na-flux methods for bulk GaN crystal growth. However, these methods are still not able to produce the large-area, uniform wafers needed for scalable GaN device fabrication [27–31]. Thus, GaN and associated AlGaN are generally grown heteroepitaxially via molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD) [1, 32, 33]. Three main substrates are used in commercial production: sapphire, Si, and SiC. In addition, AlN, ZnO2, bulk GaN and graphene have all been used as substrates for heteroepitaxial growth [34]. With many of these substrates, a nucleation layer is needed to induce growth of the GaN crystal. Although excellent end material quality is achieved for the GaN, AlGaN, and AlN layers via these growth methods [35,36], dislocation densities are still considerable. Commercial wafers are usually found to be in the $10^7 cm^{-2}$ to $10^9 cm^{-2}$ densities [37]. Nonetheless, both techniques grow the smooth and abrupt interfaces needed for high quality 2DEG formation with high electron mobility [1].

There are three main causes for these high dislocation densities. The first is that during the initial stages of GaN growth, grains form but eventually coalesce into a uniform material layer. This seeding effect can introduce lattice dislocations at the grain boundaries [38]. While AlN nucleation layers are needed to form these grains, they also induce threading dislocations in the nucleation layer itself [39]. In addition, growth methods suffer from complications due to lattice mismatch and thermal mismatch between the GaN and the substate. As Table 1.1 shows, there is significant lattice mismatch for GaN-on-Si, as well as smaller mismatch for GaN-on-

	GaN	Si	SiC (4H)	Sapphire
Lattice Structure [40]:	Wurzite	FCC	Wurzite	Trigonal
a (Å) [40]:	3.190	5.431	3.073	4.785
c (Å) [40]:	5.125		10.053	12.991

Table 1.1: Crystal parameters of materials in GaN growth

	GaN	Si	SiC (4H)	Sapphire
$CTE\ \alpha_a(K^{-1})$ [40]:	$5.59 * 10^{-6}$	$2.6 * 10^{-6}$	$4.1 * 10^{-6}$	$6.66 * 10^{-6}$
$CTE\ \alpha_c(K^{-1})$ [40]:	$2.17 * 10^{-6}$		$3.7 * 10^{-6}$	$5 * 10^{-6}$

Table 1.2: Coefficients of thermal expansion (CTE) of materials in GaN growth at room temperature

sapphire and GaN-on-SiC.

Mismatched thermal expansion rates between GaN and the substrate can introduce significant dislocations and even cracking [41]. As GaN is grown at high temperature of over 1000°C, during cool down the different materials compress at significantly different rates. Often the stresses induced by this effect are on the order of $10^9 Pa$ [41]. With a GaN-on-Si wafer, and an appropriate low temperature AlN nucleation layer, the GaN stress can be reduced to 0.15GPa [42]. Other stress relieving methods include graded AlGaN layers [43]. Often, a thick buffer layer of GaN is grown to reduce the dislocation density. This buffer is stress relieving, and reduces the effects of CTE mismatch [44, 45]. For GaN-on-Si epitaxies, a short-period superlattice (SPSL) of GaN and AlN layers is typically used to reduce dislocation counts as repeated material changes induce recombination of threading and spiral dislocation [46]. As with pure GaN buffers, a thick layer of material must be used to mitigate CTE and lattice mismatch.

In all, growing GaN for HEMT fabrication presents several problems with material quality, namely, a high dislocation density. While this dislocation density can be reduced to achieve a high-quality 2DEG, this requires thick nucleation and buffer layers, often of a total thickness greater than $2\mu m$. These buffer layers can consist

of many different material layers and are highly complex, as is the case with SPSLs for GaN-on-Si. The thermal problems associated with these structures are the main focus of this thesis.

1.2 Scope and Outline of Thesis

The overall theme of this thesis is to explore and develop novel GaN HEMT designs fabricated via wafer bonding. By bonding and transferring a GaN HEMT structure to a SiC substrate, the thermal conductivity from the heat source to sink is expected to improve by the elimination of thermally resistive buffer layers and thermal boundaries. This thesis evaluates structures first via simulation, and then by fabrication and measurement using time-domain thermal reflectance. This work required the development of novel wafer bonding techniques, as well as back etch processing to appropriately access the bonded device layers.

Chapter 1 gives background on GaN HEMTs, their operation, and the problems faced during growth. This serves as motivation for the development of novel structures fabricated via wafer bonding to overcome these problems.

Chapter 2 presents a discussion of heat generation and dissipation in GaN devices. Subsequently, the chapter reviews research into several thermal effects present in multilayered structures, and expands upon the impact these effects can have in GaN devices.

Chapter 3 proposes novel wafer bonded GaN HEMTs. First, this chapter explores state-of-the-art GaN HEMT structures grown on silicon carbide and transferred to diamond, to determine their dominant thermal resistances. The chapter then describes two novel wafer bonded designs, and compares their thermal performance to existing state-of-the-art technologies. The chapter concludes with a design optimization of the most promising structure, and gives a performance analysis of this design.

Chapter 4 develops the required GaN-SiC wafer bonding techniques to realize the structures described in Chapter 3. The chapter goes over the many experiments conducted to determine appropriate surface activation techniques needed to bond GaN and SiC. The chapter expounds upon the conditions needed to achieve reliable bonding, particularly the development of specialized high-temperature bonding fixtures and stress-relieving channels needed to achieve covalent Ga-C bonds at 1000°C. The chapter also gives an analysis of the further refinements needed to improve bond yield.

Chapter 5 describes the experiments taken to measure the thermal boundary resistance of the GaN/SiC bonded interface. The chapter begins with a discussion of the back etch processes developed to prepare the samples. A time domain thermoreflectance sensitivity analysis of the structure is then performed. The chapter continues on to describe the samples measured and outlines the results and significance of those measurements.

Chapter 6 includes a discussion of the results of this thesis, the potential impact of those results, and future work to be undertaken to expand these results.

Chapter 2

Thermal Properties of GaN Devices

This chapter will discuss heat generation and dissipation in GaN HEMTs. Particular emphasis will be given to the various thermal effects which reduce thermal conductivity in the structures and thereby limit high power performance.

2.1 Heat Generation in GaN Devices

There have been several analysis of heat generation in GaN HEMTs [47–49]. As with other HEMTs the primary concern with active devices is Joule heating. While GaN HEMTs are not typically run in a steady state, most thermal analyses have looked at the steady state temperature rise in a device [50]. While understanding behavior during use is a primary goal, there is significant complexity in simulating a pulsed device and analyzing transient self-heating. As [50] found, multiple time constants are needed to describe the transient heating behavior. This thesis will therefore focus on steady state temperature rise, as this provides an single statistic, namely max device temperature, when comparing multiple device architectures. This approach has been used in several structural comparisons, particularly those concerned with GaN-on-diamond devices [20, 51, 52]. Using an Arrhenius equation to model failure rate, the device temperature rise also gives insight into device lifetime and reliability.

The exact thermal modeling methods used in this work will be described in further detail in chapter 3.

Beyond the general modeling approach, a pressing concern is the shape and size of the heat source. While a multi-fingered HEMT of common size and configuration is modeled in chapter 3, there is still much uncertainty to the actual shape of the heat source in the literature [48]. While previous thermal analyses of devices have often assumed that the heat source is uniform and comparable to the gate length [47], several electro-thermal modeling works have found conflicting results. While there does seem to be agreement that the size of the heat source in devices is dependent upon both bias conditions and gate length, one work modeled the heat source as greater than the gate length [53], while another has modeled the heat source as lesser [54]. In [48], the author goes into great detail discussing and analyzing the assumptions of uniformity of the heat source. In summary, it is clear that heat generation is highly localized in the channel on the drain side of the gate. However, there are many factors that determine the exact level of dispersion of heat generation, which cannot be determined without full 3D electro-thermal models. While understanding these effects is important, this thesis aims to compare structures on a basis of temperature rise and reliability. Using a uniform heat source in the 2DEG, with an appropriate flux based on the dissipated power density, should provide an appropriate comparison. This conclusion was also reached by the developers of the analytical methods used in this work [55, 56], as well as other thermal studies comparing GaN technologies [20].

2.2 Heat Dissipation in Multilayered Epitaxies

While the thermal conductivity in any given bulk material is usually well characterized, there are several important effects which must be considered when looking at the thermal conductivities of thin, multilayered epitaxies. The first is the bulk con-

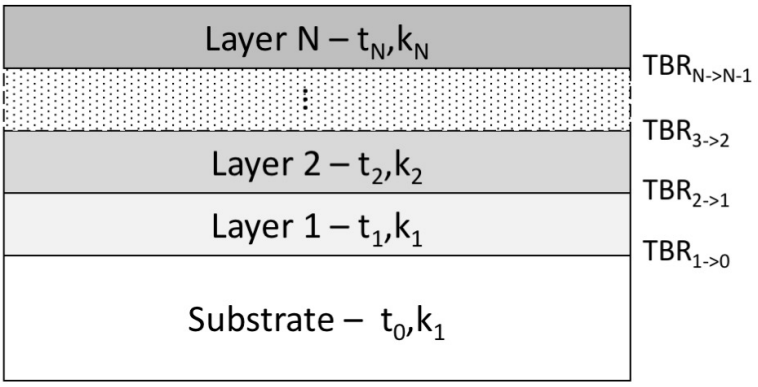

Figure 2-1: Generic epitaxial structure for thermal evaluation

ductivity of a given material, which is highly depended on concentration (in alloyed cases) as well as material quality [37, 57]. The second effect one must consider is the reduction of the material conductivities from their bulk values due to phonon mean free path suppression. This effect is critical in thin films, as the conductivities can be reduced by up to 90 percent from bulk values [58]. Finally, one must consider the interface effects due to change in material, namely the thermal boundary created therein. [59] These boundaries have a fixed resistance due to the material, and as such, they can significantly increase the overall resistance of an epitaxy. Figure 2-1 depicts a generic multilayered epitaxial structure which will be the basis for further analysis in this work. The next sections will go into detail on the thermal effects described in general above and depicted in the figure.

2.2.1 Thermal Conductivity of Materials

Table 2.1, lists the bulk thermal conductivities of the materials that are considered in this work. It is important to note the relative magnitudes of these conductivities. As is expected, stiffer, harder materials (such as SiC and diamond) both have extremely high conductivity. The ranges of values given are usually due to material quality, these uncertainties will be discussed in detail below.

While the thermal conductivity of bulk GaN has been calculated from first prin-

GaN	$Al_{0.27}Ga_{0.73}N$	AlN	Si
150 [37] - 240 [60, 61]	30 [57]	285 [40]	130 [40]

SiC (4H)	Sapphire	CVD Diamond
420 [40]	27 [40]	1200 [62] - 2000 [26]

Table 2.1: Thermal Conductivities of Materials in GaN HEMTs (W/mK).

cipals [60] there is still uncertainty about the thermal conductivity of any given GaN film, mainly due to the variable dislocation density introduced during growth. Dislocations cause diffuse scattering of heat carrying phonons, thereby impeding heat flow through the epitaxy. With several efforts taken to measure and calculate this effect [37, 61], the consensus seems that for most GaN epitaxies with a dislocation density around $10^8 cm^{-2} - 10^9 cm^{-2}$, a bulk conductivity near 150 W/mK is appropriate.

Along with dislocation density, it is key to consider the alloy concentration for $Al_xGa_{1-x}N$ layers. As the concentration x, in $Al_xGa_{1-x}N$, goes from 0 to 1 there is initially a sharp drop off in thermal conductivity, reaching as low as 14 W/mK at a 20 percent Al concentration [63]. As the Al concentration increases, there is a sharp rise around 0.9 approaching the bulk value for AlN [57]. Thus, for $Al_{0.27}Ga_{0.73}N$ layers in GaN HEMTs, a bulk thermal conductivity of 16-20 W/mK is appropriate [56, 63]. Besides alloyed impurities, doped impurities also reduce the thermal conductivity of materials. In many GaN epitaxies, C-GaN is often used as a stress relieving buffer layer, however, at a concentration of $10^{17} to 10^{18}$ the thermal conductivity of GaN is reduced to 86 W/mK [64]. Therefore, when modeling a given epitaxial structure, one must closely analyze the exact material composition and quality, as this can significantly impact the total thermal conductivity.

2.2.2 Phonon Mean Free Path Suppression

Beyond material makeup and quality, phonon mean free path (MFP) suppression can significantly reduce the thermal conductivity of an epitaxial layer. The thermal conductivity of a material can be described as an accumulation function, where phonons of a given MFP contribute to the total thermal conductivity based on the material's MFP distribution [58]. This accumulation function is described in Equation 2.1, where L is the cumulative maximum MFP, σ is the phonon polarization, $C_\sigma(l)dl$ is the volumetric heat capacity for a phonon of a given MFP, $v(l)$ is the phonon speed, and l is the MFP of the phonon.

$$k_{accum}(L) = \frac{1}{3}\sum_{\sigma}\int_0^L C_\sigma(l)v(l)l dl \tag{2.1}$$

A material's MFP distribution is critical to understanding the thermal conductivity. There have been several works to determine the MFP distributions in a variety of materials [65–67], including GaN and AlN [58]. With phonon MFPs $\leq 1\mu m$ the accumulated conductivity is $\leq 50\%$ of bulk. At phonon MFPs $\leq 30nm$ the accumulated conductivity is $\leq 10\%$ of bulk [58]. When considering a thin epitaxial layer, the MFP distribution is changed from the bulk – interfacial scattering limits phonon mean free paths to below the material thickness. A thin epitaxial layer there has a reduced conductivity compared to the bulk value. Using the accumulated conductivity directly (even though this is measured in bulk material without interfacial scattering) is an appropriate model. Measured values of the thermal conductivity in Si membranes map well to expected conductivities from these MFP calculations [68]. Although this does not seem well known, particularly for nm-thin layers, this will be the approach used in this work.

This effect becomes quite important in designing thermally optimal structures. When considering a single material layer, reducing the material thickness would seem

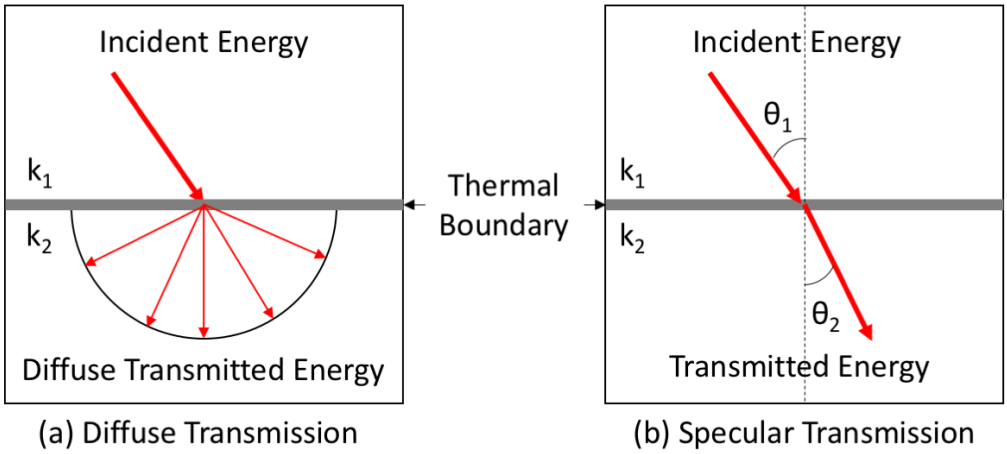

Figure 2-2: Thermal boundary resistance (a) diffuse mismatch model (b) acoustic mismatch model

to always reduce the total thermal resistance. However, considering the impact of MFP suppression, a non-zero thermally optimal thickness exists. This is a critical effect which is ignored in thermal modeling and in design of GaN epitaxial structures [20, 56]. The rest of this thesis will use the measured accumulation functions found in [58], and further details on the values used can be found in chapter 3.

2.2.3 Thermal Boundary Conductivity

In addition to material interfaces suppressing the phonon MFP distribution, they also create an impedance to heat flow across the interface [69]. As two materials will have different phonon density of states, there is imperfect transmission of a heat carrying phonon across the interface. This effect has been well studied [52, 59, 69, 70], and there are several analytical and experimental techniques used to calculate and measure the thermal boundary resistance between two materials. Two of the main models are depicted in Figure 2-2. Per its name, the diffuse mismatch model assumes that heat transport through the boundary is via diffuse scattering of incident heat carrying phonons. For the diffuse mismatch model the thermal boundary resistance is found to be [59]:

$$R_b = \left[\frac{k_b^4 \pi^2}{30\hbar^3} \left(\sum_j c_{1,j}^{-2} \right) \alpha_{1->2} \right]^{-1} T_2^{-3} \tag{2.2}$$

Where $c_{i,j}$ is the phonon speed in the i'th material with the j'th polarity and

$$\alpha_{1->2} = \frac{\sum_j c_{2,j}^{-2}}{\sum_j c_{1,j}^{-2} + \sum_j c_{2,j}^{-2}} \tag{2.3}$$

is the thermal transmission coefficient between material 1 and 2.

The acoustic mismatch model assumes that each incident phonon transports heat across the boundary in a specular nature. As such, the transmission coefficient of a given phonon across the boundary is dependent upon its polarization and orientation to the interface. However, this model quickly becomes untenable unless simplifications are made. Under the assumptions of uniformity of phonon speeds in all directions, the transmission coefficient becomes [71]:

$$\alpha_{1->2} = \frac{4 \frac{\rho_2 c_2 cos\theta_2}{\rho_1 c_1 cos\theta_1}}{(\frac{\rho_2 c_2}{\rho_1 c_1} + \frac{cos\theta_2}{cos\theta_1})^2} \tag{2.4}$$

where ρ_i is the density, θ_i is the angle of incidence, and c_i is the isotropic phonon speed in the i'th material. And the thermal boundary resistance is then [59]:

$$R_b = \left[\frac{k_b^4 \pi^2}{15\hbar^3} \left(\frac{\int_0^{sin^{-1}(c_1/c_2)} \alpha_{1->2} sin\theta cos\theta d\theta}{c_1^2} \right) \right]^{-1} T_2^{-3} \tag{2.5}$$

While measured TBRs for GaN HEMT interfaces are readily found, measured values include additional resistance due to interface layers. For example, the $TBR_{GaN->diamond}$ in [52] includes the resistance of both AlN nucleation layers and the adhesive bonding layer. With novel structures, on must therefore use the theoretical models described above. However, measured values are still useful in determining a bound on a given TBR. While the theoretical models, neither is particularly accurate. However, the DMM is much more tenable to calculate and has been shown to give a good lower

Source	GaN	$Al_{0.3}Ga_{0.7}N$	AlN	Si	SiC (4H)	CVD Diamond
GaN		0.5	1.34	0.8	1.31	2.7
$Al_{0.3}Ga_{0.7}N$	0.69		1.34			
AlN				0.32	0.42	0.5

Table 2.2: TBR (m^2K/GW) for boundaries in GaN HEMTs calculated from DMM

	SiC (4H)	CVD Diamond
GaN (Growth)	4-5 [51]	12-50 [72],17-41 [62]
GaN (Bonded)		38-108 [70]

Table 2.3: TBR (m^2K/GW) for GaN-substrate interfaces measured in literature (Growth signifies either substrate or GaN)

bound on the TBR at high temperatures [59, 69]. Table 2.2 gives DMM calculated values and Table 2.3 lists measured interfaces in the literature.

2.2.4 Thermal Conductivities of Buffer Layers

When looking at complicated buffer layers, the many effects outlined above result in a large reduction in the total conductivity of the layers. Many GaN HEMTs, particularly those grown on Si, use short period superlattices of alternating AlN and GaN layers as a method to reduce strain and eliminate dislocations [46, 73]. Thus, there are many fixed thermal boundary resistances, along with reduced conductivities in each of the SPSL layers due to MFP suppression. Thus, when considering such a buffer, it can be modeled as a single layer, with a net thermal resistance of a lower conductivity material. This is depicted in Figure 2-3 While the exact structure can impact the conductivity significantly, a SPSL of 53nm of GaN and 4nm AlN has an effective conductivity roughly 1/10th of the bulk value of GaN at 17 W/mK [73]. This reduced conductivity buffer layer is quite resistive, and due to it's thickness the SPSL will dominate the total thermal resistance. As such, GaN-on-Si structures are rendered so thermally inefficient that they are not considered in this work.

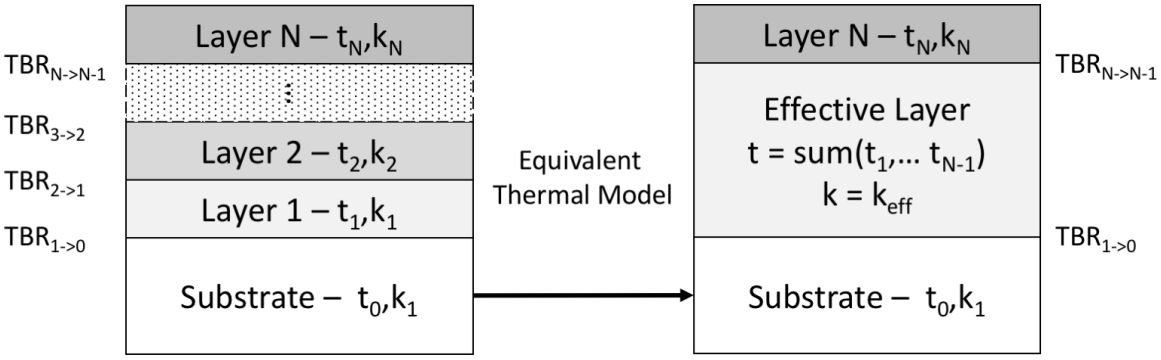

Figure 2-3: Equivalent thermal models for a multi-layered structure

Chapter 3

Thermally Efficient GaN-on-SiC Epitaxies via Wafer Bonding

GaN HEMTs are a critical technology for high power RF amplification and many other uses. However, there are a variety of thermal problems in GaN HEMTs related to the limitations of growth technology. When analyzing such a device, there are also a variety of ways to thermally simulate a given structure. This chapter will discuss the specifics of the thermal modeling technique that was used to compare the thermal performance of several GaN HEMT technologies. This technique is a computationally efficient analytical method, which provides the same accuracy as numerical physics simulations. Subsequent sections focus on a given GaN design and components of the total thermal resistance are analyzed for each device. A novel GaN HEMT design is then presented, discussed, and analyzed; its thermal performance and reliability are compared to existing state-of-the-art HEMTs.

3.1 Thermal Modeling of GaN Devices

Finite element methods (FEM) are often used in simulating GaN devices [20, 48, 49, 69, 74]. While FEM give consistent and convergent results, the high aspect ratio of

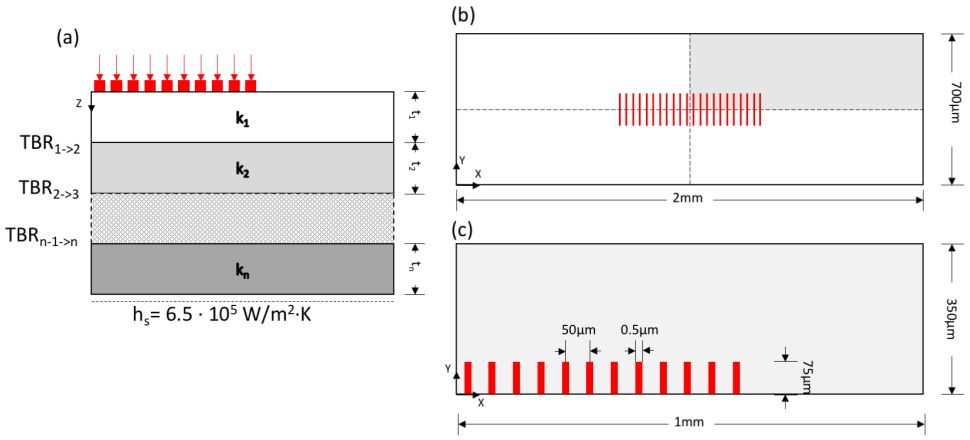

Figure 3-1: Generic epitaxial thermal structure (a) side view (b) top view (c) symmetrically reduced top view

gate length as compared to chip structure can make meshing difficult. There have been several recent works to develop analytical methods to calculating temperature rise in a device [55,56]. This is the approach that is used in this work. This analytical method is highly accurate as compared to FEM, but requires a fraction of the runtime and calculation setup [56]. The author of this method was generous enough to share his Matlab framework, which was used as a foundation for the simulations described below.

3.1.1 Analytical Method

The generic thermal structure to be modeled is shown in Figure 3-1. A 22 fingered HEMT mask is assumed, consistent with GaN PAs [56]. While the exact relation between gate length and heat source is still not fully understood, as this is a cross-design comparison, the exact choice is not that significant. A 0.5 μm heat source was chosen for this simulation. This choice is consistent with several studies on thermal generation in GaN HEMTs [48, 54, 75]. Due to the exploitable symmetry, we can reduce our calculations to only consider a single quadrant, with symmetric (i.e. floating) boundary conditions at the edges. The total size of the die, along with the gate pitch and width is shown in Figure 3-1. Instead of choosing a specific bias

point, the power dissipation itself was chosen. Full electro-thermal simulations are needed to determine the exact heat dissipation for a given bias. As this work is simply focused on thermal performance of a given structure, the power dissipation is really all that matters. A dissipation of 5 W/mm was assumed; this implies a corresponding areal heat flux of $10^{10} W/m^2$ for the sources. Beyond the layout, the technical details of the method are given in Appendix A. As was mentioned in section 2.2, when modeling a given structure, one must consider the interface conductivity between two materials. However, in some cases, the measured values found in literature are for an "effective" TBR which includes the resistance of an interlayer [51, 52, 70]. This does not present a problem for this method, as an interlayer can be dropped from the wafer stack and modeled solely by the effective TBR between the surrounding materials. As described in , determining the thermal conductivity of a thin layer is a non-trivial problem. The model used generally accepted value for the thermal conductivities; for thin GaN layers, phonon mean free path suppression was calculated as in [58].

3.2 Performance of Current GaN Technologies

Now that the modeling method has been described, it will be used to compare standard and state-of-the-art GaN HEMT structures. Particular focus is given on the impact of near junction resistances such as the GaN-substrate thermal interface.

3.2.1 GaN-on-SiC

While GaN-on-Si devices are important for GaN integration into Si-based technologies, they have substantial thermal and structural limitations. GaN-on-SiC devices are the preferred design for high powered use (particularly for the simulated MMIC structures). This is due to their increased thermal efficiency resulting from SiC's high thermal conductivity. A GaN-on-SiC HEMT structure is shown in Figure 3-2

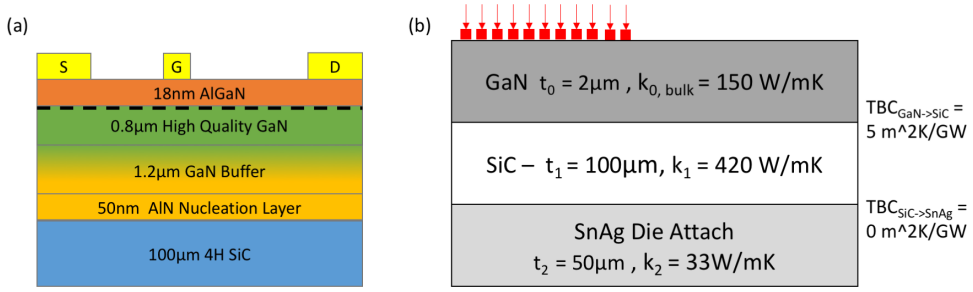

Figure 3-2: Standard GaN-on-SiC HEMT (a) epitaxial structure (b) modeled structure with parameters listed.

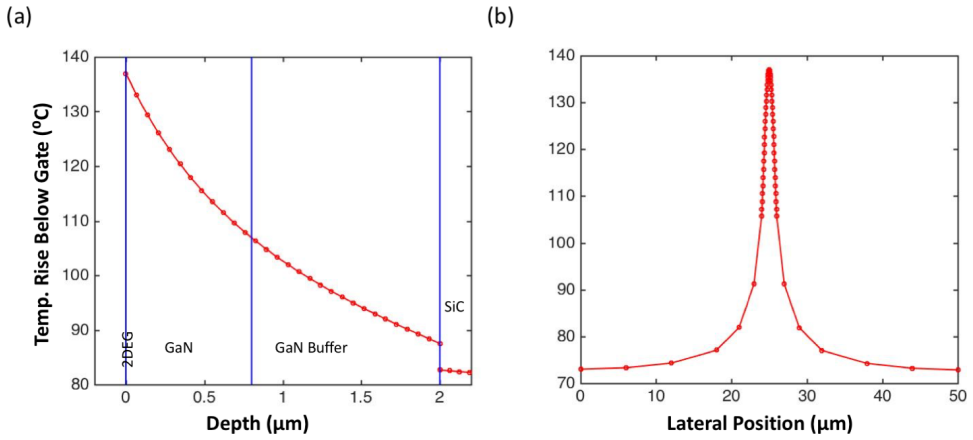

Figure 3-3: Standard GaN-on-SiC HEMT simulated temperature rise at 5W/mm power dissipation (a) under central heat source (b) on surface around central heat source

along with the simplifications made for simulation. Using the values as listed in the figure, the simulated temperature rise is shown in Figure 3-3. Note that the value of 150W/mK given for GaN is the assumed bulk conductivity. For a 2 μm thick GaN layer, this implies a suppressed conductivity of roughly 90 W/mK. The best growth TBR reported is assumed for the GaN-SiC, at $0.2 GW/m^2K$ [51].

The max temperature rise in this device is 136.9C. Between devices, the surface cools to 72.86C. Within a micron of the heat source, the temperature drops over 31.2C. The contributions to the total thermal resistance are shown in Table 3.1. In general, heat is highly concentrated under the sources. The package makes up a considerable contribution to the total thermal resistance, as the relatively low GaN/SiC TBR and SiC substrate resistance are not a significant percentage of the total. The GaN

Region:	GaN Epi	GaN/SiC TBR	Substrate	Package
Percent of Total:	35.9%	3.7%	2.1%	58.3 %

Table 3.1: GaN-on-SiC thermal resistance

material is a significant portion of the near junction thermal resistance; ignoring the package, the GaN material is over 85% of the thermal resistance on the chip. As there is not much that can be done to reduce the growth TBR of GaN-SiC (the AlN nucleation layer is critical for GaN wetting and high quality growth), the simplest optimization would be to thin the GaN layer. If phonon MFP suppression is ignored, then simply reducing the GaN buffer thickness to close to 0 is optimal. However, when one models the MFP suppressed thermal conductivity, a true minimum arises at roughly 200nm. This relation is shown in Figure 3-4. If GaN growth could be terminated at that thickness, this would decrease the near junction thermal resistance by 15%. However, the high dislocation density would reduce 2DEG conductivity, and the net electrical performance would be much lower. However, if there were a way to reduce the GaN thickness without other performance loss, then the overall performance can be significantly improved.

3.2.2 GaN-on-Diamond

As discussed in section 1.1, GaN-on-diamond technologies are seen as a promising method to improve thermal performance. Diamond substrates have the highest bulk thermal conductivity measured at up to 2000 W/mK theoretical maximum [62, 70], Therefore, replacing the SiC substrate in a GaN HEMT with diamond should yield an significant thermal performance improvement due to improved thermal spreading. As was discussed, both regrowth and wafer bonding methods have been approached. Each yields a different quality of GaN-diamond interface, as well as different diamond quality. For high quality growth interfaces, the diamond quality ranges from 800 to

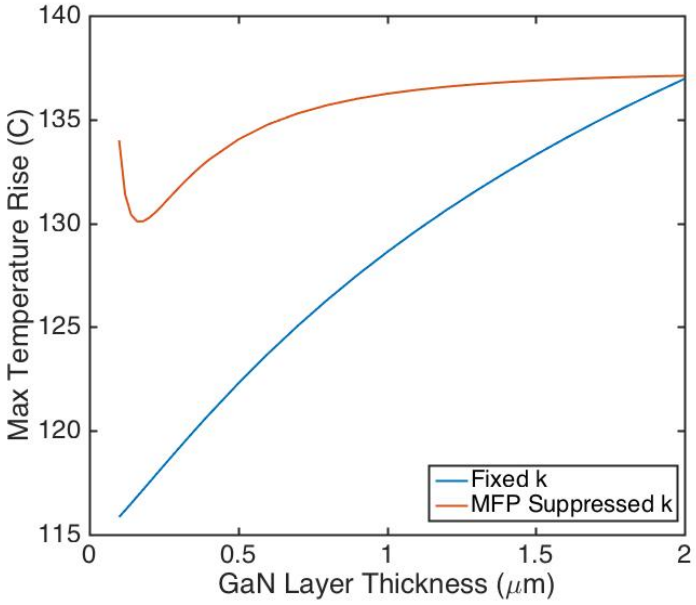

Figure 3-4: Max temperature rise in GaN-on-SiC HEMTs as a function of GaN buffer thickness

1600 W/mK realized conductivity, with TBRs reliably around 20 m^2K/GW [62, 72]. Better diamond substrates (up to 1800 W/mK) are used in bonded devices, but the thermal interface is significantly worse, ranging from 36 to 100 m^2K/GW [70]. While the fabrication methods are different, both yield essential the same structure, the only thermal difference being in the GaN-diamond TBR and the conductivity of the diamond. A GaN-on-diamond HEMT structure is shown in Figure 3-5.When evaluating these structures, the question of what TBRs and conductivities to use is a pressing one. As a best case scenario, the simulation use the maximal conductivity achieved for diamond wafers (1800 W/mK), and the lowest TBR measured for GaN-diamond interfaces (20 m^2K/GW). The more reasonable scenario assumed a 50 m^2K/GW TBR and a 1200 W/mK diamond conductivity. These scenarios are shown in Figure 3-6.

Both GaN-on-diamond devices offer a significant performance improvement over GaN-on-SiC. The max temperature rises are 131.1C and 113.0C for the average and best case scenarios. These devices have an even more compressed temperature dis-

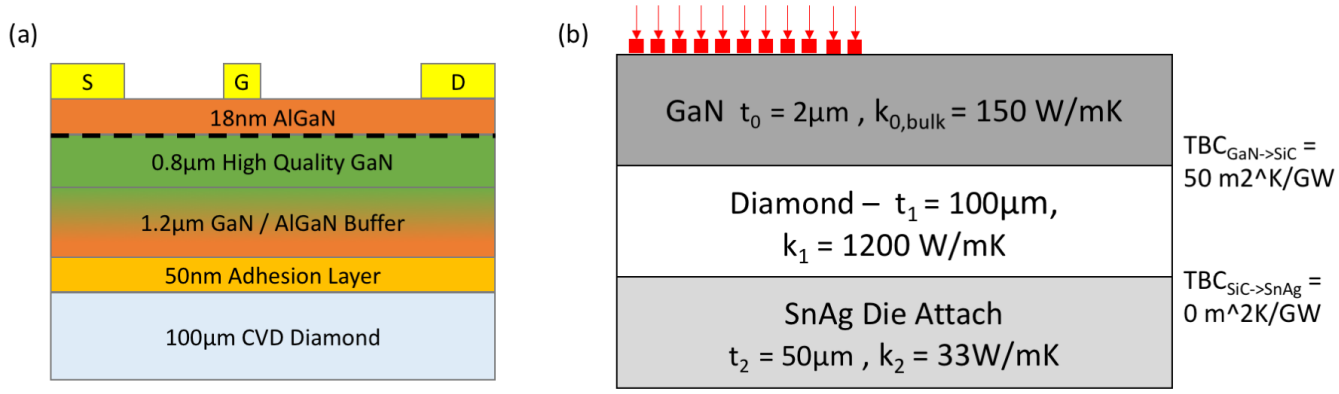

Figure 3-5: Standard GaN-on-Diamond HEMT epitaxial structure with model parameters listed.

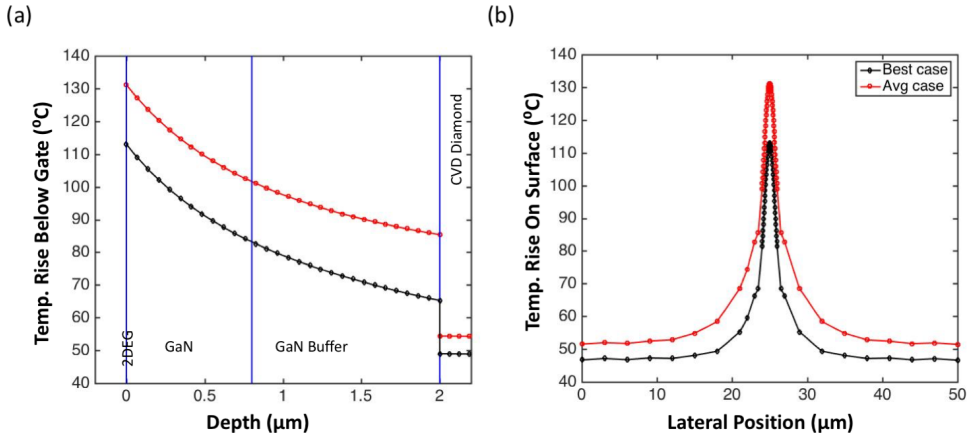

Figure 3-6: Standard GaN-on-Diamond HEMT simulated temperature rise at 5W/mm power dissipation (a) under central heat source (b) on surface around central heat source

tribution on the surface, with the minimum temperature significantly lower at 55.3C and 48.7C respectively. Again the main source of thermal resistance is in the GaN material and the GaN-diamond TBR. However, the TBR is now an extremely significant percentage of the total thermal resistance in the average case. Table 3.2 shows the distribution in the two cases. In general, GaN-on-diamond is an interface limited technology. If good material interfaces can be achieved (approaching the 3 m^2k/GW DMM value) then these devices will have exemplary performance. However, for current technology, while still outperforming SiC, they do not achieve their full potential.

Region:	GaN Epi	GaN/SiC TBR	Substrate	Package
Best Case:	51.1%	5.6%	3.9%	39.4 %
Avg Case:	35.6%	23.7%	4.8%	35.9%

Table 3.2: GaN-on-Diamond thermal resistance

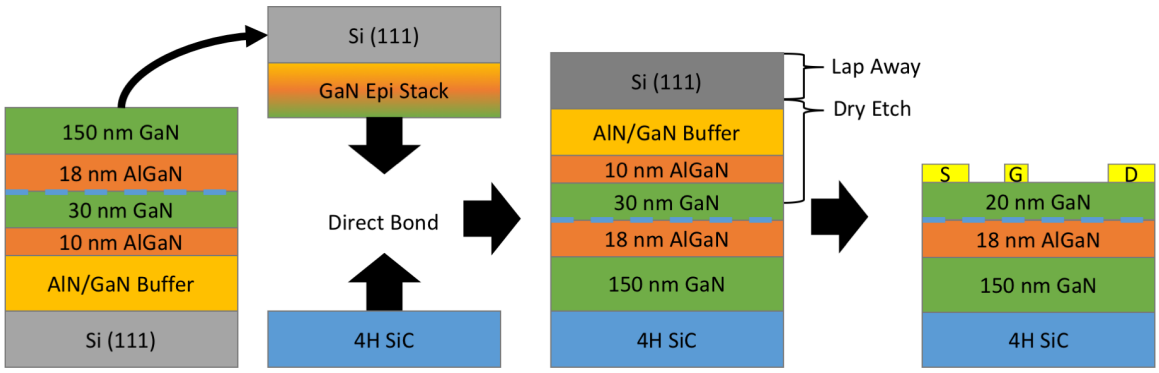

Figure 3-7: Wafer bonding process for GaN-on-SiC HEMTs.

3.3 GaN-on-SiC via Wafer Bonding

After comparing the common GaN HEMT epitaxial structures there are several key conclusions. Reducing the thermally resistive buffer layers and having thermally conductive interfaces from GaN to the substrate is key. While both GaN-on-SiC and GaN-on-diamond HEMTs achieve some of these design ideals, neither is optimal, mainly due to the high TBRs because of nucleation and inter layers, as well as the thick GaN buffer layers needed for high material quality at the 2DEG. The goal is then to somehow achieve this reduced thickness, keep the GaN-substrate TBR low, and also maintain material quality and electrical performance. The subsequent sections propose and analyze two possible wafer bonding processes to achieve these goals. The main idea is to take a GaN-on-Si wafer, bond it to a new SiC substrate. Once that is done, the original Si and buffer material can be removed, thus leaving a thin, high quality transistor layer in good thermal contact with the carbide substrate. This will achieve two things. First, by direct bonding the GaN to the SiC, the thermal boundary resistance should be improved over growth interfaces. Second, the exact

thickness of GaN material can be chosen to optimize the thermal performance of the structure.

3.3.1 GaN-SiC Direct Bonded Structure

Beginning with a GaN-on-Si epitaxially grown HEMT, an additional 25nm - 200nm thick GaN cap is grown. This cap will become the new bonding buffer material. This wafer is then direct bonded to an SiC wafer, yielding the structure shown in Figure 3-7. The original Si substrate is the etched away, along with the nucleation and buffer layers, yielding from top down a thin GaN layer, with an AlGaN layer below that, and a final GaN buffer layer bonded to a SiC substrate. The total final thickness is $\leq$300nm of GaN material, and the GaN HEMT can be N-face contacted. Similar devices have been fabricated previously, although a Si substrate wafer was used, and a thick interlayer of SiO2 was used to achieve bonding [76]. The benefits of this bonded GaN-SiC structure are a highly conductive substrate, a reduced TBR between GaN and SiC (due to lack of interlayer in the bonding and the high quality of the bonded GaN surface) and most importantly, a reduced GaN buffer layer. Unfortunately, the AlGaN layer cannot be ignored, as it is now between the 2DEG (heat source) and the substrate (heat sink). The key to fabricating such a structure is developing appropriate wafer bonding techniques to create high quality interfaces. Back etch techniques are needed to remove the original Si substrate and GaN buffer layers. Although explored previously [76], there are still additional complications that could arise in such processing.

3.3.2 GaN-on-SiC Double-Bonded Structure

A second wafer bonding structure could be fabricated in a manner similar to the GaN-on-diamond bonded structures. While using a more complicated process, this results in a simpler structure. A Si handle is attached to GaN-on-Si wafer surface via

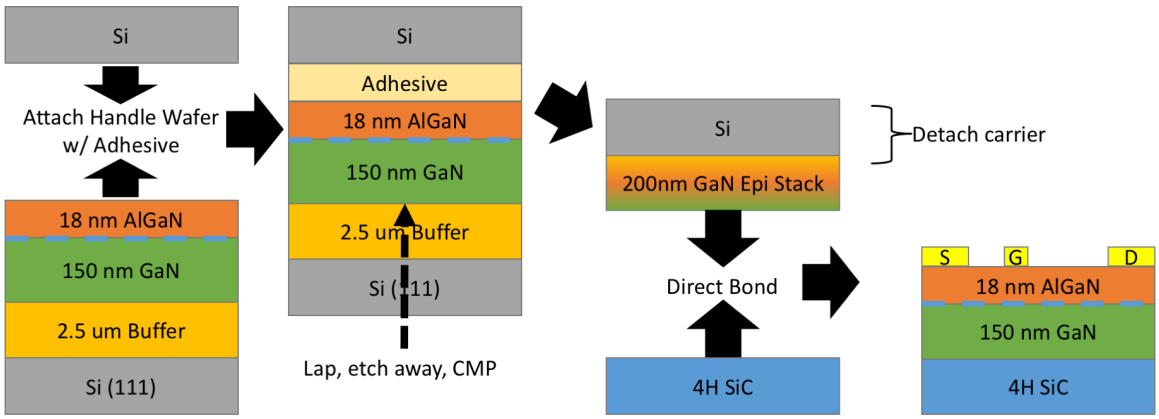

Figure 3-8: Double wafer bonding process for GaN-on-SiC HEMTs.

an adhesive. Subsequently, the original substrate is removed and the GaN material is mechanically polished down till the GaN thickness is 300nm. After chemical mechanical polishing (CMP) this surface to achieve a smooth interface, this wafer is direct bonded to a polished SiC wafer. The carrier is then removed and devices can be fabricated on the surface. This structure has the benefit of both being a standard Ga-face HEMT, with a high conductivity substrate, while removing substantial amounts of resistive buffer material. The key to fabricating such a structure is the CMP of the GaN material in order to bond the GaN and SiC. This structure will not be pursued much beyond an initial evaluation of its potential, as the extra processing required is well beyond the scope of this work.

3.4 Performance of Wafer Bonded GaN-on-SiC HEMT

The key consideration when simulating this structure is the GaN-SiC TBR. While several values have been measured, they all include the resistance of AlN nucleation layer (see section 2.2). Thus, a analytical model must be used. From a DMM calculation, the value is $1.31 m^2K/GW$. This value presents a strong upper bound on the interfacial conductivity, and the measured TBRs including nucleation layer present a good lower bound at $4-5 m^2K/GW$ [52]. For the TBR of the AlGaN/GaN interface,

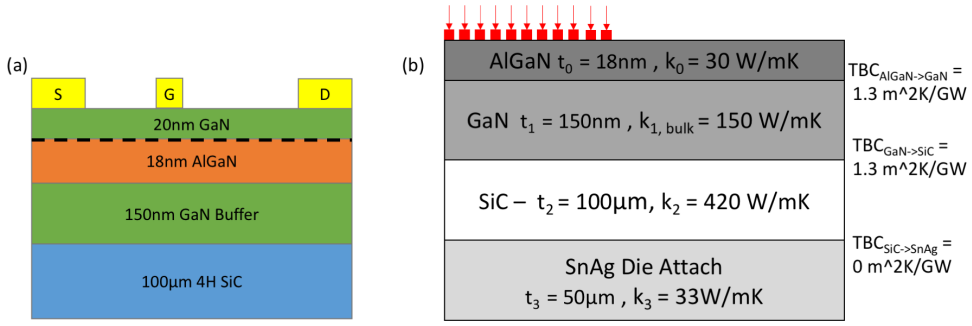

Figure 3-9: Bonded GaN-on-SiC HEMT epitaxial structure with model parameters listed.

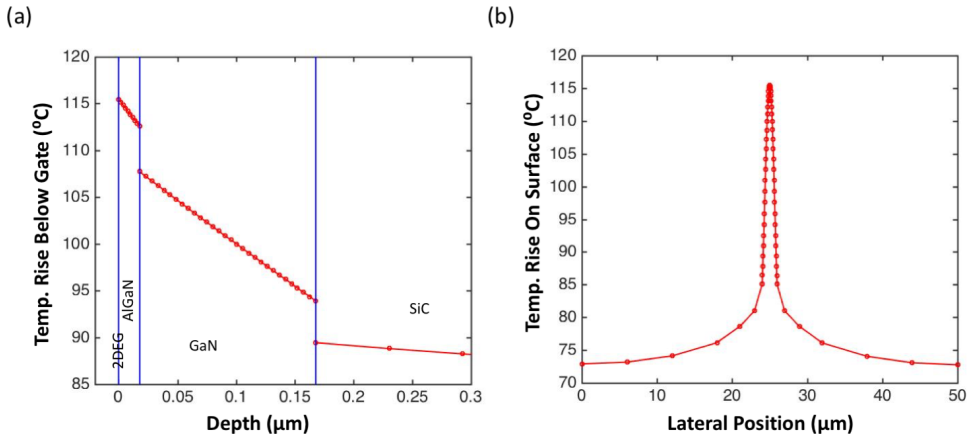

Figure 3-10: Bonded GaN-on-SiC HEMT simulated temperature rise at 5W/mm power dissipation (a) under central heat source (b) on surface around central heat source

we again appeal to a DMM; the value is $1m^2K/GW$ as an upper bound. Finally, for the AlGaN layers a 30 W/mK conductivity was used [57]. As will be seen in the simulations below, varying these parameters beside the GaN-SiC TBR does not significantly affect the performance of these devices.

The max temperature in this device is 115.5C, which is significantly lower than a standard GaN-on-SiC structure, as well as the GaN-on-Diamond average case. Like the standard GaN-on-SiC, the bonded HEMT has a surface temperature minimum of 72.7C, with a similar peak sharpness. As is seen in Figure 3-10, the reduction in the GaN buffer significantly makes up for the increased resistance of the AlGaN layer when compared with GaN-on-diamond. The relative contributions to the total resistance

Region:	GaN Epi	GaN/SiC TBR	Substrate	Package
	18.6%	3.9%	18.4%	59.1 %

Table 3.3: Bonded GaN-on-SiC thermal resistance

are shown in Table 3.4. Now, the near junction thermal resistance is approaching its minimum. The SiC substrate is roughly 45% of the near junction, and the GaN epitaxy is the other 45% with the TBR making up the rest. Effectively, the only way to begin making more efficient devices is the second proposed bonding method.

3.4.1 Variations of Model Assumptions

As mentioned above, there are several assumptions made in modeling this structure, the key being the assumed TBR of a bonded GaN-SiC interface. If these assumptions are shifted, then several trends can be observed. Figure 3-11 shows the general trends, as well as the points of comparison evaluated in this structure. We see under all assumptions except for perfect interfacial thermal contact, the bonded GaN structure underperforms the best case diamond system. However, for an average diamond GaN HEMT, the bonded GaN-SiC structure has a lower temperature rise, assuming the TBR is no worse than the growth case. This is highly promising, as we expect a lower bonded TBR versus growth due to the lack of an interlayer. While not shown for clarity, varying the AlGaN or GaN conductivities by 10% did not have a significant effect on thermal performance. The key conclusions from this analysis are that the performance of this structure is highly dependent upon the thermal boundary at the bonded interface. While the structure pretty always outperforms a standard GaN-on-SiC HEMT, its performance relative to GaN-on-diamond devices is dependent upon the bond interface quality.

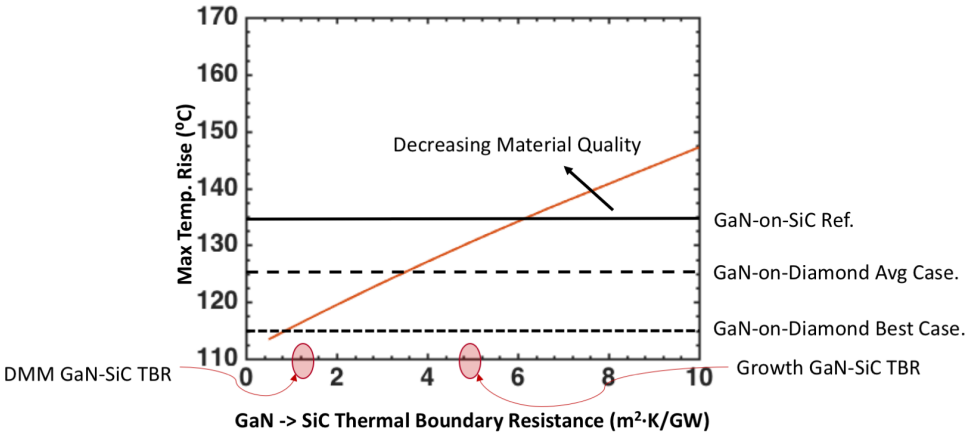

Figure 3-11: Max temperature rise in bonded GaN-on-SiC HEMTs as a function of GaN/SiC Thermal Boundary Conductivity

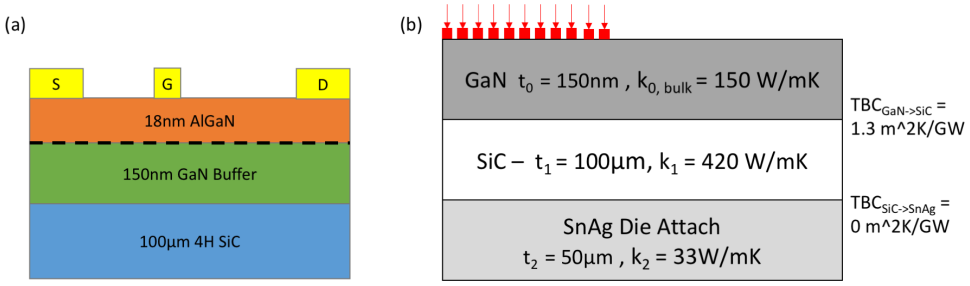

Figure 3-12: Double bonded GaN-on-SiC HEMT epitaxial structure with model parameters listed.

3.4.2 Thermal Performance of Double Bonded Structure

In the double bonded GaN HEMT, the end structure is extremely simple. Effectively, this can achieve the optimal minimum found when considering variable GaN-on-SiC thicknesses. As the optimized thickness was 200nm, this value was chose for the final layer thickness. As with the above bonding case, the DMM was assumed for the GaN-SiC TBR yielding 1.3 m^2K/GW. Mean free path suppression was likewise assumed; the end model of this structure can be seen in Figure 3-12. The simulated temperature rise is shown in Figure 3-13. As to be expected, this is an ideally efficient GaN-on-SiC HEMT. The max temperature rise was only 107.9C, with a very low percentage of the thermal resistance found in the near junction. In a case like this, the only improvements which can be made are switching to higher conductivity materials.

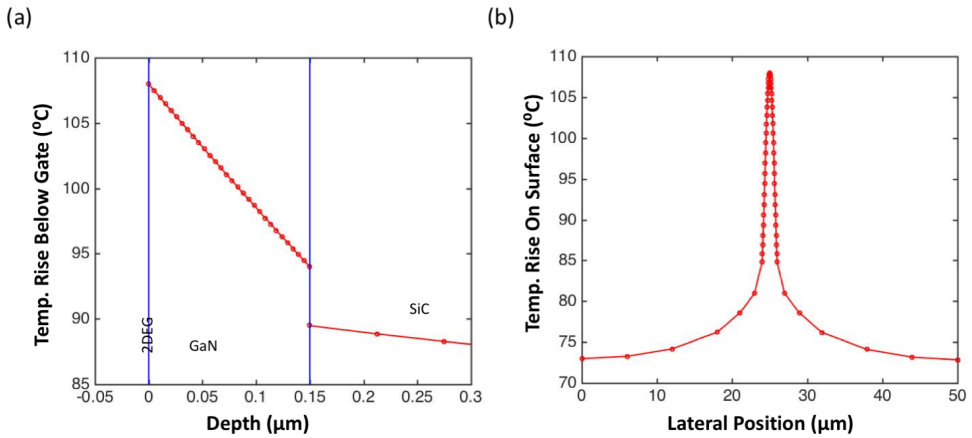

Figure 3-13: Double bonded GaN-on-SiC HEMT simulated temperature rise at 5W/mm power dissipation (a) under central heat source (b) on surface around central heat source

Region:	GaN Epi	GaN/SiC TBR	Substrate	Package
	12.7%	4.2%	7.9%	75.0 %

Table 3.4: Double bonded GaN-on-SiC thermal resistance

3.5 Summary of Performance Characteristics

The following table summarizes the performance of the various devices considered in the above simulations. For each device, the power dissipation was modified until the max surface temperature reached 250C. The goal of this was to gain an understanding of the increase in power density achievable with these structural changes. Using an Arrhenius equation to model the mean time to failure, the growth GaN-on-SiC was used as a reference, and the energy of activation was assumed to be 1.0 Ev [77]. As one can see, the bonded Gan-SiC HEMT significantly outperforms average GaN-on-diamond, and GaN-on-SiC devices. Under best case assumptions for GaN-on-diamond, the proposed structure is only marginally behind.

Structure:	TBR (m^2K/GW)	Max Temp. Rise (C)
GaN-on-SiC:	5	136.9
GaN-on-Diamond (best):	20	113.0
GaN-on-Diamond (avg):	50	126.3
Bonded GaN-on-SiC:	1.3	115.5
2x Bonded GaN-on-SiC:	1.3	107.3
	Max Power Density (W/mm)	Reliability Increase
GaN-on-SiC: 8.7	ref.	
GaN-on-Diamond (best):	11.2	335.2%
GaN-on-Diamond (avg):	9.9	93.5%
Bonded GaN-on-SiC:	11.1	292.7%
2x Bonded GaN-on-SiC:	11.6	405.2%

Table 3.5: Makeup of total GaN-on-diamond thermal resistance

3.6 Discussion

The goal of these simulations was to explore novel structures and use the results to optimize their design. The wafer bonded structures proposed in this chapter have high promise in therms of expected performance improvements. This suggests that experimental work should be undergone to realize and test these devices. The points of comparison were difficult to choose, as there are several variations of devices which have similar structures, but different thermal performance. The aim was to simply these aspects away, and create a more standard model as a point of comparison. To that end, the best values reported in the literature were used, and so the analysis is in the times with the literature. With the GaN-on-diamond case, while the idea TBR and diamond conductivities yielded the best device, to date no one has realized a 20 m^2K/GW or lower TBR while also achieving a 1800 W/mK diamond substrate. Part of this lies in the trade off between growth and bonding. With a bonding approach, a high quality substrate can be obtained, however the need for interlayers reduces the thermal boundary conductivity [52]. On the other hand, while optimizing the growth interface yields a lower TBR, the diamond quality is sacrificed, as grain formation during growth significantly reduces thermal conductivity [62]. In all, the proposed

method yields improved results because it should have both a high quality substrate and a high interface conductivity. The approach taken herein has been novel in that several thermal effects are modeled in addition to the basic structure and bulk conductivities. Overall, this analysis has yielded fruitful results, and is hoped to inform future device design and optimization works.

Chapter 4

GaN - SiC Wafer Bonding Technology

A directly bonded GaN HEMT is of high promise due to expected thermal improvement over current designs. However, there is very little in the literature on bonding GaN and SiC. GaN and SiC had been previously bonded in a ultra-high vacuum, high temperature bonding system [78]. With this method, the authors were able to reliably bond a GaN layer grown on Si to a pristine 6H SiC wafer. As with any bonding process, rigorous cleaning was a necessity, and the system was highly temperature dependent; reliable bonding only occurred at 1000C. While this method is promising, there are several key differences between the proposed structure and that previously bonded. The first is that the substrate was 6H polytype SiC versus a 4H polytype. While both are wurtzite crystal structure, the 6H polytype has different periodicity and hexagonal symmetry. They also both have slight differences in their coefficients of thermal expansion; most notably, the 4H thermal expansion is more anisotropic than that of 6H SiC [79]. Secondly, the proposed epitaxial structure is significantly different than that previously bonded. Compared to the 0.5 μm GaN layer with a 100nm AlN nucleation layer reported, the 3 μm structure proposed consists of many AlN, GaN, and AlGaN layers. Each of these materials have a different thermal expansion and the internal stresses are drastically different.

Besides direct bonding, there are several examples of interlayer bonding of GaN to other substrates [23, 52, 76, 80, 81]. While the actual interlayers are not often published, particularly for the GaN-on-diamond technologies, they are only a few standard materials. When bonding to Si substrates, SiO_2 is a well known adhesive interlayer, particularly when coated in the form of HSQ [76, 82]. In addition to SiO_2, Al_2O_3, also been used in interlayer bonding [83]. SiN_x is used in GaN-on-diamond wafers where the diamond is deposited [72]; it is therefore a likely bonding interlayer as well. While metal-metal bonding and eutectic bonding are both well characterized and optimized processes, the high temperature annealing required for the creation of ohmic contacts render these techniques unusable. Overall, interlayer bonding is a promising candidate for this GaN-SiC system if simple bonding is required. However, with any interlayer comes an increased GaN-SiC TBR; the goal of this work is the development of thermally efficient devices. These indirect methods will therefore be ignored, and a direct bonding method is subsequently developed.

4.1 Principals of GaN-SiC Bonding

When considering bonding novel materials, the exact chemistry of the bond is important to analyze. While GaN can be grown in both N and Ga polarizations, the growth of the proposed epitaxial structure limits the bonding surface to the Ga face. However, SiC is a bulk substrate which can polished on either the Si or C faces. While the Si-face epi-ready polish is common for GaN growth, C-face polished SiC is also available. In order to determine what orientation will bond optimally, it is important to analyze the bond strength of various configurations. First, consider the most basic method of determining bond strength: electronegativity difference. Table 4.1 gives the electronegativity differences for the four possible bonding configurations of GaN and SiC. The difference is greatest for Si-N bonds, explaining the Si-face used for Ga-

	Ga	N
Si	0.2	1.2
C	0.9	0.5

Table 4.1: Electronegativity differences for the possible GaN-SiC bond configurations

polar GaN growth. As the GaN-on-Si wafers are the same polarity, this leaves Ga-Si and Ga-C as possible bonding configurations. The Ga-C electronegativity difference of 0.9 is substantially greater than the 0.2 value of Ga-Si. This suggests that bonding the Ga-faced GaN to the C-face of the SiC wafer is optimal.

Besides electronegativity differences, there have also been *ab initio* calculations to determine GaN-SiC growth interfaces in the four possible configurations [84]. While these simulations were considering 6H SiC as the growth substrate, the results can help give some understanding of a GaN-SiC(4H) interface. In a 4H polytype, the chemical bonding in the Ga-C and Ga-Si cases is expected to be as depicted in Figure 4-1. For the Ga-C bond, the bond distance was calculate to be 1.99 versus 2.43 for the Ga-Si bond. The Ga-C bond and Ga-Si bond have an energy difference of -1.07 eV per atom suggesting a more strongly covalent bond in the Ga-C case [84]. Thus, from both a polarity perspective and and energy perspective, bonding Ga-faced GaN to C-faced SiC seems the most likely to succeed. This was also the conclusion reached in [78], and their results found that the C face bonding more readily. This is easy to understand as this bonding configuration yields the least disruption to the molecular structure of the terminating materials. The interfaces should therefore be more of a melded crystal structure without a large amorphous region.

Besides the actual end bond, the process of achieving that bond must be considered. There are two main bonding processes: hydrophilic or hydrophobic. For example, two wafers of Si can be bonded both with and without surface hydroxylation. In the first case (hydrophilic bonding), the wafers are wet cleaned via RCA, then rinsed. The surfaces are then placed in contact, and then pressure and tempera-

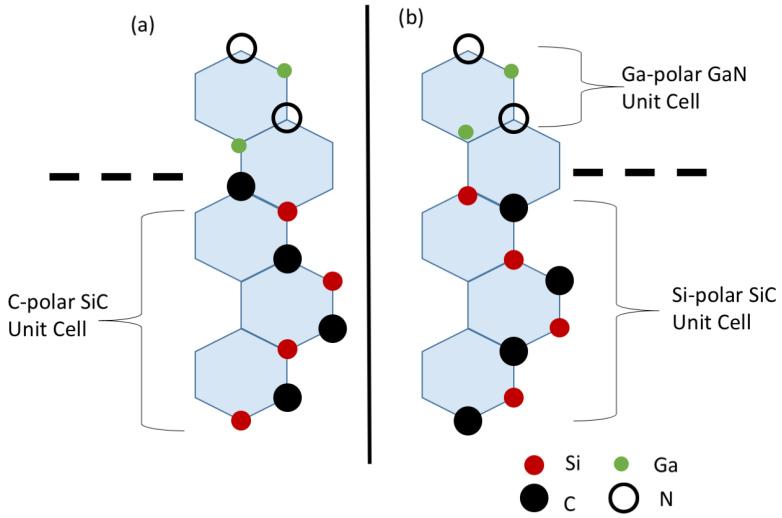

Figure 4-1: Pictorial representation of the bonding chemistry

ture are applied. The Si-OH OH-Si surfaces are polymerized to form Si-O-Si bridges, with the excess H_2O migrating away. In the second case, a long HF dip is done after the RCA clean, the wafers are blown dry and the bare surfaces immediately put into contact. This strips the hydroxide from the surface and instead forms Si-H surfaces. During bonding, the H_+ atoms form H_2 and migrate out of the wafer – a straight Si-Si bond is formed [85]. In general, both methods offer high bond strength, and the Si-O-Si bridges can turn into Si-Si bonds at high enough anneal temperatures. As the end goal is a high quality thermal interface, and high temperatures bondings were previously used, it seems that hydrophilic bonding methods are appropriate.

4.2 Thermal Mismatch During Bonding

While it seems likely that the GaN and SiC can form strong covalent bonds, the mechanics of maintaining that bond over a large area are less clear. While GaN and SiC do not suffer significant lattice mismatch (approximately 3.4 %), the thermal mismatch is a much larger issue. Assume that the coefficients of thermal expansion for both GaN and SiC remain constant from 300 K to 1300 K (this is simplifying assumption as both GaN and SiC have increasing coefficients with temperature [79,

86]). Consider a 1 x 1 cm square piece of each material. Then the free expansion of the materials from 300 K to 1300 K is:

$$\delta l_{GaN} \geq (5.59 \times 10^{-6} m/mK) \cdot (1 \times 10^{-2} m) \cdot (1000K) = 5.6 \times 10^{-5} m = 56\mu m \quad (4.1)$$

$$\delta l_{SiC} \geq (4.1 \times 10^{-6} m/mK) \cdot (1 \times 10^{-2} m) \cdot (1000K) = 4.1 \times 10^{-5} m = 41\mu m \quad (4.2)$$

Thus, as the SiC shrinks less on cool down, the stress on the GaN material at the interface is:

$$\sigma_{GaN} = 181GPa \cdot (41\mu m - 56\mu m)/1cm = -0.27GPa \quad (4.3)$$

This tensile stress is quite significant and is on the same order of magnitude of poorly buffered GaN epitaxies with significant cracking. While the exact value relies upon the complete integration of the expansion rate – temperature curve, GaN has a consistently higher expansion than SiC – this tensile stress will remain. Complete analysis of the structure including the Si substrate and buffer layers requires finite element analysis to accurately model. Although Si has a large CTE mismatch with both GaN and SiC, the buffer layers will help relieve stress as they do in growth cool down. It is quite possible that specialized buffer structures can be developed to improve bonding ability with further analysis of the high temperature mechanics of the structure. Overall, these thermal mismatch problems are the most significant impediment to wafer bonding with these materials.

4.3 Proposed Bonding Technique

The previously reported bonding methods form a solid starting point for process development. However, there is one major challenge to overcome, namely, the lack of a high temperature bonding system in MIT's Microsystems Technology Lab. The EV501 wafer bonding system in the lab is able to apply several thousand Newtons of force, but can only operate at up to 600C. For sustained bonding, 500C is the operational maximum. The bonder is able to maintain a vacuum of 10^{-3} torr or provide a nitrogen or forming gas atmosphere. As the reported method required 900C for direct bonding, it seems unlikely that this system will covalently bond samples. Thus, we used the wafer bonder to create initial van der Waals bonding between the GaN and SiC pieces. These weakly bonded samples can then be loaded into a high temperature diffusion furnace. This annealing will help to form covalent bonds between the Ga and C. As is discussed in section 4.6, this method did not entirely work, but only one major modification was needed to achieve a high yield process. The basic process and possible variations will now be described.

4.3.1 Step 1: Sample Cleaning

The first step to a successful bonding is to rigorously remove any surface contamination and oxidation via a wet clean. In general, these wet cleans are meant to remove any surface contamination or particulate which could impede bonding. They are also used to control surface carbon and oxygen levels, and strip any hydroxides on the surface. One key thing to note is that in general, the bonding process should occur immediately after cleaning. Control over surface chemistry is lost soon after the samples are removed from the cleans. For example, standard wafer boxes can sublime hydrocarbons which contaminate the bonding surface. Storing cleaned wafers for a prolonged time before bonding will reduce effectiveness [87].

The most suitable candidates to clean these wafers are Piranha (H_2SO_4 : H_2O_2 3:1) and standard RCA 1 & 2 (H_2O : NH_4OH : H_2O_2 5:1:1 at 80C followed by H_2O : HCl : H_2O_2 6:1:1 at 80C). The goal of this clean is to remove surface residual carbon and oxygen, so that the surfaces are either activated or -H terminated. Both Piranha and RCA have been found effective at removing surface carbons, however HF or HCl dips are required for oxygen removal on GaN [88,89]. For SiC, there is less information in the literature, however, as with GaN and Si, it is likely that Piranha or RCA followed by a HF dip will be effective at removing surface contamination and hydroxides.

4.3.2 Step 2: Surface Activation

While wet etches can be used to control the surface energy and chemistry, several bonding methods utilize some form of enhanced surface activation. The goal of these methods is to free surface states, and ablate away any contaminants. These freed electrons can then form covalent bonds with the new material. There are several ways to activate the surface of wafer, and the applicability of each method depends greatly upon the material chemistry. Several chemistries including UV/O_3, Ar, and He plasma have all been used [83,85,90–93]. These methods effectively use mechanical action to strip the surfaces of contaminants, however, they risk significant surface degradation if overused. These methods are very promising, and have been found particularly effective in heterogeneous systems.

4.3.3 Step 3: Preliminary Bonding

After surface activation, the wafers must be promptly put into contact and undergo initial bonding. This process entails the application of mechanical pressure at an elevated temperature under either vacuum or non-reactive atmosphere. With larger wafers, pressure is usually applied at the center, with flags holding the edges of the

two wafers apart. These flags are then removed and the bond is allowed to propagate to the edges, thereby reducing voiding. Voiding can result from a variety of factors, such as surface contaminants, chemical reactions, or gases trapped by the bonding front [85]. With smaller pieces, voiding effects usually result in complete bonding failure, and are less prevalent. However, for both wafers and pieces, bow and warp are significant problems in surface contact and pressure. Generally, the best remedy is to obtain flatter samples, however, increased contacting pressure doubtless helps.

4.3.4 Step 4: Bond Annealing

Once wafers are bonded, the bond quality can be significantly improved by prolonged annealing under a high temperature. This annealing increases molecular energy so that the activation energy of covalent bonding can be surmounted. While chemically strengthening, it can also cause degassing at the interface, creating interface bubbles [85]. However, in general, this step greatly increases the strength of the bond. For example, with Si-Si bonding proper annealing at 1000C+ yields an interface which is as strong as the crystalline material itself [87]. However, as discussed in section 4.2 at these high temperatures CTE mismatch can become a significant issue in heterogeneous systems. Often, this step is combined with the previous in a high temperature bonding system. In UHV bonders, there is a mechanism for applying pressure at high temperatures (such as expanding molybdenum rods) which is highly effective at bonding [94]. Attempt will be made at annealing the bonded GaN-SiC samples in a diffusion furnace, however, no mechanical strain is applied. As will be seen, this can cause significant problems with the anneal step.

4.3.5 Experimental Methodology

The general approach was as follows: first, experiment with the bond conditions, cleaning chemistries, and surface activation methods. The goal is to achieve a reliable

preliminarily bonding method for GaN and SiC pieces with strong bond quality. Then analyze the strength and characteristics of these bonds. Subsequently, determine optimal anneal temperatures and times needed to induce covalent bonding. The goal is to achieve a bonded GaN-SiC wafer which can survive subsequent processing to achieve material transfer. While this approach was successful, additional development of high temperature bonding fixtures was needed. Preliminary fixture designs were explored and tested for effectiveness.

4.4 Bonding Materials

Novasic, Inc., supplied 100nm 4H SiC wafers with C-face epi-ready polishing. These wafers were then diced into 1.5 cm x 1.5 cm pieces, although several initial experiments used hand-scribed samples. Thick resist was used to protect the bonding surfaces during this processing. The resist was not baked, to allow for easy removal. A triple solvent clean was then performed, with a 15 minute sonication in acetone to begin the clean. They where then double piranha cleaned to remove any contaminants or particulates from the dicing/scribing process. The GaN wafers were grown by Dr. Richard Molnar at MIT-Lincoln Lab. The wafers were grown via molecular beam epitaxy and are of a standard design with the slight modifications proposed in section 3.3. The exact growth structure is given in Table 4.2 and the wafers were 200 mm in diameter. The SPSL had a 49nm period and roughly 30 periods were grown; additional GaN buffer material was grown before and after the SPSL. As the SPSL was to be etched away, no Fe^{3+} ion doping was used. The GaN wafer was diced into 1.2 cm x 1.2 cm pieces, and the same surface protection and cleaning processes were applied as with the SiC pieces.

The surface roughnesses of both the GaN and the SiC were measured via AFM. A 100 μm^2 area of a GaN sample had an RMS roughness of 7.87Å. A similar measure-

Layer	Material	Thickness
Layer 6	GaN	150 nm
Layer 5	AlGaN 27%	18 nm
Layer 4	AlN	1 nm
Layer 3	GaN	30 nm
Layer 2	AlGaN 27%	10 nm
Layer 1	GaN Buffer / SPSL	2.6μm
Layer 0	AlN	240 nm
Substrate	Si(111)	1.1mm

Table 4.2: Epitaxial growth structure used in wafer bonding experiments

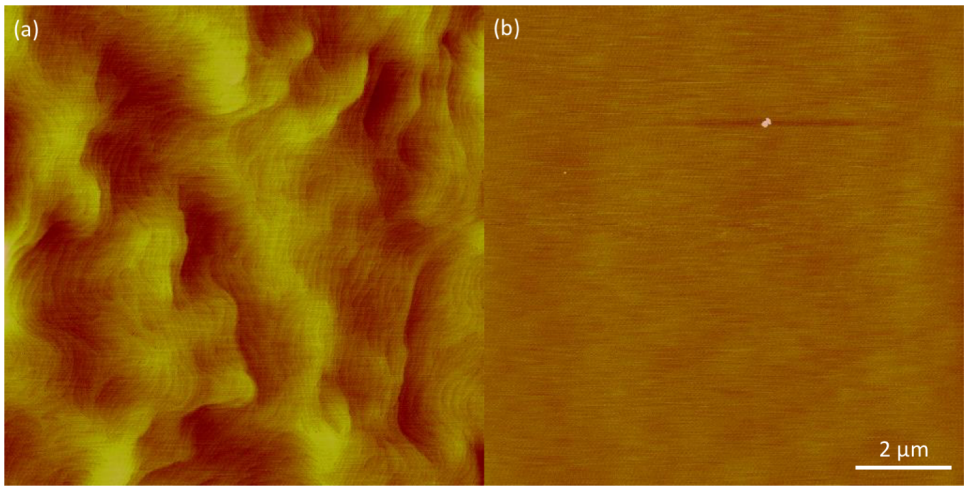

Figure 4-2: AFM measurement of (a) GaN and (b) SiC samples

ment on an SiC sample yielded a RMS roughness of 1.71Å. The surface morphologies of the wafers are shown in Figure 4-3. The SiC is very smooth, with no major patterns in its surface besides a small particle. The GaN surface exhibited the standard terraced ridge and valley morphology that is commonly found in MBE GaN. Around the edges of the wafer there were visible cracks in the epi, however, out of the 200nm wafer there was significant material with a high quality surface. Overall, these wafers should be smooth enough to bond.

Process Step	Description
1.) Sample Cleaning:	10' Piranha Clean 2' 25C DI H_2O Dip 2' 90C DI H_2O Dip 10' 10:1 $H_2O : HF$ Dip 2' 25C DI rinse N_2 blow dry
2.) Surface Activation:	Ar Plasma 24 W RF platten power, max flow, 25C
3.) Initial Bonding:	1hr at 500C $10^{-3} mtorr$, 1500 N
4:) High-T Anneal:	1hr at 1000C under N_2 using special fixture, 2hr ramp up/down

Table 4.3: Epitaxial growth structure for wafer bonding experiments

4.5 Bonding Results

First, a summary of the overall experimental results will be given. Then several key process methodologies and choices will be examined, to shed light on the various modifications needed to achieve reliable wafer bonding. The final process found to give high yield is outlined in Table 4.3 (both SiC and GaN were processed simultaneously). Note that one of the biggest factors in bonding ability was the care taken with sample handling. Any contact of wafer surfaces after the surface activation step greatly reduced bond quality and yield. When loading samples into the bonder, flexible graphite sheet was used as a pressure shim to avoid stress concentration in the corners of the pieces.

4.5.1 Cleaning & Surface Activation Experiments

The first attempts at bonding were largely unsuccessful, the results are summarized in Table 4.4. The tested chemistries and surface activations are listed on the right, along with the various bonding temperatures, times, and contact forces. All were bonded under 10^{-3} torr vacuum. Several other combinations of temperature and mechanical

Clean:	Surface Activation	400C, 15' 1000N	500C, 60' 1500N
Piranha	None	x	x
Piranha + HF	None	x	x-1
Piranha + HF	O_2 1000W Plasma, 5'	-	x
Piranha + HF	UV/O_3, 5'	-	x-1
Piranha + HF	Ar 24W Plasma, 5'	-	2-3
Piranha + 90C H_2O + HF	Ar 24W Plasma, 5'	-	2-3
RCA + HF	None	x	x
RCA + HF	Ar 24W Plasma, 5'	-	2

An x indicates no bonding, a - indicates the combination was not tested, and otherwise the number indicates the yield (out of 3) which had some form of bonding. A range indicates multiple test results.

Table 4.4: Results of initial GaN-SiC bonding experiments

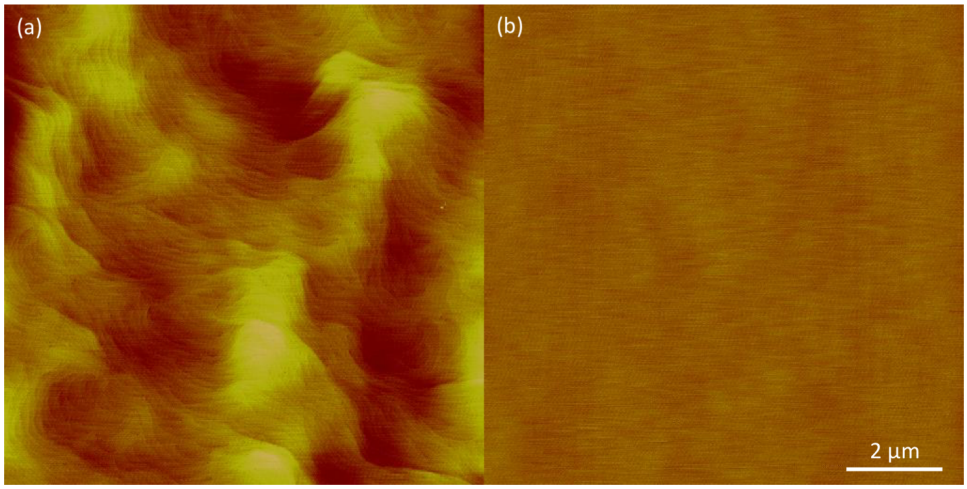

Figure 4-3: AFM measurement of (a) GaN and (b) SiC samples after 24W Ar plasma exposure

force were tested, but they were all too low for bonding to occur. Increasing the mechanical force to 2000N started cracking a high number of pieces due to stress points at the corners of the samples. The yields for all methods except for the Ar plasma were very low. The best method by far was the Piranha followed by a 90C H_2O bath, an HF dip, and Ar plasma exposure. Towards the end, almost 100% piece yield could be obtained, although the areal yield for any given piece was significantly lower, and seemed to be relatively random due the individual bows in any two pieces.

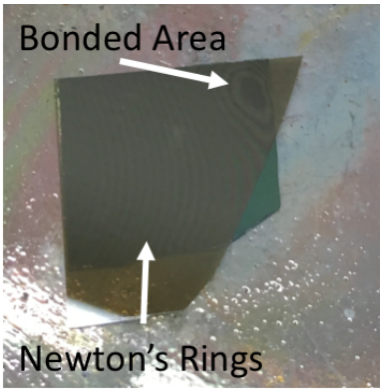

Figure 4-4: Sample with small visible bonding region

The wattage and time for the Ar plasma was determined from several tests once the method showed progress. Initially, 12W of RF power was used for 2'; this resulted in a single bonded pair. Although concerned about surface ablation, AFM yielded no changes in the surface roughness for any RF powers tested. Increased power at 24W only improved yield, and AFM showed no change in the surface roughness for the powers tested. The plasma process had high flow, but low plasma power, so that there was high density of weak bombardment.

The strength of the bonded samples was determined destructively. A standard method utilizes a razor as a separating cantilever. After it has been inserted, the length of separation of the pieces determines the adhesion strength [85]. However, for the small pieces used, this method is not functional. Instead, material transfer was looked for as a sign of bond strength. If the samples break apart cleanly, they were only held together by van der Waals forces. If cracking action occurs into the SiC or the GaN, then the samples are strongly bonded for at the crack the interface bond was stronger than the crystal bonds. Luckily, the SiC is optically transparent, and thus the boned regions can be distinguished by their darkness, with surrounding newtons rings indicating separated material. Using an IR camera with backside sample illumination gives another way to determine bond area. However, due to the low resolution present, the Newton rings were found most effective. For example, Figure 4-4 shows a sample

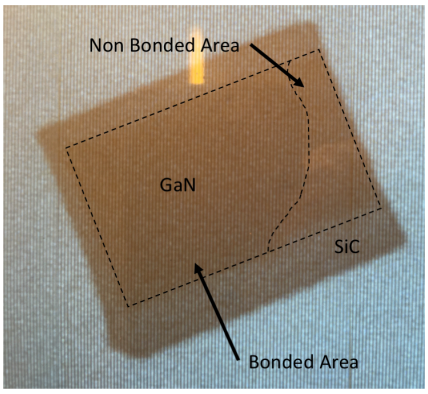

Figure 4-5: Initial bond quality examined under IR camera

with small bonding area. For the experiments above where bonding was reported, the samples were firmly held together, but they could be separated with sufficient force. Any prolonged lateral pressure would eventually break the two pieces cleaning apart, with no signs of material transfer. Attempts to subsequently process the samples, such as wet cleans, SF_6 RIE, or mechanical Si lapping would separate the pieces. Therefore this bonding alone is not sufficient to achieve the desired structure.

4.5.2 High Temperature Annealing

After a reliable pre-bond method was developed, several attempts were made to anneal the samples. At first, the samples were simply loaded into a diffusion tube. Under nitrogen atmosphere, they were annealed at 900, 950, or 1000C for either 10' , 30', 1 hour, or 4 hours. Over a dozen samples were tested, but only one sample stayed bonded together. Upon examining the surface of the failed bonding materials under an optical microscope, they appeared as in Figure 4-6.

The GaN samples degraded significantly over longer anneal times. The SiC surface also had discoloration located where the GaN material had been. At temperatures above 800C, GaN can begin to dissociate with N_2 diffusing away and Ga left behind [95]. However, this is not a negative effect in bonding. In GaN-GaN direct bonding, it is hypothesized that nitrogen dissociation frees Ga to form interface bonds [96]. This

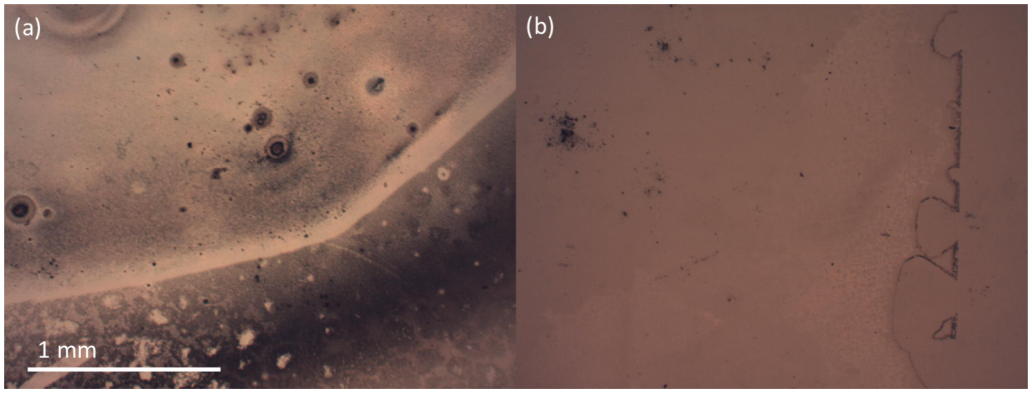

Figure 4-6: After failed anneal at 1000C for 1hr (a) GaN degradation and (b) SiC surface under 5X magnification

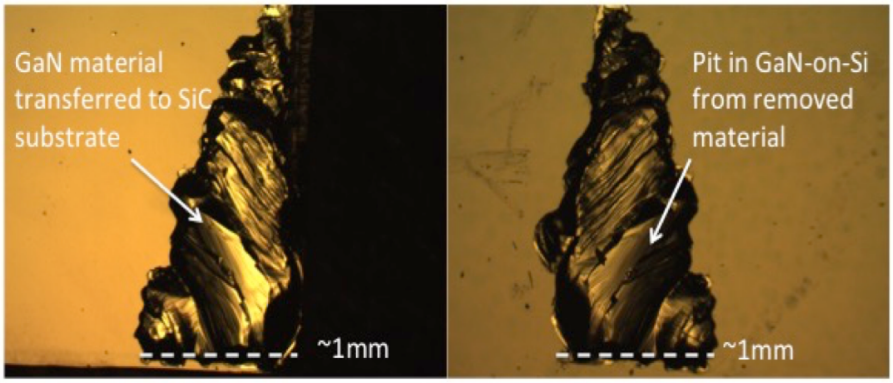

Figure 4-7: Transferred GaN/Si material after annealing

mechanism is also expected in GaN-SiC bonding [78]. Increased surface pressure was found to limit Ga extraction [96], and it therefore seems that mechanical force is needed on the wafers at high temperatures. In these samples, the CTE mismatch and bow differences break apart the initial bond; the close proximity of the SiC extracts gallium from the GaN lattice. Bare GaN samples did not have the same degradation even after mirrored processing steps. Therefore, while observing this dissociation mechanism affirms the bonding process, it presents the challenge of how to maintain pressure on the samples during the anneal steps.

During a 1000C anneal for 1hr with a 2 hour ramp up/down, a small section of GaN and SiC remained bonded. Testing the strength of the bond via the edge method, the pieces broke apart, but a chunk of GaN/Si material was transferred and firmly

bonded to the SiC wafer. Although only 1 x 2 mm, this transfer demonstrates the promise of the bonding method. This transferred material can be seen in Figure 4-7. The surrounding GaN surface has minimal degradation, suggesting that there was sufficiently high surface pressure in this region. Overall, these experiments showed the promise of bonding these materials; however, a surface contacting force is needed to reliably bond the samples.

4.6 High Temperature Bonding Fixtures

When considering a high temperature bonding fixture there are several limiting factors: the materials, the stresses involved, and the total weight. The main aim of the fixture is to apply vertical pressure to the pieces, and maintain that pressure up to 1000C. Initially a press-like fixture was considered. However, constructing such a press turned out to be difficult. The initial design consisted of graphite plates, with a central block to apply pressure evenly over the piece. To tighten the press, graphite screws were considered, but were extremely difficult to source. Molybdenum screws were manufactured, but after several tests, they oxidized, likely due to insufficient material purity. A static device was then considered, taking inspiration from [97]. A quartz tube acts as a constraining collar for two half-rods of graphite (see Figure 4-8). The pieces could then be inserted between the graphite halves with graphite shims; the thermal expansion of the graphite over the quartz would provide the proper pressure. The coefficient of thermal expansion for fine-grain graphite is at least $2 \times 10^{-6} m/mK$ whereas high quality quartz only expands at $0.77 \times 10^{-6} m/mK$. Thus, the pressure applied is roughly 5.3 MPa (assuming a Young's modulus of 4.1 GPa for graphite). This would be equivalent to over 500N of force on a 1 cm^2 , which is on the same order as the bonding machine. This pressure is lower than the stress limits for quartz tubing [97] and should not shatter the quartz.

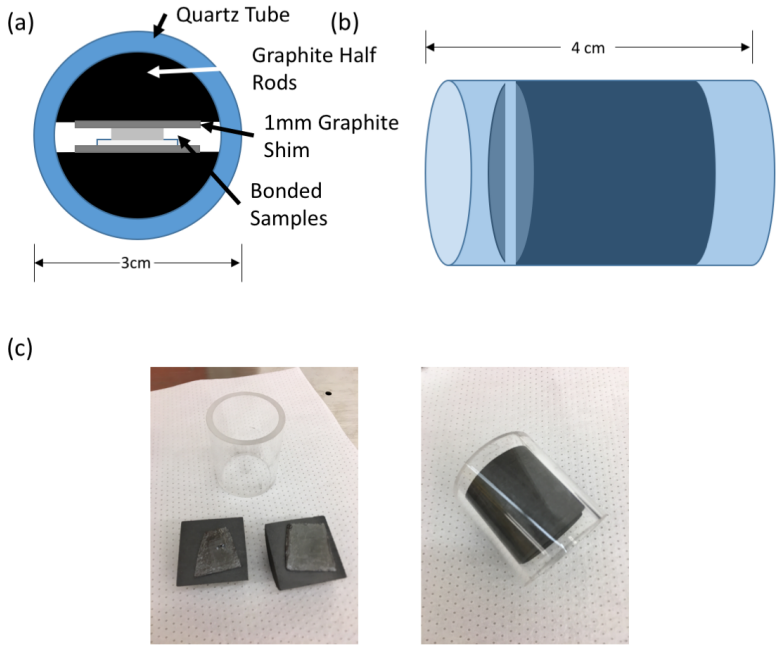

Figure 4-8: Graphite bonding fixture

Several of these fixtures were fabricated by hand due to difficulties in purchasing the machined parts. A graphite rod of the appropriate diameter was cut to length and sanded to the needed thickness. While fine grain paper was used, the surface was still not particularly even. But with graphite shims, samples fit snuggly.

4.7 Stress Relieving Etched Channels

While the fixtures described should help keep the faces in contact, etched channels have been used as a stress relieving mechanism for heterogeneous bonding [94]. By allowing the smaller pads of GaN material to expand and contract more freely, they hopefully will reduce the bonding stress. They should also work to improve gas flow at the interface, aiding in the dissociation mechanism described above. To fabricate these structures, a mask with 300, 500, and 1000 um pads was made, with 10um channels between neighboring pads. A 2 micron high frequency oxide layer was deposited on the pieces, and standard positive lithography was used to open the channels in

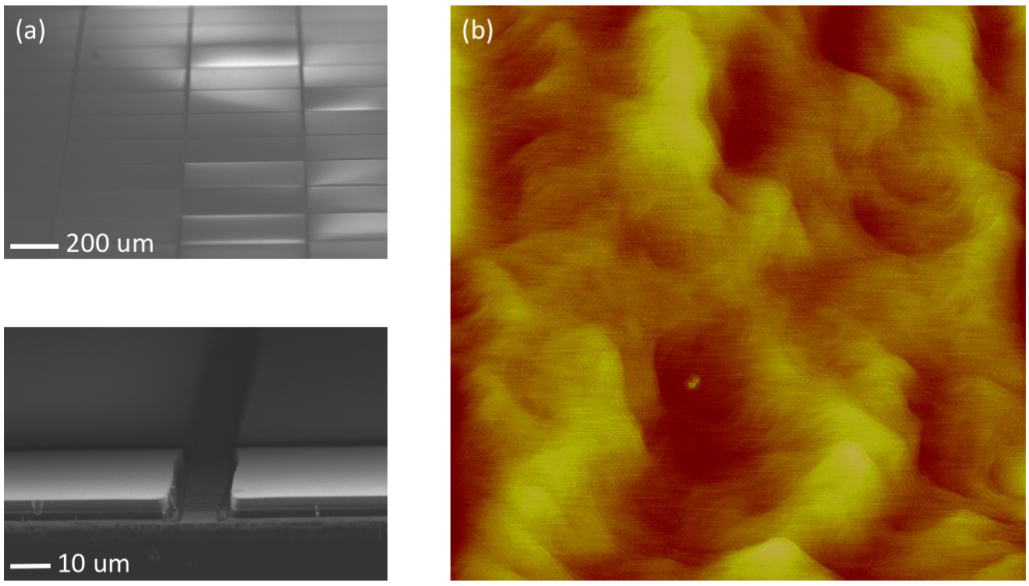

Figure 4-9: Stress relieving channels etched into GaN (a) SEM Images (b) Surface AFM after etch processing

the resist. The oxide was then etched via Cl-based plasma. The GaN and underlying layers were etched with Cl_2/BCl_3 high powered plasma (at a rate of 250nm / minute). The GaN was slightly over-etched to ensure complete removal in the channels. After etching, samples underwent an HF dip to remove the oxide; a surface profilometer was used to measure the channel thickness. The surface roughness was measured via AFM and found to be 6.91Å.

These etched channels were critical in the bonding process, and samples without the channels had significantly lower yield during the anneal (when fixtures were used). They also seemed to improve the surface degradation observed on earlier pieces. While still present, the degradation is limited to the centers of the pads, and is visibly better even on failed anneals. This can be seen in Figure 4-10.

4.8 Final Bond Annealing

ch3:finalanneal With the above changes to the process, a second set of wafer bonding tests was conducted. Although there were some initial difficulties with loading the

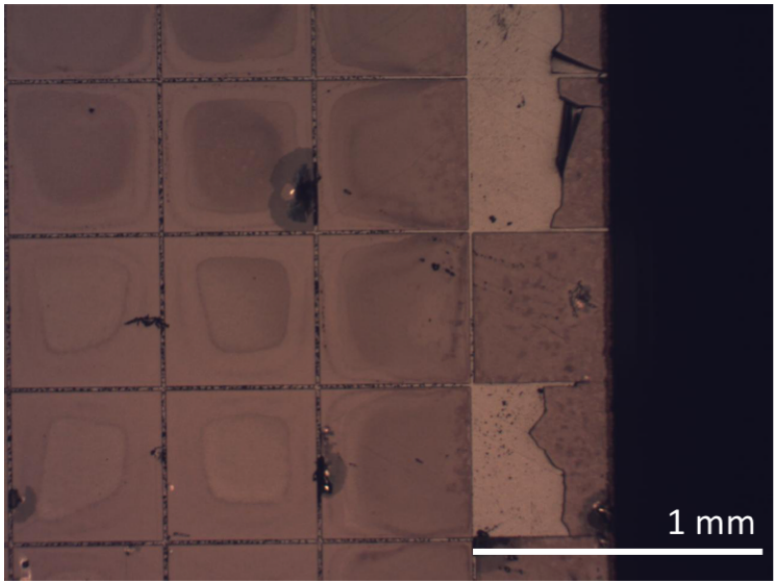

Figure 4-10: GaN surface after failed anneal with stress-relieving channels, optical microscope 5X mag

Figure 4-11: Final bond yield on best sample

wafer bonding fixture, the process ended up being relatively high yield. In a final experiment, out of 7 samples initially bonded, 6 ended up with some part strongly bonded. Of these 6 samples, 3 had very small bonding areas (around 5mm x 5mm), one had a 4mm x 8 mm bonding area, while two approached 50 % yield (see figure Figure 4-11. In general, these variations seemed to result from uneven applied pressure applied by the bonding fixtures.

A sample was scribed and its interface was examined under He+ Ion Microscopy (compared to SEM, this method offered a nominal 1nm resolution, and was able to

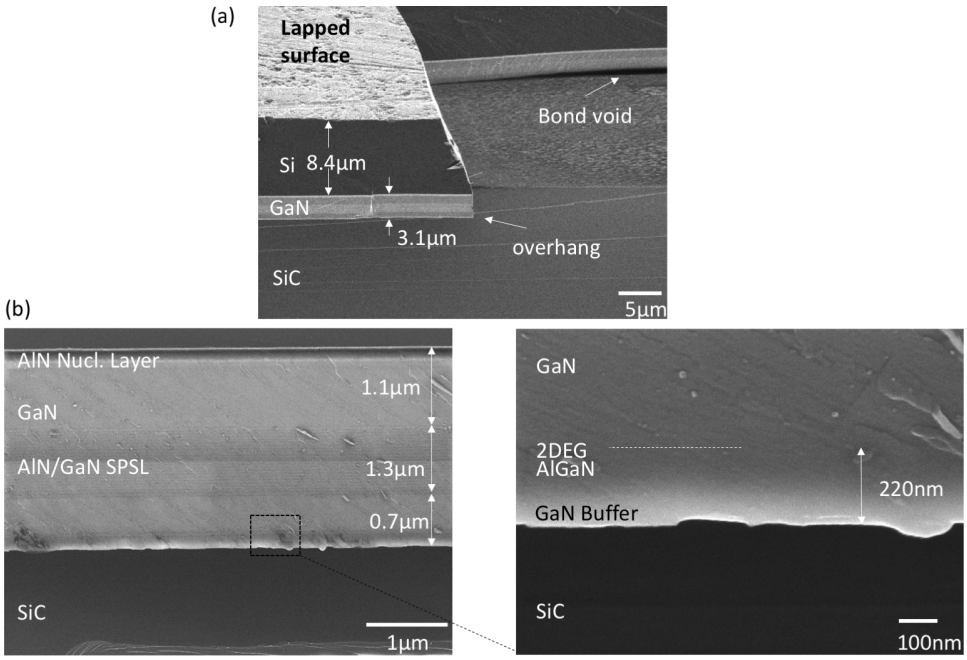

Figure 4-12: He+ ion microscopy imaging showing (a) void at scribed edge (b) side view of bond interface

excite the SiC such that details were visible). The interface appears to be good, with a thin amorphous region in the GaN buffer. However, the light region in the image could also be a charging effect or a result of the scribing. While some microscopic voiding was observed, there was not a visibly significant amount. Overall, the bond quality seemed to be high, with a predominantly cohesive crystalline interface.

4.9 Bonding Discussion

In general, the wafer bonding of GaN and SiC proved to be a finicky process. After several optimizations, including specialized bonding fixtures, the process was of sufficiently high yield such that further processing was feasible. There are several steps which could be taken to refine the process even further. The most critical being the fabrication of high quality wafer bonding fixtures. By properly manufacturing the fixture to provide uniform surface pressure, the yield will undoubtably increase. However, transitioning the process to a specialized high temperature bonding sys-

tem seems a more successful avenue. By combining the bonding and annealing steps into a single process, many sources of error can be eliminated. Beyond mechanical improvements, there are still potential process refinement in terms of exact bonding time, temperature, pressure, chemical cleaning, and surface activation. In the current state, the process has too many sources of error to properly control in parameter optimizing experiments. However, once a highly repeatable process is obtained the effects of step modifications can be accurately determined. For example, the 90C water bath post Piranha clean seemed to greatly improve bonding yield. However, it was hard to control all other variables in the process to accurate test whether this step was needed. Likewise, it was impossible to run a controlled test to optimize power and exposure time for the Ar plasma.

While there is still much work to be done on this process, the results presented herein provide excellent proof that GaN-SiC wafer bonding is feasible, and potentially high yield. As will be seen in the next chapter, the bonded samples are able to survive both mechanical lapping and RIE etch processes. The incremental process improvements for scalability are therefore all that remain, and these can easily be approached as described above. Overall, this work demonstrates the potential of GaN-SiC wafer bonding as a scalable method for fabricating devices.

Chapter 5

Thermal Measurement of GaN-SiC Bonded Structure

With the development of a wafer bonding process, thermal measurement of the GaN-SiC thermal boundary resistance can occur using time domain thermoreflectance. This is a key step to determining the accuracy of the simulations in chapter 3 and the promise of this fabrication method for GaN HEMTs. After bonding there are several processing steps required to obtain measurable samples. First, the original Si substrate must be removed and second the original GaN/AlN buffer material needs to be thinned to an appropriate point in order to maximize measurement sensitivity. The attempts to do so are described herein, as well as the experimental methodology for the TDTR measurements and their results. There were several difficulties faced in this back etch process, namely micro masking and associated GaN pillaring during the etch. Several chemistries were attempted to reduce the formation of these pillars, however, it was never entirely eliminated. Nonetheless, good signal quality was achieved with TDTR; the GaN-SiC TBR was extracted from data fits.

5.1 Sample Preparation

While using 200mm wafers in the bonding experiments gave large areas of high quality material, the corresponding 1.1 mm of Si substrate was difficult to remove. Several methods were explored in removing this Si in an efficient manner while also maintaining good surface quality of the GaN material. The effect on the bonding interface and underlying N-face GaN of the various removal chemistries was not well known, but both mechanical, wet and dry Si removal methods were explored. After the Si had been removed, a etch process was needed to thin down the GaN and other buffer layers such that remaining GaN material was optimal for the TDTR measurements. There were several challenges in this step, namely micro masking and associated pillaring. The selectiveness of a modified GaN etch was tested as a method to eliminate or reduce the pillars, as well as create a smooth surface for thermal measurement on a stop etch layer.

5.1.1 Lapping of Si

While DRIE etch methods yield smooth, selective removal of the Si over the AlN/GaN film, they are prohibitively expensive and time consuming for a 1.1 mm bulk etch. Several wet methods exist, but the Si (111) orientation makes both KOH and TMAH unusable. HNA etching was tested, but resulted in uneven Si removal and GaN peeling due to the bubbling nature of more aggressive HNA etches. The GaN flakes would then end up on the remaining bonded material in the solution, and would fuse to the surface.

The mechanical removal of the Si via a lapping machine was therefore an extremely promising alternative to these methods. Although polishing steps reduce roughness, lapping can increase the roughness of the Si from the original backside polished value. However, the high selectivity of DRIE etches do not translate this roughness to the

GaN. Therefore, the proposed process was to a lap away 1mm of the Si substrate. Initially a very rough, 120 grit (140 micron) SiC paper was was used to remove the first 750 μm. This took 30 minutes, as the lapping rate is quite aggressive at 25 $\mu m/min$ on small pieces. The paper was then changed to 400 grit (40 micron) SiC paper. This was used to remove another 200 or so microns, and took another 20 minutes. The final paper was 800 grit (25 micron) SiC paper, which was used to polish the surface until visibly reflective (roughly 20 minutes). During this process, the strain of lapping would often break the non-bonded regions of the GaN-on-Si wafer away. While initially troubling, this was not problematic, as it did not reduce the bonded area. Later lapping tests utilized 30 micron (600 grit) diamond paper. This would still quickly remove the Si material, and once the mechanical stop had been reached, would also polish the Si surface. Overall, this method was a strong alternative to a wet or dry chemical etch, as it allowed the quick removal of the bulk Si material. While the surface roughness was not measured, the lapped surface optically appeared smoother than the initial substrate; additional polishing steps could be taken to reduce roughness even further. To achieve atomic smoothness, however, CMP is needed. Figure 4-11 contains a sample which underwent lapping to remove all but 30 μm of the Si. The sample therein is reduced to the bonded regions, but the surface is quite smooth. After lapping, the sample was sonicated in acetone for 30 minutes, then a triple solvent clean was performed, followed by a double Piranha to bring the samples back to clean room cleanliness.

5.1.2 SF_6 RIE

SF_6 RIE was initially used as the sole Si removal method on the first bonded sample (shown in Figure 4-7). However, with larger bonding areas and full wafer thickness it presented several problems. Namely, it was difficult to create a carrier wafer which could withstand the several hours of SF_6 etching needed to go through 1.1mm of Si.

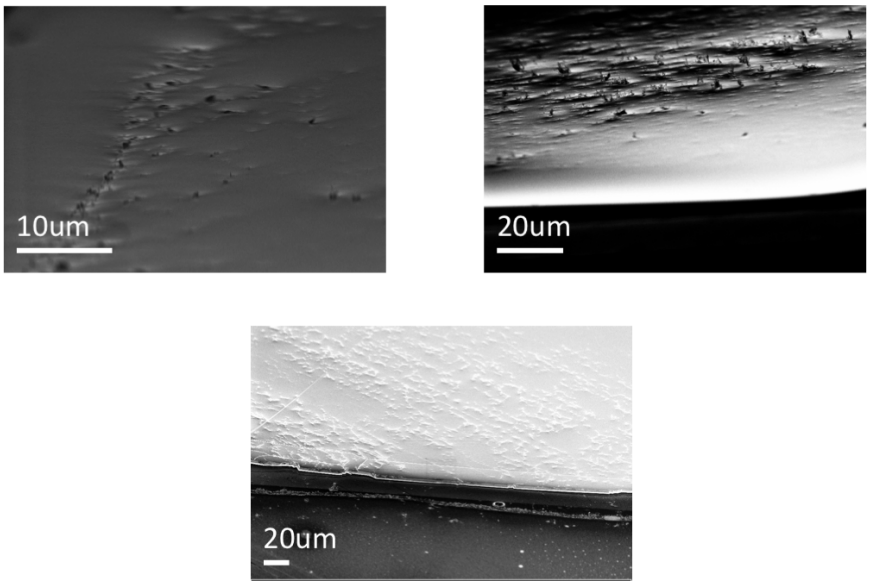

Figure 5-1: The transferred film surface in various samples after removal of Si via SF_6 with a 20% over etch

Thus, the SF6 etching was primarily used as a method of removing the final 100 or so μm left after the lapping process. The chemistry used was a straight SF_6 isotropic etch process with 600W of RF power. The samples were loaded onto a coated quartz wafer, with Kapton tape used to hold down the sample. While this method removed the Si, it seemed to either leave a residue or slightly damage the AlN surface. This residue is shown in Figure 5-1 for three different samples, each with slightly different surface morphology after etching. The appearance of both particulate and surface roughness around the particulate indicates that this each leaves a poor surface for subsequent GaN RIE.

The chamber of the etch tool likely contaminated the surface. As the dry etching system is often used for Bosch process etching, this material could possibly be a teflon byproduct. However, this should be removed by a prolonged SF_6 over etch. An second issue with the SF_6 etching is that it partially etches the SiC at the edges of the GaN material. This also opens up the bonding interface to the plasma, which is weakened and etched away. This results in significant peeling of the bonded GaN film, which presents significant reduction in the usable area. While peeling might

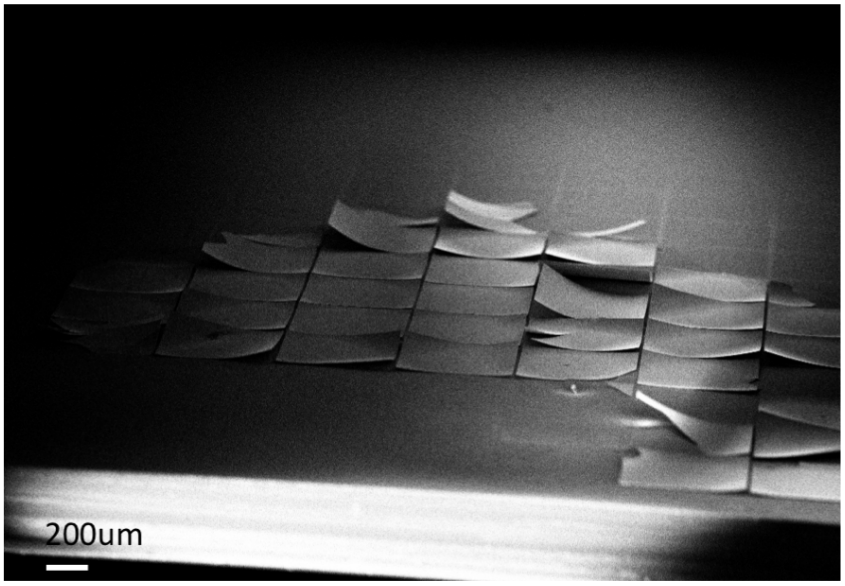

Figure 5-2: GaN film peeling due to SF_6 etch seep

be due to poor bond quality, it was significantly worsened by prolonged etching. In samples with uneven Si (from GaN/Si material ripped out of the Si substrate), the regions which were first etched has significantly worse peeling than regions which had been exposed to the plasma at a later time. It is hypothesized that the plasma is undercutting the GaN, causing initial peeling. The bond interface is exposed as the GaN peels, worsening the peeling as etching continues.

While the SF_6 problems only became apparent during the later GaN etch stages, several attempts were made to clean subsequent samples. While Piranha was deemed to be too aggressive, commercially available Nanostrip (a "cold" Piranha) was used in a 10 minute clean at room temperature. The minimal effect this clean had can be seen in Figure 5-3. It seemed to partially remove and dissolve the surface contamination, but also seemed to damage the AlN and several of the GaN pads were either dislodged or cracked due to the processing. The dissolving effect of the clean also only made the areal contamination worse than initially. An HF dip was also attempted to remove the contamination. A 2 minute dip in 10:1 H_2O : HF removed all but a few of the bonded pads of GaN. However, those pads that remained had extremely clean

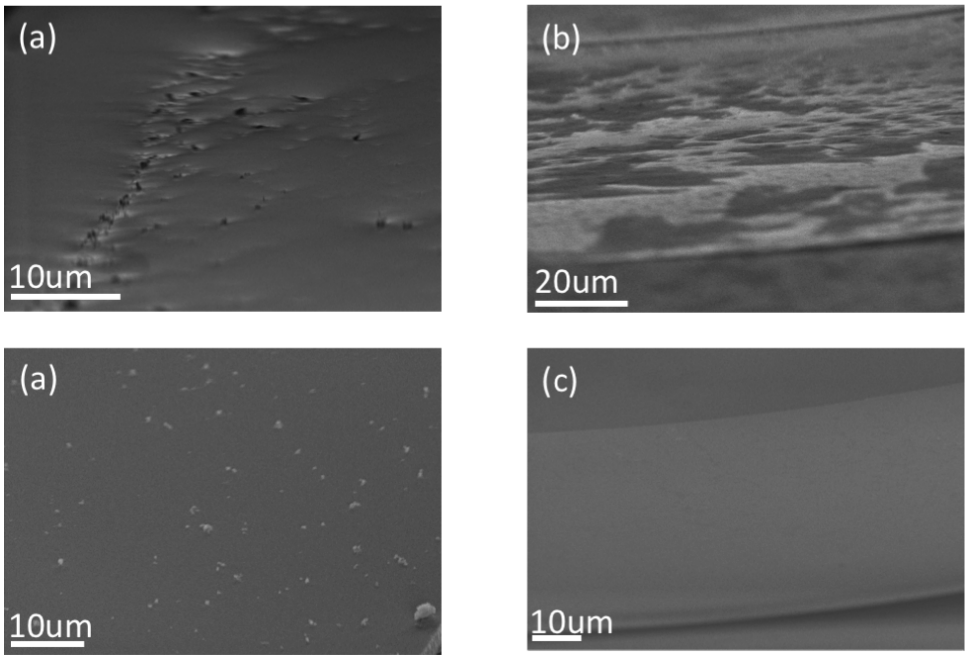

Figure 5-3: GaN film surface (a) after Si removal (b) after additional 10 min Nanostrip clean (c) after additional HF dip

surfaces, suggesting that it was effective if the peeling could be resolved. It was unclear whether a poorly bonded sample, chemical interaction, or the mechanical action of the dip, the rinse and blow dry which was responsible for the low level of adhesion. Neither method was used in subsequent samples.

5.1.3 GaN Etching

The first attempt at thinning the GaN buffer was using a standard deep GaN etch. The recipe was 20 sccm of Cl_2 and 4 sccm of BCl_3. The ECR power on the tool was set to 150W, with 75 W of RF platen bias power, and the wafer chuck cooled to 40C. This etch was developed by colleagues for use in vertical HEMT fabrication, and has a measured etch rate of 250nm/min. The results of this etch can be seen in Figure 5-4. This etch left an extremely pillared, rough surface, with pillars measuring over 1.5 μm. The etch was likely too high of power for N-face etching, as the N-face of GaN is significantly more reactive. Combined with the micro masking, the

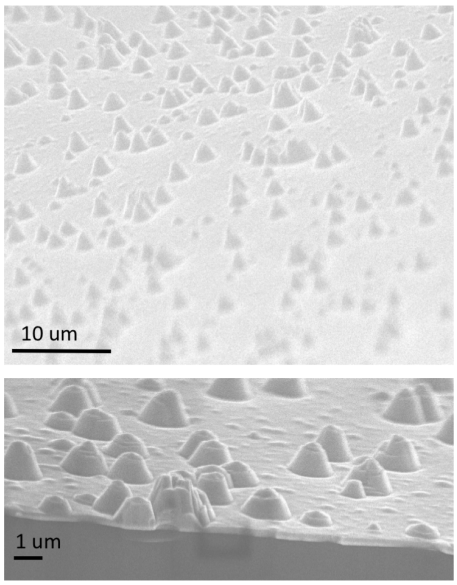

Figure 5-4: GaN film surface after 10 minutes of high power Cl_2/BCl_3 etch

net effect is a highly damaged surface that is unsuitable for thermal measurement. A lower power etch was also tried using the same chemistry; this did not offer significant improvement in the surface quality. At the recommendation of a colleague, a modified chemistry, with equivalent CF4 density as BCl_3. This addition reduced pillaring while still maintaining a moderate etch rate. The surface of the GaN film is remarkably improved over the original as overall density is significantly reduced. However, the pillars are of a wider area, and they tend to grow laterally during the etch through of the SPSL. This is likely due to the lower power etch being more selective to the AlN layers. While not perfect, this etch was used to go through the majority of the SPSL buffer and the GaN material.

5.1.4 GaN/AlGaN Selective Stop Etch

Previous wafer-bonded N-faced GaN HEMTS (bonded to Si) utilized a stop etch layer of AlGaN to control surface roughness before reaching the level for device fabrication [76, 80]. Similar layers were grown into the wafer structure used for bonding. The selective chemistry is formed by SF_6/BCl_3, with the SF_6 reducing the etch rate in

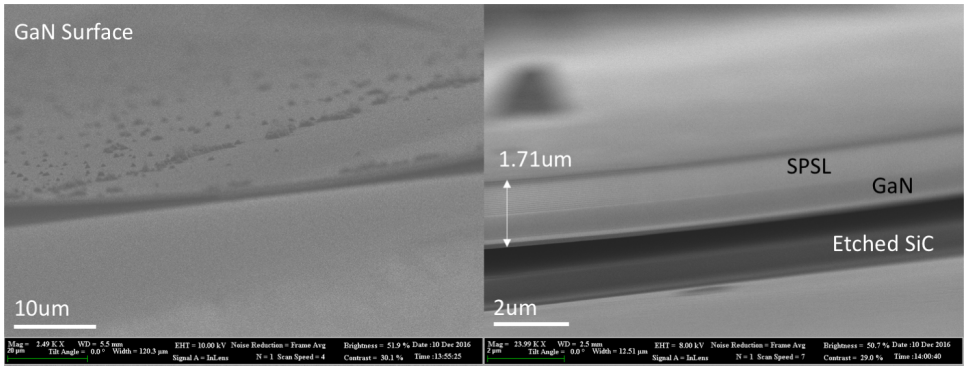

Figure 5-5: GaN film surface after one hour of $Cl_2/BCl_3/CF_4$ etch chemistry

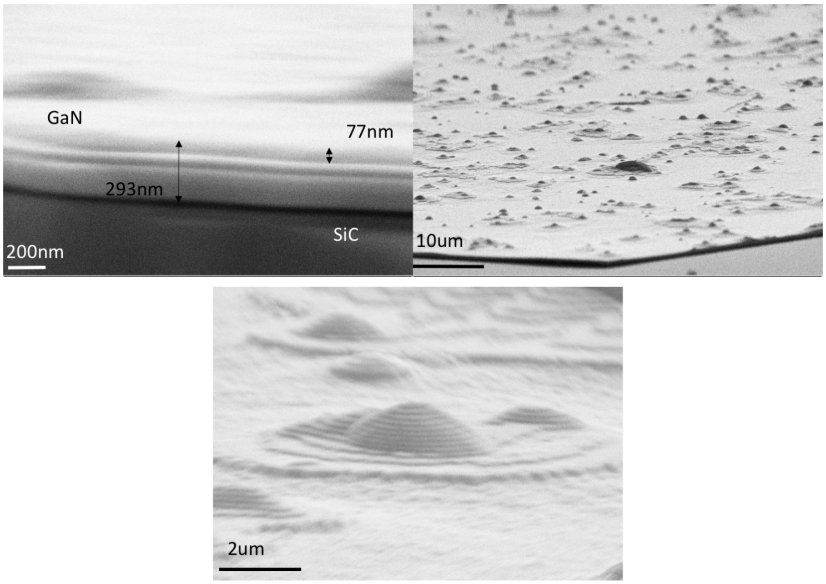

Figure 5-6: GaN film surface after 2.5 hours of $Cl_2/BCl_3/CF_4$ etch chemistry

Al-containing layers. This has been shown to provide a smooth surface at the stop layer and subsequent low power etching can be used to remove the AlGaN and reach the GaN to fabricate devices [76]. However, it is unclear if this method is selective enough to remove or reduce the pillars formed during the GaN buffer removal. To test this, the process was run for a prolonged period after the GaN buffer had been etched to within 77 nm of the AlGaN layer. After three hours of etching with this chemistry, the pillars were relatively unchanged in both diameter and height. The stop etch layer was reached, and the non-pillared regions appeared to be of good quality. Likewise the pillars, particularly those at the SPSL height, were flattened out due to the selectivity

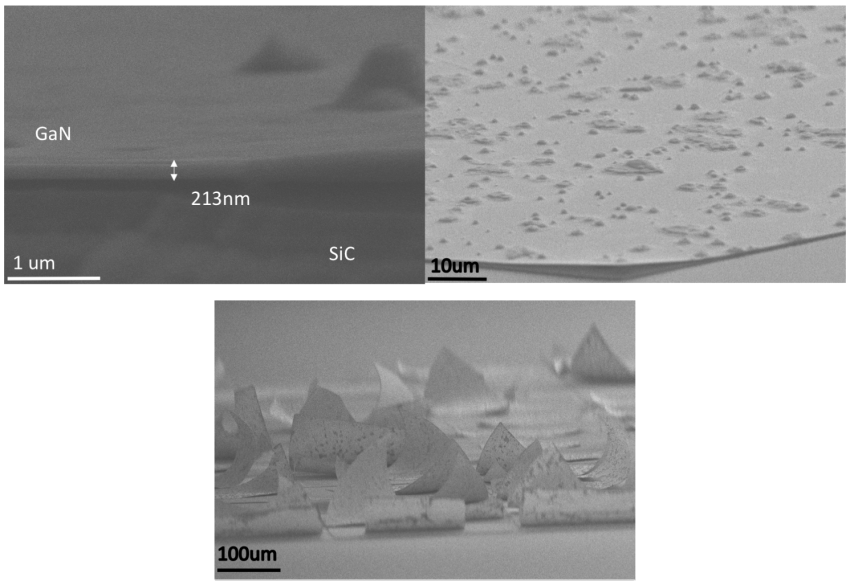

Figure 5-7: Sample after 3hrs of selective etch

to GaN over AlN. However, peeling worsened significantly; several pads of transferred material were reduced or eliminated. Overall, the stop etch recipe is highly effective at smoothing the normal roughness increases in etching, but is not effective at removing pillars. Likewise, prolonged use reduces the area suitable to device fabrication and thermal measurement. The best method to eliminate these pillars is to develop better a Si removal and surface cleaning method. For TDTR measurements, the GaN etch recipe described above was then used to remove the AlGaN stop layer, the next GaN material, the AlGaN forming the 2DEG and into the bonded GaN buffer material. The results of these etches are described in subsection 5.2.3.

5.2 Time Domain Thermoreflectance Measurement of Bonded GaN-SiC TBR

While the back etch results were less than ideal, TDTR measurements were made on several samples. A sensitivity analysis was performed to determine the optimal sample conditions to measure the GaN-SiC thermal interface conductivity. The samples were

etched to the appropriate thicknesses, and a Al transducer layer was deposited via e-beam deposition. Several spots on the surface of the two bonded samples were probed, however, only one sample yielded data without obvious measurement error. This data was fit with an appropriate model, and the TBR values extracted are discussed and analyzed.

5.2.1 Measurement Technique

Time domain thermoreflectance (TDTR) is a standard measurement technique for determining the thermal conductivity of semiconductor materials and interfaces. It is a pump-probe technique, and as such, measured data is compared to a representative model of the system and materials. The parameters of the model are then varied to fit the data; assuming there are sufficiently few parameters unknown, they can be extracted with high confidence [98]. As with any such fitting system, too many unknown variables greatly reduce the sensitivity of the method. In TDTR measurements, having the simplest system or a simplified model usually yields better results, although complicated epitaxial structures have been measured [51, 52]. While the exact specifics of this technique are beyond the scope of this thesis, a cursory description is now given.

TDTR is a two stage technique. In the first stage, a pump beam of light is pulsed onto the surface of the material under study. As this material is coated with a thin layer of Al (around 90 nm), the laser pulse is converted into thermal energy at the surface of the metal. Free electrons absorb the light and ballistically transport through the transducer layer, eventually interacting with the lattice and generating heat-carrying phonons. This transfer of energy takes time on the order of picoseconds. These phonons are then free to diffusely transport heat through and into the structure via the processes described in subsection 2.2.3. A secondary probe beam is then directed at the surface of the material. The maximum delay between these beams is

critical, as it limits the depth that the pumped heat reaches in a structure. The probed beam is reflected off of the Al surface, and the intensity of this beam is dependent upon the thermoreflectance of the material. The Al thermoreflectance is well characterized and relatively constant over changes of temperature. The reflected probe intensity can therefore be directly related to the temperature at the Al surface [98]. As the heat generated from the pump pulse decays away, a reflectance decay curve can be measured. This curve is then fit from an analytical model of thermal conduction in the sample, with the parameters of interest used to optimize the fit [51, 52, 98].

5.2.2 Sensitivity Analysis

When considering measuring a buried thermal boundary, it is critical that there are as few unknowns in the system as possible. Due to the pillaring on the surface, the sample already contains several unknown parameters, particularly the thermal boundary resistance between the Al transducer layer and the GaN. It is therefore critical to eliminate other thermal boundaries and materials that further obfuscate the desired parameter. Instead of simply stopping on the initial AlGaN stop etch, and slowly etching through it till the GaN material is reached, the samples were etched on through the 2DEG until the final GaN buffer material was exposed (see Figure 5-8. This greatly simplifies the structure under analysis to a GaN layer bonded to SiC (with some surface GaN pillars). The corresponding data fitting is also simplified as uncertainty over the AlGaN-GaN TBR and AlGaN conductivity is eliminated. With the final GaN thickness known, reasonable estimates for the GaN conductivity (via phonon MFP suppression) can be made. A important first calculation is the penetration of the heat in the system. The max delay time in the TDTR setup used is 6 ns. The thermal diffusivity of Al is $9.75 \times 10^{-5} m^2/s$, implying that 90nm of Al

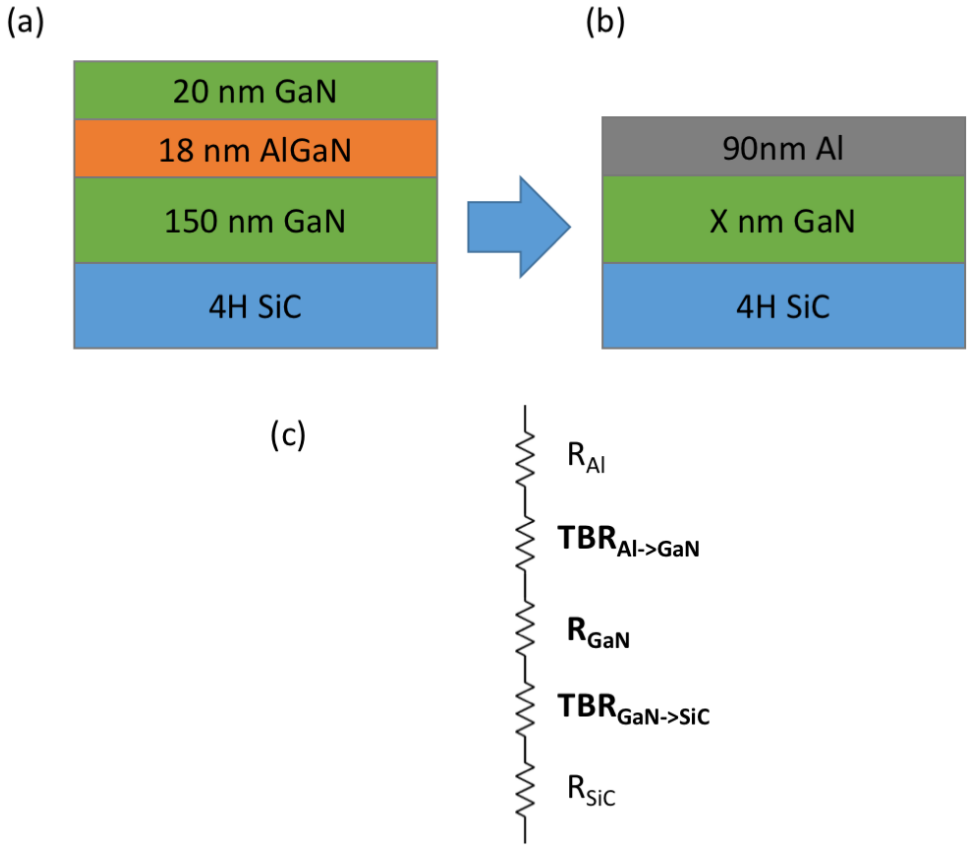

Figure 5-8: Structure (a) after original etch (b) with simplified epitaxy yielding (c) five thermal resistor model

is penetrated in 83ps. For GaN, the diffusivity is:

$$\alpha_{GaN} = \frac{k_{GaN}}{\rho_{GaN} c_{p,GaN}} = \frac{150 W/mk}{6150 kg/m^3 \times 490 J/kgK} = 4.98 \times 10^{-5} m^2/s \qquad (5.1)$$

Thus, 150 nm of GaN material is penetrated in 452 ps. The sum of these values is well within the delay time, and the pump pulse will reach the GaN-SiC interface. A sensitivity analysis of the three parameters of the fitting model ($k_GaN, G_{Al->GaN}, G_{GaN->SiC}$ was conducted for various GaN material thicknesses. The results of that analysis are found in Appendix A. When looking at the plots therein, larger absolute differences in the desired parameter ($G_{GaN->SiC}$) and the other model parameters imply that TDTR measurement will be sensitive to that parameter. As can be seen from Figure B-1, in a time domain analysis, fitting the amplitude yields higher sensitivity for

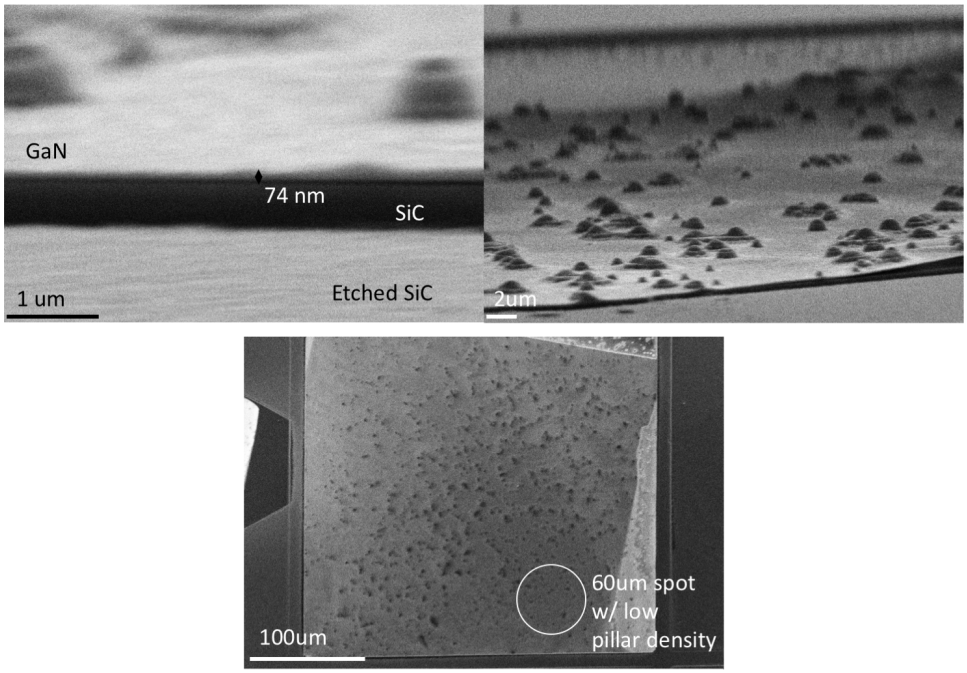

Figure 5-9: Sample 1 for TDTR measurement

thinner GaN layer. In order to be maximally sensitive to the GaN-SiC interface, the samples must have a thin GaN layer, ideally around 25 nm.

5.2.3 Samples Measured

From the results of the sensitivity analysis, two samples were prepared. Their nominal GaN layer thickness (excluding pillars) were 75nm and 33 nm respectively . The thicker sample had considerable pillaring, however, it also had several larger areas to probe, many with low pillar densities. The thinner sample had significant material loss from peeling, but the remaining areas were sufficiently large for the 60 micron spot size of the TDTR beam. The precise thickness of the thin sample was difficult to measure. By looking at several reference points (including the peeled edges), the thickness could be determined. SEM images of these samples are shown in Figure 5-9 and Figure 5-10 . After the etch processes described above, a 90 nm Al transducer layer was deposited via electron beam evaporative metal deposition. A sapphire control sample was also included in this deposition to measure the exact Al thickness

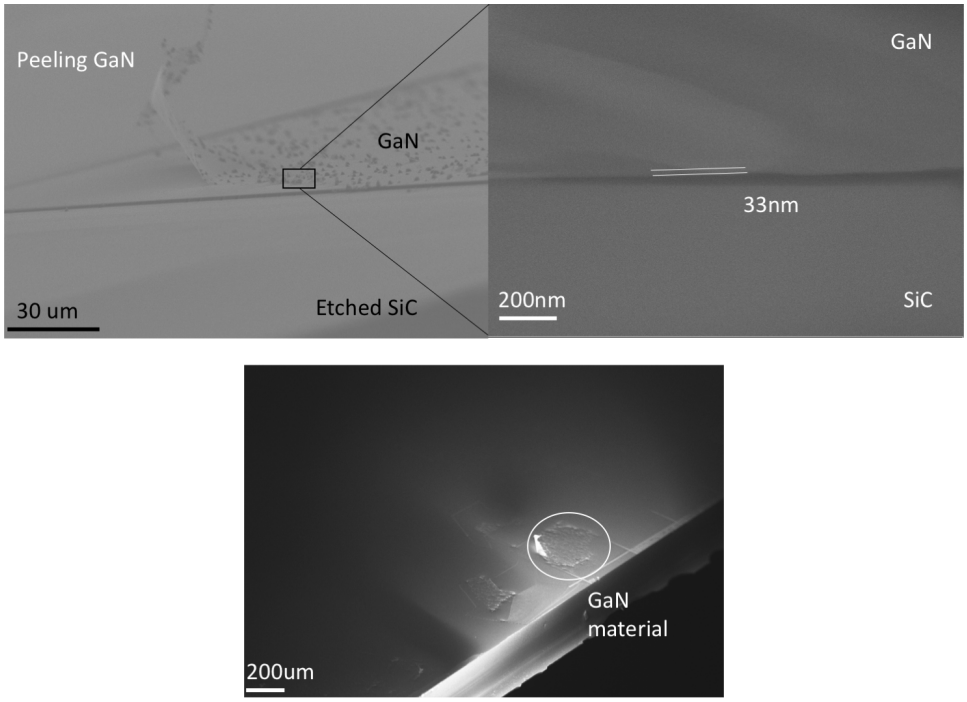

Figure 5-10: Sample 2 for TDTR measurement

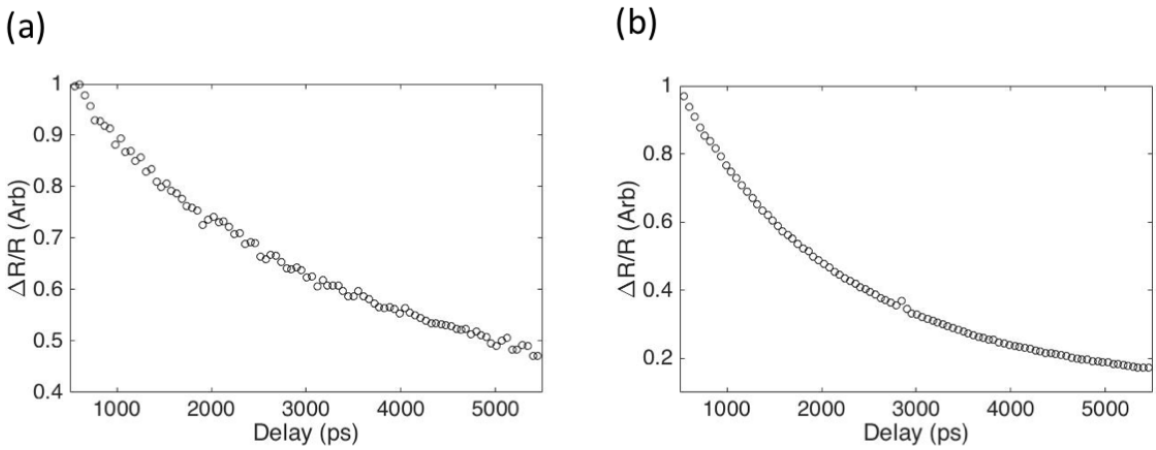

Figure 5-11: Sample (a) 75nm (b) 33nm GaN measured thermoreflectance

using the TDTR setup.

5.2.4 Measured Results

After the Al thickness was measured, and the TDTR system calibrated, the two samples were measured. The first sample, with 75nm of GaN, yielded poor, oscillatory output. In discussion with the TDTR user, this oscillatory behavior has been

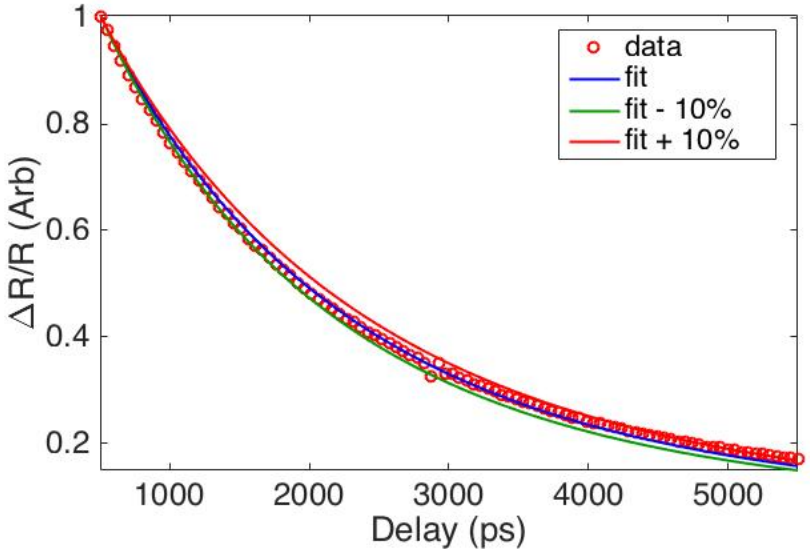

Figure 5-12: Sample 2 measured thermoreflectance with best fit

seen in samples in which the Al transducer layer is not thermally well attached. The second sample, with 33nm of GaN, had a smooth decay in thermoreflectance. Extrapolating from [58] the phonon MFP suppression implies $k_{GaN} = 30W/mK$. Previously measured Al-GaN TBRs have ranged from 6 to 21 m^2K/GW. A value of $G_{Al->GaN} = 10^8 W/m^2K$ was used as an initial starting point to the data fit. With these parameters, the best fit of the data was with a $G_{GaN->SiC} = 2.42 \times 10^8 W/m^2K$. This fit is shown in Figure 5-12.

The data is well fit by this model; it is within the 10% error margins displayed in the graph. A second set of fits was attempted by letting all parameters float save the SiC conductivity. This resulted in an initially confusing model. The best fit was with $k_{GaN} = 350W/mK$, $G_{GaN->SiC} = 2.09 \times 10^8 W/m^2K$ and $G_{Al->GaN} = 10^9 W/m^2K$. With slightly different starting conditions to the fit, a second set of values was found with $k_{GaN} = 416W/mK$, $G_{GaN->SiC} = 1.94 \times 10^8 W/m^2K$ and $G_{Al->GaN} = 10^{10} W/m^2K$. Effectively, these fits are driving to a model simplification, namely a single thermal resistance between the Al and the SiC, as the fit GaN conductivity is effectively that of a SiC layer, and the measured $G_{GaN->SiC}$ is reduced to counteract

	SiC (4H)	CVD Diamond
GaN (Growth)	4-5 [51]	12-50 [72],17-41 [62]
GaN (Bonded)	**4 [This Work]**	38-108 [70]

Table 5.1: TBR (m^2K/GW) for GaN-substrate interfaces measured in literature (Growth signifies either substrate or GaN)

this change. However, these measurements do imply an upper bound on the GaN/SiC TBR of 5.15 m^2K/GW. As there is some thermal resistance in the GaN material, the TBR is likely below $5.15m^2K/GW$, and is closer to the fitted value of $4.1m^2K/GW$.

5.3 Discussion of Results

Overall, the results of these thermal measurements are very promising. The fit quality with an assumed GaN conductivity is remarkably good, with the data well within a 10% error margin in the GaN-SiC interface conductivity. The thermal boundary resistance value of $4.1m^2K/GW$ is one of the lowest reported between GaN and any substrate. Table 5.1 compares this value with others in the literature.

These results significantly strengthen the potential of wafer bonding as a fabrication method for thermally efficient GaN-on-SiC HEMTs. An initial analysis of the secondary fits seems to suggest that heat was flowing outside the limits of the pad, as then the reduced thermal resistance would be the dominant path for heat flow. However, the lateral Al penetration length is 2.8 microns. Combined with the spot size of 60 microns, the total probed region is still well within the GaN pad, and so the system is measuring the resistance to vertical heat flow instead of another path. However, these results are not completely conclusive; additional data is required. Particularly, the impact of the pillars is not well understood. While they are adding thermal resistance, the max penetration depth in GaN is only 0.5 microns. This would effectively yield a high thermal resistance (in the pillar) in parallel with that in the GaN material. Therefore, the total resistance measured could be slightly lower than the actual

value. Further work is needed to ensure smooth samples for measurement. Samples with different GaN thicknesses would allow for better extraction of fitting parameters, particularly the conductivity of the bonded GaN material. Finally, although the values of the bonded thermal boundary are only moderately better than the growth case, this is without any process refinement in the bonding. The GaN/SiC bonded TBR will undoubtably improve as bond quality is increased.

5.3.1 Improved Backside Etching

Significant improvements can be made in Si backside removal and GaN buffer etch processes. The most obvious goals are developing a Si removal method which does not cause peeling, and a N-face GaN etch which does not pillar. These are process development which can readily be solve. Initial tests were made to evaluate XeF_2 as a gentler form of Si removal. The results of these tests were promising, but some micro masking still remained. However, peeling was greatly reduced. It is possible that the peeling results from the mechanical pressure of lapping, and is therefore unavoidable. If this were the case, then refining wet etch methods seems to be a good next step. Finally, if thermal measurement is the sole end goal, performing a windowed backside etch, such that the edges of the GaN pads / bond interface are never exposed to the Si etch chemistry. This could be done with a simple oxide deposition, lithography, and Bosch etch process. The GaN surface could then be cleaned via an HF dip, and subsequent buffer thinning. Improved N-face GaN etching is also required for device fabrication. While the need of a stop etch seems unavoidable, a controlled N-face GaN etch would greatly reduce the need for long selective etches and the peeling problems they pose. This would require significant experimentation with the process chemistry, but the availability of bulk GaN substrates allows for easy test of these methods without the need for the earlier bonding steps. Overall, these backside etching problems seem readily solvable with focused process development.

Chapter 6

Conclusion and Future Work

This thesis explores a novel solution to thermal management problems in GaN HEMTs. The thick buffer material needed for a high quality 2DEG is thermally resistive. It also contains many thermal boundaries, which only worsen heat conductivity through the epitaxy. While moving to higher thermal conductivity substrates offers a substation performance boost, nucleation and bonding interlayers greatly increase the GaN-substrate TBR. Overall, the substrate contributes very minimally to the near junction thermal resistance; the majority is found in the GaN material and the TBR. A new fabrication method is needed such that these thermal resistances can be reduced and eliminated. The solution explored herein utilizes wafer bonding in a novel fashion. Instead of using a carrier wafer and simply performing a substrate swap, a new substrate is wafer bonded directly to the surface of a modified GaN-on-Si epitaxy. The modifications made include a bonding buffer layer which can be of any thickness. As a direct bonding process is used, the thermal boundary resistance is greatly reduced. The original substrate and GaN buffer material is removed, resulting in a thin GaN film bonded to a SiC wafer. It is this film on which devices can then be fabricated.

Simulations of this bonded structure, as well state-of-the-art structures were performed. Due to the reduction in buffer material, significant performance improve-

ments are expected, implying that this GaN-to-SiC bonding technology can outperform even state-of-the-art GaN-on-diamond devices in terms of power density and reliability. Even under varying degrees of material and bond interface quality, the structure greatly outperforms growth GaN-on-SiC. There is therefore strong motivation to pursue the fabrication of these devices.

With appropriate back etch techniques this wafer bonding method eliminates the need for thick, thermally resistive buffers. Several experiments were performed to develop a GaN-SiC wafer bonding process. The process described in this thesis presents the first recorded method for direct bonding multilayered GaN HEMT structures to a 4H SiC substrate. To do so, specialized bonding fixtures were fabricated to overcome the lack of a high temperature bonding system. While the process was highly reliable in that most samples would bond, the areal yield was quite low, only approaching 50% in the best case. However, there are several refinements which can be made in order to scale the process. After successful bonding, back etch processing was performed to realize thin, transferred GaN epitaxies. Samples as thin as 30nm of GaN material were fabricated. While these eliminated the 2DEG, they prove the feasibility of transferring thin GaN films using the bonding and back etch methods. Substantial pillaring during the GaN etching poses a problem, but with sufficient process engineering this can no doubt be eliminated.

Time domain thermoreflectance measurements of the wafer bonded structures yielded a good first estimate for the interface conductivity between the GaN and SiC. At 0.242 GW/mK, this interface conductivity is one of the highest ever measured between GaN and a substrate (Table 6.1), although the best growth interfaces between GaN and SiC range nearby. With an interface of this quality, the bonded GaN structure has an equivalent thermal performance to GaN-on-diamond technology as shown in Figure 6-1. If the bonding interface can approach the theoretical maximum, then this implies a significant performance improvement over diamond devices. Consid-

	SiC (4H)	CVD Diamond
GaN (Growth)	4-5 [51]	12-50 [72],17-41 [62]
GaN (Bonded)	**4.1 [This Work]**	38-108 [70]

Table 6.1: TBR (m^2K/GW) for GaN-substrate interfaces measured in literature (Growth signifies either substrate or GaN)

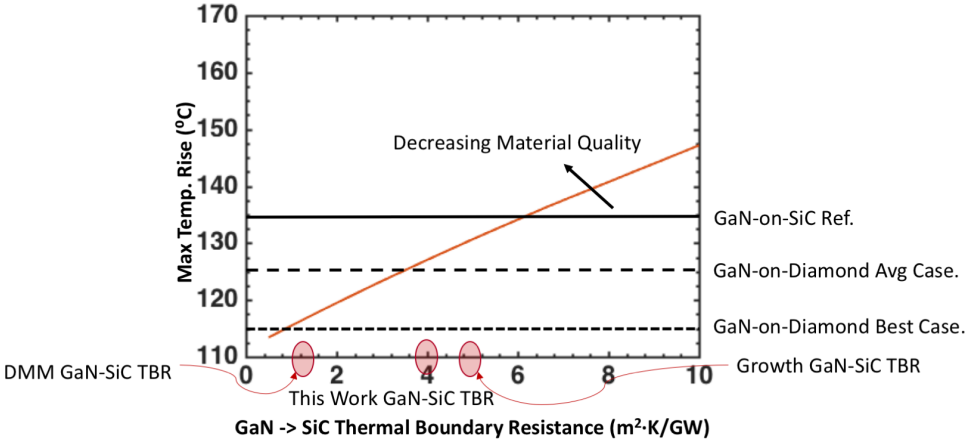

Figure 6-1: Max temperature rise in bonded GaN-on-SiC HEMTs as a function of GaN/SiC Thermal Boundary Conductivity

ering the immaturity of the bonding process, the interface quality, along with yield, can be increased via suitable bonding refinements. Besides the thermal benefits, this technology should be substantially lower cost, as SiC is a more mature substrate than CVD diamond. Overall, there is significant promise in further developing this process and using it to fabricate high performance GaN devices. There are several possible avenues for further exploration of this technology. Improving the bonding process to achieve higher yield and reliability is a key first step. To do so, one could improve the bonding fixtures such that the pressure applied is even across the wafer. A second approach would be the use of specialized high temperature bonding systems, which apply pressure at the 1000C required to bond the wafers. With sufficient uniform pressure, the yield is expected to substantially improve. After these developments, additional refinement to the surface activation and cleaning steps can be performed to create high quality interfaces. Additionally, back etch process development is required to ensure uniform yield. Several alternatives to the delaminating SF_6 etch have been

proposed. Hopefully these allow for clean removal of the Si material such that pillaring and peeling of the GaN are avoided. With these process improvements, better measurements of the GaN-SiC interface conductivity can be made. Doubtless, there is a set of bonding conditions which optimizes the thermal interface, but exploring this requires a highly repeatable bonding and back etch process.

Taking this bonding configuration, and sing a similar process but instead bonding to diamond would be a promising extension. However, significant evaluation is needed to determine the feasibility of direct bonding GaN and diamond. Current systems all rely on adhesive interlayers to achieve bonding, likely due to insufficient surface quality. If diamond surface quality continues to improve than it is likely that direct wafer bonding can be attempted. Beyond the simple improvements of this process for GaN HEMTs, this idea of thin epitaxial transfer via direct wafer bonding holds promise as a general technique for device fabrication. If general processes can be developed, then devices will be no longer constrained by the limits of epitaxial hope. Overall, this work gives several promising avenues of subsequent research into novel and efficient designs.

Appendix A

Thermal Modeling Method

The following gives a basic derivation of the modeling method. Within a given material layer, Laplace's equation governs heat flow and transfer.

$$\frac{\delta^2\Theta_j}{\delta x^2} + \frac{\delta^2\Theta_j}{\delta y^2} + \frac{\delta^2\Theta_j}{\delta z_j^2} = \nabla^2\Theta_j = 0 \tag{A.1}$$

The last equality being due to the absence in this model of any internal heat generation (as it is assumed heat is solely generated as a interfacial flux at the sources). In Equation A.1, Θ is defined as:

$$\Theta_j(x, y, z) = T_j(x, y, z) - T_{ambient} \tag{A.2}$$

Where the j index is for a given material layer, and z_j indicates the depth in the j'th material layer. Thus, all that is left is to determine the appropriate boundary conditions at both the heat source and sink, the edges, and the epitaxial material boundaries. As the heat sources are interfacial in the z-direction, under a given source Equation A.3 holds.

$$-k_1\frac{\delta\Theta}{\delta z_1} = q \tag{A.3}$$

Here q is the areal heat flux of the source. Elsewhere on the surface, Equation A.4 holds.

$$\frac{\delta\Theta}{\delta z_1} = 0 \tag{A.4}$$

Similarly, at the non-internal edge boundaries either

$$\frac{\delta\Theta}{\delta x_j} = 0 \tag{A.5}$$

or

$$\frac{\delta\Theta}{\delta z_j} = 0 \tag{A.6}$$

govern, as conduction is assumed to be so slow as to be effectively thermally insulating. The final boundary conditions are those between material layers, and that to the heat sink. At the heat sink with a given heat transfer coefficient h_s, the condition is:

$$-k_N \frac{\delta\Theta}{\delta z_N} = h_s \Theta_N(x, y, t_N) \tag{A.7}$$

And between layers n, n+1 with

$$-k_n \frac{\delta\Theta}{\delta z_n} = h_n[\Theta_n(x, y, t_n) - \Theta_{n+1}(x, y, 0) \tag{A.8}$$

$$k_n \frac{\delta\Theta}{\delta z_n} = k_{n+1} \frac{\delta\Theta}{\delta z_{n+1}} \tag{A.9}$$

where the partial derivatives are evaluated at $z_n = t_n$ and $z_{n+1} = 0$. Thus, the above descriptions fully specify the problem. To find a specific value, a Fourier solution to these equations can be found. While the exact derivation is beyond the scope of

this work, rigorous solutions have been found for a variety of conditions, including non-perfect boundaries, multiple sources, and convection in the source plane [55, 56]. These solutions utilize heat spreading function in each layer. In general the form of the solution is:

$$\begin{aligned}\Theta_n(x,y,z_n) = A_{0,n} + B_{0,n}z + \sum_{i=0}^{\infty} A_{1,n}cos(\lambda_i x)[cosh(\lambda_i z_n) - \phi_n(\lambda_i)sinh(\lambda_i z_n)] \\ + \sum_{j=0}^{\infty} A_{2,n}cos(\delta_j y)[cosh(\delta_j z_n) - \phi_n(\delta_j)sinh(\delta_j z_n)] \\ + \sum_{i,j=0}^{\infty} A_{3,n}cos(\lambda_i x)cos(\delta_j y)[cosh(\beta_{i,j} z_n) - \phi_n(\beta_{i,j})sinh(\beta_{i,j} z_n)]\end{aligned} \tag{A.10}$$

Where $\phi_n(\gamma_i)$ is the spreading function for a given layer and eigenvalue. The benefit of this method is that these spreading functions can be recursively found. $\Theta_n(x, y, z_n)$ can therefore be numerically computed by using a finite sum of Fourier coefficients. For the system described above, the recursive relation is given by Equation A.11 and Equation A.12.

$$\phi_n(\gamma_i) \equiv \frac{B_{k,n}}{A_{k,n}} = \frac{\frac{k_n}{k_{n+1}}tanh(\gamma_i t_n) + \phi_{n+1}(\gamma_i) + \frac{k_n}{h_n}\gamma_i\phi_{n+1}(\gamma_i)tanh(\gamma_i t_n)}{\frac{k_n}{k_{n+1}} + \phi_{n+1}(\gamma_i)tanh(\gamma_i t_n) + \frac{k_n}{h_n}\gamma_{i+1}\phi_{n+1}} \tag{A.11}$$

$$\phi_N(\gamma_i) \equiv \frac{B_{k,N}}{A_{k,N}} = \frac{1 + \frac{k_N}{h_s}\gamma_i tanh(\gamma_i t_N)}{\frac{k_N}{h_s}\gamma_i + tanh(\gamma_i t_N)} \tag{A.12}$$

Appendix B

Sensitivity Analysis for Time Domain Thermoreflectance Measurements

The following plots show the sensitivity analysis of the bonded GaN/SiC samples using the standard method for the TDTR system [98]. When fitting in the amplitude R, the sensitivity is found by

$$S_{R,x} = \frac{dln(R)}{dln(x)} \tag{B.1}$$

where x is the delay time, or frequency if doing frequency domain thermoreflectance (FDTR). If using fitting in system phase, then:

$$S_{\Phi,x} = \frac{d\Phi}{dln(x)} \tag{B.2}$$

The sensitivity of the fit was determined for both phase and amplitude fits in TDTR and FDTR measuring configurations. The following four plots show that analysis for three different GaN thicknesses. In each plot, either R or Φ is fit either in delay space or frequency space. In these plots, interface 1 signifies the Al/GaN TBR, interface 2 signifies the GaN/SiC TBR. Ideally, there is maximum sensitivity difference between

interface 2 and the other two lines.

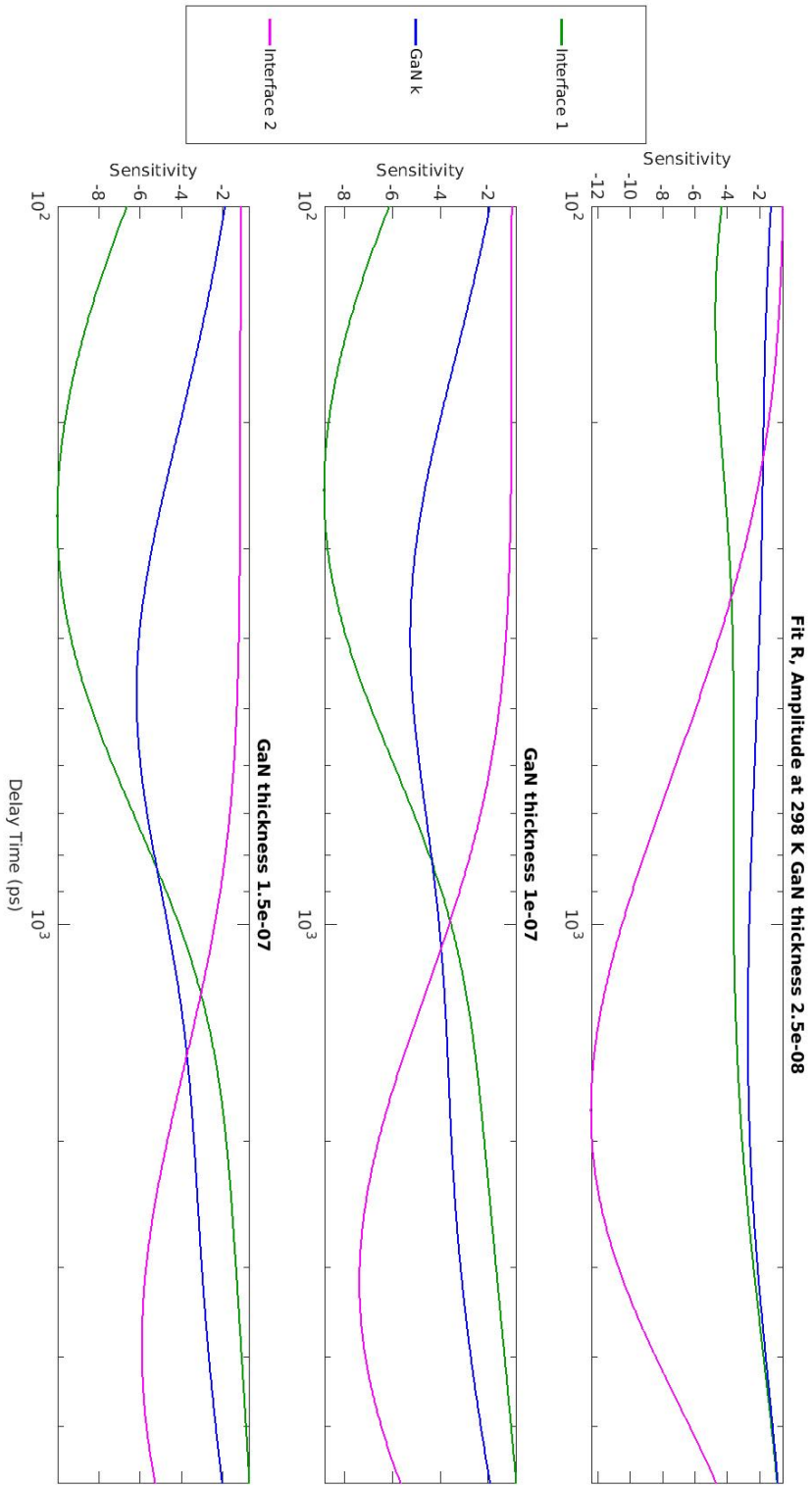

Figure B-1: Sensitivity analysis, fit R in delay space

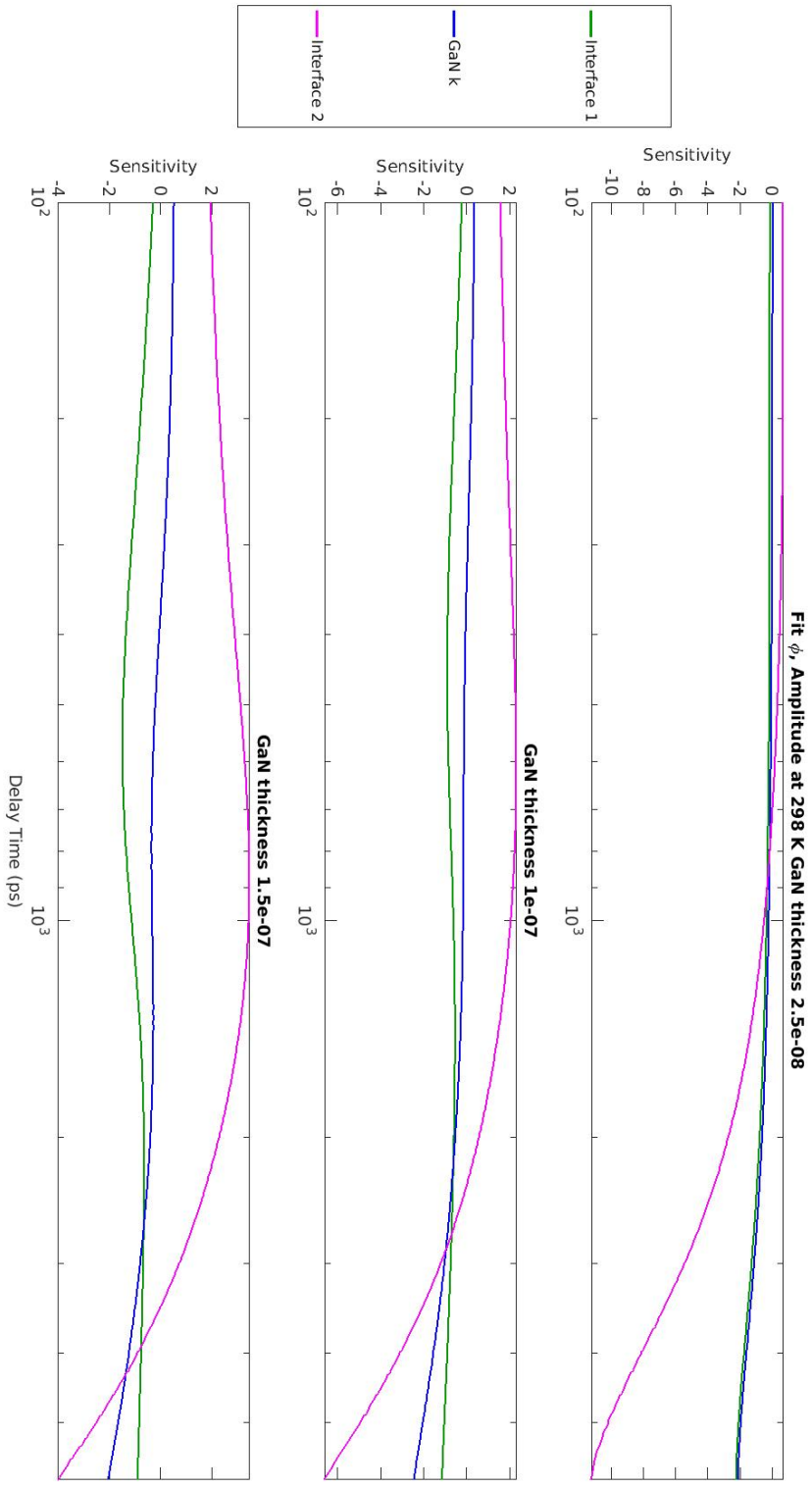

Figure B-2: Sensitivity analysis, fit Φ in delay space

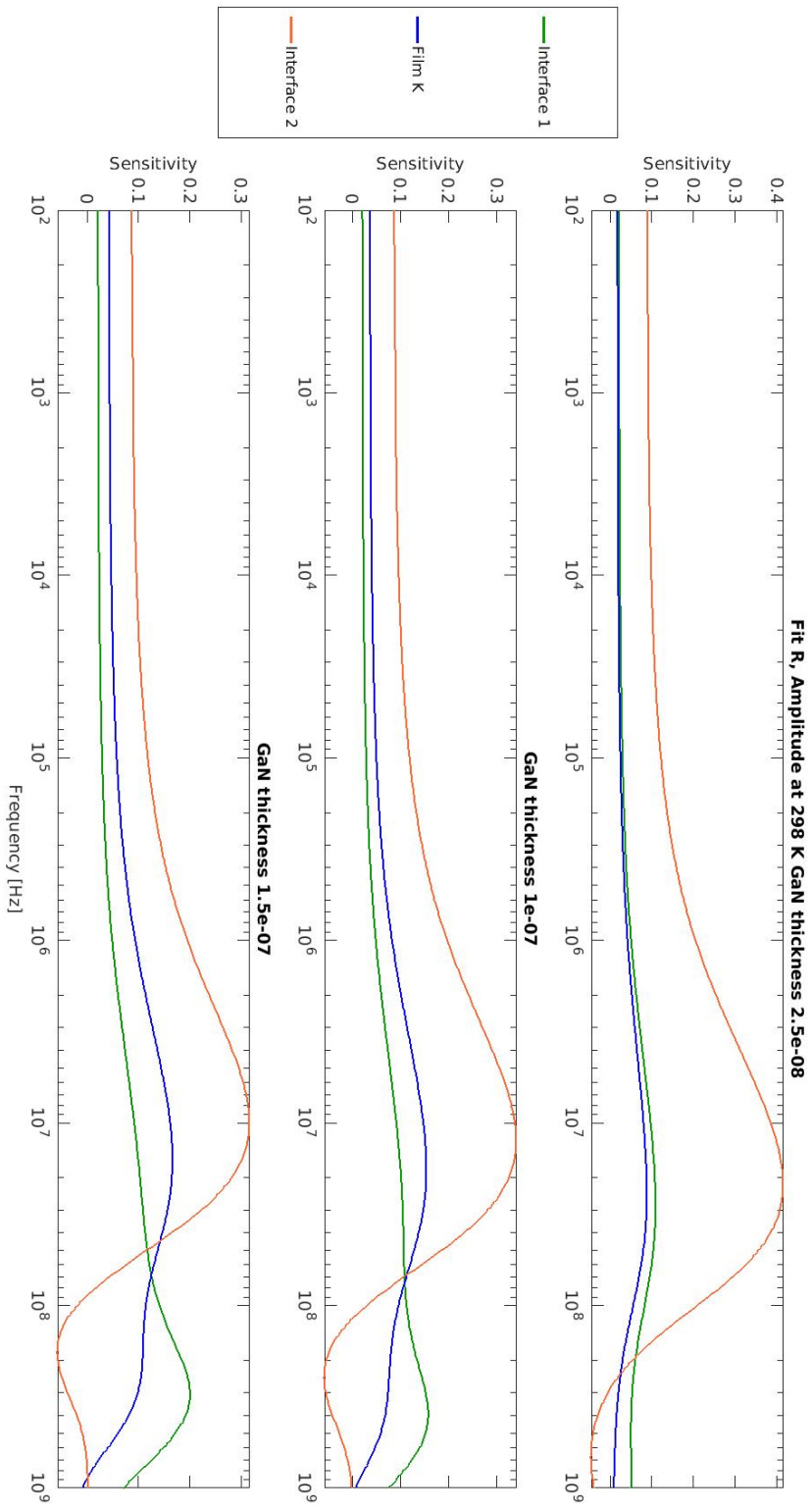

Figure B-3: Sensitivity analysis, fit R in frequency space

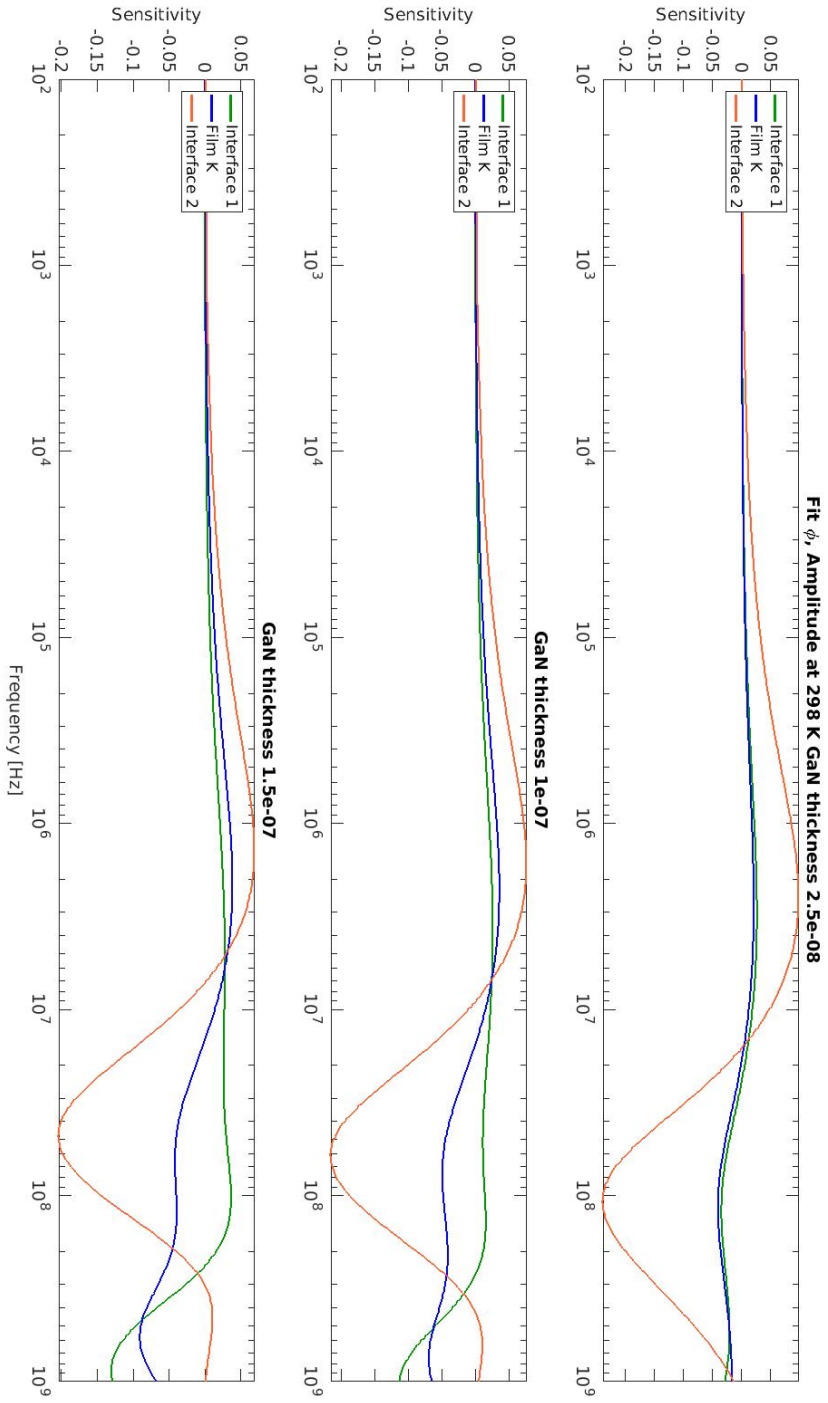

Figure B-4: Sensitivity analysis, fit Φ in frequency space

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