Terahertz Beam-Steering Imager Using a Scalable 2D-Coupled Architecture and Multi-Functional Heterodyne Pixels

by

Guo Zhang

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

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Abstract

The topic covered by this thesis is the project of designing a terahertz imager chip on nowadays commercialized mature silicon platform. In the project, we developed the design method of a multi-functional heterodyne pixel and a scalable array architecture. The pixel is a compact electromagnetic structure simultaneously performs voltage-controlled 140 GHz local oscillation, 280-GHz-signal receiving, sub-harmonic mixing, and intermediate frequency (IF) signal extraction. Each pixel consumes 10 mW power and achieves a sensitivity of 2.9 pW in simulation. The local oscillator (LO) of the pixel is phase coupled with its neighbors; the whole oscillator array is then stabilized by an on-chip THz phase-locked loop. This architecture gives excellent array scalability. First, the LO power is evenly distributed and does not degrade in a larger array scale as a normal centralized array does. Second, the phase noise of the coupled LO network improves linearly with the array size. The simulated phase noise at 1-MHz frequency offset is -90 dBc/Hz for an 8×8 array and -101 dBc/Hz for a 32×32 array. This chip is capable of digital beam steering, too. The first version of the chip prototype with a 10×10 array is fabricated using a 130-nm SiGe BiCMOS process and tested.

Thesis Supervisor: Ruonan Han
Title: Assistant Professor of Department of Electrical Engineering
and Computer Science

Acknowledgments

Firstly, I should thank my thesis supervisor Prof. Ruonan Han for this work. Ruonan provided the core idea, useful simulation and also part of the layout, especially the challenging layout of the pixels in this thesis. These things gave me a starting point.

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Last and also the most important, I would like to thank my parents and girlfriend for all they have given to me. Their endless love make me strong. They never question about me, never doubted about my ability, always encourage me when I am low and always praise me when I am hardworking or doing something good. I cannot imagine how I can survive these 2 years without their understanding and support.

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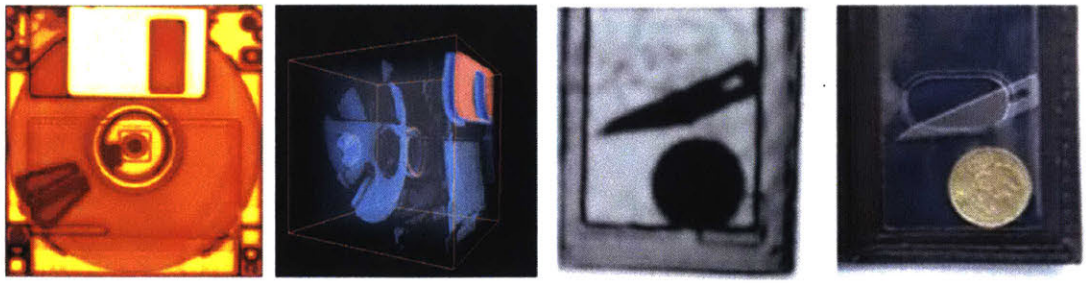
Chapter 1

Backgrounds

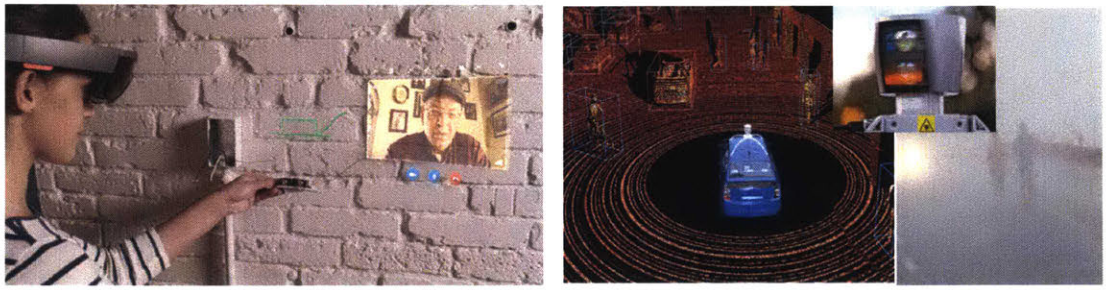
Terahertz (THz) imaging is gaining increasing potentials in industrial quality control (figure 1-1a), security screening (Figure 1-1b), and accurate distance mapping for short-range applications such as robots, augmented reality (Figure 1-1c), and virtual reality sensing [8, 9, 12, 13]. With the development of a high-power THz illumination source [1, 6, 7, 10, 19], future deployment of THz imaging in autonomous vehicles is also possible in order to complement lidar, which fails to operate under foggy and dusty conditions (Figure 1-1d), as well as microwave/mmWave radar, which does not provide high resolution. An ideal imager calls for high spatial/ranging resolution, high sensitivity, fast scanning speed, and low SWaP-C (size, weight, power, and cost). A THz imager formed by a large-scale heterodyne sensing array in a silicon integrated circuit provides the opportunity to achieve all these requirements at once.

The organization of the thesis is as following: We discuss about the backgrounds of THz imager on chip and the design methodology called highly-versatile electromagnetic structure in the following part of chapter 1. We then described how we design the muti-functional pixel by versatile on-chip electromagnetic structure in detail in chapter 2 and how we design the chip architecture in chapter 3. Then in chapter 4 we discussed about our simulation and experiment results and corresponding analysis of the prototype chip. Finally in chapter 5 we make a summary of the whole thesis.



(a) Industry quality control [13]

(b) Security screening [8]



(c) Augmented reality

(d) Automotive driving

Figure 1-1: Possible applications of THz imaging

1.1 On-chip terahertz imager

Differen ways of making an on-chip THz imager has been reported before. Usually, they can be divided into two groups based on their scheme of detection, homodyne detection or heterodyne detection.

Homodyne detection makes use of the nonlinearity of the detector devices. Suppose the input-output relation of a detector device is

$$V_{homoOut} = a_1 V_{in} + a_2 V_{in}^2 \tag{1.1}$$

When we inject a signal $V_{in} = A_{in} cos(\omega_0 t + \phi_0)$ into the detector, the square term of equation (1.1) gives us a DC term $V_{DC} = a_2 A_{in}^2/2$ by triangular formula. We often use chopping method here to reduce flicker noise or to reduce the DC intereference from other sources. Because chopping is like to modulate the DC signal thus its center frequency will move away from DC. Taking chopping into account, our the

fundamental tone of the final measured signal is

$$V_{homoMeasure} = \frac{a_2 A_{in}^2}{\pi} cos(\omega_{chopping} t + \phi_{chopping}) \tag{1.2}$$

where $\omega_{chopping}$ and $\phi_{chopping}$ is the frequency and initial phase of the chopping control signal.

This scheme is relatively easier to implement by circuits thus early attempt on THz imager are mostly based on homodyne detection [3, 9, 15, 18]. It is also easier to form a larger array because homodyne detector's less complex structure can be easier put under the limited area under the antennas. This property becomes more useful when frequency goes higher as the antenna size shrinks together with the wavelength λ. Combined with its no requirement for local oscillation signal for detection at high frequency, which is as hard as making a high frequency source, nowadays this scheme find its advantage on large array size, high detection frequency and broad-brand imaging ability.

In [14], a 8 $\times$ 8 imager array based on diode connected NMOS is reported to working best at 823 GHz. In [3], a 32 $\times$ 32 imager array implemented on CMOS platform with NMOS as detector device is reported to have a 3-dB bandwidth of at least 790-960 GHz. In [4], another MOSFET based 31 $\times$ 31 imager array is reported to image from 200 GHz to 2.5 THz. And higher frequency single pixel homodyne detector based on CMOS platform has already achieved 9.74 THz by using Schotty-barrier-diode [2].

The drawbacks of homodyne imager is as severe as as its advantages. It is a wide-band detector thus it can not tell what frequency it is exactly looking at. In heterodyne detection, we mix the received signal $V_{in} = A_{in} cos(\omega_0 t + \phi_0)$ with a local oscillation signal $V_{LO} = A_{LO} cos(\omega_{LO} t)$ and filter out the lower frequency one. Thus the basic formula for heterodyne detection scheme is

$$V_{heteroMeasure} = \frac{A_{in} A_{LO}}{2} cos((\omega_0 - \omega_{LO}) t + \phi_0) \tag{1.3}$$

Comparing equation 1.2 with equation 1.3, we can see 2 more disadvantage of the

homodyne scheme over heterodyne scheme. Less output signal thus less sensitivity when the input signal is weak, which is most of the case for detection or imaging. According to an analysis in [12], the improvement of sensitivity of heterodyne over homodyne can be as high as 40 to 50 dB in some circumstances. Losing of phase information, which is a key factor for beam-steering. Nowadays all the imagers at THz range are using mechanical scanning, and this makes the imaging system quite bucky and low efficenct.

Different method for design on-chip homodyne imager has been tried in THz range. In [17], a 2 $\times$ 2 heterodyne imager array is formed based on multiplier chain and harmonic mixer. In [16] a single heterodyne imager pixel is formed by injection locking. And in [12], a 8 cell array is formed by an on chip PLL and power distribution network. The previous array design are using a kind of centralizing LO and distributing method [12], or using a LO generation structure whose size is far larger than the antenna's [16]. Thus when array size becomes larger, the even distribution of enough amount of LO power to different pixels with the same phase become more and more challenging. This make the previous methods hard to scale.

High sensitivity in detection, low phase noise for the LO signal, and large array size thus large physical aperture on chip, we propose to address all of these challenging problems for an ideal imager at once with our scalable heterodyne imager array based on an innovatively designed highly-versatile electromagnetic structure on chip.

1.2 On-chip highly-versatile electromagnetic structure design

Electromagnetic (EM) structures such as wave guides, transmission lines, baluns, filters and antennas have been keeping playing vital roles in microwave engineering and vacuum electronics as essential parts of large systems. However, with the operation frequency of chips becoming higher and higher, especially when the frequency is high enough that the wave length is comparable with or smaller than the chip size,

integrated EM structure also begin to find possibilities in chip design.

A representative early work on this trying can be found published in 2000 [5] where researchers tried to investigated the feasibility of doing clock distribution on chip through wireless signal. So they integrated an antenna on chip. However, the working frequency of the system is so low at that time thus the EM structure is big and finally only one single on chip EM structure is feasible for a reasonable total chip size, a 2 mm $\times$ 10 μm short dipole, which plays a simple role but nowhere a simply ignored size. This design mark as the first step towards a more complex, larger scale and more functional integrated EM structure on a single CMOS chip.

The situation expected happens at THz range, where the wave length become 1 mm at 300 GHz and 100 μm at 3 THz in free space. And when operate on chip, the wave length is even a little smaller because the on-chip medias are usually SiO_2, Si_3N_4 and Si. All of them have a ϵ_r larger than 1 and will slow down the EM wave thus result in smaller wavelength. The EM structure now can be confined into dimensions of 10s or 100s microns and making an on chip system with an antenna array with other funcional part become feasible.

For example in [10] , the EM structures around the transistors in the radiator pixel simultaneously perform 250 GHz oscillation, 1 THz radiation, and mutual pixel coupling. In [19] , the Active Molecule Probe (AMP), a transistor and EM structure combination that designed to work in 10 different channels from 220 GHz to 320 GHz by only slight modification, performs frequency doubling, heterodyne down mixing, and signal radiation at the same time. These kind of versatile EM structure enables the highest on chip CMOS radiation power [10, 11, 22] around 1 THz and rapid, wide-range gas detection with absolute specificity [19, 20, 21, 22] from 220 GHz to 320 GHz.

These designs are already big enough steps from the early attempt but are still away from the limit. As compared to the size of active devices on the chip, i.e. the transistors, the passive structures or the EM structures are still dominating in size. Therefore every progress made on the integratability of these passive structures, can give us an increase in the complexity thus functionality of on-chip THz circuit design.

Making the on-chip EM structure more and more versatile is a possible essential way.

In this thesis's imager design, we tried to push this complexity boundary by our EM structure to perform 140 GHz local oscillation, 280 GHz signal receiving, 280GHz sub-harmonic mixing, low frequency IF signal extraction and mutual pixel coupling at the same time in a single pixel that is just the size of a 280 GHz patch antenna, i.e. $\lambda/2 \times \lambda/2$, where λ is the wave length for the 280 GHz on chip EM wave. This method can give us the largest scale and most area efficient heterodyne imager array around 300 GHz with the highest sensitivity.

Chapter 2

Multi-Functional Pixel Design

We are using heterodyne detection scheme, and thus a frequency controllable local oscillation signal is needed in each imager pixel. The signal has to be both low phase noise and high power for better imaging accuracy and sensitivity. We achieved this by our pixel design and the de-centralized LO array architecture described in this and the next chapter.

In each pixel, a return-path gap coupler (RPGC) based self-feeding structure is used to maximize local oscillation power and compress the even mode oscillation of the transistor pair [6, 7]. A 3D structure of the pixel in HFSS simulation tool is shown in Figure 2-1. It looks like a slotted box.

The fundamental oscillation of the pixel is designed to be around 140 GHz and we use the 2nd harmonic to mix with the near-280-GHz signal we are going to illuminate the target with. In the real imaging case, the fundamental oscillation frequency and the illuminating signal frequency has to be carefully chose so that the IF frequency is within the measurement equipment's range as well as provide a lower noise floor.

The orthogonality of different EM wave mode is the core to achieve multiple function in the limited area.

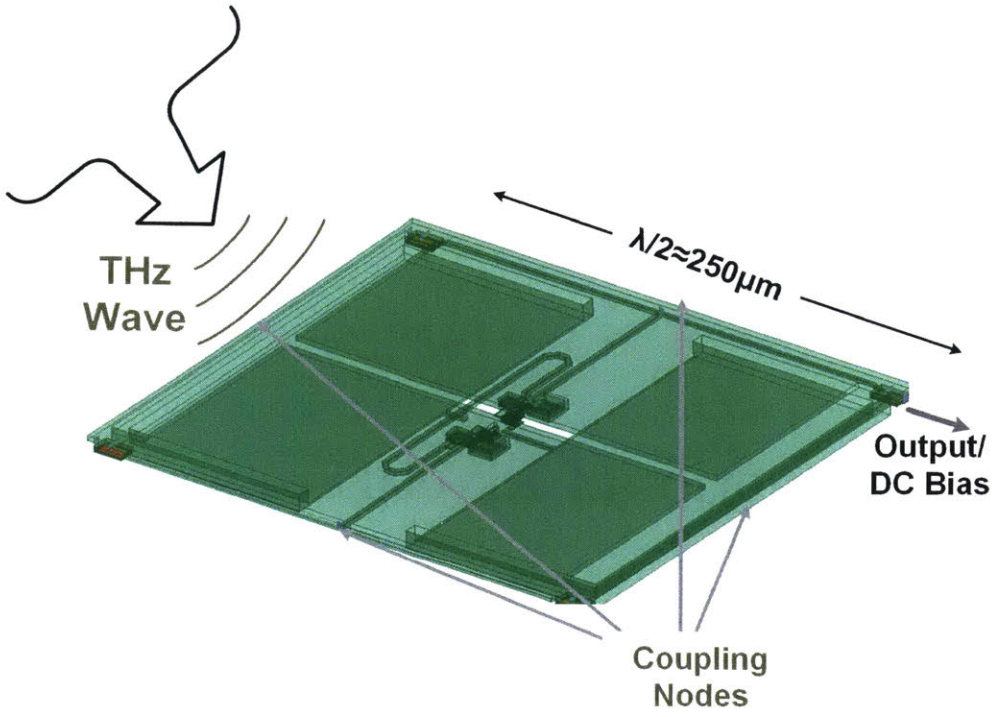


Figure 2-1: 3D structure of a pixel shown in HFSS

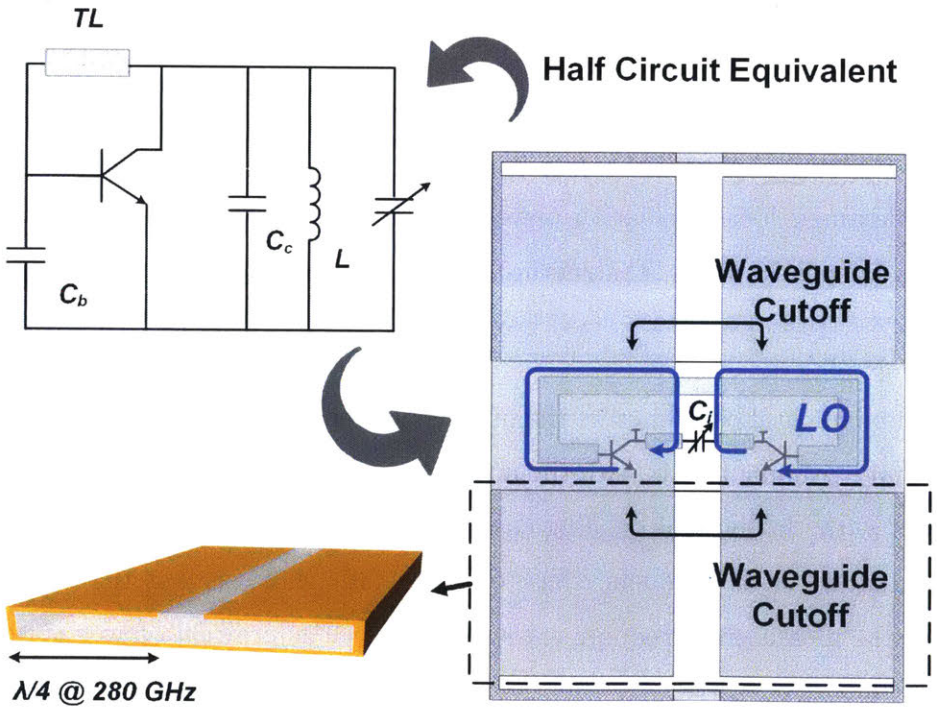


Figure 2-2: Principle of the the fundamental oscillation

2.1 Fundamental oscillation generation

Figure 2-2 shows the fundamental oscillation principle of the pixel, including the equivalent half circuit schematic, the phase relation of the fundamental oscillation signal, and the cut-off wave guide structure. Note that the capacitors connected to the emitter of the transistor, C_b and C_c are not presented in the EM structure on the right in order to simplify the expression.

The core of the pixel is a self-feeding oscillator, the micro strip transmission line and the RPGC structure in the middle of the pixel act as the self-feeding path and is presented as TL in the schematic. The pixel is a leaky wave antenna structure for 280 GHz. So the distance from the center to the side wall of the box which act as the ground, is quarter wave length. Thus, when working at the 140 GHz fundamental frequency, this half antenna becomes a $\lambda/8$ fat transmission line, and transform the ground on the side wall into a inductor as we see in the schematic.

The RPGC structure support the TEM mode wave propagation while reject the TM mode wave [7]. This means when the 2 transistors in the pixel are oscillating out of phase, the power can flow through this coupler in the form of TEM wave and a loop for self-feeding can be formed. Proper design of the electrical length and impedance of the PRGC and transmission line of the loop can form a positive feedback and maximize the devices oscillation power at fundamental frequency. The details about the calculation of these lengthes and impedances can be found in [6, 7]. On the other hand, if the 2 transistors are oscillating in phase,then the wave wants to propagate along the RPGC will be a TM mode wave, it will be cut off in this structure and no feed-back loop can form in this case. Thus the 2 transistor will be stable and no oscillation is happening. Therefore, even mode oscillation is compressed while differential mode oscillation is supported and optimized.

An important factor for successful oscillation is that the quality factor Q for the resonance tank has to be high enough. Therefore it is important to control the loss of fundamental signal to unwanted places such as radiation or propagation loss. Therefore we change the top and bottom part of the return gap into a leaky

rectangular wave guide structure as shown in Figure 2-2. This wave guide is high pass and has a cut-off frequency of 240 GHz for its TEM mode. Thus fundamental signal is confined into the central part of the pixel. Loss is reduced.

The second harmonic of the oscillator can not radiate neither. Because the fundamental signal is differential and result in the second harmonic's being in-phase on the 2 sides of the gap. It can not propagate along the RPGC or the leaky wave guide structure thus no 2nd harmonic radiation will happen. These 2 mechanisms ensure the high Q of the fundamental oscillation tank.

The final thing needs to worry about is the calculation of C_b and C_c as shown in the Figure 2-2 schematic. The procedure to derive them is adopted from [6, 7] with the assumption that both Y_1 and Y_2 (Figure 8 in [6]) are lossless. The assumption is reasonable because the oscillator is not designed to drive any load and the radiation of both fundamental and 2nd harmonic are compressed. Finally both Y_1 and Y_2 are positive imaginary number and they are realized as capacitors in the design as C_b and C_c.

2.2 Signal receiving and sub-harmonic mixing

The schematic for the signal around 280 GHz is shown in Figure 2-3. Note that at this frequency, the emitters of the transistors are virtually grounded because each of them has a $\lambda/2$ transmission line between between it and a (virtual or RF) ground (see Figure 2-4). Each of the transistors collector is virtually open because it is $\lambda/4$ away from the grounded side wall.

The leaky wave guide at the top and bottom of the pixel working as blockers for fundamental 140 GHz TEM signal but working as antennas for linear polarization wave that is higher than 240 GHz. When a 280 GHz signal with right polarization is shining onto the pixel, it will be received by the antenna and propagate from top and bottom to the center of the pixel where it will be picked up by the microstrip transmission line used for self-feeding before. The signal guided to the base will add up with the 2nd harmonic of the local oscillation. Due to nonlinearity of the

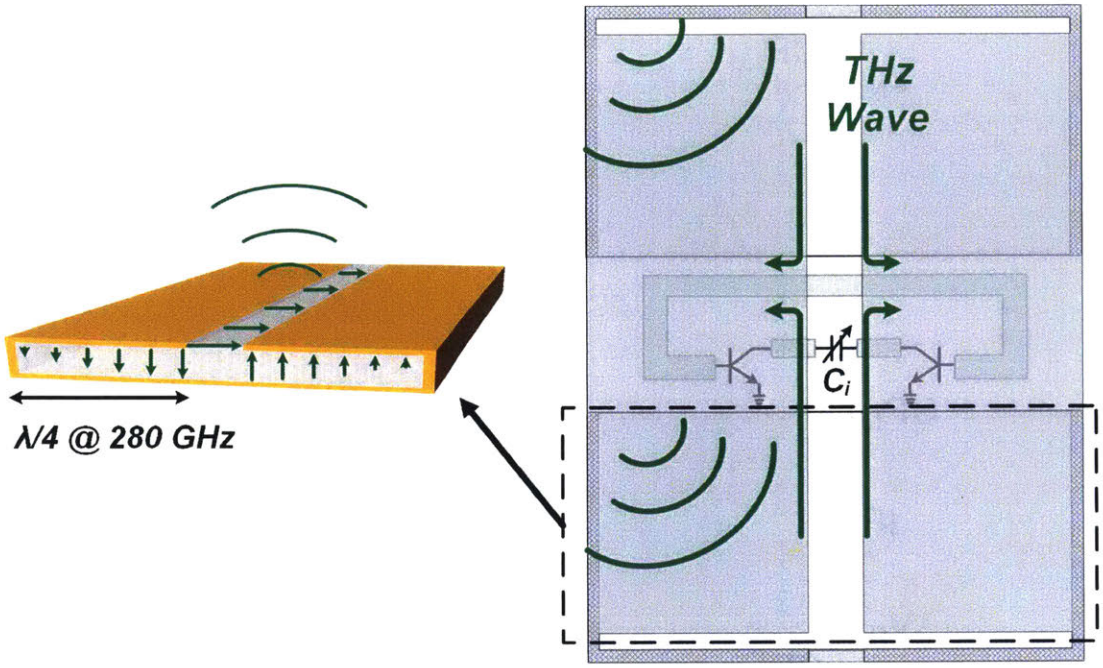


Figure 2-3: Leaky wave guide antenna and received signal path at 280 GHz

transistor's I-V relationship, a multiply term will be found in the current flow out from the emitter. This multiplying term gives us the frequency differential signal, i.e. the down mixing signal, we want.

Note that we are not considering the signal go into collectors because the non-linearity from collector voltage to emitter current is so weak and can be neglected[1].

Let's talk more about the the leaky wave guide antenna. The electric field distribution in the antenna is shown in figure 2-3 when it is radiating or receiving. It can be regarded as a folded patch antenna and thus the two of them has similar properties such as directivity. When combined the up, medium and bottom parts together, the pixel has a simulated gain of 0.9 dB and a radiation efficiency of 41.7%. The interesting part of this kind of antenna is that it is front side radiation, so we can get rid of the lossy path for backside radiation in the silicon substrate. The back side of the chip can now be directed attached to a big metal and get better heat dissipation. And the most important, this structure naturally provided a slot in the middle that can be connected to the RPGC perfectly, making the design more versatile and compact.

[1]We even did not show this signal path in Figure 2-3

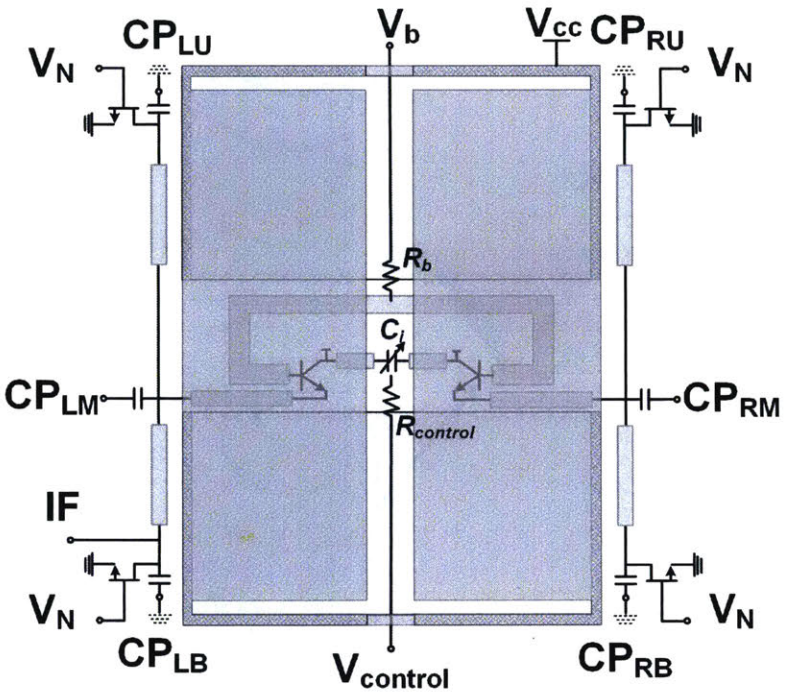


Figure 2-4: Circuit for DC bias and IF signal extraction

2.3 DC bias and IF signal extraction

The DC bias for the pixel is a little complex as we have to deal with multiple frequency that should not be influenced by the DC bias trace.

Firstly, the whole metal box made up with the up and bottom leaky wave guide antenna, the middle RPGC is connected to Vcc, which is the collector bias for the transistors. The transistors' collectors then are connected to the middle of the structure at the 2 edge of the gap to get this feed. The base bias V_b and varactor control voltage $V_{control}$ are then feed through 2 traces in the middle of the pixel. The middle line of the pixel is a virtual ground for the fundamental oscillation as the 2 transistors oscillate differentially. The emitters of the transistors are connected to NMOS current sources. At the drain of the current source a capacitors connected to virtual ground ($CP_{LU,RU,LB,RB}$) are provided. The capacitor value is selected so that at 140 GHz it is shorted while at IF frequency, which is usually several MHz, it is open. the electrical length at 140 GHz from the drain of the NMOS to the emitter is $\lambda/4$ so

what emitters see at the fundamental frequency is open. None of the bias above thus influence the oscillation.

At the middle of the transmission lines connecting BJT emitter and the NMOS drain, capacitors are added. They are used for mutual coupling between pixels, and $CP_{ML,MR}$ are vitual open. The virtual ground $CP_{LU,RU,LB,RB}$ mentioned before is also the result of coupling and boundary condition. They will be explained in detail in chapter 3.

As discussed before in section 2.2, the mixing result is a low frequency small AC current signal flow out from the BJT emitter. This current will change the drain voltage of the current source. We extract it from the drain of the current source which is shown to be virtual ground for fundamental so that oscillation will not be influenced.

Chapter 3

Scalable THz Imager Architecture Design

Coherence between transmitter signal and LO signal of every pixel of the receiver is needed for heterodyne detection. We propose the imaging chip set architecture shown in Figure 3-1. System wise, the illuminating source chip[1] and our imager chip is using the same off chip clock signal f_{ref} as reference. Chip wise, all of the pixel of the imager is a heterodyne detector having its own VCO, antenna and mixer. And each pixel is coupled with its neighbors completely out of phase at the 140 GHz fundamental frequency, thus their 2nd harmonic are all in phase across different pixels. Then a PLL loop is designed on chip to control the whole chip's VCO array and phase lock it to the off chip clock signal we just mentioned.

When a 280 GHz sigal come, each pixel will produce by sub-harmonic mixing and send out its own IF signal at several MHz contains different amplitude and phase information which is determined by the target property and it's position. These IF signal are then selected by on chip MUX and sampled by a off chip lock-in amplifier. Finally a PC processes the sampled data, do digital beam forming and form a image that is seen by the system.

[1]This chip is not contained in this thesis

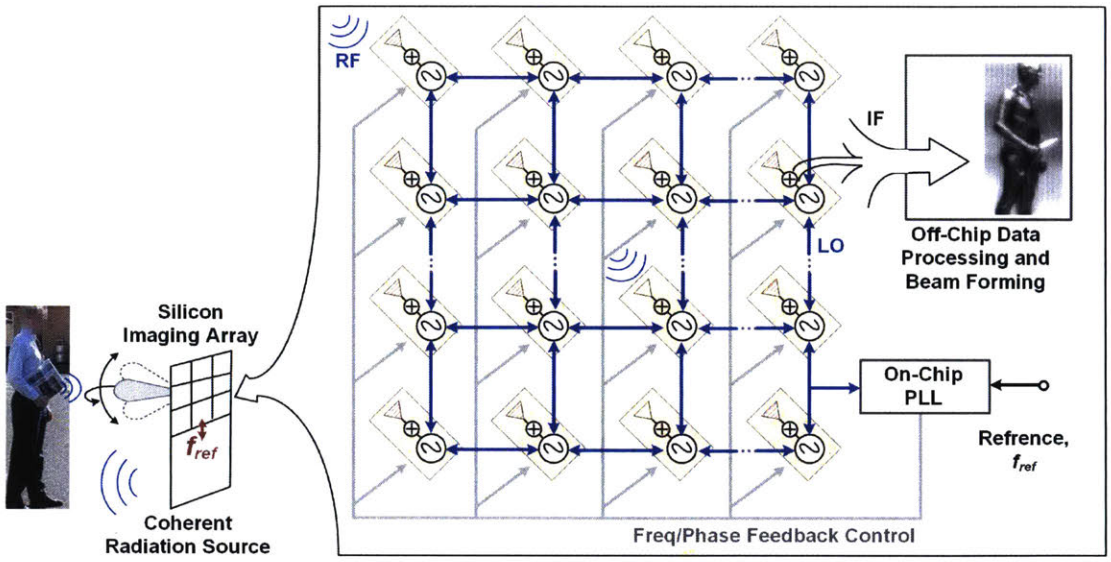


Figure 3-1: Architecture of the imaging chip set and imager chip

3.1 Inter-LO coupling

The way LOs are coupled is shown in Figure 3-2. The core idea of coupling is that only the kind of phase relationship desired between neighbors can result in stable oscillation while other kinds of oscillation modes will die out.

From chapter 2, we know that the oscillation of each pixel is stable only when coupling ports $CP_{LR,RU,LB,RB}$ are (virtual) ground. Thus at the boundary of the array, we direct connect the coupling ports with V_{cc}, which is DC and thus RF ground for fundamental signal; In the middle of the array, we direct connect the $CP_{LB,RB}$ of a pixel with the $CP_{LU,RU}$ of the pixel that is below it. Because virtual ground has to be formed, thus the signal connected has to be completely out of phase. If there is no virtual ground formed, the up and down pixel pair's BJT's emitter will have a load at fundamental frequency and oscillation will be disturbed. This kind of connection assured that every vertical pair is oscillation completely out of phase.

In horizontal direction, we know that the oscillation of each pixel is stable only when coupling ports $CP_{ML,MR}$ are virtual open. Therefore, we directly leave the $Cp_{ML,MR}$ on the boundary floating. For the ones that are connected to their horizontal neighbors, we add a resistor at the middle of each pair. This resistor consumes a lot

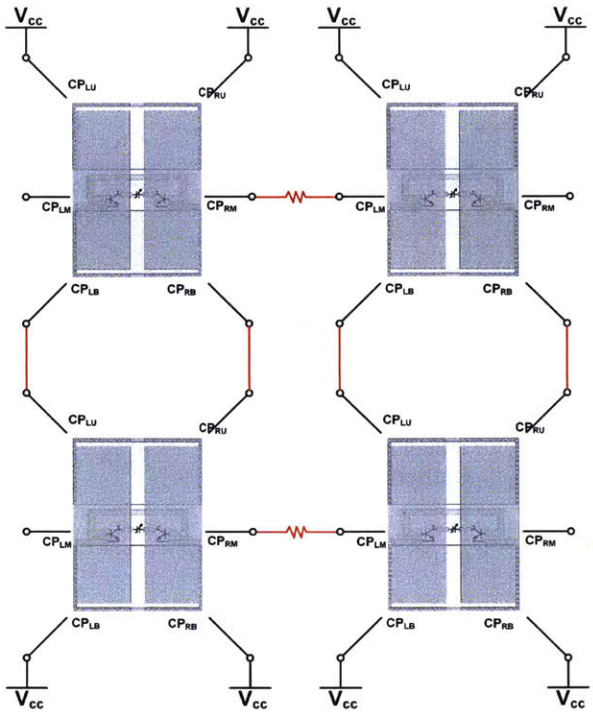


Figure 3-2: Mutual coupling method for LO in different pixels

of power when the signal on its two sides are differential and consumes little power when the signal on its two side are even. Thus the oscillation mode that will provide differential signal on the two ports of the resistor will be drained out by the resistor, which happens when the horizontal pair are oscillation in phase. Thus every horizontal pair also oscillation completely out of phase.

Every pixel is completely out of phase with its neighbors. The whole LO array is coupled together. It is worth noting that in figure 3-2, the pixel seems to be far away from each other. This is just for showing ideas and in actual lay out each pixel is touching each other (see Figure 4-8). Thus the electrical length by this inter pixel connection can be neglected.

3.2 Phase-locked-loop design

A PLL is fully integrated on chip except that its loop filter is designed on PCB board for the ease of tuning, as shown in Figure 3-3. The whole coupled LO array

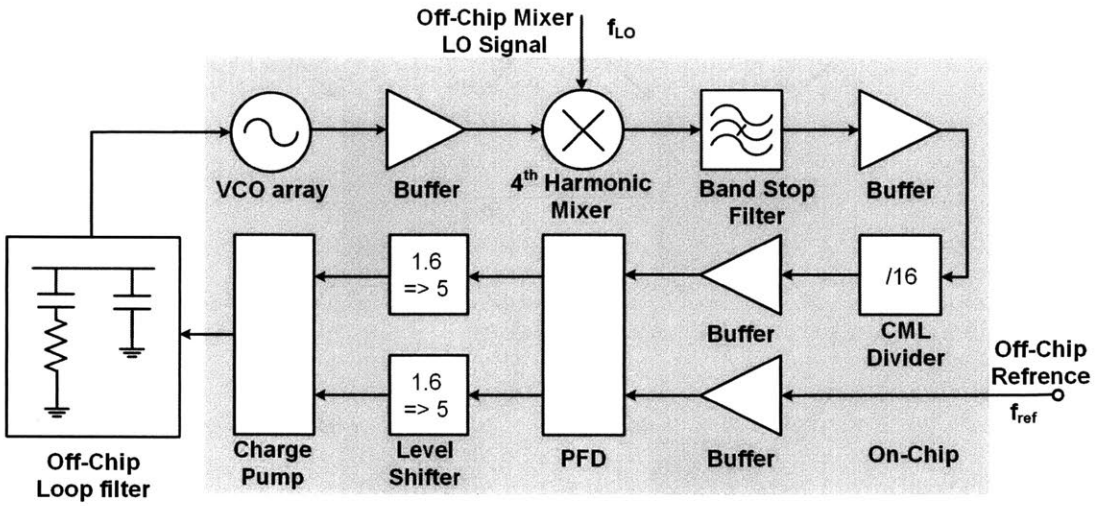


Figure 3-3: PLL architecture

is controlled by the output of the loop filter. The LO signal from a certain one pixel is feed in to the buffer for phase locking. Because the buffer has good isolation and only a small amount of power is dragged from the pixel, the coupling of the whole array should not be influenced.

The amplified LO signal then mix with the 4th harmonic of a 32.5 GHz external signal f_{LO} and produced a 10 GHz down converted signal. This 10 GHz signal is then divided by 16 (a 4 level divided by 2 chain) to 625 MHz and compared with the external reference signal f_{ref}. There are two things that are not always seen in an ordinary PLL. The first is the use of a band stop filter before the CML divider. This filter is an on chip series connected RC resonator to stop the leaky 32.5 GHz f_{LO} signal. Another thing is the level shifter after the phase-frequency detector (PFD) because a larger control voltage is needed for wider range of tuning for the VCO array.

3.3 Pixel selection network

Usually the number of ADCs we can use for IF signal sampling is limited, especially if we want to use lock-in amplifier as an ADC. Thus when the array size goes too large, on chip pixel selection network will be in desperate need. We use shared bus for this

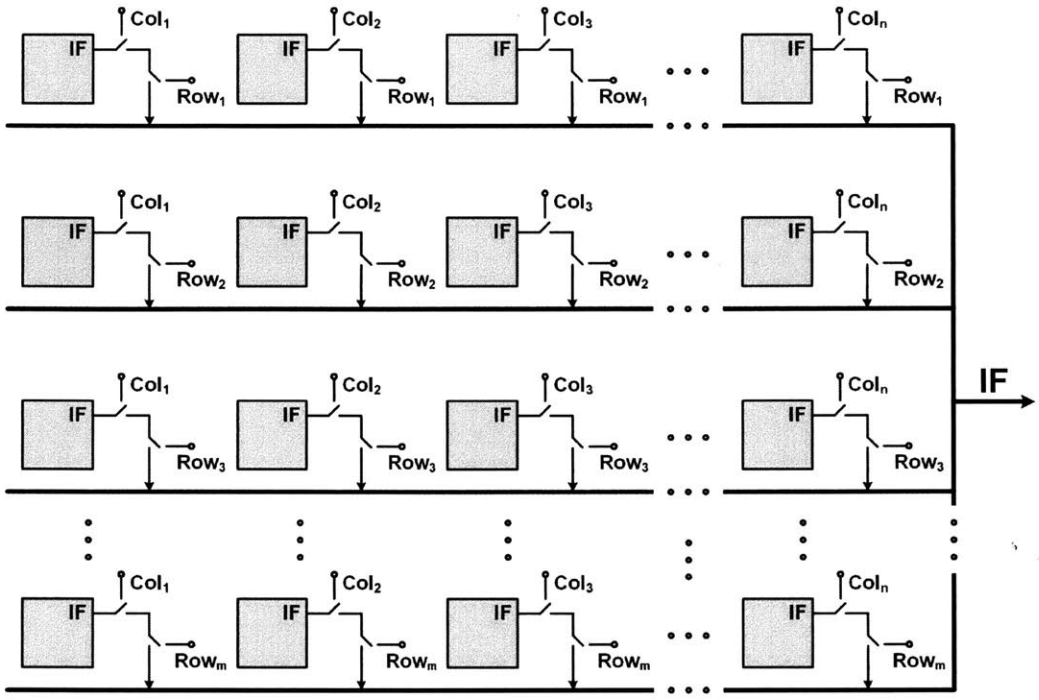


Figure 3-4: Pixel selection network

purpose as shown in Figure 3-4. Every pixel is receiving THz signal and producing its own IF at the same time, but only pixel ij that have both Col_i and Row_j to be 1 is selected, connected to bus and then read out by the on PCB ADC or off-board equipment.

Chapter 4

Simulation and Experiment Results

Some core simulation results reveal the characteristics of the design are presented in this chapter. We also make a tape-out to verify our design. However, early test shows negative result due to a lay out error. Analyses on this are also presented.

4.1 Simulation results

Let's look at the properties of a single pixel first. The DC power of a single pixel is simulated to be around 10 mW. The responsivity of a single pixel is shown in Figure 4-1, which is equal to 60 kV/W without base band amplifier when input power is low ($<$ 0 dBm). And in Figure 4-2, the pixel's output noise is calculated. The noise floor is approximate 8.92 $nV/\sqrt{Hz}$. With a bandwidth of 1 kHz and assumption that the noise spectrum is flat in this 1 kHz, the sensitivity is calculated to be 2.9 pW. This is around 25 $\times$ better than the prior art[12].

Array wise, the simulation result in Figure 4-3 shows that the proposed LO array is working successfully. Strong local oscillation and completely in-phase/out-phase inter-LO coupling across the array are achieved. 2nd-harmonic operations of the pixels are thus all in phase. Phase noise improvement with LO array enlarge is observed as shown in 4-4. This is because the LO power of the network are coherent and are added up constructively, while the noise power is completely uncorrelated and is averaged out. Extrapolate the line and we can predict the phase noise of a 8

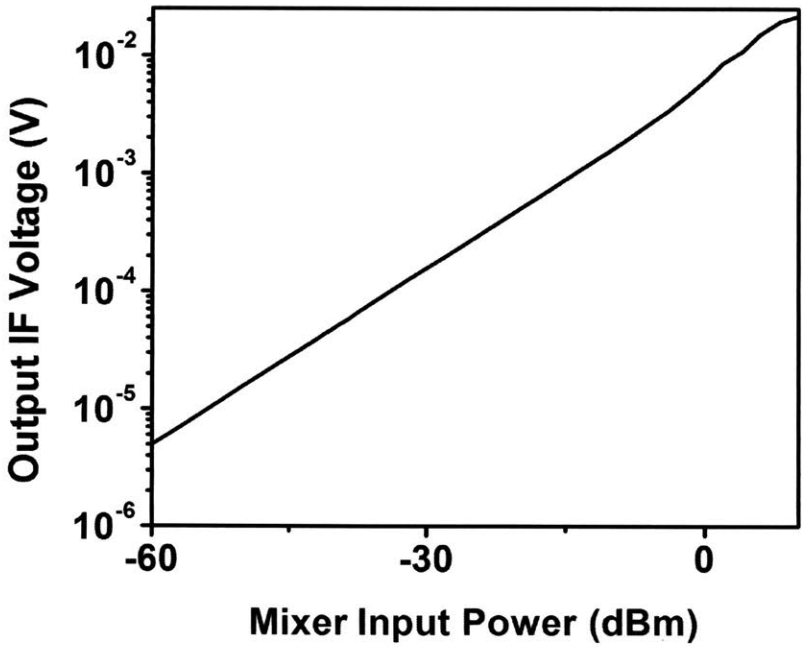


Figure 4-1: Responsivity of the pixel mixer

$\times$ 8 array and 32 $\times$ 32 array will be as low as -90 dBc/Hz and -101 dBc/Hz with Δf = 1MHz.

The directivity of an 8 x 8 and a 32 x 32 array are also calculated and shown in Figure 4-5 and Figure 4-6. We can see that narrower beam from highly scalable array leads to ultra-fine beam-steering resolution (Figure 4-7).

The simulation results show that the whole array is working perfect as we designed.

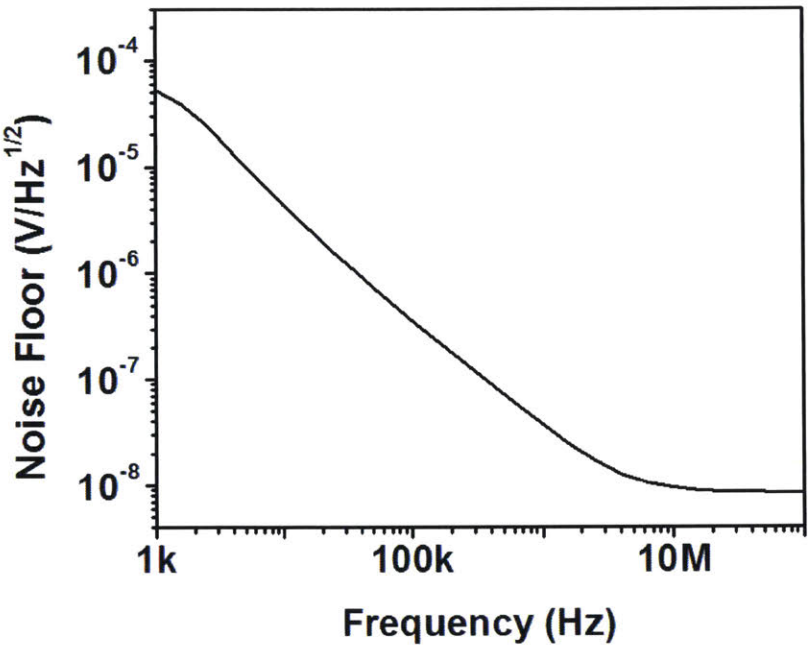


Figure 4-2: Noise output from the pixel

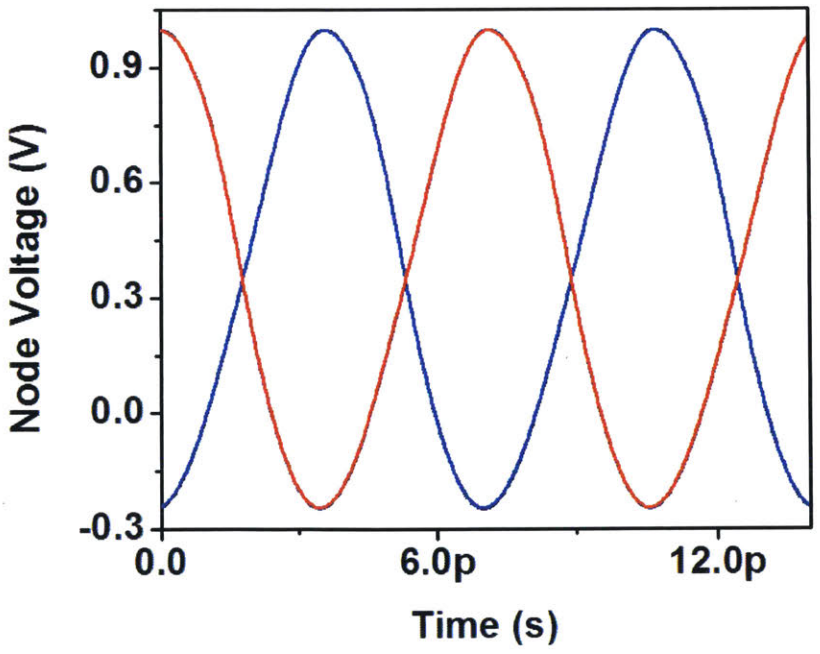


Figure 4-3: The fundamental oscillation of different pixels in the array

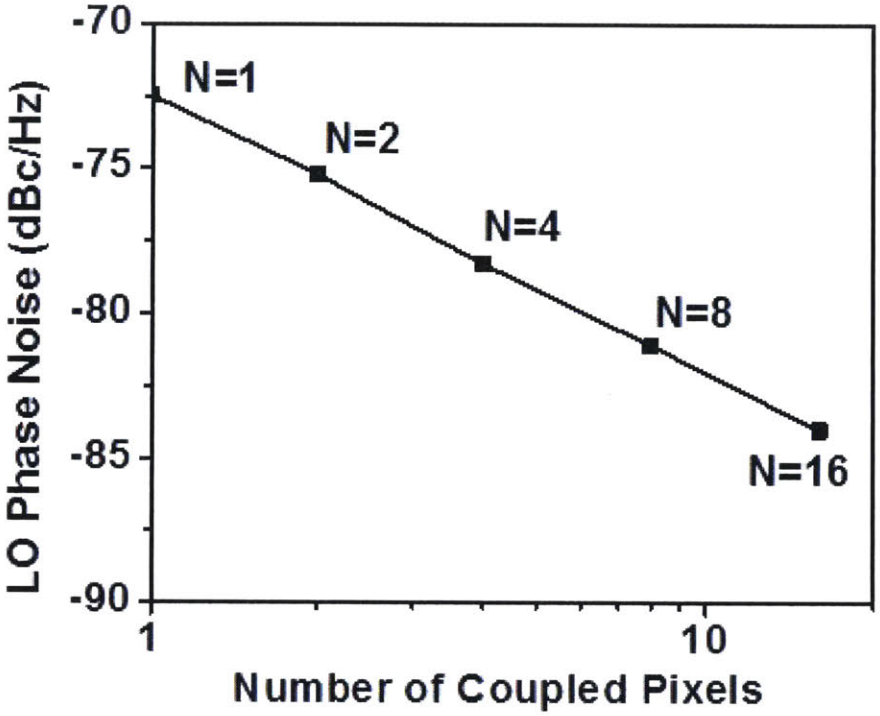


Figure 4-4: Phase noise improvement with scaling

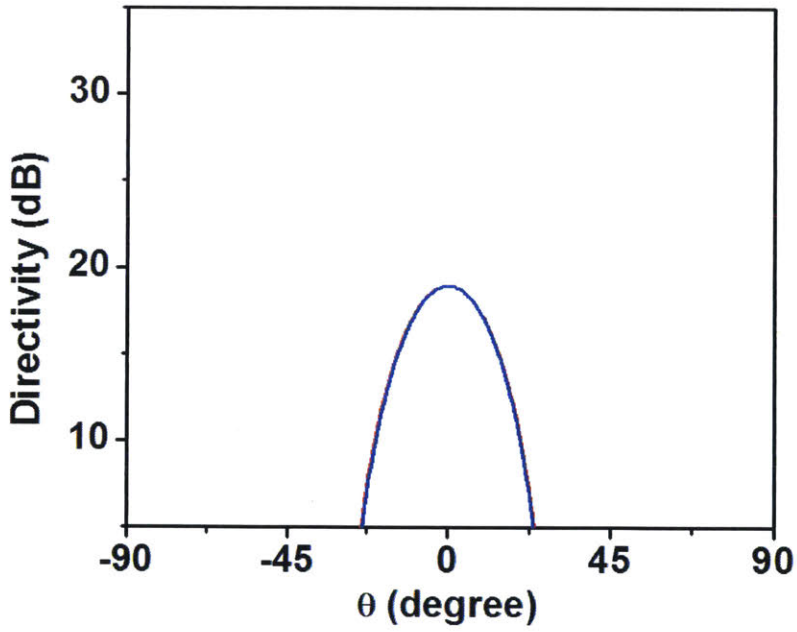


Figure 4-5: Directivity of 8 by 8 array

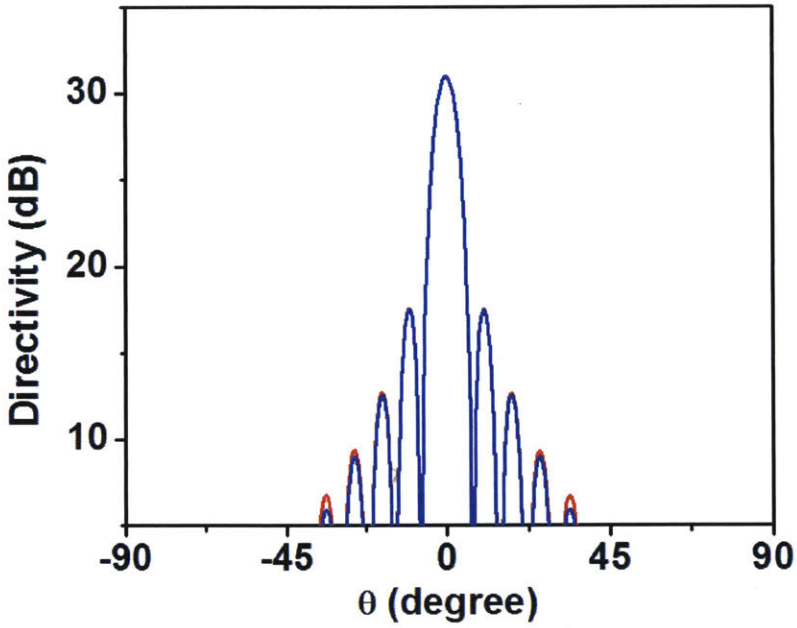


Figure 4-6: Directivity of 32 by 32 array

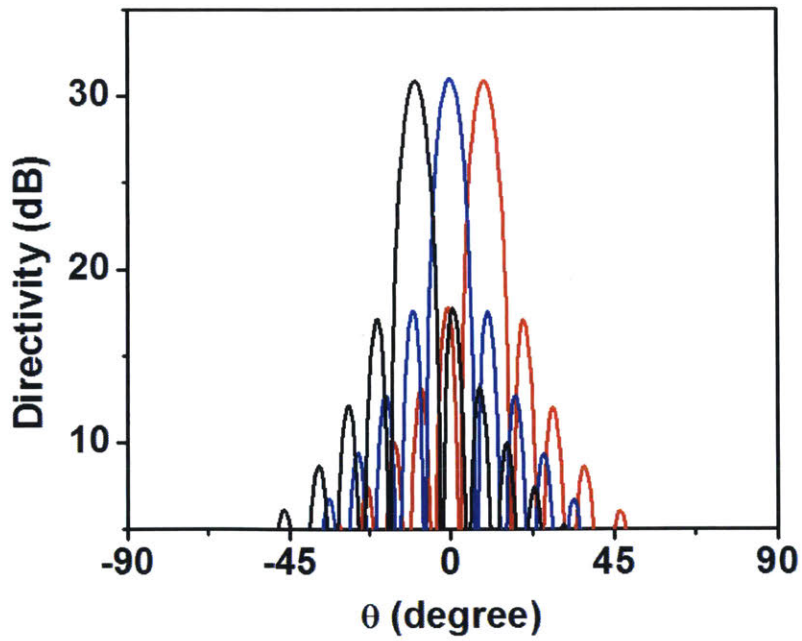


Figure 4-7: Beam-steering on 32 by 32 array

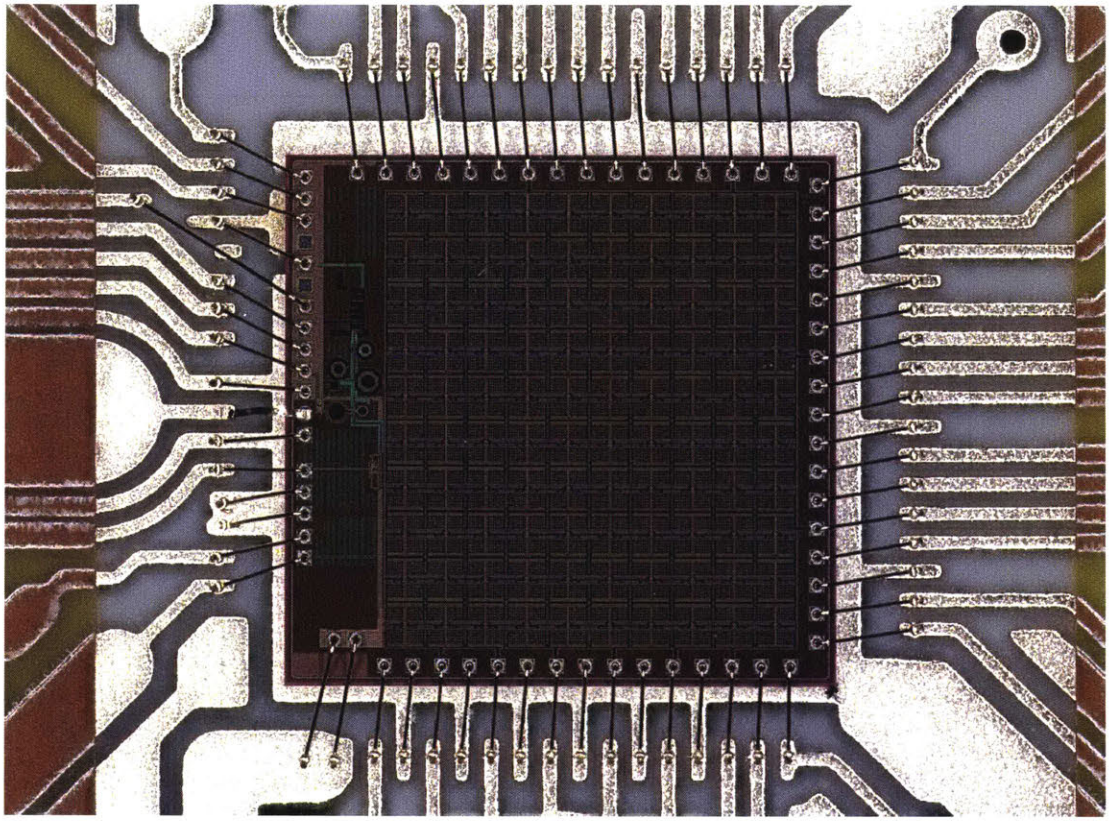


Figure 4-8: Bonded die photo of the 10 by 10 prototype chip

4.2 Chip prototype

We made a chip prototype based on IHP's 130 nm SiGe BiCMOS process. It has HBTs with $f_T/f_{max} = 300/500$ GHz.

The size of the chip is measured by 3.7mm $\times$ 3.6mm. It contains a 10 by 10 heterodyne pixel array, an on-chip PLL (with on PCB loop filter) and an on-chip IF selection network as we have described in chapter 2 and chapter 3. A photo of the chip bonded on a PCB board is shown in Figure 4-8. We can see that the imaging pixels consume the main area of the chip, which means the whole array is efficient in change physical chip area into physical imager aperture due to the area-efficient versatile EM structure design. As can be derived from Table 5.2, this chip has the largest array size and most high imager pixel density in the low THz range, even compared with homodyne scheme imager array, whose complexity is much lower.

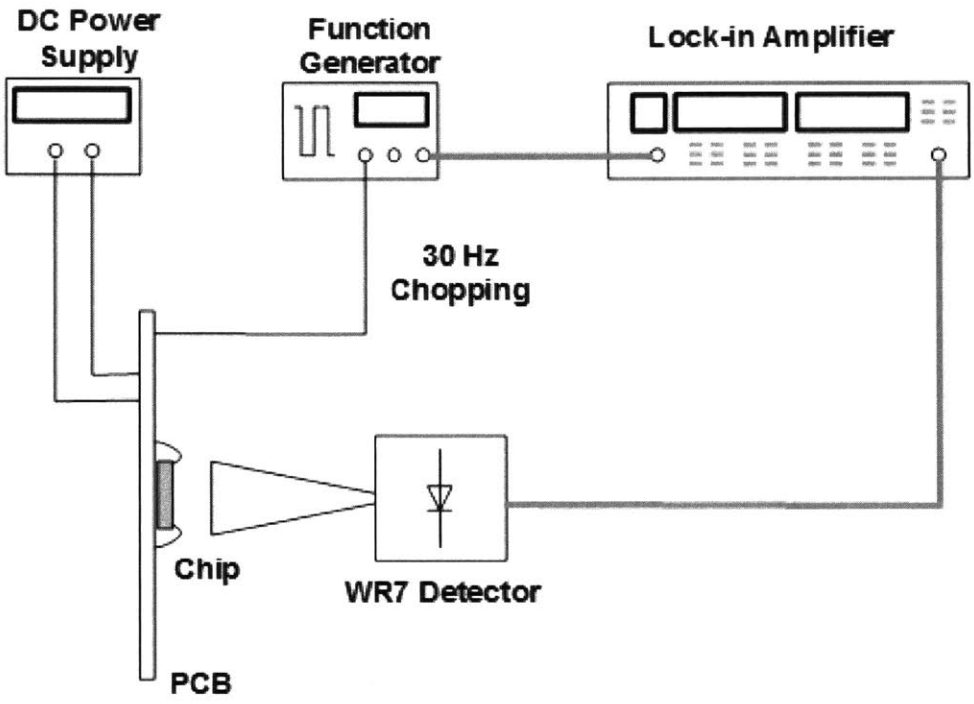


Figure 4-9: Fundamental leakage measurement by WR8 diode detector

4.3 Measurement and analysis

We did measurement for the chip. All the DC bias match perfectly with the simulation. However, we can not find enough clue that the array oscillates.

The first measurement we tried is to use WR7 diode detector to measure the leakage of the fundamental signal of the chip. The set up is shown in Figure 4-9. Different chips show different results in this measurement. But all are very close to the noise floor of the measurement system. This means nearly no fundamental leakage is detected.

We then tried to use a WR8 even harmonic mixer to repeat the measurement. The set up is shown in Figure 4-10. Also no IF signal that is associate to the fundamental oscillation leakage is observed.

The third approach we tried is to produce a illuminating signal and sweep around 280 GHz, trying to observe the IF produced by the 2nd harmonic mixer of the chip as shown in Figure 4-11. Unluckily, we still did not find anything.

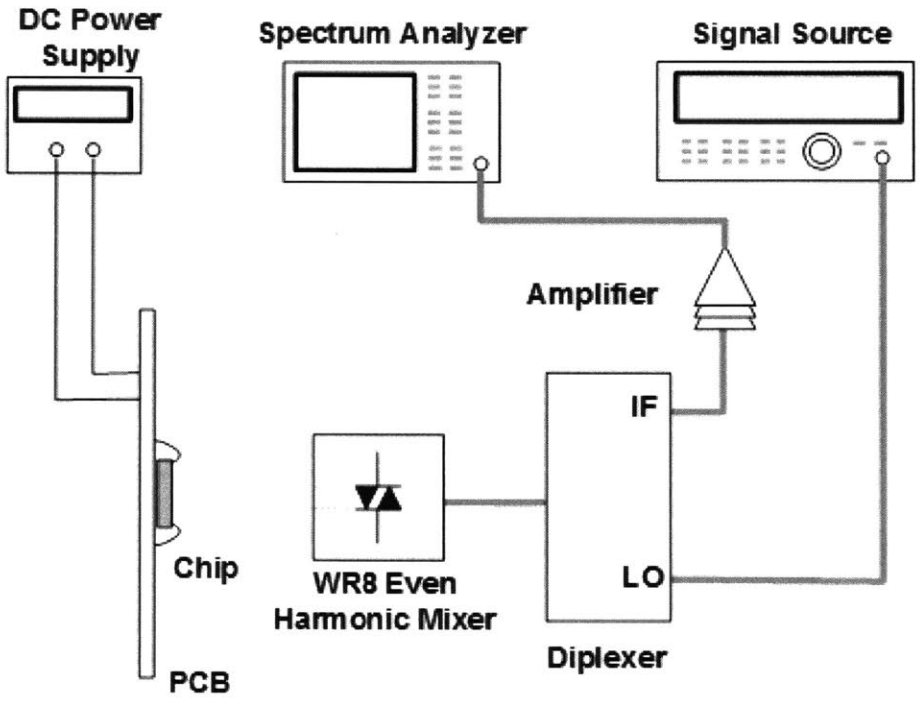


Figure 4-10: Fundamental leakage measurement by WR8 even harmonic mixer

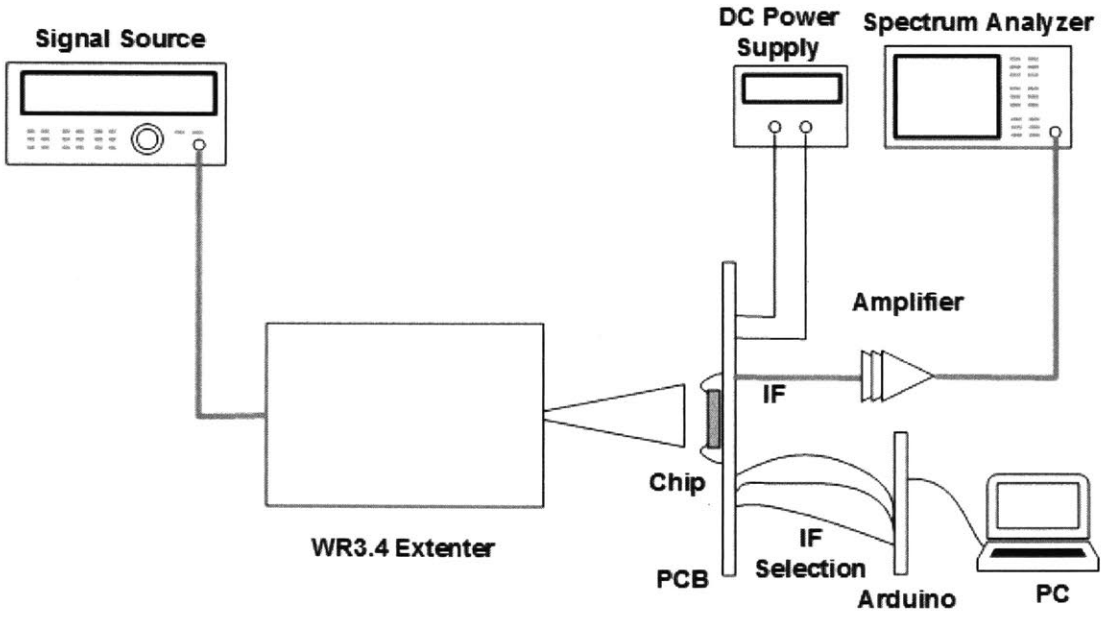


Figure 4-11: IF signal measurement

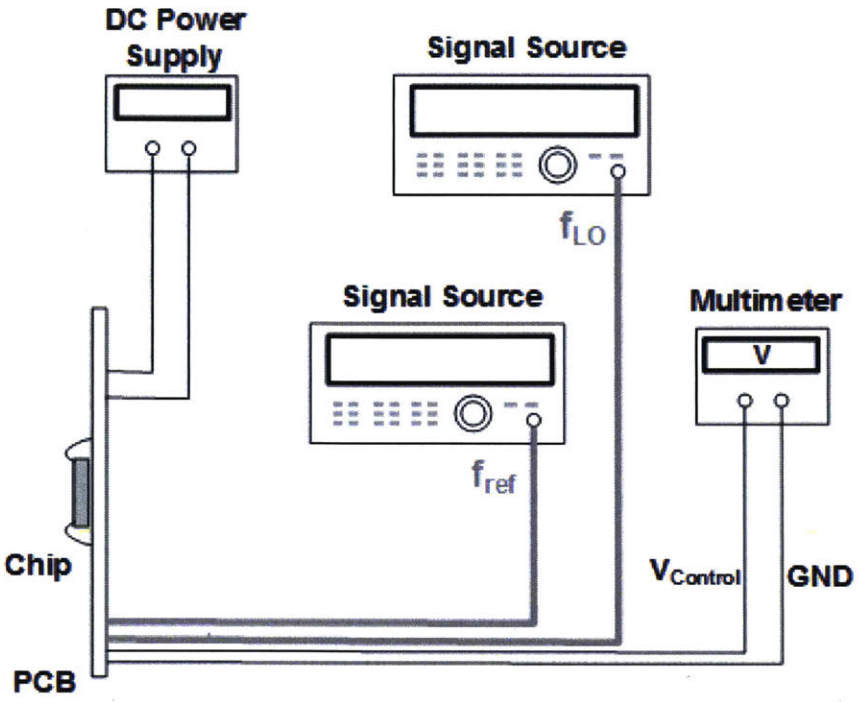


Figure 4-12: Charge pump output measurement

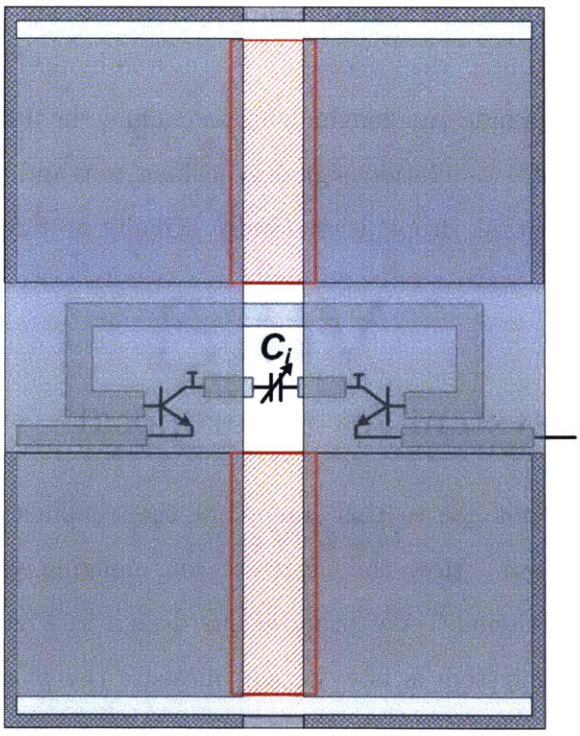


Figure 4-13: GND accidentally slotted pixel

Finally we power the whole chip up and measure the output of the charge pump as shown in Figure 4-12. The logic behind this is: If the system works, the sign of frequency difference between the down converted fundamental signal and reference signal will determine the level of charge pump output. We should see it goes to a high or a low level when we change the reference signal frequency. Note that the discussion is the open loop case where the output of the charge pump is not connected to the array's $V_{control}$ through the loop filter. However, during the measurement, we did not observe such phenomenon. And the charge pump kept at its highest output. It means the f_{ref} is always the one with higher frequency, which can only happen when the down converted and then divided signal is DC. The array is not oscillating.

The above 4 experiments drive us to form the conclusion that the oscillator of the prototype chip is not working properly, even though it is not what we want. After careful review of the design procedure we find that it is because a fault in layout rather than the design. Thus all of the design, analyses and simulations above still make sense. To be accurate, what happened in the layout is that the leaky wave antenna blocker in the pixel (see Figure 2-2), is accidentally lay out to be like Figure 4-13. The ground plate under the middle slot is removed by accident (the red shadow part). Thus this wave guide can longer help to confine the 140 GHz fundamental signal. The fundamental oscillation signal is leaking out and the Q factor of the fundamental oscillation tank drops dramatically. Finally no fundamental oscillation exists anymore.

4.4 Imaging system set up proposal

Even though we have not got to this stage, but this remains to be an important problem to discuss about. How the beam-steering imaging system should be set up as a whole in experiment? We propose our design in Figure 4-14. The most challenging part of the system is how we can measure the phase different between different pixels.

In this proposed system, all of the signal source, including the signal source in

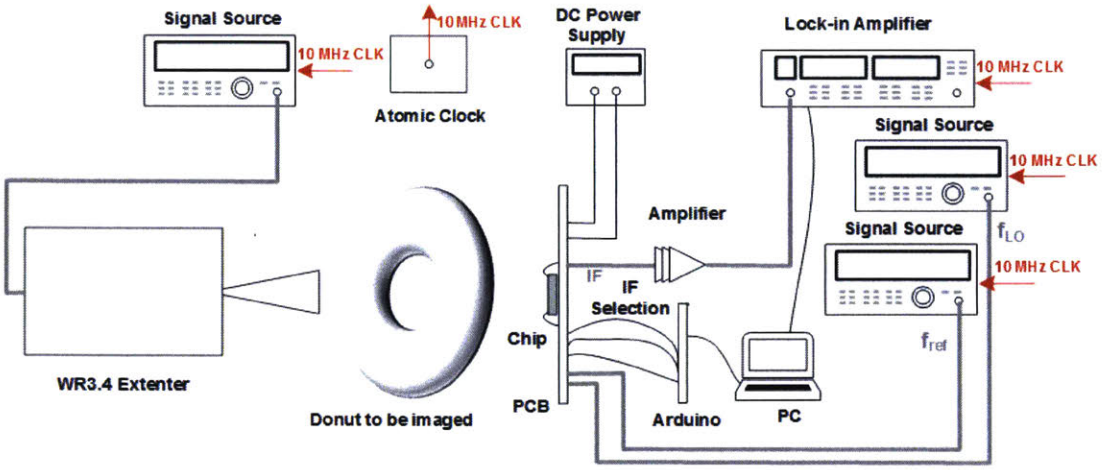


Figure 4-14: Proposed beam-steering imaging system set up

the lock-in amplifier, are phase locked to the same atomic clock signal in order to make them have the same stable time reference. When we want to measure the phase difference of different pixels, we have to find a reference signal to compare with. Any pixel's IF signal can not be used as a reference in this case, because on the one hand, great chances will be that the signal's power will be so low that it is below the noise floor, so it is extremely hard to produce a clean reference signal with enough power form the pixel's IF output; on the other hand, we only have one IF signal selected one time for the whole array, thus there is no extra IF signal can be used as reference for us.

Therefore we propose to produce this signal by using the lock in amplifier's internal source. We first calculate the IF frequency accurately from the already known frequency from the 3 signal source we are using, and then we set our lock-in amplifier's international source to be exactly working at that frequency. Because nowadays's signal source's frequency can be accurate to mHz level, this means that it will take nearly 1000 seconds before the error on this frequency will give us a 360 degree of phase error. Thus if we can finish the phase measurement of 1 pixel in 1 seconds, the error caused by this frequency misalignment can be neglected.

To further reduce the accumulated phase error with time, we proposed to me measure in a back and force sequence like this: pixel 1, pixel 2, pixel 1, pixel 3 ...

pixel 1, pixel n rather than measure pixel 1, 2, 3 ... n in series. We calculate the relative phase difference by substrate the phase of the signal of each pixel with the pixel 1 phase just measured before this measurement. In this way the longest phase error accumulation time will be just the time take to do one pixel measurement.

Chapter 5

Summary

In this thesis, a THz beam-steering imager using a scalable 2D coupled architecture and multi-functional heterodyne pixels is presented. The first version of the prototype, a 10 by 10 imager is fabricated based on the design described in this thesis. Even though the chip is not working because of some fault on layout, the whole chip design and experimental system set up techniques are well explored.

The predicted and simulated array performance are summarized in Table 5.1. It shows that the phase noise and directivity improves with array size enlarge while the sensitivity keeps constant.

A comparison of the prototype chip design/simulation results are summarized in Table 5.2. With our novel design method, we produced the state of art sensitivity, largest area size and highest pixel density at near 0.3 THz band.

If the chip worked properly, it would also be the first receiver/imager one in THz range that can do digital beam steering.

Table 5.1: Predicted and simulated array performance

Array Size	8 ×8	32 × 32	10 × 10
Area (mm × mm)	2 × 2	8 × 8	3.7 × 3.6
Estimated DC Power (W)	0.7	10.3	1.1
LO Array Phase Noise (dBc/Hz, Δf =1MHz)	-90	-101	-92
Directivity (dB)	19	31	21
Sensitivity (pW, BW = 1 kHz)	2.9	2.9	2.9

Table 5.2: Comparison with previous state-of-art imager array work

Ref.	Frequency	Technology	Array Size	Chip Area	Sensitivity
[9]	0.28 THz	130-nm CMOS	4 × 4	2.3 mm × 2.4 mm	917 pW
[3]	0.86 THz	65-nm CMOS	32 × 32	2.9 mm × 2.9 mm	3.16 nW
[15]	0.28 THz	130-SiGe	4 × 4	2.5 mm × 2.5 mm	250 pW
[12]	0.32 THz	130-SiGe	8 cell array	1.7 mm × 1.8 mm	70.1 pW
This Work	0.28 THz	130-SiGe	**10 × 10**	3.7 mm × 3.6 mm	**2.9 pW**

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