Integration of GaAsP Alloys on Si for High-Efficiency III-V/Si PV

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Chapter 1
Introduction and Background

1.1 Motivation

The motivation of this work is to create a platform that leverages the large area and low cost of Silicon wafers with the high performance of III-V materials. III-V semiconductor materials have enabled a host of electronic devices from record setting solar cells, high efficiency light emitting diodes, power amplifiers and high-mobility electron transistors. The last 60 years of research and development by the Si microelectronics industry has made the use of Si for microelectronics, power electronics and photovoltaics (PV) ubiquitous and low cost. The low cost of silicon technology is due to a mature and well developed supply chain infrastructure built from the microelectronics industry. While there has also been decades of research into III-V materials and electronic devices, widespread utilization has been limited due to the high cost of III-V substrates. Consequently III-V technologies have been limited to applications of high value added devices. Integration of high quality III-V materials on Si would open new dimensions of design space for electronic devices with high performance and at low cost. Potential applications could be the integration of light emitters, power amplifiers, RF radios and CMOS all on one large area low cost substrate. However, integration of these materials in non-trivial. Considerable challenges related to lattice mismatch, coefficient of thermal expansion mismatch, polarity mismatch and chemical incompatibility can degrade material quality and negate the potential benefits of III-V integration. This research specifically focuses on how to overcome these integration challenges to enable a high-efficiency, low-cost III-V/Si tandem solar cell. While the project motivation is solar, integration of III-V on Si in amenable for
many semiconductor applications and the processes developed here can be generalized for other device structures.

This research investigates the effect of growth processing parameters on the microstructure, electronic and optical properties of GaAs$_x$P$_{1-x}$ alloys grown on Si substrates. From the knowledge gained in those studies, we demonstrate world class GaAs$_x$P$_{1-x}$ single junction solar cells grown on Si substrates. This body of work serves as a demonstration of the potential of GaAs$_x$P$_{1-x}$ solar cells integrated with Si solar cells and provides a tool kit for further optimization of cell design, processing and implementation.

1.2 Organization of the thesis

In the first chapter we will motivate the integration of III-V materials on Si for solar as well as review the literature relevant to this thesis. Areas covered will be the various approaches to integrating III-V materials on Si substrates. This will include methods for accommodating the strain due to lattice mismatch and an overview of defects that form at the III-V/IV interface. Integration of III-V materials on Si is not a new challenge and there has been considerable progress made in the past 30 years that provides a foundation for interpreting the results presented in this work. The second chapter details the growth methods – metal-organic chemical vapor deposition (MOCVD) and ultra-high vacuum chemical vapor deposition (UHVCVD) and characterization techniques used for analyzing material microstructure and properties. The following chapters present original results from our investigations. Chapter 3 presents results of the growth, microstructure and processing parameters for GaAsP growth on SiGe graded buffers. This chapter focuses on the optimization of GaAsP/SiGe growth processing parameters to suppress defect nucleation at the III-V/IV interface. Dislocations and other defects are detrimental to potential solar cell performance. We identify the source of defect nucleation and discuss means to suppress those defects. Chapter 4 investigates other growth challenges faced at the III-V/IV interface. This
work focuses on the optimization of the GaAs/Ge interface and the effect of AsH$_3$ partial pressure on material quality. Having optimized the growth procedure for GaAsP alloys, we investigate their performance as solar cells in Chapter 5. Chapter 6 investigates the optical properties of GaAsP alloys and their relevance to solar applications. Chapter 7 summarizes important contributions of from this work and outlines future studies necessary for realizing a commercial implementation of GaAsP-Si tandem solar cells.

1.3 Photovoltaic solar cells

1.3.1 Introduction

Solar cells are electrical devices that convert the energy of photons into electrical energy through the photovoltaic effect. When photons with energy greater than the bandgap of a solar cell are absorbed, they excite an electron from the valence band into the conduction band. The built in electric field of a solar cell from the p-n junction then sweeps the excited electron out of the solar cell. A comprehensive review of solar cells is provided by Martin Greene. Additionally an interactive educational resource by Christina Honseberg and Stuart Bowden from the Solar Power Labs at Arizona State University at PVeducation.org is recommended for an overview of the operation, manufacturing and optimization of solar cells. A brief overview of the operating principle of a Si p-n junction solar cell is given below. Different architectures and materials for solar cells have been demonstrated, but the same basic physics govern the efficiency of a device. In general a solar cell requires the absorption of photons that generate electron-hole pairs. The generated carriers must be separated and extracted from the solar cell to an external circuit to provide useful work. The efficiency of a solar cell is the amount of usable electrical power produced by a solar cell divided by the incident solar power. Increasing solar cell efficiency requires tuning
Chapter 1 – Introduction and Background

Figure 1 a.) Price history of Si PV cells from 1977 - 2014. B.) Module price and installed price for <10kW PV installations over time. The BOS cost is nearly 4x the module cost in 2014.

The absorption and extraction properties of the solar cell design and materials to improve performance. Additionally improving material quality via the reduction of defects is paramount for solar cell efficiency, which will be the main focus of this work.

The adoption of solar cells for electrical energy generation has increased dramatically since their inception in the 1970s. During that time solar cells were prohibitively expensive for anything other than niche applications. The early solar materials were expensive as the Si microelectronics industry was still in its infancy. The high cost of materials and manufacturing coupled with low cell efficiency prevented solar from becoming a main stream power generation technology. Despite these humble beginnings, solar energy is rapidly gaining traction. Solar energy represents a large fraction (>50%) of the new installed electrical power generation capacity for the United States in 2015. The rapid increase in installed capacity has been driven by reducing costs of module production and installation. 40 years of research, development and cost reductions made rooftop solar a viable reality as the price dropped from $76/Watt to $0.36/W Figure 1a. Solar installation costs are typically given in $/W_{peak}$ capacity. This metric refers to
the cost to of the component (cell, module, balance-of-system, etc.) normalized by the peak power production of the module under AM1.5 standard testing conditions. Concurrent with dropping module prices has been an explosion in installed solar capacity—1000x increase in installed capacity in 20 years after 1995. While the solar cell absorber and processing costs dominated the economics of early generations, streamlined manufacturing and production capacity has made current Si PV modules account for less than 20% of the cost of a solar installation (<$0.80/watt and falling). The other costs associated with solar (inverter, labor, permitting, racking, etc...) dominate the current residential solar price ($>4/watt). Permitting, racking materials, labor and permitting currently cost 3x – 5x the cost of the solar module. This means that even if the panels were free, the cost to install a typical American home (5kW installed capacity), would still cost $20,000. Considerable effort has been made to streamline the installation process and bring down the balance-of-system cost, both by industry and through government sponsored research such as the DOE SunShot initiative. Standardizing mounting and racking systems in addition to consolidation within the solar installer market has drastically reduced the time necessary to install a typical residential site. A strong driver to reducing the BOS costs is increasing module efficiency. Beyond streamlining installations, the BOS costs are very sensitive to cell efficiency. Given an installed capacity, more efficient solar cells mean less glass, less metal, fewer workers climbing on roofs, and less transportation costs. The BOS scales with area, therefore a small increase in cell efficiency can mean a big reduction in installed cost due to less of all of the other system parts. Increasing the efficiency of Si solar is a major motivation of this work.

1.3.2 Solar cell efficiency and the case for multijunction cells on Si

The efficiency of a solar cell depends on the illumination spectrum, absorber material, material quality, and cell design. The energy distribution of photons emitted from the surface of the Sun can be
approximated by a blackbody source at about 6000K. The actual spectrum just outside Earth’s atmosphere (AM0) and at the surface (AM1.5) differs from the 6000 K blackbody spectrum due to scattering and absorption along the optical path. The AM (air mass) number is the path length which light takes through the atmosphere normalized by the shortest path length possible—ie when the sun is directly overhead (AM1). For standard testing conditions AM1.5G is used, the G refers to a global diffuse average irradiance.

Equation 1.1

\[ AM = \frac{1}{\cos(\theta)} \]

Under standard AM1.5 conditions the total solar power flux is 1000W/m\(^2\). The efficiency of a solar cells is defined as the fraction of the total incident solar energy that is converted into electrical power. Solar cell materials can absorb photons with energy greater than their bandgap. For the case of Si, this means photons with \( \lambda < 1117 \) nm can be absorbed and potentially converted to usable electrical energy. Absorbed photons excite electrons deep into the conduction band and holes into the valence band. The

![Figure 2 AM0 (space) and AM1.5 (surface) solar irradiance.](image)

Figure 2 AM0 (space) and AM1.5 (surface) solar irradiance. The energy distribution for a 6000 K blackbody is shown. Deviations between blackbody and measured spectrum result from atmospheric scattering and absorption. [77]
carriers quickly thermalize back to the band edge, losing all of the energy greater than the bandgap—this represents thermalization losses. Additionally photons with energy less than the bandgap of the solar cell are not absorbed—this represents transmission losses. The theoretical efficiency of a solar cell based solely on the incident solar spectrum and the bandgap was originally calculated by Shockley–Queisser [1]. The efficiency calculated by Shockley–Queisser (SQ) limit is based on a series of simplifying assumptions:

1. The solar cell consists of a p-n junction made from one material with a single bandgap ($E_g$)
2. All photons with $E > E_g$ are absorbed and produce one electronic charge $q$. Photons with $E < E_g$ are not absorbed.
3. The mobility is infinite, meaning that carriers generated anywhere within the solar cell are collected.
4. Non-radiative recombination due to Auger Recombination, traps and defects is not considered. Only radiative recombination is considered.

Figure 3 Shockley–Quiesser limit efficiency for a single junction solar cell as a function of bandgap given AM1.5 irradiance. b.) Breakdown of loss mechanisms that limit the efficiency of a single junction cell. Reproduced from Wikipedia.
The cell has a finite temperature >0K, therefore some fraction of the incident photons will be remitted via blackbody radiation—leading to cell loss. The SQ-limit defines an upper bound for the efficiency of a single junction solar cell based on its bandgap—real world implementations will be lower due to recombination. The theory of detail balance is invoked to account for the photo-generation rate and recombination rate (radiative and extracted carriers). The excess carriers excited in the solar cell create the voltage and current that contributes to the usable electrical power that can be extracted from the cell. From the SQ limit calculations we see that the maximum efficiency for a single junction solar cell is 33.7% ($E_g = 1.34$eV). The 1.1eV bandgap of Si is not optimal, but is still has a radiative limit efficiency of 29%. Modern high-efficiency Si cells have been able to reach nearly 85% of the SQ limit, a testament to cell and material quality optimization over the past 40 years. The progress of Si and other solar technologies is shown in Figure 4. The National Renewable Energy Laboratory's Best Research-Cell Efficiencies graph illustrates the evolution of solar cell technology over the decades, with modern cells reaching efficiencies close to the theoretical limits.
Laboratory curates a list of the record solar cell efficiencies for various materials and solar technologies since the 1970's. From the chart it can be seen that Si solar record efficiencies have largely stagnated since 1990's. The efficiency of production Si cells is approaching that of record lab cells (SunPower's all back contact production Si cell has efficiency of 24.2%). The highest efficiency solar cells on the chart are multijunction solar cells—these reduce both the thermalization losses and transmission losses by cascading a series of solar cells with differing bandgaps. The highest bandgap cell absorb the high energy photon enabling the extraction of electrons at a high voltage. The lower energy photons pass through the cell and are absorbed by lower bandgap subcells. While multijunction PV is capable of achieving >44% efficiencies, these cells are prohibitively expensive for applications other than space and military. They are typically grown on III-V substrates or Ge substrates which are very expensive (on order $10,000/m^2 compared to typically $300/m^2 module costs for roof top Si solar). Integration of III-V materials on Si could enable the high efficiency of multijunction solar cells at the price point of Si solar technology.

Figure 5 Efficiency of a 2-terminal dual junction solar cell based on a particular top and bottom cell bandgap combination assuming AM1.5G illumination and the radiative limit [78]. B.) 2-terminal Si-tandem cell efficiency as a function of top cell bandgap and top cell efficiency. The curves represent top cells of operating at various fractions of the SQ-limit efficiency for a given bandgap energy.
The highest efficiency solar cells demonstrated are multijunction solar cells as they can more effectively absorb the incident solar energy. The challenge with creating multijunction Si solar cells is multifaceted. The optimal material to integrate should have the right bandgap, must be high quality and should be scalable. Geisz and other have calculated what the efficiency of arbitrary solar cell combinations would be with different bandgap combinations Figure 5. The ideal combination for a 2-terminal Si based solar cell stack is 1.7eV top cell, which yields a 37% theoretical efficiency. This represents a 25% relative improvement in efficiency over a Si cell alone. Choosing the right bandgap governs the maximum theoretical efficiency, but the material quality governs the real world efficiency. There are many challenges to the integration of III-V materials on Si that can lead to the nucleation of defects that degrade cell performance. If the top cell is highly defective the reduction of thermalization losses due to a large bandgap top cell are negated if non-radiative recombination losses dominate in that cell preventing the high-energy electron-hole pairs from being extracted. Mass produced Si solar cells are currently capable of 22% conversion efficiency, therefore any III-V/Si tandem cell worth implementing must be capable considerably greater efficiency than Si alone or the integration is never worth doing. In the next section we will look at possible 1.7eV bandgap top cell materials and the integration challenges associated with them.

1.4 III-V Integration on Si

The material space for III-V semiconductor alloys is quite broad. There is a variety of direct and indirect bandgap and lattice constant combinations available Figure 6. Commercially available substrates for III-V epitaxy are typically elemental and binary compounds such as Ge, GaAs, GaP, InP or GaSb. While there are a variety of candidate materials for a 1.7eV top cell to integrate with silicon (GaAs$_x$P$_{1-x}$, In$_x$Ga$_{1-x}$P, Al$_x$Ga$_{1-x}$As), none of these are lattice matched to Si. Lattice mismatch represents one of the largest
challenges to heterointegration of III-V materials on Si. If not properly accounted for even a small amount of lattice mismatch (1%) can lead to catastrophic nucleation of dislocations which are detrimental to solar cell performance. In this study we focus on GaAs$_x$P$_{1-x}$ alloys since they have the least amount of lattice mismatch with respect to Si to accommodate (about 3% for a 1.7eV GaAs$_{0.75}$P$_{0.25}$ cell). In addition to lattice mismatch, the growth of polar materials such as III-Vs on non-polar materials such as Si presents its own set of challenges relating to chemical compatibility and a reduction in symmetry that can lead to antiphase domain formation. Both lattice mismatch and antiphase disorder must be accommodated or the resulting material quality will suffer. The following sections briefly review the physics behind these defects and strategies to mitigate their effect.

![Figure 6 Bandgap vs lattice constant for various III-V semiconductor alloys. Tie lines between binary compounds represent the ternary bandgap properties and lattice constant.](image-url)
1.4.1 Effect of lattice mismatch

The basics of lattice mismatch epitaxy and integration schemes will be reviewed in this section. High quality epitaxial films can only be obtained when the amount of lattice mismatch between the film and substrate is minimal. Difference in lattice constant leads to a buildup of strain energy in the film which eventually relaxes via the nucleation and glide of dislocations. Lattice mismatch is defined as:

**Equation 2**

\[ f = \frac{a_s - a_f}{a_f} \]

Where \(a_s\) is the lattice parameter of the substrate and \(a_f\) is the lattice parameter of the film. The strain due to lattice mismatch can be accommodated either by elastic or plastic deformation of the film.

**Equation 3**

\[ f = \epsilon - \delta \]
Figure 7 a.) Schematic representation of misfit strain being accommodated in two ways a.) The film is below the critical thickness and therefore is elastically strained. B.) beyond a critical film thickness, the strain energy in the film drive nucleation of dislocations that relieve the lattice mismatch strain. Reproduced from McGill [72].

Where $\epsilon$ is the elastic strain in the film and $\delta$ is the strain relaxed through plastic deformation of the crystal lattice via dislocation nucleation and glide. During the initial stages of mismatch epitaxy film growth (for $f < 2\%$), the film grows coherently with the underlying substrates—straining the bonds in the film such that the film has the same in-plane lattice constant. As the film thickness ($h_{\text{film}}$) increases, the total strain energy stored within the film ($E_{\text{elastic}}$) rapidly increases based on the amount of strain ($\epsilon$) and the modulus of the material ($Y$):

Equation 4

$$E_{\text{elastic}} = \epsilon^2 Y h_{\text{film}}$$

At a certain thickness the strain energy reaches a critical level such that it becomes energetically favorable disrupt the registry of some of the interface bonds between the film and substrate to relieve misfit strain. The registry disruption is known as a dislocation within the crystal lattice. The amount of misfit accommodated by a dislocations is proportional $b/S$ where $b$ is the Burgers vector of the dislocation and $d$ is the spacing between dislocations. While there is an energy penalty for broken and partially satisfied
bonds at the dislocation core, the strain relaxation in the film represents a net reduction of the system energy. An array of dislocations introduced into a solid to relieve misfit strain (ε) will have an energy per unit area of:

\[ E_{\text{dislocation}} = 2 \left( \frac{1}{5} \right) \frac{1}{2} Db \left( 1 - v \cos^2(\alpha) \right) \ln \left( \frac{R}{b} \right) + 1 \]

Where the 2 comes from the 2 sets of dislocations along each of the <110> directions, \( 1/5 \) is the number of dislocations per unity length along the interface, \( b \) is the magnitude of the Burgers vector, \( v \) is the Poisson ratio, \( R \) is the outer cut-off radius of the dislocation energy, \( \alpha \) is the angle between the burgers vector and the dislocation line, and \( D \) is the average shear modulus of the interface. The total energy of the system is given by the elastic strain energy and the dislocation strain energy. Taking the derivative of the sum of these components enables us to find the cross over between where dislocation relaxation becomes energetically favorable. The process of psuedomorphic growth and relaxation via dislocation

Figure 8 a.) Schematic illustration of a 60° dislocation showing the tilt, screw and edge components in the a/2<110>{111} slip system. (b) Glide of a pre-existing threading dislocation to create a misfit dislocation at the strained interface (b) nucleation of a half-loop followed by loop-expansion to create a misfit at the interface (c) typical misfit dislocation network with orthogonal <110> directions. Reproduced from Mukherjee [71].
nucleation is shown schematically in Figure 7. By performing an energy minimization analysis of a growing thin film, based on the misfit and the mechanical properties, the critical thickness at which plastic deformation and strain relaxation begins can be calculated. This formal analysis of the critical thickness was developed by Matthews and Blakeslee [2]. Fitzgerald continues to develop the theory of mismatch epitaxy and strain relaxation in an in-depth review article[3]. Comprehensive and in-depth studies related to the critical thickness along with dislocation nucleation and glide mechanics for mismatch epitaxy can be found in the following reference [4]–[7]. While the Matthews-Blakeslee critical thickness calculates the point at which dislocations become thermodynamically favorable, in practice films remain fully strained beyond the critical thickness due to kinetic barriers related to breaking bonds and moving defects. A brief review of pertinent details relating to dislocations in zinc-blende and diamond cubic systems are presented here in the context of relaxing strain for heterointegration of III-V materials on Si. The primary slip system for III-V and IV semiconductor materials involves an a/2<110> type Burgers vector and a {111} type glide plane. The glissile dislocations can either be 60° dislocations or screw dislocations, but only the component of the Burgers vector that lies in the plane of the mismatch relieves strain. An example of a 60° dislocation is shown in Figure 8. Strain relaxation can be achieved either through the glide of an existing dislocation or nucleation of a dislocation loop at the film surface. Either way, the length of the misfit segment (the portion of the dislocation that lies along the interface) governs the amount of strain relaxation that takes place. The process of glide, by which the dislocation moves through the crystal, is a thermally activated process where the glide velocity is determined by:

Equation 6

\[ v = v_0 \left( \frac{\tau}{\tau_0} \right)^m \exp \left( -\frac{E_a}{kT} \right) \]

Where \( v \) is the dislocation glide velocity, \( \tau \) is the resolved shear stress, \( T \) the temperature, and \( v_0, \tau_0 \) and \( m \) are fitting parameters, \( E_a \) is the glide activation energy and \( k \) is the Boltzmann constant. The glide
activation energy has been shown to be proportional to the bandgap of the material and the degree of
iconicity as both of these properties relate to the nature and strength of the chemical bonds within the
crystal that must be sheared during glide. Typical glide velocities observed in lattice mismatch epitaxy are
on order $1 - 10 \mu m/s$. In instances where a large amount of strain is introduced to the film rapidly (large
strain rate), the large over potential of strain energy within the film drive the nucleation of many
dislocation half-loops within the film since the dislocations cannot glide fast enough to relieve the strain
before additional nucleation events take place Figure 9. While relaxation still takes place in the high strain
rate scenario, a high density of threading segments remain. Direct integration of films with large degree
of mismatch has been attempted by many authors using a “two-step” growth process by which the film
is nucleated at low temperatures to prevent islanding. After coalescence, the subsequent film is grown at
a high temperature. While the two-step process can produce planar films, there is still a high density of
threading dislocation segments throughout the film. Additional film growth and thermal cycling can
reduce the TDD somewhat through dislocation-dislocation annihilation, but there are diminishing returns
as the density decreases as it becomes less and less likely a dislocation will “see” another dislocation.
Typical two-step germanium on Si is able to produce thin films with TDD in the high $10^6$ cm$^{-2}$ to low $10^7$
cm$^{-2}$ range. While this represents a vast improvement, the density is still too high for solar applications.

Figure 9 a.) Schematic illustration of high-strain rate, large mismatch epitaxy (Ge/Si 4% strain). b.)
cross section TEM of Ge thin film grown direction on Si vis two-step growth.
Figure 10 a.) Illustration of misfit relaxation in a step graded buffer via the nucleation of a half loop and subsequent glide of threading segments. b.) XTEM image of a SiGe step graded buffer from Si to Si$_{0.36}$Ge$_{0.70}$. Notice the absence of threading dislocation segments in the cap and regrowth segment.

If the strain is introduced slowly, existing threading dislocation segments can glide thereby relaxing the strain energy through the increase in the misfit line segment before ever reaching the critical nucleation strain energy. Composition graded buffers exploit the difference of activation energies between glide and nucleation so that existing threads can be "recycled" throughout the graded buffer by gliding at each mismatched interface Figure 10. In this way the strain can be relaxed before it ever reaches a level where nucleation events are favored. Successful demonstration of a composition graded buffer relies on the unimpeded glide of threading dislocation segments. If they are pinned by dislocation-dislocation interaction, surface roughness or particle/precipitate interaction, strain energy will build until the dislocation is either able to break free from that pinning site or a new segment is nucleated. The latter is not ideal, but does happen in buffers, which explains the general trend of slowly increasing TDD with continued grading.
Typical Si substrates have threading dislocation densities on order $10^3$ cm$^{-2}$. The direct growth of lattice mismatched $1.7$eV GaAs$_x$P$_{1-x}$ (~3% strain) would result in the nucleation of $>10^9$ cm$^{-2}$ threading dislocations, a level unsuitable for minority carrier device operation. The strategy employed in this thesis is to use Si$_y$Ge$_{1-y}$ composition graded buffers to relax the lattice mismatch between the GaAs$_x$P$_{1-x}$ solar cell and the Si substrate. Leitz et al studied the dislocation relaxation in graded buffers and have determined that the equilibrium threading dislocation density $\rho_t$ necessary to relieve strain without further nucleation to be [8]:

$$\rho_t = \frac{2R_g R_{gr} \exp\left(\frac{E_a}{kT}\right)}{b v_0 Y^m \epsilon_{eff}^m}$$

Where $R_g$ is the growth rate, $R_{gr}$ is the grading rate (in units or lattice mismatch per unit thickness), $E_a$ is the dislocation glide activation energy, $b$ is the magnitude of the Burgers vector, $Y$ is the Young's modulus of the film, $m$ and $v_0$ are fitting parameters and $\epsilon_{eff}$ is the residual strain in the top-most layer of the growing film. The equilibrium threading dislocation density is linearly dependent on the grading rate and exponentially dependent on the activation energy of glide. This makes intuitive sense in that during faster grade rates, the dislocation cannot relieve the strain fast enough to suppress nucleation of new dislocations. Additionally, a reduction in activation energy reduces the total barrier to glide making it that much easier for relaxation to occur. In the case of GaAsP integration on Si, there are a few graded buffer integration routes available (GaAsP/InGaP GB/GaP/Si, GaAsP/GaAsP GB/GaP/Si, and GaAsP/SiGe GB/Si). To first order the SiGe graded buffer represents the most promising system to span the lattice mismatch since the bandgap for SiGe alloys is lower therefore the activation energy for glide is lower. While Equation 1 above determines the equilibrium threading dislocation density and is independent of the total amount of strain relaxed, barriers to dislocation glide such as pinning due to dislocation-dislocation interaction and surface roughness can lead to TDD levels in excess of the equilibrium value Figure 11. During the growth of compositionally graded buffers, undulating surface morphology, known as cross-hatch,
Figure 11 Illustration of dislocation glide blocking mechanisms in compositionally graded buffers. Strain fields from orthogonal misfit dislocations and surface undulations can pin gliding dislocation segments. Reproduced from Pitera [10] based on work from Samavedam[79].

develops due to the strain fields associated with the orthogonal array of misfit dislocations. The strain field leads to local variations in growth rate ultimately causing the undulating crosshatch texture observed in lattice mismatch epitaxy. This crosshatch can pin dislocation glide and lead to the nucleation of additional threads. The surface roughness in compositional graded buffers can be removed by an intermediate chemical-mechanical polishing (CMP) step. This process unpins the threading dislocation segments allowing them to continue gliding and relieving strain. The development of SiGe graded buffers and intermediate CMP step can be found in the work of previous Fitzgerald Group members: Samavedam, Pitera, Currie, and Leitz [8]–[11]. Using the optimized Si$_y$Ge$_{1-y}$ graded buffer process developed in the Fitzgerald group, we are able to span the lattice mismatch between Si and Ge with $< 10^6$ cm$^{-2}$. The importance of a low TDD virtual substrate platform is discussed in the following section.
1.4.2 Effect of dislocations on solar cell performance

One major limitation of top cell efficiency is the density of non-radiative defects like dislocations. Dislocations are a 1-dimensional crystallographic defect that is a strong non-radiative recombination center. Dangling bonds and impurities within the dislocation core act as trap states that enable carriers to rapidly recombine. Defects within about a diffusion length of the dislocation will be recombined and cannot contribute to the extracted electrical power of the solar cell. While a devices grown on a lattice matched substrate have on order $10^4 \, \text{cm}^{-2} - 10^5 \, \text{cm}^{-2}$ threading dislocations, the TDD in devices grown on highly mismatched substrates is up to $10^8 \, \text{cm}^{-2}$ to $10^{10} \, \text{cm}^{-2}$. The high density of dislocations degraded device performance, as any carriers generated within the cell would rapidly recombine. Dislocations can be modeled as having an infinite surface recombination velocity within a cylindrical radius of the dislocation core. The expression for luminescence efficiency (and vis versa solar cell efficiency) is:

Equation 1.7

$$\eta = \frac{\eta_0}{1 + \pi^2 L^2 \rho_t}$$

Where $\eta_0$ is the dislocation-free maximum efficiency, $L$ is the minority carrier diffusion length, and $\rho_t$ is the threading dislocation density. The minority carrier diffusion length is the only material dependent property in the Equation 1. and depends considerably on the material quality, processing, doping and specific material attributes.

Equation 1.8

$$L = \sqrt{D \tau} = \sqrt{\frac{\mu k T \tau}{q}}$$
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Figure 12 Plot of relative LED efficiency as a function of dislocation density and diffusion length based on the Rodel model.

Where $D$ is the minority carrier diffusivity, $\tau$ is the minority carrier lifetime, $\mu$ is the mobility, $k$ is the Boltzmann constant, $T$ is the temperature of the semiconductor, and $q$ is the charge of an electron. Typical diffusion lengths in solar cell materials range from tens of nanometers to microns. The diffusion length is a function of both the mobility of the carrier and the lifetime. A high diffusion length is desirable for solar cell operation since it enables thicker cells to be designed that can better absorb light while still achieving good carrier collection. The requisite for carrier collection is that they can diffuse to the junction before recombining. A high density of dislocations within the solar cells represents a high probability that carriers will recombine before they make it to the junction.

Early attempts at III-V integration on Si sought to deposit the III-V materials directly on Si —such as GaAs directly on Si. Yamaguchi studied the effect of dislocations in GaAs solar cells grown directly on Si extensively. The high degree of lattice mismatch lead to high dislocation densities, despite thermal cycling and many other processing steps. The question posed by this foundational research was at what level dislocations would no longer be detrimental to solar cell performance. For GaAs, the efficiency of a solar cell no longer becomes limited by the density of dislocations for densities $< 10^6 \text{cm}^{-2}$, which corresponds to an average spacing of $10 \mu\text{m}$ between threading dislocations. The reason for the cell efficiency TDD threshold comes from the spacing of the dislocations becoming larger than the minority carrier diffusion
Figure 13 Effect of threading dislocation density on solar cell performance. At low TDD (<10⁶ cm⁻²) the effect of dislocations on solar cell performance becomes negligible. Adapted from Yamaguchi et al. [23]

length. This means that most of the carriers generated within the solar cell cannot diffuse far enough to ever see a dislocation and therefore will not recombine there. This is not to say the solar cell is optimal or perfect once the dislocation density falls below this critical value. There are still other recombination pathways, radiative and non-radiative, that can limit solar cell performance. Once the material quality is optimized, cell architecture and other second order optimizations can be applied to further improve the cell quality. Demonstrating a high baseline material quality is necessary and a primary focus of this work.

1.4.3 Effect of polar/non-polar interface

The challenges associated with the III-V/IV interface have been investigated by many authors at the composition end points of GaAs/Ge [12]–[15] and GaP/Si [16]–[20], where lattice mismatch is minimal. From a mechanical strain perspective, the GaAs/Ge interface is an ideal candidate for the study of polar on non-polar substrates since the degree of lattice mismatch (0.08%) and a coefficient of thermal (CTE)
expansion mismatch (2.8%) are very low. For comparison, GaP/Si has a lattice mismatch and CTE mismatch of -0.3% and 78.8% respectively. Growth of polar III-V semiconductor materials on a non-polar IV semiconductor materials presents unique heteroepitaxy challenges. The zinc-blende structure of III-V materials has a reduction in symmetry with respect to the diamond cubic lattice structure of Si and Ge. There are two distinct orientations of the zinc-blende cubic structure that correspond to a 90° rotation of the lattice Figure 14a. During the growth of III-V materials on a group IV substrate, such as GaAs on Ge, there is a site ambiguity for the incoming Ga and As atoms that leads to multiple domains of GaAs being nucleated on the Ge surface. Antiphase disorder results when separate domains of each orientation are nucleated and impinge on one another, forming electrically-active planar defects known as antiphase boundaries (APBs) between them. APBs consist of either a boundary of As-As bonds or a boundary of Ga-Ga bonds that propagate from the interface through the material Figure 14b. Both boundary types represent high energy perturbations to the GaAs crystal lattice which effect both the growth and electrical properties of the material. Surface roughening results due to variation in growth rates caused by the strain fields and high energy of APBs. Surface roughening is detrimental for majority carrier devices such as high electron mobility transistors (HEMTs) as it increases carrier scattering in high mobility channels. For minority carrier devices APBs act as shunt paths and strong non-radiative recombination centers which reduce minority carrier lifetime and degrade device performance. Regardless of the intended application, APBs present a III-V integration challenge that must be solved for successful implementation of III-V devices on Si.

The reconstruction of the group IV surface is an important parameter in determining if APBs will form or not. With a single domain surface (As or Ga first) the III-V film will not undergo dimer rotation and there will not be the formation of antiphase domains. A single domain surface can be achieved through a
double-step surface reconstruction Figure 15. In practice the double step surface can be controlled through the use of deliberately offcut wafers and appropriate annealing conditions. When a (001) Si wafer or (001) Ge wafer is offcut a few degrees toward one of the [110] direction, the irregular array of surface
steps is converted to a regularly spaced series of atomic steps in the offcut direction. The spacing of these steps \((w)\) is determined by the offcut angle \((\theta)\) and the step height \((d)\):

Equation 1.9

\[
w = d \tan(\theta)
\]

Using the right offcut angle and annealing condition will cause the surface to reconstruct into a series of double steps. The driving force for this reconstruction is a reduction in the surface free energy of the crystal. Typically a high temperature anneal is required to provide the thermal activation energy for surface reconstruction (650°C – 850°C for Ge and Si respectively). A double step surface in addition to either a group-V or group-III first initiation provides APB free growth of III-V materials on group IV substrates. All of the experiments presented in this thesis are performed on wafers 6° offcut towards the [111] direction. In Chapter 4 we investigate more closely the growth and specifically the initiation conditions necessary to suppress APB formation during the growth of GaAs on Ge.

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Figure 15 Example of a double-steped single domain group IV surface. The double-step structure is important for suppressing the formation of APBs. Reproduced from Groenert [56]
Chapter 2
Materials Growth and Characterization

The research presented in this thesis interrogates the microstructure and material properties of semiconductors as a function of the process conditions used. Understanding of the fundamental material processes is gained through iterations of growth/processing and materials characterization. From the basic studies conducted we can elucidate the source of defects generated during the material growth and ultimately determine a process window where high quality, low defect material can be grown reproducibly. In addition to growth and materials characterization, electrical and optical characterization is performed to connect the processing and microstructural properties to the device performance. This work involves the use of multiple semiconductor growth processes, materials characterization techniques and device fabrication & testing. This chapter gives an overview of these methods, the underlying physics that govern each process and the sort of information or structure that is gained from each.

2.1 Materials Growth

2.1.1 Ultra-high vacuum chemical vapor deposition (UHVCVD)

The growth of Si$_x$Ge$_{1-x}$ graded buffers in this work was performed with ultra-high vacuum chemical vapor deposition (UHVCVD). The background pressure in a UHVCVD chamber is on order $<10^{-9}$ torr, which
provides a very clean ambient to perform epitaxial growth of materials which in turn leads to ultra-pure, high quality materials. The rate at which contaminants adsorb on a surface and ultimately get incorporated into the bulk epitaxial film is proportional to the contaminants partial pressure in the CVD chamber. For a silicon surface at room temperature, near unity surface coverage is achieved after 1 Langmuir of exposure \((1L = 10^{-6} \text{ torr-s})\). The partial pressure of \(O_2\) and \(H_2O\) in the UHVCVD is \(<10^{-10} \text{ torr}\), which means it takes on order \(10^4\) seconds for the surface to saturate with a contaminant. The slow adsorption rate means that during epitaxy the background concentration of contaminant species will be \(<10^{15} \text{ cm}^3\). Besides being detrimental to electronic properties of Si, Ge, and \(Si_yGe_{1-y}\) alloys, C and O contamination can act as potential pinning sites for dislocation glide—which could increase the ultimate TDD of a graded buffer.

The UHVCVD used in this work is a custom built vertical hot-walled reactor. The reactor has a load lock to minimize contamination of the reactor chamber during loading/unloading of wafers. The UHVCVD reactor consists of a heated quartz tube that is evacuated with a turbo-molecular pump. A schematic of the UHVCVD reactor used for the \(Si_yGe_{1-y}\) buffer growth in this research is given in Figure 16. The quartz tube is heated by a three-zone electric resistance heater and is capable of temperature up to 900°C. The turbo-pumps are backed by a large roots-blower mechanical roughing pump capable of pumping to base pressures of \(10^{-5} \text{ torr}\) through a common foreline. The reaction chamber is bakes out to base pressures of \(10^{-9} \text{ torr}\). The bake-out process takes about a week after exposure to atmospheric contamination. After the bake-out process, any residual surface contaminants are buried by coating the quartz tube in Si by flowing \(SiH_4\) into the chamber while it is heated to 900°C. The chamber background pressure improves following the coat since background pressure is proportional to the vapor pressure of surface contaminants, which are now buried. The process gasses are injected directly into the top of the quartz tube from a computer controlled gas manifold. The rate at which the process gasses are injected to the process chamber is controlled by a series of mass-flow controllers (MFCs) and pneumatic valves in the gas
During a growth the CVD chamber pressure is between 5 – 30mtorr depending on the amount of gas injected and position of the throttle valve over the process turbo pump.

The precursors used for the growth of Si and Ge are SiH₄ and GeH₄ source gases respectively. The ratio of SiH₄ and GeH₄ injected into the reactor governs the fraction of Si and Ge incorporated into the deposited film. The dopants precursors used for the SiₓGe₁₋ₓ films are 1% B₂H₆ in H₂ and 1% PH₃ in H₂ gases for p-type and n-type doping respectively. The dopant sources can be further diluted with Ar prior to injection to the UHVCVD reactor through by two stages of dilution. The double dilution lines enable a wide dynamic range for doping: from 10¹⁵ – 10¹⁹ cm⁻³. A quartz boat is loaded with 10 wafers at a time for deposition within the UHVCVD. The low growth pressure enables batch processing of multiple wafers simultaneously. As the pressure of a gas is reduced, the probability of collisions between gas molecules is

Figure 16: Schematic of the UHVCVD system. Reproduced from Leitz [8]
reduced and therefore the mean-free path increases. When the mean-free path becomes on order the size or larger than the size of the reaction chamber, the reactants flow by in a ballistic free molecular flow fashion and are able to get between the multiple wafers that are stacked in the quartz boat. The large mean-free path plus hot wall reactor design enable many Si$_x$Ge$_{1-y}$ graded buffers to be grown at one time. While typical growth rates in the UHVCVD reactor are about 40x less than the growth rates in reduced pressure CVD, the effective growth rate from batch processing makes this process highly scalable.

The growth temperature can be varied from 400°C to 900°C depending on the composition and type of growth. The gate valve over the reactor turbo pump can be partially closed to throttle the pump and control the growth pressure within the reactor chamber. Since the UHVCVD is a hot-walled reactor, growth occurs on both sides of the wafer. The use of double side polished substrates provides epitaxial growth on both sides of the wafer. A benefit of deposition Si$_x$Ge$_{1-y}$ buffer on both sides of the wafers is a reduction is wafer curvature since the thermal strain due to coefficient of thermal expansion (CTE) mismatch between the film and substrate is balanced. Typical waferbow of Si$_{0.50}$Ge$_{0.50}$ graded buffers grown on 150mm Si wafers in the UHVCVD reactor is about 10μm. The wafer bow for similar epitaxial structures grown by reduced pressure CVD on only one side of the 150mm Si wafer results in about 100μm of wafer bow, which makes processing and future growth difficult.

The ultimate threading dislocation density of compositionally graded buffers depends on the unimpeded glide of dislocations to relax the lattice mismatch induced strain. Dislocation glide is a thermally activated process and favors high temperature for glide velocities necessary for low TDD graded buffers. The graded buffer growth temperature is limited by energy barrier for nucleating dislocations which is also thermally activated. At too high of a temperature both dislocation nucleation and dislocation glide become energetically favorable. Additionally, the low cracking temperature of GeH$_4$ leads to gas phase nucleation of Ge particles during growth of Ge rich films at too high of a temperature. Both dislocation nucleation and gas phase nucleation are undesirable and lead to degraded film quality.
activation energy for dislocation glide in Si$_x$Ge$_{1-y}$ alloys decreases with increasing Ge content in the film, which would be expected given the reduction in bandgap and melting temperature as well. The optimal temperature for Si$_x$Ge$_{1-y}$ graded buffer growth can be reduced at high Ge content films while maintaining reasonable glide velocities without gas-phase nucleation. The growth temperature of the graded buffer was maintained between 0.7T$_m$ and 0.8T$_m$ as shown in Figure 17, where T$_m$ is the absolute melting temperature of the growing Si$_{1-x}$Ge$_x$ film. Typical graded buffer growth temperatures are 900°C for Si – Si$_{0.50}$Ge$_{0.50}$, 750°C for Si$_{0.50}$Ge$_{0.50}$ – Si$_{0.25}$Ge$_{0.75}$, and 650°C for Si$_{0.25}$Ge$_{0.75}$ – Ge.

Prior to growth, Si wafers are typically subjected to a two-step wet chemical clean consisting of a 10 minute piranha clean (3:1 H$_2$SO$_4$:H$_2$O$_2$) followed by a 1 minute HF dip (10:1 H$_2$O:HF), which yields a clean hydrogen-terminated surface. The piranha clean attacks any organic contaminants that might be on the Si wafer surface and leaves a SiO$_2$ oxide layer. The HF dip removes the oxide layer leaving the Si wafer surface hydrogen passivated. The oxide layer left by the piranha clean leaves the Si wafer hydrophilic while the H-passivated Si surface is very hydrophobic. The hydrogen terminated surface prevents surface
oxidation while transferring the Si wafer into the deposition chamber. The clean, oxide free surface is ideal for epitaxy and will last for about 30 minutes in atmosphere. The boat of wafers is immediately loaded into the UHVCVD load lock and pumped down to <10^{-8} \text{ torr} prior to transferring to the UHVCVD growth chamber. The wafers typically sit in the load lock for 2 – 12 hours prior to growth. Once transferred to the UHVCVD growth chamber, the wafers are held at roughly 200°C for 30 minutes to desorb any contaminants that might be on the surface. The wafers are then raised into the hot region of the furnace and subjected to a high temperature desorption step for 10 minutes (typically at 900°C). The high temperature step drives off any other contaminants and desorbs any potential oxide that may have formed while in the load lock. Finally, a 1 \mu m homoeptaxial buffer layer is then deposited to bury any residual impurities, yielding a pristine growth surface. The SiGe compositional graded buffer is then deposited following the homoeptaxial buffer growth.

2.1.2 Metal-organic chemical vapor deposition (MOCVD)

The growth of III-V semiconductor materials in this work is performed using metal-organic chemical vapor deposition (MOCVD). The growth process of MOCVD involves the controlled pyrolysis of metal-organic reactants and hydride reactants on the wafer surface to provide the desired group III atoms (Ga, In, and Al) and group V atoms (As and P) respectively. The byproducts of the decomposition from precursor species react to form other volatile adducts (H_2, CH_4, etc.) which desorb from the wafer surface and are swept away by the carrier gas flowing through the reaction chamber. A comprehensive overview of the art and science of MOCVD growth is given by Stringfellow.

Important processing parameters that govern MOCVD growth are temperature, gas flow rates and ratios, V/III ratio, reactant partial pressure, and carrier gas. Temperature represents one of the strongest process parameters affecting MOCVD since gas-phase diffusion, precursor cracking, surface diffusion, and
desorption are all thermally activated processes. Additionally the surface vapor pressure, surface reconstruction and energy barrier for defect nucleation & dislocation glide are all strongly affected by temperature. The CVD and MOCVD growths performed in this work are done in the mass-transport limited regime, resulting in a $T^{3/2}$ dependence of growth rate on temperature. Typically the effect of temperature on growth rate is minor, while the flow of group III species ultimately determines the rate of film growth.

The ratio of group V to group III in the reactor chamber is another important growth parameter. At elevated temperatures the vapor pressure of the group-V species is quite high and can lead to desorption which can leave behind metallic droplets of group-III elements. An overpressure of group-V precursors suppress this desorption and is why group-V flow is maintained when heating up and cooling down III-V materials. Typical V/III ratios used for the growth of III-V materials range from 20 – 200. Industry growth favors lower V/III ratio as it limits the amount of expensive group-V precursor that goes to the exhaust, but a minimum V/III ratio of 10-20 is maintained to ensure good material quality.
The close-coupled showerhead prevents gas phase reactions since the injected group-III and group-V species do not interact until they reach the wafer surface. The showerhead consists of a series of holes connected to two separate gas plenums designed to segregate the group-III and group-V precursors until they are injected to the chamber. The wafers sit in a SiC coated graphite susceptor that is heated by a 3-zone graphite electrical resistance heater. The size of the heater and susceptor determine the wafer sizes that can be grown in a given system. The MOCVD reactor in the SEL is capable of growing on 2", 4", 6", and 8" wafers. This reactor has the unique capability of depositing both group III-V and group IV species, thus allowing the in situ growth of GaAsP/SiGe heterostructures. The system also features in-situ reflectivity and temperature monitoring through a Laytec® EpiTT reflectivity measurement system. The growth pressure is controlled via an Ebara dry mechanical roughing pump and an MKS butterfly style throttle valve. The entire reactor body is enclosed in an N₂-purged glovebox which prevents contamination from oxygen and water, which are detrimental to semiconductor growth, during loading and unloading of wafers into the MOCVD.

Figure 18 a.) Schematic illustration of a showerhead MOCVD reactor. The process gasses are injected from the top of the chamber onto a heated, rotating wafer susceptor. The reaction products and unused precursors are exhausted by a dry mechanical pump. Reproduced from Sharma [30] b.) Photograph of the MOCVD reactor in the Substrate Engineering Lab at MIT used for these studies.
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The susceptor temperature was measured using broadband optical pyrometry with measurement accuracy to within 1°C. Temperature uniformity is an important process parameter for ternary alloy growths as the incorporation rate of precursors into the thin film vary with temperature. Maintaining uniform and accurate growth temperature is critical in achieving high film quality of GaAsP on SiGe. The temperature settings are calibrated under well-controlled conditions: freshly cleaned and Si coated quartzware with an uncoated 4” susceptor. The optical pyrometers are calibrated with a black-body temperature standard. The heater setpoint and power settings for each heater zone are altered until the desired temperature and uniformity (<1°C variation across the susceptor) are achieved. These temperature and power settings are used for all subsequent growths to achieve the desired temperature conditions up to 850°C. Different temperature balances needed for N2 carrier gas and H2 carrier gas due to the different thermal conductivity.

2.2 Materials Characterization

2.2.1 Transmission electron microscopy (TEM)

Transmission electron microscopy is used extensively in this work to characterize interface quality and quantify defect density within semiconductor thin films. A TEM consists of a high-energy (~200keV) electron source and a series of electronic lenses that use either magnetic or electric fields to shape and steer the electrons into a parallel beam of electrons. The incident beam interacts with the atoms in the sample as it passes through. The result of this interaction generates the contrast detected by the CCD below the sample. The mechanisms for this contrast can be due to absorption, inelastic scattering (mass-thickness) and elastic scattering (diffraction). Variations in the periodicity of the crystal lattice lead to
variations in the diffracted electron beam intensity. These intensity variations lead to special contrast within the TEM image, which is particularly useful for imaging strain fields and other things that distort the crystal lattice—like dislocations. Diffraction contrast is used extensively in this thesis to image dislocations and other defects (APBs, stacking faults, twins) within epitaxial growth structures. Additionally high-resolution (HRTEM) images can be formed by imaging the interference patterns that develop as the parallel beam of electrons interacts with the periodic potential of the crystal lattice. From these HRTEM images individual columns of atoms and atomic planes can be resolved. A comprehensive review of TEM theory, operation and analysis can be found in Transmission Electron Microscopy by Williams and Carter.

TEM requires some sample preparation to make the sample “electron transparent”. The TEM foil is prepared through a series of polishing steps followed by ion milling at a shallow angle. For cross section

![Diagram of TEM and STEM imaging](image)

Figure 19 A-D Schematic showing bright-field and dark-field imaging in a TEM and scanning-TEM (STEM). (E) The sample can be tilted such that the incident beam strongly diffracts off of a particular set of hkl planes. This is used for diffraction contrast imaging. Reproduced from Williams & Carter.
TEM, two wafer pieces are glued together to make a cross sections sandwich. The sandwich is then mounted on a pyrex stub with wax for grinding. Planview sample preparation does not require a sandwich, rather, the sample is affixed to the stub film side down. CrystalBond wax is used for temporary mounting since it can be softened with temperature or dissolved in acetone. The pyrex stub is loaded into a Gatan 550 disc grinder which has a micrometer to advance the sample during grinding. Wet grinding and polishing is performed on a series of progressively finer grits using rotary polishing wheels (500, 800, 1200, 2200, 4000, 3µm diamond paste). Grinding progresses until the sample is < 10µm in thickness (this can be approximated based on the color of transmitted light through the Si wafer clads). With patience and practice, one can polish up to 4 TEM samples at one time in the course of about 90 minutes—two samples per stub, one grinder per hand. Following grinding, the sample is mounted to a copper grid for support and released from the stub using acetone. Care should be taken to rinse off all of the wax residue from the sample with acetone and IPA prior to ion milling as it can lead to TEM artifacts. The samples are ion milled with Ar+ ions accelerated at 5kV – 4kV, at a beam current of about 4mA – 5mA using a Fischione Ion Mill. The milling angle starts at 15° to give good material removal rate and gradually reduced to about 12° for final polishing steps. The ion milling step burns a small wedge shaped hole in the TEM foil. At the end of the film the sample is electron transparent <500nm. Typically TEM sample thicknesses for imaging are on order 50nm – 200nm for most samples. Higher electron energy can enable thicker samples to be imaged. The samples are then imaged using a JEOL 2011 TEM operated at 200keV using a lanthanum hexaboride (LaB₆) filament electron source. A double-tilt sample holder was utilized to access multiple tilt orientations for diffraction analysis.

Typical imaging conditions used consist of on-pole mass-thickness imaging conditions, HRTEM imaging condition and two-beam diffraction contrast imaging condition. The on-pole imaging condition provides mainly information about the atomic weight of the species being imaged (high atomic weight atoms lead to more scattering of the electron beam and therefore lower intensity and a darker contrast in
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the image. The two-beam diffraction imaging condition is set up by tilting the sample in such a way that the beam strongly diffracts off a particular set of lattice planes. Perturbations to those planes or bending of planes into the diffraction condition cause the electron beam to be scattered strongly. With an appropriate aperture, the diffracted electrons can be excluded from the camera which results in a dark spot in the spatial region of the perturbation. The $g = 220$ two-beam diffraction condition is typically used for imaging crystallographic defects—especially dislocations due to them having a Burgers vector of the $<220>$ type. The images contrast is proportional to the dot product between the perturbation (Burgers vector in this case) and the diffraction vector $g$. Another useful diffraction condition employed in this thesis is the $g = 004$ diffraction condition, which is sensitive to perturbations in the out of plane lattice constant. The 004 diffraction condition can be used to image strain fields within semiconductor films.

TEM imaging can be used to quantify the defect density within the sample. For high densities of defects $>10^7 \text{ cm}^{-2}$, TEM is particularly useful as it can resolve individual dislocations at these high densities. Other defect quantification methods (etch pit density, electron beam induced current and cathodoluminescence) have spot sizes too wide to resolve that high of a defect density. One unfortunate limitation of TEM is the very finite area of material that can be sampled in a TEM foil. The low area makes it difficult to quantify dislocation densities $<10^6 \text{ cm}^{-2}$ in planview. Other complimentary techniques like EPD, EBIC and CL are used for low defect density analysis. In cross section TEM images, the absence of observed defects does not indicate the absence of defects in the film. Typical imagable areas are on order 10$\mu$m – 50$\mu$m of interface. Since the sample is on order 100nm thick, this represent a total area of about $10^8 \text{ cm}^{-2}$ per XTEM foil. PVTEM must be done to give any quantification of defect density.

2.2.2 Differential Interference Contrast (Nomarski) Microscopy

Optical microscopy can provide valuable information about surface morphology in semiconductor
processing. Conventional optical microscopy relies on variations in surface reflectivity and morphology to create contrast. Epitaxial films are typically grown on polished wafers—therefor there are only very minor variations in surface reflectivity across the wafer. This makes it difficult to image semiconductor films using standard optical microscopy techniques due to the poor contrast. Differential interference contrast microscopy (DICM or Nomarski) utilizes a beam-shearing prism to produce an illumination source with two optical paths that are slightly out of phase from one another. Small variations in surface step height or refractive index produce contrast by changing the phase of the light slightly—the interference leads to observable contrast. Using nomarski, the image contrast is greatly improved and step heights on order tens of nanometers can be resolved when the change in height is quite sharp. This is especially useful for imaging morphological defects that are grown into the epitaxial film—pits due to APB formation, particles, cross hatch, ect... Additionally the nomarski contrast is used to image the etch pits caused by selective chemical etching that decorate the surface and reveal the locations and density of dislocations within the film.

2.2.3 Etch-Pit Density (EPD)

Properly quantifying the defect density within semiconductor thin films is a straight forward concept—count the number of defects and divide by the imaged area. While straight forward, there are many examples of misunderstanding of how to quantify defect density properly and the limitations of techniques used to quantify defect density. For moderate defect densities, PVTEM is the most dependable since it directly images dislocations and other crystallographic defects. Etch Pit Density (EPD) and other techniques require some process to be accelerated or retarded in the area near a defect, and that process can then be imaged and quantified. In the case of EPD, the sample is submerged in some etchant that preferentially attacks threading dislocations through a combination of oxidant and acid/base. Defects
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represent high energy sites due to strain and disruption to the crystal lattice and can be attacked more easily. If the etch rate between the bulk film and the dislocation differs enough, pits or mounds will form below/above the dislocation. These pits can easily be resolved in the nomarski microscope. The benefit of EPD is that it is quite fast and easy to perform and enables very large areas to be sampled. PVTEM is not a good option for measuring $TDD < 1 \times 10^6 \text{ cm}^{-2}$ due to the limited observable sample area. EPD can easily measure defect densities in the $10^3 - 10^5 \text{ cm}^{-2}$ range. One major limitation to EPD and other techniques is that at high densities, the distance between defects becomes on order or less than the feature size of these secondary quantification techniques. In the case of EPD, the etch pits start to merge together and we can no longer distinguish different defects. The result of this is that one could observe a low density of pits ($<10^6 \text{ cm}^{-2}$) when in actuality there are $>10^8 \text{ cm}^{-2}$ in the sample. One should always do PVTEM to spot check some of the EPD results. Additionally the etch process can depend highly on the thickness, doping, composition and illumination of the thin film layer being investigated, leading to high variability in EPD processes.

![Figure 20 Typical Nomarski image of a Si_{0.50}Ge_{0.50} graded buffer after EPD etch. Crosshatch texture in addition to pits are observed.](image)

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The defect density in the SiGe graded buffer samples is quantified using EPD. The process has been validated by PVTEM within the Fitzgerald group numerous times over the last 10 years of SiGe growth optimization. The Schimmel etch has been used extensively in literature and within the group for characterizing EPD of Si and SiGe films with Ge content up to 70%. A solution of hydrofluoric acid, chromium trioxide and water is prepared (8g CrO$_3$, 200mL HF, 250mL H$_2$O) and the samples are etch for 2 – 3 minutes. The etch rate slows with increasing Ge content, so longer etch times are necessary for high Ge content films. The etchant produces small pits that can be easily observed on nomarski Figure 20. Characterizing SiGe films with EPD works quite well, but attempts to develop an EPD chemistry for GaAsP films did not work well. Etch chemistries based on chromium trioxide + HF as well as molten potassium hydroxide were both investigated to great length, but the results were not reliable nor reproducible.

2.2.4 Electron Beam Induced Current (EBIC)

EBIC measurements use the electron beam of a scanning electron microscope (SEM) to excite carriers within a p-n junction or Shottky junction device. As the electron beam rasters across the sample, a current meter connected to the diode measures the output current of the diode Figure 21. The current can be plotted as an x-y map with a 1-to-1 correlation to the secondary electron image generated used in conventional SEM imaging. The contrast in the current image arises from the collection probability of

![Figure 21 Schematic illustration of charge collection geometries for EBIC. (a) and (b) illustrate the cross section and planar p-n junction geometry in which the space-charge region is represented by the cross hatched region. Reproduced from Leamy [80]](image)
carriers generated at various locations across the sample as the electron beam rasters. Carriers generated near an electrically active defect such as a dislocation, APB, or stacking fault quickly recombine—lowering the current collected from that location. This appears as a dark spot on the EBIC current image Figure 22. Using the EBIC image the electrically active defect density within solar cells and diode structures can be rapidly quantified—even at low densities due to the large area sampled. A typical EBIC image samples 100x the area of a typical PVTEM image. One limitation, similar to EPD, is that at high defect densities the dark spots blur together making it difficult to quantify the density. For GaAsP cells, EBIC is suitable for defect levels $<10^7$ cm$^{-2}$.

Figure 22 Representative SEM (left) and EBIC (right) image of a GaAsP solar cell imaged in the plan-view orientation. The white line in the SE image and corresponding black line in the EBIC image is the top contact bus bar of the solar cell. The black dots in the EBIC image correspond to threading dislocations within the cell structure.

2.2.4 Atomic force microscopy (AFM)

Atomic force microscopy (AFM) is used for characterizing the surface morphology of deposited films. This is done by rastering a Si cantilever mounted on a piezoelectric driver across the film surface.
Chapter 2 – Materials Growth and Characterization

The tip of the cantilever is sharpened to a fine point to probe microscopic features of the sample surface. Depending on the operating mode used, contact mode or tapping mode, deflection of the cantilever due to interaction with the surface is measured by monitoring the position of a laser beam that is reflected off the end of the cantilever. Small deflections of the cantilever can be measured with great accuracy in this manner. The deflection of the cantilever is fed into the piezoelectric driver to maintain a constant force through an applied voltage. This applied voltage can be used to generate a x-y surface map of the surface height. Samples quickly adsorb a layer of water on the surface when exposed to ambient conditions. This layer can lead to the tip sticking—which is a major limitation of contact mode AFM. Tapping mode AFM alleviates this trouble by oscillating the AFM tip near the resonant frequency of the AFM tip. Van der Waals forces and other surface interactions represent a damping force on the oscillating cantilever. The piezoelectric drive voltage needed to maintain the drive frequency with the changing damping function can be used to generate an image of the surface height. Additionally since the sample is tapping, it does not get stuck to the surface. All of the AFM measurements performed in this thesis are done in tapping mode. From AFM scans the root-mean-squared (RMS) surface roughness as well as step height, and min-to-max height amplitude can be determined. The strain fields near defects in growing thin films disrupts the local growth rate leading to increase surface roughness. To first order the surface roughness of a sample is proportional to the defect density.

2.2.5 X-ray diffraction (XRD)

X-ray diffraction can be used to determine both the composition and strain state of epitaxial thin film alloys samples by measuring the in-plane and out of plane lattice constants. In an unstrained film, the in-plane and out-of-plane lattice constants will be equal. If this is the case, then we can directly use Vegard’s law to determine the composition of the film by comparing its lattice constant to the binary or
elemental endpoint lattice constants (GaP and GaAs for GaAsP films and Si and Ge for SiGe films). Mismatch between film layers and incomplete relaxation cause the film to be tetragonally distorted \((a = b \neq c, \alpha = \beta = \gamma = 90^\circ)\). The difference between the in-plane and out-of-plane lattice constants is then related by the mechanical properties of the film and the Poisson ratio of the material. Given this, we can solve for the residual strain in the film and the unstrained lattice constant. XRD measures the intensity of diffracted x-rays as a function of the angles \(\omega\) and \(2\theta\). The angles \(\omega\) and \(2\theta\) are shown Figure 23. A rocking curve scan is a plot of the diffracted beam intensity as a function of \(\omega\). A coupled scan plots the intensity of the diffracted x-ray beam as a function of \(2\theta\) while \(\omega\) is changed in a way to maintain the relation \(\omega = 0.5(2\theta) + offset\). Peaks in the \(2\theta\) coupled scan can be used to determine the spacing between particular lattice planes using Bragg's law. A combination of rocking curves and coupled scans is performed during reciprocal space maps. The XRD scans are performed about the 004 and 224 diffraction peaks to measure both the in-plane and out of plane lattice constant of the film with respect to the substrate. The RSMs were analyzed using the MATLAB and EXCEL script developed by Adam Jandl in the Fitzgerald Group. The full theory and code can be found in the appendix of his thesis.

Figure 23 Schematic illustration of XRD geometry.
2.2.6 Secondary ion mass spectroscopy (SIMS)

Secondary ion mass spectroscopy (SIMS) was used to measure chemical concentration of various species as a function of depth in epitaxial films. The composition of alloys in addition to doping levels can be quantified throughout an epitaxial film stack. This involves the controlled sputtering of the thin film. The removed material is analyzed via a mass-spectrometer and in this way the atomic species can be determined. SIMS analysis is used to calibrate dopant flows and incorporation as well as determine contamination levels within films and measure interdiffusion between layers. The sample is damaged and destroyed during the SIMS analysis process. Evans Analytical Group was contracted to perform all of the SIMS work done in this study.
Chapter 3
Integration of GaAs$_x$P$_{1-x}$ on Si

3.1 Introduction

In chapter 1 we motivated multijunction III-V/Si solar cells due to the increased efficiency and their potential to be low cost and highly scalable. A 1.7eV band gap top cell is ideally suited to couple with a 1.1eV silicon subcell, enabling a theoretical tandem cell efficiency of 37% under AM1.5G irradiance[21]. GaAs$_x$P$_{1-x}$ alloys have large tunable direct bandgaps between 2eV – 1.4eV[22], but compositions with large bandgaps have considerable lattice mismatch with respect to any commercial substrate—including silicon. Lattice mismatch makes growth and integration of GaAs$_x$P$_{1-x}$ alloys challenging since the strain can lead to nucleation of dislocations that are detrimental to cell performance. Realizing the high theoretical efficiency of multi-junction solar cells integrated on large area silicon substrates requires high quality GaAs$_x$P$_{1-x}$ thin films with a low threading dislocation density (TDD) [23], [24]. Successful techniques for accommodating the lattice mismatch between GaAsP/Si demonstrated in literature involve the use of composition graded buffers. However, current state of the art GaAs$_x$P$_{1-x}$ cells grown on Si substrates have high densities of threading dislocations, 9.2x10$^6$ cm$^{-2}$ – 2x10$^8$ cm$^{-2}$, regardless of the graded buffer (GB) system used (GaAs$_x$P$_{1-x}$/GaAs$_x$P$_{1-x}$, GB/GaP/Si or GaAs$_x$P$_{1-x}$/Si$_x$Ge$_{1-y}$ GB/Si) [25], [26]. Moreover, defect nucleation at the III-V/IV heterointerface alone leads to a 10x – 100x increase in TDD, despite being lattice matched. Lattice matching alone is not a sufficient criteria for the growth of high quality GaAsP on SiGe graded buffers.
We performed a series of studies that investigated the effect of the GaAsxP1-x initiation sequence and the effect of strain at or near the heterointerface to elucidate the cause of defect nucleation at the III-V/IV interface. We identified two major defect mechanisms at the interface related to the reaction of P-Si and point defect condensation at the interface. Having identified the mechanism of defect nucleation at the GaAsP/SiGe interface, we developed methods to suppress these nucleation pathways. Ultimately we were able to demonstrate GaAs0.64P0.36 films grown on Si0.35Ge0.65 virtual substrates with TDD = 1x10^6 cm^-2. Before discussing the details of these studies, we will discuss key results in literature pertaining to the growth of high quality GaAsxP1-x films on SiyGe1-y substrates.

3.2 Review of GaAsP/SiGe Integration Literature

Integration of III-V semiconductor materials on Si has been a goal of the semiconductor research community since the 1970’s. There is extensive literature on the growth of GaAs on Ge and GaP on Si since there is minimal lattice mismatch at these III-V/IV heterointerfaces. The Fitzgerald Group has been investigating the optimal process window for nearly 20 years. The research presented in this thesis builds on the foundation built by the Fitzgerald Group members who pushed the boundary of III-V epitaxy on group IV substrates. Ting et al investigated the optimal growth conditions for GaAs on Ge in both molecular beam epitaxy (MBE) and MOCVD as an integration pathway for III-V on Si via GaAs/Ge/SiGe GB/Si. He found a narrow temperature window around 650°C for low-defect density GaAs on Ge [27], [28]. Dorhman et al continued the III-V integration work of Ting and investigated the growth of GaAsxP1-x alloys on relaxed SiyGe1-y virtual substrates. Dorhman found that the optimal growth temperature for GaAsxP1-x/Si yGe1-y varied with the fraction of P and Si in the layers respectively[29]. For SiyGe1-y virtual substrates with y<0.2, the optimal temperature was 650°C, similar to GaAs/Ge, whereas for virtual substrates with y > 0.2, the optimal temperature was higher, about 700°C. As the composition
shifts towards GaP/Si, the melting temperature of the two alloys increases, and the activation energy for surface reconstruction and other processes necessary for good quality epitaxy increases. Dorhman also found that the GaAsP/SiGe interface was more sensitive to surface contamination from atmospheric exposure than the GaAs/Ge interface. Dorhman was able to demonstrate mostly planar lattice matched GaAs\textsubscript{x}P\textsubscript{1-x} films on Si\textsubscript{y}Ge\textsubscript{1-y} virtual substrates (y = 0.2 – 0.5), but quality of these films was not sufficient for minority carrier device applications. Sharma continued the work of Dorhman, building on his process window [30]. He found that the deleterious effect of atmospheric surface contamination could be mitigated by burying the contaminants with a homoepitaxial layer of lattice matched Si\textsubscript{y}Ge\textsubscript{1-y} prior to growth of GaAs\textsubscript{x}P\textsubscript{1-x}. The pristine homoepitaxial surface reduced the number of heterogeneous nucleation sites that could lead to rampant formation of stacking faults, dislocations and other defects Figure 24.

Sharma showed that planar films free of antiphase domains and stacking faults was possible for GaAsP grown on SiGe virtual substrate (y = 0.15 – 0.5) using the homoepitaxial layer to suppress surface contamination. He also observed a narrowing process window as the GaAsP/SiGe composition shifted towards GaP/Si (i.e. more P and Si in the GaAsP and SiGe respectively) [31]. The temperature growth window proposed by Dorhman was further investigated by Sharma, who found that 725°C was optimal.
for GaAs$_{1-x}$P$_x$ films with $x < 0.7$ and 650°C was optimal for GaAsP films with $x > 0.7$. Considerable progress had been made by Sharma, but there was still a 10×–100× increase in the TDD of the GaAsP film with respect to the underlying SiGe virtual substrate. Sharma broadly stated that there was a narrowing process window, but did not specify a specific reasons. Additionally the mechanism of defect nucleation at the III-V/IV interface was still unclear. Using the platform for GaAsP/SiGe integration on Si, we sought to better understand the heterointerface, identify the mechanism for defect nucleation and ultimately suppress their formation to improve the material quality.

### 3.3 Experimental Methods

The studies performed focus on the GaAs$_{0.63}$P$_{0.37}$/Si$_{0.35}$Ge$_{0.65}$ interface based on the narrowing process window proposed by Sharma. This specific interface provides an ideal platform to study the defect nucleation mechanisms at the heterointerface between GaAs$_{1-x}$/Si$_{1-y}$Ge$_{1-y}$ since it has reasonable quality but is still sensitive to the growth and initiation conditions used to elucidate the active defect nucleation mechanisms at the III-V/IV heterointerface. We investigated the effect of AsH$_3$ and PH$_3$ exposure to the Si$_{0.35}$Ge$_{0.65}$ virtual substrate just prior to the growth of GaAs$_{1-x}$ and its effect on the TDD and film quality of the GaAs$_x$P$_{1-x}$ layer. The second series of experiments investigated the effect of strain at or near the GaAs$_{0.63}$P$_{0.37}$/Si$_{0.35}$Ge$_{0.65}$ interface.

All of the experiments in this chapter involve the deposition of GaAs$_{1-x}$P$_x$ thin films on Si$_{1-y}$Ge$_{1-y}$ virtual substrates grown on 150mm Si wafers. The process of producing these epitaxial thin film stacks consists of two distinct parts: the UHVCVD graded buffer growth from Si to Si$_{0.35}$Ge$_{0.65}$ and the MOCVD growth of additional composition grading Si$_{1-y}$Ge$_{1-y}$ and GaAs$_x$P$_{1-x}$ growth. The standard processing UHVCVD SiGe graded buffer growth was established in the Fitzgerald Research Group by Currie, Pitera and Dorhman.
Figure 25 Schematic representation of the GaAsP/SiGe integration process flow. The Si wafers are subjected to a wet clean before growth. The initial Si<sub>0.50</sub>Ge<sub>0.50</sub> graded buffer is grown in the UHVCVD. A CMP step is used to remove crosshatch surface morphology caused by the graded buffer. Finally, additional grading and growth of GaAsP is performed in the MOCVD reactor.

Additional details of the growth optimization can be found in their work. The standard MOCVD process for SiGe regrowth, additional composition grading and growth of GaAsP was developed by Dorhman and Sharma—shown in Figure 25. We use the process parameters established by these previous group members to start our optimization studies. The standard process for creating the Si<sub>x</sub>Ge<sub>1-y</sub> virtual substrate and subsequent GaAs<sub>x</sub>P<sub>1-x</sub> deposition used by Sharma is listed below. After outlining the standard GaAsP/SiGe growth protocol, we will discuss the specific variables investigated for our optimization studies.

### 3.3.1 Preparation of Si<sub>0.50</sub>Ge<sub>0.50</sub> Virtual Substrates

All of the growths in this study were performed on 150mm double-side polished CZ (100) Si wafers with a 6° offcut towards the nearest (111) plane purchased from Okmetic. The 6° offcut is important for
the formation of a double stepped surface reconstruction that leads to the suppression of anti-phase boundaries that can form during the growth of III-V semiconductor materials on group IV semiconductor materials. Under appropriate annealing conditions, the surface goes from a combination of single and odd numbered surface steps to an array of single domain double step surfaces. This reconstruction is driven by a reduction in the surface free energy [32].

The Si wafer surfaces are prepared for growth through a series of wet chemical cleans designed to strip any surface particles, organic contaminants or surface oxide layers that could impede epitaxy. The wafers are submerged in a boiling (T>100°C) piranha mixture (3:1 H₂SO₄:H₂O₂) for 10 minutes. The reaction of mixing H₂SO₄ and H₂O₂ is exothermic leading to the spontaneous heating of the acid solution. Piranha mixture is a strong oxidizer that is very effective at removing organic contaminants on the wafer surface. After 10 minutes, the Si wafers are hydrophilic due to the silicon surface oxide layer being –OH terminated. The wafers are rinsed in flowing DI water until the rinse effluent has a resistivity of 18.8 MOhm-cm (approximately 20 – 40 minutes). After rinsing, the wafers dipped in a dilute HF solution (1:10 HF:H₂O) for 1 minute. The HF solution strips the surface oxide layer by forming gaseous and water soluble silicon fluoride compounds, yielding a pristine hydrogen terminated Si surface that is hydrophobic. The hydrogen terminated surface resists oxidation during the time period of wafer cleaning to being loaded into the CVD reactor [33], [34].

The initial Si₆Ge₆-x graded buffer growth is batch processed 10 wafers at a time in an ultra-high vacuum chemical vapor deposition (UHVCVD) reactor at a nominal growth pressure of 25 mTorr. The growth pressure is set by adjusting a throttle gate valve over the main process turbo. The growth of graded buffers from Si to Si₀.₅Ge₀.₅ is done at 900°C with SiH₄ and GeH₄ precursors. Doping of the graded buffer is done with either PH₃ or B₂H₆ for n-type and p-type respectively. The quartz wafer boat is coated in 1µm of Si to bury any surface contaminants prior to loading wafers. The 10 cleaned Si wafers are loaded into the freshly coated quartz boat and put in the load lock were they are pumped to a based pressure of
<10\(^{-8}\) torr prior to transferring to the main reaction chamber. The growth begins with a homoepitaxial Si layer to bury any surface contaminants that might remain after the surface clean or were introduced while pumping down the load lock. A pristine surface is important for graded buffer growth as contaminants could pin dislocation glide or act as heterogeneous nucleation sites for dislocations. After the growth of a homoepitaxial Si layer, a compositionally step-graded $\text{Si}_x\text{Ge}_{1-x}$ buffer is grown consisting of a series of 200nm layers with increasing Ge content, 2% Ge per layer, for a nominal grade rate of $\Delta x_{\text{Ge}} = 0.10/\mu\text{m}$. The graded buffer growth continues to $\text{Si}_{0.5}\text{Ge}_{0.5}$ and capped with a 1.5 $\mu\text{m}$ thick, fully relaxed $\text{Si}_{0.5}\text{Ge}_{0.5}$ layer.

During the growth of graded buffers the misfit strain is relaxed via the glide of dislocations, resulting in an orthogonal array of misfit dislocations. The strain field around these dislocations influences adatom surface mobility, locally increasing and decreasing growth rates. The variation in growth rates leads to the evolution of a crosshatched surface morphology characteristic of lattice mismatched epitaxy. The undulating crosshatch morphology can impede the glide of threading dislocation segments during continued grading, which can cause dislocation pile-ups and potentially increase threading dislocation density. The surface morphology due to cross hatch is removed with chemical mechanical polishing (CMP), which yields a specular smooth surface (RMS roughness < 1nm). The $\text{Si}_x\text{Ge}_{1-x}$ graded buffers with relaxed $\text{Si}_{0.5}\text{Ge}_{0.5}$ cap are removed from the UHVCVD reactor and both sides of the wafer are planarized using CMP to remove the surface crosshatch. Following the CMP process, the wafers are cleaned with two consecutive rounds of piranha/HF wet chemical etches. Multiple cycles of oxidation/oxide-removal eliminate any residual surface contaminants from the CMP process such as slurry particles. Following the double wet clean, the wafers are ready for continued $\text{Si}_x\text{Ge}_{1-x}$ graded buffer growth and integration of lattice matched $\text{GaAs}_x\text{P}_{1-x}$.
The subsequent depositions are performed in a specially designed Aixtron close-coupled showerhead metal-organic chemical vapor deposition (MOCVD) reactor that has precursors for both III-V compounds and IV compounds in the same chamber. This unique characteristic enables the integration of GaAs$_x$P$_{1-x}$ alloys on Si$_y$Ge$_{1-y}$ substrates without exposure to atmospheric contamination between depositions. The remaining Si$_y$Ge$_{1-y}$ graded buffer growth and GaAs$_x$P$_{1-x}$ growth is deposited in the MOCVD at a growth pressure of 100 torr using either an N$_2$ or H$_2$ carrier gas flowing at 20 slpm using SiH$_4$, GeH$_4$, AsH$_3$, PH$_3$ and tri-methyl gallium (TMGa) as precursors for the Si, Ge, As, P and Ga, respectively. Just prior to loading in the reactor, the Si$_{0.5}$Ge$_{0.5}$ substrates are subjected to the same pirhana/HF clean mentioned previously. The Si$_{0.5}$Ge$_{0.5}$ virtual substrate is annealed at 825°C in N$_2$ for 10 minutes to desorb any moisture or other atmospheric contamination prior to initiating growth. Similarly to the UHVCVD growth, a Si$_{0.5}$Ge$_{0.5}$ homoepitaxially is grown at 825°C under an H$_2$ ambient to bury any remaining contaminants and to ensure a pristine surface for subsequent growth. The temperature is reduced to 750°C for additional Si$_y$Ge$_{1-y}$ grading. The Si$_y$Ge$_{1-y}$ graded buffer is terminated with a 1µm constant composition Si$_y$Ge$_{1-y}$ cap layer.

Following the growth of the Si$_y$Ge$_{1-y}$ graded buffer, the carrier gas is switched to N$_2$ and the temperature is reduced to 725°C for the growth of GaAs$_x$P$_{1-x}$. Growth of GaAs$_x$P$_{1-x}$ is initiated by flowing TMGa, AsH$_3$ and PH$_3$ into the reactor simultaneously. The GaAs$_x$P$_{1-x}$ film is nucleated with a high V/III ratio (>200) for the first 50 nm of growth by flowing TMGa at 20 sccm. Following the nucleation layer the TMGa flow is increased to 50 sccm for the remainder of the film growth to achieve a reasonable growth rate. A total flow of AsH$_3$ + PH$_3$ is maintained at 400 sccm during growth of GaAs$_x$P$_{1-x}$. The fraction of AsH$_3$ and PH$_3$ in the gas phase determines the fraction of As and P incorporated into the GaAs$_x$P$_{1-x}$ film. The rate of incorporation is based on the cracking activation energy for the precursors. Stringfellow found the functional relationship for incorporation of As and P into the GaAsP film to be:
Equation 10

\[
\frac{1-x}{x} = c \frac{P_{PH_3}}{P_{AsH_3}}
\]

Where \( x \) is the fraction of \( P \) in the film and \( P_{AsH_3} \) and \( P_{PH_3} \) are the partial pressures of \( AsH_3 \) and \( PH_3 \) respectively and \( c \) is a fitting constant that is temperature dependent. From the GaAsP films grown in the SEL, the fitting parameters are 0.38, 0.12, 0.05 and 0.35 for 725°C, 650°C, 600°C and 550°C growth temperature respectively. Figure 26. Drift in the temperature balance and calibration of the MOCVD graphite heater can lead to composition drift for a given \( AsH_3 \) and \( PH_3 \) flow. Spot check calibration growths are performed periodically to recalibrate the flows for particular GaAsP compositions.

Figure 26 a.) GaAsP growth temperature calibration data from Stringfellow. b.) GaAsP Growth calibration data for films grown in the SEL.
3.4 GaAs_{x}P_{1-x} Initiation Study

3.4.1 Initiation Experimental Parameters

Just prior to growth of the GaAs_{x}P_{1-x} layer, the Si_{0.35}Ge_{0.65} surface is exposed to either a short (3sec) or long (10sec) pre-flow of AsH_{3}, AsH_{3} + PH_{3}, or PH_{3}. Immediately following the pre-growth hydride exposure, a lattice matched GaAs_{0.63}P_{0.27} layer is grown by introducing TMGa, AsH_{3} and PH_{3} to the reactor. The initiation flow rates for AsH_{3} and PH_{3} are the same flows used during growth, 140 sccm and 260 sccm respectively. The GaAs_{x}P_{1-x} film is nucleated with a high V/III ratio of 257 for the first 50nm after which the TMGa flow is increased and the remainder of the film is grown at a V/III ratio of 103. The growth rate of the GaAs_{x}P_{1-x} film during the high and low V/III ratio periods is about 0.12nm/s and 0.6nm/s respectively.

Post-growth analysis of epitaxial interface quality is done by cross section transmission electron microscopy (XTEM) and film defect density is measured using plan view transmission electron microscopy (PVTEM). All TEM measurements are performed using a JEOL 2011 TEM at 200keV accelerating voltage using a double-tilt sample holder. Composition and strain of epitaxial layers is characterized using high resolution x-ray diffraction (HRXRD) on a Bruker D8 HRXRD with a copper anode x-ray source and a four-bounce Ge(022) incident beam monochromator. Surface morphology is characterized using atomic force microscopy (AFM) performed with a Veeko NanoScope IV operated in tapping mode.
3.4.1 Effect of group-V hydride pre-flow exposure prior to growth of GaAs$_x$P$_{1-x}$ on Si$_{0.35}$Ge$_{0.65}$ substrate

An exemplar Si$_{0.35}$Ge$_{0.65}$ substrate is used to establish a baseline TDD and surface roughness by which the GaAs$_x$P$_{1-x}$ initiation experiments can be compared. Increases in TDD and surface roughness are indicative of defect nucleation at the heterointerface. The as-grown exemplar wafer is specular with cross-hatch surface morphology characteristic of metamorphic graded buffers observable in Nomarski optical microscopy Figure 27. From AFM scans of the exemplar wafer, the root-mean squared (RMS) surface roughness and minimum-to-maximum height are 6.4 nm and 36 nm respectively. Dislocation selective etch pit density measurements (EPD) performed on the exemplar Si$_{0.35}$Ge$_{0.65}$ substrate show an average defect density of $4.3 \pm 0.6 \times 10^5 \text{cm}^{-2}$. The standard error of the sample mean is reported as the uncertainty in the average EPD/TDD values listed in this report. The EPD measurements confirm that the ~2.7% lattice

<table>
<thead>
<tr>
<th>Sample Conditions</th>
<th>20um x 20um RSM Roughness (nm)</th>
<th>Min-to-Max (nm)</th>
<th>EPD/TDD ($10^6 \text{cm}^{-2}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si$<em>{0.35}$Ge$</em>{0.65}$ Exemplar</td>
<td>8.4</td>
<td>36</td>
<td>0.43 ± 0.06</td>
</tr>
</tbody>
</table>

Table 1 Summary of surface morphology and defect density measured via AFM and EPD/PVTEM for a Si$_{0.35}$Ge$_{0.65}$ exemplar wafer and GaAsP/SiGe initiation samples.
mismatch between Si and $\mathrm{Si}_{0.35}\mathrm{Ge}_{0.65}$ can be accommodated while retaining high material quality. A summary of the EPD/TDD and surface morphology measurements for the $\mathrm{Si}_{0.35}\mathrm{Ge}_{0.65}$ exemplar sample as well as the GaAsP/SiGe initiation samples are listed in Table 1. AFM scans of the $\mathrm{PH}_3$ initiation sample reveal a rough, pitted surface while the other GaAsP/SiGe initiation samples exhibit similar cross hatch morphology as the $\mathrm{Si}_{0.35}\mathrm{Ge}_{0.65}$ exemplar with only slight fine scale surface texturing. Samples with any pre-exposure to $\mathrm{PH}_3$ generally have rougher surface morphologies and considerably higher densities of threading dislocations observed in PVTEM compared to those samples with either a short $\mathrm{AsH}_3$ exposure or no initiation sequence (i.e. flow TMGa, $\mathrm{PH}_3$, and $\mathrm{AsH}_3$ simultaneously) as shown in Figure 28. Cross section TEM of the $\mathrm{PH}_3$ initiation sample reveals an interface fraught with dislocations, indicating the high density of threading dislocations observed in PVTEM are a result of nucleation events at the
**Short PH$_3$ initiation (3s)**

TDD = $1 \times 10^9$ cm$^{-2}$

**TMGa + AsH$_3$ + PH$_3$ (control)**

TDD = $1 \times 10^7$ cm$^{-2}$

**Short AsH$_3$ initiation (3s)**

TDD = $5 \times 10^6$ cm$^{-2}$

---

Figure 29 Bright field XTEM ($g = 220$ two-beam) images showing the GaAsP/SiGe interface for various initiation conditions.

In contrast to the PH$_3$ initiation samples, XTEM of the no initiation and short AsH$_3$ exposure sample shows a smooth interface without defect contrast, indicative of minimal defect nucleation.

This massive increase in dislocation density and surface roughness in the PH$_3$ initiation sample is attributed to the high reactivity of Si and P at elevated temperatures on the wafer surface. Scanning tunneling microscopy (STM) studies by Lutz, Wang, Kipp, and more recently Curson revealed phosphine exposure to silicon (100) surfaces generate excessive amounts of vacancies and surface disruption due to ejected silicon atoms[35]–[37]. The formation of P-P surface dimers leads to the development of surface stress. This stress can be relaxed by forming Si(111):P microfacets—shown in Figure 30. Similar trends are observed at high Si(100) surface coverages with As as well. PH$_3$ These P-passivated facets can lead to the formation of stacking faults or APB formation during subsequent epitaxy. Silicon surface degradation under PH$_3$ exposure has been well documented in the GaP/Si community, so it is not surprising that it would degrade the GaAsP/SiGe interface, especially at the high temperatures used in this study. While damaging to Si surfaces, STM studied have shown that extended PH$_3$ exposure does not degrade Ge
These findings correlate well with the narrowing GaAsP/SiGe process window reported Sharma. The pre-growth exposure of PH₃ to the SiₓGe₁₋ₓ saturates the surface with P, which reacts negatively with Si and ultimately degrades the GaAsₓP₁₋ₓ film quality.

Figure 30 STM filled state image (+2V bias) of a Si(100) surface following 5min anneal at 500°C (approximate dimensions 90nm x 90nm); (b) Schematics of a vacancy line parallel to the P-P dimer rows (black bars) that continues of monoatomic steps and appears then as a vacancy line perpendicular to the dimer rows; (c) Possible atomic structure of vacancy lines parallel (left) and perpendicular (right) to dimer rows on phosphorous passivated Si(100). The trenches are formed by Si(111):P micro facets to relieve stress and reduce the number of dangling bonds. P and Si atoms are plotted as full and open circles respectively. Reproduced from Lutz [36]
As the initiation condition shifts from a PH\textsubscript{3} ambient to a mixed ambient of PH\textsubscript{3}+AsH\textsubscript{3}, there is nearly a 15x reduction in the GaAs\textsubscript{x}P\textsubscript{1-x} film threading dislocation density. AsH\textsubscript{3}, PH\textsubscript{3} and their subsequent dissociation products directly compete for surface sites during the short hydride exposure which limits the amount that Si and P can react, thereby improving film quality. The threading dislocation density is further reduced by nearly a factor of 5 when TMGa is introduced to the reactor simultaneously with the hydride precursors. In addition to site competition, the Ga atoms rapidly bind with As and P during the growth of the GaAs\textsubscript{x}P\textsubscript{1-x}. Based on growth rate, approximately one second after all of the precursors are introduced to the reactors all of the Si\textsubscript{0.35}Ge\textsubscript{0.65} surface sites are filled with Ga, As and P atoms, with the P strongly bond to the Ga. This leaves little time for side reactions between silicon and phosphorus to take place, thereby reducing surface roughness and threading dislocation density.

![Figure 31 TEM images of the long (10s) AsH\textsubscript{3} initiation sample (a) PVTEM orientation (b) cross-section orientation.](image-url)
A short AsH$_3$ initiation provides the lowest TDD and surface roughness of the lot—comparable to that of the Si$_{0.35}$Ge$_{0.65}$ exemplar. The short exposure enables the AsH$_3$ to adsorb to the Si$_{0.35}$Ge$_{0.65}$ surface, decompose, and fill the available surface sites with arsenic atoms. This functions to further limits interaction between Si surface sites and P by populating many of the Si sites with adsorbed As. While a moderate exposure to AsH$_3$ prior to film growth greatly improved the GaAs$_x$P$_{1-y}$ quality, prolonged exposures to AsH$_3$ increased the threading dislocation density in the film from $5 \times 10^6$ cm$^{-2}$ to $2.33 \times 10^8$ cm$^{-2}$ which is readily seen in Figure 31. Other authors have shown that in the case of GaAs growth on Ge grown by molecular beam epitaxy, prolonged exposures to As$_2$ lead to the formation of antiphase boundaries dislocations at the III-V/IV interface[39]. McMahon studied the surface effects of AsH$_3$ and PH$_3$ exposure to Si surfaces using STM. He observed that at high surface coverages—especially at elevated temperature—the As or P atoms dimerize on the surface—this is shown schematically in Figure 32. As the

![Figure 32 Model for dimer exchange mechanism during As adsorption on Si(100)-(2x1): (a) Si dimers on the clean surfaces; (b) the incoming As atoms breaks the existing dimers and creates a new As dimer on top; (c) the pair of As atoms then exchanges places with a pair of underlying Si atoms; (d) the top Si dimer diffuses away; (e) a new As dimer is formed on top; (f) the place exchanges process is repeated; (g) the top Si dimer diffuses away, leaving two new As-dimers parallel to the original Si dimers. Reproduced from Yu [81].](image-url)
surface dimers shift from a Si-Si bonded pair to Si-As and finally As-As, a substantial amount of surface stress develops. The Si surface can relax this surface stress through the formation of faceted trenches and other rough surface morphology Figure 33. The same sort of surface morphology was observed in PH$_3$ exposure studies. McMahon concluded that the dimer surface strain was causing the surface roughening for both AsH$_3$ and PH$_3$ exposure. In addition to the strain relaxation mechanism, atomic H from decomposing AsH$_3$ and PH$_3$ leads to etching of the Si substrate. The two effects are seen clearly in STM images of AsH$_3$ exposed surfaces—long trenches form as a strain relaxation mechanism and shallow wide trenches form due to etching. The higher reactivity of P-Si could lead to faster roughening than As-Si. Additional STM studies have reported that prolonged exposure to AsH$_3$ at elevated temperatures, especially at the high AsH$_3$ fluxes like those used in MOCVD growth, etches Si surfaces[40] and Ge surfaces[38]. The optimal initiation condition is one that is long enough to suppress P-Si interaction, but not so long that the Si$_{0.35}$Ge$_{0.65}$ surface begins to roughen due to AsH$_3$ attacking the Si$_x$Ge$_{1-y}$ surface.
3.4.2 Time dependence of As and P adsorption to Si$_y$Ge$_{1-y}$ Surfaces

The optimal GaAs$_x$P$_{1-x}$ initiation sequence is shown to be sensitive to hydride species exposure and duration, which is attributed to competition between AsH$_3$ and PH$_3$ for Si surface sites. The adsorption kinetics of AsH$_3$ and PH$_3$ behave similarly on Si(001) and Ge(001) surfaces and both have been show to rapidly dissociate into As, P, and H at temperature $>500^\circ$C [41], [42]. Hydrogen readily desorbs form Si(001) and Ge(001) surfaces at these elevated temperatures, therefore As and P will account for most of the filled surface sites. The fraction of surface sites filled by As or P can be calculated using a competitive Langmuir model, which is composed of an adsorption rate term and desorption rate term. Both processes have been shown to exhibit second-order reaction kinetics for this system and have the functional form:

Equation 11

$$\frac{d\theta_{AS}}{dt} = \frac{(J_{ASH}S_{ASH})}{N_s}(1 - \theta_{AS} - \theta_P - \theta_H)^2 - k_{d,AS}\theta_{AS}^2$$

Equation 12

$$\frac{d\theta_P}{dt} = \frac{(J_{PH}S_{PH})}{N_s}(1 - \theta_{AS} - \theta_P - \theta_H)^2 - k_{d,P}\theta_P^2$$

Equation 13

$$\frac{d\theta_H}{dt} = \frac{3(J_{PH}S_{PH} + J_{ASH}S_{ASH})}{N_s}(1 - \theta_{AS} - \theta_P - \theta_H)^2 - k_{d,H}\theta_H^2$$

Where $\theta_i$ is the fraction of surface sites filled by an adsorbed chemical species, $J_i$ is the molecular flux of hydride species, $k_{d,i}$ is the desorption rate constant, $N_s$ is the adsorption surface site density, for Si this is $6.8 \times 10^{14}$ cm$^{-2}$, and $S_i$ is the zero-coverage reactive sticking probability. AsH$_3$ and PH$_3$ surface kinetics data
Figure 34 Langmuir adsorption model showing fraction of Si sites filled with P, As, or H as a function of time under MOCVD growth conditions ($T = 725^\circ C$ and $J_{AsH_3} = 1.87 \times 10^{17} \text{cm}^{-2}\text{s}^{-1}$ and $J_{PH_3} = 3.48 \times 10^{17} \text{cm}^{-2}\text{s}^{-1}$). All sites are empty at $t=0$. a.) PH$_3$ exposure only.

From gas-source molecule beam epitaxy studies are used for the desorption rate and sticking coefficient. The desorption rate constant for As, P and H on a Si(100) surface are $k_{d,As} = 1 \times 10^{13} \exp(-3eV/k_BT)$ and $k_{d,P} = 4.2 \times 10^{11} \exp(-2.64/k_BT)$, $k_{d,H} = 1 \times 10^{15} \exp(-2.52/k_BT)$. $S_{AsH_3}$ and $S_{PH_3}$ are the zero-coverage reactive sticking coefficient for AsH$_3$ and PH$_3$; for a Si surface the values are 0.3 and 1 respectively. The molecular flux of AsH$_3$ and PH$_3$ to the wafer surface used for all of the experiments in this study is $1.87 \times 10^{17} \text{cm}^{-2}\text{s}^{-1}$ and $3.48 \times 10^{17} \text{cm}^{-2}\text{s}^{-1}$ respectively. The fraction of Si surface sites filled with As or P as a function of exposure time is calculated using equations 1 – 3 given an incident flux of PH$_3$, AsH$_3$ + PH$_3$ or AsH$_3$ Figure 34.

From the Langmuir model we see that even a short exposure of either PH$_3$ or AsH$_3$ leads to nearly all available silicon sites being filled with P or As respectively. The AsH$_3$ + PH$_3$ initiation also has near unity site coverage, but As and P compete for sites, thus the fraction of surface sites filled by either species is lower than the fraction for AsH$_3$ or PH$_3$ exposure alone. Because of the high hydride gas flux during MOCVD growth, the surface coverage rapidly saturates in about 0.5s. It is possible shorter AsH$_3$ initiation exposures ($t_{AsH_3} = 0.5s - 3s$) would suffice to prevent P-Si reaction and limit possible etching of the Si$_x$Ge$_{1-y}$ surface from excessive exposure. While the calculated surface coverages presented here only
accounts for Si surface sites and rely on surface kinetic data from AsH$_3$:Si and PH$_3$:Si GS-MBE studies, they provide insight to Si$_x$Ge$_{1-x}$ surfaces exposed to group-V hydride precursors at the temperature and flows typical of MOCVD growth.

3.5 GaAsP Initiation Study Conclusions

Growth of high quality GaAs$_x$P$_{1-x}$ material requires careful initiation procedures to suppress defect nucleation at the III-V/IV interface. Any PH$_3$ exposure to the Si$_{0.35}$Ge$_{0.65}$ interface leads to considerable surface roughening and to a 100x – 1000x increase in TDD with respect to the underlying Si$_{0.35}$Ge$_{0.65}$ substrate. We demonstrated that a short (3 sec) exposure of AsH$_3$ prior to growth of GaAs$_{0.63}$P$_{0.27}$ on Si$_{0.35}$Ge$_{0.65}$ produced the best quality films (TDD = 5x10$^6$ cm$^{-2}$) by suppressing adverse Si-P reactions that

![Threading dislocation density graph](image)

Figure 35 Threading dislocation density for lattice matched GaAsP films grown on SiGe virtual substrates are shown as a function of the initiation condition used. The initiation condition and duration is listed next to the points on the plot. While an AsH$_3$ initiation improves the TDD, there is still a 5x increase in TDD with respect to the underlying SiGe substrate.
degrade film quality. While a short exposure of AsH₃ is found to improve GaAsP film quality, long exposures (10 sec) are shown to cause high TDD (>10⁸ cm⁻²). The competitive Langmuir model showed that Si surface sites saturate rapidly with As under MOCVD growth conditions. It is possible that shorter AsH₃ initiations (t_{AsH₃} < 3sec) might improve quality as it reduces time for side reactions that degraded the Si₀.₃₅Ge₀.₆₅ surface while still maintaining the same level of As coverage. While the optimized GaAsP/SiGe initiation sequence enables growth of high quality GaAsP films suitable for PV applications, there is still almost a 10x increase in TDD occurring at the III-V/IV interface. Continued investigation of the GaAsP/SiGe interface is necessary to elucidate and suppress the remaining defect nucleation mechanisms at work.

3.6 Effect of strain at the GaAsP/SiGe interface

3.6.1 Introduction

In the previous section we optimized the initiation of GaAsP/SiGe to suppress the reaction between Si and P at the heterointerface. This improved the material quality, but there is still a 5x increase in the TDD of the GaAsP film compared to the underlying SiGe virtual substrate. The subsequent sections investigate the nucleation source that leads to an increase in TDD. We performed a series of experiments to investigate the effect of strain at or near the GaAsₓP₁₋ₓ/SiₓGe₁₋ₓ interface. Strain is a potential handle that can be altered experimentally to interrogate and bias defect mechanisms at the GaAsP/SiGe interface one way or another. Strain can be intentionally introduced epitaxial thin films by adjusting the composition of either the GaAsₓP₁₋ₓ or SiₓGe₁₋ₓ layer with respect to one another. The sign of the strain at the GaAsP/SiGe interface turned out to be an important parameter in determining the quality of GaAsP films.
All of the experiments listed below implement the optimized 3 sec AsH$_3$ GaAs$_x$P$_{1-x}$ initiation sequence. The goal of these studies is to identify the source of the 5x increase in TDD at the GaAsP/SiGe interface that persisted despite suppressing the P-Si reaction. Three sets of experiments are performed. The first investigate the effect of straining only the GaAs$_x$P$_{1-x}$ film. We identified point defect condensation as the cause of the dislocation source. These point defects condense into dislocation loops that expand to the thin film surface, forming a half-loop with two threading segments. The second set of experiments investigated using thin strained layers near the interface to confine the dislocation loops and prevent their expansion into half-loops. The last set of experiments investigated the use of thin strained layers at the GaAsP/SiGe interface to bias the concentration of point defects and ultimately suppress their condensation into loops. These studies culminated in the demonstration of GaAs$_x$P$_{1-x}$ on Si$_{0.35}$Ge$_{0.65}$ with a TDD = 1.2x10$^6$ cm$^{-2}$, approximately the same level as the underlying Si$_{0.35}$Ge$_{0.65}$. 

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3.6.2 Effect of strain in GaAsP grown on Si$_{0.35}$Ge$_{0.65}$

We investigated the effect of small amounts of lattice mismatch in the GaAs$_x$P$_{1-x}$ film with respect to the Si$_{0.35}$Ge$_{0.65}$ virtual substrate. The deliberate lattice mismatch in the GaAs$_x$P$_{1-x}$ layer introduces a small amount of strain in the film. For this study, three different compositions of GaAs$_x$P$_{1-x}$ films were deposited on Si$_{0.35}$Ge$_{0.65}$ virtual substrates. The composition of the GaAs$_x$P$_{1-x}$ films were $X_{As} = 0.58$, 0.63 and 0.69 which corresponds to 0.2% tensile strained, lattice-matched and 0.2% compressive strained GaAs$_x$P$_{1-x}$ films with respect to the lattice constant of Si$_{0.35}$Ge$_{0.65}$. Schematics of the structures grown are shown in Figure 36.

The GaAs$_x$P$_{1-x}$ films were grown to a thickness of 500nm, which is greater than the Matthews-Blakeslee critical thickness. The GaAs$_x$P$_{1-x}$ film is capped with a thin InGaP cap layer to prevent surface roughening due to uncontrolled non-stoichiometric depletion of As and P species from the wafer surface as it cools to the room temperature. The samples were characterized with plan-view and cross-sectional transmission electron microscopy (PVTEM and XTEM) to study the microstructure and interface quality of the thin films. The composition and strain within the epi-layers is measured using high-resolution x-ray diffraction (HRXRD).

![Figure 36 Schematic illustrations of (a) 0.2% tensile strained, (b) lattice-matched and (c) 0.2% compressive strained GaAsxP1-x on Si0.35Ge0.65 structures fabricated as part of this study. The final Si fraction for the films examined in this study was $Y_{Si} = 0.35$](image-url)
3.6.3 Experimental Results

From visual inspection of the wafers, the compressive samples appear hazy while the other samples are specular in appearance with the typical crosshatch morphology being visible. Plan-view TEM done on these samples reveals a high density of threading dislocations and stacking faults in the compressively strained sample (TDD>10⁹ cm⁻²) Figure 38. The lattice matched and tensile strained samples had a TDD = 5x10⁶ cm⁻² and were free of stacking faults. XTEM of these samples was performed to identify from where the dislocations observed in PVTEM were originating. The lattice matched and tensile strained sample exhibit smooth interfaces with few if any defects visible at the GaAsP/SiGe interface whereas the compressive strained GaAsP/SiGe interface is fraught dislocations and stacking faults Figure 37. The XTEM images indicate the high density of threading dislocations observed in PVTEM of the compressive strained sample are the result of some nucleation process active at the heterinterface and is not an artifact of the SiₓGe₁₋ₓ graded buffer. AFM scans of the tensile strained and lattice matched sample exhibited similar smooth surface morphology whereas the compressive sample exhibited a rough pitted surface Figure 39. The increased surface roughness and pitting is attributed to defects that nucleate at the III-V/IV interface and locally suppressed the growth rate.
Figure 38 Representative plan-view <220> bright field TEM image of (a) 0.2% tensile strained, (b) lattice-matched and (c) 0.2% compressive strained GaAsxP1-x grown on Si0.35Ge0.65 virtual substrates.

Figure 37 Cross-sectional <220> bright field TEM of (a) 0.2% tensile strained, (b) lattice-matched and (c) 0.2% compressive strained GaAsxP1-x on Si0.35Ge0.65 virtual substrates.

Figure 39 Representative AFM images of (a) 0.2% tensile strained, (b) lattice-matched and (c) 0.2% compressive strained GaAsxP1-x grown on Si0.35Ge0.65 virtual substrates.
3.6.4 Discussion

The results show clearly that the GaAsP/SiGe interface is not tolerant to compressive strain in the GaAsP layer, but tensile strain seems to have minimal effect. Clearly there is some mechanism that is at work that depends strongly on the sign of the strain not just the magnitude. It is surprising that this level of strain (0.2%) would lead to nucleation of additional threading dislocation segments given that it is comparable to the amount introduced during graded buffer growth. Furthermore, the amount of dislocations nucleated, if any, due to relaxing this amount of strain via nucleation rather than glide is expected to be equivalent for tensile and compressive strain. Observing a 100x increase in TDD from relaxation alone in the compressive case is unlikely, rather there is some other mechanism at work. Additionally when we performed a similar set of experiments on the Si$_{0.15}$Ge$_{0.85}$ lattice constant and observed the same sensitivity to compressive strain, though to a lesser extent, and minimal effect from tensile strain Figure 40. Faucher et al observed a 10x increase in TDD at the GaAsP/SiGe interface GaAsP single junction solar cells grown compressively mismatched on a Si$_{0.2}$Ge$_{0.8}$ virtual substrate [43]. These multiple observations demonstrated that the defect nucleation in compressive strained GaAsP was not particular to the Si$_{0.35}$Ge$_{0.65}$ lattice constant, but characteristic of the GaAsP/SiGe heterointerface as a whole.

![GaAsP micrographs](image)

Figure 40 XTEM micrographs of strained GaAs$_x$P$_{1-x}$ grown on Si$_{0.15}$Ge$_{0.85}$ virtual substrate. a.) 0.3% tensile strain b.) 0.2% compressive strain
3.7 Dislocation loops at the GaAsP/SiGe interface

To explain the vastly different dislocation density observed in compressive strained GaAs$_x$P$_{1-x}$ films we propose that an excess of point defects accumulate at the GaAsP/SiGe interface which then condense into dislocation loops. These dislocation loops then expand until they reach the surface of the thin film, leaving behind a half-loop dislocation with two threading dislocation segments. The process is shown schematically in Figure 41. Experimental observation of dislocation loops and expanded half-loop threading segments were observed in XTEM and PVTEM of the tensile GaAsP/SiGe interface Figure 42.

![Figure 41 Proposed dislocation loop mechanism: point defects accumulate during the nucleation of GaAsP/SiGe. Super-saturated point defects condense into dislocation loops. Dislocation loops continue to grow as they absorb point defects until they reach the crystal surface—leaving a half loop with two threading segments. These threading segments remain after continued growth.](image-url)
Figure 42 XTEM micrograph of the GaAsP/SiGe interface imaged under the g = 220 two-beam condition. A.) Dislocation loop nucleating at the heterointerface. B.) A dislocation loop that broke into a half loop after intersecting the surface during growth.

Point defects present at the III-V/IV interface can be the result of multiple processes. Charged point defects could be generated to maintain charge neutrality at the III-V/IV interface. Harrison et al showed that an As-first or Ga-first interface between (001) GaAs/Ge results in an accumulation of charge that is not energetically favorable or stable [44]. Mixing of Ga, Ge and As over multiple monolayers in addition to generating charged point defects prevents this charge accumulation. SIMS scans of the GaAsP/SiGe interface show considerable amounts of intermixing—both Si and Ge going into the GaAs$_x$P$_{1-x}$ as well as As and P into the Si$_y$Ge$_{1-y}$. In addition to an imbalance of diffusion rates across the GaAsP/SiGe interface, heavy doping of GaAs films has been shown to increase the vacancy concentration through positron annihilation lifetime studies by Chichibu et al [45]. The strain state and composition of the thin film layers effects the vacancy formation energy. In the case of Si$_x$Ge$_{1-x}$ alloys, the vacancy formation energy is inversely proportional to the fraction of Ge in the film[46] Figure 43a. Choi et al investigated the formation energy of vacancies in Ge single crystals through density-functional theory models and found the
formation energy decreases with biaxial compressive strain[47] Figure 43b. In addition to vacancies being more easily formed in compressive strain fields, it is also energetically favorable for the vacancies to cluster in compressive strain fields [48] Figure 43c. The combination of high germanium content at elevated temperatures with biaxial compressive strain creates an environment favorable to high concentrations of vacancies that tend to want to cluster. Combined, these favor the formation of voids and dislocation loops. From a thermodynamic perspective, the type of point defect is likely vacancies as this would explain in the previous study why compressive strained GaAsP had such a high density of dislocations observed in PVTEM. It is unfavorable for vacancies to form in a tensile strain field and there is less driving force for them to diffuse towards a tensile strained region.

The driving force for point defect condensation is a super saturation of these defects above the equilibrium concentration. The concept of vacancy condensation into dislocation loops was proposed by Nabarro in 1947. Since then the theory has been expanded on by many others: Frank, Reed, Fisher and Krouta [49]. Extensive details on the mechanics of dislocations and their interactions with point defects can be found in the above listed authors work. Excess vacancies above the equilibrium concentration level drives their precipitation into either spherical voids or dislocation loops. The free energy of these two structures relates to the geometry where
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Equation 14

\[ E_{\text{spherical void}} = \frac{4}{3} \pi r^2 \gamma \]

Equation 15

\[ \text{Surface Area} = \frac{4}{3} \pi r^2 \sim n b^2 \]

Equation 16

\[ E_{\text{spherical void}} = 4\pi \left( \frac{3}{4\pi} \right)^{\frac{2}{3}} b^2 n^\frac{2}{3} \gamma \]

Equation 17

\[ E_{\text{loop}} = 2\pi r^* \frac{\mu b^2}{4\pi (1 - v)} \left( \ln \left( \frac{8r}{r_c} \right) - 1 \right) \]

Equation 18

\[ \text{Area} = \pi r^2 = n b^2 \]

Equation 19

\[ r = \sqrt{\frac{nb^2}{\pi}} \]

Equation 20

\[ r_c \sim b \]

Equation 21

\[ E_{\text{loop}} = \frac{2\mu b^3 n^\frac{1}{2}}{\pi^2 (1 - v)} \left( \ln \left( \frac{1}{n^2} \right) - 1 + \ln \left( \frac{8}{\pi} \right) \right) \]

Where \( r \) is the radius of a loop or spherical void, \( n \) is the number of vacancies in the void/loop, \( b \) is the Burgers vector, \( \mu \) is the shear modulus, \( v \) is the poisson ratio, \( r_c \) is the dislocation core minimum radius cut off (which we approximate with \( b \)), and \( \gamma \) is the surface energy. Using these equations and the
material properties for GaAs$_{0.65}$P$_{0.35}$, we can calculate the energy of a loop or spherical void for a given number of vacancies. Since the surface energy and shear modulus for GaAs$_{0.65}$P$_{0.35}$ is not well known, the values for GaAs and GaP are used as an approximation for GaAs$_x$P$_{1-x}$ using Vegards law. The material properties of GaAs are 3.17 J/m$^2$, 32GPa, 0.31 and 0.4nm for $\gamma$, $\mu$, $\nu$, and $b$ respectively. The material properties of GaP are 4 J/m$^2$, 39GPa, 0.31 and 0.385nm for $\gamma$, $\mu$, $\nu$, and $b$ respectively. The energy of a loop or void given $n$ vacancies can be calculated and from the total energy, voids are favored at small sizes $r < 9$nm, but loops are favored for larger clusters of vacancies due to a reduction in the surface energy term.

The absolute value of $r_{\text{critical}}$ for the sphere/loop transition is not exact as it depends highly on the surface energy and shear modulus, which are not well known. It is likely that voids form in the initial stage of GaAsP growth once a critical embryo of vacancies have clustered. These clusters act as sinks for near-by vacancies which then lead to void growth. Eventually the void reaches the critical size such that it transformed into a loop by forming into a disc geometry and then welding the two faces together. The above calculations are for equilibrium conditions in a strain free environment and without any other potentials, such as charge. These will all bias the rate at which voids/loops nucleate and the critical number of vacancies at which they transform. In general we can see from the functional form of the relation that loops are favored for large populations of vacancies. It is possible that spherical voids with $r < 10$nm are present at the interface, but are not readily observed. Spherical voids are efficient sinks for vacancies since the radius grows as $n^{1/3}$, meaning voids could absorb many vacancies before they reach the crystal surface or active device layers. The process of collapsing a spherical or disc shaped void of vacancies into a dislocation loop is shown schematically in Figure 44. The cross over between the energies
Figure 44 Schematic representation of the formation of a dislocation loop via the collapse of a vacancy disc cluster. In the initial stages, vacancies for clusters to reduce the system free energy. At large agglomerations, the vacancy disc collapses into a dislocation loop to reduce the surface free energy of the vacancy cluster. Reproduced from Hull [5]

defines regimes where loops or voids are more energetically favorable. To transform from a spherical void to a dislocation loop, the void needs to collapse into a disc shaped void, which is a higher energy structure due to the increased surface area. The energy penalty of a disc formation represents an activation energy barrier for transformation to dislocation loops. The prevalence of dislocation loops observed in PVTEM indicates that there is a strong driving force for the condensation of vacancies into loops and indicates that at the interface there is a high super saturation of vacancies in the initial stage of growth.

While both point defects of interstitial atoms and vacancies are present at the GaAs₁₋ₓPₓ/Si₁₋ₓGeₓ interface and could both potentially lead to dislocation loop condensation, we believe vacancies to be the primary suspect given the results of the strained GaAsP/SiGe study. Under a strain state of compression, vacancies are more thermodynamically favored; conversely under a strain state of tension vacancies are thermodynamically unfavorable [49]. Interstitial atoms exhibit an inverse relation to strain compared to vacancies. If an excess of vacancies were the source of point defect condensation into dislocation loops,
Figure 45 Schematic illustration of epitaxial structures used in this study. A. GaAsP/SiGe initiation conditions structure. B. Dislocation trapping structure. C. Interface strain study.

we would expect to see a reduction of loops and thereby threading dislocation density in a tensile strained interface and an increase for a compressively strained interface. This trend is readily observed in the strain study above.

Having identified point defect condensation into dislocation loops at the GaAsP/SiGe interface we developed two strategies to mitigate their effect on the TDD. The first approach, termed “loop trapping”, attempts to prevent the loops from expanding to the crystal surface with thin strained layers just above the GaAsP/SiGe interface. The dislocation trapping experiment consisted of thin 0.2% strained layers of GaAs$_{0.1}$P$_{0.9}$ grown slightly above the interface (15nm) by shifting the AsH$_3$/(AsH$_3$ + PH$_3$) flow ratio—increased AsH$_3$ flow for compressive layers and reduced AsH$_3$ for tensile layers. The group-V hydride flow ratio change for the strained layers corresponds to a 5% absolute As composition shift in the GaAs$_y$P$_{1-y}$ film locally. This is shown schematically in Figure 45B. The second approach, termed “loop suppression”, focuses on preventing loop formation by biasing the initial concentration of point defects at the heterointerface through thin strained layers at the heterointerface. The strain in the thin SiGe layer was achieved by changing the ratio of GeH$_4$/SiH$_4$+GeH$_4$) flow. The gas flow change corresponds to a 5% absolute composition shift in the either the GaAs$_x$P$_{1-x}$ or Si$_x$Ge$_{1-x}$ alloys in either the compressive or tensile direction. The approximate thickness of each strained is 10nm in all cases. The strain study epi-structures
are shown schematically in Figure 45B&C. All of these growths utilized the 3 second AsH\textsubscript{3} initiation condition as well.

The control, loop trapping and loop suppression samples were characterized in a similar manner as the previous GaAsP/SiGe samples. The TDD and surface roughness of the samples is summarized in Table 2.

Table 2 Summary of GaAsP/SiGe optimization data showing the starting material quality for a Si\textsubscript{0.3}Ge\textsubscript{0.65} exemplar and the effect of initiation treatments as well as the effect of loop trapping and loop suppression treatments.

3.8 Loop Trapping Experiments

XTEM of the loop trapping structure revealed multiple dislocation loops at the GaAsP/SiGe interface. Many of the loops have a height of 15 nm Figure 46, which corresponds to the thickness of the
lattice-matched layer under the strained zone, confirming that the loop was prevented from expanding by the strained zone. The loops observed in XTEM have flat features at the top, further indicating that the zone formed a barrier inhibiting the expansion of the loops. These loops were also visible in the PVTEM images of the sample and the dimensions matched with those seen through XTEM. However some of the loops observed at the interface had expanded to a height of 60nm Figure 47, suggesting that more strain and/or thickness would improve the film even further. The strained zone was partially effective in containing the loops at the interface as many were prevented from expanding and the threading dislocation density in the strained zone sample was slightly lower than the conventional lattice matched film sample (TDD_{loop trapping} = 3 \times 10^6 \text{ cm}^{-2} \text{ vs TDD}_{null} = 5 \times 10^6 \text{ cm}^{-2})$. Multiple cross section and plan-view TEM samples were made for this sample to study the dislocation loops, which were observed in each sample. The fact that they were observed in all of the TEM samples is significant and means that the loops are not a one-off feature, but representative of the wafer as a whole. Additionally, the density of loops observed
in PVTEM was on order mind-10^7 cm^-2, which is in the density that they should be readily observed in XTEM.

3.8.1 G.b Analysis of dislocation loops

We hypothesized that the source of the dislocation loops observed at the GaAsP/SiGe interface was due to vacancies accumulation and condensation. The TEM is a powerful tool for determining the nature of the dislocation loops as the contrast that results from various imaging conditions is sensitive to perturbations in the crystal lattice. Using G.b contrast analysis and inside-outside contrast analysis we can determine the nature of the dislocation loop. These techniques are based on the fact that the contrast in a TEM images is proportional to the dot product of the diffraction vector chosen and the perturbation to the lattice. In the case of dislocations, the perturbation is the Burger’s vector and the diffraction vector (g) is selected by tilting the sample into some orientation such that that diffraction condition is satisfied. Using selective area diffraction aperture we can select only the electrons that are being strongly diffracted
from that condition and block all others. This imaging condition is known as the two-beam condition.

Extensive details of diffraction analysis and TEM imaging can be found in the Transmission Electron Microscopy Handbook by Williams and Carter. Dislocation loops that form via the condensation of point defects can be imaged as a disc of vacancies or interstitials that are inserted into a crystal lattice. Along the boundary of that disc, the atoms reconstruct to form a dislocation loop around the disc while the faces of the point defect disc match the crystal structure. This is shown schematically in Figure 48. Depending on how the loop was formed, either by injecting a plane or removing a plane, the diffraction contrast when imaged under different +g vectors will change. This is the basis of how the character of a dislocation loop can be determined is the interaction of the g vector and the contrast of the loop.

Inside-outside contrast method was first described by Groves and Kelly and has had additions from Mazey et al[50] and Edmondson and Williamson[51]. The techniques were of great interest to study point defect condensation in irradiated materials found in nuclear reactor design. From their framework, analysis of dislocation loops formed in semiconducting materials has been performed to study the effect of doping, strain and temperature on grown in dislocations found in boules of Si, GaP and GaAs[52]–[54]. Under kinematical diffraction conditions, which the two-beam approximation applies, the contrast that results due to a dislocation loop lies either inside or outside of the actual loop position depending on the diffraction vector used and the nature of the loop (interstitial or vacancy) and the orientation of the loop with respect to the incident electron beam. If one can know the orientation of the dislocation loop, which can be determined through various tilting experiments, and the burgers vector of the loop, which can be obtained through g.b analysis, the character of the loop can be determined through how the contrast shifts from the inside to the outside of the projection of the loop.

Since the loop trapping sample prevented many of the loops from expanding, they were readily observable in TEM, which provided an ideal platform to study the nature of the dislocation loops that nucleated at the interface. It should be noted that dislocation loops were observed in multiple cross
Chapter 3 – Integration of GaAsP on Si

Figure 48 The effect of tilting sample on the image of the interstitial and vacancy loops. The dashed line shows the projection of the actual position of the loop; the full line show the position of the diffraction contrast image. When an extinction contour passes through the loops the apparent ellipticity changes are opposite senses for the two cases. Reproduced from [51]

section and plan view samples made from the loop trapping experiment sample. This further indicates that the loops are a global defect tends and not just specific to one particular region of the sample.

Diffraction contrast analysis of the dislocation loops was performed in the TEM using multiple zone-axis and diffraction conditions to determine the burger vector and type of loop. Performing diffraction studies on PVTEM samples of the as grown samples is difficult since the loops were confined near the GaAsP/SiGe interface, approximately 500nm below the surface. A timed wet etch (1:1:3 HCl:H₂O₂:H₂O) is used to remove the top 400nm of GaAsP film. The etch rate of this solution varies depending on the age of the H₂O₂, composition of the GaAsₓP₁₋ₓ film, temperature of the solution and age of the solution. Nominally
the etch rate is between 100nm/s – 140nm/s. Iterations between wet etching and surface profilometry performed on a masked region of the sample enabled accurate depth etching. Following the wet chemical thinning, PVTEM samples were made in the conventional manner. The samples were imaged under multiple diffraction conditions and along multiple zone axis to perform g,b contrast analysis and inside-outside contrast analysis.

Figure 49 PVTEM micrographs of dislocation loops imaged under various diffraction vectors. A.) along the 100 Zone Axis. The diffraction condition (g) is labeled for each image. The loops appear as circular dark regions while threading dislocation segments can be observed as lines with “zebra” contrast. Diffraction contrast analysis on the same area is used to establish the Burgers vector. B.) Zoomed in region of a dislocation loop viewed along the <111> zone axis showing the characteristic inside-outside contrast as the sign of g is inverted.
From g.b contrast experiments, we were able to determine that the loops have a burgers vector of the [011] type. The loop normal is assumed to be on the 111 plane since it is the low energy surface for vacancies to condense on and given the 2d projection of the loop when observed in the 100, 110, and 111 direction. Given n and b, we set out to determine the inside-outside contrast of various dislocation loops. The 100 and 111 zone-axis were chosen for the diffraction experiments Figure 49. From Figure 49b, we observe “outside” contrast when (g.b)s > 0 and “inside” contrast when (g.b)s < 0. From the loop analysis procedure set by Foll and Wilkins, this corresponds to vacancy-type dislocation loops.

The TEM diffraction contrast analysis confirms that the dislocation loops nucleated at the GaAsP/SiGe interface are due to the accumulation of vacancies. This proves our hypothesis based on the TDD increase in compressive strained samples and the lower vacancy formation energy for compressive strain. Having identified vacancies is the culprit for the loop nucleation, we set about to prevent their formation by biasing the GaAsP/SiGe interface with thin strained layers grown directly at the interface.

3.9 Loop Suppression

The loops suppression experiments investigate the effect of strain at the interface and its effect at biasing the concentration of point defects. The first set of experiments involved strained couples, tensile strained GaAsP/compressive strained SiGe (t-GaAsP/c-SiGe) and compressive strained GaAsP/tensile strained SiGe (c-GaAsP/t-SiGe). The complementary strain couple balances the strain between the two layers. The thickness of each strained layer is approximately 10 nm. The second set of experiments investigates the effect of strain only in the SiGe$_{1-x}$ surface (c-SiGe or t-SiGe). The effect of each strain treatment is assessed via PVTEM to count dislocation density, XTEM and AFM to determine surface roughness. The results of the PVTEM and AFM are summarized in Table 2. The unstrained 3 second AsH$_3$ initiation GaAsP/SiGe sample is used as a reference control to assess if the strain treatments improve
or degraded material quality. The reference unstrained sample with a 3sec AsH\textsubscript{3} initiation has a baseline TDD = 4.8x10\textsuperscript{6} cm\textsuperscript{-2}.

From the strained couple sample series we observe that the c-GaAsP/t-SiGe sample exhibited a lower RMS roughness and a reduction in TDD compared to the control, TDD = 3.5x10\textsuperscript{6} cm\textsuperscript{-2}, while the t-GaAsP/c-SiGe sample exhibited an increase in both RMS roughness and TDD with respect to the control, TDD = 1.9x10\textsuperscript{7} cm\textsuperscript{-2}. From the previous strained GaAsP study we saw that compressive strain in the GaAsP layer is not well tolerated, yet the c-GaAsP/t-SiGe sample exhibited the lowest TDD of the lot. It appears that the tensile strain in the SiGe surface is counteracting the negative effects of compressive strain in the GaAsP film. Conversely, compressive SiGe seems to be degrading the material quality, since tensile strained GaAsP was shown to not degrade material quality. We hypothesized that the strain in the SiGe cap layer biases the concentration of vacancies, increased for compressive strain and decreased for tensile strain. By suppressing the concentration with tensile strain, it limits the possibility of reaching a critical concentration level necessary for nucleating dislocation loops, hence the reduction in TDD despite having compressive strained GaAsP. The results of the strained couple experiments indicated that the SiGe layer strain state controls the loop nucleation. We performed a second set of experiments with a thin strained SiGe layer only with the hypothesis being a thin tensile strained SiGe cap should yield the best material quality and conversely the c-SiGe sample should degraded the material quality.

PVTEM of the SiGe strained only samples reveals a threading dislocation density of 1.2x10\textsuperscript{6} cm\textsuperscript{-2} and 1x10\textsuperscript{8} cm\textsuperscript{-2} for the tensile and compressive samples respectively. The material quality of the tensile SiGe capped sample was the best of the GaAsP/SiGe samples. The t-SiGe sample had a 4x reduction in TDD compared to the unstrained GaAsP/SiGe control sample. The TDD and surface roughness were comparable to the Si\textsubscript{0.35}Ge\textsubscript{0.65} exemplar sample, which indicates there is minimal defect nucleation at the GaAsP/SiGe interface. At this point improvements in the GaAsP material quality require improvements in the SiGe graded buffer defect density. We found that after performing a wet chemical etch on the MOCVD
shower head that the growth of SiGe graded buffers resulted in less of an increase in a lower TDD in the SiGe virtual substrate. This opens up the opportunity for producing GaAsP/SiGe with TDD < 1x10^6 cm^-2.

Further refinement of the GaAsP/SiGe initiation sequence: the AsH₃ initiation time, growth temperature and amount of strain in the SiGe cap, can all be further optimized to limit defect nucleation at the GaAsP/SiGe interface. Even without this future optimization, the material quality of the GaAsP has been reduced to 1x10^6 cm^-2, by nearly 2 orders of magnitude, putting it in the regime where dislocations should not limit device performance. A summary of all of the GaAsP initiation and strain samples is shown graphically in Figure 50.

Figure 50 Summary of the GaAsP/SiGe initiation experiments and progress. The optimal GaAsP growth condition involved a thin tensile strained SiGe cap and 3second AsH₃ initiation. Continued optimization could bring the density down to the 10^5 cm^-2 with the improved SiGe graded buffer growth following etching of the MOCVD showerhead.
3.10 GaAsP/SiGe growth optimization conclusions

Careful study of the GaAsP/Si$_{0.35}$Ge$_{0.65}$ interface enabled the elucidation of two defect nucleation mechanisms that lead to a 100x increase in TDD at the heterointerface. We showed that lattice matching is not enough of a criteria for the integration of GaAsP/SiGe—reactions at the surface must be accounted for. The reaction between P-Si has been known to degrade GaP/Si so it was not surprising that it degraded the growth of GaAsP/SiGe. We demonstrate that a 3 second exposure to AsH$_3$ prior to growth of GaAsP suppresses the Si-P reaction and improves the material quality dramatically. While great improvements were found with this short initiation sequence, it is possible that a shorter time is more optimal. Additionally the time necessary to passivate the surface might change for different GaAsP/SiGe compositions as well as for different substrate temperatures. Future optimization studies could look at this in more fine detail to help reduce the defect nucleation at the heterointerface even more. Secondly we showed that small amounts of compressive strain were particularly damaging at the GaAsP/SiGe interface due to the nucleation of dislocation loops. Vacancy condensation was shown to be the cause of the material degradation and dislocation nucleation. A finer optimization of the amount of strain at the interface (thickness of ε-SiGe layer and amount of ε) could be important parameters to tune for further reducing in TDD. Additionally the amount of strain will likely need to be tuned at different compositions and temperatures due to the formation energy of vacancies at those temperatures and the thermal activation barrier.

The demonstration of GaAsP films on Si with TDD = 1x10$^6$ cm$^2$ in an important milestone for the realization of high efficiency 1.7eV GaAsP/Si tandem solar cells. The material quality demonstrated by TEM analysis of the growths performed in this chapter provides a platform for solar cell demonstration.
4.1 – Introduction

In the previous chapter we investigated the GaAsP/SiGe interface and found that the surface coverage and initiation condition used is important for the growth of good quality III-V material. In this chapter we investigate the growth of GaAs/Ge and how As surface coverage affects defect density. The GaAs/Ge interface is important for solar applications as well as general integration of III-V materials on Si. While demonstrations of GaAs/Ge have been done previously in our group using atmospheric pressure MOCVD (AP-MOCVD), challenges exist in reduced pressure MOCVD. Our work helps unify previous experimental observations and define a clear process window for low defects density GaAs on Ge. From the knowledge gained through this study, successful growth of GaAs/Ge has been demonstrated in three MOCVD reactors—the 7x2” Aixtron MOCVD at MIT, an 8” Aixtron Crius MOCVD in the SMART labs at Singapore, and a commercial industrial reactor in the US. The reproducibility in multiple systems demonstrate that the findings are not reactor specific, but speak to the governing physics of the GaAs/Ge interface.

Despite many years and multiple theses devoted to the growth of GaAs/Ge, there is still a large amount of ambiguity around optimal growth of GaAs/Ge—even within the Fitzgerald Group. The growth of GaAs/Ge is an important interface to integrate III-V devices on Si, either through two-step Ge or SiGe graded buffer growth. Surprisingly, transferring the GaAs/Ge growth process developed for AP-MOCVD to reduced pressure MOCVD (100 torr) was a non-trivial task. Initial attempts produced GaAs films fraught
with pits, stacking faults and APBs. The breakthrough that enable growth of high-quality GaAs/Ge in the RP-MOCVD in the SEL at MIT came about through a collaboration with Kohen in the SMART LEES lab in Singapore. We found that that partial pressure of AsH₃, and ultimately the surface coverage of As, was the key process parameter that governed that defect density of GaAs films grown on Ge. Identifying As surface coverage enables us to unify the varying process window presented by the many authors who have investigated GaAs/Ge over the years. Having develop this frame work we demonstrate multiple experimental process parameter “handles” that can be altered to reach an ideal growth window.

4.3 Review of GaAs/Ge growth optimization

Integration of III-V materials on Si has been an active research area for the last 30 years. Consequently the problem of APB formation during zinc-blende growth on diamond cubic has been studied extensively by numerous authors, for many substrate and film combinations, and by multiple deposition techniques. The key findings of these studies is summarized below. Readers interested in specifics of the optimization of the GaAs/Ge interface are directed to read the work of Chen [55], Ting [28], and Groenert [56]. According to Li, APB-free GaAs/Ge can be achieved if the growth is “performed at a high V/III ratio, a relatively low growth rate, a reasonably high temperature and on a substrate a few degrees off (001) towards <110>” [57]. The effect of V/III ratio on GaAs/Ge film growth has been investigated heavily, with an inverse correlation between V/III ratio and APD density. While V/III is an important process parameter, it is not a purely independent variable. Changing the V/III ratio is accompanied with a change in the AsH₃ partial pressure in the system. This will lead to a change in the As surface coverage. Li reported that at pAsH₃ = 0.4mbarr, etch pit density was in excess of 10⁶ cm⁻². A minimum partial pressure of AsH₃ of 2mbarr was recommended by Li for APB free growth of GaAs/Ge. Beyond partial pressure, the growth window
Figure 51 XTEM of GaAs/Ge showing high density of ABPs nucleated at the interface. Some APBs terminate near the interface, but others propagate to the surface. The GaAs surface roughens considerably due to the APBs. Reproduced from Ting.

for GaAs/Ge has a narrow temperature window. Chen showed a narrow growth window (640°C – 680°C) for the optimal GaAs/Ge growth in AP-MOCVD [55]. Outside of this relatively narrow temperature regime, the defect density increased and solar cells performance suffered. Ting and Groenert studied GaAs/Ge growth in both MBE as well as MOCVD during their tenure with the Fitzgerald Group. Ting investigated the growth of GaAs/Ge in both MBE and AP-MOCVD and found that a growth temperature > 600°C was necessary for good quality growth of GaAs/Ge, as this represented the minimum thermal activation energy to reconstruct the Ge surface into a double-step structure. Groenert carried on the work of Ting and found that high growth temperatures (>675°C) and very high V/III ratios (>225) yielded the best material quality, but at temperatures >700°C, the Ge surface roughened and degraded the film quality. Using the optimized growth conditions (5min anneal at 700°C, V/III = 225, Tgrowth = 700°C) Groenert demonstrated stacking fault density <3x10^3 cm^2 by plan view TEM. From these AP-MOCVD growth conditions, similar growth conditions were applied to GaAs/Ge in reduced pressure MOCVD (P = 100 torr). The results of the growth transfer reveals defective growths with defect densities on order 10^6 cm^-2 – 10^7 cm^-2. Understanding the change in growth window that results in 1000x increase in defect density motivated this work.
4.4 Effect of AsH$_3$ partial pressure on GaAs/Ge nucleation

For this study we performed a series of GaAs/Ge growths under various AsH$_3$ partial pressures ranging from 0.99 torr – 5.17 torr. The growths are performed on n-type 2" (001) Ge wafers offcut 6° towards the <110> (purchased from AXT). The growths were performed under an N$_2$ carrier gas ambient. The reactor chamber is coated in GaAs prior to performing the GaAs/Ge epitaxy experiments. The epi-ready Ge wafer and a GaAs control wafer are loaded in the MOCVD reactor for each experiment. AsH$_3$ is flowed (200 sccm) while ramping to the growth temperature (650°C). The wafer is baked under AsH$_3$ for 5 minutes at 650°C, which enables time for double-step surface reconstruction. The surface of the Ge wafer is then exposed to some AsH$_3$ partial pressure for 5 seconds prior to and during the nucleation of GaAs. The partial pressure is determined by:

Equation 22

$$p_{AsH_3} = \frac{AsH_3\ Flow}{AsH_3\ Flow + Carrier\ Flow}$$

Where $p_{AsH_3}$ is the partial pressure of AsH$_3$, $p_{reactor}$ is the MOCVD reactor chamber pressure, AsH$_3$ flow is the flow of AsH$_3$ into the chamber and the carrier flow is the total flow of either N$_2$ or H$_2$ carrier gas into the chamber. The typical growth conditions used in our MOCVD reactor are $p_{reactor} = 100$ torr, AsH$_3$ flow = 100 – 300 sccm and carrier flow = 20,000sccm. The partial pressure of AsH$_3$ was changed by modifying either the AsH$_3$ flow, N2 carrier flow or total reactor pressure. A summary of the process parameters used and the respective AsH$_3$ partial pressure is given in Table 4.3. Sample A and Sample B investigate the effect of $p_{AsH_3}$ by increasing the AsH$_3$ flow. This is the most straightforward approach to altering the partial pressure of AsH$_3$, but it is limited by the maximum flows of the MFCs. After maxing out the AsH$_3$ MFC at 300 sccm, achieving higher partial pressures is done by either increasing the reactor
Table 4.3 Summary of GaAs/Ge nucleation partial pressure study experimental parameters

<table>
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<tr>
<th>Sample</th>
<th>Growth Temp (°C)</th>
<th>Growth Pressure (torr)</th>
<th>TMGa Flow (sccm)</th>
<th>AsH3 Flow (sccm)</th>
<th>N2 Carrier Flow (sccm)</th>
<th>AsH3 Partial Pressure (torr)</th>
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Figure 52 Nomarski micrograph showing the effect of AsH3 partial pressure during GaAs/Ge nucleation for Samples B – E.

pressure (Samples B – E) or by reducing the N2 carrier flow (Sample F). After the partial pressure treatment, an undoped GaAs film is nucleated at a high V/Ill ratio (336) and at a slow growth rate (0.12nm/s) for about 10nm of total film thickness. Doping at the GaAs/Ge interface lead to an increase in
pit density, but the 10nm undoped layer was found to suppress that problem. After the nucleation, the reactor is ramped back to the nominal bulk GaAs growth conditions ($p_{\text{reactor}} = 100$ torr, Flow$_{\text{AsH}_3} = 200$ sccm, Flow$_{\text{N}_2} = 20,000$ sccm). For the bulk GaAs film growth, the TMGa flow is increased to 50 sccm from the 10 sccm nucleation flow. This increases the growth rate to 0.6 nm/s. A p-n junction is grown on top of the nucleation layer to enable EBIC analysis to be performed on the samples. The p-n layers consisted of 300nm n-type GaAs followed by 100nm p+ GaAs. Following growth of the GaAs films, the samples are cooled under and AsH$_3$ over pressure to prevent surface roughening due to As desorption. Mesa isolation and ohmic contacts (Pt/Ti/Pt/Au p-type GaAs and Ti/Al n-type Ge) were made using convention e-beam evaporation and photolithography processes.

Figure 53 AFM showing the reduction in pit size and depth as AsH3 partial pressure is increased.

a.) Sample B ($p_{\text{reactor}} = 100$ torr).  b.) Sample E ($p_{\text{reactor}} = 350$ torr)
Chapter 4 – GaAs/Ge Interface Optimization

The surface morphology and pit density of the samples is characterized by Nomarski contrast optical microscopy. The samples with low AsH$_3$ partial pressure reveal a surface covered with pits in a high density ($>10^7$ cm$^{-2}$) for the lowest $p_{\text{AsH}_3}$ treatment (0.99 torr). In contrast, Sample E which had the highest partial pressure treatment ($p_{\text{AsH}_3} = 5.17$ torr) had a pit density of $2\times10^4$ cm$^{-2}$, nearly a 1000x reduction in defect density. Optical microscopy reveals a monotonically decreasing pit density for increasing $p_{\text{AsH}_3}$ treatments. AFM scans of the surface morphology reveal smooth surfaces with some step bunching across the surface. The defects observed in Nomarski are confirmed to be pits that are about 1µm wide and 40nm deep. Given the geometry of the AFM tip, it is possible the tip is bottoming out and not able to resolve the full depth and morphology of the pit structure. A representative AFM scan for Sample B along with profile plot is shown in Figure 53. As the AsH$_3$ partial pressure is increased, the density of pits observed in AFM decreases as does the width and depth of the pits. For Sample E ($p_{\text{AsH}_3} = 5.17$ torr) the pit width is about

Figure 54 TEM micrographs of GaAs/Ge Sample B ($p_{\text{reactor}} = 100$ torr, AsH$_3 = 300$ sccm). (a) APBs are observed in cross section nucleating at the GaAs/Ge interface. (b) PVTEM of a similar defect. (c) – (d) Pits in the Ge substrate formed during GaAs/Ge epitaxy.
350nm and the depth about 10nm. TEM is performed on the samples to identify the particular defect that is leading to the formation of the pits observed in nomarks and AFM Figure 54. APBs are observed forming at the GaAs/Ge interface for the low pAsH3 initiation (Sample B). The density observed in PVTEM is on order $10^7$ cm$^{-2}$, which corresponds well with the density observed in nomarski ($6 \times 10^6$ cm$^{-2}$). The discrepancy between the two densities can be due to the fact that in nomarski the pits have varying “strengths”—where some are sharp and well defined while others are smoother with less contrast. It is likely that nomarks undercounts the true density of APBs the formed at the interface. Additionally APBs and pits are observed punching down in to the Ge layer Figure 54 (c) & (d). Sharp faceted features like this have been observed during the growth of GaAs/Si and were explained by the Ga layer locally etching the Si. It is possible at with incomplete surface coverage of As, some of the Ga will react with the underlaying Ge layer in a similar fashion. In contrast to this, no defects were observed in either PVTEM or XTEM performed on the high pAsH3 Sample (E). The density of pits in this sample is too low to be detected in the very small amount of area sampled by TEM.

Given the low density of pits and defects we were investigating EBIC was employed to quantify the low density defects and determine if they were electrically active. In general, the IV curve of the samples with high density of pits appeared shunted—almost like a resistor. The samples with lower density of pits had a more diode like behavior to the IV curve. From the secondary electron (SE) and EBIC images there is a 1-to-1 correlation between the pits observed in SE and the dark spots observed in EBIC Figure 55. The pit density vs dark spot density observed in nomarks and EBIC correlate quite well. As mentioned with the correlation between nomarks and PVTEM, it is likely the sensitivity of detecting “strong” and “weak” pits is the cause of the discrepancy between nomarks and EBIC. The same monotonic decrease in dark spots observed in EBIC with increasing pAsH3 is observed.
Figure 55 (a) SE and EBIC image of Sample B, showing a high density of pits and electrically active defects. (b) Plot of pits counted in Nomarski vs dark spots observed in EBIC showing good correlation between the two techniques.
4.5 Ge surface coverage as a function of partial pressure

The partial pressure experiments demonstrate a clear trend for improved surface morphology and reduction in APB density with increased partial pressure of AsH₃ during the nucleation of GaAs on Ge. We hypothesized that the increased partial pressure leads to more complete coverage of the surface with As prior to growth of GaAs. The high As surface coverage suppresses nucleation of Ga-first GaAs domains which would lead to APBs or potentially surface etching. As mentioned in Chapter 3 regarding the As and P adsorption to a SiGe surface, we can model the surface coverage of As on Ge using the Langmuir adsorption. The rate at which surface sites fill is a function of the adsorption rate and the desorption rate.

Equation 23

\[
\frac{d\theta_{As}}{dt} = \alpha P_{AsH_3}(1 - \theta) - k_{dAs}(\theta)
\]

Where \(\theta\) is the fraction of sites filled with As, \(\alpha\) is a sticking coefficient, \(P_{AsH_3}\) is the partial pressure of AsH₃, and \(k_{dAs}\) is the desorption rate of As from Ge. The desorption rate is a thermally activated process that follows an Arrhenius behavior:

Equation 24

\[
k_{dAs} = v \exp\left(-\frac{E_{As}}{kT}\right)
\]

Where \(v\) is an attempt frequency, \(E_{As}\) is the desorption energy for As from a Ge surface, \(k\) is the Boltzman constant, and \(T\) the Ge surface temperature. The desorption kinetics of As from Ge surfaces has been studied by Berrie using single-photon ionization time-of-flight mass spectroscopy and found \(E_{As} = 1.2 \pm 0.4\text{eV}\) [58] and the time constant \(v_{As} = 7.8 \times 10^7 \text{s}^{-1}\). Langmuir adsorption equation consists of an
adsorption term based on the partial pressure and a desorption term that has an Arrhenius relation with temperature. During the partial pressure experiments the desorption rate was kept constant since all of the experiments were performed at the same temperature, but the adsorption term was ratcheted up with increasing AsH\textsubscript{3} partial pressure, which increased the equilibrium surface coverage. Using the process parameters from the partial pressure study we can calculate the As surface coverage prior to adding TMGa to the reactor chamber shown in Figure 56. For the samples with low $p_{\text{AsH}_3}$ exposure (<2.5 torr) at 650°C, the surface coverage is below 99%. The best quality GaAs/Ge films were grown with a $p_{\text{AsH}_3} = 5.17$ torr, which corresponds to 99.3% surface coverage. If surface coverage is the dominant factor determining the GaAs/Ge defect density, then fixing the partial pressure of AsH\textsubscript{3} and changing the substrate temperature should exhibit a similar trend where lower temperature leads to a decrease in desorption rate, therefore increased surface coverage for a given $p_{\text{AsH}_3}$—lowering the pit density. Conversely, increasing the temperature will increase the desorption rate and should lead to a higher density of pits.
Table 4 Summary of GaAs/Ge nucleation temperature study

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<th>Desorption Study</th>
<th>Growth Temp (°C)</th>
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</table>

Figure 57 GaAs/Ge nucleation temperature study Nomarski contrast images. The pit density increases with temperature for the samples.
To test this theory we repeated the growth of Sample D at different growth temperatures 600°C – 675°C. Sample D was chosen since it represented a mid-range partial pressure and mid range surface coverage. If the temperature improves or degrades the material quality it should be easily observable for this partial pressure. The growth temperature experimental parameters are summarized in Table 4. The growth temperature study samples exhibited similar morphology and structure in as the partial pressure study samples when observed in optical microscopy. The 675°C sample exhibited a high density of sharply defined pits, whereas the lower temperature samples had lower density of pits that were less severe. The 600°C sample As the substrate temperature is reduced from 675°C to 600°C the surface quality improves and the pit density is reduced Figure 57. The growth at 675°C has a sharp increase in defect density compared to the 3 other temperature samples (600°C, 625°C and 650°C). We speculate that at these elevated temperatures and high partial pressure of AsH₃, the Ge surface degrades due to etching. Chen observed that the growth window for GaAs/Ge was quite small—680°C was optimal while >700°C and <650°C were severely degraded. Furthermore, we performed PVTEM on the 675°C sample to determine the nature of the defects observed and potentially elucidate why there was such a high increase in pit density.

![Figure 58 PVTEM of the 675°C GaAs/Ge sample. Elongated pit like defects are present at similar density to pits observed on Nomarski.](image)
density compare to the other temperature study samples. A high density of elongated pit/APB like structures were observed in TEM of the sample. The size and aspect ratio of the defects differed greatly from those observed at 650°C: 500nm (675°C) vs 100nm (650°C). It is possible some second order process is activated at these temperature.

The activation energy is extracted by fitting a line to the defect density data when plotted as $\ln(p_{\text{pits}})$ vs $1/kT$. The slope of the curve will be equal to $-E_A$. If the high temperature point ($T = 675°C$) is removed from the fit, we find the activation energy $E_A = 1.4\text{eV}$. This is comparable to the activation energies listed in literature (1.2±0.4 eV). This demonstrates that the adsorption and ultimate the Ge surface coverage with As dominates the defect formation on Ge substrates—within a narrow temperature range of 650°C. Combined with the previous AsH$_3$ partial pressure study and the desorption temperature study, the results show that surface coverage of Ge with As prior to GaAs growth is necessary for suppressing APB formation.

![Figure 59](image)

Figure 59 Plot of natural log of defect density vs $1/kT$. The points corresponding to 600°C, 625°C and 650°C are fit to extract an activation energy of 1.35eV
4.5 GaAs/Ge Integration Conclusion

The partial pressure and temperature studies conducted in this chapter demonstrate the sensitivity of the III-V/IV interface to growth conditions. We find that a high surface coverage (>99%) is necessary for APB free nucleation of GaAs/Ge. We showed that the high surface coverage can be achieved in a variety of ways: increasing AsH₃ flow, reducing carrier flow, increasing reactor pressure, changing substrate temperature. The underlying physics of these growth control parameters is the adsorption and desorption rate. Using this understanding we have demonstrated these GaAs/Ge optimizations in three separate MOCVD reactors. Having multiple experimental “handles” for changing the partial pressure of AsH₃ is important as some most MOCVD reactors are limited in MFC maximum flow or operating pressure. The work presented here unifies the widely varying reported process conditions for GaAs/Ge growth. Successful demonstration of high quality APB free GaAs/Ge/Si has been realized on 150mm and 200mm wafers, enabling large area III-V/Si device integration.
Chapter 5
GaAsP Solar Cells on Si Substrates

5.1 Introduction

In the previous chapters we demonstrated methods to improve the material quality of GaAsP thin films grown on SiGe virtual substrates. This resulted in a low TDD of $1 \times 10^6 \, \text{cm}^{-2}$, nearly an order of magnitude improvement. Low TDD is an important result, but it is not the most important result. The true metric for successful integration of III-V materials on Si is the demonstration of working, high efficiency devices. In this chapter we present the performance of GaAs$_x$P$_{1-x}$ single junction solar cells grown on Si substrates. We will discuss the process optimizations made to improve cell quality from a growth and fabrication perspective. Multiple iterations of solar cells were grown for this study, they will be referred to by “Generation” to represent the learning and improvement made from these studies.

5.2 Overview of Solar Cell Device Structure and Operation

The band diagram for a typical p+/n homojunction solar cell in the dark and under illumination is shown in Figure 60. The p+/n nomenclature refers to a p+ doped emitter layer and a n-doped base layer with the cell being illuminated from the emitter side. Typically the emitter layer is doped more heavily and is thinner than the base region of a solar cell structure. In addition to the emitter and base regions,
window and back surface field (BSF) heterostructures are integrated into solar cell designs reduce recombination by to passivating dangling bonds on the surface and by “reflecting” minority carriers back towards the junction due to the band-offset or band-bending. Large bandgap materials are chosen for the heterostructures for two reasons: first to limit the amount of parasitic absorption in the window layer and to provide the band offset necessary for blocking minority carriers. The window layer and BSF layer materials should be lattice matched to the emitter and base to prevent the nucleation of defects at the interface. In the case of GaAsP solar cells, lattice matched alloys of AlInGaP and AlGaAsP are suitable candidates.

Solar cell device performance depends on its ability to absorb photons and utilize their energy. Photons with energy greater than the bandgap of the solar cell absorber material can excite electrons from the valence band into the conduction band. The rate of absorption is described by the Beer-Lambert Law:
Equation 5.25

\[ I = I_0 \exp(-\alpha t) \]

Where \( I_0 \) is the incident light intensity, \( \alpha \) is the absorption coefficient for the medium, \( I \) is the intensity of light after propagating through a thickness \( t \) of absorbing medium. The optical path length through a solar cell should be large enough to absorb most of the light. Indirect bandgap semiconductors such as Si have low absorption coefficients (on order \( 10^3 \) cm\(^{-1}\)) and therefore require thick solar cells to minimize transmission losses Figure 61. Surface texturing is used to minimize transmission losses by increasing the effective optical path length through light trapping. Even with good light trapping schemes, the minimum thickness for efficient Si cells is on order 50\( \mu \)m – 100\( \mu \)m. Direct bandgap semiconductors like GaAs require about 1 – 3\( \mu \)m of material due to their high absorption coefficient (> \( 10^4 \) cm\(^{-1}\)). Photons with energy less than the bandgap are not absorbed and this represents transmission losses for cell efficiency. One might
assume the optimal solar cell structure is one that has a very small bandgap to ensure absorption of the entire solar spectrum, but this leads to large thermalization losses which arise from photons with \( E > E_g \). High energy photons excite carriers high into the conduction band and valence band, but these rapidly thermalize back down to the band edge, losing the potential energy to heat. The optimal combination for a single junction solar cell involves choosing a bandgap that is small enough to ensure sufficient absorption of the solar spectrum, but not so low that thermalization losses dominate.

Under illumination electron/hole pairs are generated within the solar cell device. These carriers diffuse around within the solar cell structure—some towards the junction and some away from the junction. Those carriers that reach the junction are immediately swept across by the built in electric field after which they become majority carriers. Ideally the carriers that diffuse away from the junction will be reflected back by either the window layer or BSF layer. The current generated by illumination \( (J_{light}) \) represents the current of electrons in the emitter layer \( (J_n) \), holes in the base layer \( (J_p) \) and the carriers generated in the depletion region \( (J_d) \). The illumination generated current flows in the opposite direction of conventional diode current under an applied bias:

Equation 5.26

\[
J = J_{dark}(V) - J_{light}
\]

Where \( J \) is the total current, \( J_{dark}(V) \) is the current of a diode in the dark with applied bias \( V \). To first order the dark current of a diode under bias follows the Shockley diode equation:

Equation 5.27

\[
J_{dark} = J_0 \exp \left( -\frac{V}{n k T} \right)
\]

Where \( J_0 \) is the reverse bias saturation current, \( n \) is the diode ideality, \( k \) the Boltzmann constant and \( T \) the temperature of the diode. To extract any usable energy from a solar cell it must be connected to a load. The current through the load is \( J \) and the voltage across the load is equal to the voltage across
the junction. From these sets of equations we can see that the highest current results from when \( J_{\text{dark}} = 0 \) (ie \( V = 0 \)). This is known as the short circuit current density \( (J_{\text{sc}}) \). While this produces the highest current, the available power out of the cell is zero since the voltage is zero. Similarly, the highest cell voltage is achieved when \( J_{\text{dark}} = J_{\text{light}}, \) (ie \( J = 0 \)). This is known as the open circuit voltage \( (V_{\text{oc}}) \). One can apply various loads to a solar cell under illumination and measure the current and voltage to plot its performance. In reality this is done by applying a voltage to the cell and measuring its current under illumination. The product of voltage and current for a given operating point gives the power that can be extracted from the solar cell. From the illuminated \( JV \) curve we can see key metrics for cell performance: \( V_{\text{oc}}, J_{\text{sc}}, \) fill factor \( (FF) \), max power point \( (MPP), J_{\text{mp}}, V_{\text{mp}}. \)

The basic structure of solar cell is a semiconductor p-n junction. The difference in doping density and type creates a strong built in electric field. This electric field will be used to sweep out minority carriers. Carriers generated within the depletion region are immediately swept out by the electric field.

![Graph of solar cell IV measurements](image)

**Figure 62** Schematic plot of solar cell IV measurements conducted under illumination. The maximum amount of power that can be extracted from a solar cell under illumination is the max power point. An ideal solar cell has a high \( I_{\text{sc}}, V_{\text{oc}} \) and the shape of the curve should be as square as possible to enable the most power extraction possible.
Carriers generated in the quasi-neutral region must diffuse to the junction and are then swept out. There is a characteristic time scale for recombination of the electron hole pairs. Defects within the solar cell material are efficient non-radiative recombination centers. Carriers generated within a diffusion length of an electrically active defect will recombine and the energy stored in the excited electrons is lost to heat. This represents an efficiency loss. Approaching the theoretical efficiency limit of a solar cell made from a particular material is highly dependent on the quality of the material.

5.3 Review of GaAs\textsubscript{x}P\textsubscript{1-x} solar cell literature

GaAsP solar cell research started in the 1980’s with the preliminary work being done by Vernon[59], Fraas[60], Negley [61] and Wanlass [62]. They represented both industry (Chevron, Spire, AstroPower) as well as government funded research (NREL & SERI). The research conducted by these authors was motivated by the potential boost in efficiency granted from cascading a high bandgap solar cell with a Si solar cell[60],[63]. The initial demonstrations of GaAsP solar cells used III-V substrates such at GaP or GaAs. Despite the larger lattice mismatch (nearly 3% strain for 1.7eV GaAsP), GaP was attractive since it had a large bandgap making it transparent to photons not absorbed in the GaAsP cell. This made it amenable for mechanical stacking or bonding to a Si cell. Additionally, compressive grading of GaAsP does not suffer from “facet trenches”, a defect that results from the splitting of partial dislocations during tensile grading [64]. The quality of the cells demonstrated on these III-V substrates varied greatly depending on the growth conditions used, specifically the graded buffer process conditions implemented. Temperature, grade rate, grading material system (\text{In},\text{Ga},\text{P} vs \text{Ga},\text{As},\text{P}) and grade type (compressive vs tensile) are all important parameters [25],[65]–[67]. The most successful GaAs\textsubscript{x}P\textsubscript{1-x} cells reported involved a 14um graded buffer from GaAs to GaAs\textsubscript{0.8}P\textsubscript{0.2} done by Vernon at Spire Corp [59]. With an anti-reflection coating, efficiencies of 17% were demonstrated for GaAs\textsubscript{x}P\textsubscript{1-x} single junction solar cells with $E_g = 1.6eV$ –
1.8eV. While the initial demonstrations were promising and provided a high enough efficiency to enable GaAsP/Si tandem cells with efficiency greater than Si cells alone, the cost of producing GaAs<sub>x</sub>P<sub>1-x</sub> cells on III-V substrates and the cost of III-V graded buffers used prevented their adoption. Research of GaAs<sub>x</sub>P<sub>1-x</sub> solar cells picked up again in the 1990's and 2000's as groups such as the Ringel Group at The Ohio State University [16], [17], [68], the Lee Group at Yale University [25], [66], [67] and the Opila Group at University of New South Wales[69] focused on integration on Si substrates. Unfortunately the material quality of GaAs<sub>x</sub>P<sub>1-x</sub> cells grown on Si, either via GaAsP/GaP/Si or GaAsP/SiGe/Si has suffered from dislocation nucleation at the III-V/IV interface. Prior to the work done for this thesis, the best demonstrated GaAs<sub>x</sub>P<sub>1-x</sub> cells on Si had TTD > 10<sup>7</sup> cm<sup>-2</sup>.

The GaAsP solar cell design used in literature reports is very similar across the board. A typical solar cell has an In<sub>1</sub>Ga<sub>1</sub>P back surface field layer, 1µm GaAs<sub>x</sub>P<sub>1-x</sub> base doped to 10<sup>17</sup> cm<sup>-3</sup>, 100 nm – 300 nm emitter layer doped 10<sup>18</sup> cm<sup>-3</sup>, and a 50 nm In<sub>1</sub>Ga<sub>1</sub>P window layer. A schematic of a typical GaAsP solar cell structure used in literature and used for this study is shown in Figure 63. Both p+/n and n+/p architectures have been demonstrated in literature. In general, n+/p is preferred given the higher mobility of electrons which are the minority carriers for the base material. It is expected that they will more easily be able to diffuse to the junction over a long distance given their mobility. The cell design we focused on in this study is the p+/n to simplify the growth process. As shown in Chapter 3, considerable cross doping occurs at the III-V/IV interface, leading to a large diffusion of Si and Ge into the GaAs<sub>x</sub>P<sub>1-x</sub> layer and As and P into the Si<sub>y</sub>Ge<sub>1-y</sub> layer. All of these species are n-type dopants. By choosing the p+/n architecture we can eliminate the possibility of an unintentional junction being in our cell structure. While representative of GaAsP solar cells demonstrated in literature, this is not a perfect solar cell design. There are some transmission losses, especially near the band edge, from the limited cell thickness. To absorb all of the photons with E > E<sub>g</sub> the GaAs<sub>x</sub>P<sub>1-x</sub> cell would need to be >2µm thick. Additionally the InGaP window layer contributes losses due to photon absorption in the 50nm thickness. Despite these this cell design provides
a good first order structure for investigating the effect of material quality on cell performance. Given our materials optimization for the growth of GaAsP/SiGe provided GaAsP thin films with TDD almost 10x lower than those demonstrated in literature, we sought to determine how the quality would affect cells performance. From this starting point, we can characterize the cell performance and materials properties to enable modeling for future cell optimization.

Solar cell performance is typically gauged by device metrics such as short-circuit current density ($J_{sc}$), open circuit voltage ($V_{oc}$), fill factor (FF), and efficiency ($\eta$). Typically solar cells have a fixed band gap for the materials of interest, for example Si or GaAs. GaAs$_x$P$_{1-x}$ solar cells in literature have varying compositions and therefore varying bandgaps, typically between 1.85eV – 1.6eV. Different bandgaps will
produce different $V_{oc}$, and $J_{sc}$ under AM1.5 conditions. The Schockley-Quessar efficiency limit predicts a theoretical efficiency for a solar cell under a particular illumination given a particular bandgap\[1\], Figure 64. The actual efficiency of a solar cell is less than the calculated SQ limit, but the fraction of the SQ limit can be indicative of the overall material quality and cell performance. The best performing single junction solar cells demonstrated in lab, a thin film GaAs single junction cell by NREL in 2014, achieved an efficiency of 28.8% which is 86% of the SQ limit. Typical production Si solar cells have efficiencies on order 18% - 22%, which translates to 54% - 64% of the SQ limit. These industry metrics provide brackets for what sort of efficiency good quality solar cells should achieve. Reaching high efficiencies requires high material quality. The $V_{oc}$ is strongly affected by non-radiative recombination within the solar cell. For an ideal diode, the open circuit voltage is:

Figure 64 a.) Solar irradiance spectrum for space (AM0) and terrestrial applications (AM1.5 D & G). The dips in the solar irradiance correspond to absorption from the atmosphere—mainly water b). calculated SQ-limit efficiency for a single junction solar cell as a function of its band gap and AM1.5 irradiance.
Equation 28

\[ V_{OC} = \frac{k_b T}{q} \ln \left( \frac{J_{\text{photon}}}{J_{\text{dark}}} + 1 \right) \]

Where \( k_b \) is the Boltzmann constant, \( T \) is temperature in K, \( q \) is charge of an electron, \( J_{\text{photon}} \) is the photogenerated current and \( J_{\text{dark}} \) is the reverse bias saturation current density of the diode. Increased defect density reduces \( V_{oc} \) in two ways: first increased TDD leads to a larger dark current and second recombination at non-radiative defects limits the photogenerated current. From this relation we can see that to first order higher \( V_{oc} \) is associated with better material quality for a solar cell. For solar cells with only one bandgap, \( V_{oc} \) can be directly compared to determine the quality of a solar cell. But the varied bandgap of ternary GaAs\(_x\)P-x alloys does not allow for this comparison. We can use the bandgap-voltage offset \( (W_{oc}) \) figure of merit to normalize the performance of solar cells with differing bandgaps:

![Graph showing relationship between band gap and Voc](image)

Figure 65 Experimental Voc for a wide range of single-junction solar cell band gaps, from 0.67 to 2.1 eV, showing that the band gap–voltage offset, \( W_{oc}=(E_g/q) - V_{oc} \), is roughly constant over this range experimentally. The band gap–voltage offset \( W_{oc} \) is calculated for a semiconductor layer with radiative recombination only, and using the detailed balance model, also showing the approximate constancy of \( W_{oc} \) as predicted from theory. The measured band gap–voltage offset for some solar cell materials approaches the calculated value for radiative recombination only. Reproduced from King et al [83]
Equation 29

\[ W_{oc} = \frac{E_g}{q} - V_{oc} \]

Where \( E_g \) is the bandgap of the solar cell, \( q \) the charge of an electron and \( V_{oc} \) is the open circuit voltage of the solar cell under illumination. The semi-empirical limit for the \( W_{oc} \) figure of merit is 0.4V for most solar cells as it is weakly dependent on \( E_g \). From Figure 65 we see that the \( W_{oc} \) metric both theoretical and empirical demonstrations only varies by about 20% over the bandgap space of 0.67eV – 2.1eV for optimized low defect density solar cells. For the bandgaps of interest of GaAs\(_x\)P\(_{1-x}\), the \( W_{oc} \) calculated by assuming only radiative recombination and for the detail balance limit varies only by a few percent. This means that we can use \( W_{oc} \) for various GaAs\(_x\)P\(_{1-x}\) cells published in literature and \( W_{oc} \) for our own GaAs\(_x\)P\(_{1-x}\) cells to compare how the material quality affects the cell performance. From the chart of TDD vs \( W_{oc} \) (Figure 66), we see that there is a strong correlation of \( W_{oc} \) with TDD, which is expected. We also see that

![Image of chart showing correlation between TDD and \( W_{oc} \)]

Figure 66 \( W_{oc} \) as a function of TDD for various single junction GaAsP solar cells grown on either III-V or Si substrates published in literature. Additionally the solar cells grown in this work are shown with solid red circles. [21], [25], [43], [59], [60], [62], [63], [66], [84]–[86]
Figure 67 2-terminal tandem III-V/Si solar cell efficiency calculations based on the top cell $E_g$ and the efficiency of the top cell as a function of the SQ limit. Adapted from Buonassisi project work for Bay Area Photovoltaic Consortium (BAPVC). The dashed line represents the minimum 2T tandem efficiency requirements for multijunction solar given the expected improved performance of Si solar cells.

cells grown on Si suffer nearly 10x – 100x higher TDD than comparable cells grown on III-V substrates as well as almost a 100 meV increase in $W_{oc}$ compared to the best cells demonstrated on III-V substrates.

The goal of this work is to demonstrate that GaAsP cells grown on Si can have comparable performance as those cells grown on expensive III-V substrates. The key metrics for success will be the demonstration of a 1.7eV GaAs$_x$P$_{1-x}$ solar cell with $TDD = 10^6$ cm$^{-2}$ and an efficiency such that if it was coupled to Si, the tandem system efficiency would be >25%. Since current production Si cells can achieve efficiencies of 22%, any practical tandem cell must be better than Si both today and in the future. Therefore we choose the 25% as a minimum tandem efficiency target for our GaAsP cells Figure 67. The required efficiency of a single junction GaAsP top cell to add any benefit to a high quality crystalline Si solar cell is >15%. The work presented in this chapter focuses on improving the efficiency of single junction GaAsP cells grown on Si to demonstrate the materials quality is sufficient to warrant their integration with
Si solar cells. We investigate the growth conditions and processing parameters necessary for making high efficiency GaAsP solar cells. While the SiGe graded buffer is too opaque to allow the Si substrate to be used as a solar cell, the single junction GaAsP cells grown on the SiGe/Si serve as a proof of concept and a platform for additional cell architecture optimization.

5.3 GaAsP solar cell growth and fabrication

The growth of the GaAs_{1-x}P_{1-x} solar cells on Si substrates can be divided into three main parts: metamorphic growth of the Si_{1-y}Ge_{y} composition graded buffer, nucleation of lattice matched GaAs_{1-x}P_{1-x}, and growth of the GaAs_{1-x}P_{1-x} solar cell. Details of the growth and preparation of the Si_{1-y}Ge_{y} substrates and the subsequent growth of GaAs_{1-x}P_{1-x} on Si_{1-y}Ge_{y} substrates is given in Chapter 3. The epitaxial growth of GaAs_{0.75}P_{0.24} solar cells on Si_{0.25}Ge_{0.75} substrates is performed in an Aixtron close-coupled showerhead metal-organic chemical vapor deposition (MOCVD) reactor. Arsine (AsH₃), phosphine (PH₃), trimethylgallium (TMGa), and trimethylindium (TMIn) are the precursors used for the growth of GaAs_{1-x}P_{1-x} and InₓGa_{1-x}P. Dimethylzinc (DMZn) and disilane (Si₂H₆) are used as p-type and n-type dopants respectively during growth of the III-V layers.

Following the growth of the Si_{0.25}Ge_{0.75} buffer capped with a thin 10nm tensile strained Si_{0.30}Ge_{0.70}, the temperature is then lowered to 725°C for the GaAs_{1-x}P_{1-x} nucleation layer. A short (3 second) pulse of AsH₃ is introduced to the chamber prior to the growth of GaAs_{1-x}P_{1-x} to saturate the Si_{0.25}Ge_{0.75} surface sites and suppress deleterious reactions between PH₃ and Si in the Si_{0.25}Ge_{0.75} substrate [70]. Immediately following the AsH₃ initiation, lattice matched GaAs_{1-x}P_{1-x} is grown by simultaneously introducing TMGa, AsH₃ and PH₃ into the reactor. The GaAs_{1-x}P_{1-x} films are grown with a V/III ratio of 100 and at a growth rate of about 0.6 nm/s. The GaAs_{1-x}P_{1-x} buffer layer is n-type doped to 2x10¹⁸ cm⁻³. After the growth of the buffer layer, the temperature is ramped to 650°C under an over pressure of AsH₃ and PH₃ for the growth of the
GaAs$_{0.76}$P$_{0.24}$ solar cell. Ramping the temperature from 725°C to 650°C is an important process parameter, as the InGaP/GaAsP interface is highly defective when initiated at high temperatures (725°C). Experiments and details of the InGaP/GaAsP interface optimization will be given in a later section.

The solar cell consists of a 50 nm In$_{0.36}$Ga$_{0.64}$P:Si ($N_A = 1 \times 10^{18}$ cm$^{-3}$) back surface field, 1 μm n-type GaAs$_{0.76}$P$_{0.24}$:Si ($N_A = 1 \times 10^{17}$ cm$^{-3}$) base, a 200 nm GaAs$_{0.76}$P$_{0.24}$:Zn ($N_D = 2 \times 10^{18}$ cm$^{-3}$) emitter, a 50 nm In$_{0.36}$Ga$_{0.64}$P:Zn ($N_D = 2 \times 10^{18}$ cm$^{-3}$) window layer, and a highly doped 100 nm p+ GaAs$_{0.76}$P$_{0.24}$:Zn ($N_D = 1 \times 10^{19}$ cm$^{-3}$) contact layer. The doping and layer thicknesses used in this solar cell structure were deliberately chosen to closely match GaAs$_x$P$_{1-x}$ single junction cells reported in literature so that the results will be directly comparable. A schematic of the solar cell structure and representative TEM cross section of the solar cell structure are shown in Figure 63.

Three “generations” of GaAsP solar cells were grown and fabricated. The general solar cell structure and nominal composition for the cells remained the same for each generation. Growth optimizations were performed with each generation. The Gen1 GaAsP solar cells were grown at 725°C, which resulted in defects nucleating at the InGaP/GaAsP interface. The Gen2 solar cells were grown at 650°C, based on the InGaP/GaAsP growth optimization study. Gen2 had a marked improvement in cell performance over Gen1, but still suffered from some lattice mismatch of the cell with respect to the underlying buffer layer. Careful growth calibrations were performed to better lattice match the GaAs$_x$P$_{1-x}$ cell to the buffer layer for the Gen3 cells. This along with thinning of the InGaP window layer resulted in marked improvement of cell performance.

We fabricated 1 mm x 1 mm, 2 mm x 2 mm, and 4 mm x 4 mm solar cells via standard photolithography and wet-chemical etching processes. An image of a typical 1mm x 1mm cell is shown in Figure 68. Details of the process flow and mask design can be found in the process flow appendix A. The front side Pt/Ti/Pt/Au p-type contacts and backside Ti/Al n-type Si$_{0.35}$Ge$_{0.65}$ contacts were deposited by e-
Figure 68 Nomarski optical micrograph of a fabricated 1mm x 1mm GaAsP single junction solar cell grown on Si. The gold metal lines provide contact while the mesa etch provides isolation from the other cells on the wafer. The cell surface shows characteristic cross-hatch texturing from the SiGe graded buffer growth.

beam evaporation. The front side metal also serves as an etch mask for the removal of the highly doped GaAsP contact layer which would incur shading losses.

Post-growth analysis of epitaxial interface quality and layer thicknesses was done by cross section transmission electron microscopy (XTEM) and film defect density was measured using plan-view TEM (PVTEM). Electron beam induced current (EBIC) imaging is also used to quantify solar cell defect density. Composition and strain of epitaxial layers was characterized using high resolution x-ray diffraction (HRXRD). Photoluminescence (PL) spectroscopy was performed using a 150 mW continuous-wave argon ion laser with emission at 514.5 nm. The bandgap of the solar cell and qualitative material quality were determined by PL. The fabricated solar cells are tested using a Newport Oriel 91194 solar simulator with a 1300 W Xe-lamp, an AM1.5G filter, and a Newport Oriel 68951 flux controller. Si reference cells are used to calibrate the photon flux and irradiance. Reflectance is measured using a Perkin Elmer Lambda 950 UV-
VIS-NIR Spectrophotometer. Other electrical characterization of the solar cells (dark IV and TLM) was performed on a semiconductor parameter analyzer probe station.

### 5.4 Gen0 and Gen1 GaAsP solar cells

The first generation of GaAsP single junction solar cells were based on the process developed by Sharma for GaAsP/Si tandem cells[30]. Sharma had successfully grown a GaAs$_0.71$P$_{0.29}$ cell on a Si cell through the use of a Si$_{0.35}$Ge$_{0.65}$ graded buffer, GaAsP graded buffer and a GaAsP tunnel junction. TEM of the cell revealed a low $10^6$ cm$^{-2}$ TDD, which was promising, but the electrical performance of the cells were poor. The cells had a $J_{sc} = 1.7mA/cm^2$, $V_{oc} = 1.22V$, $FF = 29\%$ and $\eta = 0.6\%$ Figure 69. The relatively high $V_{oc}$ given that almost no light is reaching the Si cell is indicative of good GaAsP material quality, but the poor $J_{sc}$ and $FF$ are due to severe shading losses. The Si$_{1-y}$Ge$_y$ graded buffer absorbs nearly 80% of the photons intended for the Si solar cell Figure 70. These initial cells, termed Gen0, did not incorporate a window layer or InGaP back surface field layer. The lack luster performance of the tandem cells motivated investigation of single junction GaAsP cells on Si substrates as a proving ground since the absorption due to the Si$_{1-y}$Ge$_y$ graded buffer was unavoidable.
The Gen1 solar cells used the process developed by Sharma to investigate single junction GaAsP cells grown on SiGe, which included nucleating the GaAsP layer under N2 carrier gas at 725°C, then ramping the temperature to 650°C and switching to H2 carrier gas for the growth of the cell. The 725°C N2 nucleation of GaAsP was used since that is the optimized growth conditions developed in Chapter 3. The growth at 650°C under H2 was chosen for two reasons, first the growth rate is nearly double under H2
Figure 70 The SiGe graded buffer leads to considerable absorption losses for a buried Si cell. a.) The available photon irradiance is shown in blue and the green curve represents what light is available for a Si cell after passing through a Si→Si0.35Ge0.65 graded buffer grown under standard grading rates (10%Ge/µm). Nearly 80% of the available energy is lost. b.) EQE measurements of a Si solar cell showing the shading effect of either a thick Si buffer or thick SiGe graded buffer layer.

and secondly the Zn doping was optimized for this temperature to get reasonable doping levels. Two sets of solar cells were growth for the Gen1 series: the first (Gen1-A) used the same N2/H2 GaAsP switching procedure developed by Sharma and the second (Gen1-B) grew the entire solar cell at 725°C under N2 without any temperature or carrier gas switches.

Characterization of the Gen1-A solar cells (XRD and TEM) revealed the GaAsP films had considerable mismatch between the layers (~10% composition) that resulted in dislocation nucleation and glide at the interfaces. The incorporation of As and P into the GaAsP film changes both with temperature due to cracking efficiency of AsH3 and PH3 and with carrier gas (H2 vs N2) due to changing boundary layer thickness. This shift lead to a large mismatch in the composition between the 725°C N2 GaAsP nucleation layer and the 650°C H2 GaAsP Cell layers. The misfit dislocation segments are readily observed in XTEM and PVTEM of the Gen1-A cell Figure 71. PVTEM and EBIC both reveal a high density of misfit segments and TDD = 3x10⁷ cm², indicating nucleation of defects at the GaAsP/GaAsP or InGaP/GaAsP interface since
Figure 71 Lattice mismatch between the H2/N2 GaAsP layers resulted in dislocation glide. a.) XTEM of single junction GaAsP cell showing dislocations at GaAsP/GaAsP (H2/N2) interface and InGaP BSF/GaAsP interface. b.) PVTEM showed $3 \times 10^7 \text{ cm}^{-2}$ threading dislocation density in addition to misfit dilocation segments being overserved in the cell. c.) EBIC image of the cells showing highly defective film (TDD > $10^7 \text{ cm}^{-2}$) and high density of misfit segments.

the GaAsP/SiGe interface appears clean and free of defects in XTEM. These defects limited the cell performance.

The Gen1-B cells simplified the growth process by removing temperature and carrier gas switches, therefore there shouldn’t be any lattice mismatch between the various layers of the solar cell. The cells were nucleated at 725°C under N2 following the optimized growth procedures developed earlier. XRD of the solar cell shows only one peak at the lattice constant corresponding to GaAs$_{0.77}$P$_{0.23}$. A satellite peak is observed in the 004 RSM which is attributed to highly phase separated InGaP in the window layer of the cell Figure 73. Growing the entire cell at one temperature alleviated the defect nucleation due to lattice mismatch, but the InGaP/GaAsP interface became highly defective at the increased growth temperature. While the InGaP/GaAsP interface was fine when grown at 650°C in the previous Gen1-A cells, it appears highly defective when grown at 725°C. The InGaP/GaAsP interface quality is paramount to high performance solar cells. In the next section we performed a series of experiments to investigate the optimal switching conditions necessary for high quality GaAsP/InGaP growth.
Figure 72 HR-XRD RSM about the 004 reflection of the Gen1-A GaAsP solar cell grown on Si. The 650°C H2 GaAsP cell peak is mismatched from the buffer by nearly 0.3% lattice mismatch.

Figure 73 Growing the entire Gen1-B at one temperature (725°C N₂) lead to a high degree of lattice matching between the layers. B.) HR-XRD 004 RSM of the GaAsP/SiGe cell showing one peak near the GaAs₀.₇₇P₀.₂₃ lattice constant. The satellite peak observed is due to highly phase separated InGaP. B.) XTEM (g=220) of the Gen1-B solar cell. GaAsP/SiGe interface is smooth and free of defects, but the InGaP layers are defective. The InGaP window layer is highly defective and filled with phase separation, stacking faults and dislocations.
5.5 Optimization of the InGaP/GaAsP interface

The Gen1 GaAs$_{1-x}$P$_x$ solar cells suffered from defects nucleated at the InGaP/GaAsP interface. We performed a series of growth experiments to investigate the effect of growth temperature and initiation condition used for the growth and switching between InGaP and GaAsP. Mukherjee observed that switching from InGaAs to AlInP or InGaP worked well at 650°C, but at high temperature the interface degraded [71]. We investigated the effect of temperature on switching between the growth of InGaP and GaAsP. Additionally, we investigated the growth of InGaP at high temperature as a means to suppress ordering within the InGaP layer which lowers the bandgap. Reduced bandgap is non-ideal for window layer applications as it leads to increased absorption [72].

The test structure initiated nominally lattice matched In$_{0.35}$Ga$_{0.65}$As$_{0.74}$P$_{0.26}$ at 650°C, grew about 200nm, then ramped the temperature to 725°C while continuing to grow InGaP. This high temperature region would enable us to study the extent of ordering in TEM and observe the transition from ordered to disordered. Following the growth of InGaP at 725°C, an additional 200nm, the growth switches back to lattice matched GaAsP to grow 500nm before switching to InGaP at high temperature (725°C). The epi-structure is shown schematically in Figure 74a. Following growth, the samples are characterized with XTEM to investigate the interface quality as a function of growth temperature. Additionally, the selected area diffraction (SAD) pattern of the InGaP grown at various temperature is recorded to assess the degree of ordering based on the presence of super spots. XRD and PL are used to assess the material composition and degree of bandgap reduction.

From the XTEM it is quite apparent that the 650°C initiation of InGaP on GaAsP is of much better quality than the 725°C interface. The 725°C initiated InGaP exhibits a high density of defects and phase separation, whereas 650°C InGaP has no observable defects at the interface. The “speckle” contrast observed in the InGaP layers is due to fine scale In segregation, and is typical for growth in In-containing
Figure 74 InGaP/GaAsP Growth temperature optimization study. a.) Schematic of epi-stack, target thickness and growth temperatures. b.) XTEM image of InGaP/GaAsP. InGaP initiated at 725°C leads to high density of dislocations and defects nucleated in the InGaP layer while 650°C appears to be good quality. The inset shows the selected area electron diffraction patterns for the InGaP grown at 650°C and 725°C. The appearance of super-spots in the 650°C sample is indicative of ordering. The high temperature growth disorders the InGaP.

materials. The temperature ramp experiments demonstrates that there is no innate property of $\text{In}_{0.36}\text{Ga}_{0.54}\text{P}$ that prevents its growth at 725°C, it is solely an issue with the heterointerface which is sensitive. Being able to grow InGaP at high temperatures is important for preventing ordering as the observed bandgap reduction for this composition is about 140meV. This reduction in bandgap can affect the amount of light that is converted to electrical energy in a solar cell, as photons are absorbed in the window layer rather than in the body of the solar cell. An ideal InGaP window layer would be nucleated at 650°C and then grown to the desired thickness at a high temperature to suppress the ordering.

It is possible that small degrees of lattice mismatch between the nominally lattice matched layers, intermixing between the As and P species, and phase separation between In and Ga lead to an accumulation of local pockets of strain at the interface. At elevated temperatures the activation barrier for diffusion is reduced as well as the activation barrier for nucleating defects. This leads to additional intermixing and nucleation of dislocations and other crystallographic defects which degrade the film. We
speculate that the improved InGaP/GaAsP interface quality achieved at reduced temperatures is due to reduction of intermixing, less As being incorporated into the InGaP film, and a reduction in the thermal energy for activating defects nucleation. The low temperature switching between InGaP/GaAsP at 650°C under N₂ carrier gas is implemented for all of the following solar cell growth structures.

5.6 Regrowth on GaAsP Virtual Substrates

In the first generation of GaAsP cells we faced challenges with dialing in the flow of AsH₃ and PH₃ to achieve good lattice matching between all of the cell layers. Performing multiple cell iterations was labor intensive and time consuming since each cell structure required the preparation of a GaAsP/SiGe/Si virtual substrate on which to build the cell. One way around this limitation is to grow a GaAsP virtual substrate, remove it from the reactor, cleave it and perform experimental splits on the pieces. This enables us to observe the effect of various cell growth parameters growth on its performance independent of the GaAsP/SiGe interface. In addition to allowing faster iteration between cells, the ability to regrow on a GaAsP surface is an important step in being able to recycle GaAsP virtual substrates if a lift-off process is implemented.

We performed a series of GaAsP regrowth experiments to investigate the effect of pre-growth surface clean treatments. The treatments tested investigate the efficacy of various surface cleaning processes (DI water rinse, solvent clean, UV-OZONE clean) and compared them to a control sample which received no treatment—referred to as the null sample. All of the regrowth samples were cleaved from the same GaAsP virtual substrate (SEL 2729). The virtual substrate was prepared by growing a lattice matched GaAs₀.₇₄P₀.₂₆ layer on a Si₀.₂₅Ge₀.₇₅ capped graded buffer using the optimized growth procedures developed in Chapter 3. During the cool down, the AsH₃ and PH₃ flows were continually ramped to
maintain the GaAs\(_x\)P\(_{1-x}\) surface composition. The calibration data shown in Chapter 3 was used to select the appropriate AsH\(_3\) to PH\(_3\) flow for a given temperature during the cool down process. This same virtual substrate would be used for the Gen2 and Gen3 GaAs\(_x\)P\(_{1-x}\) solar cell studies. The GaAsP virtual substrate is removed from the reactor and glove box. A piece is cleaved from the GaAs\(_x\)P\(_{1-x}\) virtual substrate, approximately 3cm x 3cm, for each regrowth clean experiment. It should be noted that the GaAsP virtual substrate was stored in a fluoroware container on a shelf in the SEL between growths—no dry box or O\(_2\) free ambient was used. The DI sample is rinsed in flowing DI water for 10 minutes and blow dried with an N\(_2\) gun just prior to loading in the reactor. The solvent cleaning treatment consisted of ultrasonicking the

![Figure 75](image-url)  

Figure 75 (a) Schematic illustration of the epi structure used for the GaAsP regrowth study. XTEM (g = 220) of the GaAsP regrowth interface for the (b) UVZONE treatment and (c) the null case-no treatment. (d) PL spectrum from the GaAsP regrowth samples showing reduced emission intensity for the UVZONE and DI-rinse treatments compared to the NULL case.
sample in various solvents (Acetone/Methanol/IPA) for 10 minutes. The sample was blow dried with the
N$_2$ gun following the last solvent clean. The UV-OZONE sample received a 10 minute treatment with the
platen heated to 100°C. For control, the UV-OZONE and null sample both “blow dried” with the N$_2$ gun
prior to loading in the reactor.

Regrowth of GaAs$_{0.74}$P$_{0.26}$ and a lattice matched InGaP cap was performed simultaneously on all
pre-cleaned samples of the GaAs$_{0.74}$P$_{0.26}$ virtual substrate pieces. The samples were heated under an over
pressure of AsH$_3$ and PH$_3$. The fraction of the two gasses was changed with temperature to maintain a
constant surface composition, similar to the procedure used for cool-down. The regrowth samples are
baked at 725°C for 5 minutes under the AsH$_3$ and PH$_3$ flows that will be used for growth. The bake is
intended to drive off moisture and other atmospheric contaminants that might be on the surface. A GaAsP
layer is nucleated with a low TMGa flow (20sccm) for the first 50nm, after which the TMGa flow is
increased to the normal growth flow (50sccm). Prior to growing the InGaP layer, the temperature was
dropped to 650°C. The quality of the regrowth was assessed using a combination of XTEM and PL
spectroscopy.

The results of the regrowth study are summarized in Figure 75. In general the “wet” cleans
produced the poorest quality regrowth interface. We hypothesize that this is in part due to the N$_2$ blow
dry step that follows the wet process. After the growths it was discovered that the N$_2$ gun particle filter
was spoiled and could have been depositing particles on the surface. The “dry” cleans had the best quality
regrowth as can be seen in the PL spectrum. Contaminants at the regrowth interface lead to the nucleation
of dislocations and other defects that degrade the material quality. We found that the optimal regrowth
scheme involved no pre-clean. Despite the adsorption of moisture, oxygen and carbon, the GaAsP virtual
substrate regrowth without any clean demonstrated an interface that is undetectable in TEM—indicating
the high quality of this interface. We compared the TDD of the GaAsP virtual substrate to the TDD of a
GaAsP film grown on the virtual substrate and found they were almost identical.
(TDD$_{\text{GaAsP Virtual Substrate}} = 2.3 \pm 0.6 \times 10^6$ cm$^{-2}$ vs TDD$_{\text{GaAsP Cell on GaAsP VS}} = 1.9 \times 10^6$ cm$^{-2}$). Furthermore, we will see in the next sections that EBIC of the regrowth does not show any macroscale defect nucleation due to regrowth.

All of the following solar cell results are grown on GaAsP virtual substrates—specifically SEL2729. By cleaving the wafer and doing re-growths, multiple experimental splits can be performed with the same starting substrate quality. This enables us to separate effects of the GaAsP/SiGe growth from effects of the GaAsP cell growth.

5.7 Gen2 GaAsP cell growth and heteroepitaxy

Etch pit density measurements performed on exemplar Si$_{0.25}$Ge$_{0.75}$ graded buffer structures show threading dislocation densities in the high $10^5$ cm$^{-2}$ range, confirming that the $\sim 3\%$ lattice mismatch between Si and GaAs$_{0.76}$P$_{0.24}$ can be accommodated while retaining high material quality. No antiphase domains, stacking faults, microtwins or dislocation nucleation are observed at the GaAsP/SiGe heterointerface in XTEM, indicating minimal, if any, TDD increase at the heterointerface. Symmetric (004) and asymmetric (224) HRXRD reciprocal space maps of the solar cell epi-stack show two peaks near the lattice constant of Si$_{0.25}$Ge$_{0.75}$, indicative of slight composition mismatch in the GaAs$_x$P$_{1-x}$ layers grown at 725°C and 650°C, on the order 1% – 2% P absolute composition. Despite the slight composition shift, PVTEM for the cell structure reveals a dislocation density of $3.4 \pm 1.3 \times 10^6$ cm$^{-2}$ for the best cells and $5.7 \pm 1.6 \times 10^6$ cm$^{-2}$ for the worst of the lot. EBIC revealed similar, but lower, defect densities. The TDD calculated by PVTEM and EBIC is listed in Table 5. The total area observed per sample in PVTEM and EBIC is about 1000 $\mu$m$^2$ and 100,000 $\mu$m$^2$ respectively. The difference in TDD calculated by the two methods is due to the limited area sampled in PVTEM which makes accurate quantification of low TDD difficult. Some misfit dislocation segments were observed in PVTEM, indicating that the slight composition mismatch
between the layers was relaxed by causing the available threading dislocation segments to glide. This is not ideal as it increases the dislocation line length, adding strong non-radiative recombination sites within the cell, reducing quantum efficiency. This can be readily seen in EBIC of the cells, which show long segments of reduced current collection Figure 77. The high density of misfit dislocation segments affects the cell performance of Sample A and B, especially for larger area cells which have lower \( V_{oc} \).

5.8 Gen2 GaAsP Cell performance

The GaAs\(_x\)P\(_{1-x}\) solar cells (107 in total) were tested under approximate AM1.5G irradiance conditions; the uncorrected results are summarized in Table 1. Typical production solar cell metal coverage is about 5% whereas the mask used for these cells has between 3% – 18% metal coverage depending on the design. The 0.01 \( \text{cm}^2 \) cells generally have the best \( V_{oc} \), but shading losses from relatively high metal coverage (up to 12%) and shading losses from the shadow cast by the contact probe limited the \( j_{SC} \) of the small cells to about 11 mA/cm\(^2\). The \( j_{SC} \) for these small cells was very sensitive to the manner in which they were contacted, the current could vary by about 10% depending on how much shading loss was incurred by the probe tip. The small cells have a higher maximum measured \( V_{oc} \) since it is possible to sample a small region of the wafer with minimal density of dislocation pileups and misfit segments. In general the larger cells had lower metal coverage, ~5%, and were less sensitive to probe shading losses consequently the \( j_{SC} \) of the larger cells is up to 11.8 mA/cm\(^2\), but the \( V_{oc} \) of these large cells was generally lower.
### Table 5 SUMMARY OF SOLAR CELL PROPERTIES AND PERFORMANCE

<table>
<thead>
<tr>
<th>Sample</th>
<th>TDD PVTEM (#/cm²)</th>
<th>TDD EBIC (#/cm²)</th>
<th>$E_g$ (eV)</th>
<th>Area (cm²)</th>
<th>Metal Coverage (%)</th>
<th>$V_{oc}$ (V)</th>
<th>$W_{oc}$ (V)</th>
<th>$J_{sc}$ (mA/cm²)</th>
<th>FF (%)</th>
<th>η (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>$3.5 \pm 1.4 \times 10^6$</td>
<td>$2.2 \pm 0.5 \times 10^6$</td>
<td>1.71</td>
<td>0.01</td>
<td>8.7</td>
<td>1.22</td>
<td>0.48</td>
<td>11.0</td>
<td>82.9</td>
<td>11.2</td>
</tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>0.04</td>
<td>5.4</td>
<td>1.20</td>
<td>0.51</td>
<td>11.6</td>
<td>82.2</td>
<td>11.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.16</td>
<td>7.4</td>
<td>1.19</td>
<td>0.52</td>
<td>11.8</td>
<td>81.1</td>
<td>11.4</td>
</tr>
<tr>
<td>B</td>
<td>$5.7 \pm 1.6 \times 10^6$</td>
<td>$3.4 \pm 0.5 \times 10^6$</td>
<td>1.69</td>
<td>0.01</td>
<td>8.7</td>
<td>1.18</td>
<td>0.51</td>
<td>10.9</td>
<td>82.3</td>
<td>10.6</td>
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<td></td>
<td></td>
<td>0.04</td>
<td>5.5</td>
<td>1.18</td>
<td>0.51</td>
<td>11.3</td>
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<td>10.9</td>
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<td></td>
<td></td>
<td>0.16</td>
<td>5.1</td>
<td>1.18</td>
<td>0.52</td>
<td>11.0</td>
<td>76.8</td>
<td>9.9</td>
</tr>
<tr>
<td>C</td>
<td>$3.4 \pm 1.3 \times 10^6$</td>
<td>$1.9 \pm 0.4 \times 10^6$</td>
<td>1.72</td>
<td>0.01</td>
<td>8.7</td>
<td>1.23</td>
<td>0.49</td>
<td>11.1</td>
<td>80.7</td>
<td>11.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.04</td>
<td>7.9</td>
<td>1.22</td>
<td>0.49</td>
<td>11.2</td>
<td>72.3</td>
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<td></td>
<td></td>
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<td>1.22</td>
<td>0.49</td>
<td>11.5</td>
<td>80.7</td>
<td>11.3</td>
</tr>
</tbody>
</table>
Figure 76 a.) JV performance for a 0.01 cm$^2$ solar cell fabricated from Sample A under AM1.5 irradiance at 25° C. b.) Plot of IQE (dots) & EQE (solid line) measurements for samples A, B, and C. All of the samples had similar measured reflectance, plotted as a dashed black line.

The bandgap of the GaAs$_x$P$_{1-x}$ solar cells are determined by both fitting a Gaussian function to the GaAs$_x$P$_{1-x}$ PL emission spectrum for each sample and by taking the x-intercept of a linear fit to the square of the product of the near-edge EQE and the photon energy (ExEQE)$^2$. Both methods yield $E_g$ that are in close agreement and are shown in Table 1. Several cells from Sample A and Sample C had $V_{oc} = 0.48 \text{ V} - 0.49 \text{ V}$, a 45 meV improvement over prior art. Quantum efficiency measurements were performed without light or voltage bias on the large 4 mm x 4 mm cells, with an illumination spot size of approximately 2.3 mm$^2$. Since the spacing of the contact fingers is smaller than the illuminated spot size, shading losses
Figure 77 EBIC of the Gen2 GaAsP Solar cell structures. The dark black streaks observed correspond to misfit dislocation segments whereas the black spots correspond the threading dislocation segments. Samples with more lattice mismatch lead to a higher density of misfit segments.

(between 3% - 6%) will be incurred in the EQE measurements, therefore the actual EQE is likely higher than the measured value shown in Figure 76. The samples have considerable reflection losses, as high as 50% around $\lambda = 425$ nm, due to the lack of an anti-reflection coating. With an appropriate single-layer or double-layer ARC, the average reflectivity would drop to about 7% for wavelengths between 300nm – 750nm, greatly improving the current and cell efficiency [12]. The shape of the EQE curve is similar between the three samples. Losses due to absorption in the InGaP window layer account for some of the reduced short wavelength response. The higher TDD of sample B leads to increased non-radiative recombination at dislocations and a net lowering of the EQE curve compared to Sample A and C which have a lower TDD. Regardless of TDD, all of the samples exhibit a shoulder in the EQE starting at 610 nm due to lack of absorption of photons in the 1.2 $\mu$m thick cell and potential surface recombination at the InGaP BSF. Accounting for reflection losses, the maximum IQE for Sample A and Sample C exceeds 93%, indicative of the high material quality.

Using the measured reflectivity, EQE and absorption coefficients for InGaP and GaAsP, we analyzed the sources of the various loss mechanisms. The Beer-Lambert Law allows us to calculate the fraction of photons absorbed for a given wavelength given the absorption coefficient and the thickness of
the InGaP window layer and GaAsP emitter-base thickness. The fraction of light lost to various mechanisms can be accounted for using the following relations based off $\alpha$, EQE, and $R$ for a given solar cell:

Equation 5.30

\[ \text{Reflection Loss}(\lambda) = R(\lambda) \]

Equation 5.31

\[ \text{Absorption}_{\text{InGaP}} = \text{ABS}_{\text{InGaP}}(\lambda) = (1 - R(\lambda))(1 - \exp(-\alpha_{\text{InGaP}}(\lambda)t_{\text{InGaP}})) \]

Equation 5.32

\[ \text{Absorption}_{\text{GaAsP}} = \text{ABS}_{\text{GaAsP}}(\lambda) = [(1 - R(\lambda)) - \text{ABS}_{\text{InGaP}}(\lambda)][1 - \exp(-\alpha_{\text{GaAsP}}(\lambda)t_{\text{GaAsP}})] \]

Equation 5.33

\[ \text{ABS}_{\text{Total}}(\lambda) = \text{ABS}_{\text{GaAsP}}(\lambda) + \text{ABS}_{\text{InGaP}}(\lambda) \]

Equation 5.34

\[ \text{Window Loss}(\lambda) = [\text{ABS}_{\text{Total}}(\lambda) - \text{EQE}(\lambda)] \frac{\text{ABS}_{\text{InGaP}}(\lambda)}{\text{ABS}_{\text{Total}}(\lambda)} \]

Equation 5.35

\[ \text{Cell Loss}(\lambda) = [\text{ABS}_{\text{Total}}(\lambda) - \text{EQE}(\lambda)] \frac{\text{ABS}_{\text{InGaP}}(\lambda)}{\text{ABS}_{\text{Total}}(\lambda)} \]

Equation 5.36

\[ \text{Transmission Loss}(\lambda) = [1 - (R(\lambda) + \text{ABS}_{\text{InGaP}}(\lambda) + \text{ABS}_{\text{GaAsP}}(\lambda))] \]

The results of the loss analysis are shown in Figure 78 for Samples A – C for the Gen2 solar cells. As expected, the lack of an ARC leads to considerable reflection losses, 8mA/cm$^2$ – 8.4mA/cm$^2$. Losses due to surface recombination (mainly in the InGaP window layer) and defect recombination (both the InGaP window and the GaAsP cell) account for 2 mA/cm$^2$, 2.2 mA/cm$^2$ and 1.5 mA/cm$^2$ for Samples A, B and C respectively. About 13% - 20% of the current actually absorbed by the cell is lost to defects within the cell.
a.)

Figure 78 the fraction of light lost to Reflection, Transmission, and recombination in InGaP and GaAsP layers. The analysis shows that a considerable amount of short wavelength light is absorbed in the InGaP window. Misfit dislocations are especially harmful to cell performance. Samples A and Sample B have a high density of misfit dislocations in the body of the cell whereas Sample C has few—which leads to better EQE throughout the solar spectrum. B.) the total current density lost/collection for each mechanism is calculated by summing over the AM1.5 solar spectrum. The change in total photon current incident on the cell is due to the different bandgaps.
losses in the cell. The transmission loss for the cells is approximately the same for all of the cells due to a similar thickness between the cells. With a GaAsP thickness of 1.2μm, about 8% of the non-reflected photons are lost to non-absorption. Increasing the cell thickness to 2μm would reduce this loss to only 4.2% of non-reflected photons. There will be a trade-off between increasing the amount of absorbed photons and the ability to collect those photons based on the diffusion length.

5.9 Gen3 GaAsP Solar Cells

The characterization and loss analysis performed on the Gen2 motivated the direction for the Gen3 iteration of GaAsP solar cells. The first focus is resolving the lattice mismatch issue that led to dislocation glide Figure 77. The loss analysis performed on the Gen2 solar cells revealed how damaging the presence of misfit dislocations within the active cell region can be—almost 33% increase in losses despite similar TDD between Sample B and C. Additionally the InGaP window for the Gen3 solar cells is thinned from 50nm to 25nm to reduce the amount of short wavelength photons absorbed in the window layer. For the 3rd iteration of GaAsP cells we performed a series of GaAsP and InGaP calibration growths

![Figure 79 a.) Schematic illustration of a GaAsP & InGaP calibration structure. The GaAsP layers 1 - 3, progressively increase the PH3 flow with each layer. The InGaP is approximately lattice matched to the GaAsP layer 3 to minimize strain and phase separation. b.) Typical 224 RSM of the multi-layer calibration epi stack. C.) The InGaP peak is determined by scanning the sample again after selectively etching the InGaP with HCl.](image-url)
Figure 79. The multilayer GaAsP calibration structure enables the composition calibration of about 3 – 4 \( \text{AsH}_3 + \text{PH}_3 \) flow combination and their respective composition in XRD. The InGaP layer composition is targeted to be nominally lattice matched to the GaAsP Layer 3 to minimize strain during the growth of InGaP that could lead to phase separation or lattice latching—both of which would give non-representative In incorporation in the XRD analysis. Post growth the samples are characterized with HRXRD-RSMs. The InGaP peak can be de-convoluted from the GaAsP peaks with an additional RSM scan following selectively etching of the InGaP layer with HCl. Performing the calibration growth immediately prior to growing the Gen3 solar cell structures ensures there will be minimal calibration drift. In addition

Figure 80 a.) Schematic of Gen3 GaAsP cell structure—the window layer is thinned to 25nm b.) PL of the GaAsP Cell \( E_g = 1.73 \text{eV} \) (GaAs\(_{0.75}\)Po\(_{0.25}\)) c.) Representative EBIC image of the fabricated Gen3 solar cell. The dark spots are counted from multiple images, given a TDD = 2.3E6 cm\(^{-2}\). No misfit dislocations were observed.
Figure 81 Gen3 GaAsP cell performance (a) illuminated JV measurement of a 2mm x 2mm cell (b) QE and reflectivity of the cell. Eliminating misfit dislocations and thinning the InGaP window layer improved the spectral response.

to XRD, we performed PL spectroscopy on the samples to confirm the XRD composition analysis and determine the bandgap of the GaAsP and InGaP films.

Using the optimized GaAsP and InGaP growth calibrations, we grew a GaAsP solar cell using the same virtual substrate used for the Gen2 GaAsP solar cells. The InGaP window layer is reduced in thickness to 25nm to improve the blue response of the solar cell. PL and XRD confirm the target composition of the GaAsP cell we achieved. EBIC of the cells verify that there is minimal lattice mismatch between the GaAsP cell and the virtual substrate as there are no observed misfit dislocation segments. Additionally the TDD is found to be $2.3 \pm 0.4 \times 10^6 \text{ cm}^{-2}$, essentially the same as the underlying virtual substrate. This confirms that the regrowth on the GaAsP virtual substrate and the subsequent cell growth did not degrade the material quality.

JV and EQE characterization of the Gen3 solar cell reveal vast improvements over the Gen2 solar cells. The reduction in misfit dislocation density greatly improved the $V_{oc}$ of the solar cells, especially the
large area cells. The performance of 0.01 cm$^2$, 0.04 cm$^2$ and 0.16 cm$^2$ cells were similar, indicating that the GaAsP material quality is high and uniform across the wafer. The results show that even large size cells can have high Voc, Jsc and FF.

EQE measurements show a more “square” curve, with considerable improvements in the short wavelength regime. Thinning the InGaP window greatly improved the response for $\lambda < 400$nm. When corrected for reflective losses, the IQE of the Gen3 cells >93% for the wavelength region of 375nm – 525nm, almost a 10% absolute improvement over the Gen2 solar cells. When corrected for metal shading losses (about 4%), the maximum IQE reaches 99%. The absorption depth for these photons is approximately equal to the depth of the depletion region and one diffusion length. Removing misfit dislocations from the emitter and depletion region enables unity collection probability for the photons that are mainly absorbed in that region. The collection probability starts tapering at about 560nm when the photons start getting absorbed deeper in the cell—greater than one diffusion length. From the IQE

Figure 82 Loss analysis on Gen3 GaAsP cells. After optimization of the InGaP window thickness and lattice matching of the cell, recombination losses within the cell account for only 7% reduction in current.
curve and knowledge of the absorption depth, we estimate the diffusion length to be about 500nm. Quantification of this will be done in future sections based on bias-dependent QE and TRPL.

5.10 Effect of defects on minority carrier lifetime

To assess the effect of defects on the minority carrier lifetime of the GaAsP solar cells, we performed a series of time-resolved photoluminescence spectroscopy (TRPL) measurements. In TRPL, very short pulses (<50ps) of a short wavelength laser are used to pump the semiconductor sample. The emission of light from the sample is recorded as a function of time. Using the intensity vs time data for a given sample, we can extract a lifetime:

Equation 5.37

\[ I(t) = I_0 \exp \left( -\frac{t}{\tau} \right) \]

Where \( I \) is the intensity of emission, \( t \) is the time and \( \tau \) is an effective lifetime. From TRPL plots, the lifetime can be extracted from the negative inverse of the slope of a semilog plot of \( I \) vs \( t \). TRPL data was collected for the Gen2 and Gen3 GaAsP single junction solar cells to measure the effect of misfit dislocations on lifetime within the cell. The Gen2 samples with high density and low density of misfit dislocations (Sample B 2790 and Sample C 2783) were measured along with the Gen3 solar cell (Sample 2866). The samples were pumped with a 550nm laser source that had an average power of 500nW over
Figure 83 TRPL data for Gen2 (2790 and 2783) and Gen3 GaAsP solar cells (2866). The extracted effective lifetimes are 250ps, 450ps, and 550ps for sample 2790, 2783 and 2866 respectively.

As expected we see in increasing lifetime with improving material quality. The extracted lifetime of 550ps for the Gen3 GaAsP solar cells is lower than expected for the solar cell performance. This is likely due to a convolution of the lifetime with many other non-radiative recombination processes. The effective lifetime extracted from TRPL will be a convolution of the recombination rates due to radiative recombination, non-radiative recombination at traps/dislocations and surface recombination. In an ideal TRPL study one would grow multiple samples with varying thickness to extract out the surface recombination rate from the bulk lifetime. The solar cell structures have non-uniform doping density and type in the emitter and base layers. Given the absorption depth of 550nm light, the extracted lifetime is likely dominated by recombination in the highly doped emitter layer and potentially some surface recombination between the window and emitter. The actual lifetime of the base layer is expected to be
higher, on order a nanosecond given the measured IQE, diffusion length and mobilities of n-type GaAsP. The lifetimes measured here provide a baseline for the minimum lifetime of the GaAsP material in the cells, while the actual lifetime is likely much higher. Having a number for lifetime is a useful parameter to bound models of GaAsP cells as we further optimize the design. The TRPL data coupled with bias dependent QE helps fill out the design kit toolbox for optimizing GaAsP solar cells.

5.11 Conclusions

The single junction GaAsP solar cells presented here demonstrate high material quality. When corrected for reflection losses, the single junction cell efficiencies could be as high as 16% - 18%. Future cell improvements will involve reducing the TDD in the virtual substrate and reducing the TDD in the GaAsP Cell. Further reduction in TDD has the potential to reduce the current losses to defects. Thinning the InGaP window layer reduced parasitic absorption losses to about 1%. Further improvements could be made using a higher bandgap window layer—either by incorporating Al or disordering the InGaP. The real areas of optimizing are the doping levels and thicknesses of the base and emitter. This could lead to improved diffusion lengths, enabling a bump in efficiency up to 5% by improving the long wavelength current collection. Finally we demonstrated that the material quality of our GaAsP cells is quite high and has diffusion lengths on order 500nm – 1000nm. Further improvement in the current collection could be gained by increasing the thickness of the solar cell stack. Increasing the cell thickness to 2µm would reduce transmission losses by 4% absolute.

The performance of the GaAsP single junction solar cells presented in this work is comparable to the best single junction GaAsP solar cells demonstrated on any substrate—III-V or Si. With a suitable ARC coating and integration with a high efficiency Si cell, tandem efficiencies on of >28% are attainable.
Achieving this high level of efficiency requires careful attention to cell growth and minimization of misfit dislocations as well as threading dislocations within the active region of the cell.
Chapter 6
Optical properties of GaAs\textsubscript{x}P\textsubscript{1-x} alloys for solar cell applications

6.1 Introduction

GaAs\textsubscript{x}P\textsubscript{1-x} alloys possess ideal bandgaps for integration with silicon solar cells to enable high efficiency tandem PV cells. While the bandgap of GaAs\textsubscript{x}P\textsubscript{1-x} as a function of composition is has been well characterized, the other optical properties (refractive index and absorption coefficient) are not well known. What literature there is available has widely varying results for the same composition due to poor quality samples. Modeling and optimization of GaAs\textsubscript{x}P\textsubscript{1-x} cells and especially GaAs\textsubscript{x}P\textsubscript{1-x} /Si tandem cells requires knowledge of the optical properties for designing ARCs and optimizing cell thicknesses for current matching. In this chapter we map the optical property space of GaAs\textsubscript{x}P\textsubscript{1-x} alloys from GaP to GaAs using ellipsometry. While standard testing conditions for solar cells is 25°C, real world devices frequently are exposed to temperatures as high as 50°C for rooftop and heat-sinked concentrator applications. The effect of temperature on optical properties of GaAs\textsubscript{x}P\textsubscript{1-x} is important for designing real world solar cells. Additionally doping is known to change the optical properties of materials as well. We investigate the effect of temperature and doping on the optical properties of GaAs\textsubscript{0.77}P\textsubscript{0.23}. The dataset collected in this chapter enables future tandem solar cell devices to be better designed for optimize current matching and minimize reflection—in tests and in the field.
6.2 Review of GaAs\textsubscript{x}P\textsubscript{1-x} Optical properties literature

Existing literature on the material properties of GaAs\textsubscript{x}P\textsubscript{1-x} alloys beyond the bandgap is sparse—most of the characterization was performed in the 1980's on samples of poor quality. The mobility of GaAs\textsubscript{x}P\textsubscript{1-x} alloys vary by nearly a factor of 3x – 5x for a given composition depending on the author cited. Much of this is attributed to a wide degree of material variability between growers. What was measured is some convolution of the actual GaAs\textsubscript{x}P\textsubscript{1-x} material property and the defects. The same trend applies to published GaAsP optical properties. Clark et al published the first report on the optical properties, refractive index and absorption coefficient, of GaAs\textsubscript{x}P\textsubscript{1-x} alloys spanning from GaP to GaAs in 1967 [74] Figure 85a. The work of Clark focused on near band edge and sub-bandgap photon energies and did not include any information on the absorption for photon energies with $E_{\text{photon}} > E_g$, a severe limitation of the data for solar applications. In addition to the wavelengths of interest being limited to the sub bandgap regime, the material quality of the samples used for this study were classified as either being “clear”, “cloudy” or “partly cloudy”. Given two different samples with the same composition, the reported absorption coefficient could vary by a factor of 3. This severely limits the utility of the initial data set.

![Figure 84 Literature values for GaAsP alloy refractive index for the visible and near-IR photon range. Reproduced from Clark [74]](image_url)
refractive index data for GaAs$_x$P$_{1-x}$ alloys assembled by Clark appears to be more consistent and matches well with the values measured in this study Figure 84. Unfortunately the blue photon range is not included in the data set, making ARC design difficult. In the 1980's the optical properties of GaAs$_x$P$_{1-x}$ alloys was further expanded on by Hasegawa [75] and Nelson & Holonyak [76] as GaAs$_x$P$_{1-x}$ alloys were popular.
choices for LED materials. While these authors reported the absorption coefficients for photons with $E > E_g$, the composition space was limited as the resolution of the data near the band edge and considerably above the band edge Figure 85b. The current matching criteria for tandem solar cells makes accurate data for absorption an important cell parameter for optimization. Accurate modeling of absorption in GaAs$_x$P$_{1-x}$ solar cells would be limited by the available GaAs$_x$P$_{1-x}$ literature. While a reasonable amount of data exists for GaAs$_x$P$_{1-x}$ alloys at cryogenic temperatures, there is far less at room temperature and almost none for elevated temperatures. Our goal for this study is to build out the existing library of GaAs$_x$P$_{1-x}$ optical properties to better enable cell designers with a more complete tool kit.

6.3 GaAsP Optical Properties Experimental Methods

We used the procedures developed in Chapter 3 to grow a series of high quality lattice matched GaAsP thin films on SiGe graded buffers with various compositions spanning the Si-Ge composition space. The lattice matched GaAs$_x$P$_{1-x}$ films were grown by metal organic chemical vapor deposition (MOCVD) on Si$_{1-y}$Ge$_y$ virtual substrates. The Si$_{1-y}$Ge$_y$ virtual substrates were grown in either a ultra-high vacuum chemical vapor deposition (UHVCVD) reactor or a chemical vapor deposition (CVD) reactor and consist of compositionally graded Si$_{1-y}$Ge$_y$ buffers with a thick uniform composition cap Figure 86. The details of the graded buffer growth can be found in Chapter 3. GaAs$_x$P$_{1-x}$ films of various compositions were grown lattice matched on virtual substrates, allowing us to avoid much of the material degradation due to strain that plagued the preliminary GaAs$_x$P$_{1-x}$ characterization work Figure 86. A total of five samples with GaAs$_x$P$_{1-x}$ compositions $x = 0.83, 0.75, 0.69, 0.63,$ and $0.58$ were grown. Reference values for GaP and GaAs were also used included. In addition to growing unintentionally doped (UID) GaAs$_x$P$_{1-x}$ samples across the composition space, two samples were grown with either N or P type doping at GaAs$_{0.77}$P$_{0.23}$ composition to study the effect of doping on the optical properties of GaAs$_x$P$_{1-x}$. This composition is chosen since it has
Chapter 6 – Optical Properties of GaAsP Alloys for Solar Cell Applications

Figure 86 a.) Schematic of epi-stack for GaAsP composition n-k study. b.) Schematic of epi-stack structure for studying the effect of doping on n-k properties of GaAs$_{0.77}$P$_{0.23}$.

an idea bandgap (1.7eV) for GaAs$_{1-x}$/Si solar integration. The thickness of the constant composition Si$_{y}$Ge$_{1-y}$ cap and lattice matched UID GaAs$_{1-x}$ layer are both 500nm. A doping of 5x10$^{18}$ cm$^{-3}$ of either n-type or p-type is achieved by doping the GaAs$_{1-x}$ film with Si or Zn respectively.

After growth, the samples were characterized by high resolution x-ray diffraction (HRXRD) to determine the composition and spectroscopic ellipsometry to determine the optical properties. The ellipsometry measurements were performed over a wavelength range of 193nm to 1690nm using an angle of incidence of 55° to 75° in 10° increments on a Woolam M-2000 DI kinetic ellipsometer. From the phi and delta data, the refractive index (n) and extinction coefficient (k) can be determined. The GaAs$_{x}$/Si$_{y}$Ge$_{1-y}$ epi stack was first measured, then the GaAs$_{x}$ layer was selectively wet etched away so the Si$_{y}$Ge$_{1-y}$ virtual substrate layer could be measured independently. With both sets of data, the optical properties of the GaAs$_{x}$ film could be de-convoluted from the combined structure measurement data.

Ellipsometric data analysis and fitting was performed using the CompleteEASE version 4.91 ellipsometry suite. The effect of temperature on optical properties of GaAs$_{x}$ was also studied using a heated stage on the ellipsometer. Ellipsometry measurements were performed for stage temperatures between 25° C and 150° C. The same deconvolution method mentioned above is used at each stage temperature.
6.4 Effect of GaAs$_x$P$_{1-x}$ composition on optical properties

The multilayer structure of GaAs$_x$P$_{1-x}$ films grown on Si$_y$Ge$_{1-y}$ virtual substrates complicates the data collected during ellipsometry measurements. The GaAs$_x$P$_{1-x}$ and Si$_y$Ge$_{1-y}$ layers can be interrogated individually by selecting different wavelength ranges of interest due to the differing band gaps between the two materials—long wavelengths ($E_{\text{photon}} < E_{\text{GaAsP}}$) are suitable for gathering information on Si$_y$Ge$_{1-y}$ while ($E > E_{\text{GaAsP}}$) will provide data for GaAs$_x$P$_{1-x}$. Fitting the ellipsometric data is broken into three parts. The GaAs$_x$P$_{1-x}$ film is transparent to near IR light due to its relatively large bandgap (1.4eV – 2.2eV), while Si$_{1-y}$Ge$_y$ alloys are good absorbers of near IR due to their relatively low bandgap (0.67eV – 1.1eV).

Analyzing ellipsometric data is an iterative process that starts with performing measurements on a sample. Following measurements, a model of the sample is constructed in the ellipometric modeling package CompleteEASE. The model is compared to the experimental data. Changes to the layer thickness, surface roughness and surface layers are modified until an optimal fit is achieved. For the GaAsP/SiGe samples, the samples are measured and a simple model of the sample is constructed. Initial fitting focuses on photons in the near-IR wavelength range since light penetrates all the way to the Si substrate. The ellipsometry data for a GaAsP/SiGe sample is shown in Figure 87a. There are a series of large oscillations in Psi and Delta for photons with energy less than the bandgap of GaAs$_x$P$_{1-x}$ due to the thickness of the transparent GaAs$_x$P$_{1-x}$ layer. A series of small oscillations observed in the longer wavelengths are due the thickness of the many thin layers of Si$_y$Ge$_{1-y}$. A course fit to the data is made from the near IR data which specifies the nominal thickness of the GaAs$_x$P$_{1-x}$ film and the nominal composition Figure 87. This course fit is refined by considering the UV and visible wavelengths of light which are primarily absorbed by the GaAs$_x$P$_{1-x}$ film Figure 87b. Final model optimization considers surface roughness and allows the nominal values of composition and thickness for the GaAs$_x$P$_{1-x}$ and SiGe layers to vary slightly so the model can converge on a best fit Figure 87c. After the model converges to a good fit of the experimental data, the
refractive index and extinction coefficient of the GaAs$_x$P$_{1-x}$ film is extracted. The same sort of fitting is done for the doping and temperature study samples.

Figure 87 a.) Near IR light is used to generate a course fit of the GaAsP/SiGe ellipsometry data with a model. Large oscillations in Psi and Delta are used to fit GaAsP film thickness while small oscillations provide thickness and composition data for the SiGe virtual substrate. B.) UV and visible light gives direct information about the GaAsP film since it is highly absorbing. The optical properties of the GaAsP layer in the model are varied to improve the fit based on part a. C.) Surface roughness and multiple thickness/composition iterations converges on a best fit of the model to experimental data.
The results of the n-k data extraction from the various GaAsP composition samples appear to fit between the GaAs and GaP reference data from SOPRA. While the general shape of the curves look good

**Figure 88** Refractive index of GaAs$_{x}$P$_{1-x}$ alloys with various P compositions from this study. GaAs and GaP refractive index values from SOPRA are also plotted. B.) Extinction coefficient of GaAs$_{x}$P$_{1-x}$ alloys with various P composition. GaAs and GaP extinction coefficient values from SOPRA are also plotted

**Figure 89** A.) Doping has nominal effect on the real portion of the refractive index for GaAs$_{0.77}$P$_{0.23}$. b.) The imaginary part of the refractive index of GaAsP$_{0.23}$ is extended to longer wavelengths when the material is doped.
Figure 91 Effect of temperature on the refractive index and absorption coefficient for $\text{GaAs}_{0.77}\text{P}_{0.23}$

Figure 90 Plot of the difference in refractive index between room temperature and elevated temperature $\text{GaAs}_{0.77}\text{P}_{0.23}$

for $E_{\text{photon}} > E_{\text{g, GaAsP}}$, there is some subbandgap absorption. Two possible mechanisms are proposed for this sub-bandgap absorption. One possibility is that the absorbing SiGe virtual substrate is not fully being subtracted from the GaAsP properties in the model fitting. Since the k-values are very close to zero in the sub-bandedge region this is a possibility. Another possibility cause of sub-bandgap absorption is free carrier absorption at the GaAsP/SiGe interface. During heteroepitaxy, Si and Ge diffuse into the GaAsP
film and As and P diffuse into the SiGe film creating a thin (~30nm) highly n-type doped ($10^{19}$ cm$^{-3}$ - $10^{20}$ cm$^{-3}$) layer at the interface Figure 92. From the intentionally doped samples we can see that doping does increase absorption, especially in the sub-bandgap region. The UID-GaAsP samples likely have $10^{18}$ cm$^{-3}$ level Si and Ge doping present. While the trail off in the absorption curve might not be representative of the pure GaAsP material properties, this is indicative for GaAsP grown on SiGe.
6.5 Discussion of experimental results

The optical properties of GaAs alloys have been shown to change with doping. Specifically, the absorption are shown to change with doping level and doping type. This phenomena has to do with increase free-carrier absorption as well as an increase in the density of states below the band edge due to donor and acceptor levels. This creates states with \( E < E_g \) for photon absorption. The effect is really only

![Graph of optical constants vs. nm](image)

**Figure 92 a.)** n-k data for growth SEL 1461 showing sub-bandgap absorption. **B.)** SIMS of a typical GaAs\(_{x}\)P\(_{1-x}\)/SiGe growth. Considerable Si and Ge doping in the GaAs\(_{x}\)P\(_{1-x}\) film exists due to auto-doping and diffusion from the SiGe.
prevalent doping levels >5E18 cm⁻³. For single junction cells, the change in absorption will have minimal effect, but for tandem cells this can lead to reduced current in the bottom cell. For optimal tandem performance the composition of the top cell might be pushed slightly higher in $E_g$ to compensate for doping effects.

The temperature properties of GaAs$_x$P$_{1-x}$ alloy show that there is an effective lowering in the bandgap of the alloy as the temperature increases. This is to be expected from thermal expansion which will move the atoms in the lattice further apart, thereby reducing their periodic potential and reducing the bandgap. The shift in refractive index is relatively minor, only 0.1 for temperatures up to 100°C. Knowing the temperature effect on refractive index is vital for designing an optimal ARC for GaAs$_x$P$_{1-x}$ cells and GaAs$_x$P$_{1-x}$/Si tandem cells.

### 6.6 Conclusion

High quality materials lead to better quality data that enables one to elucidate what the physical properties of a material are and not just the effects of defects and processing issues. Multijunction solar cells can be better optimized now that n-k data is known.
Chapter 7
Conclusions and Future Work

7.1 Summary of results and implications

Integration of III-V materials on Si substrates is a challenge despite the past 30 years of research in the field. Successful integration of III-V material on Si via a low cost scalable process would unlock a new generation of electronic device that go beyond high efficiency solar. While the commercialization of III-V on Si is still some time out, the body of research presented in this thesis pushes integration of III-V on Si closer to actualization with the demonstration of high quality (TDD = 2x10^6 cm^2) GaAs_{x}P_{1-x} solar cells monolithically integrated on 150mm Si wafers. The high quality if the GaAsP films was demonstrated by the good cell performance, in particular the high V_{oc}. The high material quality enabled the realization of high efficiency 1.7eV GaAsP cells (\eta_{ARC CORRECTED} = 17%) on large area, low cost substrates through an industrially scalable process. Reaching this material quality goal and cell performance milestone required development of knowledge across multiple material systems and optimization of growth as well as fabrication and device design. The platform developed in this thesis along with the design tool kit enable further optimization of GaAs_{x}P_{1-x} cell performance and high efficiency III-V/Si tandem PV cells.

The integration of III-V materials with group IV materials has many unique challenges associated with it that vary based on composition and temperature. In this work we discovered two defect mechanisms at play that degraded the material quality at the GaAsP/SiGe interface. The first being the reaction between Si-P that degrades the film quality of GaAs_{x}P_{1-x} grown on SiGe—particularly for high Si
& P composition SiGe and GaAsxP1-x respectively. An AsH3 passivation processes was developed to prevent this reaction. The second mechanism identified was the condensation of vacancies into dislocation loops that ultimately expanded into threads. We demonstrated that thin tensile strained layers at the heterointerface can be used to bias the concentration of vacancies such that they do not reach a critical level necessary for condensation. Identifying and understanding these mechanisms enabled a 10x reduction in the TDD of GaAsxP1-x films grown on lattice matched Si0.35Ge0.65 virtual substrates compared to the standard process.

Using this optimized initiation conditions we demonstrated 1.7eV GaAsxP1-x solar cell monolithically integrated on Si substrates with a TDD = 2x10^6 cm^-2, which represents a 4x reduction compared to best published results in literature. These fundamental improvements in integration and material quality were paramount to developing high efficiency cells. With the incorporation of a suitable ARC and integration with a Si solar cell, the GaAsxP1-x cells demonstrated in this work would enable GaAsxP1-x/Si tandem cells with η >25%. With the availability of high quality GaAsxP1-x films we were able to map out the optical properties of GaAsxP1-x alloys across the composition space. This is an important result for continued cell design and optimization. Knowing the optical space is important for continued innovation and improvements. Additionally accurate knowledge of absorption is paramount for cell characterization and loss analysis.

7.2 Suggestions for future work

7.2.1 Continued GaAsP/SiGe growth optimization

We demonstrated a large reduction in the defect density of GaAsxP1-x films grown on SiGe virtual substrates throughout the course of this thesis. Further improvement of the GaAsxP1-x film quality will
require improving the quality of the relaxed SiGe graded buffer layer and further optimization of the initiation sequences used. We found that the cleanliness of the MOCVD reactor drastically effects the material quality of the SiGe graded buffer. A typical $\text{Si}_{0.50}\text{Ge}_{0.50}$ virtual substrate has an EPD in the low $10^5$ cm$^{-2}$ range. EPD performed after continued grading to $\text{Si}_{0.35}\text{Ge}_{0.65}$ or $\text{Si}_{0.25}\text{Ge}_{0.75}$ will increase to high $10^5$ cm$^{-2}$ if the cleanliness of the reactor is not maintained. We found that after etching the MOCVD shower head, there was no longer an increase in EPD when grading to $\text{Si}_{0.25}\text{Ge}_{0.75}$. Developing a more robust process for growing the SiGe graded buffer and GaAs$_x$P$_{1-x}$ nucleation layer will be important for achieving repeatable low defect density materials. Additionally the GaAsP/SiGe initiation studies were performed at the $\text{Si}_{0.35}\text{Ge}_{0.65}$ lattice constant while the cells were all grown on $\text{Si}_{0.25}\text{Ge}_{0.75}$ virtual substrates. It is possible that different amounts of tensile strain in the SiGe cap and different durations of AsH$_3$ initiation could lead to improved GaAs$_x$P$_{1-x}$ virtual substrate material quality.
7.2.2 Mapping GaAs$_x$P$_{1-x}$ alloy properties and cell optimization

In Chapter 6 we explored the optical properties of GaAs$_x$P$_{1-x}$ alloys since the available literature values were either missing or unreliable. Similar gaps in knowledge exist for other pertinent material properties of GaAs$_x$P$_{1-x}$ alloys, notably the electronic mobility and minority carrier lifetime. Knowledge of these properties is vital for modeling and optimizing cell performance. Studies that map the mobility as a function of both doping as and composition would be valuable for the field. Additionally the lifetime of GaAs$_x$P$_{1-x}$ films as a function of TDD and doping would be very useful for modeling cells and predicating performance given a particular material quality. Given these material parameter and the optical properties we can start building one dimensional cell models using packages like PC1D.

![GaAsP Electron Mobility](image)

Figure 93 GaAsP electron mobility as a function of composition measured by Tienjen and Ku
7.2.3 Layer transfer & wafer recycling

One major limitation of using SiGe graded buffers for the integration of GaAsP on Si is the fact that the SiGe buffer is opaque. In an ideal world the Si substrate could be used as a Si solar cell, but nearly 80% of the available photons with $E < E_{GaAsP}$ would be lost to the SiGe graded buffer layers. While there is considerable development of the GaP/Si and the use of transparent GaAsP graded buffers, the material quality is still lacking—TDD $> 8 \times 10^6$ cm$^{-2}$. To leverage the high material quality enabled via GaAsP/SiGe integration, we propose layer transfer and substrate removal as a possible avenue for realizing high efficiency GaAsP/Si cells Figure 94. First the GaAsP cell is bonded to a Si cell or suitable carrier either through direct wafer bonding or some adhesive bonding. The bonded stack is submerged in a selective etchant that attacks the release layer. After some time the GaAsP buffer and substrate can be removed and the GaAsP cell is transferred to the Si cell/handle. Similar layer transfer schemes have been proposed for recycling GaAs substrates used for high efficiency multijunction III-V solar cells. An added benefit to

![Figure 94 Schematic illustration of GaAs$_x$P$_{1-x}$ cell layer transfer, substrate removal via selective etching and wafer recycling.](image-url)
this process is that the SiGe graded buffer and GaAsP nucleation layer could be recycled for future cell
growths—enabling the initial substrate and epi investment to be recouped. Realizing the layer transfer
and recycling requires the development of a suitable sacrificial etch layer. GaAs/AlGaAs is the archetype
for layer transfer and substrate recycling as the Al bearing film layers can be etched highly selective against
the GaAs films. Typically this is done with a heated HF solution. For GaAs_{x}P_{1-x} films, AlAs_{x}P_{1-x} or Al_{y}Ga_{1-
}yAs_{x}P_{1-x} could be used as a sacrificial etch layer.

Realizing layer transfer and substrate removal will require development of appropriate etch layer
composition and thickness in addition to appropriate etch chemistries. Fortunately the work of previous
layer transfer schemes can be leveraged to accelerate this process. One additional challenge that must be
overcome is crosshatch surface roughness from the graded buffer. RMS surface roughness >1nm prevents
direct semiconductor-semiconductor wafer bonding. Incorporating a CMP step after grading to the final
desired SiGe composition could enable very smooth GaAsP layers to be grown. Being able to form an
electrically active bond with no interlayer between the GaAsP cell and a Si cell is necessary for a 2-terminal
tandem cell configuration. Sharma demonstrated the ability to grow tunnel junctions in GaAsP, so the
only missing pieces are the etch layer and wafer bonding process development [30].

7.2.4 Triple junction cells on Si

Given a high quality GaAs_{x}P_{1-x} template layer on large area Si substrates, the integration of a third
junction is not too hard and has the potential to increase the efficiency. Top cell candidate materials
include In_{x}Ga_{1-x}P and AlInGaP since they can be lattice matched to the underlying GaAsP layer and provide
bandgaps in the 2eV range. Grassman and others have calculated the efficiency of a III-V/Si triple junction
as a function of the top cell and middle cell band gap in a similar fashion as the tandem cell calculations.
From those calculations we see that theoretical efficiencies on order 40% - 46% are achievable for a lattice
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matched InGaP/GaAsP/Si triple junction cell—representing a 10% - 20% relative increase in efficiency compared to a GaAsP/Si tandem cell. Realizing this triple junction stack requires developing an optimal In$_2$Ga$_{1.2}$P cell structure, appropriate window layers and a tunnel junction to connect the two. We grew a very preliminary In$_{0.36}$Ga$_{0.64}$P cell on the GaAsP/Ge$_{0.75}$/Si virtual substrate that was developed through the course of this thesis. The structure and doping of the cell was not optimized— it is essentially the GaAs$_x$P$_{1-x}$ cell structure used from Chapter 5 but with InGaP as the absorber material and AlInGaP as the window/BSF material. From this first attempt we see that high quality 1.97eV In$_{0.36}$Ga$_{0.64}$P cells can be grown on the GaAsP virtual substrate with minimal defect nucleation (TDD$_{GaAsP}$ = 2.3x10$^6$ cm$^{-2}$ VS TDD$_{InGaP}$ cell = 3.5x10$^6$ cm$^{-2}$). The JV and EQE of this initial demonstration is far from optimal, but is a promising first step to realizing a InGaP/GaAsP/Si triple junction cell. There are considerable “blue” photon losses in the window and emitter layers. This is likely due to the window layer being too absorbing. The layer could be grown at higher temperatures to disorder it or be grown with a higher Al content to increase the bandgap and reduce absorption. Additionally the high doping and thickness of the emitter

![Figure 95](image.jpg)

Figure 95 Iso-efficiency plots for series-connected triple-junction III-V/Si tandem cells, calculated at the ideal radiative limit and with effective top-cell thicknesses adjusted for optimized current-matching, under (a) one-sun AM0, (b) one-sun AM1.5G, and (c) 100x concentrated AM1.5D illumination. The dashed lines denote iso-efficiency cross sections attainable with internally-lattice matched metamorphic III-V top and middle cells. Reproduced from Grassman [88]
Figure 96 Preliminary InGaP top cell demonstration for a 3-junction III-V/Si cell. (a) Schematic of the epi-stack based on the GaAsP single junction cells. (b) EBIC image of InGaP cell showing good lattice matching and TDD = 3.5x10^6 cm^-2. (c) JV measurements of a 1mm x 1mm InGaP cell illuminated with approximate AM1.5 spectrum. (d) Photoluminescence from the InGaP cell showing bright light emission at 630nm (E_g = 1.97eV). (e) EQE measurements performed on a 4mm x 4mm.

layer could be contributing to the short wavelength photon losses. InGaP cells grown at Yale and NREL have been shown to be more successful with thinner emitter layers or with inverted structures. Investigating these avenues is important for further optimization. The minority carrier diffusion length in the base layer of the InGaP cell appears to be low. This could be the cause of the EQE roll off near the band edge. Despite these limitations of this preliminary InGaP cell, development of a high efficiency cell is not out of the realm of possibility. Determining the cell material properties such as absorption coefficient and diffusion length are necessary for building a cell model in PC1D. Growth iterations similar to those performed for the GaAsP cells in Chapter 5 would be useful for mapping the appropriate processing space for InGaP cells. One other benefit to high bandgap materials integrated on the
GaAsP/SiGe/Si platform is the possibility of other devices such as visible red and yellow light emitters—LEDs and Lasers—and high power transistors.
References


Appendix A:

GaAsP Cell Fabrication Process

The process flow listed below was used to fabricate the GaAsP cells presented in this work. The STS-CVD was down for the duration of the GaAsP cell fabrication process, so a hard mask could not be used for the mesa etch procedure. This complicated the process since the typical arsenide wet etch (NH₄OH:H₂O₂:H₂O) strips photoresist. An alternate etch chemistry was developed (HCl:H₂O₂:H₂O). The etch rate varies with GaAsP composition and age of solution. The mesa depth was checked periodically during the mesa etch with a profilometer. The InGaP window layer is selectively etched in neat HCl. If the PR is not hard-baked at high temperature 130°C – 140°C the etchant will start to remove the PR during the mesa etch. The non-standard high temperature hard bake was adapted to alleviate this problem. The GaAsP contact removal etch uses the front side metal as an etch mask and stops on the InGaP window layer. The NH₄OH:H₂O₂ solution will attack the backside Al contact, therefore it must be protected during the contact etch. A stainless steel carrier and CrystalBond wax are effective at protecting the backside during the etch and can easily be removed afterwards.
## Appendix A: GaAsP Cell Fabrications Process

### P-on-N Cell (Mesa Last)

<table>
<thead>
<tr>
<th>Step</th>
<th>Process</th>
<th>Discription</th>
<th>Lab</th>
<th>Machine</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Rinse with acetone, methanol, isopropanol</td>
<td>Organic clean</td>
<td>TRL</td>
<td>Photo-wet</td>
</tr>
<tr>
<td></td>
<td>Photolithography</td>
<td></td>
<td>TRL</td>
<td></td>
</tr>
<tr>
<td></td>
<td>HMDS</td>
<td></td>
<td>TRL</td>
<td>HMDS</td>
</tr>
<tr>
<td></td>
<td>Spin coat AZ5214</td>
<td></td>
<td>TRL</td>
<td>Hotplate 300</td>
</tr>
<tr>
<td></td>
<td>Soft-bake 90C: 30min in oven or 5min on hotplate</td>
<td></td>
<td>TRL</td>
<td>MA6</td>
</tr>
<tr>
<td>2</td>
<td>Expose 9s</td>
<td>Mask layers for top-contact</td>
<td>TRL</td>
<td>Hotplate 300</td>
</tr>
<tr>
<td></td>
<td>Image reversal bake 110C 2min</td>
<td></td>
<td>TRL</td>
<td>MA6</td>
</tr>
<tr>
<td></td>
<td>Flood expose 98sec</td>
<td></td>
<td>TRL</td>
<td>Photo-wet</td>
</tr>
<tr>
<td></td>
<td>Develop with AZ422</td>
<td></td>
<td>TRL</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Ash 5 min 1000W and/or 1:80 H2SO4:DI 30s</td>
<td>descum</td>
<td>TRL</td>
<td>Asher and/or Acidhood</td>
</tr>
<tr>
<td>4</td>
<td>HCl:H2O (1:3) for 30 seconds</td>
<td>remove surface oxide</td>
<td>TRL</td>
<td>Acidhood 1</td>
</tr>
<tr>
<td>5</td>
<td>Evaporation deposition of p-type metal: 1000A Cr + 2000A Au or 100A Pt/400A Ti/100A Pt/1000A Au</td>
<td>p-type contact metal</td>
<td>TRL</td>
<td>eBeamA u or eBeamFP</td>
</tr>
<tr>
<td>6</td>
<td>sonicate in acetone</td>
<td>Liftoff</td>
<td>TRL</td>
<td>Photo-wet</td>
</tr>
<tr>
<td>7</td>
<td>Rinse with acetone, methanol, isopropanol</td>
<td>Organic clean</td>
<td>TRL</td>
<td>Photo-wet</td>
</tr>
<tr>
<td>8</td>
<td>Ash 5 min 1000W and/or 1:80 H2SO4:DI 30s</td>
<td>descum</td>
<td>TRL</td>
<td>Asher</td>
</tr>
<tr>
<td></td>
<td>Photolithography</td>
<td></td>
<td>TRL</td>
<td></td>
</tr>
<tr>
<td></td>
<td>HMDS</td>
<td></td>
<td>TRL</td>
<td>HMDS</td>
</tr>
<tr>
<td></td>
<td>Spin coat SPR700-1</td>
<td></td>
<td>TRL</td>
<td>Coater</td>
</tr>
<tr>
<td></td>
<td>Expose</td>
<td></td>
<td>TRL</td>
<td>MA6</td>
</tr>
<tr>
<td></td>
<td>Develop</td>
<td></td>
<td>TRL</td>
<td>Photo-wet</td>
</tr>
<tr>
<td></td>
<td>Hard Bake at 130C for 5 minutes to set PR for Mesa etch</td>
<td></td>
<td>TRL</td>
<td>Hotplate 1</td>
</tr>
<tr>
<td>11</td>
<td>Wet etch mesa HCl:H2O2:H2O (1:1:3) (110 nm/s approximate etch rate)</td>
<td>Etch Mesa</td>
<td>TRL</td>
<td>Acidhood 1</td>
</tr>
<tr>
<td>12</td>
<td>sonicate in acetone</td>
<td>Remove PR</td>
<td>TRL</td>
<td>Photo-wet</td>
</tr>
<tr>
<td>13</td>
<td>Rinse with acetone, methanol, isopropanol</td>
<td>Organic clean</td>
<td>TRL</td>
<td>Photo-wet</td>
</tr>
<tr>
<td>14</td>
<td>Photoresist to protect frontside during backside contact dep</td>
<td>Mask layers for mesas</td>
<td>TRL</td>
<td></td>
</tr>
<tr>
<td></td>
<td>HMDS</td>
<td></td>
<td>TRL</td>
<td>HMDS</td>
</tr>
<tr>
<td></td>
<td>Spin coat SPR700-1</td>
<td></td>
<td>TRL</td>
<td>Coater</td>
</tr>
<tr>
<td></td>
<td>Hard bake</td>
<td></td>
<td>TRL</td>
<td>MA6</td>
</tr>
<tr>
<td>15</td>
<td>1:80 H2SO4:H2O descum (30s), 1:3 HCl:H2O (30s) 1:10 HF:H2O (30s)</td>
<td>remove native oxide</td>
<td>TRL</td>
<td>Acidhood 1</td>
</tr>
</tbody>
</table>
### Appendix A: GaAsP Cell Fabrications Process

<table>
<thead>
<tr>
<th>Step</th>
<th>Process Description</th>
<th>P-Type Contact</th>
<th>TRL</th>
<th>Equipment</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>Sonicate in acetone</td>
<td>Remove PR</td>
<td>TRL</td>
<td>Photo-wet</td>
</tr>
<tr>
<td>13</td>
<td>Rinse with acetone, methanol, isopropanol</td>
<td>Organic clean</td>
<td>TRL</td>
<td>Photo-wet</td>
</tr>
<tr>
<td>14</td>
<td>Mount cells on stainless steel carrier with crystalbond wax to protect backside contact during GaAsP contact etch.</td>
<td>Mount sample</td>
<td>SEL</td>
<td>Hotplate</td>
</tr>
<tr>
<td>15</td>
<td>Etch GaAsP contact layer with 1:2:50 NH4OH:H2O2:H2O (200s - 300s)</td>
<td>Etch contact layer</td>
<td>SEL</td>
<td>AcidHoo d</td>
</tr>
<tr>
<td>16</td>
<td>Remove cells from carrier &amp; strip wax with Acetone</td>
<td></td>
<td>SEL</td>
<td>Hotplate</td>
</tr>
</tbody>
</table>