Design-Space and Scalable Technology for GaN Based Power Transistors

by

Daniel Piedra
B.S., Massachusetts Institute of Technology (2009)
M.Eng., Massachusetts Institute of Technology (2011)

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 2018

Signature redacted

Signature of Author .....
Department of Electrical Engineering and Computer Science
January 16, 2018

Signature redacted

Certified by .....
Tomás Palacios
Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Signature redacted

Accepted by.....
Leslie A Kolodziejski
Professor of Electrical Engineering and Computer Science
Chair, Department Committee on Graduate Students

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Abstract:

As silicon devices approach their intrinsic material and technological limit, there is an opportunity for alternative semiconductor materials to push the performance of electronics forward. Gallium nitride (GaN) has demonstrated very promising performance for advanced electronics, but there is still room for improvement. This thesis discusses several new transistor designs to improve the performance of GaN-based power devices as well as demonstrations of their scaling potential and integration capability with silicon. Specifically, we have developed a wide-periphery GaN fin-based high electron mobility transistor process for power switching. The process was developed with emphasis on the passivation, field plates, gate periphery scaling, and packaging. A CMOS compatible GaN processing technology on 200-mm wafers was developed and optimized, with particular attention focused on the recess etching through the wide-bandgap AlGaN barrier to reduce the contact resistance. A study of a heterogeneous integration technology to integrate GaN and Si devices was conducted. This involved an approach to monolithically integrate GaN and Si devices which used a bonded SOI wafer with a Si (111) substrate and Si (100) device layer with windows opened to access the (111) layer to selectively grow GaN. Characterization of the transistor properties in GaN windows of different sizes was performed to qualify the optimal window size for power devices in future integrated systems.

Thesis Supervisor: Tomás Palacios
Title: Professor of Electrical Engineering and Computer Science

Acknowledgements

This thesis has been a long journey and certainly one that I could not have accomplished on my own. It is a testament to all of the support I've had throughout the years. First and foremost I'd like to thank my advisor Tomás Palacios. His constant enthusiasm has been an inspiration and a source of optimism, especially in hard times. He gave me the freedom to pursue research I thought was interesting and all of the resources I needed to be successful. I'd also like to thank my committee Professor Jesús del Alamo and Professor Dave Perreault for their valuable input on this thesis as well as previous collaboration projects.

I feel very privileged to have been part of such a great research group to provide support throughout the years. Will Chung, the first member of the group, set the standard of excellence that the group grew upon. I'd like to acknowledge Bin Lu, the group's power device guru, for his mentorship, especially in my first few years. Omair Saadat was always very supportive, whether it was in the measurement lab, debugging a fab problem, or dispensing advice. Mohamed Azize provided valuable insight to all of my questions about epitaxial growth as well as a friendly, fun atmosphere. Puneet Srivastava, Tatsuya Fujishima, Amir Nourbakhsh and Jie Hu always provided interesting discussion and expert perspective from their times at IMEC and Rohm Co. and it was a pleasure to get the chance to work with them. I'm lucky to have had such amazing office-mates. Allen Hsu who was my office mate for several years, is one of the smartest, most technically proficient engineers I've ever met yet manages to supplement this with a humble, genuine, friendly personality. Lili Yu who took over the desk after Allen graduated, is one of the most determined, hard-working individuals I've met. Min Sun, Yuhao Zhang, Sameer Joglekar, Xu Zhang were fantastic group mates and reliable fab-buddies and I'm glad to have them as friends. Robert Radway, Maddy Aby, Stephanie Rennesson, Marco de Fazio, Takamichi

Sumitomo, Elison Matioli, Alex Paschoal, Dong Seup Lee, Feng Gao, Hyung Seok Lee, Benjamin Mailly, Tadahiro Imada, Han Wang, Kevin Ryu, Andrew Potter, Jose Maria Tirado, Fred Mieville, Zhihong Liu, Ahmad Zubair, Marek Hempel, Cosmi Lin, Noelia Trivino, Hiro Okumura, Elaine McVay, Nadim Chowdhury, Charles Mackin made the group a fun enjoyable place to be while also performing research. The building 39 sixth-floor residents, particularly the research groups of Prof. Akinwande, Prof. del Alamo, Prof. Antoniadis, Prof. Weinstein really made the work environment feel like a community

I had the opportunity to work with many wonderful collaborators on the various projects that make up this thesis. The Lincoln Lab group (Chang-Lee Chen, Jeff Knecht, Rich Molnar) provided very valuable insight to large scale wafer fabrication and material for my projects on 200-mm GaN. I am very grateful toward SungWon Chung and Professor Mihai Sanduleanu who designed the circuits which utilized the GaN-IC process. Dave Otten and Seungbum Lim designed and measured the power converter using our GaN power switch and were very helpful in answering all of my power converter related questions. Eyal Aklimi and Professor Ken Shepard led the initiative to try the GaN/CMOS face-to-face bonding experiments and were wonderful to work with throughout that project. Professor Akira Uedono provided his expertise on positron annihilation spectroscopy which was crucial for helping us understand material properties of GaN and dielectrics. The IBM Research group (Devendra Sadana, Ko-tao Lee, and Can Bayram) were very helpful in providing material and analysis expertise in the heterogeneous integration project. I'd also like to thank Professor Jesus Grajal and Ujwal Radhakrishna for lending support on all of my RF related problems and having the patience to answer my questions.

The work carried out in this thesis was heavily dependent on the micro/nano-fabrication facilities at MIT. I'd like to thank the staff of the Microsystems Technology Lab and Mark Mondol for their tireless effort in maintaining and supporting the fabrication tools at MIT. The administrative staff, particularly Debb Hodges-Pabon and Joe Baylon, are superstars and ensured that the day-to-day operations runs smoothly and never failed to brighten my day.

Finally, I'd like to thank my friends and family for their continued support.

Table of Contents

Chapter 1: Introduction

Since the replacement of vacuum tubes by solid-state devices, silicon based semiconductor power devices have been dominant in power electronics [1]. In spite of the excellent performance demonstrated by Si-based electronics, the relatively low critical electric field of silicon, low operating temperatures, and its low carrier mobility open the door for a new replacement material. A new switching technology that would improve the switching frequency, on-resistance, and maximum temperature is desirable, since all these metrics impact the losses and form factor of power switching devices.

Nitride semiconductors have the material characteristics needed to fabricate devices that would make an improved switching technology possible. The nitride family of semiconductors span a very large direct bandgap range, from 0.6eV in InN to 3.4eV in GaN to 6.2eV in AlN, which makes them well suited for many applications. In particular, gallium nitride (GaN) has outstanding properties for power electronics. First reported in single crystal form in 1969 by Maruska and Tietjen [2] of RCA, gallium nitride positioned itself to transform both the lighting and electronics industry.

Early difficulties with the semiconductor growth quality (particularly p-type) abated the immediate progress of GaN. In 1989, however, Amano and Akasaki's use of low-energy electron beam irradiation to decrease the resistance of Mg doped GaN films improved the quality of p-GaN enough to make a viable p-n diode [3]. This led to more widespread acceptance of the technology and paved the way for the development of the very popular green, violet, blue LED as well as the first blue semiconductor laser by Nakamura [4]. The success of the LEDs funneled consideration and research funding toward electron devices [4].

GaN for Electronic Devices

Although originally used in optoelectronic devices, GaN's wide bandgap and high critical electric field made the semiconductor promising for electrical devices as well. As shown in Table 1.1, GaN stacked up well when compared to other semiconductors often used for power electronics. Khan *et al.* reported the first observation of enhanced electron mobility in AlGaN/GaN heterojunctions [5] in 1991 which led to the high electron mobility transistor in 1993 [6]. It was this breakthrough which was important in paving the way to high- performance devices and differentiating GaN from other semiconductors to allow it carve out a niche for itself as an ideal material for high voltage, low on-resistance electronics.

Table 1.1. Comparison of material properties of Si, GaN, and SiC [6]

	Si	GaN	4H-SiC
Band Gap E_g (eV)	1.1	3.39	3.26
Breakdown Electric Field E_{br} (MV/cm)	0.3	3.3	3.0
Peak drift velocity v_{sat} (10^7 cm/s)	1.0	2.5	2.0
Electron mobility μ_n (cm^2/Vs)	1350	2000 (2 dimensional electron gas)	700
Relative dielectric constant ε	11.8	9.0	10
Johnson Figure of Merit ($E_{br}\, v_{sat}/2\pi$)	1	27.5	20
Baliga's Figure of Merit ($\varepsilon\mu E_C^3$)	1	1507	548

On-resistance and breakdown voltage are two of the most important metrics for semiconductor power swiches. When studying power devices it is useful to understand the

relationship between them. To study this, we will assume a lightly doped drift region which would support the off-state voltage as a power switch as shown in Figure 1.1.

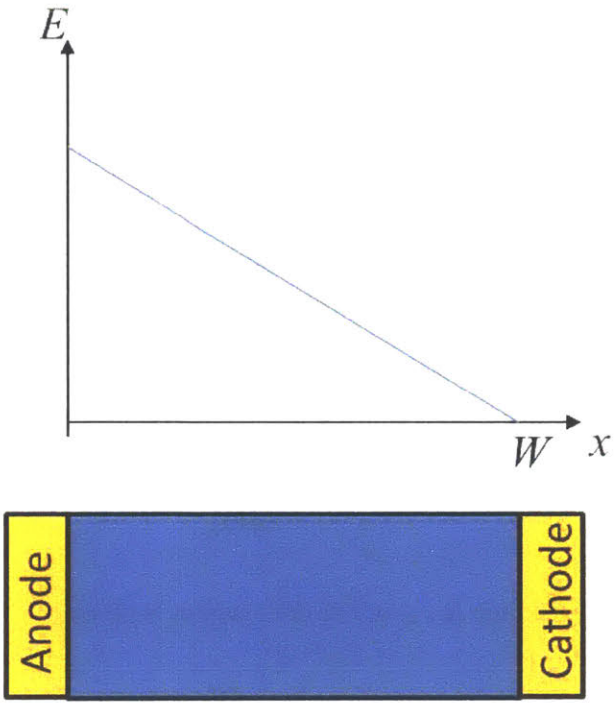

Figure 1.1. Generalized ideal lightly doped drift region and the corresponding electric field

The breakdown voltage, V_{bk}, is the voltage at which the critical electic field of the material is reached. Assuming a uniform doping of the drift region and a depletion width of W, this breakdown voltage is given by:

$$V_{bk} = \frac{E_{cr}W}{2}$$

Using **Gauss's Law** to relate the electric field to the charge in the drift region with doping N_d, and permitivity of ε_s, the breadown voltage follows as:

$$E = \int \frac{\rho}{\varepsilon} dx = \frac{qN_d W}{\varepsilon_s}$$

$$V_{bk} = \frac{qN_d W^2}{2\varepsilon}$$

The depletion width under the breakdown condition is given by:

$$W = \frac{2V_{bk}}{E_{cr}}$$

And the doping concentration in the drift region needed to reach this breakdown voltage is thus given by:

$$N_d = \frac{\varepsilon E_{cr}^2}{2qV_{bk}}$$

The specific on-resistance $R_{on,sp}$ of the drift region is given by:

$$R_{on,sp} = \frac{W}{q\mu N_d}$$

Substituting the depletion width and the doping concentration leads to:

$$R_{on,sp} = \frac{4V_{bk}^2}{\varepsilon\mu E_{cr}^3}$$

Figure 1.2 illustrates this breakdown vs. specific on-resistance realtionship for Si, SiC, and GaN.

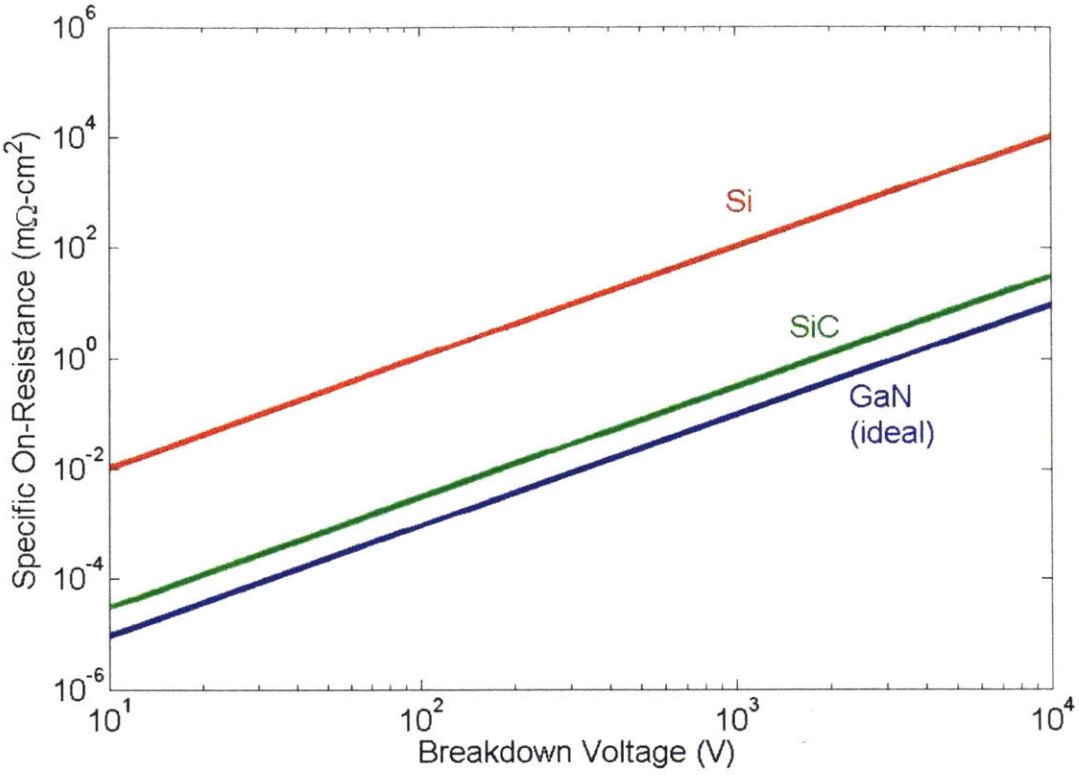

Figure 1.2. Theoretical specific on-resistance and breakdown voltage for materials used in power electronics

In addition to its intrinsic semiconductor properties, another key advantage of GaN over other wide bandgap semiconductors such as SiC, is its ability to form heterojunctions that can be utilized in heterojunction field effect transistors. In other FET devices, such as the JFET or MESFET, the charge in the conduction channel is provided by dopants which can in turn cause impurity scattering and reduce the mobility. MOSFETs avoid this dopant scattering (if the semiconductor is lightly doped) as the carriers that form the channel are induced by inversion, however the MOSFET will encounter interface roughness scattering at the Si/SiO_2 to degrade its mobility [8]. Heterostructures can be epitaxially grown to create a device that avoids these mobility degradation problems. In a heterostructure field effect transistor (HFET), the channel is

formed by the junction of two materials with different bandgaps. Traditionally, the larger bandgap material is doped and the carriers are pushed to the lower bandgap material where they are confined in a triangular quantum well at the heterointerface. This results in a device where the channel carriers are spatially separated from the doped material and have high mobility due to the lack of impurity scattering (thus the popular name high electron mobility transistor or HEMT) [9]. A common example is the AlGaAs/GaAs system, shown in Figure 1.3. In this structure, electrons originating from the doped wide bandgap AlGaAs populate the accumulation region near the interface in the undoped GaAs and are restricted by the potential energy barriers to the 2-dimensional plane perpendicular to the page. Electrons accumulated in the potential well are referred to as the 2-dimensional electron gas (2DEG) [10].

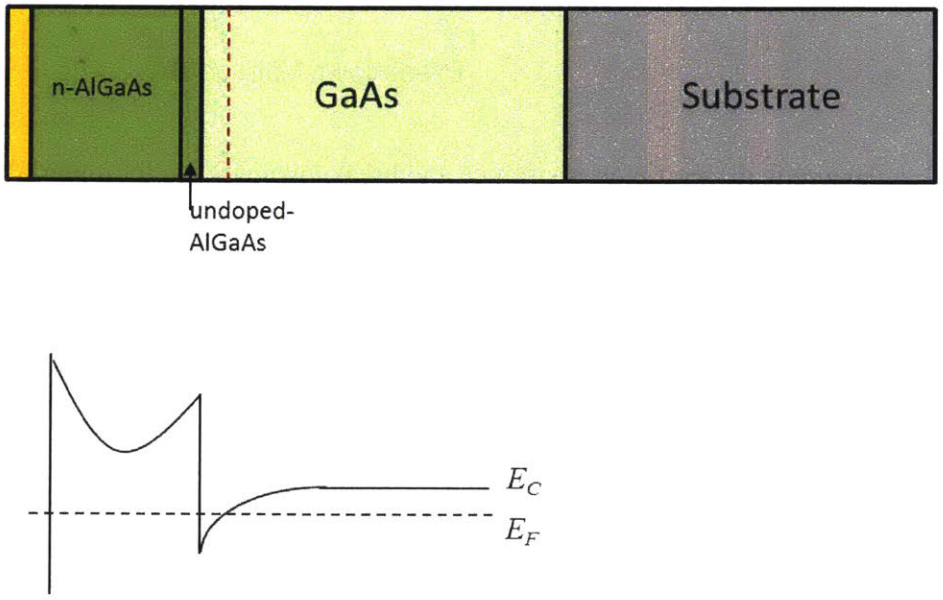

Figure 1.3. AlGaAs/GaAs High Electron Mobility Transistor (HEMT).

Unlike the AlGaAs/GaAs HEMT system described above, in which the channel electrons are provided by the intentionally doped barrier, in GaN HEMTs, the channel electrons come from polarization effects and ionized surface donor states. Nitride materials are wurtzite and thus lack inversion symmetry. This causes the material to show piezoelectric properties and polarization in the [0001] direction as shown in Figure 1.4. The polarization induced charge leads an electric field and a screening dipole, in the form of an ionized state, is formed. The origin of the 2DEG is closely tied to surface donors [12]. Figure 1.5 shows a GaN sample grown on a foreign substrate and the corresponding charge and band diagram. The internal polarization leaves $+Q_{\pi,GaN}$ and $-Q_{\pi,GaN}$ charge at the ends of the GaN layer and the built-in electric field cause the bands to bend as shown in Figure 1.5. E_{DD} denotes the energy level of surface donors. As the GaN becomes thicker, E_{DD} gets closer to the Fermi level and more surface donors become ionized contributing to the charge N^{+}_{DD}.

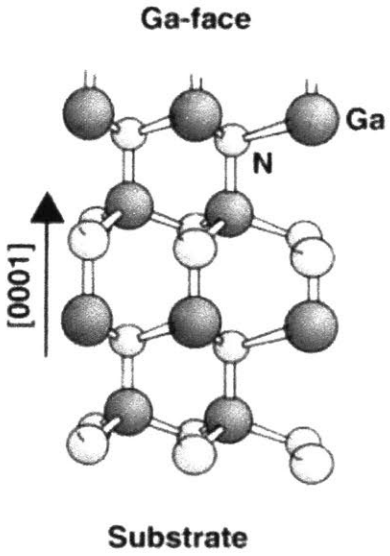

Figure 1.4. Crystal structure of gallium nitride, showing polarization in the c-plane direction [11]

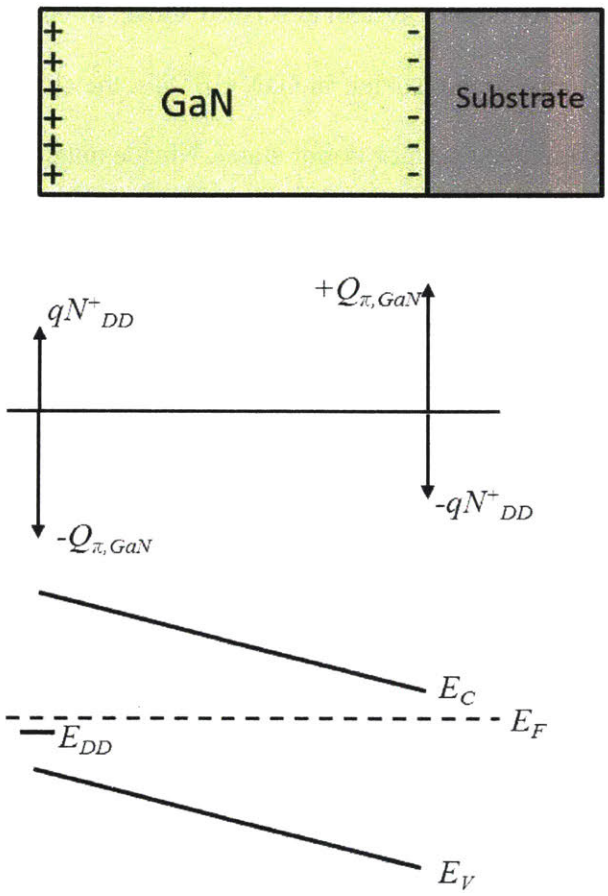

Figure 1.5. Gallium nitride grown on a foreign substrate with corresponding charge diagram and band diagram showing position of surface state.

This phenomenon can be extended to the AlGaN/GaN system, with a few modifications. Due to the lattice mismatch, the AlGaN is under tensile strain and so there is also a piezoelectric contribution to the total charge, so $Q_{\pi,AlGaN}$ encapsulates both spontaneous and piezoelectric charge. At the heterointerface, the net polarization is given by:

$$Q_{\pi,net} = Q_{\pi,AlGaN} - Q_{\pi,GaN}$$

From the band diagram (Figure 1.6), it is seen that:

$$\phi_s - \left[\frac{Q_{\pi,net} - qn_s}{\varepsilon_{AlGaN}}\right] - \frac{\Delta E_C}{q} + V_{di}^{-} = 0$$

Where V_{di}^{-} is the amount the conduction band goes below the Fermi level and is given by:

$$V_{di}^{-} = \frac{qn_s}{\varepsilon_{AlGaN}} \Delta d$$

and Δd is the centroid of the 2DEG charge distribution. Solving for n_s gives:

$$n_s = \frac{Q_{\pi,net} d_{AlGaN}}{q(d_{AlGaN} + \Delta d)} - \frac{\varepsilon_{AlGaN}}{q^2(d_{AlGaN} + \Delta d)} [q\phi_s - \Delta E_C]$$

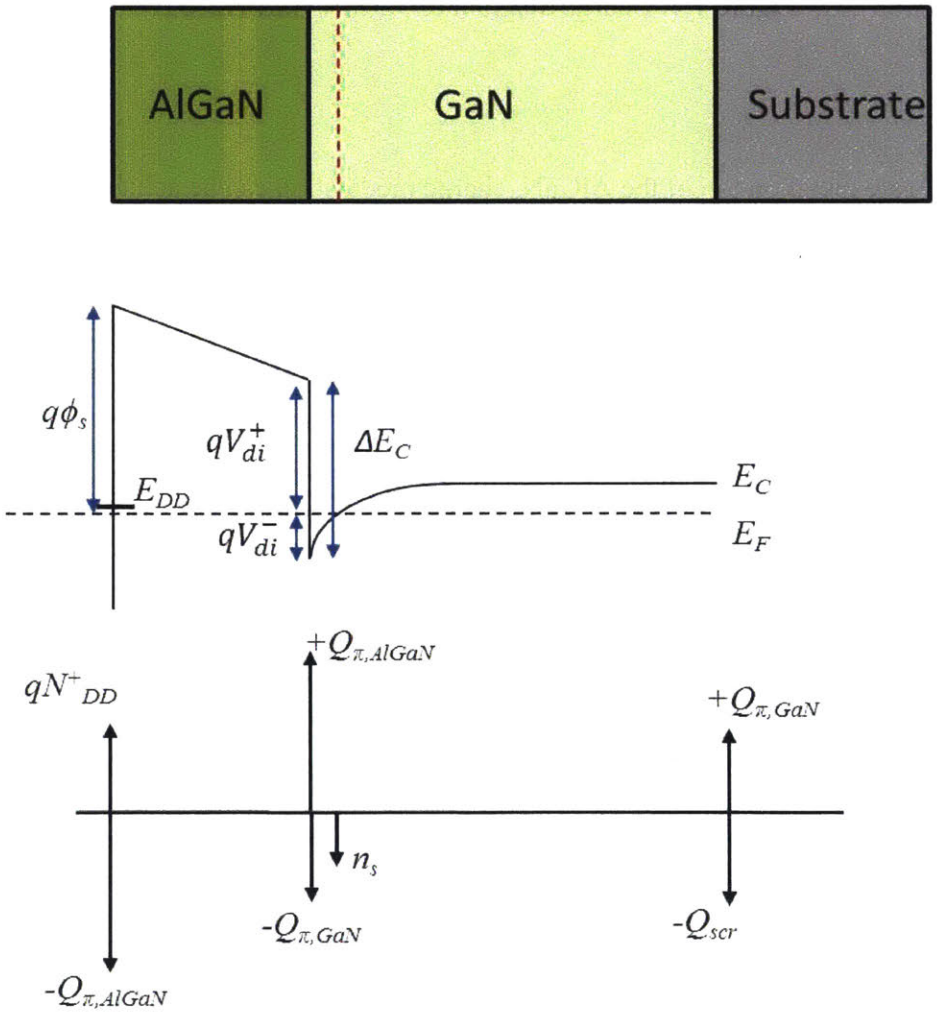

Figure 1.6. Band diagram of AlGaN/GaN HEMT.

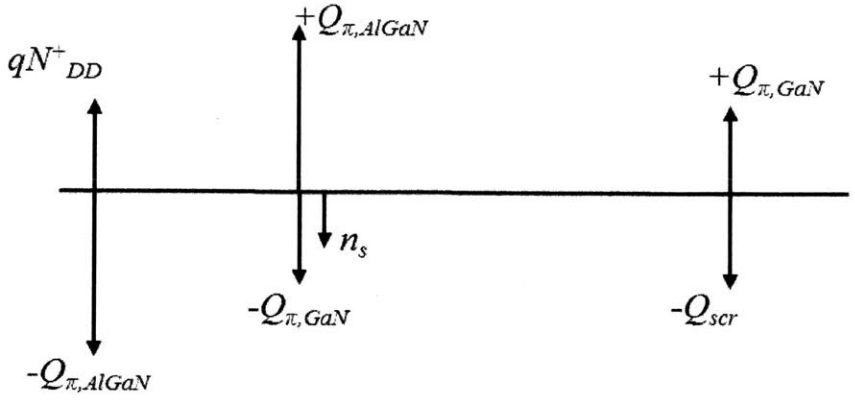

Figure 1.7. Charge diagram of AlGaN/GaN HEMT.

By placing a gate metal on top of the AlGaN, charge modulation can be achieved. The surface potential ϕ_s is then replaced by potential barrier $\phi_b - V_G$.

$$n_s(V_G) = \frac{Q_{\pi,net} d_{AlGaN}}{q(d_{AlGaN} + \Delta d)} + \frac{\varepsilon_{AlGaN}}{q^2(d_{AlGaN} + \Delta d)}[qV_{GS} - q\phi_B + \Delta E_C]$$

As can be seen, the charge density in the HEMT channel is influenced by the AlGaN thickness and the net polarization. Very high charge densities on the order of $2 \times 10^{13} cm^{-2}$ can be formed in this system [12].

Power Switch Operation

As discussed in the preceding sections, GaN has a high critical electric field, which maximizes the breakdown voltage for a given device dimensions. This, combined with the excellent transport properties of this material and the high carrier density possible at the AlGaN/GaN heterointerface, leads to excellent power transistors, as it will be discussed below.

An ideal power switch should block voltage with no leakage current in the off-state and conduct current with no resistance in the on-state. However, real power switches cannot sustain indefinitely high blocking voltage in the off state, they exhibit non-negligible leakage current, and have some non-zero resistance in the on-state as pictured in Figure 1.8.

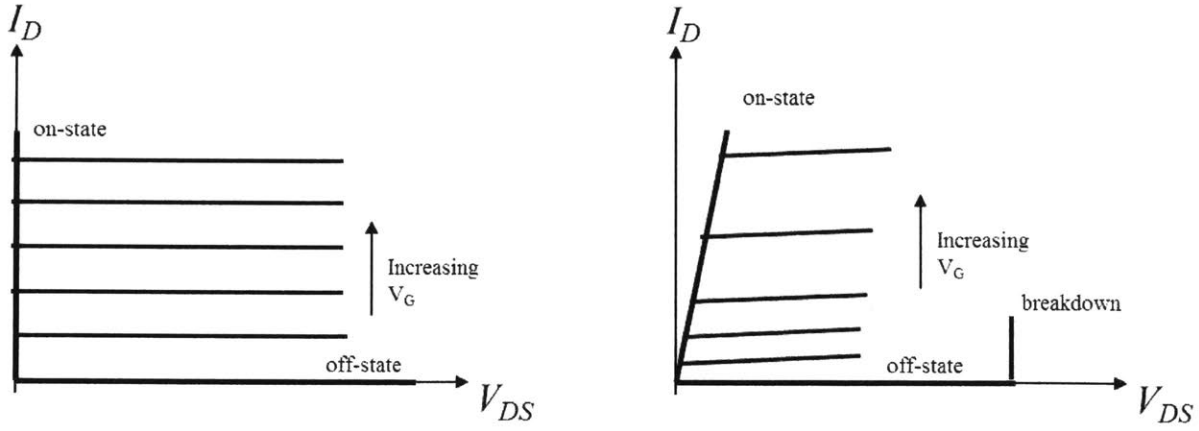

Figure 1.8. Characteristics of ideal transistor power switch and typical power switch

The chief contributor to the total on resistance in medium and high voltage transistors is the resistance of the 2DEG channel:

$$R_{2DEG} = \frac{L_{2DEG}}{q\mu_{2DEG}N_{2DEG}W_{2DEG}}$$

The access (ungated) regions of the transistor can have different mobility and carrier concentration than the gated region, so the two are written separately:

$$R_{DS(on)} = R_{2DEG} + R_{2DEG(gate)} + 2R_C$$

This transistor on-resistance will contribute to conduction losses:

$$P_{cond,FET} \approx i_{sw,rms}^2 R_{DS(on)}$$

GaN's high critical electric field should give it high blocking voltage for a small device dimension (and thus reduced cost), and the combination of this small dimensions with the high charge density and high mobility in the 2DEG give it low resistance leading to low FET conduction losses.

A second loss mechanism appears in these transistors under switching operation. For example, when operating the transistor in a hard-switching converter, there are instances in the switching transitions where there are both voltage across and current through the drain-source of the transistor, leading to switching loss. For example, in the buck converter in Figure 1.9:

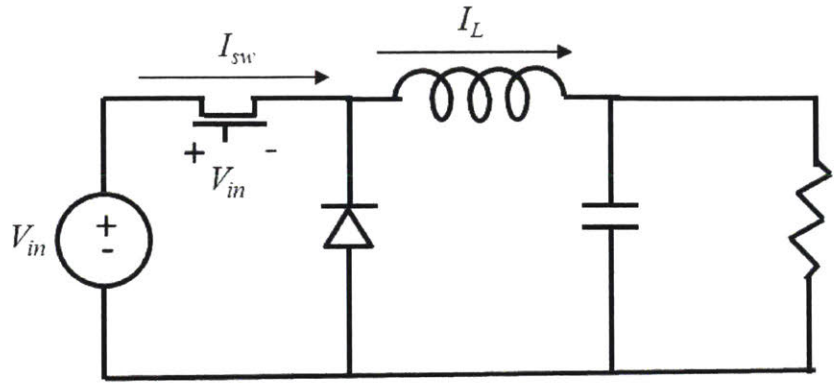

Figure 1.9. Example of buck converter used in hard-switching configuration.

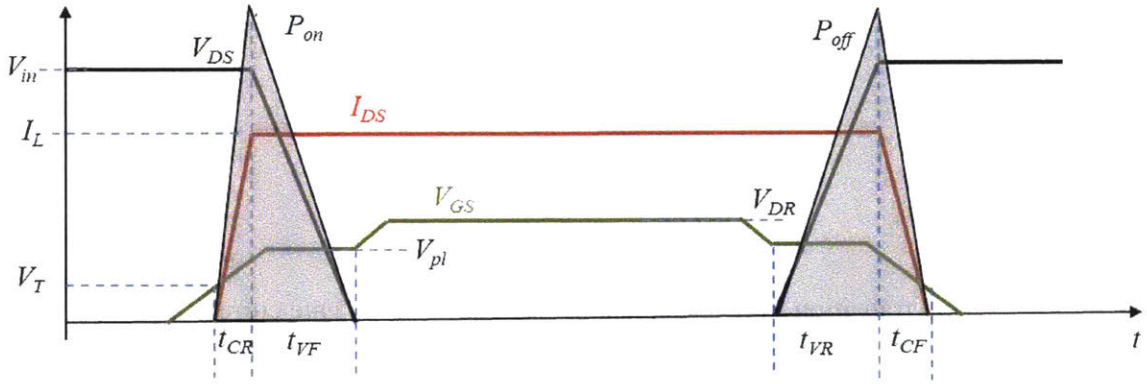

Figure 1.10. Waveforms of current and voltage in hard-switching buck converter [13].

The switching loss is the sum of the voltage transition loss P_{Vt} and the current transition loss P_{Ct}.

$$P_{sw,FET} = P_{Vt} + P_{Ct} = \frac{1}{2} V_{in} I_L (t_{VR} + t_{VF}) f_{sw} + \frac{1}{2} V_{in} I_L (t_{CR} + t_{CF}) f_{sw}$$

The switching commutation times t_{xR} and t_{xF} are given by the gate charge.

$$P_{Vt} = \frac{V_{in} I_L}{2} (t_{VR} + t_{VF}) f_{sw} = \frac{V_{in} I_L}{2} \left(\frac{Q_{GD}}{I_{G,VF}} + \frac{Q_{GD}}{I_{G,VR}} \right) f_{sw}$$

During the voltage fall transition time t_{VF}, as the device turns on, the gate current $I_{G,VF}$ is:

$$I_{G,VF} = \frac{V_{DR} - V_{pl}}{R_{G,on}}$$

During the voltage rise transition time t_{VR}, as the device turns on, the gate current $I_{G,VR}$ is:

$$I_{G,VR} = \frac{V_{pl}}{R_{G,off}}$$

The switching commutation times t_{CR} and t_{CF} are given by the gate charge.

$$P_{Ct} = \frac{V_{in}I_L}{2}(t_{CR} + t_{CF})f_{sw} = \frac{V_{in}I_L}{2}\left(\frac{Q_{GS}}{I_{G,CF}} + \frac{Q_{GS}}{I_{G,CR}}\right)f_{sw}$$

During the current rise transition time t_{CR}, as the device turns on, the gate current $I_{G,CR}$ is:

$$I_{G,CR} = \frac{V_{DR} - \left(\frac{V_{pl} + V_T}{2}\right)}{R_{G,on}}$$

During the current fall transition time t_{CF}, as the device turns on, the gate current $I_{G,CF}$ is:

$$I_{G,CF} = \frac{\left(\frac{V_{pl} + V_T}{2}\right)}{R_{G,off}}$$

$$P_{on} = P_{Vt} + P_{Ct} = \frac{V_{in}I_L f_{sw} R_{G,off}}{2}\left[\frac{Q_{GD}}{V_{pl}} + \frac{Q_{GS2}}{V_{DR} - \left(\frac{V_{pl} + V_T}{2}\right)}\right]$$

$$P_{off} = P_{Vt} + P_{Ct} = \frac{V_{in}I_L f_{sw} R_{G,off}}{2}\left[\frac{Q_{GD}}{V_{pl}} + \frac{Q_{GS2}}{\left(\frac{V_{pl} + V_T}{2}\right)}\right]$$

Thus, the lower gate charge Q_{GD} and Q_{GS} in GaN result in smaller switching loss when compared to Si [13].

Challenges of GaN HEMTs and Scope of Thesis

Although GaN HEMTs hold much promise as a power switching technology, they still face some important key challenges. This thesis attempts to explore and overcome some of those challenges.

As seen in the discussion of the formation of HEMTs above, GaN HEMTs are intrinsically depletion mode devices. The channel (2DEG) is induced by the accumulation of electrons at the AlGaN/GaN heterojunction through spontaneous polarization, not by the gate induced inversion layer as in a Si MOSFET. Therefore, typical GaN devices will conduct with no gate voltage and require a negative gate voltage to turn off the channel. These depletion mode transistors are not the preferred choice for power switching applications, so the ability to control and increase the threshold voltage is desirable. Chapter 2 discusses a threshold voltage control technology, the development of a wide-periphery transistor process, and the use of these to demonstrate state-of-the-art power switch transistors for high frequency DC-DC converters. Chapter 3 discusses the use of the technologies demonstrated in Chapter 2 in other circuits as well as extensions of the technology for use in RF GaN HEMTs and fabrication of GaN integrated circuits.

Most early GaN research has been on small wafers and using non-CMOS compatible processes. While this is fine for research and small scale manufacturing, it is unsuitable for larger markets. Chapter 4 will discuss the development of a CMOS compatible GaN process performed for large diameter 200 mm GaN on silicon wafers.

While GaN's strength is power switches and RF amplifiers, it cannot compete with Si CMOS technology in building logic or memory systems. Chapter 5 will discuss the monolithic, heterogeneous integration of GaN with Si.

Chapter 6 will conclude and address future work.

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Chapter 2: Gallium Nitride Power Switch Development

Gallium nitride's material properties have led to large interest in its use for power electronics applications. Its high critical electric field and high mobility give it the potential for an impressive switching device with large blocking voltage and low on-resistance.

However, for wider adoption of GaN in the power switching field, several issues need to be resolved. First, typical AlGaN/GaN HEMTs are normally-on (depletion mode) devices. Such devices are undesirable for power switching applications as they add complexity due to the negative power supply needed to turn off the device as well as safety and reliability concerns.

To make the devices normally-off, additional processing steps or circuit techniques are needed. A common approach to make enhancement more devices is to use a p-type gate injection transistor structure [1]. In this approach, a p-type AlGaN (or GaN) cap is grown on top of gate region of the standard AlGaN/GaN HEMT structure, which increases the potential at the channel and deplets the 2DEG under the gate causing the structure to be off with zero gate bias as shown in Figure 2.1. The disadvantage of this approach is the increased epitaxial growth complexity, time, and cost compared to conventional AlGaN/GaN HEMTs.

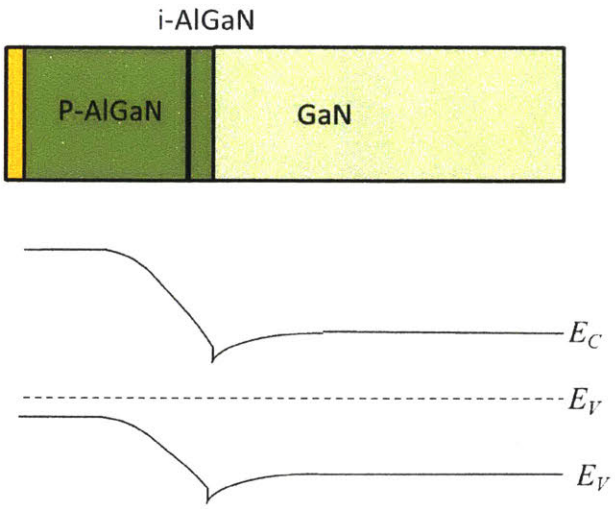


Figure 2.1. Bandgap for p-AlGaN enhancement mode HEMT

Several groups [2, 3, 4] have demonstrated normally-off devices by implanting fluorine or hydrogen ions under the gate region to deplete the channel electrons as shown in Figure 2.2. Incorporated fluoride ions provide negative charge in the AlGaN barrier to deplete channel electrons and shift the threshold voltage. At high enough fluoride concentrations, the normally depletion mode devices can then become enhancement mode. Although fluorine-implantation is a very simple way to make e-mode devices, the threshold voltage obtained through this technology has been shown to shift negative at elevated temperatures [5] and high gate forward voltage [6].

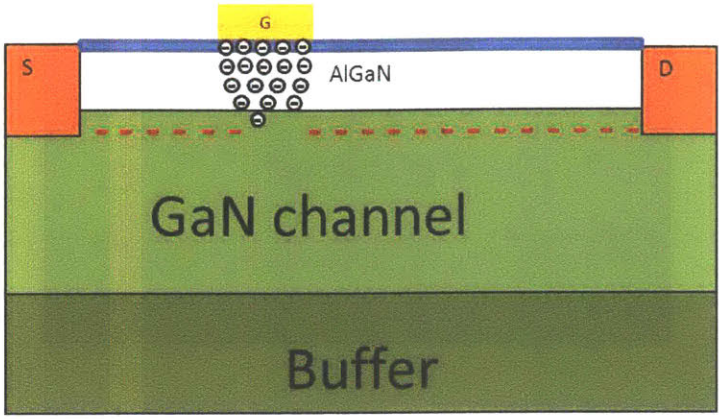


Figure 2.2. Fluorine implantation for enhancement mode operation

Gate recess technology is promising as it involves a physical removal of the barrier material which has a direct impact on the electron concentration at the AlGaN/GaN heterointerface. This method should also be more stable than the case of fluorine implantation, and the epitaxial structure is simpler than in the case of the p-GaN gate [7]. However, the intricacies involved in the patterning and etching of the recess can cause addition difficulties. As there are not wet etching chemistry available to etch the AlGaN barrier, a plasma dry etching process is needed. This dry etching imparts damage on the AlGaN/GaN reducing the carrier mobility [8] and increasing side wall leakage [9]. Furthemore, since the recessed part of the channel is not a HEMT (it lacks the AlGaN/GaN heterojunction that provides the 2DEG) it does not have the same high mobility as the unrecessed parts of the channel and thus represents a point for high resistance. To minimize these negative effects, it is desirable to make this recessed area as small as possible. In [7], the authors used electron-beam lithography to pattern a 95 nm gate recess, and were able to achieve enhancement mode operation with a V_T of 2.9V. However, these devices had high off-state leakage current due to a parallel leakage path under the e-mode channel.

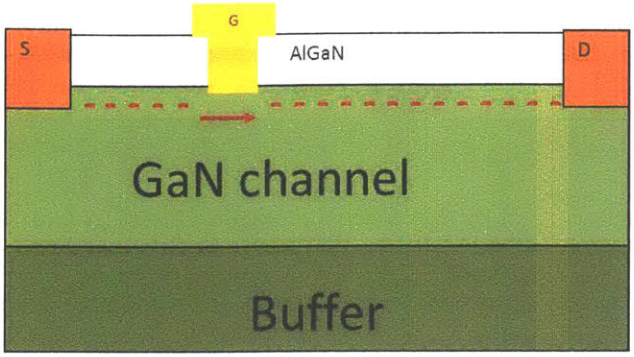


Figure 2.3. AlGaN barrier gate recess for enhancement mode operation. A narrow gate recess, while desirable to limit the damage done by plasma etching, can also lead to electron punch through and increased, uncontrollable off-state leakage.

A promising approach that addresses the normally-on problem as well as the high leakage and short channel effects commonly associated with a submicron gate recess is the tri-gate MISFET technology [10]. Improved channel confinement, brought about through the sidewall gates, lowers short-channel effects the off-state leakage current to acceptable levels.

While the devices presented in [7] represent a breakthrough in gallium nitride processing technology, they have some important limitations. First, these transistors were relatively small (W_G=100 μm). This is acceptable as a proof a concept of the tri-gate technology, but not as a power switch in an actual circuit that requires low resistance and high current. Second the devices were not properly passivated. Vetury et al [11] shows that lack of proper passivation will cause GaN HEMTs to suffer from significant current collapse and would unable to provide enough current in high frequency, high voltage switching scenarios. And third, they did not have any field plates. Field plate have been shown to be effective in increasing the breakdown voltage of the device [12], controlling current collapse [13], and improving reliability [14].

The goal of this chapter is to take an immature, early technology such as the tri-gate GaN technology, and improve it to the point where its potential can be benchmarked in real power electronic circuits. To do this, we developed a multi-finger technology, optimized for high voltage operation and developed new packaging techniques for these very high frequency devices. This chapter describes these efforts

Wide-periphery GaN Transistors

Large amounts of current flow through the power devices required in power switching circuits, a target application space for our devices. To accommodate such a high current level, large transistors with very long gate widths (on the order of tens to hundreds of millimeters) are necessary.

However, transistors of such a large size, while ideal for high voltage situations, represent an obvious departure from the typical dimensions used in GaN transistors for RF amplifier applications. Circuits composed of several of these twenty-millimeter gate width transistors would be massive compared to circuits built with the 150-micrometer gate width RF counterparts. Furthermore, the gate resistance present in such a large transistor would degrade the frequency performance of the device. The ideal power transistor would combine the best of both worlds and fit a large gate width into a microscopic package. Multi-finger transistor technology could be used to fabricate micrometer scale gallium nitride transistors that have the advantages of long gate widths. The essence of the idea is to fabricate a linear structure with alternating separate source/drain pads. A single gate is intertwined between the separate source and drain pads, giving a structure resembling traditional transistors. This approach provides the

long gate width required for power electronics, but since the gate is intertwined between the separate sources and drains (rather than laid out in a single straight line), space will be conserved. The completed multi-finger devices will have the equivalent gate width of much larger devices, but occupy a smaller area, as seen in Figure 2.4. This structure, although common in commercial devices, has never been demonstrated in tri-gate structures like the ones described in this thesis.

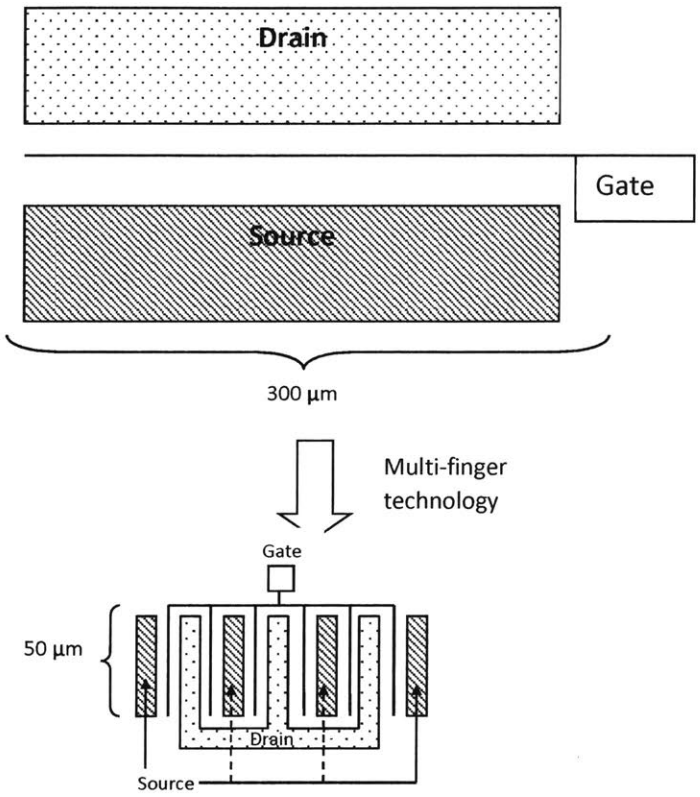


Figure 2.4. The Advantage of Multi-finger devices. In the figure above, the transistors have the same gate width, but the multi-finger device is more compact (6 fingers of 50µm each).

Process Flow for GaN HEMT Wide-periphery Devices

Device isolation

The devices studied in this work were processed on an AlGaN/GaN wafer grown by MOCVD on a 6-inch Si substrate. The epitaxial structure consisted of a 3-nm GaN cap layer/18-nm $Al_{0.26}Ga_{0.74}N$ barrier/1.2 μm GaN channel/2.8 μm AlN/GaN buffer.

The first step in fabricating the GaN HEMTs is defining the regions of the AlGaN/GaN which will contain the device, isolating the areas in-between. As the AlGaN/GaN HEMT has a normally-on 2DEG, there is thus a conducting channel everywhere that needs to be eliminated to isolate individual devices. Inadequate device isolation could lead to leakage effects between devices and inability to turn device off. Ion implantation to damage the crystal can be used, but mesa dry etching was done for this process.

Mesa isolation was done first to avoid photoresist problems caused by plasma etching. Plasma in the etcher made the masking resist insoluble to acetone, and thus very difficult to remove. Neither acetone nor heated *N*-Methyl-2-pyrrolidone (NMP) provided a reliable method of removing resist. Exposure to oxygen plasma for 15 minutes successfully removed the photoresist from the sample. However, prolonged time periods in oxygen plasma could damage any metal resulting in poor device performance. Performing mesa isolation first gives the freedom to expose to oxygen plasma since there is not yet any deposited metal on the sample. After patterning the mesa, etching was performed in an inductively coupled plasma tool with Cl_2/BCl_3 etching chemistry. An etching depth of ~120 nm was etched to ensure proper device isolation.

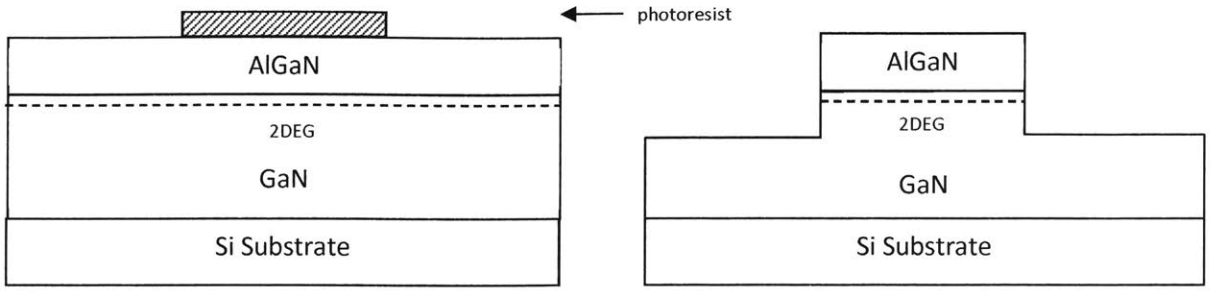


Figure 2.5. Mesa Isolation. After etching, area not protected by photoresist is etched away creating electrical isolation between devices by cutting off the 2DEG

Source/drain contacts

One of the most critical processing steps for any electronic device is the ohmic contacts. An ideal ohmic contact should be able to provide the required current with a small voltage drop that is negligible compared to the voltage drops in the active areas of the device [15]. Poor ohmic contacts will drop excessive voltage across them and become sources of resistive loss. In GaN HEMTs, an unsatisfactory ohmic contact technology can negate the advantages of the low resistance channel.

Generally, a metal-semiconductor junction requires a high density of states at the interface to push the Fermi level of the semiconductor very close to the conduction band. By increasing the doping level in the junction, the depletion region decreases and if the doping level is high enough, the depletion region can be thinned to an extent that it is on the order of a de Broglie wave length [16]. At this scale, quantum tunneling becomes possible and is the mechanism for ohmic contacts.

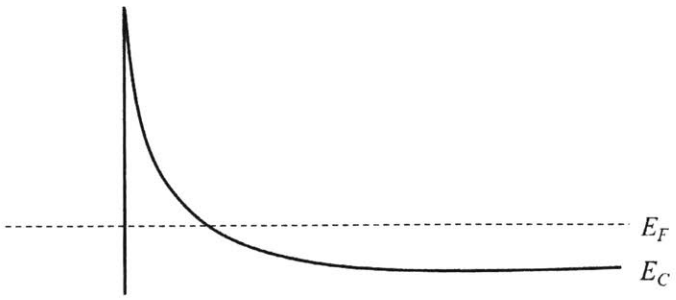


Figure 2.6. Degenerately doped n-type semiconductor, ideal for ohmic contacts

In Si, the high doping levels required for ohmic contacts are provided by doping mechanisms such as implantation. However, the wide-bandgap of GaN makes doping through this technology difficult. The activation temperature of implanted dopants, such as Si, in GaN is above 1000°C and exposure to these temperatures can damage the heterointerface and degrade the mobility of GaN transistors [17]. N-doped GaN can be selectively regrown in the ohmic contacts and annealed at lower temperatures (600-700°C) to achieve ohmic contacts [18]. However, this necessitates the use of MOCVD or MBE during the device process and in the interest of maintaining process simplicity, an alternative method was used.

As opposed to intentionally doping the GaN through the methods mentioned, interfacial layer reaction chemistry can be used to dope the material to get ohmic contacts. Annealing Ti/Al/Ni/Au based contacts has proven to be a reliable way to employ this. The titanium forms TiN at the AlGaN surface, thus leaving nitrogen vacancies in the AlGaN. These nitrogen vacancies act as donors to increase the carrier concentration, decrease the depletion width and enable the tunneling which makes a good ohmic contact [19]. Aluminum alloys with the Ti to prevent an overly aggressive Ti-GaN reaction which could lead to formation of voids (thus the Ti/Al ratio is rather sensitive) [20]. Gold is added as a high conductivity layer and to reduce the surface oxidation, while the nickel is placed under it to act as a diffusion barrier to prevent Au

from reacting with the Al and forming a high resistance compound. It has been hypothesized that a spike path is facilitated by Au. Gold in the contacts are responsible for the contact roughness, providing a preferential contact path between the 2DEG and the metal stack [21].

In this process, the ohmic contacts were deposited by lift-off. The contacts were patterned by spin coating AZ5214 image reversal photoresist on the sample and prebaking at 80°C on a hotplate to cure the resist. An initial 8 second exposure (with the ohmic contacts mask, Figure 14) established the pattern on the sample and a 110° C reversal bake crosslinks the exposed areas of photoresist, making those areas inert to developer. The sample then underwent an 80 second flood exposure (without a mask), which makes all areas that are not crosslinked soluble to developer. The sample was then agitated in AZ422 developer to dissolve all soluble areas of photoresist (where ohmic contact metal will ultimately be). The metal stack of 200Å Ti, 1000 Å Al, 250Å Ni, 500 Å Au was deposited by electron beam evaporation. The sample was then placed in acetone to dissolve the underlying photoresist and liftoff the metal in all areas around the contact areas.

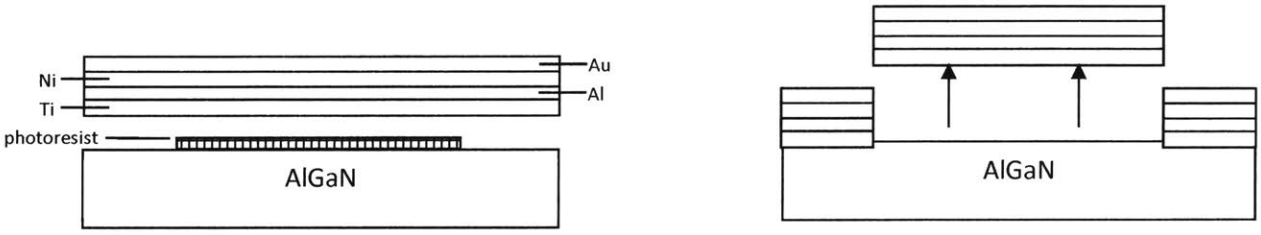


Figure 2.7. Liftoff of ohmic contact metals. The e-beam evaporation deposits a uniform layer of metal on the entire sample. Photoresist dissolves in acetone, lifting off metals in the regions around the contacts. Figure is not drawn to scale.

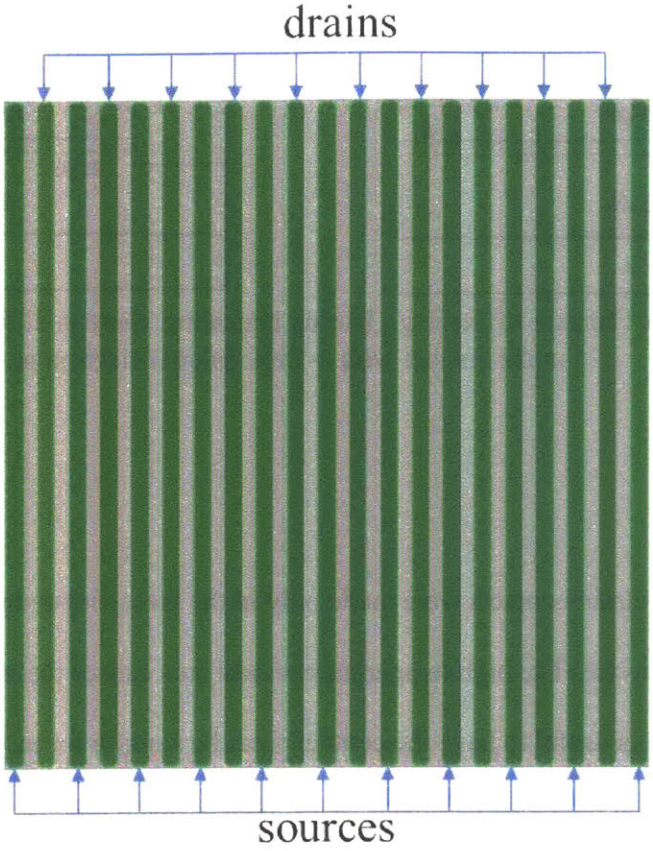


Figure 2.8. Source/drain ohmic contact multi-finger layout

The sample then underwent a rapid thermal anneal at 870°C for 30 seconds in a nitrogen atmosphere. High temperature annealing caused the metal alloy to vertically diffuse into the surface. The sample was then cleaned with acetone, isopropyl, deionized water and baked at 130° C to evaporate solvents. The resulting ohmic contacts had a contact resistance of 0.3 Ωmm, as determined by TLM characterization.

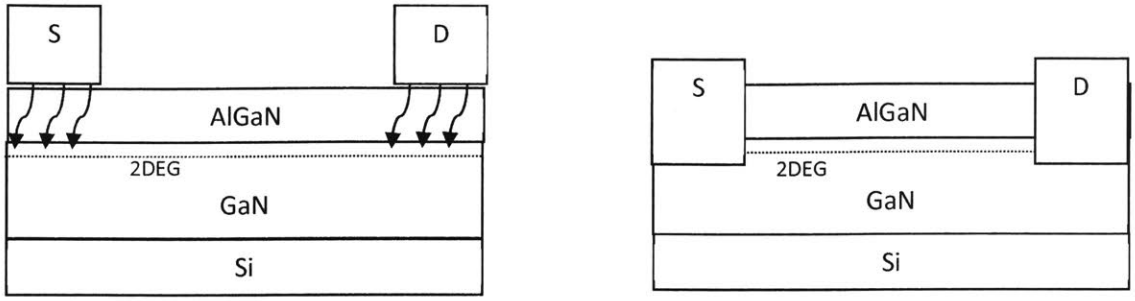


Figure 2.9. Rapid Thermal Annealing. During annealing, there is diffusion of ohmic metals to make contact with 2-Dimensional electron gas

Pad metallization

The source-drain contacts were made only in the mesa isolated regions which make the active part of the device. The high temperature anneal step causes the metal stack to become rough. However, it is useful to have the contact areas be smooth for more uniform probing and contact to upper level interconnect metals. Also, thicker metal reduces the resistance and increases the amount of current each finger can carry before burning out. It is beneficial to add this additional metal after the deposition and anneal of the ohmic metal so as to not have to modify the base ohmic contact metal stack. Thus a post-ohmic pad (Figure 2.10) metallization is patterned in AZ5214 resist, deposited by electron beam lithography (15 nm Ti, 300 nm Au), and lifted off.

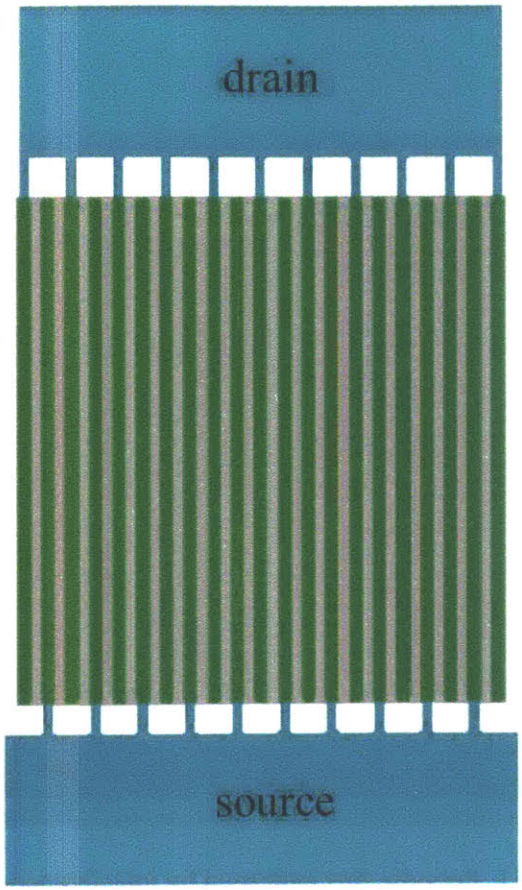


Figure 2.10. Pad Metallization patterns

Trigate/Gate-recess/gate/gate oxide

Low leakage and threshold voltage control are important requirements of power electronic switches. To achieve these requirements in our fabricated devices, tri-gate recessed channel technology [10] with gate dielectric was implemented. First a 220 nm layer of SiO_2 was deposited by plasma enhanced chemical vapor deposition over the entire sample to act as a hard mask for subsequent etching steps. Interference lithography was performed to pattern a periodic grating over the entire sample surface in PFi-88 i-line resist with a period of 400 nm. The sample was etched in CF_4 based plasma with the intention of thinning the oxide hard mask from 220 nm to 40 nm, resulting in a structure as shown in Figure 2.11.

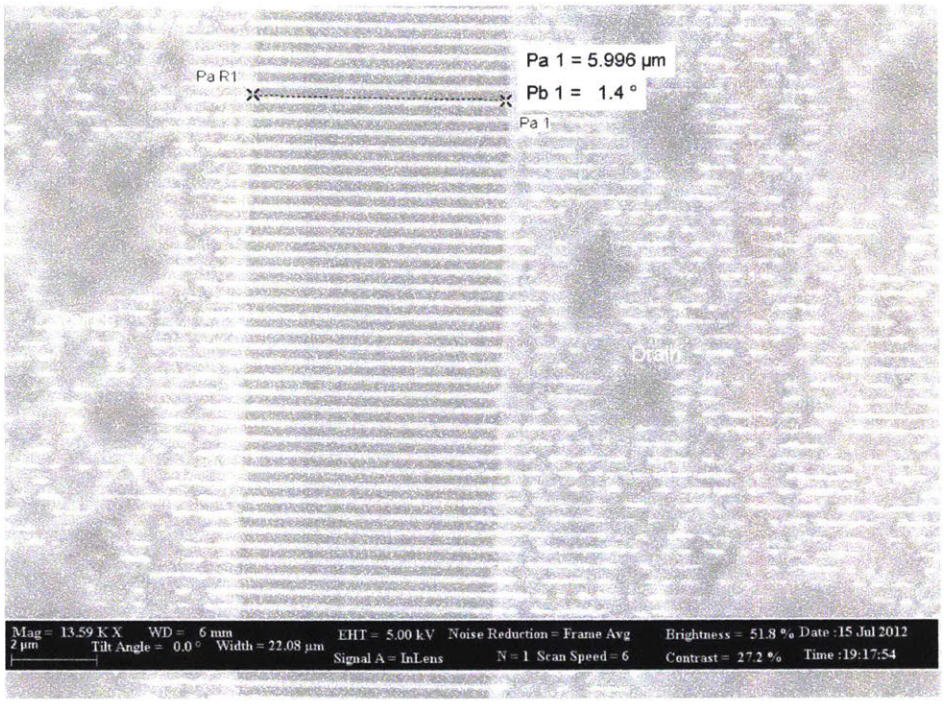


Figure 2.11. Periodic fins patterned by interference lithography.

Next, electron beam lithography was used to pattern a 670-nm-long strip between the source and drain to demarcate the trigate region. CF_4 plasma was used to etch the remaining 40 nm in this area, then a BCl_3/Cl_2 based plasma was used to etch the AlGaN barrier and some of the GaN channel not protected by the oxide hard mask. The resist on the sample was removed through a solvent clean and the oxide hard mask was stripped with a HF based buffered oxide etch solution. Finally, electron beam lithography was used to pattern a 160 nm line down the center of the trigate region and the BCl_3/Cl_2 based plasma etched the AlGaN barrier in this line. The purpose of the removal of the AlGaN barrier in this line was to shift the threshold voltage positive.

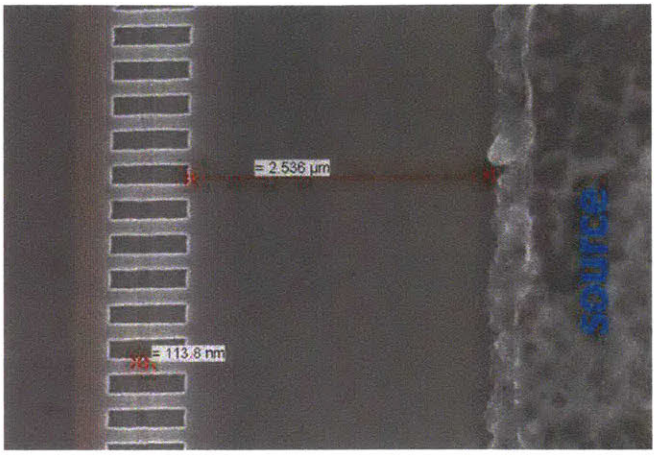


Figure 2.12. Tri-gate pattern and submicron barrier recess shown in relation to the source contact.

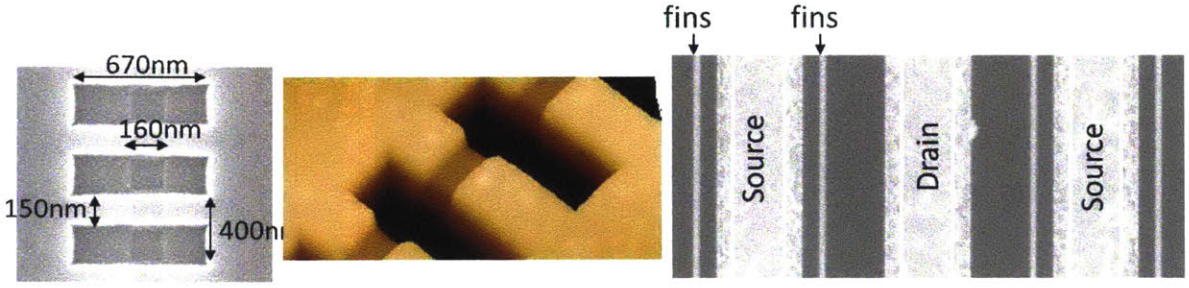


Figure 2.13. Tri-gate, e-mode recess in multifinger GaN HEMT

To reduce the gate leakage in the device, a gate dielectric is needed. A layer of 18 nm SiO_2 was deposited by atomic layer deposition (ALD). Lift-off of an e-beam evaporated stack of Ni/Au/Ni on patterns defined by photolithography was done to make the gate electrodes.

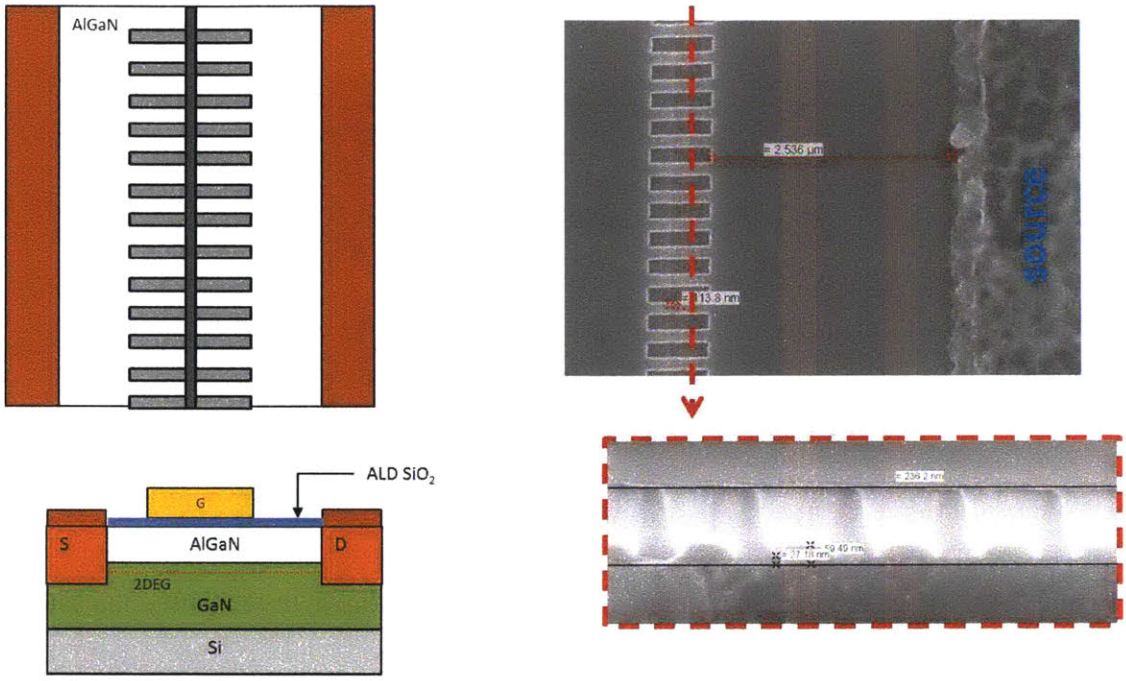


Figure 2.14. Diagram of tri-gate in channel with gate recess and integrated gate dielectric

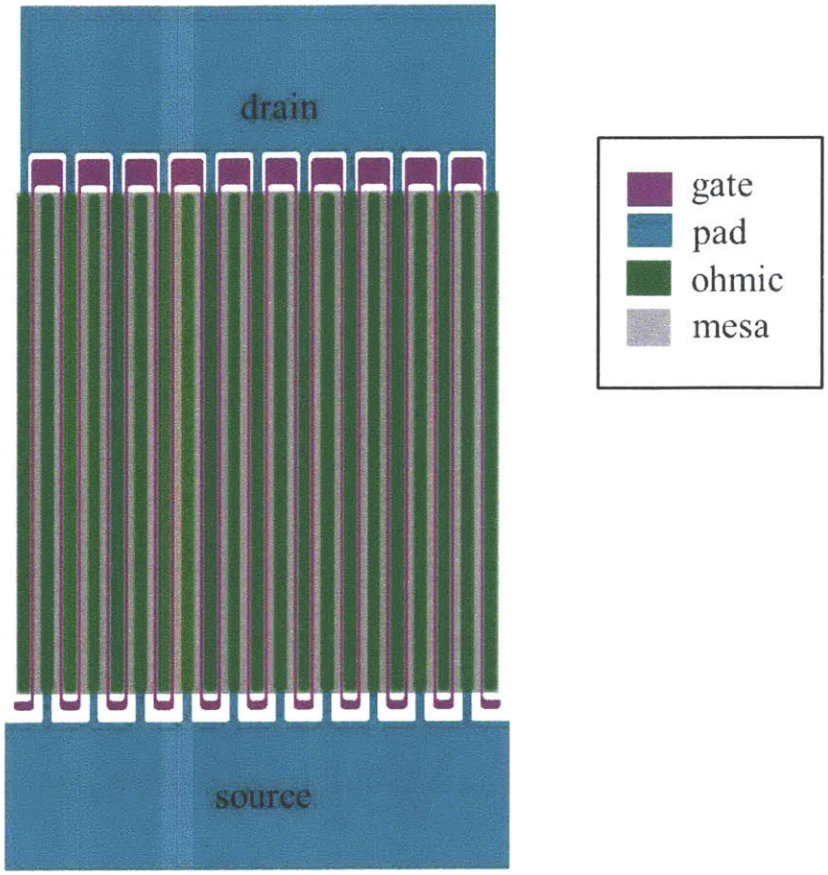


Figure 2.15. Gate pattern shown in multifinger wide periphery device.

Surface passivation

At this point the in the fabrication process, the devices are similar to those in [10]. However, these devices are still missing surface passivation. As discussed in chapter 1, since the surface states are responsible for the 2DEG channel, unwanted surface effects can greatly impair the performance of the device. Negative charge trapped on the surface can change the surface potential and deplete channel electrons. This can be explained by conceptualizing the negative charge on the surface as a "virtual gate." Like a physical gate, the virtual gate can modulate the drain current but unlike the physical gate, the virtual gate is controlled by the presence and

amount of trapped charge at the surface rather than by an applied potential. Furthermore, the frequency performance (i.e. switching speed) of the virtual gate is significantly slower than that of the physical gate as it is governed by the time constants of the detrapping process (which is dependent on the energy level of the trap). Larger amounts of charge are trapped at deep-level traps (with longer time constants) by higher electric fields that are present in the high voltage off-state of the device. During the off-state, surface traps are populated by electrons from the gate thus forming the virtual gate. When the device is quickly transitioned to the low voltage on-state, the virtual gate cannot respond fast enough leading to the channel remaining partially depleted even though the device is biased on. This manifests itself by a drop in the current and an increase in the on-resistance, hence the names "current-collapse" and "dynamic on-resistance". Practically, these trapping effects are noticed by the reduction output power and power added efficiency of a GaN amplifier at higher frequencies due to a drop in the current and increase in the knee voltage. [22].

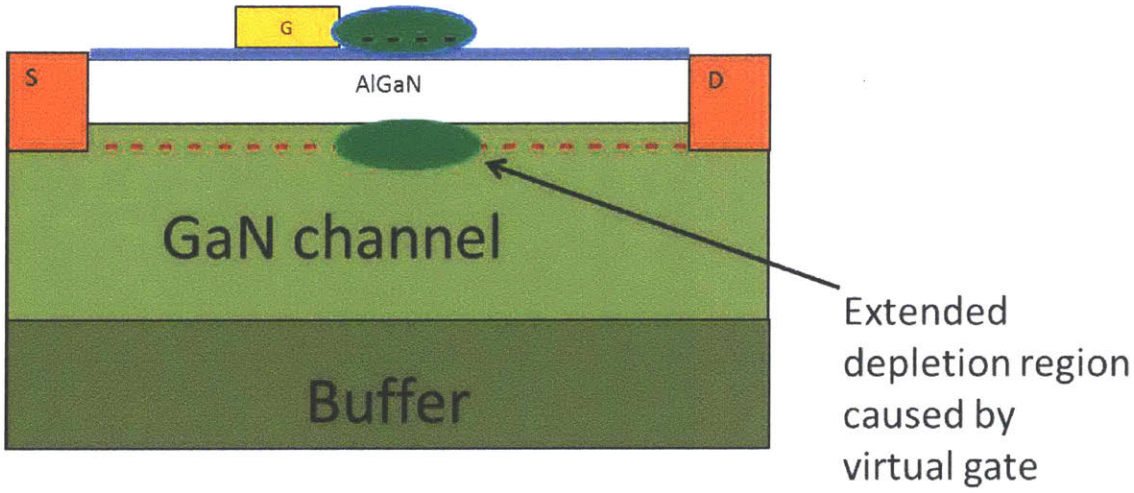


Figure 2.16. Surface traps causing a "virtual gate" effect that depletes the 2DEG

While unpassivated devices exhibit significant dynamic on-resistance, surface passivation has proven effective in reducing it. [23, 24]. It is proposed that surface passivation impedes the formation of a virtual gate by burying the surface donors which are responsible for the 2DEG and blocking them from electrons coming from the gate metal [11]. It is also hypothesized that ambient moisture in the atmosphere may contribute to the surface traps and a passivation layer blocks this [25].

A common way of characterizing the extent of the current collapse is through pulsed-IV measurements [26]. Using a dual pulsed (drain and gate pulsers) system such as the Auriga AU4750, we are able to quickly and precisely switch the transistor between different set bias states and measure the output current at those states. For the current collapse measurement most relevant for power switching situations, the device is biased at a high voltage off-state point (called the quiescent point) and held there for a length of time (usually 99-99.9% of the period). During this high-voltage state, there is a high electric field which can exacerbate the population of electron traps. The device is then pulsed to a low voltage on-state (called the non-quiescent point) and the current is measured. This measurement is repeated for different non-quiescent points and different pulse widths to build a set of IV curves that can be compared to the non-pulsed DC curves to see the extent of the current collapse.

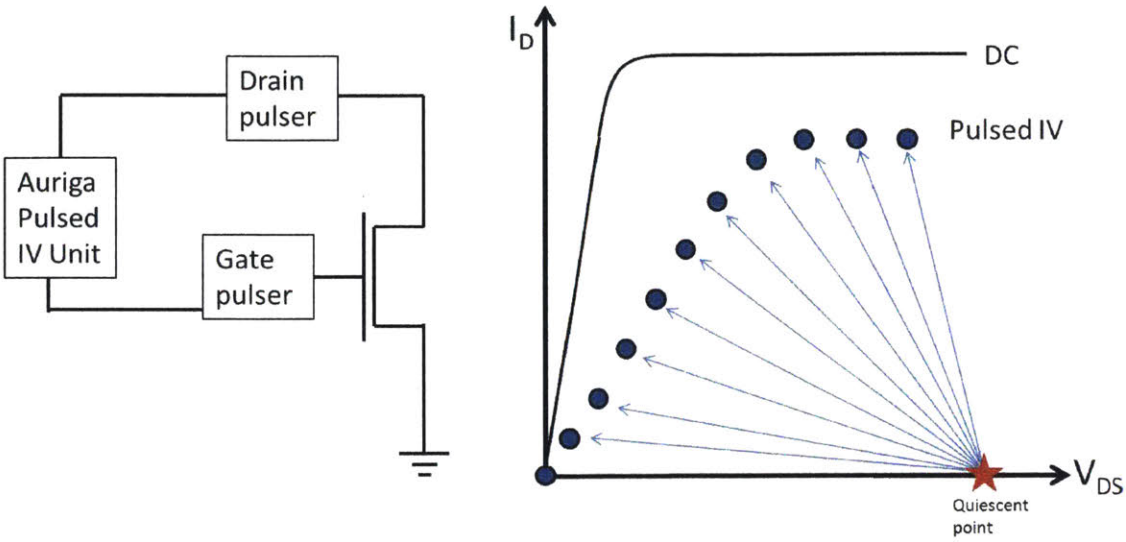


Figure 2.17. Pulsed-IV setup and illustration of pulsed-IV sweep

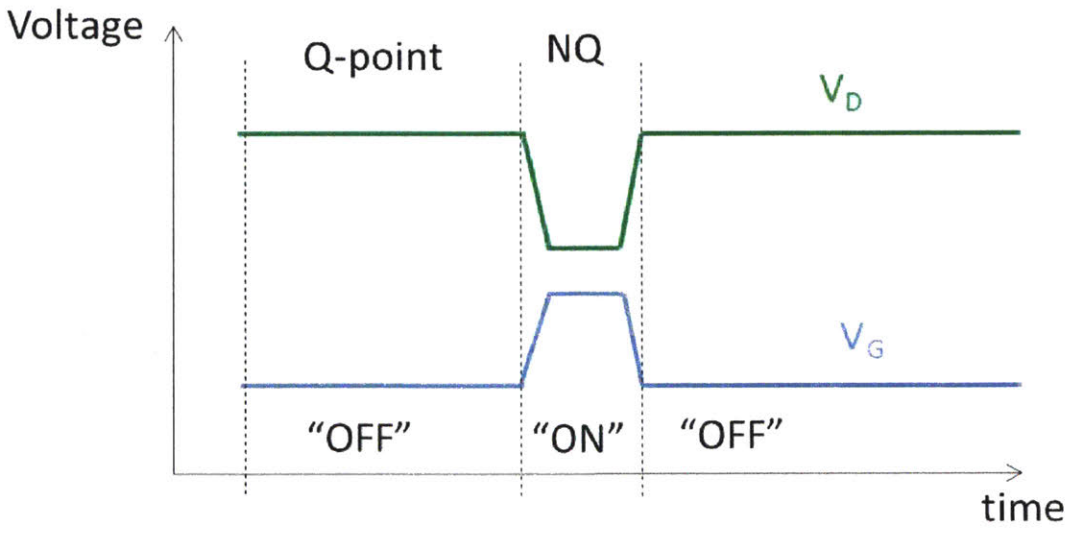


Figure 2.18. Illustration of Pulsed IV Waveform for a FET measurement

PECVD silicon nitride was deposited on the sample as this film has been shown to be effective in suppressing current collapse [27]. The thickness was varied since this silicon nitride layer not only passivated the surface but also acted as a foundation layer for supporting field

plates. As will be explained in the next section, the distance from the field plate to the 2DEG, dictated by the thickness of the passivation, is an important parameter in tuning the electric field.

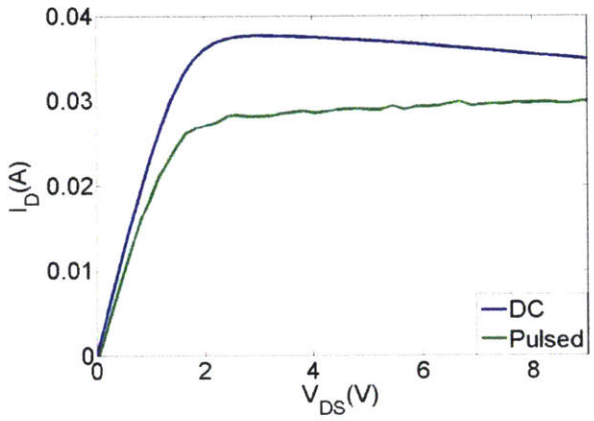


Figure 2.19. Pulsed IV Measurements. The transistor is switched from an off-state quiescent point of Vg=-4 V, Vds=10 V to an on state Vds=0 V and swept through the VDS range of 0 V to 9V. The pulse time widths were 500 ns and the on-state duty cycle was 0.1%.

Field plate

Silicon nitride has been demonstrated to be an effective material to passivate the surface of GaN HEMTs. However, after passivation and reduction of the surface state density, the electric field in the channel is less uniformly spread, which significantly reduces the breakdown voltage of the device. A field plate is needed to smooth the electric field and prevent low voltage breakdown [28], [29]. Field plates have also shown to reduce current collapse by alleviating the high electric field [30].

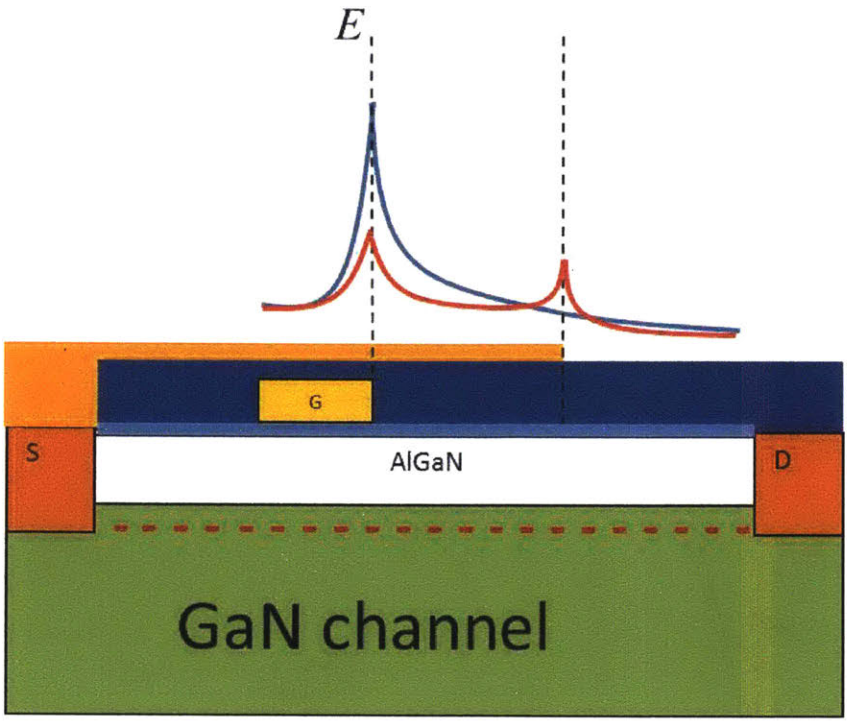


Figure 2.20. Electric field distribution without field plate (red) and with source connected field plate (blue)

To identify the optimal silicon nitride thickness for our devices, we deposited several different thicknesses on test samples and measured the breakdown voltage by turning off the transistor (V_G=-8 V) and sweeping the V_{DS} until the off-state leakage current was 1 μA for W_G=100 μm devices. Figure 2.21 is an example of such a sweep. The results of this test are compiled in Figure 2.22. An optimal thickness of ~170 nm of silicon nitride was obtained to maximize the V_{BK}.

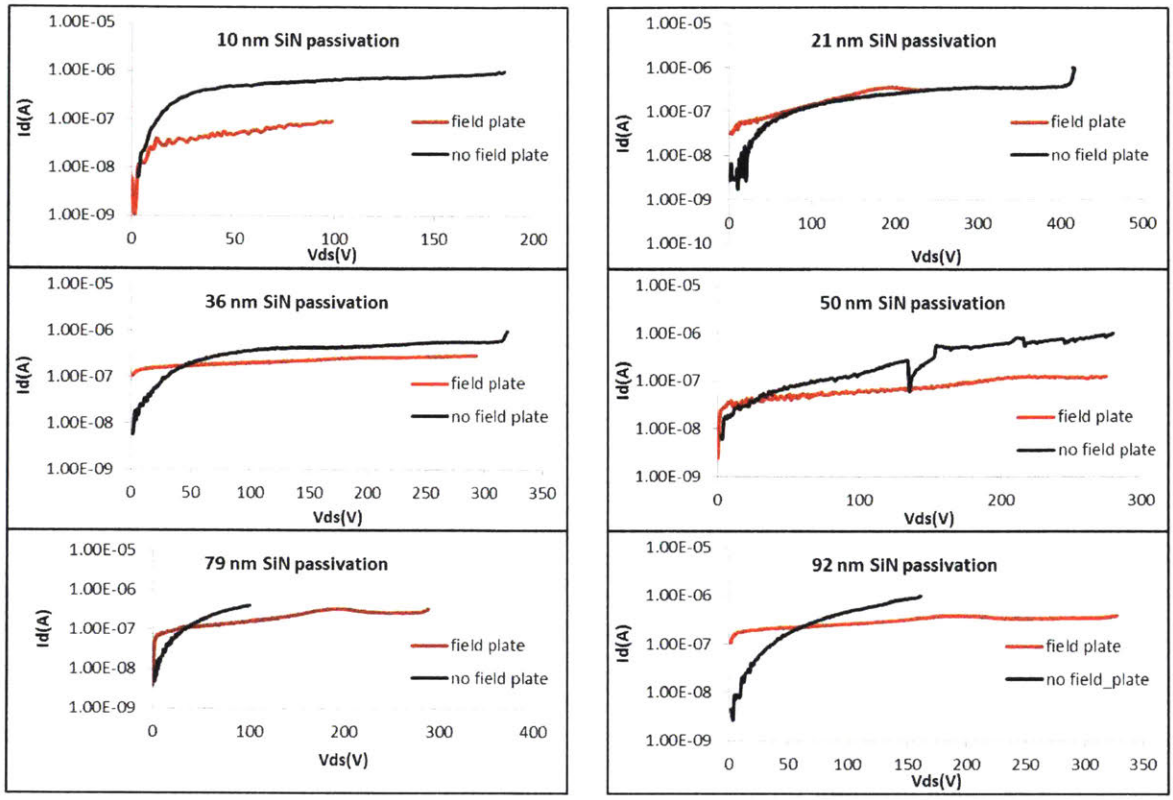


Figure 2.21. Breakdown Voltage measurements for field plated and non-field plated devices.

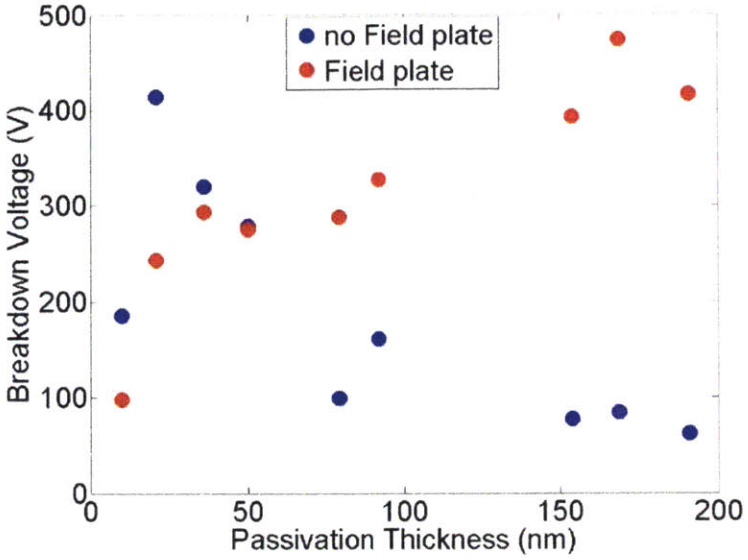


Figure 2.22. Summary of breakdown voltage measurements. Using this data, the optimal passivation thickness giving the highest breakdown voltage (473 V with 170 nm of passivation) was identified

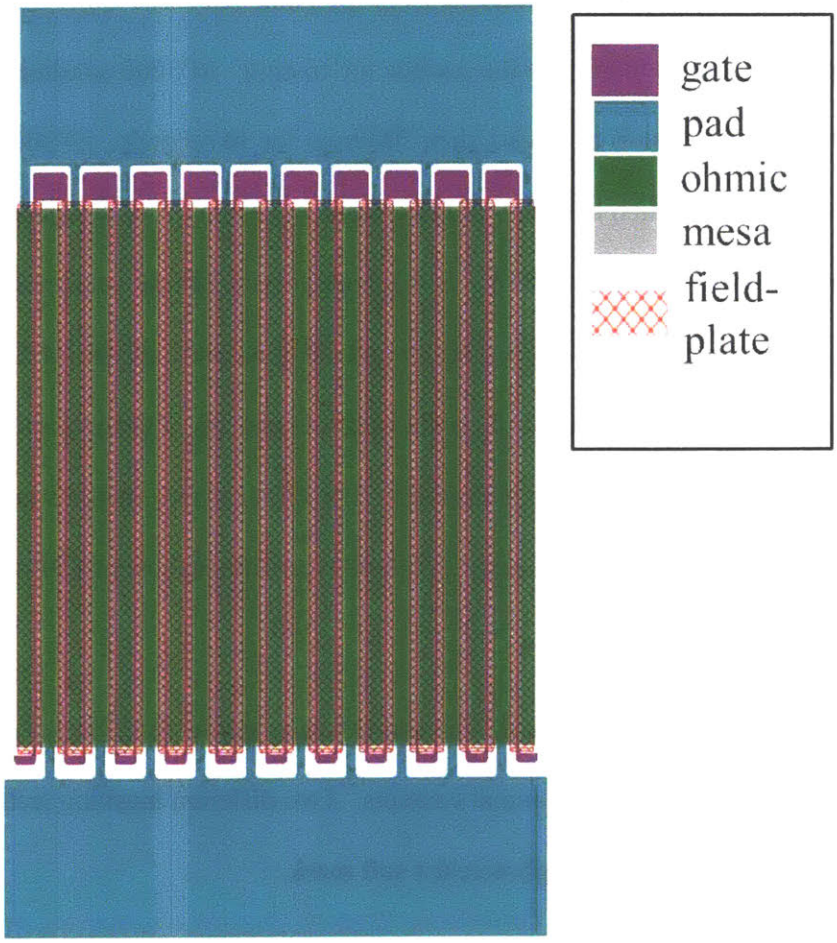


Figure 2.23. Field-plate layout on multifinger devices

Interlayer Dielectric

At this point the devices are fully functional as passivated, field-plated transistors. Now the isolated gate fingers need to be connected to make wide-periphery multi-finger devices. An interlayer dielectric is needed to separate the device from the interconnect metal.

Initially, the low-k dielectric polymer benzocylcobutene (BCB) was chosen. This was selected for its low dielectric constant to reduce the capacitance contributed by the overhanging interconnect metals.

The sample was cleaned with acetone, isopropyl, and deionized water and baked at 130°C to evaporate solvents to prepare the surface for coating. AP3000 solution was spun on the sample at 500rpm for 5 seconds to spread, then 2000rpm for 30 seconds. AP3000 is a silane based adhesion promoter which enhances the interfacial adhesion of BCB to inorganic surfaces, which is otherwise poor [31]. Next, BCB was dispensed on the sample and spun on at 500rpm for 5 seconds to spread, then 1500 rpm for 60 seconds for a target thickness of 2 micrometers. T1100 rinse solution was lightly swabbed on the backside and edges of the piece to remove excessive BCB. The coated piece was prebaked at 110° C to remove solvents and stabilize the film. The sample was then placed in an oven with nitrogen atmosphere at 250°C for one hour to cure the BCB.

At this point in the process, the entire sample was coated with BCB and openings had to be patterned and etched to access the metal contacts. Two different masking techniques were tested: a chromium hard mask and a photoresist soft mask.

AZ4620 thick photoresist was dispensed and spun at 1500rpm for 9 seconds to spread, 4000rpm for 60 seconds, and 5000rpm for 10 seconds to remove edge bead. The sample was then placed in a pre-bake oven at 95°C for 10 minutes to cure the resist, exposed in the contact aligner, and developed in AZ400 to remove the photoresist above the areas that needed to be opened. The resist acted as a soft mask (sacrificial layer) in the etching process.

A chromium hard mask was deposited on another sample. A 750Å layer of Cr deposited by electron beam evaporation and patterned by the same liftoff process described above.

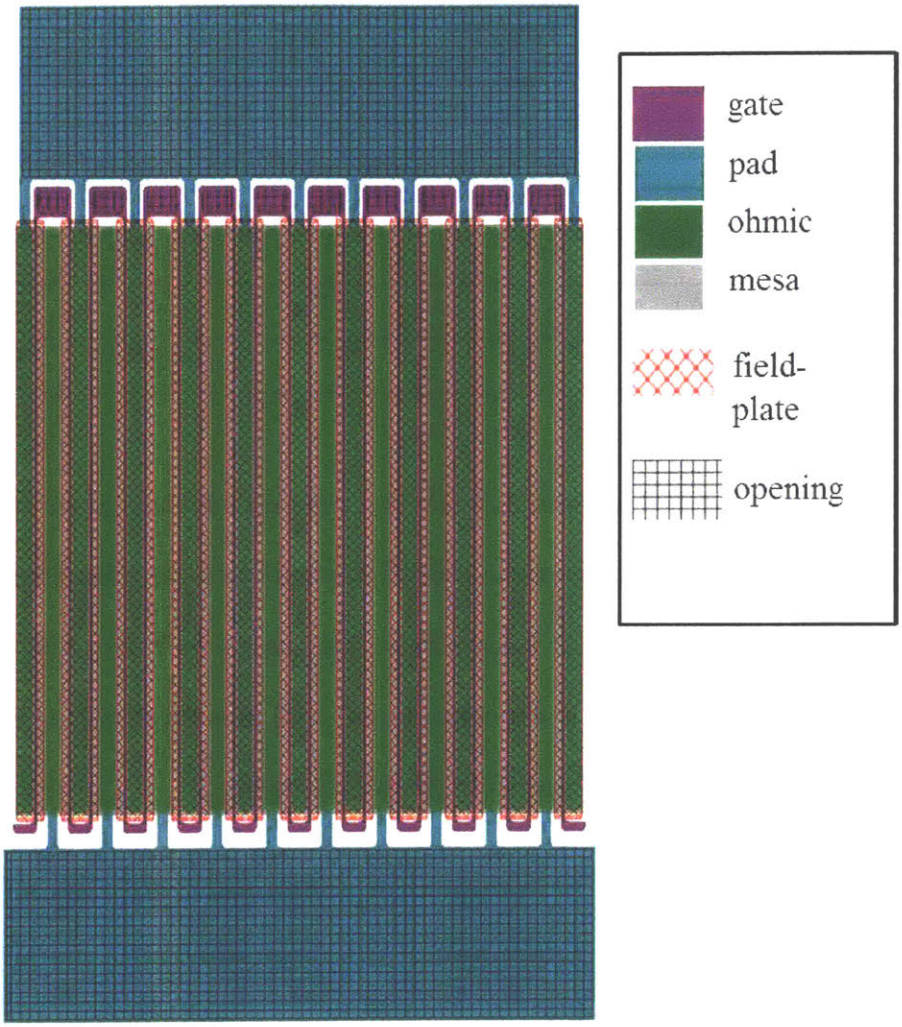


Figure 2.24. Openings in the interlayer dielectric

Prior to etching the sample, work was done to determine the etch rate of BCB with a given etch chemistry and power. A dummy silicon piece was prepared by spinning on BCB as described in the preceding paragraph. ECR etching was performed on the silicon dummy piece. The etch conditions are shown in the table below.

Table 2.2. BCB etch conditions

	Step 1	Step 2	Step3
O_2 (sccm)	40	40	40
CF_4 (sccm)	5	5	5
Pressure (mTorr)	10	10	10
ECR (W)	0	15	100
RF (W)	0	30	30
Time (s)	30	5	vary

The piece was etched for three different times and the thickness of the BCB layer after each etch was measured using a spectroscopic reflectometry tool, the Nanometrics Nanospec. The results are shown in Figure 2.25 below. From this data, the etch rate of BCB in O_2/CF_4 was extrapolated. With this etch rate, it was determined that 21 minutes of etching would remove the approximate 2 micrometers thick layer of BCB on the sample.

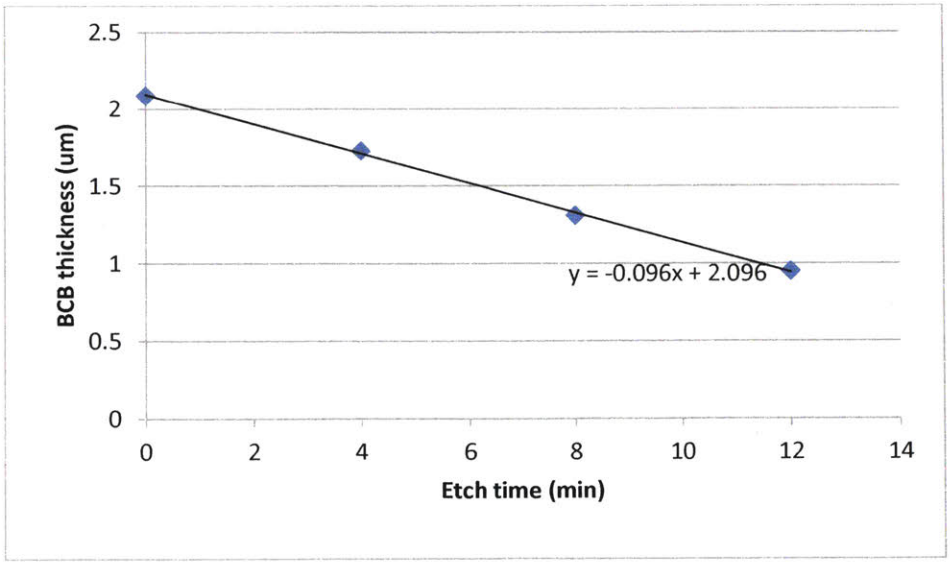


Figure 2.25. Etch rate of BCB in CF_4/O_2 plasma = 0.096 micrometer/minute

The GaN samples with transistors were etched for the necessary time to remove the BCB not shielded by a masking material, thus creating openings to the metal contacts. Agitation in acetone removed the remaining photoresist on the sample with the soft mask, and a 30 second immersion in Cr etchant removed the remaining chromium on the sample with the hard mask.

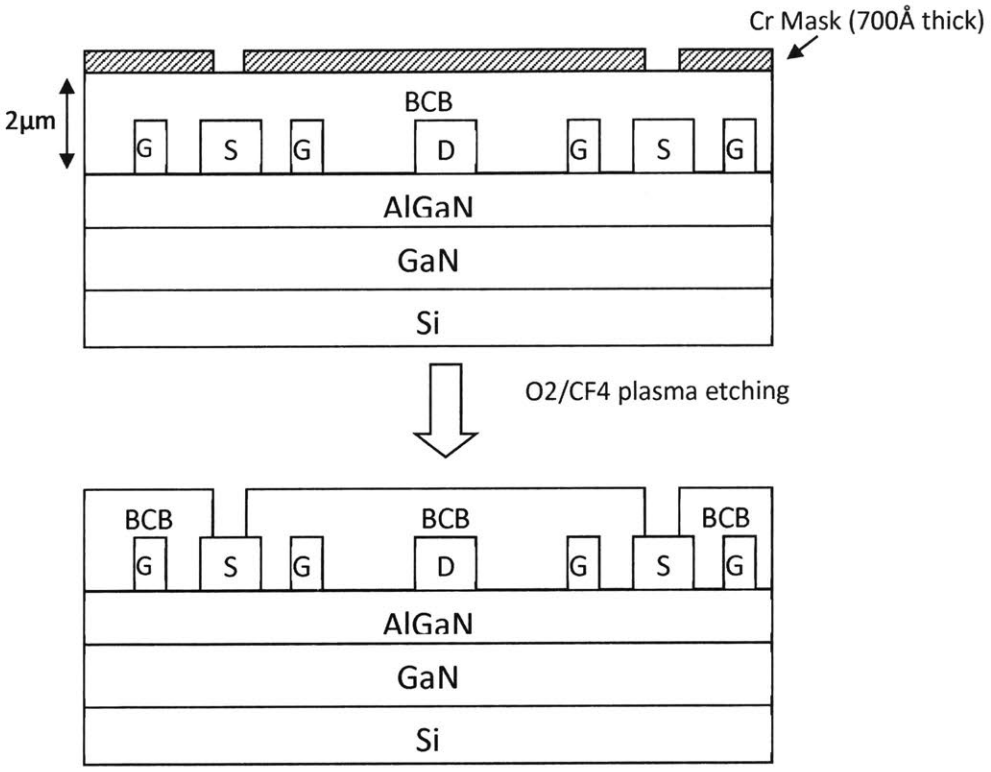


Figure 2.26. BCB Etching. Areas above the source contacts not covered by masking material are etched.

Different results occurred from the different masks. Figures 2.27 and 2.28 below illustrate the differences. In these micrographs the source openings have been coated with gold

(as required to connect the separate sources). The openings etched with photoresist mask had poor definition and uniformity. As seen in Figure 2.27, the openings have a round shape and the features on the left of the figure are much more etch than the features on the right.

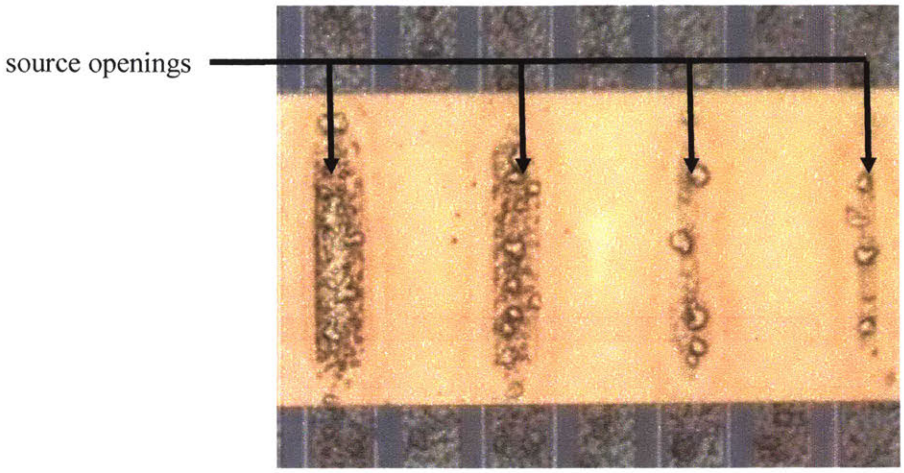


Figure 2.27. Etched source openings with photoresist mask.

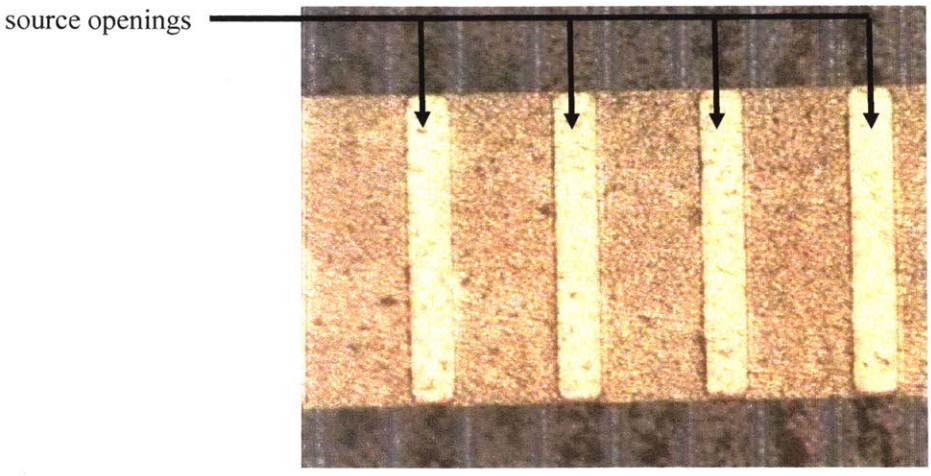


Figure 2.28. Etched source openings with Cr mask.

The differences in quality of etch definition for the openings can be explained by a fabrication effect called the aspect ratio dependent etching (ARDE) lag. Variations in the size of the pattern opening will cause variations in the etch rate of the specific material. Specifically, larger features (having smaller depth to width aspect ratios) will etch faster than smaller features (having larger depth to width aspect ratios).

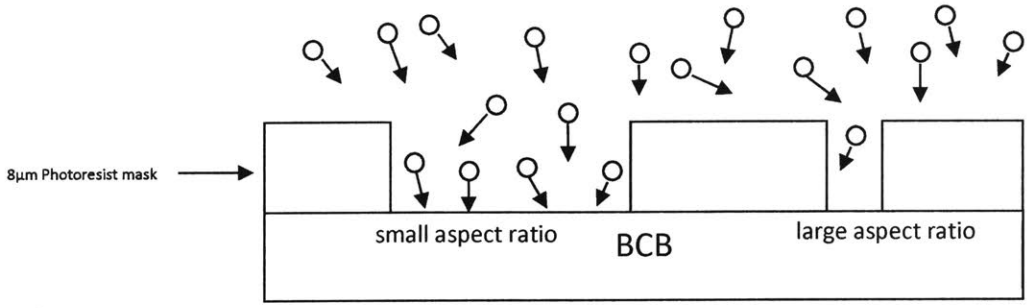


Figure 2.29. Thicker masking layer results in blocking of etching species in the smaller openings. This results in a non-uniform etch

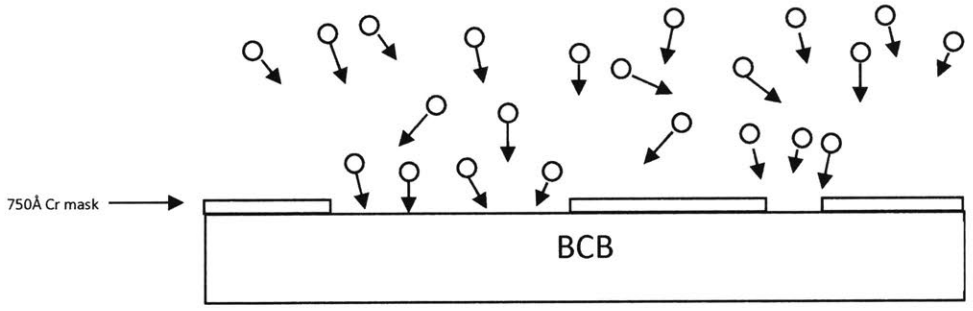


Figure 2.30. Thinner masking layer results in less blocking of etching species in the smaller openings. There is a small aspect ratio for all features, resulting in a uniform etch.

The etch resistance of Cr in BCB etch chemistry is much better than photoresist, and thus a thinner layer will suffice and there ARDE lag will not be as drastic, meaning that the piece can be etched more uniformly. It was thus decided that the thin Cr mask was the better option and subsequent devices were processed using this hard mask.

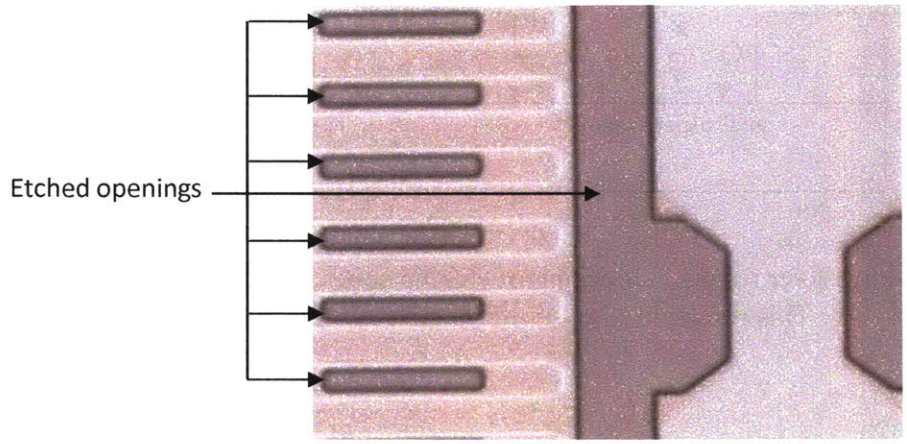


Figure 2.31. Micrograph of BCB etched piece

Problems with BCB and Suitability of SiO_2

Although BCB seemed to be a promising candidate as the interlayer dielectric, subsequent processing steps showed problems with the film. Stresses induced by deposited layers (hard-mask etching layer and device interconnect metallization) can cause cracking in the dielectric film, as shown in Figure 2.32. While this may not be a significant problem in smaller

periphery devices, it is not ideal for large currents present in the large periphery devices we are targeting as the current burns the metal interconnects as shown in Figure 2.33.

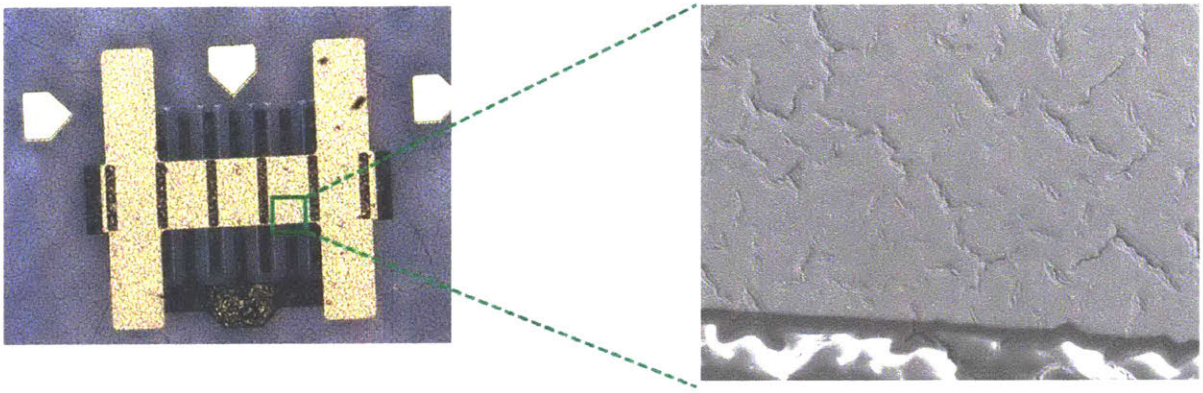


Figure 2.32. BCB cracking after metal deposition

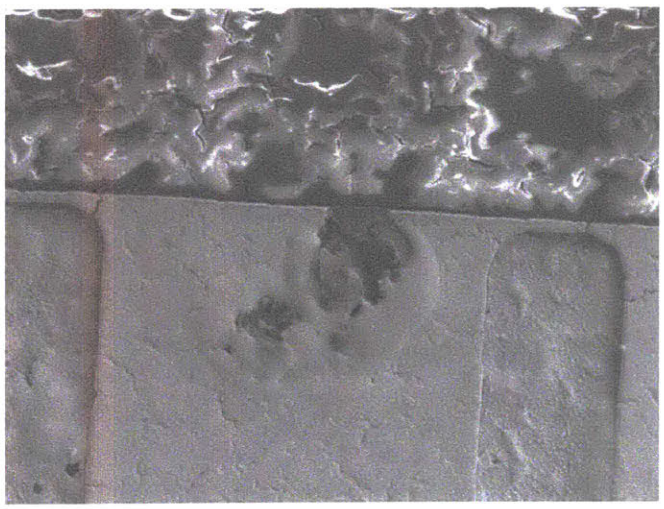


Figure 2.33. Burned metal interconnect on cracked BCB

Metal layer deposited on the BCB filled the cracks resulting in sharp points which could have high localized electric field leading to premature breakdown. These metal sharp points were

confirmed by Focused Ion Beam cross-sectional cuts and observing the different layers. These factors led to the conclusion that BCB was not an appropriate interlayer dielectric material.

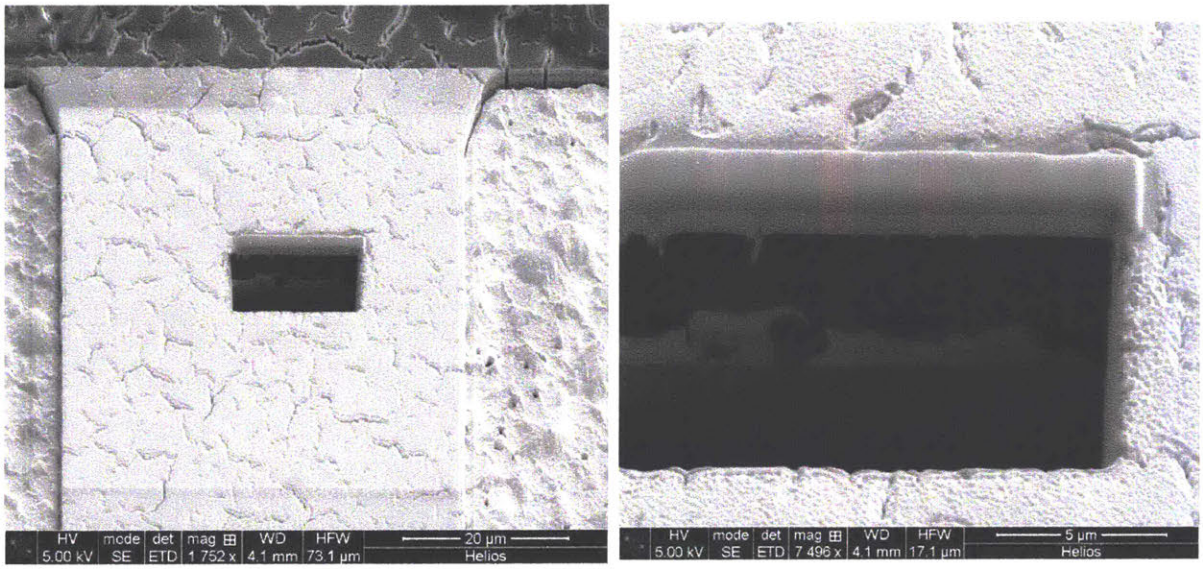


Figure 2.34. Interconnect metal in BCB cracks

Silicon oxide deposited by plasma enhanced chemical vapor deposition was the alternative chosen. While it does have a higher dielectric constant than BCB (ε_{SiO2}= 3.9, ε_{BCB}= 2.65), the improved thermal/stress stability, layer uniformity, and dielectric strength make it a reasonable alternative. Characterization of test SiO_2 metal-insulator-metal (MIM) capacitors (Figure 2.35) showed that it more than met the requirements of the interlayer dielectric for these devices. Two-micrometer-thick SiO_2 was deposited on the samples. Via openings were patterned by photolithography and etched by CF_4 based plasma dry etch. The masking photoresist was then removed with acetone, isopropyl alcohol solvent clean.

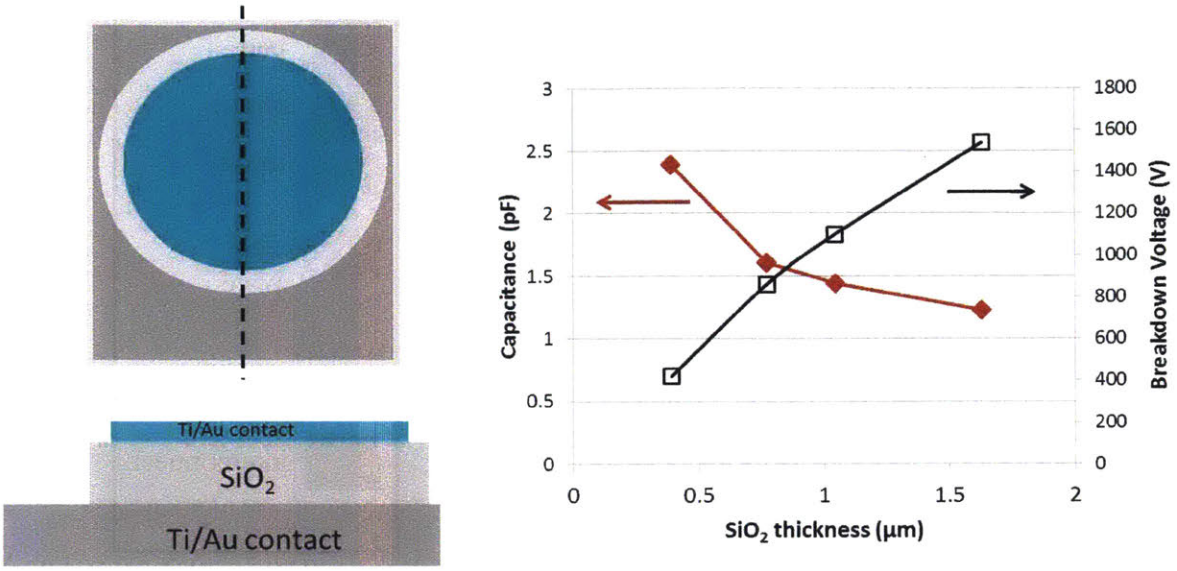


Figure 2.35. Characterization of PECVD SiO2 breakdown voltage and capacitance.

Interconnect metal

The final step in making the multi-finger devices was the interconnect metal which ties together the individual transistor fingers to make the wide periphery device. Ti (15 nm)/Al (1 μm) was sputtered on the sample. The interconnect patterns (Figure 2.36) were patterned and a Cl_2/BCl_3 dry etch was performed to remove the Ti/Al in all of the unmasked areas of the sample. Attention is needed for the temperature of the etch, since higher temperature etching reduces the sticking probability of etched metal particles on the surface of the sample and results in a cleaner etch (Figure 2.37).

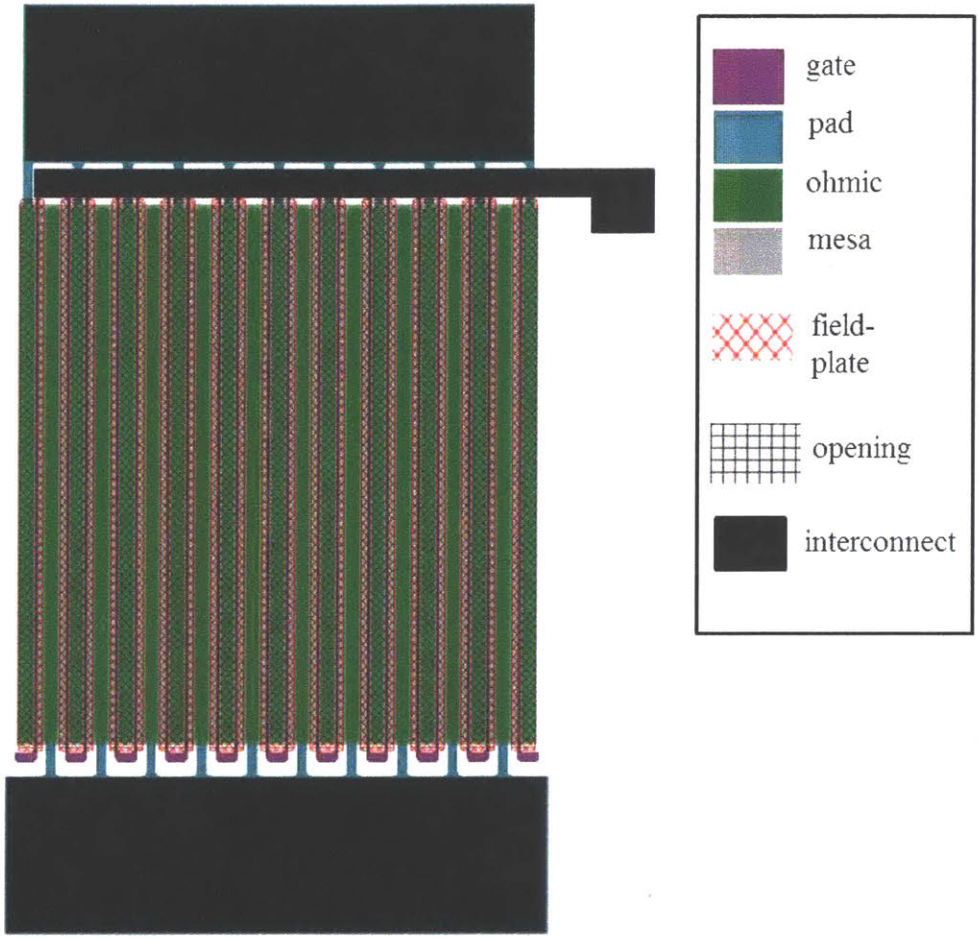
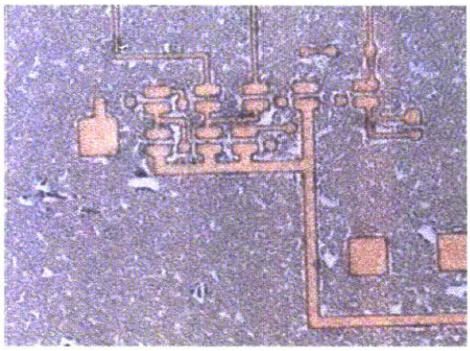
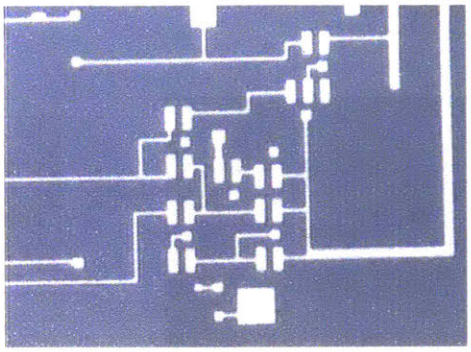


Figure 2.36. Interconnect layout pattern



Chuck temp=15C,
ECR=140W, RF=25W



Chuck temp=50C,
ECR=100W, RF=15W

Figure 2.37. Etching of Ti/Al at different chuck temperatures; the higher temperature etch resulted in a cleaner etch.

Packaging Considerations

Now that the devices on the wafer coupons are complete, the individual HEMTs are diced out and need to be packaged for testing in the converter circuit PCB. Initially, the devices were glued into a chip package and the contacts of the transistor were wire bonded to the output leads of the package. Several wire bonds were made to each contact to increase the current carrying capability and ensure redundancy in case a wire broke or burned out. While this packaging method was rather simple, it was not ideal particularly for the high-frequency switching applications sought by these devices (~MHz). The wire bonds introduced extra parasitic inductances which slow down the system and prevent the user from realizing the full potential of the high speed GaN switch. Thus an alternative packaging method was used. For this second method, after wafer dicing, solder ball bumps were placed into the transistor contacts. The device was then connected directly to the PCB through a flip-chip bonding, eliminating in this way the need for intermediary wire bonds.

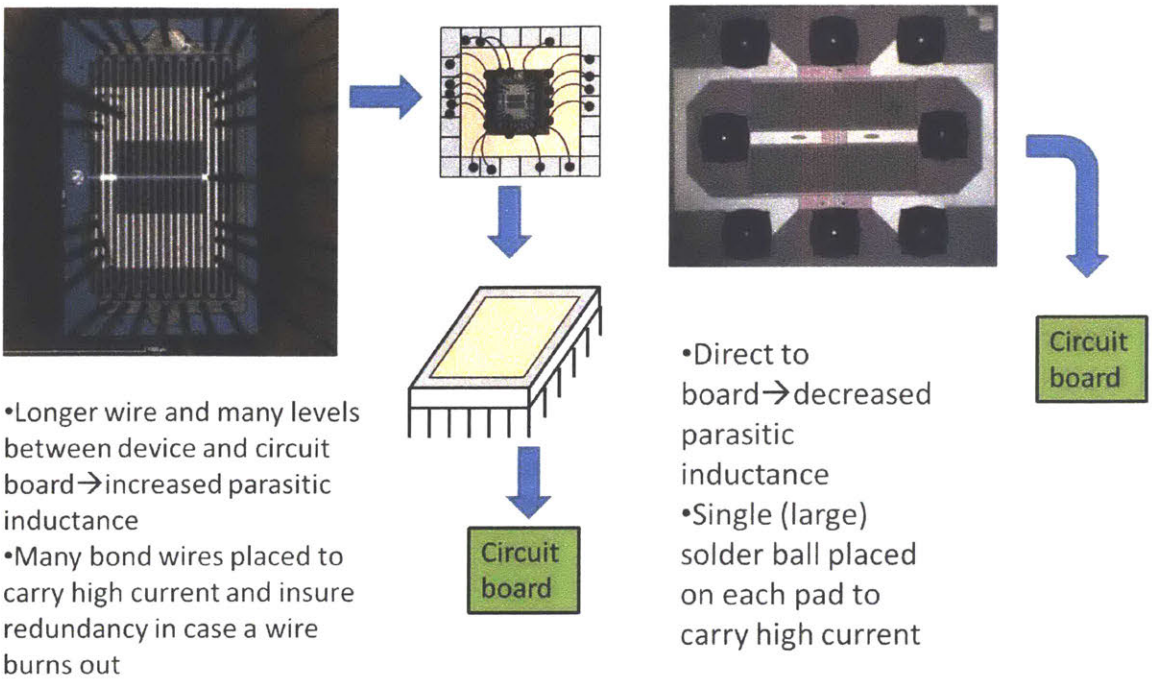


Figure 2.38. Packaging Considerations

Device Results

The device DC characteristics were measured using an Agilent B1505 power semiconductor analyzer and a Cascade Tesla probe station. The transfer characteristics were measured by keeping V_{DS} constant at 1 V and sweeping V_{GS} from -8 V to 0 V, to show the off-state leakage level, the threshold voltage and the on-state current. Figure 2.39 shows the transfer characteristics of a device with tri-gate barrier recess and a device without tri-gate barrier recess (both devices had W_g=250 μm). The barrier recess was effective in shifting the device threshold from -7.8 V to -1.9 V.

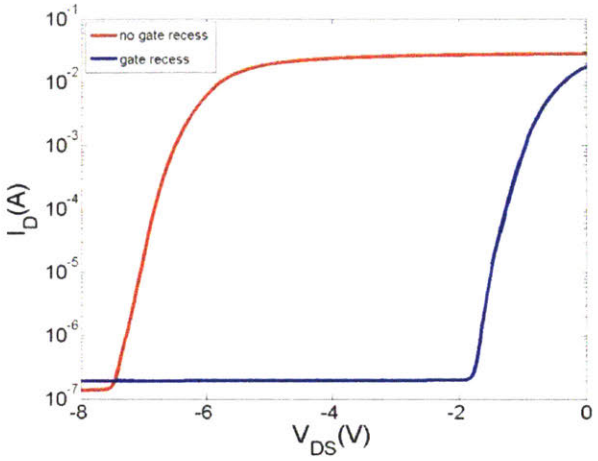


Figure 2.39. Transfer characteristics of a device with tri-gate structure and barrier recess (blue curve) and a device with no tri-gate or barrier recess (red curve).

The transfer characteristics of devices with various gate peripheries were also measured (shown in Figure 2.40). As seen in the figure, there is not as smooth a transition from the off-state to the on-state in the wide-periphery transistors. It is believed that this is due to etching non-uniformities in the gate recess. This would cause certain gate fingers or certain parts of the channel to turn on before other parts. Improvements in this step will be sought as future work for this project.

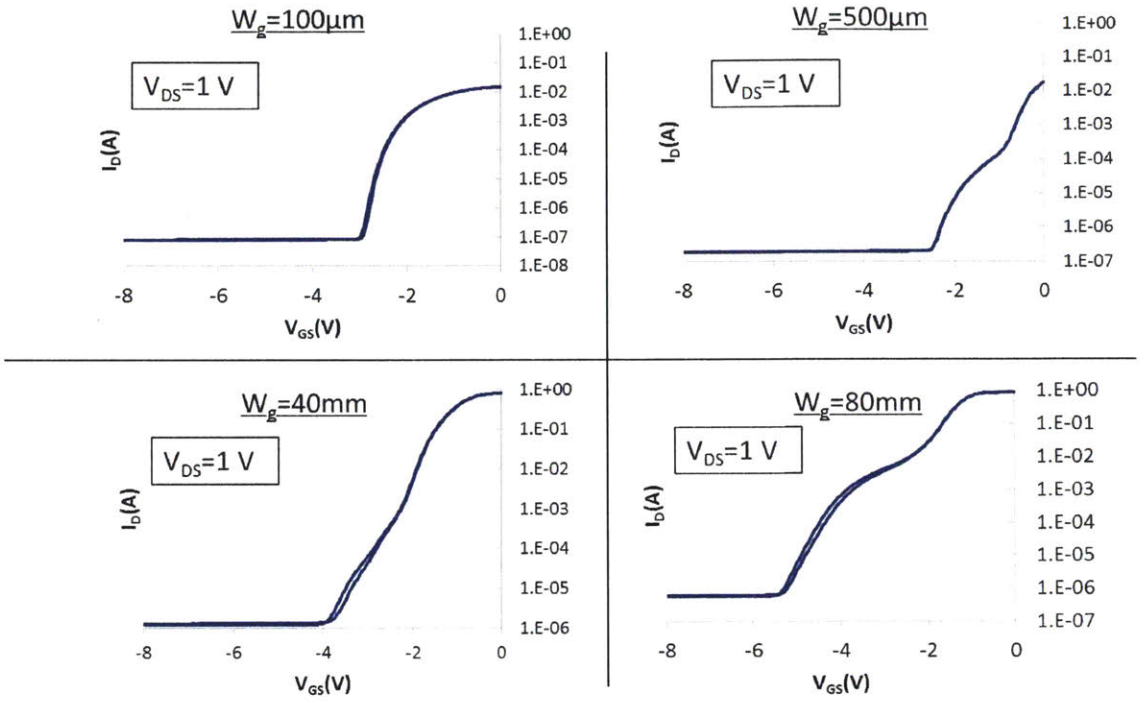


Figure 2.40. Transfer Characteristics of devices with different gate peripheries.

Pulsed IV measurements were performed with an Auriga AU4750 system. In this set of measurements, the drain current was measured while sweeping through V_{DS}=0-9V and returning to an off-state quiescent point (V_G= -4 V,V_{DS}=10 V). The resulting pulsed IV curve is shown in Figure 2.41. Comparing to the DC measurement of the same device, it is seen that there is approximately a 25% decrease in maximum current due to current collapse.

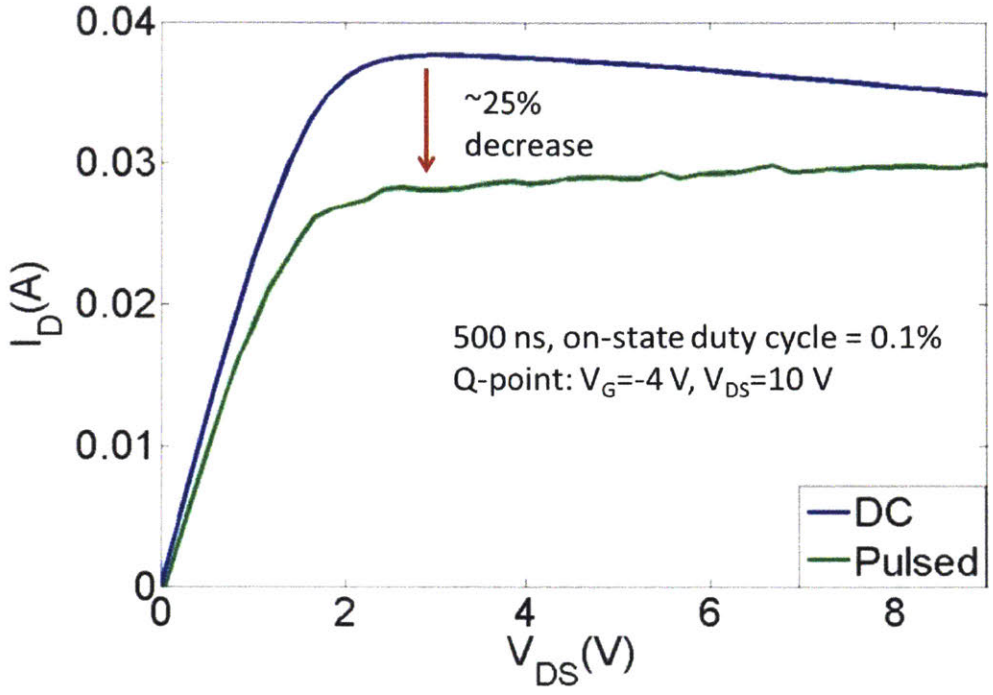
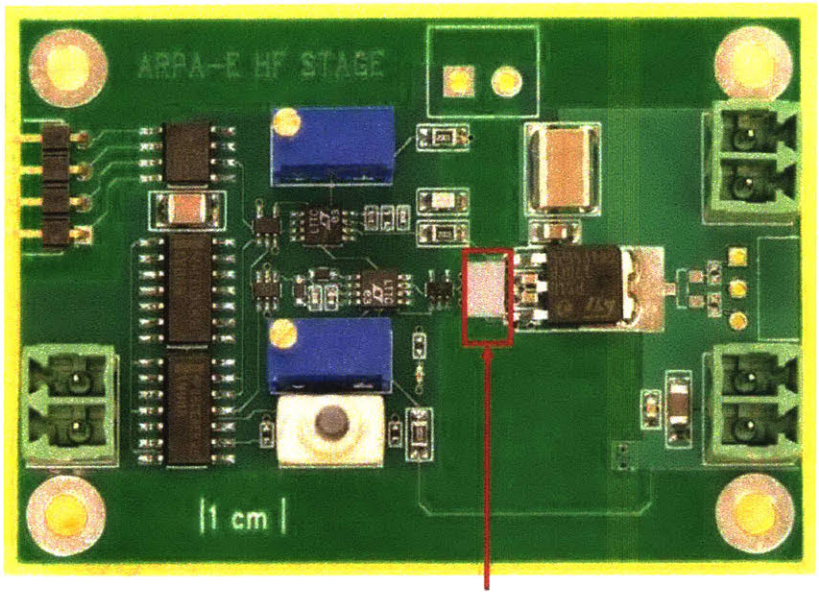


Figure 2.41. Pulsed IV measurement results.

The packaged GaN HEMTs were used as a power switch in a DC-DC buck converter operating at 5 MHz with 100 V input **designed in Prof. David Perreault's group at** MIT and the efficiencies were measured. It was observed that the W_g = 40 mm GaN device had a higher efficiency that the best commercially-available GaN HEMTs at low power levels (below 20 W). At higher power levels, the efficiency begins to taper off. It is believed that this is due to device self-heating and subsequent high temperature effects. Thermal solutions such as a heat sinks or optimization of the gate-to-gate pitch could alleviate this problem.



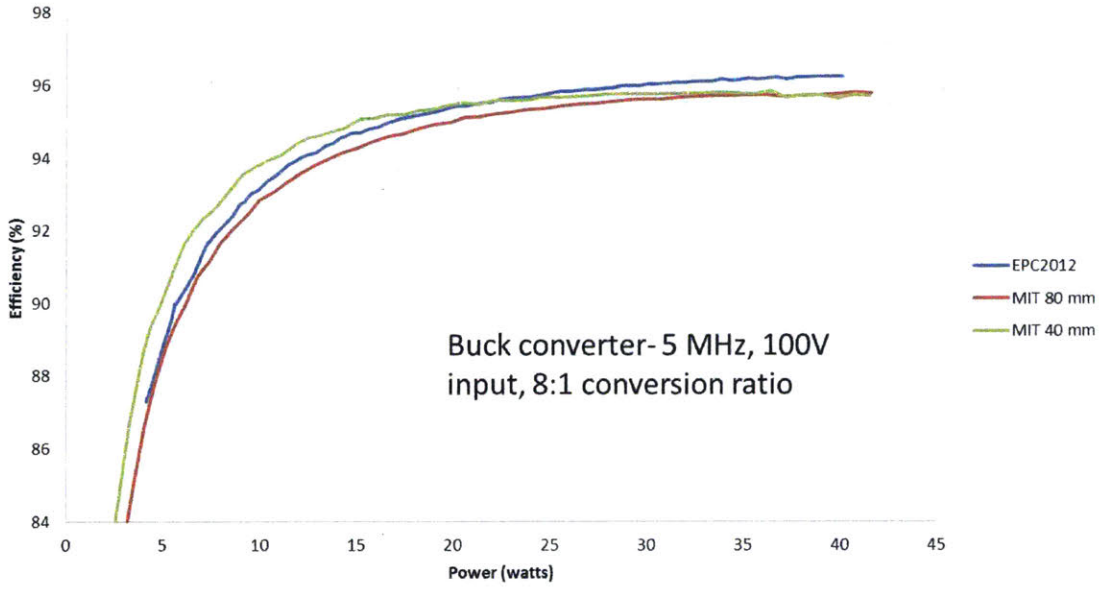


Figure 2.41. Efficiency of buck converter circuit with different GaN HEMTs used as the power switch.

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Chapter 3: Applications and Integration of Wide-Periphery Technology

The previous chapter detailed the process optimization for producing wide-periphery AlGaN/GaN fin HEMT power switches. With this technology in place, slight modifications can be performed to tailor the device to specific applications. Now that we have ability to fabricate devices over a large range of sizes in this chapter we show how to take advantage of this to implement this technology in other forms and applications.

DC-DC multiphase buck converter

The decrease of supply voltages for modern processors coupled with the stationary or increasing input dc voltage levels call for high-efficiency DC-DC converters with higher conversion ratios. While the DC-DC down conversion can be accomplished in many steps, reducing the number of converter steps would increase the overall efficiency. For example, in data centers DC-DC conversion from the high-voltage grid to lower-voltage components (like CPUs) may be realized with multiple steps, with each step bringing the voltage down to an intermediate level to be input to the next converter, as shown in Figure 3.1 [1]. The overall conversion efficiency can be improved by reducing the number of intermediate steps for which high-conversion ratio, high input voltage converters are required. Such converters that use high voltage switches in discrete packages may see a switching frequency improvement through an integrated method.

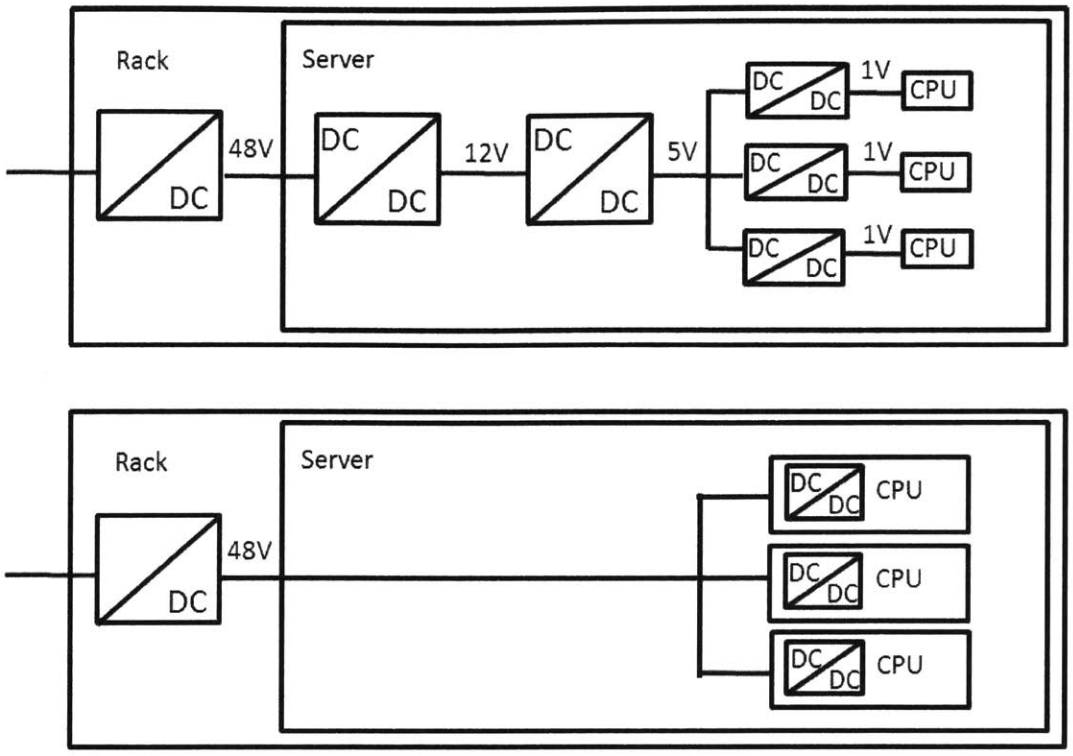

Figure 3.1. Two power distribution approaches for data centers, with the more traditional approach of multiple intermediate steps of conversion between the high-voltage grid and low-voltage components (top) and an alternative approach reducing the number of conversion stages that could be realized with a CMOS/GaN integrated voltage regulator [1].

Integrated voltage regulators, with the converter and load sharing the die promise to reduce interconnect parasitics [1] to effectively run at higher frequencies. Such regulators commonly use Si CMOS devices, but the introduction of GaN with high breakdown voltage would spur improvement.

In addition to conventional discrete packaged solutions, one could have a monolithic integration solution. Si CMOS on the same wafer as GaN (which is discussed in Chapter 5) brings many advantages in interconnect reduction, but requires drastic changes to the CMOS process line and re-optimization of the GaN devices. A compromise is face-to-face bonding of the GaN chip with the Si CMOS so that the chips are intimately connected with small parasitic

inductances. This allows for the decoupling of the GaN and CMOS processing. To accomplish this, the design of the CMOS chip and the GaN transistors must be coordinated and our wide periphery HEMT processes provided the flexibility to enable this.

Chapter 2 described the process flow to fabricate discreet packaged GaN HEMT switches with tri-gate barrier recess for threshold voltage control. This process was adaptable to use for power switches in a 40 MHz hybrid CMOS/GaN integrated multiphase dc-dc switched-inductor buck converter with 20 V input voltage [1], designed by Professor Ken Shepard and Eyal Aklimi. This could find use in high-conversion ratio, high input voltage point-of-load converter.

Arrays of AlGaN/GaN HEMT were fabricated on 1 mm by 2 mm GaN on Si chips for integration in this project. The epitaxial wafer, output characteristics, and layout are shown in Figure 3.1 and Figure 3.2. These transistors were depletion mode, so they did not undergo the tri-gate or AlGaN barrier recess processing. The array chip consisted of sixteen HEMT switches that was then flip-chip bonded directly to a 2 mm by 4 mm CMOS chip as shown in Figure 3.3. The Si chip (manufactured in 180 nm CMOS technology) consisted of capacitively coupled level shifters and gate drivers for high side and low side GaN switches. The CMOS chip was thermosonically bonded with Au-bumps in preparation for receiving the GaN chip. The two chips were joined by thermocompression face-bonding at 260°C. Figure 3.5 shows the efficiency of the converter for an operating frequency of 40 MHz at different conversion ratios.

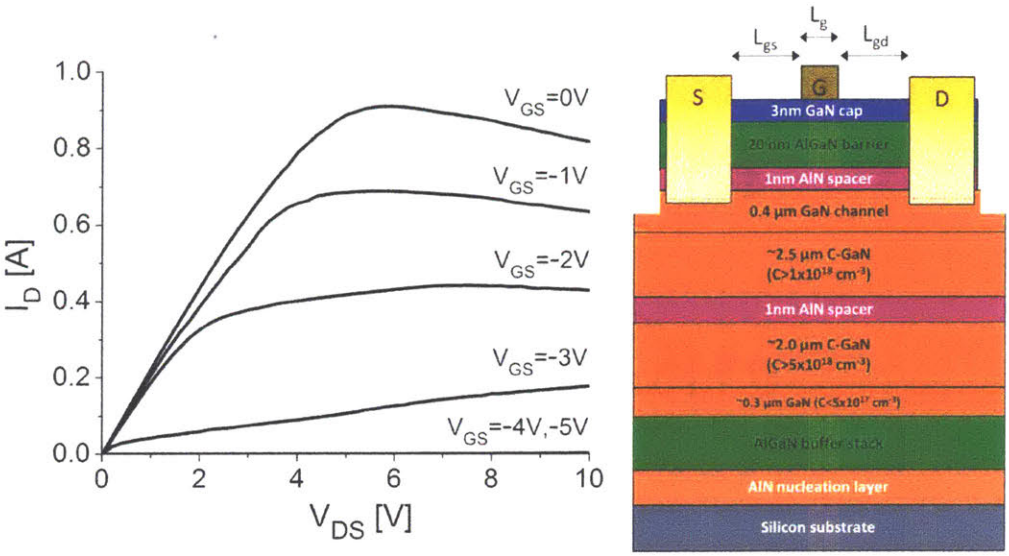

Figure 3.2: IV-curve and GaN HEMT structure

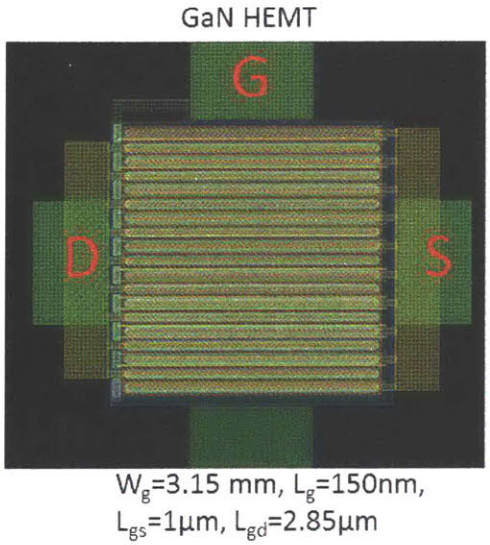

Figure 3.3: Layout of individual GaN HEMT switch and its corresponding dimensions

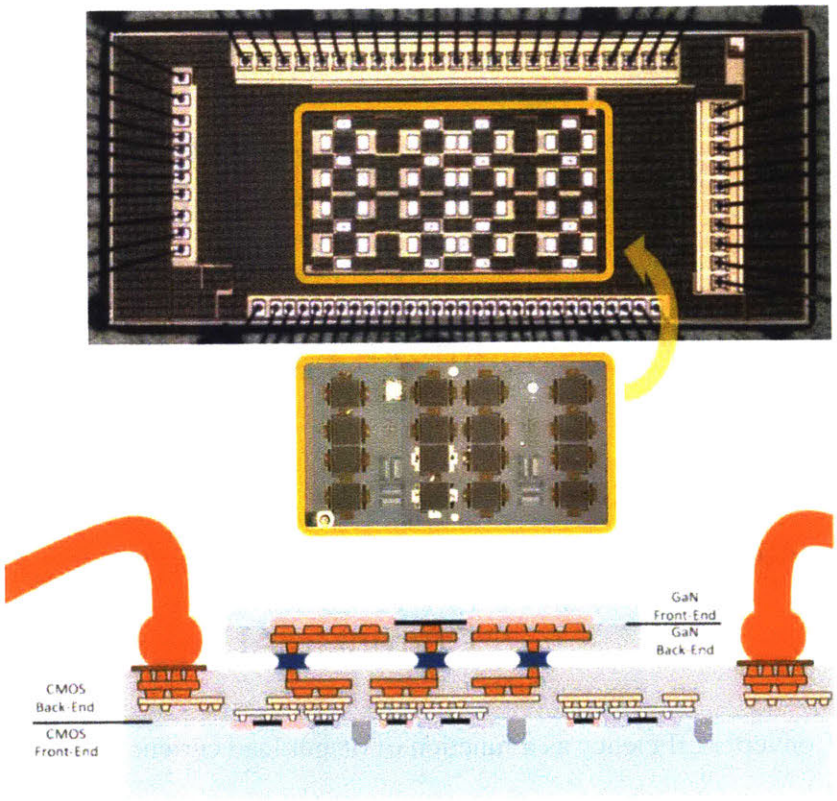

Figure 3.4: Micrograph of silicon CMOS die and attaching GaN die with array of HEMT switches; gold-gold thermocompression bonding diagram

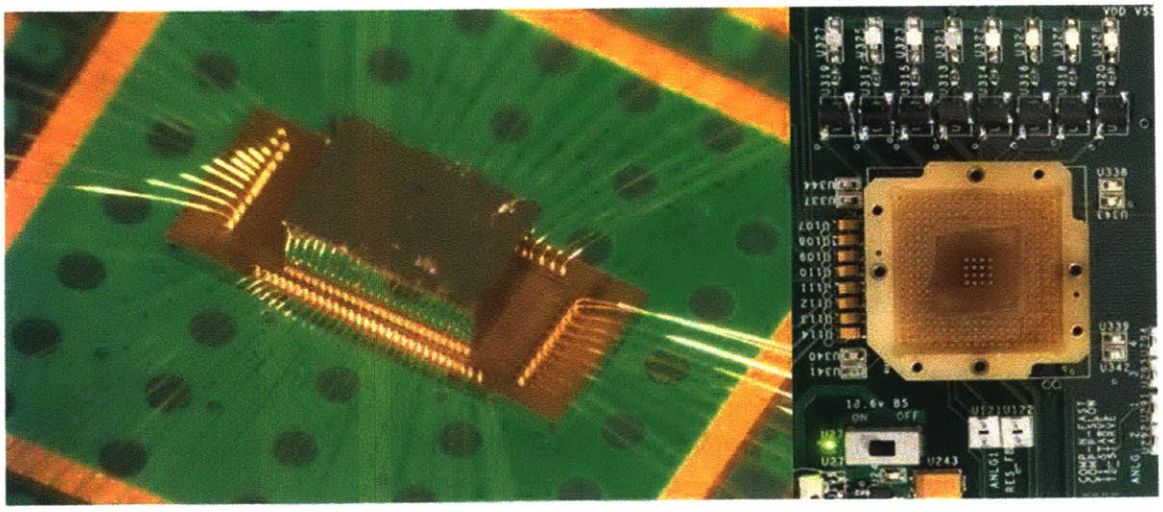

Figure 3.5: Assembled hybrid converter of GaN chip and CMOS die; prototype PCB showing the converter receptacle

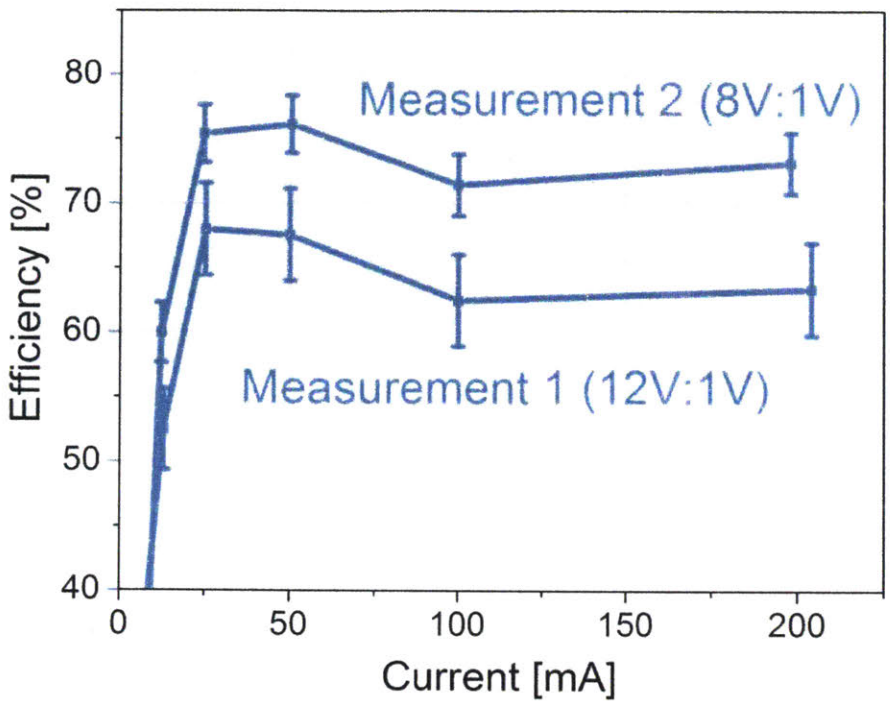

Figure 3.6: Converter efficiency as a function of output load current for 8:1 and 12:1 ratio

InAlN barrier GaN Devices

Traditionally, most GaN high electron mobility transistors (HEMTs) have been fabricated with AlGaN as the top barrier material, but the InAlN/GaN heterostructure gives a higher 2DEG charge density, thus enabling higher current density and lower on-resistance [2, 3].

Previous work on InAlN/GaN HEMTs has focused on their use in high frequency applications and their performance as a function of submicron gate length scaling [4, 5] and barrier thickness scaling [6], but to our knowledge there has not been a study of gate width scaling or a demonstration of large-periphery (>2.5 mm) devices. Using the wide-periphery technology developed in this thesis, InAlN barrier devices with a total gate periphery of 39.6 mm have been demonstrated.

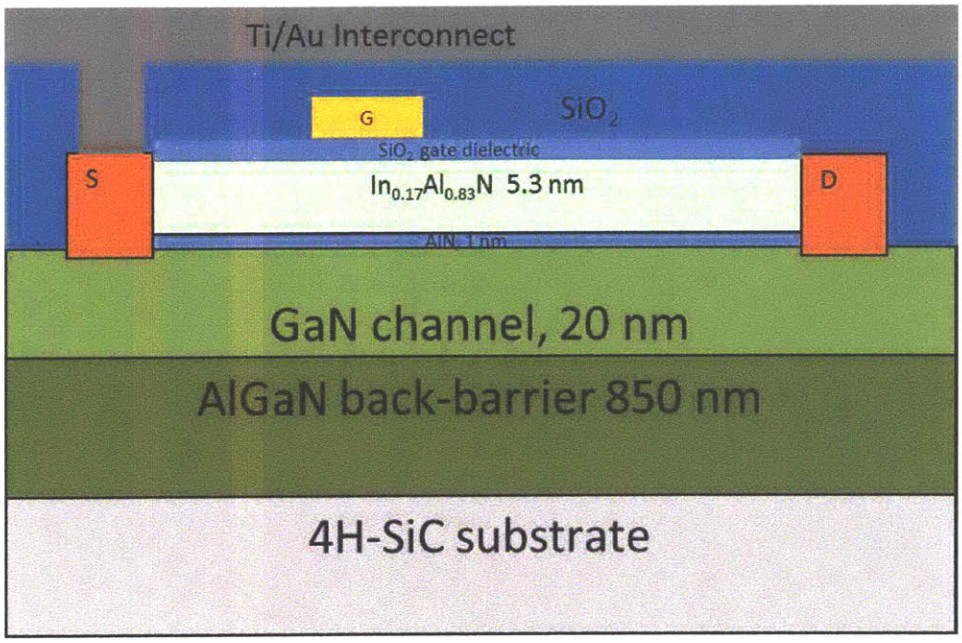

Figure 3.7: InAlN/GaN devices for wide-periphery demonstration

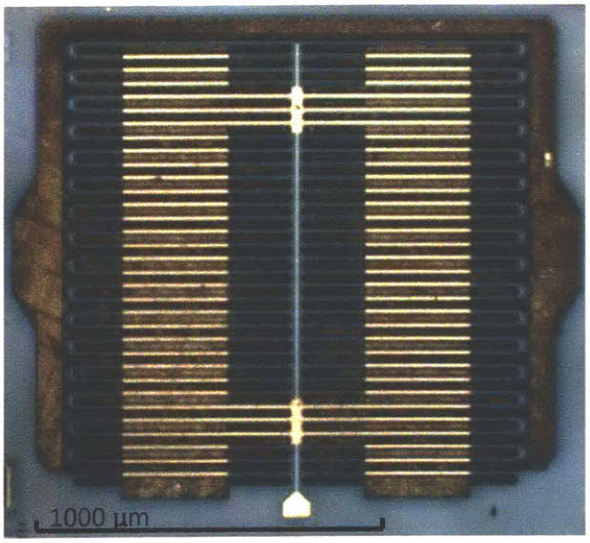

Figure 3.8: Optical micrograph of wide-periphery multi-finger HEMT, W_g=39.6 mm

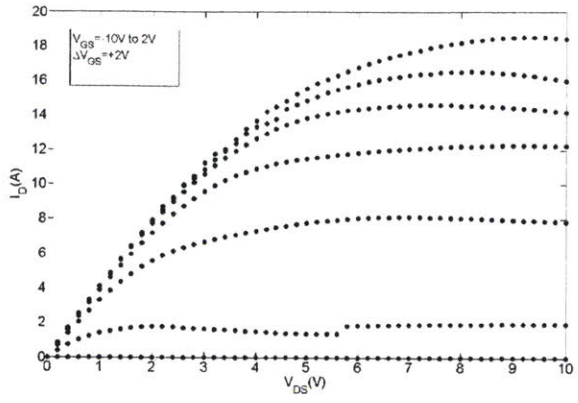

Figure 3.9: Output curves of wide periphery HEMT, with W_g=39.6 mm

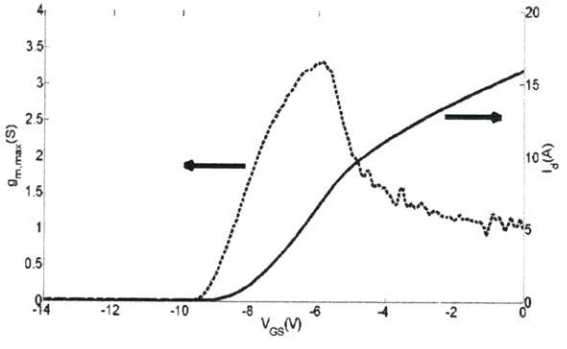

Figure 3.10: Transfer curves of wide periphery HEMT, with Wg= 39.6 mm

RF GaN HEMTs

The preceding discussion was about devices targeted for mid-level voltage in power switching applications. As an important metric for those switches was breakdown voltage, the devices have had large L_{gd} (8 to 30 μm) and a large 2 μm gate width. While these large spacings and gate lengths are fine for power switches, they are unsuitable for RF applications.

RF performance is largely governed by two important figures of merit: the unity current-gain cutoff frequency f_T and the unity power-gain cutoff frequency f_{max}. The current-gain cutoff frequency is the frequency at which the magnitude of the short-circuit current gain is unity and is given as:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} = \frac{v_{sat}}{2\pi L_g}$$

The equation shows why it is imperative to have as small gate length as possible to maximize the f_T and why the transistors used in the power switches will not yield a high cutoff frequency.

The unity power-gain cutoff frequency is given as:

$$f_{max} = \frac{f_T}{2}\sqrt{\frac{1}{g_o(R_g + R_i)}}$$

As can be seen, it in addition to having small gate length, it is also necessary to reduce the gate resistance. The combination of these two requirements is why it is very beneficial to have a "T" shaped or "Γ" shaped gate, as the gate foot (which define the L_g) can be small while the gate head can be large and thick to reduce the R_g.

In addition to a modified gate geometry, RF devices can be improved by also using a different barrier material than AlGaN. Since f_T scales with g_m, it would be beneficial to have the gate as close to the channel as possible (to increase the transconductance g_m). InAlN is a better suited barrier material than AlGaN to meet this requirement since equivalent charge densities can be achieved with thinner barrier layers.

The process flow for fabricating T-gate RF transistors was similar to the flow for the AlGaN/GaN power switches described in Chapter 2 with two main modifications. First, an

alternative epitaxial structure with InAlN (7 nm) barrier was used as shown in Figure 3.10. Second, the gate processing is altered. Since, there is not as strong of a need for enhancement mode devices in RF power amplifiers, the tri-gate, gate recess step for threshold voltage control was omitted. Instead, following the formation of the ohmic contacts, an 80 nm layer of PECVD silicon nitride is deposited on the sample. Next, a 90 nm gate foot is patterned by e-beam lithography and etched into the SiN to the InAlN barrier. This is followed by a 300 nm gate head patterning and an e-beam evaporation of Ni (30 nm)/Au (250 nm). The remaining passivation and multi-finger processing is completed as described in the previous chapter. With f_T up to 120 GHz and f_{max} up to 140 GHz, these devices will provide a base-line transistor process for more complicated integrated circuits.

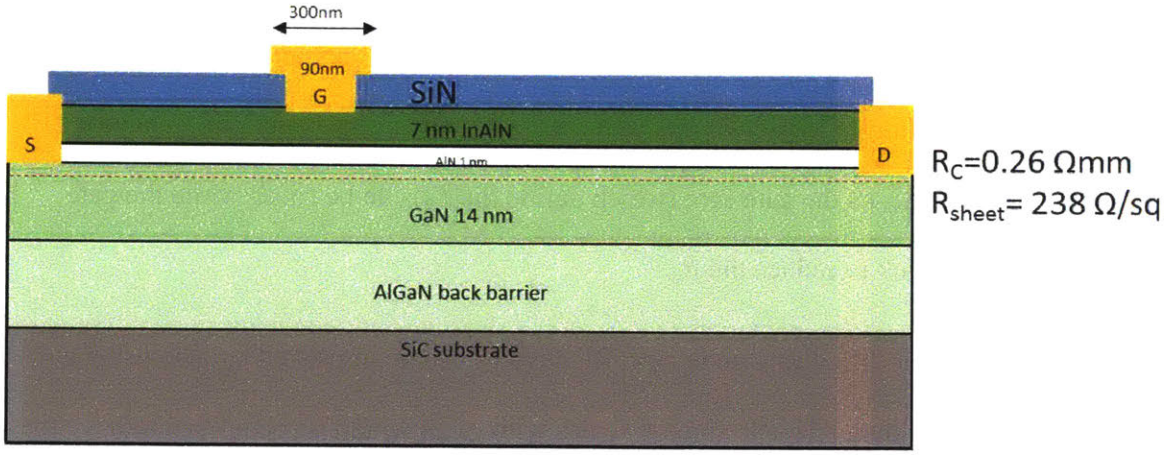

Figure 3.11: InAlN barrier GaN RF HEMT

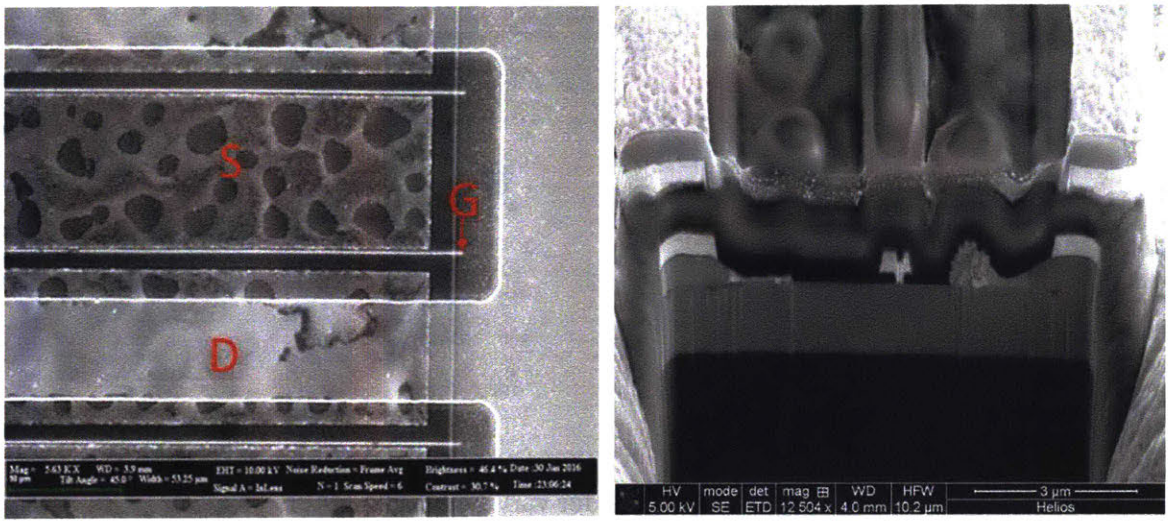

Figure 3.12: SEM of "T" gate RF HEMT

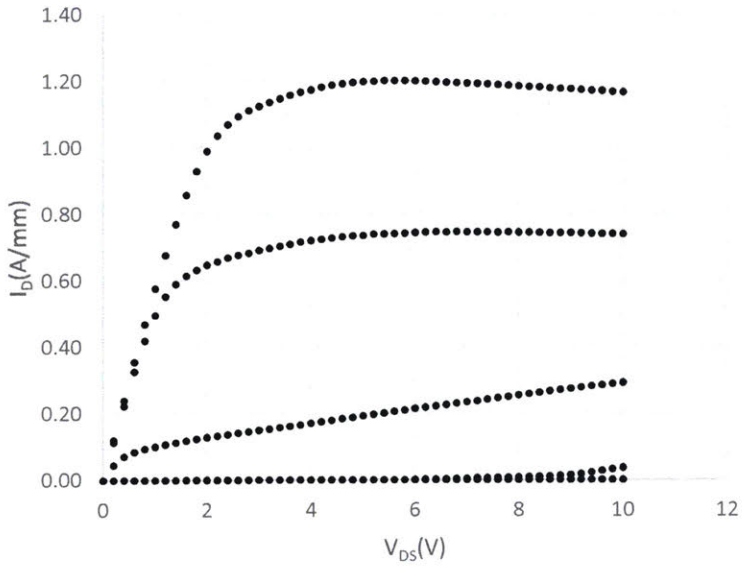

Figure 3.13: Output characteristics of RF transistor

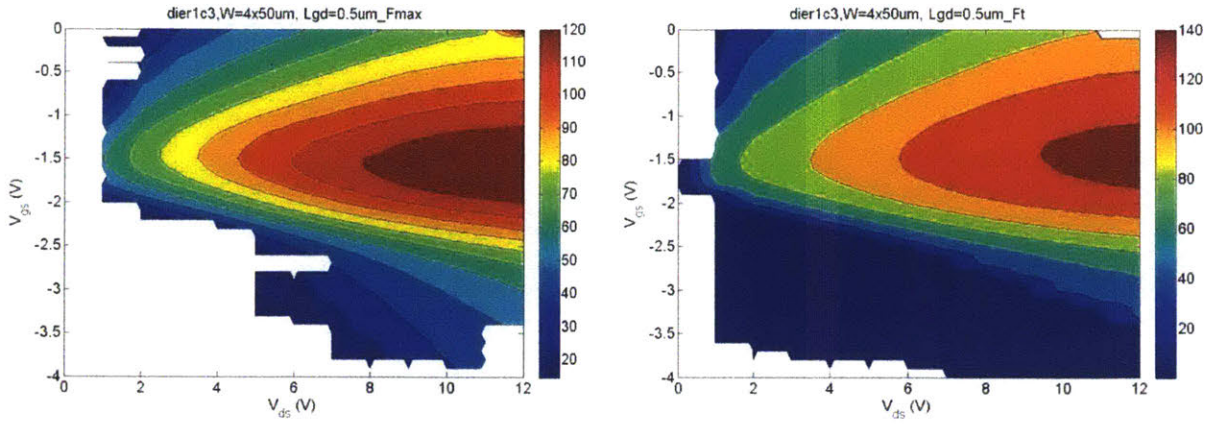

Figure 3.14: f_T and f_{max} for varying bias points

GaN IC's

Through the development of the wide-periphery devices, we employed interlayer dielectrics and interconnect metals to connect the isolated fingers of the device into a single large transistor. A natural extension of this process technology to applications is to fabricate GaN integrated circuits. The interlayer dielectric can be used to support the interconnect bridge metal layer which could be used as an interconnect metal for different devices. Furthermore, the passivation dielectric and field plate metal can be used to give the circuit another interconnect metal layer, thus expanding the potential complexity of the circuits.

In addition to the transistors, other elements are needed to complete the IC. Namely resistors and capacitors. In this process thin film NiCr resistors were used.

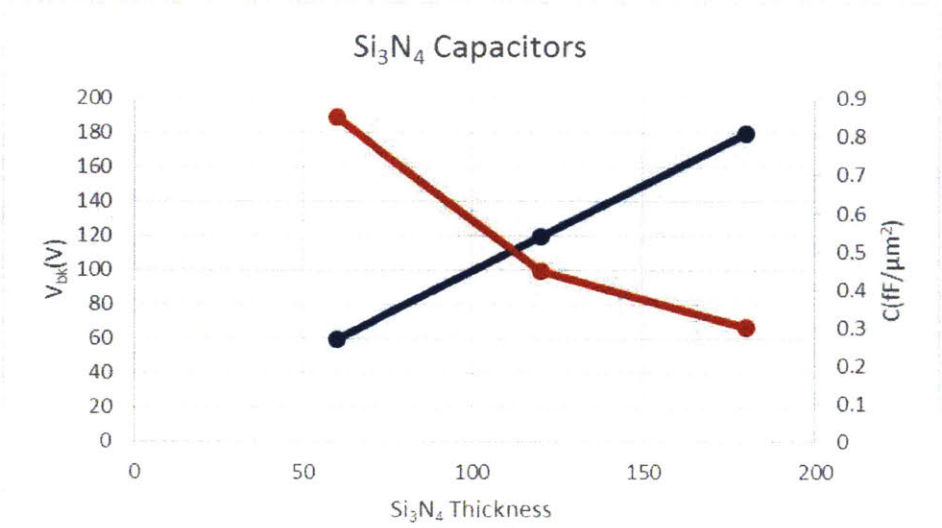

Figure 3.15: Breakdown voltage and areal capacitance for PECVD silicon nitride.

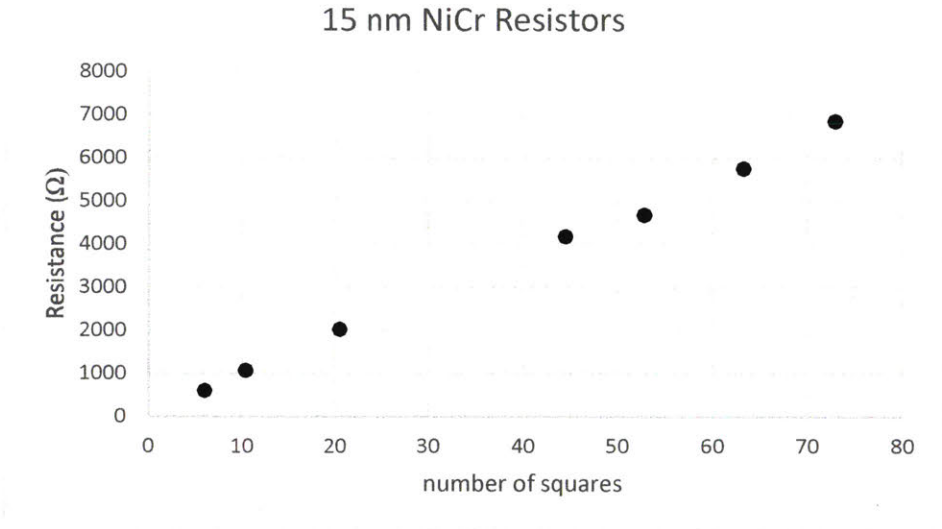

Figure 3.16: Resistance characterization for NiCr thin film resistors

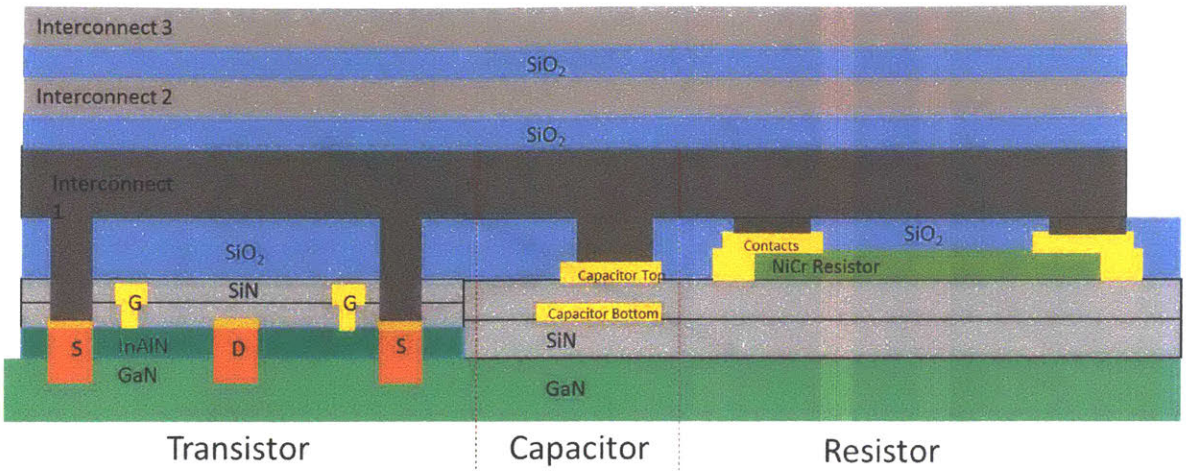

Figure 3.17: GaN HEMT based integrated circuit

The ability to fabricate GaN ICs greatly expands the number of useful applications. Two example circuits were fabricated for this thesis: a track and hold circuit and a switch mode power amplifier.

For track-and-hold sampling circuits, a trade off exists between the signal-to-noise ratio and the power consumption determined by the maximum input signal swing [7]. A high voltage signal swing can be employed if using GaN HEMTs which could achieve a high signal-to-noise ratio with less power consumption than a purely CMOS solution. Track and hold sampling circuit were fabricated in GaN on SiC for the first time in this project. This work was done in collaboration with Professor Hae-Seung Lee and SungWon Chung who designed the track-and-hold circuit. This GaN IC technology was successfully utilized in making a track-and-hold sampling circuit demonstrating over 100 dB signal-to-noise ration with 700 MHz bandwidth [7].

A much more complicated power amplifier circuit, designed by Professor Mihai Sanduleanu, has been implemented using this GaN IC technology and work is currently underway to characterize the circuit shown in Figure 3.18.

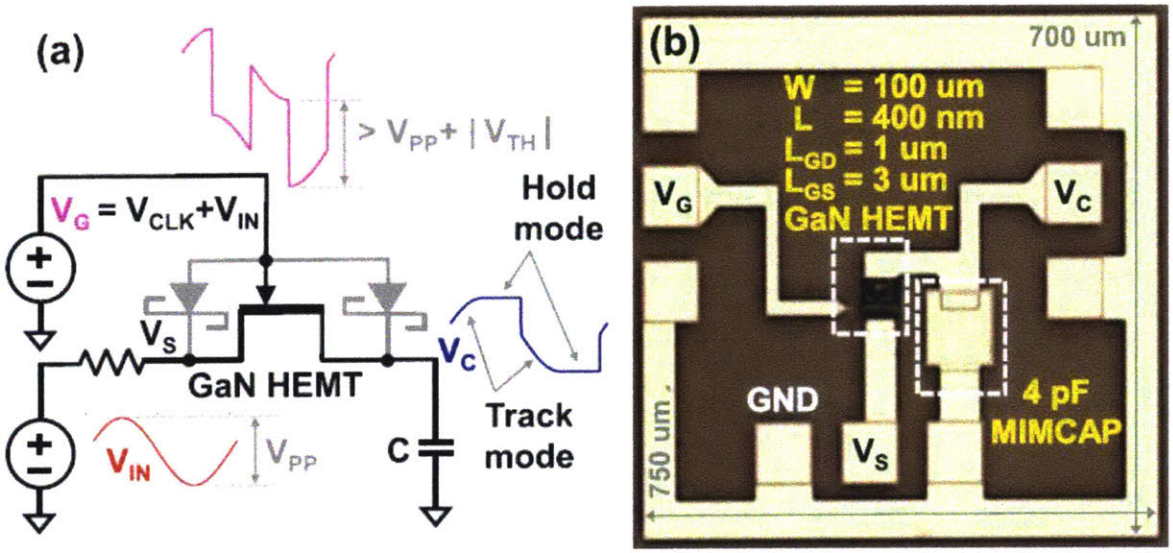

Figure 3.18: GaN HEMT track-and-hold sampling circuit

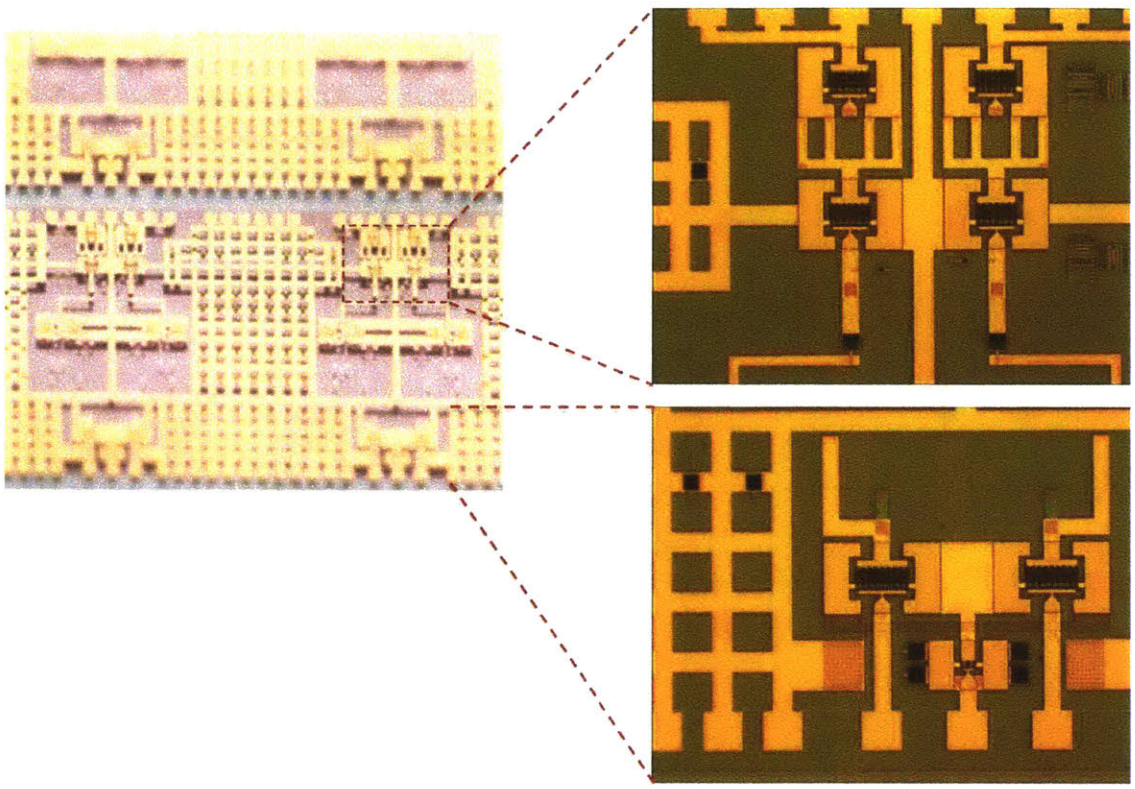

Figure 3.19: Power amplifier GaN integrated circuit

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Chapter 4: CMOS Compatible Process Optimization for 200-mm GaN on Silicon Substrate Wafers

In the twenty-five years since the initial demonstration of the GaN HEMT, research groups around the world have already shown impressive device performance in many avenues. Record power density [1] and f_T, f_{max} [2] have been achieved using GaN. Although many record breaking devices and interesting device concepts have been demonstrated by the GaN research community, most of these have been fabricated using GaN on silicon carbide or GaN on sapphire wafers of small diameter. GaN can be grown on silicon, silicon carbide, sapphire, or free-standing gallium nitride, each with their own unique material properties (summarized in Table 4.1) and advantages/disadvantages.

Sapphire has been the substrate of choice for most epitaxially grown GaN-based LEDs as well as early research level electronics [3]. Relatively low cost 2- and 4-inch substrates have been readily available to support these endeavors. Although it is not particularly well lattice matched (13% mismatch), sapphire substrates have led to impressive power densities [4]. However low thermal conductivity is an issue for high power devices and lack of low-cost larger wafers may hinder more widespread use.

Silicon carbide has proven to be a very popular choice for GaN growth substrates, especially for electronics. Silicon carbide is more closely lattice matched to GaN than any of the other commonly used foreign substrates (only 3.4% mismatch), leading to lower defect density [3]. Furthermore the thermal coefficient of expansion is lower so there is less cracking upon cooling. The high thermal conductivity also bodes well for high power devices. Unfortunately larger wafer diameters are still very expensive and only available in limited quantities.

Bulk gallium nitride crystals offer the smallest defect density, as there is no lattice mismatch. However, these wafer substrates are even more expensive than SiC substrates. It is uncertain if the reduction in defect density can justify the price.

Table 4.1: Substrate materials for GaN epitaxial growth

Material	Lattice Constant a (Å)	Mismatch to GaN (%)	Themal conductivity, κ_L ($Wm^{-1}K^{-1}$)	Coefficient of thermal expansion (10^{-6} K^{-1})	Isolation (resistance) (Ω cm)	Reference
GaN	3.189	0	130	5.59	$\geq 10^9$	[5]
6H SiC	3.08	3.4	490	4.2	$\geq 10^{11}$	[5]
Sapphire	$4.758/\sqrt{3}$	13	50	7.5	-	[6]
Silicon	5.4301	17	150	3.59	$\sim 10^4$	[5]

Si is by far the most widely available for GaN. It is very inexpensive and widely available in large wafer diameters. However, the growth of GaN on Si has proven to be the most difficult because of the large lattice mismatch (17%) [3]. The large difference in coefficients of thermal expansion between GaN and Si also leads to cracking of the film upon cooling from the greater-than-1000°C growth temperature. To alleviate these problems AlN interlayers, graded buffers structures, and AlGaN/AlN superlattices have been employed [7]. The increased growth complexity should be offset by the dramatic decrease in overall cost that could be wrought from using large diameter wafers and the ability to use more advanced CMOS processing lines.

Many of the state-of-the-art GaN devices have been processed on small wafer diameters using SiC or sapphire substrates. While these are acceptable for research devices or small niche markets that can accept high cost, the wide adoption of gallium nitride would be excelled by using silicon substrates. To drive down the cost it would be greatly beneficial to have gallium nitride devices on 200 mm Si substrates with a Si-CMOS-compatible process flow that would allow the wafers to be run through a Si fabrication facility.

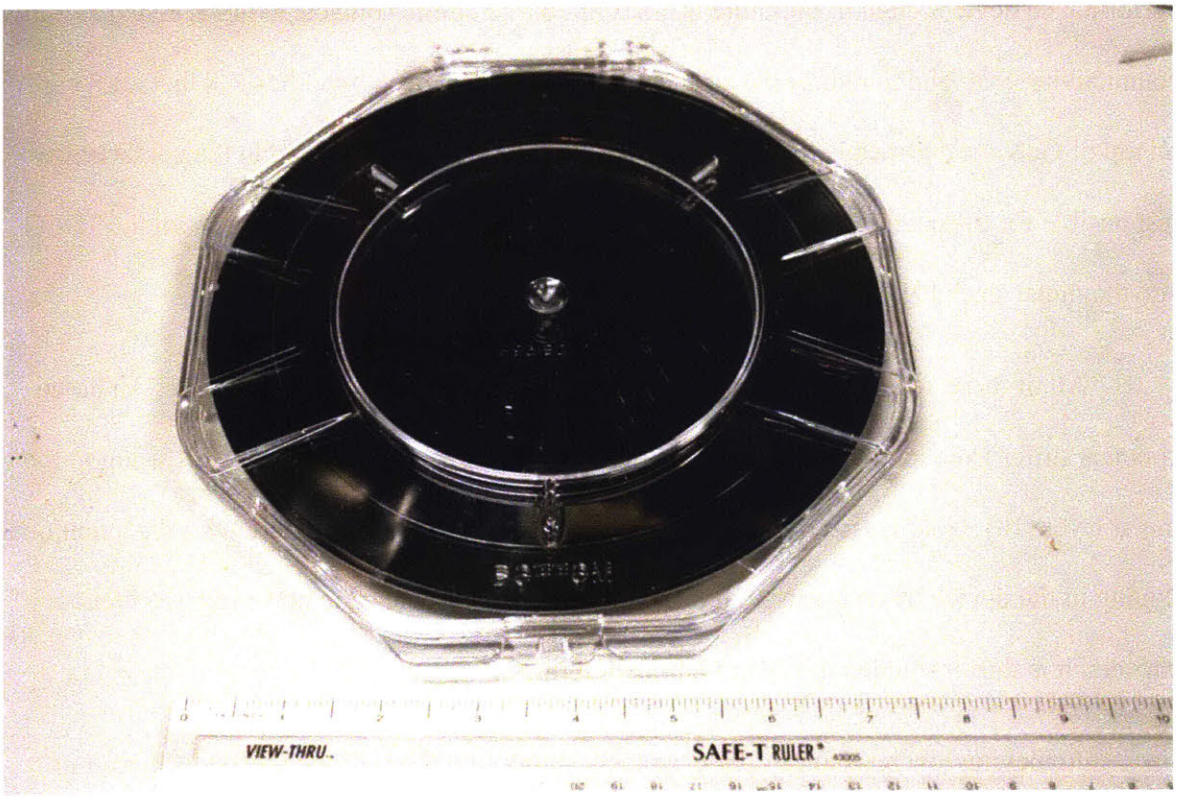


Figure 4.1. AlGaN/GaN HEMT structure grown on 8" Si substrate

Au-free ohmic contacts

Introduction to Au-free ohmic contacts

One of the key steps in obtaining a fully CMOS compatible device process flow is developing a gold-free ohmic contact process. Traditionally, AlGaN/GaN HEMTs have used Au-based metal stacks annealed at high temperatures (above 800°C) [8]. Many of the record performance devices cited in literature utilize gold based ohmic contacts. Gold is added as a high conductivity layer and to reduce the surface oxidation. It has been hypothesized that alloying Au on top of GaN creates metal spikes that facilitate the ohmic contacts. Gold in the contacts are responsible for the contact roughness, providing a preferential contact path between the 2DEG and the metal stack [9].

All of these advantages of gold as a contact material are not without a price. Au based contacts suffer from long term degradation thought to be attributed to Au inter-diffusion in the metal layer [10]. Gold is also a deep level trap in silicon and would interfere with the intentional doping in the device by compensating the charge as well as reduce the non-radiative lifetime of carriers, it is thus forbidden in CMOS fabrication lines..

Achieving low resistance ohmic contacts without gold has proven difficult. Lee *et al.* have use Ti/Al/W annealed 870°C to obtain contact resistance of 0.49 Ωmm [11]. While very promising, low contact resistance obtained at a lower annealing temperature would be desirable, to meet the thermal budget imposed by other processes. A lower annealing temperature would also facilitate smoother surface morphology [12]. IMEC has shown Au-free contact resistances below 1 Ωmm using a Ti/Al/TiN based metallurgy and an alloy temperature of 550°C [13]. In that work, a single recess of the barrier was performed down to the 2DEG.

Seeing the promising results obtained by using a barrier recess, we have conducted a study testing the resulting contact resistance for different recess depths. The goal of this work was to develop a reproducible, reliable, uncomplicated ohmic contact process aiming for a minimum contact resistance.

Characterization of Ohmic Contacts

The key metric being optimized in this study was the contact resistance, R_C. To quantify this resistance, the transfer length method (TLM) was employed. The transfer length method, originally proposed by Shockley [14] uses a test structure that consists of metal-semiconductor contacts of length L and width Z with unequal spacing distances d_x, between the contacts, as shown in Figure 4.2. The voltage is measured between two adjacent contacts using 4-point Kelvin method and the total resistance is extracted.

$$R_T = \frac{R_{sheet}d}{Z} + 2R_C$$

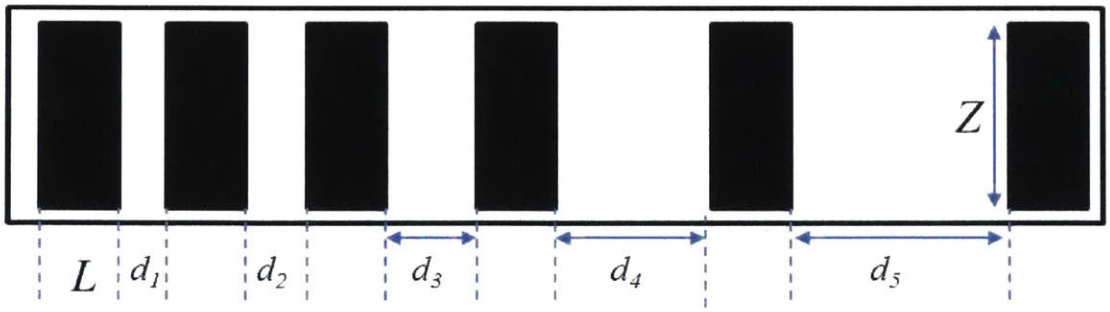


Figure 4.2: Contact test structure for Transfer Length Method

The resistance between the different contact spacing is measured and plotted against the spacing distances as shown in Fig. The extrapolated intercept at d=0 is $2R_C$, as each contact

contributes its contact resistance, while the intercept at R_T=0 gives twice the transfer length – d=2L_T.The slope gives the sheet resistance.

$$\frac{\Delta R_T}{\Delta d} = \frac{R_{sheet}}{Z}$$

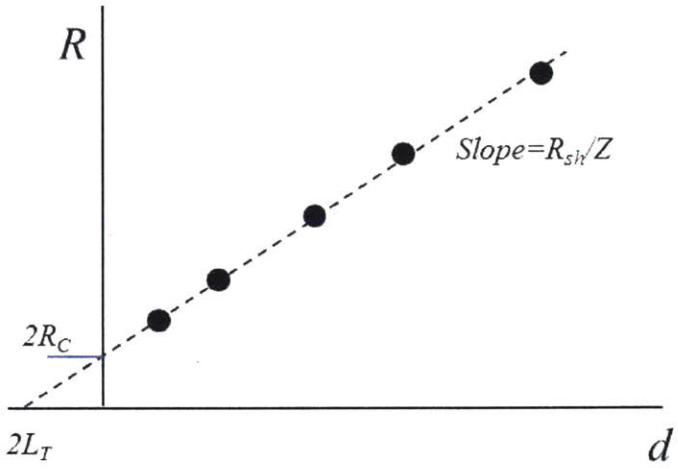


Figure 4.3: Plot to extract contact resistance

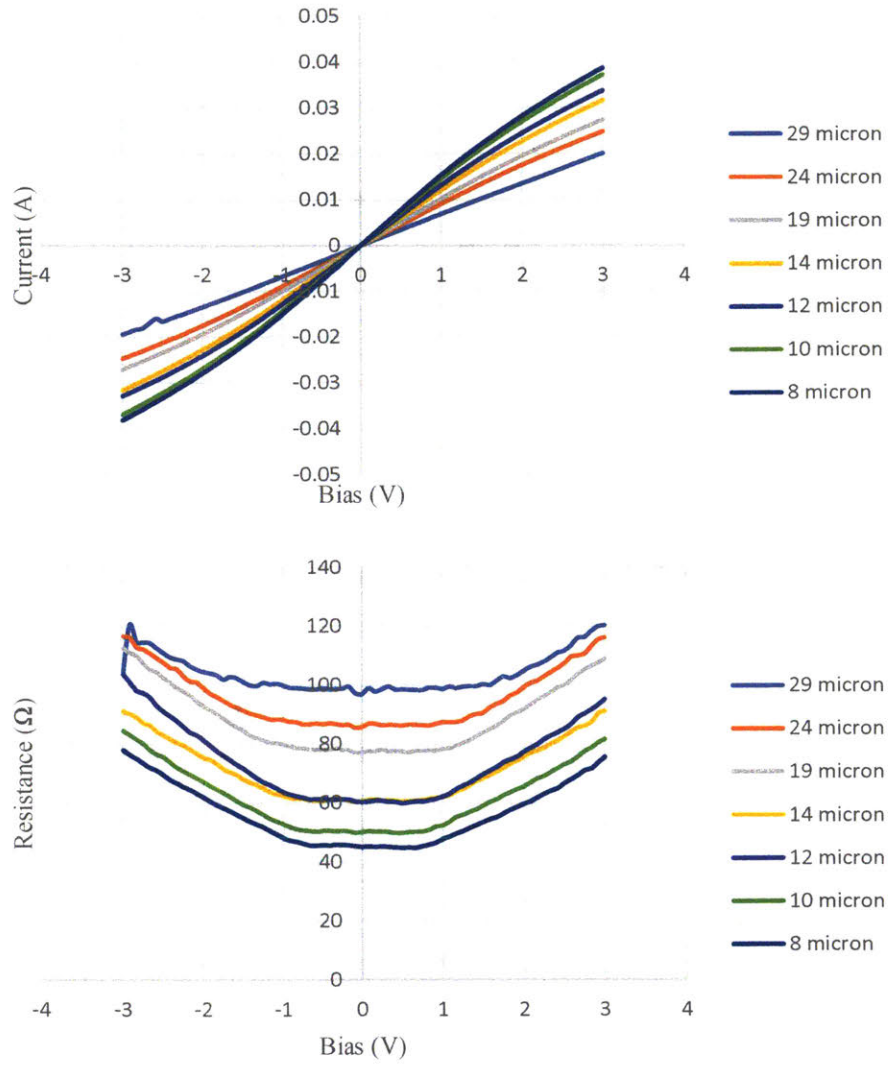


Figure 4.4: Experimental IV curves of TLM pads (top) and corresponding resistance sweeps (bottom)

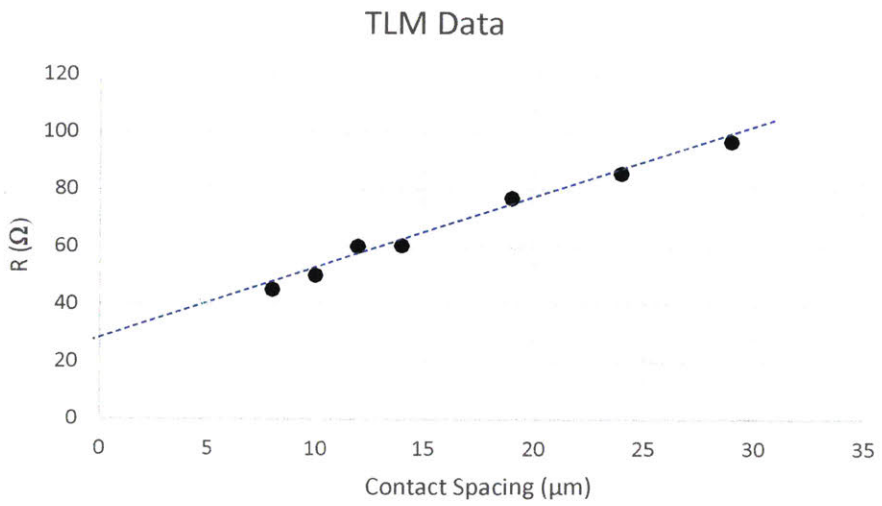


Figure 4.5: Extrapolation of contact resistance with experimental TLM data

Optimization process

The wafer used in this study is shown in Figure 4.6. To start, the sample was cleaned in a piranha solution of 1 part hydrogen peroxide to 3 parts sulfuric acid for 10 minutes, rinsed in de-ionized water for 2 minutes, and dried with nitrogen. The samples were then loaded into a PECVD chamber to deposit silicon nitride which would act as a passivation layer and partial etch mask for later steps. Eighty-nm of high frequency silicon nitride was deposited. Mesa isolation structures were patterned and etched using CF_4 plasma to dry etch the silicon nitride passivation layer and BCl_3/Cl_2 plasma to etch the AlGaN/GaN.

Next ohmic recess opening patterns were made on the sample with SPR-700 resist and photolithography. CF_4 based plasma was used to completely etch the silicon nitride mask in the opened regions and inductively coupled BCl_3/Cl_2 based plasma was used to the GaN top layer, AlGaN barrier, and GaN channel with different target etch depths. This chlorine plasma recipe (shown in Table 4.2) is significantly less powerful than the mesa isolation etch step, so as to

result in a lower etch rate to more accurately control the sensitive etch depths for this step, which would be the primary optimization variable.

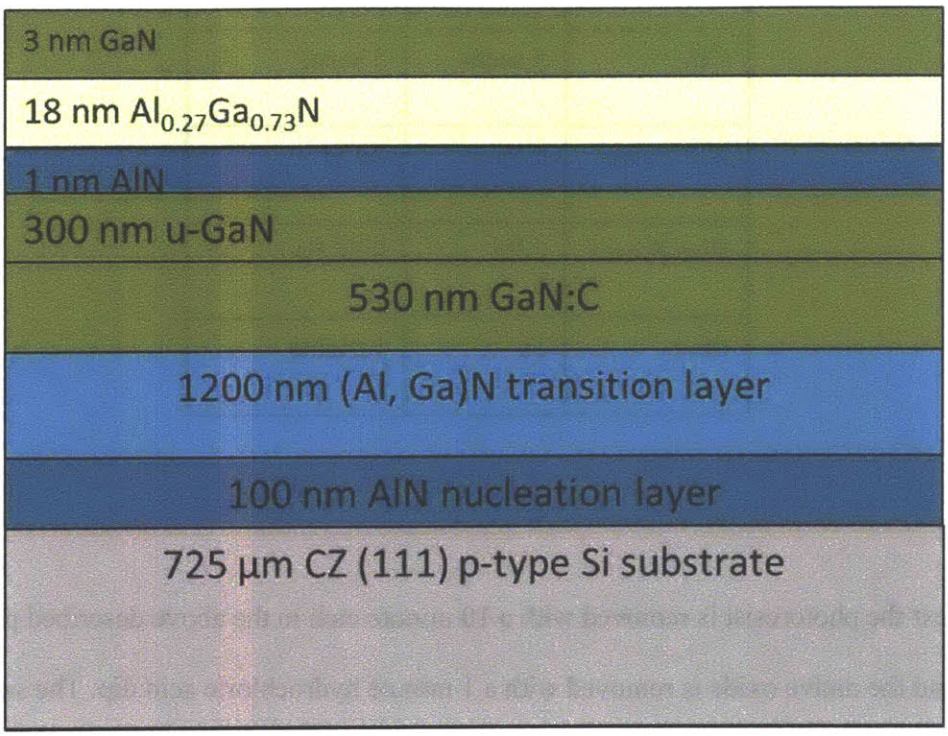


Figure 4.6: AlGaN/GaN on 200 mm Si (111) wafers used for this study.

Table 4.2: AlGaN/GaN Ohmic Recess etch recipe

	Step 1	**Step 2**
BCl3	10 sccm	10 sccm
Cl2	5 sccm	5 sccm
ICP Power	0 W	20 W
Bias Power	2 Pa	0.25 Pa
time	5s	variable

Next the photoresist is removed with a 10 minute etch in the above described piranha solution and the native oxide is removed with a 1 minute hydrochloric acid dip. The samples are loaded into the sputtering deposition chamber (with varying amounts of time between the acid cleans and the sample loading to understand the effects of these steps on the contact resistance). Varying thickness of titanium and aluminum were deposited.

Ohmic pads were patterned using SPR-700 resist and photolithography. The Ti/Al metal was etched in BCl_3/Cl_2 electron cyclotron resonance plasma. The remaining photoresist was removed with a 2 minute dip in nanostrip. The samples were annealed in a rapid thermal anneal system for 5 minutes at 550°C. The contact resistance was measured using the TLM procedure described in the preceding section.

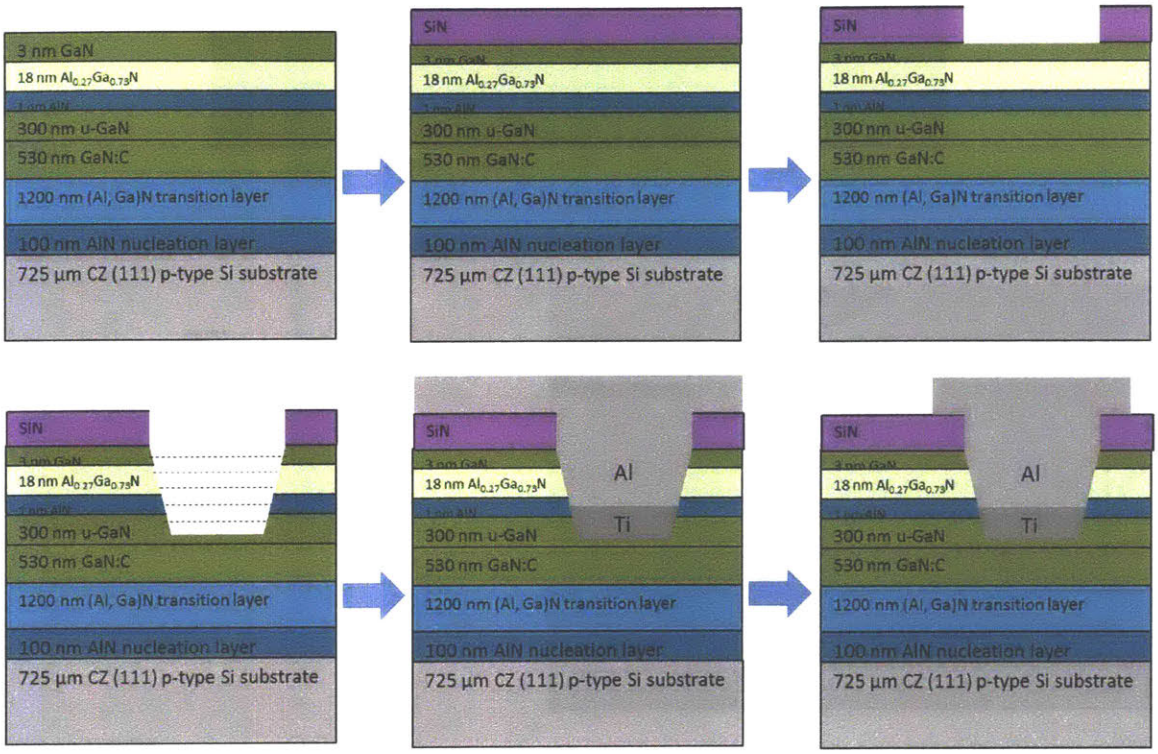
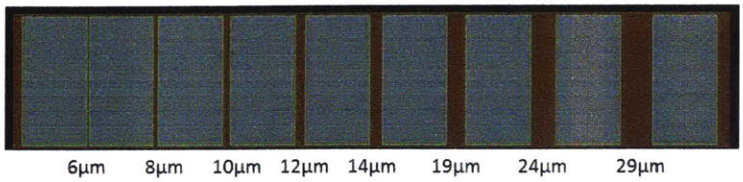


Figure 4.7: Process flow for ohmic contacts

Optimization Study

As described in Chapter 2, ohmic contacts are formed by increasing the tunneling probability through the Schottky barrier that is formed at the metal-semiconductor junction. This can be achieved by increasing the doping density (N-vacancies in the case of GaN) or lowering the Schottky barrier height. Recessing the AlGaN is believed to make this barrier thinner [15] and has shown effective to increase the tunneling probability [16]. A comprehensive study of the effect of recess depth on contact resistance was performed. Different depths were etched in the ohmic openings as described above and Ti (20nm)/Al (100 nm) was sputtered, patterned, etched and annealed. A cross-sectional scanning electron microscope image of the recessed contact is shown in Figure 4.8 and the contact resistances were collected and shown in Figure 4.9.



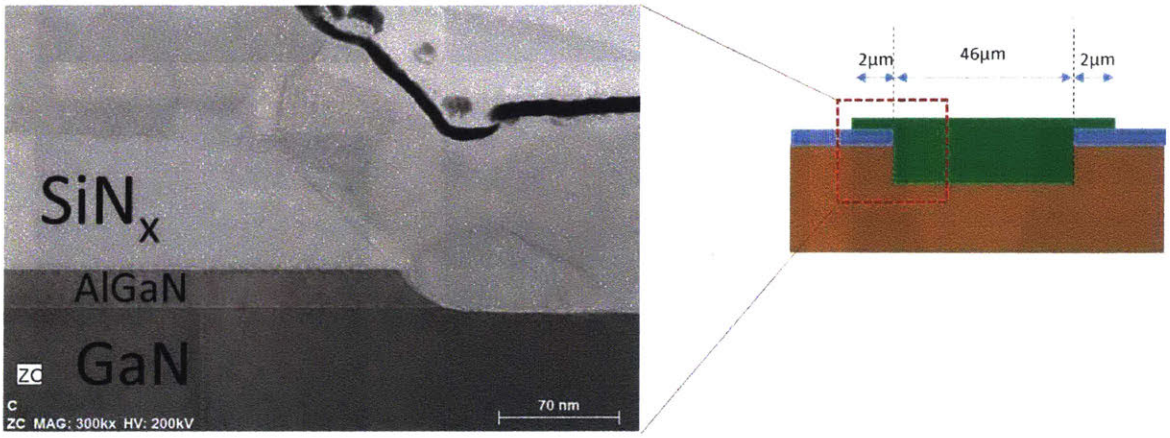


Figure 4.8: TLM pattern used, dimensions of contact pad and cross-sectional SEM of the ohmic contact

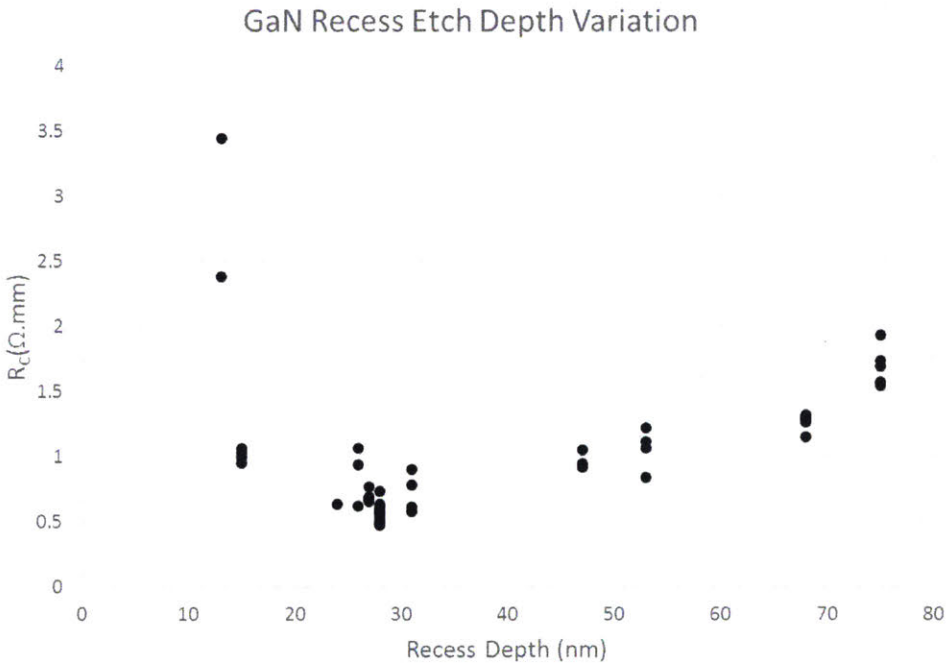


Figure 4.9: Contact resistance in AlGaN/GaN HEMT for varying recess depths

As can be seen from the figure, a recess etch is necessary (unrecessed contacts have R_C in excess of 5 Ωmm) and by recessing into the AlGaN, the contact resistance quickly drops to manageable levels. Contact resistance reaches a minimum of 0.5 Ωmm at an etched depth 27 nm. The contact resistance slowly increases at deeper depths, but remains below 1 Ωmm over a recess depth of about 20 nm. This wide process window is reassuring as it is not critical to hit an exact etching depth. The optimal depth of ~27 nm is below the AlGaN barrier and into the GaN channel, suggesting that an ohmic contact mechanism may be based on sidewall contact. An experiment was performed to confirm this.

Two samples were processed in unison: one sample had the Ti/Al pads patterned so that they would overlap the recess, thus conformally contact the sidewall of the recess; the other sample had the Ti/Al pads patterned so as to not have any sidewall contact as shown in Figure 4.10. The sample without sidewall contact did not show ohmic contact, while the conventional sample with sidewall contact had R_C=0.7 Ωmm.

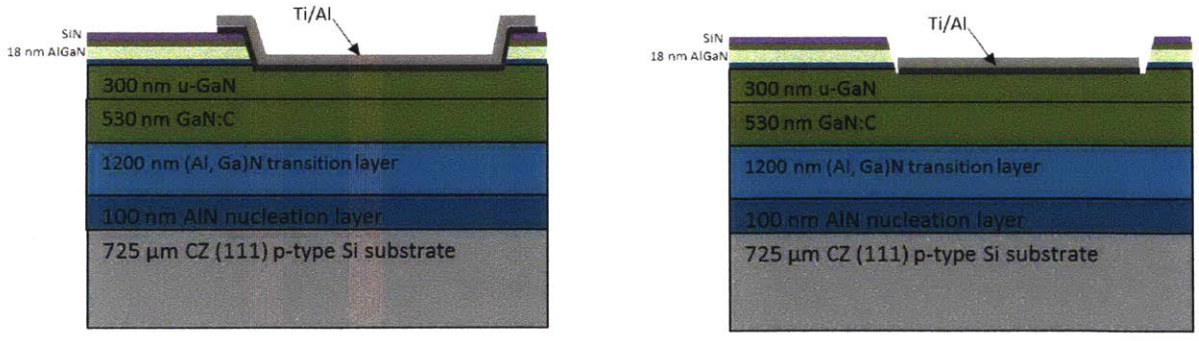


Figure 4.10: Contacts to test contribution of sidewall

Progressively more aggressive cleaning steps (in between the recess etch and metal deposition) were performed to observe the effects of each acid component on the contact resistance. Sample 1 was placed in the sputtering chamber after recess etching and solvent clean. Sample 2 had a 10 minute piranha clean after recess etch and before metal deposition. Sample 3 had the piranha solution, HCl solution, and was left exposed to open air for 60 minutes before being loaded into the metal deposition chamber. Sample 4 and 5 had piranha solution, HCl solution, and were left in open air for 30 min and 5 min respectively. The contact resistances of these samples is summarized in Figure 4.11. As is seen from the Figure a piranha clean greatly reduces the R_C, suggesting that some organic contamination present on the sample (without piranha) degrades the contact. HCl is effective in further lowering the R_C, which indicates a surface oxide forms to prevent good ohmic contact.

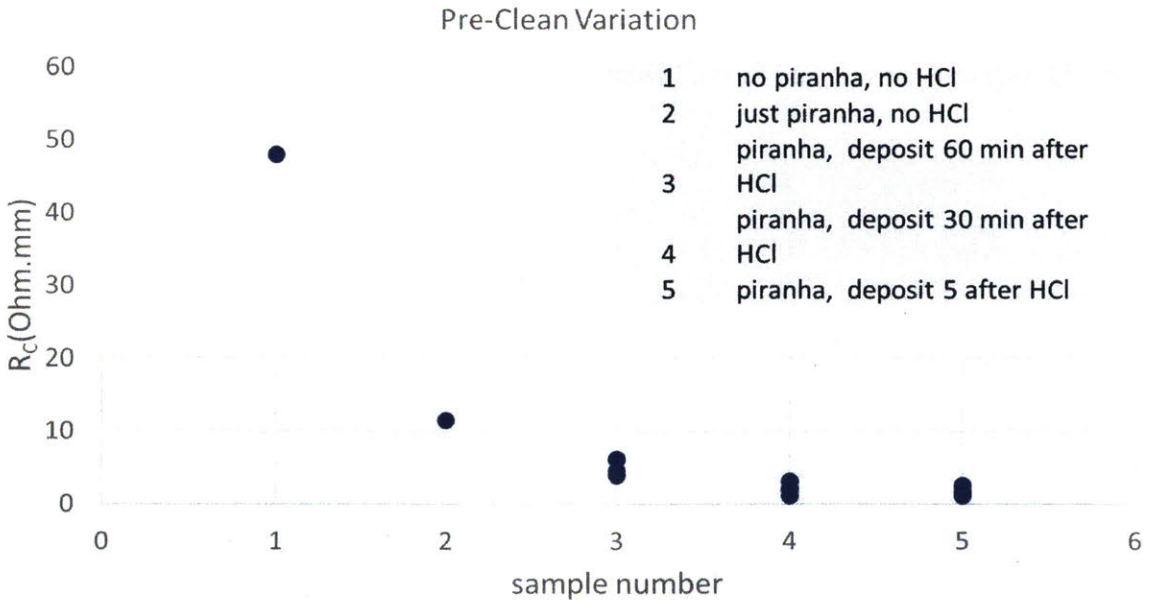


Figure 4.11: The effect of acid clean steps on contact resistance

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Chapter 5: Heterogeneous Integration of Gallium Nitride Power Switch Development

Introduction and motivation

Silicon CMOS technology has been at the forefront of the microelectronics revolution, benefitting from years of process development allowing for advances in device scaling and integration density. It is practically unparalleled in the fields of memory and logic. Furthermore, it has reached the point of ubiquity that nearly every electronic system has at least one Si chip running them and that will be the case for the foreseeable future. The International Technology Roadmap for Semiconductors (ITRS) states that "if the performance requirements can be satisfied by silicon they will be, primarily for cost and integration density reasons [1]."

With this established, there is however, a strong need for alternative semiconductor electronics. Again the ITRS states that "...[III-V] devices will continue to serve niche or performance-driven applications where silicon performance is not adequate" [2]. One of these "performance-driven applications" is power electronics. Deeply scaled Si CMOS faces challenges in high-voltage and high-power density applications. Gallium nitride's strength is in these very areas. However, in most cases, it would not be financially prudent to manufacture entire systems (including control circuits, logic, etc.) in gallium nitride.

It would be best to leverage best of both worlds through an integration scheme. Fabricating power amplifiers and power conversion switches in gallium nitride, while keeping digital control circuitry in highly scaled silicon would enable unprecedented levels of performance. This can be accomplished by fabricating discrete silicon and advanced semiconductor chips and connecting them together in a multichip modules [3]. This has been the solution for cellular telephones, which have both Si and GaAs chips. Chapter 3 demonstrated an

examples of a multiple chip systems by bonding power transistors on a GaN chip to control circuitry on a Si CMOS chip. However, size constraints, losses in the chip-to-chip interconnections, and cost all impose limitations on multichip modules [1]

Heterogeneous direct integration is a more attractive option to leverage the best part of each technology. Losses in the chip-to-chip interconnects and imprecise placement of the devices can be avoided by having the GaN and Si circuits on the same wafer. Several different approaches to integrating Si CMOS devices and GaN devices have been attempted and demonstrated, each presenting their own unique challenges and advantages, as described below.

There has been large interest in growing high quality GaN on Si substrates (as discussed in the previous chapter). It might seem a natural extension to simply fabricate silicon CMOS devices on the Si substrate on which the gallium nitride was grown. There is an inherent problem with this approach because the preferred Si orientation for GaN growth is (111) as the surface has a threefold symmetry and hexagonal atomic arrangement to align closer to the hexagonal crystal of GaN [4]. The preferred orientation for CMOS is (100) which has fourfold symmetry leading to two differently aligned domains [5]. GaN films grown on this showed extremely rough surfaces and higher dislocation densities compared to films grown on (111) [4]. Silicon transistors fabricated on (100) wafers have shown higher electron mobility and reduced interface trap density [6]. Attempts at CMOS in other orientations have shown slight improvement in hole mobility at the expense of increased interface traps and degraded reliability due to these interface traps [7].

Despite the challenges stacked against this method, there have been attempts of processing MOS devices in the Si (111) substrate used to grow the GaN as shown in Figure 5.1 [8]. The performance of the Si devices suffer at the expense of the GaN devices in this approach.

NMOS devices had higher D_{it} and poor subthreshold sweep [8]. Furthermore, the GaN stack consisted of alternating AlN and GaN stress management layers, 1.4 μm GaN buffer, and a 200 nm GaN channel layer for a total thickness of about 1.5 μm above the silicon surface. This large height difference would result in a highly non-planar wafer that would preclude the use of state-of-the-art lithography due to depth of focus problems.

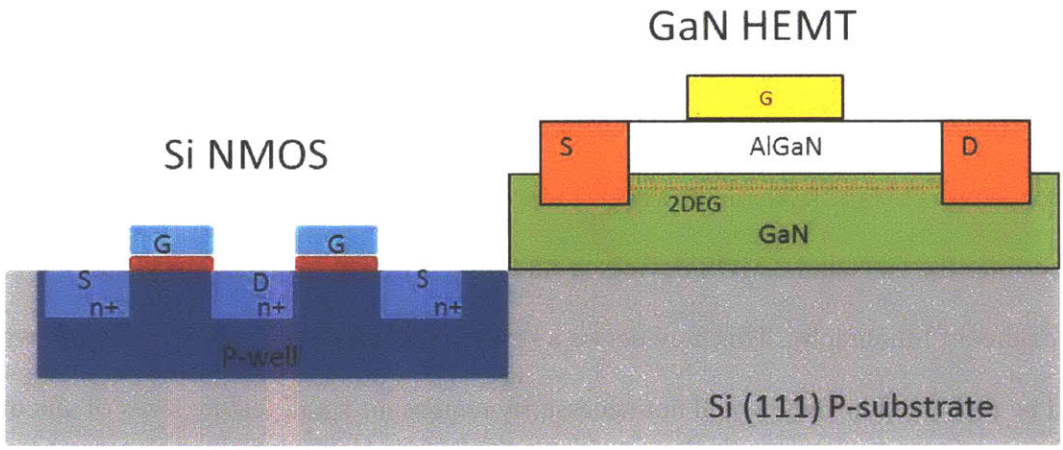

Figure 5.1: Si CMOS device fabricated in Si (111) for heterogeneous integration with GaN HEMT

Another approach is the layer transfer and wafer bonding method, where a Si (100) wafer is bonded to an already grown AlGaN/GaN on Si (111) wafer and the original substrate is removed. This approach decouples the growth of GaN and Si, so the material growth constraints are relaxed (i.e. the GaN can be grown on any orientation of Si or even sapphire or SiC, since the CMOS quality Si wafer will be bonded to it and often the starting substrate is removed anyway). The layer transfer method has been attempted with a few different bonding materials. Wong et al. took advantage of the relaxed constraints by growing GaN on sapphire and bonding to Si with a Pd-In metallic bond [9]. Funato et al. grew GaN on GaAs substrates and bonded to Si with

AuGe for the purpose of integrating GaN-based optoelectronics with Si-based microelectronics [10]. One of the downsides of these technologies is the relatively low melting temperatures of the bonding materials. As such, these methods would only be suitable to bonding already processed Si-devices to processed GaN devices so the wafer set does not have to undergo the high temperatures of typical CMOS diffusion processes.

Silicon oxide has proven to be a more thermally robust bonding material. This technology has been used to demonstrate GaN-Si integration scalable up to 4-inch wafers by bonding to a silicon (100) wafer as shown in Figure 5.2. A hybrid power amplifier was demonstrated using this technology [11] [12]. Again, however, there is the disadvantage of the nonplanarity of the surface since the GaN and CMOS devices would be at different heights, thus limiting the use of state-of-the-art lithography. This may not be a severe problem since the power devices which would be processed in GaN would not necessarily require the small feature sizes of silicon CMOS devices.

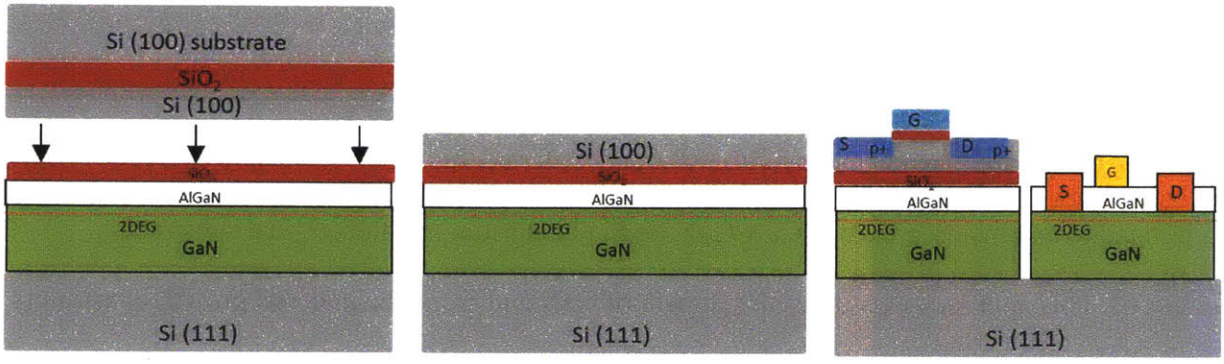

Figure 5.2: Si substrate bonded to GaN HEMT wafer through the use of SiO_2; substrate is then removed.

Finally, another approach utilizes a double bonded silicon on insulator (SOI) wafer as the means of achieving heterogeneous integration. A bonded Si (100) device layer to a Si (111)

substrate with buried oxide separator provides a platform where both the Si device processing and GaN growth can be done with their preferred Si type. Patterned windows are opened down to Si (111) and GaN can be selectively grown these opened windows. The growth of GaN in etched windows should eliminate the height difference found in the preceding methods and result in wafer planar enough to allow the use of state-of-the-art lithography. Growth of GaN layers by molecular beam epitaxy (MBE) on SOI wafers with prefabricated CMOS devices was used in [13]. The prefabricated CMOS devices imposed a strict thermal budget on the growth of the gallium nitride since long exposure to high temperatures (as is usual in nitride growth) would cause silicon dopant redistribution. To satisfy this thermal budget, the group in [13] used a low temperature plasma molecular beam epitaxy (~750 °C), which increased cost and reduced wafer throughput.

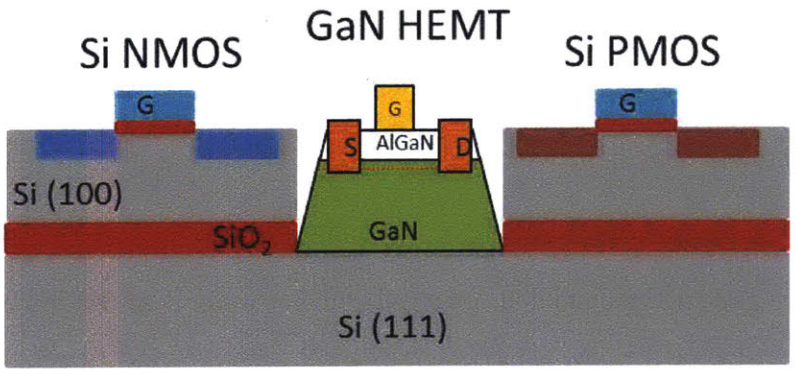

Figure 5.3: GaN HEMT grown by plasma enhanced MBE in windows on Si (111)

MOCVD GaN on SOI

In this thesis, we have demonstrated in collaboration with IBM Research a new approach to monolithically integrate GaN and Si devices. Like the work in [13], our approach also involved bonded SOI wafer with a Si (111) substrate and Si (100) device layer with windows opened to access the (111) layer to selectively grown GaN. However, unlike [13] this approach grows the GaN before any CMOS processing is done. In this way, high temperature MOCVD can be used with no temperature restrictions, ensuring the highest quality of GaN possible.

Beginning with double-bonded SOI wafers, a low temperature oxide is deposited as a masking layer. The windows are patterned and reactive ion etched approximately 2 μm deep into the silicon substrate. The masking layer is stripped and 160 nm of silicon nitride is grown to act as a diffusion barrier. Photoresist is deposited and the SiN on the protective oxide mask is removed by CMP, leaving the SiN in the etched windows only. AlGaN/GaN is grown resulting in high quality material in the windows and a rough unusable poly-HEMT outside the windows (which can be removed by CMP in later steps). This process flow is detailed in Figure 5.4. An image of this patterned growth done on a full 200 mm wafer is shown in Figure 5.5 and top-view and cross-sectional view of the GaN window shown in Figure 5.6.

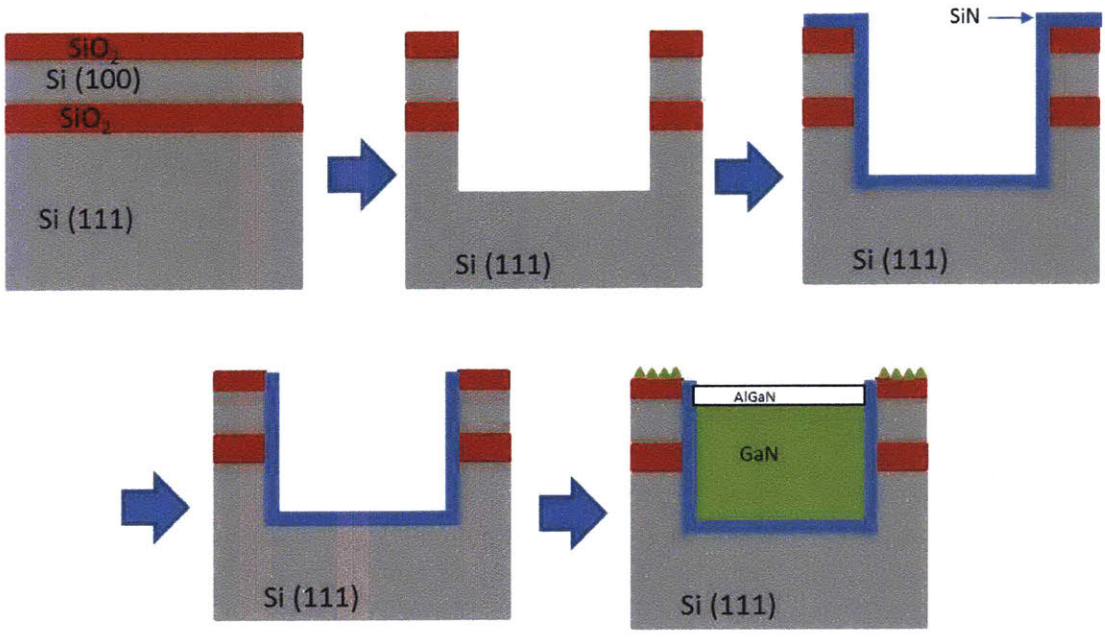

Figure 5.4. Growth of Patterned GaN on SOI wafer

(a)

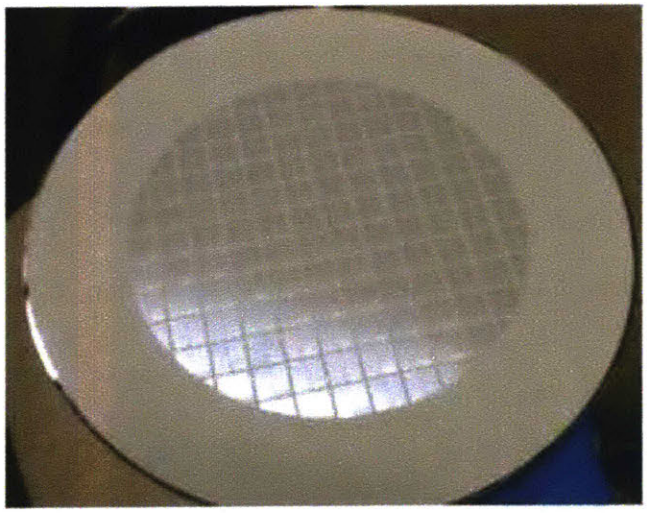

Figure 5.5: Patterned GaN Windows grown on 200 mm SOI wafer

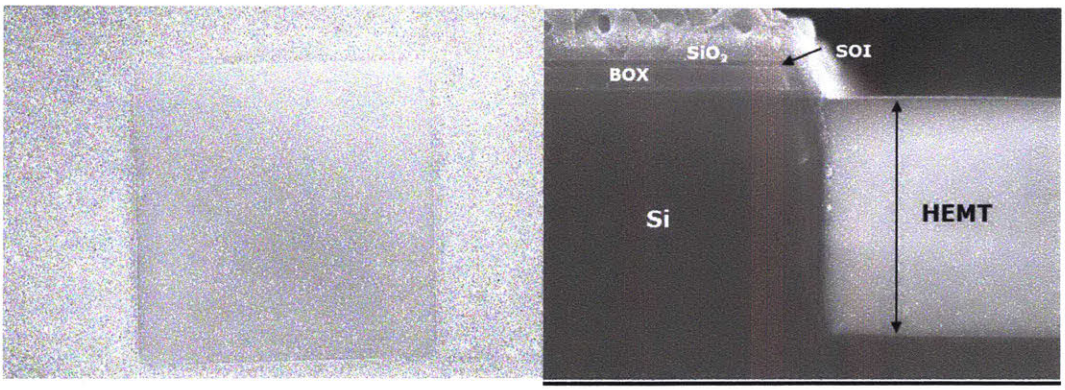

Figure 5.6. SEM and cross section of patterned GaN window

Material Characteristics and 2DEG transport properties of GaN windows

At the onset of this project, the optimum size of the patterned GaN window was undetermined. Considerations such as Si device proximity would be important, but it was also crucial to examine the material properties and device performance of transistors fabricated in different sized GaN windows. A comprehensive study would help guide the decision of what sized GaN windows would ultimately be used or at least understand potential tradeoffs.

As shown in the Figure 5.7, an array of patterned GaN windows, differing in size and shape was grown. Squares with side length of 25 μm, 50 μm, 100 μm, 150 μm, 200 μm were grown.

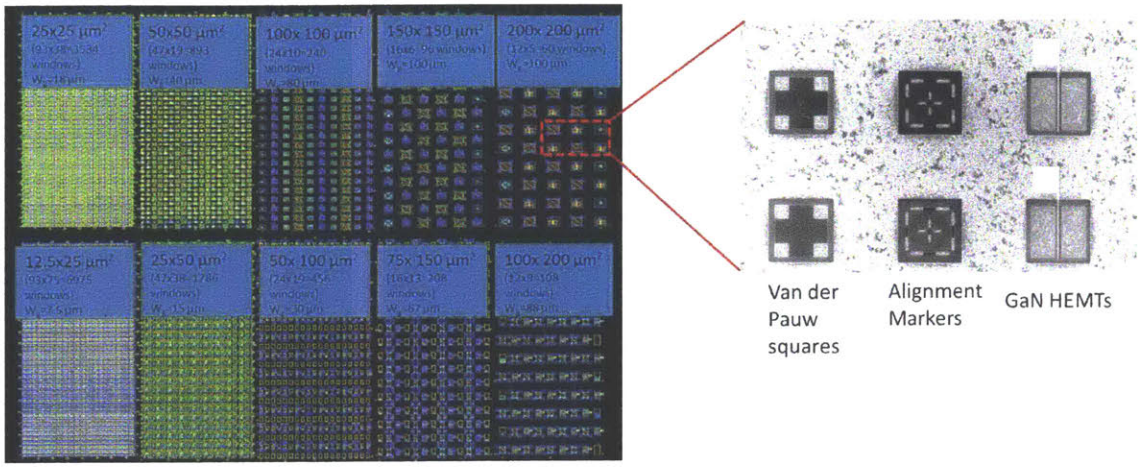

Figure 5.7. Patterned GaN Window and device layout

Van der Pauw structures were fabricated to test the electron Hall mobility (results shown in Figure 5.8) and 2DEG concentration (results shown in Figure 5.9). This entailed mesa isolation and ohmic contact formation as detailed in the earlier chapters. Also contact pads that extended outside the GaN windows so probing could be performed.

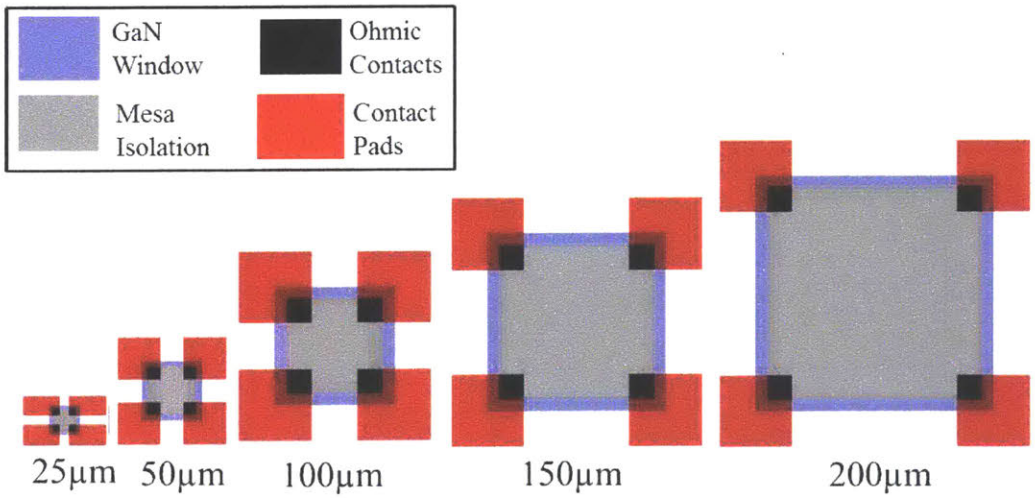

Figure 5.8: Van der Pauw structures for measuring 2DEG density and Hall mobility

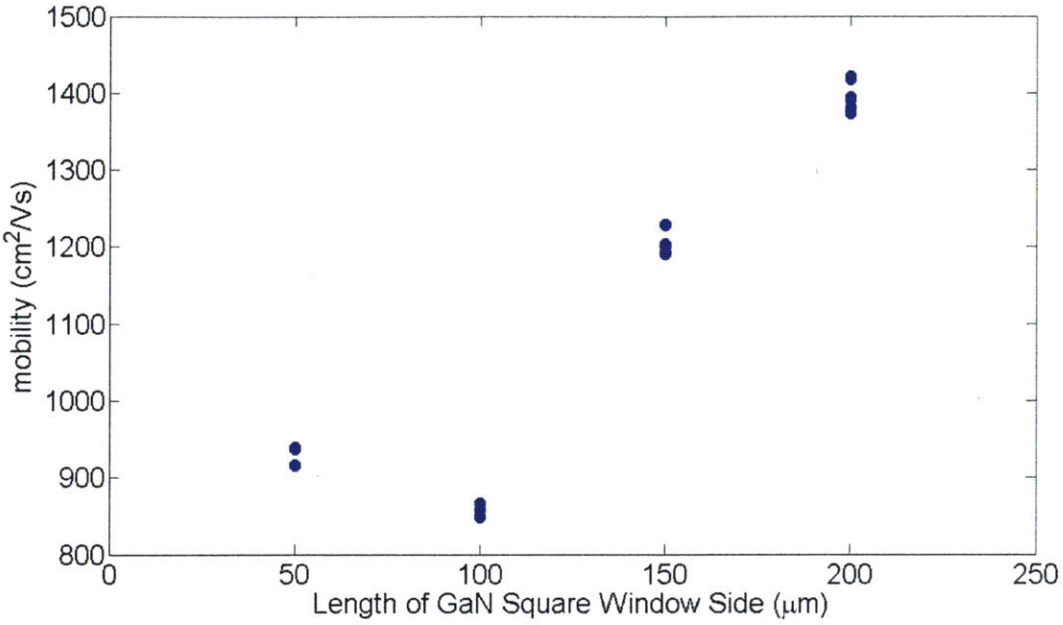

Figure 5.9: Hall mobility as a function of GaN window size.

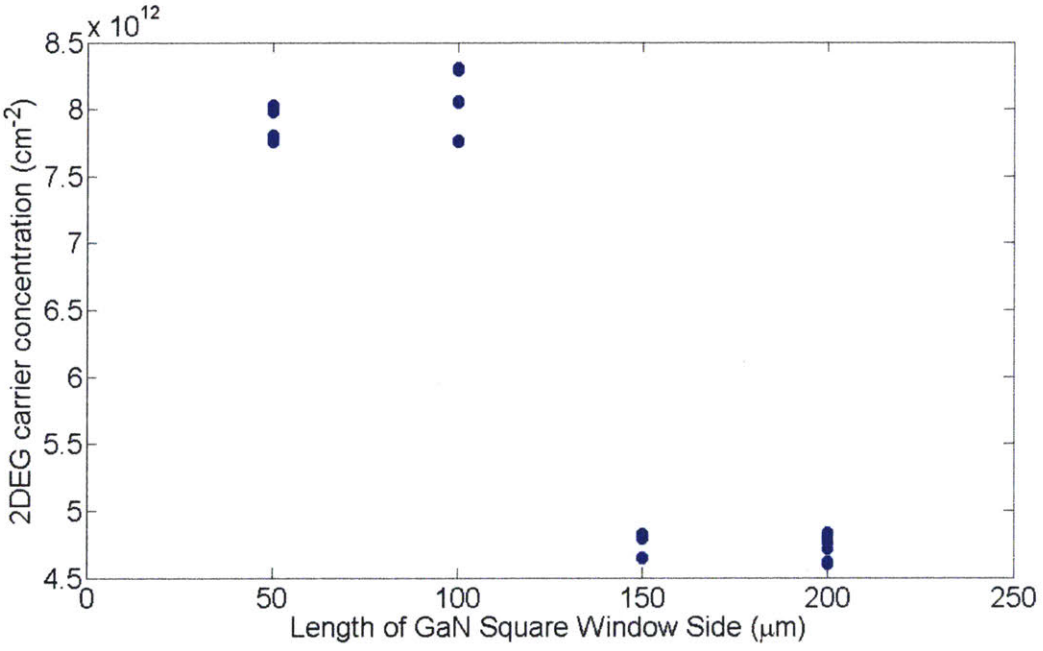

Figure 5.10: 2DEG concentration as a function of GaN window size.

Transistor characteristics in GaN windows

In addition to material transport properties, transistor characteristics relevant for power switching devices were also measured. GaN HEMTs (an example of which is shown in Figure 5.11) were fabricated in the windows to test various device properties. Gate electrodes (of 1 μm and 3 μm length) were patterned by contact lithography and gate metal was deposited by electron beam deposition and liftoff. Layouts of the HEMTs for the different sized windows are shown in Figure 5.12 with an example IV-curve shown in Figure 5.13. A summary of the maximum drain current density is shown in Figure 5.14.

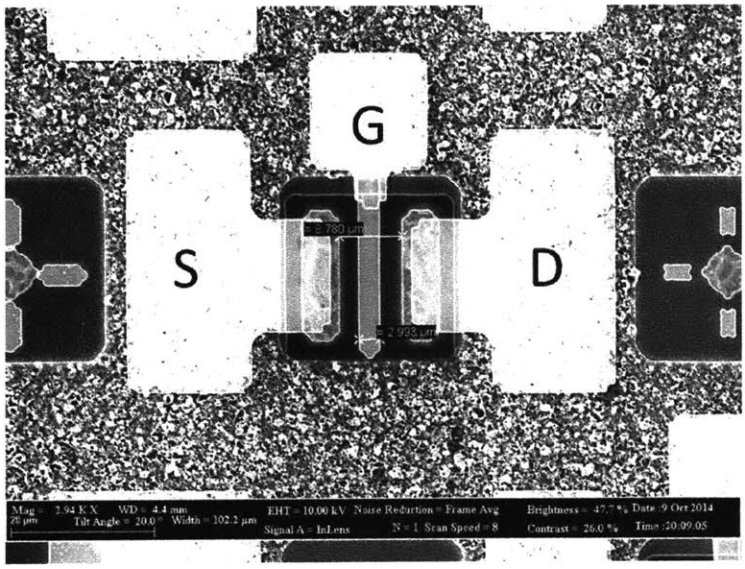

Figure 5.11: GaN HEMT in a 25 μm x 25 μm window .

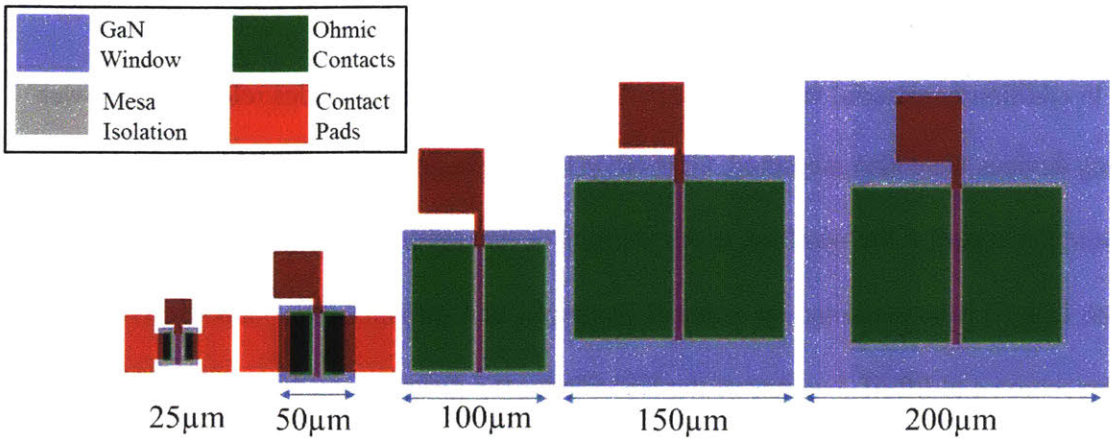

Figure 5.12: GaN HEMT in a 25 μm x 25 μm window.

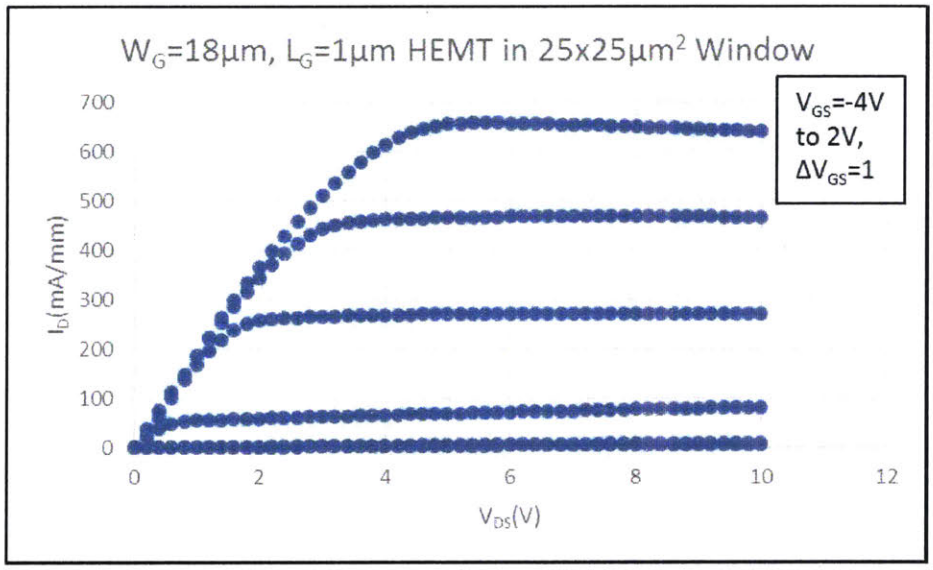

Figure 5.13: GaN HEMT in a 25 μm x 25 μm window.

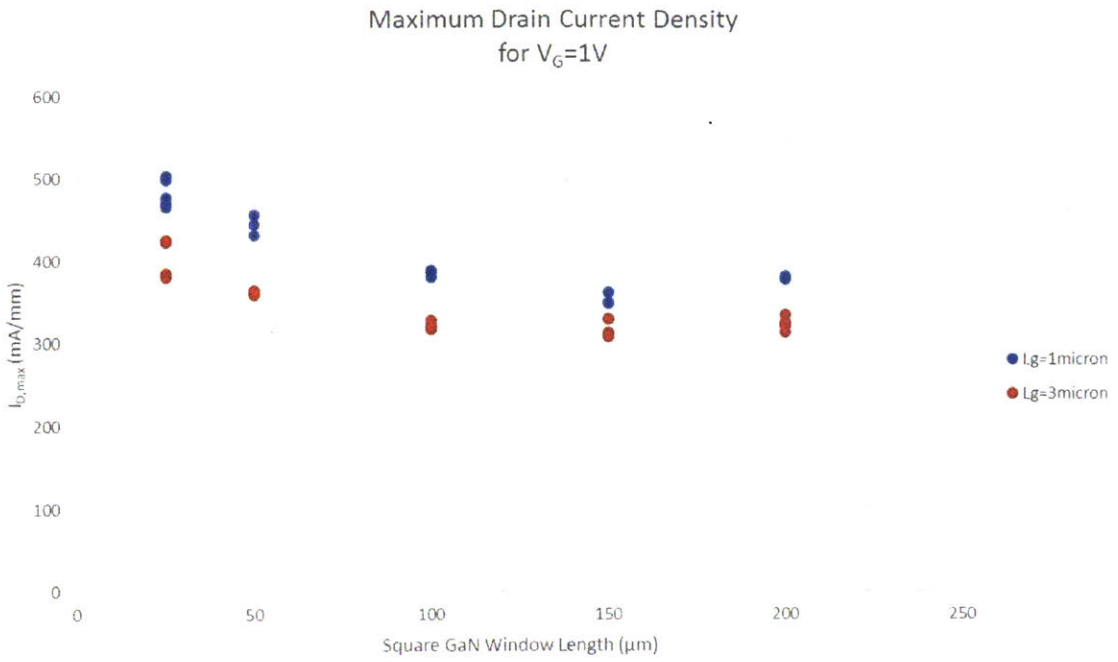

Figure 5.14: GaN HEMT in a 25 μm x 25 μm window.

As these transistors are intended to be power switches, it is important to characterize the dynamic on-resistance and breakdown voltage. Pulsed IV measurements were done at 500 ns with a quiescent point of {V_{GS}=-3V, V_{DS}=40V} and the non-quiescent point swept from V_{DS}=0V to 10V as shown in Figure 5.15. The dynamic on-resistance for the various window sizes is summarized in Figure 5.16. The three-terminal breakdown voltage of the transistors in different windows and normalized leakage current were measured and summarized in Figure 5.17 and Figure 5.18 respectively. Two-terminal buffer structures were also fabricated as shown in Figure 5.19 with the results shown in Figure 5.20.

Across these transistor measurements, it is seen that there is an optimal window size of 100x100 μm^2. A systematic analysis of the occurrence of micro cracks in the GaN windows

show that this window size tends to have low occurrence of cracks compared to the larger windows (Figure 5.15). This could be an indication of the overall quality of the material which is translated to transistor properties.

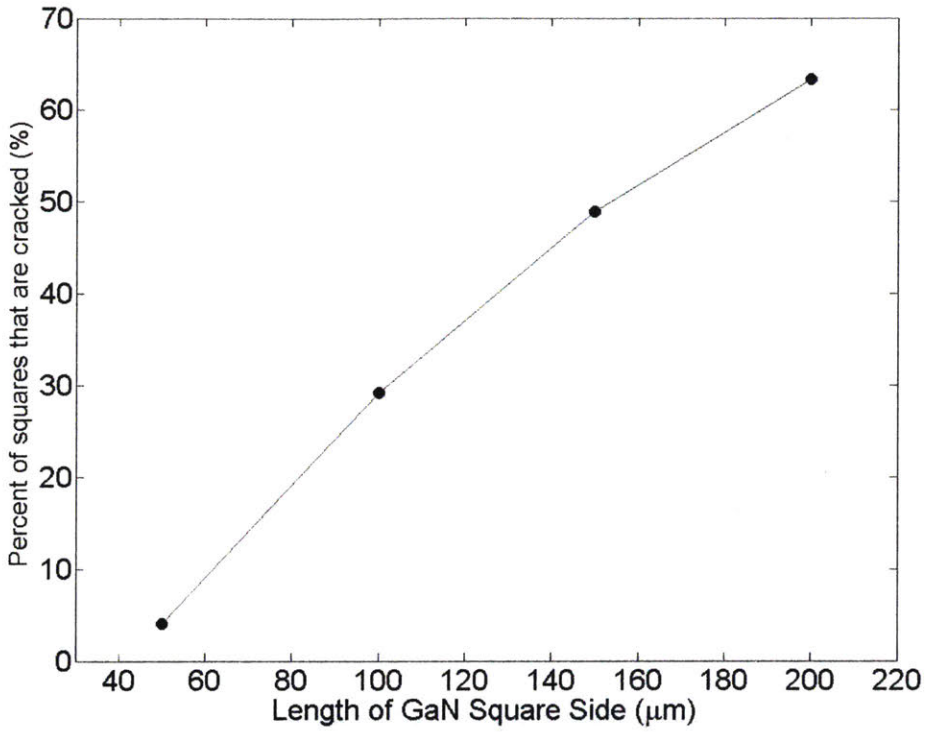

Figure 5.15. Occurrences of micro cracks in patterned GaN squares

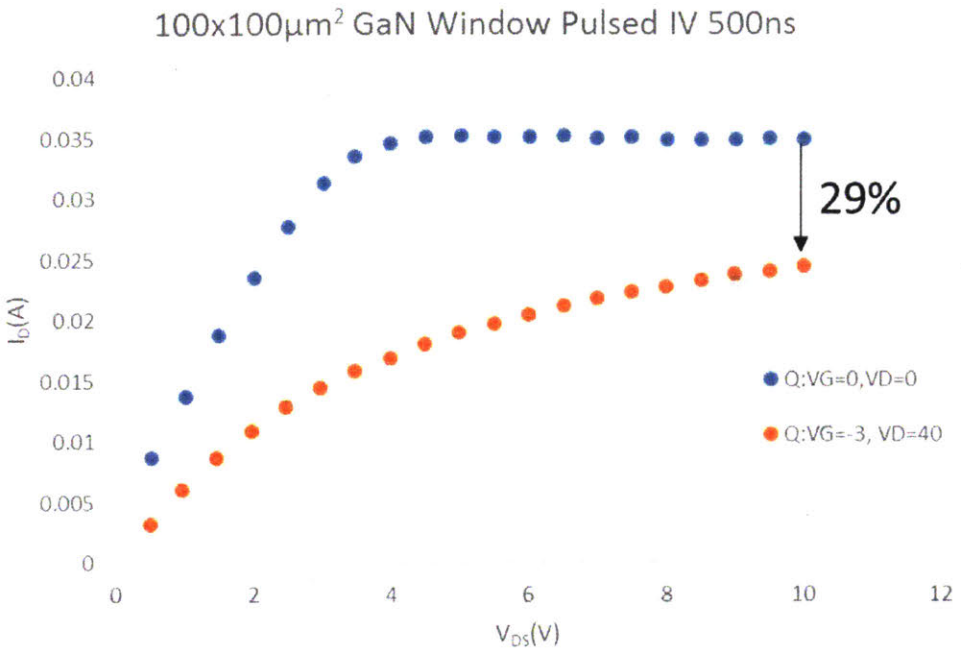

Figure 5.16. Example of pulsed-IV curve for HEMT current collapse measurement in 100x100 μm^2 GaN Window

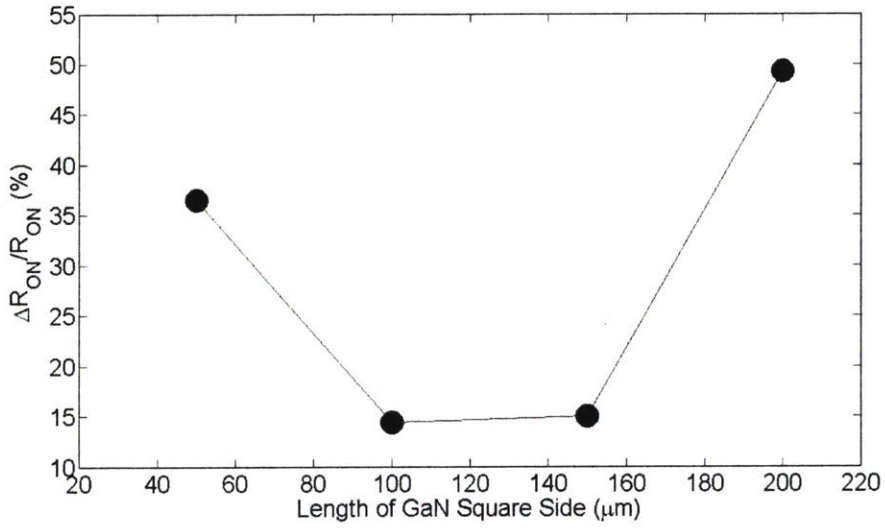

Figure 5.17. Dynamic on-resistance as a function of GaN window size.

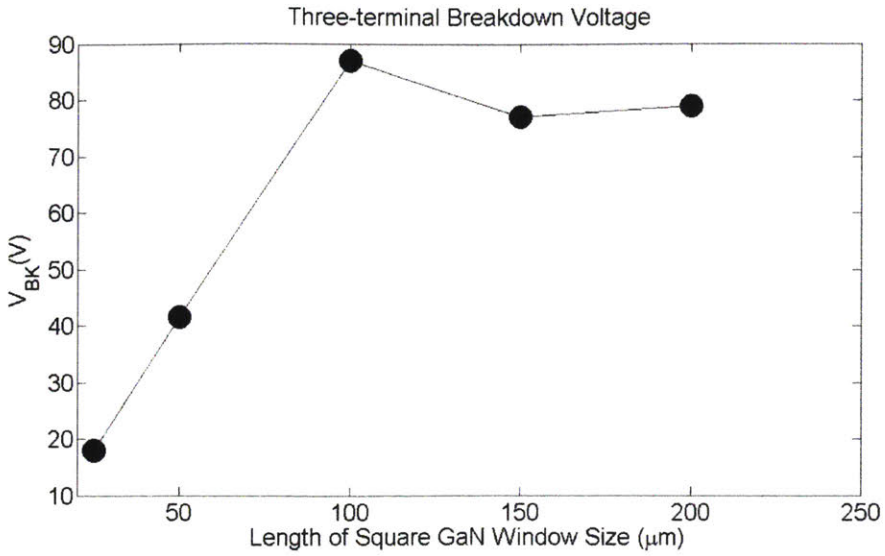

Figure 5.18: Three-terminal HEMT breakdown as a function of GaN window size.

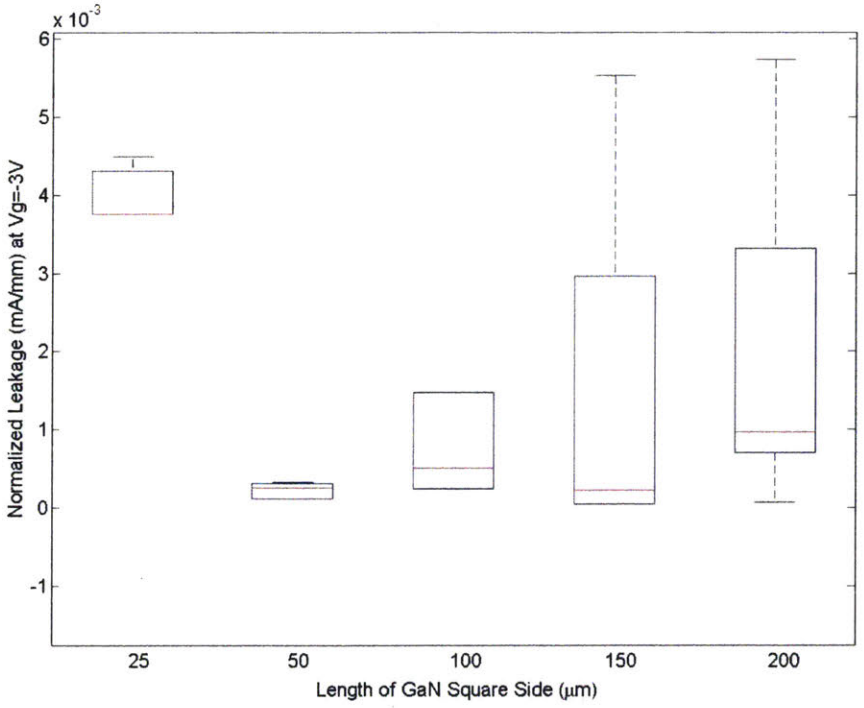

Figure 5.19: Normalized Leakage current across different GaN Window sizes

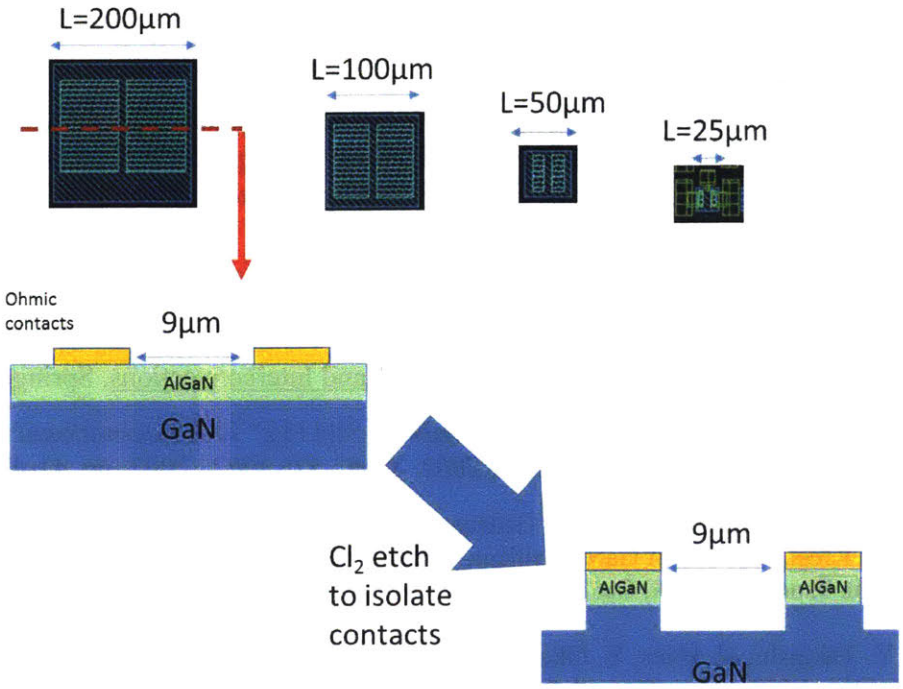

Figure 5.20: Two-terminal buffer breakdown structures in different window sizes

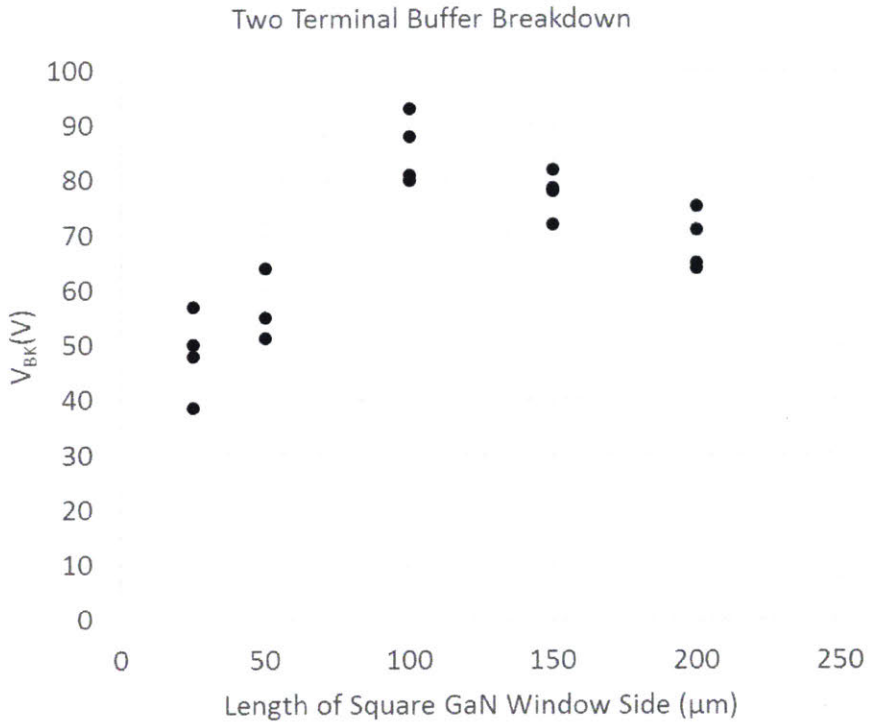

Figure 5.21: Two Terminal Buffer Breakdown results.

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Chapter 6: Conclusion and Future Work

GaN HEMTs hold much promise as a power transistor technology. However, they still face some important key challenges and this thesis has sought to explore and overcome some of those challenges.

Chapter 1 introduced the reader to the research history and material properties of gallium nitride. The origin of the two-dimensional electron gas to form a high electron mobility transistor was discussed. Additionally, the operation of power switches why the advantages of GaN could lead to a superior device were examined.

Chapter 2 explained the need for low leakage enhancement mode transistors. Other e-mode GaN technologies were mentioned and the merits of the GaN tri-gate device were expounded to show why this device is a good candidate for power switching applications. The process developed was detailed with emphasis on the passivation, field plates, and gate periphery scaling. The device was used a buck converter built and designed by Professor Perreault's group to show the potential of this technology in a power circuit application.

Chapter 3 explored extensions of the wide-periphery technology. A multi-phase buck converter was made by integrating a GaN power switch array and CMOS devices in collaboration with Professor Shepard's group. Thin film resistors and MIM capacitors were developed to be used with the wide-periphery devices for a gallium nitride integrated circuit technology and a track and hold circuit was developed in collaboration with Professor Lee's group. The IC technology laid the foundation for more complicated circuits.

Chapter 4 discussed the need for CMOS compatible GaN processing technology and the importance of demonstrating this technology on 200 mm GaN-on-Si wafers. A gold-free ohmic

contact process was developed and optimized in collaboration with MIT Lincoln Laboratories to satisfy this need. Particular attention was focused on the recess etching through the wide-bandgap AlGaN barrier to reduce the contact resistance.

Chapter 5 outlined the advantages of monolithic heterogeneous integration of GaN with Si CMOS and reviewed examples of various methods to accomplish such integration. We demonstrated in collaboration with IBM Research a new approach to monolithically integrate GaN and Si devices which used a bonded SOI wafer with a Si (111) substrate and Si (100) device layer with windows opened to access the (111) layer to selectively grow GaN. This approach used MOCVD to grow the GaN before any CMOS processing is done. Characterization of the transistor properties in GaN windows of different sizes was performed to qualify the optimal window size for power devices in future integrated systems.

Future Work

In this thesis, work has been done to demonstrate the full potential of gallium nitride as the semiconductor of choice for power electronics applications. In this thesis, the foundation has been laid to propel many future projects:

- Issues with self-heating appear to be limiting the performance of the GaN power switch. The efficiency of the power converter with the MIT GaN switches saturated and tapered off at higher power levels (compared to the commercially produced GaN switches). This heavily suggests that thermal issues are impeding better performance. Further exploration of this is needed and potential solution (such as a heat-sink) are needed.
- The variation of the threshold voltage of the GaN switch should be reduced for more predictable device performance. More uniform etching of the gate recess across the entire

sample to get better control of the threshold voltage is needed. Although this might prove to be prohibitively difficult with just a timed etch, an etch-stop layer could potentially be introduced to the epitaxial structure and the etching chemistry could be modified to accommodate this layer.

- The advanced RF power amplifier circuit described in Chapter 3 should be more thoroughly characterized and improvements could be made based on the initial measurements.
- The Au-free ohmic contact technology developed in Chapter 4 was an effective way of making source/drain without introducing too much extra process complexity. However, to achieve even lower contact resistances, more complicated methods should be investigated. Ion implantation or selectively regrown highly doped contacts for example could lower the resistance at the expense of complex simplicity.
- With this technology in place and access to state of the art fabrication facilities, large scale use of GaN in RF circuits should be investigated. This work is already underway at Lincoln Labs. This work also consists of developing processing technology for the gate, as well as studying the impact of the epitaxial structure (buffer doping, compensation methods, Si substrate type and resistivity) on the RF performance. These devices would be the foundation of MMICs to be processed in a CMOS compatible 200 mm foundry.
- Only the GaN process development was explored for the patterned GaN windows. It was determined that the 100 μm windows yielded the lowest breakdown voltage and lowest current collapse. With this knowledge in hand the project is in place to proceed to the next step. Patterned wafers for Si/GaN circuits can be grown with a focus on 100 μm windows. Furthermore, it was proposed to use a CMOS compatible back-end-of- the-line

(BEOL) process to fabricate integrated magnetics on the CMOS/GaN wafers. Electroplated NiFe or electrolessly-plated CoWP based alloy were suggested for the magnetic materials in the integrated power inductors. This project could be continued to process the CMOS devices and magnetics components and integrate the system to see the full potential of this technology.