Effect of multi-field plates on the reverse breakdown and leakage characteristics of GaN-on-silicon HEMTs

Effect of Multi-Field Plates on GaN-on-Silicon HEMTs Reverse Breakdown and Leakage Characteristics

T. Boles [1], D. Carlson [1], L. Xia [1], A. Kaleta [1], C. McLean [1], D. Jin [1],
T. Palacios [2], G. W. Turner [3], R. J. Molnar [3]

[1] MACOM Technology Solutions, Lowell, MA 01851
[2] Massachusetts Institute of Technology, Cambridge, MA
[3] Massachusetts Institute of Technology, Lincoln Laboratory, Lexington, MA 02420-9108

ABSTRACT — MACOM Technology Solutions has a continuing joint development efforts sponsored by the Department of Energy(*) with MIT main campus and MIT Lincoln Laboratory to develop GaN on silicon three terminal high voltage/high current switching devices. The initial developmental goals were for a three terminal structure that has a reverse breakdown characteristic of >1200 volts and is capable of switching 10 amperes of current, with a current breakdown target of 3000 volts. This paper presents an update on the progress of this multi-year development project against these on-state current handling, reverse leakage and breakdown goals.

DISCUSSION – As reported by the authors at CS MANTECH in 2013[1], an individual breakdown on a single finger 250 µm GaN-on-silicon HEMT device with a SCFP of >1630 volts at a current of 250 µA (1 mA/mm) was achieved. Also, over 5.5 amperes of I_{max} current utilizing a HEMT structure without a SCFP and having 10 mm of gate periphery, corresponding to a normalized current handling of at least 550 mA/mm was observed and an I_{max} of 4.5 amperes and a normalized current density of 450 mA/mm was realized on a identical transistor geometry but with the addition of a SCFP.

While these results were clearly more than competitive when compared to findings reported in the literature and industry, see Figure 1, it was clear that in order to both improve the reverse breakdown characteristic and have the ability to produce a practical HEMT for high voltage switching applications, the baseline leakage needed to be reduced significantly.

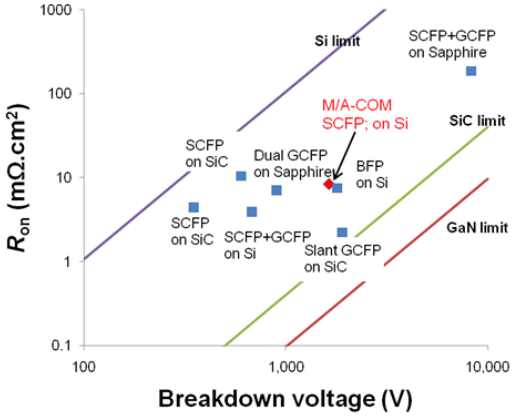

Fig. 1- MTS GaN HEMT - Comparison to Literature/Industry

A study of the basic tunnelling mechanisms that dominate the leakage characteristics of GaN Schottky diode electrodes was undertaken. The results of this investigation have been published[2]. It was found that Frenkel–Poole (FP) trap-assisted emission and Fowler-Nordheim (FN) tunnelling are the two overriding sources of leakage in GaN Schottky electrodes. Further, each of these mechanisms governs the reverse Schottky junction in different electric field regimes, as shown in Figure 2. Also, as seen in Figure 2, FN tunnelling is temperature independent, and is the dominant leakage mechanism for electric field values >1.6 MV/cm. Thus, in order to control the high voltage leakage and reverse breakdown characteristic, it is critical to properly engineer the spreading of reverse electric field by means of proper field plate design.

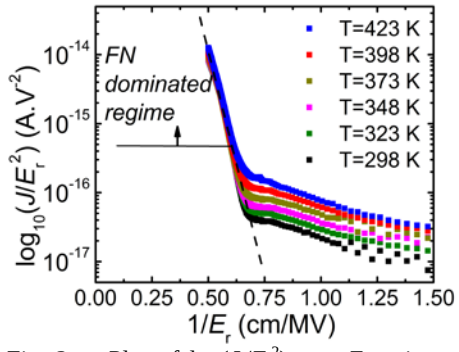

Fig. 2. – Plot of $\log(J_r/E_r^2)$ as a Function of $1/E_r$. Showing both FN and FP Tunneling Regimes

Extensive modeling studies on the design of stem slope, gate connected, and source connected field plates and corresponding dielectric thickness have been completed for single, double, and triple field plate structures. This modeling optimization utilized a 2-D structure simulator from Silvaco to analyze the effect of the field plate overlap on the drain side of the gate, the dielectric thickness and dielectric constant, the total number of field plates required, and the specific transistor terminal connections. The output from the field simulator predicted that for a combined GCFP/SCFP design, the structure simulator predicted that the peak electric fields occur, both in the GaN channel and the AlGaN barrier layer, adjacent to the gate on the drain side of the HEMT transistor, at the edge of the GCFP field plate, and at the edge of the SCFP. Since there are multiple peak electric fields in these multiple field plate configurations, to maximize device reverse breakdown the goal is to optimize the field plate structures to maintain all of the peak electric fields below 3.0×10^6 V/cm, the theoretical field strength limit for gallium nitride.

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Based upon this structure modeling, a HEMT test reticule was designed. A screen capture of the final layout is shown in Figure 3. It can be seen that this multi-field plate test reticule consists of 152 single gate variants with non-field plated devices as controls; source connected field plated (SCFP) structures of various overlap dimensions; gate connected field plated (GCFP) configurations of different overlap dimensions; combined multi-field plate designs with dual source connected and gate connected field plated configurations. In addition, multiple gate-to-drain spacings ranging from 5 µm to 20 µm to support the total applied reverse field. The goal of these field plate variants is to spread and reduce the peak fields at the drain side edge of the gate; the edge of the GCFP; and the edge of SCFP. In addition, there are 24 variants of high current, multi-gate HEMT transistors having a total of 20 mm of gate periphery. These multi-gate devices are a mixture of SCFP, GCFP, and dual SCFP&GCFP structures and having fixed 10 µm gate-to-drain spacings.

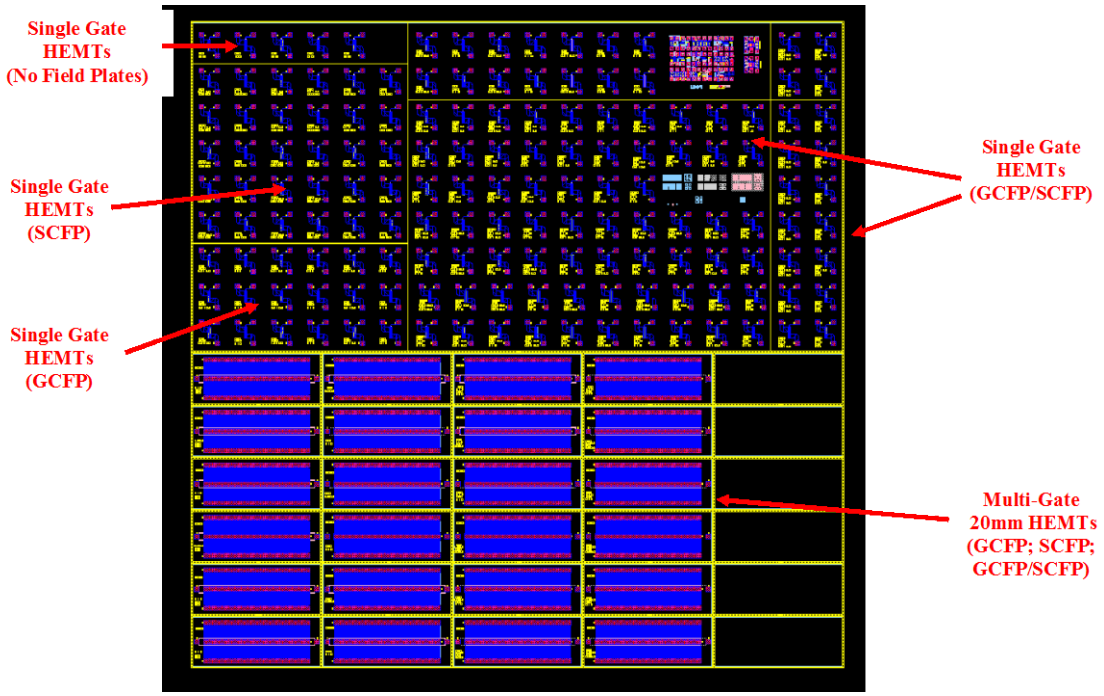

Fig. 3 - Screen Capture of HEMT Multi-Field Plated Test Matrix

In Figure 4, the details of a typical single gate HEMT device are presented. The critical dimensions of these structures are a 1 µm gate length, and a 250 µm gate width, with the specific field plate design and proportions labeled on each HEMT. In the example shown in Figure 4, it can be seen that this device has a GCFP with a 1.5 µm overlap onto the drain dielectric as measured from the edge of the gate stem. In a similar construction, this device also has a SCFP with a 4.5 µm overlay from the edge of the gate stem. The second dimension shown on each GCFP/SCFP label is the spacing from the edge of the respective field plate to the drain contact. By adding the indicated field plate-to-drain contact spacing the corresponding field plate overlap spacing, it can be seen that for the single gate example, the gate-to-drain feature is 10 µm in length. Lastly, it can be seen that the spacing between the probe pads is a minimum of 400 µm in order to prevent arcing between the probe tips during on wafer characterization.

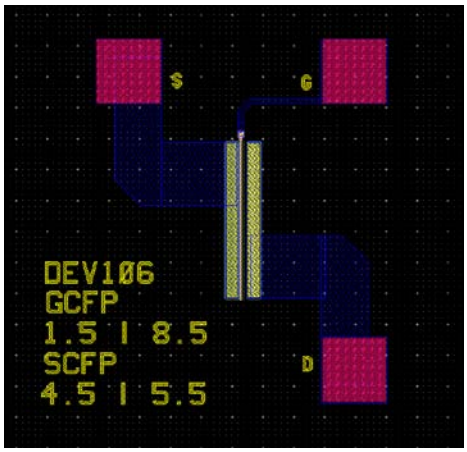

Fig. 4 – Single Gate HEMT Device with a Dual GCFP and SCFP Field Plate

An initial lot of this multi-field plated design was initiated into the wafer fab utilizing an eight wafer split of epitaxial materials having a range of 12.4 nm to 13.5 nm thick Schottky barrier active layers to reduce the sheet charge in the 2DEG conduction layer. In addition, both P+ doped, CZ silicon substrates with a 4.8 µm thick AlGaN buffer layer, and high resistivity FZ silicon substrates with a 2.7 µm thick buffer layer were employed to minimize vertical, ohmic-to-ohmic buffer leakage through the substrate.

Preliminary test results for one wafer from this initial experimental lot are presented below in Figure 5. This initial wafer had a P+ doped, CZ silicon substrate with a 4.8 µm thick AlGaN buffer layer and a Schottky barrier active layer that was 12.4 nm in thickness. Of the 152 single gate design variants, data for six units from each of two specific devices, both designs employing a combination of a gate stem sloped field plate, a GCFP, and a SCFP with different SCFP & GCFB drain overlap dimensions and field plate offsets, is shown in Figure 5. Both device designs utilize a gate to drain spacing of 20 µm.

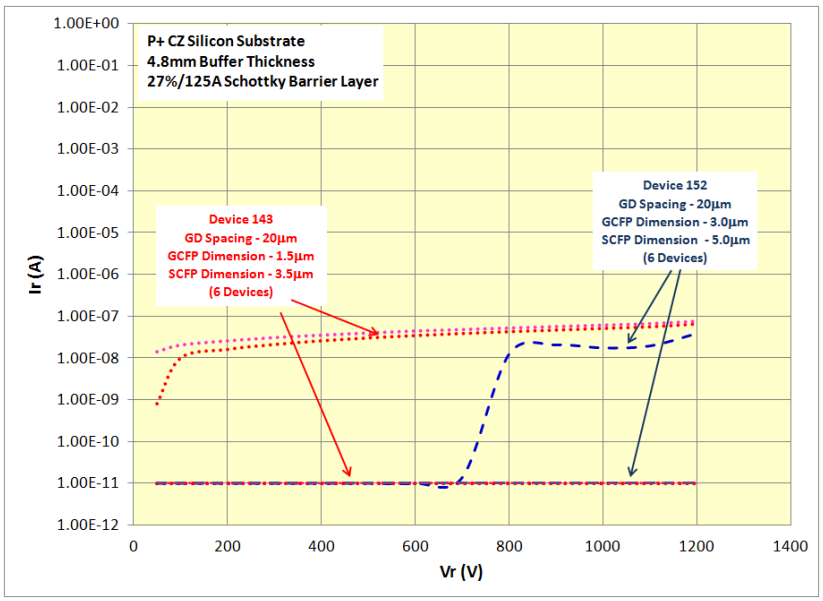

Fig. 5 – Initial Reverse HEMT Leakage/Breakdown Test Results

It can be seen in Figure 5 that all twelve measured units, regardless of the specific field plate geometries, reached the on-wafer auto-tester voltage limit of 1200 volts before avalanche breakdown was achieved. It can also be observed nine of the twelve devices, again with a similar insensitivity to the field plate layout, had a baseline leakage of less than $1.0x10^{-11}$ amperes, analogously limited by the low level leakage compliance on the auto-tester. Since these single gate HEMT devices have a gate periphery of 250 µm, this low level leakage normalizes to a current level of $4.0x10^{-8}$ mA/mm of gate periphery. This very low reverse baseline leakage current contrasts dramatically with the leakage floor of approximately $1.0x10^{-3}$ mA/mm that was observed previously[1], a five order of magnitude improvement.

The remaining three devices that were tested, again from both field plate geometries, have a baseline leakage response that is more characteristic of devices having trapping/channeling effects in the drain depletion region. While the cause of this reverse leakage curve is not understood at this time, the absolute leakage level is approximately $8.0x10^{-8}$ amperes, normalizing to $3.2x10^{-5}$ mA/mm of gate periphery, which is still an improvement a factor of 200 over previously reported results.

Lastly, as seen in the paper from CS MANTECH 2013[1], an average reverse breakdown voltage was achieved with a SFCP design of 1322 volts at a defined 1.0 mA/mm leakage level. It can be seen in Figure 5that the worst case unit has a minimum breakdown of 1200 volts, actual voltage not able to be determined due to tester compliance, at a leakage level of $3.2x10^{-5}$ mA/mm, a five order of magnitude improvement in gate-to-drain leakage.

CONCLUSIONS – A study was performed to understand the fundamental behavior of tunneling currents in GaN Schottky electrodes. Two dimensional simulations were performed on gate stem sloped field plates, GCFP, SCFP, and multi-field plates geometries to spread and reduce the peak fields at the edge of the gate and the edges of the field plates. Based upon the fundamental studies and the 2-D structure simulations, a three terminal evaluation mask was designed having a series of single finger HEMT structures to validate the effect of the field plate variants and the gate to drain spacing on the reverse leakage and breakdown performance. An average three terminal breakdown of 1200 volts was measured on a single finger 250µm GaN-on-silicon HEMT devices utilizing multi-field plate geometries, sloped stem FP/GCFP/SCFP geometries. Even more impressive is the observed 10^5 times improvement in the HEMT reverse leakage current which validates the modeling of the fundamental tunneling leakage mechanisms enabling further high voltage reverse breakdown improvement..

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