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CMOS-Compatible Ti/Al Ohmic Contacts (R_c <0.3 Ωmm) for u-AlGaN/AlN/GaN HEMTs by Low Temperature Annealing (<450 ^{o}C)

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Recently the development of CMOS-compatible fabrication technologies for GaN HEMTs has attracted increasing levels of interest [1]-[4]. A low temperature ohmic contact technology is required for gate-first device fabrication and CMOS-first GaN-Si integration process, however, typical ohmic contacts need annealing at > 800 ^{o}C [1], [2]. In the past, we have reported an approach to realize low contact resistance (R_C) using CMOS-compatible metal schemes annealed at 500 ^{o}C through an n^+-GaN/n-AlGaN/GaN structure [4]. This method has a drawback that the n-doped AlGaN barrier increases the gate leakage current. In this work, we present the first low temperature (<450 ^{o}C) CMOS-compatible Ti/Al ohmic contact technology for conventional unintentionally-doped AlGaN/AlN/GaN HEMT structures.

Fig. 1 shows the schematic of the u-AlGaN/AlN/GaN structure, same as that in [2]. Hall measurements show that the wafer has a 2DEG density of $1x10^{13}$ cm^{-2} and mobility of 2100 cm^2/Vs. The structure was grown by a conventional MOCVD in a planetary reactor. CMOS-compatible ohmic contacts were formed by a recess etch using low-power BCl_3/Cl_2 plasma and then Ti/Al (40/200 nm) ohmic metallization. The schematic of the ohmic contact is shown in Fig. 1. Fig. 2 (a) shows the optical micrograph of the TLM patterns after 500 ^{o}C RTA. The Ti/Al metal surface remains smooth after 500 ^{o}C annealing. Fig. 2(b) shows the *I-V* characteristics measured between two ohmic metal pads with 6-μm distance after RTA at various temperatures. High saturation current was achieved using low-temperature annealing and Au-free ohmic contact. Fig. 2(c) shows the TLM results of total resistance versus pad distance at different temperatures; Fig. 2(d) shows the R_C and saturation current after RTA at various temperatures. Low R_C of <0.3 Ωmm was achieved after RTA at 450 ^{o}C - 500 ^{o}C for 30 s. Fig. 3 shows the lowest R_C achieved at various RTA temperatures with a recess depth optimized at each temperature point. R_C<0.5 Ωmm can be achieved over a wide RTA temperature window from 425 ^{o}C to 550 ^{o}C. A u-AlGaN/AlN/GaN HEMT was demonstrated through BCl_3/Cl_2 mesa etching, Ti/Al ohmic contact as abovementioned, and then Ni/Al gate metallization. Fig. 4 shows the DC characteristics ((a) output characteristics; (b)(c) transfer characteristics and (d) gate current characteristics) of the device. Similar characteristics were achieved compared to those devices fabricated with Au-contained ohmic and gate contact. This shows the great potential of this low-temperature ohmic contact technology.

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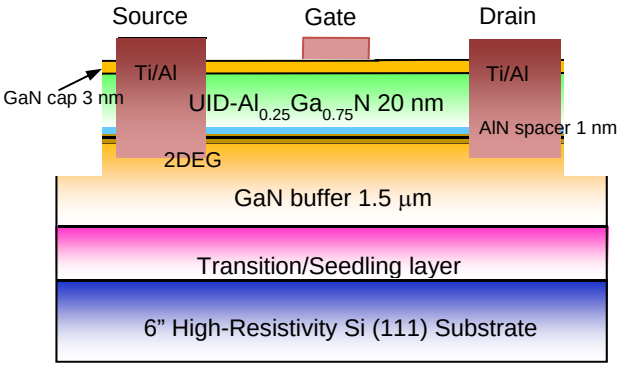

Fig. 1 Schematic of the wafer structure and source/drain ohmic contact by means of recess.

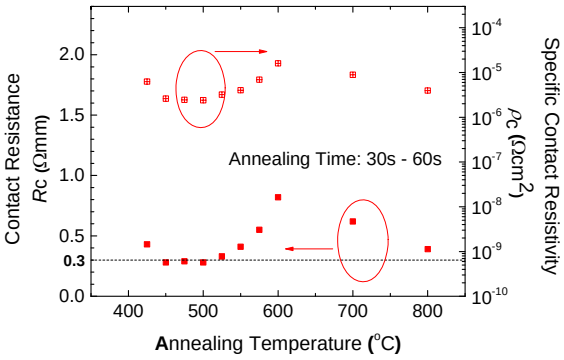

Fig. 3 Best ohmic contact results at different annealing temperatures achieved with recess depth optimized at each temperature point.

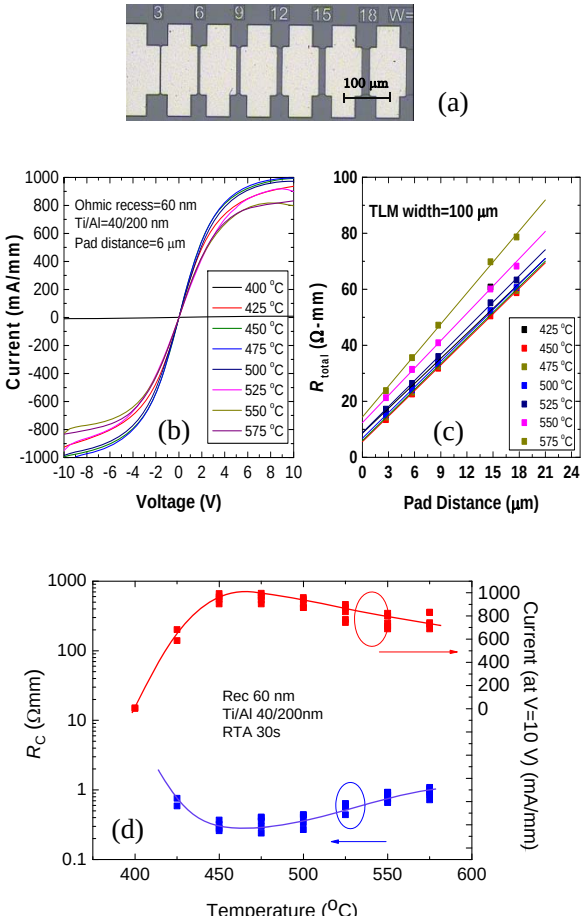

Fig. 2 (a) Optical micrograph of TLM patterns after annealing at 500 °C; (b) Current-voltage characteristics of a TLM pattern with pad distance of 6 μm annealed at various temperatures; (c) The total resistances versus pad distances in TLM patterns after annealing at various temperatures; (d) R_c and saturation current (10V, 6 μm distance) after annealing at various temperatures.

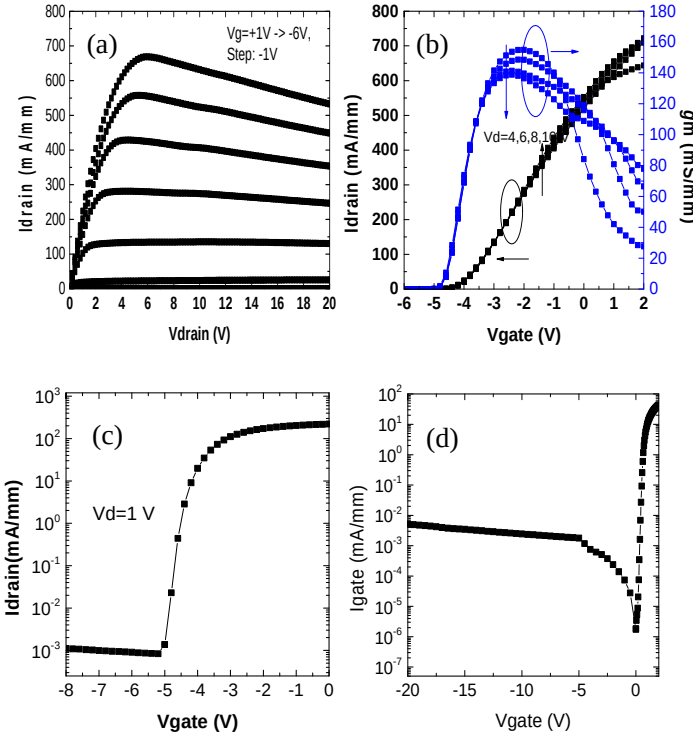

Fig. 4 (a) DC output (b), (c) transfer and (d) gate characteristics of a GaN HEMT fabricated using the developed low-temperature CMOS-compatible ohmic contact technology. The device has L_g=2 μm and L_{sd}=7 μm. The device shows I_{dmax}(V_g=1V)=670 mA/mm, R_{on}=4.2 Ωmm, g_{mmax}=155 mS/mm, Subthreshold Slope (SS)=159 mV/dec. I_{on}/I_{off}=2.7x10^5, I_{leak}(at V_{gd}= - 20V) = 5x10^{-3} mA/mm.