# Extreme-Submicrometer Silicon-on-Insulator (SOI) MOSFETs

by

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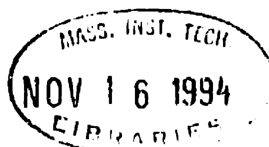

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## Abstract

As the feature sizes of MOS technologies are scaled to smaller and smaller dimensions, considerable challenges arise in the area of device design. Recent literature has suggested that silicon-on-insulator (SOI) technology can provide additional leverage in terms of performance and scalability for mainstream digital applications.

This work examines some of the critical intrinsic device design issues surrounding the integration of SOI technology into mainstream CMOS applications. In the area of SOI channel design, the tradeoffs among the various SOI design variables such as silicon film thickness, doping concentration, gate oxide and buried oxide thickness, and gate work-function are examined. A physical understanding of the mechanisms that govern SOI short-channel effects and their implications on the optimal design space for sub-0.25 μm technologies are presented. It is shown that for scaling into the deep-submicrometer region, fully-depleted devices require ultra-thin silicon films on the order of 50 nm or less.

One concern with the use of ultra-thin silicon films is the significant parasitic series resistance that it potentially entails. The dependencies of the parasitic series resistance in SOI are studied through two-dimensional numerical simulations as well as process experiments. It is found that the contact geometry favors the use of ultra-thin silicides that do not fully-consume the silicon film. This is accomplished using a novel titanium/cobalt process for forming self-aligned cobalt disilicide. Deep-submicrometer devices with effective channel length down to 0.12 μm were fabricated with record-low parasitic series resistances of 250 Ω-μm in thin-film SOI. This demonstrates that with appropriate design of the contact, parasitic series resistance does not limit SOI performance.

The low thermal conductivity of the silicon dioxide layer in SOI films has also been a concern because significant device self-heating exists under typical device operating conditions. An experimental measurement technique was developed to measure static self-heating in SOI MOSFETs as a function of a wide range of device parameters. These data were then used to calibrate a thermal model of SOI devices to predict the temperature fields throughout the device. Transient measurements of self-heating show that the thermal time constants are long compared to electrical time constants in typical digital applications, thus self-heating does not limit the current drive under dynamic operating conditions. A parameter extraction technique was developed to extract the non-self-heated device characteristics from static characteristics using a bulk MOSFET model with minor modifications for fully-depleted SOI.

The dependencies of the electric field in thin-film SOI MOSFETs was examined through the measurement of hot-carrier gate currents in SOI

NMOSFETs. The gate current was found to be higher in partially-depleted devices than in fully-depleted devices, and a significant decrease was observed for thinner silicon films. This is a departure from previous simulation studies that showed that thinning the silicon film would greatly increase the electric field and thus adversely affect the reliability. Hot-carrier degradation verifed the dependencies in the gate current and allowed the study of some of the interface coupling issues in fully-depleted devices. When significant current flows at the back-interface of the device, interface coupling is found to be important in the evaluation of device degradation.

Finally, the performance of bulk and SOI technologies were examined by studying the intrinsic tradeoff between current drive and short-channel effect. A wide range of experimental devices were used to study the effect of silicon film thickness, channel doping, gate oxide thickness, and source/drain structure. For fully-depleted SOI, the trends are very similar to bulk devices with the performance also being quite comparable. In partially-depleted SOI, the floating-body-induced threshold voltage shifts complicate the comparison. The use of partially-depleted SOI devices will depend greatly on the ability to harness the benefits of the floating body effects (such as super-steep subthreshold slope) reproducibly in a dynamic environment.

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# Chapter 1

# Introduction

Metal-oxide-semiconductor field-effect transistors (MOSFETs) are the basic building blocks of most very large scale integrated circuits (VLSI). The primary utility of the MOS device for digital operation comes from its ability to function as a switch with the input isolated from the output and also its charge storage capability. These functions form the basis of the large-scale computation and memory elements that comprise present-day microprocessors and semiconductor memories. The strength of MOS technology lies in the relative ease with which millions of transistor elements can be integrated on a given chip. With the advent of modern fabrication tools, the rate at which technology is advancing is astronomical. For example, in 1972, the prototype microprocessors and logic circuits had about 4000 transistors with a minimum dimension of about 6 μm [1]. Today, the state-of-the-

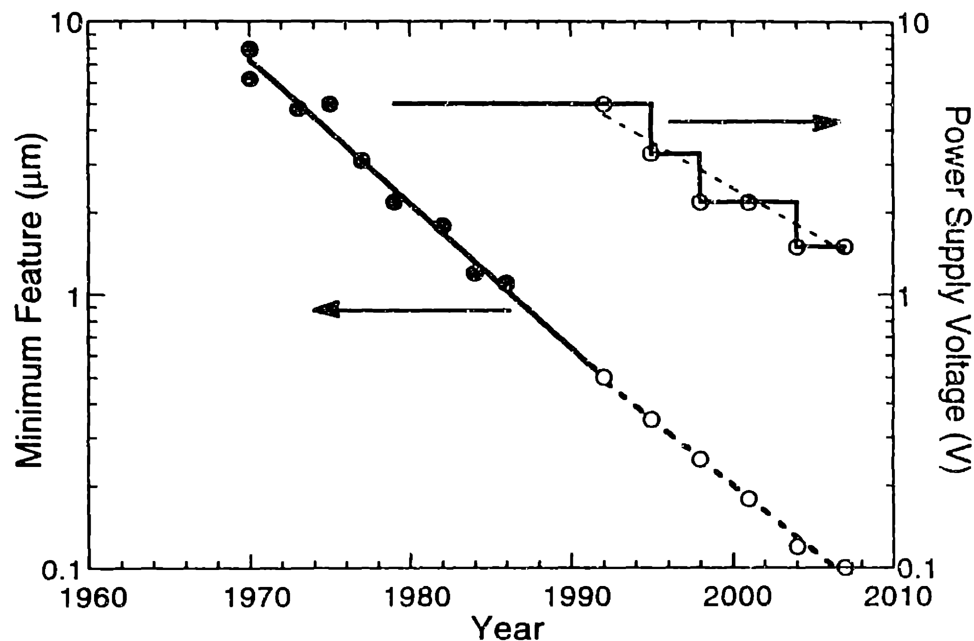


Figure 1-1: Scaling of the minimum feature size of commercial products in production with time from Sze [1]. The data in the dashed line is taken from the Semiconductor Industry Association (SIA) Roadmap [4]. On the right axis is the scaling of power supply voltage with minimum dimension.

art Pentium™ or PowerPC™ microprocessor has approximately 3 million transistors with a minimum dimension of 0.6 µm [2].

The main force of this progress is the shrinking of the minimum dimension of the transistor as shown in Fig. 1-1. MOS devices are continually being scaled to smaller and smaller dimensions at a rate of about a factor of two every 5 years. The drive towards miniaturization is led by the promise of improved circuit performance, reduced chip sizes, and the potential for higher levels of integration [3]. Currently, critical dimensions for commercial products in production are approaching the 0.5 µm level and projections are that dimensions will be less than 0.25 µm by the year 2000 [4]. However, as devices are scaled, considerable challenges arise in the areas of device design and fabrication.

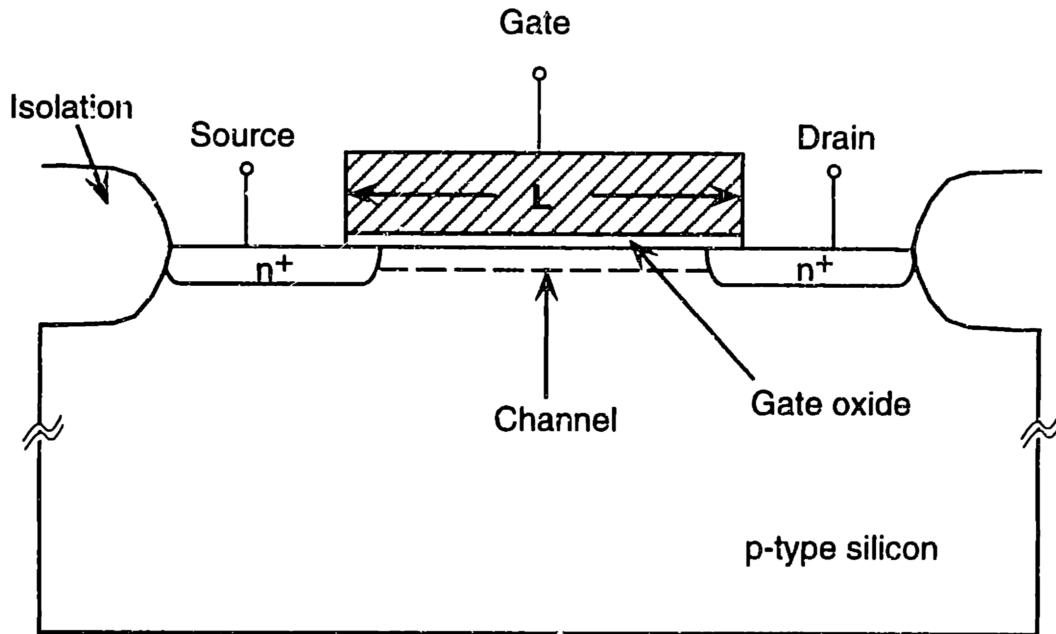


Figure 1-2: Cross-sectional view of a conventional bulk NMOSFET.

## 1.1 Conventional MOSFET Scaling

Figure 1-2 shows a cross-section of a typical MOSFET. The MOSFET is a two-dimensional device where the two dimensions (lateral from source to drain, and transverse from gate to substrate) can essentially be decoupled in the ideal case. In the transverse direction, the MOS structure controls a mobile surface inversion charge layer by electrostatically imaging a gate charge in the substrate. The magnitude of the gate voltage modulates the inversion charge and thus the channel conductivity. Current flow takes place in the lateral direction from drain to source along the so-called "channel" or inversion region. The presence of the gate insulator isolates the input (gate) from the output (drain) of the device and also allows charge storage on the capacitor. The critical parameters for device design in a MOSFET include:

**channel length:** The distance from the source to drain over which current flows across the device.

**channel width:** The device width in the z direction (into the page).

**gate insulator:** The thickness of the insulator that separates the gate from the channel area.

**junction depth:** The depth of the heavily-doped regions of the source and drain.

**channel doping:** The impurity doping in the channel region of the device.

A detailed description of the principles of operation can be referred to any standard semiconductor text such as Muller and Kamins or Tsividis [5,6].

Up to the 0.5 μm technology generation, devices have typically been reduced by following classical scaling laws such as the "constant field" or "constant voltage" scaling principles [7,8]. In both approaches, the device designer starts with a well-behaved device at a current generation, and scales the lateral (gate length and device-to-device spacing) and vertical (gate oxide, junction depths, and depletion widths) dimensions by roughly the same parameter. The objective is to fully scale the device so that the transistor proportions remain roughly the same. In the "constant field" approach, every parameter is scaled including the power supply voltage which allows the internal device electric fields to remain the same (Table 1-1). The advantage of this approach is that by keeping the internal electric fields constant, high-field effects and reliability problems are alleviated. However, this approach is hard to implement in practice because certain physical MOS parameters such as junction built-in voltages can not be scaled. In practice, as the device dimensions are reduced, the power supply voltage has remained roughly constant or has been scaled slowly. This approach has been described as "constant voltage"

Table 1-1: Scaling factors for constant field and constant voltage scaling adapted from Tsividis [6].

| Quantity | Constant field scaling ($\kappa>1$) | Constant or quasi-constant voltage scaling ($1<\beta<\kappa$) |
|---|---|---|
| device length, $L$ | $1/\kappa$ | $1/\kappa$ |
| device width, $W$ | $1/\kappa$ | $1/\kappa$ |
| gate oxide, $t_{ox}$ | $1/\kappa$ | $1/\beta$ or $1/\kappa$ |
| channel doping, $N_a$ | $\kappa$ | $\kappa$ |
| junction depth, $x_j$ | $1/\kappa$ | $1/\kappa$ |
| power supply, $V$ | $1/\kappa$ | 1 or $1/\beta$ |
| threshold voltage, $V_T$ | $1/\kappa$ | 1 or $1/\beta$ |

Table 1-2: Predicted device requirements for future generation technologies from SIA Roadmap [4].

| | 1992 | 1995 | 1998 | 2001 | 2004 |
|---|---|---|---|---|---|
| **Physical Gate Length, $L$ (μm)** | 0.35 | 0.25 | 0.18 | 0.12 | 0.10 |
| **S/D junction depth, $x_j$ (nm)** | 100 | 60 | 40 | 25 | 10 |
| **Channel doping, $N_a$ ($cm^{-3}$)** | mid $10^{17}$ | $6 \times 10^{17}$ | $8 \times 10^{17}$ | $10^{18}$ | $10^{18}$ |
| **Gate oxide, $t_{ox}$ (nm)** | 12 | 9 | 7 | 6 | 4.5 |

or "quasi-constant voltage" scaling and is useful because it accounts for the non-scalability of some of the physical MOS parameters and has the added advantage that it allows backwards compatibility with existing chips. Although the magnitudes of the electric fields are allowed to increase, the general "shape" of the field and potential distributions are preserved.

For devices in the sub-0.35 μm regime, classical scaling is not easily implemented. Table 1-2 gives the typical dimensions required using approximate scaling arguments for sub-0.35 μm technologies (taken from the Semiconductor Industry Association Roadmap [4]). The requirements of junction depths under 100 nm and latch-up free isolation on the order of 0.35 μm or less are not trivial from a fabrication standpoint [3]. In terms of the device architecture, doping levels above $10^{17}$ $cm^{-3}$ are required to control short-channel effects and drain-induced barrier lowering (DIBL) [9]. This presents additional concerns because the inversion-layer mobility is degraded and device parasitic capacitances are increased with higher doping levels. Because of these challenges, many alternative device structures are being explored for deep-submicrometer devices.

## 1.2 Silicon-on-Insulator (SOI) Devices

To alleviate some of these problems, there has recently been much interest in the use of silicon-on-insulator (SOI) devices for scaled CMOS technologies [10,11,12]. A cross-section of a silicon-on-insulator MOSFET is shown in Fig. 1-3. A SOI device is very similar to a conventional bulk device except that a buried insulator, most commonly, silicon dioxide, separates the active portion of the device from the silicon substrate. The presence of the buried oxide results in several novel advantages for SOI in comparison to conventional bulk technologies. The basic core of the device is the same as a conventional bulk MOSFET, i.e. the source, drain, and

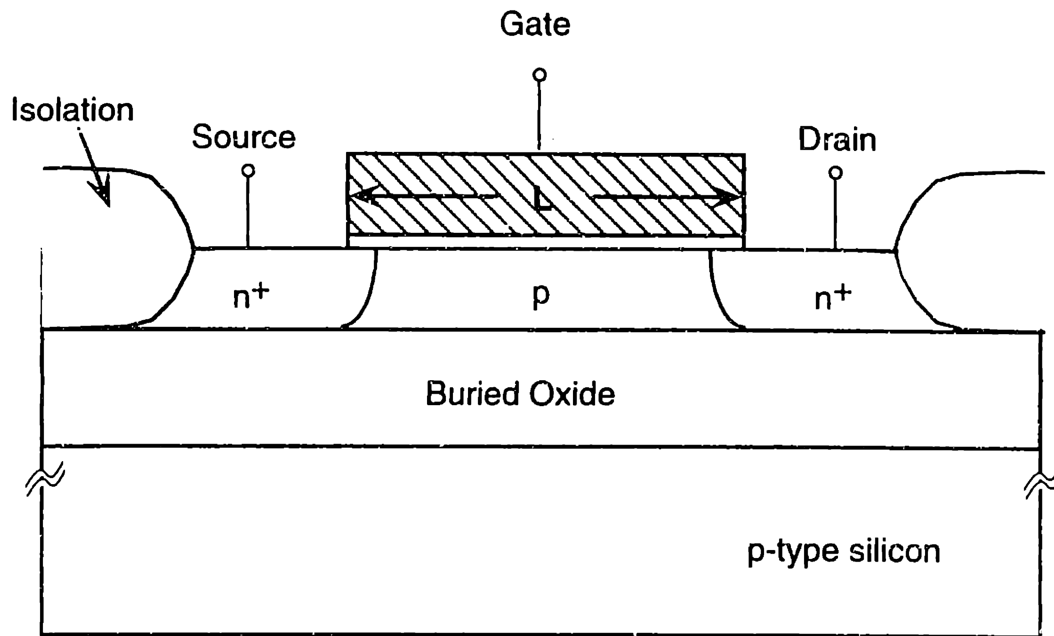


Figure 1-3: Cross-sectional view of a SOI NMOSFET.

gate are the three terminals that control device operation. However, the device is fully dielectrically isolated from neighboring devices via the buried oxide and device isolation. This potentially results in significantly fewer parasitics than in a conventional bulk technology.

The parasitic capacitance from the source and drain to the substrate of an SOI MOSFET is reduced considerably when compared to the bulk case because the buried oxide thickness is typically much larger than the corresponding depletion regions of a bulk source and drain. The full dieletric isolation eliminates the potential of latchup, which is a parasitic phenomenon that can occur in bulk devices as a result of bipolar action between the source, drain and substrates of neighboring MOS devices.

Device fabrication processes can potentially be simplified in a SOI technology because the formation of shallow junctions is not determined by implantation and

thermal cycles, but by the thickness of the silicon film. Also, well formation is considerably simplified because there are no substrate effects to consider. The device-to-device spacing is essentially limited by lithography constraints unlike bulk technologies in which the isolation, latchup-protection and well formation usually constrain the minimum spacing between the devices. This potentially can result in increased packing density at a given lithography dimension. These are a few of the reasons that silicon-on-insulator technology has received so much attention in recent years. A detailed description of all of the advantages can be found in Chapter 2.

Although there has been much literature in the SOI community demonstrating the potential advantages of SOI over conventional bulk technologies, there are still no reports of commercial products on SOI for high-performance CMOS applications. This is primarily due to the fact that bulk technologies have advanced with relative ease into the 0.5 μm generation with continuously improving process and device technology. SOI can only make an impact on the mainstream CMOS market at an integration level where bulk technologies have significant difficulties and SOI technologies can provide some solutions. Alternatively, if performance advantages in SOI are significant enough so that they can be treated as an alternative to scaling at any given technology generation, i.e. 0.25 μm SOI technology can provide equivalent performance to 0.18 μm bulk technology, this may also have a significant impact. Given the present state of silicon technology with 0.5 μm geometries in production and 0.35 μm geometries in advanced development, a realistic target insertion point for SOI would be at the 0.25 μm level of integration and below. However, at these dimensions, there are still a considerable number of questions surrounding the integration of SOI technology.

## 1.3 Thesis Goals

The goal of this thesis is to assess the technical viability of SOI technology as a potential challenger to bulk silicon for the mainstream CMOS market at the insertion technology generation of 0.25 μm and below. However, instead of focusing on the potential advantages that have been widely discussed in the literature, this thesis focuses on several of the critical intrinsic device issues that must be addressed before SOI technology can be integrated.

Deep-submicron SOI MOSFETs were designed and fabricated in the MIT Microsystems Technology Laboratory to study several of the critical intrinsic device issues that face SOI technologies. The four SOI device issues that are studied in detail in this work are the SOI channel design, parasitic series resistance, self-heating effects, and high-field effects. Each of these issues must be well understood at the 0.25 μm technology insertion generation before SOI technology can be integrated into mainstream commercial products. The goal of this thesis in each of these areas is to provide an understanding of the device physics, assess the advantages or disadvantages as compared to bulk technologies, and propose solutions to improve the current state-of-the-art of SOI technology. Finally, a comparison of the performance tradeoffs between SOI and bulk technologies is performed.

This thesis is divided into eight chapters and one appendix.

**Chapter 2** describes the current state-of-the-art in SOI technology and provides a detailed background of the history, potential advantages and issues facing the integration of SOI into mainstream applications.

**Chapter 3** discusses the SOI channel design. Two-dimensional simulations are used to examine the SOI channel design and understand the appropriate design spaces for sub-0.25 μm SOI technologies.

**Chapter 4** examines the issue of device parasitics, in particular the parasitic series resistance. The parasitic series resistance is examined through two-dimensional simulations and process experiments and a novel salicidation technology using titanium/cobalt bimetallic laminates is explored.

**Chapter 5** studies the self-heating effects in SOI MOSFETs and provides a methodology for the measurement and modeling of self-heating for SOI device and circuit operation.

**Chapter 6** explores the issue of high-field effects in SOI. In particular, the behavior of the SOI electric field with regard to hot-electron effects is examined through the measurement of gate currents and hot-electron degradation.

**Chapter 7** studies the intrinsic performance tradeoffs in SOI technologies as compared to bulk technologies. A methodology is presented for the evaluation of the performance tradeoffs in deep-submicrometer MOSFETs focusing on the intrinsic tradeoffs between current drive and short-channel effects.

**Chapter 8** presents a summary of the main conclusions of this thesis and makes some recommendations for future directions.

**Appendix A** presents the detailed fabrication processes for the devices that were fabricated as part of this thesis work.

# Chapter 2

# Background

This section discusses the historical background of silicon-on-insulator (SOI) technology; the potential advantages over conventional bulk silicon technologies; and the current issues that face its integration into mainstream CMOS applications. Through the discussion of the current issues facing the technology, some motivation is provided for the specific areas that were explored in this research.

## 2.1 Historical Background

Silicon-on-insulator (SOI) technology was originally proposed in 1963 by Manasevit and Simpson by the epitaxial growth of a silicon film on a single-crystal insulator (sapphire) [13]. Even as early as the mid-70s, SOI was considered to have great potential for high-speed devices and circuits because the presence of an

insulator isolating the active device area from the substrate reduced many of the parasitic effects that plagued bulk MOSFETs. In addition, SOI had the potential of allowing three-dimensional integration of devices. However, although SOI appeared to be an interesting technology in theory, it was difficult to obtain epitaxial silicon on an insulator with material quality close to conventional bulk silicon. All of the methods for forming SOI, heteroepitaxial techniques (epitaxial silicon growth on a single-crystal insulator), laser or e-beam recrystallization of polysilicon on oxides, or homoepitaxial techniques (epitaxial lateral overgrowth of silicon) suffered from high dislocation densities, stacking faults, or grain boundaries [14]. Thus, devices made in these films had inferior mobilities, high interface trap density at the silicon-insulator interface, and generally inferior performance. In addition, there were compatibility issues concerning the use of such materials as sapphire in a mainstream CMOS environment.

However, even with these material problems, SOI developed particularly well in niche applications for radiation-hard environments in the aerospace and military industry. The major advantages of SOI for these applications are that the full dielectric isolation of the device reduces the sensitivity of device parameters to single-event upset caused by the penetration of alpha particles into reverse-biased p-n junctions in bulk devices. The reduction of the depletion area in SOI also reduces the amount of photocurrent generation due to large doses of X-rays or gamma rays. Thus, many commercial products currently exist today using SOI or SOS technology for radiation-hard environments [14].

The advent of SIMOX (Separation by Implantation of Oxygen) technology in 1977 by Izumi et al. proposed a more IC compatible technology of creating the insulating layer [15]. Using this method, the buried $SiO_2$ layer is formed by implantation of oxygen and then a subsequent high-temperature anneal shown

schematically in Fig. 2-1. In addition, other methods such as the bond and polish or etch-back technique for forming SOI have also been developed that allow the realization of high-quality SOI substrates [16]. In the bond and polish or etch-back technique, two hydrophilic silicon surfaces are contacted, bonded, and annealed at high temperature. Then, subsequent to the bonding, most of one of the wafers is polished or etched-back to form the SOI wafer as shown schematically in Fig. 2-2. This technique potentially provides the highest quality silicon and insulator layer and also allows full flexibility of all of the layer thicknesses.

Because of these improvements in material quality, the potential use of SOI for mainstream CMOS technology has become an active area of research over the past 10-15 years. There are still some remaining material concerns with both the SIMOX and bond-and-etch-back SOI fabrication techniques. In the SIMOX case, the main issues are the quality of the buried oxide and the $Si/SiO_2$ interface [17,18], the existence of pipes, i.e. small areas where surface defects or particles cause the implanted buried oxide to be discontinuous, and the dislocation density (approximately $10^4$-$10^5$ $cm^{-2}$ in commercially-available SIMOX) [19]. In the bond and polish or etch-back SOI, the major concerns are the silicon film thickness control and the cost of the starting substrates [20]. Although these issues of material quality are extremely important, the focus of this work is on the design and fabrication of SOI devices for mainstream CMOS technologies. The following sections will describe some of the advantages and issues in SOI devices.

## 2.2 SOI Advantages

The primary advantages of SOI for scaled CMOS can roughly be divided into

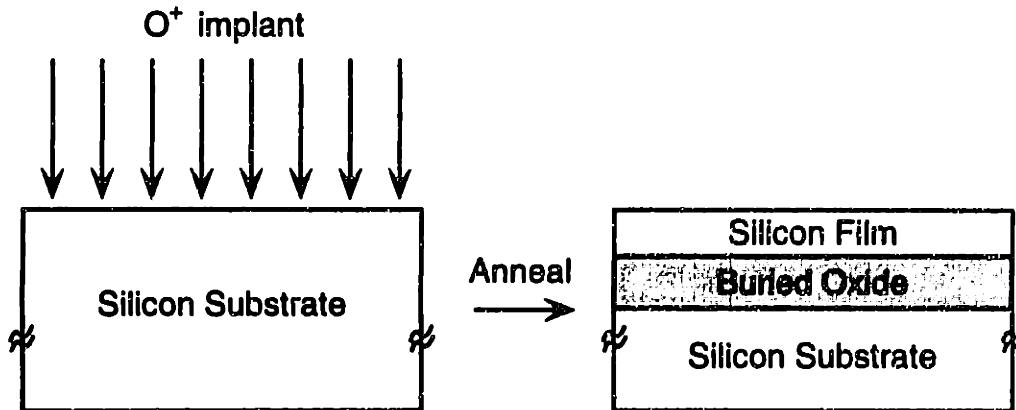


Figure 2-1: Schematic diagram of the formation of SOI wafers using the SIMOX implantation technique.

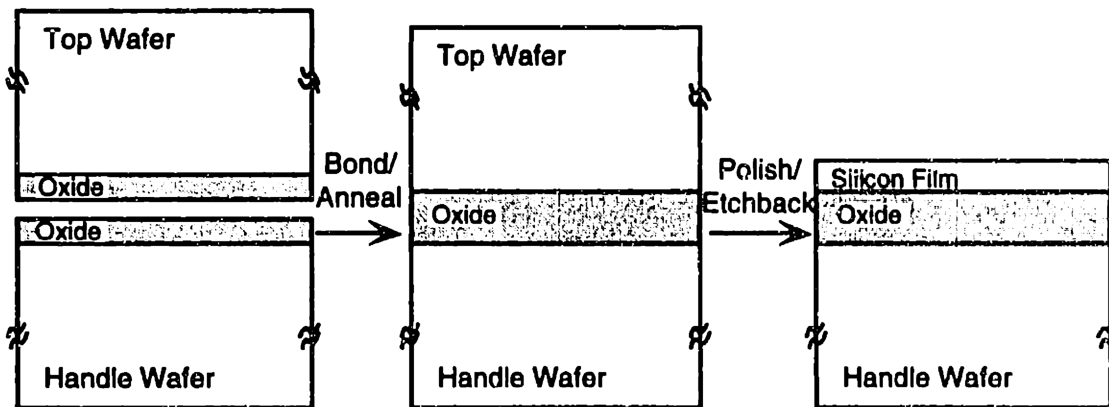


Figure 2-2: Schematic diagram of the formation of SOI wafers using a wafer bonding and polish or etch-back technique.

two categories: (i) process advantages, which result in simpler unit processes and reduced process complexity and (ii) performance advantages, which result in reduced parasitics and improved device and circuit speed. The main advantages from the fabrication side include simpler device isolation, suppression of latchup, and simpler shallow junction formation. On the performance side, SOI provides reduced parasitic capacitances, reduced sensitivity to back-gate bias, and improved immunity to single-event upset. When fully-depleted SOI devices are used, additional improvements in subthreshold slope and current drive can be obtained. Each of these advantages is described in detail below.

## 2.2.1 Fabrication Issues

*(i) Device isolation and latchup:* The SOI structure results in simple and planar device isolation for scaled geometries because the thickness of the LOCOS (local oxidation) or trench isolation need only consume the thickness of the silicon film which is typically below 100 nm. This results in a more planar process than conventional bulk technologies where isolation is typically on the order of 400-600 nm for sub-0.5 μm processes if LOCOS isolation is used [21,22]. This structure is also completely immune to latchup because the active device is fully dielectrically isolated from neighboring devices. Thus, well-to-well design rules can be significantly reduced leading to the potential for more compact layout in comparison to bulk processes [23].

*(ii) Shallow junction formation:* The SOI structure also allows the simple formation of shallow junctions because the junction depth of a device for thin silicon films is self-determined by the thickness of the silicon film ($t_{si}$). This eliminates the need for complex shallow junction techniques such as pre-amorphization and drain extensions that are necessary in bulk technologies [24] and potentially allows

simpler control of short-channel effects and drain-induced barrier lowering in SOI [25]. In addition, because the junction depth of the devices extends throughout the silicon film to the buried oxide, shallow junction leakage problems due to metal spiking or salicidation are also eliminated.

### 2.2.2 Performance issues

*(i) Source and drain junction capacitances:* The presence of the buried insulator reduces the areal junction capacitance of the device because typically the thicknesses of the buried oxide are substantially larger than the typical junction depletion widths of a scaled MOS device and the permittivity is a factor of 3 smaller for oxide than silicon. For a 0.25 μm technology, a reasonable substrate concentration is $1 \times 10^{17}$ $cm^{-3}$ [9], which results in a depletion width of 100 nm, and an areal capacitance of 1 $fF/\mu m^2$. This is in comparison to typical buried oxide thicknesses of 200-400 nm which result in areal capacitances of 0.08-0.17 $fF/\mu m^2$ [26]. The peripheral component of the source/drain capacitances in SOI devices is also substantially reduced from bulk processes because the device is fully-dielectrically isolated from the substrate.

*(ii) Back-gate bias effect:* The presence of the buried oxide prohibits a direct contact to the body of the film, thus the body is floating. This can be advantageous because the body or back-gate bias effect can be very small. In bulk devices, a non-zero source to body potential results in an increase in the device threshold voltage and correspondingly a decrease in drive current [6]. In SOI devices, the only control of the channel region from the back-gate is through a thick buried oxide (typically on the order of 400 nm). Although, the back-gate can influence the channel charge state, the potentials required for any modulation are much greater than typical power supply voltages. Thus, any typically-induced non-zero source to body

potential will have negligible effect on the device threshold voltage [10, 26]. This is particularly advantageous in stacked circuits, where several devices are connected in series, and pass transistors, where both nodes may vary over the full range of supply voltage [23].

*(iii) Soft-error immunity:* Single-event upset due to soft-errors occur when an energetic particle such as an alpha particle or a heavy ion (cosmic ray) penetrates a reverse-biased p-n junction [14]. In bulk devices, the path of the particle extends on the order of ten micrometers and creates electron-hole pairs along its trajectory. In the case of a NMOS transistor, for example, the holes created as a result of the alpha particle are collected by the p-type substrate as substrate current. The electrons are collected by the depletion layer and can potentially alter the charge state of the $n^+$ source or drain node if a large enough amount of charge is collected. It is the collection of these electrons that results in single-event upset. For deep-submicron technologies, the nodal capacitance and power supply voltages are decreasing thereby reducing the amount of charge needed to cause a soft-error. Thus, this issue is becoming increasingly important for future generation memories.

In SOI devices, the junctions are isolated from the substrate by the buried oxide so even if the trajectory of the alpha particle extends through the buried oxide into the substrate, it will not significantly alter the charge state at the source or drain depletion regions because there is minimal exposed depletion area.

### 2.2.3 Fully-depleted devices

All of the previous issues that have been discussed are advantages that are inherent to SOI regardless of the device design, i.e. they can be obtained with a bulk device design fabricated on an SOI substrate. To obtain additional advantages,

unique, SOI-specific device design options can be exploited. In particular, the channel doping of an SOI device can be designed such that the depletion width of the channel determined by $x_d = \sqrt{\frac{4\varepsilon_{si}\Phi_F}{qN_a}}$ is less than the thickness of the silicon film, $t_{si}$ where $\varepsilon_{si}$ is the permittivity of silicon, $\Phi_F$ is given by $\frac{2kT}{q}\, ln\left(\frac{N_a}{n_i}\right)$, and $N_a$ is the doping concentration. In this case, the device is said to be *fully-depleted* because the channel depletion region extends throughout the thickness of the silicon film and additional performance advantages can be obtained.

*(i) Steeper subthreshold slope:* The subthreshold slope of a conventional MOS device is given by [6]:

$$S = \frac{dV_G}{d(logI_D)} = \frac{kT}{q}\, ln\,(10)\,(1 + \frac{C_D}{C_{ox}}) \tag{2.1}$$

where $C_D$ is the depletion capacitance per unit area, $\frac{\varepsilon_{si}}{x_d}$, and $C_{ox}$ is the gate oxide capacitance per unit area, $\frac{\varepsilon_{si}}{t_{ox}}$. In fully-depleted SOI devices, because the depletion region extends throughout the film, the effective depletion capacitance of the device is a series combination of the silicon film capacitance, $C_{si} = \frac{\varepsilon_{si}}{t_{si}}$, and the buried oxide capacitance, $C_{box} = \frac{\varepsilon_{ox}}{t_{box}}$, therefore $C_D = \frac{C_{si}C_{box}}{(C_{si}+C_{box})}$. In typical SOI devices $t_{box}$ is on the order of 400 nm, thus $C_D$ in fully depleted devices is very small. This allows the subthreshold slope to approach the theoretical value of 60 mV/decade at room temperature [27]. In bulk devices, the subthreshold slope is closer to 80 mV/decade [9]. This steeper subthreshold slope can potentially allow the use of lower threshold voltages in SOI devices given the same off-state leakage requirements, which is particularly useful as power supply voltages are scaled down.

*(ii) Improved drive current:* Similar to the analysis above for subthreshold slope, the drain current of a long-channel MOSFET in the saturation region is given by [28]:

$$I_{dsat} = \frac{W\mu_n C_{ox}}{2L(1+\alpha)}(V_G - V_T)^2 \quad (2.2)$$

where $W$ and $L$ are the width and length of the device, $\mu_n$ is the carrier mobility, and $V_G$ and $V_T$ are the gate voltage and device threshold voltage. For partially-depleted and bulk devices, the $\alpha$ in this case approximately accounts for the amount of gate voltage that is used to support the excess depletion charge under the inversion region as the potential varies along the channel. A simple expression for $\alpha$ can be obtained by approximating the square root dependence of the localized threshold voltage in the channel with a straight line and is given by $\alpha = \frac{C_D}{C_{ox}}$ [6]. In a fully-depleted device, there is no additional charge to deplete in the body. Although the potential along the channel increases, the closest charge to deplete is beneath the buried oxide so the dependence of the localized threshold voltage in the channel on the channel-substrate voltage is quite weak. An exact expression for the dependence can be obtained by solving Poisson's equation at both interfaces in the SOI and is given by $\alpha = \frac{C_{si}C_{box}}{(C_{si}+C_{box})C_{ox}}$ [28]. This results in a smaller $\alpha$ in fully-depleted devices than in bulk devices, hence, the drive current and the device transconductance are potentially increased in fully-depleted SOI devices [29, 30].

Given these advantages, SOI circuits were predicted to have significantly improved circuit performance over conventional bulk technologies while simultaneously achieving scaled geometries with a simpler fabrication process [11].

# 2.3 SOI Issues

Of course, as with any technology, SOI also has some disadvantages and remaining issues that must be solved before its implementation into commercial products. As mentioned in the introduction, given the present maturity of bulk silicon technology with 0.5 μm geometries in production, and 0.35 μm in advanced development [4], a realistic target insertion point for SOI would be at the 0.25 μm level of integration and below. However, systematic studies evaluating the issues surrounding SOI technology at the device dimensions of interest are needed to assess SOI's true potential. The intrinsic SOI device issues that require investigation in the deep-submicrometer region include the channel design, parasitic source/drain series resistance, heat flow effects and high-field effects.

## 2.3.1 SOI Channel Design

The core issue at the center of SOI devices is the design of the channel or the appropriate channel engineering. There have been many reports in the literature about the various options available for SOI devices in terms of the channel design [31]. These include options such as fully-depleted vs. partially-depleted devices [32]; various gate materials to adjust the gate work-function [31,33]; and the tradeoffs between substrate concentration, silicon film thickness, oxide thickness and buried oxide thickness [31,34]. The various combinations of these options determine the threshold voltage, subthreshold slope, and short-channel behavior of SOI devices. Although any one of these parameters has been studied or optimized in the literature, this has often been done at the expense of unrealistic values for other parameters. One frequent problem is the difficulty in obtaining reasonable threshold voltage values for fully-depleted devices with good

short-channel behavior. This is difficult because in order to achieve full-depletion in the silicon film, either thin films and/or light channel doping concentrations are required, but both of these tend to decrease the absolute value of the threshold voltage. The challenge is to evaluate the design space where all of the parameters satisfy the requirements for a particular application or technology so that reasonable and fair comparisons can be made between bulk and SOI technologies.

### 2.3.2 Parasitic Source/Drain Resistance

Related to the channel engineering discussed in the previous section, most SOI devices in the deep-submicrometer regime require ultra-thin silicon films ($t_{si} <$ 80 nm) to adequately control short-channel effects [31,35]. However, as the silicon film thickness decreases, the sheet resistance of the source/drain increases proportionally, thus increasing the parasitic source/drain series resistance. This effect tends to obscure most of the intrinsic performance advantages of SOI for ultra-thin films [35,36] and thus must be minimized. The impact of this series resistance must be accounted for in the device design so that the optimal silicon film thickness is chosen to maximize the benefits of SOI.

### 2.3.3 Self-Heating Effects

Heat flow effects in SOI devices are complicated because the thermal conductivity of silicon dioxide is 100 times lower than that of the silicon substrate. The presence of the silicon dioxide between the active region and the silicon substrate heat sink impedes device cooling and causes device temperatures to rise [37]. This is a potential concern because increased circuit operating temperatures may lead to metal reliability issues if the interconnects are subjected to high temperatures and large temperature gradients. In addition, device temperature

rises can potentially lead to more difficult device modeling and parameter extraction because both electrical and thermal time constants must be considered. Thus, self-heating in SOI MOSFETs is a critical issue and temperature rises must be measured and modeled.

### 2.3.4 High-field Effects

In terms of high-field effects, the SOI device is unique because the presence of the buried oxide creates a floating body with no contact to the substrate. This becomes important in the high-field region because majority (channel body) carriers generated by impact ionization near the drain cannot be collected by the substrate as occurs in bulk devices. Those carriers accumulate in the body region and in the most severe case can forward bias the body-source junction and cause breakdown at much lower voltages than typical bulk devices [38]. In addition to the reduction in breakdown voltage, the floating body is also a concern for hot-carrier reliability. Because SOI devices do not have substrate contacts, the typical monitor for device degradation, i.e. substrate current, is not available. This lack of a reliable monitor for device degradation makes standard lifetime extrapolation very difficult. In addition, the overall issue of hot-electron degradation is clouded by the presence of two silicon/silicon dioxide interfaces in the device. To effectively design SOI devices, the breakdown voltage and hot-carrier reliability must be characterized and optimized.

### 2.3.5 Summary

Given the advantages and issues described in the previous sections, the primary goals of this work are two-fold: (a) to systematically evaluate the potential advantages of SOI in the context of sub-0.25 μm technologies for high-performance

CMOS applications and (b) to study the intrinsic device issues and problems associated with SOI technologies, assess their severity and potentially propose solutions. Each of the topics discussed above will be examined in detail in the next four chapters. After the examination of the intrinsic device issues, a comparison of the device performance tradeoffs in SOI technology in comparison to bulk technologies will be made. In particular, the tradeoff between current drivability and short-channel effects is studied.

# Chapter 3

# SOI Channel Design

## 3.1 Introduction

Scaling devices into the deep-submicrometer region, SOI offers unique options for the SOI channel design. The primary issue in deep-submicrometer SOI device design is the control of short-channel effects. As discussed earlier, there are many options for the control of short-channel effects in SOI. These include the use of fully or partially-deleted devices; tradeoffs between channel doping concentration ($N_a$), silicon film thickness ($t_{si}$), gate oxide thickness ($t_{ox}$), and buried oxide thickness ($t_{box}$); and the option of using novel gate materials to engineer the metal-to-semiconductor work function ($\phi_{ms}$).

Previous work has shown that scaling silicon film thickness and buried oxide thickness are important in the reduction of SOI short-channel effects [35, 39]. Some work has also explored the different design considerations in SOI [31]. However, to exploit the unique options in SOI, a careful examination of the design tradeoffs focusing particularly on the short-channel effects in the deep-submicrometer region is necessary. In this section, short-channel effects in SOI are examined in comparison to conventional bulk devices for scaling into the deep-submicrometer region using two-dimensional numerical simulations. Using the results of these simulations, optimal design regions which satisfy both nominal and short-channel threshold voltage constraints are studied for deep-submicrometer SOI technologies. The results of the simulations are used to design the devices that are fabricated in the following sections.

## 3.2 Simulation Strategy

Two-dimensional numerical simulations using MINIMOS5 [40] are used to calculate the long-channel threshold voltage; $V_T$ shift due to the short-channel effect ($\Delta V_{T(SCE)}$); and $V_T$ shift due to drain-induced barrier lowering ($\Delta V_{T(DIBL)}$) in SOI as a functicn of device parameters. In this work, the short-channel effect is specifically referring to two-dimensional charge-sharing, i.e. the reduction of the channel charge due to the encroachment of the source and drain depletion regions as the device channel length is reduced [41]. Drain-induced barrier lowering (DIBL) refers to the lowering of the potential barrier at the source due to an increase in drain potential [42]. Although DIBL is also a measure of short-channel effects in a given technology, it is defined independently because it is used in determining the optimal design space for a nominal effective channel length.

The simulated structure is an SOI MOSFET with uniform doping in the channel, source, and drain regions. Two different technology generations are simulated. The electrical effective channel lengths, $L_{eff}$, of the simulated devices are 0.2 μm and 0.1 μm with gate oxide thicknesses of 7 and 5 nm and maximum drain voltages of 2.5 and 1.5 V, respectively. Abrupt source and drain junctions are used to fix the $L_{eff}$ of the device over a large range of channel dopings and silicon film thicknesses. This does not change the results significantly from graded junction profiles because the depletion region is mostly absorbed in the channel. In comparing abrupt and graded profiles, the *electrical* effective channel length should be fixed although the metallurgical channel length may vary. This is particularly critical in the deep-submicrometer region because even 10 nm difference in $L_{eff}$ can result in large differences in short-channel characteristics. In this study, $L_{eff}$ is extracted electrically from simulation data using the technique reported in [43,44].

# 3.3 Threshold Voltage Simulations

## 3.3.1 Long-Channel Threshold Voltage

Figure 3-1 shows the results of simulations of long-channel threshold voltage as a function of silicon film thickness for four different channel doping concentrations. Threshold voltage is defined as the gate-to-source voltage at a constant current of $I_D=10^{-7}(W/L_{eff})$ (A) where the width, $W$ of the device is 10 μm. The channel doping, $N_a$, and the silicon film thickness, $t_{si}$, determine the mode of operation for SOI devices, i.e. whether the device is fully or partially-depleted. Notice that for the thicker silicon film thicknesses, the $V_T$ is independent of silicon film thickness which is an indication that the device is partially-depleted. For these

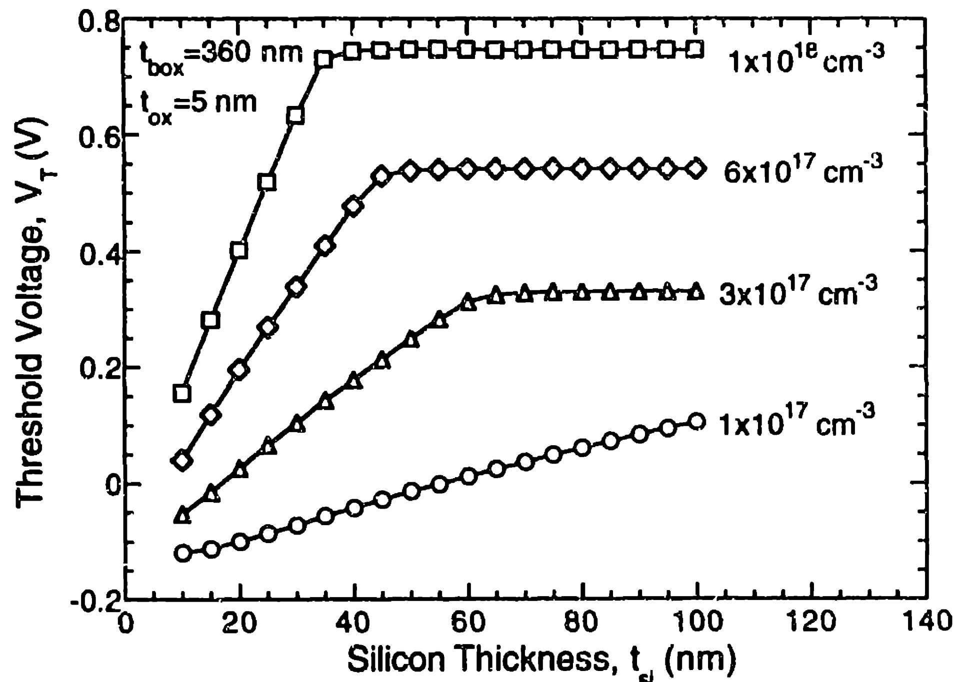


Figure 3-1: Long-channel threshold voltage vs. silicon film thickness for several channel doping concentrations.

devices, once the gate oxide thickness and the channel doping concentration are chosen, the $V_T$ is determined by conventional long-channel theory of MOSFETs.

For thin silicon films, the $V_T$ is linearly dependent on silicon film thickness because the amount of channel charge is limited by the silicon film, i.e. $t_{si} < x_d$ where $x_d = \sqrt{\frac{4\varepsilon_{si}\Phi_F}{qN_a}}$, thus these devices are called fully-depleted. For the devices in Fig. 3-1, full-depletion occurs for $t_{si}$ less than approximately 35 nm for $N_a$ = 1x10$^{18}$ cm$^{-3}$, 45 nm for $N_a$ = 6x10$^{17}$ cm$^{-3}$, 60 nm for $N_a$ = 3x10$^{17}$ cm$^{-3}$, and 100 nm for $N_a$ = 1x10$^{17}$ cm$^{-3}$. Although the devices examined in this study are NMOSFETs, surface-channel PMOSFETs using p$^+$ polysilicon would exhibit similar trends, with the channel doping being n-type.

### 3.3.2 Short-Channel Threshold Voltage

The most important factor for deep-submicron channel design is the sensitivity of the device to short-channel effects. Figures 3-2 and 3-3 show the results of simulations examining the $V_T$ shift due to the short-channel effect, $\Delta V_{T(SCE)}$ and the $V_T$ shift due to drain-induced barrier lowering, $\Delta V_{T(DIBL)}$ for a nominal $L_{eff}$ = 0.1 μm device, where

$$\Delta V_{T(SCE)} = V_T(L_{eff} = 1\ \mu m) - V_T(nominal\ L_{eff})\ @\ V_{DS} = 0.05\ V \tag{3.1}$$

$$\Delta V_{T(DIBL)} = V_T(V_{DS} = 0.05\ V) - V_T(max.\ V_{DS})\ @\ nominal\ L_{eff} \tag{3.2}$$

The same quantities for a bulk device with uniform channel doping and a junction depth of 80 nm are shown on the right axis for comparison.

For both SCE and DIBL, the $\Delta V_T$ is a strong function of $N_a$ and $t_{si}$. As $t_{si}$ is reduced, the $\Delta V_T$ is reduced in fully-depleted devices. This occurs because the effective source and drain depth of the device is reduced with decreasing $t_{si}$ and the front gate's influence on the back-surface potential is increased, both of which improve short-channel effects and DIBL. For partially-depleted SOI devices, the $\Delta V_T$ approaches the bulk case because the devices have similar junction depths and channel doping. However, near the transition between full and partial depletion, a peak, i.e. worst-case condition, exists in the $\Delta V_T$ curve.

Examination of the two-dimensional potential contours indicate that this peak is due to coupling through the buried oxide region (Fig. 3-4). Physically, the depletion charge in the source and drain cannot terminate in the buried oxide region, and thus must either terminate in the substrate below the buried oxide or in the channel region. Because the buried oxide is thick, a portion of the depletion

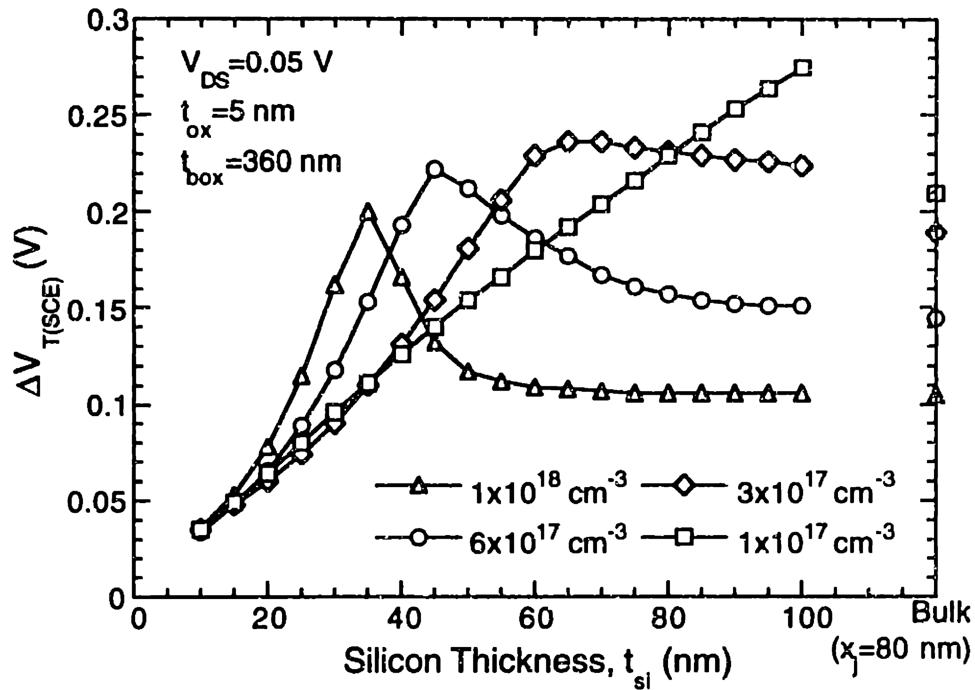


Figure 3-2: Threshold voltage shift due to the short-channel effect, $\Delta V_{T(SCE)}=V_T(L_{eff}=1\ \mu m)-V_T(L_{eff}=0.1\ \mu m)$, as a function of silicon film thickness for four different channel dopings, $V_{DS}$ = 0.05 V, $t_{ox}$ = 5 nm, and $t_{box}$ = 360 nm.

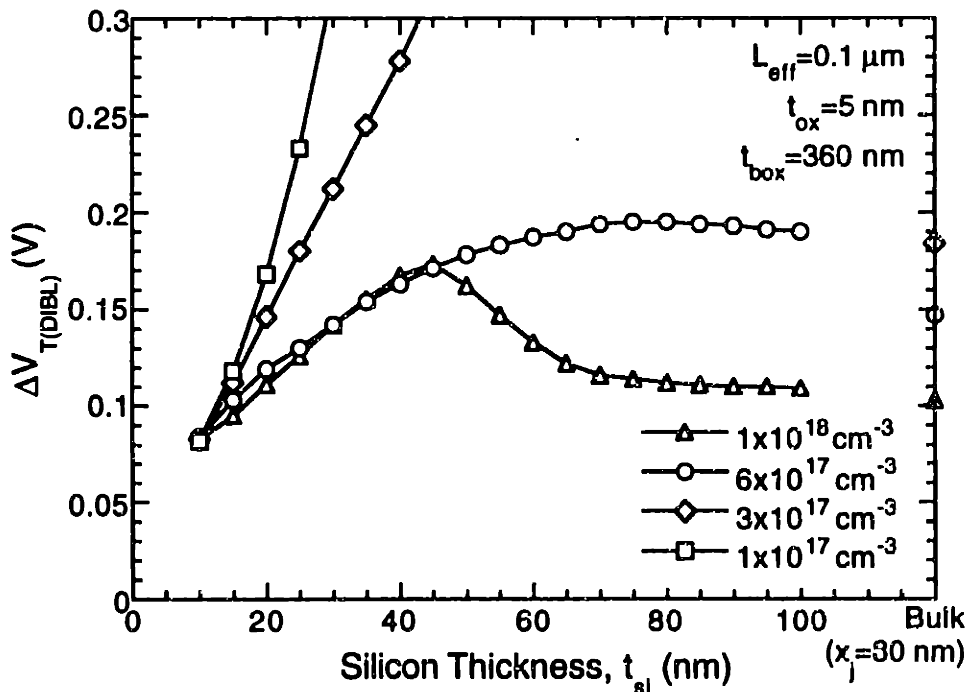


Figure 3-3: Threshold voltage shift due to drain-induced barrier lowering, $\Delta V_{T(DIBL)}=V_T(V_{DS}=0.05\ V)-V_T(V_{DS}=1.5\ V)$, as a function of silicon film thickness for four different channel dopings, $L_{eff}$=0.1 µm, $t_{ox}$=5 nm, and $t_{box}$=360 nm.

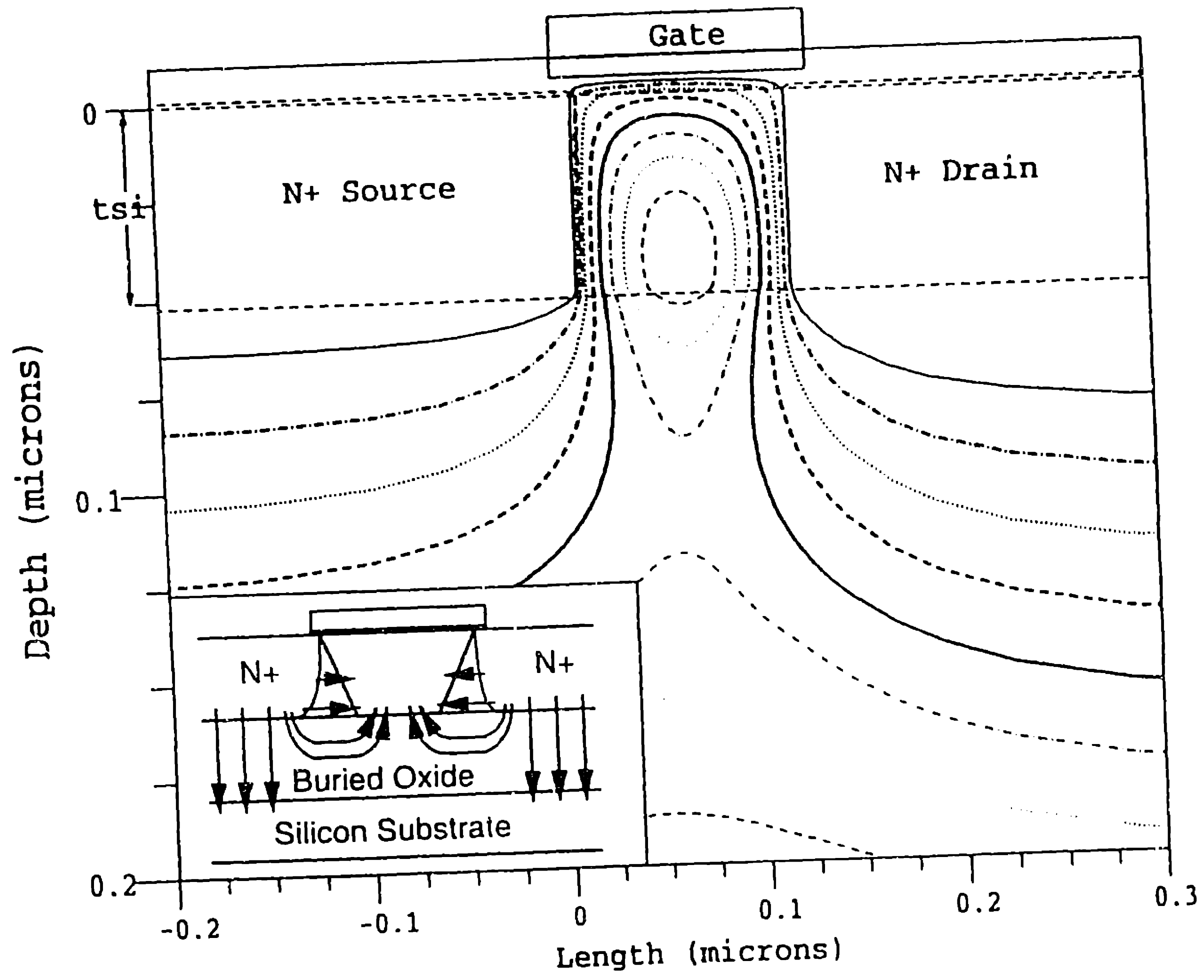


Figure 3-4: Electrostatic potential contours in a SOI device indicating 2-D coupling through the buried oxide. Electric field lines (shown schematically in the inset) can be drawn perpendicular to the potential contours. Device parameters are $L_{eff} = 0.1$ μm, $V_{DS} = 0.05$ V, $V_{GS}=V_T$, $N_a = 6\text{x}10^{17}$ cm$^{-3}$, $t_{si} = 50$ nm, $t_{box} = 360$ nm.

charge will terminate in the channel resulting in an additional short-channel effect in thin-film SOI. This is shown qualitatively in Fig. 3-4 by the potential contours in the channel and buried oxide region. Electric field lines can be drawn perpendicular to the potential contours and show the coupling from the source and drain into the channel [45]. Hence, fully-depleted SOI can exhibit aggravated short-channel effects, i.e. *larger* $\Delta V_T$, than partially-depleted or bulk devices depending on the device design. To achieve improved short-channel effects in fully-depleted SOI, $t_{si}$ must be considerably smaller than the junction depth of a comparable bulk technology. Partially-depleted devices are similar to bulk devices as long as the silicon film thickness is far from the breakpoint between full and partial depletion.

Reducing the buried oxide thickness, $t_{box}$, can help alleviate the two-dimensional charge-sharing through the buried oxide as shown in Fig. 3-5. This improvement occurs because the bottom substrate is brought closer to the source and drain regions provided there is no significant depletion in the substrate. Note that in reducing $t_{box}$ from 360 nm to 100 nm, the improvement in $\Delta V_{T(DIBL)}$ is most significant for the lower channel doping concentrations. Physically, this can be understood because the drain-to-channel depletion widths of the lower channel doping concentrations are on the order of 60-100 nm. Thus, by reducing $t_{box}$ to 100 nm, more of the field lines will terminate underneath the oxide. However, for $N_a$=1x10$^{18}$ cm$^{-3}$, the drain-to-channel depletion width is less than 40 nm. Hence, even though $t_{box}$ has been reduced, the drain-to-channel depletion width is still much smaller than $t_{box}$ and the improvement in $\Delta V_{T(DIBL)}$ is minimal. To obtain improved short-channel effects, $t_{box}$ should be on the order of the drain-to-channel depletion width for a given channel doping concentration. However, the lower limit of $t_{box}$ is probably about 80 nm because of performance tradeoffs with junction

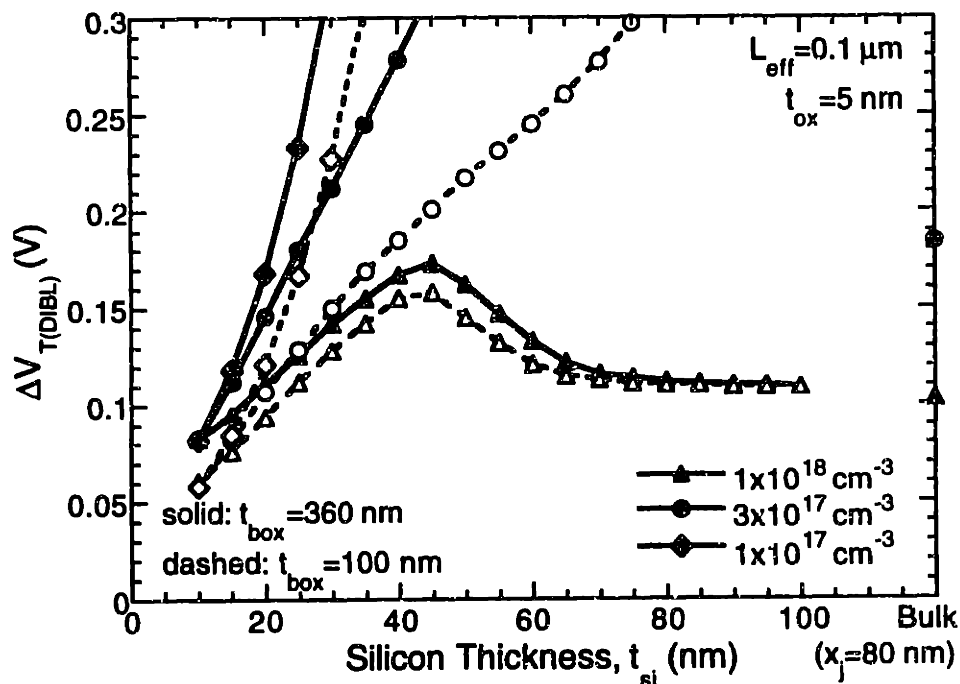


Figure 3-5: Threshold voltage shift due to drain-induced barrier lowering for two different buried oxide thicknesses, $V_{DS}$=1.5 V, $t_{ox}$=5 nm, $L_{eff}$=0.1 μm.

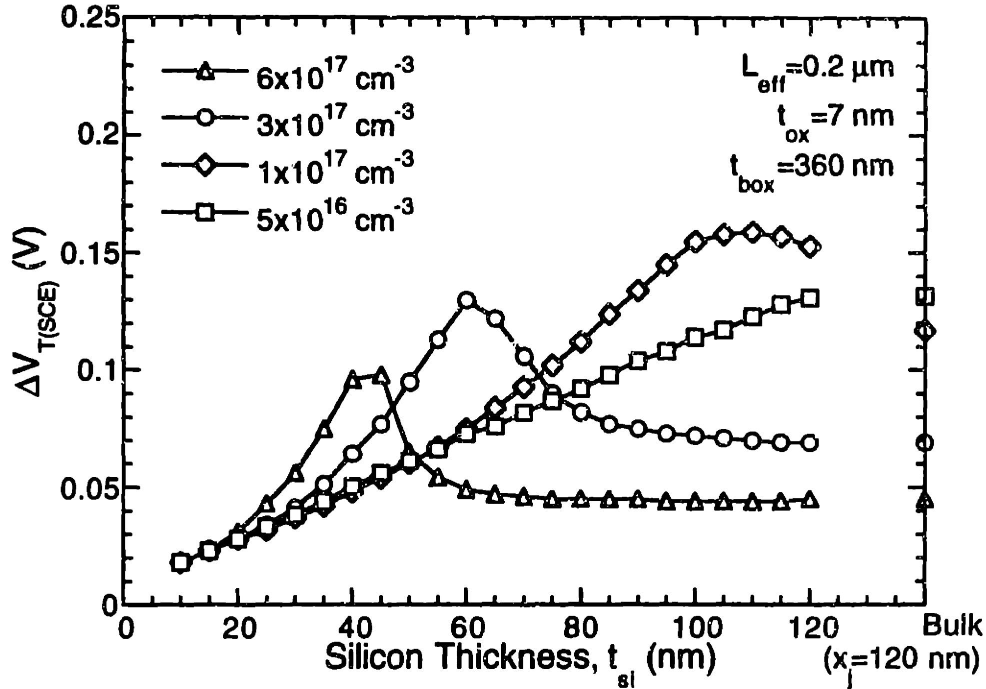


Figure 3-6: Threshold voltage shift due to the short-channel effect, $\Delta V_{T(SCE)}=V_T(L_{eff}=1\ \mu m)-V_T(L_{eff}=0.2\ \mu m)$, as a function of silicon film thickness for four different channel dopings, $V_{DS}$=0.05 V, $t_{ox}$=7 nm, and $t_{box}$=360 nm.

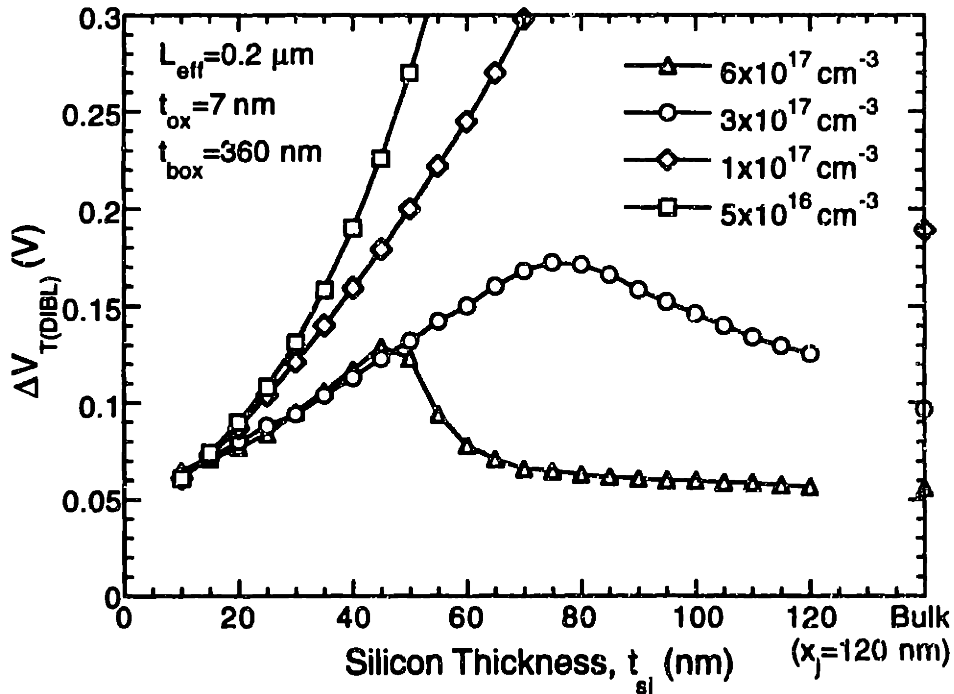


Figure 3-7: Threshold voltage shift due to drain-induced barrier lowering, $\Delta V_{T(DIBL)}=V_T(V_{DS}=0.05\ V)-V_T(V_{DS}=2.5\ V)$, as a function of silicon film thickness for four different channel dopings, $L_{eff}$=0.2 μm, $t_{ox}$=7 nm, and $t_{box}$=360 nm.

capacitance. Similar trends in the $\Delta V_{T(SCE)}$ and $\Delta V_{T(DIBL)}$ are observed in $L_{eff}$ = 0.2 µm devices as shown in Figs. 3-6 and 3-7.

### 3.3.3 Limitation of the Simulations

The simulations were done using a single-carrier, drift-diffusion model without impact ionization to focus on the electrostatic behavior. This simplification is valid in fully-depleted devices because the $V_T$ is relatively insensitive to the impact-ionization-triggered floating-body effect. In partially-depleted devices, floating-body effects can cause a decrease in $V_T$ at high drain biases even at long channel lengths. In the total design of the SOI MOSFET, this must be considered. This will be discussed further in the next section.

## 3.4 Optimal Design Space

Using this type of analysis, the optimal design space in 0.2 µm and 0.1 µm $L_{eff}$ technologies is examined. In the previous figures examining the short-channel effect and DIBL, the absolute value of the $V_T$ varied over a large range. The challenge with SOI device design is to achieve acceptable absolute value of $V_T$ as well as acceptable short-channel effect and DIBL. The two criteria used for the design space analysis are: a) low-$V_{DS}$ nominal $V_T$ between 0.4 and 0.7 V at the minimum $L_{eff}$ and b) total $\Delta V_T/\Delta V_{DS}$ shift due to DIBL less than 60 and 100 mV/V for supply voltages of 2.5 and 1.5 V in the 0.2 µm and 0.1 µm technologies respectively ($\Delta V_{T(DIBL)} \leq 150$ mV). The results of the simulations are shown in Figs. 3-8 and 3-9. Both $n^+$ polysilicon and mid-gap workfunction, e.g. TiN or poly-SiGe[46,47], gate materials are used to examine inversion-mode SOI MOSFETs. The use of alternate gate materials reduces the doping concentrations needed to achieve acceptable nominal $V_T$ values. The shaded areas represent the intersection

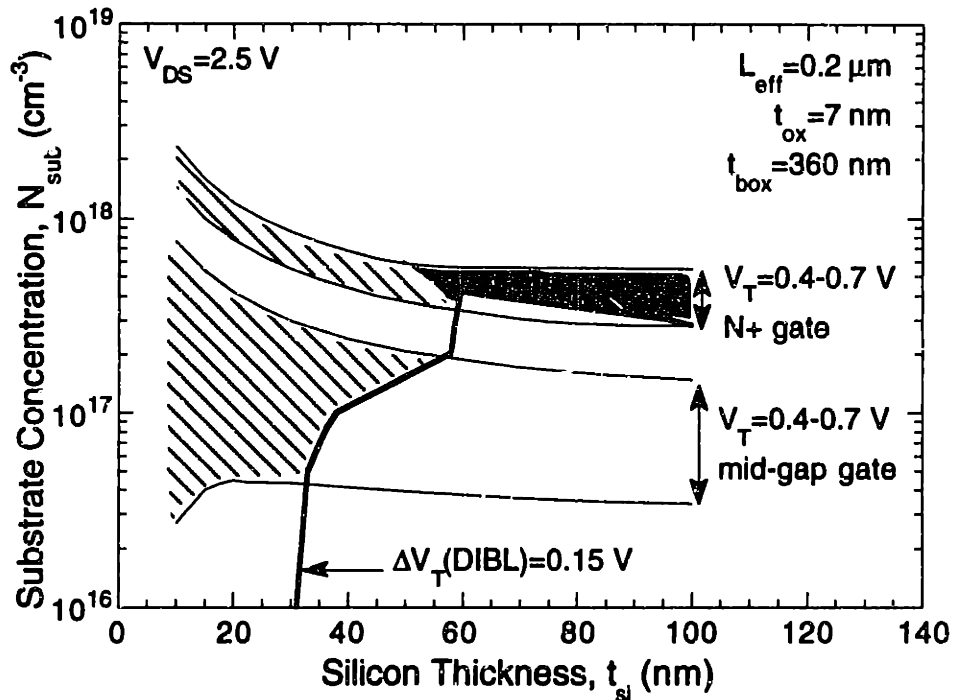


Figure 3-8: Threshold voltage design curves for $L_{eff}$ = 0.2 μm. Nominal threshold voltages of 0.4 to 0.7 V at $V_{DS}$ = 0.05 V defined in lighter lines; "acceptable" DIBL values, $\Delta V_T(DIBL) \leq$ 150 mV at indicated $V_D$ values defined in the heavy solid line. Shaded areas correspond to the intersection of the regions which satisfy acceptable nominal threshold voltage and DIBL constraints. The dashed region represents fully-depleted devices and the dark shaded region represents partially-depleted devices that satisfy the two criteria. The device parameters for the 0.2 μm technology are $t_{ox}$ = 7 nm, $t_{box}$ = 360 nm, and maximum $V_D$ = 2.5 V.

of the regions that satisfy both the nominal and DIBL criteria with the dashed lines indicating the fully-depleted region and the dark shading indicating the partially-depleted region.

As shown in Fig. 3-8, for $L_{eff}$ of 0.2 µm, $t_{si}$ must be under 60 nm to achieve fully-depleted devices with $n^+$ polysilicon gate material in the specified $V_T$ range. In the case of mid-gap workfunction gate material, $t_{si} < 40$ nm is required because the lower channel dopings required to achieve $V_T$'s in the same range have worse short-channel effects.

Scaling devices into the 0.1 µm regime, even thinner silicon films as well as higher channel dopings are required (Fig. 3-9). For the mid-gap workfunction gate material, fully-depleted devices require $t_{si}$ less than 25 nm. Such very thin silicon films are difficult to use from a manufacturing standpoint because of the intrinsic variation in $t_{si}$ across a wafer and the high parasitic source/drain resistance associated with very thin silicon films. For $n^+$ polysilicon gates, $t_{si}$ should be kept below 35 nm and $N_a$ above $8 \times 10^{17}$ cm$^{-3}$. Although the film thickness restrictions are somewhat relaxed, such high channel dopings in fully-depleted devices are also a concern because the sensitivity of $V_T$ to $t_{si}$ variation increases with increasing channel doping. Reducing $t_{box}$ to 100 nm as shown in Fig. 3-9 increases the acceptable design region by about 5-10 nm. This increases the acceptable $t_{si}$ to about 40 nm for n+ polysilicon gates, but silicon thickness uniformity requirements for these films must still be very tight.

Another possible strategy for the design of 0.1 µm devices is to use partially-depleted devices (i.e. $t_{si} > 60$ nm). In this case, the film thickness restrictions are removed and the design for short-channel effects is identical to the conventional bulk case. However, partially-depleted devices suffer from floating body effects, which can increase the off-state leakage current. As noted earlier, these floating

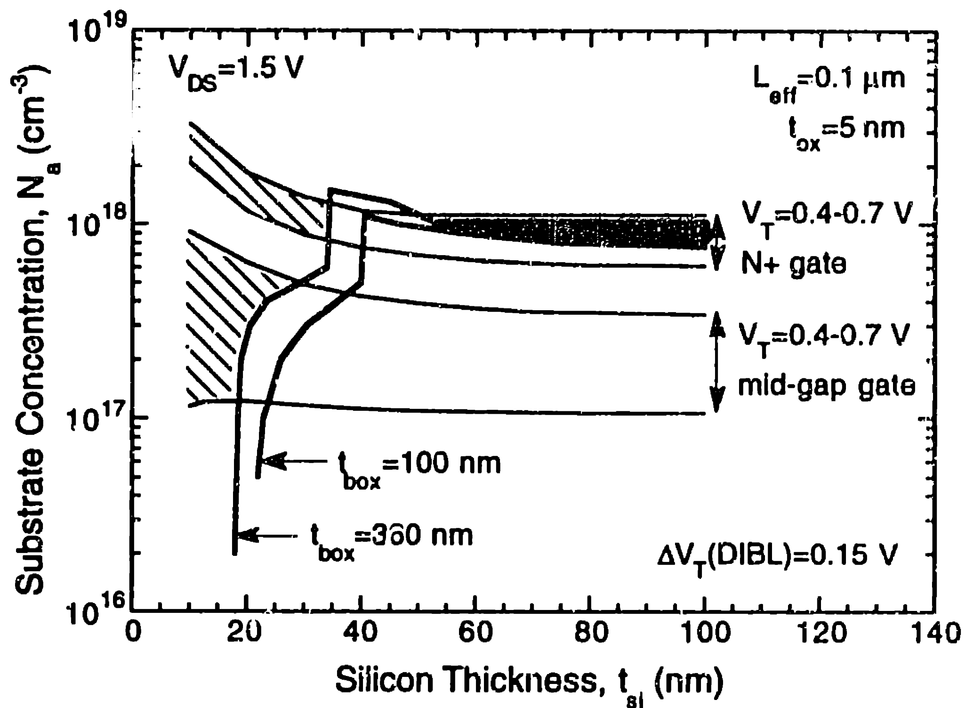


Figure 3-9: Threshold voltage design curves for $L_{eff}$= 0.1 μm. Same regions as in Fig. 3-8. The device parameters for the 0.1 μm technology are $t_{ox}$ = 5 nm, $t_{box}$ = 360 nm, and maximum $V_{DS}$ = 1.5 V. The effect of reducing $t_{box}$ to 100 nm is shown for comparison.

body effects result in a channel-length *independent* shift in the device $V_T$ at high drain biases which is not accounted for in these simulations. This does not modify the electrostatic behavior, i.e. channel-length *dependent* shifts in $V_T$, however to achieve acceptable off-state leakage, the low-$V_{DS}$ nominal $V_T$ for partially-depleted devices would likely be confined to the high end of the allowable range. This effect will be examined in more detail in Chapter 7.

## 3.5 Accumulation-mode Devices

Another strategy that has been suggested for the design of SOI devices is the use of accumulation-mode devices [48]. These devices are similar to a bulk buried-channel configuration, i.e. NMOS devices use $p^+$ polysilicon gate material and n-type channel doping and PMOS devices use $n^+$ polysilicon gate material and p-type channel doping. Conduction in these devices occurs when the device is accumulated with carriers at the interface as opposed to the "conventional" surface-channel inversion-mode devices discussed in the previous section, in which conduction occurs through an inversion layer at the surface. Although these devices have been used for 0.5 μm technologies with some success, they were not examined in this study because the short-channel effects are even more severe than in the fully-depleted case with mid-gap gate workfunction. Simulations show that accumulation-mode devices require significantly thinner $t_{si}$ to meet $L_{eff}$ = 0.1 μm device requirements. Subthreshold simulations for accumulation-mode NMOS devices are shown in Fig. 3-10. To achieve a reasonable $V_T$ of about 0.5 V, a n-body doping of $3 \times 10^{17}$ $cm^{-3}$ is required for $t_{si}$=20 nm and $1 \times 10^{18}$ $cm^{-3}$ for $t_{si}$=10 nm. However, the $\Delta V_{T(DIBL)}$ for $t_{si}$=20 nm is 350 mV which is unacceptably high. To achieve acceptable short-channel effets, i.e. $\Delta V_{T(DIBL)} < 150$ mV, $t_{si}$ must be in the

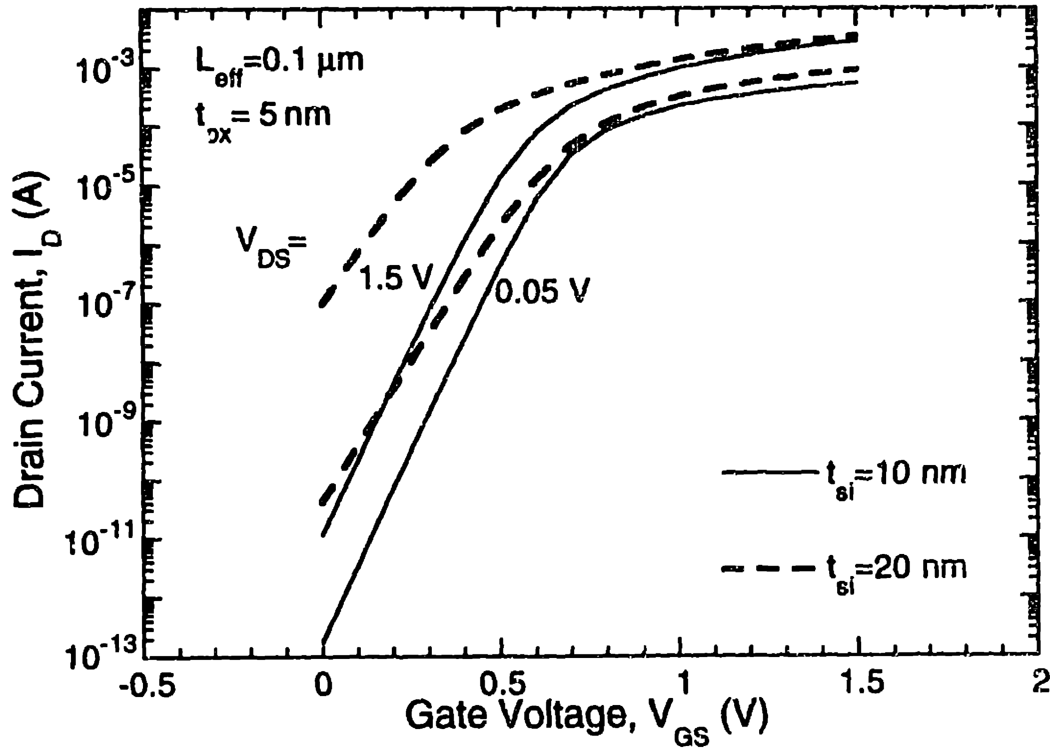


Figure 3-10: Simulations of accumulation-mode devices for $L_{eff}$=0.1 µm and $t_{ox}$=5 nm. To achieve nominal low-$V_{DS}$ $V_T$ of ~0.5 V, n-body doping of 3x10$^{17}$ cm$^{-3}$ is required for $t_{si}$=20 nm and 1x10$^{18}$ cm$^{-3}$ for $t_{si}$=10 nm. The $\Delta V_{T(DIBL)}$ for $t_{si}$=20 nm is 350 mV and for $t_{si}$=10 nm is 140 mV.

range of 10-12 nm. Thus, accumulation-mode devices are more difficult to scale than surface-channel inversion-mode devices.

## 3.6 Parametric Sensitivities

The final issue to be examined through simulations is the sensitivity of SOI parameters to silicon film thickness. SOI wafers intrinsically have a variation in silicon film thickness across the wafer and from wafer to wafer. This variation can lead to additional $V_T$ and $I_{off}$ spread as compared to conventional bulk MOSFETs because of the dependence of both long-channel and short-channel $V_T$ on $t_{si}$.

Figure 3-11 shows the sensitivity of threshold voltage to silicon film thickness variation, $\frac{\Delta V_T}{\Delta t_{si}}$, for several channel doping concentrations. The sensitivity is extracted from simulations by:

$$\frac{\Delta V_T}{\Delta t_{si}} = \frac{V_T(@nominal t_{si}) - V_T(@nominal t_{si} - 5nm)}{5nm} \quad @\, max.\ V_{DS} \qquad (3.3)$$

To understand the behavior of these curves, it is useful to examine the magnitude and sign of the sensitivity components. The sensitivity can be decomposed into long-channel and short-channel components.

The magnitude of the long channel sensitivity can be simply formulated in the fully-depleted case because the one-dimensional channel bulk charge is given by $|Q_B| = qN_a t_{si}$, thus $\frac{\Delta Q_B}{\Delta t_{si}} = qN_a$. From this formulation, it is clear that the magnitude of the one-dimensional sensitivity increases with increasing doping concentration. Also note that the sign of the sensitivity is positive in this case, i.e. a decrease in $t_{si}$ will decrease $Q_B$ and the magnitude of $V_T$.

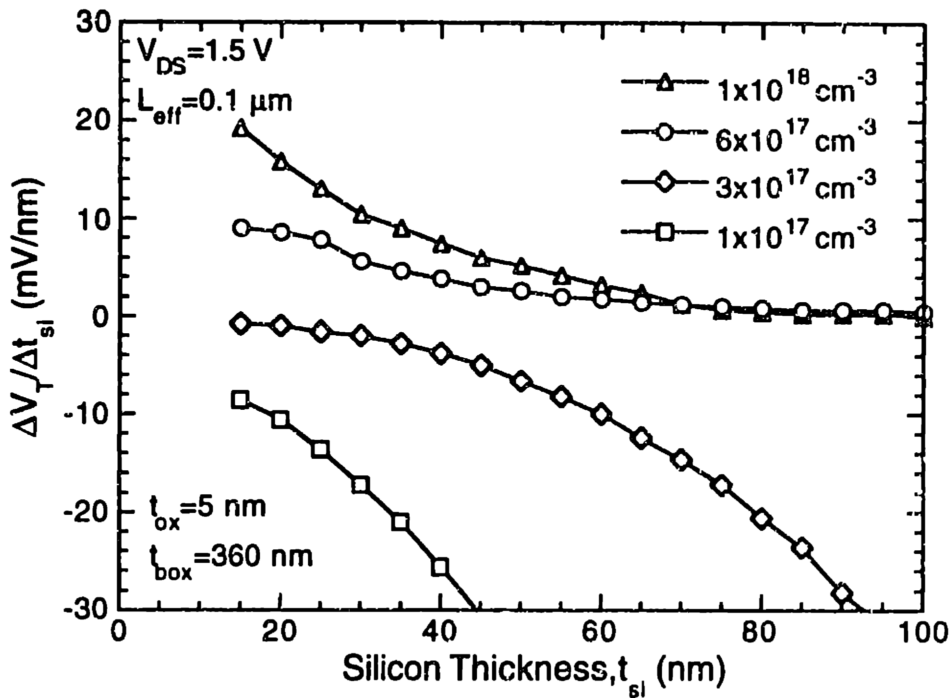


Figure 3-11: Threshold voltage sensitivity, $\frac{\Delta V_T}{\Delta t_{si}}$ vs. silicon film thickness for four different constant doping concentrations including both long-channel and short-channel effects.

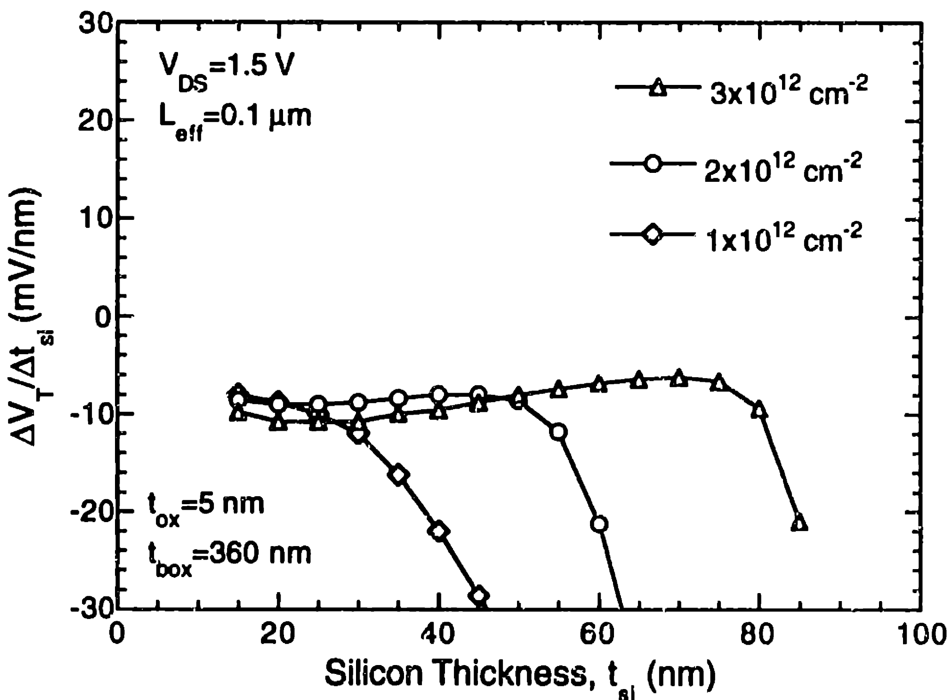


Figure 3-12: Threshold voltage sensitivity, $\frac{\Delta V_T}{\Delta t_{si}}$ vs. silicon film thickness for three different channel doses including both long-channel and short-channel effects.

For the short-channel or two-dimensional case, the sensitivity of $V_T$ to $t_{si}$ comes from the short-channel effects and DIBL. Referring back to the plots of $\Delta V_{T(SCE)}$ and $\Delta V_{T(DIBL)}$ in Figs. 3-2 and 3-3, notice that in the fully-depleted region, as $t_{si}$ decreases, $\Delta V_T$ decreases. In some cases, the slope of the $\Delta V_T$ changes quite significantly over a small range of $t_{si}$. The magnitude of the sensitivity (or the slope of the $\Delta V_T$ curves) increases with decreasing doping concentration, i.e. the short-channel effects at lower doping concentrations are more sensitive to $t_{si}$ variation. Also, the sign of the sensitivity is negative, i.e. as $t_{si}$ increases, the magnitude of $\Delta V_T$ increases, and the absolute value of $V_T$ decreases. Thus, the long-channel and short-channel $\frac{\Delta V_T}{\Delta t_{si}}$ are competing phenomena.

Given these phenomena, the behavior of the total sensitivity as shown in Fig. 3-11 can be understood. For the heavier channel dopings, the dominant component of the sensitivity is the long-channel component because the short-channel effects are well-controlled. However, for lower channel dopings, the dominant component of the sensitivity is the short-channel component, particularly for thicker silicon films.

In all the previous simulations, the dopant concentration was assumed to be constant throughout the film and was varied over a range of silicon film thicknesses. However, from the sensitivity analysis, the use of a constant concentration over a range of silicon film thicknesses results in fairly high sensitivity of threshold voltage to silicon film thickness. It has been suggested that the $V_T$ sensitivity to $t_{si}$ can be reduced considerably by following a constant dose approach, i.e. the total dose in the film is kept constant over a range of silicon film thicknesses [49]. Although the ideal case of constant dose cannot be achieved, optimization of the implantation schedule can achieve a minimization of the dose variation over a range of silicon film thicknesses [50]. Using this approach, the

simulations show that the sensitivity to $t_{si}$ can be reduced as shown in Fig. 3-12. Once again, the total sensitivity is composed of the long-channel and short-channel $\frac{\Delta V_T}{\Delta t_{si}}$. However, if the dose is kept constant, the channel charge, $Q_B$ is approximately constant with silicon film thickness because as the silicon film is thinned, the total concentration in the film increases. Hence, the long-channel $V_T$ sensitivity to $t_{si}$ is very small. The most significant component of the sensitivity is now the short-channel component. For heavier doses, the devices are quite well-behaved and thus the total sensitivity is small. For thick films and lighter doses, the $\frac{\Delta V_T}{\Delta t_{si}}$ increases, because the devices are very sensitive to short-channel effects in this regime as was the case in the constant concentration as well. This data shows that although the parametric sensitivities in SOI are more prominent than in bulk devices, with proper engineering of the channel implant doses, the sensitivity can be reduced.

## 3.7 Summary and Conclusions

Short-channel effects in deep-submicrometer SOI devices have been examined using two-dimensional numerical simulations. To obtain improved short-channel performance in SOI over bulk technologies, the silicon film thickness must be smaller than the comparable bulk junction depth and far from the transition between full and partial depletion. Optimal design regions for nominal and short-channel threshold voltage exist for both fully and partially-depleted devices using mid-gap gate and conventional gate materials. However, in the 0.1 μm regime, very thin films are required to achieve well-designed, fully-depleted devices. The use of mid-gap workfunction gate material or accumulation-mode devices require even

thinner silicon film thicknesses. Partially-depleted devices are advantageous from the manufacturing standpoint to relax the constraints on silicon film thickness although the remaining issue of the floating body is still an important one. This issue will be examined in more detail experimentally in Chapter 7 where the tradeoffs between current drive and short-channel effects are explored.

Threshold voltage sensitivity in SOI devices was found to be composed of both one-dimensional (long-channel) and two-dimensional (short-channel) phenomena. Although the sensitivity is significant when constant concentrations are examined, it is expected that optimization of the implantation schedule will be able to reduce the sensitivity by using a "near-constant-dose" approach.

# Chapter 4

# Parasitic Series Resistance Issues

## 4.1 Introduction

As discussed in the previous section, to reduce short-channel effects in deep-submicrometer, fully-depleted SOI MOSFETs, ultra-thin silicon films ($t_{si}$ <70 nm) are needed. However, most of the results to date on ultra-thin films have exhibited high parasitic source/drain resistance, which tends to obscure the performance advantages of SOI [34,35].

One potential solution to this problem is the use of self-aligned silicides, i.e. salicides, to reduce the source/drain sheet resistance. However, even the use of conventional salicides does not guarantee good parasitic resistance because the limited silicon film complicates the silicidation process. Kistler et al. have reported very high parasitic series resistance in thin-film SOI MOSFETs using self-aligned $TiSi_2$, although the sheet resistivity measured on van der Pauw structures was low

[51]. It has also reported that using $TiSi_2$, an insulating layer or void may be formed in the region adjacent to a silicided silicon layer if non-optimum titanium thicknesses are used [52,53].

In this section, the parasitic series resistance in ultra-thin film SOI is studied through the use of 2-D numerical simulations and process experiments. The optimum silicide thickness from both a theoretical and fabrication standpoint are explored. A novel cobalt salicidation technique using titanium/cobalt laminates is used to demonstrate ultra-thin silicides with low parasitic series resistance in fully-depleted, thin-film SOI devices.

## 4.2 Simulations

Parasitic series resistance in MOSFETs is dependent on the source/drain structure. In SOI MOSFETs, this region is limited by the silicon film thickness, and as the film thickness is reduced, the sheet resistance increases proportionally. The use of salicides can reduce the sheet resistance of the source/drain regions. However, for ultra-thin film SOI, the salicide thickness will be on the same order as the film thickness itself, and thus the salicide geometry can influence the device series resistance. 2-D MEDICI [54] simulations were performed to examine the effects of silicon film thickness, contact resistivity and silicide depth on SOI device series resistance [55].

Figure 4-1 shows the structure used to simulate the source/drain of a SOI MOSFET. The doping concentration was uniform $n^+$, $1x10^{20}$ $cm^{-3}$ and the silicide region was treated as a perfect conductor. The gate-voltage dependent components of series resistance [56,57] were omitted to highlight the geometrical tradeoffs in the drain/silicide structure.

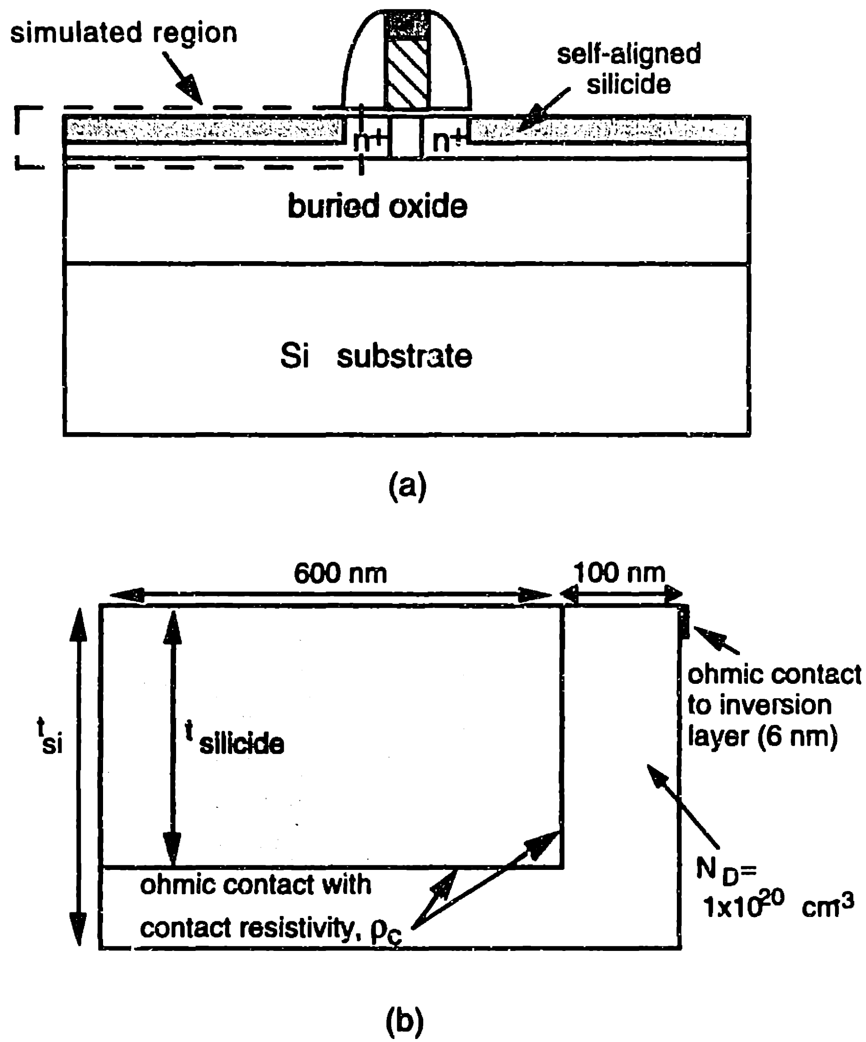


Figure 4-1: (a) Schematic cross-section of a SOI MOSFET with silicided source/drains; (b) simplified structure of an SOI MOSFET source/drain used in MEDICI simulations.

Figure 4-2 shows the resistance of the structure vs. silicide thickness for four different contact resistivities. As shown, the total resistance of the structure is nearly independent of the silicide thickness until the silicide becomes an appreciable portion of the total drain depth. As the silicide approaches full consumption of the silicon film, the resistance of the structure increases sharply. This sharp increase in the resistance is aggravated in the higher contact resistivity cases. For the lowest contact resistivity of $10^{-8}$ Ω-cm$^2$, the resistance is relatively flat over the entire range of thicknesses.

Physically, the increase in resistance is due to a reduction in contact area once the silicide fully consumes the silicon layer because the horizontal portion directly underneath the silicide is no longer available for contact. For the lowest contact resistivity, the decrease in contact area is not as important because current can flow unrestricted through the vertical portion of the contact. However, for the higher contact resistivities, the current through the vertical portion of the contact is restricted, thus explaining the large increase in resistance. This behavior is further highlighted by examining the current flow contours in Figs. 4-3 and 4-4. For $t_{silicide}$ = 40 nm (Fig. 4-3), the current flow in the structure is significant through both the vertical and horizontal portion of the two-dimensional contact region. However, when $t_{silicide}$ is increased to 48 nm (Fig. 4-4), the amount of current flow through the horizontal portion of the contact is severely reduced which leads to the increased resistance. This indicates that the horizontal portion of the contact is quite important for finite contact resistivities. The contact resistivity in typical self-aligned silicides in modern MOSFETs is $10^{-6}$-$10^{-7}$ Ω/cm$^2$ [58,59,60].

An examination of various silicon film thicknesses in Fig. 4-5 shows that a systematic trend can be observed in the resistance as a function of the fraction of silicon film thickness ($t_{silicide}/t_{si}$) consumed due to the effect of the silicide

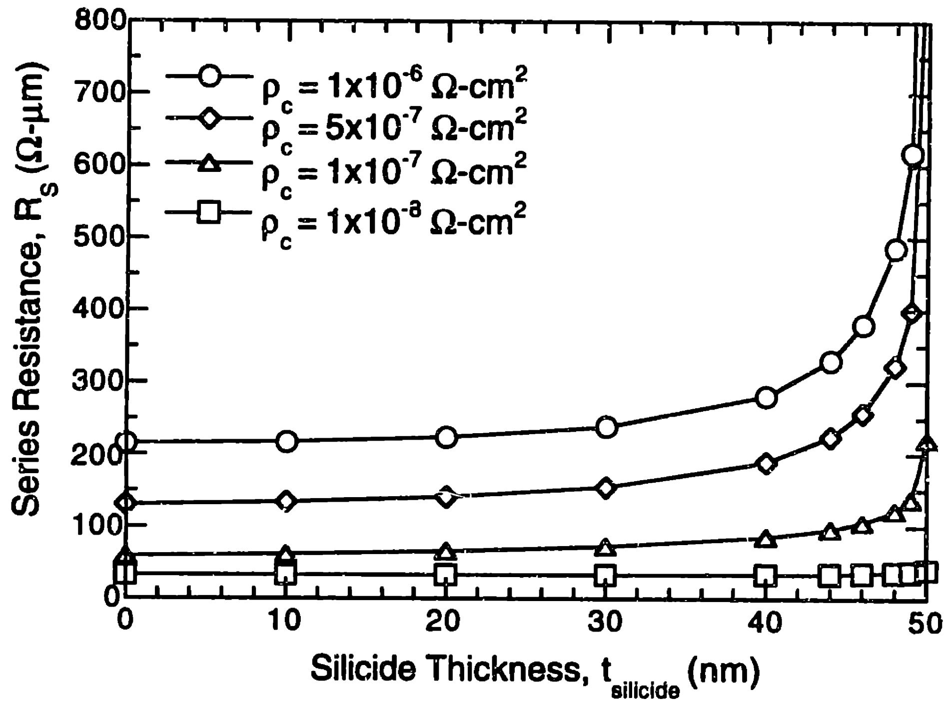


Figure 4-2: Simulated series resistance, $R_S$ as a function of silicide thickness for various contact resistivities between silicide and silicon, $\rho_C$. The silicon film thickness is 50 nm.

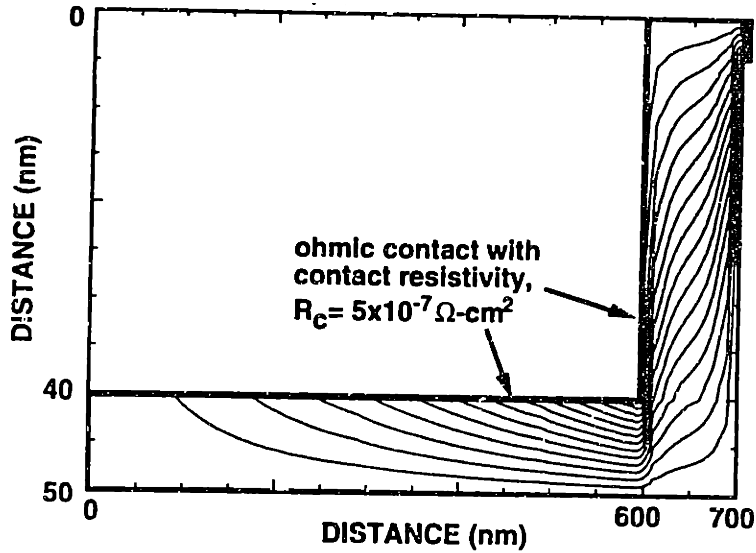


Figure 4-3: Simulated current flow contours for a silicide thickness of 40 nm and a $\rho_c$=1x10$^{-7}$ Ω-cm$^2$ (not drawn to scale). Note that significant amount of current flows through the horizontal portion of the contact.

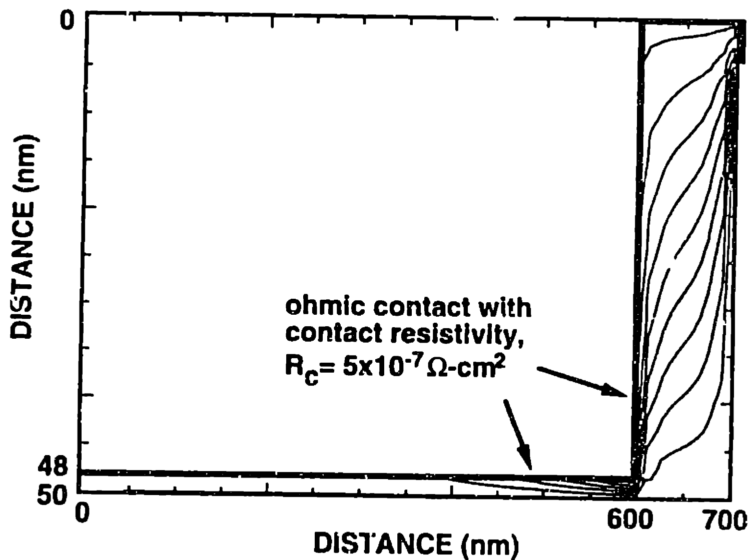


Figure 4-4: Simulated current flow contours for a silicide thickness of 48 nm and a $\rho_c$=1x10$^{-7}$ Ω-cm$^2$ (not drawn to scale). Constant contours are drawn with the same steps as Fig. 4-3. Note that current is being restricted from flowing in the horizontal portion of the contact as compared to Fig. 4-3 and the density of the current flow contours is significantly less.

geometry. The behavior for different film thicknesses is very similar to Fig. 4-2 in that for a given film thickness, the resistance is relatively flat over most of the $t_{silicide}/t_{si}$ range until the silicide thickness approaches full consumption of the silicon film. At that point, the resistance increases sharply for all three silicon film thicknesses.

For a given silicon film thickness, the optimum silicide thickness can be determined by choosing the thickest possible silicide to achieve the lowest sheet resistance without entering the high resistance region due to contact geometry effects. From these simulations, the optimum $t_{silicide}/t_{si}$ ratio is about 60-80% to operate in the flat region of the curves.

It should be noted that these simulations are simplified in that the finite resistance of the silicide layer is not taken into account. This is a reasonable approximation for most silicide thicknesses because the sheet resistance of the silicide (5-15 Ω/sq.) is significantly less than the sheet resistance of the $n^+$ silicon film (100-300 Ω/sq.) for typical silicon and silicide thicknesses. For ultra-thin silicides, $t_{silicide} < 5$ nm, the silicide sheet resistivity is no longer negligible so the simulations are not accurate in this region. Qualitatively, the resistance would increase as $t_{silicide}$ approaches zero because of the finite resistance of the silicide layer.

The case of zero silicide thickness in the simulations corresponds to a raised source/drain structure, e.g. selective CVD tungsten [61] where the resistivity of the metallic film can be very low although there is no consumption of the silicon film. This case can also provide good device series resistance as long as the contact resistivity between the raised source/drain and the doped region is reasonably low.

These simulation results were recently independently confirmed by Suzuki et al. [62] who derived an analytical formulation of the series resistance in SOI MOSFETs using a transmission line model.

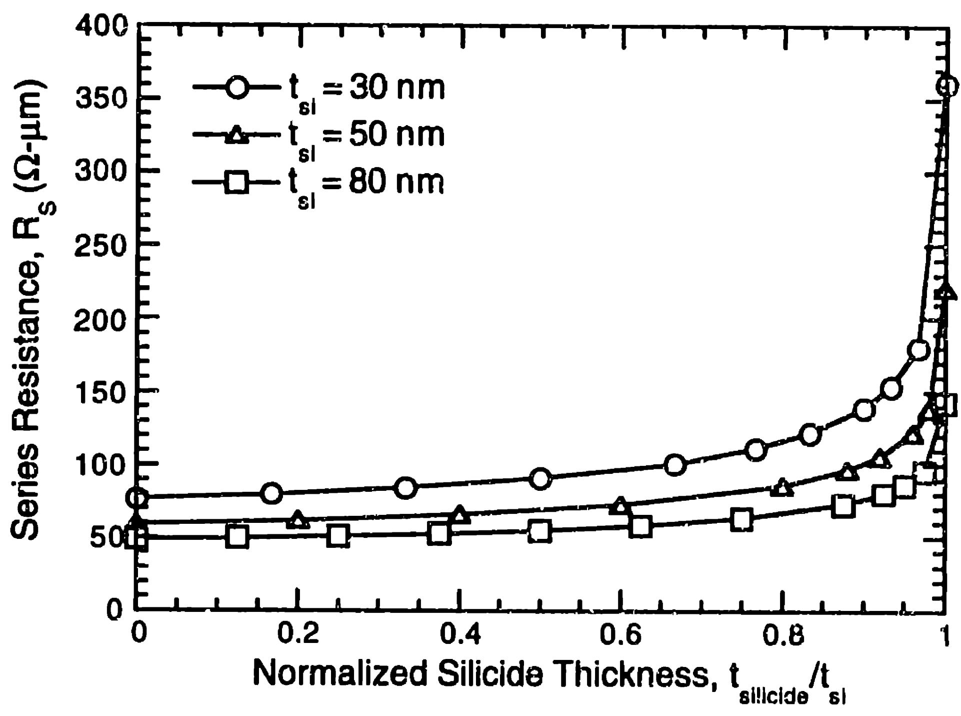


Figure 4-5: Simulated series resistance, $R_S$ as a function of the normalized silicide thickness for various silicon film thicknesses. The contact resistivity, $\rho_c$, between the silicide and silicon was $1x10^{-7}$ Ω-cm$^2$.

# 4.3 Silicide Process Experiments

## 4.3.1 Conventional Cobalt Disilicide

From a process standpoint, it is important to understand the effects of metal thickness and the amount of silicide formed, on the actual device series resistance. Previous work using $TiSi_2$ has shown that when the silicide fully consumes the silicon layer in thin-film SOI, the silicide layer exhibits a high sheet resistance because a metal-rich silicide is formed that is more prone to agglomeration [52].

Experiments were performed on both bulk and SIMOX SOI substrates to study the silicidation process. Both patterned and unpatterned substrates were used to measure the silicide sheet resistance and the silicide-to-$n^+$ contact resistance. The silicide and $n^+$ sheet resistance was measured using four-point resistance measurement on unpatterned substrates and van der Pauw structures on patterned substrates. The contact resistance was measured on line resistors adapted from Scott et al. [63]. The silicide was selectively masked in some areas with a low-temperature oxide. An arsenic implant dose of $4x10^{15}$ $cm^{-2}$, at an energy of 25 keV and a 15 s, 1000 °C RTA anneal were used to form the $n^+$ regions. The conventional $CoSi_2$ process consisted of a cobalt evaporation and a subsequent two-step RTA anneal process (1st step RTA: 30 s, 390 °C, 2nd step RTA: 60 s, 750 °C). Figure 4-6 shows the sheet resistance and $n^+$ to silicide contact resistance of $CoSi_2$ vs. silicon film thickness for a fixed cobalt thickness of 21 nm.

As shown, the resistance of the silicide is fairly constant for silicon film thicknesses greater than 80 nm. However, as the silicon film thickness is reduced, the resistance of the silicide increases dramatically. The same behavior is also observed for the silicide-to-$n^+$ contact resistance. The breakpoint between the high

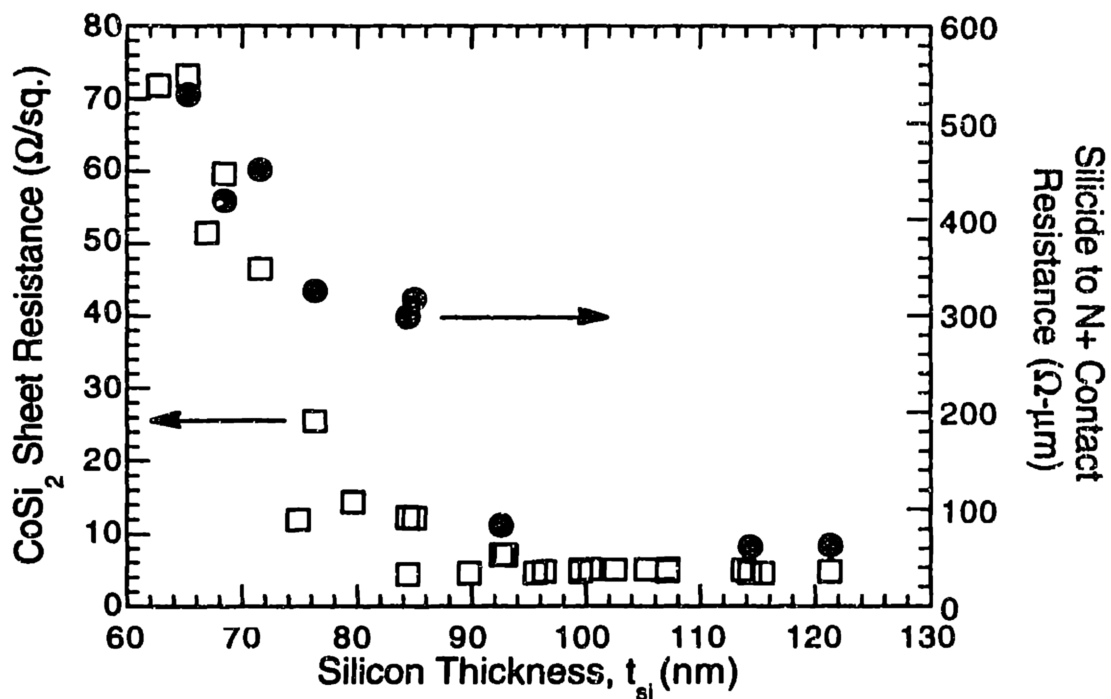


Figure 4-6: $CoSi_2$ sheet resistance and contact resistance vs. silicon film thickness for a silicided device. $CoSi_2$ was formed by 21 nm evaporation of cobalt and subsequent 2-step RTA anneal. Final silicide thickness was ~ 80 nm.

resistance region and the low resistance region corresponds approximately to the point at which the silicide fully consumes the silicon layer. The consumption of silicon in the $CoSi_2$ formation process is approximately 3.5-4 times the thickness of the metal [64]. In this case, the evaporated cobalt thickness was 21 nm which corresponds to approximately 80 nm of silicon consumption. For silicon films under 80 nm, the silicide reaction is silicon-starved and thus stoichiometric $CoSi_2$ can not be formed.

TEM analysis by Hsia et al. has indicated that conventional cobalt silicide films that fully consume the silicon layer result in CoSi instead of $CoSi_2$ [65]. This is consistent with our experimental results because CoSi usually has a higher resistance than $CoSi_2$ [66].

More recent work by Hsia et al. has shown that epitaxial $CoSi_2$ can be formed on a fully-consumed SOI film by using co-evaporation of cobalt and silicon to form a CoSi/Ti bimetallic laminate that is self-limiting [67]. However, this is still not desirable from a device standpoint because of the contact geometry effects discussed in the previous section.

### 4.3.2 Ti/Co Laminate for Cobalt Disilicide Formation

To avoid the formation of a metal-rich silicide and the contact geometry problems shown in the simulations, the silicide thickness in ultra-thin SOI devices should be less than the silicon film thickness. From the above simulations, for a target silicon film thickness in the range of 30-70 nm, the silicide thicknesses required are in the range of 20-50 nm. Silicides on the order of 20 nm are very difficult to achieve from a process standpoint for both bulk and SOI devices. For silicide thicknesses in this range, conventional $CoSi_2$ and $TiSi_2$ show signs of agglomeration even on bulk devices [68,69]. To avoid this problem, a novel $CoSi_2$

scheme using a titanium-cobalt (Ti/Co) bimetallic laminate was explored in this study. Using the Ti/Co laminate, the cobalt diffuses through the titanium layer to form stoichiometric $CoSi_2$. The primary function of the titanium in the reaction is two-fold. It serves as a getterer of oxygen to remove any native oxide on the wafer surface prior to the evaporation and it also slows down the silicide reaction so that a more uniform silicide is formed. A thin composite layer of Ti-Co-Si is formed at the surface which is removed later in the process. Previous work has demonstrated that a Ti/Co laminate achieves epitaxial $CoSi_2$ with excellent agglomeration-resistance [70,71]. However, no device results using this technology have been reported to date.

The primary concern of the Ti/Co laminate is gate-to-source/drain leakage due to bridging because the addition of Ti requires a higher reaction temperature. Bridging occurs when silicon from the source and drain diffuses onto the spacer to react with the evaporated metal at elevated temperatures. When this occurs, an electrical "bridge" or leakage path between the gate and source/drain is formed. Most of the literature to date has advocated the use of a one-step, relatively high temperature RTA anneal to form epitaxial $CoSi_2$. However, these experiments were all on unpatterned substrates. Anneal conditions were varied to obtain low $CoSi_2$ sheet resistance with minimal gate-to-source/drain leakage due to bridging. Tables 4-1 and 4-2 show the results of the process experiments.

A common diagnostic to assess the quality of a thin silicide layer is to measure the sheet resistance on both un-doped and heavily-doped material as a function of silicide anneal temperature. It has been shown that heavily-doped material has a tendency to impede the silicide reaction and degrade the silicide quality more so than silicides formed on un-doped silicon. In this experiment, blanket bulk and SOI monitors were used to form $CoSi_2$ by the conventional Co and

Ti/Co processes. The implant conditions for the $n^+$ doped material were arsenic, dose of $4 \times 10^{15}$ $cm^{-2}$, energy of 25 keV. The thermal cycle for these wafers was an RTA anneal of 1000 °C, 15-20 s.

For $CoSi_2$ formed by the conventional process, low sheet resistances were obtained on both un-doped and $n^+$ doped material with a cobalt thickness of 21 nm. However, when the thickness of the cobalt was scaled to 12 nm, which is necessary to form ultra-thin silicides in SOI, there was a large differential between the sheet resistance on un-doped and $n^+$ doped material. In addition, the final sheet resistance of the silicided $n^+$ doped material was a strong function of the silicide anneal condition. These are clear indications of a poor quality silicide that is likely agglomerated.

For the Ti/Co bimetallic laminate, the sheet resistance of the $CoSi_2$ is stable on both un-doped, $n^+$ and $p^+$ material [72] over a large range of RTA anneal conditions for cobalt thicknesses as thin as 8 nm. It should be noted that the sheet resistance of the silicide is somewhat high for the thinner cobalt films because the silicide is thin not because of any agglomeration problems.

Given the thermal stability of the Ti/Co films demonstrated above, the only remaining issue is the gate-to-source/drain leakage due to bridging. Experiments were conducted on patterned polysilicon samples to optimize the RTA anneal conditions to reduce leakage. A gate stack consisting of 5.5 nm gate oxide, 300 nm polysilicon was deposited, patterned, and implanted with arsenic, dose of $4 \times 10^{15}$ $cm^{-2}$, energy of 25 keV. Then a 15 nm LTO and 70 nm nitride spacer was deposited and etched; and 3 nm Ti/10 nm cobalt was evaporated. Various RTA conditions were used to complete the formation of $CoSi_2$. As shown in Table 4-2, using a one-step high temperature RTA anneal as advocated in the literature results in significant gate-to-source/drain leakage using the Ti/Co process. This leakage

Table 4-1: Silicide process experiments.

Conventional $CoSi_2$

| Cobalt Thickness | RTA Conditions | Sheet R (undoped) | Sheet R ($n^+$ doped) |
|---|---|---|---|
| 21 nm | 390 °C, 30 s<br>+ 750 °C, 60 s | 5.5 Ω/sq. | 5.5 Ω/sq. |
| 12 nm | 390 °C, 30 s<br>+ 650 °C, 60 s<br>+ 750 °C, 60 s | 10 Ω/sq.<br>10 Ω/sq.<br>10 Ω/sq. | 23.5 Ω/sq.<br>31.1 Ω/sq.<br>81.5 Ω/sq. |

$CoSi_2$ by Ti/Co laminate

| Ti/Co Thickness | RTA Conditions | Sheet R (undoped) | Sheet R ($n^+$ doped) |
|---|---|---|---|
| 5 nm/14 nm | 850 °C, 60 s | 6.7 Ω/sq | 6.8 Ω/sq |
| 5 nm/10 nm | 800-850 °C, 60 s | 12-14 Ω/sq | 12-14 Ω/sq |
| 5 nm/8 nm | 600-800 °C, 60 s | 14-16 Ω/sq | 14-16 Ω/sq |

Table 4-2: Gate-to-source/drain leakage experiments.

| Ti/Co Thickness | RTA Conditions | Leakage Current @ $V_{GD}$=3 V |
|---|---|---|
| 5 nm/10 nm | 850 °C, 60 s | ~ 50 pA/µm |
| | 750 °C, 60 s | ~ 1 pA/µm |
| | 650 °C, 60 s | ~ 1 pA/µm |
| | 550 °C, 30 s<br>+ 700 °C, 60 s | < 50 fA/µm |
| 15 nm (Co only) | 390 °C, 30 s<br>+ 750 °C, 60 s | < 50 fA/µm |

probably originates from some diffusion of the silicon onto the spacer during the silicide reaction. By reducing the temperature of the first step anneal, the leakage can be reduced to some extent, however even at 650 °C, there is a non-negligible leakage current.

A two-step RTA anneal improves the gate-to-source/drain leakage considerably. The two-step RTA anneal for the Ti/Co process is similar to the conventional Co process but utilizes a higher first step reaction temperature because of the addition of Ti. A two-step reaction is beneficial compared to the one-step process because the unreacted metal is stripped after a relatively low temperature first-step anneal. Thus, the likelihood of gate-to-source/drain leakage is reduced. The resulting leakage current from the two-step process is less than 50 fA/µm and is quite suitable for device fabrication.

## 4.4 Device Integration Results

### 4.4.1 Device Fabrication Process

Using the results of the simulation and process experiments, deep-submicrometer, non-LDD SOI NMOS devices were fabricated down to $L_{eff}$=0.12 µm. All SOI devices were fabricated on commercially-available SIMOX material obtained from IBIS Corp. The key device parameters were silicon thickness of 60-70 nm, gate oxide thickness of 6.5-9 nm, and buried oxide thickness of 360 nm. Deep-submicrometer gate lengths were obtained by optical lithography with over-exposure at the gate level. Polysilicon gates were defined using a $CCl_4$ plasma etch. After an arsenic source/drain implant dose of $4x10^{15}$ $cm^{-2}$ at 25 keV, either a 900 °C, 30 minute furnace or a 1000 °C, 20-35 s RTA anneal was performed. The spacer

was formed by a low-temperature oxide/nitride stack of 15 nm LTO and 50-70 nm nitride. The Ti/Co layers were 3.5 nm Ti/8 nm Co using the two-step RTA process outlined above (1st step RTA: 550 °C, 30 s; 2nd step RTA: 700 °C, 60 s). The unreacted metal was stripped after the first step RTA using a 2 minute 4:1 $H_2SO_4$:$H_2O_2$ solution. 400 nm LTO was deposited as an interlevel dielectric. Contact hole etch was performed using a plasma etch in $CF_4/CCl_3$ for 90% of the interlevel dielectric thickness, and the remaining LTO was removed with a short dip in buffered oxide etch (BOE). Conventional 1 μm Al/1% Si was deposited, patterned and sintered in forming gas to complete the device fabrication. Appendix A contains a full process traveller with detailed recipes for the device fabrication. The final silicide sheet resistance was 14 Ω/sq. measured on van der Pauw structures.

### 4.4.2 Materials Analysis

Cross-sectional transmission electron micrographs (TEM) of the finished bulk and SOI devices were performed by T. S. Sriram at Digital Equipment Corporation. Approximately 12 transistors in bulk and SOI of varying gate lengths from 0.25 μm-1.5 μm were examined. Figure 4-7 shows a cross-sectional image of a SOI device and Fig. 4-8 shows a cross-sectional image of a bulk device. The active areas, spacer and polysilicon gate are defined in the micrograph. As shown, the $CoSi_2$ using the Ti/Co laminate is continuous and has a relatively uniform thickness. The LTO/nitride spacer is thin (~ 40 nm) but very well defined. There is no evidence of lateral overgrowth of the silicide onto the spacer. This indicates that the optimization of the RTA conditions was able to successfully suppress lateral overgrowth.

The thickness of the silicon film for the device in Fig. 4-7 is about 70-80 nm. This is about 10 nm higher than the thickness that is measured electrically using

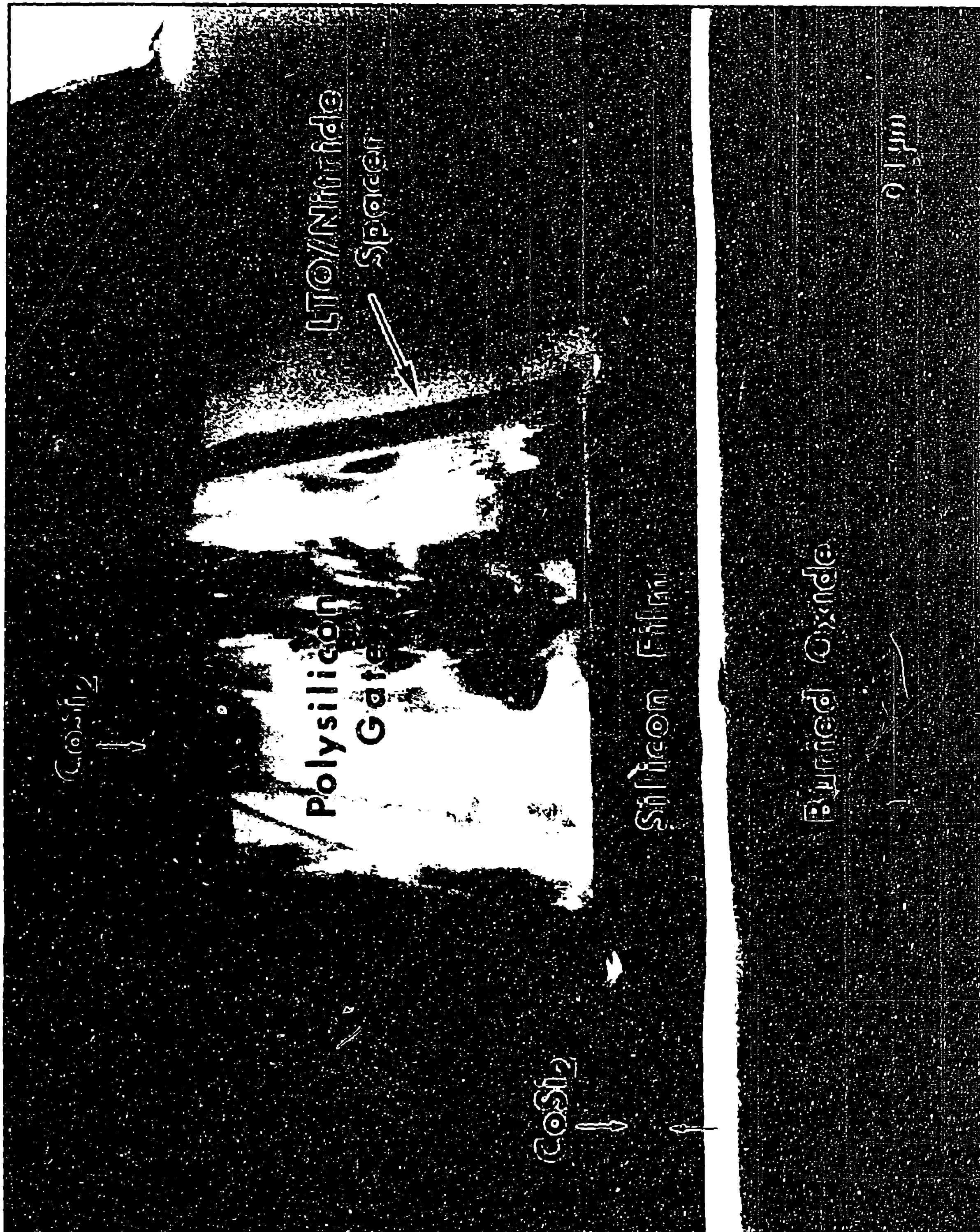


Figure 4-7: Transmission electron micrograph of SOI device fabricated with self-aligned $CoSi_2$ formed by Ti/Co laminates, magnification of 270,000 X.

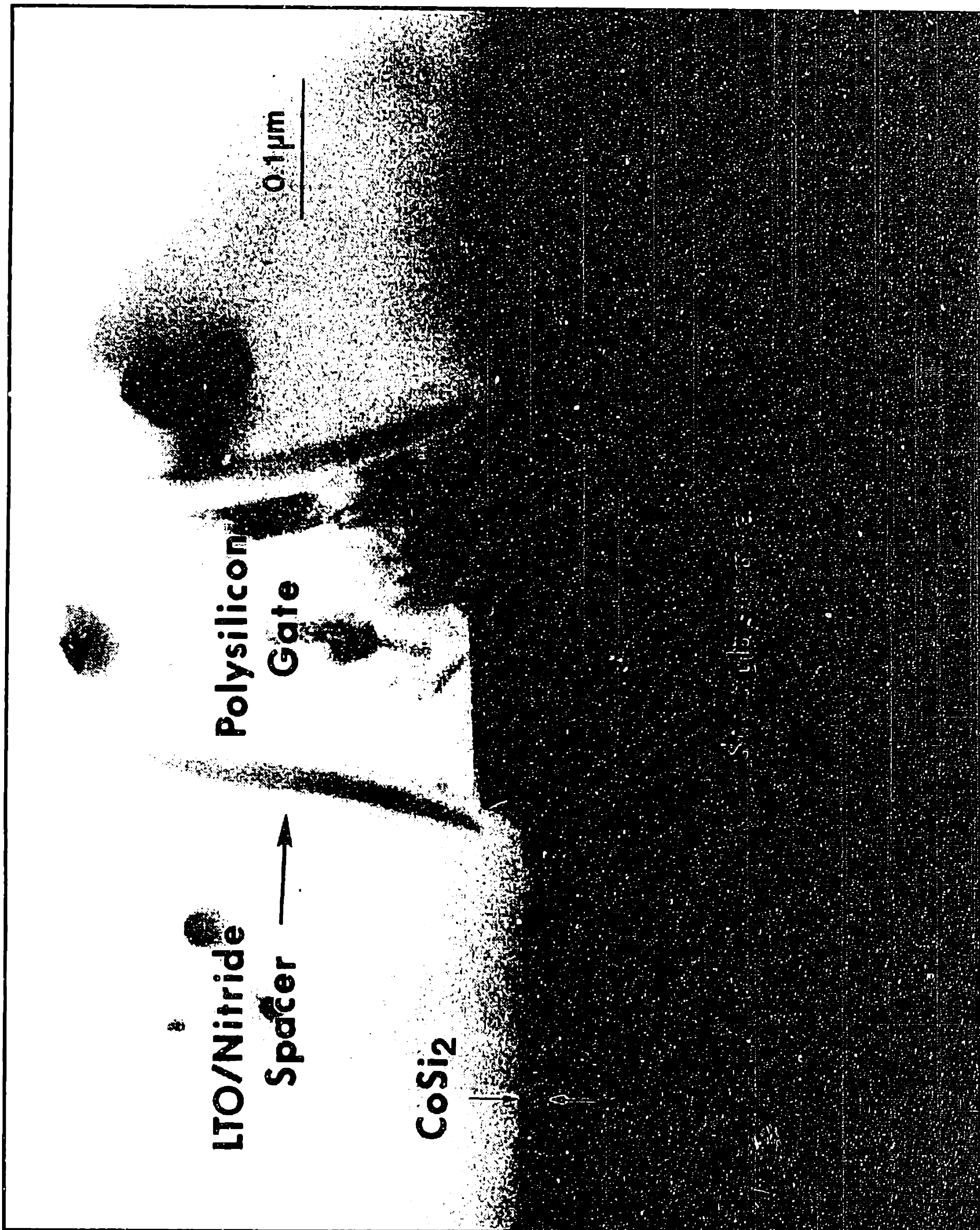


Figure 4-8: Transmission electron micrograph of a bulk device fabricated with self-aligned $CoSi_2$ formed by Ti/Co laminates, magnification of 270,000 X.

the capacitance technique but may be due to variation in silicon film across the wafer or an inherent offset in the capacitance measurement technique itself [73]. The silicon in the source/drain is significantly thinner than the active channel area in both the bulk and SOI device. This is due to significant over-etching during the polysilicon gate etching step. Although the plasma process was optimized to reduce the amount of overetch into the silicon, the selectivity of the $CCl_4$ plasma etch was about 5:1 Si to $SiO_2$ which was not sufficient for thin gate oxides. Subsequent runs utilized an improved polysilicon etch process using a pure $Cl_2$ plasma etch [74].

Even with the overetch of the silicon in the source/drain area, the silicide formation was not impeded. Figures 4-9 and 4-10 show high resolution TEM images of the Si/$CoSi_2$ interface from the SOI and bulk samples, respectively. The majority of the grains are not epitaxial although there are some epitaxial grains. This is probably due to the fact that the reaction temperature of the process used here is significantly lower than that used by others who have reported epitaxial films [70,71]. The silicide thickness is 10-25 nm for both bulk and SOI in most regions. The interface roughness is of the order of 10-15 nm.

At the edge of the active area and field oxide, there is a thickening of the silicide in both bulk and SOI devices and a void formed at the edge of the bird's beak. Figures 4-11 and 4-12 show examples of this on a SOI and bulk device respectively. One possible explanation is that excess metal at the field oxide step would have a tendency to form a silicide if there is any silicon available. During the first step RTA anneal, silicon is known to be the diffusing species, thus silicon diffuses from the edge of the bird's beak. This results in the formation of a void at the bird's beak edge and a hillock on the field oxide. There is no evidence of the voiding or thicker silicide growth at the spacer edge in any of the samples that were examined. This could be due to a beneficial effect of poor step coverage of the

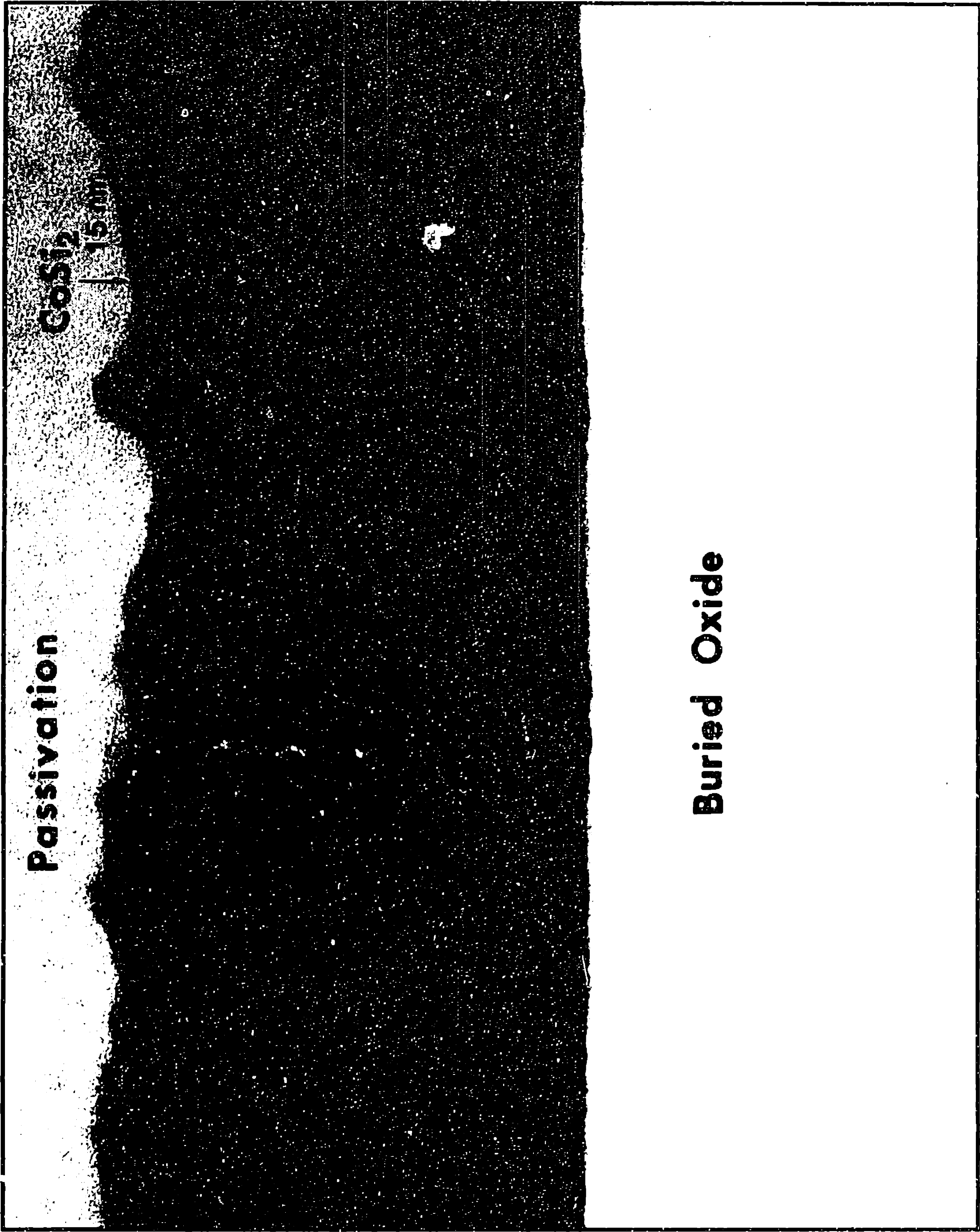


Figure 4-9: High-resolution transmission electron micrograph of a self-aligned $CoSi_2$ formed by Ti/Co laminates from a SOI device, magnification of 1,600,000 X.

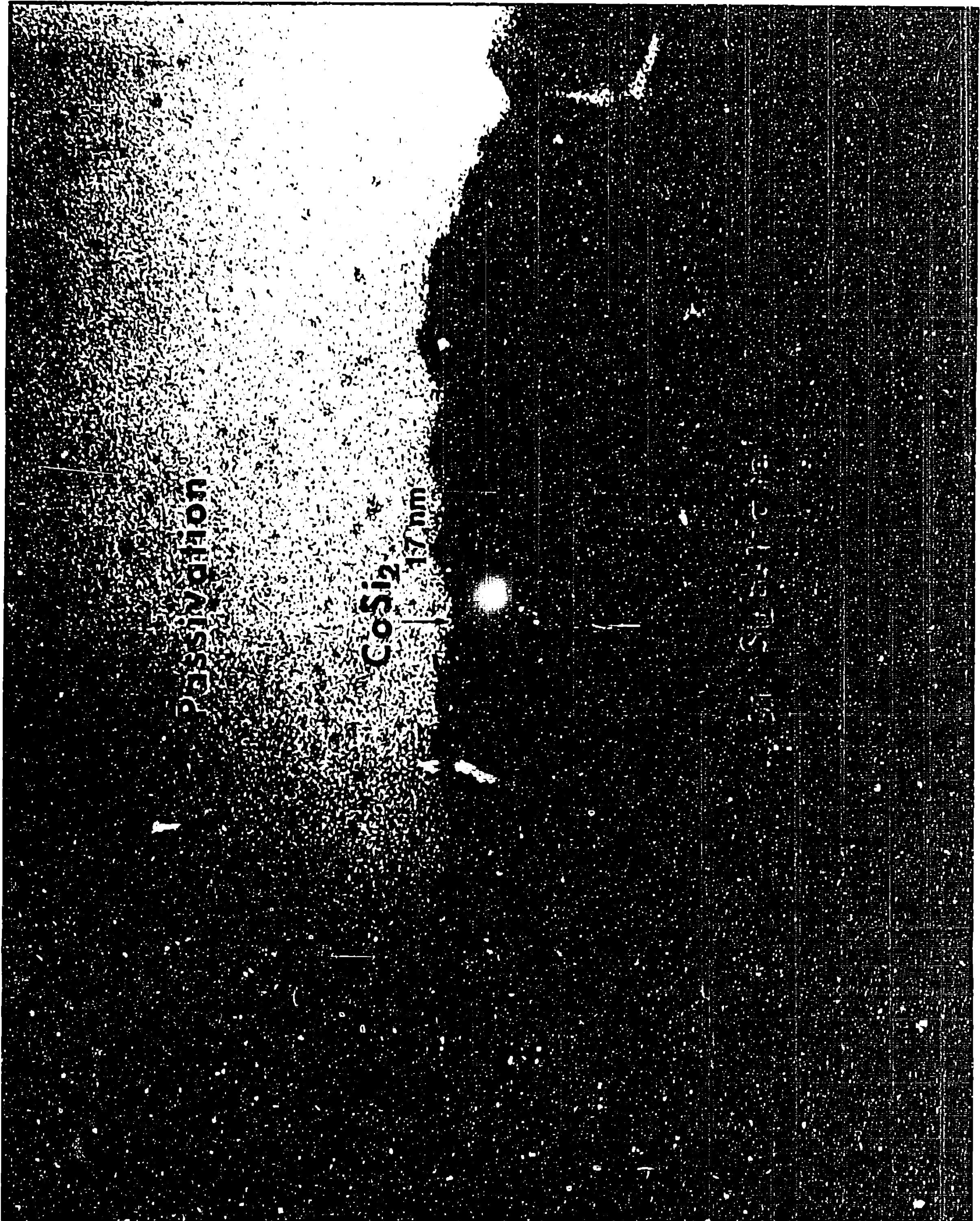


Figure 4-10: High-resolution transmission electron micrograph of a self-aligned $CoSi_2$ formed by Ti/Co laminate from a bulk device, magnification of 1,400,000 X.

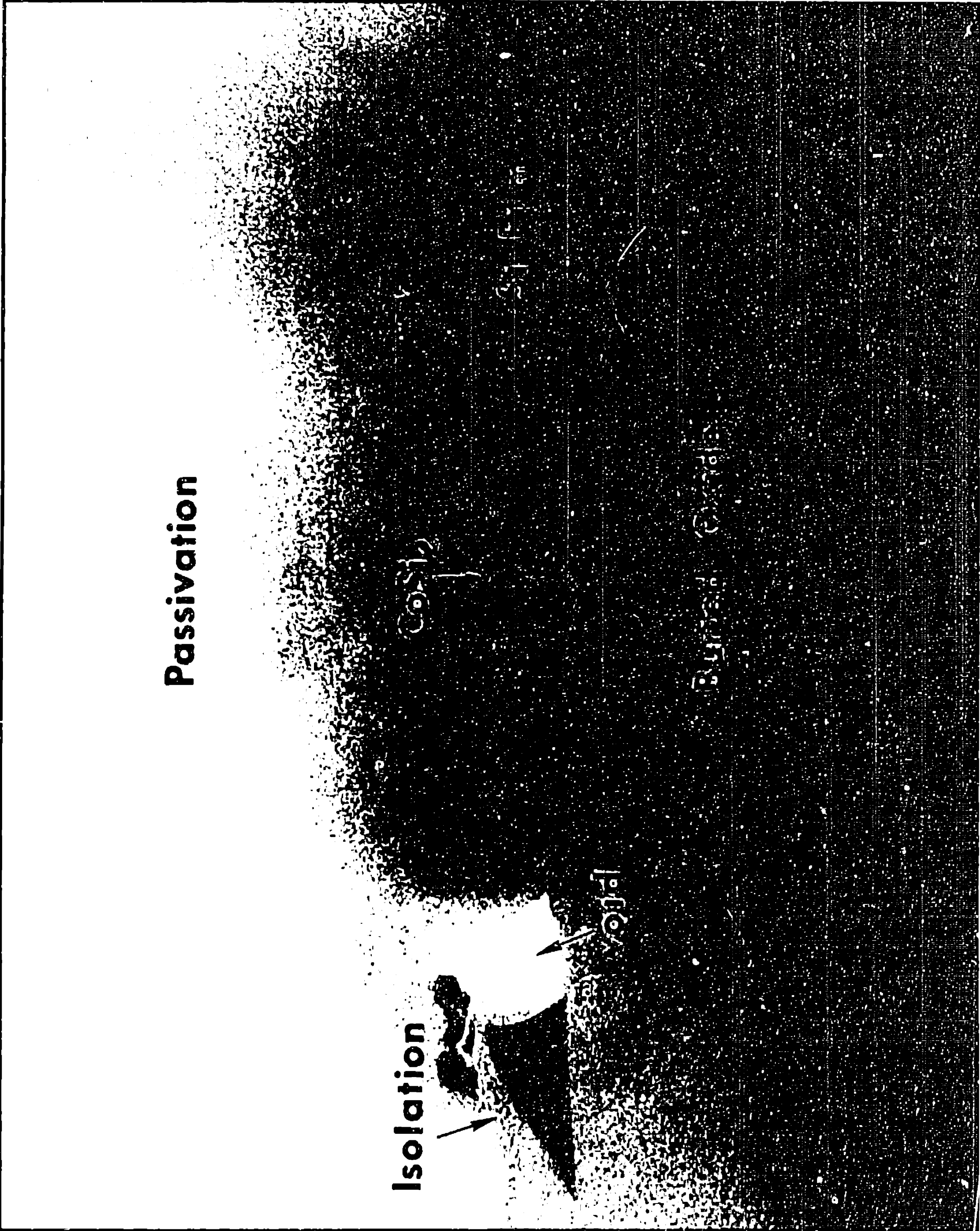


Figure 4-11: Transmission electron micrograph of an active area/field oxide edge from a SOI device showing the thickening of the $CoSi_2$ near the field oxide edge and the subsequent void formation, magnification of 270,000 X.

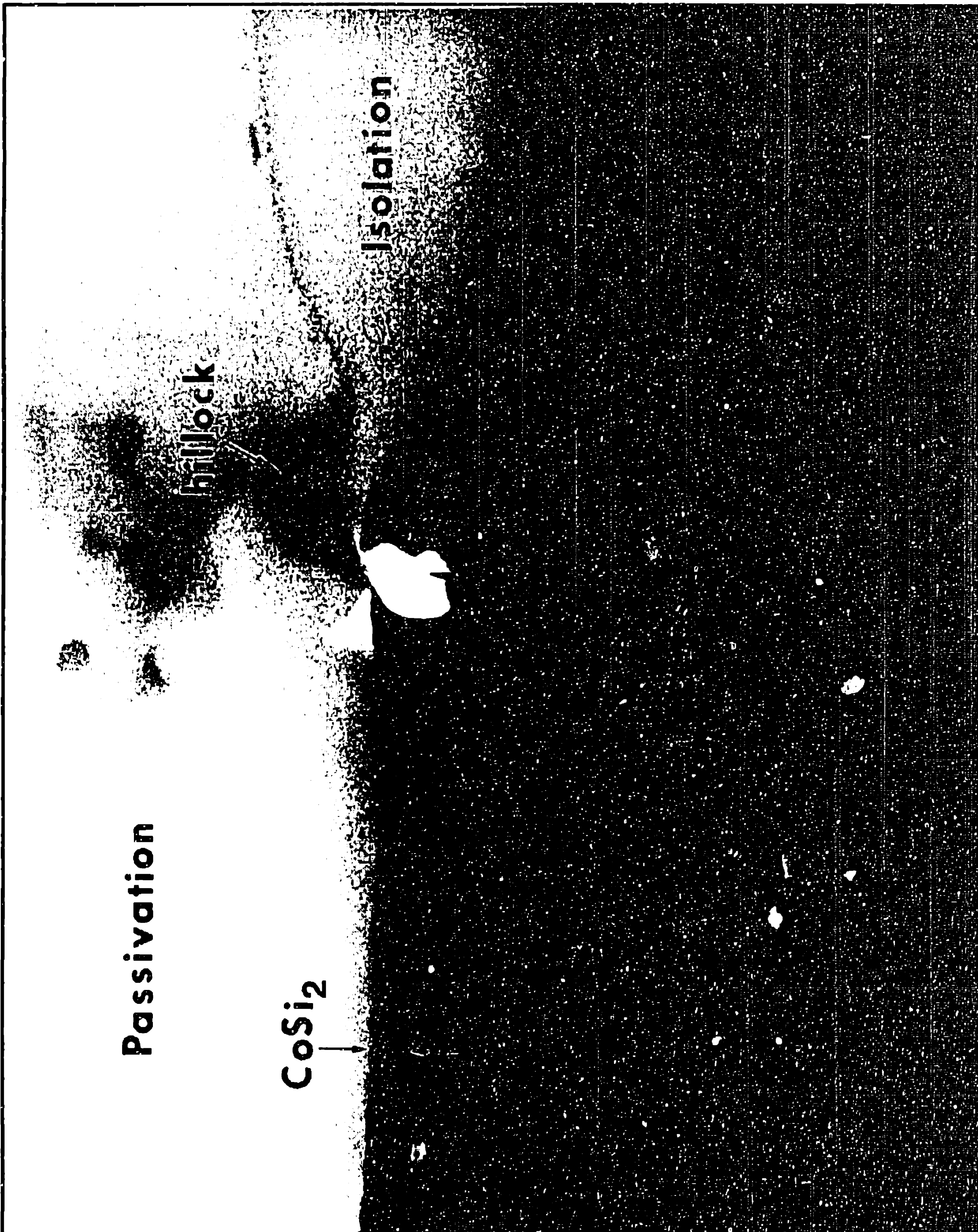


Figure 4-12: Transmission electron micrograph of an active area/field oxide edge from a bulk device showing the thickening of the $CoSi_2$ near the field oxide edge and the subsequent void formation. Magnification of 270,000 X.

evaporated metal at the spacer edge. The void formation and the thicker silicide did not affect the electrical characteristics of the measured devices that are discussed in the next section. However, in bulk devices this would likely lead to increased perimeter leakage currents particularly on edge-intensive devices. Thus, a better understanding of this phenomenon is clearly necessary.

### 4.4.3 Electrical Characteristics

Excellent device characteristics with low parasitic series resistances were obtained in SOI devices with $t_{si}$ = 60 nm as shown in Fig. 4-13. Parasitic resistances and effective channel lengths were extracted using the technique described in [43,44]. For the devices fabricated using a furnace anneal for the source/drain activation, the silicided and non-silicided device parasitic resistances, $R_{SD}$, were 550 Ω-µm and 1100 Ω-µm respectively. No gate-to-source/drain bridging was observed as demonstrated by the low subthreshold leakage for $L_{eff}$ = 0.17 µm shown in Fig. 4-14. It should be noted that the threshold voltage of this device is about 0.1 V for $L_{eff}$=0.17 µm because of the low channel doping concentration. These data are presented here to obtain the highest mobility and drive current. A large range of devices were fabricated with various channel doping concentrations and will be explored further in the subsequent chapters.

Further optimization of the process by using a relatively long RTA anneal (1000 °C, 35 s) resulted in device $R_{SD}$'s of 250-300 Ω-µm as shown in Fig. 4-15. Note that there is no limitation of the drain current by the parasitic series resistance as the $L_{eff}$ is reduced from 0.17 µm to 0.12 µm. These are believed to be the lowest reported $R_{SD}$ values for SOI devices with $t_{si}$ of 60-70 nm and are comparable to the best $R_{SD}$ results obtained in bulk devices. The relatively long RTA anneal is helpful in both silicided and unsilicided devices to fully activate the dopants in the source,

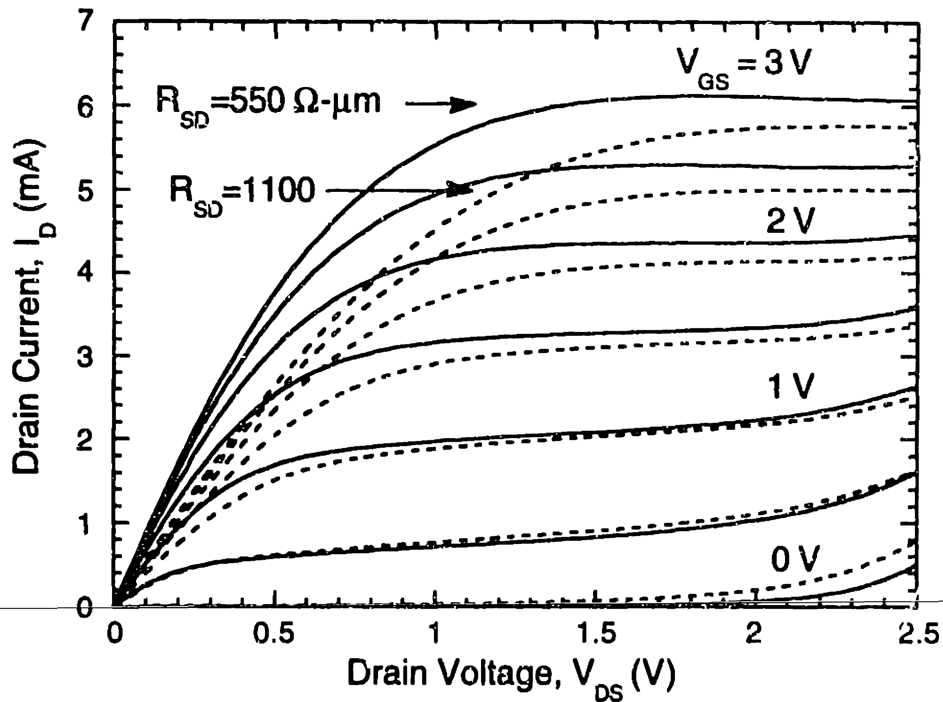


Figure 4-13: Drain current characteristics for a silicided and unsilicided device with $W_{eff}$=8.5 μm, $L_{eff}$=0.17 μm, $t_{si}$=60 nm, $N_a$=1.5x10$^{17}$ cm$^{-3}$, and $t_{ox}$=6.5 nm. The silicided and unsilicided $R_{SD}$'s are 550 Ω-μm and 1100 Ω-μm respectively.

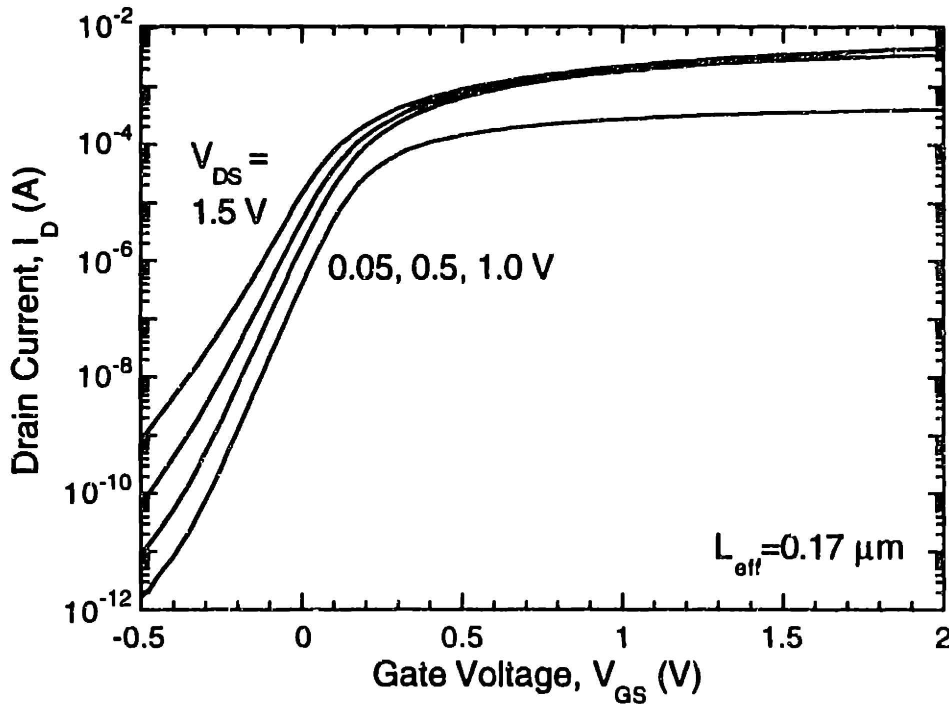


Figure 4-14: Subthreshold characteristics for a silicided device with $W_{eff}$=8.5 μm, $L_{eff}$=0.17 μm, $t_{si}$=60 nm, $N_a$=1.5x10$^{17}$ cm$^{-3}$, and $t_{ox}$=6.5 nm.

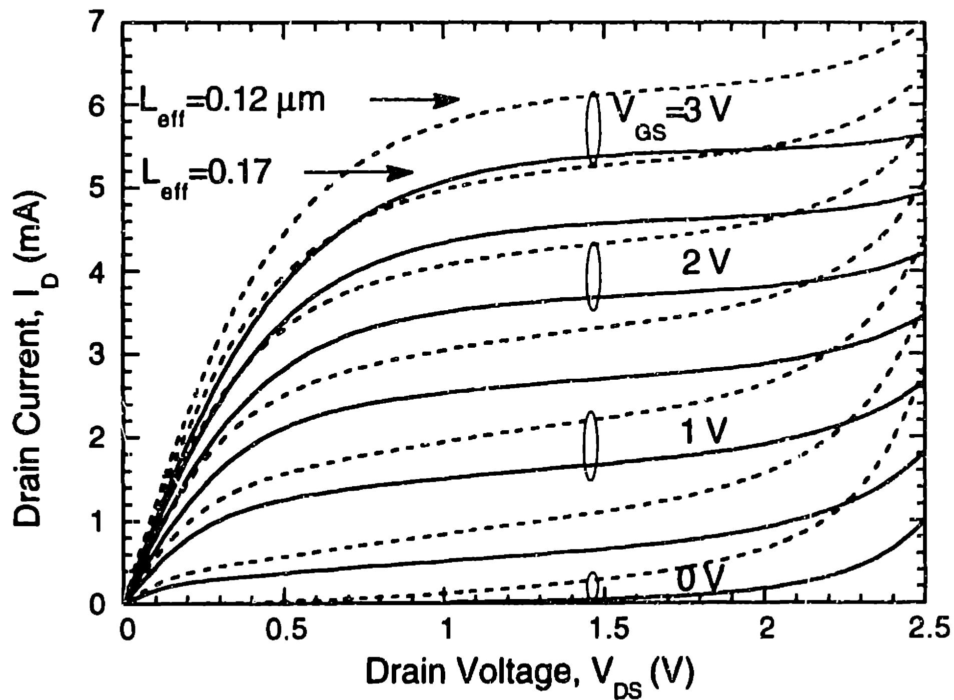


Figure 4-15: Drain current characteristics for silicided devices using RTA source/drain anneal. Extracted $R_{SD}$ is 250-300 Ω-μm. Device parameters are $W_{eff}$=8.5 μm, $L_{eff}$=0.17 and 0.12 μm, $t_{si}$=60 nm, $N_a$=1.5x10$^{17}$ cm$^{-3}$, $t_{ox}$=9 nm.

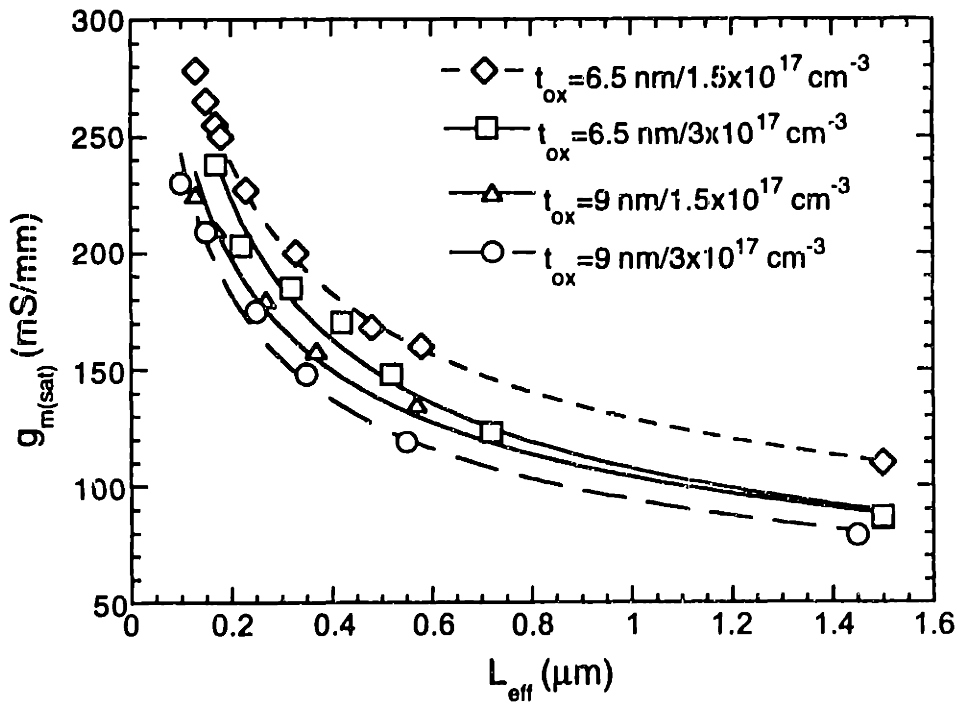


Figure 4-16: Measured peak saturated transconductance at $V_{DS}$=1 V vs. $L_{eff}$ for silicided devices with two different channel dopings and gate oxide thicknesses.

drain and gate and to recrystallize the silicon film after the heavy source/drain implant. The requirements on the thermal budget in SOI processes are not as stringent as in bulk processes because the junction depth is self-determined by the thickness of the silicon film, thus the longer RTA anneal is permissible. The primary constraints on the thermal budget for SOI MOSFETs is the suppression of boron penetration in the channel of PMOS devices and the control of the source/drain overlap capacitances. The boron penetration issue is significant even in conventional bulk processes and may require the use of nitrided gate dielectrics for deep-submicron MOSFETs [75]. The control of the source/drain overlap capacitance can be accomplished by implanting the heavy source/drain implant after a thin spacer [76].

The measured peak transconductance in the saturation region, $g_{m(sat)}$, at $V_D$=1 V is shown in Fig. 4-16. As expected, the higher doping concentrations have a lower transconductance due to a lower channel mobility. The $g_{m(sat)}$'s correspond to average carrier velocities ($g_m / WC_{ox}$) of 5-6x$10^6$ cm/s for the shortest devices. These values are comparable to what can be expected in bulk devices especially since all SOI devices exhibit device self-heating under static, steady-state bias conditions which tends to reduce the measured $g_m$ and $I_{dsat}$'s which is discussed further in Chapter 5.

# 4.5 Discussion

## 4.5.1 Comparison of Experimental Results to Simulations

Given the electrical results in the previous section, it is useful to compare with the original simulations. Shown in Fig. 4-17 is a comparison of the total series

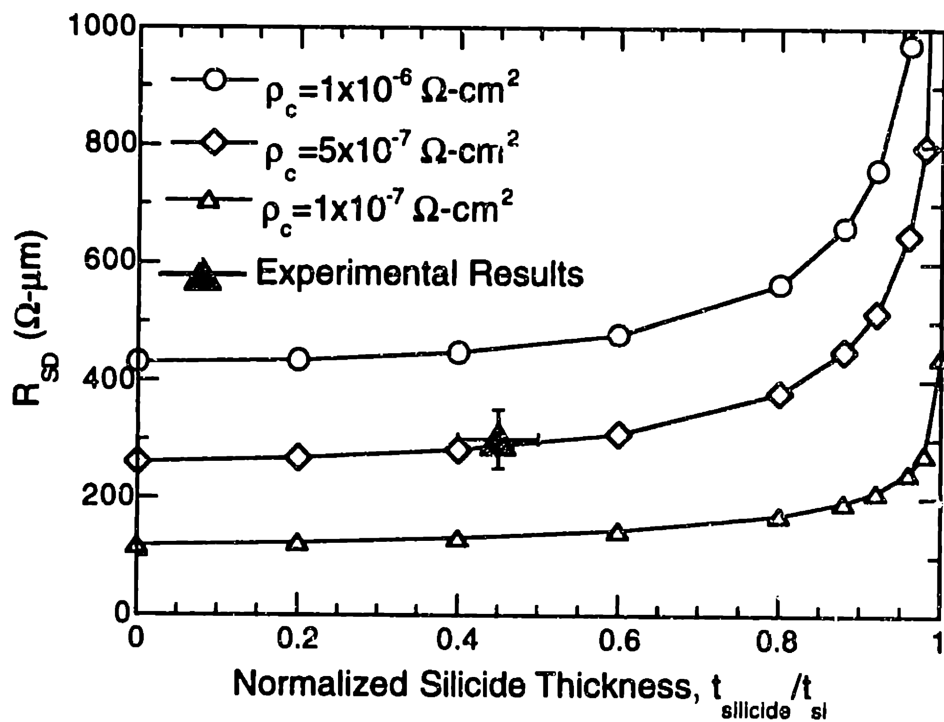


Figure 4-17: Simulated total series resistance, $R_{SD}$ vs. fraction of silicon film thickness consumed for three different contact resistivities compared to the experimental results.

resistance, $R_{SD}$, as predicted from simulations for three different contact resistivities, as well as the achieved experimental results. For the silicide geometry in the experiments, the results correspond very well to a contact resistivity of about $5 \times 10^{-7}$ Ω-cm$^2$. This value is quite reasonable for the contact resistivity from silicide to $n^+$ silicon and indicates that the simulations were useful in providing guidance for the design of the contact geometry. It should be noted that because the simulations do not take into account the gate-voltage dependent component of series resistance, the $5 \times 10^{-7}$ Ω-cm$^2$ estimate of contact resistivity is the worst-case, with the actual contact resistivity likely being slightly lower. For our device runs, there was no independent measure of contact resistivity from silicide to silicon because an extra masking layer is necessary to measure contact resistivity in self-aligned silicide processes.

### 4.5.2 Resistance Components of $R_{SD}$ in MOSFETs

To understand the potential of self-aligned silicides in improving parasitic series resistance, it is important to analyze the components of the series resistance. Ng and Lynch's simulation study showed that the series resistance can be divided into four components as indicated in Fig. 4-18, namely the accumulation resistance, $R_{ac}$; spreading resistance, $R_{sp}$; the component due to the source/drain sheet resistance, $R_{sh}$; and contact resistance, $R_{co}$ [77]. The main benefit of self-aligned silicides is to reduce the $R_{sh}$ and $R_{co}$ component. The $R_{sh}$ component is reduced because the value of the silicide sheet resistance is typically much lower than heavily-doped $n^+$ or $p^+$. The $R_{co}$ component is reduced because the length of the contact area is increased to include the entire source and drain region with the exception of the spacer width. The actual reduction in each component depends heavily on the layout geometry.

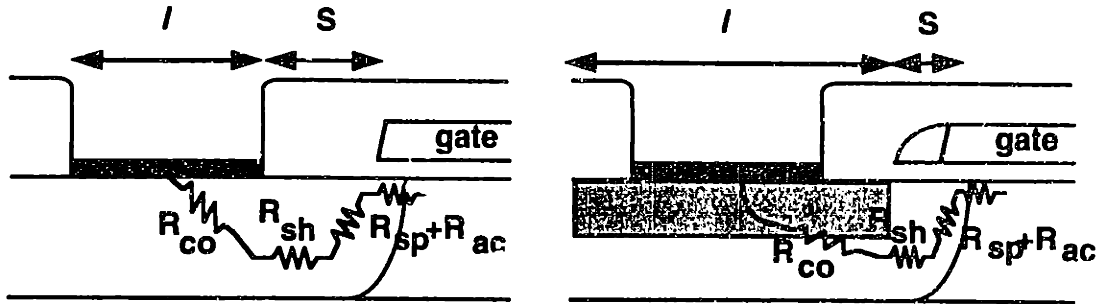


Figure 4-18: Schematic diagram of four components of parasitic series resistance for an unsilicided and silicided source/drain geometry (from Ng and Lynch [77]).

In the experimental results in this study, it was found that in comparing the silicided and unsilicided devices, the extracted $R_{SD}$'s were 550 Ω-μm and 1100 Ω-μm respectively. The difference of 550 Ω-μm can be mostly attributed to a reduction in the $R_{sh}$ component of the series resistance. The contribution of the component due to the sheet resistance, can be calculated by:

$$R_{sh} = \frac{\rho_{sh} S}{W} \tag{4.1}$$

where $\rho_{sh}$ is the sheet resistance of the $n^+$ layer, $S$ is the distance from the polysilicon gate to the contact hole edge, and $W$ is the width of the device. For the experimental devices, $\rho_{sh(unsilicided)}$ is approximately 170 Ω/sq., $S_{unsilicided}$ is 1.5 μm, and $W$ is 1 μm to normalize the width component. The $\rho_{sh(silicided)}$ is approximately 15 Ω/sq. and $S_{silicided}$ corresponds to the spacer width which is typically 0.1 μm. Thus, including both the source and drain sides, the difference in sheet resistance between silicided and unsilicided devices can be calculated by:

$$\Delta R_{sh} = 2[\rho_{sh(unsilicided)} - \rho_{sh(silicided)}](S_{unsilicided} - S_{silicided}) \tag{4.2}$$

$$= 2\,(170\ \Omega/\text{sq.} - 15\ \Omega/\text{sq.})\,(1.5\ \mu\text{m} - 0.1\ \mu\text{m}) = 434\ \Omega\text{-}\mu\text{m}$$

Thus, most of the 550 Ω-µm difference measured in experiments can be attributed to the $\Delta R_{sh}$ calculated above as we would expect.

For this layout geometry, the $R_{co}$ component is not significantly reduced. Theoretically, $R_{co}$ can be derived from a transmission line analysis:

$$R_{co} = \frac{\sqrt{\rho_{sh}\rho_c}}{W} \coth\left(l\sqrt{\frac{\rho_{sh}}{\rho_c}}\right) \tag{4.3}$$

where $l$ is the length of the contact region, $\rho_c$ is the contact resistivity, and $\rho_{sh}$ is the unsilicided sheet resistance. This formula assumes that the sheet resistance of the silicided region is zero. For small $l$, $R_{co}$ approaches $R_{co} \approx \frac{\rho_c}{Wl}$ because coth $x \approx 1/x$ for small $x$. For large $l$, $R_{co}$ approaches $R_{co} \approx \frac{\sqrt{\rho_{sh}\rho_c}}{W}$ because coth $x \approx 1$ for large $x$. Physically, this can be understood because for small contact lengths, an increase in $l$ increases the amount of area available for contact. However, above a certain contact length, $R_{co}$ saturates to a minimum value and a further increase in $l$ does not improve the resistance. Using this insight, a contact transfer length, $l_c = \sqrt{\frac{\rho_c}{\rho_{sh}}}$ can be defined as the breakpoint between small and large $l$.

In the devices that were fabricated, $l$ is 4 µm, while the typical contact transfer length for our technology is $l_c \approx 0.5$ µm. Hence, $l >> l_c$ and the improvement due to the silicide's increase in the contact area is minimal.

### 4.5.3 Silicide Contribution to $R_{SD}$ Reduction in Fully-Scaled Devices

The experimental devices in this study were partially-scaled devices in that only the gate length was scaled down while most of the other layout and design rules followed approximately 1.5 μm ground rules. In modern technologies, all of the lateral and vertical dimensions are scaled including the gate to contact-hole spacing, contact hole length, etc. These are referred to as fully-scaled devices. In a fully-scaled device, the layout ground rules are much more stringent than those in the partially-scaled case. It is relevant to study the amount of improvement that can be expected from the silicide in this case. The typical layout ground rules for a fully-scaled 0.25 μm technology would be a gate to contact length, $S_{unsilicided}$ of 0.25 μm, contact hole length, $l$ of 0.25 μm, and distance from far edge of the contact hole to the field edge of 0.25 μm. In the silicided case, $S_{silicided}$ is decreased to the width of the spacer, 50-100 nm. The length of the contact area is increased to include the entire source and drain area, with the exception of the spacer, which can be estimated as 0.6 μm.

Given these dimensions, the same estimations as in the previous section can be performed. The improvement in the $R_{sh}$ calculated from eq. (4.2) is approximately 45 Ω/sq. This is quite small because the distance from gate to contact has been reduced considerably. On the other hand, the length of the contact area has also been reduced considerably. Given the same silicide technology, the length of the contact area is now smaller than the contact transfer length of 0.5 μm calculated previously. Thus, increasing the contact area will have a beneficial impact on the $R_{co}$ component of the series resistance.

The amount of impact of the silicide on $R_{co}$ can be examined through the use of simulations. Figure 4-19 shows the simulations of the total series resistance, $R_{SD}$

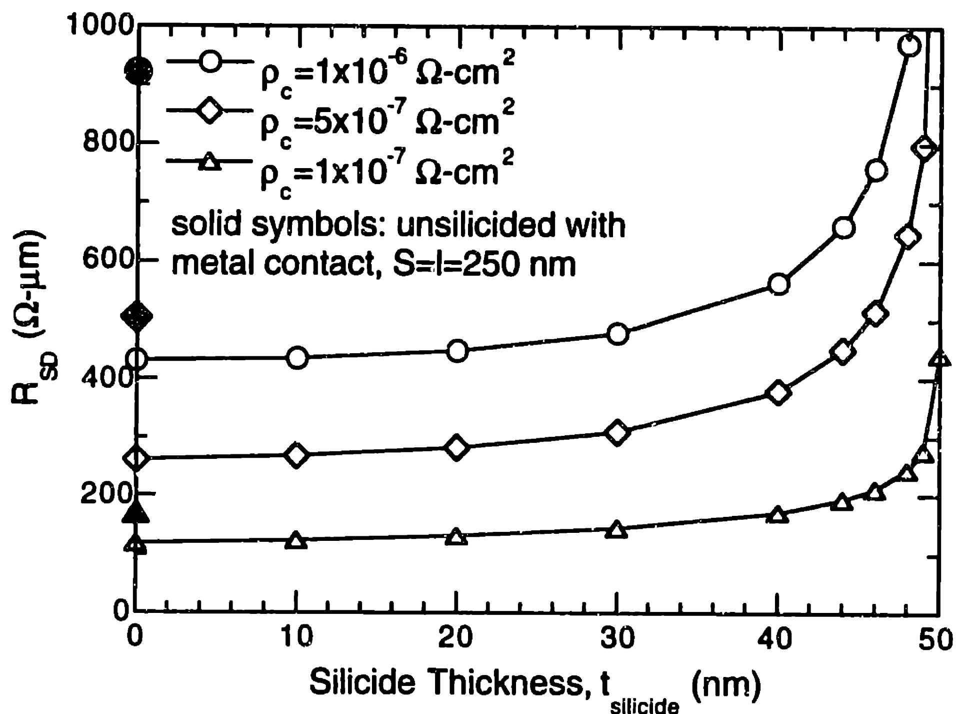


Figure 4-19: Simulated total series resistance, $R_{SD}$, vs. silicide thickness for three different contact resistivities in a fully-scaled 0.25 μm technology. Solid symbols on the left axis indicate the $R_{SD}$ for a unsilicided device with gate to contact spacing and contact hole width of 0.25 μm.

as a function of silicide thickness for three different contact resistivities with the contact geometry discussed. In the solid symbols on the left-most axis are the simulated points for unsilicided devices with a metal contact ($t_{silicide} = 0$). As shown, depending on the contact resistivity from metal or silicide to silicon, the silicide can substantially improve the $R_{SD}$ in these fully-scaled structures. For a $\rho_c = 5 \times 10^{-7}\ \Omega\text{-cm}^2$, the reduction in $R_{SD}$ is from 500 Ω-µm to 250 Ω-µm and for $\rho_c = 1 \times 10^{-6}\ \Omega\text{-cm}^2$ the reduction is from 900 Ω-µm to 400 Ω-µm.

## 4.6 Other Technology Integration Issues

### 4.6.1 Gate Resistance

This work has concentrated on the reduction of the parasitic source/drain device series resistance. However, the polysilicon gate resistance must also be minimized for high-speed operation in the deep-submicrometer regime. It has been shown in bulk analyses, that the gate resistance for a 0.1 µm device technology with a sheet resistance of 10 Ω/sq. contributes 15% of the delay [78]. This will be even more important in SOI because of the reduced parasitic capacitances.

A critical issue in the recent literature has been the drastic increase in polysilicon silicide sheet resistance as the gate length is reduced. It has been shown from very early studies that $TiSi_2$ gates have a tendency to remain in a high resistivity $C_{49}$ phase, instead of transforming to the low-resistivity $C_{54}$ phase when the linewidths are narrow [68]. Much work has been devoted to this issue including the study of PtSi to eliminate this linewidth dependence [79], the use of metal-strapped gates [80], and separate silicidation of the gate and source/drain with $TiSi_2$ polycide and salicide [81].

The linewidth dependence of the gate sheet resistance of the titanium/cobalt laminates studied in this work is shown in Fig. 4-20. The data shown in this figure were obtained from a Ti/Co process using 3.5 nm Ti/14 nm Co for our extreme-submicrometer bulk devices [82] fabricated by x-ray lithography. As shown, the polysilicon gate resistance is fairly independent of linewidth down to 0.2 μm. There are few data points under 0.2 μm so the trends are not quite as clear under 0.2 μm. However, this is already significantly improved over the conventional $TiSi_2$ technology [83]. The excellent linewidth dependence of $CoSi_2$ has also been verified by other researchers forming $CoSi_2$ with a TiN cap [84].

However, it should be noted that the gate resistance in Fig. 4-20 is about 10-15 Ω/sq. This is still on the high side for 0.1 μm technologies but is due to the very thin silicide as opposed to linewidth dependence or silicide quality problems.

For ultra-thin SOI, this becomes a technology integration problem because ultra-thin silicides are needed. This is a drawback of direct silicidation of the source/drain/gate as compared to selective epitaxial or selective tungsten techniques [61,85]. On the other hand, selective deposition techniques are not necessarily available or straightforward as process modules in typical fabrication lines. Full integration of the silicide technology could involve the separate silicidation of the gate and source/drain by use of a polycide or the improvement of the Ti/Co silicidation technology on polysilicon to reduce the resistivity. Further exploration of this is needed for high-performance CMOS applications.

## 4.7 Summary and Conclusions

Device series resistance in ultra-thin film SOI MOSFETs has been studied through 2-D numerical simulations and process experiments. To achieve low

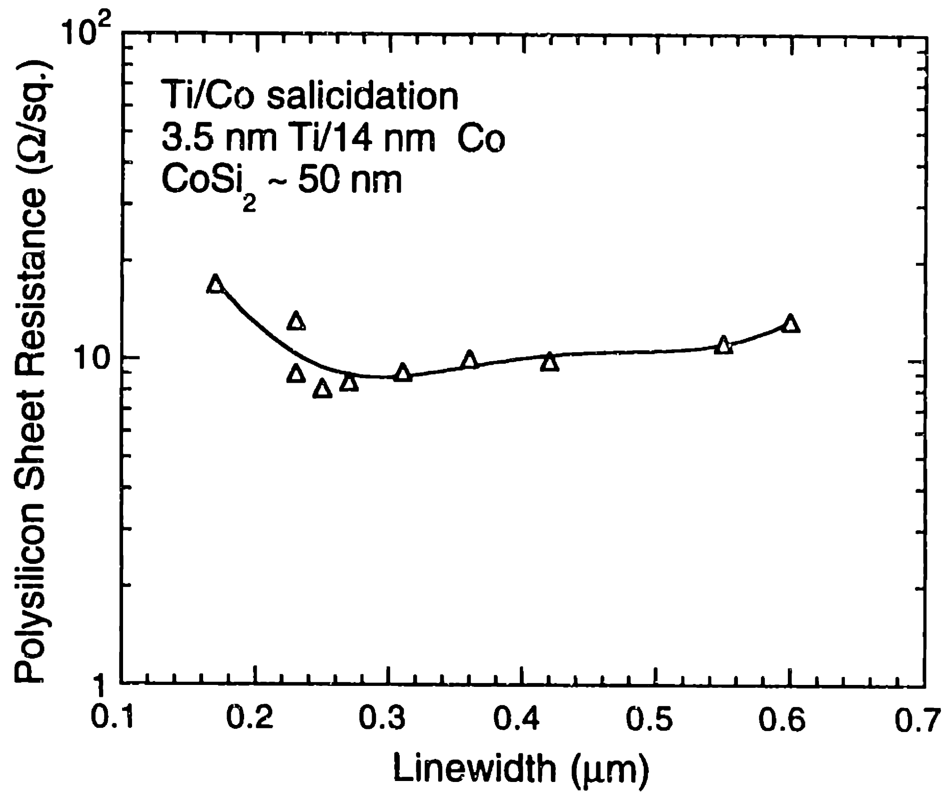


Figure 4-20: Measured polysilicon gate resistance as a function of linewidth for $CoSi_2$ formed by 3.5 nmTi/14 nm Co.

parasitic series resistance, very thin silicides are required that do not fully consume the SOI silicon film. A novel titanium/cobalt silicidation technique was explored to achieve agglomeration-resistant, thin self-aligned $CoSi_2$. Using this process, SOI NMOS devices with excellent performance and record low device series resistance were fabricated. This work demonstrates that the series resistance in ultra-thin film SOI can be comparable to the best bulk technologies; thus removing the concern that high series resistance will negatively impact performance in deep-submicrometer SOI.

# Chapter 5

# Self-Heating Effects

## 5.1 Introduction

The low thermal conductivity of the underlying silicon dioxide layer, which is about two orders of magnitude less than that of silicon, inhibits cooling in SOI devices and causes severe self-heating. This results in higher channel operating temperatures and is evidenced by the negative differential conductance at high gate biases that is characteristic of most SOI devices [86,87]. The device mobility is reduced as a result of the elevated temperatures and results in reduced maximum drain saturation current and more complicated device modeling. In addition, high channel temperatures lead to increased interconnect temperatures at the silicon-metal contact and make conduction cooling through the source, drain and interconnects important [88]. These factors motivate a need for accurate

measurement and modeling of channel and interconnect temperatures in SOI MOSFETs.

Self-heating effects in SOI MOSFETs have been measured previously using a liquid crystal technique [87], the temperature dependence of leakage currents [89], and noise thermometry [90]. Thermal models have also investigated the temperature rise [88,91,92,93]. These initial data indicated a significant temperature rise. However, a systematic study of the temperature rise as a function of critical device dimensions, e.g. buried oxide thickness, and a comparison of direct temperature measurements to thermal modeling were not available. In addition, the severity of the self-heating problem in terms of circuit operation has not been evaluated.

In this chapter, a simple technique for temperature measurement in SOI MOSFETs is developed and channel temperatures are measured over a wide range of device parameters. Measurements are compared with thermal model predictions and the impact on circuit design is assessed. A methodology for extraction of appropriate parameters for circuit simulation is also proposed.

## 5.2 Temperature Measurement Test Structure

The test structures for temperature measurement are MOSFETs with the gate configured for four-point resistance measurements as shown in Fig. 5-1. The polysilicon gate serves as a temperature-sensing resistor for the channel region, where the device power is dissipated. This technique was first proposed by Mautry and Trager for temperature measurement in conventional bulk MOSFETs [94]. Accurate measurement of the channel temperature can be obtained from the gate temperature because the gate and channel are separated only by a thin gate oxide.

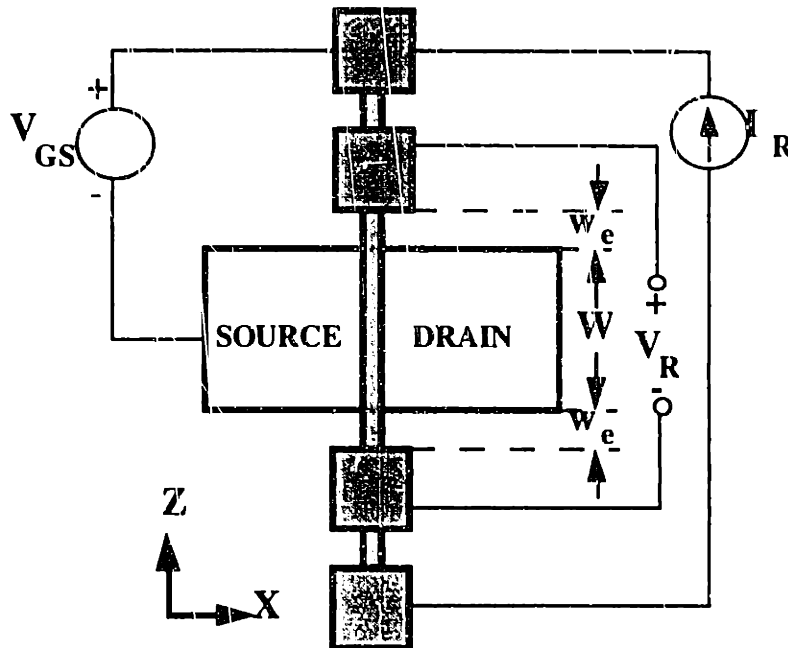


Figure 5-1: Top-view of the experimental test structure for temperature measurement. $W$ is the channel width and $w_e$ is the region between the device edge and the gate contact pad.

This assumes that the current that is flowing through the polysilicon gate, $I_R$ is small enough so that Joule-heating is negligible along the gate width. This work performs additional thermal analysis to extract the channel temperature from the gate temperature in SOI devices.

## 5.2.1 Device Fabrication

Test structures are fabricated on commercially available SOI wafers formed by the SIMOX technique (Separation by Implantation of Oxygen) with various silicon thicknesses ($t_{si}$), buried oxide thicknesses ($t_{box}$), and gate-to-metal contact spacings ($L_d$) and on conventional bulk wafers for comparison. The devices used in this experiment are unsilicided $n^+$ polysilicon, non-LDD nMOSFETs fabricated

process presented in Appendix A. The channel doping is boron 6x10$^{17}$ cm$^{-3}$, the gate oxide thickness is 5.5 nm and the W/L ratio is 10 μm/0.3 μm. The completed SOI devices are partially-depleted with a threshold voltage of 0.7 V. A cross-section of the finished device is shown in Fig. 5-2. The dimensions of the structure and the thermal conductivities are given in Table 5-1 [95,96].

## 5.2.2 Measurement Technique

The resistance of the polysilicon gate, $R_G(P)$, is measured as a function of device power, where $P=I_D V_{DS}$. The temperature dependence of $R_G$ is calibrated by varying the substrate temperature using a variable temperature chuck with the device turned off, i.e. an isothermal gate. From the resulting calibration function and $R_G(P)$, an average gate temperature $T_{G(avg)}(P)$ is obtained.

The average channel temperature, $T_C$, is approximately equal to the local gate temperature directly above it because the thermal resistance of the gate oxide is small and heat transfer to the ambient air is negligible [97]. However, the value of $T_C$ is not equal to $T_{G(avg)}$ because the calibration technique assumes the entire gate is heated. During device operation, only the regions of the gate directly above the channel are heated and contribute to a change in $R_G$. The difference between $T_C$ and $T_{G(avg)}$ depends on the shape of the temperature profile in the gate region. In bulk devices, the high thermal conductivity silicon substrate tends to distribute the heat in the gate region and broaden the temperature profile, thus, $T_C$ is well-approximated by $T_{G(avg)}$ [94]. In contrast, in SOI devices, the length-scale for heat conduction is on the order of a few microns as discussed in section 5.4.1. The temperature distribution along the gate width is significant and must be considered.

The temperature profile can be approximated as a constant temperature in

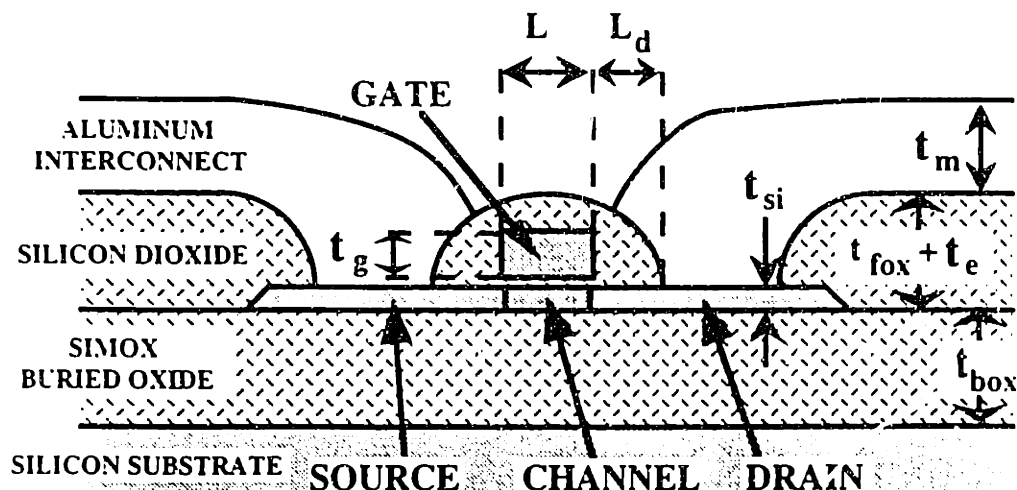


Figure 5-2: Cross-sectional view of silicon-on-insulator (SOI) MOSFET. The critical dimensions for the thermal measurements and model are given in Table 5-1.

Table 5-1.
Thermal conductivities and device dimensions.

| | | |
|---|---|---|
| silicon dioxide conductivity, $k_{ox}$ | 1.40 | W/mK |
| aluminum conductivity, $k_m$ | 239 | W/mK |
| source/drain/gate conductivity, $k_d$ | 63 | W/mK |
| channel and substrate conductivity, $k_c$ | 148 | W/mK |
| channel length, $L$ | 0.30 | μm |
| channel width, $W$ | 10 | μm |
| silicon thickness, $t_{si}$ | 41-177 | nm |
| gate oxide thickness, $t_{ox}$ | 5.5 | nm |
| SIMOX buried oxide thickness, $t_{box}$ | 0.293-0.503 | μm |
| channel-metal contact separation, $L_d$ | 0.8-3.8 | μm |
| channel-gate contact separation, $w_e$ | 2 | μm |
| interconnect width, $w_m$ | 6 | μm |
| gate polysilicon thickness, $t_g$ | 0.29 | μm |
| aluminum interconnect thickness, $t_m$ | 1 | μm |
| field oxide thickness, $t_{fox}$ | 0.25 | μm |
| gate-metal interlevel oxide thickness, $t_e$ | 0.35 | μm |

the heated portions of the gate, and a linear decrease to the substrate temperature, $T_0$, at the gate pads. The resultant temperature profile along the gate width is shown schematically in Fig. 5-3(a). The local gate electrode resistance per unit width in the Z direction, shown schematically in Fig. 5-3(b), is obtained from the calibration function and the assumed temperature profile. The integration of the calculated gate electrode resistance per unit width in the Z direction yields the total resistance, $R_G$, for a gate electrode having a channel temperature, $T_C$. Using this technique, the channel temperature is found by iteratively calculating $R_G$ for increasing $T$ until the measured $R_G$ is reached.

This $T_C$ somewhat underestimates the actual channel temperature because the temperature profile assumes that the channel is isothermal and neglects heat conduction through the buried oxide layer to the substrate in the region between the device edge and the gate contact pad. The error from these assumptions is less than 8% for our SOI test structures ($W$ = 10 μm) and is included in the measurement error [98]. This error can be further reduced by using test structures with larger $W$.

## 5.3 Experimental Results

Channel temperature measurements were performed on test structures with varying $t_{si}$, $t_{box}$, and $L_d$. Figure 5-4 shows an example of the raw data from device and calibration measurements. Typical operating conditions for a 0.3 μm technology ($V_D$=2-3 V, $V_G$=2-3 V) were used for the device measurement. Good sensitivity of the technique was obtained with the arsenic-implanted gate resistor. The sheet resistance of the gate resistor was typically 250-280 Ω/sq. because the polysilicon gate was doped by arsenic implantation. The resistance of the gate

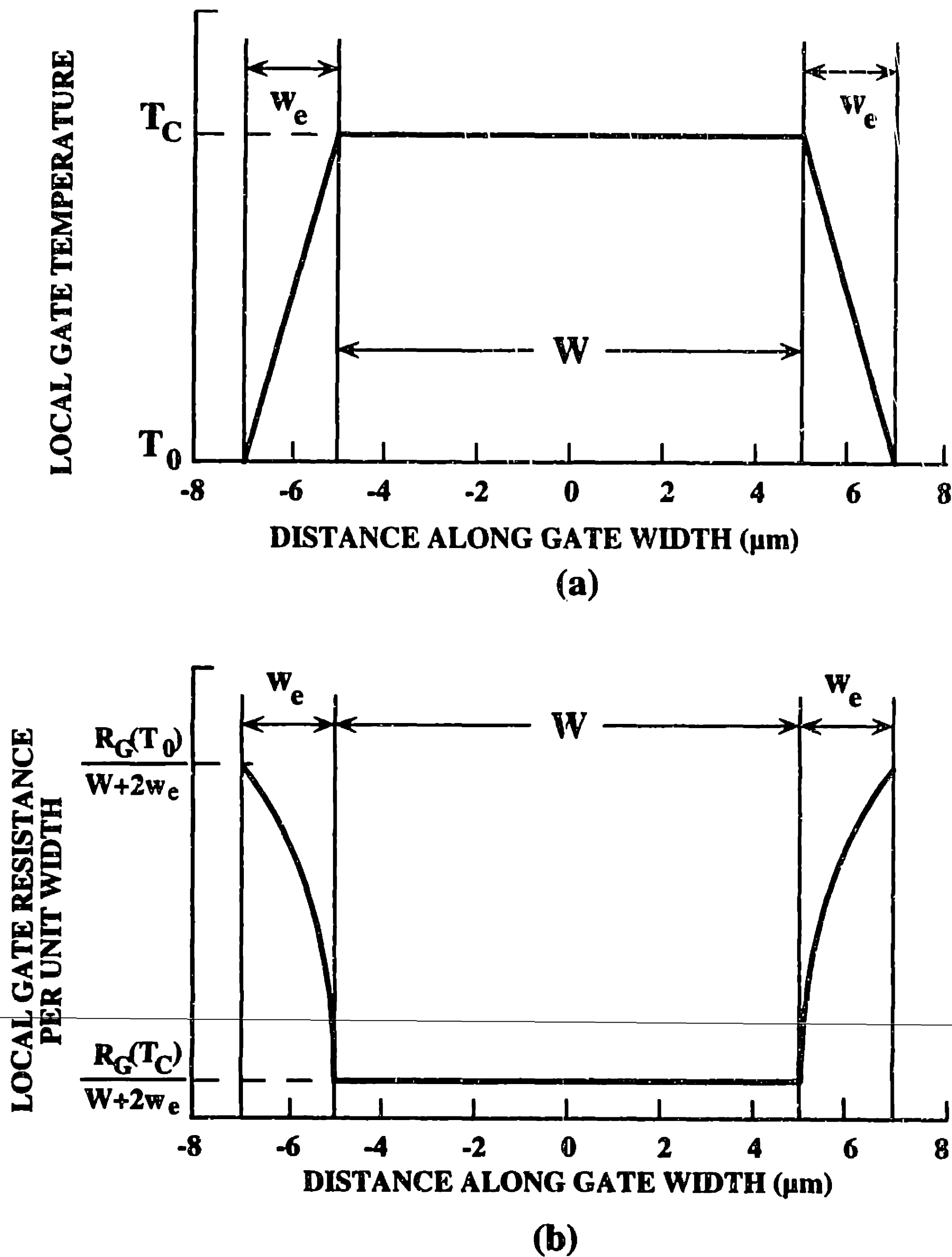


Figure 5-3: (a) Assumed temperature profile along the gate electrode (in the Z direction) of a SOI MOSFET. (b) Corresponding gate electrode resistance per unit width (in the Z direction) of a SOI MOSFET.

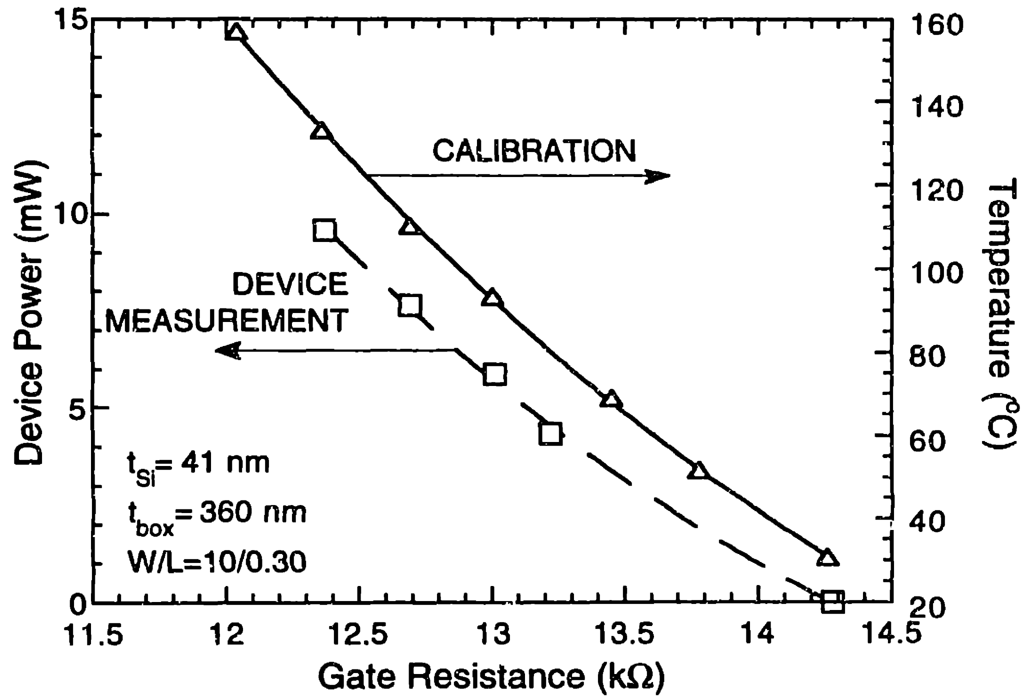


Figure 5-4: Calibration and device measurement data for a typical SOI device.

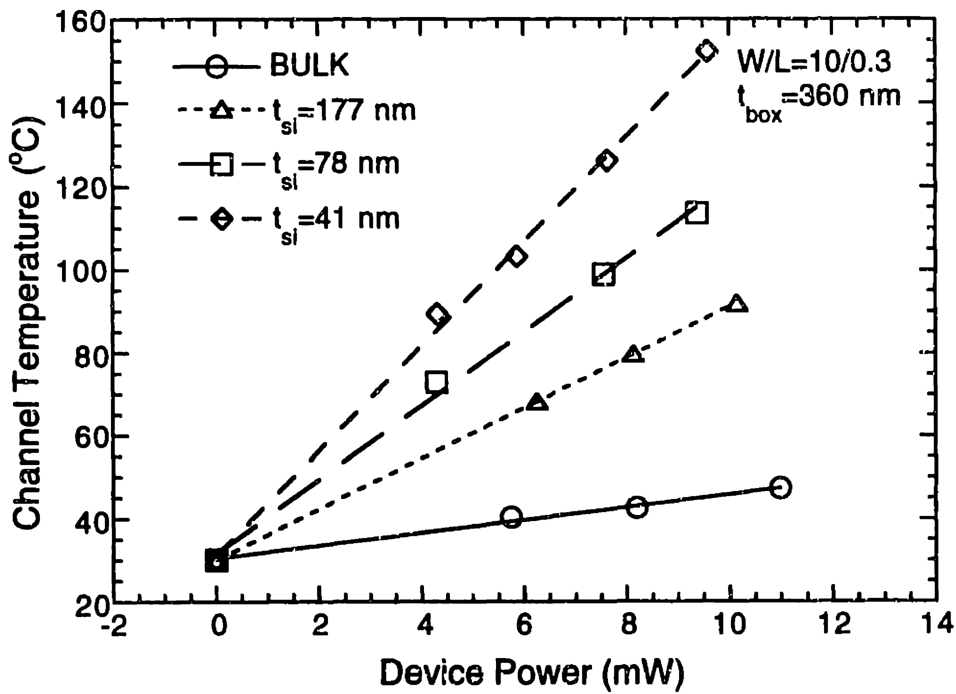


Figure 5-5: Channel temperature vs. power for SOI devices for several silicon thicknesses and a bulk device.

resistor was not dependent on the gate bias or the magnitude of the current flowing along the gate. This indicated that polysilicon depletion did not affect the resistance measurement, and any change in the resistance was due to temperature.

Figure 5-5 shows the extracted channel temperature for SOI devices of varying silicon thicknesses and for a bulk device. The temperature rise, $T_C$-$T_0$, in each case is proportional to the power $P$, and for a given power is much larger in the SOI device than in the bulk device, e.g., 70 K for $P$=8 mW and $t_{si}$=78 nm vs. only 10 K in the bulk device. As $t_{si}$ is reduced, the channel temperature increases. The channel temperature vs. power slope for each case can be interpreted as a thermal resistance from the channel at temperature $T_C$ to the chuck at temperature $T_0$, $(T_C - T_0)/P$.

Figure 5-6 shows channel temperature data for varying buried oxide thicknesses. As $t_{box}$ is reduced, the temperature and its derivative with respect to power are reduced. Figure 5-7 shows the channel temperature for varying channel-metal contact separation. Although the channel temperature decreases with decreasing $L_d$, there is little change for the range of $L_d$ investigated.

## 5.4 Steady-State Thermal Model

### 5.4.1 Model Description

A steady-state thermal model [88] was used to understand the experimental data. The thermal model treats the source, drain, gate, and interconnects as cooling fins for the power dissipated in the channel heater. Figure 5-8 schematically shows the fin geometry. A plane of symmetry is drawn through half

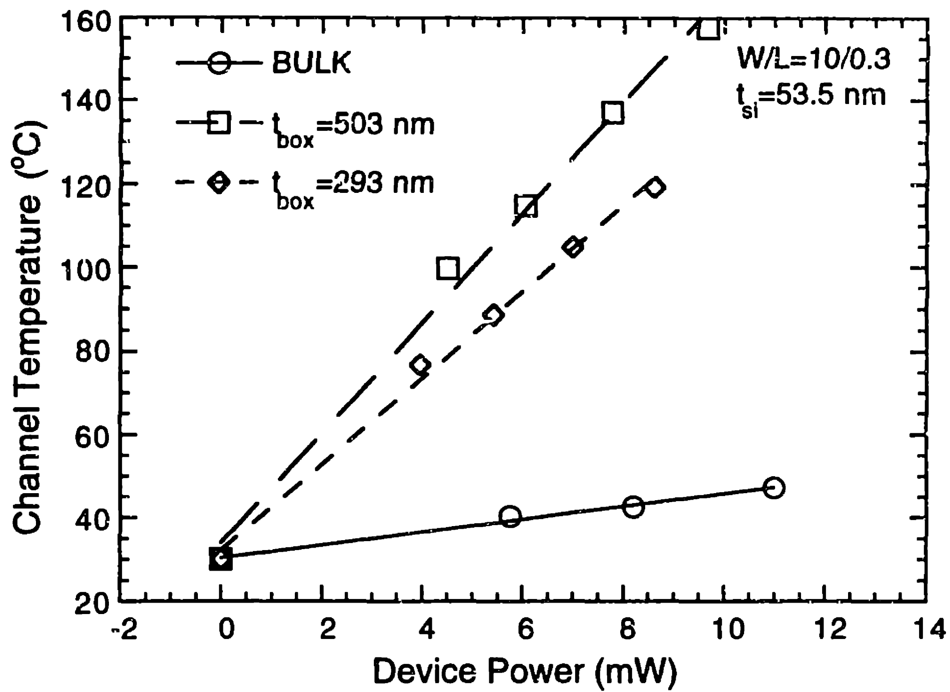


Figure 5-6: Channel temperature vs. power for several buried oxide thicknesses.

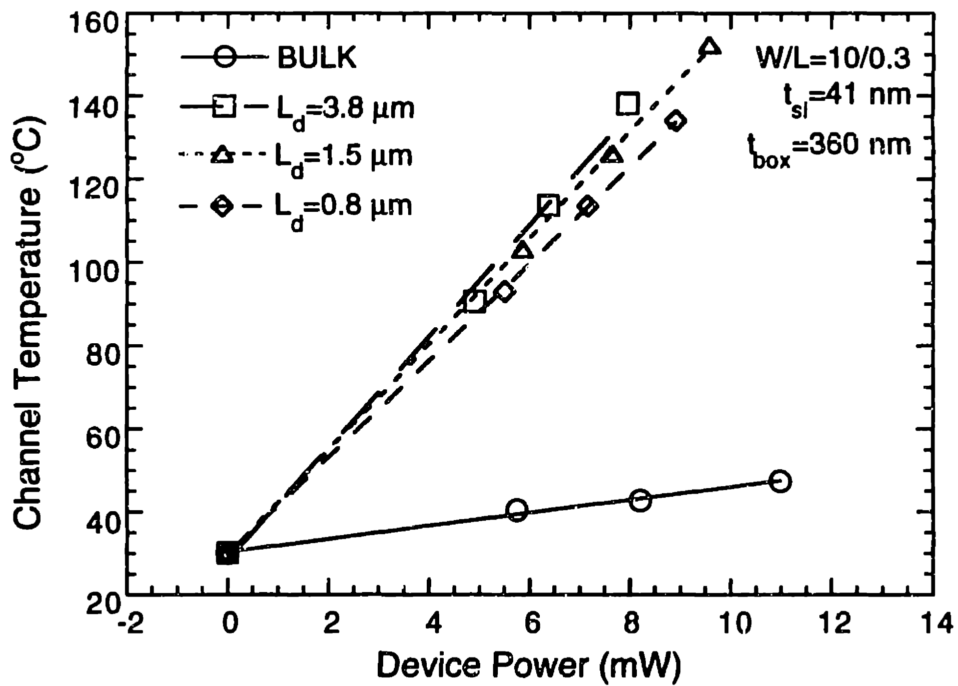


Figure 5-7: Channel temperature vs. power for several channel-metal contact separations.

of the gate in the Y-Z direction and in the X-Y direction. The model assumes an isothermal channel and an isothermal substrate at the temperatures $T_C$ and $T_0$, respectively. The heat equation is solved in each fin with the conditions of temperature continuity and energy conservation at the fin interfaces. The resulting temperature distributions are given by:

$$T_m - T_0 = Z_1 \exp[m_m(L_m - x_m)] \tag{5.1}$$

$$T_d - T_0 = Z_2 \exp[m_d x_d] + Z_3 \exp[-m_d x_d] \tag{5.2}$$

$$T_g - T_0 = Z_4 \exp[-m_g x_g] \tag{5.3}$$

$T_{m,d,g}$ and $x_{m,d,g}$ are the temperatures and the locations within the metal interconnect, gate, and drain, respectively. The parameters $Z_1$, $Z_2$, $Z_3$, and $Z_4$ are uniquely found by solving a fourth-order matrix equation [88,97].

A useful physical quantity that is obtained from the fin equations is the thermal healing length, $\frac{1}{m}$, which is a measure of the length-scale for thermal conduction in each fin. The distance from a heating source over which the fin temperature decays to the substrate temperature is on the order of several thermal healing lengths. The thermal healing length is given by $\frac{1}{m} = \left(\frac{kt}{h}\right)^{1/2}$, where $k$ and $t$ are the thermal conductivity and thickness of the fin. The parameter $h$ is the heat transfer coefficient from the fin to the substrate through the silicon dioxide and is approximately equal to $k_{ox}/t_{lo}$, where $k_{ox}$ and $t_{lo}$ are the thermal conductivity and thickness of the silicon dioxide separating the fin and substrate [88]. For typical device dimensions as given in Table 5-1, $\frac{1}{m_m} = \left(\frac{k_m t_m}{h_m}\right)^{1/2} \approx 13$ µm in the

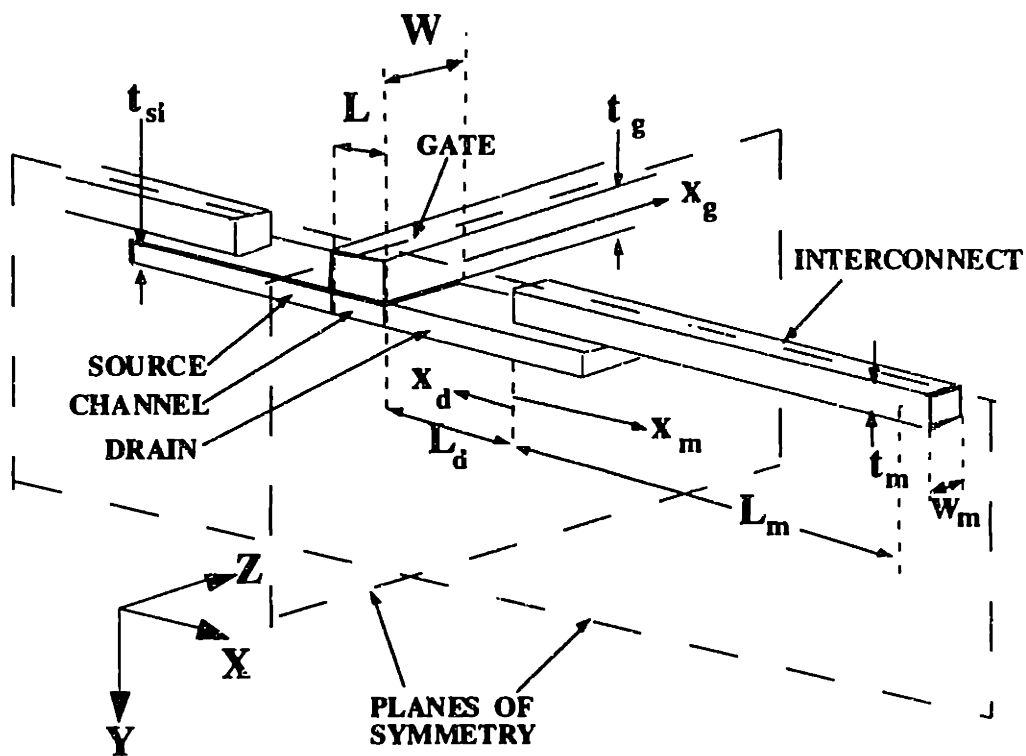


Figure 5-8: Schematic of the fin geometry in the thermal model of a SOI MOSFET.

interconnects, $\frac{1}{m_d} = \left(\frac{k_d t_d}{h_d}\right)^{1/2} \approx 1$ μm in the source and drain, and $\frac{1}{m_g} = \left(\frac{k_g t_g}{h_g}\right)^{1/2} \approx 2$ μm in the gate. The external probe pads in the experimental test structure are placed at least a thermal healing length away to minimize their effects on the internal device cooling.

The thermal conductivities used in the model are those reported in bulk samples and are not used as fitting parameters [95,96]. The thermal conductivity of the SIMOX buried oxide measured in a separate experiment is within 10% of the bulk value for silicon dioxide [98,99]. The temperature dependencies of the thermal conductivities are neglected. This is a reasonable approximation for silicon dioxide and aluminum. In the heavily-doped source and drain regions, the temperature dependence is significant. The value of $k_d$ in Table 5-1 is chosen at $T = 349$ K which is the average of $(T_0+T_C)/2$ for all the data, where $T_C$ is the largest measured channel temperature in a given device.

### 5.4.2 Comparison of Predictions and Data

Figure 5-9 compares the experimental data with the model predictions of the channel-substrate thermal resistance, $R_C$, as a function of the silicon film thickness. The channel-substrate thermal resistance corresponds to the slope of the channel temperature vs. power curves shown in Figs. 5-5, 5-6, and 5-7. Each data point is the average of thermal resistance measurements at several powers on a single device. The error bars take into account the uncertainties in the device physical parameters (i.e. $t_{si}$, $t_{box}$, $t_{ox}$, $k_d$, $k_{ox}$, etc.) and the approximation employed calculating the channel temperature from the gate resistance. As the silicon thickness is reduced, the temperature rise in the device increases, showing the

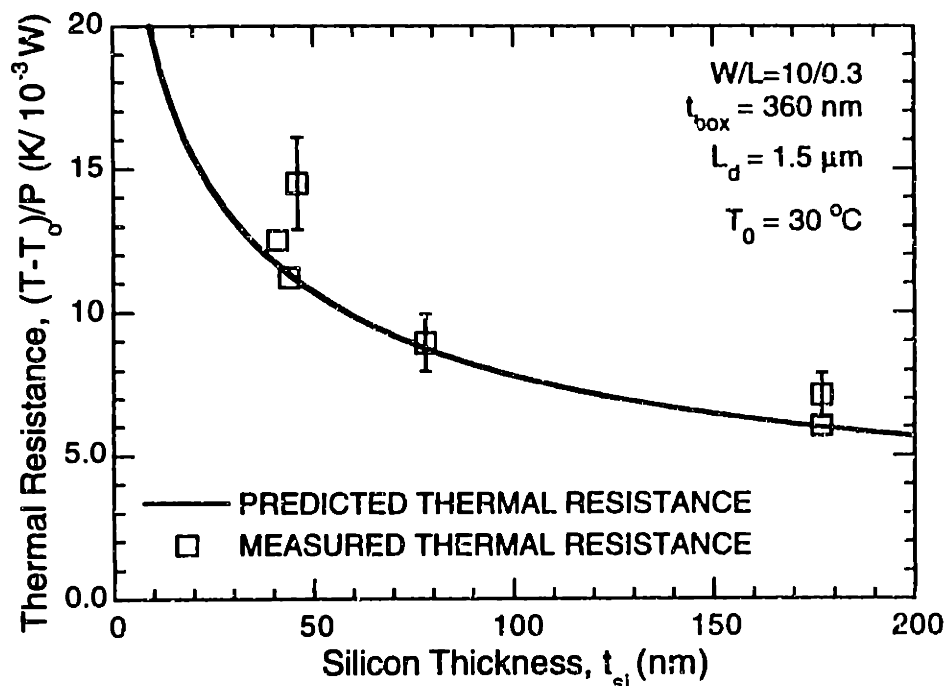


Figure 5-9: Prediction of the channel-substrate thermal resistance as a function of source and drain thicknesses.

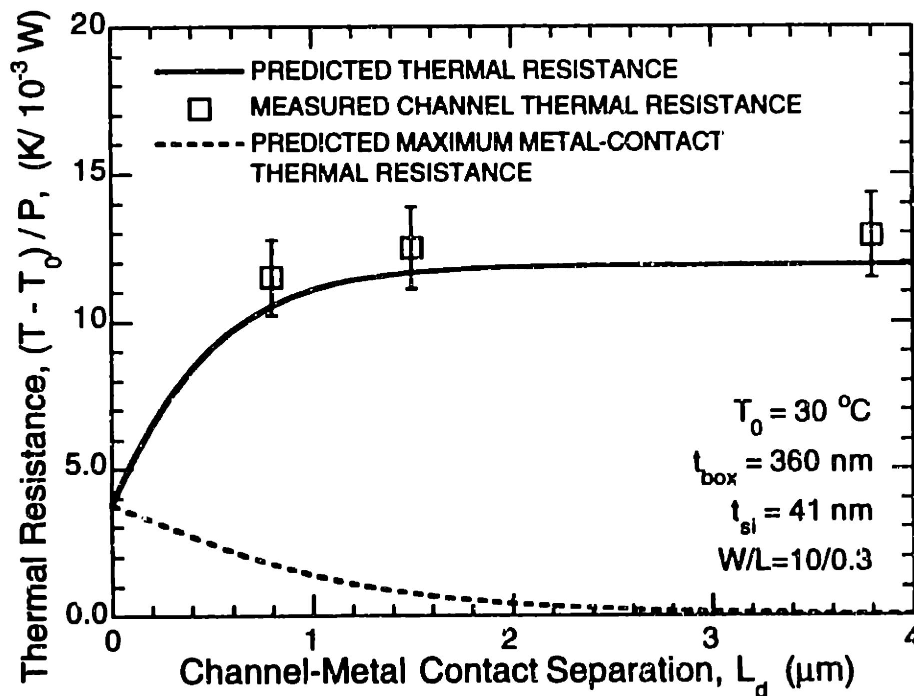


Figure 5-10: Prediction of the channel-substrate thermal resistance as function of channel-metal contact separation.

same trend as the data. Physically, this can be understood through the relationship between $t_{si}$ and the thermal healing length $\frac{1}{m_d}$. As $t_{si}$ increases, the thermal healing length or the area of the source and drain that participates in appreciable cooling to the substrate is increased, and $T_C$ and $R_C$ are reduced. The agreement between the thermal model predictions and the data is very good considering the uncertainty in the thermal conductivities and device dimensions used in the model.

Figure 5-10 shows the SOI device thermal resistance as a function of the channel-metal contact separation. For large $L_d$, this parameter has little effect on the temperature rise because the temperature has decayed in the source and drain before the interconnect is reached. As $L_d$ is reduced to less than 1 μm, comparable to the thermal healing length in the source and drain, the interconnects become more important as cooling fins, and the device temperature is reduced. This causes the metal contact temperature to increase.

Figure 5-11 illustrates the dependence of the channel-substrate thermal resistance on the buried oxide thickness. The device temperature decreases as $t_{box}$ decreases because the thermal resistance of the oxide layer decreases. But, the dependence is not linear as predicted from simple 1-D thermal conduction, where $R_C = \frac{t_{box}}{(Ak_{ox})}$ and $A$ is the area of the drain region [86]. This can be understood from the fin analysis. The effective area where conduction is significant can be approximated as $A \approx \frac{2W}{m_d}$ if $\frac{1}{m_d} < L_d$. Substituting this expression for A into $R_C = \frac{t_{box}}{(Ak_{ox})}$ yields

$$R_C \approx \frac{1}{2W}\left(\frac{t_{box}}{k_{ox}k_d t_{si}}\right)^{1/2} \tag{5.4}$$

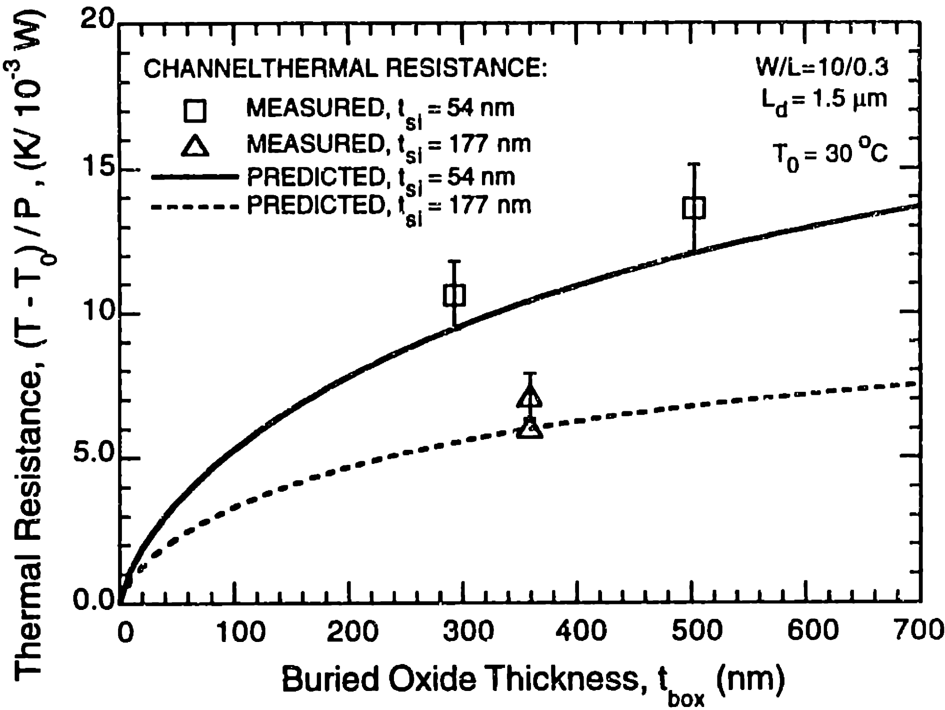


Figure 5-11: Prediction of the channel-substrate thermal resistance as a function of buried oxide thickness.

which is in good qualitative agreement with the data. This simple scaling analysis shows that $R_C$ is roughly proportional to the square root of $(t_{box}/t_{si})$, thus halving $t_{box}$ or doubling $t_{si}$ have the same impact, if all other parameters are held constant.

## 5.5 Transient Measurements

The measurements and the modeling show that the temperature rise in SOI devices is linearly proportional to static power dissipation with the proportionality constant depending on device dimensions. In the typical range of operation of modern MOSFETs, this temperature rise is significant. Under dynamic operating conditions, the temperature rise will not follow the instantaneous power dissipation because the thermal time constants may be much longer than typical electrical periods (e.g. clock) [92,100].

Figure 5-12 shows the dynamic response of a typical SOI MOSFET. In this measurement, the drain voltage is kept constant and the gate voltage consists of a square wave with adjustable minimum and maximum levels. The current is measured with a current probe connected to a digital oscilloscope. The low level of the gate voltage is always higher than the threshold voltage so that interface trap transients do not contaminate the measurements. The devices measured in this experiment are silicided, fully-depleted, non-LDD SOI MOSFETs with a silicon thickness of 60 nm, oxide thickness of 9 nm, and buried oxide thickness of 360 nm (same as in Chapter 4). As shown in Fig. 5-12, for moderate power dissipation (curve C), the drain current is initially high and decreases as the device self-heats. For increased power dissipation (curve B), the magnitude of the transient increases. In the bulk and the SOI case with low power dissipation (curves A and D), the

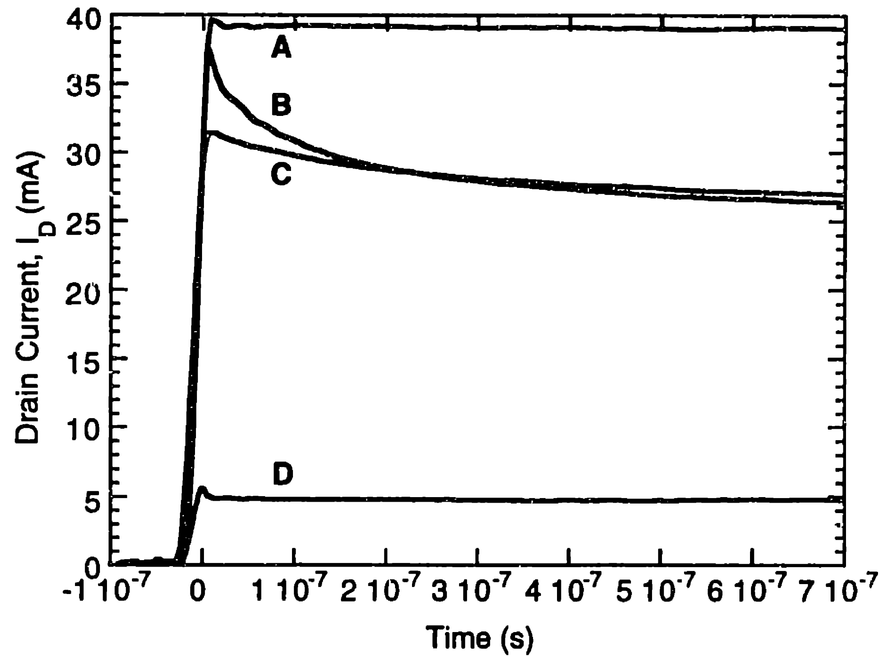


Figure 5-12: Transient drain current measurements for a SOI MOSFET ($t_{si}$=60 nm) at various bias conditions and a conventional bulk MOSFET. Device parameters are $t_{ox}$ = 9 nm, $L_{eff}$ = 0.35 μm, $W$ = 50 μm. Bias conditions are curve A: Bulk MOSFET, $V_D$ = 3 V, $V_G$ = 4 V; curve B: SOI MOSFET with high power dissipation, $V_D$ = 4 V, $V_G$ = 4 V; curve C: SOI MOSFET with moderate power dissipation, $V_D$ = 2 V, $V_G$ = 4 V; curve D: SOI MOSFET with low power dissipation: $V_D$ = 1 V, $V_G$ = 1 V.

transient is insignificant. This clearly indicates that the observed transients are due to the self-heating effect. The time constants of the transients are on the order of 150-250 ns and are dependent on power dissipation. This is comparable to other measurements which have reported time constants in the range of 100 ns-1 μs [92,100,101].

In a typical digital circuit, devices are only dissipating power during a switching event. The maximum time a device is "on" is about 1/10 of the clock cycle. For sub-0.5 μm technologies with clock cycles of 50 MHz or above, this translates to 2 ns or less. Hence, during circuit operation, the device temperature can be well-approximated as a constant temperature, which can be estimated from the average power dissipation, as in any bulk circuit. The most serious remaining issue then becomes the extraction of proper constant temperature parameters for SOI circuit simulation.

## 5.6 Extraction of Model Parameters

### 5.6.1 Methodology

Because of the long thermal transient, device modeling parameters obtained from static measurements are not appropriate for dynamic circuit calculations. Constant temperature parameters, i.e. the non-self-heated device characteristics, are needed. Transient drain current measurements [92,101] and frequency-dependent measurements of the output conductance [100] have been performed to analyze the dynamic behavior of heating in SOI MOSFETs. Although both methods are useful in the analysis of device self-heating, they are relatively complex for device characterization and thus are not suitable for large numbers of

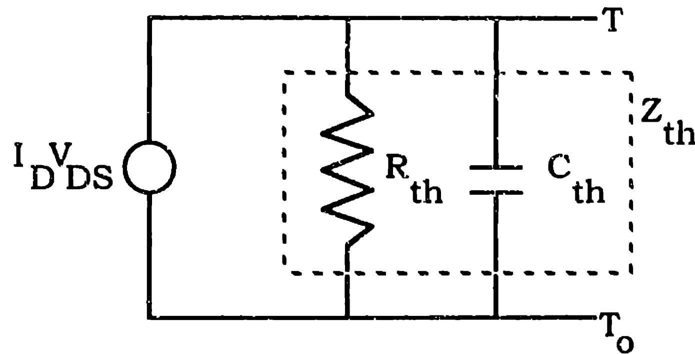


Figure 5-13: Equivalent thermal circuit for self-heating effects.

measurements. Analytical modeling of the self-heating effect has also been used in circuit simulation [102], but, the addition of a full-scale thermal model in a circuit simulator adds complexity and requires a number of additional parameters.

In this section, a simple methodology is proposed for accurate parameter extraction in SOI devices for circuit simulation with minimal additional complexity. Simple modifications to an existing physically-based, conventional short-channel bulk SPICE model (PCIM - Physically based Continuous IGFET Model) [103] have been performed and used to extract accurate parameters appropriate for the simulation of fully-depleted SOI circuits.

In typical bulk technologies, model parameter extraction is done by performing static measurements on devices with varying geometries and bias conditions to fit the experimental data. With a device model that includes the known temperature dependencies of the physical parameters, this methodology can be extended to SOI with minor modifications. Here, we demonstrate this using the existing physically-based bulk MOSFET model, PCIM [103] which is suitable for SPICE circuit simulation.

The PCIM model is modified for SOI by allowing the temperature to vary at each operating point depending on the device power. The temperature is assumed to be dependent on the device operating power:

$$T = T_0 + (I_D V_{DS}) Z_{th} \tag{5.5}$$

where $T$ is the operating temperature, $T_0$ is the ambient temperature, $I_D$ and $V_{DS}$ are the drain current and drain-source voltage, and $Z_{th}$ is the thermal impedance of the device. The equivalent circuit is shown in Fig. 5-13 with power being the thermal analog of current and temperature being the thermal analog of voltage. In the static measurements, the thermal impedance $Z_{th}$ is simply equal to the thermal resistance, $R_{th}$ and the relationship between temperature and power is linear as shown in the static temperature measurements.

The other SOI-specific modification in the model is a reformulation of the channel bulk charge, $|Q_B| = qN_a t_{si}$, to reflect the fully-depleted device, where $N_a$ is the channel doping and $t_{si}$ is the silicon film thickness. Short-channel effects are accounted for using the conventional bulk model [104] with fitting coefficients extracted from device data from several channel lengths.

The temperature dependent parameters in the model are $V_{FB}$, the flatband voltage; $\phi_F$ the Fermi potential; $\mu_o$, the low field mobility; and $\upsilon_{max}$ the saturation velocity [103]. The temperature dependencies of $V_{FB}$, $\mu_o$, and $\upsilon_{max}$ are fitted using device data at varying channel lengths and substrate temperatures and are found to be:

$$\mu_o(T) = \mu_o(T_0)\left(\frac{T_0}{T}\right)^{1.7} \tag{5.6}$$

$$V_{FB}(T) = V_{FB}(T_0) - (1.2x10^{-3})T \tag{5.7}$$

$$v_{max}(T) = v_{max}(T_0) - (2.3x10^{3})T \tag{5.8}$$

A room temperature saturation velocity of $7.6x10^6$ cm/s for electrons is used.

### 5.6.2 Model Fit

With these temperature-dependent parameters fixed, an optimization routine is used to self-consistently find the best-fit model parameters as one would do for a bulk technology [104]. The only additional SOI-specific parameter is the thermal resistance, $R_{th}$. Because of the earlier onset of impact ionization effects on SOI $I_D$ characteristics relative to bulk, a simple impact ionization model is also added to PCIM for more accuracy. The impact ionization model is the same as given in [105] for bulk silicon devices except that constants $C_1$ and $C_2$ are very different in SOI, so that the drain current with impact ionization becomes:

$$I_{DS} = I_{DS0}\left(1 + C_1(V_{DS} - V_{DSAT})e^{\frac{-C_2}{(V_{DS} - V_{DSAT})}}\right) \tag{5.9}$$

where $I_{DS0}$ is the drain current without impact ionization given by Eq. (14) in Ref. [103], $V_{DSAT}$ is the drain saturation voltage, and $C_1$ and $C_2$ are the impact ionization constants which are found to be 35 $V^{-1}$ and 12 V respectively.

Figures 5-14, 5-15, and 5-16 show the measured and calculated data in the subthreshold and saturation regions. Excellent fit is found with one set of device parameters for effective channel lengths ranging from 0.25 µm to 4.5 µm. Note that the model is fully continuous from the subthreshold to the saturation region and that the subthreshold slope behavior of the fully-depleted SOI devices is modeled

well. For the 4.5 μm, 0.5 μm, and 0.25 μm device above $V_G$ of 1 V, the average percentage error is less than 2% with a maximum error of 6%. For the 0.25 μm channel length at $V_G = 0.5$ V, the slightly larger discrepancy is due to the onset of impact-ionization-induced breakdown which is more severe in SOI than in bulk devices [38]. The addition of a more sophisticated impact-ionization model for SOI would reduce this error considerably.

The extracted device parameters used to model short-channel effects, field-dependent mobility, and source/drain parasitic resistances are quite consistent with expected values for this type of technology. This indicates that the simple modifications to the bulk PCIM model can correctly model and predict device characteristics for fully-depleted devices once self-heating is properly taken into account. The fitted thermal resistance $R_{th}$ = 3330 K/W (50 μm wide device) is in good agreement with our measured thermal resistance values. The measured thermal resistance for these devices is 3080-3162 K/W. This corresponds to a temperature rise of approximately 160 K at $V_D$=$V_G$=2.5 V for the $L_{eff}$=0.25 μm case. Note that in this case, the measured devices had silicided source, drain and gates and the channel width was larger than those measured in Section 5.3 ($W$=50 μm). Because of the silicided gate, the temperature coefficient of the gate resistor for the static temperature measurement is positive and linear unlike Fig. 5-4. However, good sensitivity of the technique is still obtained. In addition, a somewhat higher $R_{th}$ normalized per unit width results from these devices as compared to those measured in Section 5.3. This may be due to the fact that for wide channel widths, there is little heat dissipation through the unheated portions of the gate between the edge of the field oxide and the probe pad. Measurement of silicided and unsilicided devices fabricated at the same time resulted in $R_{th}$ values that were quite close.

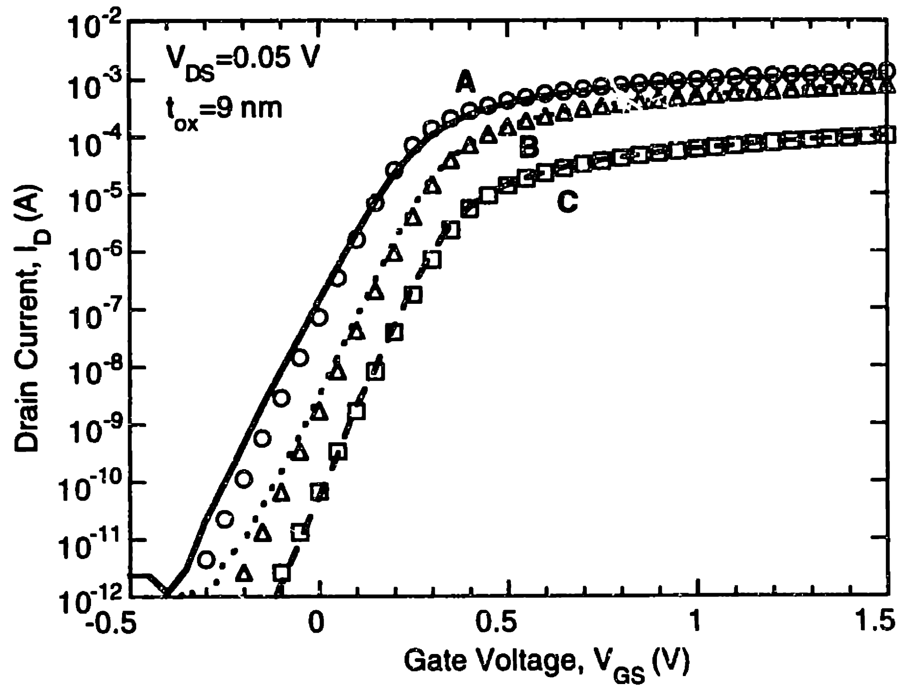


Figure 5-14: Subthreshold current characteristics for SOI devices with $L_{eff}$ = 0.25, 0.5 and 4.5 μm from measurements (curves) and model (open symbols). Device parameters are $t_{ox}$ = 9 nm, $t_{si}$ = 60 nm, and $W$ = 50 μm. Circles (curve A) represent characteristics for $L_{eff}$ = 0.25 μm, triangles (curve B) represent $L_{eff}$ = 0.5 μm, and squares (curve C) represent $L_{eff}$ = 4.5 μm.

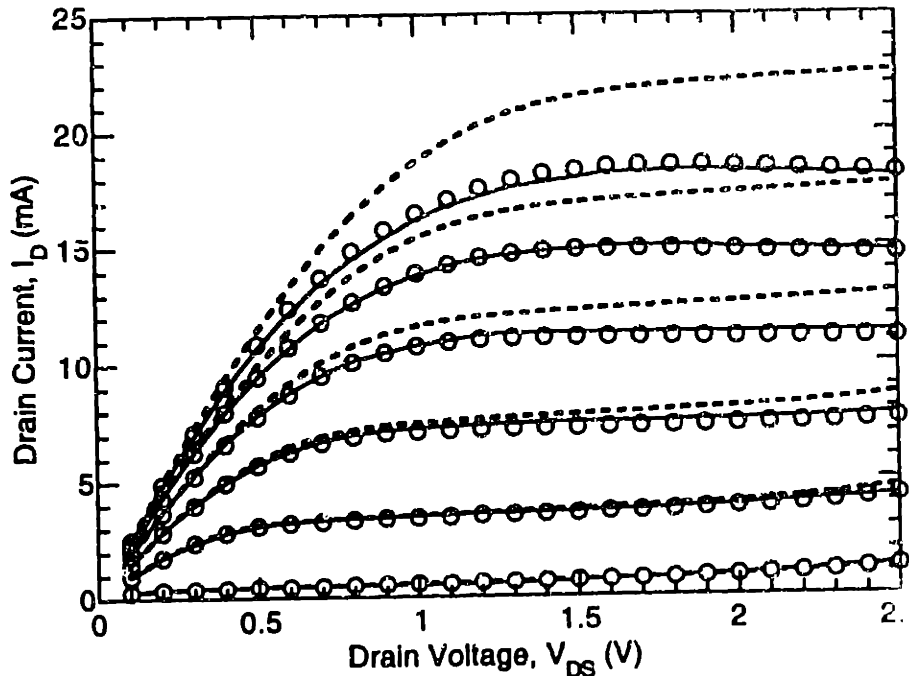


Figure 5-15: $I_D$-$V_{DS}$ characteristics for an SOI device with $W/L_{eff}$ = 50 μm/0.50 μm from measurements (solid lines) and modeling (open circles). Gate voltage is stepped from 0.5 V to 3 V in 0.5 V steps. The dashed lines represent data from the model setting $Z_{th}$ = 0 (non-self-heated device).

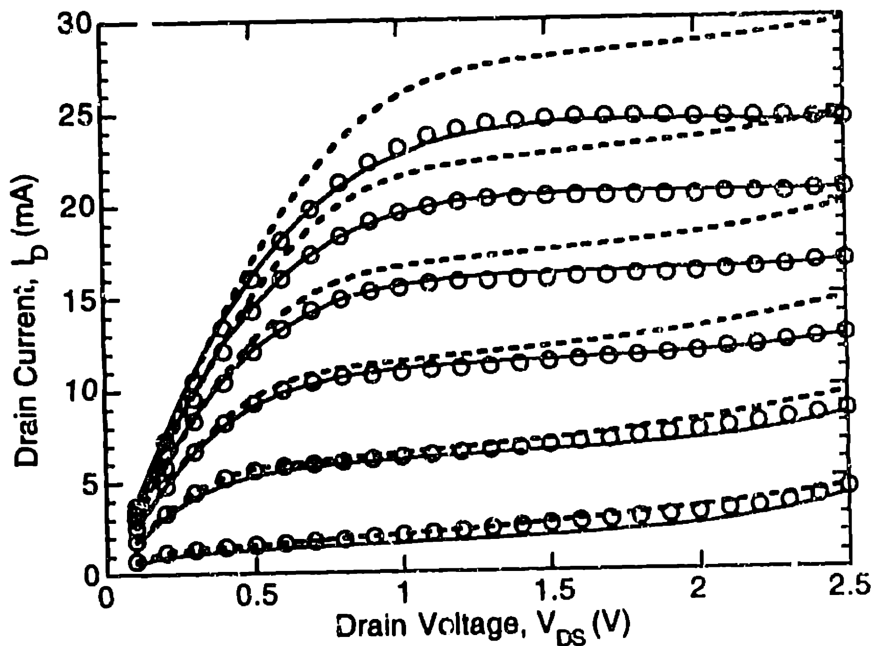


Figure 5-16: $I_D$-$V_{DS}$ characteristics for an SOI device with $W/L_{eff}$ = 50μm/0.25 μm from measurements (solid lines) and modeling (open circles). Gate voltage is stepped from 0.5 V to 3 V in 0.5 V steps. The dashed lines represent data from the model setting $Z_{th}$ = 0 (non-self-heated device).

### 5.6.3 Constant Temperature I-V Characteristics

Once the model parameters have been fitted, constant temperature I-V characteristics at any given ambient temperature, e.g. 25 °C, can be calculated by setting $Z_{th} = 0$ (Figs. 5-15 and 5-16). This models the behavior for typical digital circuit operation because the frequency of operation is much greater than the thermal time constant, thus $C_{th}$ appears as a short circuit. Note that the constant temperature curves do not exhibit the negative differential conductance observed in the measured characteristics, but show a positive output conductance as one would expect in a short-channel device.

For devices operating at frequencies close to the thermal pole of $Z_{th}$, the full equivalent thermal circuit shown in Fig. 5-13 can be added to SPICE for more accuracy. The value of $C_{th}$ can be extracted from transient temperature measurements as shown in Fig. 5-12 using the measured $R_{th}$ values. In this case, each device in the circuit would be allowed to vary in temperature. The instantaneous temperature obtained from the thermal circuit based on the instantaneous power dissipation can then be used in the SPICE model to obtain the correct current-voltage characteristics.

## 5.7 Interconnect Reliability Considerations

In a practical digital circuit, the maximum interconnect temperature is most critical because of electromigration considerations. In the worst case found here (static operation), for $t_{si}$=41 nm, $L_d$=0.4 μm, $t_{box}$=360 nm, this temperature rise approaches 25 K at the metal contact for a device power of 1 mW/μm device width (from Fig. 5-10). But, devices are only operating a fraction of the time in a real

circuit and the static power predicts too large a temperature rise in the interconnects.

The steady-state temperature rise during circuit operation in the metal contact can be estimated using the thermal model if the transient temperature fluctuations at the metal contact are small. The thermal diffusion length is a measure of the length over which the transient temperature fluctuations are significant and is approximately $(\alpha\tau)^{1/2}$, where $\alpha = 0.33$ cm$^2$/s is the thermal diffusivity of heavily doped silicon, and $\tau$ is the clock period. Using $\tau = 5$ ns (200 MHz clock), the thermal diffusion length is 0.4 µm, and the time-averaged power can be used with the steady-state thermal model to estimate the temperature rise in the metal contact. The power dissipation of importance in this case is the average power dissipation per unit *active area* (not the power per total chip area) because cooling occurs primarily in the active area.

The average power dissipation per unit *active area* of a representative heavily loaded NMOS transistor (e.g. clock driver) in a 0.4 µm CMOS technology is estimated to be about 3000 W/cm$^2$. The length of the active area in that technology would be about 2.8 µm ($L_d$ of 0.4 µm, contact hole width of 0.4 µm, contact spacing to edge of active area of 0.4 µm). Hence, the time-averaged power dissipation is 0.084 mW/µm device width. For this case, the model predicts a steady-state metal contact temperature rise on the order of 3 K.

The above analysis assumes a device layout of an isolated test device. If the device is very wide, and is laid out in a serpentine fashion with multiple fingers, as is common for such devices, the power dissipation per unit width almost doubles because neighboring devices share a source/drain. In this case, the source/drain regions and the metal interconnect become less important for heat removal. A worst-case approximation of this case would return to simple 1-D thermal

conduction in the direction normal to the substrate. Under such conditions, the metal contact regions and channel exhibit the same temperature rise, $T_C - T_0 = \frac{Pt_{box}}{Ak_{ox}}$, which is approximately 8 K.

From these simple calculations, it may be concluded that for a 0.4 µm device technology and the SOI parameters chosen, the temperature rise under operating conditions will not greatly reduce metal reliability. However, the actual impact will depend on the particular application, the maximum power dissipation per unit active area in the chip, and the corresponding SOI parameters chosen. With further scaling, e.g. into the 0.25 µm region and below, it may be required that device dimensions, e.g. $t_{box}$, be reduced to minimize the effects of self-heating.

## 5.8 Summary and Conclusions

The steady-state temperature rise in SOI devices is measured and modeled as a function of various device parameters. The temperature rise is significant, and dependent on the buried oxide thickness, silicon thickness, and channel-metal contact separation. The difference in temperatures between device characterization and actual circuit conditions requires accurate measurement and modeling of temperature rises.

Channel-temperature measurements are needed in addition to typical current-voltage characterization to extract appropriate modeling parameters for dynamic circuit calculations. A methodology for the proper extraction of parameters for circuit simulations is proposed. A conventional bulk MOSFET model with minor modifications is used to demonstrate this modeling methodology for fully-depleted SOI. Excellent fit between experimental and modelled data is achieved.

Steady-state analysis indicates that self-heating effects do not appear to limit the use of SOI technology in terms of electromigration resistance. However, certain worst-cases do exist in which devices may be operating at high power dissipation for extended periods of time. In this case, optimization of device dimensions (e.g. layout geometries) and full dynamic modeling of the device will be necessary. This work provides the foundation for this optimization and modeling.

# Chapter 6

# High-Field Effects

## 6.1 Introduction

High-field effects in MOSFETs are important because they determine the breakdown voltage and the hot carrier reliability of MOS devices which in turn govern the maximum allowable power supply voltage for a given technology. In SOI devices, high-field effects are unique because of the existence of the floating body. This leads to a reduced breakdown voltage in SOI devices as compared to their conventional bulk counterparts, as well as a more complicated evaluation of device lifetime [38,106].

Previous work in SOI hot-carrier effects have yielded conflicting results in comparisons to bulk reliability and regarding the effects of structural parameters (such as $t_{si}$) on SOI device lifetime [106-112]. This difficulty in characterizing SOI high-field effects can be partially attributed to the fact that substrate current, a

convenient monitor of electric field in bulk devices, can not be measured accurately in fully-depleted SOI. Thus, other methods are needed to understand high-field phenomena in SOI.

Previous work has measured hot-electron gate currents in p-channel SOI MOSFETs but no data on NMOSFETs were presented [113]. In this work, hot-electron gate current is measured as a function of back-gate bias, silicon film thickness, and channel doping to provide insight into the SOI lateral channel electric field in NMOSFET devices. Device degradation data is presented to verify the dependencies of electric field shown in gate currents. In addition, the interaction between the two silicon/silicon dioxide interfaces is studied in NMOSFET devices.

# 6.2 Hot-Electron Gate Current

## 6.2.1 Theory

All hot-carrier effects in MOS devices are driven by the maximum channel electric field, $E_m$. The channel field drives impact ionization which leads to substrate current; light emission; hot-electron emission in the form of gate current; and device degradation through the formation of interface states. Substrate current, $I_{sub}$ is simply measured in conventional bulk MOSFETs and thus is often used as a monitor of the device lifetime, $\tau$. Using the lucky-electron model, $I_{sub}$ and $\tau$ can be written as [114]:

$$I_{sub} = C_1 I_D \, e^{-(\phi_i / E_m q \lambda)} \tag{6.1}$$

$$\tau = C_2 \frac{W}{I_D} e^{-(\phi_{it} / E_m q \lambda)} \tag{6.2}$$

where $\lambda$ is the hot-electron mean free path, $I_D$ is the drain current, $C_1$ and $C_2$ are constants, $\phi_i$ is the minimum energy (in electron-volts) required to create impact ionization, and $\phi_{it}$ is the minimum energy required to create interface states. The maximum channel electric field, $E_m$ is given by:

$$E_m = \frac{V_D - V_{DSAT}}{l} \tag{6.3}$$

where $V_{DSAT}$ is the drain saturation voltage and $l$ is the characteristic length of the high-field region. In eqs. (6.1) and (6.2), $\phi_i/qE_m$ is the distance that an electron must travel in the field $E_m$ to gain energy $\phi_i$, and $e^{-(\phi_i/E_m q\lambda)}$ is the probability that an electron will travel that distance without an energy-losing collision. Thus, from eqs. (6.1) and (6.2), it is clear that $I_{sub}$ is correlated to $\tau$ through the exponential relationship on $E_m$.

However, $I_{sub}$ is not available in fully-depleted SOI MOSFETs because of the lack of body contact. And, even when contact to the body is available using special test structures, the resistance of the body in a fully-depleted film is quite large which limits the amount of current that can be collected [115]. As an alternative we have explored the use of hot-electron gate currents.

Hot-electron gate currents result from channel hot-electron injection. In an NMOSFET, gate current is collected when channel electrons gain enough energy from the channel electric field to surmount the Si/$SiO_2$ barrier height; and the oxide electric field in the high-field region is in a direction that is favorable for electron collection. A schematic diagram of the processes is shown in Fig. 6-1. Gate current has been modeled as the product of the probability that an electron will gain enough energy from the channel electric field to surmount the barrier and that the

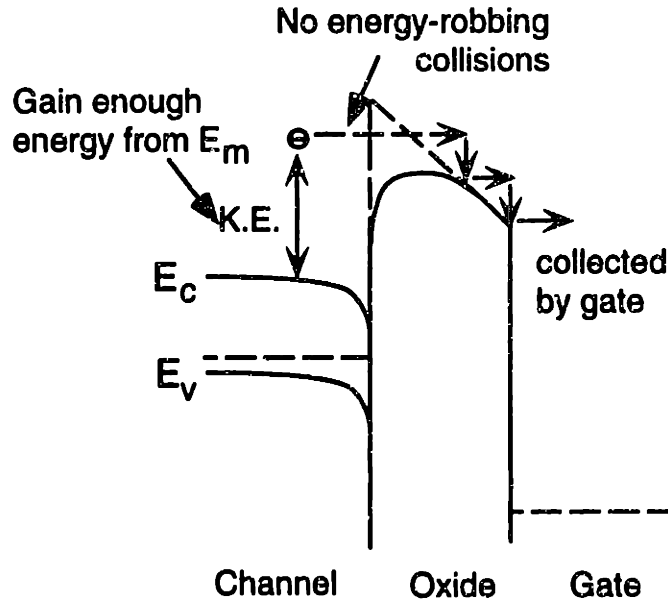


Figure 6-1: Energy band diagram at the gate-drain end of a MOSFET depicting the processes that are involved in hot-electron injection to the gate. The applied potential in this case is such that $V_G > V_D$ so that the $E_{ox}$ is in a direction favorable for electron collection.

energetic electron will be able to retain its energy as it is redirected towards the Si/SiO$_2$ interface. An approximate analytical expression has been derived by Tam et al. using the lucky electron model [116]:

$$I_G = P(E_{ox})I_D \, e^{-(\phi_b(E_{ox})/E_m q\lambda)} \tag{6.4}$$

where $E_{ox}$ is the oxide electric field at the drain end which can be approximated by $E_{ox} = \dfrac{V_G - V_D - \Phi_F}{t_{ox}}$, $\phi_b(E_{ox})$ is the oxide barrier height that is dependent on $E_{ox}$, and $P(E_{ox})$ is the probability of the electron reaching the Si/SiO$_2$ interface. It should be noted that this expression is approximate because it does not account for the fact the oxide electric field is a function of the position in the channel.

From eq. (6.4), it is clear that gate current has a similar dependence to $I_{sub}$ and $\tau$ in that all three are exponentially dependent on the channel electric field. In

bulk devices, gate current has been experimentally shown to be highly correlated with substrate current [117] and hence, should provide insight into the hot-carrier phenomena in SOI.

### 6.2.2 Experimental Devices

The devices used in this section were $n^+$-polysilicon gate, non-LDD, non-silicided nMOSFETs fabricated on SIMOX and conventional bulk substrates with the process outlined in Appendix A. Several silicon thickness ($t_{si}$=70, 100, and 180 nm) and substrate dopings ($N_a$=5x10$^{16}$, 1x10$^{17}$, and 3x10$^{17}$ cm$^{-3}$) were used, producing SOI devices ranging from partially to fully-depleted. The gate oxide thickness, $t_{ox}$, and buried oxide thickness, $t_{box}$, were 10.8 nm and 360 nm respectively. All measurements were performed on 50 µm wide devices with no contact to the substrate in SOI devices.

### 6.2.3 Gate Current Characteristics

Typical gate current characteristics for a fully-depleted SOI MOSFET and a bulk MOSFET are shown in Figs. 6-2 and 6-3. The dependences are quite similar for the two devices. Two distinct regions exist in the gate current characteristics, and can be understood from eq. (6.4). For $V_G < V_D$, although the magnitude of $E_m$ is large, the gate current is limited by the oxide electric field, because the direction of $E_{ox}$ at the gate-drain end opposes the collection of electrons at the gate. In this regime, $E_{ox}$ is favorable for the collection of holes, however, the hot-hole current is several orders of magnitude lower than the hot-electron current and is difficult to measure [118]. For $V_G > V_D$, the magnitude of $E_{ox}$ at the gate-drain end becomes favorable to the collection of electrons at the gate (as shown in the band diagram in Fig. 6-1). Electrons are then collected at the gate because the magnitude of the

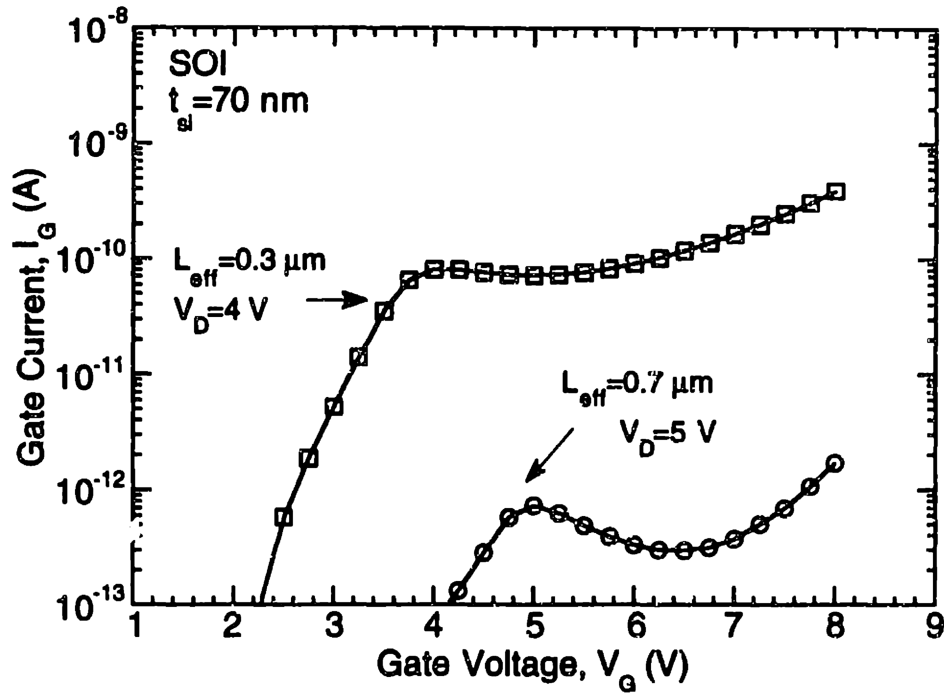


Figure 6-2: Gate current vs. gate voltage for two SOI devices with $L_{eff}$=0.7 and 0.3 µm, $t_{si}$=70 nm, $N_a$=1x10$^{17}$ cm$^{-3}$.

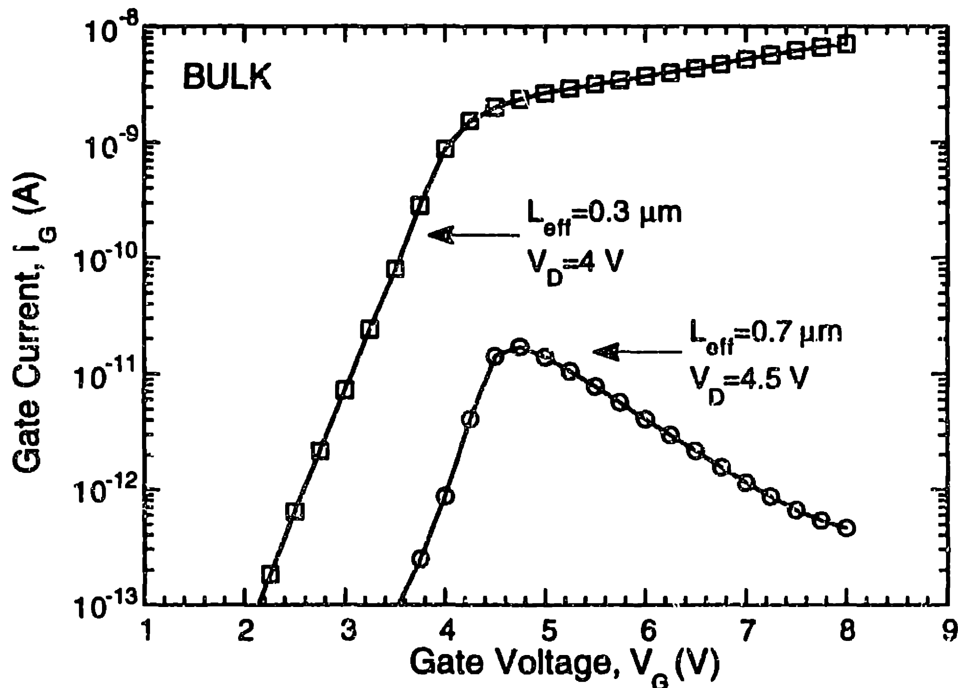


Figure 6-3: Gate current vs. gate voltage for two bulk devices with $L_{eff}$=0.7 and 0.3 µm, $N_a$=1x10$^{17}$ cm$^{-3}$.

electric field is also high. The sign of the gate current is positive, i.e. the current flows into the gate terminal because the electron flow is from channel to gate. In long-channel devices, the gate current drops as the gate voltage is further increased above the drain voltage because the device approaches the linear region of operation where the electric field is smaller.

In short-channel devices, the behavior for $V_G < V_D$ is the same as in the long-channel cases with the gate current essentially limited by $E_{ox}$ at the drain end. However, for $V_G > V_D$ the gate current is roughly constant. This behavior is consistent with reported bulk characteristics [119]. One explanation of this is that in short-channel devices and at high gate voltages, the drain current and the mobile charge in the channel is high. This can cause the mobile charge in the channel to be comparable or higher than the drain doping concentration near the channel/drain edge. This serves to extend the length of the high field region into the drain and this extension region is only weakly controlled by the gate. Thus, $E_m$ does not drop as quickly as predicted by Eq. (6.3) with increasing gate voltage, and $I_G$ remains roughly constant in short-channel devices [119].

For $V_G >> V_D$, the gate current increases again in the SOI devices. This behavior does not occur in the bulk devices and may be due to the significant self-heating that occurs in SOI devices. The channel temperature when $V_G >> V_D$ is much higher than typical operating temperatures because of the higher power dissipation. Further investigation of this phenomena is needed.

### 6.2.4 Back-gate Bias Dependence

The application of back-gate bias, $V_{BS}$, in SOI devices alters the electric field and results in significant changes in the observed gate current. The various device

Table 6-1: Back-channel charge state for various bias conditions in a fully-depleted SOI MOSFET.

| Bias Conditions | Back-Channel Charge State (at source) |
|---|---|
| $V_{BS} > V_{BT}$ | Inverted |
| $V_{BT} > V_{BS} > V_{BFB}$ | Depleted |
| $V_{BFB} > V_{BS}$ | Accumulated |

configurations are described in Table 6-1. In an NMOS device, the back-channel threshold voltage, $V_{BT}$ is in the range of 5-30 V depending on the channel doping concentration. The back-channel flatband voltage, $V_{BFB}$ is approximately 0.8 V with a p-type substrate. Gate current is observed to decrease with positive $V_{BS}$ (back-channel depletion and inversion), and increase with negative $V_{BS}$ (back-channel accumulation) as shown in Fig. 6-4. In the shorter-channel device, the effects of $V_{BS}$ are less prominent in that the range over which gate current is modulated by back-gate bias is somewhat smaller.

In Fig. 6-5, the dependence of gate current on $V_{BS}$ of a fully-depleted device is compared with a partially-depleted device ($t_{si}$=180 nm). To compare devices with different silicon thicknesses, the gate and drain voltages were normalized for the differences in parasitic source/drain resistance. For the partially-depleted device, because the back interface is decoupled from the front interface at $V_{BS}$ = 0, no modulation of the gate current is observed for back-channel accumulation. For back-channel depletion, the device depletes from the back and the dependence is similar to the fully-depleted case in that the gate current decreases with increasing positive back-gate voltage.

### 6.2.5 Drain Voltage Dependence

Figure 6-6 shows the dependence of normalized gate current on drain voltage for various fully-depleted, partially-depleted, and bulk devices. The $t_{si}$=100

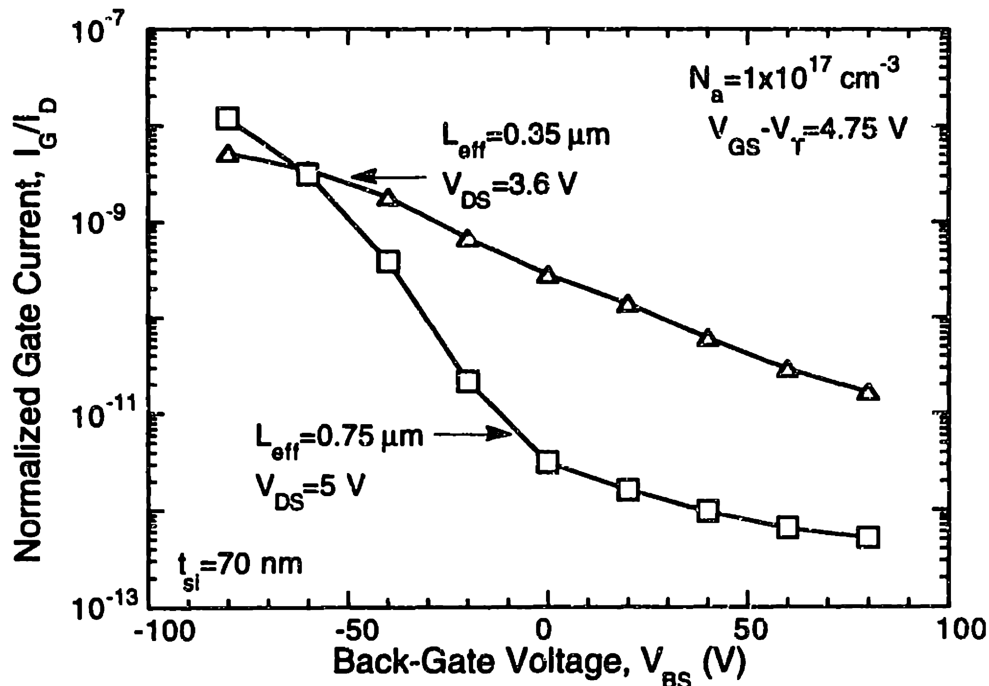


Figure 6-4: Normalized gate current vs. back-gate voltage for two different channel lengths, $L_{eff}$=0.75 and 0.35 µm, $t_{si}$=70 nm, $N_a$=1x10$^{17}$ cm$^{-3}$. Back-channel charge state for various bias conditions given in Table 6-1.

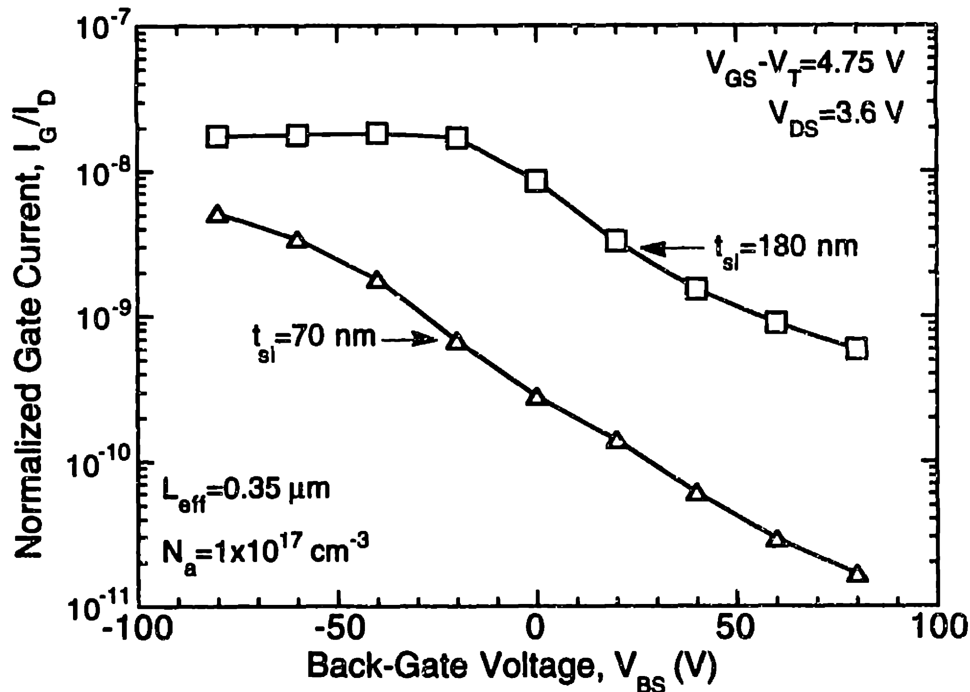


Figure 6-5: Normalized gate current vs. back-gate voltage for two different SOI film thicknesses, $t_{si}$=70 and 180 nm, $L_{eff}$=0.35 µm, $N_a$=1x10$^{17}$ cm$^{-3}$. Back-channel charge state for various bias conditions given in Table 6-1.

nm/$N_a$=3x10[17] cm[-3] device is partially-depleted, and the remainder of the SOI devices are fully-depleted. Significantly reduced gate current is observed for all SOI devices in comparison to the bulk device, with the thinnest film fully-depleted device ($t_{si}$=70 nm/$N_a$=5x10[16] cm[-3]) exhibiting the least gate current. The same trends are observed in shorter-channel length devices (Fig. 6-7); however, once again, the differences are less prominent than in the long-channel case.

### 6.2.6 Discussion

The trends observed in gate current provide insight into the behavior of SOI lateral electric field. SOI electric field has been modeled as in Eq. (6.3) where both $V_{DSAT}$ and $l$ (the characteristic length of the high-field region) are dependent on the back-channel charge condition (whether accumulated or depleted) [28,120]. The dependence of $V_{DSAT}$ and $l$ on the back-channel charge condition has been derived for long-channel SOI devices by analytical solution of Poisson's equation at both interfaces and can be expressed as [28]:

$$V_{DSAT} = \frac{V_G - V_T}{1+\alpha} \tag{6.5}$$

$$l = \left(\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox} t_{si} \frac{\beta}{2(1+\alpha)}\right)^{1/2} \tag{6.6}$$

where, $\alpha = \frac{C_{si}}{C_{ox}} = \frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox} t_{si}}$ and $\beta = 1$ for accumulation at the back interface and $\alpha = \frac{C_{si} C_{box}}{(C_{si}+C_{box}) C_{ox}} \approx 0$ and $\beta = 1 + \frac{C_{si}}{(C_{si}+C_{box})} \approx 2$ for depletion at the back interface. Note that Eq. (6.5) neglects the effects of velocity saturation that would tend to reduce $V_{DSAT}$ at short channel lengths [121].

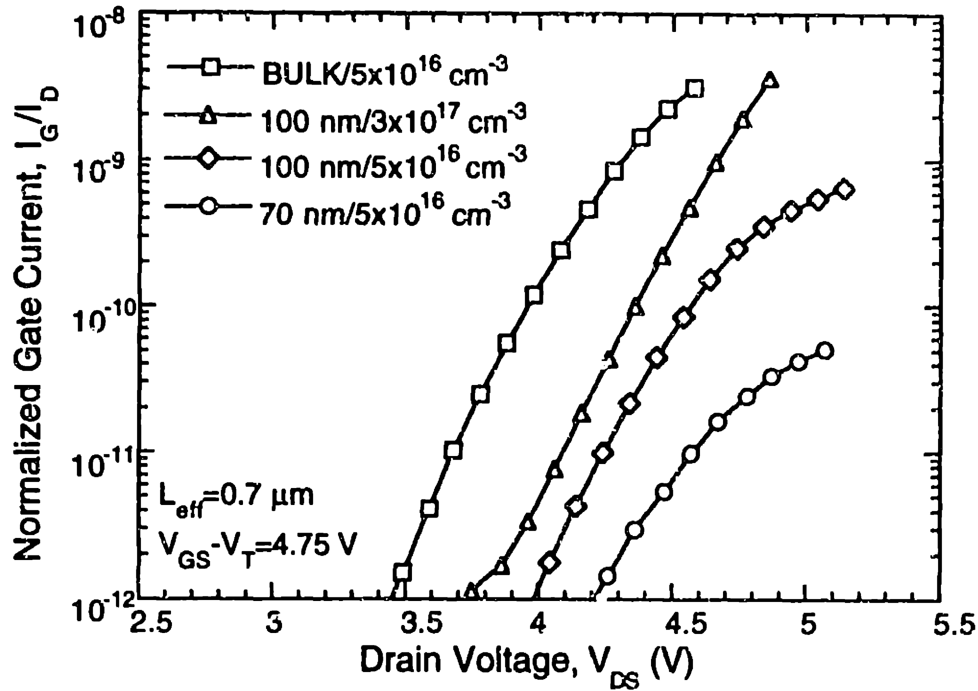


Figure 6-6: Normalized gate current vs. drain voltage for a bulk and three SOI devices with $L_{eff}$=0.7 μm. SOI $t_{si}$=100 nm/$N_a$=3x10$^{17}$ cm$^{-3}$ is partially-depleted; SOI $t_{si}$=100 nm/$N_a$=5x10$^{16}$ cm$^{-3}$ and $t_{si}$=70 nm/$N_a$=5x10$^{16}$ cm$^{-3}$ are fully-depleted.

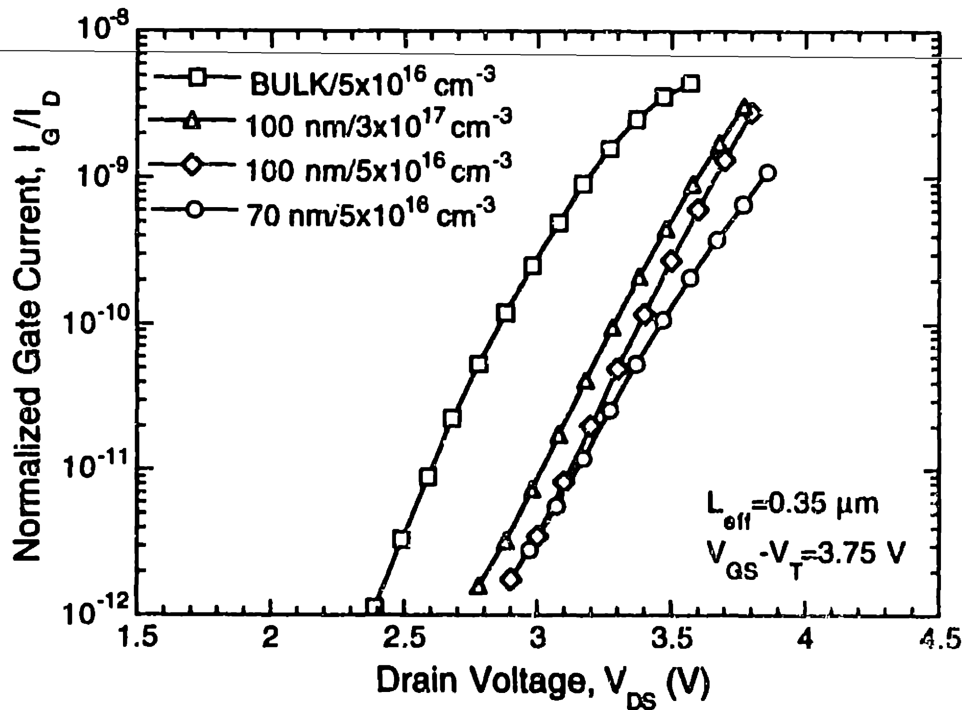


Figure 6-7: Normalized gate current vs. drain voltage for $L_{eff}$=0.35 μm. The structural parameters for the four devices are the same as in Fig. 6-6.

From eqs. (6.5) and (6.6), $V_{DSAT}$ and $l$ in fully-depleted films are increased, thereby reducing $E_m$. Physically, this is attributed to the fact that the depletion region near the drain is limited by the thickness of the silicon film whereas in bulk and partially-depleted SOI MOSFETs, the depletion region increases as one moves from the source to drain end. Because the depletion region does not increase in fully-depleted MOSFETs, the gate voltage that is needed to support the depletion charge, can be used to support additional electrons. Thus, the apparent effect is an increase in the drain saturation voltage and pinch-off region. This is another manifestation of the increased drain current phenomenon in fully-depleted devices that has been reported for fully-depleted devices [29,30].

As the device approaches either strong accumulation or strong inversion, the accumulation or inversion regions decouple the front and back interfaces. Thus, the gate current begins to saturate. Note that the saturation of the gate current occurs considerably after the onset of strong accumulation or inversion as defined at low drain bias or near the source. This saturation is gradual because the front-gate has strong control in the high-field region and tends to keep that region depleted although the portion of the channel near the source may be accumulated or inverted.

Changing the film thickness (from 70 nm to 180 nm in Fig. 6-5) or the substrate doping (from $t_{si}$=100 nm/$N_a$=5x10$^{16}$ cm$^{-3}$ to 3x10$^{17}$ cm$^{-3}$ in Fig. 6-6) results in a transition from full to partial depletion. Thus, the front and back gates are less coupled and resemble the case of back-channel accumulation. This results in increased gate current and an increased drain electric field. MINIMOS5 simulations are shown in Fig. 6-8 to verify the dependence of lateral electric field on the substrate doping and silicon film thickness.

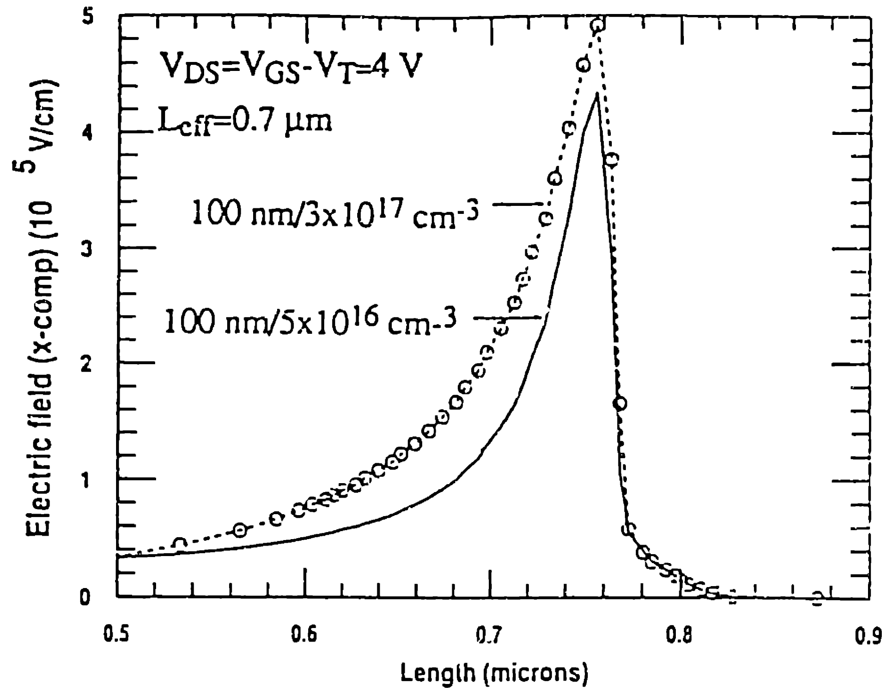


Figure 6-8: MINIMOS5 simulations of the lateral electric field at the surface in a fully-depleted ($t_{si}$=100 nm, $N_a$=1x0$^{17}$ cm$^{-3}$) and a partially-depleted SOI MOSFET ($t_{si}$=100 nm, $N_a$=3x10$^{17}$ cm$^{-3}$) for $L_{eff}$=0.7 µm.

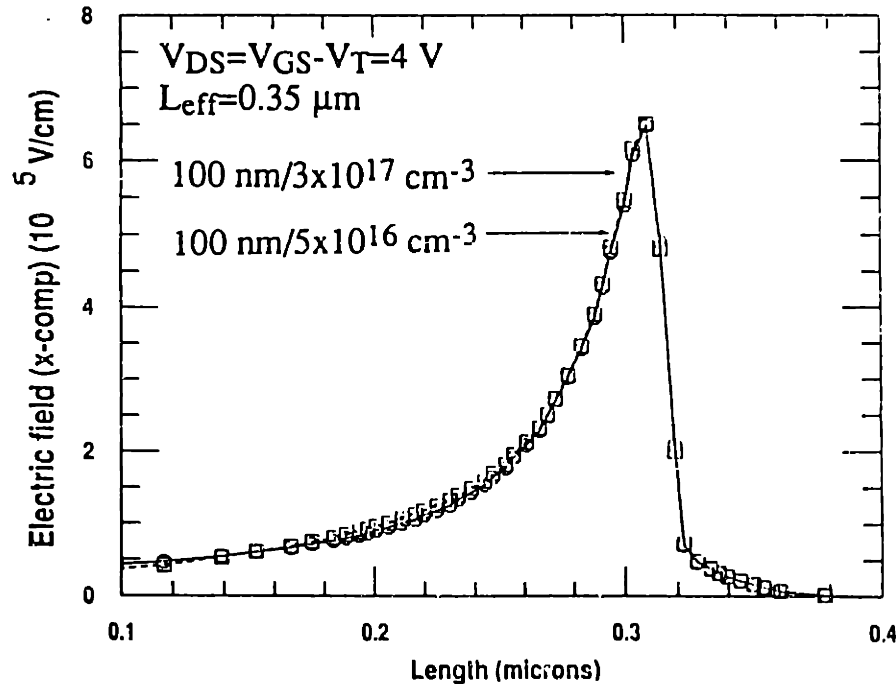


Figure 6-9: MINIMOS5 simulations of the lateral electric field at the surface in a fully-depleted ($t_{si}$=100 nm, $N_a$=1x0$^{17}$ cm$^{-3}$) and a partially-depleted SOI MOSFET ($t_{si}$=100 nm, $N_a$=3x10$^{17}$ cm$^{-3}$) for $L_{eff}$=0.35 µm.

As channel lengths are shortened, the effects of back-gate bias and full-depletion are weakened because $V_{DSAT}$ is dominated by velocity saturation effects [121]. Thus, the dependence of gate current on these parameters is reduced in the 0.35 μm devices in Fig. 6-7. Simulations of the electric field shown in Fig. 6-9 also verify that the electric fields of partially and fully-depleted devices are much closer in short-channel devices.

For devices that are fully-depleted, the data show a reduction in gate current with thinner silicon films. This suggests a further reduction in electric field and is in agreement with other experiments [109]. However, earlier analytical modeling and simulations using the local-field model predicted an increase in electric field for decreasing silicon thickness [45,120,122].

Based on this and other experimental data, recent work has suggested that this discrepancy is due to the highly peaked nature of the electric field in thin silicon films, i.e. the increased gradient of the electric field as the silicon film is thinned. The large gradient causes the carriers to be swept out of the high field region before a steady-state temperature can be reached. Omura et al. [109] and recent work by Krishnan and Fossum [123] have shown that using non-local analytical modeling and two-dimensional simulation of the carrier temperature in thin-film SOI, the qualitative silicon film thickness dependence shown in the gate current data can be explained.

This is a significant result for the scaling of SOI films because it was previously believed that scaling silicon film thickness would degrade the hot-carrier reliability which would limit the device design options.

# 6.3 Hot-Electron Degradation

## 6.3.1 Degradation Characteristics

Hot-electron degradation experiments were performed to provide further insight into hot-carrier phenomena and verify some of the trends observed in gate currents. Various combinations of stress and measurement conditions were used to determine the worst-case stress conditions, the front and back-channel degradation characteristics, and the primary area of damage. Both the front and back-channel characteristics were monitored in most cases. Table 6-2 outlines the stress and measurement conditions that were used.

The worst-case stress conditions were determined by stressing a representative set of fully-depleted devices as a function of $V_{GS}$-$V_T$. The linear current degradation was monitored at $V_{GS}$-$V_T$=1 V and $V_{DS}$=0.05 V for the front-gate transistor, and $V_{BS}$-$V_{BT}$=30 V and $V_{DS}$=0.05 V for the back-gate transistor (condition 1 in Table 6-2). The drain voltage during stress was chosen to obtain measurable degradation for a stress time of 1 hour without operating in the heavy avvalanche regime. This was also aided by choosing measurement conditions for the front and back-gate transistor at a relatively low $E_{eff}$ so that the percentage degradation would be greater. Thus, the absolute amount of degradation for the devices measured here are somewhat high. The data presented here are most useful for understanding the qualitative dependencies of degradation.

As shown in Fig. 6-10, the most severe degradation occurs for small $V_{GS}$-$V_T$ (~0.15 V). The threshold voltage in this case is defined as the extrapolated threshold voltage at low $V_{DS}$. The severe degradation at low gate voltages is caused

Table 6-2: Stress and measurement conditions used in hot-electron degradation experiments.

| | Stress Conditions | Front-Channel Measurement | Back-Channel Measurement | Comments |
|---|---|---|---|---|
| 1 | $V_{DS}$ high<br>$V_{GS}$-$V_T$ var.<br>$V_{BS}$=0 V | $V_{DS}$=0.05 V<br>$V_{GS}$-$V_T$=1 V<br>$V_{BS}$=0 V | $V_{DS}$=0.05 V<br>$V_{BS}$-$V_T$=30 V<br>$V_{GS}$=0 V | Determine worst-case stress conditions |
| 2 | $V_{DS}$ high<br>$V_{GS}$-$V_T$=0.15 V<br>$V_{BS}$=0 V | $V_{DS}$=0.05 V<br>$V_{GS}$-$V_T$=1 V<br>$V_{BS}$=0 V | $V_{DS}$=0.05 V<br>$V_{BS}$-$V_T$=30 V<br>$V_{GS}$=0 V | Measure linear current degradation characteristics under "typical" bias conditions |
| 3 | $V_{DS}$ high<br>$V_{GS}$-$V_T$=0.15 V<br>$V_{BS}$=10 V | $V_{DS}$=0.05 V<br>$V_{GS}$-$V_T$=1 V<br>$V_{BS}$=0 V | $V_{DS}$=0.05 V<br>$V_{BS}$-$V_T$=30 V<br>$V_{GS}$=0 V | Vary the peak electric field through the back-gate bias to verify $I_G$ dependencies, measurement conditions typical |
| 4 | $V_{DS}$ high<br>$V_{GS}$-$V_T$=0.15 V<br>$V_{BS}$=-10 V | $V_{DS}$=0.05 V<br>$V_{GS}$-$V_T$=1 V<br>$V_{BS}$=0 V | $V_{DS}$=0.05 V<br>$V_{BS}$-$V_T$=1 V<br>$V_{GS}$=0 V | Vary the peak electric field through the back-gate bias to verify $I_G$ dependencies, measurement conditions typical |
| 5 | $V_{DS}$ high<br>$V_{GS}$-$V_T$=0.15 V<br>$V_{BS}$=10 V | $V_{DS}$=0.05 V<br>$V_{GS}$-$V_T$=1 V<br>$V_{BS}$=-20 V | $V_{DS}$=0.05 V<br>$V_{BS}$-$V_T$=1 V<br>$V_{BS}$=-3 V | Monitor degradation with decoupled front and back interfaces to determine location of degradation |

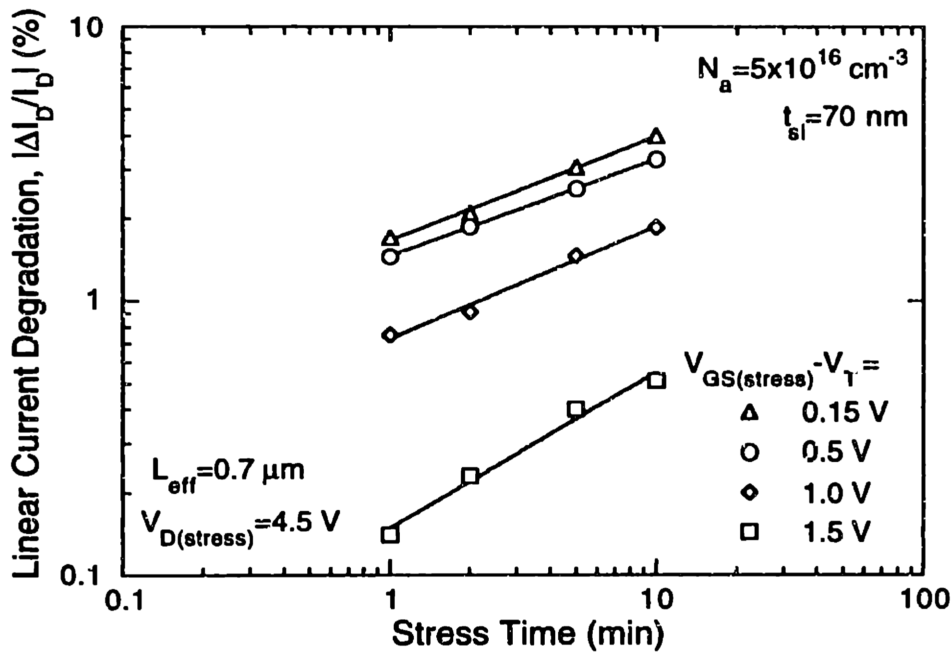


Figure 6-10: Linear current degradation vs. stress time for several different gate biases, $L_{eff}$=0.7 μm, $t_{si}$=70 nm, $N_a$=5x10$^{16}$ cm$^{-3}$. Note that peak degradation occurs at low gate voltage, $V_{GS}$-$V_T$=0.15 V.

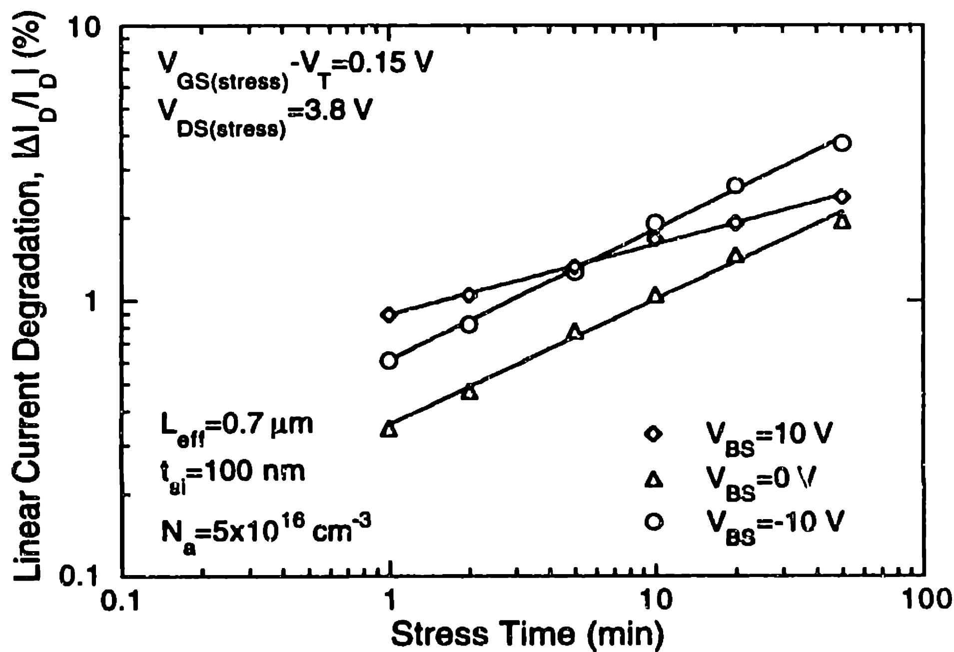


Figure 6-11: Linear current degradation vs. stress time for a fully-depleted device as a function of back-gate bias, $L_{eff}$=0.7 μm, $t_{si}$=100 nm, $N_a$=5x10$^{16}$ cm$^{-3}$.

by the parasitic bipolar effect which amplifies impact ionization current and causes premature breakdown in SOI devices [38,124]. This is in contrast to conventional bulk devices, for which peak degradation usually occurs at $V_{GS}=V_{DS}/2$. This behavior has also been reported by Acovic et al. [125]. For all of the remaining degradation experiments, the devices are stressed at the worst-case degradation of $V_{GS}-V_T=0.15$ V.

In Fig. 6-11, SOI front-gate linear current degradation is measured as a function of back-gate bias. When the back channel is accumulated (condition 4 in Table 6-2) during stress, degradation increases as compared to the zero bias case. However, when the device is stressed with the back channel in depletion (positive back-gate bias, condition 3 in Table 6-2), the degradation slope changes. More initial degradation is observed, but with a weaker time dependence.

Figure 6-12 shows the corresponding linear current degradation when the back-gate transistor characteristics are monitored (same devices as in Fig. 6-11). Similar to the front-channel characteristics, the back-gate transistor exhibits significant initial degradation for positive back-gate bias. For the back channel accumulated and the zero back-gate bias case, the amount of degradation at the back interface is significantly smaller.

To investigate the true degradation at the front interface due to the electric field, the influence of the back interface degradation must be decoupled from the front interface degradation. This can be done by stressing under the same conditions but monitoring the degradation with the back interface in accumulation (condition 5 in Table 6-2). By accumulating the back interface, any degradation that has occurred at that interface will be masked and will not influence the front interface characteristics. It should be noted that when accumulating the back interface, the threshold voltage of the device is increased substantially. To make

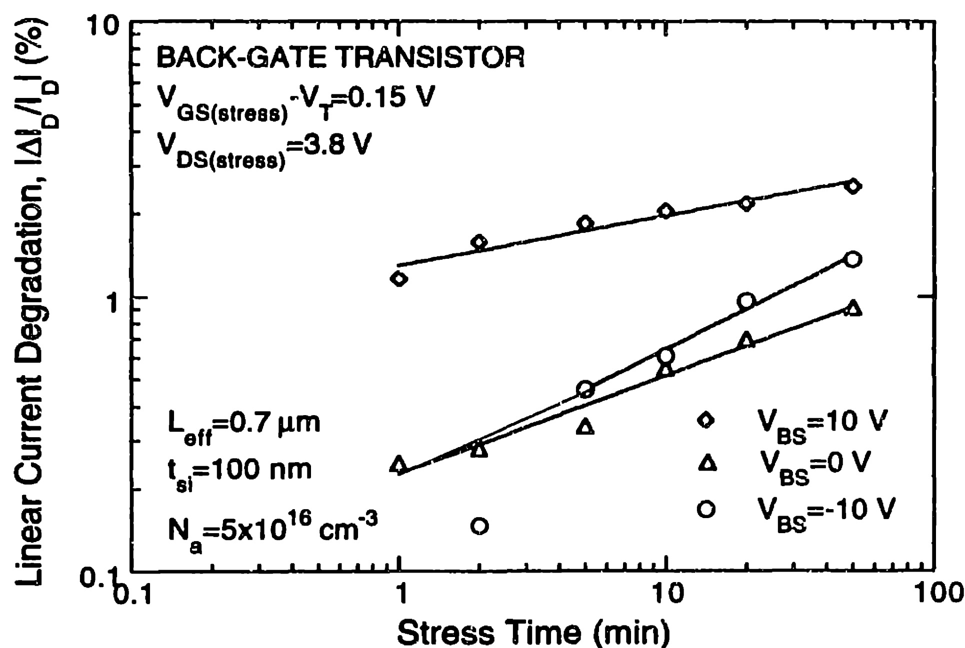


Figure 6-12: Back-transistor linear current degradation vs. stress time as a function of back-gate bias for $L_{eff}$=0.7 μm, $t_{si}$=100 nm, and $N_a$=5x10$^{16}$ cm$^{-3}$.

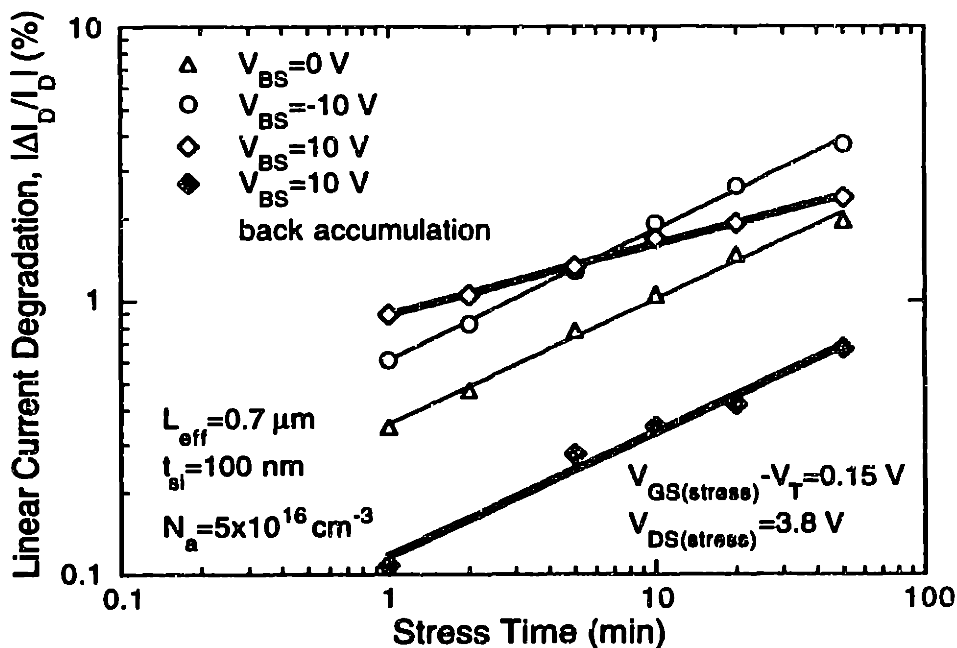


Figure 6-13: Linear current degradation vs. stress time for a fully-depleted device as a function of back-gate bias, $L_{eff}$=0.7 μm, $t_{si}$=100 nm, $N_a$=5x10$^{16}$ cm$^{-3}$. In the heavy solid line, degradation for $V_{BS}$=10 V is monitored with the back channel in accumulation. The measurement conditions are adjusted to the same $V_{GS}$-$V_T$.

fair comparisons of the amount of degradation, the measurement condition of $V_{GS}$-$V_T$ must be kept constant where $V_T$ is the threshold voltage at the appropriate back-gate bias.

Figure 6-13 shows the same data in Fig. 6-11 with the degradation also monitored with the back channel in accumulation for the $V_{BS}$=10 V case. As shown when the degradation is monitored with the back channel in accumulation, the larger initial degradation disappears and the slope of the time dependence is now parallel to the time dependence of the other two cases. This is a clear indication that the cause of the larger initial degradation and reduced time dependence was due to degradation of the back-channel transistor influencing the front channel characteristics through interface coupling. This effect has also been observed by Yoshino et al. [126] and Cristoloveanu et al. [127] when the back-gate transistor of SOI MOSFETs was intentionally stressed. For $V_{BS}$=0 V and -10 V, there is no difference in the degradation when it is monitored with the back channel in accumulation or depletion. This indicates that in those two cases, the degradation is primarily at the front, and the back-channel degradation is not playing a significant role.

Comparing the hot-electron degradation data of devices with various structural parameters, Fig. 6-14 shows front-gate linear current degradation (condition 2 in Table 6-2) for a partially-depleted ($t_{si}$=100 nm, $N_a$=3x10$^{17}$ cm$^{-3}$) and two fully-depleted devices ($t_{si}$=100 nm and 70 nm, $N_a$=5x10$^{16}$ cm$^{-3}$). The partially-depleted case shows increased degradation as compared to the fully-depleted ones. For the two fully-depleted devices, there is no significant difference between the two silicon film thicknesses.

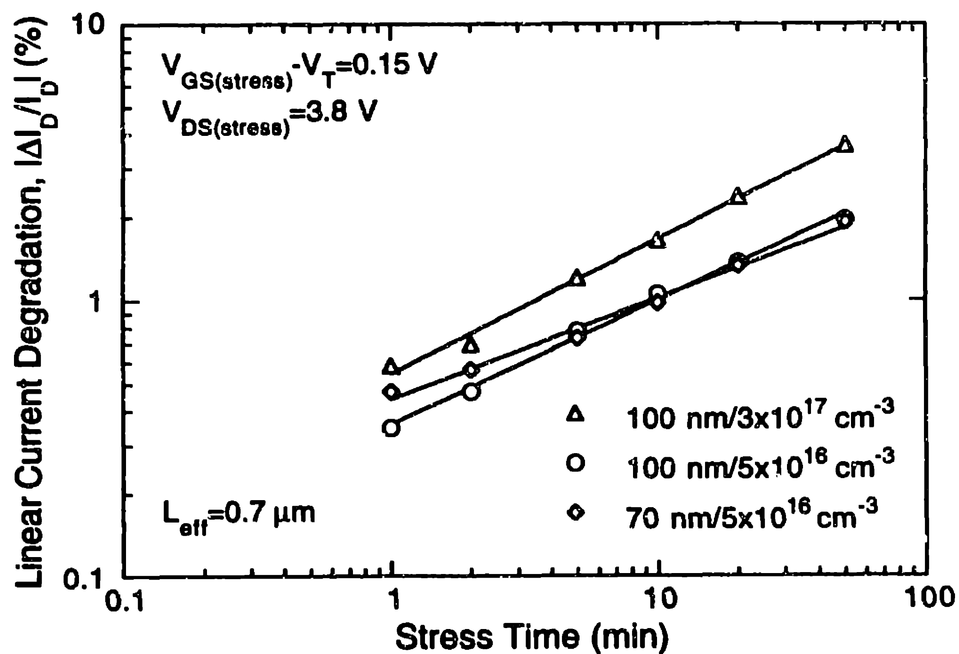


Figure 6-14: Linear current degradation vs. stress time for a partially-depleted device ($t_{si}$=100 nm, $N_a$=3x$10^{17}$ cm$^{-3}$) and two fully-depleted devices ($t_{si}$=100 and 70 nm, $N_a$=5x$10^{16}$ cm$^{-3}$).

### 6.3.2 Discussion

The observed dependencies of the hot-electron degradation on back-channel accumulation and partial depletion are in good agreement with the trends shown in gate current. In both of these cases, the primary degradation occurs at the front interface and any degradation at the back interface does not significantly affect the front-channel characteristics.

For back-channel depletion, significant degradation occurs at the back interface from the subthreshold or weak-inversion current. This damage is then reflected in the front-channel characteristics because the front and back interfaces are coupled in fully-depleted devices. This is illustrated by the change in the slope of the time dependence of the degradation.

To properly model and understand the device degradation characteristics and dependencies, the degradation at the front and back interface must be decoupled. One method for doing so is to monitor the degradation with the opposite interface in accumulation to mask the damage. When this is done, it is shown that the degradation when the back channel is depleted is significantly lower than for the zero back-gate bias case and the back channel in accumulation. This is in good agreement with the trends observed in gate currents.

It should be noted though that transistors would not normally operate with positive bias at the back-gate, thus the degradation of the back-channel transistor biased in this configuration is not necessarily a significant problem. For all of the transistors biased at zero back-gate bias, including thin silicon films ($t_{si} \approx 50$ nm), there was no evidence that back-channel degradation influenced the front-channel characteristics, i.e. there was no difference between linear current degradation that was measured with the back-channel in accumulation or depletion. It has been reported that the influence of the back-channel transistor is more significant in

PMOS devices because they tend to be forward-biased on a p-substrate. If this is the case, there would be some concern from the process control standpoint because the degradation of the back-channel transistor would be greatly affected by the back-interface material quality. However, typically PMOS transistors are much less susceptible to hot-carrier degradation because of the lower hole mobility. Nevertheless, this issue still needs to be verified and further understood.

Finally, the degradation of fully-depleted films showed a very weak dependence on silicon film thickness. However, the gate current data suggested a significant reduction in electric field as $t_{si}$ is decreased. These data are not necessarily in contradiction because hot-electron degradation is a sensitive function of many other parameters. Further work to examine the degradation mechanisms in SOI as a function of silicon film thickness and other structural parameters is needed.

Because of the questions that still remain regarding the degradation mechanisms in SOI, there was no attempt to compare bulk and SOI reliability in this work.

## 6.4 Summary and Conclusions

This work produced the first experimental data showing the dependencies of gate current in SOI NMOSFETs as a function of back-gate bias and structural parameters. It was shown that hot-electron gate current is a good indicator of SOI channel electric field. The electric field is increased with back-channel accumulation and partial depletion, and decreased for back-channel depletion, fully-depleted devices, and thin silicon films. Hot-electron degradation experiments verified most of the dependencies in gate current. This indicates that gate current can potentially be a monitor of device degradation in fully-depleted SOI devices.

However, the device degradation in fully-depleted SOI devices is more complicated than in bulk devices because of the existence of two $Si/SiO_2$ interfaces at which degadation can occur. To model and understand the device degradation behavior, it is important that the degradation at each interface be decoupled. This can be done by monitoring the degradation with the opposite interface in accumulation to screen out any damage that may be present at that interface. For devices under regular bias conditions, there is no apparent influence of back-channel degradation on the front-channel characteristics.

Based on the qualitative results and trends of this work, recent data by another group has indeed shown that gate current can serve as a monitor of hot-electron degradation in SOI NMOS devices [128]. However, clearly additional work into the degradation mechanisms and the influence of the back-interface material quality is still needed to fully understand the hot-carrier phenomena in SOI. Once the degradation mechanisms in SOI are fully understood, a "fair" comparison between bulk and SOI device degradation can be done.

# Chapter 7

# Performance Comparison

## 7.1 Introduction

In the preceding four chapters, some of the intrinsic device issues surrounding SOI technologies were examined in comparison to bulk technologies to gain an understanding of the device physics and in some cases propose solutions to improve the state-of-the-art of SOI technology. The final topic to be discussed is a comparison of performance aspects of the two technologies.

There have been countless studies examining the performance of both bulk and SOI MOSFETs in the deep-submicrometer region [78-83,129,130]. Typically, the goal of most of these studies has been to achieve the highest device performance, i.e. transconductance and current drive. However, equally important to device performance is the magnitude of the short-channel effect which directly translates into off-state leakage current. Although there have also been numerous

studies of MOSFET scaling that have focused on the preservation of the device electrostatic integrity (as in [7,8,131,132] and Chapter 3), the relationship between performance and short-channel effects is not usually made explicit. When comparing two different technologies (e.g. bulk and SOI) or even when considering various design options in a given technology (e.g. channel engineering options), it is important to explicitly consider the tradeoffs of both performance and short-channel effects in the device design.

In this work, a methodology is presented that allows the direct comparison of the performance in bulk and SOI technologies as well as an evaluation of the various design options available in both. This methodology was first used to compare our extreme-submicrometer 0.1 μm bulk technology fabricated by x-ray lithography [82] with the published literature and is particularly useful for examining the *intrinsic* performance of devices.

The key design variables that are examined are (1) channel design: gate oxide thickness, $t_{ox}$; threshold voltage, $V_T$; and channel doping profile, $N_a$; and (2) source/drain design: junction depth, $x_j$, or silicon thickness, $t_{si}$; parasitic resistance, $R_{sd}$; and junction abruptness ("halo" structure). Bulk and SOI NMOSFETs with a wide range of the above parameters were used to study the tradeoffs between the short-channel effect and performance experimentally. The measures of short-channel effect that are used are the threshold voltage shift due to drain-induced barrier lowering (DIBL) and the off-state leakage current ($V_D$=1 or 2 V, $V_G$=0 V). The measures of performance are peak saturation current, $I_D$ @ $V_G$=$V_D$=1 or 2 V and peak saturated transconductance, $g_m$.

It should be noted though that this study focuses on the intrinsic performance. In a full evaluation of a technology, short-channel effects and current drive are not the only two important figures-of-merit but issues such as hot-carrier

reliability and cost are also extremely important. These are discussed further in section 7.6.

## 7.2 Experimental Devices

The experimental devices used in this chapter include bulk and SOI devices over a wide range of device parameters. The uniformly-doped bulk devices were all fabricated during the same process runs as the SOI devices using variations of the process flow in Appendix A. The devices with super-steep retrograde channel doping were fabricated in a separate experiment by H. Hu [82]. In most cases, the devices were silicided using the process described in Chapter 4. The effective channel length and parasitic series resistance were measured using the technique in [43,44]. The doping concentration was estimated from SUPREM3 simulations of the process flow. In the performance comparison, directly measured transconductance normalized for device width, $g_m/W$ was used whenever possible. However, when comparing devices with different gate oxide thicknesses, the intrinsic speed, $g_m/WC_{ox}$ was used. The gate oxide thickness that was used for normalization of the transconductance was measured experimentally on large devices (50 μm x 50 μm). The effective width was determined by using the ratios of the transconductances in the linear region for a $W$=50 μm device and the test device. For the devices in section 7.3, the device transconductance is measured at the peak in saturation for a drain voltage of 2 V. For the SOI data in section 7.4 and the comparison of bulk to SOI in section 7.5, the device transconductance is measured at the peak in saturation for a drain voltage of 1 V to minimize the self-heating effects. As discussed in Chapter 5, the self-heating effect will not be present under most circuit operating conditions. Hence, to evaluate the intrinsic device performance the self-heating effect should be minimized.

# 7.3 Bulk MOSFET Performance

## 7.3.1 Channel Design

Figures 7-1 and 7-2 show the threshold voltage shift due to DIBL vs. $L_{eff}$ for several uniform doping concentrations. From classical scaling theory [131], it is well-known that increasing $N_a$ and decreasing $t_{ox}$ reduces DIBL. However, increasing the surface impurity concentration reduces the inversion-layer mobility [133]. The inversion-layer mobility can be expressed as a universal function of the effective vertical electric field at the interface which for electrons is defined by [134]:

$$E_{eff} = \frac{Q_B + 0.5Q_n}{\varepsilon_{si}} \tag{7.1}$$

where $Q_B$ is the depletion charge given by $qN_ax_d$ and $Q_n$ is the inversion charge which can be approximated by $C_{ox}(V_G\text{-}V_T)$. Thus, when $N_a$ is increased, the effective vertical field is increased, which decreases the mobility. Even though short-channel devices show significant effects of velocity saturation, the low-field mobility is still an important contributing factor to the performance [135]. Figure 7-3 shows the measured saturated $g_m/W$ vs. $L_{eff}$ for several doping concentrations. As shown, the $g_m/W$ can indeed be observed to decrease with increasing doping concentration.

Figure 7-4 shows the measured saturated $g_m/W$ vs. $L_{eff}$ for several gate oxide thicknesses. As $t_{ox}$ is decreased, $g_m/W$ is increased, but in a circuit, this is accompanied by an increase in gate capacitance of the next stage that is being driven. When transconductance is normalized by the gate oxide capacitance,

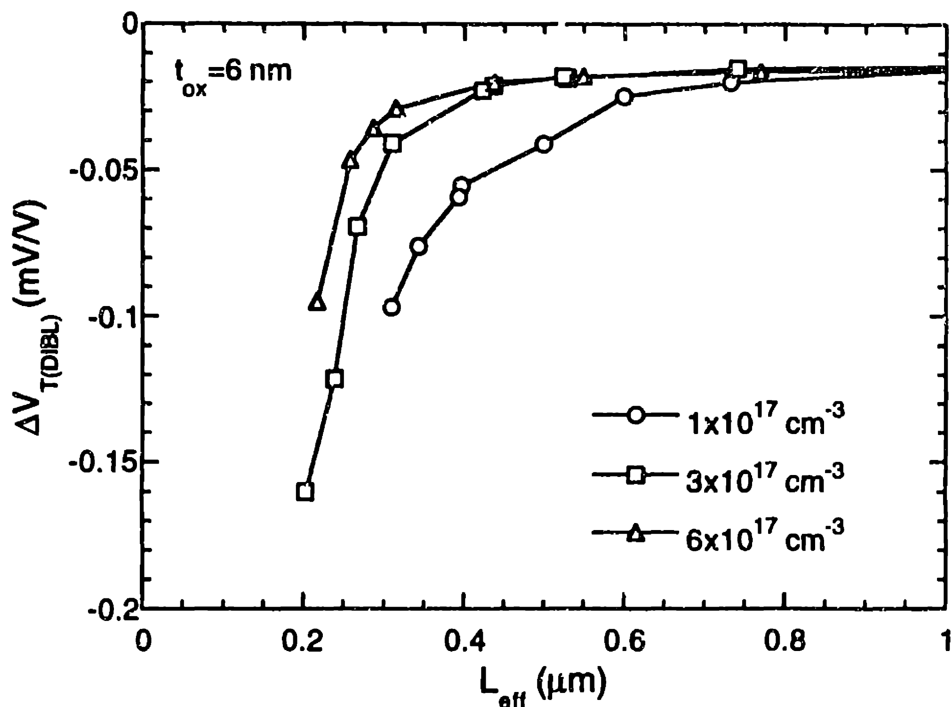


Figure 7-1: Drain-induced barrier lowering, $\Delta V_{T(DIBL)}$ vs. $L_{eff}$ for several uniform doping concentrations in bulk devices ($t_{ox}$=6 nm).

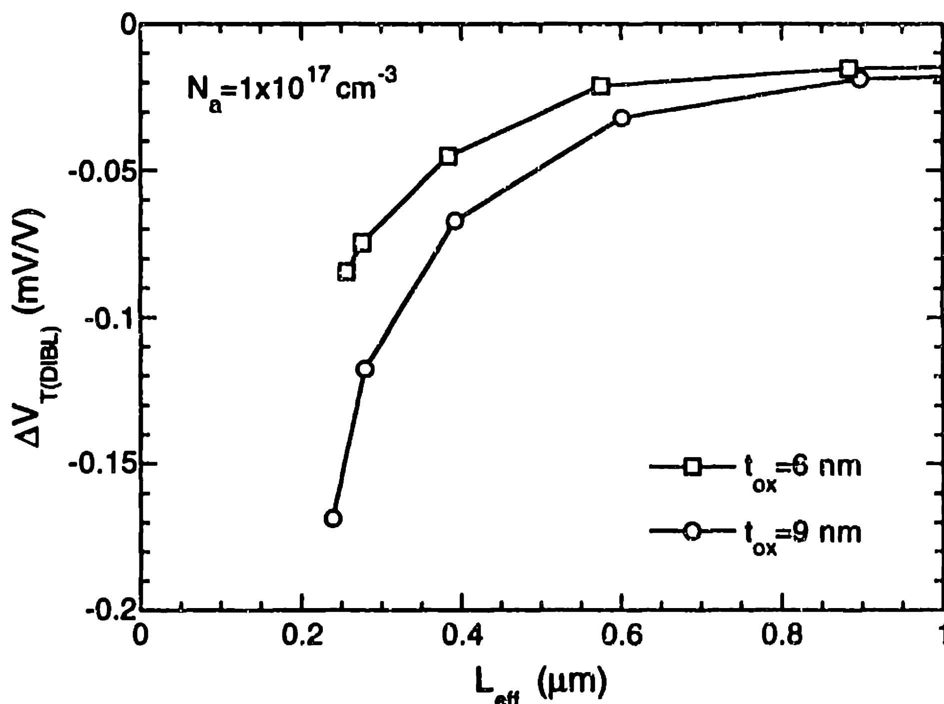


Figure 7-2: Drain-induced barrier lowering, $\Delta V_{T(DIBL)}$ vs. $L_{eff}$ for two gate oxide thicknesses in bulk devices ($N_a$=1x10$^{17}$ cm$^{-3}$).

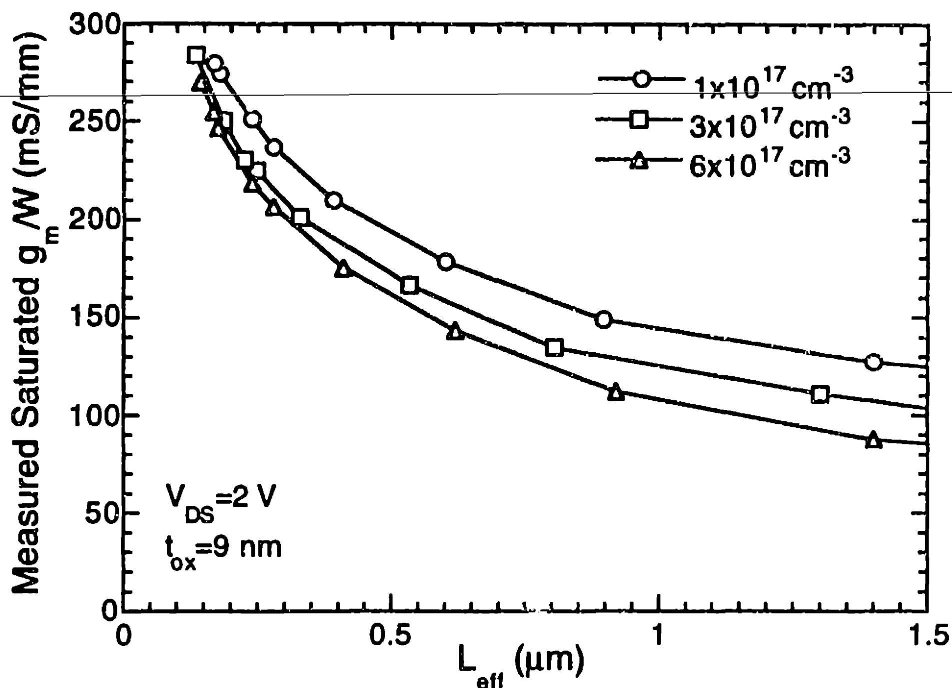


Figure 7-3: Measured saturated transconductance, $g_m/W$ vs. $L_{eff}$ for several doping concentrations in bulk devices ($t_{ox}$=9 nm, $V_{DS}$=2 V).

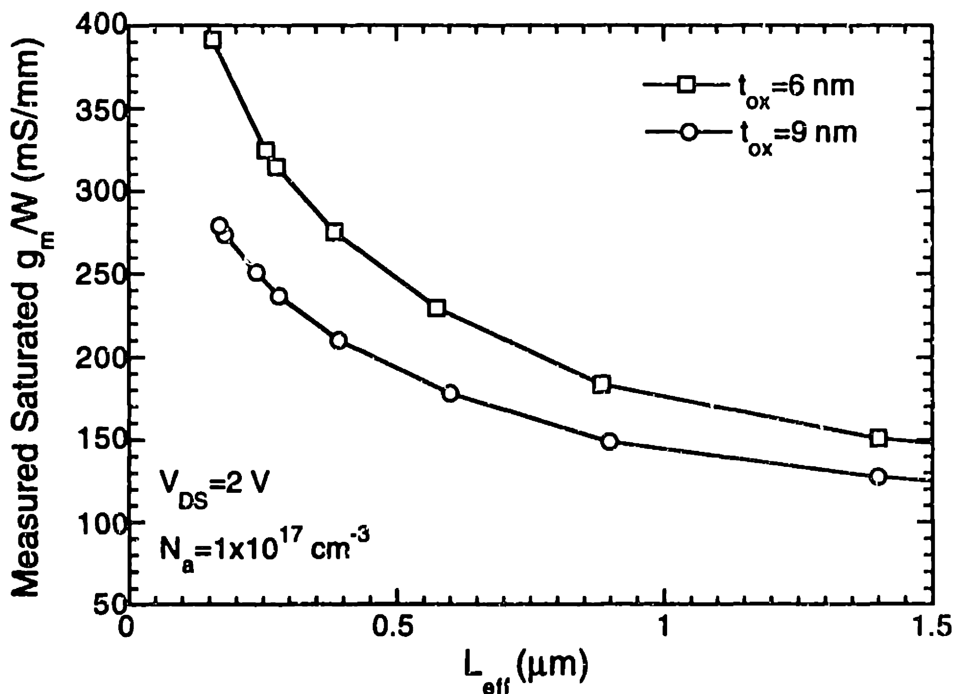


Figure 7-4: Measured saturated transconductance, $g_m/W$ vs. $L_{eff}$ for two gate oxide thicknesses in bulk devices ($N_a$=1x10$^{17}$ cm$^{-3}$, $V_{DS}$=2 V).

$g_m/WC_{ox}$, this is often referred to as the intrinsic device speed and is a good measure of the intrinsic driving capability over a range of gate oxide thicknesses.

To compare the tradeoff between performance and short-channel effects for the various $N_a$ and $t_{ox}$, the $g_m/W$ and $g_m/WC_{ox}$ can be plotted directly vs. DIBL as shown in Figs. 7-5 and 7-6. Plotting these quantities directly against each other is advantageous because only measured quantities are used, thus inaccuracies in $L_{eff}$ extraction do not confuse the interpretation.

Notice that examining both the $t_{ox}$ and $N_a$ dependence, there is a somewhat universal relationship between the performance measured by transconductance or intrinsic speed and DIBL. The universality with respect to $N_a$ is somewhat unexpected but can be understood because although the DIBL is reduced by increasing $N_a$, the mobility is also reduced which decreases $g_m$.

For the $t_{ox}$ dependence, decreasing $t_{ox}$ reduces DIBL. However, from eq. (7.1), the effective vertical field at the interface is increased when the gate oxide thickness is decreased through the inversion charge, $Q_n$ term. Thus, when $g_m/W$ is normalized for gate oxide capacitance, the mobility is reduced due to an increase in the vertical field. This explains the universality of the $g_m/WC_{ox}$ vs. DIBL dependence with respect to $t_{ox}$.

These results suggest that although varying $N_a$ and $t_{ox}$ will result in a large range of $V_T$'s and device architectures, the intrinsic device performance tradeoff is not substantially affected. Note that the $L_{eff}$ values along each of the curves in Figs. 7-5 and 7-6 are different although when normalized for a given DIBL, the intrinsic performance is universal.

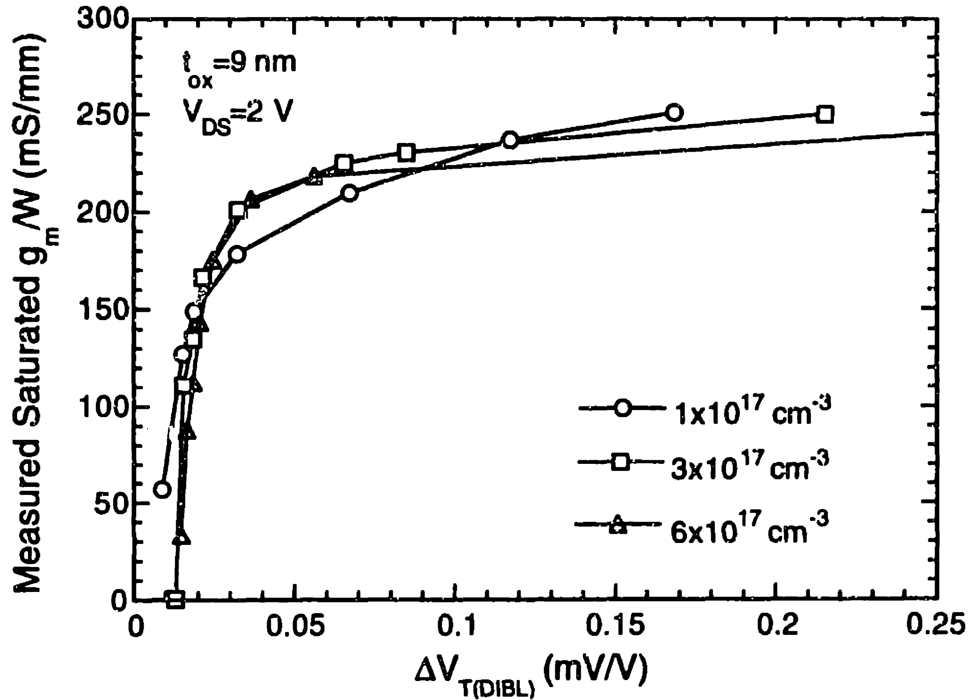


Figure 7-5: Measured saturated transconductance, $g_m/W$ vs. drain-induced barrier lowering, $\Delta V_{T(DIBL)}$ for several uniform doping concentrations in bulk devices ($t_{ox}$=9 nm, $V_{DS}$=2 V).

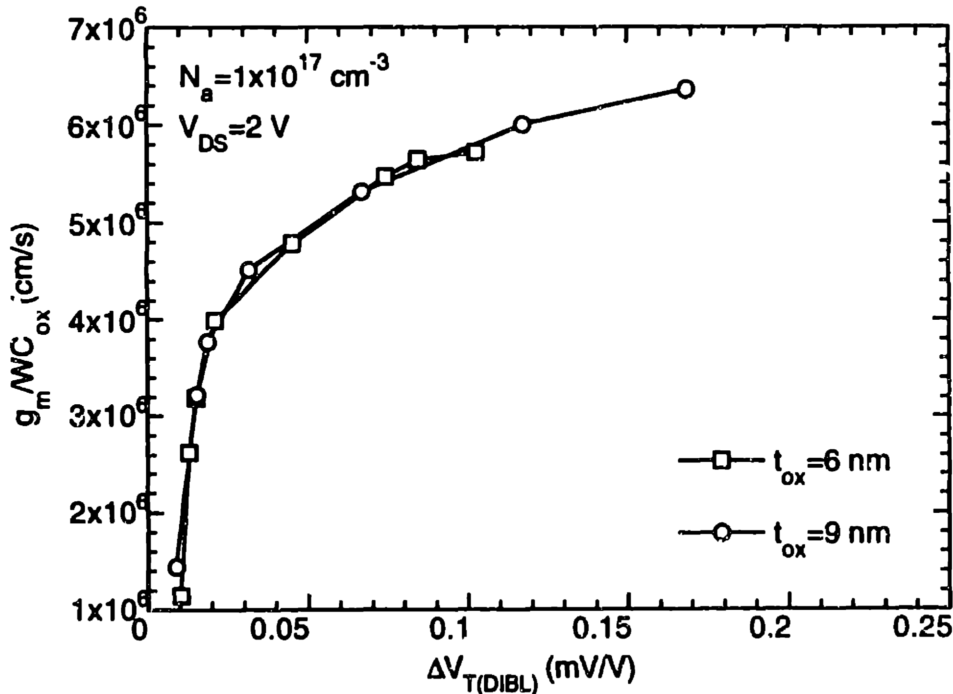


Figure 7-6: Intrinsic speed, $g_m/WC_{ox}$ vs. drain-induced barrier lowering, $\Delta V_{T(DIBL)}$ for two gate oxide thicknesses in bulk devices ($N_a$=1x$10^{17}$ cm$^{-3}$, $V_{DS}$=2 V).

### 7.3.2 Source/Drain Design

The other major device design option is the source/drain technology. The problem with the channel design optimization, was that given the options, the DIBL could not be improved without adversely affecting performance and vice versa. On the other hand, source/drain technology potentially provides an independent means to reduce short-channel effects.

One option that has been discussed in the literature is the use of a halo region around the source and drains to reduce drain-induced barrier lowering and punchthrough [136]. The halo is a counter-doping implant around the source and drain of a device that serves to localize the depletion regions. Various fabrication methods for this halo have been suggested including large-angle tilt implants [136]. Recent work has shown that the use of a source/drain halo in 0.1 μm devices formed by indium and antimony implant in NMOS and PMOS respectively can be very beneficial in reducing short-channel effects. Because indium and antimony are relatively heavy ions, they serve to pre-amorphize silicon and hence lead to shallow junction formation as well as to the formation of a thin halo of increased substrate doping around the source and drains [81, 137].

Figures 7-7 and 7-8 show the $g_m/W$ and $g_m/WC_{ox}$ vs. DIBL tradeoff for devices with and without halo doping. As shown in Fig. 7-7, unlike the channel variables, the use of a halo around the source/drain significantly improves the $g_m/W$ vs. DIBL tradeoff. The halo allows even lightly doped uniform profiles ($1 \times 10^{17}$ cm$^{-3}$) to have intrinsic performance equivalent to heavily-doped retrograde profiles [82] (Fig. 7-8). Thus, from this data, it can be concluded that for a given value of DIBL, the source/drain technology is more effective in improving the intrinsic device performance of bulk devices than the channel variables.

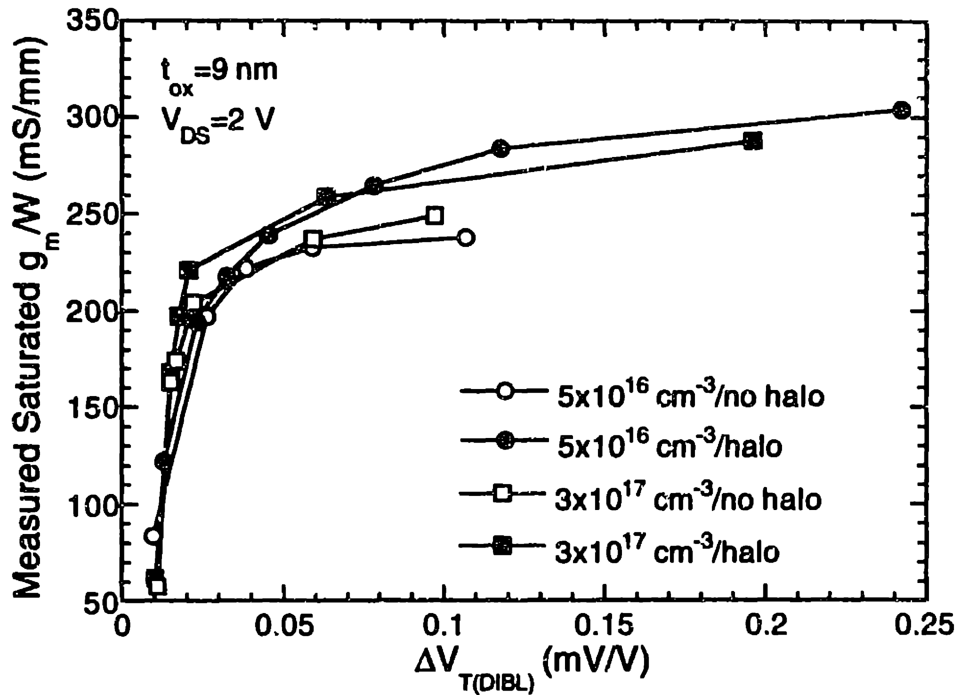


Figure 7-7: Measured saturated transconductance, $g_m/W$ vs. drain-induced barrier lowering, $\Delta V_{T(DIBL)}$ for two uniform doping concentrations with and without a halo around the source/drain ($t_{ox}$=9 nm, $V_{DS}$=2 V).

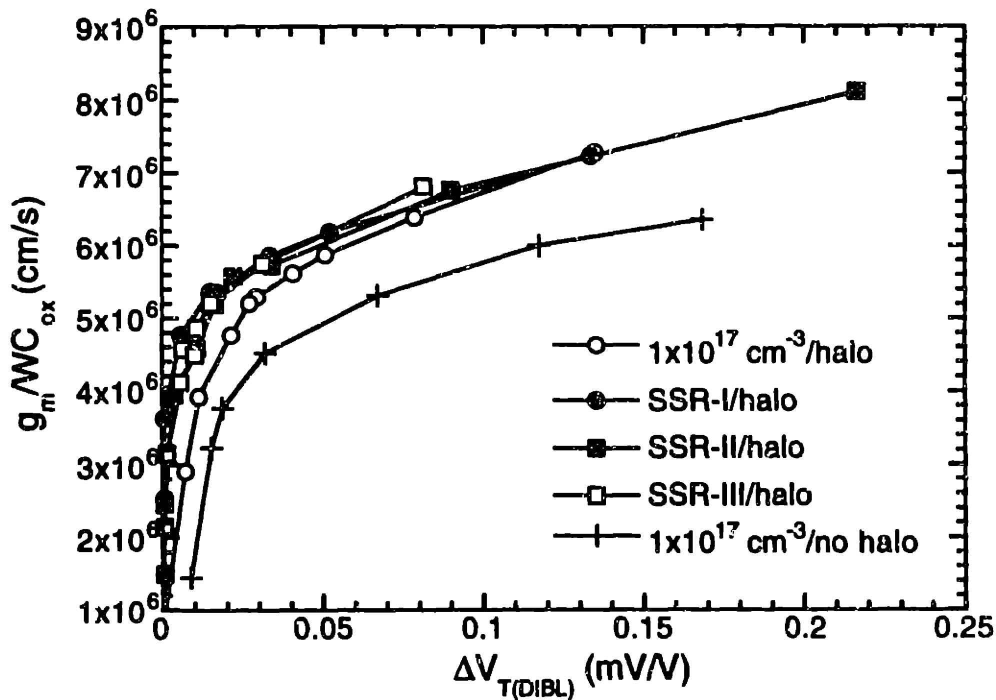


Figure 7-8: Intrinsic speed, $g_m/WC_{ox}$ vs. drain-induced barrier lowering, $\Delta V_{T(DIBL)}$ for uniform $1x10^{17}$ $cm^{-3}$ doping with and without halo and three retrograde profiles with halo doping. The implant and process conditions for the three profiles (SSR-I, II, and III) are given in Ref. [82].

### 7.3.3 Drive Current vs. Off Current

In the preceding plots the $V_T$ and the supply voltage were not explicitly stated. To compare practical device configurations, Fig. 7-9 shows $I_{dsat}/W$ vs. $I_{off}/W$ for several doping profiles with long-channel $V_T$ of 0.3-0.5 V. The use of $I_{off}/W$ includes the effect of long-channel $V_T$, DIBL and the subthreshold slope of the device. Once again, $L_{eff}$ is a hidden parameter in the $I_{dsat}/W$ vs. $I_{off}/W$ plot. Note that the drain currents for $t_{ox}$=6 and 9 nm were normalized to a gate oxide thickness of 5.3 nm by multiplying by the ratios of the gate oxide thicknesses, 6/5.3 and 9/5.3 respectively. This was done so that drive currents of devices with different gate oxide thicknesses could be compared.

For the uniform profiles, the difference in $I_{off}/W$ in the 1-100 pA/µm range is primarily due to long-channel $V_T$, however, at larger $I_{off}/W$ (shorter $L_{eff}$), the curves approach one another. The two retrograde cases with halo also behave similarly although there is no cross-over in the curves.

This behavior can be understood because at long $L_{eff}$, the ratio between $I_{dsat}/W$ and $I_{off}/W$ is primarily determined by $V_T$ which is constant. However, at shorter $L_{eff}$, $I_{off}/W$ is dominated by DIBL and increases more quickly than $I_{dsat}/W$. This reduces the slope of the curve. Note that the retrograde with halo have a higher $I_{dsat}/W$ at a given $I_{off}/W$ than the uniform without halo, which is consistent with the $g_m/WC_{ox}$ vs. DIBL plots.

From these trends in conventional bulk devices, it is clear that this methodology can be used to compare the intrinsic device performance of various design options in a given technology, as well as comparing two different technologies such as bulk and SOI.

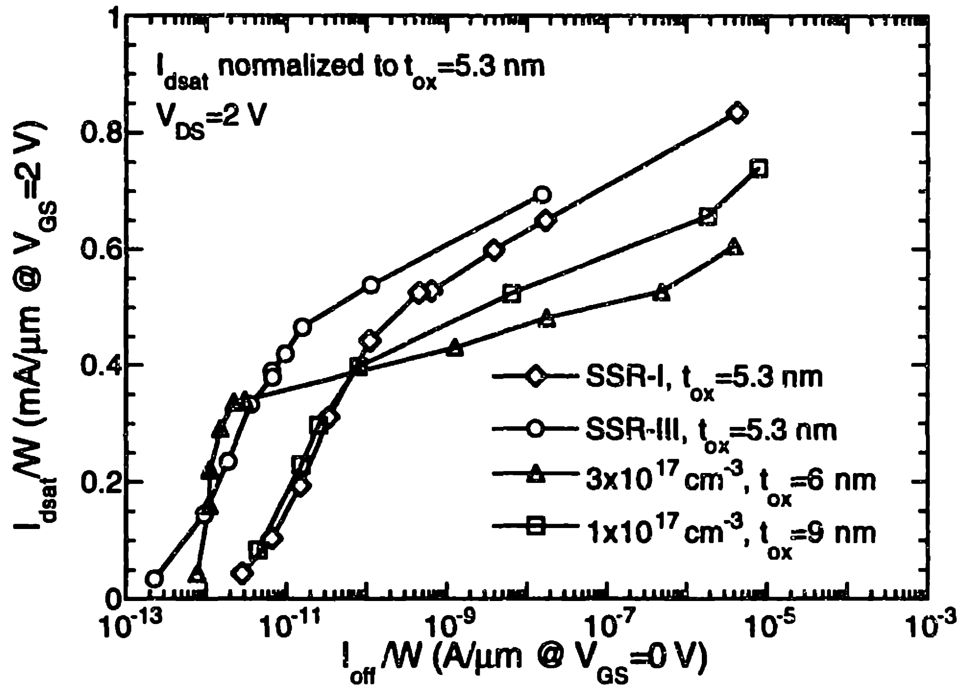


Figure 7-9: Maximum drive current, $I_{dsat}/W$ @ $V_{GS}$=$V_{DS}$=2 V vs. off current, $I_{off}/W$ @$V_{DS}$=2 V, $V_{GS}$= 0 V for two retrograde doping profiles and two uniform doping profiles. The drain current was normalized to a $t_{ox}$ of 5.3 nm.

# 7.4 SOI MOSFET Performance

## 7.4.1 Channel and Source/Drain Design

For SOI, a similar approach can be used to study the intrinsic device performance. Figure 7-10 shows the DIBL vs. $L_{eff}$ for several doping concentrations in SOI. For a silicon film thickness of 40 nm as shown in the figure, the two lower doping concentrations are fully-depleted while the highest doping concentration ($6 \times 10^{17}$ cm$^{-3}$) devices are partially-depleted. Similar to the bulk data, when $N_a$ is increased, the DIBL is reduced. However, for the partially-depleted device ($6 \times 10^{17}$ cm$^{-3}$), the apparent DIBL includes both electrostatic effects and a floating-body-induced self-bias that reduces $V_T$. This causes the behavior to be somewhat different from bulk and fully-depleted devices. There is a significant $V_T$ shift even at long $L_{eff}$ and hence although the roll-off with $L_{eff}$ is less severe than for the lower $N_a$, the magnitude of the $V_T$ shift is larger. This was discussed as an important point that was not taken into account in the simulations in Chapter 3. The problem with the floating-body induced $V_T$ shift, is that this can potentially increase the off-state leakage current. However, the floating-body effect also induces a super-steep subthreshold slope (less than 60 mV/dec) which can counteract the larger floating-body induced $V_T$ shift [138]. This will be examined further in the tradeoff relationships.

Figure 7-11 shows the DIBL vs. $L_{eff}$ for several silicon film thicknesses. For a doping concentration of $1 \times 10^{17}$ cm$^{-3}$ as shown in the figure, the two thinner silicon films are fully-depleted while the thickest silicon film ($t_{si}$=180 nm) devices are partially-depleted. The DIBL is improved in fully-depleted devices ($t_{si}$=40 nm and 65

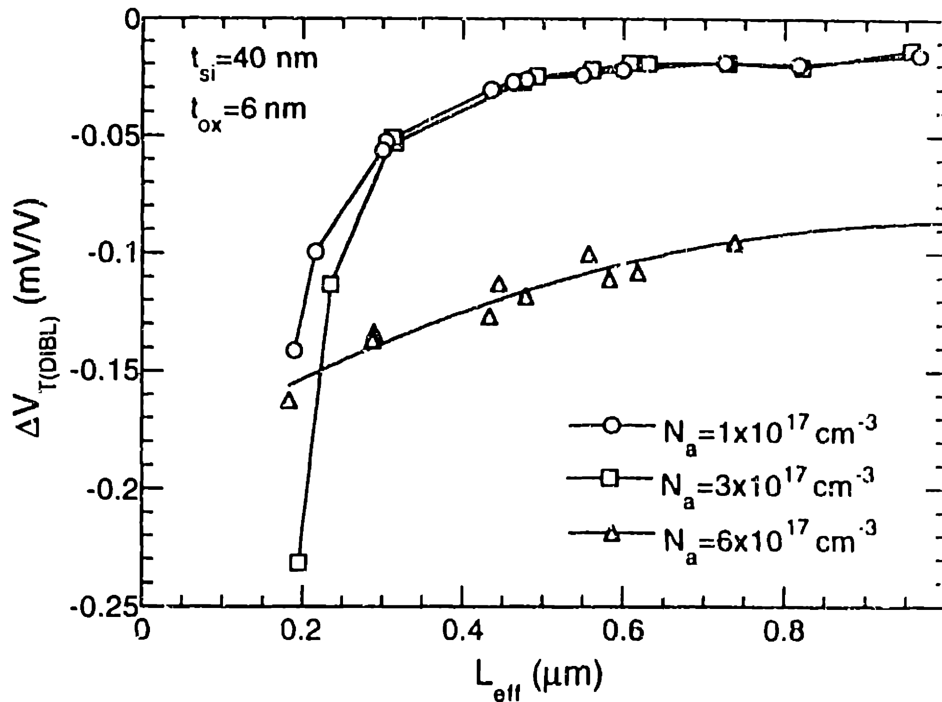


Figure 7-10: Drain-induced barrier lowering, $\Delta V_{T(DIBL)}$ vs. $L_{eff}$ for several doping concentrations in a SOI device ($t_{si}$=40 nm, $t_{ox}$=6 nm).

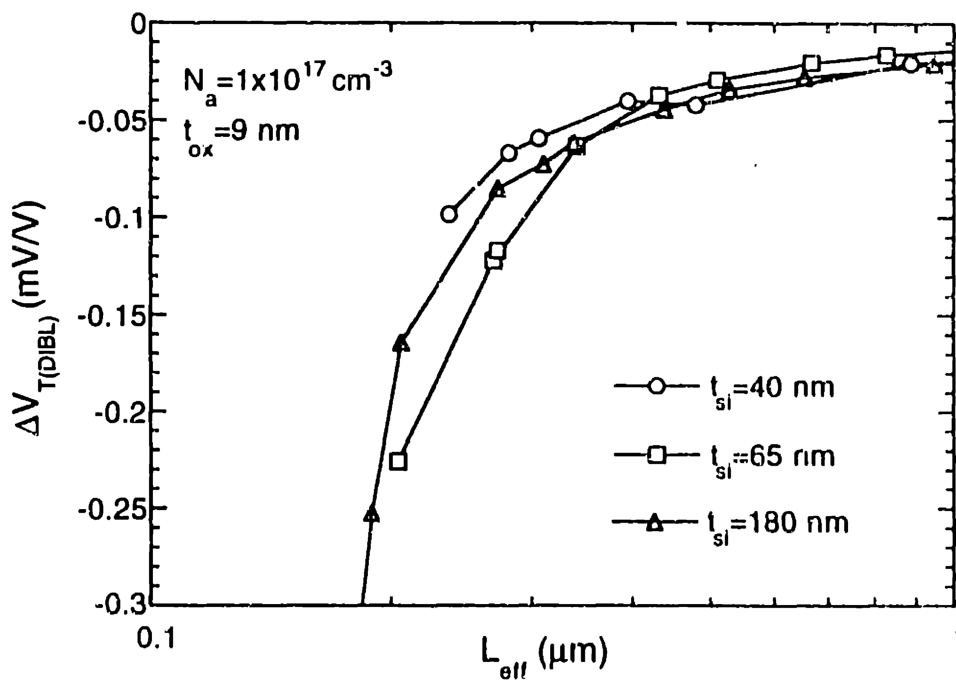


Figure 7-11: Drain-induced barrier lowering, $\Delta V_{T(DIBL)}$ vs. $L_{eff}$ for several SOI silicon film thicknesses ($N_a$=1x10$^{17}$ cm$^{-3}$, $t_{ox}$=9 nm).

nm) with decreasing $t_{si}$ because the source and drain depth is reduced. However, the partially-depleted device ($t_{si}$=180 nm) has smaller DIBL than the $t_{si}$=65 nm case. This is due to the two-dimensional coupling in the buried oxide that was discussed extensively in Chapter 3. Because the $t_{si}$=180 nm film is partially-depleted, the channel is electrostatically shielded which improves the short-channel effects over the $t_{si}$=65 nm case. Interestingly, the floating-body-induced self-bias for $t_{si}$=180 nm is significantly less than in the 6x10$^{17}$ cm$^{-3}$ devices in Fig. 7-10. This may be due to the fact that a lower $N_a$ results in less severe floating-body effects.

Figure 7-12 show $g_m/W$ vs. $L_{eff}$ for several doping concentrations. The lower $N_a$ devices have higher $g_m/W$ than the higher $N_a$ devices. This can be understood because mobility in SOI devices behaves similarly to bulk devices and displays a universal mobility behavior when compared at the same effective vertical field [139]. Thus, as $N_a$ is increased, the effective vertical field is increased, which decreases mobility and hence reduces $g_m/W$. This behavior is similar to the bulk devices in Fig. 7-3.

Figure 7-13 shows the $g_m/W$ vs. $L_{eff}$ for several silicon film thicknesses. The fully-depleted devices ($t_{si}$=65 nm) exhibit higher $g_m/W$ than the partially-depleted devices ($t_{si}$=180 nm). For these two silicon film thicknesses, the increase in mobility is very minimal because the effective vertical electric fields are not significantly different. The improvement in transconductance for the fully-depleted devices is due mainly to the suppression of body charge that was discussed as one of the advantages of SOI in Chapter 2 [29,30]. The thinnest film ($t_{si}$=40 nm) has the lowest $g_m/W$ due to a poor parasitic resistance ($R_{SD}$ ~ 1000 Ω-μm) because it was not silicided.

Figure 7-14 shows the results of directly plotting $g_m/W$ vs. DIBL in the SOI

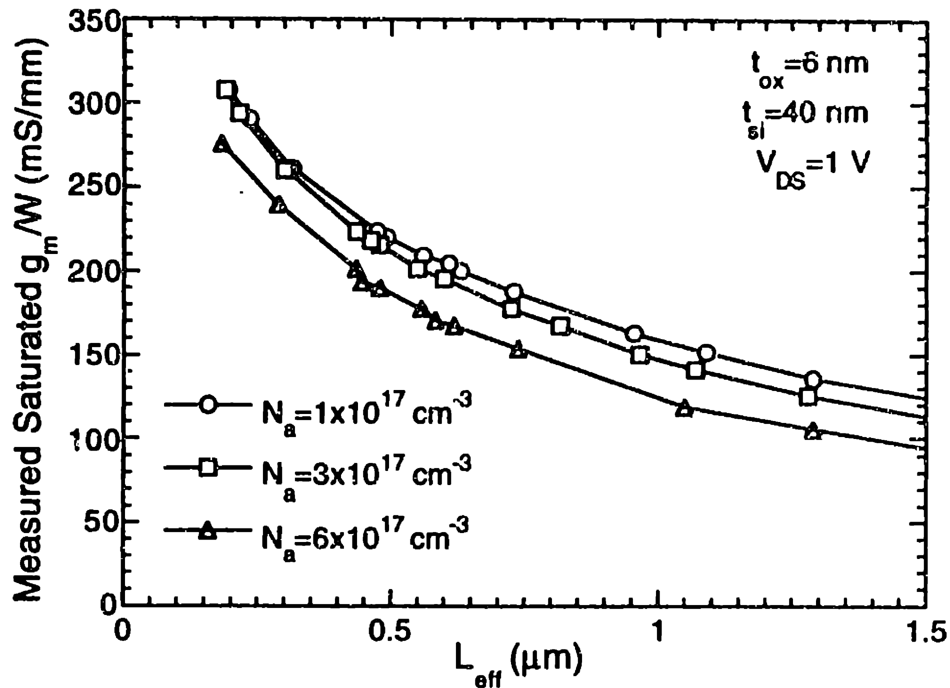


Figure 7-12: Measured saturated transconductance, $g_m/W$ vs. $L_{eff}$ for several doping concentrations in SOI devices ($t_{si}$=40 nm, $t_{ox}$=6 nm, $V_{DS}$=1 V).

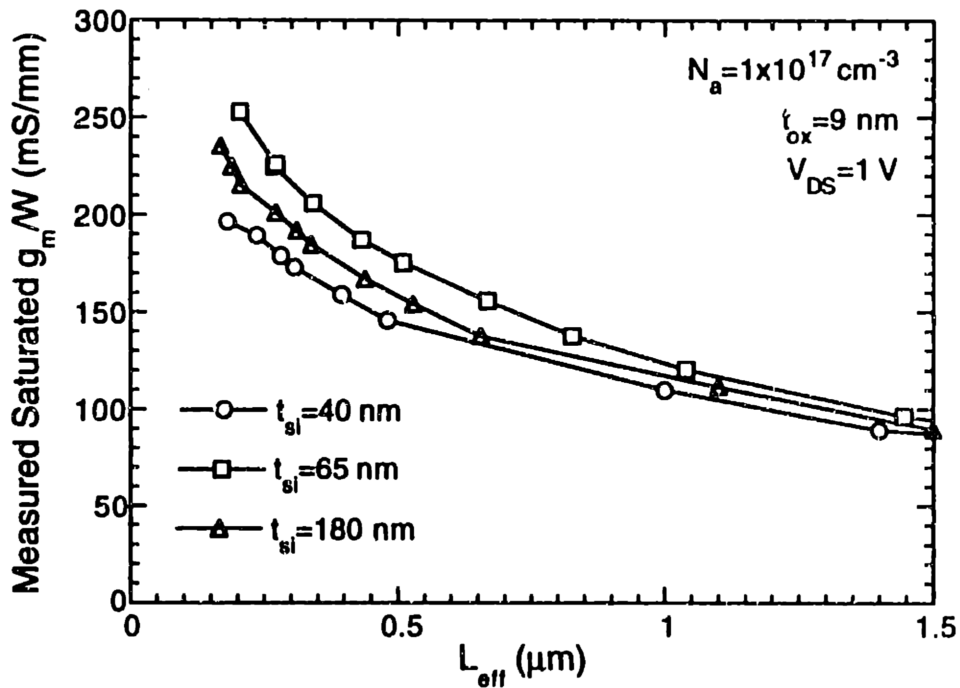


Figure 7-13: Measured saturated transconductance, $g_m/W$ vs. $L_{eff}$ for several SOI silicon film thicknesses ($N_a$=1x10$^{17}$ cm$^{-3}$, $t_{ox}$=9 nm, $V_{DS}$=1 V).

devices with varying $N_a$. The fully-depleted devices are similar to the bulk in that the performance behavior with respect to $N_a$ is rather universal. The partially-depleted behavior is more complicated at low DIBL values because of the self-bias effect discussed earlier. This results in a much worse and non-universal behavior at low DIBL values ($L_{eff} > 0.3$ µm). At shorter $L_{eff}$, the magnitude of the electrostatic component begins to dominate the DIBL behavior of the partially-depleted devices, so the data approaches that of the fully-depleted devices.

The gate oxide thickness dependence of the performance vs. short-channel effects tradeoff in SOI was also examined and data showed a universal dependence similar to that which was obtained in bulk devices.

This data suggests that in fully-depleted SOI devices, channel engineering does not significantly alter the performance tradeoff as in the bulk case. The situation in partially-depleted devices is more complicated because of the floating-body-induced threshold voltage shift. Because this results in a significant change in subthreshold slope, a more appropriate comparison of the partially-depleted case requires examination of the off current in Section 7.5.

Varying $t_{si}$ affects both channel and source/drain design because $t_{si}$ determines the junction depth and the mode of operation (full or partial-depletion) in SOI. Figure 7-15 shows the $g_m/W$ vs. DIBL tradeoff for several silicon film thicknesses. Thinning the $t_{si}$ from 180 to 65 nm improves the $g_m/W$ vs. DIBL tradeoff. This occurs because of the increase in $g_m$ due to the suppression of the body charge near the drain. In the $t_{si}$=40 nm case, the series resistance is significant and reduces the measured $g_m/W$ significantly which adversely effects the performance tradeoff. The intrinsic transconductance can be extracted from the measured transconductance correcting for series resistance according to the following relationship [140]:

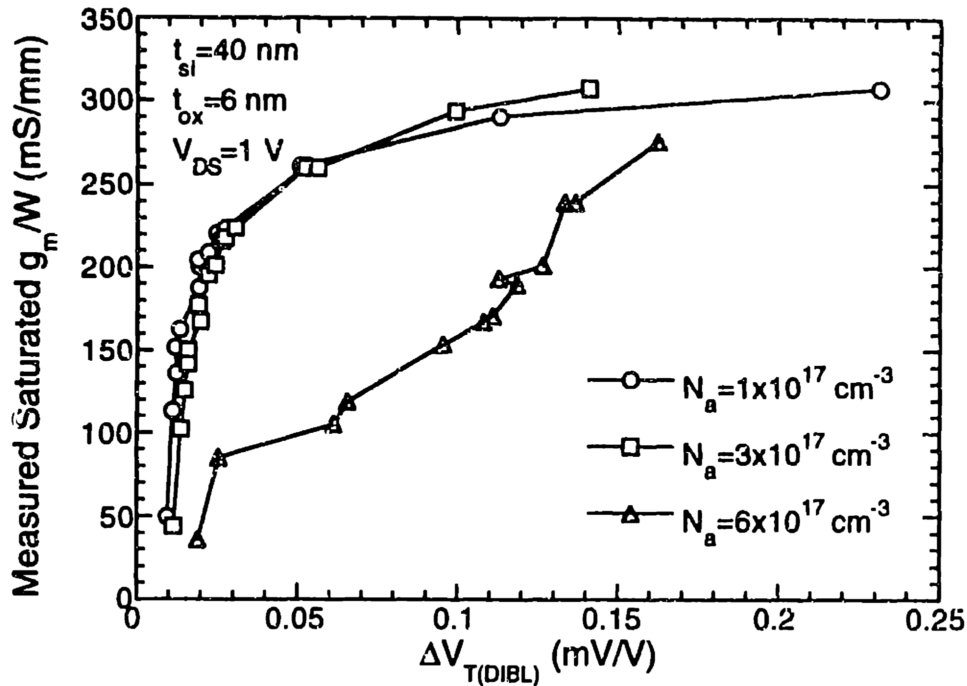


Figure 7-14: Measured saturated transconductance, $g_m/W$ vs. DIBL for several doping concentrations in SOI devices ($t_{si}$=40 nm, $t_{ox}$=6 nm, $V_{DS}$=1 V).

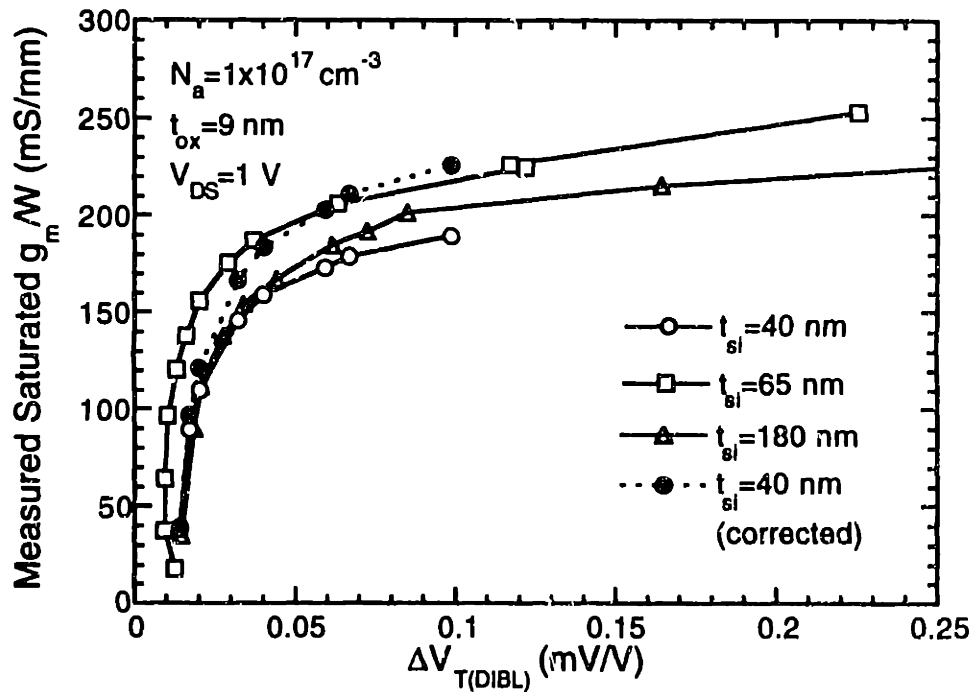


Figure 7-15: Measured saturated transconductance, $g_m/W$ vs. DIBL for several SOI film thicknesses ($N_a$=1x10$^{17}$ cm$^{-3}$, $t_{ox}$=9 nm, $V_{DS}$=1 V). Also shown is the intrinsic $g_{mi}/W$ for $t_{si}$=40 nm.

$$g_{mi} = \frac{g_m}{1-g_m R_s} \tag{7.2}$$

Once the $t_{si}$=40 nm is corrected for parasitic $R_S$, the saturated $g_m/W$ also increases above the $t_{si}$=180 nm. The series resistance in the $t_{si}$=60 nm and 180 nm cases are sufficiently low so that correcting for the parasitic resistance results in minimal change in their results. Thus, varying $t_{si}$ alters the performance curves primarily by changing the device operation from partial to full-depletion without degrading the mobility.

It should be noted that the halo doping strategy that was so successful in the bulk devices is also potentially very helpful in improving the SOI performance tradeoff.

## 7.5 Bulk and SOI Comparison

Figure 7-16 shows $g_m/WC_{ox}$ vs. DIBL for bulk and SOI technologies that were fabricated with similar fabrication processes. Comparing the fully-depleted devices ($N_a$=1x10$^{17}$ cm$^{-3}$, $t_{si}$=65 nm) to the bulk devices, the behavior is rather universal (within 5%). For the partially-depleted devices, there is some spread in the data, and the characteristics clearly show the effect of the floating-body-induced DIBL.

In Figs. 7-17 and 7-18 the $I_{dsat}/W$ vs. $I_{off}/W$ for partially-depleted and fully-depleted devices are shown in comparison to the bulk devices. In the fully-depleted devices, the measured maximum drain saturation current for a given off current is

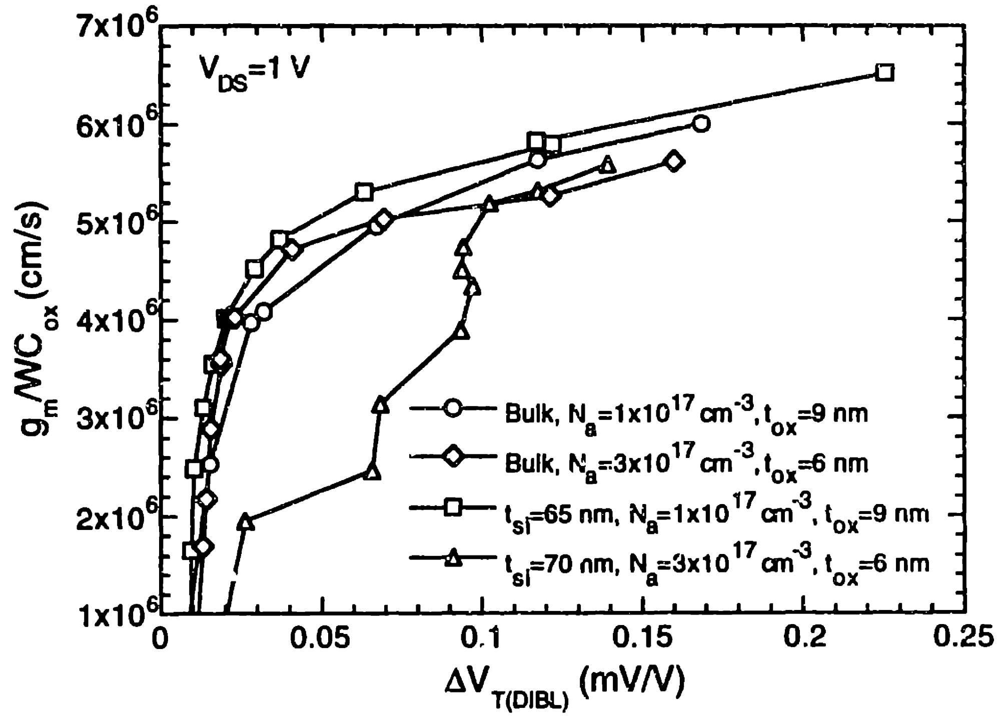


Figure 7-16: Intrinsic speed, $g_m/WC_{ox}$ vs. DIBL for two doping concentrations and gate oxide thicknesses in bulk and SOI devices ($V_{DS}$=1 V).

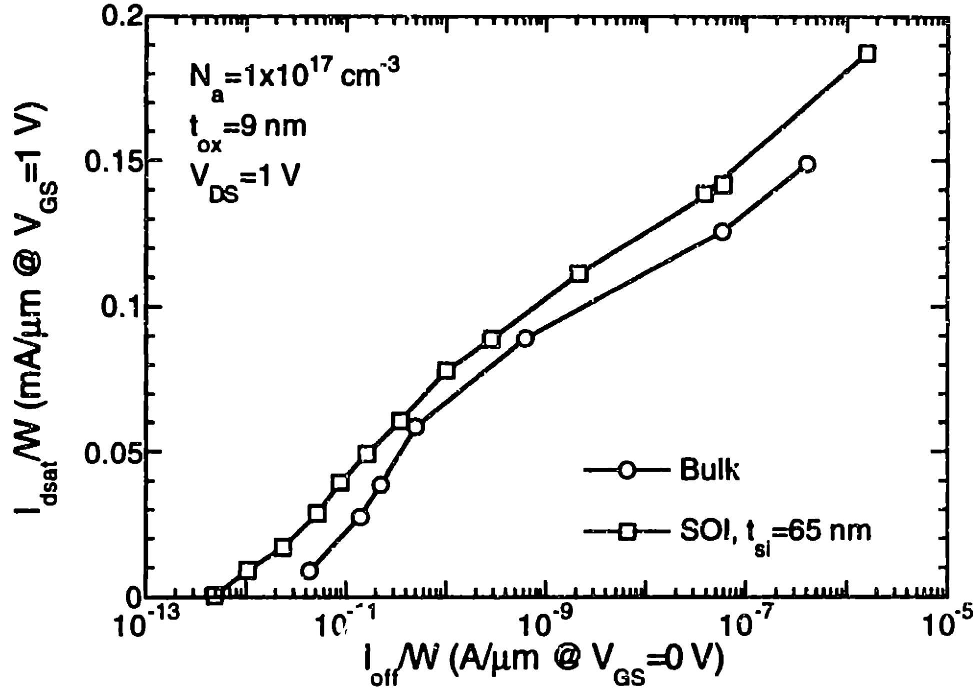


Figure 7-17: Maximum drive current, $I_{dsat}/W$ @ $V_{GS}$=$V_{DS}$=1 V vs. off current, $I_{off}/W$ @$V_{DS}$=1 V, $V_{GS}$= 0 V for a bulk and fully-depleted SOI device ($N_a$=1x10$^{17}$ cm$^{-3}$, $t_{ox}$= 9 nm).

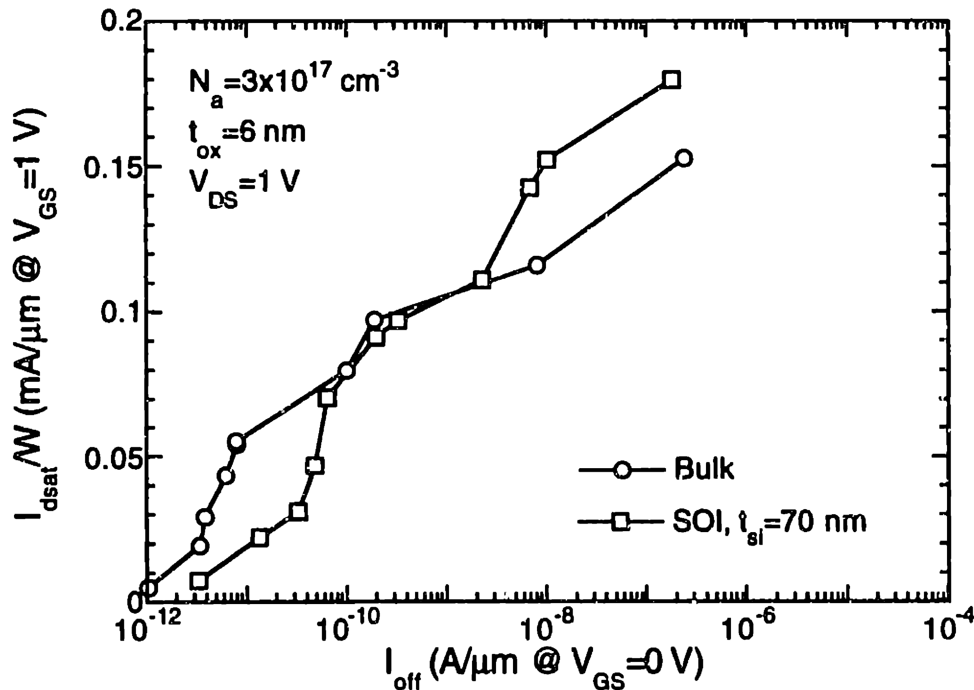


Figure 7-18: Maximum drive current, $I_{dsat}/W$ @ $V_{GS}$=$V_{DS}$=1 V vs. off-current, $I_{off}/W$ @$V_{DS}$=1 V, $V_{GS}$= 0 V for a bulk and partially-depleted SOI device ($N_a$=3x10$^{17}$ cm$^{-3}$, $t_{ox}$= 6 nm).

relatively linear and quite close to the bulk devices. The slightly higher $I_{dsat}/W$ at a given off current in the SOI devices is due to a small difference in the long-channel threshold voltages for the two technologies. The fact that the curves are almost parallel indicate that the performance vs. short-channel effects are similar for the two cases. This verifies the universal behavior that was observed in the $g_m/W$ vs. DIBL plot in Fig. 7-16.

For the partially-depleted devices in Fig. 7-18, the behavior is more complicated. The long-channel threshold voltages of the two technologies are the same but the floating-body effects cause $I_{off}/W$ to increase. Hence, for the same $I_{off}/W$, the $I_{dsat}/W$ of the partially-depleted devices are below the bulk devices at relatively long channel lengths. Interestingly, for short channel lengths (higher $I_{off}/W$), the two curves cross. Recalling the $g_m/W$ vs. DIBL curves in Fig. 7-16, although the partially-depleted device curve approached the bulk curves, it never surpassed it. For the curves to cross, this indicates that the floating-body effects in the partially-depleted devices must be inducing a super-steep subthreshold slope which is able to significantly reduce the off current for a given threshold voltage.

From these data, it can be concluded that the current drive of similarly designed bulk and fully-depleted SOI devices is quite close when comparing the $g_m/W$ vs. DIBL tradeoff. In partially-depleted devices, the characteristics are more complicated due to the floating-body effects. There is a potential that the super-steep subthreshold slope in partially-depleted SOI can result in improved tradeoffs between $I_{off}/W$ and $I_{dsat}/W$. However, more detailed investigation of the dependencies of the floating-body effects must be done before this can be utilized. In particular, there are questions regarding the dynamic response of the floating-body effects and the reproducibility of using such a transient phenomenon.

## 7.6 Other Performance Issues

This work has primarily examined the tradeoff between short-channel effects and current drive. Although this is the most basic tradeoff for device design, there are other issues that should be considered.

For high-performance applications, the effect of reliability on the performance tradeoff particularly with regard to the floating-body effects in partially-depleted devices must be considered. Previous studies of 0.25 μm bulk CMOS technology, have identified reliability as a key design concern that dictates the voltage scaling of devices [9]. This would be also true for SOI if the breakdown voltage or hot-carrier reliability is found to be a limiting factor that requires extensive drain-engineering. For devices with doping concentrations and effective channel lengths similar to the ones in this study ($L_{eff} \approx 0.25$ μm, $t_{si} = 100$ nm, $N_a = 1\text{x}10^{17}$ cm$^{-3}$), the breakdown voltage is about 2.5 V [141]. This is consistent with some of our own measurements and is probably not acceptable for the highest performance 0.25 μm technologies which might have supply voltages around 2.5 V. A major challenge in this arena would then be to add a third dimension of design optimization that would seek to increase breakdown voltage without adversely affecting the performance and short-channel effects too greatly. The goals here would be similar to the study done by Chung et al. for 0.25 μm bulk technologies [142].

It should be noted though that much of the interest in SOI is now centered on the low-power front, which would mean supply voltages of 1-1.5 V [143,144]. For these applications, reliability concerns will be significantly reduced and the main tradeoffs will be current drive, short-channel effect and power dissipation. SOI has

significant advantages in the area of low-power technologies because of the reduced parasitic capacitances and the potential for improved subthreshold slope.

## 7.7 Summary and Conclusions

In conclusion, a methodology has been demonstrated for assessing intrinsic device performance and a wide range of bulk and SOI devices have been studied. The primary issue in assessing device performance involves the tradeoff between intrinsic speed (measured by transconductance and current drive) and the short-channel effects (measured by drain-induced barrier lowering and off current). For the range of devices studied, the current drive vs. DIBL is determined primarily by the junction technology in bulk devices and the mode of operation in SOI. Comparing bulk and SOI, fully-depleted devices show a behavior very similar to bulk, i.e. the $g_m/W$ at a given DIBL constraint are about the same if the parasitic resistances are comparable. In partially-depleted devices, the behavior is more complicated due to the floating-body effects. Floating-body effects induce a non-negligible shift in the threshold voltage even at long channel lengths which tend to degrade the performance tradeoff. However, in the short-channel regime, the DIBL is increasingly dominated by the electrostatic effects instead of the floating-body effects. This coupled with the super-steep subthreshold slope of the partially-depleted devices can potentially provide improved $I_{dsat}$ vs. $I_{off}$ tradeoff in SOI. However, it remains to be seen whether these transient bipolar effects can be actually used in a circuit environment.

# Chapter 8

# Summary and Conclusions

The goal of this work was to contribute to the assessment of the technical viability of SOI technology as a potential challenger to bulk silicon for the mainstream CMOS market at an insertion technology generation of 0.25 μm and below. To this end, several of the critical intrinsic device issues that face SOI technologies have been investigated including the SOI device electrostatics and channel design, parasitic series resistance, self-heating effects, hot-carrier phenomena, and the tradeoff between current drive and short-channel effects.

## 8.1 Summary

The main contributions of this work can be roughly divided into three categories: advances in the understanding of the device physics of SOI devices, proposed technology and modeling solutions. The majority of the work has dealt

with improving the understanding of SOI device physics and its comparison to conventional bulk technologies.

In the area of device electrostatics and channel design, it has been shown that in the sub-0.25 μm channel length regime, SOI can not be expected to have significantly improved short-channel effects over conventional bulk technologies. This is somewhat contrary to previous predictions that SOI devices exhibit reduced short-channel effects as compared to bulk technologies for channel lengths greater than 0.5 μm [10,11,25]. For SOI to exhibit improved short-channel effects over bulk technologies, the thickness of the silicon film must be significantly thinner than the source/drain junction depth in the comparable bulk technology. Comparing a bulk device and SOI device where the junction depth is the same as the silicon film thickness, the short-channel effects are at best the same for both devices when using partially-depleted SOI, and can actually be worse in the SOI case for fully-depleted devices. This work has identified the appropriate design options for fully and partially-depleted devices in the deep-submicrometer channel length regime. It is important to note though that in terms of the device physics, short-channel effects can not be considered an area in which SOI exhibits significant advantages over bulk technologies.

The contributions of this work in the area of parasitic series resistance are in understanding the theoretical issues surrounding the contact geometry design and in suggesting a potential technological solution. From the theoretical standpoint, it is clear that to obtain the lowest parasitic series resistance, the contact geometry is very important and that silicides that do not consume more than 60-80% of the silicon film are needed. For typical silicon film thicknesses in the sub-0.25 μm channel length regime, this translates into self-aligned silicides that are as thin as 20 nm. A cobalt disilicide technology using titanium/cobalt laminates is explored to

demonstrate ultra-thin, thermally-stable silicides at the required dimensions. This technology was used to demonstrate record-low parasitic series resistances of 250 Ω-μm in SOI devices and should also be applicable in conventional bulk technologies as well. With the correct design of the contact geometry and optimization of the fabrication processes, the parasitic series resistance in SOI devices can be comparable to bulk technologies and will not be a limiting factor.

In the topic of self-heating effects, contributions have been made in the areas of measurement techniques, understanding of the structural dependencies, and temperature and device modeling. The key conclusion of the self-heating work is that although temperature rises for SOI devices operating under static, steady-state conditions are indeed large (greater than 100 °C for typical operating conditions in 0.3 μm devices), the average temperature under typical dynamic conditions for digital circuits is much lower. The most important issue then becomes the accurate modeling of device characteristics that are appropriate for circuit simulation. A modeling methodology which uses only minor modifications from a bulk SPICE model to fit fully-depleted SOI including self-heating is demonstrated. In cases where devices will operate under static conditions in a circuit environment, the temperature model developed by Goodson and Flik and verified in this work allows the foundation for calculation of the temperature fields throughout the device. With accurate measurement and modeling of the temperature in SOI devices, there is no evidence that self-heating poses a fundamental problem for the integration of SOI technologies into mainstream CMOS applications.

In the area of hot-carrier effects, the main contribution of this work has been in providing experimental data examining the use of hot-carrier gate currents as an indication of device electric fields and its potential as a reliability monitor for

device lifetime. From the data, it is clear that gate currents do provide some important insight into the hot-carrier phenomena, however device degradation in SOI is more complicated than in bulk devices because of the floating body effects and the existence of two silicon/silicon-dioxide interfaces. In addition, the reliability is quite dependent on the specific technology, i.e. source and drain parameters, the quality of the buried oxide interface, etc. The work presented here provides some foundation for the evaluation of the device reliability in SOI, however, a complete study of the device reliability as well as a comparison of bulk and SOI technologies is extremely important and still needs to be completed.

Finally, the evaluation of the intrinsic performance tradeoffs between short-channel effects and current drive reveals that the current drive of fully-depleted SOI devices appears to be very close to bulk devices fabricated in the same technology for a given amount of drain-induced barrier lowering or off current. Partially-depleted devices have lower current drive for a given amount of apparent drain-induced barrier lowering because of the floating-body-induced threshold voltage shift. However, the super-steep subthreshold slope of partially-depleted devices can potentially result in higher drive current for a given off current. The viability of partially-depleted devices will depend on whether or not the super-steep subthreshold slope can be used reproducibly in a dynamic circuit environment.

## 8.2 Technology Perspectives

From the results of this work and the vast amount of recent literature demonstrating well-behaved, sub-0.25 μm SOI devices (e.g. [129,130]), it is clear that SOI is a viable technology at least technically. There is no doubt that it is possible to design and fabricate both fully and partially-depleted SOI devices down to the 0.1 μm channel length regime with excellent characteristics. However, there have also

been many demonstrations of excellent 0.1 μm devices in conventional bulk technologies [78-83]. The key question then is whether the advantages or benefits of SOI are enough to justify the cost.

From a device performance perspective, it is unlikely that SOI offers any significant improvement in terms of reduced short-channel effects or improved current drive. The main advantages of SOI are the reduction in parasitic capacitance, potential for simpler and cheaper device fabrication, reduced susceptibility to soft-errors, and reduced substrate-bias effect as discussed in Chapter 2. These advantages can potentially result in increased circuit speeds for SOI over bulk technologies. However, the magnitude of the improvement is still a point of controversy.

Many comparisons of the bulk and SOI performance have been attempted in the literature, however, one must be extremely careful in interpreting some of the results. Some studies have reported more than a factor of 2 improvement in circuit speed for SOI over bulk technologies, however, the SOI devices often have lower threshold voltage and thus the off current and power dissipation are higher [11,145]. In addition, the magnitude of the improvement is extremely dependent on the optimization of the bulk CMOS process used in the comparison.

The parasitic capacitance will make the largest contribution to the improvement in circuit speed. For a buried oxide thickness of 400 nm and a low-parasitic sub-0.25 μm bulk technology, simulations show that the improvement will likely be around 20-30% in speed depending on the circuit configuration, layout, and supply voltage and about 30-40% improvement in power-delay product at a given supply voltage [146,147].

However, in terms of costs, SOI technology starts with a higher substrate cost, and a much higher technology learning curve relative to a bulk technology.

The substrate costs have continually been reduced and the goal of SIMOX manufacturers are to offer SOI substrates at about 2 times the cost of an epitaxial silicon wafer [148]. This coupled with the reduction in process steps in SOI should be sufficient to match the unit cost of a bulk chip. Some economic studies have actually predicted that the unit cost of a SOI chip will in fact be cheaper than bulk due to the increased packing density and reduced fabrication steps, but that is heavily dependent on the particular assumptions of the study [149].

The larger issue is the experience-base of SOI and the startup cost required to develop the technology. SOI should be treated as a viable option to improving a bulk process but it is by no means the only one. For high-performance digital applications, there are still many remaining issues facing SOI, the most serious ones being the impact of the breakdown voltage and hot-carrier effects on the maximum allowable supply voltage. These issues are not impossible to solve but do require further investigation to fully understand the device physics and acquire the necessary experience-base to deal with them.

However, in the low-power arena, SOI has the potential to be extremely simple to integrate into a conventional bulk process because the high-field problems are greatly reduced. In this case, SOI devices are very similar to bulk devices but have significantly improved circuit performance. For this reason, SOI is currently considered one of the leading candidates for low-power, low-voltage devices and circuits [143,144].

## 8.3 Future Directions

In terms of future directions, the demonstration of large-scale circuits on SOI substrates are extremely important to assess the commercial potential of the

technology as well as the evaluation of the effects of material quality on yield. However, these can only be evaluated in an industrial environment.

In terms of research directions, a more thorough understanding of the SOI device behavior in a circuit environment would be very beneficial. In particular, an evaluation of the portability of bulk circuit designs onto SOI as well as opportunities that SOI may offer for novel devices/circuits would be of much interest.

On the modeling front, a full understanding of the breakdown voltage and all of the related high-field phenomena is essential if SOI is to be used in high-performance applications. Also, further exploration of partially-depleted devices and their behavior in a dynamic environment are important if the floating-body effects such as super-steep subthreshold slope are to be used.

# Appendix A

# Fabrication Technology

A wide range of bulk and SOI NMOS devices were fabricated as part of this thesis research. This section outlines the process travelers, modules and splits for the devices.

## A.1 Process Flow Listing

The process traveler outlined in the following section is the most recent traveler for SOI device processing. It is an 8-mask process to fabricate enhancement and depletion-mode NMOS devices and simple circuits.

| STEP # | STEP DESCRIPTION | COMMENTS |
|---|---|---|
| 1 | Silicon Film Thinning<br>950 °C, 30 min, Dry $O_2$<br>950 °C, variable time, Wet $O_2$<br>950 °C, 30 min, Dry $O_2$<br>950 °C, 30 min, $N_2$ | variable time for different silicon film thicknesses; target $SiO_2$: 1/.44 of desired silicon consumption |

| STEP # | STEP DESCRIPTION | COMMENTS |
|---|---|---|
| 2 | Wet Oxide Etch<br>Buffered Oxide Etch | dip until de-wet |
| 3 | Stress Relief Oxide<br>950 °C, 35 min, Dry $O_2$<br>950 °C, 30 min, $N_2$ | target $SiO_2$: 22 nm |
| 4 | LPCVD Silicon Nitride<br>785°C, 120 min, $SiH_2Cl_2/NH_3$ | target $Si_3N_4$: 150 nm |
| 5 | Mask 1: Active Area Pattern<br>Job: ICL CWR1<br>Mask: SOI CD | no alignment |
| 6 | Nitride Plasma Etch<br>$SF_6$ | recipe in Table A-1 |
| 7 | P field implant | Bulk and SOI $t_{si} > 100$ nm<br>Boron, $3x10^{13}$ $cm^{-2}$, 25 keV;<br>SOI $t_{si} < 100$ nm:<br>$BF_2$, $3x10^{13}$ $cm^{-2}$, 50 keV |
| 8 | Resist Ash | |
| 9 | Field Oxidation<br>950 °C, 30 min, Dry $O_2$<br>950 °C, var time, Wet $O_2$<br>950 °C, 30 min, Dry $O_2$<br>950 °C, 30 min, $N_2$ | Bulk: target $SiO_2$: 340 nm<br>SOI: target $SiO_2$: $(1/.44)t_{si}$<br>plus 10% over-oxidation |
| 10 | Nitride Wet Etch<br>170°C, Transene Etch, 40 min | 15 s BOE dip prior to nitride etch |
| 11 | Stress Relief Oxide Wet Etch<br>Buffered Oxide Etch, ~ 25 s | dip until de-wet in scribe lanes |
| 12 | Dummy Gate Oxidation<br>800 °C, 30 min, Dry $O_2$<br>800 °C, 15 min, $N_2$ | target $SiO_2$: 5 nm |
| 13 | Mask 2: Enhancement Implant Pattern<br>Job: LSU2, 1<br>Mask: SOI2 CI | special job: expose rows 1, 5;<br>align to Mask 1 (CD) |

| STEP # | STEP DESCRIPTION | COMMENTS |
|---|---|---|
| 14 | Enhancement Channel Implant | implant rows 1, 5<br>various doping splits |
| 15 | Resist Ash | |
| 16 | Mask 2: Enhancement Implant Pattern<br>Job: LSU2, 2<br>Mask: SOI2 CI | special job: expose rows 2, 6<br>align to Mask 1 (CD) |
| 17 | Enhancement Channel Implant | implant rows 2, 6<br>various doping splits |
| 18 | Resist Ash | |
| 19 | Mask 2: Enhancement Implant Pattern<br>Job: LSU2, 3<br>Mask: SOI2 CI | special job: expose rows 3, 7<br>align to Mask 1 (CD) |
| 20 | Enhancement Channel Implant | implant rows 3, 7<br>various doping splits |
| 21 | Resist Ash | |
| 22 | Mask 2: Enhancement Implant Pattern<br>Job: LSU2, 4<br>Mask: SOI2 CI | special job: expose rows 4, 8<br>align to Mask 1 (CD) |
| 23 | Enhancement Channel Implant | implant rows 4, 8<br>various doping splits |
| 24 | Resist Ash | |
| 25 | Mask 3: Depletion Implant Pattern<br>Job: LSU, 7<br>Mask: SOI2 CIN | special job: expose columns 1, 3, 5, 7<br>align to Mask 1 (CD) |
| 26 | Depletion Channel Implant | implants columns 1, 3, 5, 7<br>various doping splits |
| 27 | Resist Ash | |

| STEP # | STEP DESCRIPTION | COMMENTS |
|---|---|---|
| 28 | Mask 3: Depletion Implant Pattern<br>Job: LSU,8<br>Mask: SOI2 CIN | special job: expose columns 2, 4, 6, 8<br>align to Mask 1 (CD) |
| 29 | Depletion Channel Implant | implants columns 2, 4, 6, 8<br>various doping splits |
| 30 | Resist Ash | |
| 31a | Gate Oxidation<br>800 °C, 30 min, Dry $O_2$<br>800 °C, 15 min, $N_2$ | target $SiO_2$: 5 nm<br>dummy gate oxide etched in 50:1 HF after RCA SC-1 |
| 31b | Gate Oxidation<br>900 °C, 7-15 min, Dry $O_2$<br>900 °C, 30 min, $N_2$ | target $SiO_2$: 7-10 nm<br>dummy gate oxide etched in 50:1 HF after RCA SC-1 |
| 32 | LPCVD Polysilicon<br>625 °C, $SiH_4$ | target polysilicon thickness: 300 nm |
| 33 | Mask 4: Polysilicon Gate Pattern<br>Job: ICL CD1<br>Mask: SOI2 CP | align to Mask 1 (CD)<br>special exposure condition to achieve deep-submicron gates |
| 34 | Polysilicon Plasma Etch<br>$CCl_4$ | recipe in table A-2<br>alternate recipe using LTO hard mask described in section A.2.2 |
| 35 | Resist Ash | |
| 36 | Reoxidation<br>900 °C, 5 min, dry $O_2$<br>900 °C, 15 min, $N_2$ | target $SiO_2$: 7 nm |
| 37 | Mask 5: $N^+$ Implant<br>Job: ICL CP1<br>Mask: SOI2 CG | align to Mask 4 (CP) |
| 38 | $N^+$ Poly/Source/Drain Implant | Arsenic, $4x10^{15}$ $cm^{-2}$, 25 keV<br>0 degree implant |
| 39 | Resist Ash | |

| STEP # | STEP DESCRIPTION | COMMENTS |
|---|---|---|
| 40 | Mask 6: $P^+$ Implant Pattern<br>Job: ICL CP1<br>Mask: SOI2 CS | align to Mask 4 (CP) |
| 41 | $P^+$ Implant | $BF_2$, $1x10^{15}$ $cm^{-2}$, 25 keV<br>0 degree implant |
| 42 | Resist Ash | |
| 43 | Poly and Source/Drain Diffusion<br>1000 °C, 15-30 s | TRL RTA |
| 44 | LTO Deposition<br>400 °C, $SiH_4/N_2/O_2$, 45 s | target $SiO_2$: 15 nm |
| 45 | LPCVD Silicon Nitride<br>785 °C, $SiH_2Cl_2/NH_3$ | target $Si_3N_4$: 75-150 nm |
| 46 | Nitride Spacer Etch<br>$SF_6$ | modified endpoint parameters<br>recipe in Table A-1 |
| 47 | Ti/Co Evaporation<br>35 Å Ti/80-140 Å Co | RCA with aggressive dip in 50:1 HF prior to wafer loading (dip until de-wet in scribe lanes) |
| 48 | RTA Anneal 1<br>550 °C, 30 s, $N_2$ | wait until chamber temperature < 100 °C prior to loading wafer |
| 49 | Unreacted Metal Strip<br>4:1 $H_2SO_4/H_2O_2$, 2 min | |
| 50 | RTA Anneal 2<br>700 °C, 60 s, $N_2$ | |
| 51 | LTO Deposition<br>400 °C, $SiH_4/N_2/O_2$ | target $SiO_2$: 400 nm<br>No 50:1 HF dip to avoid attacking the silicide |
| 52 | Resist Coat | for backside etch<br>hardbake at 130 °C, 60 s |
| 53 | Backside LTO Wet Etch<br>Buffered Oxide Etch | dip until backside de-wet |

| STEP # | STEP DESCRIPTION | COMMENTS |
|---|---|---|
| 54 | Backside Nitride Plasma Etch<br>$SF_6$ | 20 s timed etch<br>recipe in Table A-1 |
| 55 | Backside LTO Wet Etch<br>Buffered Oxide Etch | dip until de-wet (~ 15 s) |
| 56 | Backside Polysilicon Plasma Etch<br>$SF_6$ | 2 min timed etch<br>recipe in Table A-3 |
| 57 | Backside Gate Oxide Wet Etch<br>Buffered Oxide Etch | dip until de-wet (~ 5 s) |
| 58 | Resist Ash | |
| 59 | Mask 7: Contact Pattern<br>Job: ICL CP1<br>Mask: SOI2 CC | align to Mask 4 (CP) |
| 60 | LTO Plasma Etch<br>$CF_4/CHF_3$ | timed etch until 10-50 nm $SiO_2$ remaining; recipe in Table A-4 |
| 61 | LTO Wet Etch<br>Buffered Oxide Etch | etch remaining $SiO_2$ until de-wet (~ 10 s) |
| 62 | Resist Ash | |
| 63 | Metal Deposition<br>1 μm Al/1% Silicon | clean in 3:1 $H_2SO_4/H_2O_2$<br>dip in buffered oxide etch (3 s) prior to loading wafers; no sputter etch |
| 64 | Mask 8: Metal Pattern<br>Job: ICL CC<br>Mask: SOI2 CM | align to Mask 7 (CC) |
| 65 | Metal Plasma Etch<br>$BCl_3/Cl_2/CHCl_3$ | recipe in Table A-5 |
| 66 | Resist Ash | |
| 67 | Metal Sinter<br>425 °C, 15 min, forming gas | |

## A.2 Process Modules

The majority of process steps in the SOI process were modified from the MIT 2 μm baseline CMOS process [150]. Several new process modules were characterized and developed to achieve extreme-submicrometer MOSFETs. This process development was done in collaboration with the other members of the device group: Dr. Hao Fang, Hang Hu, Melanie Sherony and Isabel Yang. In addition, several SOI-specific process modules were needed. The following section provides some of the details of the process modules.

### A.2.1 SOI Silicon Thinning and Isolation

**SOI Silicon Thinning:** Starting SOI SIMOX substrates obtained from IBIS Corp. are typically 150-220 nm silicon film on 300-400 nm buried oxide. Thicknesses of the silicon film were measured by a two-film ellipsometry technique. Because silicon film thickness is a major variable in SOI device design, various silicon film thicknesses were desired in our experiments. To achieve a final desired thickness, the silicon film thickness consumption during processing must be taken into account. All process steps involving oxidation (stress relief oxide, dummy gate oxide, and gate oxide) resulted in consumption of the silicon film. The total amount of consumption during processing was calculated by summing the total oxide grown and multiplying by 0.44, the ratio of the atomic mass of Si to $SiO_2$. An initial thinning step (step 1 in the process traveler) was used when thin SOI films were desired.

The initial thinning step was a thermally-grown oxide whose thickness was determined by the amount of silicon film consumption necessary to achieve the final desired silicon film thickness. It should be noted that based on the calculations

described above, the final silicon thickness measured electrically by the capacitance technique was always somewhat lower (~ 5-10 nm) than the process calculations would have predicted. This apparent discrepancy could be due to inaccurate measurements of silicon film thickness because we use a two-film ellipsometry program instead of a more sophisticated spectroscopic ellipsometer which would be able to differentiate multiple films. Another possible explanation is a different oxidation rate between SOI substrates and conventional bulk dummy wafers, on which all of the in-process oxidations were monitored. However, this is rather unlikely since electrical gate oxide thicknesses measured on SOI and bulk substrates processed simultaneously were quite close.

To remedy the apparent discrepancy between calculated and measured silicon film thicknesses, the initial thinning step was usually calculated to achieve a silicon thickness about 5-10 nm thicker than desired so that the correct electrical thickness was achieved.

**SOI Isolation:** The SOI isolation scheme used in this work was a modified LOCOS field oxide process. The parameters for the plasma nitride etch in the LOCOS process are given in Table A-1. The thickness of the field oxide grown was determined to fully consume the silicon film using the ratios described abov Typically an additional 10% of oxide was added to the calculated amount to insure that oxidation completely consumed the thickness of the film in the isolation region and extended through to the buried oxide. Although the isolation was designed to extend throughout the film, there was still a significant amount of edge leakage that occurred when a field implant was not used. The edge leakage occurred as a result of the bird's beak of the field oxide profile that created a region near the field oxide edge with very thin silicon film. We found that a fairly high dose field implant (Boron or $BF_2$, $3x10^{13}$ $cm^{-2}$) was able to eliminate the edge leakage although even

with the field implant there were still some sporadic signs of edge leakage particularly for transistors with very high threshold voltage. Optimization of the bird's beak profile and/or a higher field implant would probably eliminate the edge leakage completely.

### A.2.2 Deep-Submicrometer Gate Definition

**Lithography:** Deep-submicrometer gates were defined by over-exposure at the polysilicon patterning level using a GCA Corporation Model 4800 DSW 10X g-line (432 nm) wafer stepper. Careful examination of a wide focus/exposure range was necessary to obtain the optimum process conditions. The key constraint was to achieve narrow linewidths with minimal linewidth variation along the device width and good step coverage over the field oxide step.

The minimum layout dimension was 0.5 μm printed (10X, i.e. 5 μm on mask) with increments of 0.05 μm up to 1 μm. Typically, the over-exposure condition was chosen so that the first few lines were washed out, so that the $\Delta L$ between layout and actual physical dimension was about 0.5-0.6 μm.

Although the over-exposure process provided excellent throughput, the process control varied greatly from wafer to wafer and run to run. Because of this, electrical effective channel length measurements were required on each individual set of devices that were used for measurements. Variations in linewidth from die to die on the order of 0.2 μm were typical.

**Polysilicon Gate Etching:** The standard polysilicon gate etch was carried out in a LAM Research Model 480 plasma etcher. A $CCl_4$ etch chemistry was used to etch the polysilicon gates (Table A-2). Typical selectivity of the process was 5:1, silicon to silicon dioxide. However, for thin gate oxides, the selectivity of the etch

was not sufficient. Significant etching of the silicon film in the source/drain regions was observed as shown in the TEMs in Figs. 4-7 and 4-8.

An improved pattern transfer technology using a LTO hard mask etched by reactive-ion etch in $CHF_3$ and then subsequent pure $Cl_2$ etch for the polysilicon gates was utilized in subsequent runs [74]. The selectivity of the pure $Cl_2$ etch was approximately 30:1, silicon to silicon dioxide. By avoiding the over-etch of the silicon film into the source/drain regions, the series resistance of unsilicided devices on thin SOI films was improved considerably.

### A.2.3 Self-Aligned $CoSi_2$ Process (Spacer and Silicide Formation)

**Spacer formation:** The spacer technology was a 15 nm LTO/70-150 nm $Si_3N_4$ stack. The spacer was etched using the same etch recipe as the LOCOS nitride (Table A-1) with modified endpoint parameters. The LTO underlayer was necessary to act as an etch-stop for the nitride plasma etch. Silicon nitride was used instead of silicon dioxide spacers because of its etch resistance to HF.

**Silicide formation:** The silicidation process included wafer preparation, evaporation, and silicide formation. The wafer preparation consisted of a standard RCA clean with an aggressive HF dip. A 50:1 HF dip was performed after both the SC-1 and SC-2 cleans. It was important that the wafers de-wetted in the scribe lane areas particularly after be SC-2 clean. The HF dip was typically on the order of 20-40 s but the actual time depended greatly on the remaining LTO after the spacer etch.

After the RCA clean, the wafers were immediately placed into a Temescal Model VES 2550. The pump down time was typically about 1 hour to obtain a vacuum of less than $10^{-6}$ Torr. 3.5 nm of titanium and 8-14 nm of cobalt were then

evaporated on the substrates. The power was adjusted to obtain a deposition rate of about 5 Å/sec for both metals.

The silicide formation consisted of a two-step RTA anneal and a wet strip of the unreacted metal. The process conditions were optimized to obtain the lowest sheet resistance with minimal gate to source/drain bridging as described in Chapter 4. The first step RTA anneal was performed at 550 °C, 30 s. The RTA reactor chamber was purged for 5 minutes in nitrogen before each run. After the anneal, the chamber was unloaded when the temperature dropped below 200 °C. Typically after the anneal, the wafer appearance changed from a metallic silver to a duller light brown color.

When doing multiple runs, it was important to allow the chamber to cool in between runs particularly at the first step RTA. The chamber temperature had to be below 100 °C before the loading of the next wafer. If the chamber temperature was above 100 °C, poor silicide quality resulted probably due to a reaction with the residual oxygen in the chamber at the elevated temperature.

After the first step RTA, a strip of the unreacted metal was performed in a 4:1 $H_2SO_4/H_2O_2$ piranha solution. Finally, after the wet strip, a second step RTA at 700 °C for 60 s was performed. This anneal was less critical than the first step RTA anneal. The chamber was once again purged in nitrogen for 5 minutes prior to the RTA anneal. After the anneal was completed, the wafers were removed from the chamber when the temperature dropped below 400 °C.

It should be noted that after silicide formation, the exposure of the silicide surface to HF was minimized to avoid etching of the silicide. Even a 20 s exposure to 50:1 HF degraded the sheet resistance of the silicide Thus, the standard 50:1 HF dip in subsequent RCA steps was avoided. It appeared that buffered oxide etch

(BOE) was less harmful to the silicide and thus it was used for the wet contact hole etch described in the next section.

### A.2.4 Contact/Metallization

**Contacts:** The contact etch step was done in two steps. The first was an anisotropic oxide etch in a Lam Research Model 594 etcher. The selectivity of the plasma etch was about 3:1, $SiO_2$ to Si. The use of a silicide improved the selectivity of the etch somewhat. To avoid etching into the silicon film, a timed etch was used to etch most of the thickness of the oxide in the plasma etch with the recipe in Table A-4, and then an isotropic wet etch was used to complete the etch process. The etch rate of the plasma etcher varied somewhat from run to run so the etch rate had to be calibrated before each run. The oxide thickness measurement on silicided wafers was not accurate and thus non-silicided wafers were needed for the calibration of the etcher.

After the plasma etch, a short ~ 10 s etch in BOE was used to complete the opening of the contact holes. The wafers were then ashed, and ready for metallization.

**Metallization:** The pre-metal clean was a 3:1 $H_2SO_4$:$H_2O_2$ piranha etch. After the piranha etch, a short 3 s BOE dip was used to insure that there was no native oxide growth in the contact holes. At this point, the scribe lanes were checked for de-wetting as an indication of the removal of all remaining oxide. Note that silicided wafers do not de-wet so unsilicided wafers were used to monitor the etch. After the BOE etch, the wafers were immediately loaded into a Varian Model 3180 sputtering system for deposition of Al/1% Si metal. No barrier metal was used. Standard baseline aluminum pattern, etch (in Lam Research Model 680 with recipe in Table A-5) and sinter were used to complete the fabrication process.

Table A-1: Nitride plasma etch recipe parameters.

| Process Parameters | Step #1 | Step #2 | Step #3 | Step #4 | Step #5 |
|---|---|---|---|---|---|
| Chamber Pressure (mTorr) | 500 | 500 | 375 | 375 | 375 |
| Top Electrode RF Power (Watts) | 0 | 200 | 0 | 250 | 100 |
| Electrode Gap Spacing (cm) | 1.50 | 1.50 | 1.00 | 1.00 | 1.35 |
| $SF_6$ Flow Rate (sccm) | 0 | 0 | 50 | 50 | 60 |
| $O_2$ Flow Rate (sccm) | 200 | 200 | 0 | 0 | 0 |
| He Flow Rate (sccm) | 100 | 100 | 20 | 20 | 10 |
| Process Time | Stabl. | 6 sec | Stabl. | Endpt. | O/E 20 s |

Table A-2: Polysilicon plasma etch recipe parameters.

| Process Parameters | Step #1 | Step #2 | Step #3 | Step #4 | Step #5 |
|---|---|---|---|---|---|
| Chamber Pressure (mTorr) | 500 | 500 | 280 | 280 | 280 |
| Top Electrode RF Power (Watts) | 0 | 200 | 0 | 300 | 300 |
| Electrode Gap Spacing (cm) | 1.50 | 1.50 | 1.50 | 1.50 | 1.50 |
| $CCl_4$ Flow Rate (sccm) | 0 | 0 | 130 | 130 | 130 |
| $O_2$ Flow Rate (sccm) | 200 | 200 | 15 | 15 | 15 |
| He Flow Rate (sccm) | 100 | 100 | 130 | 130 | 130 |
| Process Time | Stabl. | 6 sec | Stabl. | Endpt. | O/E 1-5 s |

Table A-3: Backside polysilicon plasma etch recipe parameters.

| Process Parameters | Step #1 | Step #2 | Step #3 | Step #4 | Step #5 |
|---|---|---|---|---|---|
| Chamber Pressure (mTorr) | 50 | 450 | 450 | 250 | 250 |
| Top Electrode RF Power (Watts) | 0 | 0 | 100 | 0 | 75 |
| Electrode Gap Spacing (cm) | 1.20 | 1.20 | 1.20 | 1.20 | 1.20 |
| $SF_6$ Flow Rate (sccm) | 0 | 135 | 135 | 100 | 100 |
| $O_2$ Flow Rate (sccm) | 0 | 45 | 45 | 20 | 20 |
| He Flow Rate (sccm) | 0 | 0 | 0 | 0 | 0 |
| Process Time | 2 min. Stabl. | Stabl. | Endpt | Stabl. | O/E 40% |

Table A-4: LTO contact plasma etch recipe parameters.

| Process Parameters | Step #1 | Step #2 | Step #3 | Step #4 | Step #5 | Step #6 |
|---|---|---|---|---|---|---|
| Chamber Pressure (Torr) | 3 | 3 | 3 | 3 | 2 | 2 |
| Top Electrode RF Power (Watts) | 0 | 100 | 0 | 900 | 0 | 800 |
| Electrode Gap Spacing (cm) | 0.50 | 0.50 | 0.36 | 0.36 | 0.40 | 0.40 |
| $N_2$ Flow Rate (sccm) | 0 | 0 | 30 | 30 | 0 | 0 |
| $O_2$ Flow Rate (sccm) | 100 | 100 | 5 | 5 | 5 | 5 |
| He Flow Rate (sccm) | 200 | 200 | 125 | 125 | 60 | 60 |
| $CHF_3$ Flow Rate (sccm) | 0 | 0 | 30 | 30 | 10 | 10 |
| $CF_4$ Flow Rate (sccm) | 0 | 0 | 130 | 130 | 0 | 0 |
| Process Time | Stabl. | 10 s | Stabl. | Timed Etch | Stabl. | O/E 5 s |

Table A-5: Metal plasma etch recipe parameters.

| Process Parameters | Step #1 | Step #2 | Step #3 | Step #4 | Step #5 |
|---|---|---|---|---|---|
| Chamber Pressure (mTorr) | 220 | 220 | 220 | 220 | 220 |
| Top Electrode RF Power (Watts) | 0 | 175 | 0 | 135 | 135 |
| $BCl_3$ Flow Rate (sccm) | 90 | 90 | 90 | 90 | 90 |
| $N_2$ Flow Rate (sccm) | 0 | 0 | 10 | 10 | 30 |
| $Cl_2$ Flow Rate (sccm) | 40 | 40 | 27 | 27 | 20 |
| $CHCl_3$ Flow Rate (sccm) | 0 | 0 | 17 | 17 | 17 |
| Process Time | Stabl. | 10 s | Stabl. | Endpt. | O/E 65% |

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