Flexible and Solution-Processed Organic Thin Film Transistors for High Voltage Applications

by

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Abstract

6,13-Bis(triisopropylsilylethynyl)pentacene and pentacene high-voltage organic thin film transistors (HVOTFTs) were fabricated on solid and flexible substrates via a low temperature ($<$ 120 °C) solution-processed and vacuum-deposited fabrication methods, achieving breakdown voltages and on/off current ratios beyond -550 V and 10^6 A/A, respectively, a first of its kind. The HVOTFT design was based on a dual channel architecture, where a gated region enabled FET capabilities and an offset region accommodated the high-voltage. An HVOTFT capable of driving high-voltages ($|V_{DS}| > 100$ V) while being controlled by a relatively low gate-to-source voltage ($|V_{GS}| < 50$ V) will enable new applications on arbitrary and flexible substrates, such as large electrostatic MEMS actuators, electroactive polymers, novel displays, field-emitter arrays for digital x-ray imaging as well as photovoltaic systems on glass. A high-k dielectric $Bi_{1.5}Zn_1Nb_{1.5}O_7$ and a low-k organic dielectric parylene-C were incorporated into the HVOTFT process to improve threshold voltage and mobility. Field plate designs and self-assembled monolayers were also explored to enhance the HVOTFT's electrical characteristics by directly controlling the charge carrier distribution within the channel or by improving the charge carrier injection into the organic semiconductor. Moreover, a self-shearing drop cast deposition method has been employed for the HVOTFT for the first time, growing large and highly oriented organic semiconductor grains. Solution-processing will enable room-temperature, air ambient and large-area depositions techniques, reducing fabrication overhead. Furthermore, a self-aligned solution-processing method based on surface energy engineering was developed with self-assembled monolayers to create pre-patterned organic semiconductor channels without the need for etching.

Thesis Supervisor: Akintunde Ibitayo Akinwande
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To my beloved wife, Jeannie

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Chapter 1

Introduction

1.1 The Thin Film Transistor and its Liquid Crystal Display Integration

Over the years, thin film transistors (TFT) have received tremendous attention as an electronic device for numerous applications, particularly for large area electronics such as liquid crystal displays (LCD) [1]. More recently, TFTs have found themselves in novel applications such as flexible displays, radio frequency identification (RFID) tags, as well as TFT-MEMS integrated systems [2]–[4]. The concept of making a series of thin layer depositions on seemingly arbitrary substrates enables flexible, cheap and large area electronics, a market not easily dominated by bulk semiconductor devices such as the silicon (Si) MOSFET (metal-oxide-semiconductor field-effect transistor). Although Si MOSFETs have proven vital in high speed, low power, logic and memory applications, they remain largely contained within black box devices like the smartphone or the laptop [5]–[12]. Currently, there are countless systems such as automotive shells, robotic exoskeletons, glass windows, and fabrics, among others, that do not have embedded electronics due to the lack of maturity of the TFT technology, particularly relating to the flexibility and the reliability of high electrical performances. Thus, an argument can be made that the continual advancement of the TFT technology to compliment the Si MOSFET is necessary to achieve a truly-ubiquitous electronics world.

As far back as 1973, researchers have developed the CdS and CdSe high mobility TFT of > 40 $cm^2/V{\cdot}s$ for LCD integration [13]. However, due to issues with the control of the alloy, the TFT industry had to wait until 1979 for the development of hydrogenated amorphous silicon (a-Si:H) deposited by plasma enhanced chemical vapor deposition (PECVD) to drive LCDs in active matrix liquid crystal displays (AMLCDs), shown in Fig. 1-2 [13]. a-Si:H TFT exhibits mobilities of 0.5-1 $cm^2/V{\cdot}s$, considerably lower than its CdS/CdSe predecessors, and even lower than its crystalline bulk Si MOSFETs; however, such mobilities proved sufficient to drive LCD pixels at 120 Hz. Interestingly, only 10 years separated the first research publication of the a-Si:H TFT and its universal adoption in commercial production, initiated by a joint venture between IBM and Toshiba. Moreover, the TFT driven LCD market went from $1B in 1989 to $110B in 2012, with many display companies originating in Eastern Asian countries [13].

Although TFTs do not directly compete with the MOSFET, comparing the two devices shown in Fig. 1-1 can provide insight on the novelties of the TFT. For one, the TFT device layers are grown layer by layer on top of a carrier substrate that typically does not increase or modify the device performance. This greatly enhances the potential for large area electronics on flexible, cheap, disposable, and/or biodegradable substrates. For example, 2009's generation 10 glass substrates of several meters squared have been adopted as the industry standard [1]. Secondly, the active semiconductor channel (typically amorphous or polycrystalline) is deposited over such a substrate as opposed to being formed by an ion implantation into a bulk crystalline semiconductor wafer. This results in lower electrical performance, in terms of transconductance, threshold voltage and subthreshold swing, but does simplify the fabrication procedure. Thirdly, TFT requires significantly less processing steps and photolithography masks than modern CMOS (around 5 compared to 25), endowing it with the desirable quality of being cheap and therefore suitable for large area electronics.

Several materials have been investigated as potential candidates for TFT technology. Polycrystalline Si (poly-Si) has emerged as a high mobility alternative with mo-

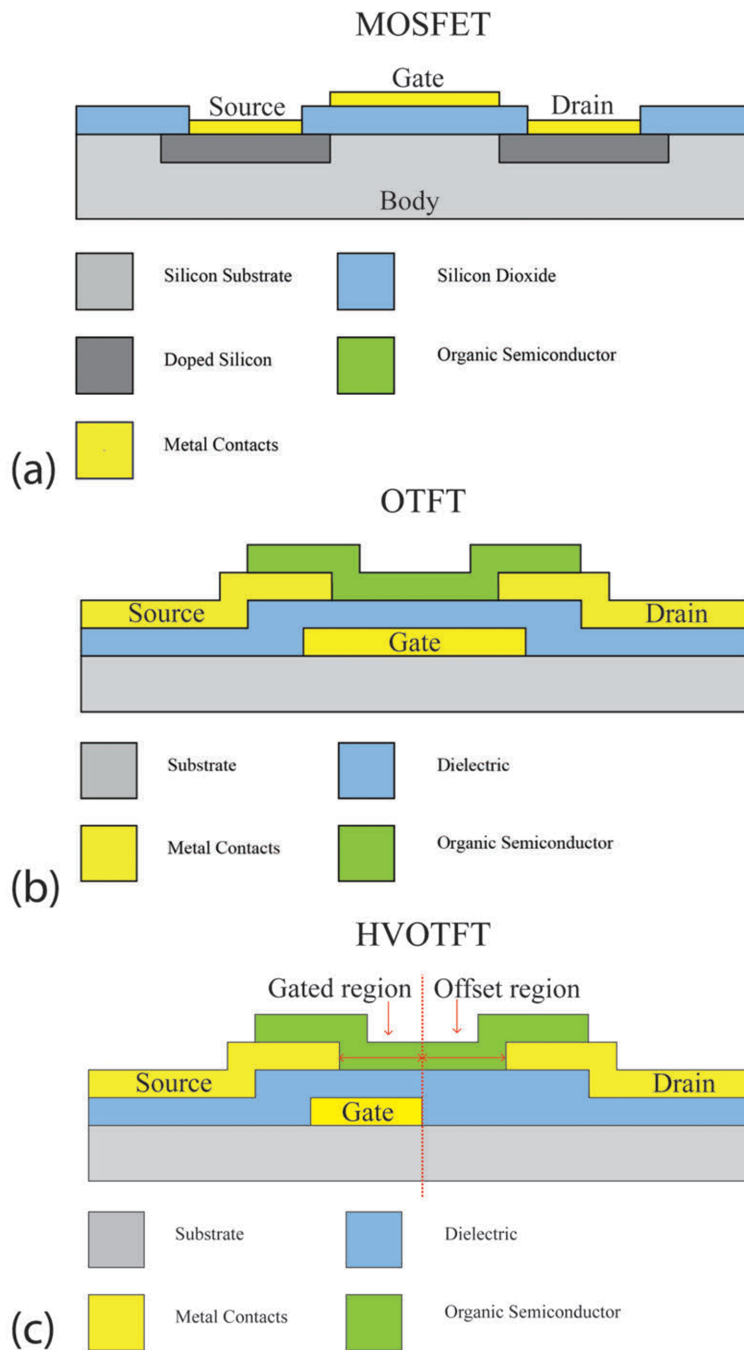


Figure 1-1: Cross-sectional diagrams for the (a) MOSFET, (b) OTFT and (c) HV-OTFT.

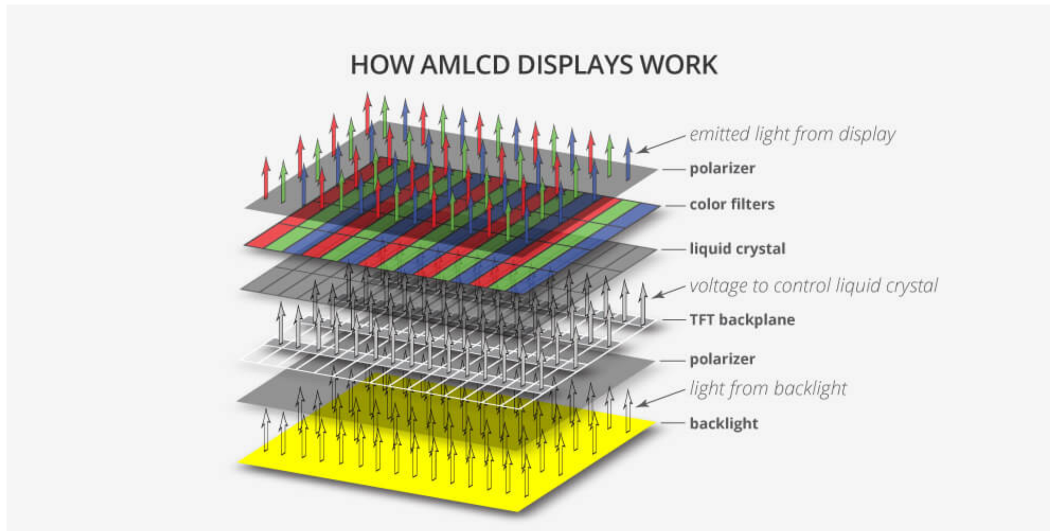


Figure 1-2: TFT for backplane LCD applications [14].

bilities routinely between 5 and 120 cm^2/V·s, and more recently reaching 900 cm^2/V·s due to having large grain sizes [15]. Such high mobilities enable more sophisticated System-on-Glass (SOG) applications such as photovoltaic-SOG (PV-SOG) as well as hand-held active-matrix organic light-emitting diode (AMOLED) displays. Typically, poly-crystallization of Si is achieved by excimer laser crystallization (308 nm), resulting in grain sizes of approximately 300 nm [16].

Amorphous metal-oxides have also received considerable attention for TFTs due to their relatively high mobility (10-20 cm^2/V·s), which results from the nature of their ionic bonding and small electron effective masses, and their uniform electrical properties compared with poly-Si which is grain dominated [17]. A common metal oxide used is the a-InGaZnO system.

Finally, this brings us to the most unique material system of organic semiconductors which is the focus of this dissertation. Since the discovery of conductive polymers and conjugated polymers in the 1970s and 1980s respectively, a large number of academic and industry research has been pushing for mature and commercially viable organic thin film transistor (OTFT) technology, particularly for displays [18]. The 1977 discovery of polyacetylene, and its subsequent doping, resulted in Alan J. Heeger, Alan G. MacDiarmid and Hideki Shirakawa to jointly receive the Nobel Prize in Chemistry in 2000 [19]. A key turning point was in the late 1990s when pentacene

OTFTs started to match and eventually surpass a-Si:H TFT's mobility, demonstrating the potential of the material system [20]. Besides being on-par or superior in electrical behavior compared to a-Si:H, organic semiconductors show promise for large area and room temperature processing, as well as lightweight, biodegradable, and flexible capabilities. It is this promise of providing flexible electronics that has proven to be the most interesting and viable niche market for the OTFT, shown in Fig. 1-3. Furthermore, large area and room temperature processing can significantly lower the cost of fabrication by having reduced materials cost, less sophisticated equipment, less stringent cleanroom environments and simpler manufacturing technologies [21]. Although there are very little commercialization of OTFT currently, large amounts of applications have been demonstrated in proof-of-concepts, such as OTFT driven AMOLED, LCD and flexible electronic paper display (EPD), as well as X-Ray imagers, RFID tags and various sensors [2], [3], [22], [23]. Several leading display companies, including LG and Sony, have been conducting research and development on OTFT technology for future novel displays [24]. In fact, in 2007, Sony was the first to demonstrate a flexible AMOLED display with integrated OTFTs [25]. Moreover, in 2017, Germany's SmartKem partnered with Taiwanese manufacturers to develop and produce OTFT-based flexible displays [24]. Hence, there is large potential for OTFT commercialization; however, there are several technological challenges that prevent the maturity of such technology: limited charge carrier mobility, high contact resistance, high operating voltage, lack of complimentary transistors (particularly n-type), reliability, stability, standard fabrication procedures, and overload in material choices [25]. Concerning the last two issues, there is currently no consensus on the best fabrication method let alone which organic semiconductor would be best suited for large area flexible applications. Such choices inevitably slow large scale manufacturing. A description of the myriad of choices is presented in section 1.3.

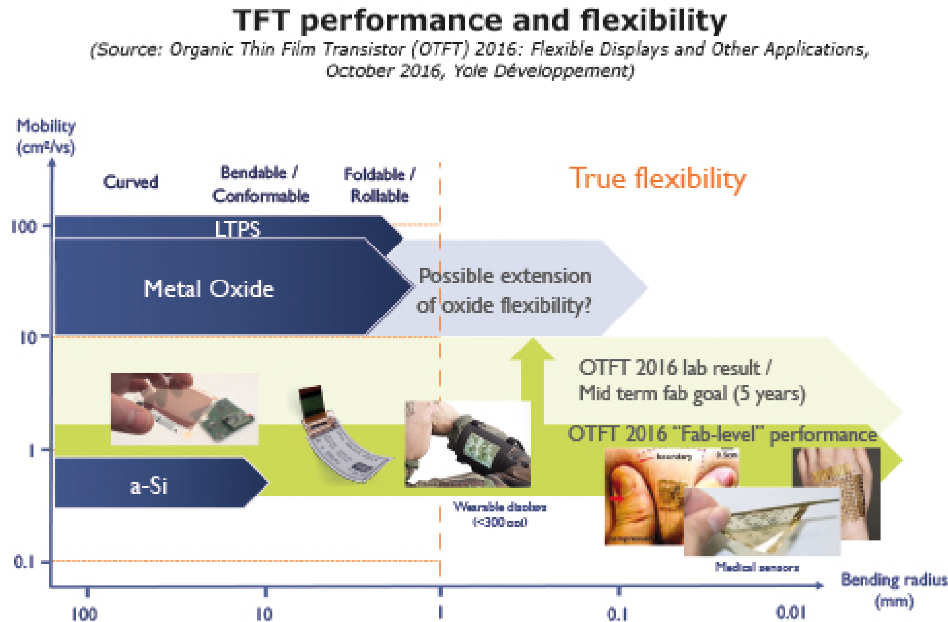


Figure 1-3: TFT performance and flexibility [26].

1.2 MEMS Integration with TFT

The majority of the market share for TFT is still mostly focused on electronic displays. However, TFT-driven microelectromechanical systems (MEMS) are being explored as a potential new application. Whereas CMOS technology is pursuing increased miniaturization below 10 nm, TFT technology thrives at the micro- and meso-scales in which MEMS are also part of. Moreover, TFT fabrication processes are compatible with that of MEMS. Typically, a post-TFT MEMS process is employed, in which the TFT is made front-end-of-line (FEOL), followed by a surface passivation, shown in Fig. 1-4. The MEMS are then built on top of the TFT as back-end-of-line (BEOL), with organic layers used as sacrificial and release layers [4].

The idea of MEMS integration with TFT is relatively new. The ability to drive MEMS devices directly on arbitrary substrates is extremely appealing and can lead to new flexible MEMS applications. Integration of MEMS on TFT has been first demonstrated by Pixtronix (Qualcomm Technologies affiliated) for displays. In this case, Pixtronix developed a digital microshutter (DMS) that removed the require-

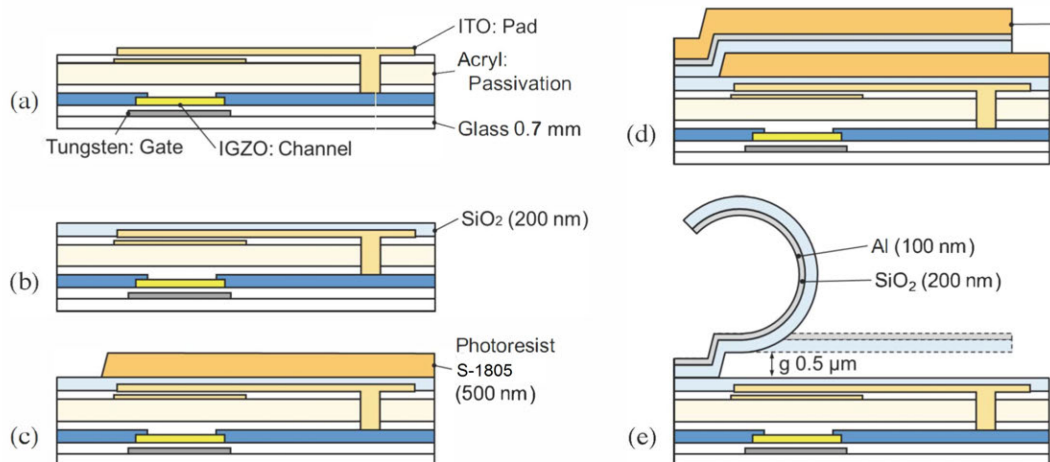


Figure 1-4: Example of post-TFT MEMS process [4].

ment of a polarizer in traditional LCDs and that improved response times, seen in Fig. 1-5 [27]. Furthermore, applications for TFT driven MEMS go beyond display technology [4]. The typical high output voltage of TFT lends itself directly to driving large electrostatic MEMS actuators, devices that require electrostatic forces for large deformation, either linearly or rotationally [4], [28]. Potential applications may include lab-on-a-chip microfluidics for biomedical sciences, artificial muscles for robotics, shape shifting materials, optical micro-mirrors, tunable shutter blades, and tunable RF capacitors [4], [28]–[30].

1.3 Introduction to Organic Semiconductors and the Organic Thin Film Transistor

The very first organic transistor was developed by Koezuka et al. back in 1987 and was based on a polythiophene organic semiconductor [32]. Since then, organic semiconductors (carbon-based) have become an emerging material system that aims to replace or compliment a-Si:H in key applications such as backplane display drivers in AMOLED, LCD and EPD. Their lower electrical performance compared with bulk Si CMOS is balanced by their potential for extremely low cost fabrication, allowing organics to exist in a different application space, illustrated in Fig. 1-6 and 1-7. Their

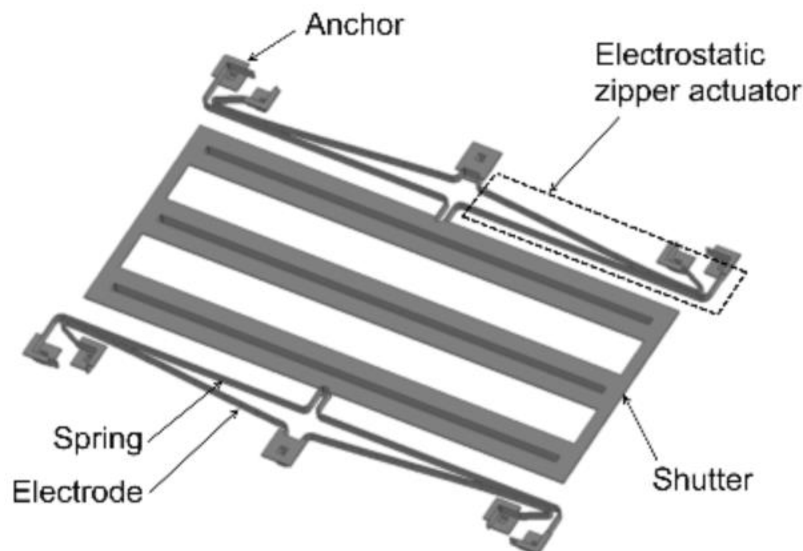


Figure 1-5: Digital MicroShutter from Pixtronix [31].

affinity for flexible, large-area and room temperature processing has attracted many researchers and companies to develop robust and reliable organic systems. Organic semiconductors have been implemented in organic light-emitting diodes (OLEDs), organic photovoltaics (OPV), as well as OTFTs. However, the development of organic semiconductors is impeded due to limited charge carrier mobility, high contact resistance, high operating voltage, lack of complimentary transistors, reliability, stability, standard fabrication procedures, and an overload in material choices.

1.3.1 Conjugated Molecular Systems

Electrically conducting and semiconducting organic molecules all have a conjugated molecular structure, consisting of alternating single and double carbon-carbon covalent bonds. A typical building block for an organic semiconductor is the conjugated benzene ring, C_6H_6. For each carbon atom in such a molecule, its orbitals of 2s, $2p_x$, $2p_y$, and $2p_z$ form three sp^2 hybridized orbitals and one 2p orbital. The three hybrid sp^2 orbitals form the basis of the benzene ring with σ-bonds between the two other carbon atoms and the single hydrogen atom. The single 2p orbital, on the other hand, forms a π-bond in the second half of the double covalent bond, but in an out of plane fashion. Due to the overlap of the π-bond between adjacent carbon atoms, the elec-

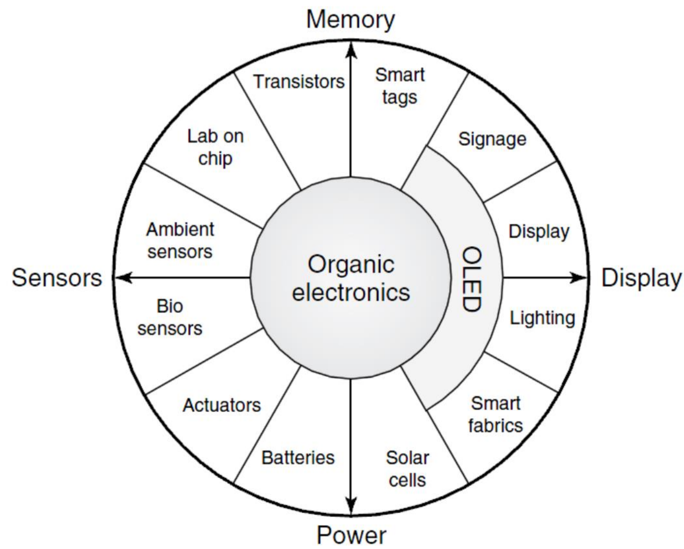


Figure 1-6: List of applications derived from organic semiconductors, including display, memory, power and sensor technology [21].

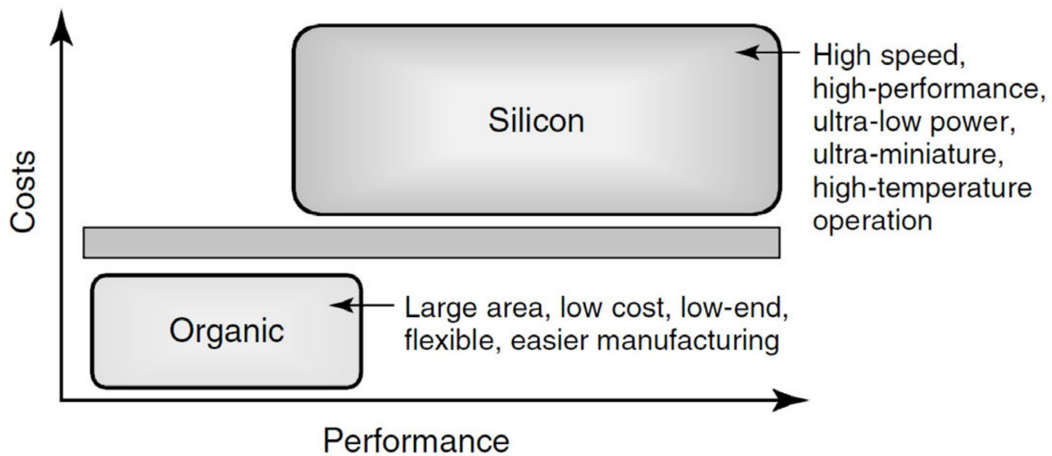


Figure 1-7: Cost vs. performance of organic semiconductors and Si. Although organic semiconductors have lower mobility than crystalline Si, there exists a large market that is available to organics [21].

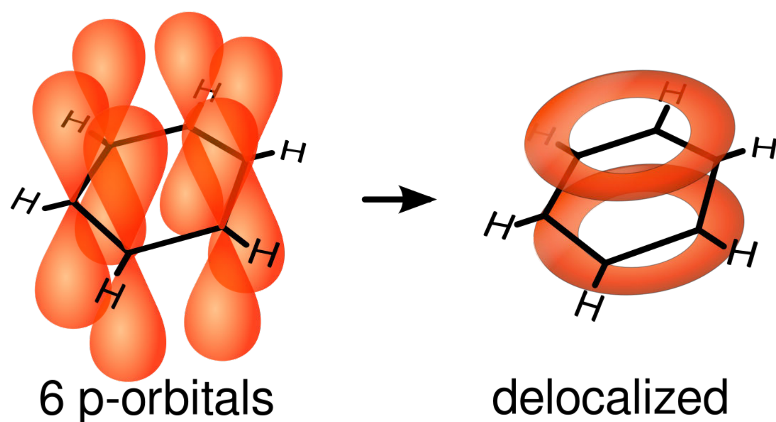


Figure 1-8: Delocalization of electrons along a conjugated benzene ring, allowing charge flow in organic semiconductors [34].

trons are weakly localized (i.e. delocalized) about the ring. This phenomenon called resonance is the basis for the conduction of charge carriers along the organic molecule, shown in Fig. 1-8 [33]. Benzene rings may be fused together to form acene rings, such as pentacene (five benzene rings covalently bonded together). Other conjugated molecules like thiophene, C_4H_4S, are also efficient building blocks for organic semiconductors such as polythiophene and poly(3-hexylthiophene) (P3HT). The conjugated molecular structure also results in the separation of bonding and anti-bonding states, leading to empty and filled π-orbitals, separated by a band gap E_G with typical values between 1 and 4 eV. In the study of organic semiconductors, the conduction band and valence band are referred to as the lowest unoccupied molecular orbital (LUMO) and highest occupied molecular orbital (HOMO).

1.3.2 Molecular Organization

To achieve charge conduction through an organic semiconductor, organic molecules need to come together, forming either a material that is amorphous, poly-crystalline, or crystalline. The higher the degree of crystallinity for organic small molecules, the stronger the electronic coupling between adjacent molecules becomes, resulting in better intermolecular transport [35]. In general, organic semiconductors are grown as

amorphous or poly-crystalline, which is why OTFT mobilities typically vary between 0.01 and 10 $cm^2/V{\cdot}s$. There are schemes to improve molecular packing and electronic coupling by selecting appropriate organic molecules and/or using self-assembled monolayers to promote a certain surface growth orientation [36].

1.3.3 Metal/Organic Contacts

Although there are recent attempts in actively doping organic semiconductors to introduce n- or p-type free chargers, typical organic semiconductors are left undoped due to the difficulty of such a procedure. In this case, in an undoped semiconductor, the channel behavior will be dictated by the metal/organic contacts and the alignment of the Fermi level of the metal contact with the band edges of the semiconductor. If the Fermi level of the metal is aligned to the HOMO level of the semiconductor, holes will be injected and the semiconductor is said to be p-type. On the other hand, if the metal Fermi level is aligned with the LUMO level, electrons will be preferentially injected into the channel, resulting in an n-type semiconductor. If the metal Fermi level aligns itself in between the HOMO/LUMO level, the device now operates in an ambipolar fashion, as shown in Fig. 1-9. Metal contact / organic interface engineering is critical in reducing either the hole injection barrier ϕ_h, the difference between metal work function and the ionization energy of the organic semiconductor, or the electron injection barrier ϕ_e, the difference between metal work function and the electron affinity. Further complications arise in energy level matching during practical fabrication, as there is usually a dipole barrier formation at the interface of the metal contact and the semiconductor due to impurities and environment exposure, as indicated in Fig. 1-10. For example, gold is the typical metal contact for OTFTs due to its cited 5.1 eV work function [37]. Such a work function aligns well with most HOMO levels of organic semiconductors, allowing for hole injection from source to channel. However, it is widely known that the exposure of gold to air or organic solvents produces a dipole barrier of 0.7 eV, reducing the effective work function to 4.4 eV [38]. Such a dipole barrier is usually attributed to the push back effect: the electron density exponentially decreases beyond the surface of the metal which results,

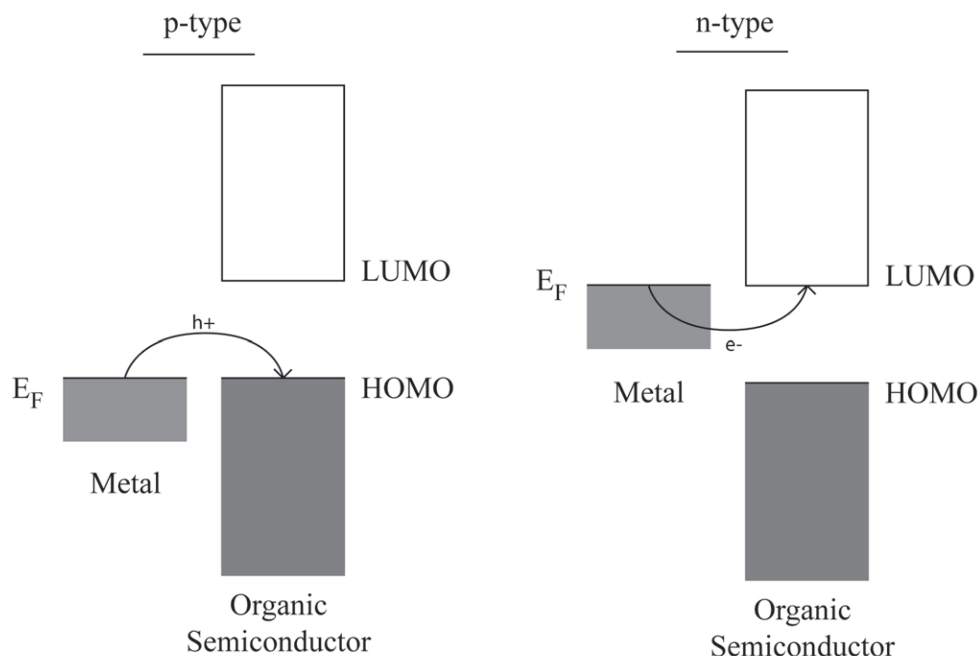


Figure 1-9: Different operating behavior of undoped organic semiconductors, depending on the work function of the source contact.

from charge neutrality, in a lower electron density at the surface [38].

1.3.4 Carrier Transport

It has been defined that carrier transport in organic semiconductors are largely dependent on the molecular organization, and whether or not there is good intermolecular π-π coupling. Additionally, charge carrier mobility is usually dependent on temperature, trap filling from gate bias and injection barrier height lowering from source-drain bias.

Unlike crystalline Si CMOS where increased temperature leads to increased phonon generation and thus perturbation of the electronic wave function, amorphous or polycrystalline organic semiconductors benefit from increased temperature. Charge transport in organics are usually modeled with a hopping process or a multiple trapping and release (MTR) model, which describes a thermal activation process to have charge

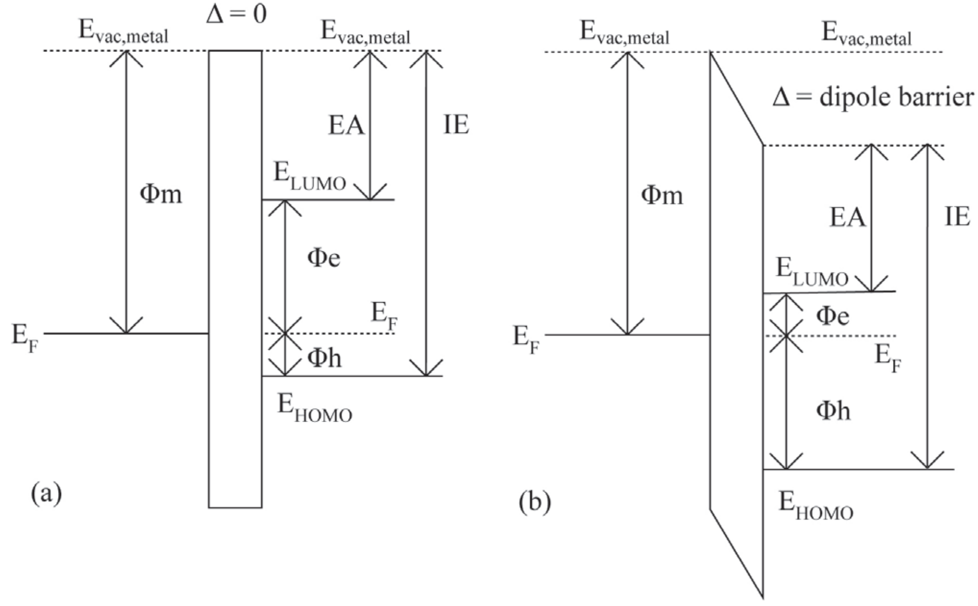


Figure 1-10: Band diagrams of the metal/semiconductor interface, where EA and IE are the activation energy and ionization energy respectively, with (a) no dipole barrier δ and with (b) metal induced dipole barrier. A dipole barrier can increase the hole injection barrier ϕ_h [39].

carriers hop from one molecule to another. The field-effect mobility is described by:

$$\mu = \mu_0 A e^{-E_A/kT} \tag{1.1}$$

where μ_0 is the trap-free mobility, A is a proportional constant representing the fraction of carriers that are either in traps or in the band, E_A is the activation energy for molecular hopping, k is the Boltzmann constant and T is the temperature. It is important to note that as the organic semiconductor becomes crystalline, the thermally activated field-effect mobility is no longer valid, and a decrease in mobility is observed. Mobility also exhibits a dependence on charge carrier density, supplied by the gate bias V_{GS}. Increased charge carrier allows the filling of traps, resulting in an expression for mobility as:

$$\mu(V_G) = \mu_0 \left(\frac{V_{GS} - V_T}{V_{AA}}\right)^{\gamma} \tag{1.2}$$

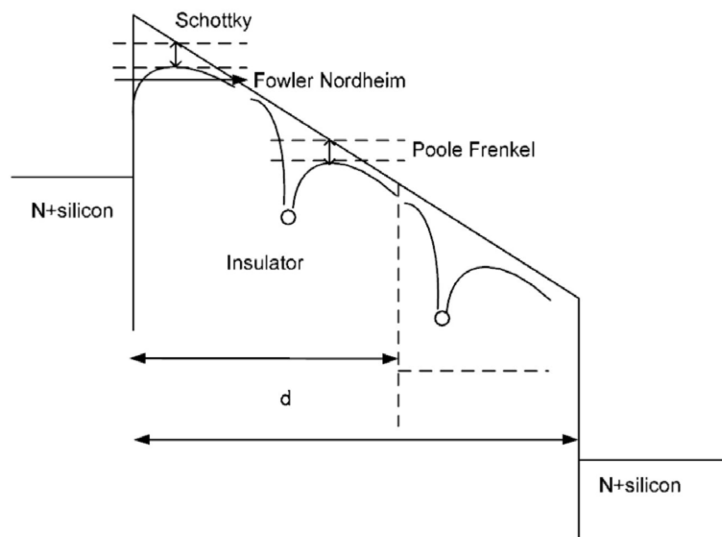


Figure 1-11: Energy barrier lowering of trap states by the Poole-Frenkel effect [40].

where γ is the mobility enhancement factor, V_{AA} is an experimentally fitted parameter and V_T is the threshold voltage.

Poole-Frenkel transport is also present in organic semiconductors, in which lateral fields decrease the energy barrier heights of trap states, allowing for either a tunnel transfer between traps or an easier thermally assisted hopping, shown in Fig. 1-11. Typically, electric fields of $>10^5$ V/cm are required for Poole-Frenkel transport [37]. This results in electric field enhanced mobility in organics, described by:

$$\mu(E) = \mu_0 e^{\frac{q}{kT}} \beta\sqrt{E} \tag{1.3}$$

where $\beta = (\pi\epsilon_0)^{-1/2}$ is the Poole-Frenkel factor.

1.3.5 Small Molecule vs. Polymer

Organic semiconductors are classified into two categories: small molecule and long molecule (polymer), seen in Fig. 1-12. Small molecules are defined as organic compounds with a low molecular weight, low enough for them to diffuse through cell membranes. These molecules tend to grow in a well-ordered fashion, achieving relatively high mobilities. Pentacene is one of the most researched small molecules,

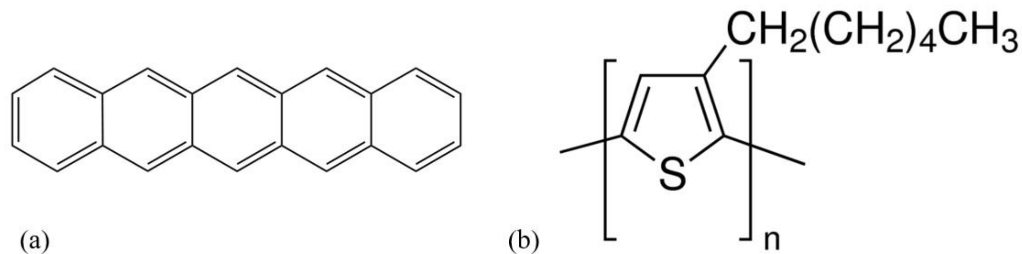


Figure 1-12: Organic semiconductors are classified as either (a) small molecules (e.g. pentacene) or (b) polymers (e.g. P3HT).

achieving mobilities as high as 5 $cm^2/V{\cdot}s$ due to improved dielectric/semiconductor interfaces [41]. Polymers, on the other hand, are long molecular chains with structural stability and high degree of solubility for solution-processes. Due to their long nature and difficulty in producing well-ordered grains, their mobilities are typically an order of a magnitude lower than small molecules. P3HT is a typical polymer organic semiconductor.

1.3.6 N-Type

A big limitation for organic semiconductors is the ability to form complimentary circuits with n-type and p-type devices. The majority of organic semiconductors make p-type devices due to their band structure and its alignment with the work function of typical IC metal contacts. Low work function metals such as Al, Mg, and Ca do exist; however, they tend to oxidize easily and may react with the organic semiconductor directly [42]. Furthermore, n-type semiconductors have poor environment stability due to its lower electron affinity, allowing them to react with O_2 and H_2O [43], [44]. Nonetheless, there have been advances in developing n-type organic semiconductor devices, which can generally be made through three different ways. Examples of n-type organic semiconductors are shown in Fig. 1-13. Firstly, one can identify organic molecules with adequately low HOMO levels to align itself with low work function metal contacts. Fullerene (C_{60}) and its derivatives, teracyanoquinodimethane (TCNQ) and its derivatives, perylene derivatives, and halogenated metal phthacoyanines are widely studied n-type organic semiconductors [45]–[49]. Secondly,

one can functionalize the p-type material with electron-withdrawing groups such as cyano and perfluoroalkyl to shift HOMO levels down [50]. Researches have fluorinated copper phthalocyanine (CuPc) to copper hexadecafluorophthlocyanine (F_{16}CuPc), cobalt hexadecafluorophthalocyanine (F_{16}CoPc), and zinc hexadecafluorophthalocyanine (F_{16}ZnPc), achieving mobilities on the order of 1 $cm^2/V{\cdot}s$ [50]. And thirdly, one can introduce dopants to either increase electron carrier density or to suppress hole carrier mobility in ambipolar devices, as depicted in Fig. 1-14 [44]. N-type doping operates through one of three mechanisms: charge transfer, charge carrier trapping and charge carrier scattering, depending on the relative HOMO/LUMO levels of the dopant and the organic semiconductor, described below [44]. P-type doping operates in the same manner, but with flipped relative positions. Charge transfer can occur from the dopant to the organic semiconductor when the HOMO of the dopant is higher than the LUMO of the organic semiconductor. Charge carrier trapping occurs when the HOMO of the dopant is found between the LUMO/HOMO levels of the organic semiconductor. In this case, there is no increase in electron carrier density, but a generation of either shallow or deep hole traps, of which injected holes from the source may find themselves in. This would effectively reduce the hole mobility, turning an ambipolar device into a purely n-type device. Finally, in the case of the HOMO level of the semiconductor finding itself between the LUMO/HOMO levels of the dopant, no electron transfer or hole trap generation would occur. Instead, the low HOMO level of the dopant would form an energy barrier that would cause scattering of injected holes from the source. Wei et al. was able to dope [6,6]-Phenyl C_{61} butyric acid methyl ester ($PC_{61}BM$), an already n-type semiconductor, with (4-(1,3-dimethyl-2,3-dihydro-1H-benzoimidazol-2-yl)phenyl)dimethyl-amine (N-DMBI), effectively increasing its electron mobility [51].

1.3.7 OTFT Architecture

Without an active substrate, the thin films of a TFT can be layered in various way to create different TFT architectures, namely bottom gate / top contact (BG/TC), bottom gate / bottom contact (BG/BC), and top gate / bottom contact (TG/BC),

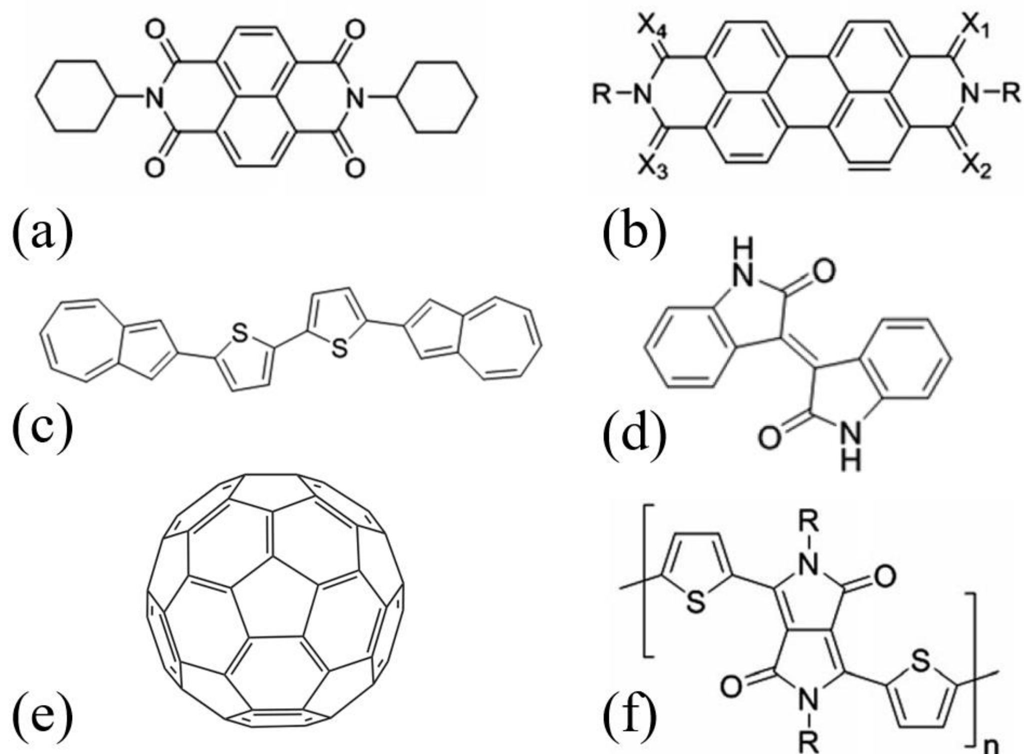


Figure 1-13: Examples of organic semiconductors with n-type characteristics. (a) Naphthalene tetracarboxylic diimide, (b) perylene diimide, (c) azulene derivative, (d) isoindigo derivative, (e) fullerene, and (f) diketopyrrolopyrrole (DPP)-based polymers.

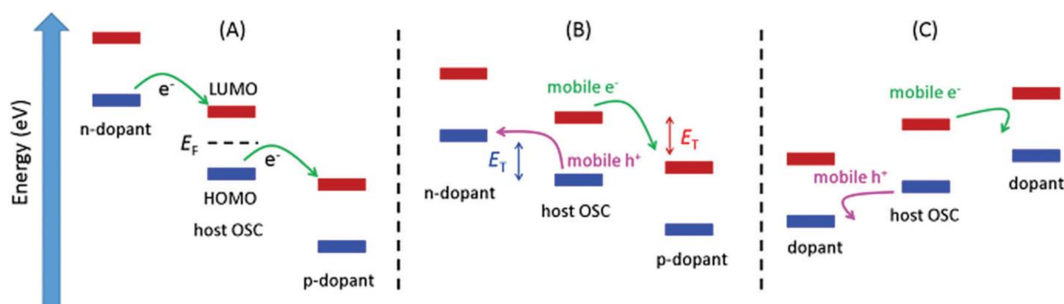


Figure 1-14: Three possible dopant schemes to modify the Fermi level in organic semiconductors [44].

shown in Fig. 1-15. There has been much debate on which architecture would prove the best for a TFT, ultimately depending on the exact layer composition and contact resistance.

With BG/BC, the organic semiconductor can be deposited and patterned above all other layers, avoiding thermal budget limitations and being able to achieve small channel lengths. Issues arise when organic semiconductors are grown over a discontinuity in materials, for example, across the metal contact and the dielectric. Pentacene was found to grow flat on the gold while growing near vertical on SiO_2, leading to distinct grain growth and a high contact resistance. Organothiol self-assembled monolayers (SAMs) were effective in modifying the surface energy of gold, leading to a more continuous grain of pentacene across the gold and SiO_2 [36]. The BG/TC architecture has been employed in the literature for its simplicity. However, depositing metal contacts directly on top of the organic semiconductor has led to unwanted damage through thermal dissipation. Furthermore, organic solvents and/or metal etchants may damage the organic layers, leading to the use of a shadow mask for metal evaporation [52]. However, channel lengths of only 10-20 μm can be achieved with a shadow mask. The TG/BC architecture is rarely used, but can provide the additional advantage of using the top gate layer as an encapsulation layer.

1.3.8 Fabrication Process

OTFT fabrication processes follow the typical material deposition (by either e-beam evaporation, sputtering, PECVD, etc.) with subsequent patterning via photolithography and etching (dry or wet). The organic semiconductor can either be vacuum thermally evaporated, as in the case of pentacene, or deposited via a solution-process, like for 6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene or TIPS-pen). Solution processing avoids vacuum and high temperature processes, and lends itself for large area and cheap electronics. It involves dissolving the organic semiconductor in a solvent, and using this solution to transfer to semiconducting material to the substrate. Solution-based deposition techniques involve drop casting, spin coating, direct printing (ink-jet printing, spray coating, etc.) and meniscus-guided coating

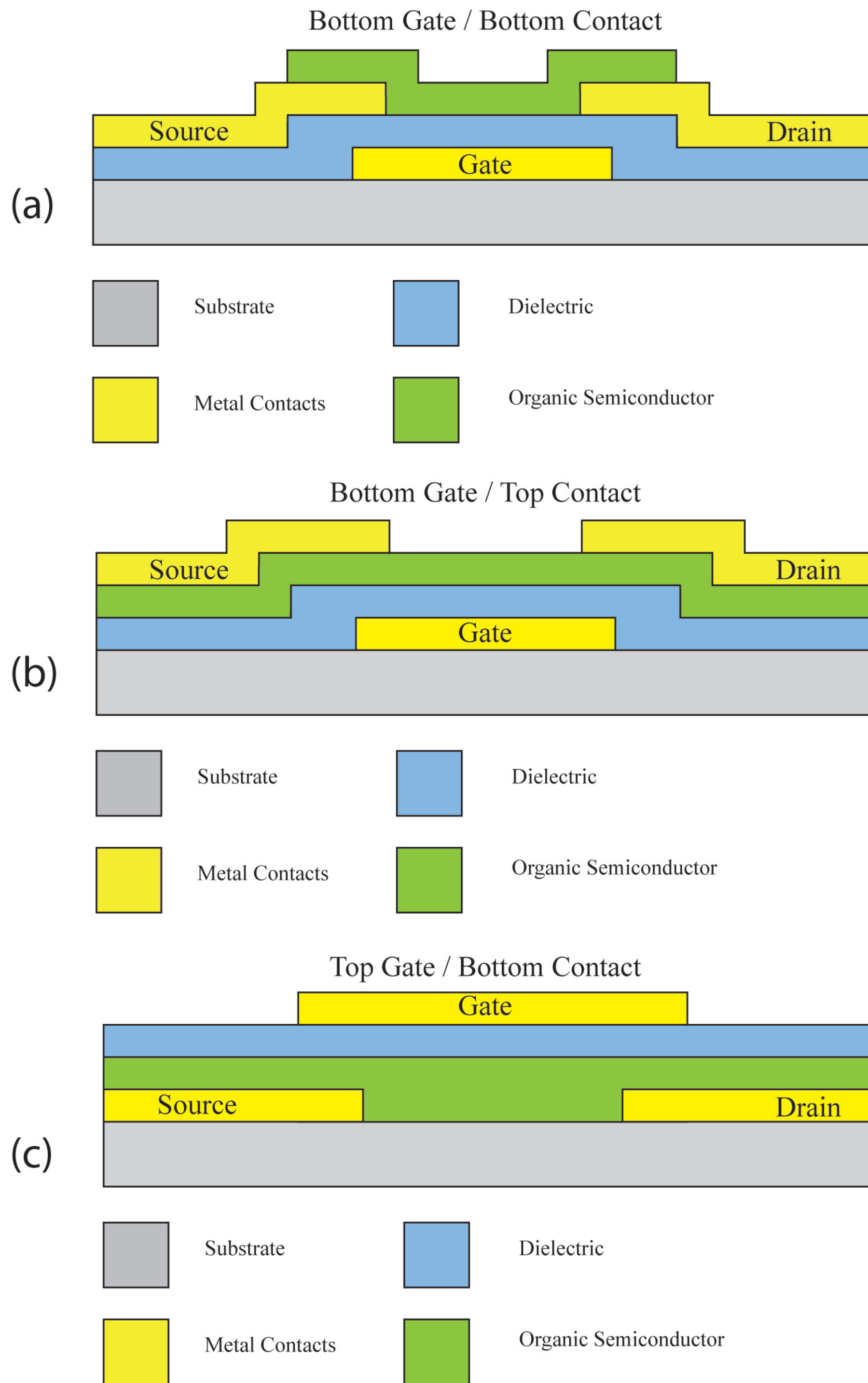


Figure 1-15: OTFT architectures: (a) bottom gate / bottom contact (BG/BC), (b) bottom gate / top contact (BG/TC) and (c) top gate / bottom contact (TG/BC).

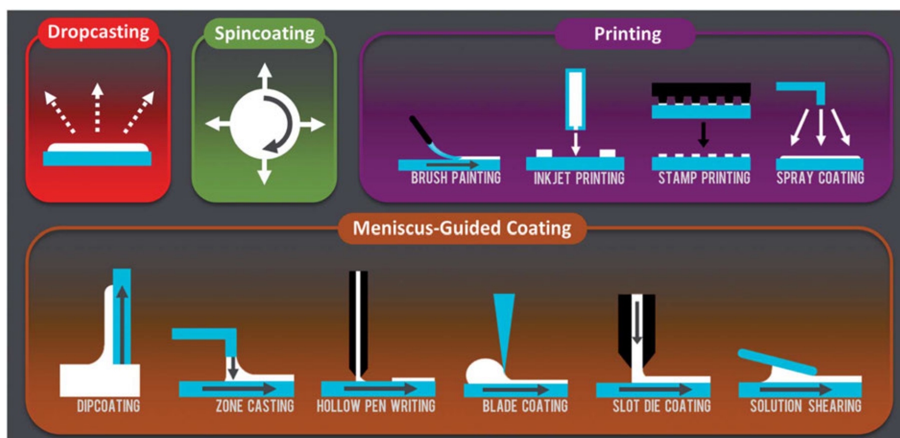


Figure 1-16: Various solution-processing techniques can be employed to deposit organic semiconductors [53].

(dip coating, zone casting, solution shearing, etc.), summarized in Fig. 1-16 [53].

A general issue with solution processing is the ability to pattern the organic semiconductor with standard photolithography, due to the solubility of the organics in traditional solvents such as acetone, ethanol and isopropyl alcohol. Patterning of the organic semiconductor is desired to have well defined channel regions and transistor to transistor isolation. Drop casting and spin coating, although simple, have varying successes in forming uniform layers of organic semiconductors, particularly with the coffee stain effect [54]. Thus, even under an encapsulation layer, the organic semiconductor is only protected from solvents to some degree. Other solution-processing methods such as ink-jet printing can deposit the organic semiconductor on selective regions of the sample without the need of photolithography. Recent studies have looked into the use of surface wettability and solvent evaporation rate variations to control where organic semiconductors are deposited, a method called self-aligned solution-processing [55]. Choi et al. utilized a spin coating technique coupled with a low surface energy dielectric called CYTOP to create a dewetting force to counter the centrifugal force during spin coating [55]. The OTFTs fabricated as part of this dissertation have been made using the thermal evaporation of pentacene as well as a self-sheared and self-aligned drop casting of TIPS-pentacene.

1.4 High-Voltage Organic Thin Film Transistor (HVOTFT) and Applications

Organic semiconductors have been identified as viable materials for flexible, cheap, and large-area electronics, even though there is a current lack of process and manufacturing maturity as well as complimentary logic for widespread commercialization. Their interest stems from the desire to explore electronics on arbitrary and flexible substrates which would enable a truly-ubiquitous electronics world outside of Si-based devices. Although transport properties of OTFTs in terms of charge carrier mobility are comparable to a-Si:H TFTs, there are currently very few efforts to broaden their performance capabilities to include high drive voltages $|V_{DS}| > 100$ V. Such high-voltages would help diversify the capabilities of TFT technology and broaden its application potential. Currently, the majority of OTFT research is geared towards low-voltage ($|V_{DS}| < 5$ V) for low power and portable devices [56]. Of particular interest in this dissertation is the development of a flexible and solution-processed high-voltage organic thin film transistor (HVOTFT), with its cross-sectional diagram shown in Fig. 1-1 (c). This new device is characterized by the ability to drive voltages beyond -100 V across its channel (V_{DS}) while having FET properties controlled by a relatively low gate voltage (V_{GS}).

There are numerous applications that would benefit from the ability to have high-voltage driving in a TFT technology platform. Novel display systems such as ferroelectric liquid crystals, electrophoretic and electro-optic displays, as well as MEMS-based braille displays for the visually impaired require relatively large driving voltages for pixel activation [57], [58]. Digital X-ray imaging is another domain that would benefit from the introduction of HVOTFTs used as the drivers for field emitter arrays (FEAs) or as a fault detection system, shown in Fig. 1-17 [59], [60]. Furthermore, photovoltaic systems-on-glass (PV-SOG) can be coupled with high-voltage thin film transistors (HVTFTs) in micro-inverter technology, where each module would have an optimized embedded inverter to do DC-AC conversion [61]. The typical DC input voltages for power inverters are several hundreds of volts.

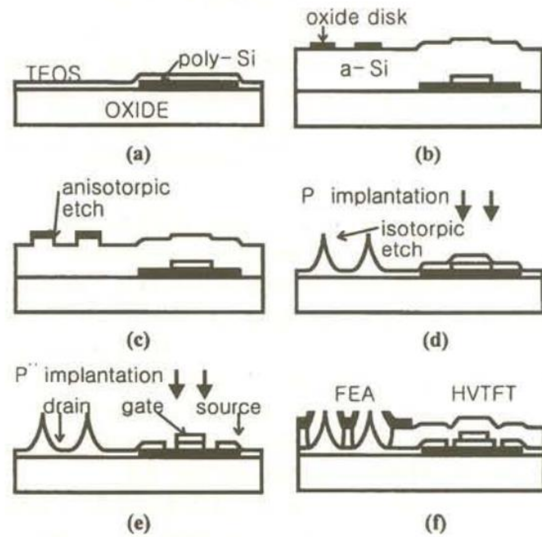


Figure 1-17: Fabrication process for field emitter array integration with HVTFT [59].

However, the most viable application for high-voltage in OTFTs is the ability to drive large electrostatic MEMS actuators on arbitrary and flexible substrates. The integration of MEMS and HVOTFTs, initially described in section 1.2, would allow for not only large displacement of large structures under large applications of force, but the ability to do this on flexible and low-temperature substrates. This is demonstrated in Fig. 1-18 and 1-19. One can imagine applications in shape shifting materials (form or function) in, say, embedded fabrics, or the wing of an aircraft for aerodynamic optimization. For example, Si MEMS roll up blind arrays have been recently demonstrated for energy and light management, which require above 100 V for release and pull-in mechanism, seen in Fig. 1-20 [62]. Macro-scale actuation can also be used in microfluidics, valves, ejectors, scanners, gears, micro-mirrors and variable capacitors [28].

Dielectric electroactive polymers (EAPs) are also of high interest for HVOTFT integration for actuation and power generation. EAPs are shapeable, deformable, flexible and low-cost polymers with uses in artificial muscles for robotics as well as MEMS devices [28], [62]–[64]. EAPs can be deformed by an electrostatic-initiated squeeze or by interaction with the dipole moments found in polymer chains to create rotational forces. In 2003, researchers from Princeton University used actuated

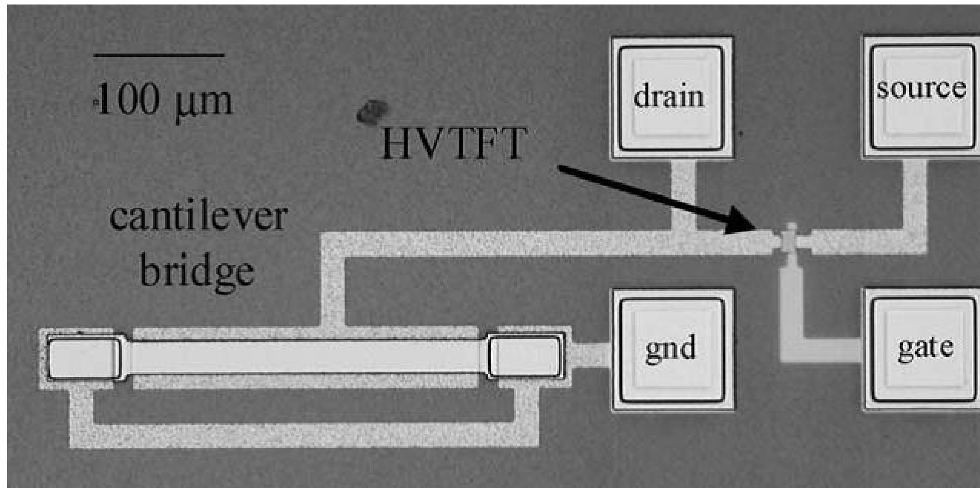


Figure 1-18: Optical micrograph of an a-Si HVTFT integrated with a cantilever bridge [28].

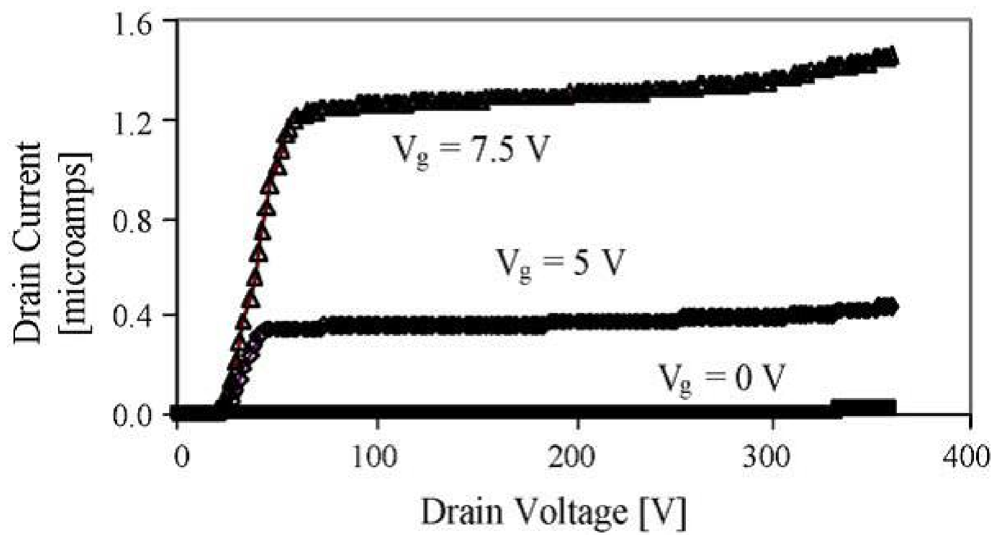


Figure 1-19: Output characteristics of an a-Si HVTFT, capable of driving above 300 V [28].

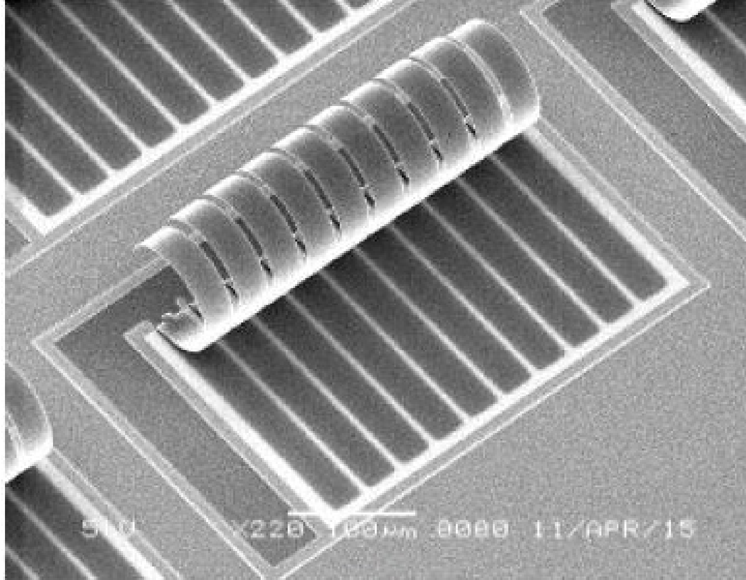


Figure 1-20: Si MEMS roll up blind array for house management [62].

EAP diaphragms with a photoconductive high-voltage switch due to the lack of high-voltage capabilities of an a-Si TFT [62].

Currently, there are a few non-organic HVTFTs reported in the literature. The first HVTFT was an a-Si HVTFT developed by Martin et al. from Xerox [57]. They successfully identified the need for high-voltage in a TFT platform for novel displays, and introduced the dual channel architecture comprising of a gated and offset region, shown in Fig. 1-21. The gated region allowed for accumulation mode operation of the transistor while the offset region prevented an excess electric field from breaking down their amorphous silicon nitride dielectric. However, issues with instabilities arose in the creation of metastable trap states at the boundary of the gated and offset channel region [57]. More recently, work by Chow et al. presented a PECVD grown a-Si HVTFT shown to actuate MEMS cantilevers with voltages of 800 V [28]. Integration was performed by fabricating the HVTFT on a glass wafer, followed by a passivation layer and MEMS structures. An off chip resistor was used to form a pull down inverter to modulate the high-voltage across the cantilever. Other material systems such as poly-Si, indium gallium zinc oxide (IGZO) and magnesium zinc oxide (MZO) have also been used in HVTFTs, reaching voltages of 240 V, 100 V, and 200 V, respectively [61]. It is in this context that we present the first HVOTFT based

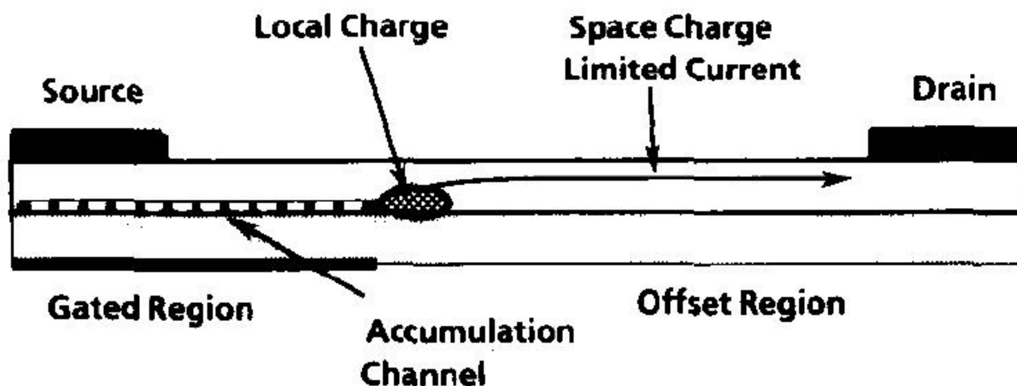


Figure 1-21: Cross-sectional diagram of the first HVTFT, showcasing the two channel region architecture [57].

on organic semiconductors for flexible MEMS integration capable of driving beyond -550 V.

1.5 Scope of Dissertation

Although there is significant research on a-Si:H and poly-Si low voltage TFTs for display technology, there is little to no work dedicated to HVTFTs, particularly for organic semiconductors. Developing HVTFTs would enable new applications with large force actuation and MEMS integration on the TFT technology platform. EAPs, field-emitters and novel displays would also benefit from the HVTFT. Furthermore, introducing organic semiconductors into an HVOTFT enables low cost, room temperature, vacuum-less and large area processing as well as integration on arbitrary and flexible substrates. The scope of this dissertation is to present a flexible and solution-processed high-voltage organic thin film transistor for MEMS integration, a first of its kind. The project was divided into three overarching goals, summarized in Fig. 1-22. First, we demonstrated the dual channel region HVOTFT technology with a vacuum-deposited organic semiconductor, namely pentacene, capable of driving beyond -550 V. Pentacene is widely used in OTFT research and can be easily deposited through a thermal evaporation. A high-k dielectric was introduced to minimize the threshold voltage required to achieve accumulation while minimizing leakage current.

Design and analysis for increasing the breakdown voltage was explored. Furthermore, field plates were added in an attempt to improve charge accumulation and prevent stress-induced trap generation. Second, a working solution-processed fabrication procedure was developed with TIPS-pentacene for the HVOTFT, resulting in devices with breakdown voltages beyond -450 V. One of the novelties of organic semiconductors is the ability to perform solution-processing at room temperature, air ambient and atmospheric pressure conditions. TIPS-pentacene growth under various solution-processing conditions was optimized for large and highly oriented crystal grains. In addition, self-assembled monolayers were introduced to improve the charge carrier injection as well as to reduce the overall surface energy of the sample for growth of thin layers of TIPS-pentacene. Lastly, a unique self-aligned solution-processing method using self-assembled monolayers and surface energy engineering was developed. This allowed for local aggregation of the organic solution, resulting in self-aligned patterns of TIPS-pentacene on top of the HVOTFT structures. Due to TIPS-pentacene's incompatibility with solvents, etching processes was avoided altogether. The self-aligned process resulted in thin layers (< 40 nm) of TIPS-pentacene, with the HVOTFTs having large breakdown voltage and on/off current ratios of -550 V and 10^6 A/A, respectively.

1.6 Dissertation Overview

The fabrication process for a novel solution-processed high-voltage organic thin transistor and its electrical measurements are presented in this dissertation. The described HVOTFT is the first of its kind, being able to drive voltages beyond -550 V. Low voltage OTFTs and vacuum-deposited HVOTFTs are also presented for comparison. The dissertation is divided into the following chapters, as shown in Fig. 1-23. Chapter 2 details the device physics of the OTFT and HVOTFT. Analytical models for electrical parameter extraction are also derived and discussed. Chapter 3 summarizes the various materials used in the fabrication of the HVOTFTs. The fabrication and characterization tools and methods are also discussed. Chapter 4 provides the step by

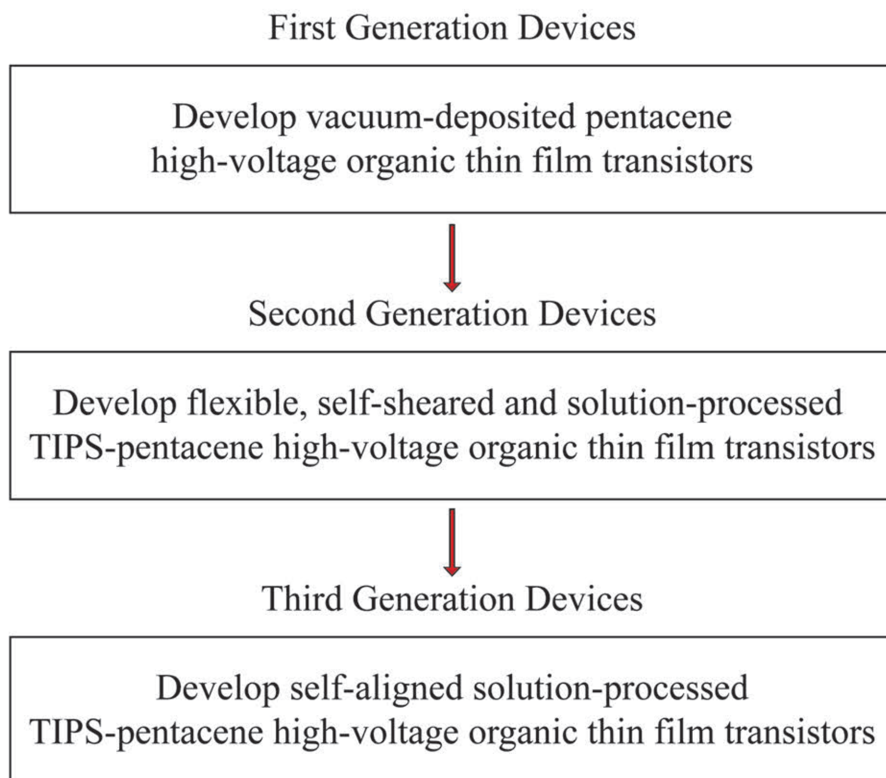


Figure 1-22: Scope of dissertation.

step fabrication processes used, their nuances, as well as the experimental characterization of the deposited materials. The electrical characterization and performance of the pentacene OTFT and the HVOTFT are given in chapter 5. Chapter 6 presents the first solution-processed TIPS-pentacene HVOTFT. Chapter 7 showcases a self-aligned solution-process that patterns the organic semiconductor without the use of etching processes. To conclude, chapter 8 discusses potential future works for the advancement of the HVOTFT technology and its integration with flexible MEMS.

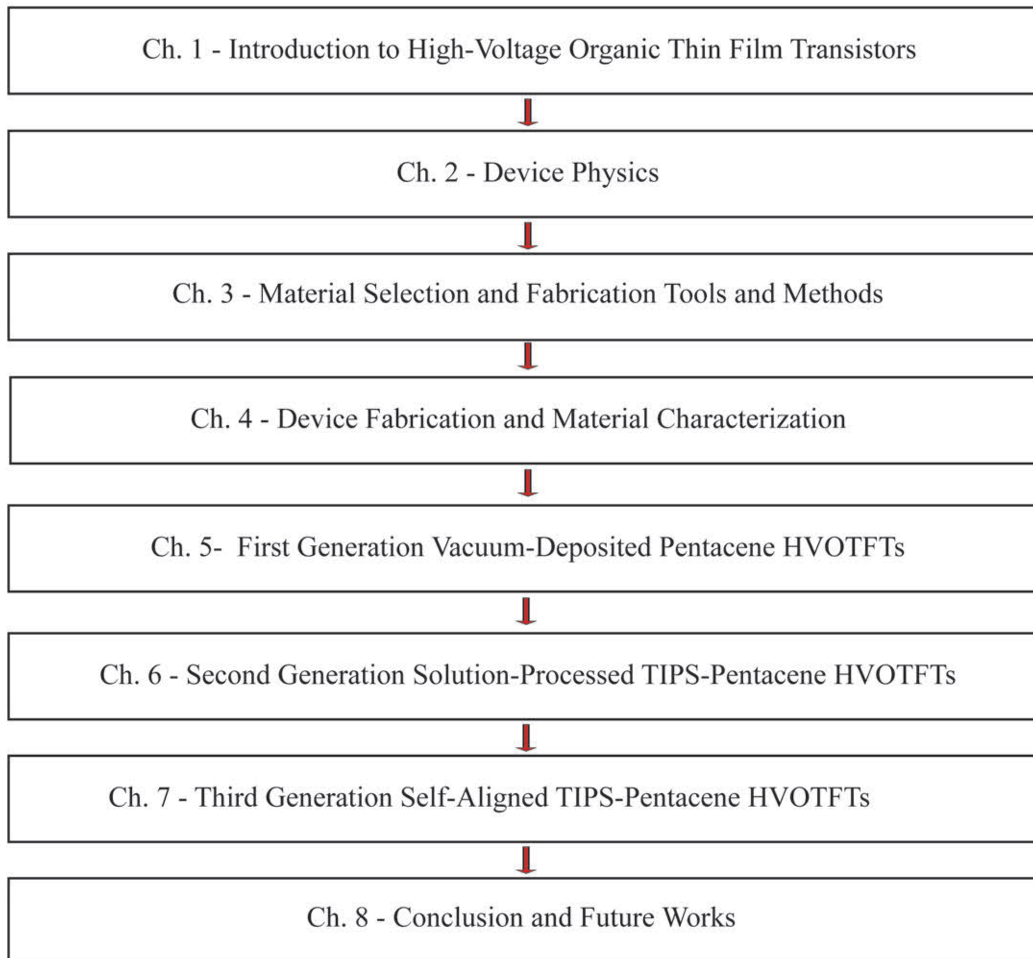


Figure 1-23: Dissertation overview.

Chapter 2

Device Physics and Parameter Extraction

Proper device modeling and subsequent parameter extraction is needed to help understand the basic electrical properties of the OTFT and HVOTFT, to predict circuit behavior as well as to have a standardized comparison method between different works. The cross-sectional diagrams of the OTFT and the HVOTFT were shown in Fig. 1-1. Since 2002, the IEEE 1620 Standard has been providing a set of recommended methods and reporting practices to help facilitate the pursuit of OTFT research [65]. The IEEE 1620 Standard, which has been universally adopted for parameter extraction in OTFTs, uses a long channel crystalline Si MOSFET model. Although convenient, there are short comings in the MOSFET model that does not account for the organic semiconductor charge transport (e.g. thermal activation) and its usually amorphous structure (e.g. field-dependent mobility). Recently, there has been development of a compact DC model for OTFTs and their associated parameter extraction protocol [66], [67]. Both models will be discussed; however, actual parameter extraction performed in this dissertation will follow the IEEE 1620 Standard. Below, we present the MOSFET, OTFT and HVOTFT structures and discuss their similarities and differences in operation and modeling.

2.1 MOSFET Model

The crystalline Si MOSFET is the most popular FET device, primarily due to its scaling ability and its low power consumption as little to no current is required to control load current. The MOSFET is comprised of four terminals, the gate, source, drain and body contacts. It can be viewed as a conjunction of a variable resistor between the source and drain contacts and a metal-oxide-semiconductor MOS (or metal-insulator-semiconductor MIS) capacitor. MOSFET models have been well developed over the decades and are also used to model TFTs with some issues. A description of the operation of the Si MOSFET is given here, first in terms of the MOS capacitor and then the complete MOSFET, followed by a discussion of the differences between it and the TFT.

2.1.1 Metal-Oxide-Semiconductor (MOS) Capacitor

The heart of the MOSFET is the metal-oxide-semiconductor (MOS) capacitor. It dictates the charge carrier density and the drain current I_D in the organic semiconductor channel between the source and drain. The MOS capacitor is a two terminal 1-D device comprised of a triple stack: a metal gate contact (typically aluminum or poly-Si), an oxide dielectric (typically SiO_2), and the semiconductor in question. A back contact is also present below the semiconductor, and is typically grounded with the source contact. The requirements for an ideal MOS structure are zero current through the oxide layer under all biasing conditions as well as a nominally thick semiconductor to allow for a field-free region to be encountered before reaching the back contact. The band diagrams of the MOS capacitor under various biasing conditions are presented in Fig. 2-1.

Under positive or negative biasing, the MOS capacitor can be found in three different regimes: accumulation, depletion and inversion. For a p-type semiconductor with majority hole carriers (used in an n-type MOSFET), if the gate metal contact (relative to the source or body contact) is biased negatively, the bands of the semiconductor bends upwards, with the valence band approaching that of the Fermi level.

This results in an accumulation of holes at the oxide-semiconductor interface. If a small positive bias is applied to the gate, the holes in the semiconductor are pushed away from the interface, resulting in a depleted channel. In this case, the bands bend downwards, with the Fermi level approaching that of the intrinsic level. Finally, if a large enough positive bias is applied to the gate, the bands bend further down, with the Fermi level going above the intrinsic level. This indicates that the electron density will surpass that of holes, resulting in an inversion regime. The polarities of the above discussion are reversed when discussing an n-type MOS capacitor (used in a p-type MOSFET). Beyond the three regimes, there are also two distinct transitions points in the MOS capacitor operation: the flatband voltage V_{FB} and threshold voltage V_T. V_{FB} is defined as the gate voltage required to achieve flat energy bands in the semiconductor and is the transition voltage between the depletion and accumulation regimes. It is equal to the work function difference between the gate metal and the semiconductor Φ_{MS} minus contributions from the oxide/semiconductor interface charge Q_{it} and the bulk oxide charge Q_{ox}:

$$V_{FB} = \Phi_{MS} - \frac{t_{ox}}{\epsilon_0 k}(Q_{it} - Q_{ox}) = \Phi_{MS} - \frac{Q_{it}}{C_{ox}} - \frac{1}{\epsilon_0 k}\int_0^{t_{ox}} \rho_{ox} x dx \tag{2.1}$$

where C_{ox} is the oxide capacitance, ϵ_0 is the permittivity of free space, t_{ox} is the oxide thickness, k is the relative dielectric constant of the oxide and ρ_{ox} is the bulk oxide charge density.

Threshold voltage, on the other hand, is defined as the gate voltage required to achieve an equal amount of majority and minority carrier concentration at the oxide/semiconductor interface. It is thus the transition voltage between the depletion and inversion regimes. The threshold voltage can be described with the following equation [68]:

$$V_T = 2V_F + \frac{\sqrt{2q\epsilon N_A 2V_F}}{C_{ox}} \tag{2.2}$$

where $2V_F$ is surface potential at the oxide/semiconductor interface and N_A is the substrate doping.

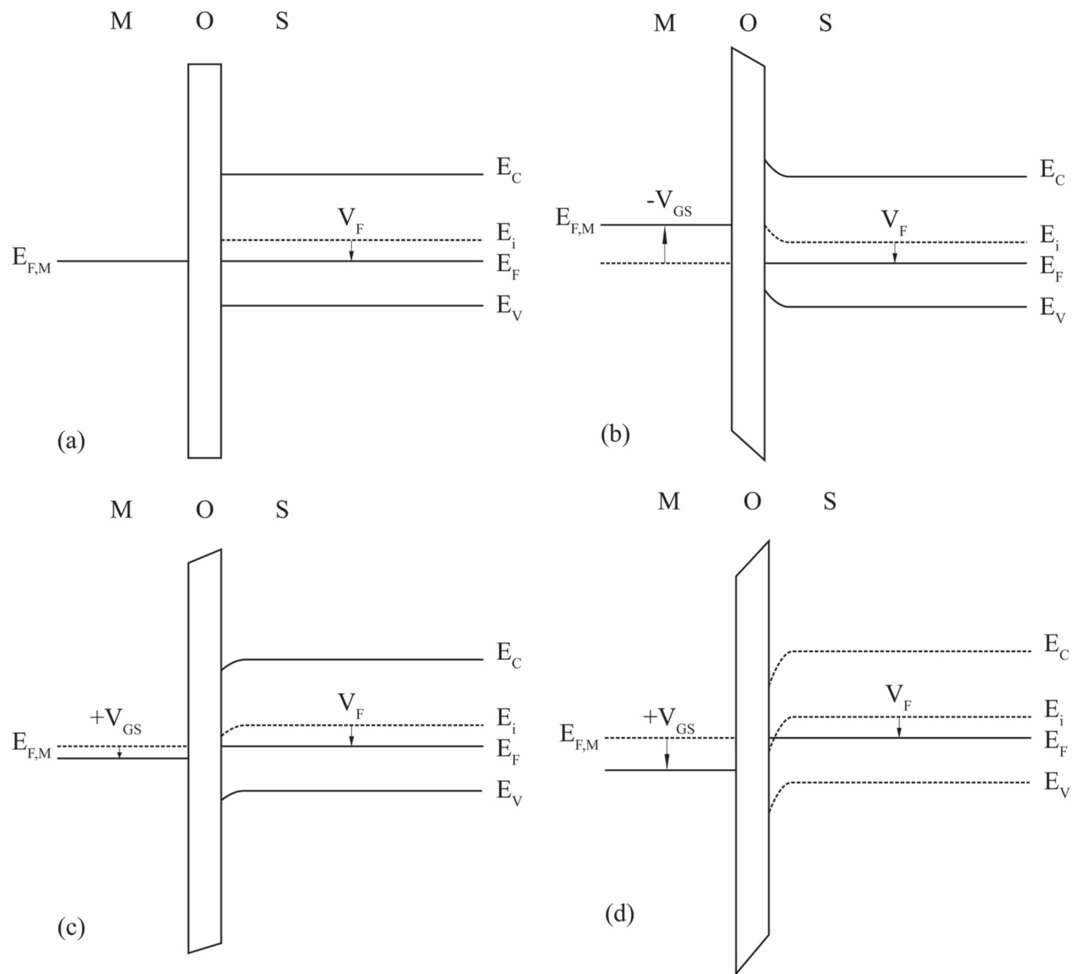


Figure 2-1: Band Diagram of an MOS capacitor under (a) flatband, (b) accumulation, (c) depletion and (d) inversion regimes.

2.1.2 Field-Effect Transistor

With the addition of the source and drain contacts to the MOS capacitor, a four terminal 2D MOSFET is created. Assuming a long-channel device with channel length L and channel width W, one can derive a model for the I-V characteristics of the MOSFET starting with defining the current density through the drain contact J_D as:

$$J_D = \sigma_n(x,y)E(y) \tag{2.3}$$

where σ_n(x,y) is the electron (hole for p-type MOSFET) conductivity and E(y) is the electric field in the direction of charge flow (between the source and drain). The conductivity is given by:

$$\sigma_n(x,y) = q\mu_n n(x,y) \tag{2.4}$$

where q is the electric charge, μ_n is the electron mobility, and n(x,y) is the electron concentration in the channel. Assuming field independent mobility, the current I_D(y) is given by the integration of the current density over the cross-sectional area of the channel:

$$I_D(y) = W\int_0^{x_i}\sigma(x,y)E(y)dx = -W\int_0^{x_i} q\mu_n n(x,y)\frac{dV(y)}{dy}dx = -q\mu_n W\frac{dV(y)}{dy}\int_0^{x_i} n(x,y)dx \tag{2.5}$$

Under the inversion regime, the charge density seen through the cross section of the channel can be represented as:

$$q\int_0^{x_i} n(x,y)dx = Q_n(y) \tag{2.6}$$

where the charge Q_n is given by the V_{GS} [69]:

$$Q_n(y) = -C_{ox}(V_{GS} - V_T - V(y)) \tag{2.7}$$

By integrating $I_D(y)$ along the channel direction and dividing by L, we arrive to the expression:

$$I_D = \frac{\mu_n W C_i}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}{V_D}^2\right] \tag{2.8}$$

Under low $V_{DS} \ll V_{GS} - V_T$, the drain current is linearly proportional to the drain-source potential:

$$I_D = \frac{\mu_n W C_i}{L}(V_G - V_T)V_D \tag{2.9}$$

Under high $V_{DS} > V_{GS} - V_T = V_{DSAT}$, the drain current saturates at I_{DSAT}:

$$I_{DSAT} = \frac{\mu_n W C_i}{2L}(V_G - V_T)^2 \tag{2.10}$$

The above drain currents are derived from the Square-Law Theory which assumes that the depletion width along the channel is independent of V_{DS} [70]. The Bulk-Charge Theory takes this into account, by giving a more accurate description of the charge Q_n:

$$Q_N(y) = -C_{ox}(V_{GS} - V_T - V(y)) + qN_A(W(y) - W_T) \tag{2.11}$$

where W(y) is the depletion width along the channel and W_T is the max depletion width under zero drain-source bias. The expressions derived for I_D in the linear and saturation regimes using the Bulk-Charge Theory is cumbersome to work with, although slightly more accurate. In fact, the accuracy of the Square-Law Theory approaches that of the Bulk-Charge Theory as the doping concentration N_A decreases. In terms of OTFTs, typical organic semiconductors are not doped.

2.2 OTFT and its Differences from the MOSFET

The above Square-Law Theory has been adopted by the IEEE 1620 standard to model OTFTs. However, there are key differences in operation and structure between that of the OTFT with the MOSFET. For one, OTFT are typically three terminal devices instead of four, without a body contact, as the substrate acts solely as a carrier wafer.

Although the body contact is typically tied with the source contact in a MOSFET, the gate potential is properly measured relative to the body contact. For an OTFT, the gate potential is measured relative to the source contact. Secondly, low I_{OFF} currents are ensured by a low conductivity of the semiconductor as opposed to the presence of a depletion region which would have prevented charge flow into the substrate. Most organic semiconductors have low conductivity due to its amorphous nature. Nonetheless, the I_{OFF} currents are typically higher in OTFTs than MOSFETS due to a lack of blocking p-n junctions at the source and drain contacts. Thirdly, there are typically no dopants involved in organic semiconductors as opposed to crystalline Si MOSFETS. Pentacene, although undoped, tends to operate like a p-type device due to an ease in removing an electron from the higher electronegative carbon backbone compared to its surrounding hydrogen atoms [71]. The high Shockley-Hall-Read recombination rate in pentacene due to deep traps originating from the amorphous nature prevents a minority carrier population to form. Thus, unlike MOSFETS, OTFTs operate in the accumulation regime as opposed to the inversion regime. It is the accumulated majority carriers that provide a conducting channel in the OTFT. If the Square-Law Theory is to be used to model OTFT, a new definition of the threshold voltage is needed in the absence of a depletion/inversion transition. OTFTs turn on when transitioning from a depleted regime to an accumulated regime. It is therefore natural to equate the flatband voltage with the threshold voltage in OTFTs:

$$V_T = V_{FB} = \Phi_{MS} - \frac{t_{ox}}{\epsilon_0 k}(Q_{it} - Q_{ox}) \tag{2.12}$$

It can be seen then that one can control the threshold voltage by varying the relative dielectric constant and the thickness of the oxide. One can also modify either the interface or the bulk charges. A last difference between the OTFT and the MOSFET is the OTFTs field and thermally activated mobility, as described previously in chapter 1.

2.2.1 OTFT Compact DC Model

The similarity between the MOSFET and OTFT has allowed the latter to adopt the MOSFET model with varying success. As mentioned above, several key differences in device operation and physics render the MOSFET model inaccurate in describing OTFTs. Moreover, large variations in fabrication procedures, material choices and even experimental data make having an exact model to describe OTFTs difficult. To tackle these issues, Marinov et al., among others, have developed generic and compact DC models that encompass the most common details about OTFTs [66]. They define a compact DC model as a model that represents the OTFT behavior, has symmetrical electrical performance about its structure, is analytical, simple and derivable, can be upgradeable, can be physically justified, and can be tuned to experimental data. They first developed a generic DC model that encompasses field-enhanced field-effect mobility, a common theme in OTFTs. From the charge drift model, we can write:

$$\frac{I_D}{W} = \mu_x Q_x |E_x| \tag{2.13}$$

where μ_x, Q_x and E_x are the mobility, areal charge density and electric field along the channel length, $0 \leq x \leq L$. The areal charge density is given by:

$$Q_x = C_{ox}(V_{GS} - V_T - V_x) \tag{2.14}$$

The main contribution in the generic model is the field-enhanced mobility, which is written as:

$$\mu_x = \mu_0 (V_{GS} - V_T - Vx)^\gamma \tag{2.15}$$

$$\mu_0 = \frac{\mu_{00}}{{V_\gamma}^\gamma} \tag{2.16}$$

where μ_0 is the mobility at the gate overdrive voltage V_γ, μ_{00} is the low-field mobility, and γ is the mobility enhancement factor [72]. By substituting Eq. 2.14 and Eq. 2.15 into Eq. 2.13 and integrating along the channel, one can derive an expression for the

generic DC model for the OTFT:

$$I_D\frac{L}{W} = \mu_0 C_{ox}\frac{(V_{GS} - V_T - V_S)^{\gamma+2} - (V_{GS} - V_T - V_D)^{\gamma+2}}{\gamma + 2} \tag{2.17}$$

where V_S and V_D are the potential of channel at the source and drain contact. The mobility enhancement factor can be associated with the characteristic energy width E_0 of the tail distribution of the density of states (DOS) [66]:

$$\gamma + 2 = \frac{2E_0}{kT} \tag{2.18}$$

From the generic DC model to a compact DC model, one can then include relevant modifications that represent the physical properties of the device. For example, channel length modulation can be added:

$$I_D\frac{L - \Delta L}{W} = \mu_0 C_{ox}\frac{(V_{GS} - V_T - V_S)^{\gamma+2} - (V_{GS} - V_T - V_D)^{\gamma+2}}{\gamma + 2} \tag{2.19}$$

$$L - \Delta L = L[1 - \lambda(V_D - V_{SAT})] \approx \frac{L}{1 + \lambda|V_D - V_S|} \tag{2.20}$$

where λ is the channel length modulation parameter. Further additions can be made to the OTFT generic model such as subthreshold operation and contact effects.

2.3 HVOTFT Device Physics

The HVOTFT has been identified as a unique electronic device able to withstand and modulate large lateral electric fields from $|V_{DS}|$ above 100 V. The integration of large electrostatic actuated MEMS with HVOTFTs on arbitrary substrates opens up new and novel applications. Here, we discuss how the structure of the HVOTFT differs from that of an OTFT as well as the implications in charge carrier flow.

2.3.1 HVOTFT Structure

The first HVTFT device was made from a-Si utilizing a dual channel region [57]. The HVOTFTs developed as part of this dissertation also uses this scheme, with its cross section shown in Fig. 1-1 (c). The organic semiconductor channel is divided into a gated region and an offset region, which can be either on the drain and/or source side. In the gated region, charge accumulation occurs as V_{GS} is applied, enabling FET operation. In the offset region, on the other hand, there is no underlying gate contact, with the semiconductor left with no charge accumulation. It is in this region that the majority of the high voltage from V_{DS} is dropped, due to the high resistivity of the amorphous organic semiconductor. In this regard, the HVOTFT differs from the OTFT in inherently having a lower mobility in exchange for high voltage driving capabilities. The amorphous offset region also prevents avalanche breakdown from lateral fields, due to elevated charge scattering. Breakdown, therefore, usually occurs from dielectric breakdown.

2.3.2 HVOTFT Electrostatics

The source and/or drain offsets relative to the gate contact affect the electrostatics and saturation current through the HVOTFT. Under accumulation and low V_{DS}, the I-V characteristic of the HVOTFT is characterized by a power law called the space-charge-limited current (SCLC). Accumulated charges from the gated channel region need to be injected into the undoped offset channel region which effectively limits the amount of current through the device. If the amount of injected charge is greater than the background charge of the offset region, the assumption that charge neutrality is maintained within the semiconductor is no longer valid. Thus, Ohmic conduction is no longer maintained [73]. Instead, the potential through the offset region is non-linear and can be described by the Mott-Guerney Law, which is obtained by solving the current continuity (Eq. 2.21) and Poisson's equation (Eq. 2.22):

$$J = qn(x)v(x) = qn_{inj}(x)v(x) \tag{2.21}$$

$$\frac{\partial^2 V(x)}{\partial x^2} = \frac{qn_{inj}(x)}{\epsilon} \tag{2.22}$$

where v is the charge velocity [73]. The charge distribution and electric field profile are shown in Fig. 2-2 for a simple volume block of semiconductor, in which the charge injection is either neglected, below background charge levels ($Q_{inj} \ll qn_0L$) , or above background charge levels ($Q_{inj} \gg qn_0L$) [73]. Rearranging Eq.2.21 and Eq. 2.22, we get:

$$\frac{\partial^2 V(x)}{\partial x^2} = \frac{J}{v(x)\epsilon} \tag{2.23}$$

Assuming that the electric field is linearly proportional to charge velocity:

$$v = -\mu E \tag{2.24}$$

then one can solve Eq. 2.23 using E(0) = 0 as the boundary condition, resulting in the Mott-Guerney Law:

$$J = \frac{9}{8}\epsilon\mu\frac{V^2}{L^3} \tag{2.25}$$

Because these two channel regions are in series and in between the source and drain contacts, current continuity is maintained with charge injecting from the gated channel region into the offset channel region. We can go one step further by including a Poole-Frenkel effect to the SCLC. Tsukagoshi et al. observed non-saturating behavior in pentacene-based OTFTs, attributed to the effective reduction in trap depth due to strong electric fields [74]. The SCLC expression is expanded to:

$$J = \frac{9}{8}\epsilon\mu\frac{V^2}{L^3}\theta_0 \tag{2.26}$$

$$\theta_0 = \frac{\rho_f}{\rho_f + \rho_t} \tag{2.27}$$

where ρ_f is the free charge density and ρ_t is the trapped charge density. Suppression of SCLC can be achieved by introducing large densities of trapped charges [75].

As V_{DS} is further increased under accumulation, a large electric field emerges at the interface between the gated and offset region, which effectively pinches off the

channel, prevents further injection into the channel, and causes current saturation [57]. Analytical expression can be derived for the linear and saturation current, the large impeding boundary electric field between the gated and offset channel regions, as well as the potential in both regions. Assuming a field-independent mobility, the accumulated charge resulting from a biased gate is given by:

$$Q = C_{ox}(V_{GS} - V_T - V(y)) \tag{2.28}$$

For a channel of width W and length dx, the current I is given by:

$$I = W\mu_{FET}C_{ox}(V_{GS} - V_T - V(y))\frac{dV}{dy} \tag{2.29}$$

Integrating the above equation between y = 0 and y = Y, with V(0) = potential at source = 0 and V = channel potential, results in:

$$IX = W\mu_{FET}C_{ox}\left((V_{GS} - V_T)V - \frac{V^2}{2}\right) \tag{2.30}$$

By evaluating at saturation where X = L_1 and V = V_{GS} - V_T, Eq. 2.30 becomes:

$$I_{SAT} = \frac{\mu_{FET}C_{ox}W}{2L_1}(V_{GS} - V_T)^2 \tag{2.31}$$

The potential in the gated region can be expressed as:

$$V = V_{GS} - V_T - \left[(V_{GS} - V_T)^2 - \frac{2XI}{W}\mu_{FET}C_{ox}\right]^{1/2} \tag{2.32}$$

The boundary electric field between the gated and offset channel regions can now be expressed by substituting Eq. 2.32 into Eq. 2.23 with X = L_1:

$$E_B = \frac{I(V_{GS} - V_T)}{2L_1 I_{SAT}(1 - I/I_{SAT})^{1/2}} \tag{2.33}$$

Thus, it can be seen that as I approaches I_{SAT}, the boundary electric field tends towards infinity. Physically, this represents an increasingly large electric field that

prevents further current increase under lateral bias. The potential drops across both the gated and offset channel region can also be derived by solving Poisson's equation [57]:

$$V_1 = V_{GS} - V_T - \left[(V_{GS} - V_T)^2 - \frac{2IL_1}{C_{ox}W\mu_{FET}}\right]^{1/2} \tag{2.34}$$

$$V_2 = \frac{1}{K\beta}[(KL_2 + H)^\beta - H^\beta] \tag{2.35}$$

where L_2 is the offset channel length and

$$K = (1+\alpha)\left(\frac{g_c k T_0}{\alpha\epsilon}\right)\left(\frac{I}{q\mu N_c W t}\right)^{1/\alpha} \tag{2.36}$$

$$H = E_B{}^{(\alpha+1)/\alpha} \tag{2.37}$$

$$\beta = \frac{1+2\alpha}{1+\alpha} \tag{2.38}$$

where g_c is the density of deep states at the conduction edge, N_C is the effective density of states, k is the Boltzmann constant, $\alpha = T_0/T$, and t is the semiconductor thickness.

2.3.3 HVOTFT High-Field Effects

Under high V_{DS} bias, non-ideal I-V characteristics start to manifest in HVOTFTs with electrical instabilities and non-saturating currents.

Instabilities occur in the form of a change of the onset to conduction V_X. V_X is defined as the value of V_{DS} needed to start having high output current I_D in accumulation mode. It can also be seen as the transition point between Ohmic conduction and space charge limited current (when injected charge equals the background charge of the offset channel region), before saturation current is reached. V_X is to V_{DS} as to what V_T is to V_{GS}. A shift in V_X can occur during high bias due to a change in the density of states in the offset channel region of the semiconductor, near the gate edge, indicating a lack of stability in the HVOTFT [57]. This has been reported in a-Si HVTFTs, shown in Fig. 2-4 [57]. Under high bias, deep trap states were formed, and needed to be overcome before injection of charge carriers occurred. Initial charge

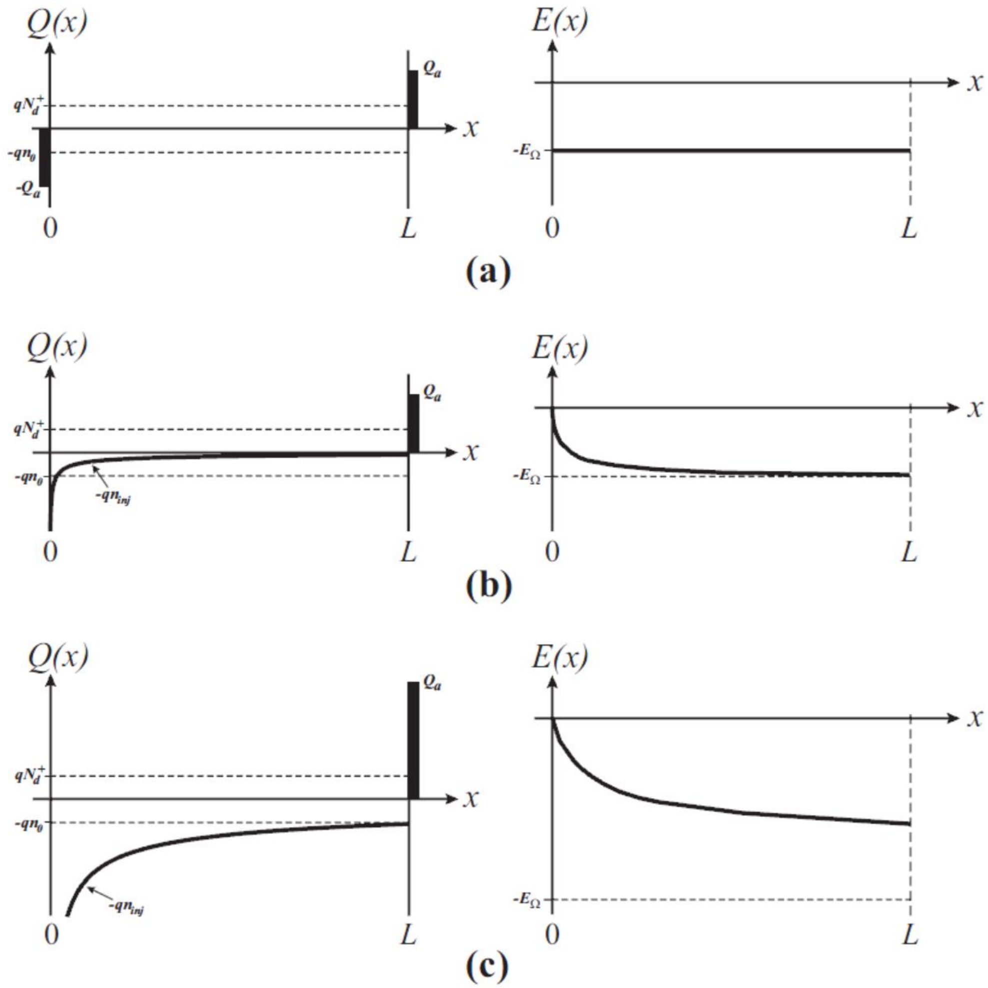


Figure 2-2: Charge distribution and electric field profile of a volume block in which the charge injection is either (a) neglected, (b) below background charge levels, or above background charge levels [73].

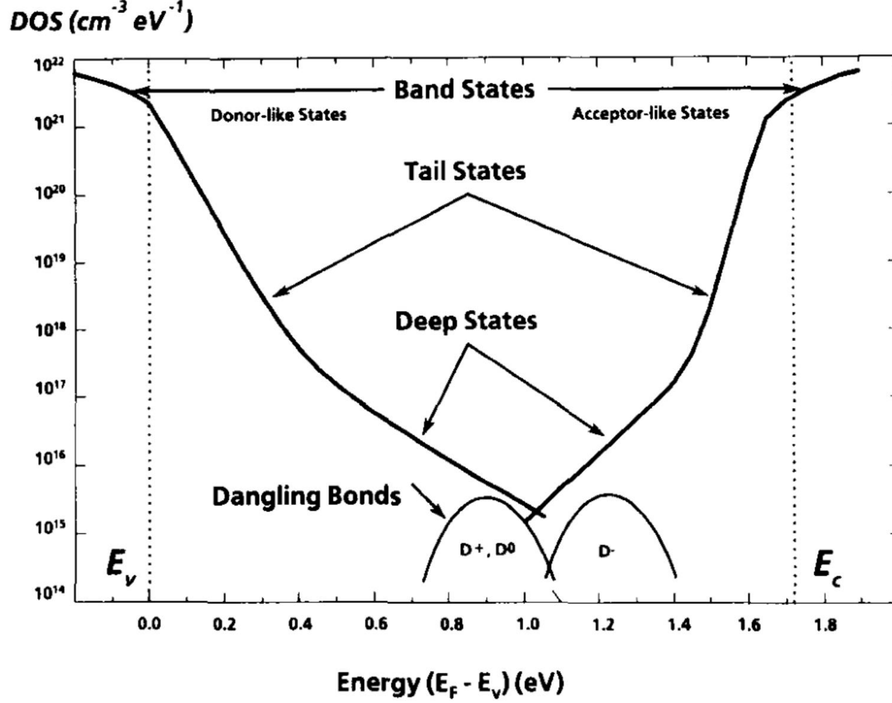


Figure 2-3: Density of states versus energy for an a-Si HVTFT with the addition of deep states being added due to high biasing from the HVTFT [57].

flow was trapped in the deep trap states, forming a localized charge that opposed further injection. The density of states for the a-Si HVTFT reported in the literature is shown in Fig. 2-3 with the addition of deep trap states.

Non-saturating behaviors can be attributed to SCLC enhanced by the Poole-Frenkel effect [75]. It can also be attributed to short-channel like effects such as channel length modulation (CLM) or self-heating effects (SHE). Although the channel lengths used in the HVOTFTs in this dissertation are between 5 and 50 μm, the high-voltage applied across the source/drain contacts does result in the necessary high electric field (0.1-1 MV/cm) to have channel length modulation [76], [77]. CLM is expressed as:

$$I_D = I_{D0}(1 + \lambda V_{DS}) \tag{2.39}$$

$$\lambda^{-1} = V_A + |V_X| \tag{2.40}$$

where I_{D0} is the drain current without CLM, lambda is the CLM parameter, V_A is the voltage extrapolated from the non-saturation slope to the V_{DS} axis, and V_X is

Table 2.1: Desired OTFT and HVOTFT parameters

Desired Parameters	OTFT	HVOTFT
μ (cm^2/V·s)	> 1	> 1
V_T (V)	$<$ -1	$<$ -10
S (V/dec)	< 0.5	< 0.5
I_{ON}/I_{OFF} (A/A)	$> 10^6$	$> 10^4$
V_X (V)	0	0
V_{BD} (V)	> 100	> 1000
$I_{G,leak}$ (A)	-1e-12	-1e-12

the onset to conduction parameter [75].

Self-heating effects (SHE), current induced temperature change, can also modify saturation current by increasing the temperature dependent mobility of organic semiconductors [78]. Heat transfer paths in a TFT structure include the channel, the encapsulation layer and the dielectric layer. In active matrix liquid crystal displays, operating temperatures can increase by 70 °C. This is in part due to the substrate having a low thermal conductivity, which prevents transfer of heat and cooling of the device. For example, glass's conductivity is only 1.1 W/m·K.

2.4 Desirable OTFT and HVOTFT parameters

Desirable OTFT parameters typically match those of inorganic TFTs. A desire for high mobility μ ($>$ 1 cm^2/V·s), high I_{ON}/I_{OFF} current ratios, low threshold voltage V_T, low subthreshold swing SS, low leakage current $I_G, leak$, and low contact resistance. For the HVOTFT, there is an emphasis on max drain/source voltage achievable or high breakdown voltage V_{BD}. Although the desired OTFT parameters still apply to the HVOTFT, the mobility requirement may be relaxed depending on the specific application, particularly for low speed and high force MEMS actuation. In Table 2.1, a summary of the desired OTFT and HVOTFT parameters are shown.

2.5 Electrical Properties and Parameter Extraction

To compare similar electronic devices, a set of electrical properties must be used as figures of merit. For the OTFT and HVOTFT, the field-effect mobility μ, the threshold voltage V_T, the I_{ON}/I_{OFF} current ratios, the gate leakage $I_{G,leak}$, the subthreshold swing SS, the onset to conduction V_X, and the breakdown voltage V_{BD} are used in this dissertation. The electrical properties are extracted using I-V and C-V measurements. The following is a description of each parameter and the method of extraction from electrical measurements.

2.5.1 Output Characteristics

Transistor electrical behavior is evaluated by measuring the output characteristics. This involves sweeping V_{DS} between, say, +20 V and -100 V, at 1 V steps for a set of finite number of V_{GS} values between, say, +10 V and -30 V, at 5 V steps. I_D is plotted in the y-axis. Linear (or square law) and saturation behavior is extracted. The onset to conduction and breakdown voltage is observed in the output characteristics.

2.5.2 Transfer Characteristics

Further transistor electrical behavior can be studied by measuring the linear and saturation transfer characteristics, in which the V_{GS} is swept between, say, +10 V and -30 V at 1 V steps for a fixed V_{DS} that is either in the linear or saturation regime. Mobility, threshold voltage, subthreshold swing, current ratios and gate leakage are extracted from the transfer characteristics.

2.5.3 Mobility μ

Mobility is defined as the ratio between the velocity of the charge carrier and the applied electric field, with units of $cm^2/V{\cdot}s$.

$$\mu = \frac{v}{E} \tag{2.41}$$

The linear relationship between carrier velocity and electric field holds true at low electric fields and for crystalline materials. However, for organic semiconductors under higher fields, the relationship becomes non-linear and becomes dependent on the charge carrier concentration. Regardless, it is possible to extract a charge mobility parameter in the linear regime without using a curve-fitting transistor model [79], [80]. If we assume that the charge carrier density is constant across the channel under very low V_{DS}, then the sheet charge density Q becomes:

$$Q(x) = Q = \frac{C_{ox}(V_{GS} - V_T)}{WL} \tag{2.42}$$

The drain current I_D is given by the amount of charges moving a velocity v through a volume:

$$I_D = \frac{Charge}{UnitTime} = WQv = QW\mu_{free}E \tag{2.43}$$

Rearranging the terms, we can express mobility as:

$$\mu_{FREE} = \frac{I_D}{WQE} = \frac{I_D L}{WQV_{DS}} \tag{2.44}$$

Finally, by substituting Eq. 2.42 into Eq. 2.44, we obtain a fundamental expression for charge mobility at low electric field:

$$\mu_{FREE} = \frac{I_D}{W}\frac{WL}{C_{ox}(V_{GS} - V_T)}\frac{L}{V_{DS}} = \frac{I_D L^2}{C_{ox}(V_{GS} - V_T)V_{DS}} \tag{2.45}$$

The above expression also assumes that all charges provided by the gate are mobile, when in fact for disordered organic semiconductors, there are traps that prevent charge motion. A correction for this is to include the proportion of free and trapped charges within the organic semiconductor [80]:

$$\mu_{FET} = \mu_{FREE}\frac{Q_{FREE}}{Q_{FREE} + Q_{TRAPPED}} \tag{2.46}$$

where Q_{FREE} is the free charge carrier density and $Q_{TRAPPED}$ is the fixed space charge in traps. As the gate bias increases, the Fermi energy level is pushed further into the

deep trap state levels, filling these deep traps. Thus, with more filled traps, the overall ratio of free and trapped charges increases along with μ_{FET} as well. However, with many OTFTs, there is presence of current crowding in the output characteristics at low V_{DS}, indicative of poor charge injection. Thus, it is usually suggested to extract mobility at higher V_{DS}, particularly in the saturation regime.

As mentioned previously, the MOSFET models are still used to extract mobility by curve fitting. From Eq. 2.8, we can derive field-effect mobilities, transconductance g_m and conductance g_d for both the linear and saturation regime:

$$\mu_{LIN} = \frac{L}{WC_{ox}V_{DS}}\frac{dI_D}{dV_{GS}} \tag{2.47}$$

$$g_{m,LIN} \equiv \frac{dI_D}{dV_{GS}} = \frac{\mu_{LIN}WC_{ox}V_{DS}}{L} \tag{2.48}$$

$$g_{d,LIN} \equiv \frac{dI_D}{dV_{DS}} = \frac{\mu_{LIN}WC_{ox}(V_{GS}-V_T)}{L} \tag{2.49}$$

$$\mu_{SAT} = \frac{2L}{WC_{ox}}\left(\frac{d\sqrt{I_D}}{dV_{GS}}\right)^2 \tag{2.50}$$

$$g_{m,SAT} \equiv \frac{dI_D}{dV_{GS}} = \frac{\mu_{SAT}WC_{ox}(V_{GS}-V_T)}{L} \tag{2.51}$$

The mobilities above are also adjusted for the fixed traps present at the interface between the oxide and semiconductor:

$$\mu_{FET} = \mu_{LIN/SAT}\frac{Q_{FREE}}{Q_{FREE}+Q_{TRAPPED}} \tag{2.52}$$

2.5.4 Threshold Voltage V_T

In OTFT and HVOTFT devices, inversion does not occur and thus threshold voltage needs to be redefined. As mentioned above, the threshold voltage in OTFTs is taken to be the point at which current starts to flow through the device, namely in the accumulation regime. In this case, the threshold voltage aligns itself with the flatband voltage.

The most common way to extract the threshold voltage is through a linear ex-

trapolation of the $I_D^{1/2}$-V_{GS} plot at a fixed V_{DS}. A linear line is drawn from the inflection point of the $I_D^{1/2}$-V_{GS} plot (the point of highest transconductance) to $I_D^{1/2}$ = 0. The intersection between the extrapolated line and the x-axis gives a value for the threshold voltage. If the fixed V_{DS} is taken in the linear regime where I_D is not constant, then the threshold voltage can be taken as:

$$V_{T,LIN} = V_{T,Extrapolated} - \frac{V_{DS}}{2} \tag{2.53}$$

However, as is the case for mobility in the linear regime, poor charge injection can further bring into question the validity of the linear extrapolation. If the fixed V_{DS} is taken in the saturation regime, and if the saturation current $I_{D,SAT}$ is indeed constant, then values for V_T is simply:

$$V_{T,SAT} = V_{T,Extrapolated} \tag{2.54}$$

Non-saturating behaviors in OTFTs and HVOTFTs do occur, making the linear extrapolation difficult. Furthermore, the slow subthreshold turn-on in the OTFTs and HVOTFTs results in significant drain current before V_{GS} reaches the extrapolated threshold voltage. This brings in more ambiguity to the actual value of the extrapolated threshold voltage.

A second method to extract V_T is by a quasi-static capacitance-voltage (QSCV) measurement. With the drain/source contacts shorted, the OTFT transitions from the depletion to the accumulation regime under V_{GS} sweeping. This can be seen in the C-V measurements through the addition of the channel or oxide capacitance in parallel with the geometrical capacitances (gate-source overlap and gate-drain overlap capacitances). The V_{GS} value at which the charge accumulation and its associated channel capacitance can be observed is designated as the threshold voltage.

2.5.5 Subthreshold Current $I_{D,SUB}$ and Swing SS

The subthreshold swing SS of a transistor indicates how fast the transition is between off and on states. It can be taken as the inverse steepest slope in the log-linear I_D-V_{GS} curve, measured below threshold. Typical units for subthreshold swing are mV/decade, indicating the necessary voltage needed to increase the drain current by an order of magnitude). Although ideal subthreshold swings for crystalline Si MOSFETs are 60 mV/decade, typical values for OTFTs range around 0.1 to 5 V/decade, due to the lack of an inversion layer. The subthreshold current and swing are given as:

$$I_{D,SUB} = \frac{W}{L} K \mu C_{ox} \left(1 - e^{\frac{qV_{DS}}{kT}}\right) e^{\frac{qV_{GS}}{nkT}} \tag{2.55}$$

$$SS = \frac{dV_{GS}}{dlog(I_{D,SUB})} = ln10 \frac{dV_{GS}}{dln(I_{D,SUB})} \tag{2.56}$$

where SS is the subthreshold swing, K is the materials device structure dependent constant, k is the Boltzmann's constant, T is the temperature and n is the ideality factor affected by the interface states Q_{it} [81].

2.5.6 Current Ratio I_{ON}/I_{OFF}

The current ratio between the on state and the off state is an important figure of merit as it indicates the degree of control the gate has on the channel as well as leakage currents. It also indicates how well the device is able to distinguish between on and off states. The current ratio is obtained from the transfer saturation characteristics (I_D-V_{GS}).

2.5.7 Gate Leakage Current $I_{G,leak}$

With the scaling of transistors, significant gate tunneling leakage current $I_{G,leak}$ arises through finite probability in direct or trap-assisted tunneling via the dielectric. $I_{G,leak}$ is measured at the gate contact for various V_{GS} at V_{DS} = 0 V, and will be used to determine the quality of the dielectrics used.

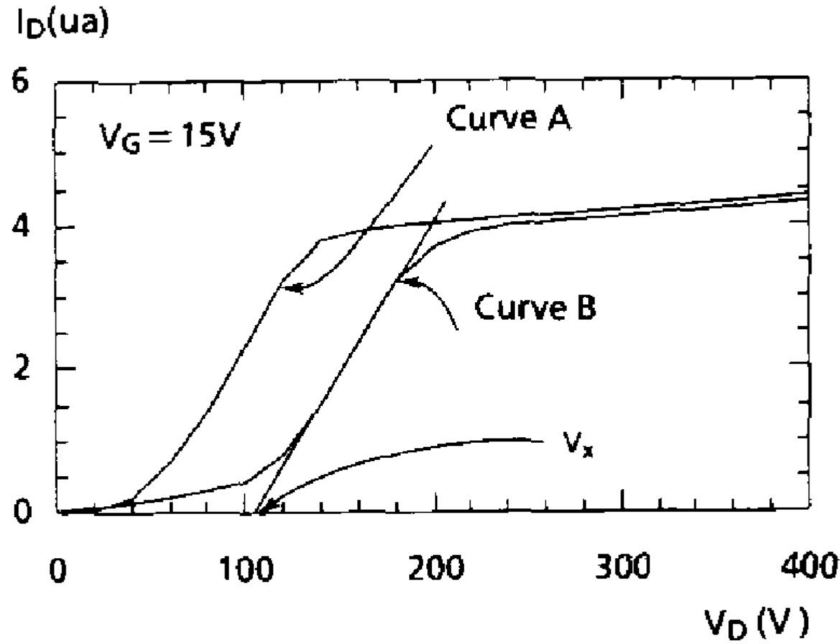


Figure 2-4: Onset to conduction V_X in a-Si HVTFTs. Curve A represents the initial output characteristic. Curve B represents the output characteristic with an increased V_X value due to high voltage stressing [57].

2.5.8 Onset to Conduction V_X

The onset to conduction V_X is defined as the V_{DS} needed to achieve a high I_D current. In typical MOSFETs and well-behaved OTFTs, the V_X is negligible and constant. However, in HVOTFTs, there have been signs of delayed currents with increasing V_{DS}, due to trap states that originate from the high-field stressing [57]. Fig. 2-4 shows the I-V characteristics of an a-Si HVTFT with increasing V_X after high voltage biasing. V_X is measured by extrapolating a straight line between the point of highest slope and the x-axis as shown in Fig. 2-4.

2.5.9 Breakdown Voltage V_{BD}

For HVOTFTs, knowing the maximum V_{DS} allowed before dielectric breakdown is of interest in building robust and reliable HVOTFTs. Output characteristics are measured for the HVOTFT, with each measurement increasing in maximum V_{DS}, until the device fails irreversibly in the off state. The measurement prior to failure is

used as the value of the breakdown voltage V_{BD}.

2.5.10 Capacitance Measurements and Dielectric Constant

Quasi-static capacitance-voltage (QSCV) and low frequency capacitance-voltage (LFCV) measurements are performed in order to obtain capacitance knowledge of the device. QSCV involves a linear voltage ramp to measure the capacitance with the following equation:

$$C = \frac{Q}{V} = I\frac{\Delta T}{\Delta V} \tag{2.57}$$

where Q is the charge, V is the voltage applied, I is the measured current through the dielectric, and $\Delta V/\Delta T$ is the ramp rate.

The HP 4156C semiconductor parameter analyzer is used to perform the QSCV measurement. LFCV measurements, on the other hand, are performed using the Keysight E4990A with a balanced bridge technique, with the maximum frequency limited by the mobility and parasitic capacitances of the OTFT. However, due to low mobility seen in organic semiconductors and high parasitic capacitances in TFTs, it is suggested to use QSCV for capacitance measurements [82].

With the OTFT having only three terminals, the source and drain contacts can be shorted together ($V_{DS} = 0$ V) to form a MOS-like structure with the dielectric and gate metal. Information on the regions of operation of the MOS (accumulation, depletion and inversion) as well as flatband and threshold voltages can be extrapolated. The interface trap density D_{it} can also be extracted by using the following equation:

$$D_{it} = \frac{C_{LF} - C_{HF}}{q\left(1 - \frac{C_{LF}}{C_{ox}}\right)\left(1 - \frac{C_{HF}}{C_{ox}}\right)LW} \tag{2.58}$$

where C_{LF} and C_{HF} are the low and high frequency capacitances [71].

It is also good practice to fabricate unique metal-insulator-metal (MIM) capacitors adjacent to the OTFTs on the same sample to extrapolate C_{OX} and the dielectric

permittivity k, independent of the organic semiconductor:

$$C_{ox} = \frac{\epsilon_0 k}{t_{ox}} \tag{2.59}$$

2.6 Summary

The semiconductor device physics and analytical models for the OTFT and HVOTFTs have been presented. A quadratic MOSFET model has been discussed to establish a basis for understanding the OTFT as a field-effect transistor. Although the MOSFET model is widely used for modeling OTFTs, key differences between the two devices bring into question the justification for using such a model. Differences include, for the OTFT, an accumulation operation as opposed to inversion, the threshold voltage being defined as the flatband voltage, a lack of traditional doping, as well as field- and temperature- enhanced mobility, among others. An OTFT compact DC model has also been discussed which addresses some of the short comings of the MOSFET model. The HVOTFT device physics has also been discussed in terms of the electrostatics, non-saturating characteristics and the non-ideal high-field effects, particularly that of the onset to conduction V_X.

A set of electrical properties have been identified as appropriate figures of merit and are to be extracted during electrical measurements. They include saturation and linear mobility μ, threshold voltage V_T, subthreshold swing SS, I_{ON}/I_{OFF} current ratio, gate leakage current $I_{G,leak}$, onset to conduction V_X and breakdown voltage V_{BD}. For simplicity, parameter extraction was done using the quadratic MOSFET model, as suggested by the IEEE 1620 standard.

Chapter 3

Material Selection and Fabrication Tools for HVOTFT Integration

The OTFTs and HVOTFTs were fabricated with various organic semiconductors, dielectric, metals, self-assembled monolayers and substrates using a mix of standard and non-standard low-temperature IC fabrication procedures. The band gaps of the materials used are summarized in Fig. 3-1. Particularly, there is an interest for solution-processing of the organic semiconductor layer for large area electronics. Here, the material selection is discussed, along with the different methods and tools used for deposition, photolithography, etching and characterization. The details of the fabrication process for the HVOTFT and the experimental material characterization are discussed in chapter 4.

3.1 Pentacene Organic Semiconductor

Pentacene ($C_{22}H_{14}$) is one of the most popular small molecule organic semiconductor to date due to its ease in deposition, its ability to form well-ordered films, and its relatively high mobility [83]. Mobilities have been reported since the 1990s, and have steadily increased from 0.002 to 5 $cm^2/V{\cdot}s$ due to improved morphology and grain size [84]. Pentacene is a conjugated linear acene molecule made of five fused benzene rings, enabling the delocalization of electrons through neighboring 2p orbitals. The

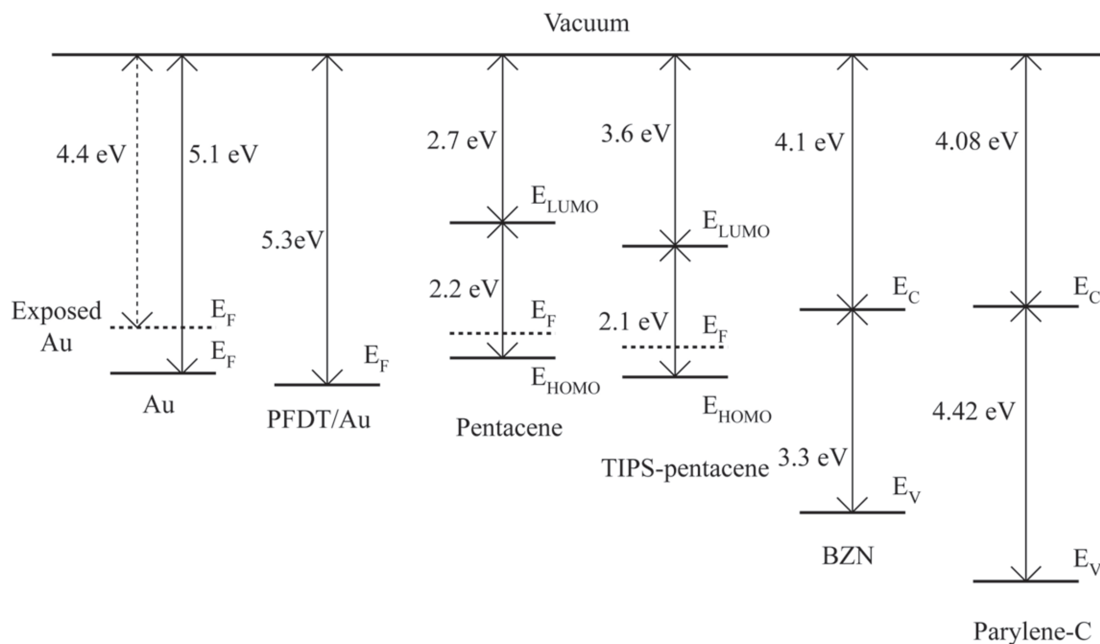


Figure 3-1: The band diagrams for the materials used in the fabrication of the HV-OTFT.

molecule, when packed correctly, forms a triclinic structure (space group P1) with a herringbone matrix, shown in Fig. 3-2 [85]. Although the herringbone matrix allows for intermolecular charge hopping, its face-to-edge packing lacks the optimal lateral π-orbital overlap seen in other organic semiconductors [86]. π-orbital overlap between the different pentacene molecules, and hence molecular packing, are critical for efficient charge conduction. As pentacene molecules come together, HOMO/LUMO bands are formed, with a typically cited band gap of 2.2 eV, as seen in in Fig. 3-1. Pentacene is characterized by its dark blue staining color, high reactivity with oxygen, and poor solvent solubility.

There have been reports of several polymorphs in bulk pentacene; however, of interest to TFTs, a "thin film phase" is observed in films with a thickness below 50 nm deposited on inert substrates [83]. The interplay between the underlying layers and the initial layers of the organic semiconductor plays a crucial role in the nature of the crystal growth. For example, low-reacting surfaces (like dielectrics) will favor pentacene-pentacene interactions over pentacene-dielectric interactions. This leads to pentacene standing near vertical. However, pentacene grown on reactive substrates

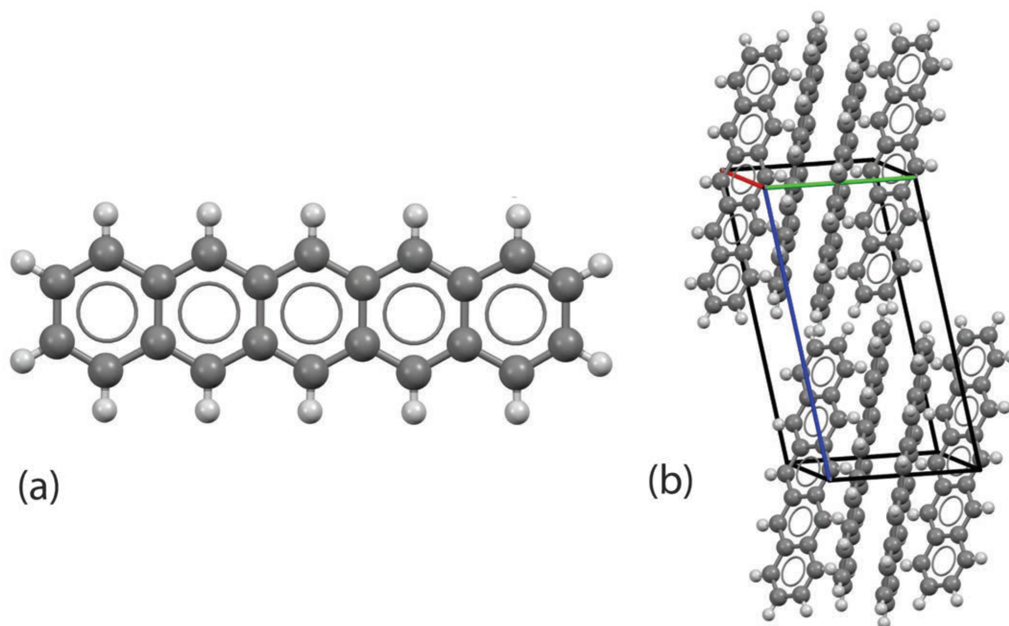


Figure 3-2: (a) Pentacene molecule. (b) Triclinic unit cell of pentacene.

like gold will result in favored pentacene-metal interactions. In this case, the initial layers of pentacene are grown horizontally on the substrate.

3.1.1 Synthesis of Pentacene

Pentacene was first synthesized in 1912 by Mills et al., whom originally called the organic molecule β,β,β',β'-dinaphtanthracene [87]. They began with pyromellitic anhydride and benzene with $AlCl_3$ as the catalyst, obtaining dibenzoylbenzene-dicarboxylic acids. With further heat and sulfuric acid exposure, dinaphtanthradiquinone was achieved, which could then be reduced to obtain pentacene molecules. Over the years, there have been several schemes that were more efficient in synthesizing pentacene [88]. Some synthesis schemes even resulted in a functionalized pentacene that can be solution-processed [84]. Upon heat treatment or ultra-violet (UV) irradiation, the functional groups can then be removed, resulting in pentacene, shown in Fig. 3-3.

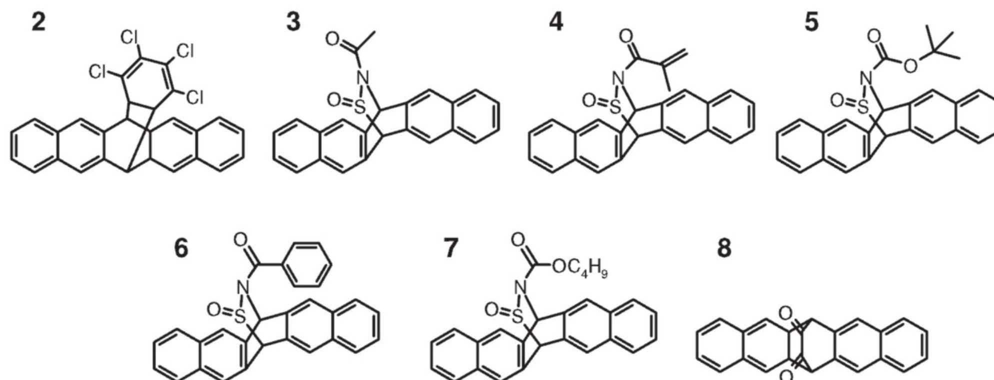


Figure 3-3: Examples of functionalized pentacene that can be solution-processed first, followed by a heat or UV treatment to reduce the molecule to pentacene [84].

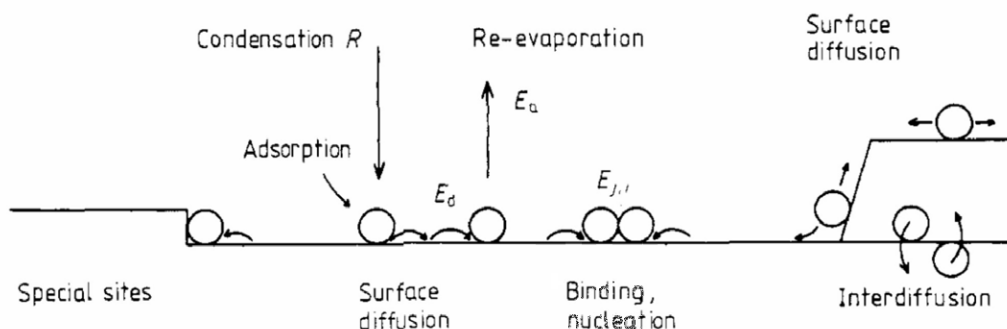


Figure 3-4: Atomistic processes of thin film growth via evaporation, showcasing condensation, adsorption, surface diffusion, nucleation and desorption/re-evaporation [89].

3.1.2 Thermal Evaporation

For the HVOTFT integration, pentacene was thermally evaporated via five atomistic processes, namely condensation, adsorption, surface diffusion, nucleation, and desorption/re-evaporation, shown in Fig. 3-4 [89]. Although it is relatively simple to deposit pentacene via thermal evaporation, it is another story to form well-ordered grains that promote high mobility. The grain size and structure depends on a number of factors such as surface roughness, surface energy and the number of nuclei, which can result in layer growth (Frank-van der Merwe), island growth (Volmer-Weber) or layer-plus-island growth (Stranski-Krastanov), shown in Fig. 3-5 [89].

Surface roughness plays an integral role in grain size. A rough surface prevents

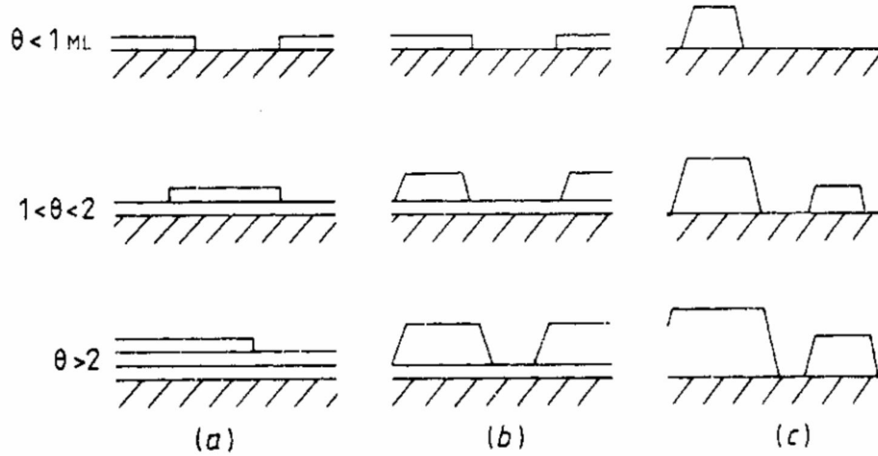


Figure 3-5: Three thin film growth methods: (a) Frank-van der Merwe layer growth, (b) Stranski-Ktrastanov layer-plus-island growth and (c) Volmer-Weber island growth [89].

the diffusion of adsorbed organic molecules, resulting in larger amounts of organic nuclei formed on the sample surface [90]. This in turn leads to a reduction in the grain size.

Surfaces with high surface energy tend to attract the face of the pentacene molecule, favoring a planar 2D Stranski-Krastanov growth, with the grain forming dendrite patterns [91]. However, low energy surfaces promote edge placements of the pentacene molecule onto the surface, which favors a 3D Volmer-Weber structure and more compact grains. Yang et al. reported increasing mobility in their OTFTs when transitioning from dielectrics with surface energy of 50 mN/m to 30 mN/m, shown in Fig. 3-6 [91].

Control of the organic nuclei density during adsorption is also critical in forming large grains. A nucleation theory by Venables at al. has been proposed, stating:

$$nuclei\ density \equiv \frac{n_x}{N_0} \sim \left(\frac{F}{N_0 v}\right)^p exp\left(\frac{E}{kT}\right) \tag{3.1}$$

where n_x is the number of clusters, N_0 is the number of sites per unit area, v is the effective surface vibration frequency, E is a conglomerate of the diffusion, desorption and binding energies, and p is related to the critical cluster size [89]. It suggests that

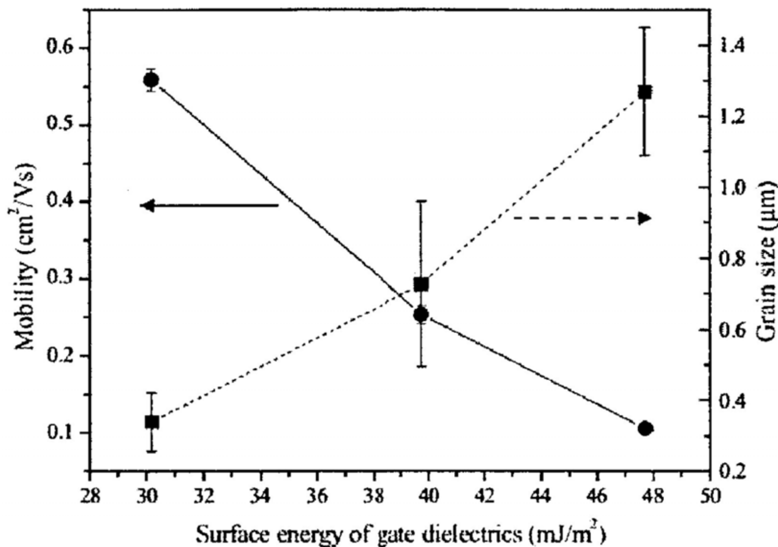


Figure 3-6: The mobility of pentacene OTFTs increased significantly when deposited on lower surface energy dielectrics, due to improved grain growth [91].

high temperatures and low deposition rates can result in a lower nuclei density and thus larger grains.

An in-house built thermal evaporator, shown in Fig. 3-7, was used to deposit pentacene. Pentacene crystals were introduced at the bottom of the chamber, attached to a heater, while the prepared samples were mounted face down in the center of the chamber. High vacuum ($< 10^{-7}$ Torr) was achieved with a turbo and roughing pump. Once base pressure was reached, the crucible heater was progressively increased to anywhere between 150 and 220 °C, resulting in a deposition rate of 0.1 to 10 Å/s.

3.2 TIPS-Pentacene Organic Semiconductor

Although pentacene is the most researched organic semiconductor molecule, it lacks the ability to do direct solution-processing, a key benefit of the material system. 6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene or $C_{44}H_{54}Si_2$) is a functionalized pentacene derivative with relatively large silicon side groups which allows it to be solution-processable in organic solvents. Several solvents have been used, such as toluene, chlorobenzene and tetralin with various degrees of success [53]. The silicon side groups also promote a 2D face-to-face stacking in a "brick layer" or columnar

Figure 3-7: In house built thermal evaporator for pentacene deposition.

matrix, as opposed to the herringbone matrix, shown in Fig. 3-8 [86], [92]. It was suggested that the silicon side groups hold the molecules together in such a way that the acene core could be brought together as close as possible [92]. Such a stacking arrangement results in an interplanar spacing of 3.47 vs 6.27 Å for pentacene, increasing the π-orbital overlap between molecules [86], [92]. The HOMO-LUMO gap for TIPS-pentacene has been measured to be 2.1 eV [93].

3.2.1 Synthesis of TIPS-Pentacene

TIPS-pentacene can be synthesized by an addition reaction of 6,13-pentacenequinone with the appropriate substitutes, followed by a reduction process [92]. This process is illustrated in Fig. 3-9 [94].

3.2.2 Drop Casting

Solution-processing techniques for organic semiconductors are of interest as it enables large area electronics, reduces overhead cost by removing high temperature and high vacuum steps, as well as produces highly crystalline organics for high mobility transistors [49]. Although there are many solution-processing techniques as mentioned

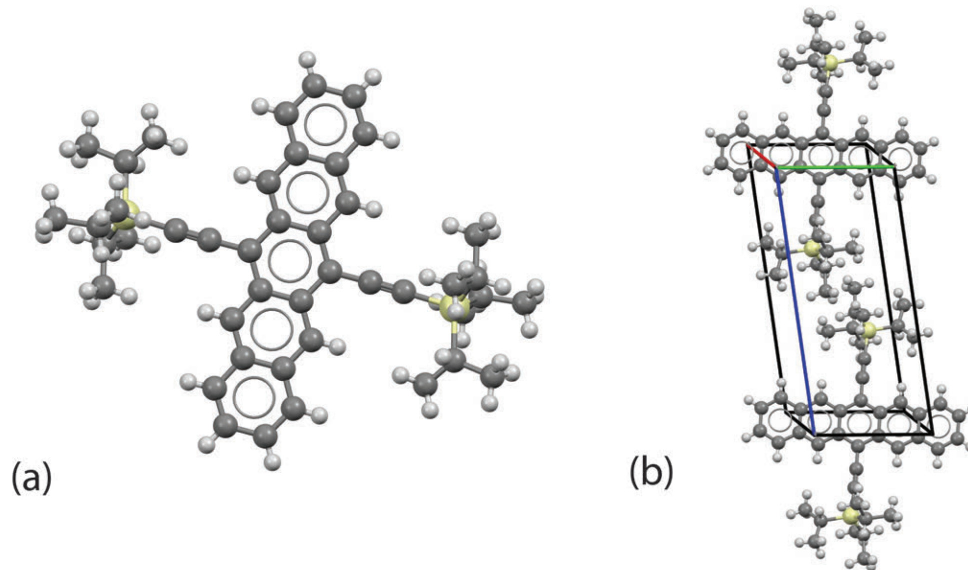


Figure 3-8: (a) TIPS-pentacene molecule. (b) Triclinic unit cell of TIPS-pentacene.

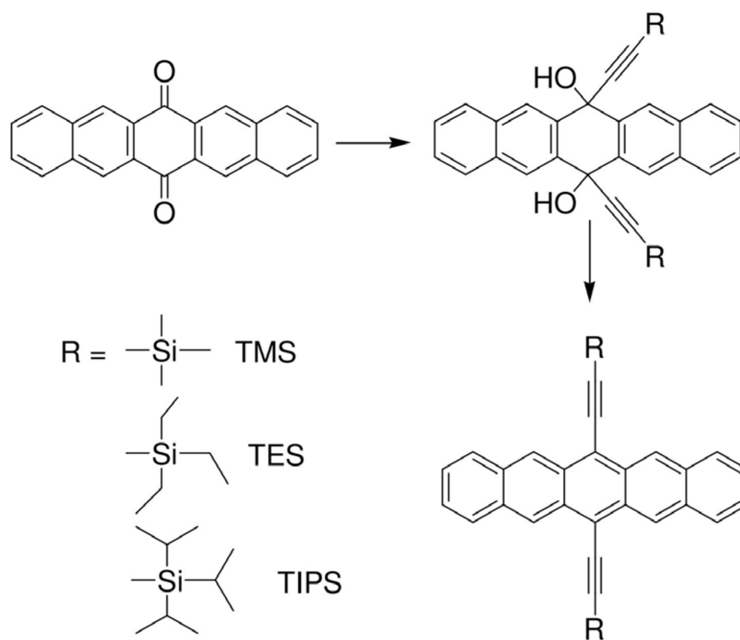


Figure 3-9: Synthesis of TIPS-pentacene (and other substituted pentacene molecules) through an addition and reduction reaction of 6,13-pentacenequinone [94]

in chapter 1, self-shearing drop casting was chosen for its simplicity and quick turn around.

In drop casting, organic semiconductor crystals are dissolved in a solvent which is dropped, via a pipette, onto the surface of a sample. Evaporation of the solvent leads to an initial nucleation and subsequent crystallization of the organic semiconductor, typically beginning at the evaporation front (at the interface between the organic solution drop and the air) [49]. Different drop casting conditions can improve the quality, size and coverage of the crystal grains as well as direct the growth orientation. For example, the choice of an appropriate solvent with a certain boiling point can vary the rate of solvent evaporation, a key factor in controlling nucleation [49]. Furthermore, dual solvent Marangoni flow for reduction of the coffee stain effect, saturated solvent environments for reduced evaporation rates, vibration assisted crystallization, pinned drop casting, and soluble additives for improved nucleation are but some of the technqiues used in the literature to improve the drop casting technique [49], [95]–[99]. It has been shown that the orientation of the grown TIPS-pentacene is also important, impacting the charge transfer between molecules and the overall mobility [100].

As part of this dissertation, a self-shearing drop casting method, shown in Fig. 3-10, was used to grow preferentially directed TIPS-pentacene crystals on top of the HVOTFT structures. A similar method was reported by Li et al. in 2015, shown in Fig. 3-11 [101]. They reported an equilibrium state for a spreading droplet over a slanted sample which described the nucleation process. As the solvent evaporated, the contact angle at the top of the slant was reduced. Although initial shearing of the solution was expected to occur to maintain mechanical equilibrium via Young's equation, nucleation at the top droplet/air interface pins the droplet in place. Once enough evaporation occurred such that the solute concentration exceeded saturation levels, further nucleation at the top interface was induced. This lead to preferentially oriented bands of organic crystals along the direction of the slant, as shown in Fig. 3-12.

In the self-shearing drop casting method used for the HVOTFT fabrication, the sample was angled at a slant (between 0 and 10 degrees relative to the horizontal). A

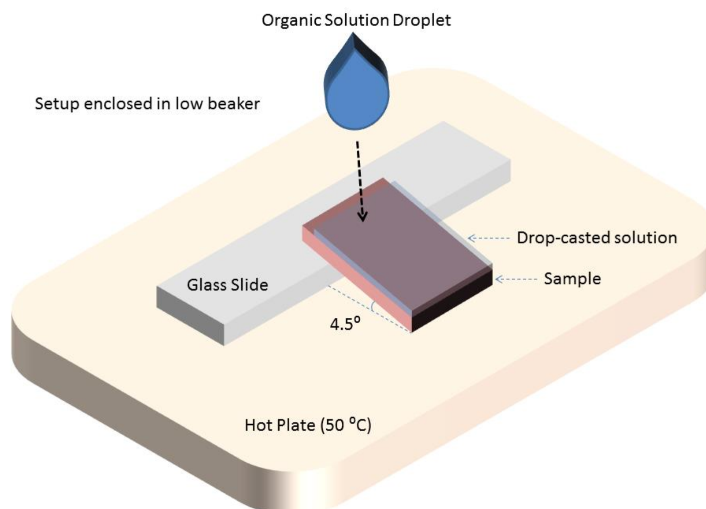


Figure 3-10: Self-shearing drop casting method used to deposit TIPS-pentacene.

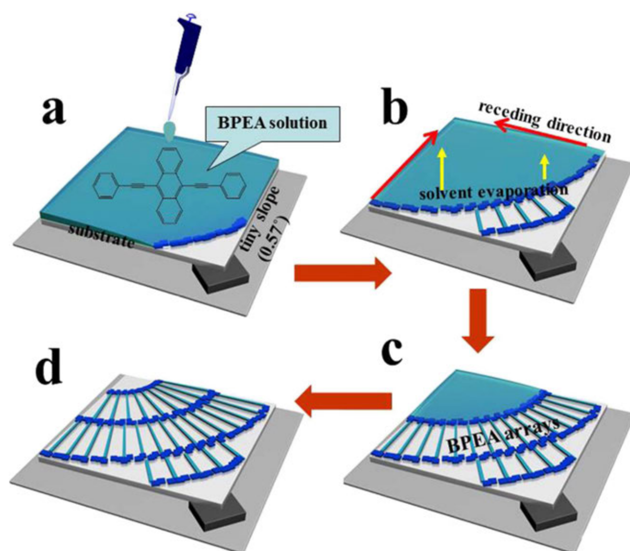


Figure 3-11: Diagram of a self-shearing drop casting method by Li et al. [101]. (a) A slant was introduced to the sample to promote directional grain growth of the drop casted organic solution. (b,c) As the solvent evaporated, nucleation and crystallization of the organic semiconductor occurred at the evaporation front. (d) Once all the solvent was evaporated, what remained was highly oriented organic crystals.

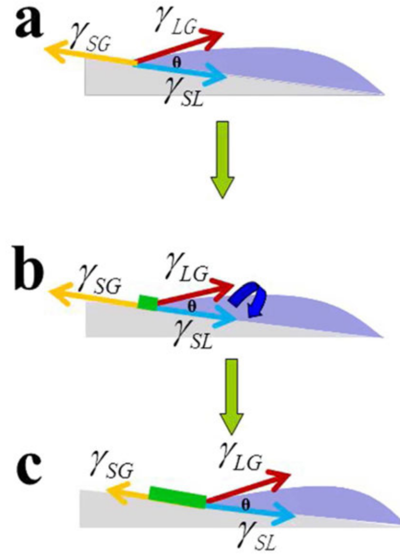


Figure 3-12: Equilibrium diagram of the interfacial tensions for a self-shearing droplet, with induced nucleation at the evaporation front [101].

hot plate, which doubled as a sample stage, was used to increase the evaporation rate and to help promote nucleation. The organic solution was dropped from a pipette onto the top of the sample, allowing for the solution to cover the majority of the sample. Typically for a 1 inch^2 sample, 300 to 400 μL of solution was drop casted to ensure proper coverage of sample. The sample slant allowed gravity to create an asymmetric solution/air boundary, leading to an evaporation front at the top of the sample only. Thus, nucleation and crystallization occurred at the top of the sample, with bands being formed in the direction of the slant as more solvent was evaporated. In chapter 4, the details of the self-shearing drop casting method (solute concentration, solvent choice, slant angle and hot plate temperature) will be discussed in relation to the size, orientation and coverage of the TIPS-pentacene.

3.3 $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ (BZN) High-K Paraelectric

One of the key aspects of the HVOTFT is the ability to control the channel with a relatively low gate to source voltage (V_{GS}) while operating under a large V_{DS}; thus, the need for a low threshold voltage device. Typical dielectrics such as SiO_2, Al_2O_3, $SrTiO_3$ and Ta_2O_5 have been investigated in OTFT design, but lack the necessary

dielectric constant to achieve low gate voltage operation while using relative thick dielectrics to prevent tunneling current[102]. It was demonstrated by Choi et al. that a certain high-k pyrochlore paraelectric, namely $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ (BZN), could lower the operating voltages in pentacene OTFTs as part of a low temperature fabrication process [103]. BZN, also referred to as the Bi_2O_3-ZnO-Nb_2O_5 system, is a cubic pyrochlore ($A_2B_2O_6O'$) paraelectric with space group Fd3m, typically seen as two interlacing structures of B_2O_6 octahedra and A_2O' tetrahedral, shown in Fig. 3-13. Bismuth and niobium atoms are inclined to occupy the A and B site due to their large and small atomic radius, respectively [102]. The zinc atoms, on the hand, can occupy both the A and B site due to their medium atomic radius. The band gap of BZN is 3.3 eV.

If crystalline, BZN can achieve room temperature permittivity as high as 200, loss tangents on the order of $5 \cdot 10^{-4}$, high resistivity of $3 \cdot 10^{13}$ Ohm·cm and dielectric breakdown strengths exceeding 5 MV/cm [102], [104]. However, to achieve such crystallinity, above 400 °C anneal is required [102], as shown in Fig. 3-14. Nonetheless, dielectric constants between 25 and 50 can still be achieved in amorphous BZN deposited at room temperature [102]. BZN is also considered a paraelectric material, one that exhibits tunability in its dielectric constant under an applied electric field. It has been shown that BZN has a tunability of up to 45%, enabling tunable capacitors for voltage-controlled oscillators [105].

3.3.1 Dielectric Strength

For an HVOTFT, the large drain to gate potential (V_{DG}) is of concern, which can lead to dielectric breakdown and the irreversible destruction of the device. The dielectric strength is the maximum electric field that can be applied to the insulator before permanent damage occurs, in the form of bond breaking and avalanche breakdown [106]. For a typical OTFT fabricated as part of this dissertation with 400 nm of BZN (dielectric strength of 5 MV/cm), an approximate maximum of 200 V can be applied between the drain and source before irreversible dielectric breakdown occurs. An offset region such as in the HVOTFT, described in depth in chapter 2, increases

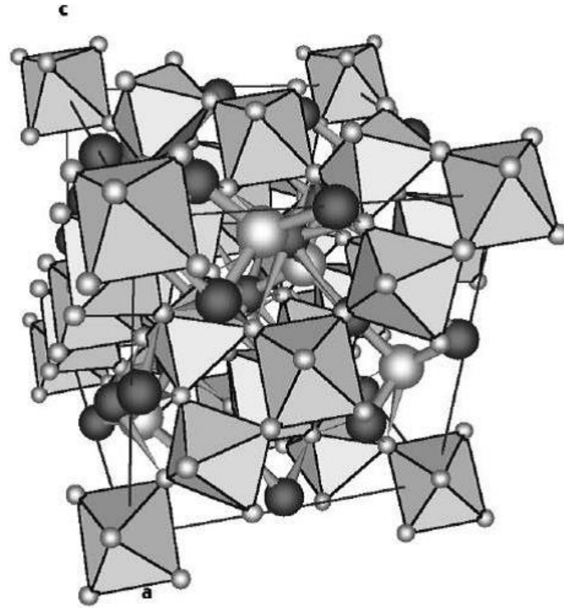


Figure 3-13: Cubic pyrochlore BZN [104].

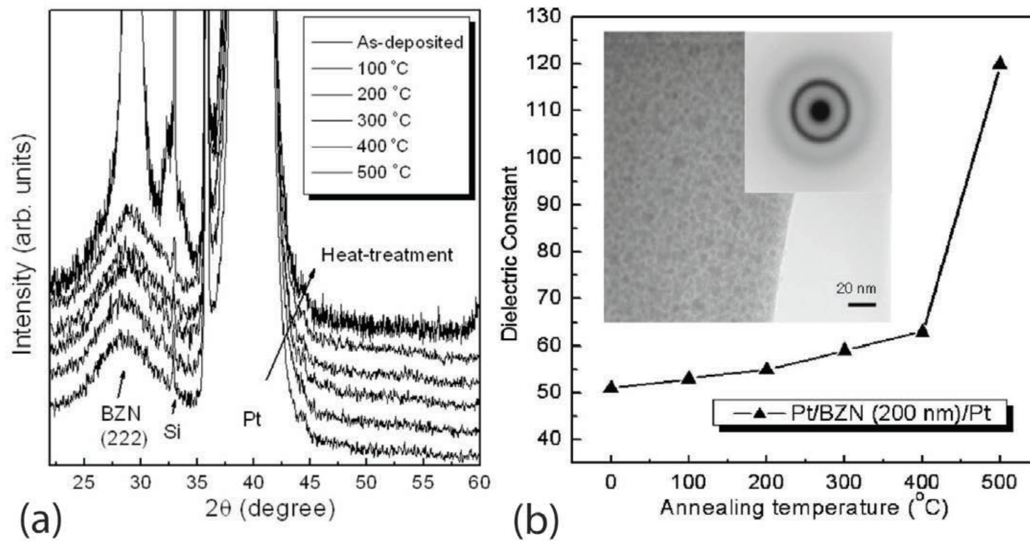


Figure 3-14: (a) XRD of BZN under various annealing conditions (b) Dielectric constant as a function of temperature [102].

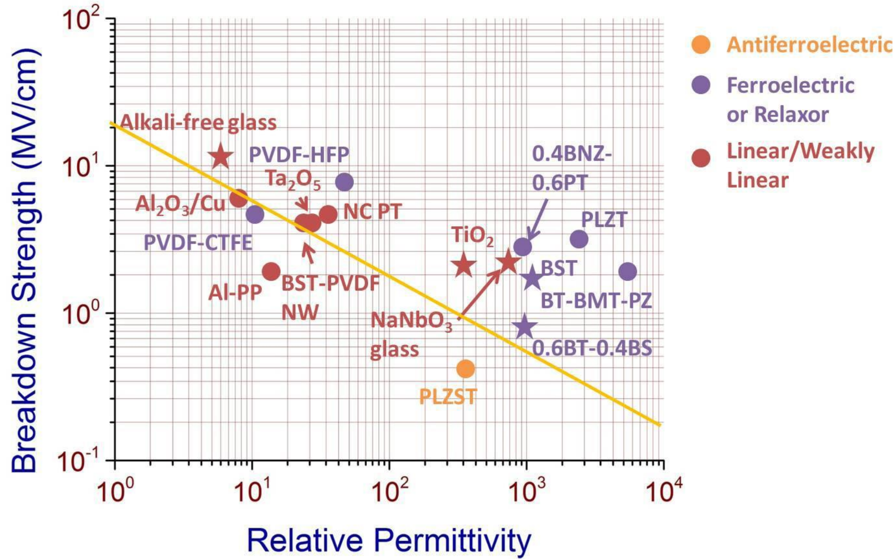


Figure 3-15: Breakdown strength vs. relative permittivity [104].

the distance between the drain and gate. This effectively reduces the electric field across the dielectric and enables the HVOTFT to operate at higher driving voltages. Moreover, there is a trade off between dielectric strength and relative permittivity. It has been shown that there is a correlation between high dielectric strength and low relative permittivity, seen in Fig. 3-15. Additional dielectrics or dielectric stacks must be investigated to optimize for breakdown voltage as well as insulator capacitance.

3.3.2 Reactive RF Magnetron Sputtering

BZN was deposited via a reactive RF magnetron sputtering process. Sputtering is a physical vapor deposition method which uses an accelerated ionized gas to eject materials from a target onto the substrate, depicted in Fig. 3-16. Typically an inert gas like argon is used as the ionized species that performs momentum transfer onto the target. Neon and xenon can be used depending on the atomic weight of the target material. On the other hand, reactive gases such as oxygen or nitrogen can also be introduced as part of the ionized gas mixture. The reactive gases form bonds with the ejected species, either at the target surface, during ejection or at the substrate surface. By controlling the ratio between the inert and reactive gases, one can control the exact stoichiometry of the resulting deposited layer, forming oxides, nitrides

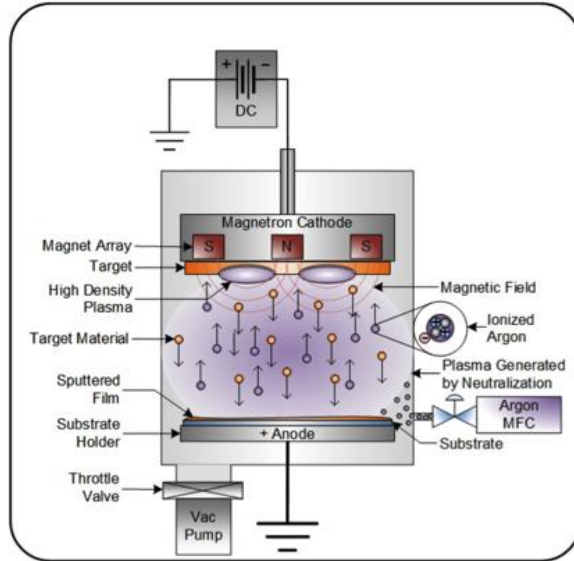


Figure 3-16: Diagram for RF magnetron sputtering deposition [107].

and/or carbides. When the ionized gas is accelerated towards the target (cathode) with enough energy, atoms can be ejected from the target material and deposited in a line of sight fashion onto the surface of the substrate (anode). A sputtering process is different from thermal evaporation in several ways. For one, high melting temperature materials can be used effectively in a sputter tool, unlike in a thermal evaporator. Secondly, the low temperature of the substrate allows for material deposition on thermally limited substrates. Thirdly, the deposition can be done top-down while thermal evaporators work bottom-up. Fourthly, multiple targets can be used simultaneously, allowing for complex alloys to be grown epitaxially. Typically, sputtering tools also include a magnetron directly behind the targets. This magnetron confines the ionized gas near the target surface, increasing the sputtering rate. Another feature of the sputter tool is the ability to perform RF sputtering (13.54 MHz). This prevents charge build up in insulating targets, which diminishes the sputtering rate.

Here, we used an AJA International Orion 5 Sputtering System with a stoichiometric-balanced $Bi_{1.5}Nb_{1.0}Zn_{1.5}O_7$ target of 2 inch diameter and 1/8 inch thickness. The sample was placed face up at the bottom of the chamber on a rotating platform, while the BZN target was mounted at the top, over a magnetron. Once high vacuum

(approximately 10^{-5} Torr) was achieved via a turbo pump, a reactive gas mixture comprising of 9 parts Ar and 3 parts O_2 was introduced into the chamber, at a controlled 3 mTorr pressure. The gas mixture was ionized at an initial power of 60 W. Power was subsequently increased to anywhere between 95 and 140 W to achieve a deposition rate between 0.2 and 0.4 Å/s.

3.4 Parylene-C Organic Dielectric

Organic dielectrics are widely used in OTFTs for their similar low temperature processing capability as well as their compatibility with the organic semiconductors. It has been reported that the oxygen in SiO_2 can oxidize organic semiconductors, leading to a reduced performance of the device [49]. A wide range of organic dielectrics have been used in OTFT development, including polymethylmethcrylate (PMMA), poly-4-vinylphenol (PVP), polyvinylalcohol (PVA), CYTOP, and polypropylene-co-butene (PPCB), all low-k dielectrics. Poly-para-xylylene based polymers, better known as parylene (PAR), has been quite popular in OTFTs as a low-k dielectric as well as a passivation layer, due to its chemical, thermal and UV stability, conformal and ultra-thin coatings, anti-moisture property and high optical transmittance [108]. Parylene forms several important derivatives such as parylene-N (poly-para-xylylene), parylene-C (poly-chloro-para-xylenene), parylene-D (poly-dicholoro-para-xylylene) and parylene-HT (tetrafluoro-poly-p-xylelene), shown in Fig. 3-17. For our HVOTFTs, we introduce parylene-C (PAR-C) as a dielectric layer with low-k (3.15), high dielectric strength (2.68 MV/cm) as well as low gas and moisture permeability properties. Parylene-C is also used as part of a dual dielectric stack to help passivate large surface dipole moments of the high-k BZN to improve charge carrier mobility at the interface between the dielectric and the organic semiconductor channel [109]. Such large surface dipoles inherent in a high-k broaden the density of states (DOS) at the interface, resulting in higher trapping. Finally, parylene-C is also used in the HVOTFT design as an encapsulation layer for the organic semiconductor to prevent air instabilities and reactions with organic solvents during photolithography. The

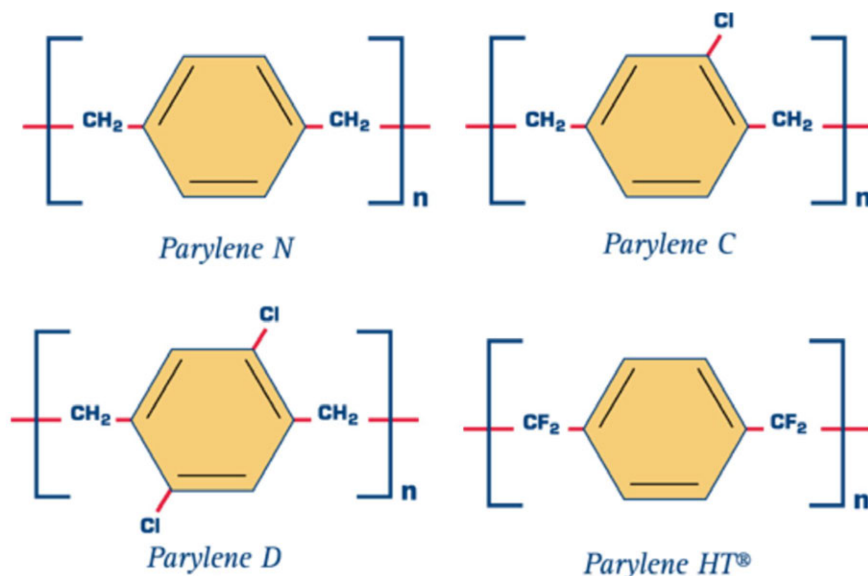


Figure 3-17: Poly-paray-xylylene based polymers, better know as parylene, and its various derivatives [110].

band gap of parylene-C has been cited to be 4.42 eV.

3.4.1 Chemical Vapor Deposition

Parylene-C, used as either an encapsulation layer or as an organic dielectric, was deposited via a chemical vapor deposition using a Specialty Coating Systems (SCS) deposition tool. Parylene-C started as a white powder/pellet dimer called di-para-xylylene, with the deposition occurring over three stages, shown in Fig. 3-18. The first stage involved vaporization via sublimation of the dimer at 150 °C. In the second stage, the gas flowed from the load chamber into the pyrolysis chamber, where the gas dimer broke into single monomers through high temperature pyrolysis. 690 °C at 0.5 Torr was applied to the gas dimer to effectively break the covalent bonds between the CH_2 compounds. Finally, the gas monomers entered the deposition chamber where the temperature and pressure were held at 25 °C and 0.1 Torr. The monomers adsorbed onto the substrate and bonded with other monomers, forming long molecular chains of parylene-C. The deposition was done through a gas diffusion process as opposed to a line of sight process, resulting in conformal depositions. Moreover, parylene-C was formed monolayer by monolayer, ensuring a uniform deposition. A

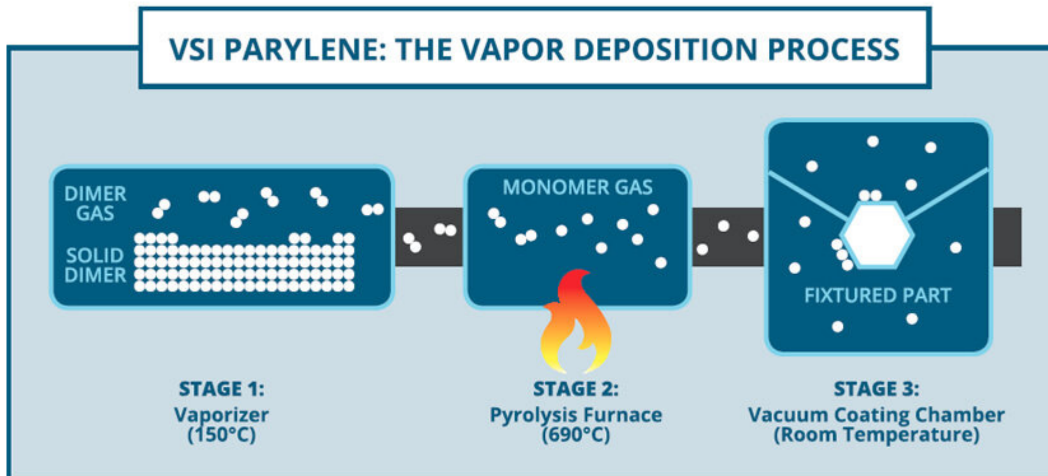


Figure 3-18: The three stages of chemical vapor deposition of parylene-C, including vaporization, pyrolysis and vacuum coating [111].

cold trap was placed between the deposition chamber and the vacuum pump, ensuring that none of the gas monomer reached the pump.

3.5 Gold Metal Contact

In undoped organic semiconductors, charge injection and unipolar charge transport is dictated by the choice of metal contact and its work function alignment with the HOMO/LUMO levels, as described in section 1.3.3. Au has been chosen as the ideal metal contact for the HVOTFT due to its high work function and high conductivity. Fig 3-19 summarizes the work function and contact resistance to pentacene of several common metals and their alignment with the HOMO level of pentacene.

3.5.1 E-Beam Evaporation

Metal contacts were deposited via e-beam evaporation using an AJA International ATC-E Series Evaporation System at a rate of 0.5-3 Å/s. The samples were loaded upside down and at the top of the deposition chamber while the metal crucibles were loaded in a rotating pocket at the bottom. A cryogenic vacuum pump in conjunction with a mechanical pump was used to achieve high vacuum (between 10^{-6} and 10^{-5} Torr) prior to deposition, with typical pump times of 30 minutes to 2 hours. Once high

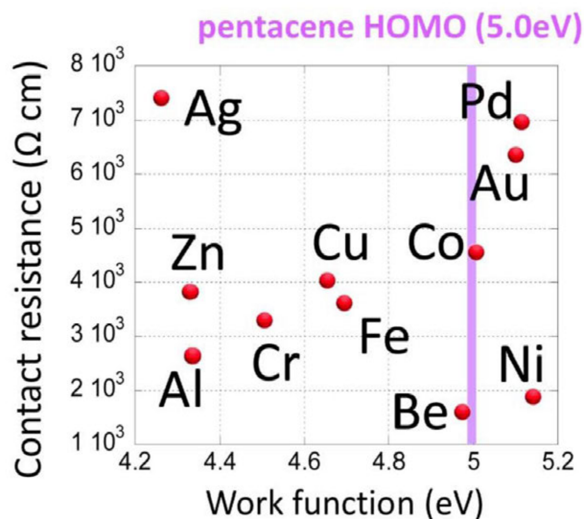


Figure 3-19: Survey of several metals compared with the pentacene HOMO level [112].

vacuum was reached, an electron beam was generated and accelerated towards the metal crucible biased at 8.2 kV. The electrons imparted the majority of their kinetic energy to the metal crucible, eventually resulting in the vaporization or sublimation of the metal. The operational diagram of an e-beam evaporator is shown in Fig. 3-20.

3.6 Self-Assembled Monolayers (SAMs)

Self-assembled monolayers (SAMs) are organic asymmetric oligomers that spontaneously adsorb onto compatible surfaces, forming a single monolayer. SAMs consist of a head group, which covalently bonds with the surface and/or neighboring head groups, a tail group, which forms a crystalline lattice with adjacent SAM molecules, and an end group, which imparts a new set of surface properties to the coated surface. In fact, a simple change of the end group from -CH_3 to -COOH can make the surface go from being hydrophobic to hydrophilic. One of the first SAM, a gold-alkylthiolate monolayer, was introduced by Bell Labs in 1983 [113]. SAMs have since then found uses in scientific fields such as bio-analytics, bio-organics, electrochemistry, as well as electronic semiconductor device [114]. Specifically for OTFT design, SAMs can im-

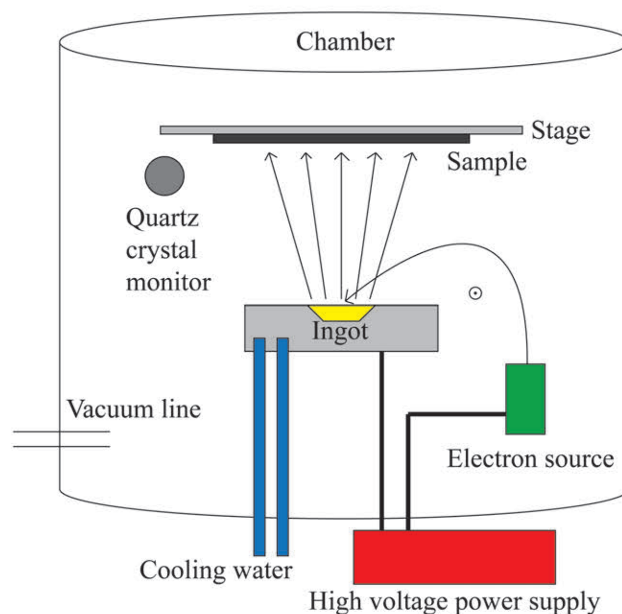


Figure 3-20: Diagram of an e-beam evaporator.

prove charge injection at the metal/semiconductor interface, modify surface energies for either improved organic grain growth or hydrophobic/hydrophilic patterning, as well as replace conventional photoresist as a photo-monolayer material.

Here, we have used a series of organothiol SAMs for Au coating such as thiophenol (TP), 4-fluorothiophenol (4-FTP), 2,3,4,5,6-pentafluorothiophenol (PFT), 1H,1H,2H,2H-perfluorodecanethiol (PFDT) and 1-Decanethiol (DT), as well as organosilane SAMs for oxide coating such as octadecyl- trichlorosilane (OTS), dodecyl-trichlorosilane (DTS) 1H,1H,2H,2H-perfluorodecyltriethoxysilane (PFDTES) and 1H,1H,2H,2H- perfluorodecyltrimethoxisilane (PFDTMS), shown in Fig. 3-21.

3.6.1 Improving Charge Injection via SAMs

Coating Au contacts with organothiol SAMs, ones with a -SH head group which readily covalently bonds with Au, is an effective way in modifying the metal work function for improved charge injection. As was discussed previously, gold exposed to air or organic solvents typically produces a dipole barrier of 0.7 eV, reducing the effective work function to 4.4 eV and reducing hole charge injection in an OTFT.

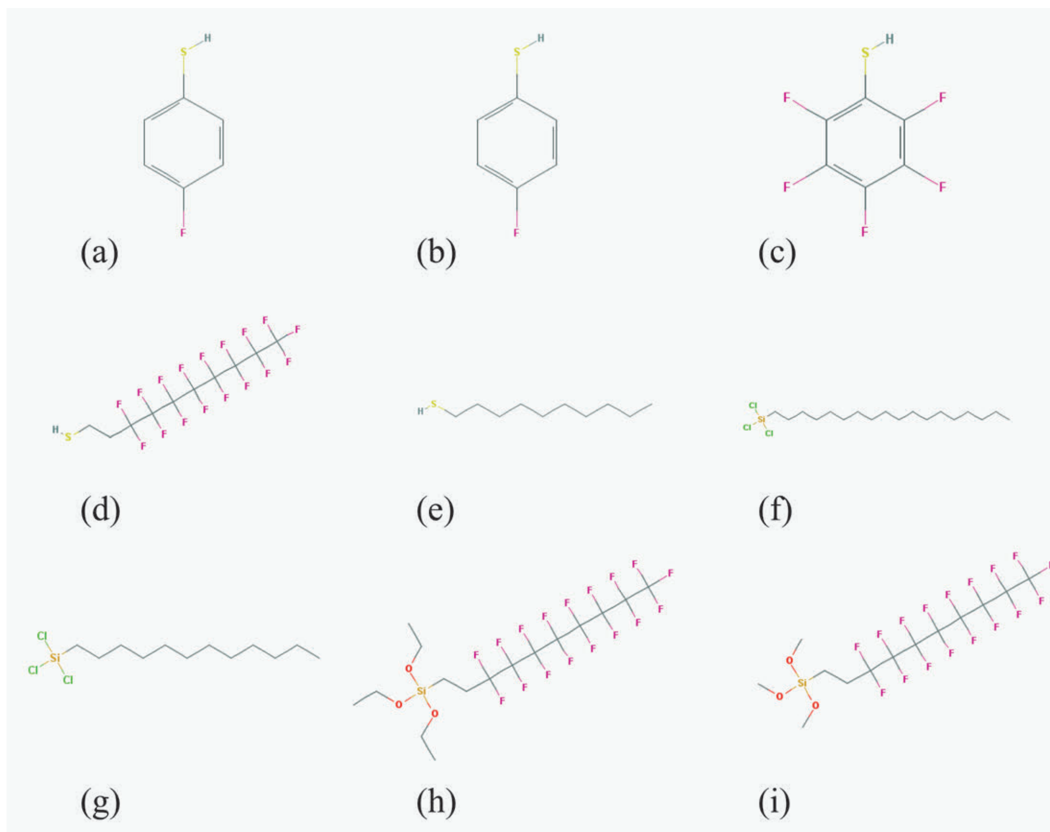


Figure 3-21: Organothiol and organosilane SAMs used in the fabrication process of the OTFT and HVOTFTs. (a) TP. (b) 4-FTP. (c) PFT. (d) PFDT. (e) DT. (f) OTS. (g) DTS. (h) PFDTES. (i) PFDTMS.

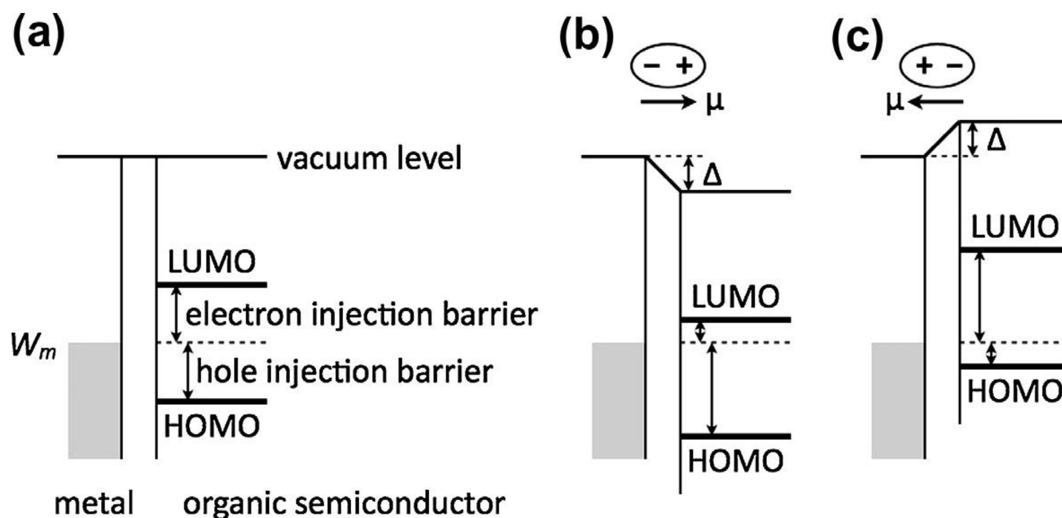


Figure 3-22: Variation in charge injection barriers due to interface dipoles originating from the SAM between the organic semiconductor and the metal contact [115]. (a) Metal and organic semiconductor energy levels. (b) Interface dipole increasing charge injection barrier. (c) Interface dipole decreasing charge injection barrier.

With a SAM, an interface dipole can be introduced to realign the work function with the HOMO/LUMO levels, shown in Fig. 3-22 [115]. If the dipole moment of the SAM molecule points away from the metal (from head to tail), the metal work function is decreased. However, if the dipole moment points toward the metal (from tail to head), the metal work function is increased. The strength of the dipole depends on the oligomer length as well as the nature of the tail and end groups. Marmont et al. demonstrated work function engineering using different types of organothiol SAMs, some of which had hydrocarbons as a tail (dipole moment pointing away from the metal) and some of which had fluorocarbons as a tail (dipole moment pointing towards the metal), shown in Fig. 3-23 [36]. It was shown that decanethiol (DT or CH_3-$(CH_2)_9$-SH) reduced the work function of Au by 0.45 eV while 1H,1H,2H,2H-perfluorodecanethiol (PFDT or CF_3-$(CF_2)_7(CH_2)_2$-SH) increased it by 0.9 eV. Devices made with DT and PFDT showed a 2x decrease and 1.5x increase in mobility, respectively, compared to untreated samples. A similar experiment was conducted by Kim et al. using biphenylthiol (C_6H_5-C_6H_4-SH) and fluorobiphenylthiol (CF-C_5H_5-C_6H_4-SH) which reduced and increased the Au work function, respectively [115].

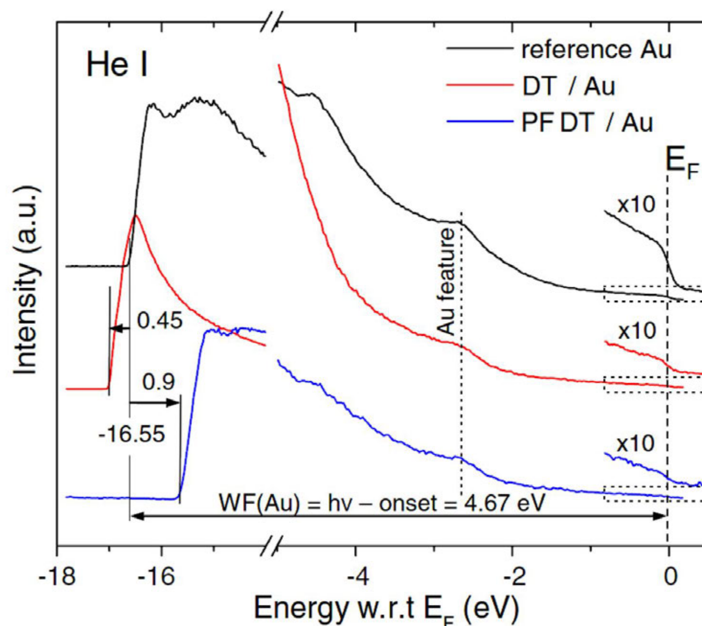


Figure 3-23: UPS spectra of Au metal and SAM coated Au. Depending on the dipole orientation of the SAM, the effective work function can either be increased or reduced. An increase in work function by 0.9 eV is observed by using PFDT on Au [36].

3.6.2 Organic Crystal Growth on SAMs

SAMs are also efficient in modifying the surface energy to promote organic crystal growth. Kafer et al. demonstrated a transition from planar orientation (parallel to the surface) growth of pentacene on bare gold to a free-standing growth of pentacene, seen in Fig. 3-24 (a) [116]. On bare gold, the planar orientation of the first layer of deposited pentacene maximized the electronic interaction of the π-orbitals with the surface. Further deposition of pentacene resulted in island growths, resulting in very rough surfaces. However, when they coated the gold with an organothiol SAM, the initial wetting layer of pentacene is prevented due to a new low surface energy. (001)-oriented pentacene crystals grow layer-by-layer on top of the SAM coated gold, as seen in Fig. 3-24 (b).

3.6.3 Surface Energy Engineering via SAMs

SAMs can also be deposited to create selective regions of varying surface energies, creating wetting and dewetting regions. For example, selective microfluidic channels

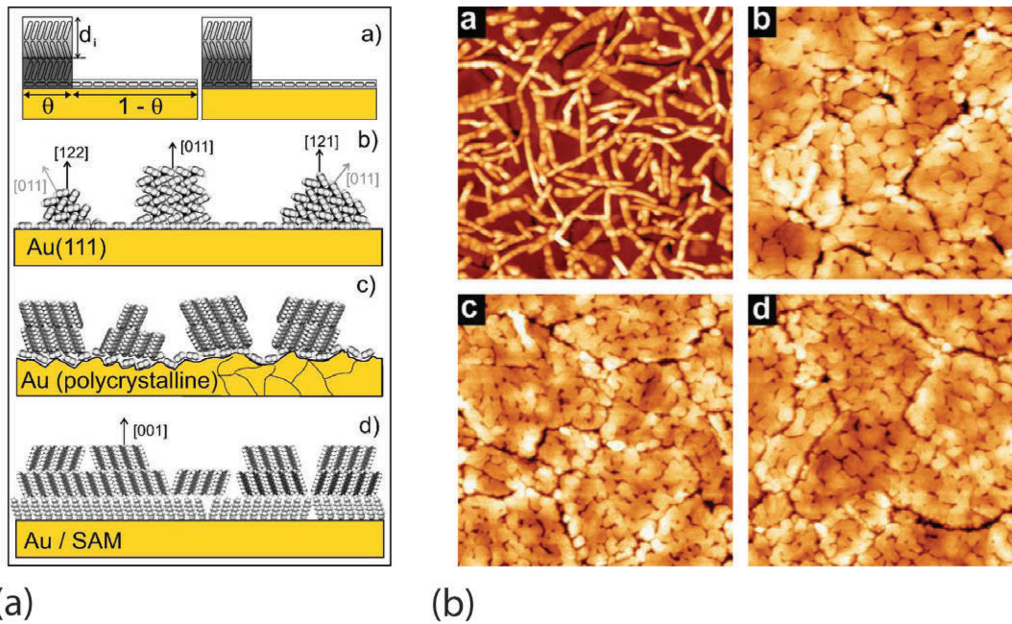


Figure 3-24: (a) Different growth schemes of pentacene deposited on various gold substrates [116]. (b) AFM images of pentacene crystals grown on gold with and without SAM treatment [36].

can be developed to partition liquid droplets of varying surface tensions, which can be used in the biomedical field or in filtration systems. Researches have also used SAMs to control the wettability of various metals and insulators. For one, controlling the wettability can help decrease the buildup of ice and snow on power network equipment such as cables and towers [117]. It was shown that ice adhesion decreased on Al alloy surfaces in the presence of a dimethyl-n-octadecilchlorosilane SAM [118]. Second, change in wettability can improve condensation heat transfer for water and refrigerant based systems by promoting water droplet formation [119]. SAMs have also been used as an anti-stiction coating for released MEMS, a common problem where the surface adhesion forces exceed that of the mechanical restoring force of the structure [120].

In the context of OTFTs, SAMs can play an integral role in selectively patterning the organic semiconductor deposited via a solution-process. The interplay between the solution and the varying surface energies on the sample can lead to a self-aligned solution-process where the organic semiconductor is deposited in wetting regions, avoiding the need for subsequent and incompatible photolithography and etching

processes. This process is discussed in detail in chapter 7.

3.6.4 SAMs for HVOTFT Integration

The two most popular classes of SAMs are the organothiol and organosilane SAMs, which are used in this dissertation.

Organothiol SAMs, such as alkanethiols or thiophenols, have a -SH functional sulfur group that readily covalently bonds with Au with a bond strength of 40 to 50 kcal/mol. Organothiol SAMs are used to improve the charge injection of hole carriers in the OTFT and HVOTFT devices as well as to create a low surface energy utilized in a self-aligned solution processing technique, described in chapter 7. The organothiol SAMs can be easily deposited onto clean Au surfaces via a gas or solution phase, with the self-assembly of the SAMs occurring over 4 steps: chemisorption, lying down phase formation, nucleation of the standing phase and completion of the standing phase, shown in Fig. 3-25 [114], [121]. It has been shown that the degree of order can be enhanced by increasing the length of the SAM [114]. Issues with SAM stability have also been brought to attention, particularly in ambient, aqueous and high temperature environments, leading to deterioration of the order of the SAM [120].

Organosilane SAMs, such as alkylsilanes, form covalent bonds with oxide surfaces such as Si wafers with native oxide, SiO_2, glass, and even Al with a native oxide layer. This results in a surface with properties such as chemical and thermal stability, resistance to solvent swelling, ultra-smooth roughness, mechanically robustness, and controlled wettability [114]. Furthermore, depending on the end group of the organosilane SAM, hydrophobic or hydrophilic properties can be achieved. It is interesting to note that organosilane SAMs allow for direct bonding between an organic molecule and an inorganic molecule. Organosilane SAMs can be deposited on the sample by either a dry (gas) or wet (solution) process. In both processes, four steps generally occur during deposition [122]. Firstly, -OH hydroxyl groups are formed at the surface of the oxide, either through direct contact with water or through water gas molecules. Secondly, the SAMs condense and migrate towards the surface. Thirdly,

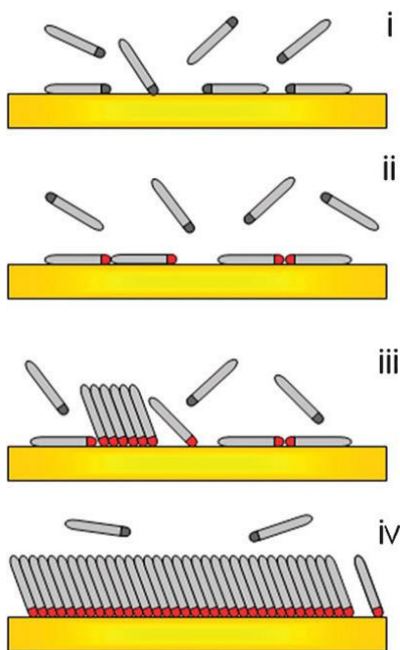


Figure 3-25: The different steps in the self-assembly of organothiol SAMs [120].

the SAMs form hydrogen bonds with the -OH groups. Finally, water molecules are removed from the surface by either a drying or curing process, resulting in covalent bonding between the organosilane SAM and the oxide sample. Typically, there is a single covalent bond between the Si atom from the SAM to the oxide surface. Unlike the organothiol SAMs, it appears that there is no initial lying down phase of the organosilane SAMs. In this case, the organosilane SAMs adsorb onto the oxide surface in an upright fashion, with neighboring SAMs migrating towards each other to form a densely packed monolayer. The difference between a dry and wet deposition process is the quality of the monolayer and the time of deposition, shown in Fig. 3-26 [123]. Under wet conditions, the organosilane SAMs have the potential to crosslink with each other prior to deposition, resulting in quick depositions of large aggregates of SAMs as well as a non-uniform monolayer. The non-uniformity may result in several monolayers being covalently deposited. For dry conditions, crosslinking of SAMs prior to deposition is prevented, with single oligomers bonding with the surface individually. This leads to relatively long deposition times, but uniformly smooth surfaces. Any additional adsorbed organosilanes can be easily washed off.

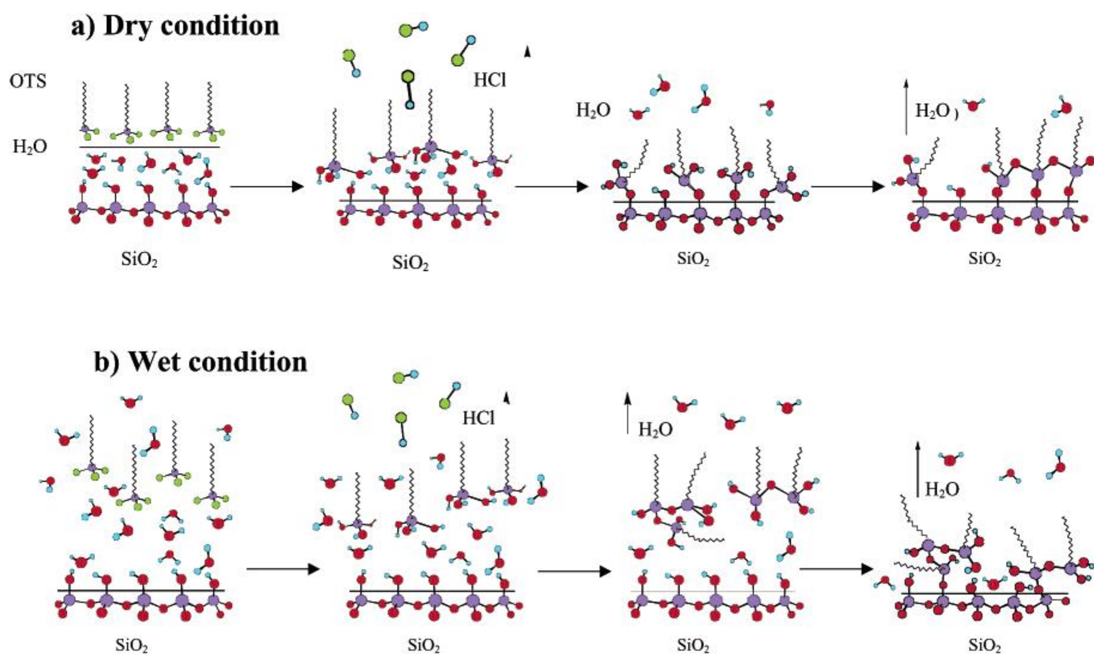


Figure 3-26: Deposition of OTS, an organosilane SAM, onto SiO_2 under (a) dry and (b) wet conditions [123].

3.6.5 Self-Assembled Monolayer Deposition

The different SAMs, summarized in Fig. 3-21. were deposited via either a solution or a desiccator. For a solution deposition of SAMs, proper cleaning of the glassware or Teflon-ware was needed to ensure homogeneous deposition. Minimizing contaminants reduced island formation of SAMs on the sample surface. A series of acetone and isopropyl alcohol rinses, followed by a boiling DI water rinse was used to clean the beakers. However, one can go above and beyond by using the cleaning procedure suggested by Wang et al. [123]. They rinsed their beakers with hexane followed by a cleaning process in a detergent bath set at 50 °C and a DI water rinse. The beakers were then soaked in concentrated nitric acid for 24 hours followed by a DI water rinse. Finally, beakers were wrapped in aluminum foil and dried in an oven for 24 hours. Once the cleaning procedure was finished, the SAM solution was prepared using 0.1-0.2 vol% of a SAM in ethanol. Samples were submerged in the solution, typically between 30 minutes and 2 hours. A toluene rinse was then performed to remove excess solvent and non-covalently bonded SAMs, followed by a DI water rinse.

A desiccator can also be used to deposit the SAMs on the sample surface, as

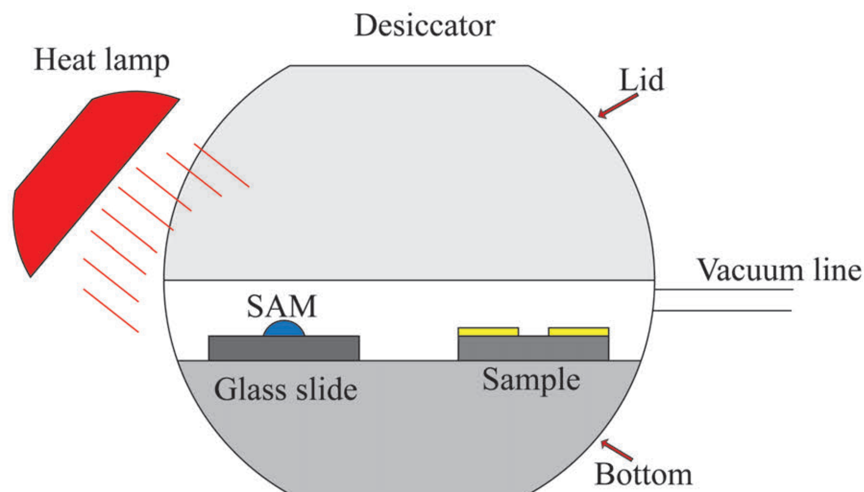


Figure 3-27: Diagram of desiccator setup for SAM deposition.

shown in Fig. 3-27. 200-400 μL of the SAM was dropped onto a clean glass slide inside a desiccator set to 0.6-0.8 atm. The samples were placed adjacent to the SAM droplets. With the reduced pressure, SAMs evaporated and deposited, over several hours, onto the samples. A heat lamp has also been used to increase the vapor pressure of organothiol SAMs to assist in deposition, as discussed in the fabrication procedure for self-aligned TIPS-pentacene HVOTFTs in chapter 7.

3.7 Substrates

Substrates used in TFT designs are usually reserved as the foundation of deposited thin layers and do not contribute to the electrical behavior of the TFT. In OTFT design, either rigid substrates (glass or silicon wafers) or flexible substrates (Kapton polyimide, polyethylene napthalate (PEN), polyethylene terephthalate (PET), aluminum or steel foils, paper or fabric) are used, each with their pros and cons. Rigid substrates have the benefit of an ease in fabrication processes, easier handling, smoother surfaces, and higher thermal budget. On the other hand, flexible substrates appeal to the main attraction of OTFT: flexible electronics. Although mechanically flexible, plastic substrates typically have a low thermal budget and are not compatible with high temperature processes. In both cases, the substrate needs to be mechan-

Table 3.1: Summary of typical substrates for OTFT designs.

Substrate Material	Flexible?	Highest Processing Temperature (°C)	Properties
Si	No	> 1000	Chemical resistant, high cost, used widely in IC fabrication, not flexible
Glass	No	450	Clear, cheap, not flexible
Kapton Polyimide	Yes	275	Chemical resistant, high cost, high moisture absorption
Polyethylene Napthalate (PEN)	Yes	150	Transparent, chemical resistance, cheap, moderate moisture absorption
Polyethylene Terephthalate (PET)	Yes	120	Transparent, chemical resistance, cheap, moderate moisture absorption
Steel foil	Yes	900	Rough surface, moderate chemical resistance, opaque
Paper	Yes	< 100	Rough surface, low chemical resistance, cheap, opaque

ically, chemically and thermally stable during the fabrication process and during operation. Table 3.1 summarizes typical substrates used in OTFT design [124].

For the OTFT and HVOTFT in this dissertation, two types of substrates are used. One is a 4 inch diameter borosilicate glass wafer of 625 μm thickness, procured from Valley Design. The other is a 8.5 inch by 11 inch sheet of Kapton polyimide PV9101, purchased from Dupont. The Kapton sheets are cut out into 4 inch circles for compatibility with the fabrication process. Furthermore, several test samples used for optimization of the fabrication process has been built on 1 inch by 1 inch square pieces of glass slides, diced from 3 inch by 1 inch glass slides.

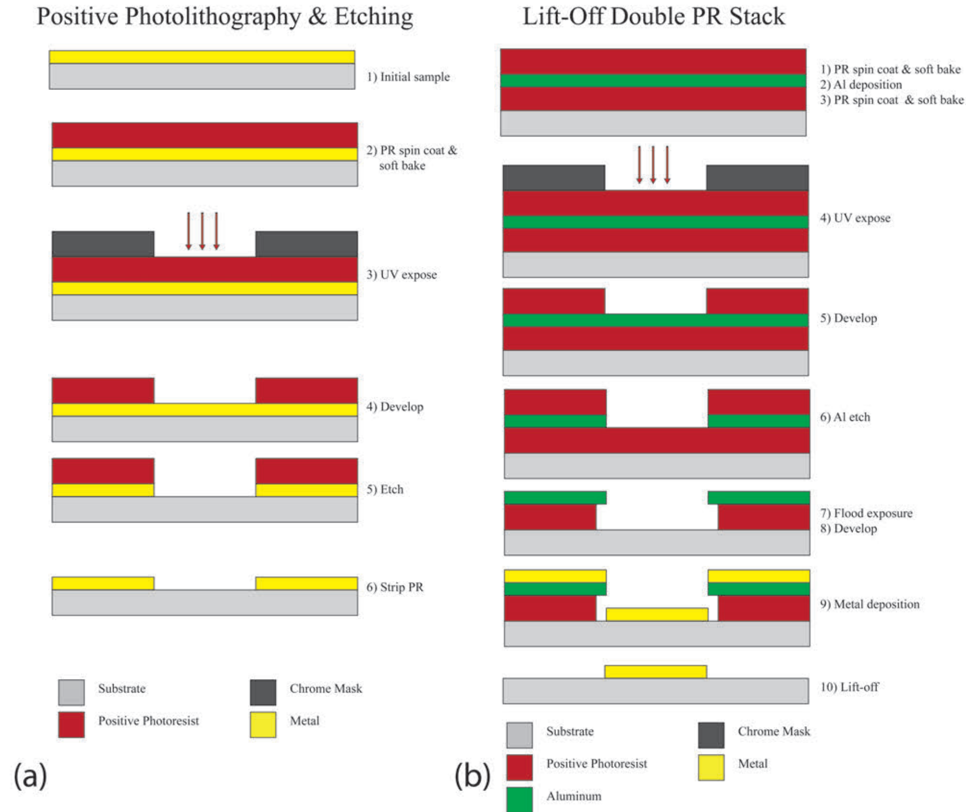


Figure 3-28: (a) Process flow for positive photolithography. (b) Lift-off process using a double positive photoresist and aluminum sacrificial layers.

3.8 Photolithography and Etching

Several methods have been employed to create μm size patterns on materials deposited in the OTFT and HVOTFT. Below is a description of those methods.

3.8.1 Photolithography

Photolithography is the industry standard in transferring a designed pattern onto the sample surface using photosensitive polymer resists (photoresist or PR). Here, photolithography was used to transfer μm size features from a chromium mask onto a positive photoresist, which then allowed selective etching and patterning of the underlying layers. The process flow is shown in Fig. 3-28 (a).

The photolithography process had five steps. The first step involved spin coating a positive photoresist (Megaposit SPR-700) at 3000 rpm for 30 seconds, resulting in

a 1-1.2 μm thickness. The second step required a soft bake in a convection oven at 90 °C for 20 minutes which helped to remove some of the solvent (ethyl lactate, anisole, etc.) from the spin coated photoresist, rendering it more structurally sound. It is noted that a 1 min soft bake over a hot plate was not used as a baking procedure due to the low thermal conductivity of the glass substrate. The third step involved the alignment of a 5 inch soda lime and chromium mask with the features on the sample, followed by a UV exposure (9-10 mW/cm^2) for 10 seconds. The chromium masks were designed using a CAD software and procured from Advance Reproductions Corporation. Alignment and exposure was performed using a Karl Suss MA4 mask aligner with a 350 W high pressure mercury lamp (wavelength of 365 & 405 nm). The fourth step required developing the exposed photoresist in Microposit MF CD-26 developer (97.6% water and 2.4% tetramethylammonium hydroxide) for 30-40 seconds, followed by a thorough DI water rinse and a nitrogen blow dry. Lastly, the sample with the developed photoresist was placed back into the convection oven for a hard bake at 120 °C for 30 minutes to further densify the resist, improving surface adhesion and reducing undercutting during subsequent wet etching.

Although photolithography is the standard in the IC industry, care must be taken when using it with organic semiconductors. Pentacene, for example, is affected by solvents (water, acetone, isopropanol, ethanol, etc.). In fact, mobility was found to decrease by an order of magnitude when exposed to common solvents [125]. This was attributed to a change in surface morphology and "film buckling", as shown in Fig. 3-29 [125]. Encapsulating the pentacene layer with parylene-C and having a bottom contact / bottom gate OTFT architecture can help minimize the effects of solvent exposure. Furthermore, a large amount of organic semiconductors are soluble in solvents, and are not compatible with standard photolithography processes. Alternate methods needed to be explored to be able to pattern solution-processed organic semiconductors, as will be discussed particularly in chapter 7.

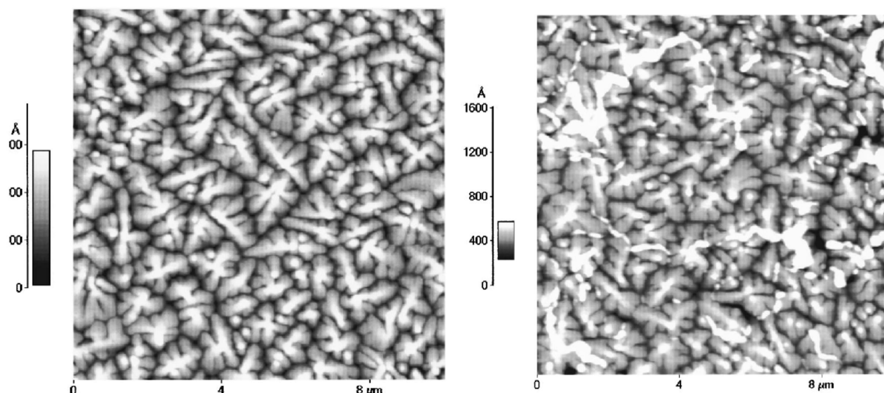


Figure 3-29: 10x10 μm^2 atomic force microscopy (AFM) scans of pentacene showing (a) dendrite grains of as-deposited pentacene and (b) elevated regions due to isopropanol exposure [125].

3.8.2 Wet Etching

Wet etching is a liquid chemical removal process of the surface layers unprotected by the photolithography patterns. Wet etching is comprised of three steps: diffusion of the liquid etchant to the surface of the sample, reduction-oxidation (redox) reactions, and diffusion of the byproducts away from the surface of the sample. Both isotropic (uniform etching) and anisotropic (vertical etching) can be observed in wet etching processes, depending on the crystallinity and grain orientation of the sample. Here, Transene Gold Etchant TFA (55% water, 43% potassium iodide, 2% iodine) and Cyantek Corporation CR-7 Chromium Etchant (85% water, 9% ceric ammonium nitrate, 6% perchloric acid) was used to etch gold and chromium, respectively. Finally, a buffered oxide etch (BOE, 12.5% hydrofluoric acid, 87.5% ammonium fluoride) diluted with DI water (40:1 DI water:BOE) was used to etch BZN.

3.8.3 Dry Etching

Plasmas or etchant gases are used in dry etching to physically (high kinetic energy) and/or chemically remove surface material. An AutoGlow Asher (20-200 W, 13.56 MHz) was used to create reactive oxygen plasma that etched away organic compounds. Parylene-C and pentacene were etched using the oxygen asher.

3.8.4 Lift-Off

In a bottom contact / bottom gate OTFT architecture, the surface of the dielectric was vital in creating a trap free interface between itself and the organic semiconductor. However, it has been reported that the presence of harsh etchants, like those used to etch gold, can change the surface properties of the dielectric [126]. Thus, to avoid contamination of the BZN from potassium iodide, a lift-off process was used to deposit patterned gold source/drain contacts. Lift-off employs a sacrificial layer, typically a photoresist, which when removed, takes the overlaying metal with it, leaving behind the material deposited in the sacrificial layer windows. Initially, AZ 5214 image reversal photoresist was used to create a sacrificial layer for the gold deposition. AZ 5214 started off as a positive resist. However, under an image reversal bake (convection oven, 90 °C, 25 minutes) immediately after exposure, the exposed regions become insoluble due to the activation of cross-linking agents, while the unexposed regions become soluble. This allowed one to create an undercut photoresist structure, which promoted separation of the metal deposited on top of the photoresist from the metal deposited inside the photoresist patterns. Issues with the image reversal process led to using a double stack positive photoresist and aluminum as sacrificial layers instead, shown in Fig. 3-28 (b). In this scheme, SPR-700 positive photoresist was spin coated at 3000 rpm for 30 seconds onto the sample. A soft bake at 95 °C for 10 minutes in a convection oven was used to reduce solvent concentration. 300 nm of aluminum was e-beam evaporated on top of the photoresist at 2 Å/s. A second layer of SPR-700 was then spin coated at 3000 rpm for 30 seconds. Another soft bake in the convection oven was performed at 80 °C for 7 minutes. Exposure (10 seconds) and development (~35 seconds) of the top photoresist was done in the regions where the gold source and drain contacts will be deposited. Transene Aluminum Etchant Type A (80% phosphoric acid, 10% water, 5% nitric acid, 5% acetic acid) was then used to etch the aluminum (5-10 Å/s). Finally, a flood exposure (45 seconds) and a slight over-development (30-35 seconds) resulted in a patterned aluminum and photoresist bilayer, with the photoresist undercutting the aluminum for lift-off promotion. Gold can now be e-beam evaporated over the sample, with gold

forming source/drain contacts inside the sacrificial bilayer windows. An ultrasonic bath and acetone soak is used for lift-off by dissolving the underlying PR and stripping away unwanted metal.

3.8.5 E-Beam Evaporation via a Shadow Mask

E-beam evaporation via a shadow mask was also explored in making bottom gate / top contact devices in conjunction with a self-aligned solution-process method, described in chapter 7. The shadow mask allowed for the deposition and direct patterning of metal without photolithography, at the detriment of resolution. This removed solvents that could dissolve soluble organic semiconductors like TIPS-pentacene, enabling top contact architectures. The 4 inch square steel shadow mask with 0.005 inch thickness was procured from Micron Laser Technologies Inc.

3.8.6 SAM Patterning

As was mentioned previously, SAMs can be used as a high resolution photoresist that can be patterned by UV radiation under an oxygen environment. However, a different tactic to achieve patterned SAMs was employed. Patterns of Au and BZN can be used to selectively deposit organothiol and organosilane SAMs, respectively. If additional patterning was required beyond material selectivity, pre-patterning a layer of photoresist can be used as a lift-off mask. This prevented SAM deposition on parts of the Au and BZN.

3.9 Techniques for Material Characterization

The quality of the materials used was vital in obtaining high performing electronic devices. Several material characterization techniques are briefly summarized here, with additional details found in appendix A, while the measured and calculated material properties are discussed in chapter 4. X-ray diffraction (XRD) under both out-of-plane coupled parallel beam (PB) and in-plane grazing incidence x-ray diffraction

(IP-GIXD) configurations was used to determine the TIPS-pentacene's crystal structure, phase composition, unit cell and Bravais lattice parameters (a, b, c, α, β, γ), inter-planar spacing (d_{hkl}), crystallite size as well as strain. X-ray photospectroscopy (XPS) and energy-dispersive x-ray spectroscopy (EDS), on the other hand, was used for elemental composition analysis, particularly for the reactive sputtered BZN. Furthermore, scanning electron microscopy (SEM) and atomic force microscopy (AFM) were used to produce high resolution images and topographies to help characterize the various material structures as well as their surface roughness. Finally, a goniometer was used to measure the contact angles of select liquid droplets on samples surfaces. Contact angles determined the sample's surface energy, the sum of the intermolecular forces present at the solid surface, which was measured via the Neumann, Owens-Wendt and Wu methods, described in appendix A. For example, a low surface energy solid typically results in poor wetting of a liquid while a high surface energy solid tends to attract other materials. Surface energy and the difference between it and the surface tension of the solvent used in solution-processing proved important in controlling the wetting regions as well as the thickness of the semiconductor, as will be described in chapter 6 and 7.

3.10 Summary

An overview of the different materials used in the OTFT and HVOTFT fabrication have been presented. Two organic semiconductors were used in this dissertation: pentacene and TIPS-pentacene. Pentacene has become a widely studied organic semiconductor due to its ease in deposition, high packing density and large mobility (superior to that of a-Si:H). TIPS-pentacene was also introduced as a functionalized pentacene for solution-processing. Solution-processable materials enable cheap and large area electronics to be developed by eliminating the need for high temperature and high vacuum processes. Two dielectrics were also employed, namely a high-k pyrochlore BZN and a low-k organic parylene-C. BZN was chosen to increase capacitance, critical for achieving low V_T in HVOTFT structures while parylene-C was

used to either passivate large dipole moments from high-k materials or to create an organic compatible dielectric/semiconductor interface with pentacene and TIPS-pentacene. Metal work function, energy band alignment, self-assembled monolayer dipole moments for improved charge injection as well as surface energy engineering via self-assembled monolayers have been discused.

Deposition methods, photolithography processes and etching techniques for OTFTs and HVOTFTs as well as material characterization methods were discussed and are summarized below:

Pentacene:
A thermal evaporator was used to deposit pentacene in high vacuum at a rate between 0.1-10 Å/s. Although pentacene in insoluble, its surface morphology is heavily affected by solvents. Therefore parylene-C was used to encapsulate the organic semiconductor. The parylene-C and pentacene stack was patterned together using photolithography and an oxygen plasma asher.

TIPS-pentacene:
TIPS-pentacene was deposited using a self-shearing drop casting technique which promoted a preferentially directed crystal growth. Variations in the solute concentration, solvent used, slant angle and hot plate temperature have been optimized for quality, size and coverage of the crystal grains, as will be discussed in detail in chapter 6.

BZN:
BZN was deposited using a reactive RF magnetron sputtering tool. 9 parts argon and 3 parts oxygen was introduced to help achieve the proper stoichiometry of BZN, verified by XPS discussed in chapter 4. The dielectric was patterned using photolithography and a diluted 40:1 DI water:BOE.

Parylene-C:
Parylene-C was used as both an organic dielectric and an encapsulation layer. It was

deposited by a chemical vapor deposition via sublimation and pyrolysis of a dimer source. Parylene-C was patterned using photolithography and an oxygen plasma asher.

Gold and Chromium:

Metals used for the contacts were deposited by e-beam evaporation at a rate between 0.5-3 Å/s. The gate metal was patterned by photolithography and a wet etch, while the source/drain contacts can also be deposited and patterned using a double photoresist and aluminum stack lift-off process. A shadow mask has also been employed to do direct deposition of source and drain metal patterns on TIPS-pentacene devices, without having ot use photolithography.

SAMs:

Self-assembled monolayers were either deposited using an ethanol solution or using a desiccator. The ethanol solution proved efficient for organothiol SAMs while the desiccator was sufficient for the organosilane SAMs.

Material Characterization Methods:

Coupled parallel beam x-ray diffraction, in-plane grazing incidence x-ray diffraction, x-ray photospectroscopy, energy-dispersive x-ray spectroscopy, scanning electron microscopy, atomic force microscopy and contact angle measurements were performed to characterize the materials used in the HVOTFT fabrication.

Chapter 4

Device Fabrication and Material Properties

OTFTs and HVOTFTs with either pentacene or TIPS-pentacene have been fabricated with the methods and tools discussed in chapter 3. Multiple iterations of the devices have been fabricated with varying dielectric and SAM layers, different solvents for solution-processing, as well as different field plate designs. Below, the design considerations for the OTFT and HVOTFT as well as the details of the fabrication process and photomasks are presented. The materials deposited were also investigated using scanning electron microscopy (SEM), x-ray photoelectron spectroscopy (XPS), x-ray diffraction (XRD) and atomic force microscopy (AFM).

4.1 OTFT and HVOTFT Design Considerations

Three generations of the OTFT and HVOTFT were fabricated as part of this dissertation, as shown in Fig. 4-1. The first generation involved using vacuum-deposited pentacene. Pentacene OTFTs with channel lengths and widths of 5 to 20 and 250 to 2000 μm, respectively, were first fabricated. Pentacene HVOTFTs were subsequently fabricated by offsetting the drain from the gate contact by 5 to 30 μm. With the offset structure, the breakdown voltage was expected to increase due to relaxed electric field across the dielectric, while the FET properties remained. Furthermore, high-k

cubic pyrochlore BZN and the low-k organic parylene-C were compared for low V_T HVOTFT integration. Although there are different operating requirements for the OTFT and the HVOTFT, the HVOTFT would be best suited for a high V_{DS} and a low V_{GS} scheme, hence, the need for a low V_T. An additional top field plate was added to the pentacene HVOTFTs to help control the electrostatics in the channel and minimize non ideal characteristics. Field plates were placed above the boundary between the gated and offset regions. This allowed the field plate to populate trap states with accumulated charges, effectively minimizing the onset to conduction V_X. Further considerations for the first generation design included the overlap of the patterned pentacene with the source/drain contacts for V_T control.

The second generation devices adopted the solution-processable TIPS-pentacene as the organic semiconductor. Control of the deposition method was critical in forming smooth and large grains of organic crystals that fully covered the sample surface. Different solvents, solute concentration and deposition conditions were optimized for the growth of TIPS-pentacene. Furthermore, SAMs were used to improve charge injection as well as control the thickness of the deposited TIPS-pentacene.

The third generation involved a self-aligned solution-process method in which the TIPS-pentacene was patterned without the use of an etching process. Instead, SAMs were used to selectively control the surface wettability, allowing for the TIPS-pentacene to preferentially grow over the channel region. This lead to transistor to transistor isolation, well-defined channel regions and thin organic semiconductor layers for improved I-V characteristics. As the self-aligned process was a major breakthrough in itself, the fabrication, measurement and discussion have been reserved for chapter 7.

4.2 Masks

5 inch chromium photolithography masks (or photomasks) and shadow masks were designed for the gate contact, dielectric vias, source/drain contacts, SAM patterns, organic semiconductor channel definition, and field plate contact, with three to five of

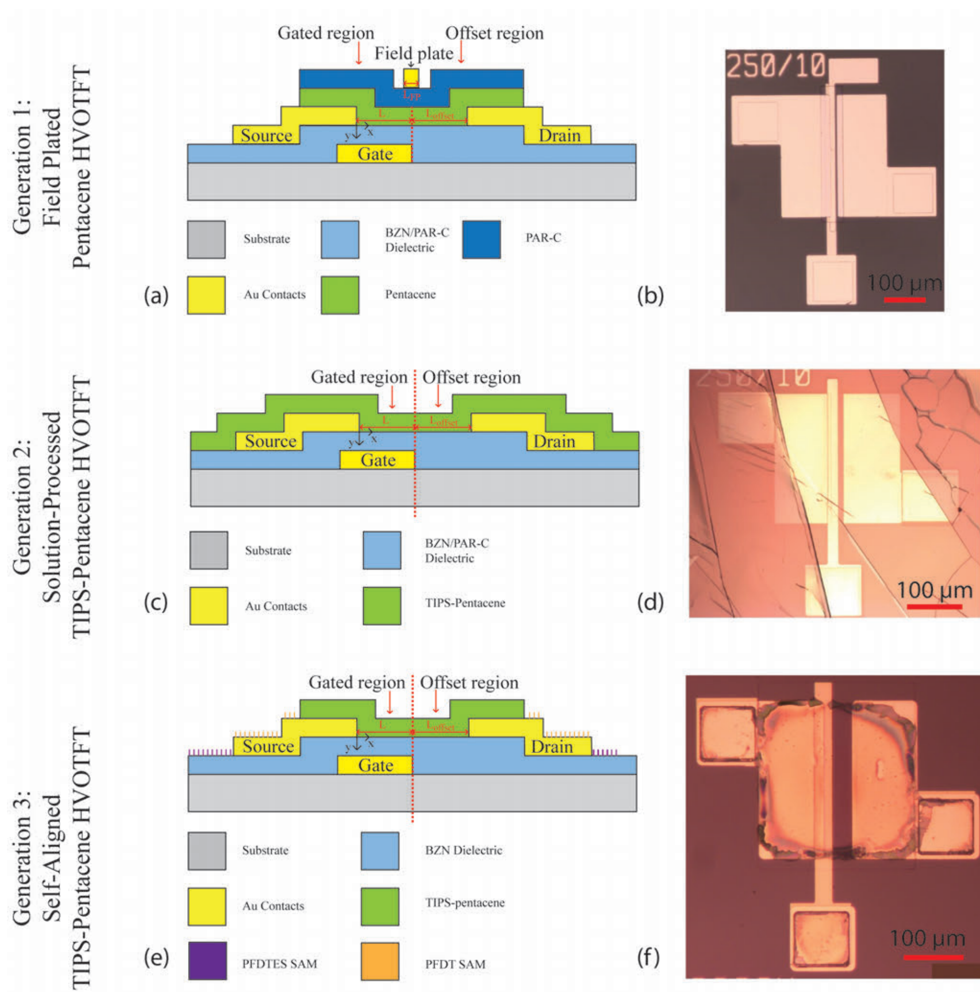


Figure 4-1: Cross-sectional diagrams and optical micrographs for the (a,b) first generation vacuum-deposited pentacene HVOTFT, (c,d) second generation solution-processed TIPS-pentacene HVOTFT and (e,f) third generation self-aligned TIPS-pentacene HVOTFT.

Table 4.1: Summary of the masks used for the different types of OTFT and HVOTFTs made from either pentacene or TIPS-pentacene.

Semi-conductor	Pentacene	Pentacene	TIPS-pentacene	TIPS-pentacene	TIPS-pentacene
Structure	OTFT	HVOTFT	OTFT / HVOTFT	OTFT / HVOTFT	OTFT / HVOTFT
Additional Feature	None	Field plate	None	Top contact	Self-aligned
Contact	BG/BC	BG/BC	BG/BC	BG/TC	BG/BC
Gate	X	X	X	X	X
Via	X	X	X	X	X
S/D	X	X	X		X
SAM	X	X	X	X	X
Channel	X	X			
Shadow				X	
Field Plate		X			

the masks being used for any single design of the OTFT and HVOTFT. The number of masks used per design depended on whether the organic semiconductor was patterned and whether a top field plate was added. Descriptions of the photomasks are given in the appendix and summarized in Table 4.1. The set of overlaid mask patterns for the OTFT and HVOTFT is presented in Fig. 4-2.

4.3 OTFT and HVOTFT Fabrication Process

The fabrication process flow for the vacuum-deposited and solution-processed OTFTs and HVOTFTs is discussed below and shown in Fig. 4-3. Further details of the fabrication process is given in detail in the appendix B.2.

The OTFTs and HVOTFTs were fabricated on 100 mm diameter borosilicate glass and flexible Kapton polyimide substrates. An initial Au gate metal (60 nm), with a Cr adhesion layer (10 nm) was e-beam evaporated and patterned with a wet etch. The gate was topped with a dielectric layer: a low-k organic parylene-C (200 nm, k = 3.15), a high-k pyrochlore BZN (400 nm, k = 25-50), or a dual dielectric stack comprising of BZN (bottom, 400nm) and parylene-C (top, 2 nm). The dual dielectric stack had an

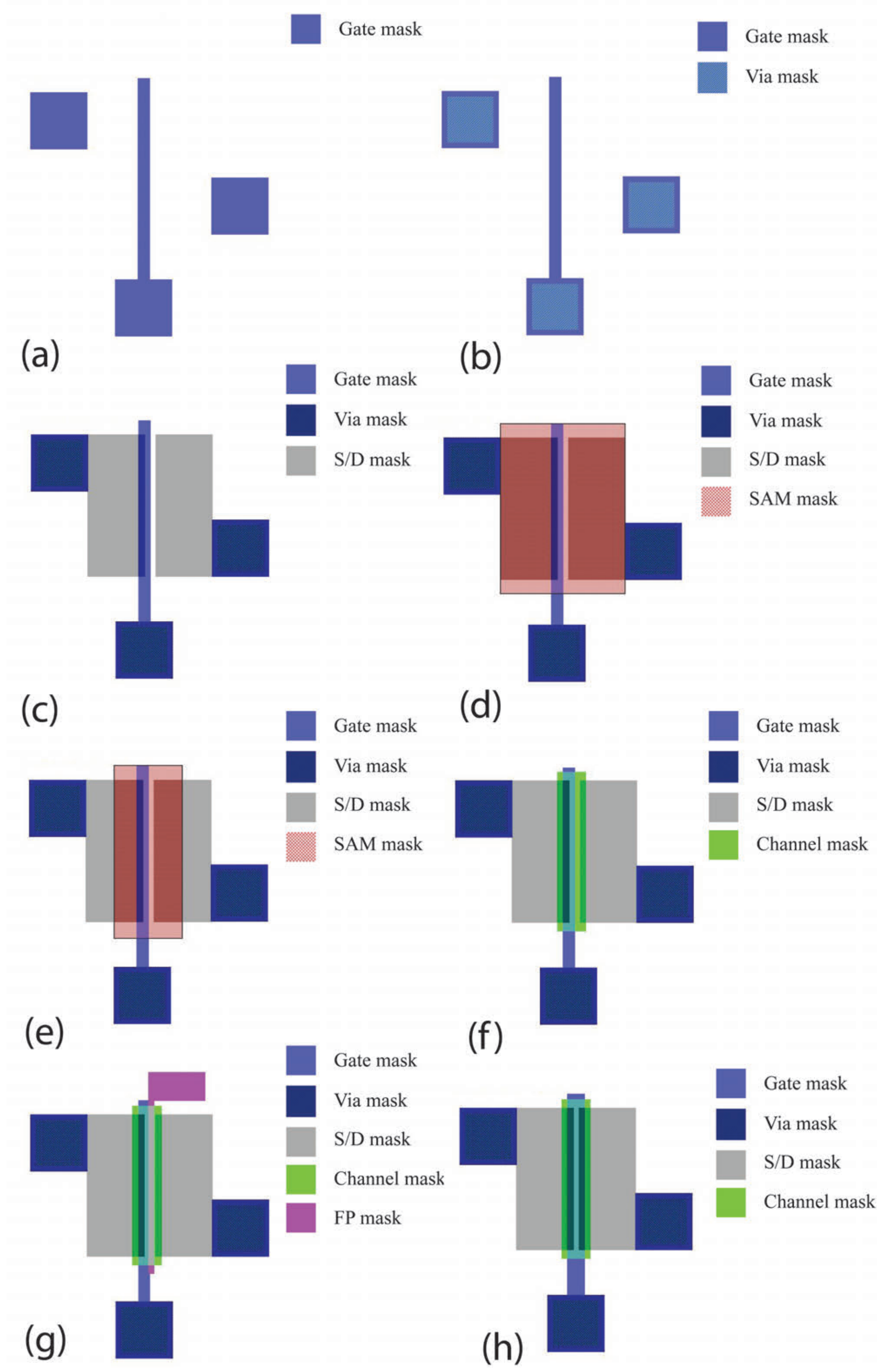


Figure 4-2: Mask set for the HVOTFT: (a) Gate mask, (b) Via mask, (c) source and drain mask, (d) large SAM mask, (e) small SAM mask, (f) channel mask and (g) field plate mask. (h) Mask set for the low-voltage OTFT.

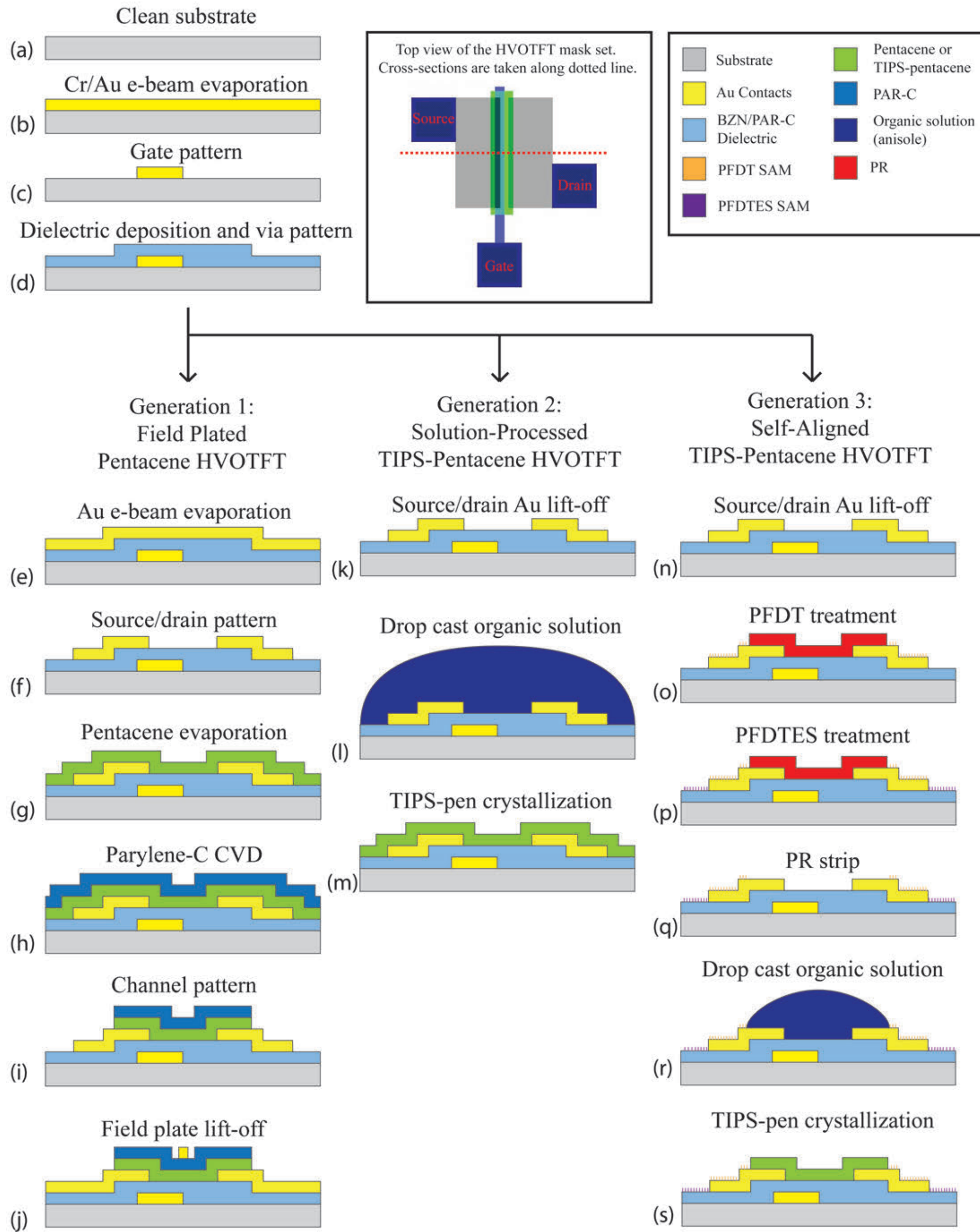


Figure 4-3: Process flow for the generation 1, 2 and 3 HVOTFTs. Initial processes involve (a) substrate cleaning, (b) Cr/Au e-beam evaporation, (c) gate patterning and (d) dielectric deposition and via etching. For generation 1, the following processes are performed: (e) Au e-beam evaporation, (f) source/drain patterning, (g) pentacene evaporation, (h) parylene-C CVD, (i) channel patterning and (j) field Au plate lift-off. For generation 2: (k) source/drain Au lift-off, (l) drop casting of organic solution and (m) crystallization of TIPS-pentacene. For generation 3: (n) source/drain Au lift-off, (o) PFDT treatment, (p)PFDTES treatment, (q) PR strip, (r) self-aligned drop casting of organic solution and (s) crystallization of TIPS-pentacene.

equivalent oxide thickness (EOT) of roughly 40 nm. The top parylene-C in the dual dielectric stack was used as a passivation layer for the surface dipole moments from the high-k BZN [109]. Parylene-C was deposited using a CVD process via sublimation and pyrolysis. On the other hand, BZN was deposited via a reactive RF magnetron sputtering process (9:3 Ar:O_2 gas ratio for plasma generation), with a stoichiometric equivalent BZN target (99.9% purity). Vias were then patterned into the parylene-C and BZN layers by an O_2 plasma asher and a buffered oxide etch, respectively. Next, source and drain Au metal contacts (100 nm) were e-beam evaporated and patterned by either a wet etch or a lift-off process, forming a BG/BC structures. For the OTFTs, the source and drain contacts were aligned to partially overlap the gate contact, forming the channel length L and width W. For the HVOTFT, on the other hand, the source was aligned to the gate contact while the drain was aligned in such a way as to not overlap with the gate, creating a dual channel architecture with a gated region and an offset region that is characterized by an offset channel length L_{offset}. The Au contacts were then coated with an organothiol SAM via an ethanol solution, primarily 1H,1H,2H,2H-perfluorodecanethiol (PFDT), to improve charge carrier injection by increasing the metal work function and reducing the hole injection barrier.

Two different organic semiconductors were used fabricate the OTFTs and HV-OTFTs, deposited by either a vacuum-deposited or solution-processed method. For the vacuum deposition method, pentacene was thermally evaporated under high vacuum (~2e-7 Torr) at a rate between 0.1 and 10 Å/s, for a thickness of approximately 20 nm. For solution-processing, self-shearing drop casting of TIPS-pentacene was chosen for its simplicity and quick turnaround. Different solution-processing conditions were explored for optimal grain growth, and are discussed in the following section 4.4. Here, the final solution-processed condition is described. The organic solution was prepared by dissolving TIPS-pentacene crystals (obtained from Sigma-Aldrich) at 2 wt% in anisole and stirred for over 24 hours over a hot plate set to 50 °C. The solution was then drop casted, in air ambient, onto samples placed on a hot plate set to 50 °C, which was then left to dry for 1-3 hours. The samples were also angled at 4.5°

from the horizontal, allowing the TIPS-pentacene to grow in a preferential directed orientation, along the slant (perpendicular to the channel length), as seen in Fig. 4-4. Nucleation and crystallization of the TIPS-pentacene occurred at the top of the sample, beginning at the evaporation front. The TIPS-pentacene grew to a thickness of anywhere between 0.5 and 3 μm with crystal bands as wide as 3 mm. Typically, thicker TIPS-pentacene layers were observed near the bottom of the sample due to the accumulation of the solution droplet. Additional organosilane SAM treatment of the sample prior to drop casting resulting in a quick shearing of the organic solution. This lead to thin ($<$ 100 nm) crystal bands of TIPS-pentacene, as shown in Fig. 4-5. Details of the benefits of the thinner TIPS-pentacene layers are discussed in chapter 6.

Both vacuum-deposited and solution-processed devices were then coated with parylene-C (200 nm), which acted as an encapsulation layer for moisture and chemical protection. The pentacene could be patterned using an O_2 asher. However, TIPS-pentacene samples were not patterned, due to the semiconductor's non-uniform surface and incompatibility with solvents. Alternatively, organosilane and organothiol SAM coatings of the oxide dielectric and the Au metal contacts, respectively, could be performed to create a self-aligned solution-process in which the solution aggregated towards the high surface energy regions (the channel). This allowed for the patterning of the TIPS-pentacene without the use of photolithography and etching. Details of the self-aligned process, electrical properties and implications are presented in chapter 7.

Au field plates (100 nm) were also patterned on top of the parylene-C encapsulation layer, for pentacene HVOTFTs, directly above the boundary between the gated and offset region. They were used to reduce the peak electric field that appeared at this boundary as well as to control the charge distribution within the channel. Field plates were not fabricated on TIPS-pentacene devices due to the organic semiconductor's solubility with solvents. Nonetheless, the field plates were deposited by e-beam evaporation at a rate of 2 Å/s and patterned via a lift-off process similar for the source and drain contacts.

Figure 4-4: Array of thick (0.5 to 3 μm) TIPS-pentacene OTFTs.

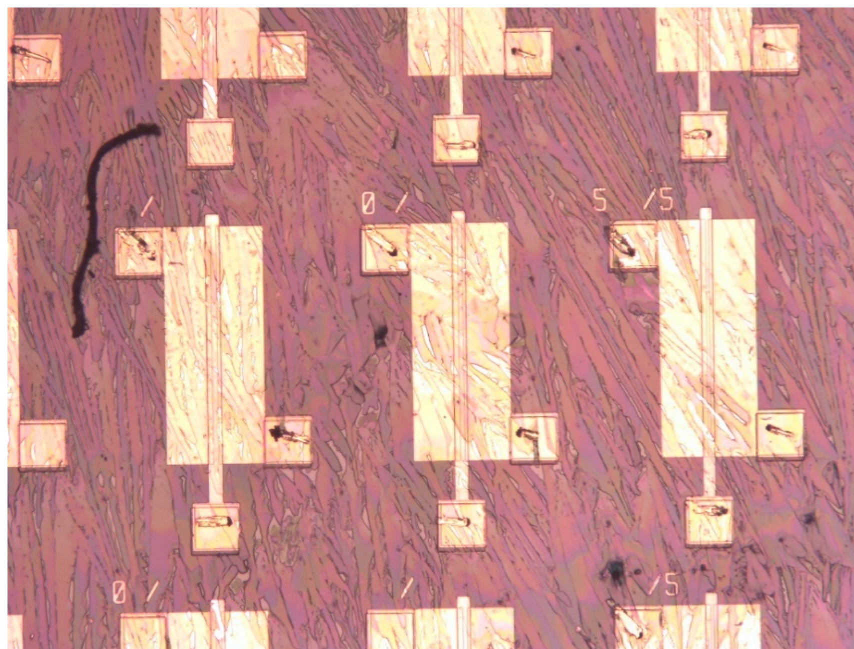


Figure 4-5: Array of thin (< 100 nm) TIPS-pentacene OTFTs.

4.3.1 Bottom Gate and Top Contact Variation

Bottom gate / top contact variations of the OTFTs and HVOTFTs were also fabricated. This allowed for the TIPS-pentacene to be deposited directly onto the smooth BZN, which we could have coated with a single patterned layer of organosilane for surface wettability control. Both BG/TC devices with organosilane SAM and BG/BC with organosilane and organothiol SAMs were used as part of a self-aligned solution process, outlined in chapter 7.

4.4 Self-Shearing Drop Casting of TIPS-Pentacene

A self-shearing drop casting deposition method of TIPS-pentacene for HVOTFT integration was presented in chapter 3, with the final deposition conditions detailed in the appendix B.2. Here, the optimization of the drop casting deposition conditions as well as optical and scanning electron micrographs are examined for grain size and overall coverage of the organic semiconductor.

Initial drop casting of 2 wt% TIPS-pentacene in anisole was performed, in air ambient in a fume hood, on piranha cleaned 1 inch^2 glass slides placed flat on a hot plate. The hot plate was set at RT, 50 and 100 °C, with the glass slides placed flat on top of the hot plate for 30 minutes prior to drop casting. Approximately 300 to 400 μL of organic solution was drop casted on the glass surface and was left to dry in air ambient for 2-5 hours. At RT, a lack of nucleation was observed, with traces of undissolved crystals of TIPS-pentacene sprinkled across the sample. In random areas where nucleation and crystallization had occurred, TIPS-pentacene crystals grew in a dendrite formation, with low overlap between adjacent bands, shown in Fig. 4-6 (a,b). When drop casting was performed on a 50 °C heated sample, crystal grains appeared wider and began to overlap with each other, aggregating into larger grains, seen in Fig. 4-6 (c,d). The thickness of the grains varied anywhere between 0.5 and 3 μm thick with 1-2 μm high coffee stain edges. It was also observed that when the initial organic solution was drop casted onto the glass substrate, initial movement of the droplet across the surface induced a directional growth of the crystal, leading to

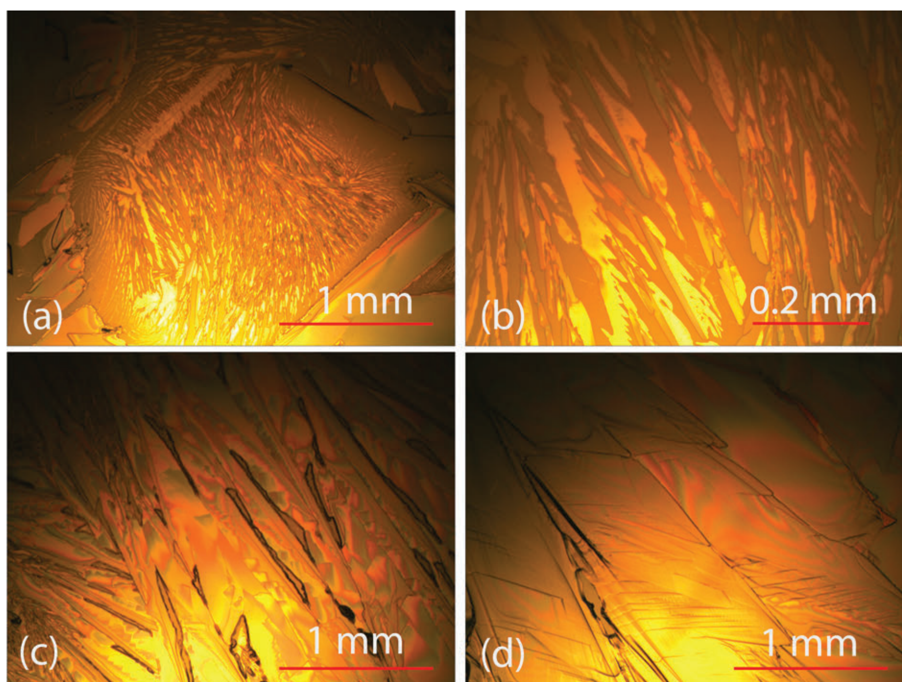


Figure 4-6: Optical micrographs of TIPS-pentacene drop casted (2 wt% in anisole) on flat glass slides at (a) RT at 5x and (b) 20x magnification, as well as at (c,d) 50 °C hot plate conditions at 5x magnification.

long bands of TIPS-pentacene and the notion of a self-shearing drop casting method. Further increasing the hot plate temperature led to a decrease in grain size and coverage of the TIPS-pentacene. This suggested that heat was necessary to promote nucleation and crystallization. On the other hand, excessive heat led to elevated rates of solvent evaporation, reducing the ability of the solute to crystallize in an organized fashion.

A sample slant was introduced to create a self-shearing effect of the solution along the direction of the slant, creating preferentially directed crystal grains. The glass samples were propped up against a micro slide, placed on top of the hot plate. The angles relative to the horizontal surface were approximately 0, 2.5, 4.5, 9 and 13.5 degrees. Initial drop casting done at RT resulted in poor crystallization, proving once again that heat was required for proper crystal growth. Drop casting of approximately 300 to 400 μL of organic solution (2 wt% in anisole) was therefore performed at 50 °C and dried for 1 to 3 hours in air ambient. It was observed that flat to low slant angles of (2.5°) resulted in crystals growing in arbitrary directions which did not cover the

entirety of the sample, as shown in Fig. 4-7. Increasing the angle to 4.5° or higher resulted in full coverage; however, the organic semiconductor aggregated towards the lower half of the sample. Regardless, once an angle of 4.5° or higher was introduced, preferentially directed grains were formed, growing from top to bottom along the direction of the slant.

There also appeared to be two distinct growth regions along the slant. At the top of the sample where the solution was initially rapidly sheared, thin, narrow and highly directed bands of TIPS-pentacene were observed, shown in Fig. 4-8 (a). Their thickness was measured to be approximately 100 nm. As the organic solution reached a quasi-equilibrium with the surface and no longer rapidly sheared, nucleation occurred at the edge of the solution/air interface, continuing the directional growth of the initially sheared crystal grains. These large bands of crystals had a width of 0.2 to 3 mm, indicating the possibility of growing grains that cover large areas of transistors without overlapping boundaries. Furthermore, it was observed that the surface of the crystal bands had plateaus, suggesting a layer by layer growth of TIPS-pentacene. Topographical and composition SEM micrographs of these crystal bands with surface plateaus are presented in Fig. 4-9. AFM scans are also presented in section 4.5.2. The self-shearing drop casting method, with a slanted and heated sample, proved effective in growing preferentially directed and large crystal bands of TIPS-pentacene.

So far, only a single solvent was used for drop casting TIPS-pentacene. Anisole was chosen as a high boiling point solvent to promote crystallization via lower evaporation rates [127]. Mesitylene and toluene were subsequently investigated. Organic solutions using one of the three solvents at varying TIPS-pentacene solute concentration between 0.5 and 2 wt% were drop casted on piranha cleaned glass samples at 4.5° slant and 50 °C hot plate conditions. The optical micrographs are shown in Fig. 4-10, with a summary of the results in Table 4.2. In general, below 1 wt% solute concentration, a lack of full coverage was observed, leaving gaps between the crystal bands. A full coverage is needed to achieve a high success rate of transistor fabrication. 2 wt%, the saturation limit in anisole, was selected for future TIPS-pentacene drop casting. Furthermore, band width differences were observed between the dif-

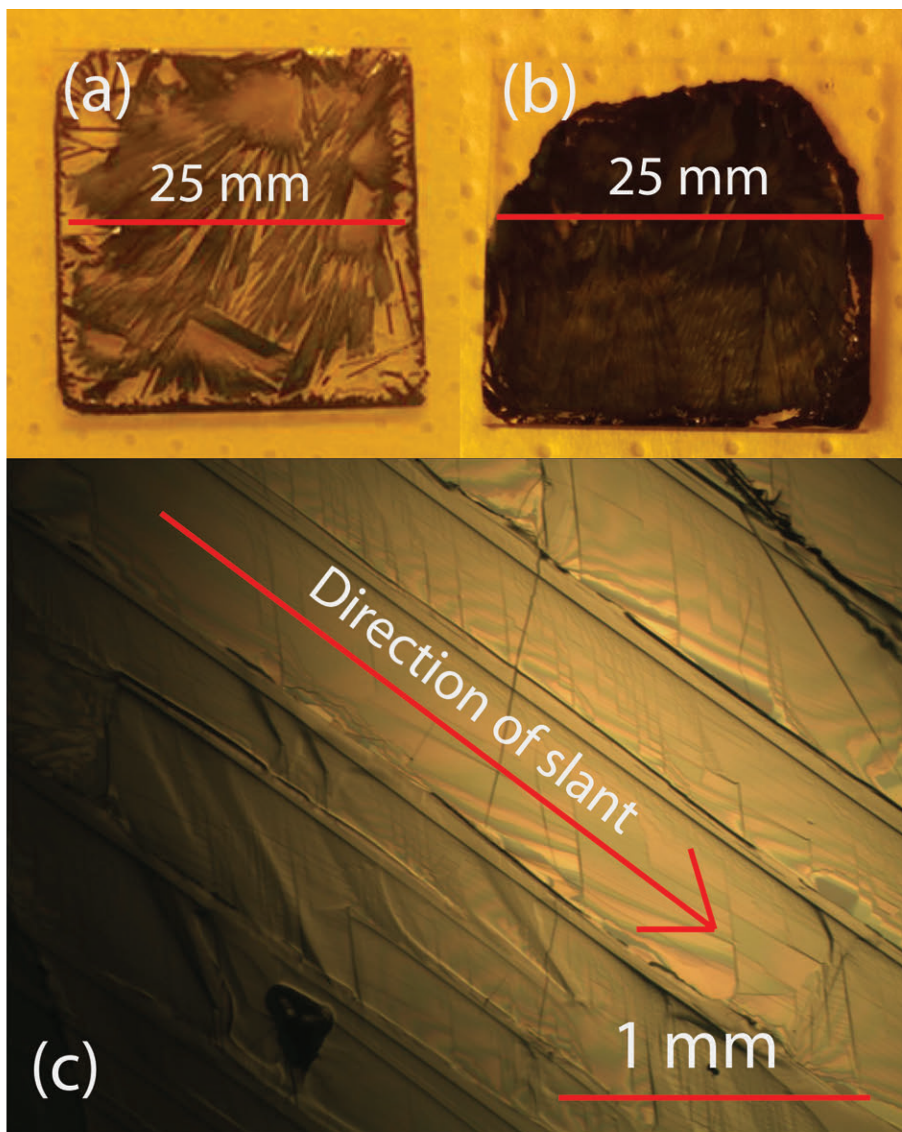


Figure 4-7: Top view of 1 in^2 glass samples with drop casted TIPS-pentacene (2 wt% in anisole) on (a) flat and (b) slanted glass slides (4.5°) over a hot plate set to 50 °C. (c) The growth direction of TIPS-pentacene aligned with the direction of the slant of the sample.

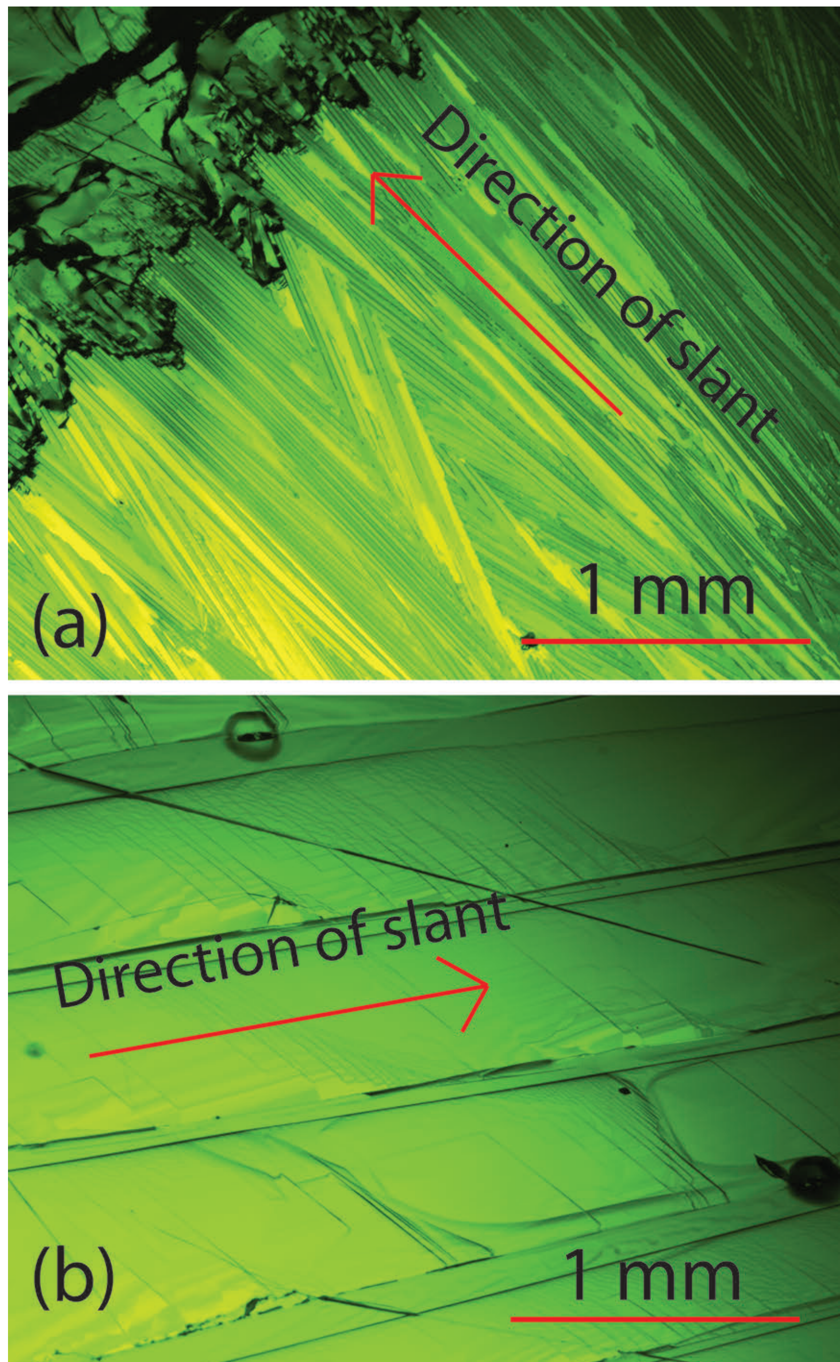


Figure 4-8: Optical micrographs of TIPS-pentacene drop casted (2 wt% in anisole) on a slanted glass slide (4.5 degrees) at 50 °C hot plate conditions, with two growth regions: (a) Initially rapidly sheared and thin bands of TIPS-pentacene at the top of the sample and (b) large overlapping bands along the rest of the sample.

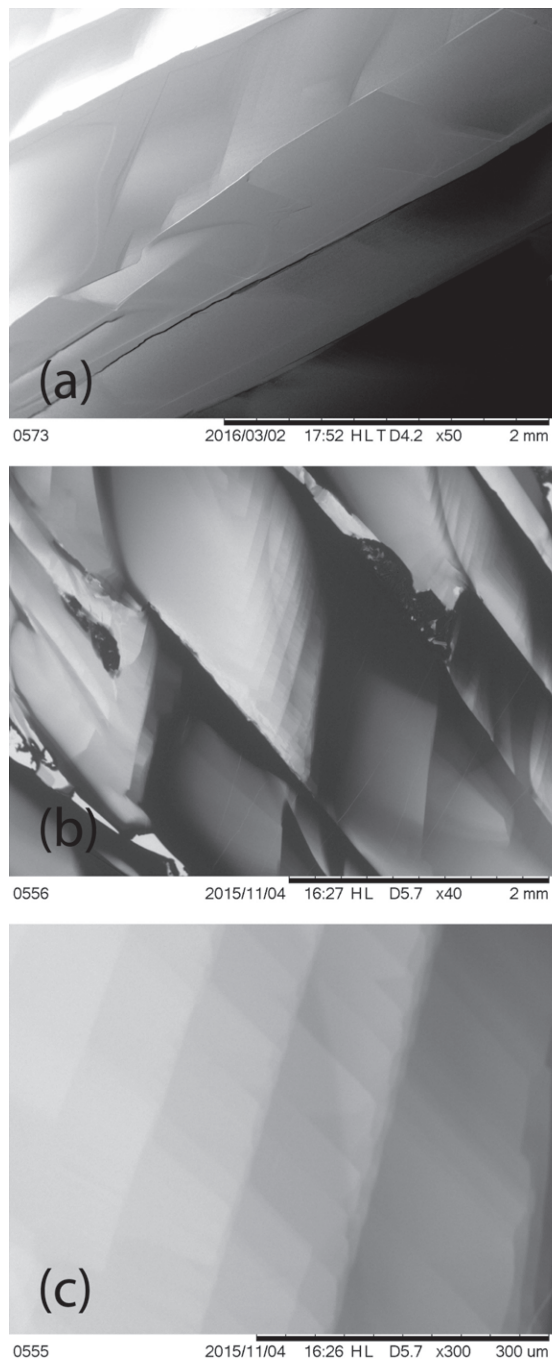


Figure 4-9: (a) SEM topographical and (b,c) SEM composition micrographs of the large TIPS-pentacene bands and its surface plateaus, grown by a self-shearing drop cast method (2 wt% in anisole, 4.5°, 50 °C hot plate conditions).

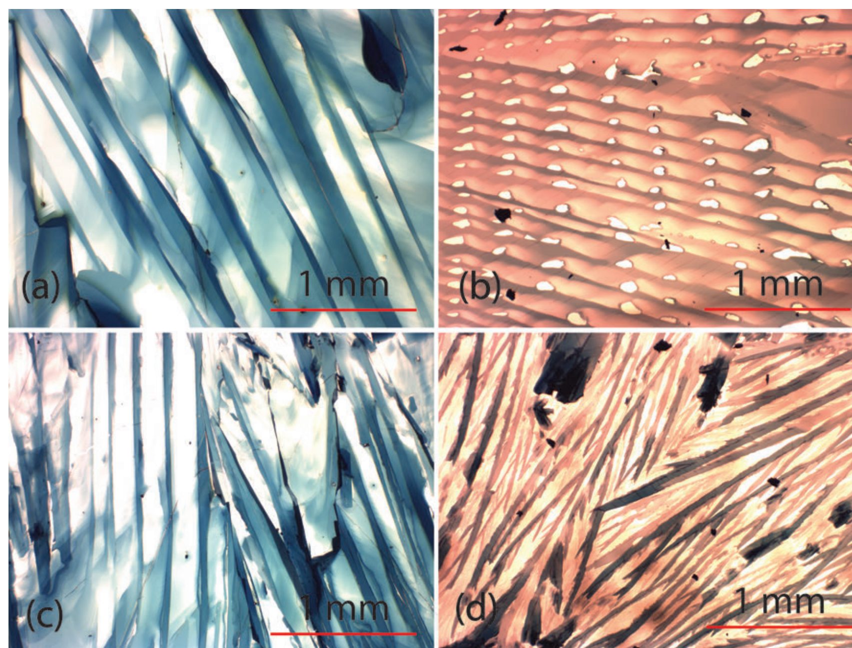


Figure 4-10: TIPS-pentacene dissolved in (a) 2 wt% anisole, (b) 0.5 wt% anisole, (c) 2 wt% mesitylene and (d) 2 wt% toluene, and drop casted on to a slanted and heated sample (4.5 degrees and 50 °C hot plate).

ferent solvents used. In particular, toluene showed narrow bands of approximately 0.1 mm wide whereas for toluene or mesitylene, the bands were 0.2 to 3 mm wide. Finally, mesitylene-based TIPS-pentacene bands, although wide, were observed to be discontinuous more often than anisole-based TIPS-pentacene. Thus, TIPS-pentacene at 2 wt% in anisole was used as the final solution for the self-shearing drop casting method for the HVOTFTs.

4.5 Characterization of TIPS-Pentacene

4.5.1 XRD for Structure and Orientation Analysis

PB XRD and IP-GIXD were performed on TIPS-pentacene crystals that were drop casted on various samples, summarized in Table 4.3. Initially, TIPS-pentacene was drop casted on Au, BZN, parylene-C and glass, materials that are present at the surface of OTFT and HVOTFT samples. From the PB XRD shown in Fig. 4-11, sharp peaks (full width half maximum (FWHM) $\approx 0.1°$) were observed, particularly

Table 4.2: Solvents used for TIPS-pentacene drop casting.

Solvent	Boiling Point (°C)	Surface Tension (mN/m)	TIPS-pentacene (wt%)	Grain features
Anisole	153.8	35.00	2	Full coverage with large bands of width as large as 3 mm
Anisole	153.8	35.00	1	Full coverage with large bands of width as large as 3 mm
Anisole	153.8	35.00	0.5	Lack of full coverage and discontinuous bands
Mesitylene	164.7	28.80	2	Full coverage of wide and discontinuous bands
Mesitylene	164.7	28.80	1	Lack of full coverage
Toluene	110.6	28.52	2	Full coverage with narrow bands of widths of 0.1 mm
Toluene	110.6	28.52	0.5	Lack of full coverage

Table 4.3: List of surfaces, and their respective reported surface energies, used for the growth of TIPS-pentacene and its subsequent XRD analysis. *The BZN surface energy was measured using the Owens-Wendt method with DI water and ethylene glycol.

Substrate for TIPS-pentacene	Surface Energy (mN/m)	Doublets?
Au/BZN/Glass	1000	No
PAR-C/BZN/Glass	27.64	Yes
Au/Cr/Glass	1000	No
BZN/Glass	46.07*	No
Glass	4400	No
SiO_2/Si	40-50	Yes
PFDTES/SiO_2/Si	25.96	No
PFDTMS/SiO_2/Si	16.95	Yes
PFDT/Au/Cr/Glass	18.95	No

Table 4.4: Pawley refinement fit unit cell parameters for TIPS-pentacene.

	a (Å)	b (Å)	c (Å)	α (degree)	β (degree)	γ (degree)
Initial unit cell	7.550	7.730	16.760	89.500	78.700	84.000
Refined unit cell	7.539	7.686	16.701	89.478	78.703	83.963

at $2\theta = 5.30$, 10.62 and 16.04 degrees. Using equation A-1 and an interplanar distance of 16.62 Å, it was found that the diffraction patterns correspond to the set of (00l) planes for TIPS-pentacene, indicating a highly oriented crystal growth and a desired 2D π-stacking on the surface [86], [128]. A Pawley refinement fit (least square of intensity) was also used to fit the diffraction peaks to the (001) planes, with the refined unit cell parameters given in table 4.4. Similar peaks have been observed by Chae et al. for their TIPS-pentacene [129].

Diffraction patterns of TIPS-pentacene grown on parylene-C displayed unique doublets centered around the 2θ peaks of the other samples. The doublets at low and high 2θ are shown in Fig. 4-12, with the 2θ separation value (between 0.1 and 0.2 degree) summarized in Fig. 4-13 (a). Typically, doublets are observed at high 2θ values

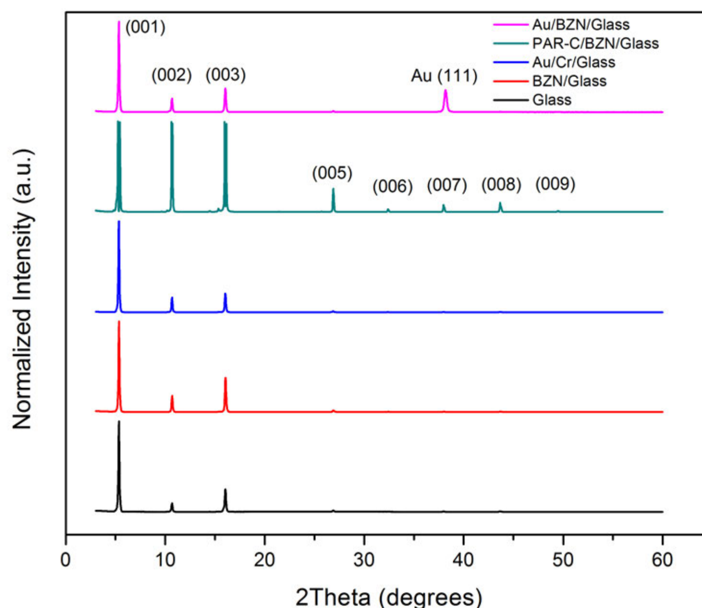


Figure 4-11: Coupled parallel beam XRD plots for TIPS-pentacene drop casted on various surfaces used in the fabrication of the OTFT and HVOTFTs, showing (00l) peaks.

and are a consequence of two x-ray wavelengths being generated by the x-ray source, namely Cu K-α1 (1.54060 Å) and Cu K-α2 (1.54443 Å). Furthermore, the secondary peak originating from Cu K-α2 has a relative intensity of half that of the Cu K-α1 peak. Although doublets of half intensity were observed at 2θ above 25 degrees, doublets were also observed at low 2θ with equal intensity. A combination of compressive and tensile strain present within the TIPS-pentacene deposited on parylene-C can cause positive and negative peak shifts, respectively. Strain was caused by the surface's low surface energy and its interaction with the relatively higher surface tension of the anisole solvent. Homogeneously strained (either compressive or tensile only) would result in a diffraction peak shift in a single direction. In an inhomogeneously strained case where we have both compressive and tensile strains, the diffraction peak is either broadened or peak shifted in both directions, as shown in Fig. 4-14. It is suggested that a either a compressive or tensile strain was present at the interface between the organic semiconductor and the substrate, with the opposite strain man-

ifesting itself at the top of the organic layer to balance out the strain throughout the crystal. Fig. 4-13 (b) shows the adjusted inter-planar d_{hkl} spacing calculated using the 2θ values for the left and right peaks of the doublets. Although strain was present in TIPS-pentacene grown on parylene-C, there was no significant difference in SEM micrographs between the organic semiconductor drop casted on various substrates.

Additional drop cast experiments were then performed on other surfaces, namely SiO_2, PFDT treated Au, PFDTES treated SiO_2 and PFDTMS treated SiO_2, summarized in Table 4.3. The expectation was to observe increased inhomogeneous strain and further broadening of the 2θ diffraction peaks for TIPS-pentacene grown on lower surface energy materials relative to parylene-C. TIPS-pentacene appeared to grow normally on SiO_2. However, in the cases for organosilane and organothiol treated samples, the surface energy difference between the anisole solvent (35 mN/m) and the SAM treated surface ($<$ 26 mN/m) lead to the formation of a bubble with a high contact angle (dewetting). The surface energy difference also lead to an outward pointing force that migrated the organic solute towards the edge of the solution bubble, resulting in the TIPS-pentacene forming a hollow 3D dome once the solvent had evaporated. An SEM micrograph of the organic structures is presented in Fig. 4-15. There was a critical interplay between how the organic semiconductors were deposited and the surface energy of the sample. It appeared that below a certain surface energy relative to the surface tension of the solvent, the organic solute no longer deposited directly on the sample surface, but crystallized along the liquid/air interface. Under PB XRD, (00l) peaks were observed for all TIPS-pentacene samples. Doublets were seen for TIPS-pentacene grown on SiO_2 (40-50 mN/m), but not on PFDT (18.95 mN/m) and PFDTES (25.96 mN/m). A slight doublet in the form of a homogeneous strained crystal (single direction peak shift) was observed in TIPS-pentacene on PFDTMS treated surfaces. The lack of an interface between the organic semiconductor and the low surface energy sample appeared to have resulted in crystals that were relaxed. The diffraction doublet due to inhomogeneous strain in TIPS-pentacene grown on parylene-C and SiO_2 indicated that at a certain surface energy, strain introduced into the crystal planes. It is yet to be concluded if such a

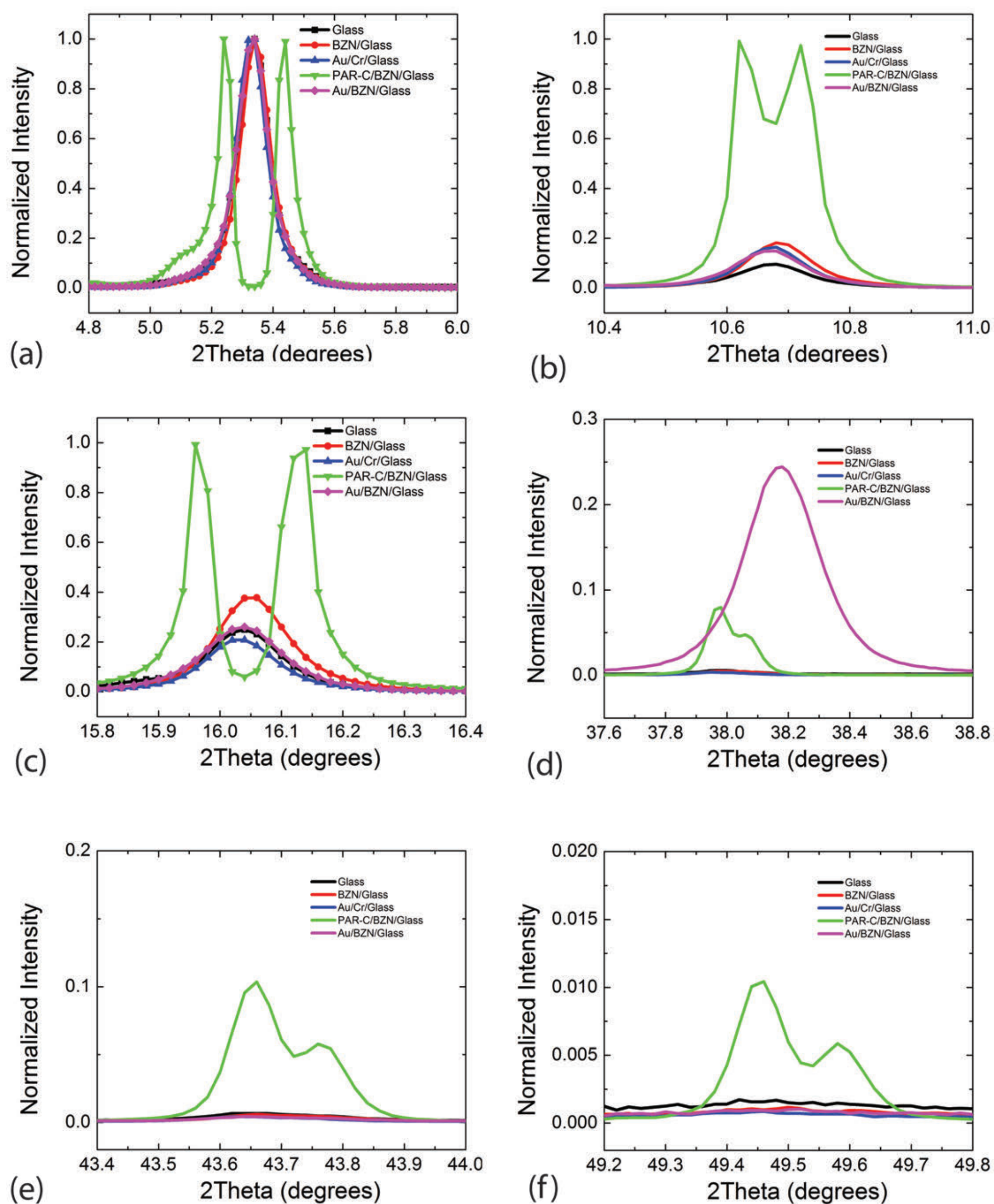


Figure 4-12: Coupled parallel beam XRD plots at low 2θ at (a) 5.30, (b) 10.70 and (c) 16.05 degrees and high 2θ at (d) 38.00, (e) 43.70 and (f) 49.50 degrees for TIPS-pentacene drop casted on various surfaces. Doublets of equal intensity at low 2θ were observed for TIPS-pentacene grown on parylene-C due to strain.

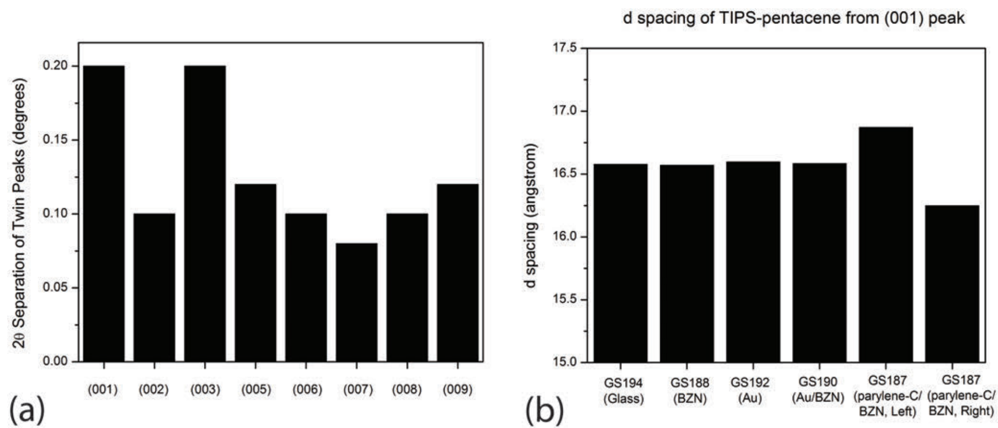


Figure 4-13: (a) 2θ separation between the doublet peaks of TIPS-pentacene grown on parylene-C. (b) Inter-planar d_{hkl} spacing, calculated with the (001) peak 2θ value, for TIPS-pentacene drop casted on various surfaces. Variation in the d_{hkl} arose in strained TIPS-pentacene grown on parylene-C.

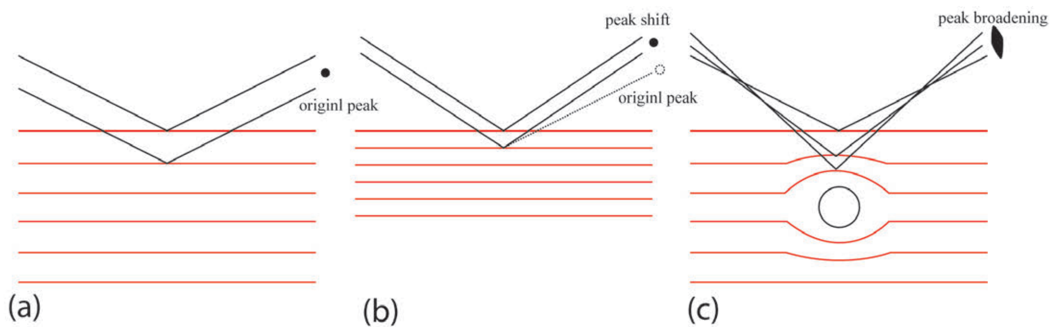


Figure 4-14: Diffraction peaks for (a) an unstrained crystal versus shifted and/or broadened diffraction peaks due to (b) homogeneously and (c) inhomogeneously strained crystals.

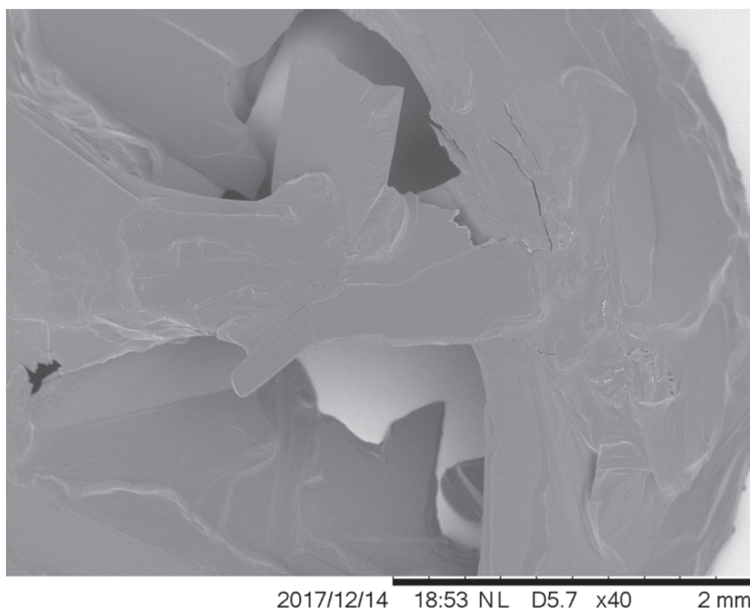


Figure 4-15: SEM micrographs of hollow 3D domes of TIPS-pentacene, grown on low surface energy substrates (SAM treated samples).

strain seen in the TIPS-pentacene grown on parylene-C or SiO_2 affected the mobility of the carriers in the transistors.

IP-GIXD was performed on TIPS-pentacene to establish if there was a preferred crystal plane along the growth direction of the crystal during the self-shearing drop cast method. α_i and α_f, the angle of the source and detector respectively relative to the surface plane was set to 0.12, 0.16 and 0.20 degrees, with the detector sweeping along the $(2\theta)_{in}$ angle. The IP-GIXD diffraction patterns for the samples are shown in Fig. 4-16 and 4-17, where the TIPS-pentacene crystal growth direction was aligned parallel and perpendicular to the incident x-ray, respectively. A (020) peak at $(2\theta)_{in}$ $= 23.2°$ was observed in the diffraction pattern with the crystal grains oriented perpendicular to the incident x-ray, indicating b crystal planes grown 11.6 degrees off of the crystal growth direction.

The crystallite size (size of the coherently diffracting domain) of TIPS-pentacene were also calculated using the Scherrer Equation, which relates inversely the peak

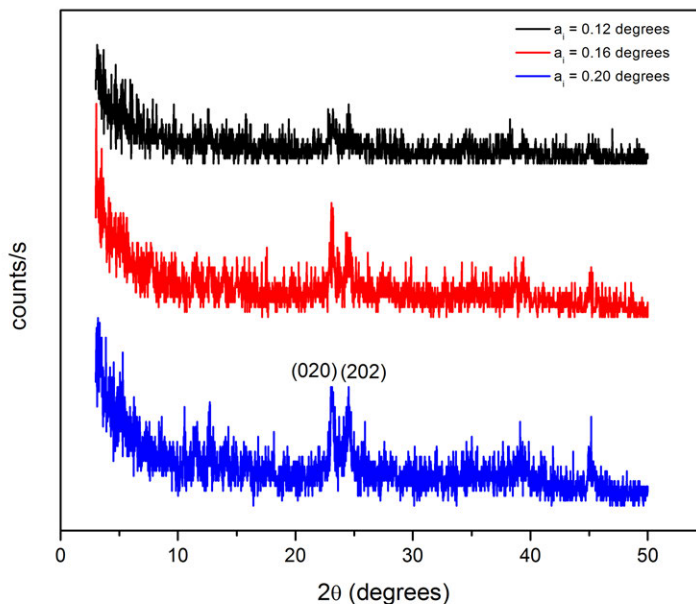


Figure 4-16: Optical micrographs of hollow 3D domes of TIPS-pentacene, grown on low surface energy substrates (SAM treated samples).

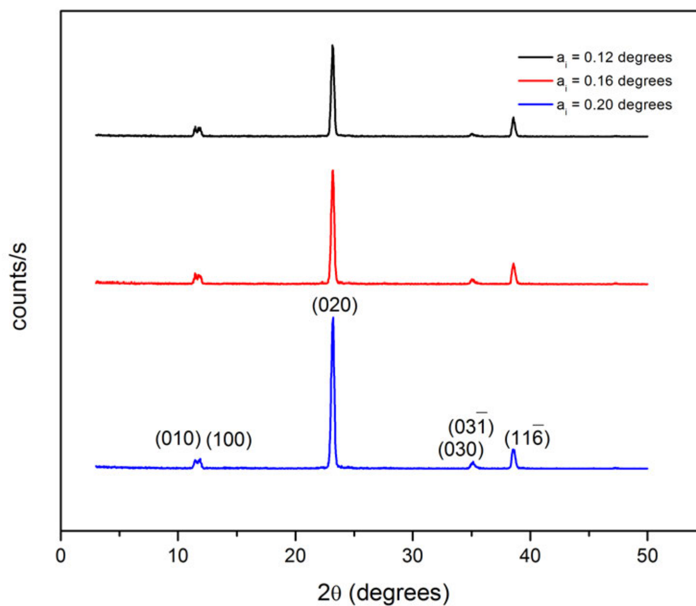


Figure 4-17: Optical micrographs of hollow 3D domes of TIPS-pentacene, grown on low surface energy substrates (SAM treated samples).

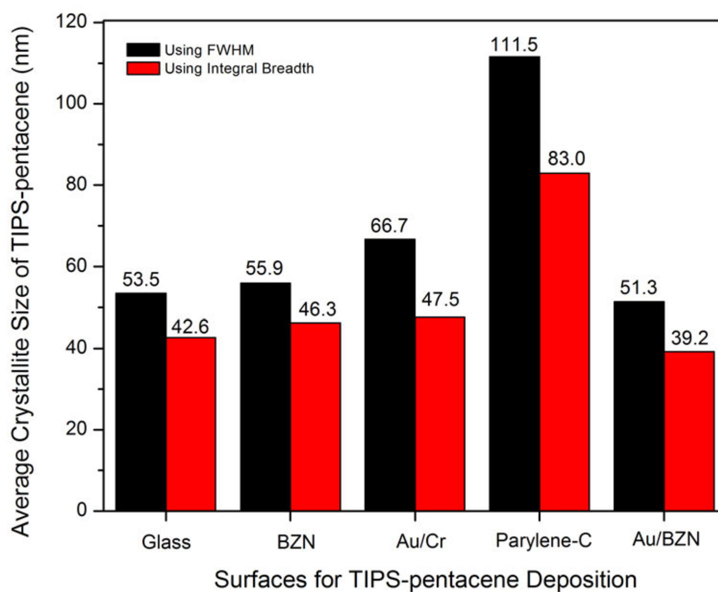


Figure 4-18: Average crystallite size of TIPS-pentacene drop casted on various surfaces, calculated using the Scherrer equation with either the full width half maximum or the integral breadth.

broadening β (in radians) with the average crystallite size D:

$$D = \frac{0.94\lambda}{\beta\cos(\theta)} \tag{4.1}$$

where λ is the x-ray wavelength used during XRD analysis and θ is the Bragg angle [130]. The average crystallite size of TIPS-pentacene drop casted on various surfaces were calculated with either the FWHM or the integral breadth of the (001), (002) and (003) diffraction peaks. The results are presented in Fig. 4-18. Under the FWHM, the average crystallite size varied bteween 51.3 and 66.7 nm for all surfaces but parylene-C, which showed a noticeably higher crystallite size of 111.5 nm. However, the FWHM and integral breaths for the parylene-C case were taken for one of the doublet peaks that arose due to strain. Nonetheless, the crystallite size is comparable or even better than what is reported in the literature, indicating highly crystalline TIPS-pentacene growth [131].

4.5.2 AFM for Surface Analysis

AFM scans were performed on TIPS-pentacene. Large contamination particles (~15 μm diameter) were found on the surface of the TIPS-pentacene. This is of no surprise as the drop casting was done in air ambient and in a non air filtered environment. Nonetheless, disregarding the particles, the surface of the TIPS-pentacene was locally extremely smooth, with Ra and Rms surface roughnesses of 0.1533 and 0.1934 nm, respectively, shown in Fig. 4-19 (a). Features such as plateaus and grain overlaps were also scanned. Fig. 4-19 (b) shows an AFM raster of an end point of a long TIPS-pentacene grain, revealing multiple plateaus having a height step between 1 and 2 nm. This suggested that individual monolayers of TIPS-pentacene were being grown on top of each in an orderly fashion. Fig.4-19 (c) is a scan across two adjacent crystal grains overlapping each other. A large step was measured between the grains, indicating large variations in their thicknesses.

4.6 Characterization of BZN

4.6.1 Determination of Dielectric Constant

Annealed BZN can achieve a dielectric constant of 200 due to its cubic pyrochlore structure [132]. Here, sputtered BZN was not annealed and was measured to have a dielectric constant between 25 and 50. Both QSCV and LFCV measurement were used to determine the dielectric constant, in conjunction with a profilometer thickness measurement of the dielectric. For 50x50, 40x40 and 30x30 μm^2 cross capacitors of 400 nm thick BZN, the dielectric constant k was measured to be ~37.8, as shown in Fig. 4-20.

4.6.2 XPS for Elemental Composition Analysis of Reactive RF Sputtered BZN

XPS analysis was performed on reactive RF sputtered BZN with varying ratios of argon and oxygen species. Si wafers were prepared and cleaned with a BOE etch,

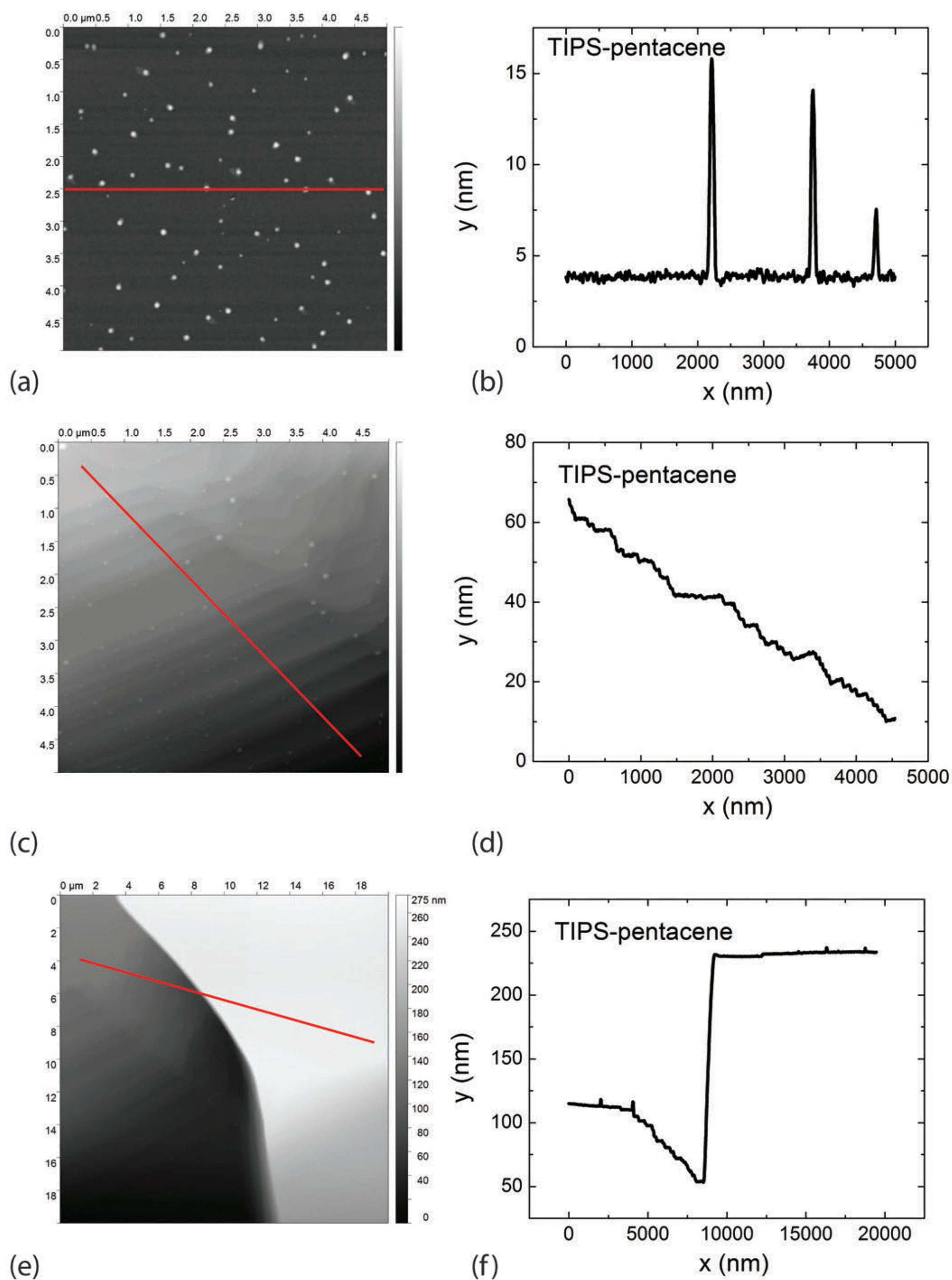


Figure 4-19: AFM scans, and their respective cut line texture along the solid red line, of TIPS-pentacene drop casted on a glass substrate. (a,b) shows smooth TIPS-pentacene surfaces that also readily attracts particles as the solution-process is done in air ambient and a non air filtered environment. (c,d) shows plateaus of TIPS-pentacene. (e,f) shows the boundary between two adjacent TIPS-pentacene crystal grains overlapping each other.

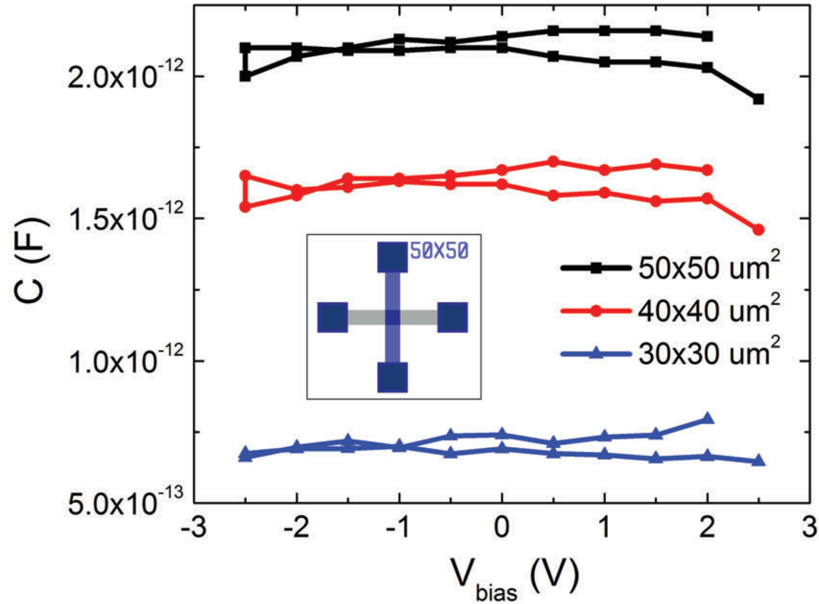


Figure 4-20: QSCV measurements of BZN cross capacitors of varying area, with the inset showing a 50x50 μm^2 cross capacitor.

piranha clean and BOE dip to remove the native oxide and any organic residues. 200 nm of BZN was reactive RF sputtered on the Si wafers at a rate of 0.3 Å/s (95-140 W) with four different argon to oxygen gas ratios: Ar only, 11:1, 9:3 and 7:5 Ar:O_2. XPS analysis was performed with an additional in-situ Ar ion etch (1000 V, 500 nA, 2x2 mm^2) at 1 minute intervals to study elemental compositions of the surface versus the bulk. From Fig. 4-22, for all four BZN prepared samples, it was found that there was a Bi rich and Nb deficient surface relative to an α-phase cubic pyrochlore BZN ($Bi_1.5Zn_1Nb_{1.5}O_7$). The surface of the BZN samples appeared to have a β-phase pseudo-orthorhombic BZN composition ($Bi_2Zn_{2/3}Nb_{4/3}O_7$). Carbon was also found at the surface of the samples, but was removed after the initial Ar etch. After 1-2 minutes of Ar etching, the number of Bi and Zn atoms started to match, as would be expected with an α-BZN. However, continual Ar etch beyond 2 minutes revealed a Nb rich bulk. The Bi metallic phase is suggested to be prominent in as-deposited films and oxidize only after annealing above 120 °C [133]. The presence of carbon may also mask some of the XPS spectra for Zn2p3 due to the low kinetic

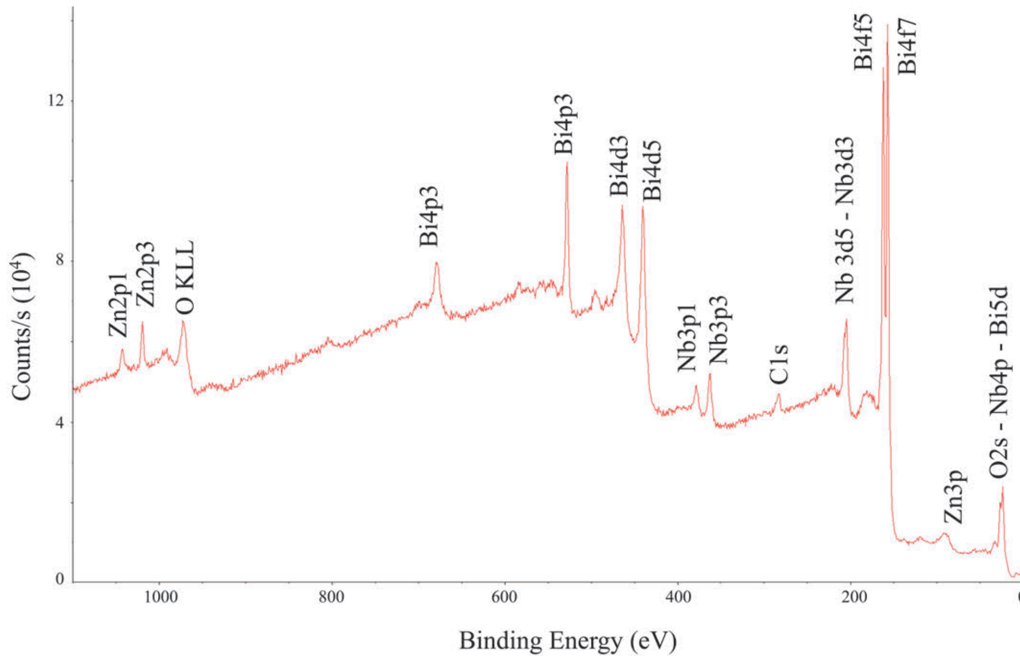


Figure 4-21: XPS spectra of BZN samples prepared at 9:3 Ar:O_2 gas ratio.

energy of the photoelectrons. Furthermore, the Ar etch is expected to remove different elements at different rates, bringing into question the exact stoichiometry of the bulk. Nonetheless, there appears to be a two or three phase BZN structure, with the surface being β-BZN, the immediate bulk being α-BZN, and the deep bulk being a third phase. The stoichiometry of the BZN for all four samples are summarized in Table 4.5. The α-BZN is the most desired structure for BZN, promoting larger polarization and higher-k through the Bi-O bonds as well as tunable dielectric properties [133], [134]. Improved dielectrics for the OTFTs and HVOTFTs may be obtained by dry etching the surface to reach the α-BZN.

When increasing the oxygen to argon gas ratio during reactive sputtering, the stoichiometry of BZN had less variation between the surface and the bulk. Increasing the oxygen reactive species proved efficient in promoting Bi, Zn and Nb sputtering rates, as can be seen in the increasing ratio of these elements relative to oxygen. With additional Bi, Zn and Nb, better structural order of the BZN may be achieved. Furthermore, at low oxygen to no oxygen present during reactive sputtering, Bi4f5/2 and Bi4f7/2 peaks at binding energies of 162.9 and 157.36 eV for Bi-O were initially

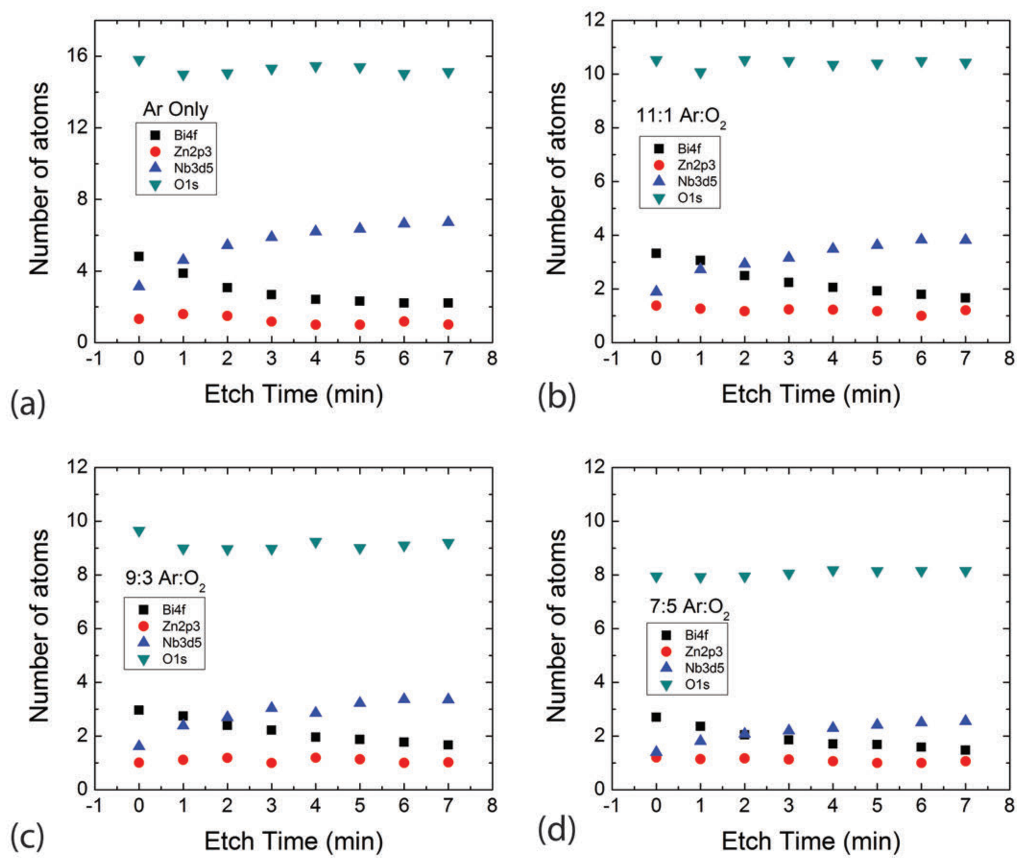


Figure 4-22: Elemental composition analysis of BZN samples prepared with varying reactive gas ratios: (a) Ar only, (b) 11:1 Ar:O_2, (c) 9:3 Ar:O_2 and (d) 7:5 Ar:O_2.

Table 4.5: Elemental composition, found via XPS, of reactive RF sputtered BZN under varying Ar:O_2 reactive gas ratios.

Sample	Ar:O_2	Etch Time (min)	Bi4f	Zn2p3	Nb3d5	O1s
I	1:0	0	4.81	1.32	3.13	15.80
I	1:0	1	3.88	1.59	4.60	14.99
I	1:0	7	2.21	1.01	6.72	15.12
II	11:1	0	3.32	1.38	1.89	10.52
II	11:1	1	3.06	1.27	2.72	10.07
II	11:1	7	1.66	1.21	3.82	10.43
III	9:3	0	2.97	1.01	1.61	9.65
III	9:3	1	2.75	1.12	2.39	8.99
III	9:3	7	1.67	1.02	3.36	9.19
IV	7:5	0	2.70	1.20	1.39	7.95
IV	7:5	1	2.36	1.14	1.81	7.93
IV	7:5	7	1.47	1.06	2.55	8.16

present at the surface, shown in Fig. 4-23 (a,b). However, after continual Ar etching, metallic Bi peaks Bi4f5/2 and Bi4f7/2 at 160.55 and 155.4 eV, respectively, started to manifest [135]. Metallic Bi4f5/2 and Bi4f7/2 peaks were not present in samples prepared with higher contents of O_2 during sputtering, seen in Fig. 4-23(c,d). This further suggested that oxygen during reactive sputtering was critical in forming Bi-O bonds as opposed to having metallic Bi phases.

4.6.3 XRD for Structure Analysis

400 nm thick BZN was reactive RF sputtered (9:3 of Ar:O_2) onto Si wafers with the structure analyzed via coupled parallel beam XRD. A broad BZN (222) peak was observed at $2\theta = 29.18$ degrees. With a FWHM of 7.88 degrees, the average crystallite size was calculated to be 1.09 nm. This suggested that BZN has low crystallinity, and corresponds well with BZN structures reported in the literature [132], [136]–[138]. Increased crystallinity and sharpness of the (222) peak can be achieved with annealing temperatures above 400 °C [132]. To stay true to the low temperature fabrication process presented in this dissertation, the BZN was annealed at 100 °C for up to 48

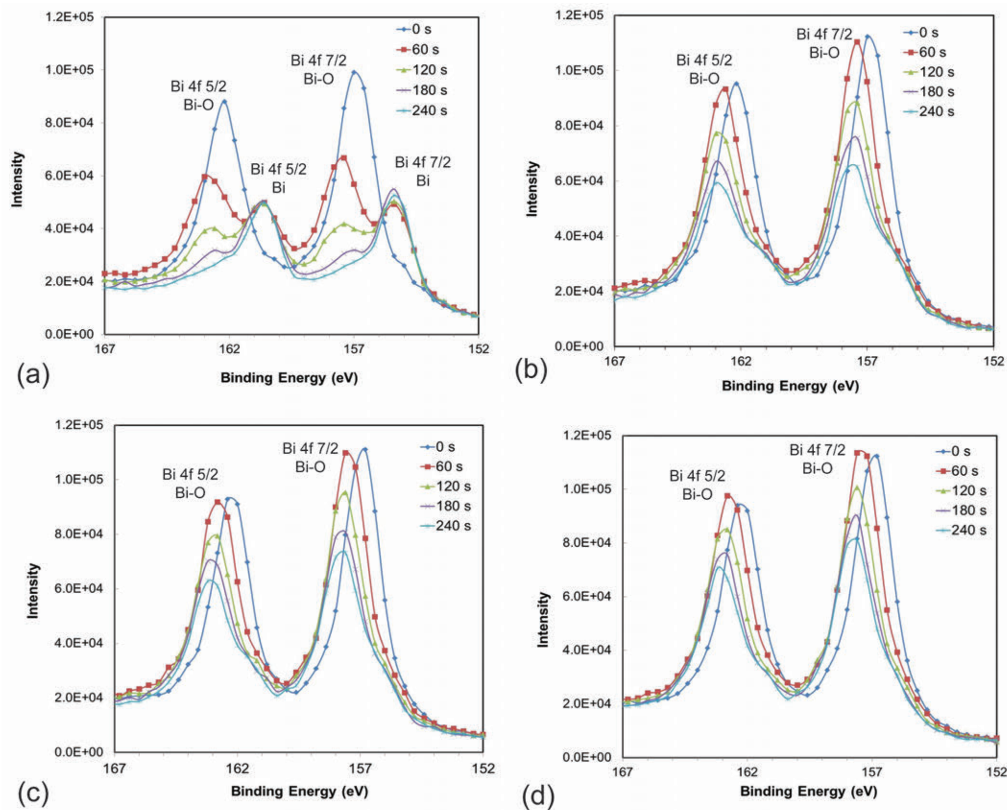


Figure 4-23: XPS spectra of Bi4f5/2 and Bi4f7/2 peaks for both Bi-O and metallic phases in BZN prepared with reactive sputtering gases of (a) Ar only, (b) 11:1 Ar:O_2, (c) 9:3 Ar:O_2 and (d) 7:5 Ar:O_2. In-situ Ar etching at 60 second intervals was performed to compare the surface and the bulk.

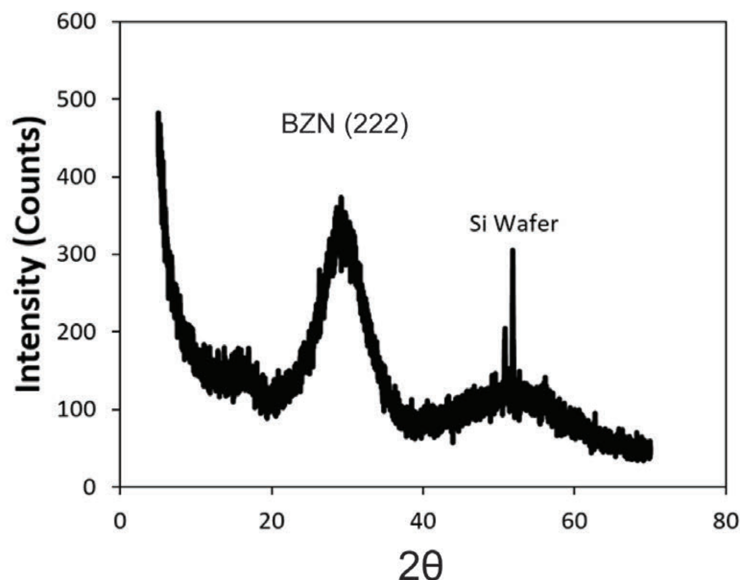


Figure 4-24: Coupled parallel beam XRD plots of reactive RF sputtered BZN.

hours; however, there was no observable change to the (222) peak. This indicated that the fabrication process did not affect the structure of the BZN.

4.6.4 AFM for Surface Analysis

AFM scans were performed on 400 nm thick reactive RF sputtered BZN (9:3 Ar:O_2) on Si. The sputtering rate and RF power were 0.2 Å/s and 95 W, respectively. A 1x1 μ^2 raster is shown in Fig. 4-25. The Ra and Rms surface roughness of the BZN was measured to be 0.1831 and 0.2278 nm, respectively, indicating an extremely smooth surface.

4.7 Characterization of Parylene-C

From QSCV measurements of 250 nm thick parylene-C deposited on glass substrates, the dielectric constant was measured to be 3.27, close to the advertised 3.15 value.

EDS was also performed on 10 μm thick parylene-C deposited on Si. EDS analysis found 90.6% carbon, 8.4% chlorine and 0.6% oxygen in the parylene layers, summarized in Table 4.6, which was close to the atomic ratios between C and Cl in $(C_8H_7Cl)_n$.

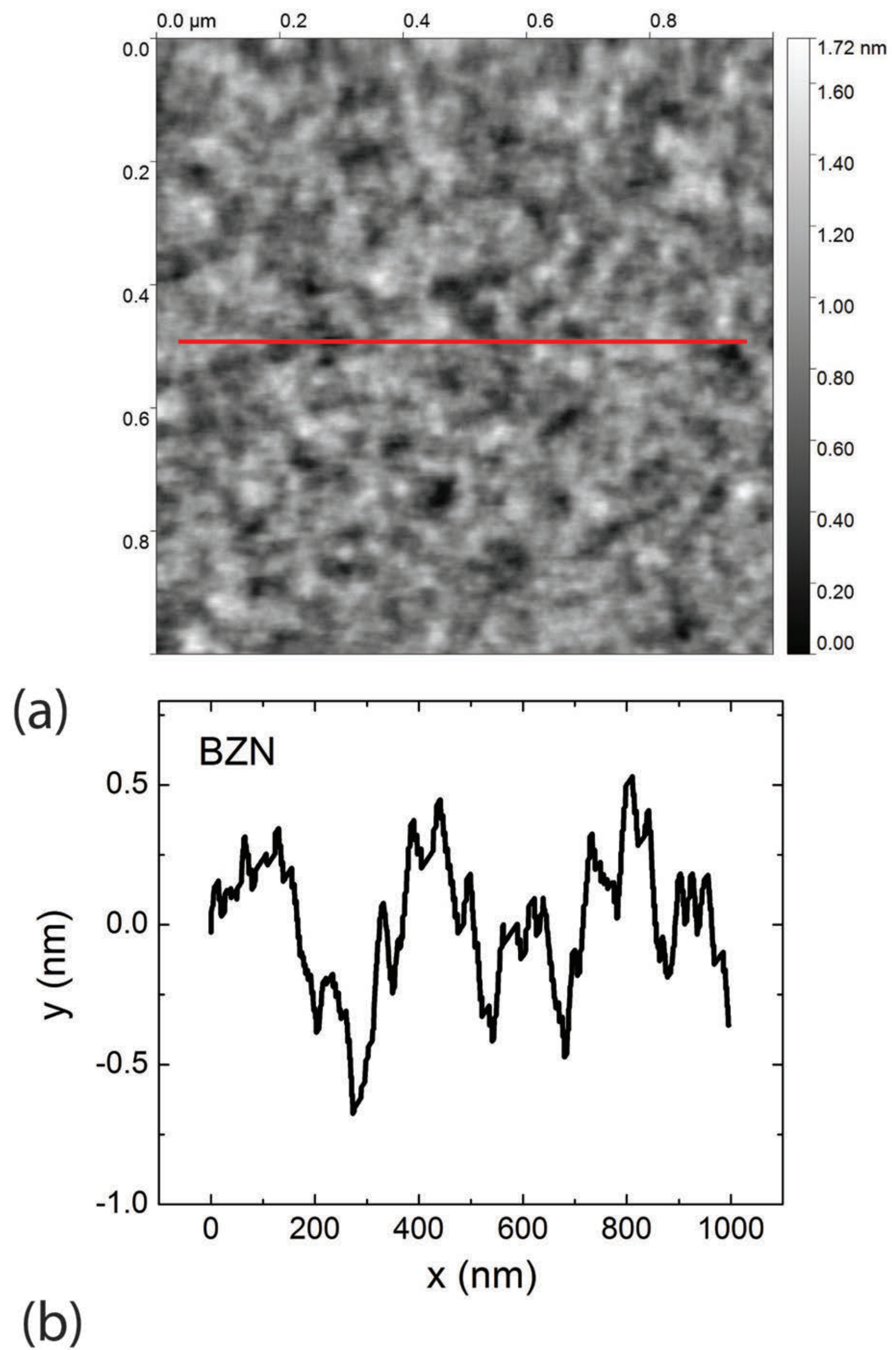


Figure 4-25: (a) AFM scan of 400 nm thick reactive RF sputtered BZN (9:3 Ar:O_2) on Si. (b) Texture cut line (red line in (a)).

Table 4.6: Elemental composition, found via EDS, of parylene-C.

Element	Atomic %
C	90.6
N	0.0
O	0.6
Na	0.2
P	0.2
Cl	8.4
K	0.0

4.8 Summary

Details of the design consideration, the final fabrication process, the set of photomasks used, as well as the material characterization of the organic semiconductors and dielectrics were discussed in this chapter. The HVOTFT was designed with gated channel lengths between 5 and 20 μm and offset lengths between 5 and 30 μm. Both pentacene and TIPS-pentacene as well as both high-k cubic pyrochlore BZN and low-k organic parylene-C have been incorporated into the HVOTFT integration. Additional field plates and self-assembled monolayers were designed to improve charge accumulation and charge injection, respectively.

Of most interest is the ability to perform solution-processing for large area and low cost electronics. Self-shearing drop cast method of TIPS-pentacene was discussed and optimized for HVOTFT integration, with the crystals investigated under SEM, XRD and AFM. It was found that drop casting the organic solution (2 wt% in anisole) over a heated (50 °C) and slanted (4.5 degrees) sample proved the most effective in growing preferentially directed and large crystal bands of TIPS-pentacene (widths of up to 3 mm). TIPS-pentacene was analyzed under coupled parallel beam XRD and was shown to be highly oriented with sharp (00l) peaks with crystallite sizes of ~60 nm. Furthermore, x-ray diffraction doublets at low 2θ were observed for TIPS-pentacene grown on parylene-C specifically. It was suggested that the low surface energy of

parylene-C (comparable to that of the surface tension of anisole) resulted in a two phase growth of TIPS-pentacene, with both a compressed and tensile strain in the lattice. Additional drop casting experiments on lower surface energies resulted in a 3D hollow bubble of TIPS-pentacene. Furthermore, AFM scans indicated locally smooth surfaces (Ra and Rms surface roughness of 0.1533 and 0.1934 nm, respectively), with a layer by layer growth dynamic, seen in the 1-2 nm plateaus at the surface of TIPS-pentacene.

BZN was reactive RF sputtered at rate between 0.2 and 0.4 Å/s under varying reactive gas ratios: Ar only, 11:1, 9:3, and 7:5 Ar:O_2. Under no anneal or low temperature anneal (100 °C), a broad (222) diffraction peak was measured under PB XRD, with a crystallite size of 1.09 nm. The elemental composition of the BZN prepared under different reactive gas ratios was also measured using XPS with an in-situ Ar etch for depth profiling. A Bi rich and Nb deficient surface was first observed for all samples, suggesting a β-phase pseudo-orthorhombic BZN composition ($Bi_2Zn_{2/3}Nb_{4/3}O_7$). However, after the in-situ Ar etch, the ratio of Bi and Nb decreased and increased, respectively, revealing a near surface α-phase cubic pyrochlore BZN ($Bi_{1.5}Zn_1Nb_{1.5}O_7$). Furthermore, increasing the O_2 reactive gas species during sputtering stabilized the stoichiometry of an α-BZN, moving from a metallic Bi phase to a Bi oxide phase. Finally, the BZN was extremely uniform as measured by AFM, with a Ra and Rms surface roughness of 0.1831 and 0.2278 nm, respectively.

Parylene-C was commercially obtained from SCS coatings, and was measured to have a dielectric constant of 3.27.

Chapter 5

Vacuum-Deposited Pentacene High-Voltage Organic Thin Film Transistors

Vacuum-deposited pentacene HVOTFTs were first fabricated, as shown in Fig. 4-1 (a,b), to demonstrate the feasibility of the dual channel architecture in improving the breakdown voltage in OTFT technology. Currently, the majority of OTFT research is centered around low-voltage operation for liquid crystal displays. There are indeed some reports involving inorganic HVTFTs that demonstrated high-voltage operation for field-emission arrays, PV-SOG and MEMS actuation. However, there is little to no research involving HVOTFTs. The development of the HVOTFT would enable novel applications that require high-voltage operation on arbitrary substrates, such as large MEMS integration on flexible substrates, while benefiting from the organic semiconductor's properties. For example, the organic semiconductor's affinity for flexibility as well as its ability to be solution-processed can be leveraged, a discussion reserved for chapter 6. Here, a vacuum-deposited pentacene was initially chosen as the semiconductor due to the relative ease in controlling the thickness of the pentacene layer (< 20 nm) through thermal evaporation, a difficult task for solution-processed organic semiconductors. The development of the pentacene HVOTFT would be a first stepping stone in broadening the operational capabilities of the OTFT technology by

incorporating high drive voltages, a necessary ability for achieving a truly-ubiquitous electronics world.

In a vacuum-deposited pentacene HVOTFT with a dual channel architecture, breakdown voltage was expected to increase with increasing offset lengths due to the reduction of the electric field across the dielectric layer, preventing early dielectric breakdown and enabling large drive voltages. Although this is the key concept behind the HVOTFT, several other key designs and fabrication optimization were required to obtain a workable transistor. Initial low-voltage OTFTs were fabricated for these purposes. For example, the high-k cubic pyrochlore BZN was introduced into the OTFT and compared with the low-k organic parylene-C to reduce the gate leakage as well as the threshold voltage of the HVOTFT. The latter would enable the HVOTFT to be controlled by a relatively low gate voltage. Device structure was also investigated in terms of channel overlap with the drain and source contacts for threshold voltage control. Transistor to transistor isolation in OTFTs is performed by patterning and etching the active channel, which can be made of arbitrary size relative to the source and drain regions. It was expected that larger overlaps would have less edge effects and varied threshold voltages. Furthermore, the deposition rate of pentacene was investigated and optimized for mobility.

Finally, vacuum-deposited pentacene HVOTFTs were successfully fabricated using the process described in chapter 4. With the addition of the offset region in series with the gated region, the HVOTFT was able to achieve large breakdown voltages VBD beyond -550 V. In fact, the breakdown voltage could be engineered by controlling the length of the offset region. Although the HVOTFT exhibited high breakdown voltages, instabilities due the high fields manifested, particularly in the form of the onset to conduction V_X. Field plates were introduced to reduce the effects of high fields by weakly accumulating charges near the interface between the gated and offset regions. Field plate structures and their affects on the electrical characteristics were numerically simulated and subsequently fabricated and measured. The following presents the electrical measurements and analysis of the vacuum-deposited pentacene OTFTs and HVOTFTs. Electrical measurements for all devices presented

Table 5.1: State-of-the-Art Pentacene OTFTs.

Substrate	Dielectric	μ (cm^2/ V·s)	Max V_{DS}	Flexi-ble?	Year	Refer-ence
Si	SiO_2	0.08	-100	No	2002	[139]
Si	SiN	0.4	-20	No	2003	[140]
Polyether-sulfone (PES)	PMMA/Al_2O_3	0.32	-25	Yes	2008	[141]
Si	Parylene-C	0.15	-25	No	2008	[142]
Polyether-sulfone (PES)	PVP/P(VDF-TrFE)	1.22	-20	Yes	2009	[143]
Poly-carbonate plastic	Organic Dielectric	0.6	-10	Yes	2014	[144]
Si	LaTiOn	2.6	NA	No	2017	[145]

in this dissertation were performed using an Agilent 4156C semiconductor parameter analyzer and a series of Keithley 237 source measure units for low- and high- voltage measurements, respectively, under air ambient and dark conditions.

5.1 State-of-the-Art Pentacene OTFTs

There have been several reports on pentacene OTFTs with varying degree of electrical performance. Of note, pentacene OTFTs have become equal or superior in mobility compared to the a-Si:H TFT used in display technology. However, outside of this work, there are no reported high-voltage thin film transistor architectures for pentacene, or organic semiconductors in general. Nonetheless, a summary of the state-of-the-art pentacene OTFTs for low-voltage applications have been tabulated in Table 5.1.

5.2 I-V Characteristics of Pentacene OTFTs

Prior to fabricating HVOTFTs with a dual channel architecture, low-voltage OTFTs were fabricated with varying dielectric materials, overlap channel structures and pentacene deposition conditions to optimize for its electrical properties, particular threshold voltage and mobility. The electrical measurements of low-voltage pentacene OTFTs and their electrical properties are presented below.

5.2.1 High-K vs. Low-K

A comparison between a high-k and low-k dielectric has been performed, namely between BZN (ϵ_r = 25-50) and parylene-C (ϵ_r = 3.15). Although parylene-C is an organic dielectric and would be compatible with an all-organic process, the high-k BZN was used to reduce the threshold voltage by increasing the amount of accumulated charge carriers in the organic semiconductor channel. Furthermore, the high-k allowed the deposition of a relatively thick dielectric layer to reduce the gate leakage current and the probability of tunneling processes such as Fowler-Nordheim, while maintaining the relatively low threshold voltage. The tunneling process through the dielectric scales exponentially with the inverse dielectric thickness. The output and transfer characteristics for parylene-C and BZN OTFTs are presented in Fig. 5-1 and Fig. 5-2, respectively. For the output characteristics, V_{DS} was typically swept from +10 V to -100 V at 2 to 5 V intervals for V_{GS} values between +10 V and -50 V at 5 to 10 V intervals. For the transfer characteristics, V_{GS} was typically swept from +20 V to -50 V at 1 to 2 V intervals for V_{DS} values in the linear or saturation regime of the transistor. A summary of the electrical properties of the pentacene OTFTs made with parylene-C, BZN and a dual stack of BZN/parylene-C is given in Table 5.2.

The electrical measurements showed, most notably, a decrease in threshold voltage with increasing dielectric constant. For similar dielectric thicknesses, pentacene OTFTs made with parylene-C had a threshold voltage of -26.95 V whereas BZN made devices had an average threshold voltage of -0.77 V. Utilizing a high-k dielectric proved crucial in achieving relatively high-speed and low-power consumption devices. The

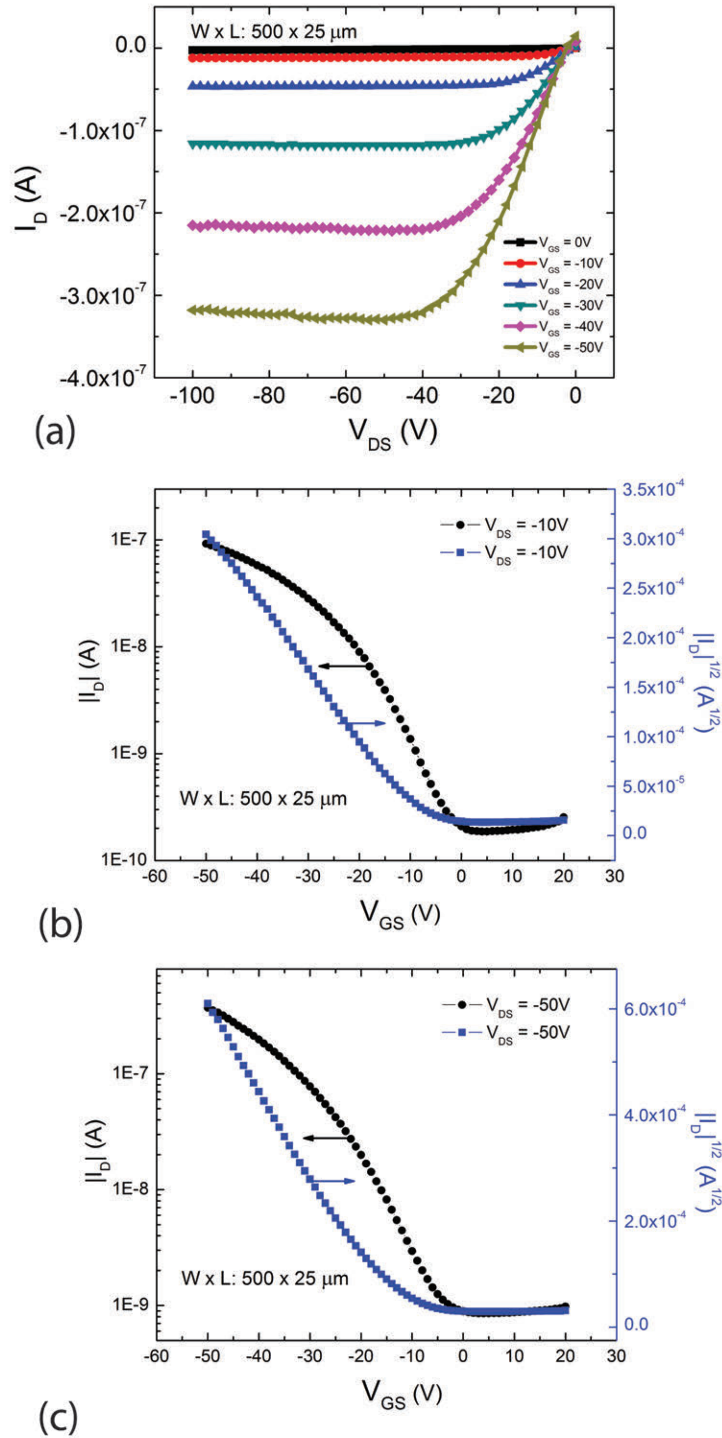


Figure 5-1: (a) Output, (b) linear transfer and (c) saturation transfer characteristics of OTFTs (W = 500 μm, L = 25 μm) made with pentacene and parylene-C (t_{ox} = 400 nm).

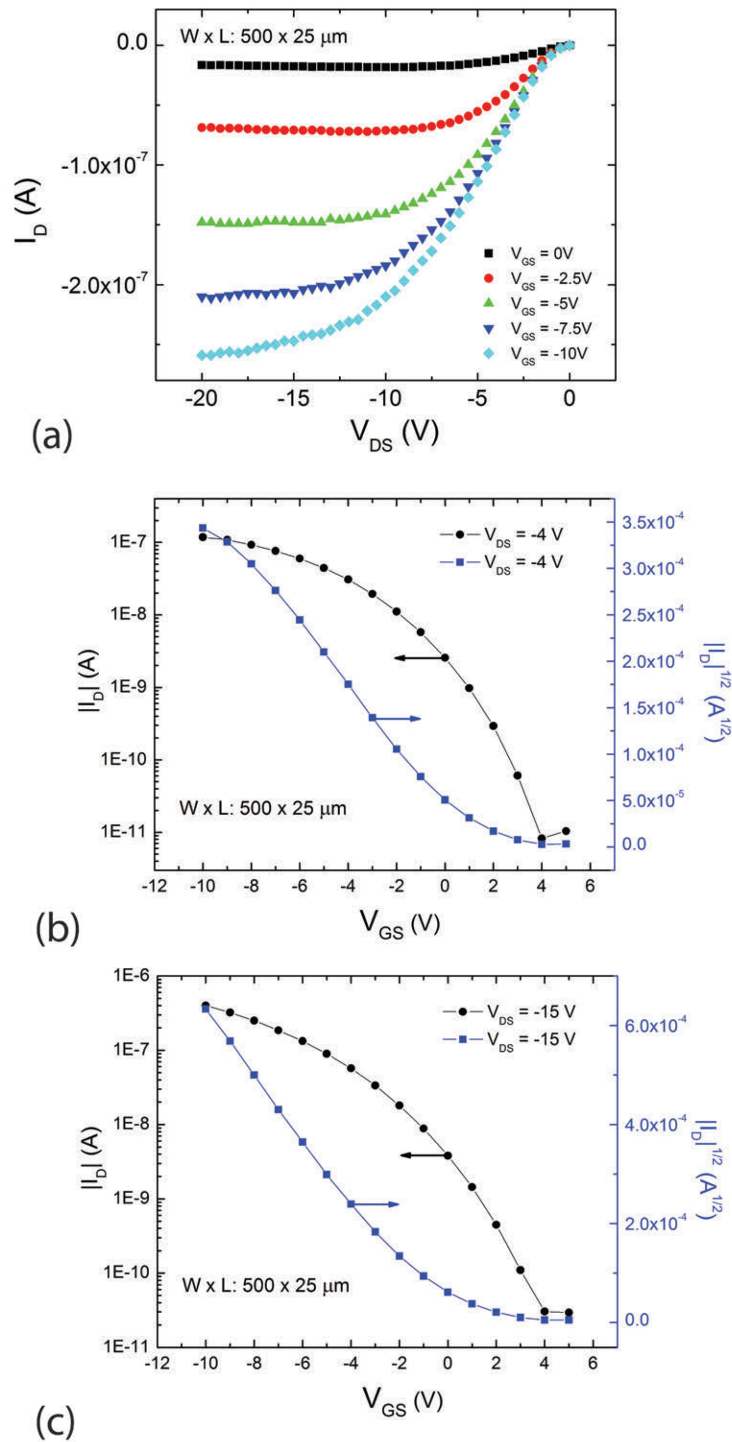


Figure 5-2: (a) Output, (b) linear transfer and (c) saturation transfer characteristics of OTFTs (W = 500 μm, L = 25 μm) made with pentacene and BZN (t_{ox} = 400 nm).

subthreshold swing was decreased from 9.19 V/dec to 1.58 V/dec going from parylene and BZN OTFTs, respectively. The point is driven further by analyzing the gate leakage current $I_{G,leak}$ versus V_{GS} at $V_{DS} = 0$, shown in Fig. 5-3. The $I_{G,leak}$ for pentacene OTFTs with parylene-C was found to be two orders of magnitude larger than that of pentacene OTFTs with BZN, at -2900 pA versus -20.5 pA, respectively. $I_{G,leak}$ through the gate is typically attributed to a tunneling process since potential barriers between the semiconductor and the dielectric prevent classical flow of charge carriers. When large negative voltages are applied between the gate contact and the semiconductor, charge accumulation occurs and the band diagram of the MOS structure is skewed in such a way a triangular barrier arises [146]. The tunneling through this triangular barrier is the Fowler-Nordheim tunneling process and is typically described as:

$$J_{FN} = \frac{q^3}{16\pi^2\hbar\phi_b}{F_{ox}}^2 exp\left(\frac{4}{3}\frac{\sqrt{2m_{ox}{}^*}{\phi_b}^{3/2}}{\hbar q}\frac{1}{F_{ox}}\right) \tag{5.1}$$

where q is the electron charge, $\hbar$ is Plank's reduced constant, ϕ_b is the semiconductor-oxide energy barrier height, F_{ox} is the electric field across the oxide and $m_{ox}{}^*$ is the electron effective mass in the dielectric. For thick dielectrics where the probability of tunneling is low, trap assisted tunneling may occur instead of Fowler-Nordheim [146]. Regardless, for a similar thickness, parylene-C was expected to have less tunneling due to its larger band gap and larger ϕ_b for holes (see Fig. 3-1). However, the pentacene OTFTs with parylene-C exhibited much larger $I_{G,leak}$ and is attributed to larger density of trap states within the dielectric or at the dielectric/semiconductor interface, indicating a poor quality of the insulator.

Mobility of the pentacene OTFTs with BZN were measured to be two orders of magnitude larger than those made with parylene-C. As the dielectric constant of the high-k BZN is larger than that of the low-k parylene-C by a factor of ∼10, additional charge carriers could be accumulated in BZN devices to fill trap states at the dielectric/semiconductor interface, resulting in increased mobility. However, it has been reported that using high-k dielectrics has a detrimental affect on mobility due to Coulombic and phonon scattering at the oxide/semiconductor interface arising

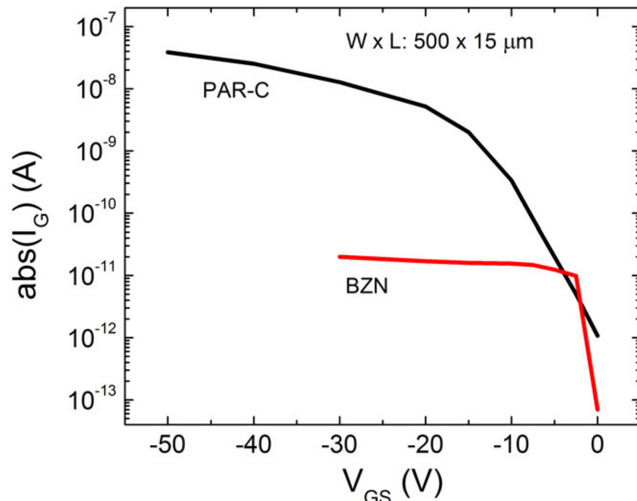


Figure 5-3: Gate leakage current through pentacene OTFTs (W = 500 μm, L = 15 μm) made with 400 nm of (a) parylene-C or (b) BZN.

from the large dipole moments native to high-k materials [109]. To prevent phonon scattering, a thin layer (2 nm) of parylene-C was deposited on top of the BZN to create a dual dielectric stack. The high-k BZN would allow for large charge carrier accumulation and prevent gate leakage current via its thickness while the low-k parylene-C was used to passivate the surface dipole moments of the BZN. The equivalent oxide thickness (EOT) of the BZN and BZN/Parylene-C dual stack are 39 and 41.5, respectively. Interestingly, the addition of the thin parylene-C layer reduced the mobility, increased the threshold voltage and reduced the current ratios. It was suggested that the quality of the parylene-C was suboptimal, introducing increased surface roughnesses or more trap states at the dielectric/semiconductor interface relative to the amount of suppressed phonon scattering from the high-k dipole moments, thus resulting in reduced mobility.

The current ratio I_{ON}/I_{OFF} for the pentacene OTFT with BZN is the largest of the three devices summarized in Table 5.2 by a factor of 20. This is attributed to the higher mobility and better quality dielectric used to control the charge carrier density in the organic semiconductor.

Table 5.2: Electrical properties for pentacene OTFTs made with different dielectrics.

Sample	I	II	III
Semiconductor	Pentacene	Pentacene	Pentacene
Structure	OTFT	OTFT	OTFT
No. of Devices Tested	30	50	20
Substrate	Glass	Glass	Glass
Dielectric	PAR-C	BZN	BZN/PAR-C
t_{ox} (nm)	400	400	400/2
ϵ_r	3.15	40	37.8
E_{OT} (nm)	495	39	41.5
C_{ox} (F/cm^2)	6.97e-9	8.85e-8	8.32e-8
Field-Plate	None	None	None
SAM	None	None	None
μ_{lin} (cm^2/V·s)	2.17e-3	1.47e-3	1.10e-3
μ_{sat} (cm^2/V·s)	4.15e-3	7.45e-3	6.20e-3
V_T (V)	-26.95	-0.77	-5.5
SS (V/dec)	9.19	1.58	1.32
I_{ON}/I_{OFF} (A/A)	1200	26000	11000
V_X (V)	-4.15	-1.42	-2.11
V_{BD} (V)	$<$ -100	$<$ -100	$<$ -100
$I_{G,leak}$ (A)	-2.90e-9	-2.05e-11	-2.70e-10
W (μm)	500	500	500
L (μm)	[5,8,10,15,20,25]	[5,8,10,15,20,25]	[5,8,10,15,20,25]
L_{offset}	0	0	0

Table 5.3: Electrical properties for pentacene OTFTs with BZN dielectric (W = 500 μ, L = 10 μm, t_{ox} = 400 nm) with varying overlap lengths L_{OL}.

Sample	I	II	III	IV
Semiconductor	Pentacene	Pentacene	Pentacene	Pentacene
Structure	OTFT	OTFT	OTFT	OTFT
No. of Devices Tested	10	10	10	10
L_{OL} (μm)	5	10	15	20
V_T (V)	-1.02	-0.74	-0.51	0.22
μ_{sat} ($cm^2/V\cdot s$)	0.0030	0.0035	0.0031	0.0030
V_X (V)	-1.62	-1.30	-1.17	-1.02
SS (V/dec)	1.35	1.66	1.32	1.50
$I_{G,leak}$ (A)	-1.1e-11	-1.4e-11	-2.9e-11	-1.3e-11

5.2.2 Structure Dependent Properties for Low-Voltage OTFTs

Transistor to transistor isolation is critical in obtaining well defined channels for reduced cross-talk and leakage current between devices. Shallow trench isolation and local oxidation of silicon is used in MOSFET architectures. However, in a TFT architecture, transistor to transistor isolation is achieved by defining and etching the active layer which may be designed to be of arbitrary size. Boundary effects along the semiconductor edge can lead to varied electrical properties such as reduced off currents. Here, the overlap length L_{OL} was defined as the distance between the drain/source edges and the edge of the patterned semiconductor, as indicated in Fig. 5-4. The gate metal was also scaled according to the overlap length. Pentacene OTFTs with BZN dielectric (400 nm) were made with various overlap lengths between 5 and 20 μm, relative to a 10 μm channel length. Their electrical properties are listed in Table 5.3. It was found that V_T became more positive, going from -1.02 to 0.22 V by increasing L_{OL} from 5 to 20 μm. This indicated an increased ability to accumulate charge relative to the length of the boundary. Depletion and enhancement mode transistors can thus be made by simply changing the overlap length. Other methods have been used to make depletion and enhancement mode transistors such as dielectric surface treatment for V_T modification [147].

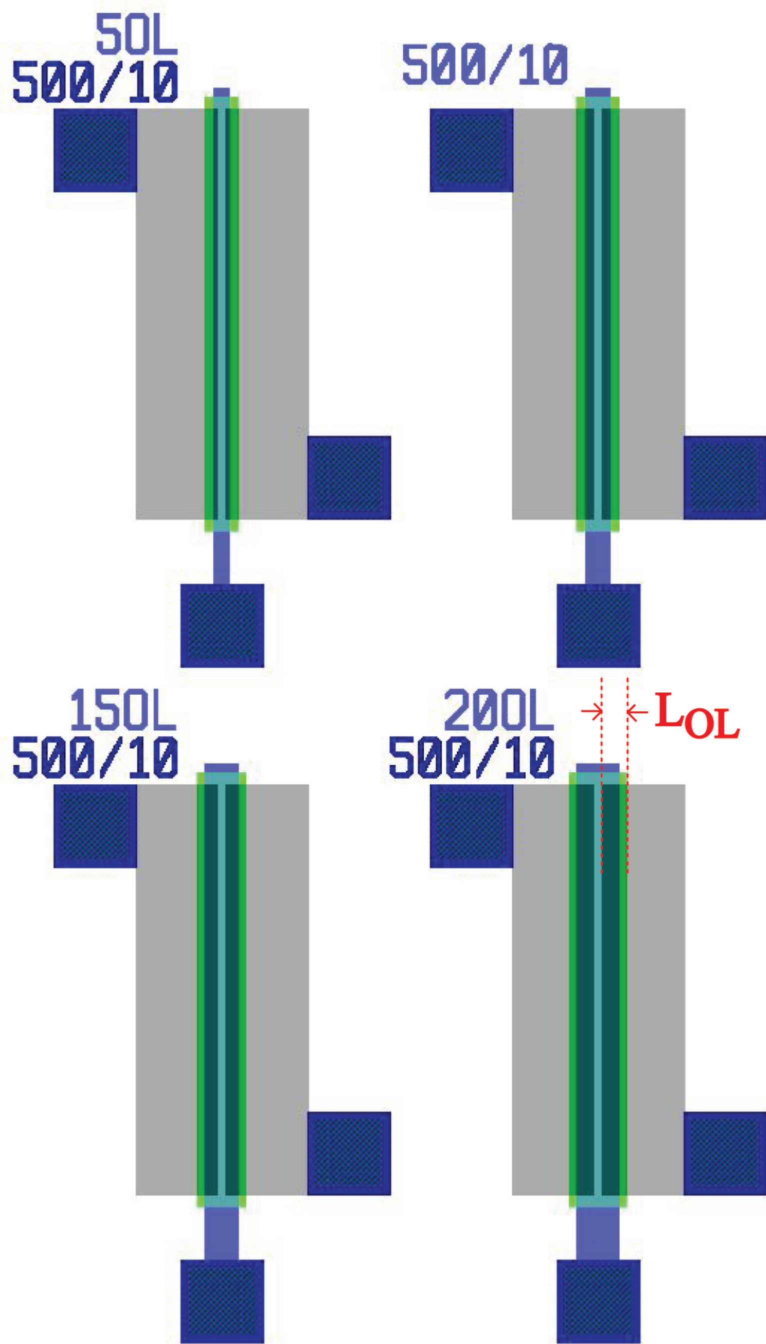


Figure 5-4: OTFTs with varying overlap lengths L_{OL}, involving the overlap of the semiconductor with the drain and source contact.

5.2.3 Pentacene Deposition Rate

The deposition rate of pentacene was also optimized to achieve the highest mobility for the OTFT. The deposition rate affected the nuclei density and grain size of pentacene, resulting in various mobilities. OTFTs with 400 nm of parylene-C dielectric were fabricated with pentacene deposited at various rates: 0.1, 1 and 10 Å/s. The electrical properties are summarized in Table 5.4 and the I-V characteristics are shown in Fig. 5-5. It was found that the linear and saturation mobility increased with increasing deposition rate, particularly when going from 0.1 to 1 Å/s, given a 40x mobility increase. However, this is in contrast with the nucleation theory (Eq. 3.1) which states an increase in nuclei density with increasing molecule flux, reducing the grain size and mobility. It is postulated that a further increase in deposition rate would eventually lead to an overload of incoming organic molecules which would then significantly increase the nuclei density and reduce mobility. However, at the current low deposition rates, local thermodynamic equilibrium was expected due to re-evaporation or decay energies being larger than that of nucleation energies [89]. This resulted in a zero net local growth of the organic semiconductor, preventing proper grain growth across the sample surface. A minimum condensation flux was required to promote diffusion and coalescence of pentacene molecules before desorption or re-evaporation. Although our in-house pentacene deposition tool was limited to a certain deposition rate, it was believed that further increasing the crucible temperature and the deposition rate beyond 10 Å would result in poor grain structure and a significant decrease in transistor mobility. A comparison of I_D vs. V_{DS} sweeps at V_{GS} = -50 V are given for the three deposition rates in Fig. 5-6.

Beyond mobility differences, an increase of the subthreshold swing was observed, going from 1.70 to 9.19 V/dec between 0.1 and 1 Å/s. The subthreshold swing is a function of interface states Q_{it}, as described by Eq. 2.55 and Eq. 2.56, which may arise from the large deposition rate damaging the dielectric surface. However, further interface state analysis is required.

Table 5.4: Electrical properties for pentacene OTFTs made with varying pentacene deposition rates.

Sample	I	II	III
Deposition Rate (Å/s)	0.1	1	10
Semiconductor	Pentacene	Pentacene	Pentacene
Structure	OTFT	OTFT	OTFT
No. of Devices Tested	10	10	10
Substrate	Glass	Glass	Glass
Dielectric	PAR-C	PAR-C	PAR-C
t_{ox} (nm)	400	400	400
ϵ_r	3.15	3.15	3.15
E_{OT} (nm)	495	495	495
C_{ox} (F/cm^2)	6.97e-9	6.97e-9	6.97e-9
Field-Plate	None	None	None
SAM	None	None	None
μ_{lin} (cm^2/V·s)	1.81e-5	2.17e-3	3.05e-3
μ_{sat} (cm^2/V·s)	7.43e-5	4.15e-3	8.48e-3
V_T (V)	-25.62	-26.95	-28.54
SS (V/dec)	1.73	9.19	15.98
I_{ON}/I_{OFF} (A/A)	1300	1200	3300
V_X (V)	-6.73	-4.15	-6.22
V_{BD} (V)	$<$ -100	$<$ -100	$<$ -100
W (μm)	500	500	500
L (μm)	[5,8,10,15,20,25]	[5,8,10,15,20,25]	[5,8,10,15,20,25]
L_{offset} (μm)	0	0	0

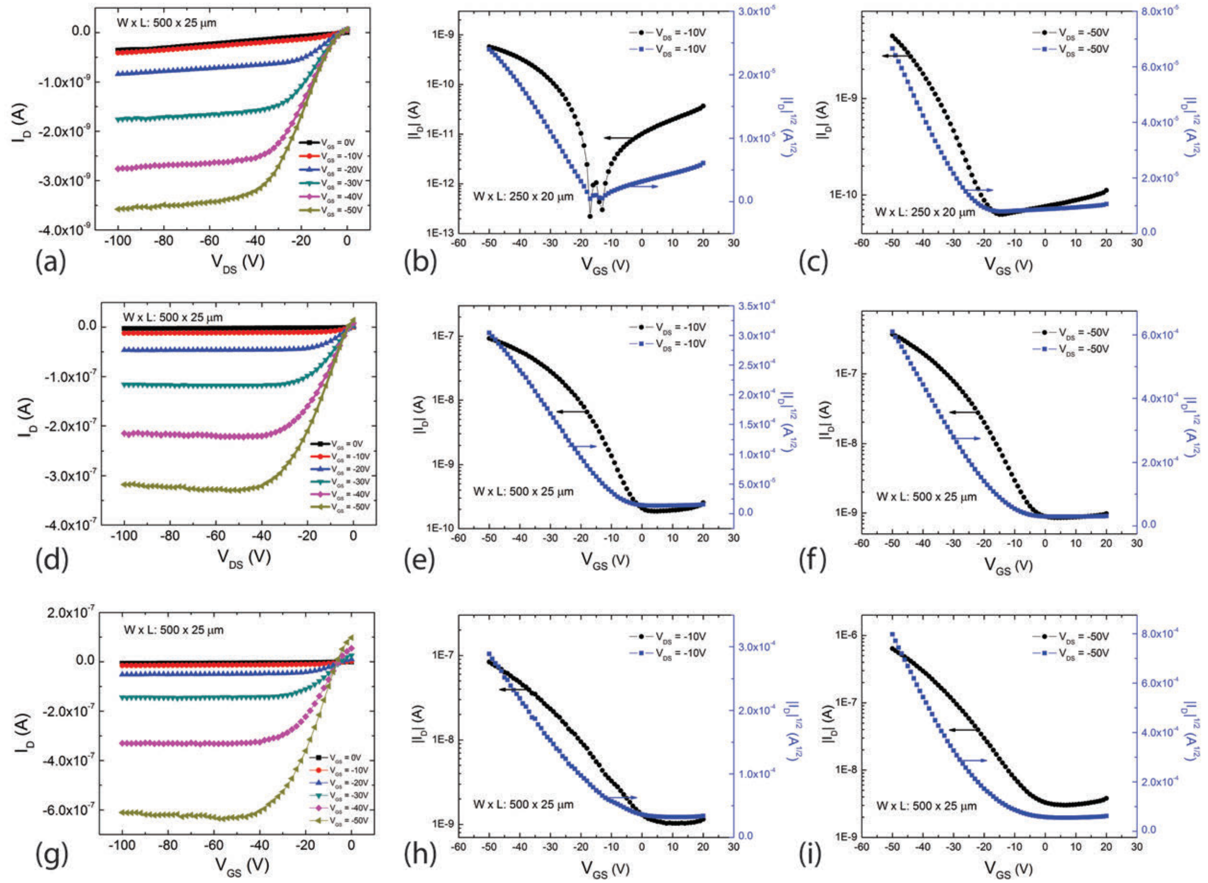


Figure 5-5: Output, linear transfer and saturation transfer characteristics of OTFTs (W = 500 μ, L = 25 μ) made with varying pentacene deposition rates. (a,b,c) 0.1 Å/s, (d,e,f) 1 Å/s and (g,h,i) 10 Å/s.

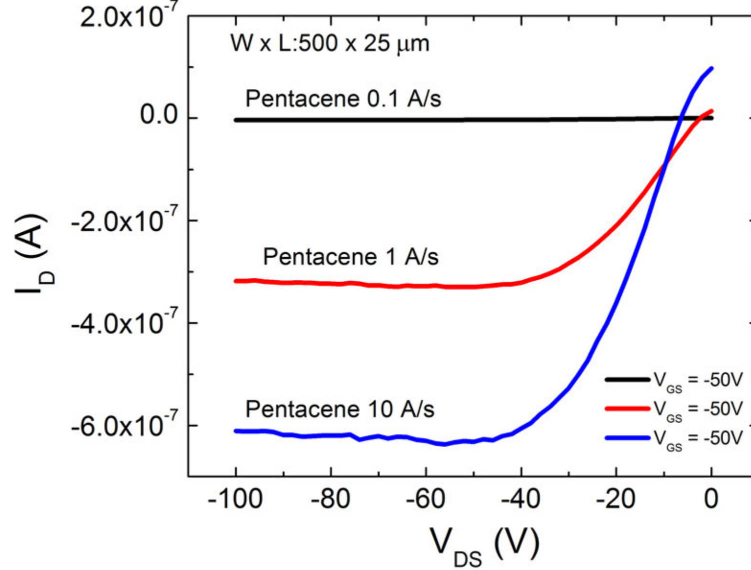


Figure 5-6: A comparison of output characteristics at V_{GS} = -50 V for different deposition rates.

5.3 I-V Characteristics of Pentacene HVOTFTs

Pentacene HVOTFTs were fabricated alongside the low voltage OTFTs described above. The HVOTFTs were uniquely characterized by an additional offset region between the source and drain contacts in which there is no overlap with the gate metal contact. As high-voltages ($<$ -100 V) were applied across the source and drain contacts, the majority of the voltage was dropped across the offset region.

The output and transfer characteristics of a pentacene HVOTFT with parylene-C dielectric is shown in Fig. 5-7. The first distinguishable electrical behavior in the output characteristics of the HVOTFTs was the ability to increase V_{DS} beyond the breakdown voltage of the OTFTs. The breakdown voltage increased from anywhere between -50 and -150 V to -350 to -550 V when adding an offset length of 10 to 30 μm, relative to a 5 to 30 μm gated region. This demonstrated the ability to increase the breakdown voltage or max allowable V_{DS} by dropping a large portion of the potential across the offset region. In fact, increasing the offset channel region length from 10 to 30 μm proved effective in increasing the breakdown voltage systematically from

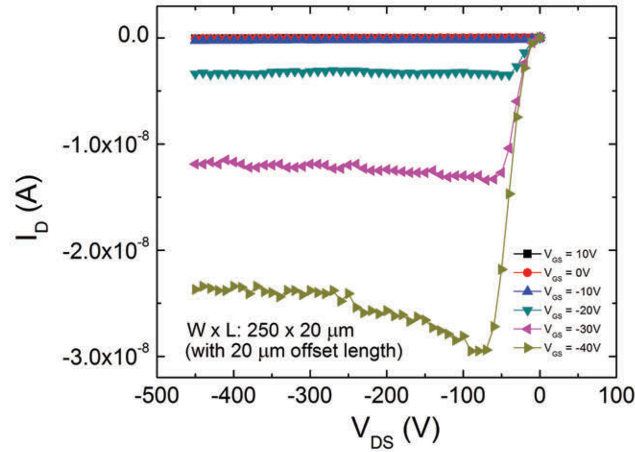
-350 to -550 V, shown in Fig. 5-10. A key point to the output characteristics of these HVOTFTs was the ability to control the channel using a relatively low V_{GS} compared to the large applied V_{DS}.

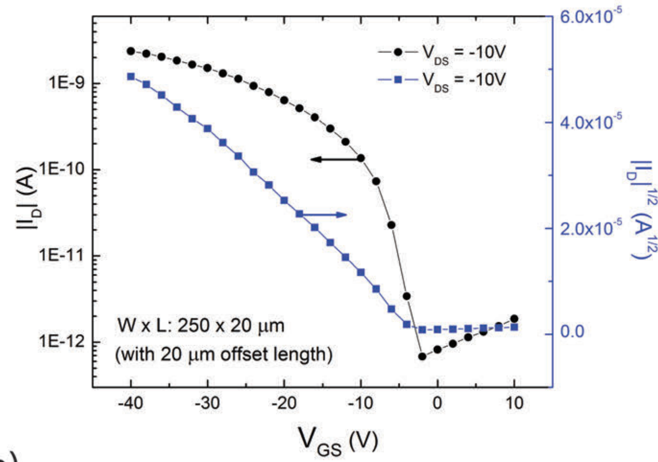
Overall, the mobility of the HVOTFTs compared to the OTFTs was 5 to 10x smaller ($\mu = 0.002$, 0.001 and 0.0003 $cm^2/V{\cdot}s$ for parylene-C, BZN and BZN/parylene-C HVOTFTs, respectively). This was attributed to the fact that the offset region acts as a limiting resistor and impeded carrier mobility as well as charge carrier injection throughout the channel.

Threshold voltages remained largely constant with the addition of the offset region, with a slight positive shift for pentacene HVOTFTs with BZN and a slight negative shift for pentacene HVOTFTs with parylene-C. Previous work has shown that O_2 plasma-treated parylene-C introduced interface traps (Q_{it}), positively shifting the threshold voltage [75]. The subthreshold swing also remained largely unaffected. However, the current ratios were improved 10x for BZN devices reaching 280,000 A/A while decreasing by 3x for parylene-C devices to 400 A/A. This was supported by the larger gate leakage current measured in the parylene-C OTFTs, as discussed in the previous section.

5.3.1 High-Field Effects

High-field effects were discussed in section 2.3.3 and related to the onset to conduction V_X and non-saturating I-V characteristics. V_X was found to become more negative with the addition of the offset channel region, with values between -10 and -30 V. Analysis on the origin of V_X was performed more thoroughly on TIPS-pentacene HVOTFTs described in chapter 6. It was found that V_X was directly related to the max V_{DS} applied during measurement. Furthermore, the majority of the pentacene HVOTFTs exhibited good saturating behavior; however, select devices did showed non-saturation I-V characteristics. As the majority of the devices tested on a single wafer were found to be saturating, slight processing variabilities may affect the electrical performance of the transistors across the sample.





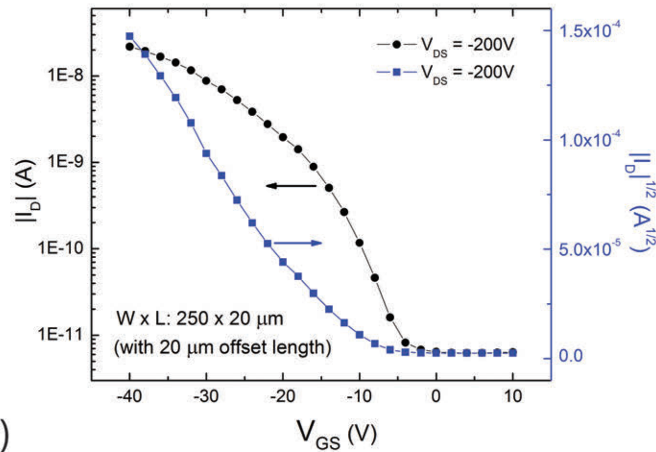


Figure 5-7: (a) Output, (b) linear transfer and (c) saturation transfer characteristics of HVOTFTs (W = 250 μm, L = 20 μm, L_{offset} = 20 μm) made with pentacene and parylene (t_{ox} = 400 nm).

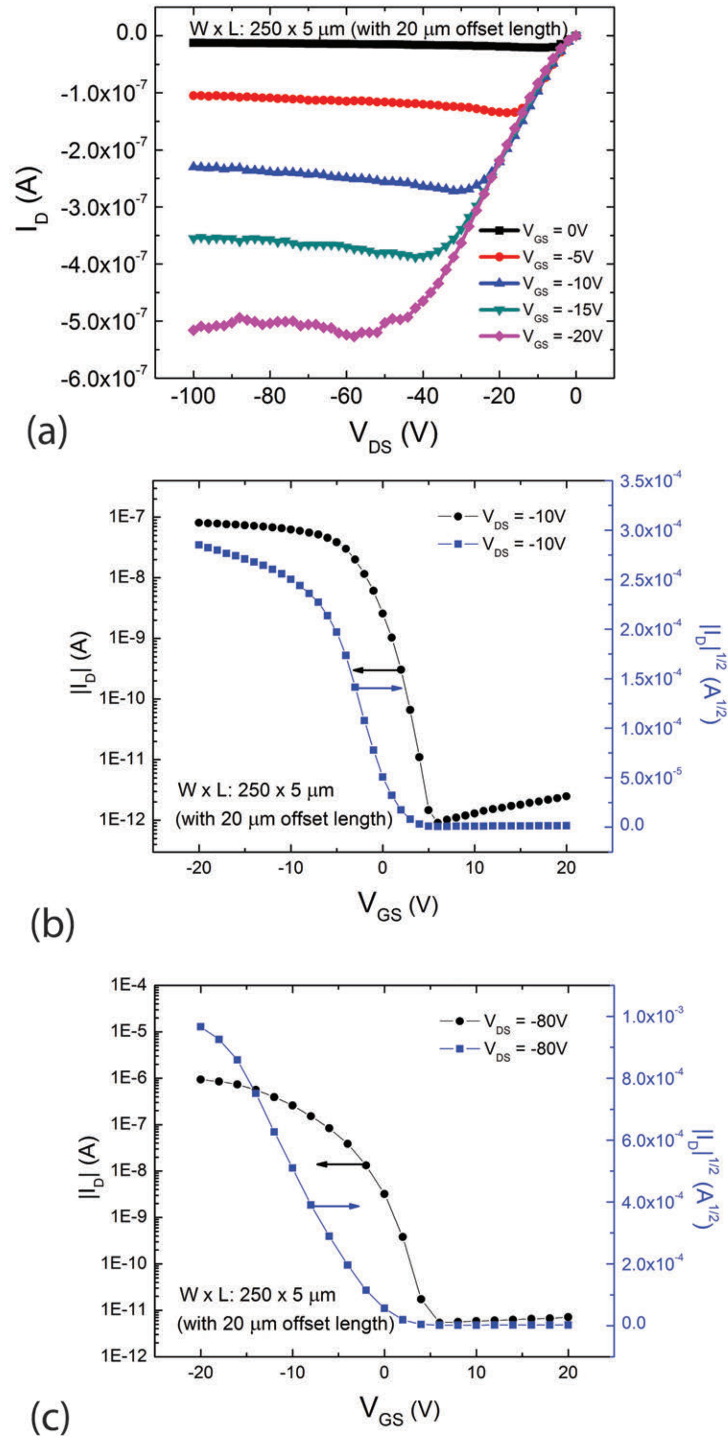


Figure 5-8: (a) Output, (b) linear transfer and (c) saturation transfer characteristics of HVOTFTs (W = 250 μm, L = 20 μm, L_{offset} = 20 μm) made with pentacene and BZN (t_{ox} = 400 nm).

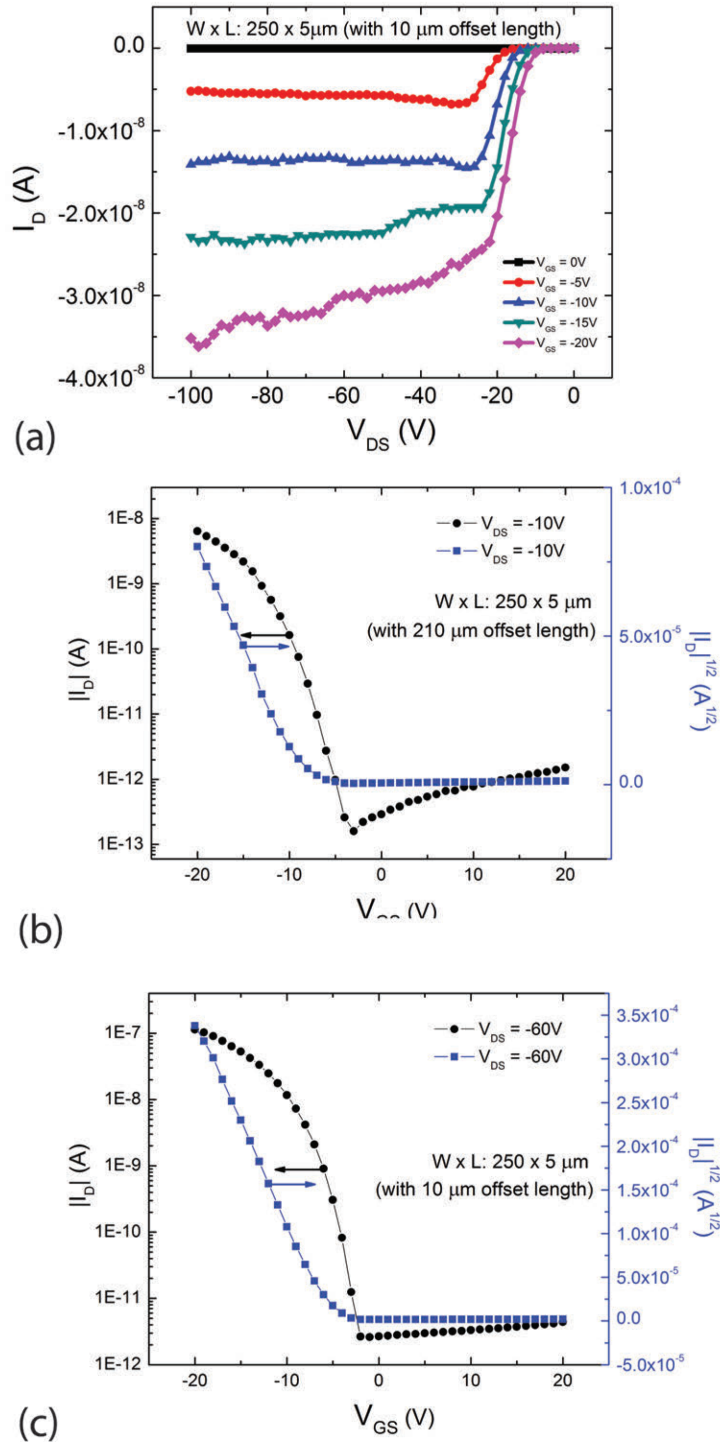


Figure 5-9: (a) Output, (b) linear transfer and (c) saturation transfer characteristics of HVOTFTs (W = 250 μm, L = 20 μm, L_{offset} = 20 μm) made with pentacene and a BZN/parylene-C dual stack dielectric (t_{ox} = 400+2 nm).

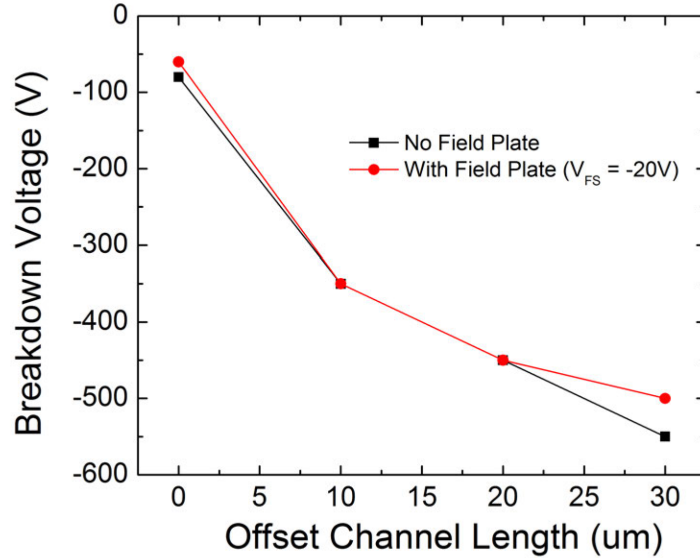


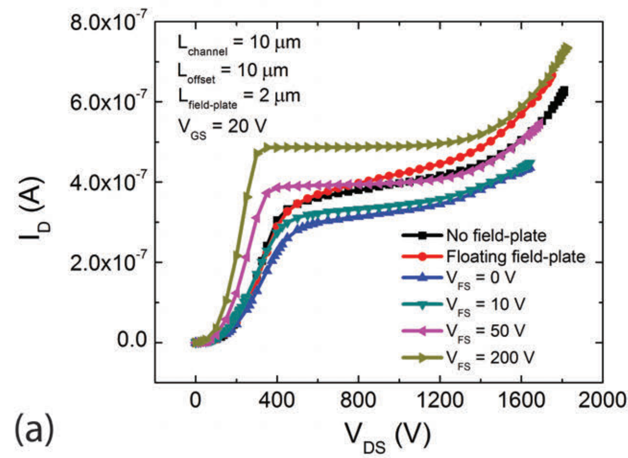
Figure 5-10: Breakdown voltage (or max allowable V_{DS}) of pentacene HVOTFTs (W = 250 μm with parylene-C dielectric (t_{ox} = 400 nm) as a function of the offset channel length. A top field plate was introduced in an attempt to control the charge distribution inside the channel to reduce the peak electric field.

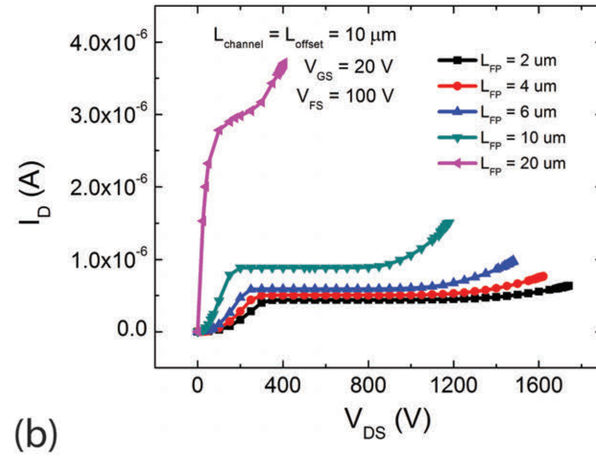
5.3.2 Field Plate Analysis

To control the electrostatics and the charge carrier distribution within the organic channel of the HVOTFT, a top field plate was placed on the parylene-C encapsulation layer, centered directly above the transition region between the gated and offset regions, as shown in Fig. 4-1 (a). Martin et al. demonstrated Si HVTFTs utilizing a field plate design, which improved the overall electrical behavior by weakly accumulating charge carriers at the field-transition region [57]. The weakly accumulated charges allowed the channel to respond to the large fringing fields, and avoided excess defect generation which would contribute to increasing V_X seen in HVTFTs. Furthermore, the field plate shortened L_{offset}, thus reducing the necessary voltage needed to achieve saturation current. Overall, the addition of a field plate increased I_D and lowered the onset to conduction V_X. Here, a field plate design for the HVOTFT with varying field plate bias (V_{FS}) and length (L_{FP}) was initially examined through 2D numerical simulations. The Atlas numerical solver from Silvaco was used to solve

the Poisson, carrier continuity and transport equations for space charge density and current density. Simulations were done for an n-type a-Si device with positive gate, drain and field plate biasing relative to the source. To relate to p-type organics, the polarity of all values should be inversed. Subsequently, field plated pentacene HVOTFTs were fabricated and measured.

2D numerical simulations of an a-Si HVTFT with dimensions listed in Table 5.5 were performed, examining the I-V characteristics and the electric field distribution across the channel. A 2 μm long field plate was biased at 0, 10, 50, and 200 V which was compared to a floating field plate and a non-existent field plate design. The output characteristics are shown in Fig. 5-11 (a). The first observation made was the increased drain current for $C_{ox,top}V_{FS} > C_{ox,bottom}V_{GS}$. As V_{FS} increased, additional free charges were accumulated into the channel, increasing the drain current. However, the opposite trend was observed for $C_{ox,top}V_{FS} < C_{ox,bottom}V_{GS}$. In this case, the field plate limited the charge accumulation at the interface between the gated and offset region, effectively reducing the drain current. Secondly, by increasing V_{FS}, the onset to conduction V_X as well as the slope of I_D versus V_{DS} in the linear regime were significantly reduced and increased, respectively, allowing the transistor to reach saturation at lower V_{DS} values. The field plate accumulated additional charge carriers at the interface between the gated and offset regions to respond to high stress induced trap states or to impeded carrier injection into the offset region. Initial simulations suggested that the field plate could reduce and smooth the electric field in both the x and y directions at the interface of the gated and offset regions. Additional electric field analysis is needed to assess whether or not this channel electric field modulation by field plate can reduce the generation of stress induced trap states. Thirdly, improved saturation characteristics was observed. As V_{FS} increased, the potential drop between the field plate and the drain contact became smaller, reducing the effects of channel length modulation. Finally, for a fixed L_{FP}, there does not appear to be any significant changes to the breakdown voltage when varying the field plate bias. The breakdown voltage remained a function of the dielectric strength, the dielectric thickness as well as the field plate size, as discussed below.





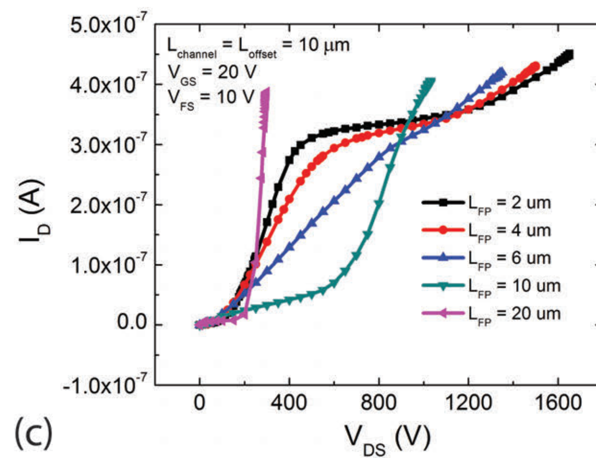


Figure 5-11: 2D simulation output characteristics of a field plated HVTFT (L = 10 μm, L_{offset} = 10 μm) for (a) varying V_{FS} at fixed V_{GS} and L_{FP}, (b) varying L_{FP} at fixed V_{GS} and high V_{FS}, and (c) varying L_{FP} at fixed V_{GS} and low V_{FS}.

Table 5.5: 2D simulation parameters used for field plated HVTFTs

Semiconductor	a-Si
Structure	HVTFT
Bottom Dielectric	SiO_2 (k = 3.9)
$t_{ox,bottom}$	400 nm
Top Dielectric	Polyimide (k = 4)
$t_{ox,top}$	1000 nm
Field Plate Length L_{FP} (μm)	[2, 4, 6, 10, 20]
L (μm)	10
L_{offset} (μm)	10

Variations in the field plate length L_{FP} were also investigated and proved critical in controlling the I_D, V_X and V_{BD}. Two schemes were found, one for $C_{ox,top}V_{FS}$ > $C_{ox,bottom}V_{GS}$, shown in Fig. 5-11 (b) and one for $C_{ox,top}V_{FS} < C_{OX,bottom}V_{GS}$, shown in Fig. 5-11 (c). For the former, as L_{FP} increased between 2 and 20 μm, the $I_{D,SAT}$ increased while V_X decreased. This is to be expected as larger field plates can perform additional accumulation over a larger area of the channel. The breakdown voltage, however, was no longer dominated by the dielectric breakdown of the bottom insulator, but that of the top insulator due to the closer proximity of the drain contact with the field plate. Thus, as the field plate became longer, V_{BD} decreased appropriately. On the other hand, for $C_{ox,top}V_{FS} < C_{ox,bottom}V_{GS}$, the field plate limited the charge accumulation at the interface region, effectively reducing the channel length. Furthermore, low V_{FS} brought parts of the channel below threshold, turning the transistor off. Thus, from an operational standpoint, $C_{ox,top}V_{FS}$ should be designed to be larger than $C_{ox,bottom}V_{GS}$. Moreover, large field plates should not be used to avoid premature breakdown of the top dielectric layer.

Field plated HVOTFTs were fabricated using parylene-C (200 nm) for both the bottom and top dielectric. An optical micrograph (top view) of a finished device is shown in Fig. 4-1 (b). The top field plate with L_{FP} of 5 to 20 μm was aligned to overlap the transition area between the offset and gated channel regions. Output characteristics for the HVOTFTs with field plates were initially measured with the

field plate floating, as seen in Fig. 5-12. The floating field plate did not appear to have any significant effect on the transistor behavior, comparable to those of transistors made without field plates. However, when the field plate was biased, the conductivity of the channel was primarily determined by V_{FS} and not V_{GS}. At a positive V_{FS}, the entire channel was turned off, regardless of the V_{GS}. At a negative V_{FS}, the conductivity of the channel could be controlled by V_{GS} up until the equivalent value of V_{FS}. Additional gate to source biasing beyond that of V_{FS} did not increase the current output. In other words, V_{FS} dictated the highest conductivity of the channel and acted as a current limiter. The effects of the field plate were also reversible in that returning the field plate back to a floating state or to any intermediate bias value brought back the original output characteristics of the transistor. The breakdown was also assessed for HVOTFTs with field plates. V_{FS} was held at -20 or -40 V while V_{GS} was varied between +10 and -40 V at -10 V intervals. V_{DS} was then swept from +10 to increasingly more negative values until breakdown occurred. When -40 V was applied to V_{FS}, the breakdown voltage was generally lower (more positive) by 100 to 200 V than those of HVOTFTs without field plates. With the field plate biased at -20 V, however, breakdown voltages were comparable. Samples after breakdown were observed under an optical microscope and it appeared that the origin of the breakdown occurred primarily along the edge of the field plate and the offset region. This suggested that dielectric breakdown occurred with the top dielectric, between the field plate and the drain contact. Other device designs and further understanding of the interplay between the gate and field plate threshold voltages are needed to help mitigate such electrical breakdown.

5.4 Summary

Low-voltage and high-voltage organic thin film transistors (OTFT and HVOTFT, respectively) have been fabricated with 20 nm of vacuum deposited pentacene. Two dielectrics were used: parylene-C, BZN, as well as a dual stack of BZN/parylene-C. The HVOTFTs exhibited very large breakdown voltages below -550 V with offset

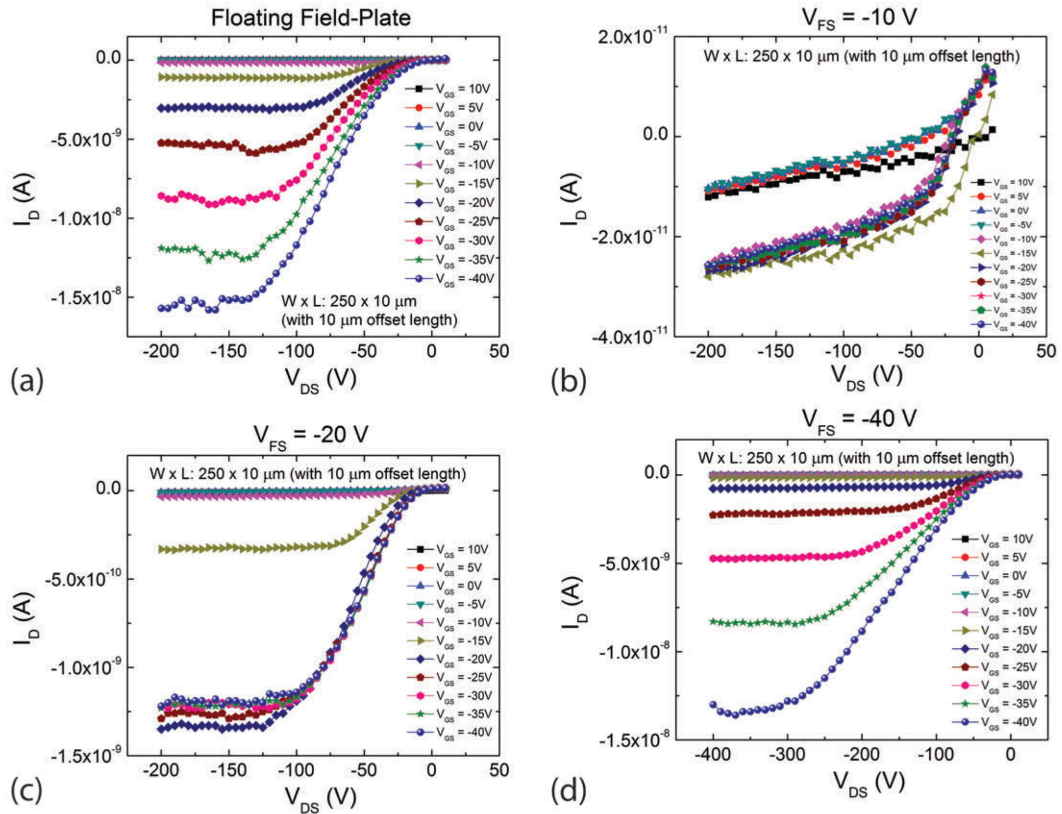


Figure 5-12: Output characteristics of a pentacene HVOTFT with a field plate (W = 250 μm, L = 20 μm, L_{offset} = 10 μm) made with 200 nm of parylene-C for both the bottom and top dielectric. The field plate was (a) Floating, or biased at (b) V_{FS} = -10 V, (c) V_{FS} = -20 V, and (d) V_{FS} = -40 V.

lengths of 30 μm relative to a 10 μm gated length. Thus, it was demonstrated that an organic TFT with an offset structure can drive large V_{DS} while being controlled by a relatively low V_{GS}, enabling future flexible MEMS integration. Below is a list of findings relating to the pentacene OTFT and HVOTFT.

Pentacene OTFTs

- Pentacene OTFTs have been successfully fabricated on glass substrates.
- High-k BZN and low-k parylene-C dielectrics have been integrated with the fabrication process.
- Significantly lower (more positive) threshold voltages were found for high-k BZN versus low-k parylene-C, critical for having a low V_{GS} operation.
- Mobility and I_{ON}/I_{OFF} current ratios for BZN devices were 2 and 1 orders of magnitude higher than those made with parylene-C, suggesting high trap densities in the organic dielectric.
- The gate current leakage $I_{G,leak}$ was found to be two orders of magnitude lower for BZN versus parylene-C made OTFTs.
- Although high-k dielectrics are reported to have Coulombic and phonon scattering at the oxide/semiconductor interface due to large surface dipole moments, the addition of a thin parylene-C layer on top of the BZN did not screen the dipole moments and did not improve the mobility. Additional surface roughness added by the extra parylene-C layer may degrade the OTFT performance.
- The overlap length L_{OL} (the overlap between the patterned semiconductor with the source/drain contacts) affected the electrical performance of the OTFT. Increasing the L_{OL} shifted the threshold voltage more positively. This allows for the fabrication of depletion and enhancement mode transistors.
- The deposition rate was optimized, and it was found that a faster deposition (at least up to 10 Å/s) led to increased mobility, at a detriment of subthreshold

swing. This was attributed to a minimum condensation flux required to promote diffusion and coalescence of the pentacene molecules before desorption or re-evaporation occurred.

Pentacene HVOTFTs

- Pentacene HVOTFTs have been successfully fabricated on glass substrates, and have exhibited breakdown voltage V_{BD} below -550 V.
- The breakdown voltage V_{BD} (the maximum allowable V_{DS} before dielectric breakdown occurred) can be engineered by increasing L_{offset}.
- Large I_{ON}/I_{OFF} current ratios were measured for HVOTFTs made with BZN versus parylene-C, indicating a high degree of control of a channel that is only partially gated.
- Minimal non-saturation effects were observed in the pentacene HVOTFTs, indicating minimal channel length modulation, self-heating effects and other short channel effects.
- Pentacene HVOTFTs with field plates were analyzed under 2D numerical simulations and were successfully fabricated.
- From the 2D numerical simulations, for $C_{ox,top}V_{FS} > C_{ox,bottom}V_{GS}$, field plated HVOTFTs exhibited increased drain current and improved onset to conduction V_X due to additional accumulated charges at the interface between the gated and offset regions. Furthermore, improved saturation characteristics were observed.
- From the 2D numerical simulations, for $C_{ox,top}V_{FS} < C_{ox,bottom}V_{GS}$, the field plate limited the charge accumulation at the interface between the gated and offset region
- From the 2D numerical simulations, for $C_{ox,top}V_{FS} > C_{ox,bottom}V_{GS}$, increasing the field plate size increased the drain current while decreasing V_X and V_{BD}.

- Fabricated HVOTFTs made with field plates behaved significantly different from simulations. When the field plate was biased, V_{FS} dictated the highest conductivity of the channel and acted as a current limiter. There was no observed improvements in drain current or onset to conduction V_X. Additional work on understanding the electric field distribution within the channel and the interplay between the gate and field plate threshold voltages are needed to help bridge the gap between simulations and measured devices.

Chapter 6

Solution-Processed TIPS-Pentacene High-Voltage Organic Thin Film Transistors

Solution-processed TIPS-pentacene HVOTFTs were successfully fabricated, as shown in Fig. 4-1 (c,d), demonstrating the ability to combine the key benefit of organic semiconductors (its ability to be solution-processed for large area electronics) with high-voltage operation. To the best of our knowledge, this is the first instance of a solution-processed HVOTFT that can drive high-voltage. In the previous chapter, pentacene HVOTFTs were initially fabricated due to the ease of the semiconductor thickness control during thermal evaporation. However, the issues with thermal evaporation are that, one, a high vacuum is needed to achieve uniform deposition and, two, the process does not lend itself to large area electronics. Therefore, a solution-processed organic semiconductor, namely TIPS-pentacene, was chosen to address these issues. Additionally, although the pentacene HVOTFTS exhibited high breakdown voltages, the mobilities were left to be desired. Improving crystallinity of the organic semiconductor film can promote charge hopping and charge transport efficiency between small molecules, thus increasing the mobility. Recently, solution-processed organic semiconductors such as TIPS-pentacene have seen large improvements in their mobility and have become an important focus of research [49].

The self-shearing drop casting method used to fabricated the TIPS-pentacene HV-OTFTs was integral in forming large and uniform crystal bands for high performing devices. The fabrication process was discussed in detail in chapter 4. It was expected that the thickness of the TIPS-pentacene layer would play a crucial role in controlling the on and off state resistances. Although wide crystal bands could be formed during self-shearing drop casting, the drop cast method resulted in a relatively thick TIPS-pentacene layer at the detriment of leakage current and breakdown voltage. To address this issue, SAMs were introduced in the solution-processed HVOTFT fabrication to not only improve charge carrier injection but to also reduce the sample surface energy. Reducing the sample surface energy promoted the quick shearing of the drop casted organic solution, resulting in the growth of thin TIPS-pentacene layers, as discussed in chapter 4. Notably, the breakdown voltage and the gate leakage current improved from -150 to -450 V and from ~-4.33e-8 to -2.20e-10 A/A, respectively, when the TIPS-pentacene layer was thinned from 0.5-3 μm to below 100 nm.

Due to the semi-random nature of the self-shearing drop casting method, the yield of working transistors was significantly reduced to about 50% of that made from the vacuum-deposited processes. The large variation in thickness and uniformity of the crystal bands as well as the random orientation of the quick shearing process for thin layers made it difficult to extract comparable electrical properties. Nonetheless, a series of working transistors with crystal grains covering the channel was fabricated and measured, shown in Fig. 4-4 and 4-5. Finally, the reliability of the HVOTFT was assessed under large biases, particularly relating to the onset to conduction V_X.

6.1 State-of-the-Art TIPS-pentacene OTFTs

To the best of our knowledge, this is the first reported TIPS-pentacene HVOTFT capable of driving voltages up to -450 V across its source and drain contacts. As a frame of reference, a summary on the state-of-the-art low-voltage TIPS-pentacene OTFTs is given in Table 6.1.

Table 6.1: State-of-the-Art TIPS-Pentacene OTFTs.

Substrate	Deposition	Solvent	μ (cm^2 / V·s)	Max V_{DS} reported	Flexible?	Properties	Year	Reference
SiO_2	Drop cast	Toluene	0.65	-40	No		2007	[148]
HMDS treated Si	Ink-jet-printed	Chlorobenzene	0.12	-40	No	Marangoni flow	2008	[54]
Polyethersulphone (PES)	Drop cast	Tetralin	0.0208	-40	Yes	PVP organic die-lectric	2008	[149]
Si	Spin coating	Toluene	0.0725	-40	No	CYTOP dielectric	2011	[55]
ITO	not reported	not reported	0.22	-20	No	Spin coated polymer dielectric	2012	[150]
Mylar	Self-shearing drop casting	Acetone	0.15	-60	Yes	Bending radius 0.1 mm	2012	[151]
Not reported	Drop cast	Anisole	0.73	-15	No	Solvent additives and PVP dielectric	2013	[129]
Si/SiO_2	Marangoni	Toluene and carbon tetrachloride	0.7	-80	No	Marangoni	2015	[96]

6.2 I-V Characteristics of TIPS-Pentacene OTFTs and HVOTFTs

The electrical measurements of TIPS-pentacene OTFTs and HVOTFTS and their electrical properties are presented below. TIPS-pentacene was drop casted using a 2 wt% anisole solution onto a slanted (4.5°) and heated (50 °C) sample. The initial thickness of the TIPS-pentacene layers presented below varied between 0.5 and 3 μm.

6.2.1 TIPS-Pentacene OTFTs: SAM Treatment for Improved Charge Injection

As discussed in section 3.6, SAMs can be used to improve the charge carrier injection from the metal contacts to the organic semiconductor by effectively increasing the metal work function. Au has a work function of $\phi_{Au} = 4.6$ eV while TIPS-pentacene has a HOMO level of $\phi_{HOMO} = 5.3$ eV, resulting in a hole injection barrier of 0.7 eV [16], [36]. A series of TIPS-pentacene OTFTs with 400 nm of BZN and 2 nm of parylene-C were fabricated with varying SAM treatments of the Au metal: no SAM, 1H,1H,2H,2H-perfluorodecanethiol (PFDT), 4-fluorothiophenol (4-FTP) and thiophenol (TP). Bottom gate / bottom contact samples were submerged in SAM/ethanol solutions (0.1 vol%) for 2 hours, followed by a toluene and DI water rinse. TIPS-pentacene was then drop casted to complete the device.

As the fluorinated organothiol SAMs have an opposite directed dipole moment (from tail to head) compared to the non fluorinated thiophenol (from head to tail), it was expected that the thiophenol would decrease the Au work function, effectively increasing the hole injection barrier. The effects of the SAMs were observed by measuring the output characteristics of the devices and comparing them to those of a non-treated sample, as shown in Fig. 6-1. The individual output and saturation transfer I-V characteristics for all four devices are given in Fig. 6-2, with their electrical properties summarized in Table 6.2.

In general, the OTFTs had better behaved I-V characteristics for PFDT and 4-

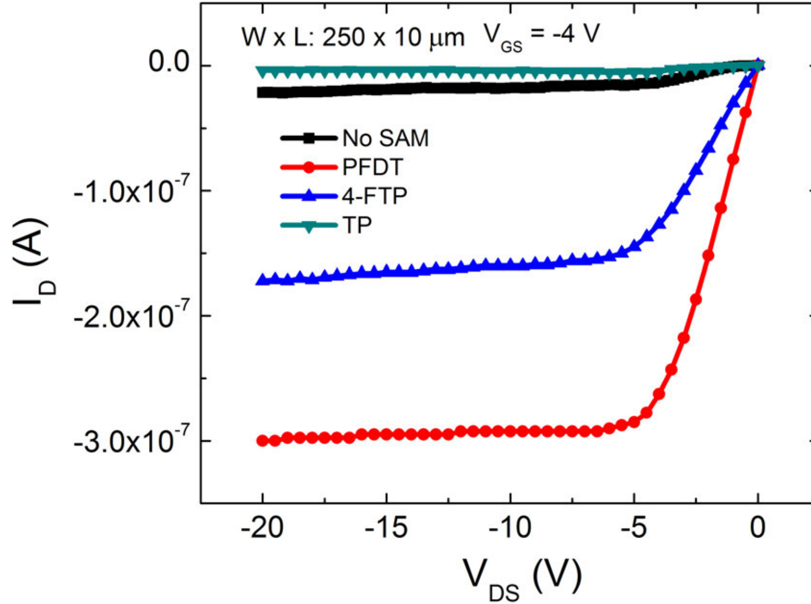


Figure 6-1: Comparison of the output I-V characteristics (at V_{GS} = -4 V) of TIPS-pentacene OTFTs (W = 250 μm, L = 10 μm) with various SAM treatments.

FTP treated samples, and worse for those treated with TP. Mainly, there was an increased output current and saturation mobility for OTFTs made with PFDT and 4-FTP compared to non-treated samples. Particularly, PFDT samples showed an increase of mobility by a factor of ~4, going from 0.005 $cm^2/V{\cdot}s$ for non-treated samples to 0.018 $cm^2/V{\cdot}s$. The higher mobility was attributed to more carrier injection due to an increased work function of the PFDT treated Au by 0.9 eV, resulting in additional filling of trap states at the dielectric/semiconductor interface and hence less scattering for the rest of the carriers [36]. 4-FTP samples also showed a slight increase in mobility up to 0.008 $cm^2/V{\cdot}s$. TP treated samples, on the other hand, exhibited a significant decrease in current output, with its mobility falling to 0.0016 $cm^2/V{\cdot}s$. This was in agreement with the charge injection barrier model. Additionally, improved I_{ON}/I_{OFF} current ratios by a factor of 5x was measured in the PFDT and 4-FTP treated samples relative too the non treated samples.

Table 6.2: Electrical properties for TIPS-pentacene OTFTs made with different SAM treatments.

Sample	I	II	III	IV
Semi-conductor	TIPS-pen	TIPS-pen	TIPS-pen	TIPS-pen
Structure	OTFT	OTFT	OTFT	OTFT
No. of Devices Tested	10	10	10	10
Substrate	Glass	Glass	Glass	Glass
Dielectric	BZN/PAR-C	BZN/PAR-C	BZN/PAR-C	BZN/PAR-C
t_{ox} (nm)	400/2	400/2	400/2	400/2
ϵ_r	37.8	37.8	37.8	37.8
E_{OT} (nm)	41.5	41.5	41.5	41.5
C_{ox} (F/cm^2)	8.32e-8	8.32e-8	8.32e-8	8.32e-8
Field-Plate	None	None	None	None
SAM	None	PFDT	4-FTP	TP
μ_{lin} (cm^2/V·s)	2.30e-3	1.20e-2	4.08e-3	4.80e-4
μ_{sat} (cm^2/V·s)	5.00e-3	1.83e-2	8.00e-3	1.62e-3
V_T (V)	1.29	-1.90	-1.62	-4.68
SS (V/dec)	0.33	0.76	0.76	2.17
I_{ON}/I_{OFF} (A/A)	200	1100	1050	300
V_X (V)	-0.22	-0.60	-3.28	-1.69
V_{BD} (V)	$<$ -50	$<$ -50	$<$ -50	$<$ -50
$I_{G,leak}$ (A)	-1.06e-7	-2..00e-8	-2.00e-8	-2.20e-9
W (μm)	[250, 500]	[250, 500]	[250, 500]	[250, 500]
L (μm)	[5, 8, 10, 15, 20]	[5, 8, 10, 15, 20]	[5, 8, 10, 15, 20]	[5, 8, 10, 15, 20]
L_{offset}	0	0	0	0

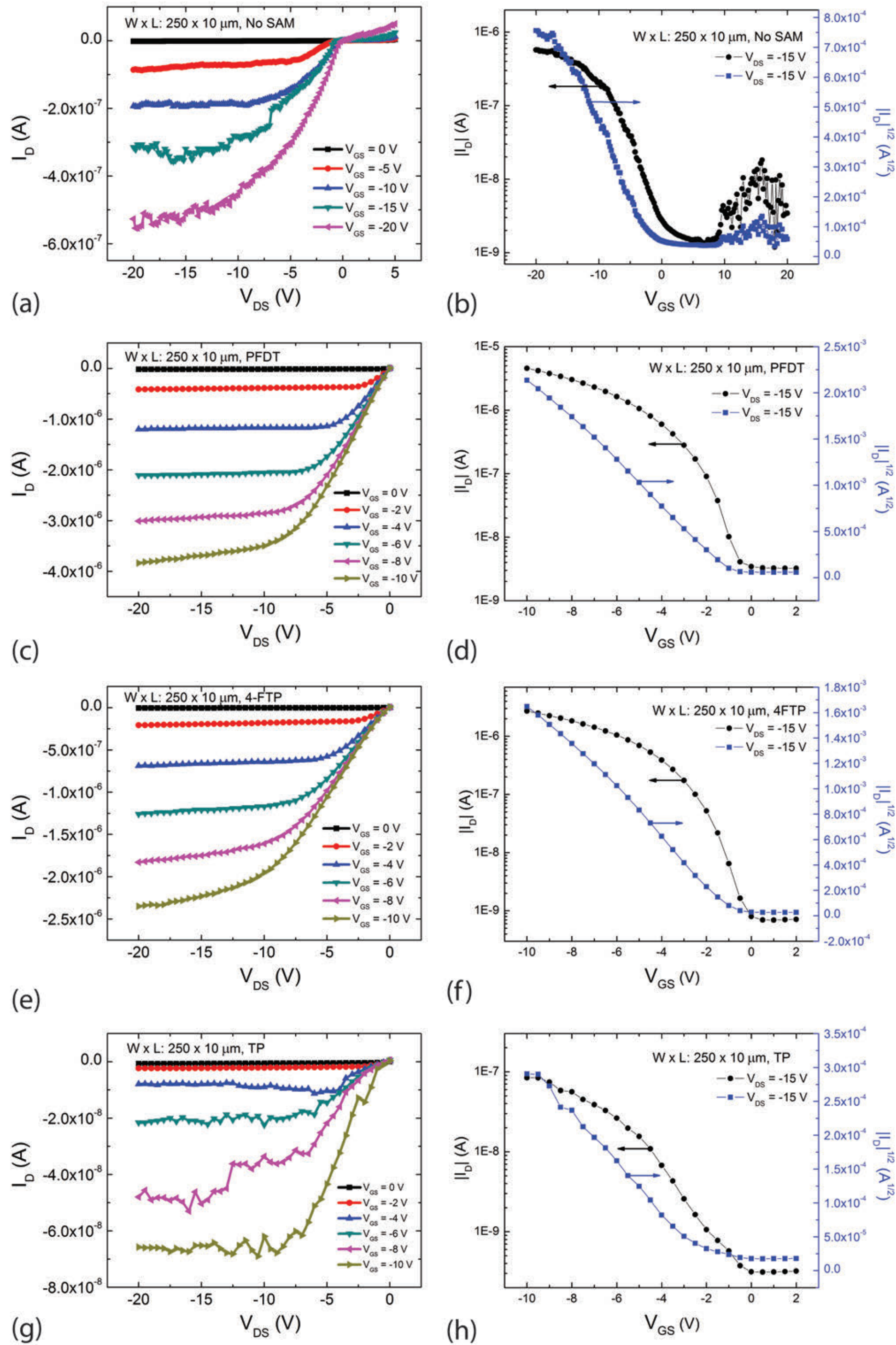


Figure 6-2: Output and saturation transfer I-V characteristics of TIPS-pentacene OTFTs (W = 250 μm, L = 10 μm) with (a,b) no SAM treatment, (c,d) PFDT SAM treatment, (e,f) 4-FTP SAM treatment, and (g,h) TP SAM treatment.

6.2.2 TIPS-Pentacene HVOTFTs

Thick TIPS-pentacene (0.5-3 μm) HVOTFTs with no SAM treatment were fabricated and are compared to TIPS-pentacene OTFTs, with their electrical properties summarized in table 6.3. The I-V characteristics of the TIPS-pentacene HVOTFT are presented in Fig. 6-3. Similar to the case for pentacene HVOTFTs, the breakdown voltage was initially increased from approximately -50 to -150 V when adding an offset length of 10 to 30 μm, relative to a 5 to 30 μm gated length. Increased breakdown voltage was once again attributed to the decreasing electric field seen by the dielectric when the drain was further offset from the gate, delaying dielectric breakdown. This was believed to be the first instance of a high-voltage operation in a TIPS-pentacene HVOTFT. The ability to fabricate HVOTFTs with solution-processes will enable novel high-voltage applications for large area electronics. Furthermore, mobility and I_{ON}/I_{OFF} decreased slightly while S increased, similar to that of pentacene HVOTFTs. The onset to conduction V_X also shifted from -0.22 to -12.10 V.

6.2.3 TIPS-Pentacene vs. Pentacene HVOTFTs

Another reason for incorporating TIPS-pentacene as opposed to pentacene in an HVOTFT was to have a poly-crystalline versus amorphous structure, promoting charge hopping between the organic molecules [49], [148]. It was expected that TIPS-pentacene transistors would have a higher mobility compared to pentacene. TIPS-pentacene OTFTs, without a SAM treatment, were measured to have a saturation mobility of 0.0050 $cm^2/V{\cdot}s$ compared to 0.0062 $cm^2/V{\cdot}s$ for pentacene OTFTs. Although more crystalline, variations in crystal growth resulted in various grain boundaries to grow over the channel region, making such comparisons difficult in practice. However, TIPS-pentacene HVOTFTs, with a saturation mobility of 0.00540 $cm^2/V{\cdot}s$ was found to be an order of magnitude larger than that of pentacene HVOTFTs with 0.00031 $cm^2/V{\cdot}s$. The V_T, V_X and S were comparable between the two organic semiconductors.

The biggest difference between the TIPS-pentacene and the pentacene HVOTFTs

Table 6.3: Electrical properties of thick and thin TIPS-pentacene OTFTs and HV-OTFTs.

Sample	I	II	III	IV
Semi- conductor thickness (μm)	0.5 - 3	0.5 - 3	$<$ 0.1	$<$ 0.1
Semi- conductor	TIPS-pen	TIPS-pen	TIPS-pen	TIPS-pen
Structure	OTFT	HVOTFT	OTFT	HVOTFT
No. of Devices Tested	10	10	10	10
Substrate	Glass	Glass	Glass	Glass
Dielectric	BZN/PAR-C	BZN/PAR-C	BZN	BZN
t_{ox} (nm)	400/2	400/2	1000	1000
ϵ_r	37.8	37.8	25	25
E_{OT} (nm)	41.5	41.5	156	156
C_{ox} (F/cm^2)	8.32e-8	8.32e-8	2.21e-8	2.21e-8
Field-Plate	None	None	None	None
SAM	None	None	PFDTES	PFDTES
μ_{lin} (cm^2/V·s)	2.30e-3	3.05e-4	3.10e-4	9.32e-5
μ_{sat} (cm^2/V·s)	5.00e-3	5.35e-3	4.14e-4	8.25e-3
V_T (V)	1.29	2.70	-0.88	-0.37
SS (V/dec)	0.33	1.79	0.38	1.76
I_{ON}/I_{OFF} (A/A)	200	40	2050	250
V_X (V)	-0.22	-12.10	2.70	-11.40
V_{BD} (V)	$<$ -50	$<$ -150	$<$ -100	$<$ -450 V
$I_{G,leak}$ (A)	-1.06e-7	-4.33e-8	-7.30e-11	-2.20e-10
W (μm)	[250, 500]	250	[100, 250, 500, 1500]	250
L (μm)	[5, 8, 10, 15, 20]	[5, 8, 10]	[5, 8, 10]	[10, 20]
L_{offset}	0	[10, 20]	0	[5, 10, 20, 30]

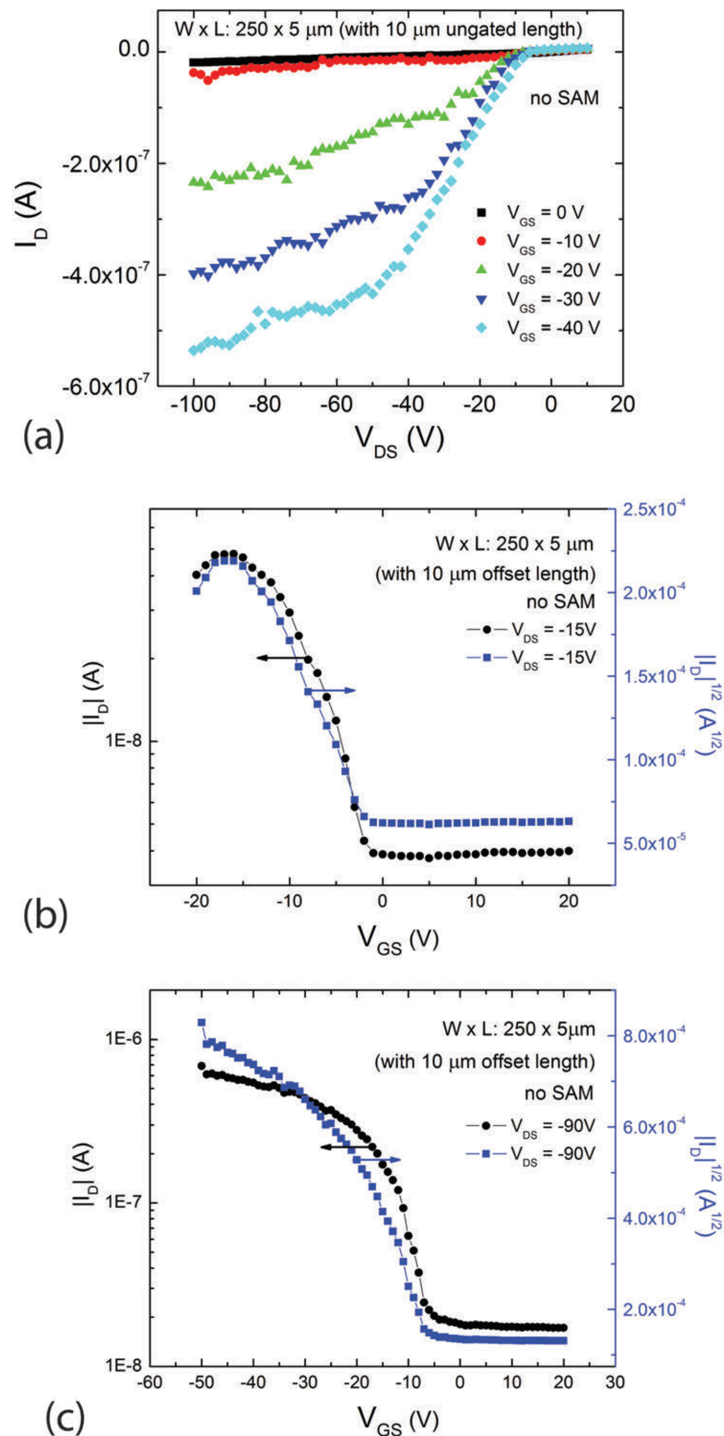


Figure 6-3: (a) Output, (b) linear transfer and (c) saturation transfer I-V characteristics of a TIPS-pentacene HVOTFT (W = 250 μm, L = 5 μm, L_{offset} = 10 μm) with no SAM treatment.

was manifested in the I_{ON}/I_{OFF} current ratios. For TIPS-pentacene compared to pentacene, I_{ON}/I_{OFF} were 1 and 4 orders of magnitude smaller for the OTFT and HVOTFT, respectively. These results can be explained by the differences in their device designs. There is a lack of transistor to transistor isolation as well as a non-uniform and thick (0.5-3 μm) semiconductor channel for TIPS-pentacene devices. Furthermore, multiple overlapping crystal grains were usually grown over the channel region, creating various line defects. Without proper definition of the semiconductor channel, the devices were susceptible to large leakage currents in the bulk of the organic semiconductor. It was believed that if there was transistor to transistor isolation as well as thin TIPS-pentacene layers (below 100 nm), improved I_{ON}/I_{OFF} current ratios and breakdown voltages can be obtained.

6.3 Thin TIPS-Pentacene on Low Surface Energy

Although large and preferentially directed crystal grains can be achieved by using the self-shearing drop casting method described in chapter 4, the organic semiconductor layers were too thick (0.5 to 3 μm) to have a well defined channel. It has been suggested that charge accumulation at the organic/dielectric interface only occurs within the first few monolayers of the organic layer [152]–[156]. Thus, any additional layers above the accumulation layer was not well controlled by the gate and can be injected with charges from a large V_{DS}, which increased the off state currents.

The I_{ON}/I_{OFF} current ratio can be significantly improved with thinner channels and is approximated by:

$$\frac{I_{ON}}{I_{OFF}} = 1 + \frac{\mu \cdot C_{ox} \cdot V_{DS}}{2\sigma_n \cdot bulk \cdot t} \tag{6.1}$$

where t is the film thickness, μ is the mobility, $\sigma_n bulk$ is the conductivity of the film and C_{ox} is the dielectric capacitance [157]. To reduce the thickness of the TIPS-pentacene layer, 1H,1H,2H,2H-perfluorodecyltriethoxysilane (PFDTES), an organosilane SAM, was used to coat the surface of the sample, via a desiccator for 12 hours, prior to drop casting. The surface energy of a PFDTES was reported to be 18.1 mN/m, significantly lower than that of the anisole used as the solvent for the organic

solution (35 mN/m). The idea was to reduce the surface energy of the sample such that the drop casted organic solution would self-sheer quicker across a larger area of the surface due to a dewetting surface environment. The quicker self-sheering would result in thinner amounts of TIPS-pentacene crystals. Although PFDTES does not bond with Au, it does make covalent bonds with an oxide surface, namely BZN, which was reported to have a surface energy of 43 mN/m [158]. A set of TIPS-pentacene HVOTFT samples (diced into 1 inch^2 samples) were prepared with 400 nm of BZN. From the point of view of the organic solution, the average surface energy of the sample (between the Au metal and the PFDTES coated BZN) was significantly lower than the original samples, which resulted in a quicker shearing process.

The growth of the TIPS-pentacene over the PFDTES coated sample resulted in a quick self-shearing growth process in the upper half of the slanted samples and a quasi-equilibrium nucleation growth process in the bottom half of the slanted sample. The TIPS-pentacene crystal bands are shown in Fig. 6-4. Although the bottom half TIPS-pentacene grew to be quite thick ($\sim$ 1 μm), the upper half TIPS-pentacene had a thickness of $\sim$ 100 nm. It is noted, however, that there was a lack of crystal growth uniformity in the upper half. The quick self-shearing from individual droplets led to randomly directed shearing, resulting in crystal bands that did not fully cover the surface. Nonetheless, OTFTs and HVOTFTs were fabricated with thin TIPS-pentacene layers, as shown in Fig. 6-5.

Resulting thin TIPS-pentacene OTFTs and HVOTFTs can be seen in Fig. 6-5 with their respective I-V characteristics shown in Fig. 6-6. Their electrical properties are summarized in Table 6.3. For thin TIPS-pentacene, the I-V characteristics are well behaved, with saturating currents being more prominent. With less material above the accumulation layers at the dielectric/organic interface, the gate has more control over the channel region. Although μ, V_T, V_X and S are comparable between thin and thick TIPS-pentacene transistors, the breakdown voltages significantly improved, reaching beyond -150 and -450 V for the OTFT and HVOTFT, respectively. Moreover, the I_{ON}/I_{OFF} current ratios and leakage currents improved by 1 and 3 orders of magnitude, respectively. This showed how important it was to control the

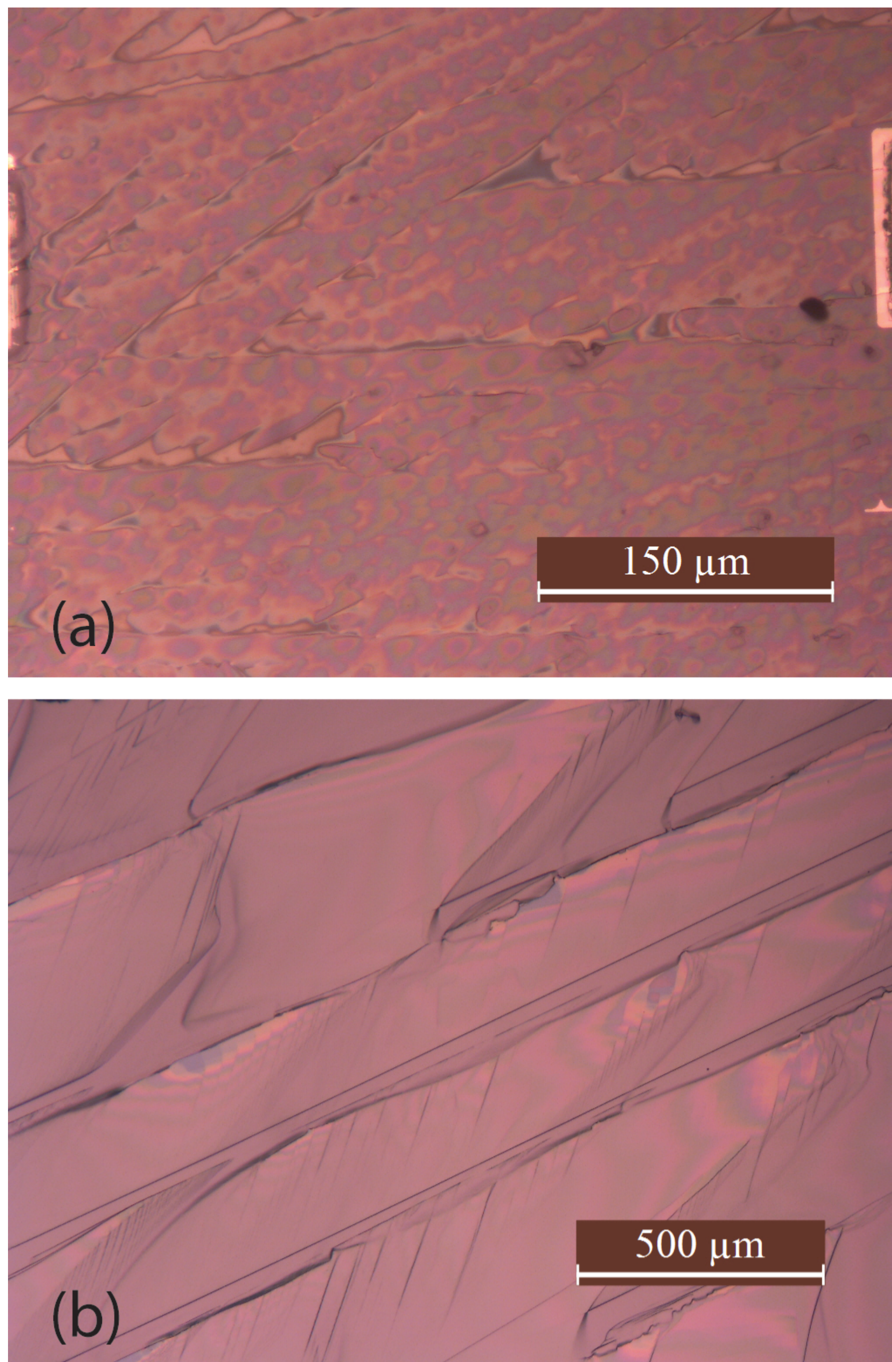


Figure 6-4: Optical micrographs of TIPS-pentacene grown via self-shearing drop cast method (4.5°, 50 °C) over a PFDTES coated sample, showing TIPS-pentacene grown in the (a) upper half and (b) lower half of the slanted sample, resulting in thin and thick layers, respectively.

thickness of the active layer for reducing non-ideal characteristics. The thin TIPS-pentacene HVOTFT was the first solution-processed thin film transistor capable of driving voltages beyond -450 V.

6.4 High-Field Effects in TIPS-Pentacene HVOTFTs

The reliability of the thin TIPS-pentacene HVOTFT was investigated by analyzing changes in threshold voltage (V_T) and onset to conduction voltage (V_X) during high-field stressing, by progressively increasing the maximum drain voltage V_{DS}. It was found that V_T became more positive with increasing maximum V_{DS}, shown in Fig. 6-8 (a). An increased presence of interface states within the gated region due to high field stressing can shift the threshold voltage [159]. For V_X, it was shown previously that the onset to conduction can be reduced with the introduction of a field plate by providing additional weakly accumulated charges to respond to the charge injection between the gated and offset region. Here, V_X became more negative with increasing maximum V_{DS}, as shown in Fig. 6-7. This delayed onset to conduction was attributed to an increased charge injection barrier at the boundary between the gated and offset channel regions [159]. However, V_X could recover by reducing the maximum V_{DS} applied in subsequent measurements, as shown in Fig. 6-8 (c,d). This is similar to what was reported by Martin et al. in their a-Si HVTFT, suggesting that metastable deep traps formed under high stress led to an increased charge injection barrier [57]. Under high bias, deep trap states were formed, and needed to be overcome before injection of charge carriers occurred. Initial charge flow was trapped in the deep trap states, forming a localized charge that opposed further injection [57]. In addition, it was found that V_X was largely invariant to V_{GS}, suggesting that only the horizontal field affected the deep trap formation, shown in Fig. 6-8 (b).

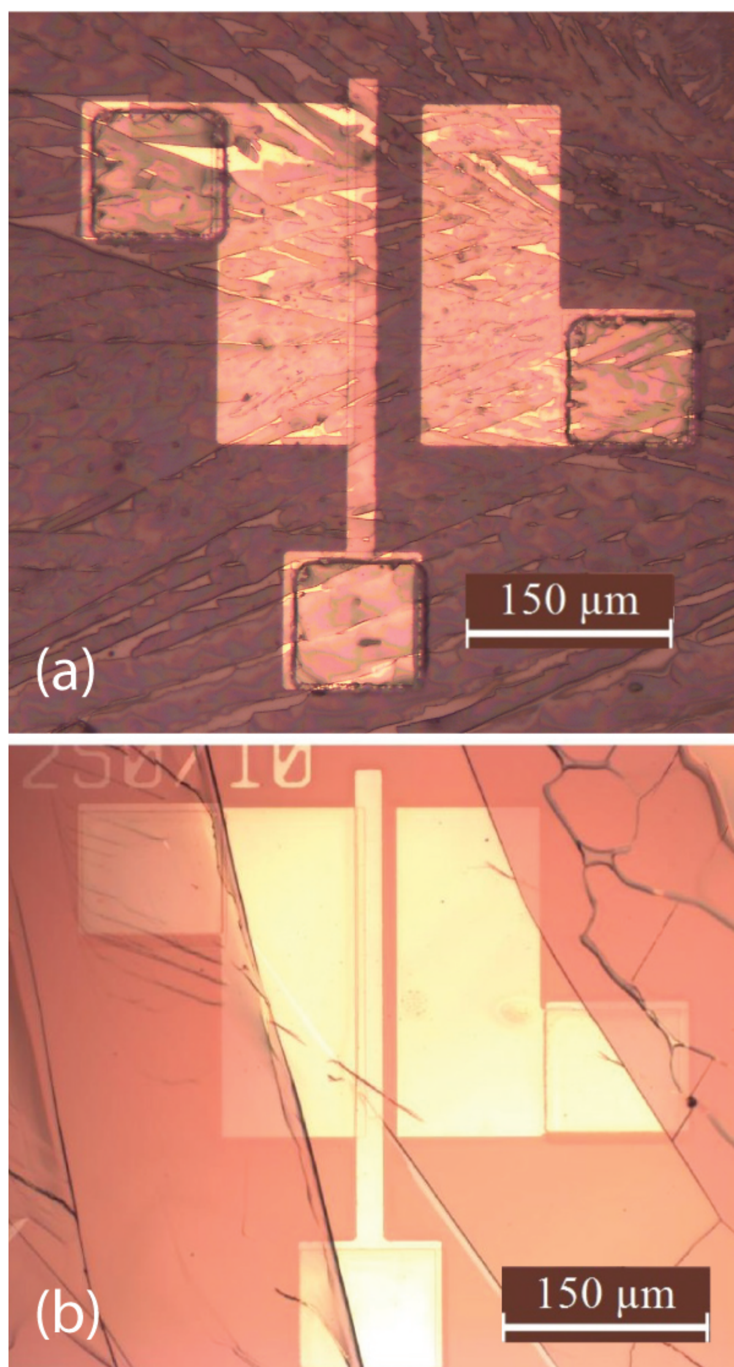


Figure 6-5: Optical micrographs of HVOTFTs with (a) thin TIPS-pentacene layers (< 100 nm) and (b) thick TIPS-pentacene layers (~ 0.5-3 μm).

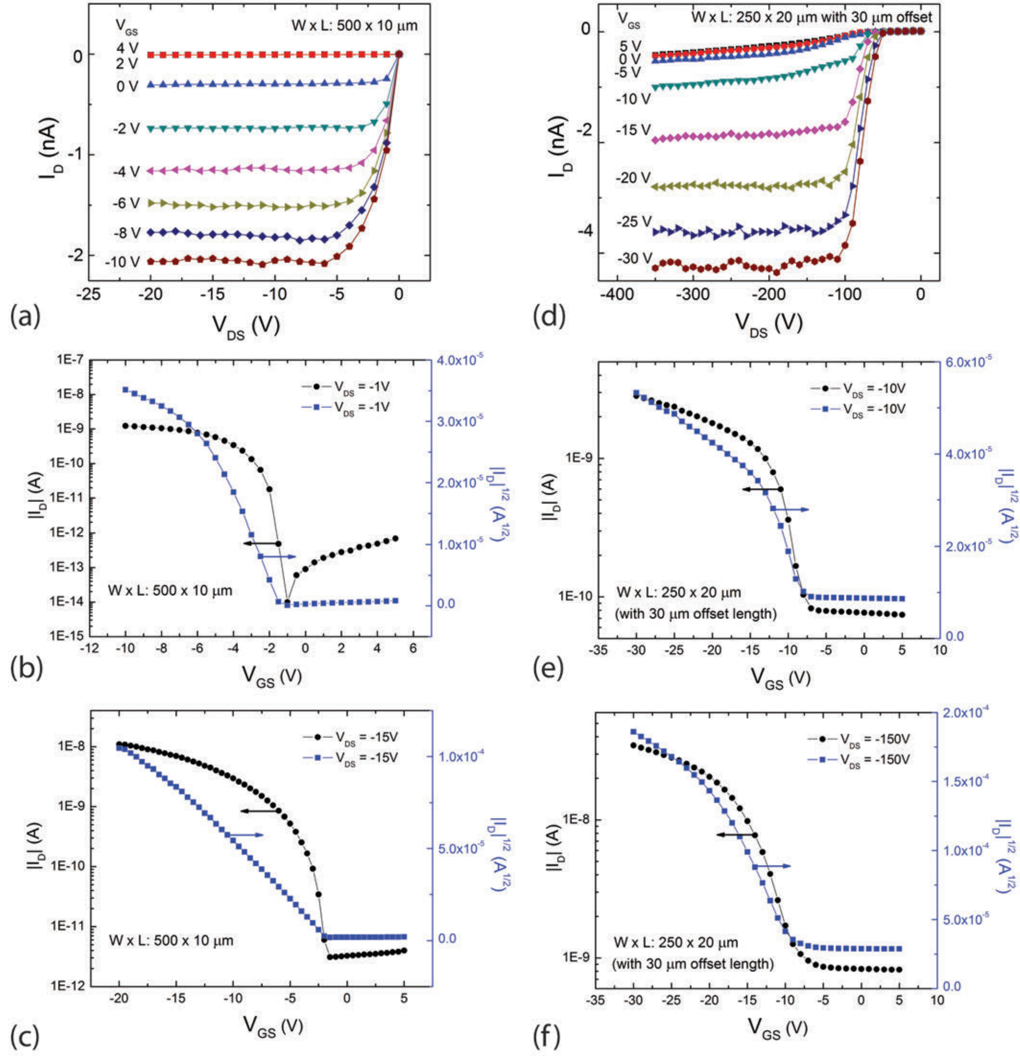


Figure 6-6: Output, linear transfer and saturation transfer I-V characteristics of a thin TIPS-pentacene (a) OTFT (W = 500 μm, L = 10 μm) and (b) HVOTFT (W = 250 μm, L = 20 μm, L_{offset} = 30 μm), made with a PFDTES SAM treatment.

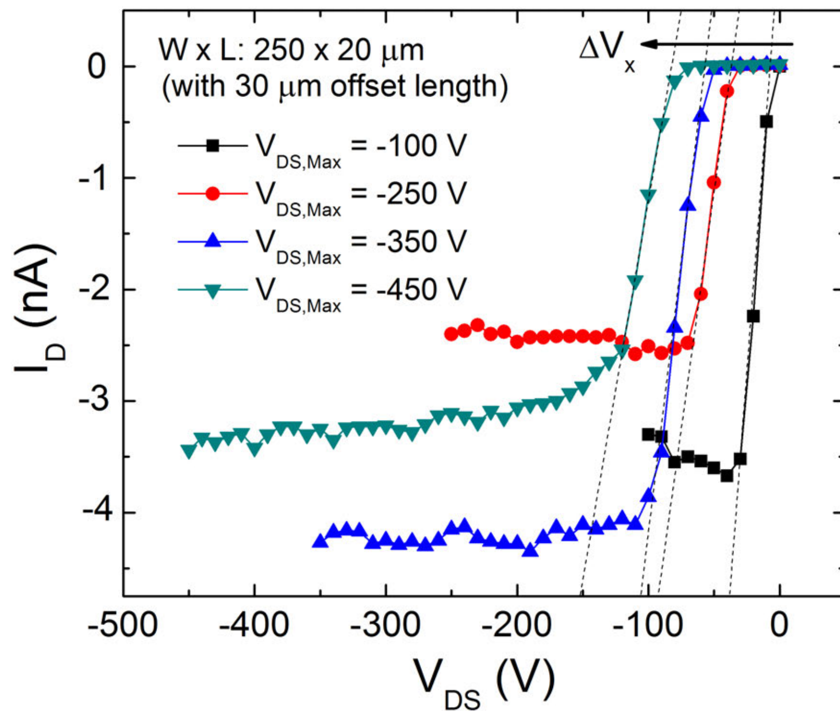


Figure 6-7: I-V output characteristics of a thin TIPS-pentacene HVOTFT (W = 250 μm, L = 20 μm, L_{offset} = 30 μm) with PFDTES treatment. Subsequent scans were performed at higher max V_{DS}, resulting in increased (more negative) onset to conduction V_X.

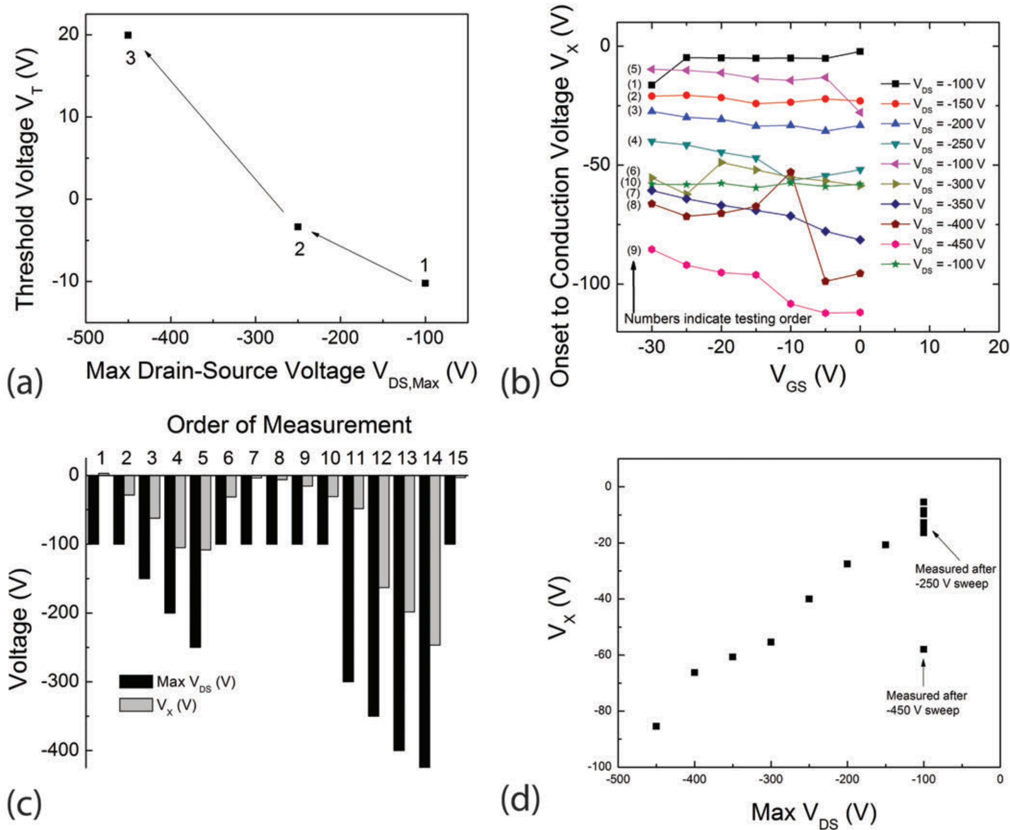


Figure 6-8: Analysis on the variation of electrical parameters (V_T and V_X) under continual bias stress, particularly increasing maximum V_{DS} values. (a) The threshold voltage becomes more positive as $|V_{DS,Max}|$ increases. (b) The onset to conduction is largely invariant to V_{GS}. (c,d) V_X is affected by the electrical bias, but was shown to return to original values under relaxed conditions.

6.5 Flexible TIPS-Pentacene OTFTs and HVOTFTs

To achieve a truly-ubiquitous electronics world as described in chapter 1, HVOTFTs would have to be fabricated on arbitrary and flexible substrates. This would enable the ability to drive large voltages on said substrates for micro- and macro- actuation. TIPS-pentacene HVOTFTs were fabricated on flexible Kapton polyimide substrates. C-V measurements were first performed to assess the reliability of the BZN and parylene-C under flexure. Cross capacitors of areas between 400 and 2500 μm^2 were measured, with the dielectric constant extracted. As shown in Fig. 6-9, the dielectric constants decreased marginally during flexure; however, upon relaxation, the dielectric was able to recover. Minimal to no delamination of the dielectric layers was observed. Electrical measurements were performed on the thick TIPS-pentacene HVOTFTs, transitioning from a flat to a more curved sample with radii of curvatures of 100, 75 and 50 mm. The sample was then brought back to being flat for comparison. The flexure was performed parallel to the channel length. As seen from Fig. 6-10, overall current output and mobility decreased with subsequent bending of the sample. For OTFT devices, mobility decreased, initially sharply, and then gradually from 6e-4 to 3.8e-4 $cm^2/V \cdot s$ while the threshold voltage became more positive, shifting from -3 to -1 V. For HVOTFTs, the trend was similar. Mobility decreased from 2e-4 to 1e-4 $cm^2/V \cdot s$ while the threshold voltage became more positive, going from -5 to -3 V. Although not perceivable by optical micrographs, it is believed that micro-cracks perpendicular to the bending direction, and thus the channel length, are being induced during flexure, which would reduce the overall mobility. Such defects would also act as charge traps, reducing the threshold voltage. Moreover, the adhesion of the thick TIPS-pentacene to the patterned substrate appeared to be slightly compromised with each bending of the sample. It is believed that adhesion can be improved with a more uniform and thin layer of TIPS-pentacene. The I-V characteristics and electrical properties of the flexed TIPS-pentacene OTFT and HVOTFT are shown in Fig. 6-11 and 6-12 and Table 6.4.

Table 6.4: Electrical properties for flexible TIPS-pentacene OTFTs and HVOTFTs made on Kapton polyimide substrates for flat and 50 mm bending radius conditions.

Sample	I	II	III	IV
Bending radius	Flat	Flat	50 mm	50 mm
Semi-conductor	TIPS-pen	TIPS-pen	TIPS-pen	TIPS-pen
Structure	OTFT	HVOTFT	OTFT	HVOTFT
No. of Devices Tested	10	10	10	10
Substrate	Kapton	Kapton	Kapton	Kapton
Dielectric	PAR-C	PAR-C	PAR-C	PAR-C
t_{ox} (nm)	200	200	200	200
ϵ_r	3.15	3.15	3.15	3.15
E_{OT} (nm)	247	247	247	247
C_{ox} (F/cm^2)	1.39e-8	1.39e-8	1.39e-8	1.39e-8
Field-Plate	None	None	None	None
SAM	PFDT	PFDT	PFDT	PFDT
μ_{lin} (cm^2/V·s)	6.11e-3	1.44e-3	3.59e-3	6.04e-4
μ_{sat} (cm^2/V·s)	1.01e-2	4.74e-3	8.00e-3	1.98e-3
V_T (V)	-6.89	-6.90	-6.22	-4.96
SS (V/dec)	2.00	5.41	2.00	4.06
I_{ON}/I_{OFF} (A/A)	4300	50	1200	50
V_X (V)	0.23	-10.95	0.34	-9.71
V_{BD} (V)	$<$ -50	$<$ -100	$<$ -50	$<$ -100
$I_{G,leak}$ (A)	-6e-9	-5e-9	-3e-7	-3e-9
W (μm)	250	250	250	250
L (μm)	[10,20]	[10,20]	[10,20]	[10,20]
L_{offset}	0	[5, 10, 20, 30]	0	[5, 10, 20, 30]

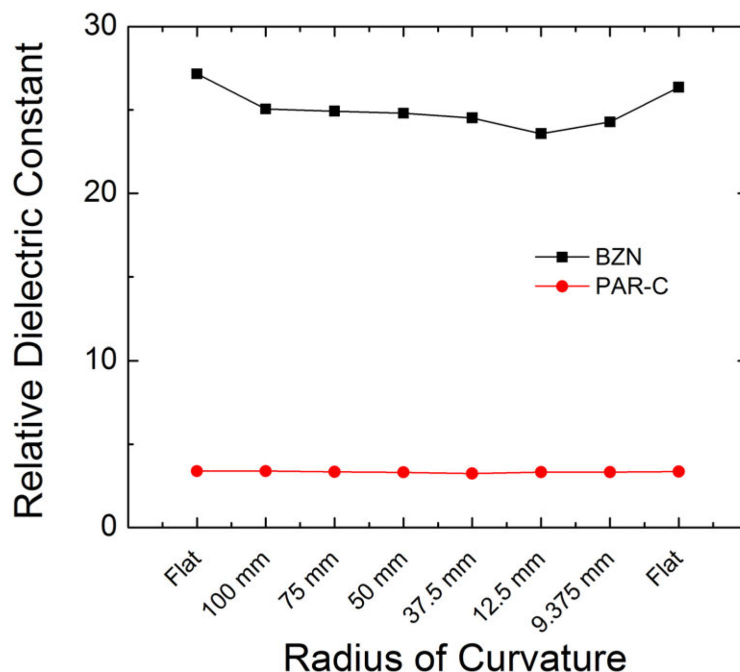


Figure 6-9: Dielectric constant of BZN and parylene-C on a Kapton polyimide substrate under flexure.

6.6 Summary

Rigid and flexible solution-processed TIPS-pentacene OTFTs and HVOTFTs were successfully fabricated with a self-shearing drop cast deposition method. The HVOTFTs had large breakdown voltages beyond -450 V, a first of its kind for an organic solution-processed thin film transistor. A summary of the findings for TIPS-pentacene OTFTs and HVOTFTs are given below.

TIPS-Pentacene OTFTs and HVOTFTs

- TIPS-pentacene OTFTs and HVOTFTs have been successfully fabricated on glass and Kapton polyimide substrates by using a self-shearing drop cast method.
- Self-assembled monolayers have been used to treat the Au contacts for improved charge injection. Particularly, fluorinated organothiol SAMs such as PFDT and 4-FTP reduced the hole injection barrier and improved carrier mobility.

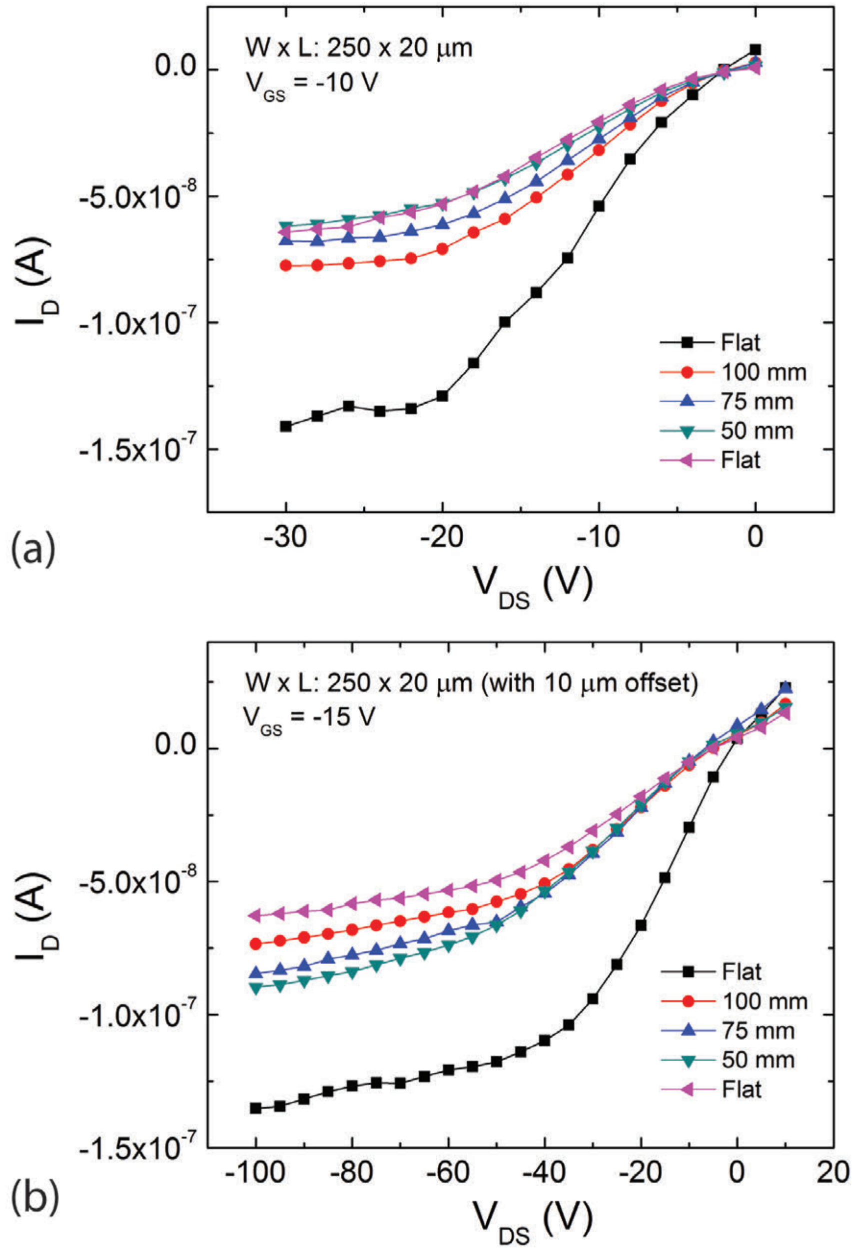


Figure 6-10: I-V output characteristics of an (a) OTFT and an (b) HVOTFT at various radius of curvature.

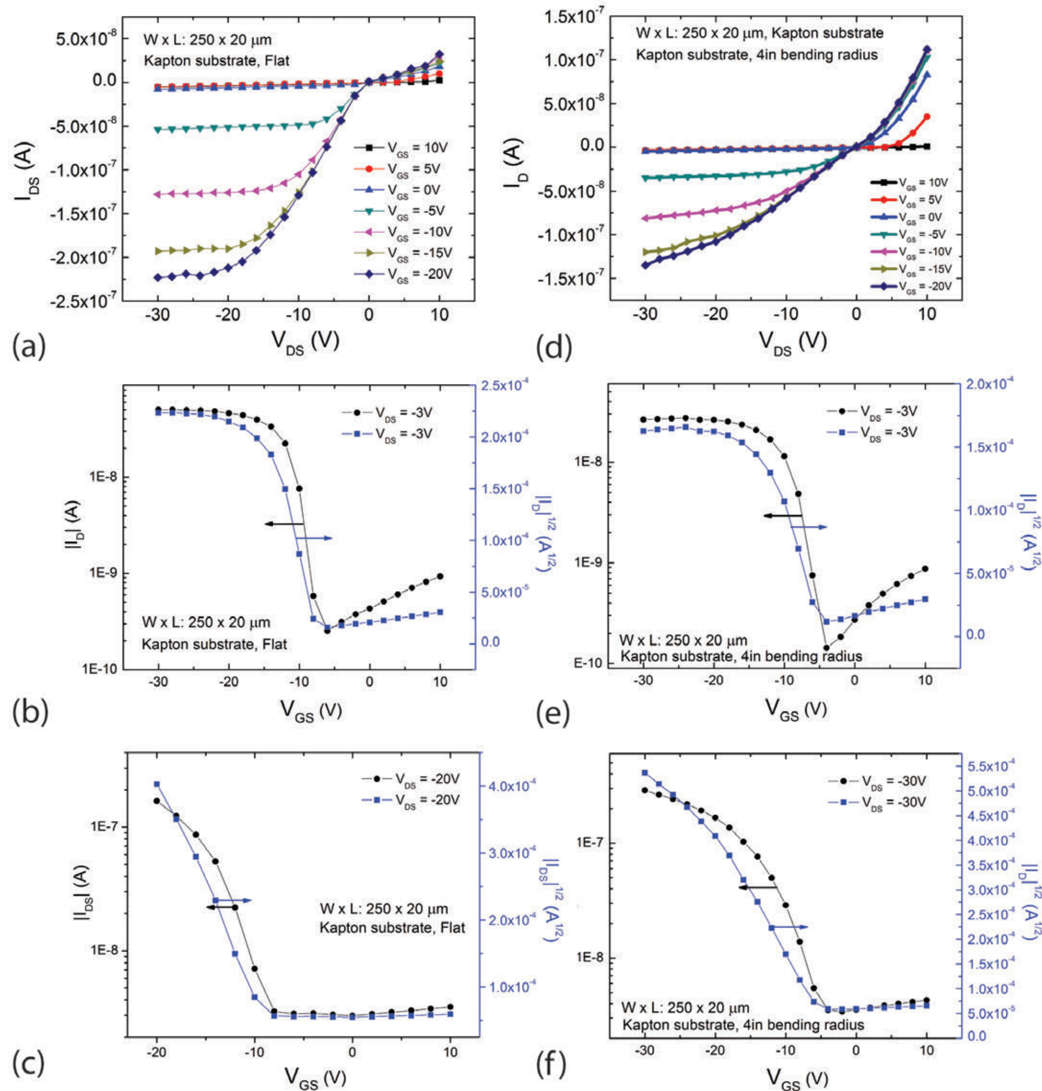


Figure 6-11: I-V output, linear transfer and saturation transfer characteristics for (a,b,c) flat TIPS-pentacene OTFT and for (d,e,f) curved TIPS-pentacene OTFT.

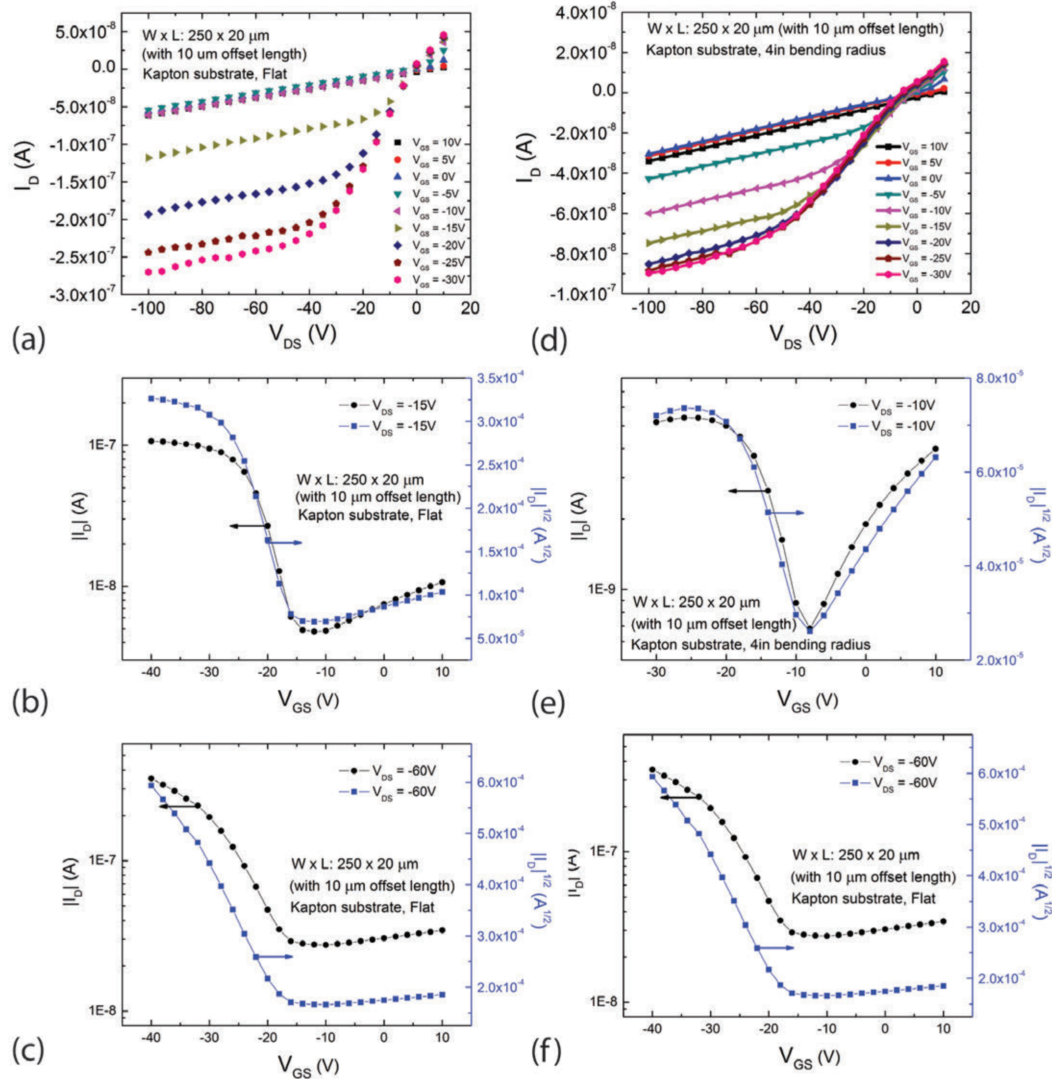


Figure 6-12: I-V output, linear transfer and saturation transfer characteristics for (a,b,c) flat TIPS-pentacene HVOTFT and for (d,e,f) curved TIPS-pentacene HV-OTFT.

Thiophenol, on the other hand, increased the hole injection barrier and reduced the carrier mobility.

- Improved saturation characteristics and I_{ON}/I_{OFF} current ratios were obtained in PFDT and 4-FTP treated samples.

- A low surface energy organosilane SAM (PFDTES) was used to treat the BZN oxide prior to drop casting, promoting an initially quick self-shearing of the organic solution. This resulted in TIPS-pentacene depositions that were much thinner at 100 nm; however, grains bands were semi-random in orientation.

- Initial breakdown voltages for thick (0.5 - 3 μm) TIPS-pentacene HVOTFTs with offset lengths between 5 and 30 μm were approximately -150 V. For thin (100 nm) TIPS-pentacene HVOTFTs, the breakdown voltage was significantly improved to -450 V.

- I_{ON}/I_{OFF} and $I_G, leak$ were improved significantly in thin TIPS-pentacene OTFTs and HVOTFTs, suggesting an optimal thickness needed for solution-processed transistors.

- For TIPS-pentacene HVOTFTs, the threshold voltage V_T became more positive under increasing max drain-source biasing.

- For TIPS-pentacene HVOTFTs, the onset to conduction V_X became more negative under increasing max drain-source biasing.

- The change in the onset to conduction V_X was reversible by reducing the max drain-source biasing. The variation in V_X was attributed to the formation of meta-stable trap states that impeded charge injection between the gated and offset regions.

- The onset to conduction V_X was found to be independent of V_{GS}, and only depended on V_{DS}

- Flexible TIPS-pentacene OTFTs and HVOTFTs were fabricated, operating at a bending radius of up to at least 50 mm.

Chapter 7

Self-Aligned TIPS-Pentacene High-Voltage Organic Thin Film Transistors

Self-aligned solution-processed TIPS-pentacene HVOTFTs fabricated with a self-shearing drop cast method over a patterned SAM sample is presented here, with the cross-sectional diagram and optical micrograph shown in Fig. 4-1 (e,f). In chapter 6, TIPS-pentacene OTFTs and HVOTFTs were developed to combine solution-processing and high-voltage capabilities for novel high-voltage applications on arbitrary substrates. However, the initial solution-processed HVOTFTs had relatively poor electrical properties due to the thick organic semiconductor layers (0.5 - 3 μm), achieving a breakdown voltage of only -150 V. Although PFDTES SAM treatments reduced the surface energy of the sample leading to thin TIPS-pentacene layers (< 100 nm) and improved breakdown voltages beyond -450 V, the resulting quick shearing of the organic solution proved difficult to control. Moreover, the semi-randomness of the organic crystal grains resulted in low transistor yields. An alternative and high yield fabrication method was needed to systematically grow thin organic semiconductor layers for high performing HVOTFTs. Researchers have already employed alternative solution-processing methods such as zone casting and ink-jet printing to achieve thin organic crystalline layers and isolated channel regions, respectively [49].

However, these methods require specialized tools to disperse the organic solution in a precise manner. Here, an alternative drop cast deposition method involving surface energy engineering was proposed, retaining the ease and quick turn around of the drop cast method while introducing a higher degree of control over the crystallization of the organic semiconductor. Surface energy engineering can be achieved by selectively depositing self-assembled monolayers. With the appropriate SAMs and low enough surface energy, dewetting and wetting regions could be defined on the HVOTFT samples resulting in selective areas where aggregation of the organic solution could occur. The only requirement for such a method is the ability to deposit and pattern one or more SAMs of which standard IC fabrication tools can perform.

The surface energy of materials with and without SAM treatments was measured to find a working combination. Ultimately, a self-aligned process, shown in Fig. 7-1, was developed in which the PFDT organothiol and PFDTES organosilane SAMs were used to coat selective areas of Au and BZN, respectively, creating wetting and dewetting regions. The SAMs reduced the surface energy of selective areas below the level of the surface tension of anisole, enabling a selective coating process. The wetting regions placed directly above the channel (where SAMs would not be present) would accumulate the organic solution during drop casting, creating a self-aligned organic semiconductor pattern without having to directly etch the TIPS-pentacene. Not only did this method create transistor to transistor isolation, but it also reduced the volume of organic solution per surface area which in turn thinned the deposited organic layer. This resulted in high yield self-aligned TIPS-pentacene HVOTFTs with large breakdown voltages and I_{ON}/I_{OFF} current ratios of -550 V and 10^6 A/A, respectively. The self-aligned fabrication procedure, atomic force microscopy of the TIPS-pentacene and the I-V characteristics of the self-aligned OTFTs and HVOTFTs are presented below.

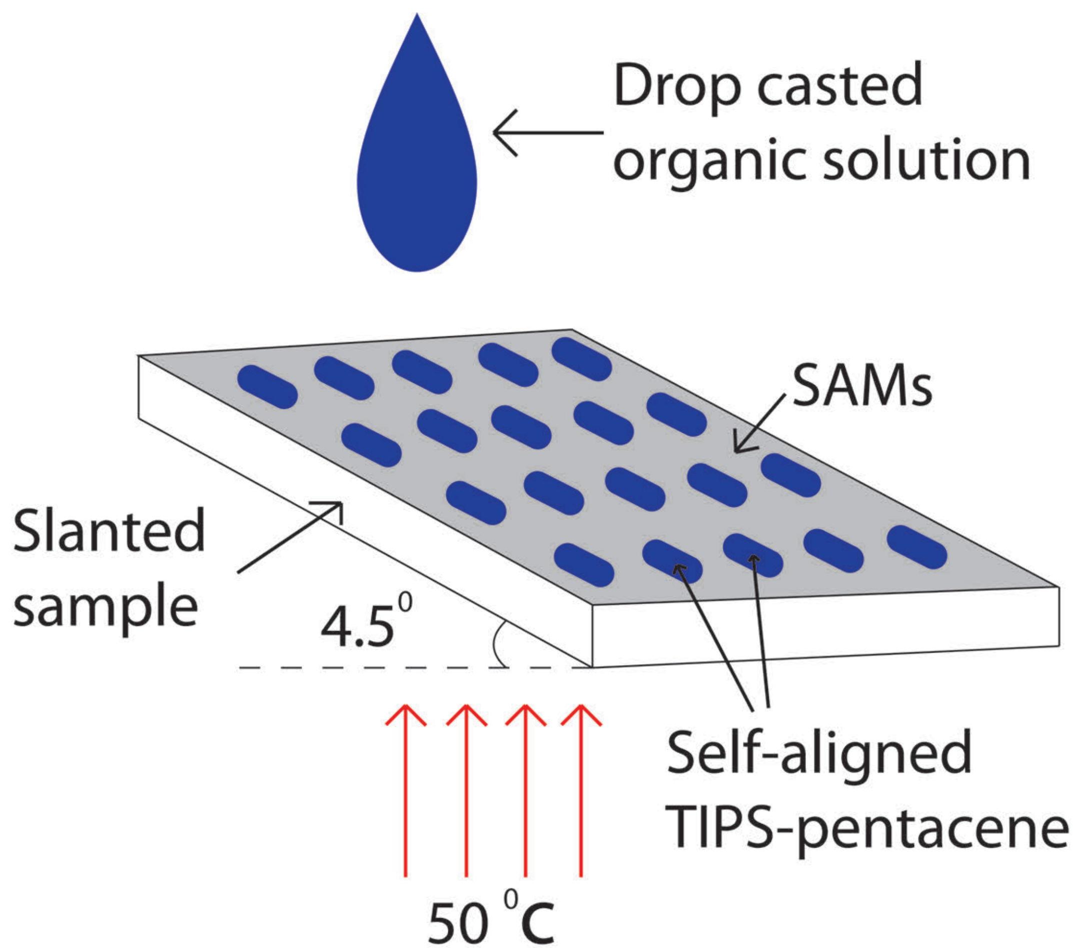


Figure 7-1: Self-aligned self-shearing drop cast method for the deposition of TIPS-pentacene. SAMs was patterned on the surface of the HVOTFT samples to create wetting and dewetting regions.

Table 7.1: Surface tension of test liquids used for surface energy measurements.

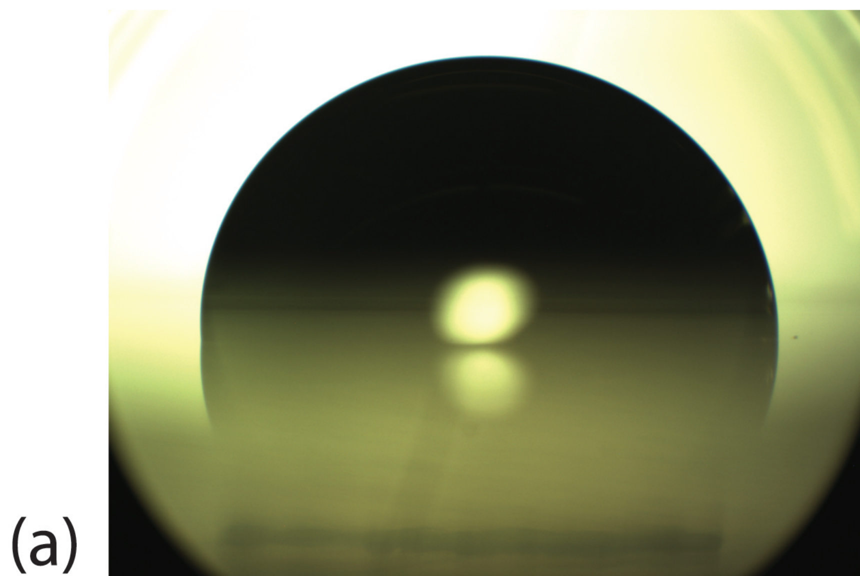
Test Liquid	DI Water	Ethylene Glycol
Surface Tension (mN/m)	72.8	48
Dispersion (mN/M)	21.8	29
Polar (mN/M)	51	19

7.1 Characterization of SAMs

The surface energies of various samples and the effects of SAM treatments were investigated using a Ramé-Hart 260 contact angle goniometer. The Neumann, Owens-Wendt (geometric mean) and Wu (harmonic mean) methods described in section A.1.5 were employed to calculate the surface energies. For both the Owens-Wendt and Wu methods, DI water and ethylene glycol were used as the two reference liquids, with their surface tension components summarized in Table 7.1. 10 μL of each liquid was dropped onto a variety of surfaces, with their contact angle measured. Images of the DI water and ethylene glycol droplets are presented in the appendix in Fig. C-1, C-2, C-3, C-4.

The absolute value of the surface energies calculated by each method is to be taken with a grain of salt as their is no consensus on the ideal method to be used for such calculations. However, the relative values within a method described the lowering or increasing of the surface energy, which can be used as an indicator of proper SAM deposition. Figure 7-2 shows the summary of all the surface energies calculated using the various methods for different surfaces. To compare between surfaces, the average value of the three methods were used. Furthermore, it is noted that the surface energy calculated with such methods has an upper limit, and cannot surpass a value of a few hundred. Thus, the surface energies of samples with values of several thousands (such as glass and Si, with values of 4400 and 1240 mN/m, respectively) cannot be directly calculated using such methods.

It was found that BZN had a surface energy of 46.07 mN/m (similar to the value of 43 mN/m, reported by Smith et al. [158]), with the polar force being the main



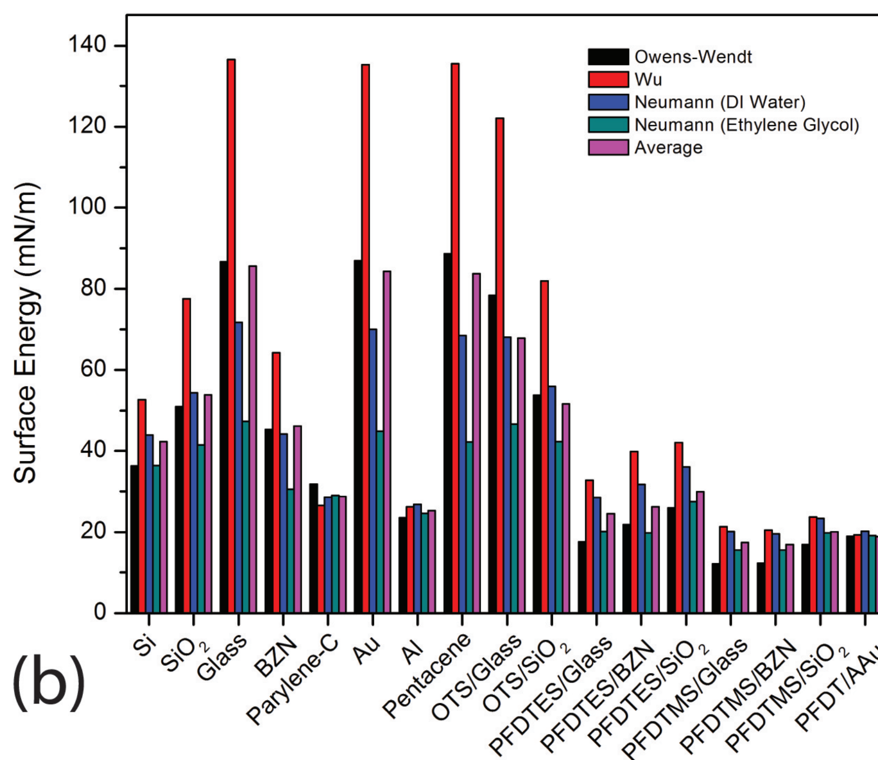


Figure 7-2: (a) DI water droplet on a PFDTES SAM treated glass sample. (b) Surface energies calculated using the Owens-Wendt, Wu and Neumann (DI water and ethylene glycol) for various surfaces and SAM-treated surfaces.

contribution originating from the hydroxyl bonds at the oxide surface. Parylene-C, on the other hand, had a significantly lower surface energy of 28.7 mN/m due to less polar bonds at the organic surface. This corresponded well with a value of 27.64 mN/m found by Chindam et al. [160]. E-beam evaporated Au was also found to have a large surface energy of 84.32 mN/m that would be wetted by the DI water and ethylene glycol.

Of particular interest were the surfaces treated with SAMs. OTS, PFDTES and PFDTMS organosilanes are reported to have surface energies of 24.0, 18.1 and 16.6 mN/m, respectively, while the PFDT organothiol has a surface energy of 20.0 mN/m. With the SAM treatments of BZN and Au, the surface energy can be reduced below the value of the surface tension of anisole (35 mN/m), creating a dewetting region. In other words, when anisole is dropped onto a SAM treated sample, the expectation would be for a droplet to form, with large contact angles above 90°. This droplet can then be easily moved across the surface by tilting the sample until the droplet finds a region of high surface energy (regions where SAMs are not present), enabling the self-aligned TIPS-pentacene growth method. The organosilanes were deposited on various surfaces, shown in Fig. 7-2, via a desiccator at room temperature for 5 hours while the organothiol was deposited via an ethanol (0.1 vol%) solution for 2 hours. The OTS on SiO_2 as well as PFDTES and PFDTMS on BZN were found to have surface energies of 51.61, 26.27 and 16.92 mN/m, respectively. Furthermore, the PFDT on Au was measured to have a surface energy of 18.82 mN/m. The surface energies correspond well with reported values, except for the case of OTS. It is believed that the vapor pressure of OTS may be lower than those of PFDTES and PFDTMS, resulting in low to no deposition in the desiccator. No vapor pressure values were found for the SAMs used to verify this claim. However, the surface energy of the OTS treated SiO_2 samples had the same value as untreated SiO_2, suggesting that no OTS was deposited. Nonetheless, it was shown that BZN and Au can be treated with SAMs that would reduce its surface energy below the surface tension value of anisole.

An experiment was then devised to verify the dewetting of anisole on SAM treated samples as well as the SAMs stability under various solvent conditions that may be

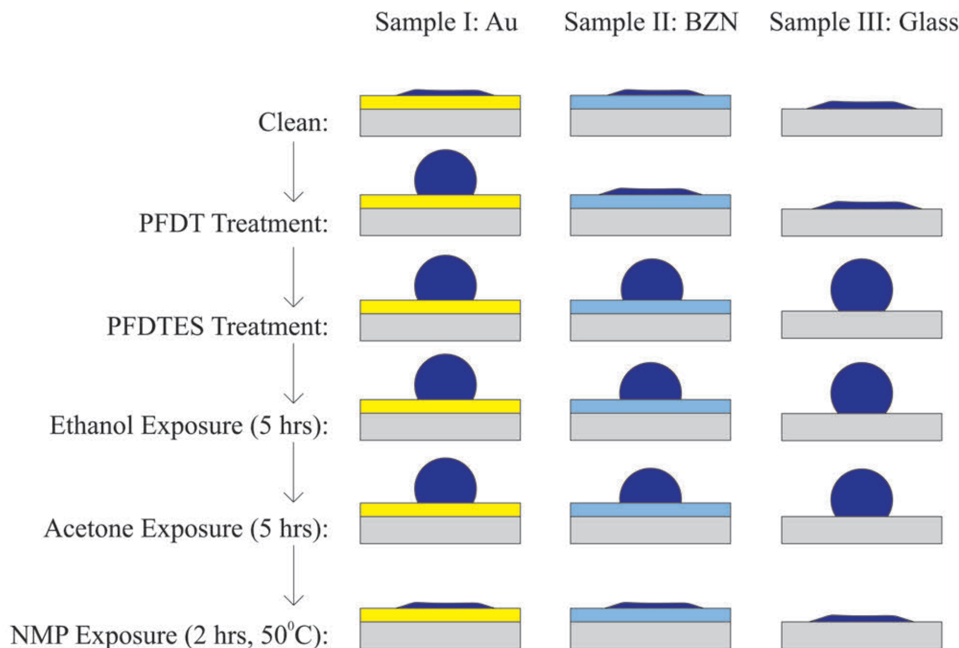


Figure 7-3: Experimental diagram for SAM treatment and SAM stability analysis of Au, BZN and glass samples under various conditions (different and subsequent SAM treatments and solvent exposures). Wetting and dewetting of the surfaces are represented by a flattened and high contact angle anisole droplet, respectively.

used during photolithography. Clean glass, Au and BZN samples were first treated with PFDT (0.1 vol% ethanol solution for 2 hours), followed by PFDTES treatment (desiccator, 12 hours). The assumption was that PFDT would not bond with the glass or BZN samples, and would leave the bare surface available for PFDTES treatment. Likewise, subsequent PFDTES treatment would not affect the PFDT monolayer on the Au. The SAM treated samples were then submerged in either ethanol, acetone or n-methyl-2-pyrrolidone (NMP) for several hours to access the reliability of the SAMs under various solvent conditions. In between each SAM treatment and each solvent exposure, 2 μL of DI water (surface tension of 72.80 mN/m) and anisole (surface tension of 35.00 mN/m) were dropped onto the surface to assess if a high contact angle droplet was formed and if the droplets would slide off with ease under a slant. If the droplets would slide off easily, the SAM would be determined as present on the surface. A summary of the results are illustrated in Fig. 7-3.

Prior to SAM treatments, the DI water and anisole was found to fully wet the

surfaces (low contact angles below 10°). After PFDT treatment, DI water and anisole formed high contact angles ($> 90°$) with the Au sample, as expected. Interestingly, anisole initially exhibited dewetting properties on PFDT treated BZN, even though the organothiol should not make covalent bonds with the oxide. However, after rinsing the BZN surface with DI water and blow drying with nitrogen, residual PFDT was removed and the surface was wetted once again by the anisole. PFDTES treatment was then performed, allowing for dewetting of DI water and anisole on all samples.

The stability of the SAMs were accessed under various solvent conditions. The PFDT and PFDTES treated samples were submerged in either ethanol, acetone, or NMP, each for 2 hours followed by an additional 3 hours. Furthermore, two NMPs were used, one at room temperature and another heated to 50° over a hot plate. It was found that the ethanol and acetone had no appreciable affect on the dewetting of DI water and anisole. However, heated NMP appeared to completely remove PFDT on Au after only 10 minutes of exposure. Furthermore, PFDTES on BZN and glass was affected by the heated NMP, visually reducing the anisole contact angle below 45°. Thus, it was concluded that glass, Au and BZN could be treated sequentially with PFDT and PFDTES to reduce their surface energy such that anisole would form a high contact angle droplet. Additionally, ethanol and acetone could be used in subsequent photolithography processes on the treated samples.

7.2 SAM Patterning

It was successfully shown that PFDT and PFDTES could be used to create high contact angle anisole droplets and enable a self-pattern fabrication method. However, the PFDT and PFDTES monolayers needed to be patterned prior to drop casting TIPS-pentacene to distinguish between a wetting and dewetting region. Specifically, an absence of SAMs over the channel region of the OTFTs and HVOTFTs was needed for the aggregation of organic solution. A photoresist mask was patterned on top of the samples, with PR covering the channel and exposing the Au and BZN to be treated with SAMs. Unfortunately, the PR was not ethanol resistant and would not survive

a PFDT SAM treatment. Attempts at hard baking the PR above 160 °C proved effective in reducing the solubility of the PR in ethanol; however, the PR could only then be removed by using heated NMP. As mentioned previously, heated NMP would have a detrimental effect on the PFDT. Alternatively and successfully, PFDT was deposited onto Au using the desiccator method with the addition of an infra-red heat lamp. The PFDT inside the desiccator was heated to approximately 60 °C, which increased exponentially the vapor pressure of the SAM for sublimation and deposition onto the Au. Thus, patterned PFDT and PFDTES was successfully deposited onto the OTFT and HVOTFT structures. The photoresist was then stripped away by submerging the sample in acetone and isopropyl alcohol for 10 minutes each, followed by a DI water rinse. Self-shearing drop casting can then be performed.

7.3 Self-Aligned Drop Casting of TIPS-Pentacene

Before fabrication of self-aligned HVOTFTs, test samples were prepared to characterize the growth of the TIPS-pentacene. Initially, pure anisole was dropped onto dummy glass substrates with patterned PFDTES. The anisole patterns were observed under an optical microscope with the sample laid at a horizontal without a slant. A time evolution of the anisole was recorded as shown in Fig. 7-4. Firstly, it was noted that the anisole successfully found its way towards the high surface energy glass and avoided the low surface energy PFDTES. Secondly, only a small volume of anisole was present in each pattern, suggesting a method to control the thickness of TIPS-pentacene by controlling the surface area of the SAM patterns. Finally, and most interestingly, the anisole volume retracted along the long axis of the SAM pattern. Evaporation of anisole, due to its high vapor pressure (0.472 kPa at 25 °C), occurred across the entire surface/air interface. However, the anisole volume did not flatten, but instead retracted along the droplet edges perpendicular to the long axis of the SAM pattern. In other words, the anisole droplet tended to minimize its surface area by reducing the long axis dimension of the droplet. This has the potential for a guided self-shearing process in which SAMs can be arbitrarily patterned to dictate

the orientation of the organic semiconductor crystal grains.

Next, TIPS-pentacene solutions were drop casted on dummy glass substrates with patterned PFDTES. To further investigate the effects of temperature, the organic solution and the substrate were either left at room temperature or heated to 50 °C. Firstly, the organic solution was heated to 50 °C and was quickly drop casted onto a slanted (4.5°) and heated (50 °C hot plate condition) sample. The organic solution was heated in an attempt to promote crystallization. However, the organic solution did not aggregate in the SAM patterns, but covered the entire surface. This can be explained by the reduced cohesive forces, and thus surface tension, from increased molecular thermal activity, which is summarized by the Eötvös rule:

$$\gamma * V^{2/3} = k(T_c - T) \tag{7.1}$$

where γ is the surface tension, V is the molar volume, k is the Eötvös constant ($\sim$ 2.1e-7 $J/K \cdot mol^{2/3}$), T_c is the critical temperature and T is the temperature [161].

TIPS-pentacene drop casted from a room temperature organic solution onto a heated (50 °C) substrate proved once again to be the best method to grow full cover TIPS-pentacene layers, as shown in Fig. 7-5. Without a heated substrate, or temperatures above 50 °C, TIPS-pentacene tended to grow in a dendrite formation with gaps between the branches. With a heated substrate, however, full cover was achieved.

7.3.1 AFM of Self-Aligned TIPS-Pentacene

AFM scans were performed on the TIPS-pentacene grown within the SAM patterns on either a non heated substrate or a heated substrate, shown in Fig. 7-6. The dendrite crystal formation of TIPS-pentacene grown on a non heated substrate displayed uniform thickness and an Ra and Rms surface roughness of 2.81 and 3.40 nm, respectively. More importantly, however, is the lack of full coverage of the surface by the branches of the dendrite formation. This lack of cover could lead to unwanted electrical characteristics and potential open circuits between the source and drain contacts. On the other hand, TIPS-pentacene deposited on heated samples displayed

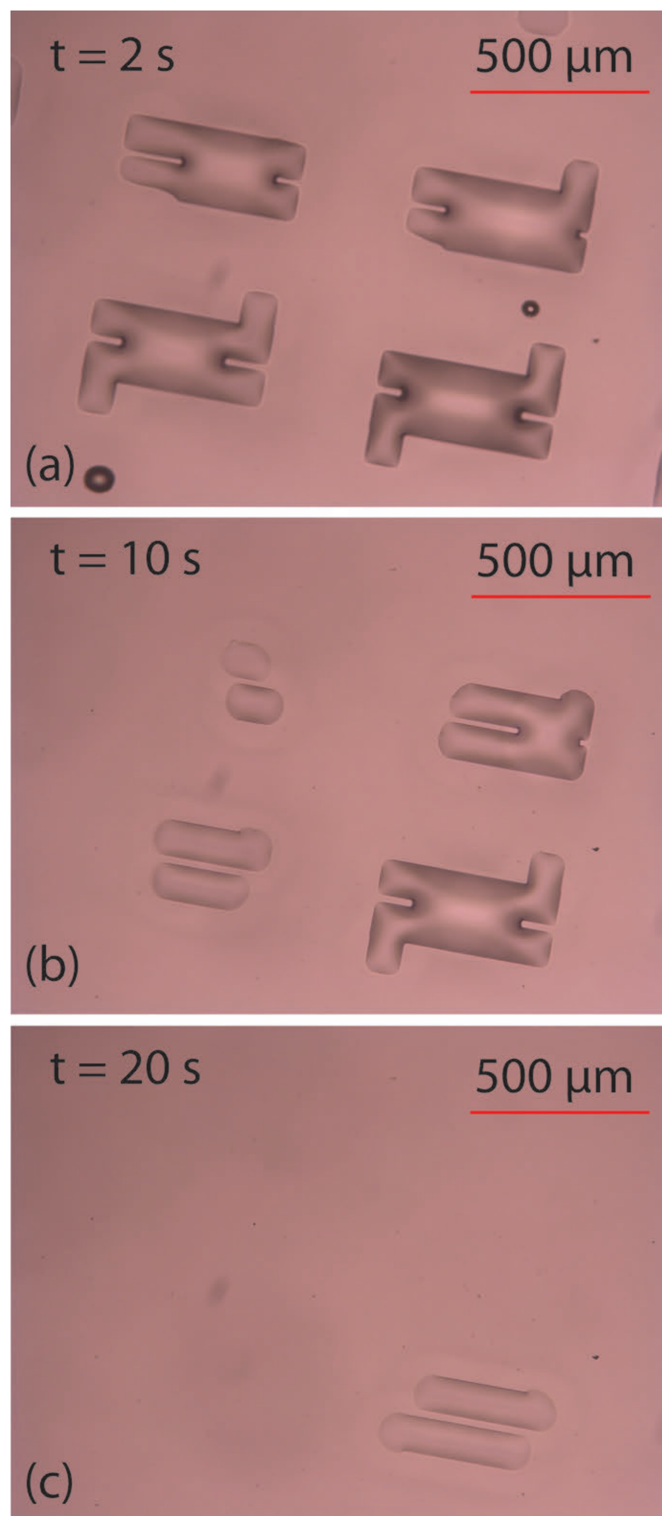


Figure 7-4: Time evolution of dropped anisole solvent over a patterned organosilane (PFDTES) SAM treated sample being evaporated at times (a) 2 seconds, (b) 10 seconds and (c) 20 seconds. The receding front of the solvent is perpendicular to the long axis of the SAM pattern.

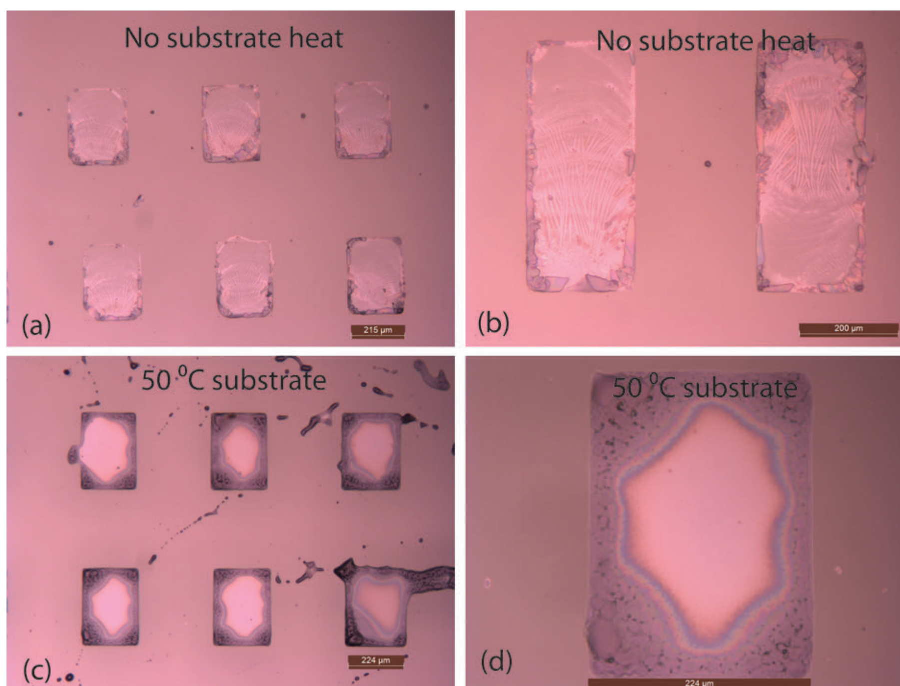


Figure 7-5: Optical micrographs of self-aligned TIPS-pentacene grown on glass, within regions defined by an organosilane (PFDTES) SAM, at different temperature conditions: (a,b) not additional heat and (c,d) 50 °C hot plate conditions.

full coverage within the SAM pattern and had a Ra and Rms surface roughness of 3.49 and 4.56 nm, respectively.

7.4 Fabrication of Self-Aligned TIPS-Pentacene OTFTs and HVOTFTs

Two device architectures were employed to fabricate the self-aligned TIPS-pentacene OTFTs and HVOTFTs: bottom gate / top contact and bottom gate / bottom contact devices. Initially, bottom gate / top contact devices were fabricated due to the relative easy in the SAM deposition. Only a single patterned organosilane would be needed to reduce the surface energy seen by the organic solution. Thus, PFDTES was deposited onto the BZN prior to the Au source and drain contacts. Once the PFDTES was patterned, the organic solution was drop casted and successfully self-aligned to the SAM patterns. Finally, a shadow mask was used to deposit Au for a top contact

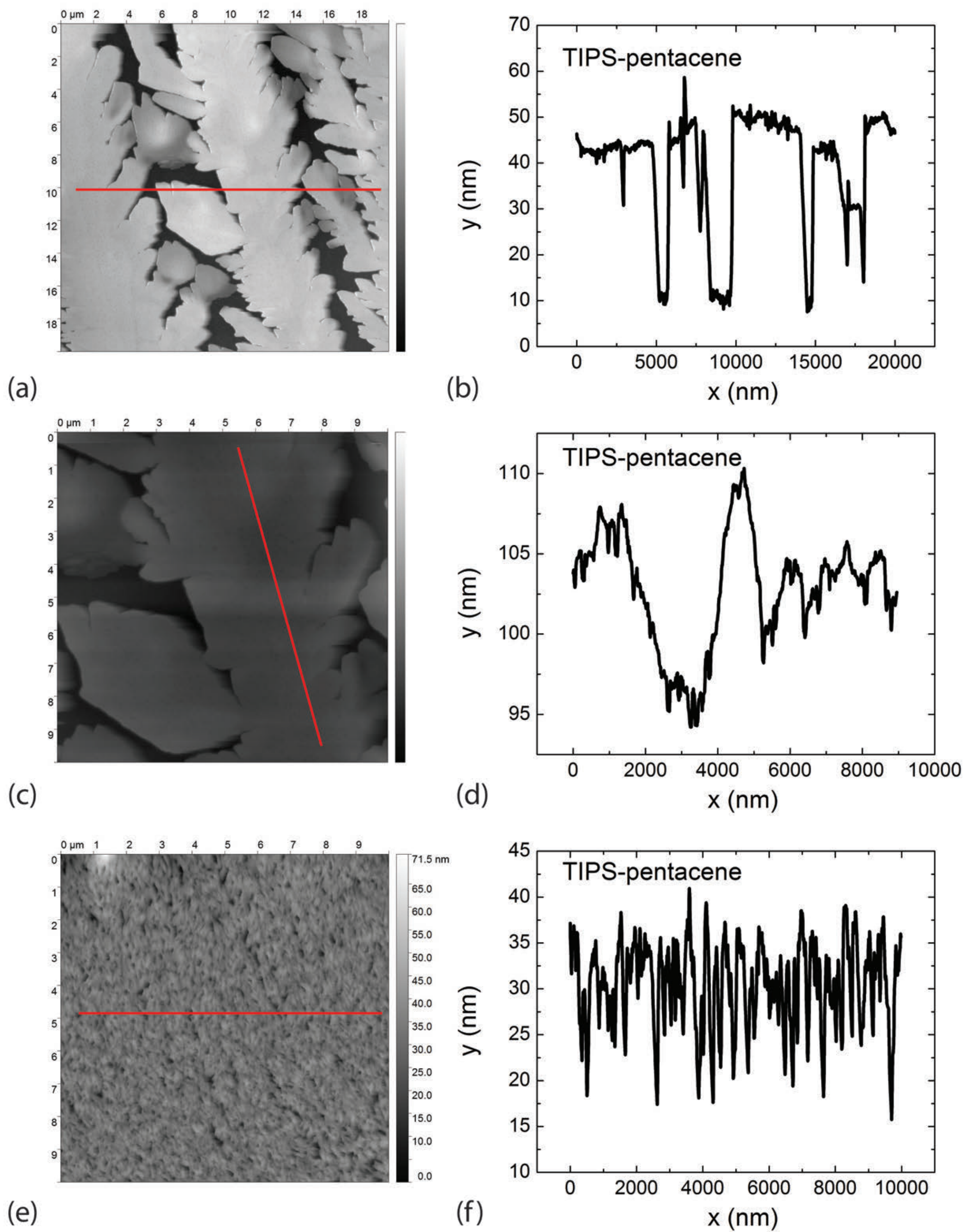


Figure 7-6: AFM scans and the texture cut line along the red line of (a,b) an initial dendrite crystal formation of TIPS-pentacene on glass, (c,d) a close up of the dendrite crystal, and (e,f) TIPS-pentacene grown inside a self-aligned pattern, under 50 °C hot plate conditions.

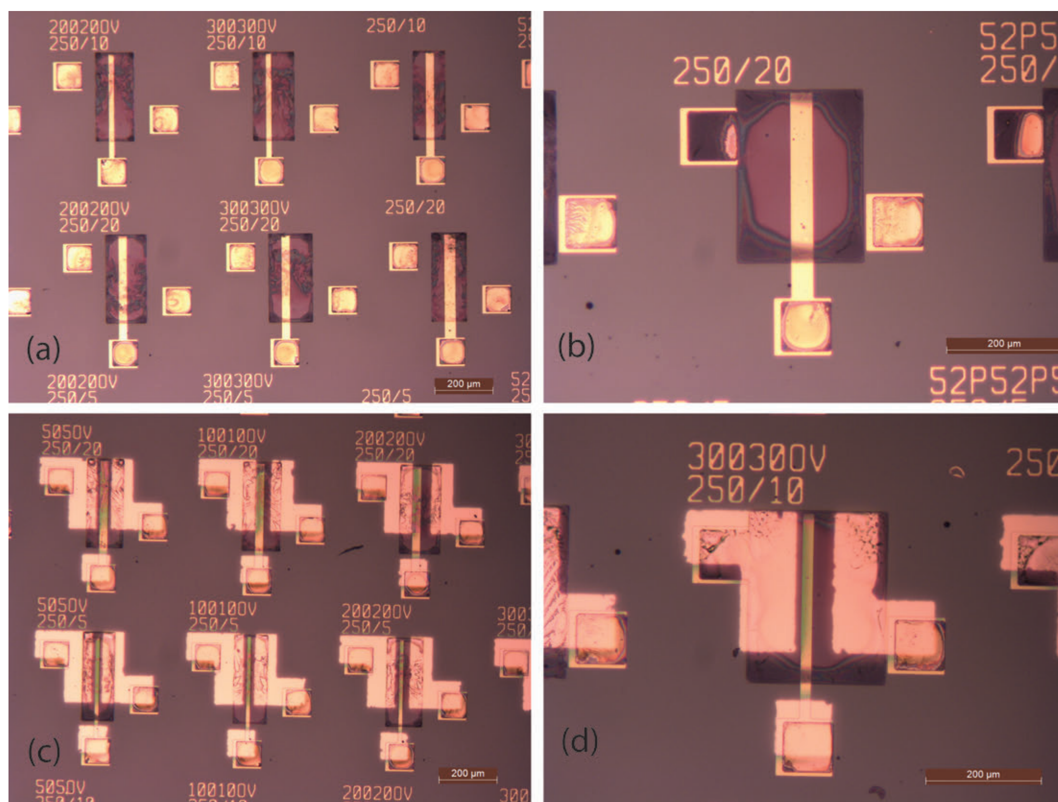


Figure 7-7: Optical micrographs of a bottom gate / top contact self-aligned TIPS-pentacene HVOTFTs, defined by a PFDTES SAM pattern. The initial growth of TIPS-pentacene is shown in (a,b) with the top Au contact, deposited via a shadow mask, is shown in (c,d). The devices did not have FET characteristics.

device, as shown in Fig. 7-7.

Unfortunately, the top contact devices did not exhibit any FET characteristics and appeared only resistive, regardless of the gate voltage. The top surface of the TIPS-pentacene was rough and non uniform, with occasional dendrite formation leading to a lack of full cover. Furthermore, the steel shadow mask or the deposited Au metal may have induced physical and temperature related damages to the TIPS-pentacene.

Thus, a bottom gate / bottom contact architecture was ultimately chosen with the dual SAM deposition and patterning method outlined in section 7.2. Prior to drop casting TIPS-pentacene, pure anisole was dropped onto the SAM patterned HVOTFT structures, as a test, and were quickly brought under a microscope, shown in Fig. 7-8. The anisole was found to successfully aggregate above the transistor channel as expected. However, the anisole droplet did not appear to be well defined. In fact,

the droplet appeared to favor a circular droplet formation, despite the rectangular SAM pattern. Moreover, for the thin SAM pattern, as shown in the mask design in Fig. 4-2, the anisole volume overflowed beyond the SAM pattern and was delimited by the Au metal boundaries. Particularly, the anisole solvent would aggregate inside the source and drain contact pads where vias where made into the BZN layer.

Finished self-aligned TIPS-pentacene HVOTFTs are shown in Fig. 7-9 for both large and small SAM patterns. The TIPS-pentacene grown within the large SAM pattern (Fig. 7-9(a,b)) was uniform in thickness with full cover. Profilometer scans along the length of the HVOTFT were taken, shown in Fig. 7-10. The thickness of the TIPS-pentacene layer was found to be between 20 and 40 nm, with an R_a surface roughness of ~1 nm. Coffee stain patterns of 200 to 500 nm in height were also present and may result in additional unwanted leakage paths and low on state resistance. Further investigation on the effects of the coffee stains is required to optimize electrical properties. On the other hand, TIPS-pentacene grown inside the small SAM pattern (Fig. 7-9(c,d)) displayed a lack of full cover with visible dendrite formations. It is suggested that a minimum volume of organic solution (and hence a minimum surface area for the SAM pattern) was needed to achieve a full cover over the channel area. Furthermore, for the small SAM pattern samples, the TIPS-pentacene grew in a circular pattern that started its nucleation beyond the boundaries of the SAM pattern.

7.5 I-V Characteristics of Self-Aligned TIPS-Pentacene OTFTs and HVOTFTs

I-V output and transfer characteristics were measured for both self-aligned TIPS-pentacene OTFTs and HVOTFTs, shown in Fig. 7-11 and 7-12, respectively. Their electrical properties are summarized in Table 7.2. I-V characteristics were swept from positive to negative biases.

Firstly, the HVOTFT was able to drive voltages beyond -550 V between its source and drain, for an offset length between 20 and 30 μm relative to 10 and 20 μm gated

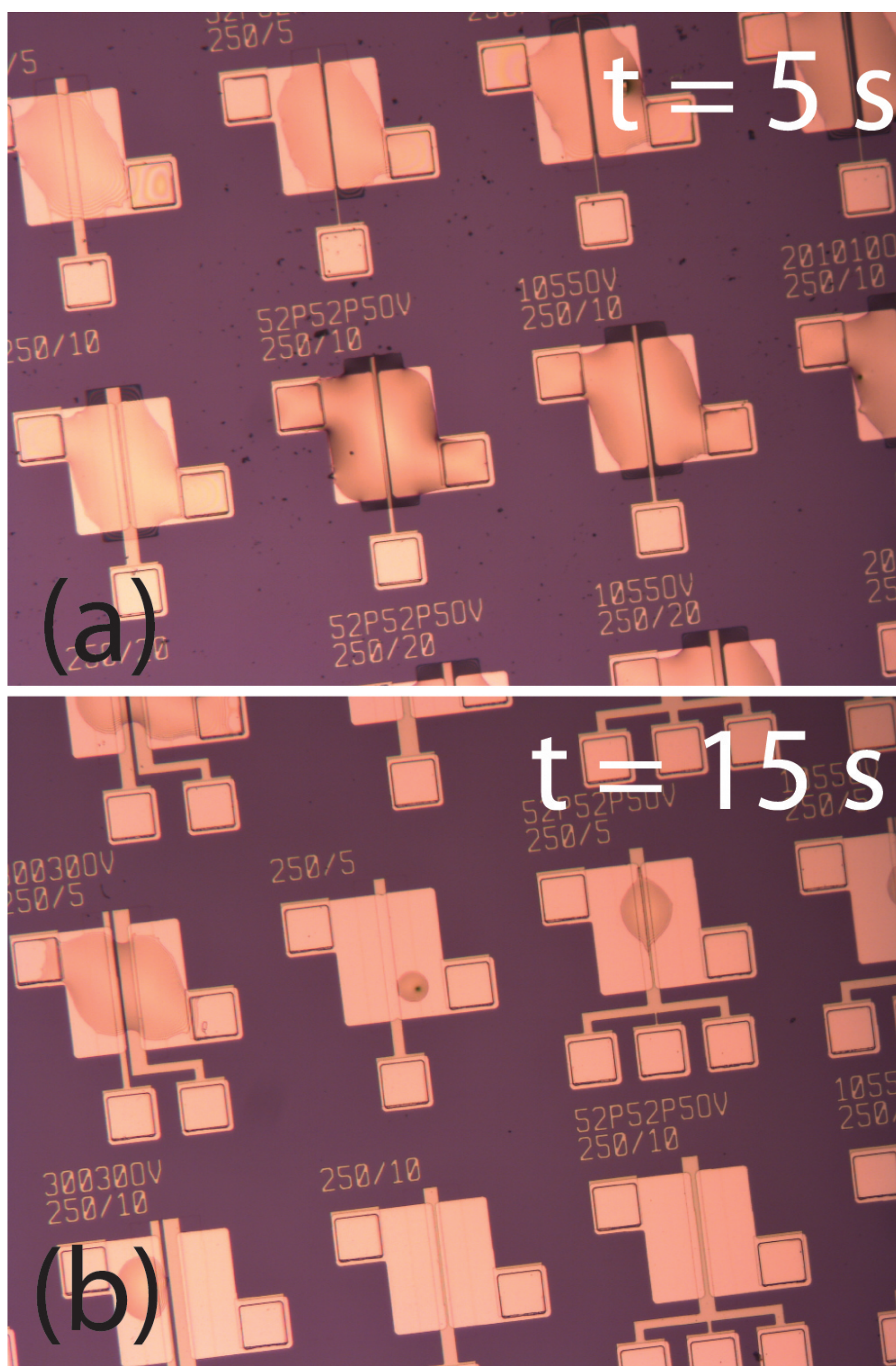


Figure 7-8: Optical micrographs of pure anisole drop casted onto a SAM treated and patterned HVOTFT sample at (a) 5 seconds and (b) 15 seconds.

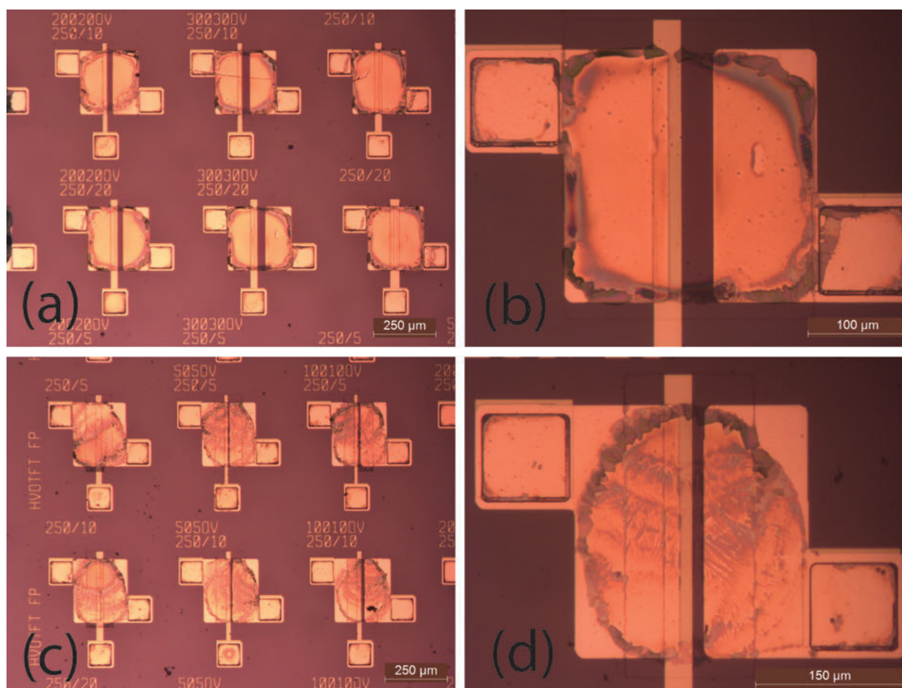


Figure 7-9: Optical micrographs of self-aligned TIPS-pentacene HVOTFTs made with (a,b) large dewetting regions (approximately 250 x 250 μm^2) and (c,d) small dewetting regions (approximately 250 x 150 μm^2).

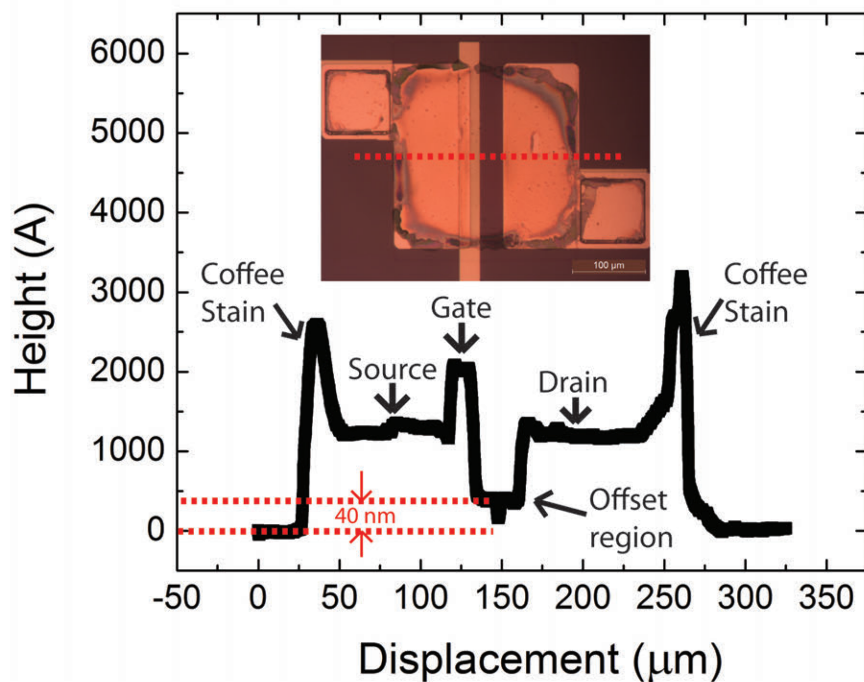


Figure 7-10: (a) Optical micrograph of a self-aligned TIPS-pentacene HVOTFT. The dashed line indicates a profilometer height scan presented in (b). The TIPS-pentacene was found to have a thickness between 20 and 40 nm.

length. Without the offset structure, breakdown voltages were found to be around -50 V for the self-aligned OTFTs. Furthermore, the HVOTFT could be turned on with a relatively low gate to source voltage, with threshold voltages between -1 and -6 V. This is the first ever demonstration of a self-aligned HVOTFT that can enable novel fabrication processes for flexible MEMS integration.

The most striking difference between the self-aligned TIPS-pentacene devices and those presented in chapter 6 was the improved I_{ON}/I_{OFF} ratios. Self-aligned OTFTs and HVOTFTs had current ratios on the order of 10^5 - 10^6 (with a highest measured value of 1.21 x 10^6) and 10^4 - 10^5, respectively, whereas the previous thick and thin TIPS-pentacene devices had ratios on the order of 10^2 and 10^3, respectively. The improved current ratio was attributed to the additional thinning of the TIPS-pentacene due to the reduced volume of organic solution per transistor. This was described by equation 6.1. With the additional thinning of the organic layer, the gate contact increased its control over the gated region by minimizing the Ohmic currents in the semiconductor furthest away from the dielectric/organic interface. Furthermore, with transistor to transistor isolation with well defined channels, there was less unwanted leakage currents.

Saturation mobilities were measured to be equivalent to those of the thick TIPS-pentacene devices, with values of 9.12e-4 and 1.15e-3 $cm^2/V{\cdot}s$ for the OTFT and HVOTFT respectively. The highest measured mobility for a single self-aligned HVOTFT (W =250 μm, L = 10 μm and L_{offset} = 5 μm) was 5.96e-3 $cm^2/V{\cdot}s$. It is expected that further optimizing the crystallization of the TIPS-pentacene, either through optimized substrate heating, evaporation rate control or solvent additives, can further improve the mobility. The subthreshold swing was 0.56 an 0.76 V/dec for the OTFT and HVOTFT, respectively. Furthermore, for increasing L_{offset} lengths, onset to conduction V_X as well as the breakdown voltage V_{BD} became more negative while the I_{ON}/I_{OFF} ratios decreased.

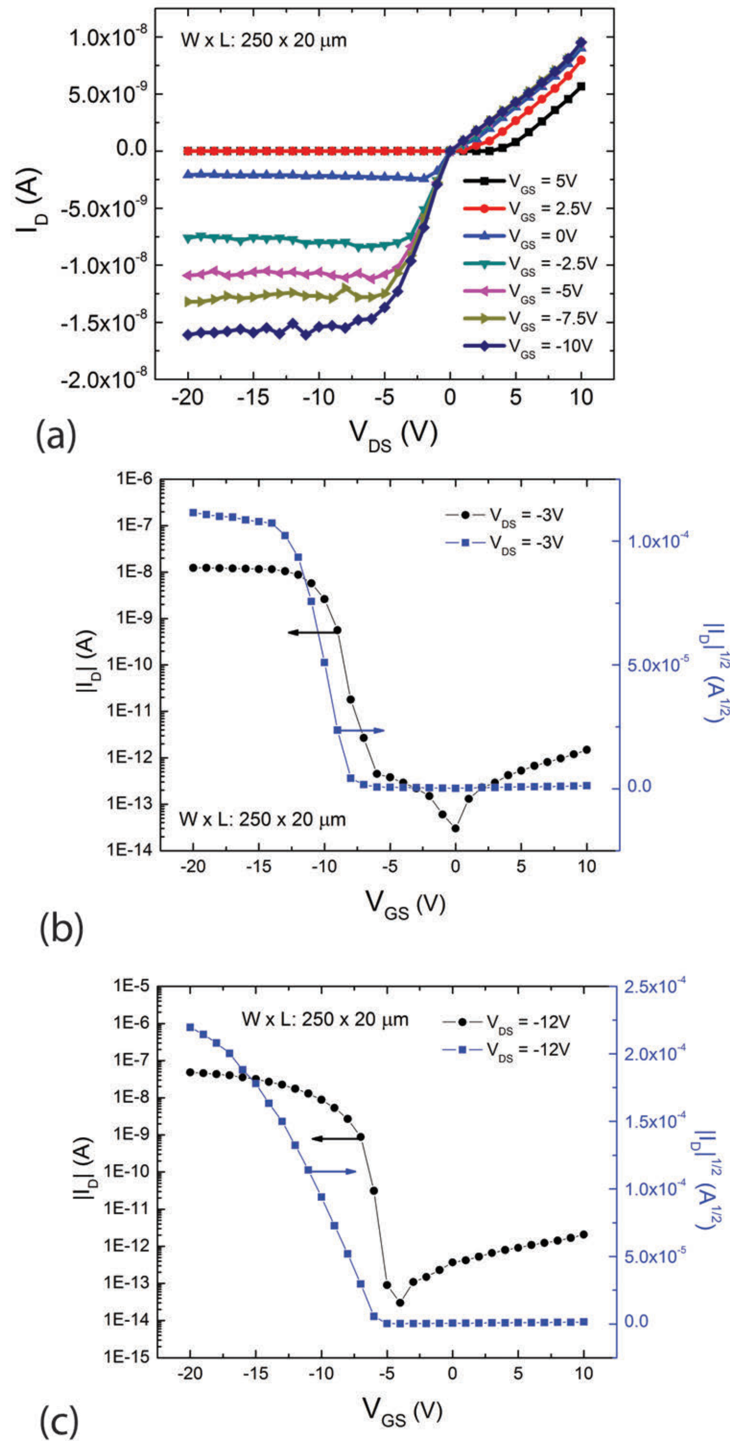


Figure 7-11: (a) Output, (b) linear transfer and (c) saturation transfer I-V characteristics of a self-aligned TIPS-pentacene OTFT (W = 250 μm, L = 20 μm) with PFDT and PFDTES SAMs.

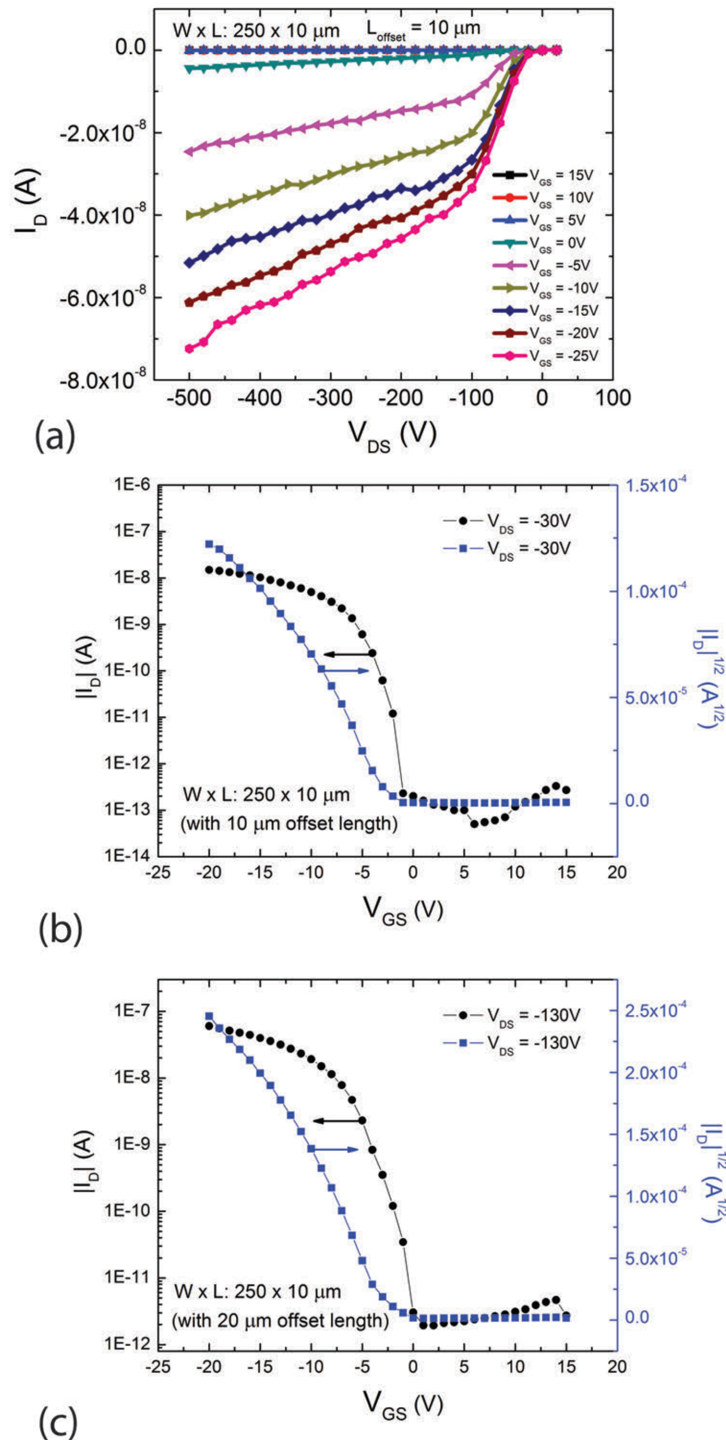


Figure 7-12: (a) Output, (b) linear transfer and (c) saturation transfer I-V characteristics of a self-aligned TIPS-pentacene HVOTFT (W = 250 μm, L = 20 μm) with PFDT and PFDTES SAMs. The breakdown voltage was $<$ -550 V.

Table 7.2: Electrical properties for self-aligned TIPS-pentacene OTFTs and HV-OTFTs.

Sample	I	II	III	IV	V
L_{offset}	0	5	10	20	30
Semi-conductor	TIPS-pen	TIPS-pen	TIPS-pen	TIPS-pen	TIPS-pen
Structure	OTFT	HVOTFT	HVOTFT	HVOTFT	HVOTFT
No. of Devices Tested	20	5	10	15	10
Substrate	Glass	Glass	Glass	Glass	Glass
Dielectric	BZN	BZN	BZN	BZN	BZN
t_{ox} (nm)	477	477	477	477	477
ϵ_r	29.3	29.3	29.3	29.3	29.3
E_{OT} (nm)	63.5	63.5	63.5	63.5	63.5
C_{ox} (F/cm^2)	5.44e-8	5.44e-8	5.44e-8	5.44e-8	5.44e-8
Field-Plate	None	None	None	None	None
SAM	PFDT / PFDTES	PFDT / PFDTES	PFDT / PFDTES	PFDT / PFDTES	PFDT / PFDTES
μ_{lin} (cm^2/V·s)	5.78e-4	6.05e-4	8.55e-5	3.50e-5	2.91e-5
μ_{sat} (cm^2/V·s)	9.12e-4	2.92e-3	1.05e-3	7.33e-4	1.44e-3
V_T (V)	-6.12	-4.15	-4.21	-1.55	-5.99
SS (V/dec)	0.56	0.47	0.57	1.40	0.71
I_{ON}/I_{OFF} (A/A)	333000	96000	23000	12000	15000
V_X (V)	2.60	-0.13	-4.91	-4.11	-5.55
V_{BD} (V)	$<$ -50	$<$ -400	$<$ -400	$<$ -450	$<$ -550
$I_{G,leak}$ (A)	-4.90e-13	-2.00e-9	-3.70e-10	-4.80e-12	-4.20e-9
W (μm)	250	250	250	250	250
L (μm)	[10, 20]	[5, 10, 20]	[5, 10, 20]	[5, 10, 20]	[5, 10, 20]

7.6 High-Field Effects in Self-Aligned TIPS-Pentacene HVOTFTs

Similar to the reliability test performed in section 6.4, the onset to conduction V_X was measured for the self-aligned HVOTFTs under increased V_{DS} bias ($V_{DS,Max}$). V_{DS} was swept from +50 V to an increasingly negative V_{DS} for V_{GS} values between +10 and -30 V. In this case, it was measured that all electrical parameters remained relatively constant as $V_{DS,Max}$ increased between -70 to -500 V, except for V_X, as shown in Fig. 7-13. It was found that V_X increased from -3.24 to -24.6 V. Furthermore, it was once again demonstrated that V_X could be returned to its original values by relaxing the V_{DS} bias, as shown in Fig. 7-14. In fact, the onset to conduction V_X appeared to be highly correlated with the max V_{DS}. This indicated that meta stable trap states, which only existed under high lateral fields, would impede charge injection from the gated region into the offset region [57].

Additional high-field effects were exhibited in the non-saturating behaviors in the output characteristics of the self-aligned HVOTFTs. In general, it was that found that the on state resistance (the inverse slope of the output characteristic in the saturation region) decreased for more negative V_{GS} values. For a typical HVOTFT, the on state resistances at V_{GS} = -10 and -30 V were 1.4e10 and 5.4e9 Ω, respectively. For the OTFT case, saturation characteristics were well behaved, with its on state resistance being largely invariant to V_{GS}. It is suggested that for the HVOTFT case, the current is limited by either the gated region of the offset region, depending on the amount of charge accumulation via the gate contact. At low V_{GS}, the current was limited by the gated region. However, at higher V_{GS}, charge accumulation increased and required significant charge injection from the gated region to the offset region. It is believed that this charge injection was the limiting factor, and resulted in progressive charge injection and reduction of the on state resistance of the offset region.

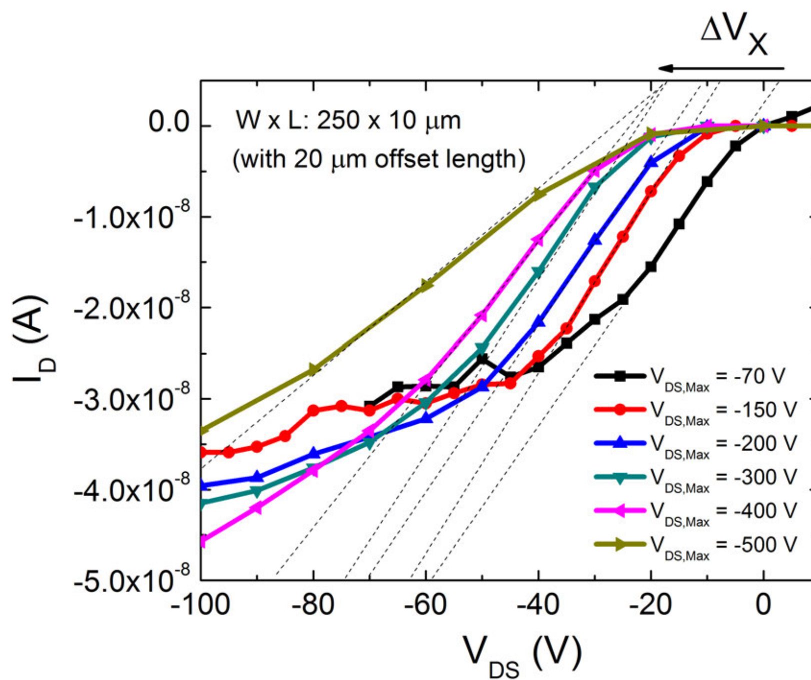


Figure 7-13: I-V output characteristics of a self-aligned TIPS-pentacene HVOTFT (W = 250 μm, L = 10 μm, L_{offset} = 20 μm) with PFDT and PFDTES SAM. Subsequent scans were performed at higher max V_{DS}, resulting in increased (more negative) onset to conduction V_X.

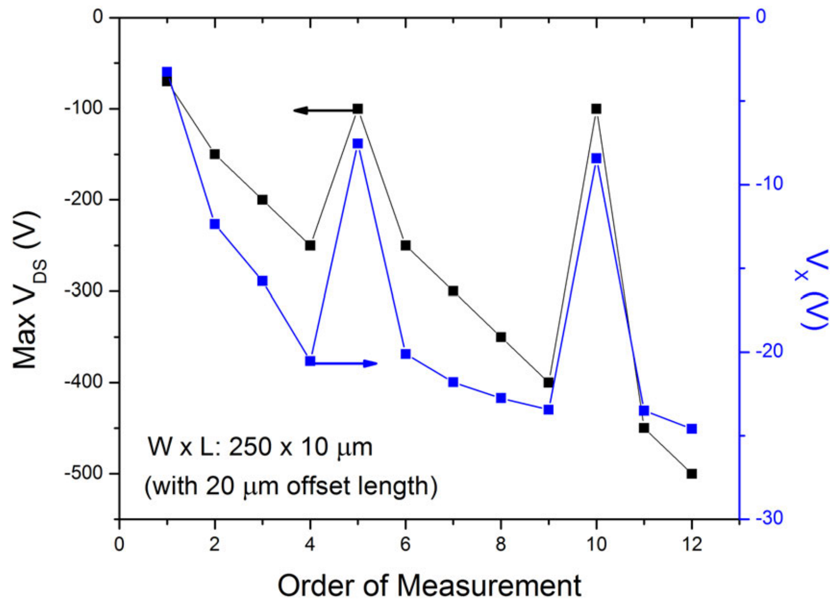


Figure 7-14: The Max V_{DS} plotted along side the V_X for a self-aligned TIPS-pentacene HVOTFT (W = 250 μm, L = 10 μm, L_{offset} = 20 μm) with PFDT and PFDTES SAM. V_X is highly correlate with the max V_{DS}.

7.7 Summary

Self-aligned TIPS-pentacene HVOTFTs, capable of driving voltages beyond -550 V, were successfully fabricated. The surface energies of various SAM treated materials as well as different fabrication processes were investigated to achieve a self-aligned patterning of the TIPS-pentacene without the use of conventional etching. This allowed for well defined regions of TIPS-pentacene to be directly deposited over the channel of the transistors, providing transistor to transistor isolation. Below is a summary of the findings of this chapter.

Self-Aligned TIPS-Pentacene OTFTs and HVOTFTs

- Surface energies were measured and calculated, using the Owens-Wendt, Wu and Neumann methods, for various SAM treated surfaces. BZN and parylene-

C had a surface energy of 46.07 and 28.70 mN/m, respectively. PFDT treated Au as well as PFDTES and PFDTMS treated BZN had surface energies of 18.82, 26.27 and 16.92 mN/m, respectively, well below the surface tension of anisole (35 mN/m).

- PFDT on Au and PFDTES on BZN were found to be stable under ethanol and acetone solvent conditions for up to 5 hours. However, the PFDT degraded completely after 10 minutes of heated NMP exposure.

- PFDT and PFDTES could be deposited sequentially onto samples with Au and BZN.

- A photoresist mask was used to protect the channel of the transistors from SAM treatments, allowing for a distinction between high and low surface energy regions.

- Heating the organic solution prior to drop casting resulted in reduced cohesive forces and surface tension, rending the self-aligned process not feasible.

- Heating the substrate on a 50 °C hot plate prior to drop casting proved effective in growing TIPS-pentacene with a full coverage within the SAM pattern.

- The Ra and Rms surface roughness of the TIPS-pentacene grown on the heated substrates were 3.49 and 4.56 nm, respectively.

- Bottom gate / top contact self-aligned TIPS-pentacene HVOTFTs were fabricated with the use of a single SAM treatment of the oxide and a shadow mask for the source/drain contacts. However, devices did not exhibit any FET characteristics.

- Bottom gate / bottom contact self-aligned TIPS-pentacene HVOTFTs were successfully fabricated with PFDT and PFDTES SAM treatment. Devices exhibited well-behaved FET characteristics.

- Self-aligned TIPS-pentacene HVOTFTs with offset lengths of 20 and 30 μm had breakdown voltages beyond -550 V while having a relatively low threshold voltage between -1 and -6 V.

- Saturation mobility varied between 10^{-5} and 10^{-3} cm^2/V·s.

- I_{ON}/I_{OFF} current ratios were significantly improved compared to TIPS-pentacene devices in the previous chapter, reaching values of 10^6 A/A.

- The onset to conduction V_X varied with the max V_{DS} applied during measurement. However, V_X could be returned to its original values by relaxing the max V_{DS}.

- The on state resistance of self-aligned HVOTFTs decreased with more negative V_{GS}, suggesting drain induced barrier lowering.

Chapter 8

Conclusion

8.1 Major Findings

The development of a high-voltage organic thin film transistor (HVOTFT) capable of driving large output voltages ($|V_{DS}| > 100$ V) while being controlled by a relatively small input voltage ($|V_{GS}| < 50$ V) enables novel applications, beyond traditional liquid crystal displays, such as electrophoretic displays, digital x-ray imaging, photovoltaic systems-on-glass and integration with electrostatic MEMS actuators, all built on arbitrary and flexible substrates. The HVOTFT has the potential to compliment Si MOSFETs, among others, in enabling a truly-ubiquitous electronics world. Analogous HVTFTs based on inorganic semiconductors have been developed sparingly over the years. However, to the best of our knowledge, there was no effort prior to this work on developing an organic-based HVOTFT. Such an HVOTFT would benefit from the organic semiconductor's affinity for flexibility as well as its ability to be solution-processed at room temperature and air ambient conditions.

In this dissertation, a technology platform was developed for the design, fabrication and characterization of pentacene and TIPS-pentacene HVOTFTs. Several key topics played an important educational role, for example the integration of reactive sputtered high-k dielectrics, analysis of x-ray diffraction patterns, development of flexible electronics on polyimide substrates, solution-processing of organic semiconductors, modification of surface properties via self-assembled monolayers, surface

energy calculations via contact angle measurements, electrical property extraction, device modeling, and mask design, among others.

The dissertation was structured to achieve three overarching goals: the development of a vacuum deposited HVOTFT, a solution-processed HVOTFT, and a self-aligned solution-processed HVOTFT. The three devices culminated in novel fabrication processes for fabricating HVOTFTs that are able to drive voltages beyond -550 V while achieving on/off current ratios of 10^6 A/A. The major findings from this dissertation are summarized below.

8.1.1 Vacuum-Deposited Pentacene HVOTFTs

Vacuum-deposited pentacene HVOTFTs were first fabricated due to the relative ease of depositing pentacene layers having thicknesses of around 20 nm by thermal evaporation. A dual channel architecture was adopted, which included a gated region for charge control capabilities and an offset region for high-voltage accommodation. The offset region successfully increased the breakdown voltage from approximately -100 V to -550 V, a first for organic thin film transistors. In fact, the breakdown voltage could be engineered directly by increasing the length of the offset region which reduces the effective electric field across the dielectric. This demonstrated the feasibility and practicality of an organic-based HVOTFT that could enable flexible MEMS integration on the TFT technology platform.

Additional findings related to the fabrication process of the HVOTFT include the pentacene deposition rate dependent mobility and the low threshold voltage via high-k BZN. Firstly, the deposition rate of pentacene was shown to be critical in promoting the coalescence of the pentacene molecules after surface adsorption, promoting larger grains and higher mobility. Secondly, the choice of the dielectric played an integral role in the threshold voltage as well as the quality of the dielectric/semiconductor interface. High-k BZN (k $\approx$ 25-50) and low-k parylene-C (k $\approx$ 3.15) were used as the dielectric, with the BZN largely out-performing the organic dielectric. Significantly lower threshold voltages of -0.77 V, gate leakage currents of -2.05e-11 A and subthreshold swings of 1.58 V/dec, as well as higher mobilities 7.45e-3 $cm^2/V{\cdot}s$ and

I_{ON}/I_{OFF} current ratios 26000 A/A, were measured for BZN-based devices. It was suggested that the parylene-C was of low quality and that a large density of traps lead to poor electrical properties.

BZN is a unique high-k cubic pyrochlore dielectric material, with reported dielectric constants as high as 200 after high temperature annealing. BZN was deposited via reactive RF magnetron sputtering, with its crystallinity and stoichiometry examined under XRD and XPS. It was found that there was an optimal ratio of reactive gas species (Ar and O_2) to achieve appropriate sputtering rates of the Bi, Zn and Nb elements as well as to obtain Bi-O, instead of metallic Bi. Bi-O bonds were necessary for a high-k α-phase cubic pyrochlore dielectric. As-sputtered BZN was measured to have a dielectric constant between 25 and 50.

A top field plate was also explored through numerical simulations and fabricated to assess its ability to control the charge carrier distribution within the channel of the HVOTFT, particularly at the interface between the gated and offset regions. From the numerical simulations, it was shown that a field plate could accumulate additional charge carriers in the channel, increasing the overall drain current and improving the onset to conduction V_X, a parameter that was defined as the necessary V_{DS} to achieve large I_D. Additionally, the electric field inside the channel could be reduced. It is suggested that a reduction in the electric field peak at the interface between the gated and offset regions could reduce the generation of stress induced meta stable trap states, responsible for the large V_X seen in HVOTFTs. Simulations also showed that increasing the size of the field plate had a detrimental effect on the breakdown voltage as the electric field across the top dielectric was increased. Thus, an ideal field plate would be relatively small in size to avoid early breakdown, and would be biased appropriately to reduce channel electric field and increase charge carrier accumulation. However, fabricated HVOTFTs with top field plates behaved differently from numerically simulated HVOTFTs. When the field plate was biased, it dictated the conduction within the channel, with additional gate bias not contributing to the FET characteristics. There was no observed improvements in drain current or onset to conduction V_X.

8.1.2 Solution-Processed TIPS-Pentacene HVOTFTs

Although the vacuum-deposited pentacene HVOTFTs performed nominally, its low mobility and its inability to be solution-processable lead to the development of the solution-processed TIPS-pentacene HVOTFTs, fabricated using a self-shearing drop cast method. TIPS-pentacene favors a 2D face-to-face stacking, as opposed to face-to-edge found in pentacene, increasing the π-orbital overlap between molecules and the hopping transport mechanism. Thus, high mobility has been routinely observed in TIPS-pentacene devices [129]. Furthermore, the ability to be solution-processed allows for cheap fabrication which removes the need for high temperature and high vacuum processes.

TIPS-pentacene was dissolved in anisole at 2 wt%, with the organic solution drop casted onto a slanted (4.5°) and heated substrate (50 °C). Several different solvents were used for drop casting; however, the high boiling point anisole proved the most effective in depositing TIPS-pentacene that fully covered the sample. The slant of the sample provided a preferential growth direction of the TIPS-pentacene, with nucleation and crystallization occurring under a self-shearing condition at the top liquid/air interface. The heated substrate, on the other hand, improved crystallization, resulting in large crystal bands of TIPS-pentacene of at most 3 mm in width with average surface roughness of 0.1533 nm. Furthermore, it was observed that highly organized plateaus of 1-2 nm in height were stacked on top of each other, resulting in TIPS-pentacene growing to thicknesses of 0.5 to 3 μm.

XRD analysis of TIPS-pentacene showed sharp (00l) diffraction peaks, indicating a highly oriented crystal packing and high crystallite dimensions. However, TIPS-pentacene grown on parylene-C resulted in characteristic diffraction doublets of equal intensity at low 2θ. Due to the low surface energy of parylene-C and its interaction with the relatively higher surface tension of the anisole solvent, it was suggested that strain was induced during the crystallization of the TIPS-pentacene. Both compressive and tensile strain would vary the inter-planar d_{hkl} spacing and would account for the symmetrical doublet, centered around the original (00l) peaks. Additional drop casting experiments were performed on other low surface energy materials. TIPS-

pentacene on SiO_2 also exhibited diffraction doublets. However, TIPS-pentacene grown on extremely low surface energies samples such as organosilane SAM treated glass or BZN (< 26 mN/m) lead to extreme dewetting of the organic solution droplet. This induced an outward pointing force acting on the solute which crystallized along the liquid/air interface instead of the liquid/solid interface, forming a 3D hollow structure. In these cases, diffraction doublets were not observed, suggesting that the lack of TIPS-pentacene/parylene-C interface relaxed the organic crystal during growth.

Solution-processed TIPS-pentacene OTFTs and HVOTFTs were fabricated with a SAM treatment to improve charge carrier injection from the Au metal to the organic semiconductor. Particularly, fluorinated organothiols such as PFDT and 4-FTP reduced the hole injection barrier via a surface dipole moment. Increased carrier injection would lead to the filling of trap states, resulting in improved carrier mobility as well as the I_{ON}/I_{OFF} current ratios. PFDTES, an organosilane SAM, was also introduced to reduce the overall surface energy of the sample seen by the organic solution. With a PFDTES treatment, the organic solution quickly sheared across the surface sample, resulting in thin depositions (< 100 nm) of TIPS-pentacene. Although the initial thick TIPS-pentacene HVOTFTs had marginal electrical properties including a breakdown voltage of -150 V, the thin TIPS-pentacene HVOTFTs fabricated on top of PFDTES resulted in improved I_{ON}/I_{OFF} current ratios and leakage current $I_{G,leak}$. Furthermore, the breakdown voltage was significantly improved to -450 V, indicating that there was an optimal thickness needed for solution-processed transistors.

The reliability of the HVOTFT was also investigated under high stress biasing. In particular, the onset to conduction V_X became more negative under increasing max V_{DS} biasing. V_X is related to the impedance of charge injection from the gated to offset region and arises from meta stable trap states being generated under high field stress. However, it was shown that by relaxing the max V_{DS} for subsequent measurements, V_X returned to its original value.

Finally, solution-processed HVOTFTs were also fabricated on flexible Kapton polyimide substrates operating at bending radii of up to 25 mm. This demonstrated the first instance of a flexible HVOTFT specifically designed for high-voltage opera-

tion.

8.1.3 Self-Aligned TIPS-Pentacene HVOTFTs

Issues arose with the performance of the solution-processed HVOTFTs, particularly concerning their low I_{ON}/I_{OFF} current ratios. A lack of transistor to transistor isolation due to their incompatibility with traditional solvents as well as the thick TIPS-pentacene layers were to blame. A novel fabrication process was then devised to tackle these issues, and involved a series of SAM treatments. Organothiol and organosilane SAMs were deposited sequentially on areas outside of the channel region, which was protected by a patterned photoresist layer. This created distinct wetting and dewetting regions, allowing the droplets of the organic solution to self-aggregate towards the channel. A series of surface materials with and without SAM treatments were investigated by calculating their surface energy to see which combination would result in the dewetting of anisole. It was found that PFDT on Au as well as PFDTES and PFDTMS on BZN were successful in reducing the surface energy of their respective materials below the value of anisole's surface tension. Thus, when anisole would be dropped onto the SAM treated surfaces, a high contact droplet would be formed until the droplet moved into a non SAM treated region. This self-aligned solution process resulted in patterned TIPS-pentacene layers without having to use traditional lithography and etching processes.

The self-aligned TIPS-pentacene HVOTFTs performed much better than the previous generation of solution-processed devices and were also generally more well-behaved. Most notably, the I_{ON}/I_{OFF} current ratios increased from 10^2 - 10^3 to 10^6 A/A due to the additional thinning of the TIPS-pentacene layer and transistor to transistor isolation. Furthermore, the breakdown voltage was measured to be around -550 V.

It was also suggested that by controlling the dewetting area in which the organic solution would aggregate, one could control the growth pattern, direction and thickness of the TIPS-pentacene layers. Thus, additional thinning of the organic semiconductor layer or highly oriented grains grown in long rectangular SAM patterns

can be achieved.

8.2 Future Work

This dissertation presents the first ever solution-processed high-voltage organic thin film transistor with breakdown voltages beyond -550 V while having a low threshold voltage between -1 and -10 V. Although the development of such an electronic device could enable flexible MEMS integration, among other high-voltage applications, many more improvements must be made before adoption of the HVOTFT.

8.2.1 Improvements in Mobility

A common narrative among organic semiconductor devices is the relatively low mobility. High mobilities in HVOTFTs is desirable to improve switching speeds, for example. It was only recently that organic FETs started to surpass the a-Si:H TFT used in LCDs, with values above 1 $cm^2/V{\cdot}s$ now routinely measured in academic research. Although using TIPS-pentacene over pentacene improved the carrier mobility marginally in the HVOTFTs, additional approaches or alternative semiconductors are needed to further this trend. For example, Chae et al. used high boiling point solvent additives such as diphenyl ether (DPE) and chloronaphthalene (CN) to induce the formation of well-ordered crystalline domains as well as to reduce the contact resistances [129]. It was suggested that the additives promoted self-assembly and the formation of elongated crystalline domains due to slower evaporation rates of the solvent mixture, resulting in mobilities of 0.7 $cm^2/V{\cdot}s$.

Additionally, work by Choi et al. presented spin coated TIPS-pentacene OTFTs with a dewetting amorphous fluoropolymer (CYTOP) and HMDS surface treatments used to confine the organic solution above the channel. By controlling the rate of spin coating, a balance of centrifugal and dewetting forces promoted the growth of highly ordered crystal grains, resulting in OTFTs with mobilities on the order of 10^{-1} $cm^2/V{\cdot}s$.

Wade et al. took a different approach and investigated the structural anisotropy of

TIPS-pentacene and its effect on charge transport [100]. Using a zone-cast deposition method and by controlling the molecular alignment relative to the channel, they were able to optimize the mobility when the crystal bands were oriented ≈35° relative to the channel length. Such an orientation could be controlled by using a self-aligned self-shearing drop cast method in which a long rectangular SAM pattern is oriented at an angle with the channel length.

Moreover, unique polymer blends have also been of interest. Hamilton et al. combined high mobility small molecules with polymers that typically lead to device uniformity [162]. They successfully blended TIPS-pentacene as well as 2,8-difluoro-5,11-bis(triethylsilylethynyl)anthradithiophene (dif-TESADT) with either poly(α-methyl styrene) or poly(triarylamine) (PTAA) for improved mobilities of 0.5 $cm^2/V{\cdot}s$. High mobility was attributed to the vertical segregation and uniformity of the TIPS-pentacene. The choice of solvents also plays an important role in phase segregation of TIPS-pentacene, as was discussed by Hwang et al [163].

8.2.2 Improvements in HVOTFT Integration, Design and Flexibility

Further works on HVOTFT integration are needed to improve the device's electrical properties and its potential for flexible applications. For one, designs on extending the offset length and/or adding a source-side offset length should be conducted in the context of improving the breakdown voltage while maintaining a high on/off current ratio as well as minimizing non-ideal I-V characteristics. It was shown that increasing the offset length was effective in increasing the breakdown voltage by reducing the electric field across the dielectric, between the drain and the gate contacts. However, it is unclear to which point the breakdown voltage can be enhanced through this method alone without having detrimental effects on mobility and I_{ON}/I_{OFF} current ratios. Secondary gates, field plates, asymmetric dielectrics between the gated and offset regions may be explored as alternative designs to improve the breakdown voltage.

Additionally, identifying the most optimal dielectric material is needed to obtain

not only higher breakdown voltages and lower threshold voltages, but also increased mobility. It has been shown that the dielectric/organic interface plays a pivotal role in charge carrier dynamics [109]. Here, a parylene-C/BZN dual stack dielectric was used in an attempt to reduce the effects of large surface dipole moments inherent in high-k materials; however, electrical performance deteriorated in fabricated HVOTFTs, due to low quality parylene-C films. Other dual dielectric combinations need to be investigated for high performance HVOTFTs. Furthermore, the breakdown field of the dielectric can also be optimized. BZN has a reported dielectric strength of 5 MV/cm, half that of SiO_2 or Si_3N_4 with 10 MV/cm [104]. Parylene-C is cited to have 2.68 MV/cm. Insulators with a higher dielectric strength would prevent early onset of breakdown and enable the HVOTFT to drive at larger voltages.

The 2D numerical simulations of a field plated HVOTFT and the literature reports of field plates for HVTFTs were promising, not in improving the breakdown voltage, but in reducing the onset to conduction V_X [57], [75]. However in practice, developing a field plate proved difficult. Additional understanding and optimization of the threshold voltage requirements for the gate and the field plate structures are needed to assess how best to use the field plate. Moreover, the thickness differences of adjacent crystal bands of TIPS-pentacene or its large coffee stain borders made it difficult to form a continuous top field plate. Alternative designs are needed to be able incorporate a field plate with the current HVOTFT structures for improved I-V characteristics.

Finally, although preliminary experiments have showcased flexible HVOTFTs on Kapton polyimide substrates, current HVOTFTs have yet to be demonstrated to be on par with state-of-the-art flexible OTFTs with bending radii below 10 mm. Yang et al. reported a pentacene OTFT operating at a bending radius of 8 mm where the field-effect mobility varied due to a bending-stress-driven phase transition between the bulk phase and the thin film phase [164]. Flexible TIPS-pentacene OTFTs have also been fabricated by, for example, Yu et al. in the context of a flexible ammonia gas sensor operating at a bending radius of 2.5 mm [165]. The organic semiconductor's suitability for flexible conditions make it an ideal material system candidate for

ubiquitous electronics and should be explored in detail.

8.2.3 Improvements in Solution-Processing

As mentioned in chapter 1, there are several solution-processing methods that may be employed to grow organic semiconductor crystals. Zone casting, ink-jet printing and solution shearing have been used with great success in growing highly oriented grains for high mobility OFETs [49]. However, the simplicity of a simple self-shearing drop cast method was used for the fabrication of the HVOTFT. Future works to incorporate different solution-processing methods should be performed to have a finer control of the grain growth. Furthermore, environmental control during solution-processing should be conducted to avoid trap generation due to moisture. For example, drop casting within a nitrogen environment as opposed to air ambient could help reduce the density of traps and increase carrier mobility.

A major contribution of this dissertation is the development of a self-aligned solution-processed method which can be further optimized to grow larger, more oriented and more uniform crystal grains. For instance, a Marangoni flow process, in which the organic solution is comprised of a major and minor solvent, can reduce the "coffee stain". Initial nucleation at the liquid/air interface pins the contact line at the evaporation front, resulting in a capillary flow of the liquid outwards from the center [54]. This leads to a disproportional amount of crystallization occurring at the contact line. However, a two solvent solution can facilitate a Marangoni flow which can recirculate the solute back towards the center of the solution, leading to a more uniform crystallization of the organic solute. The differences between the boiling point as well as the surface tension of the two solvents dictate the direction of the Marangoni flow [54]. A modified Marangoni flow could also be used in the self-shearing drop cast method developed for the HVOTFT. Due to the gravitational flow of the organic solution induced by the slanted sample, larger amounts of TIPS-pentacene was deposited at the bottom of the sample. However, if a Marangoni flow is engineered to flow up the slant, uniform deposition could occur. With anisole being the major solvent, the minor solvent would need a boiling point and surface

tension that is either both higher or lower than that of anisole to induce an upwards Marangoni flow. For example, toluene could be used as the minor solvent.

Currently, self-aligned SAM patterns resulted in a quasi-square or droplet formation of TIPS-pentacene. Additional experiments should be done with vastly varying SAM patterns to optimize and understand the crystal grain growth dynamics. For example, a very long rectangle can induce growth directions along the long axis, as was suggested by observing the reduction of the anisole volume at the short edge during evaporation. Such a SAM pattern could force the grains to grow along the long axis, giving control over the direction of the grains relative to the channel. Furthermore, it was also discussed how the volume of the organic solution that aggregated over the wetting regions can be controlled by the area of the SAM pattern. Thus, a scheme to control the volume of the organic solution per transistor would translate to the control of the thickness of the deposited layers, leading to a higher degree of control over the FET capabilities of the HVOTFT.

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Appendix A

Material Characterization

A.1 Techniques for Material Characterization

The quality of the materials used was vital in obtaining high performing electronic devices. Here, we discuss the material characterization tools and methods used.

A.1.1 X-Ray Diffraction(XRD)

X-ray diffraction (XRD) is a method to determine the crystallographic information of a material using x-rays (primarily Cu K-α). Crystal structure, phase composition, unit cell and Bravais lattice parameters (a, b, c, α, β, γ), inter-planar spacing (d_{hkl}), crystallite size as well as strain can be determined from XRD measurements. A schematic of scattering and diffraction is shown in Fig. A-1.

When x-rays are incident on a sample, they scatter due to the sample's periodic lattice crystal. A diffraction pattern occurs through destructive and constructive interference, given by Bragg's law:

$$2d_{hkl} \sin\theta = n\lambda \tag{A.1}$$

where d_{hkl} is the vertical atomic spacing between diffracting planes, θ is the incident angle of the x-ray, n is an arbitrary integer, and λ is the x-ray wavelength. Knowing the crystal system under investigation a priori (triclinic for pentacene and TIPS-

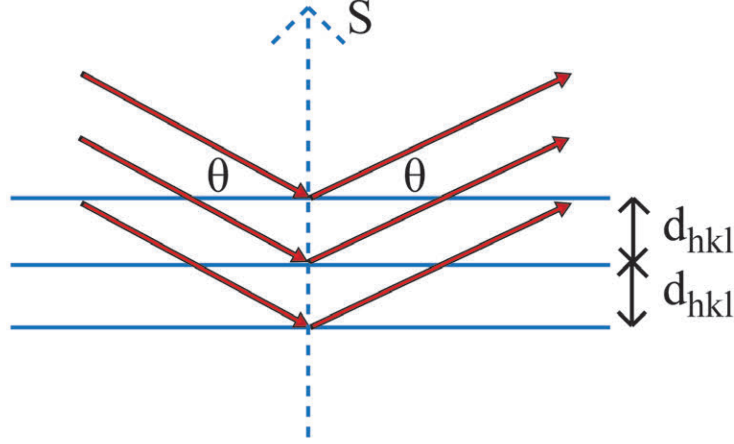

Figure A-1: Incident and scattered x-rays due to crystal planes separated by d$_{hkl}$ where s is the diffraction vector that bisects the angle between the incident and diffracted x-ray beam.

pentacene), d$_{hkl}$ and unit cell parameters can be extracted using:

$$\frac{1}{d_{hkl}^2} = \frac{1}{V^2}(S_{11}k^2 + S_{22}k^2 + S_{33}l^2 + 2S_{12}hk + 2S_{23}kl + 2S_{13}hl) \tag{A.2}$$

$$S_{11} = b^2c^2\sin^2\alpha \tag{A.3}$$

$$S_{22} = a^2c^2\sin^2\beta \tag{A.4}$$

$$S_{33} = a^2b^2\sin^2\gamma \tag{A.5}$$

$$S_{12} = abc^2(cos\alpha\ cos\beta - cos\gamma) \tag{A.6}$$

$$S_{23} = a^2bc(cos\beta\ cos\gamma - cos\alpha) \tag{A.7}$$

$$S_{13} = ab^2c(cos\gamma\ cos\alpha - cos\beta) \tag{A.8}$$

where V is the unit cell volume. The detector records and plots intensity I$_{hkl}$, the amount of x-rays scattered from the sample at various source and/or detector angles relative to the surface. The intensity is proportional to the material structure factor F$_{hkl}$, the sum of the scattering factor for reach atom in the unit cell:

$$I_{hkl} \propto |F_{hkl}|^2 \tag{A.9}$$

$$F_{hkl} = \sum_{j=1}^{m} N_j f_j exp(2\pi i(hx_j + ky_j + lz_j)) \tag{A.10}$$

where N_j is the fractional equivalent position occupied by atom j in the unit cell, f_j is the scattering factor, (hkl) is the crystal plane, and $x_j y_j z_j$ is the fractional coordinates of atom j.

A Rigaku Smartlab Multipurpose Diffractometer (9 kW rotating anode x-ray source) was used in an out-of plane coupled parallel beam (PB), and in-plane grazing incidence x-ray diffraction (IP-GIXD) configurations. The configurations are shown in Fig. A-2. Under PB XRD, both source and detector rotate equally around the sample, with the diffraction vector s being normal to the surface of the sample. A parallel x-ray beam was generated, as opposed to a diverging beam used in a Bragg Brentano configuration, to have better insensitivity to rough surfaces or height sample differences, as is the case for drop casted TIPS-pentacene. Under IP-GIXD, on the other hand, only the detector was rotated around the sample while the x-ray source was kept at a low incident angle. This limits the penetration depth of the x-ray and minimized substrate diffraction, particularly if the incident angle is below the critical angle for internal reflection. Penetration depth t is estimated as:

$$t = \frac{4.61}{2\mu} \sin\alpha \tag{A.11}$$

where α is the incident angle of the x-rays and μ is the linear absorption constant of x-rays of the material. Furthermore, under in-plane configuration, the scattering vector s is parallel to the sample surface, allowing the measurement of crystal planes perpendicular to those from the out-of-plane configuration.

A.1.2 X-Ray Photospectroscopy (XPS) and Energy-Dispersive X-Ray Spectroscopy (EDS)

X-ray photospectroscopy (XPS) and energy-dispersive x-ray spectroscopy (EDS) are quantitative techniques to determine the elemental composition, chemical state and electronic state of sample. The two techniques differ mainly in the penetration depth

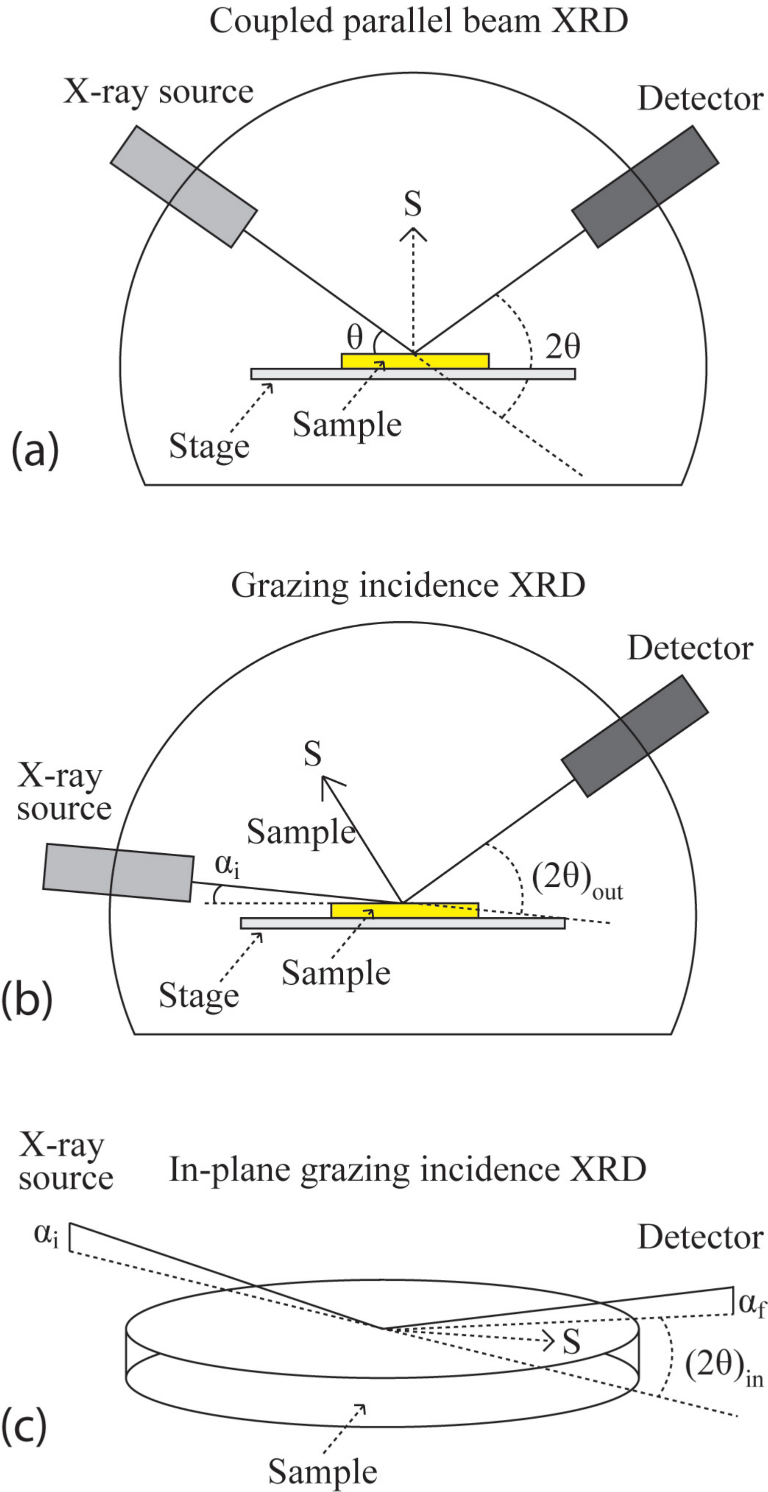

Figure A-2: (a) Coupled parallel beam XRD. (b) Grazing incidence XRD. (c) In-plane grazing incidence XRD.

and the source of signal for the detector. Whereas XPS is mainly a surface analysis tool analyzing ejected electrons, EDS investigates the bulk via characteristic x-rays.

For XPS, a monochromatic x-ray (generated via an electron emitter and a monochromater) is incident on the surface sample, resulting in the photoemission of electrons. These electrons are passed through focusing apparatuses and an energy selector, to be finally measured by an electron energy detector, as shown in Fig. A-3. The electron binding energy $E_{binding}$ is measured, indicating which elements are present at the material surface. The binding energy is given by:

$$E_{binding} = E_{photon} - (E_{kinetic} - \phi) \tag{A.12}$$

where E_{photon} is the x-ray photo energy, $E_{kinetic}$ is the kinetic energy of the electron measured, and ϕ is the work function associated with the material and the detector. A relative sensitivity factor (RSF) is used to correct the signal intensity, resulting in atomic percentages for each present element.

A Physical Electronics Versaprobe II X-ray Photoelectron Spectrometer from the Center of Materials Science and Engineering (CMSE) at MIT, with its schematic diagram in Fig. A-3, was used for elemental composition analysis, particularly for BZN. In-situ argon etching was also performed for depth profiling.

For EDS, characteristic x-rays are emitted from the sample due to the de-excitation of core electrons created by an incident electron beam. As high energy electrons impinge on an elemental atom, electrons are ejected from their core shells, resulting in a higher orbital electron relaxing and releasing a characteristic x-ray. It is this characteristic x-ray that is used to do elemental composition analysis.

A JEOL 6610LV SEM with a built in JED-2300 EDS module from the department of materials science and engineering (DMSE) was used.

A.1.3 Scanning Electron Microscopy (SEM)

Scanning electron microscopy (SEM) generates high resolution images by detecting secondary electrons emitted by the sample's atoms when excited by a focused incident

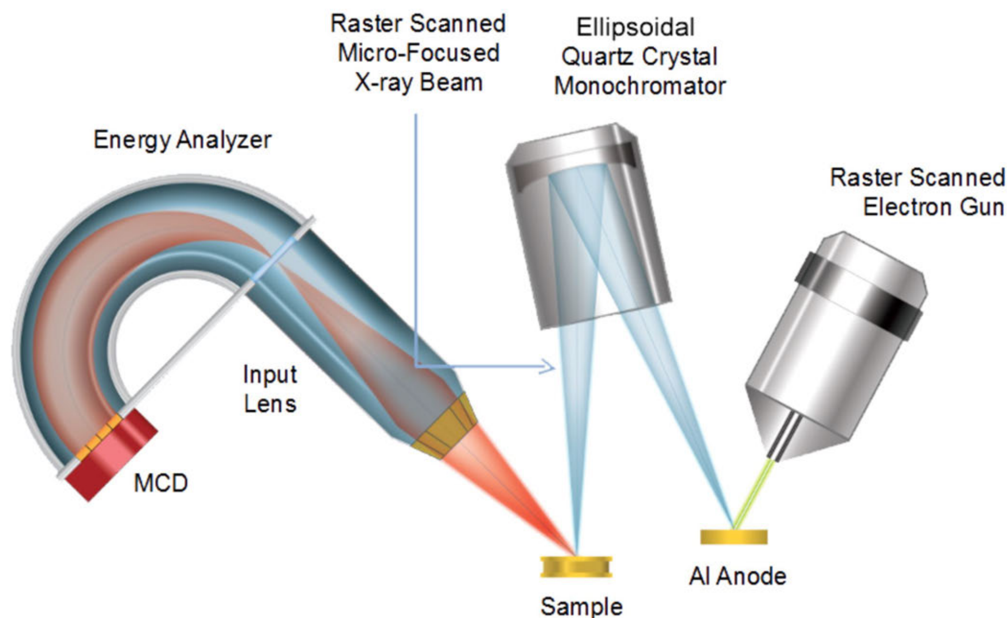

Figure A-3: Schematic for x-ray photospectroscopy [166].

electron beam. The scanning electron micrographs were obtained using a Hitachi TM3000 TableTop SEM (5 kV and 15 kV modes).

A.1.4 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a high resolution imaging tool producing topography images and surface roughness measurements by raster scanning the surface of the sample with a semiconductor tip. The forces between the sample and a semiconductor tip are converted to height measurements. An Agilent 5500 AFM tool was used.

A.1.5 Contact Angle Goniometer

A goniometer is used to measure the contact angles between selected liquid droplets and the surface of the sample. Contact angles determine the surface energy of the sample, given the surface tension of the test liquids. Here, surface energy and surface tension refer to a solid and liquid, respectively. Surface energy is the sum of the intermolecular forces present at the surface of a solid and represents the attractive

or repulsive forces of the solid onto another material. For example, a low surface energy solid typically results in poor wetting of a liquid while a high surface energy solid tends to attract other materials. Surface energy and the difference between it and the surface tension of the solvent used in solution-processing proved important in controlling the wetting regions as well as the thickness of the semiconductor.

Although the surface tension of a liquid γ_{LV} (between the liquid-gas phase) is well defined and can be measured, the surface energy of a solid γ_{SV} (between the solid-gas phase) is not. In fact, γ_{SV} cannot be measured directly due to the solid's ability to resist deformation. γ_{SV} must then be calculated using Young's equilibrium equation:

$$\gamma_{SV} - \gamma_{LS} = \gamma_{LV} \cos\theta \tag{A.13}$$

where γ_{LV} is the surface tension of the liquid, γ_{LS} is the surface tension between the liquid and solid phases, γ_{SV} is the surface energy of the solid, and θ is the contact angle made between liquid and the solid, shown in Fig. A-4 [167]. The liquid surface tension and the contact angle are known and measured, respectively. However, additional information is required to solve for both γ_{SV} and γ_{LS}. Different models have been used to approximate the relationship between solids and liquids [167]. As part of this dissertation, three surface energy methods are used: Neumann, Owens-Wendt (geometric mean) and Wu (harmonic mean).

The Neumann method utilizes contact angle data form a single liquid, and gives an empirical fitting parameter β which tends to be decent for low energy surfaces [167] Although convenient, the reliance on a single liquid means that the measurement is highly affected by the choice of solvent. The Neumann method is summarized by:

$$(1 + \cos\theta)\gamma_{LV} = 2\sqrt{\gamma_{SV}\gamma_{LV}}e^{-\beta(\gamma_{LV} - \gamma_{SV})} \tag{A.14}$$

$$\beta = 0.0001247 \tag{A.15}$$

For the Owens-Wendt method, the surface energy/tension can be defined as the sum of two forces at play: the dispersive (London-van der Waals bonds) and polar

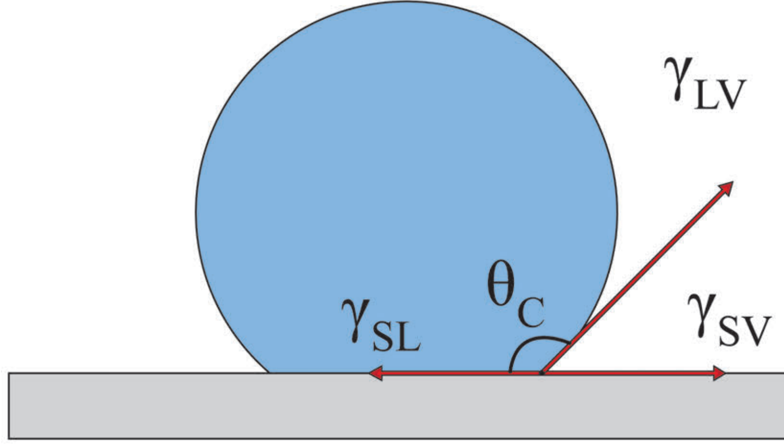

Figure A-4: Contact angle between a liquid droplet and solid surface.

(hydrogen bonds) components. The method also utilizes two liquids and is typically the method of choice. The equations for the Owens-Wendt method are:

$$(1+\cos\theta)\gamma_{LV} = 2\sqrt{\gamma_{SV}{}^{D}\gamma_{LV}{}^{D}} + 2\sqrt{\gamma_{SV}{}^{P}\gamma_{LV}{}^{P}} \tag{A.16}$$

$$\gamma_{SV} = \gamma_{SV}{}^{D} + \gamma_{SV}{}^{P} \tag{A.17}$$

$$\gamma_{LV} = \gamma_{LV}{}^{D} + \gamma_{LV}{}^{P} \tag{A.18}$$

where γ^D and γ^P are the dispersive and polar component of the total surface energy/tension, respectively [168].

An alternative method to the Owens-Wendt method is the Wu method which uses a harmonic mean instead of a geometric mean [169].

$$(1+\cos\theta)\gamma_{LV} = 4\left(\frac{\gamma_{SV}{}^{D}\gamma_{LV}{}^{D}}{\gamma_{SV}{}^{D}+\gamma_{LV}{}^{D}} + \frac{\gamma_{SV}{}^{P}\gamma_{LV}{}^{P}}{\gamma_{SV}{}^{P}+\gamma_{LV}{}^{P}}\right) \tag{A.19}$$

A Ramé-Hart 260 contact angle goniometer was used to measure the static contact angles of 10 μL of DI water and ethylene glycol on various material surfaces, discussed in chapter 7.

Appendix B

Additional Fabrication Details

B.1 Summary of Photomasks

The photomasks used in the fabrication of the OTFTs and HVOTFTs are described in detail here. An overlay of the 5 inch photomasks is shown in Fig. B-1.

B.1.1 Gate Mask

Fig. 4-2 (a) shows the gate mask used to pattern the initial chromium/gold stack, defining the gate as well as the contact pads for the source, drain and gate. As the gate mask was the first in the fabrication process, it also defined the alignment markers and resolution checks, shown in Fig. B-2

B.1.2 Via Mask

The via mask defined the openings above the contact pads. The dielectric exposed in these regions were etched away. The vias allowed for proper anchoring of the source and drain metal contacts, as well as access to the gate metal contact, as shown in Fig. 4-2 (b). They were designed to be 20% smaller than the anchoring pads, accommodating for misalignment.

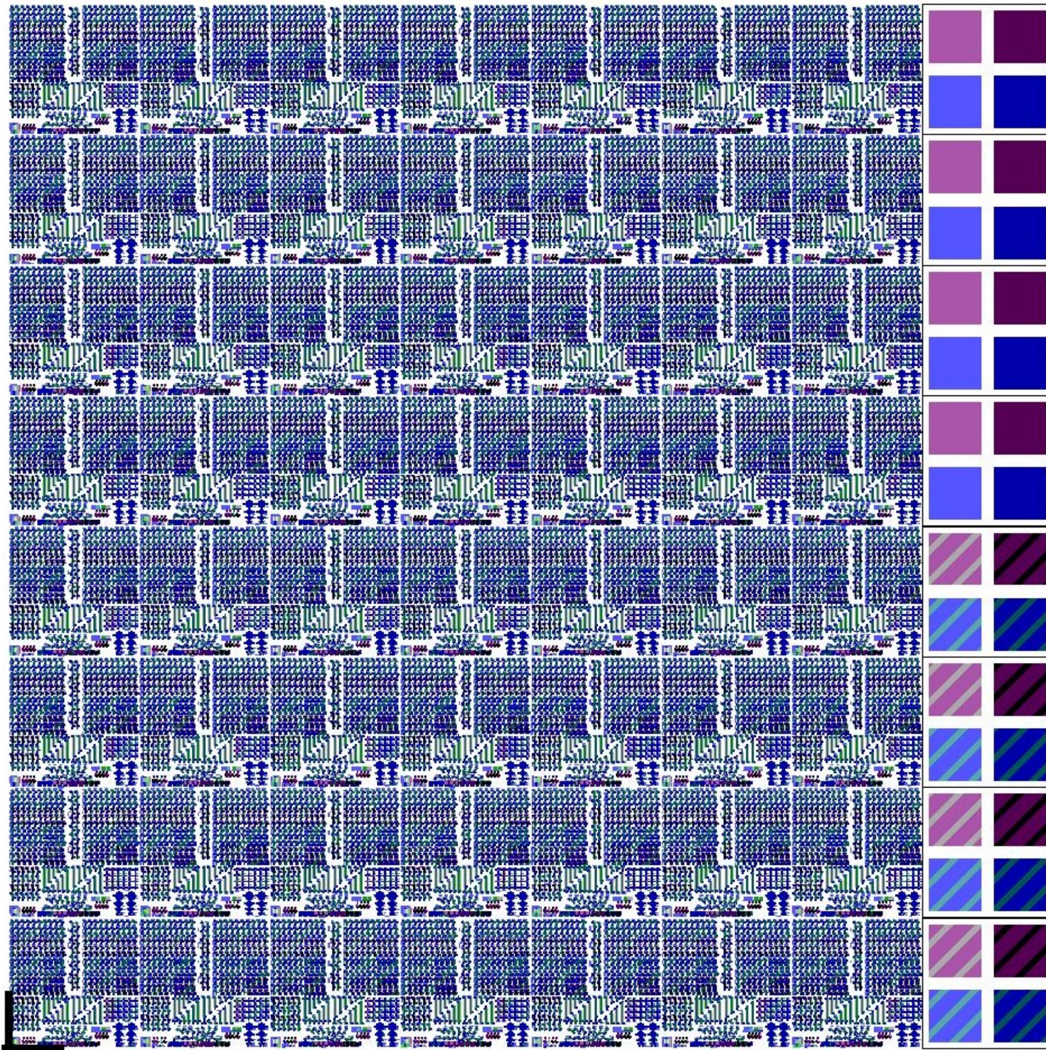

Figure B-1: 5 inch mask design, with all mask patterns overlaid on top of each other.

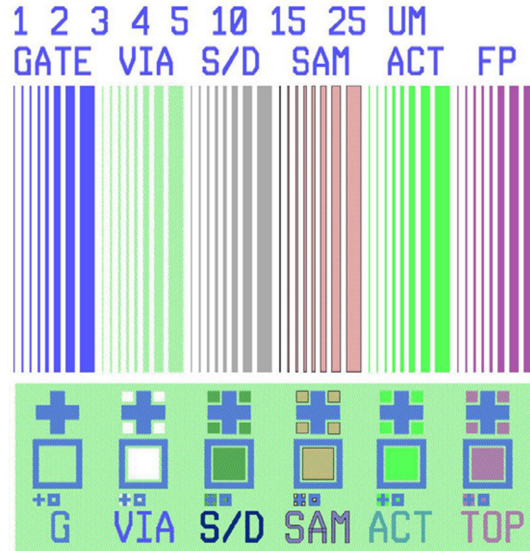

Figure B-2: Alignment markers used for aligning masks to sample.

B.1.3 Source/Drain Mask, Inverted Source/Drain Mask for Lift-Off, and Shadow Mask

One of two masks was used to define the source and drain contacts. The first was a positive pattern of the desired contacts. This source/drain mask drew the regions to be protected from the metal etchant which ultimately defined the channel length and width, shown in Fig. 4-2(c). However, as was mentioned in chapter 3, metal etchants can cause dangling bonds at the surface of the dielectric, resulting in poor electrical performance of the OTFT. Therefore, a second inverted source/drain mask was designed for Au lift-of in which etchants were avoided.

A steel shadow mask was also designed to deposit source/drain Au metal on top of soluble TIPS-pentacene without using solvents, creating a bottom gate / top contact OTFT architecture. The shadow mask design was the same as the inverted source/drain mask for lift-off.

B.1.4 SAM mask

The SAM mask, with large and small patterns shown in Fig. 4-2 (d,e), defined regions that were to be exposed to SAM treatments, either by an ethanol submerge process

or by a dry desiccator method. SAMs can be deposited on the oxide and metal contacts to define a low surface energy region, enabling a self-aligned solution process described in chapter 7.

B.1.5 Channel Mask

The channel mask, shown in Fig. 4-2 (f), defined the pentacene organic semiconductor channel. The photoresist pattern was used to cover the channel region, while the rest of the unprotected organic semiconductor could be dry etched via an oxygen asher.

B.1.6 Field Plate Mask

A final mask may be used for a top field plate for additional channel charge control in the HVOTFT, seen in Fig. 4-2 (g). The field plate metal was deposited above the boundary between the gated and offset regions.

B.1.7 Mask Set for Low-Voltage OTFTs

For low-voltage OTFTs, the gate, via, source/drain and active channel masks are shown in Fig. 4-2 (h). The difference in the OTFT patterns relative to those of the HVOTFT was how the gate metal overlapped completely the channel between the source and drain metal contacts.

B.2 Details for Fabrication Process

The fabrication process presented in chapter 4 are discussed in detail here and are summarized in Tables B.1, B.2 and B.3. The OTFTs and HVOTFTs were fabricated on 100 mm diameter borosilicate glass and flexible Kapton polyimide substrates. The wafers were eventually diced into 1 inch squares, allowing for multiple samples to be fabricated varying conditions. The glass substrates were pre-cleaned with a piranha solution for 30 minutes while the Kapton polyimide substrates were submerged in isopropyl alcohol in an ultrasonic bath for 20 minutes, both followed by a DI water

rinse. The glass and polyimide substrates were then heat treated at 100 °C in a convection oven for 1 hour for surface dehydration and thermal stability.

Bottom Cr and Au gate metal contacts (10/60 nm) were first e-beam evaporated onto the cleaned substrates at a rate of 0.5 Å/s and were patterned via a gate mask and a chemical wet etch. The photolithography process was performed as described in section 3.8. A 5:1 ratio of DI water and TFA Au etchant was used to remove Au at a rate of 8-10 Å/s while a 5:1 ratio of DI water and CR7 Cr etchant removed Cr at a rate of 4-5 Å/s. Photoresist was stripped after each etching step by submerging the sample in acetone and isopropyl alcohol for 10 minutes each, followed by a thorough DI water rinse.

The gate metal contact was topped with a dielectric layer. Devices were made with low-k organic parylene-C (200 nm, k = 3.15), high-k pyrochlore BZN (400 nm, k = 25-50), or a dual dielectric stack comprising of BZN (bottom, 400nm) and parylene-C (top, 2 nm). The dual dielectric stack had an equivalent oxide thickness (EOT) of roughly 40 nm. The top parylene-C in the dual dielectric stack was used as a passivation layer for the surface dipole moments from the high-k BZN [109]. Parylene-C was deposited using a CVD process via sublimation (150 °C) and pyrolysis (600 °C) at a rate of ∼ 0.5 Å/s, with the deposition occurring at 25 °C. On the other hand, BZN was deposited via a reactive RF magnetron sputtering process (120 W) at a rate of ∼0.2 Å/s. A stoichiometric equivalent BZN target (99.9% purity) was used. The reactive sputtering condition for achieving plasma was a 9:3 Ar:O_2 gas ratio. Vias were then patterned into the parylene-C and BZN layers by an O_2 plasma asher (0.5 Torr, 200 W, 4.5 minutes) and a diluted buffered oxide etch (40:1 ratio of DI Water to BOE, etch rate of 40-50 Å/s), respectively.

Next, source and drain Au metal contacts (100 nm) were e-beam evaporated at a rate of 0.5 Å/s and patterned by either a wet etch or a lift-off process, forming a BG/BC structure. Here, all pentacene devices were fabricated with a wet etch, while the TIPS-pentacene devices were made with the lift-off process described in section 3.8.4. For the OTFTs, the source and drain contacts were aligned to partially overlap the gate contact, forming the channel length L and width W. For the HVOTFT, on

the other hand, the source was aligned to the gate contact while the drain was aligned in such a way as to not overlap with the gate, creating a dual channel architecture with a gated region and an offset region that is characterized by an offset channel length L_{offset}. The Au contacts were then coated with an organothiol SAM, primarily 1H,1H,2H,2H-perfluorodecanethiol (PFDT), to improve charge carrier injection by increasing the metal work function and reducing the hole injection barrier. For the SAM treatment, the samples were first dehydrated on a hot plate at 100 °C at air ambient for 1 hour and were then submerged in a 0.1 wt% SAM/ethanol solution 2 hours in a cleaned Teflon beaker. The samples were rinsed with toluene and DI water to remove excess solvent.

Two different organic semiconductors were used fabricate the HVOTFTs, deposited by either a vacuum-deposited or solution-processed method. For the vacuum deposition method, pentacene was thermally evaporated under high vacuum (∼2e-7 Torr) at a rate between 0.1 and 10 Å/s, for a thickness of approximately 20 nm. For solution-processing, self-shearing drop casting of TIPS-pentacene was chosen for its simplicity and quick turnaround. The organic solution was prepared by dissolving TIPS-pentacene crystals (obtained from Sigma-Aldrich) at 2 wt% in anisole and stirred for over 24 hours over a hot plate set to 50 °C. The solution was then drop casted, in air ambient, onto samples placed on a hot plate set to 50 °C, which was then left to dry for 1-3 hours. The samples were also angled at 4.5° from the horizontal, allowing the TIPS-pentacene to grow in a preferential directed orientation, along the slant (perpendicular to the channel length). Nucleation and crystallization of the TIPS-pentacene occurred at the top of the sample, beginning at the evaporation front. The TIPS-pentacene grew to a thickness of anywhere between 0.5 and 3 μm, depending on the amount of solution drop casted. Typically, thicker TIPS-pentacene layers were observed near the bottom of the sample due to the accumulation of the solution droplet. Although the self-shearing drop casting method created semi-random crystal grains, the bands grew as wide as 3 mm. Additional PFDTES could be used to coat the samples to promote a quick shearing process during drop casting. This resulted in thin TIPS-pentacene bands, albeit random in orientation.

Both vacuum-deposited and solution-processed devices were then coated with parylene-C (200 nm), which acted as an encapsulation layer for moisture and chemical protection. The pentacene and parylene-C layers were patterned via a photolithography process with the channel mask and an O^2 plasma asher (0.5 Torr, 200 W, 5 minutes) to create isolated semiconductor channels for reduced cross-talk. However, TIPS-pentacene samples were not patterned, due to the semiconductor's non-uniform surface and incompatibility with solvents. Alternatively, organosilane and organothiol SAM coatings of the oxide dielectric and the Au metal contacts, respectively, could be performed to create a self-aligned solution-process in which the solution aggregated towards the high surface energy regions (the channel). This allowed for the patterning of the TIPS-pentacene without the use of photolithography and etching. In this case, a photoresist mask was patterned on top of the samples, leaving PR covering the channel and exposing the Au and BZN to be treated with SAMs. PFDT was deposited onto Au via the desiccator with the addition of an infra-red heat lamp. The PFDT inside the desiccator was heated to approximately 60 °C for 6-12 hours, which increased exponentially the vapor pressure of the SAM for sublimation and deposition onto the Au. PFDTES was subsequently deposited via the desiccator at RT for 6-12 hours. The photoresist was then stripped away by submerging the sample in acetone and isopropyl alcohol for 10 minutes each, followed by a DI water rinse. Finally, TIPS-pentacene solutions could be drop casted

Next, TIPS-pentacene solutions were drop casted on dummy glass substrates with patterned PFDTES. To further investigate the affects of temperature, the organic solution and the substrate were either left at room temperature or heated to 50 °C. Firstly, the organic solution was heated to 50 °C and was quickly drop casted onto a slanted (4.5°) and heated (50 °C hot plate condition) sample. The organic solution was heated in an attempt to promote crystallization. However, the organic solution did not aggregate in the SAM patterns, but covered the entire surface. This can be explained by the reduced cohesive forces from increased molecular thermal activity, which is summarized by the Eötvös rule:

desiccator can also be used to deposit the SAMs on the sample surface, as shown

in Fig. 3-27. 200-400 μL of the SAM was dropped onto a clean glass slide inside a desiccator set to 0.6-0.8 atm. The samples were placed adjacent to the SAM droplets. With the reduced pressure, SAMs evaporated and deposited, over several hours, onto the samples. A heat lamp has also been used to increase the vapor pressure of organothiol SAMs to assist in deposition, as discussed in the fabrication procedure for self-aligned TIPS-pentacene HVOTFTs in chapter 7.

B.3 Optimization of the Fabrication Process

Additional details of the fabrication procedure is mentioned here, concerning the optimization as well as fabrication nuances.

B.3.1 PR Adhesion Promotion

Photoresist adhesion becomes an issue on surfaces such as SiO_2, glass and precious medals (Au and Ag). In particular Au and Ag do not possess surface adhesion promoting defects due to their corrosion and oxidation resistance. A lack of PR adhesion on the initial Au metal lead to over-etching of the gate contact, reducing the resolution of the initial metal layer. Several methods were used to promote PR adhesion: dehydration via a hot plate (100 °C for 10 minutes), spin coated liquid HMDS and vapor deposited HMDS. The latter proved to be the most efficient, with the sample heated to $\sim$ 150 °C, providing additional dehydration of the Au surface. Fig. B-3 shows the gate level alignment markers that were etched under different PR adhesion promotion schemes.

B.3.2 Average Surface Roughness of Au

The arithmetic average surface roughness (Ra), as measured by a Dektak profilometer, of each layer leading up to the deposition of the organic semiconductor is critical in reducing the roughness seen by the charge carriers at the dielectric/semiconductor interface. 60 nm thick Au was deposited via e-beam evaporation onto 10 nm Cr on clean glass, and was found to have significantly lower surface roughnesses when

Table B.1: Part I: Fabrication procedures for the OTFT and HVOTFT.

Step	Purpose	Process	Material	Parameters
1.1a	Clean	Piranha for glass	H_2SO_4:H_2O_2 (4:1)	30 min
1.1b	clean	IPA + O_2 asher for polyimide	IPA	Ultrasonic bath: 20 min, IPA, + O_2 asher: 5 min, 100 W
1.2	Thermal Stability	Long bake		100 °C, 1 hours
2.1	Gate	E-beam	Cr/Au	10/60 nm, 0.5 Å/s
2.2	Gate	PR adhesion	Vapor HMDS	Optional
2.3	Gate	Spin coat PR	SPR700-1.0	3000 rpm, 1.3 μm thick
2.4	Gate	Soft bake		90 °C, 20 min, convection oven
2.5	Gate	UV expose		Gate mask, 10 s exposure
2.6	Gate	Develop	Developer CD-26	30 to 45 s
2.7	Gate	Hard bake		115 °C, 30 min, convection oven
2.8	Gate	Wet etch (Au)	DI Water:TFA Au etchant (5:1)	90 s
2.9	Gate	Wet etch (Cr)	DI Water:Cr etchant (5:1)	20 to 25 s
2.10	Gate	Strip resist	Acetone/IPA/DI Water	Submerge for 10/10/5 min
3.1a	Dielectric	RF Sputter	BZN	400 nm, 3 mTorr, Ar:O_2 (9:3), 95 to 120 W, 0.2-0.4 Å/s
3.1b	Dielectric	CVD	Parylene-C	200-400 nm
3.2	Dielectric	Spin coat PR	SPR700-1.0	3000 rpm, 1.3 μm thick
3.3	Dielectric	Soft bake		90 °C, 20 min, convection oven
3.4	Dielectric	UV expose		Via mask, 10 s exposure
3.5	Dielectric	Develop	Developer CD-26	30 to 45 s
3.6	Dielectric	Hard bake		115 °C, 30 min, convection oven
3.7a	Dielectric	Wet etch BZN	DI Water:BOE (40:1)	45 Å/s
3.7b	Dielectric	Wet etch PAR-C		O_2 asher: 5 min, 200 W
3.8	Dielectric	Strip resist	Acetone/IPA/DI Water	Submerge for 10/10/5 min

Table B.2: Part II: Fabrication procedures for the OTFT and HVOTFT.

Step	Purpose	Process	Material	Parameters
4.1	S/D	Spin coat PR	SPR700-1.0	3000 rpm, 1.3 μm thick
4.2	S/D	Soft bake		90 °C, 20 min, convection oven
4.3	S/D	E-beam	Al	300 nm, 0.5 Å/s
4.4	S/D	Spin coat PR	SPR700-1.0	3000 rpm, 1.3 μm thick
4.5	S/D	Soft bake		85 °C, 20 min, convection oven
4.6	S/D	UV expose		S/D mask, 10 s exposure
4.7	S/D	Develop	Developer CD-26	30 to 45 s
4.8	S/D	Wet etch (Al)	Transene Al Etchant	9 min
4.9	S/D	Flood exposure		45 s
4.10	S/D	Develop	Developer CD-26	25-30 s
4.11	S/D	E-beam	Au	100 nm, 0.5 to 1.0 Å/s
4.12	S/D	Lift-off	Acetone/IPA/DI Water	Ultrasonic bath: 10-20 min
5.1	SAM	Spin coat PR	SPR700-1.0	3000 rpm, 1.3 μm thick
5.2	SAM	Soft bake		90 °C, 20 min, convection oven
5.3	SAM	UV expose		SAM mask, 10 s exposure
5.4	SAM	Develop	Developer CD-26	30 to 45 s
5.5	SAM	Hard bake		115 °C, 30 min, convection oven
5.6a	SAM	Organothiol	Organothiol SAM	Submerge sample in ethanol/SAM solution, 2h hours
5.6b	SAM	Organosilane	Organosilane SAM	Desiccator, 300-400 μL SAM, 4-12 hours
5.7	SAM	Strip resist	Acetone/IPA/DI Water	Submerge for 10/10/5 min

Table B.3: Part III: Fabrication procedures for the OTFT and HVOTFT.

Step	Purpose	Process	Material	Parameters
I.6.1	Pentacene	Thermal evaporation	Pentacene	20 nm, 160 °C, 0.3 Å/s
I.6.2	Pentacene	CVD	Parylene-C	200 nm
I.6.3	Pentacene	Spin coat PR	SPR700-1.0	3000 rpm, 1.3 μm thick
I.6.4	Pentacene	Soft bake		90 °C, 20 min, convection oven
I.6.5	Pentacene	UV expose		Channel mask, 10 s exposure
I.6.6	Pentacene	Develop	Developer CD-26	30 to 45 s
I.6.7	Pentacene	Hard bake		115 °C, 30 min, convection oven
I.6.8	Pentacene	RIE		O_2 asher: 5 min, 200 W
I.6.9	Pentacene	Strip resist	Acetone/IPA/DI Water	Submerge for 10/10/5 min
II.6.1	TIPS-PEN	Drop cast	Anisole/TIPS solution, 2 vol%	300-400 μL per inch^2, 50 °C
7.1	Field Plate	Spin coat PR	SPR700-1.0	3000 rpm, 1.3 μm thick
7.2	Field Plate	Soft bake		90 °C, 20 min, convection oven
7.3	Field Plate	E-beam	Al	300 nm, 2.0 Å/s
7.4	Field Plate	Spin coat PR	SPR700-1.0	3000 rpm, 1.3 μm thick
7.5	Field Plate	Soft bake		85 °C, 20 min, convection oven
7.6	Field Plate	UV expose		Field plate mask, 10 s exposure
7.7	Field Plate	Develop	Developer CD-26	30 to 45 s
7.8	Field Plate	Wet etch (Al)	Transene Al Etchant	9 min
7.9	Field Plate	Flood exposure		45 s
7.10	Field Plate	Develop	Developer CD-26	25-30 s
7.11	Field Plate	E-beam	Au	100 nm, 0.5 to 1.0 Å/s
7.12	Field Plate	Lift-off	Acetone/IPA/DI Water	Ultrasonic bath: 10-20 min

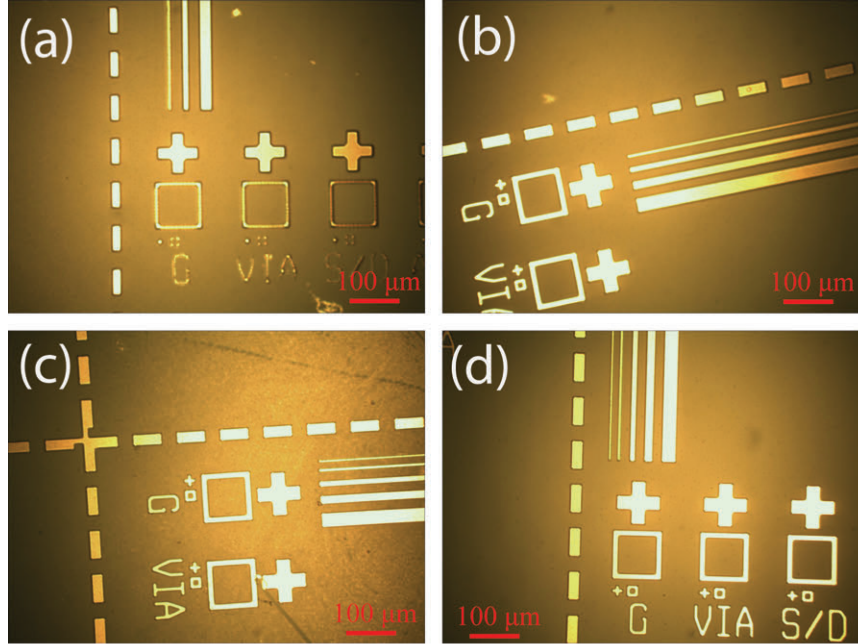

Figure B-3: Optical micrographs of gate level alignment markers (a) without PR adhesion promotion, (b) with a hot plate dehydration, (c) liquid HMDS spin coat and (d) vapor HMDS deposition.

deposited with lower deposition rates. The average roughness for Au is summarized in Table B.4 and shown in Fig. B-4.

B.3.3 Sputtering Rate of BZN

The sputtering rate of BZN versus RF power and reactive gas ratios (between argon and oxygen) was measured using a quartz crystal monitor, shown in Fig. B-5 and Fig. B-6. The sputtering rates increased near-linearly with RF power between 80 and 200 W as well as increased with a less reactive gas ratios (more argon, less

Table B.4: Au surface roughness vs. e-beam evaporation rates.

Au deposition rate (Å/s)	Average roughness (nm)
0.5	1-3
1	10-20
3	15-40
5	50-90

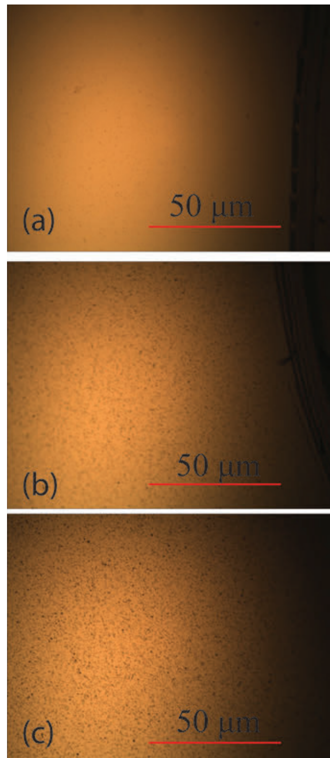

Figure B-4: Optical micrographs of Au e-beam evaporated at different rates.

oxygen). However, with less oxygen species present in the sputtering chamber, the stoichiometry of the BZN was no longer that of α-BZN, as discussed in section 4.6.2. Furthermore, the Ra surface roughness increased with decreasing oxygen content, seen in Fig. B-7, suggesting a non-uniform deposition of the elements of BZN

B.3.4 Etch Rate of BZN

To determine the etch of BZN, a series of 40:1 DI water:BOE etches were performed at different time intervals. 200 nm of BZN was reactive RF sputtered (9:3 Ar:O_2, 110 W, 0.3 Å/s) onto clean (5 min BOE strip, 20 min piranha clean and a BOE dip) Si wafers. An etch rate of ~50 Å/s was found, with the 200 nm BZN etched away after 40 seconds, as shown in Fig. B-8.

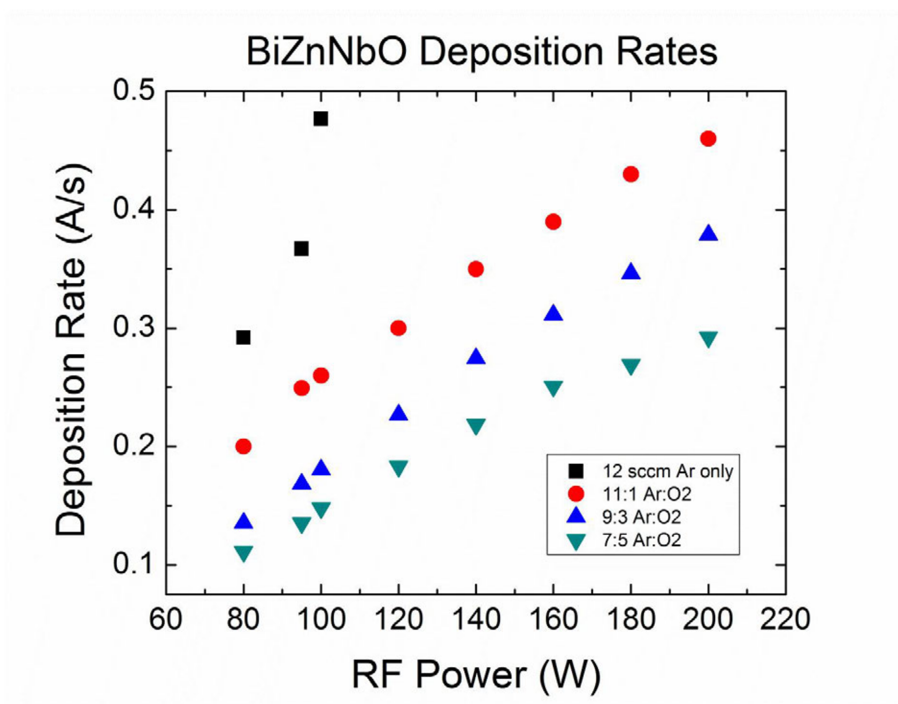

Figure B-5: Sputtering rates of BZN as a function of RF power and reactive gas ratios (Ar:O_2).

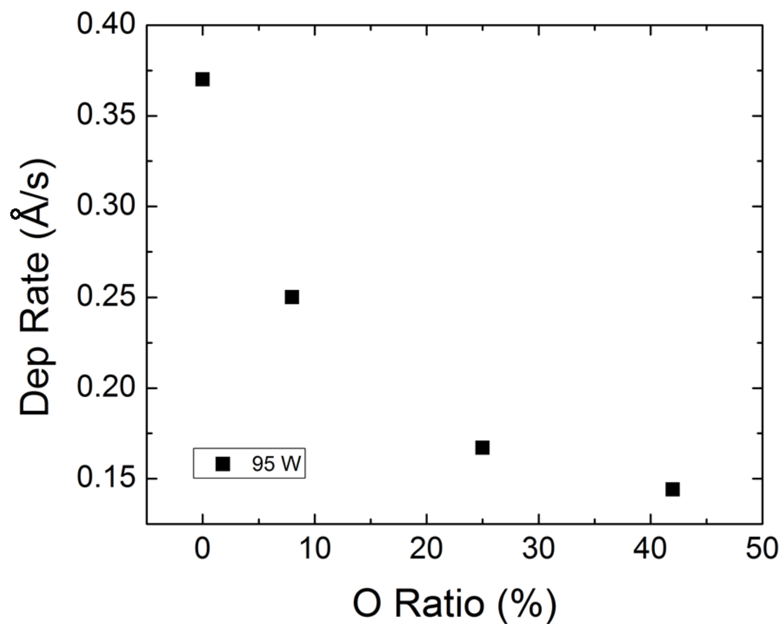

Figure B-6: Sputtering rates of BZN versus O_2 gas ratio.

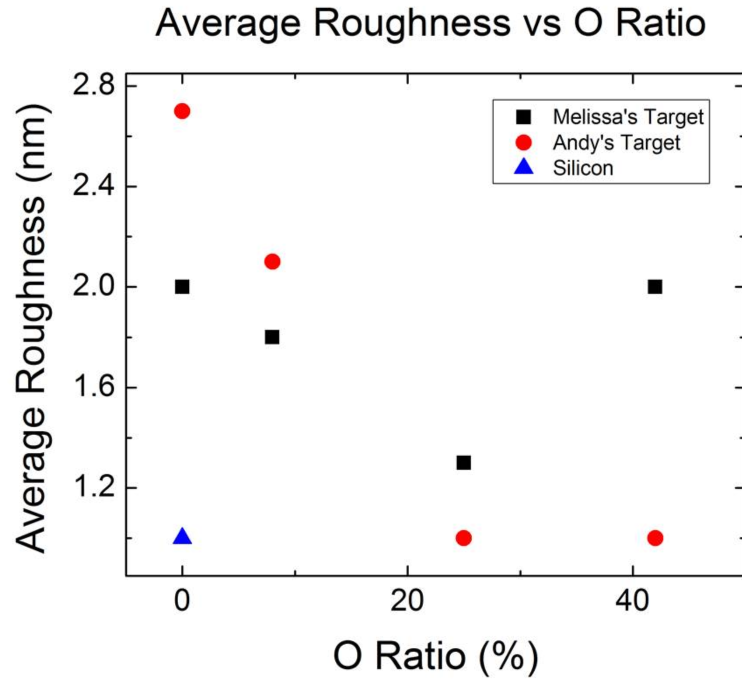

Figure B-7: Arithmetic average of the surface roughness of BZN sputtered with varying Ar:O_2 ratios.

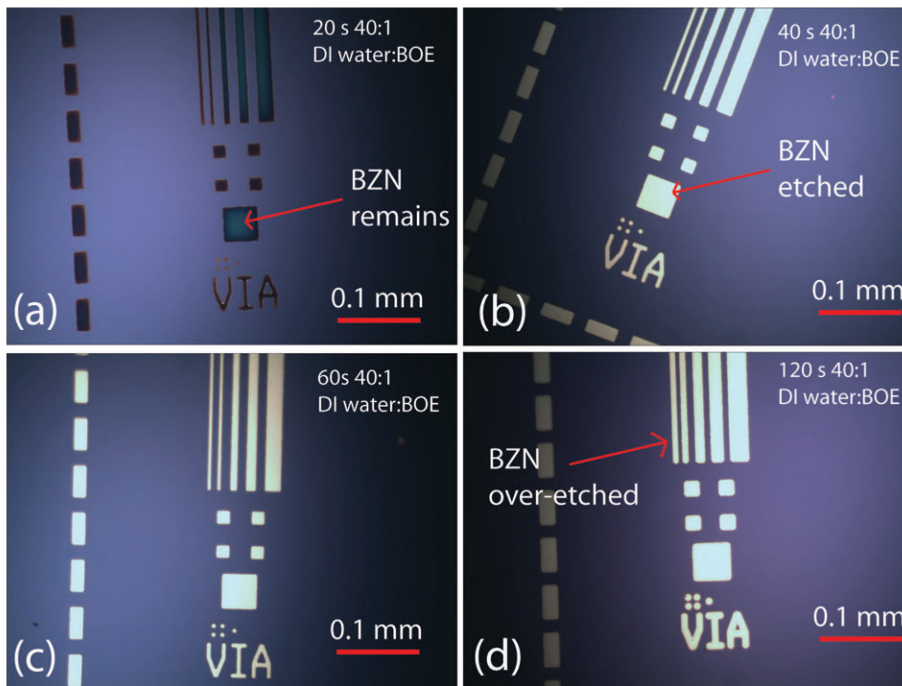

Figure B-8: BZN etched with 40:1 DI water:BOE under varying etching times: (a) 20, (b) 40, (c) 60 and (d) 120 seconds. Vias were opened in 200 nm thick BZN after 40 seconds of etching. Over-etching was observable after 80 to 100 seconds.

Appendix C

Contact Angle Measurements

C.1 Contact Angle Measurements

Contact angle measurements using a Ramé-Hart 260 goniometer were performed on numerous surface to assess their surface energy as well as their potential for a self-aligned solution-process method, as outlined in chapter 7. 10 μL of DI water and ethylene glycol were drop casted on clean surfaces and SAM treated samples, with their contact angle taken as the average of the left and right contact angles of the droplet. The analysis of the contact angles was discussed in section 7.1. Fig. C-1, C-2, C-3 and C-4 show the liquid droplet on the different surfaces.

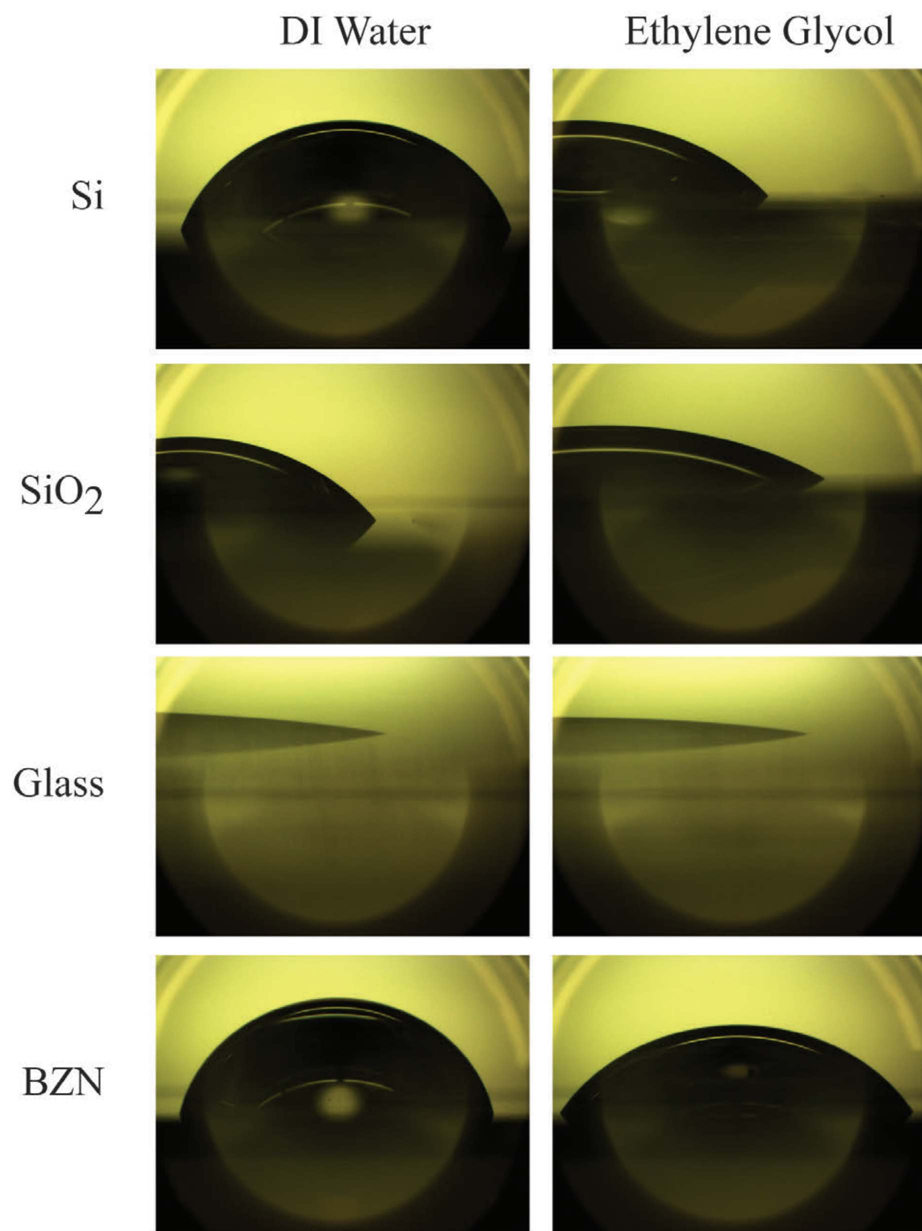

Figure C-1: Contact angle measurements, with DI water and ethylene glycol, of Si, SiO_2, glass and BZN samples.

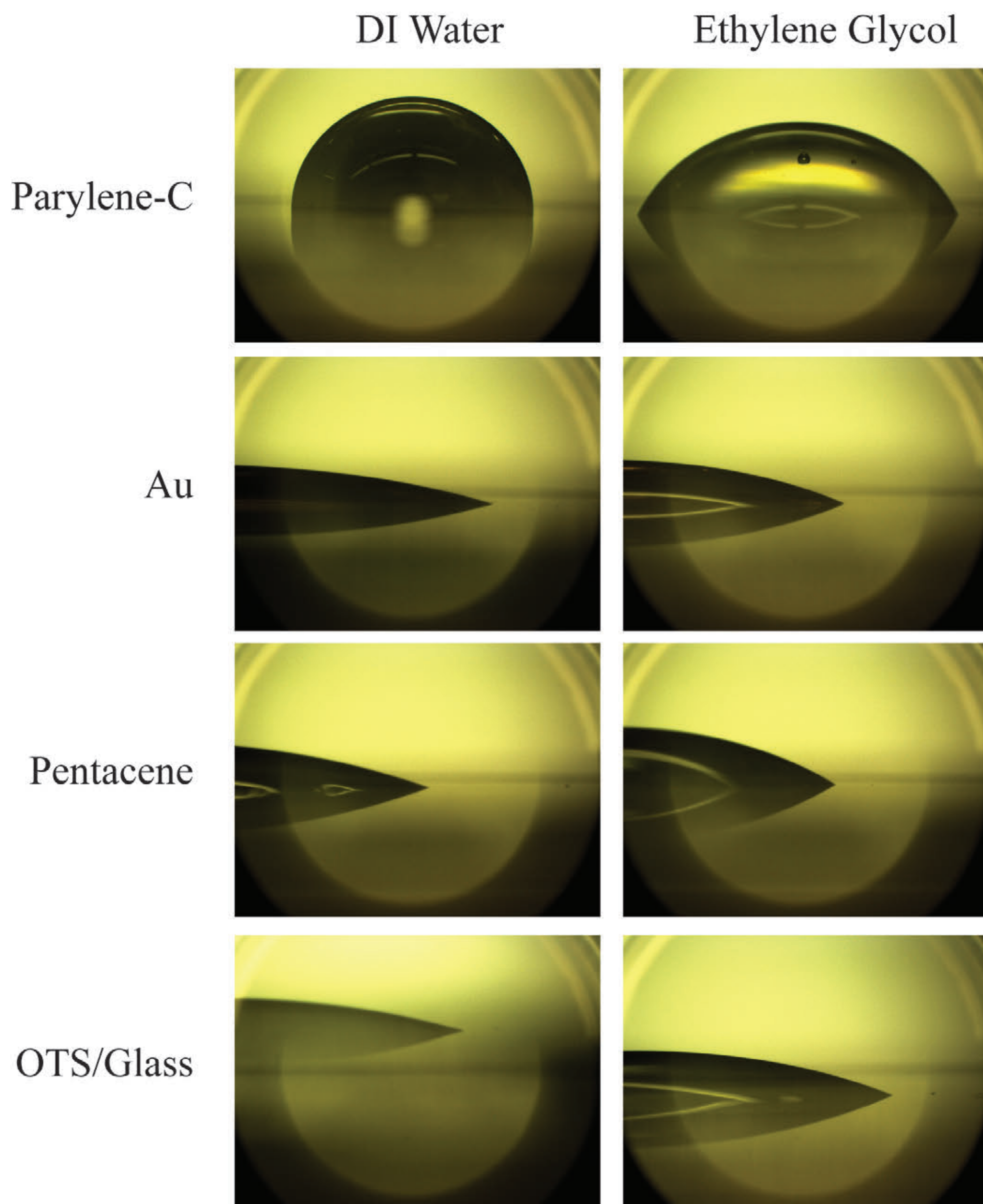

Figure C-2: Contact angle measurements, with DI water and ethylene glycol, of parylene-C, Au, pentacene and OTS/glass samples.

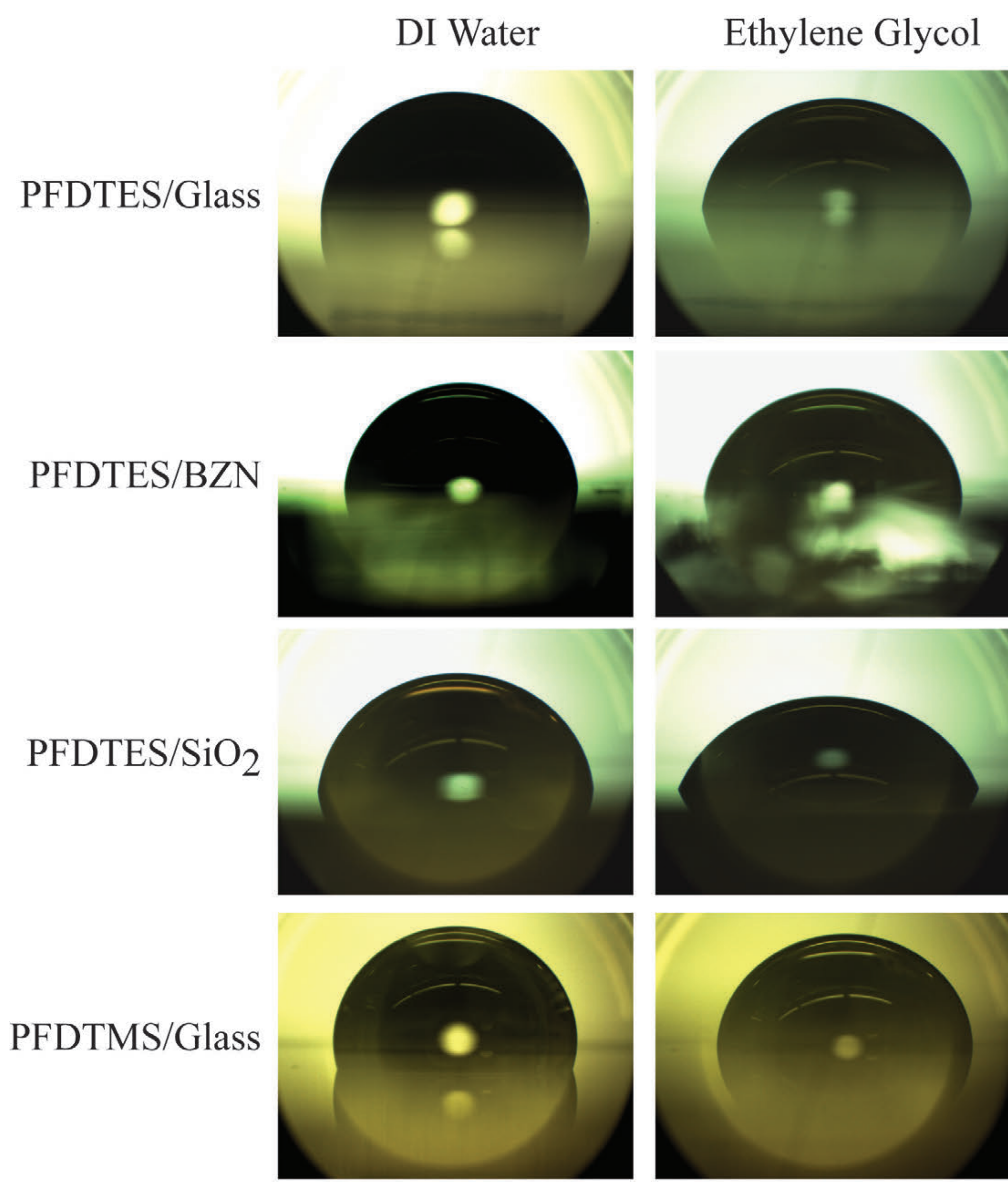

Figure C-3: Contact angle measurements, with DI water and ethylene glycol, of PFDTES/glass, PFDTES/BZN, PFDTES/SiO_2 and PFDTMS/glass samples.

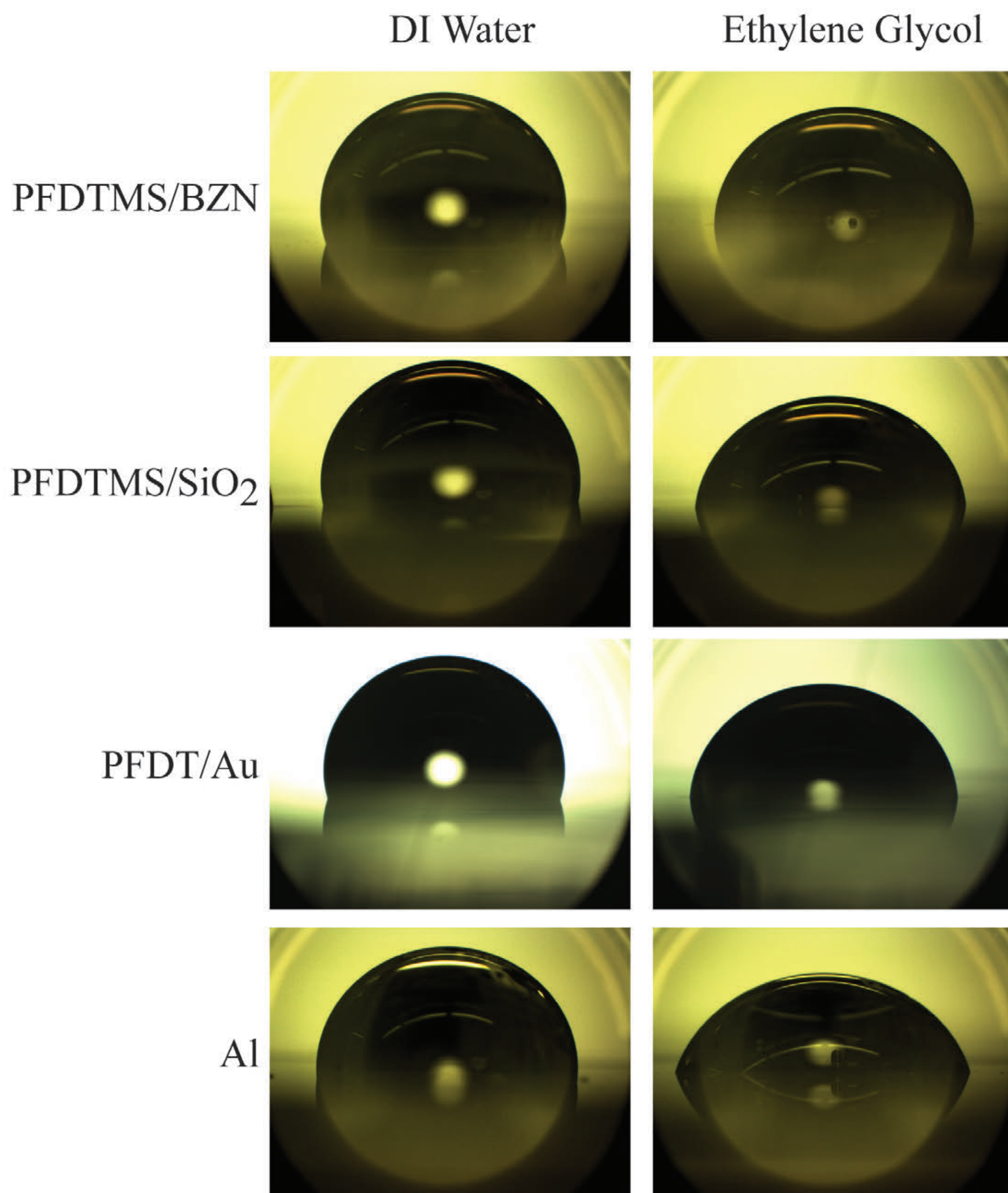

Figure C-4: Contact angle measurements, with DI water and ethylene glycol, of PFDTMS/BZN, PFDTMS/SiO_2, PFDT/Au and Al samples.