Energy Efficient Computing: From Nanotubes to Negative Capacitance

by

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B.Tech. (Hons.), Indian Institute of Technology, Kharagpur (2016)

Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Engineering and Computer Science

at the

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Abstract

Physical scaling of silicon-based field-effect transistors (FETs) has been a major driving force to improve computing energy efficiency (quantified by the energy-delay product, EDP, the product of energy consumption and circuit delay) for decades. However, continued silicon scaling is becoming increasingly challenging. This is motivating the search for beyond-silicon nanotechnologies, such as one-dimensional carbon nanotubes (CNTs) or two-dimensional nanomaterials such as transition metal dichalcogenides (TMDs) or black phosphorous. Yet simply relying on new materials alone is insufficient for realizing the next generation of energy-efficient computing. Rather, coordinated advances across several disciplines are required, as their combined benefits are greater than the sum of their individual benefits. In this work, I illustrate how by combining multiple advances - from new device physics to new nanomaterials to new device geometries – there is a feasible path towards realizing *over an order of magnitude benefit* is energy efficiency for digital very-large-scale integrated (VLSI) systems.

As a case study, this thesis focuses on CNT-based electronics. I experimentally demonstrate that by leveraging this new nanomaterial, we can naturally realize CNT field-effect transistors (CNFETs) that both take advantage of new device physics (specifically, *negative capacitance*), as well as new device geometries (specifically, *back-gate geometries*). Yet despite this potential, there is a major challenge: while new nanomaterials introduce many new opportunities (as mentioned above), they simultaneously introduce many challenges. For instance, CNFETs are unfortunately often subject to substantial off-state leakage current (I_{OFF}) which results in increased leakage power and potential incorrect logic functionality. Therefore, to

realize the potential benefits of these new nanomaterials (and the new opportunities they enable), practical obstacles must be overcome. Within this thesis, we demonstrate a path for mitigating this leakage by engineering back-gate CNFET geometries with asymmetric gates (e.g., gates that overlap the source but not the drain).

The key contributions of this thesis are the following:

1. We experimentally fabricate the world's most-scaled CNFETs that fit within a contacted gate pitch (CGP, a key metric determining the area of a FET) of 30 nm, suitable for sub-3nm technology nodes. This is enabled by exploiting back-gate FET geometries, which are naturally enabled by the unique low-temperature processing of CNFETs.
2. We use the CNFETs above to realize cascadable digital logic that fit within a world record CGP of 30 nm. This is the most scaled digital logic realized to-date.
3. We perform the first rigorous analysis of back-gate FET geometries, and show for digital VLSI circuits that in addition to scaling benefits, back-gate CNFETs improve EDP by 1.6× vs. top-gate CNFETs and 2.2× vs. gate-all-around CNFETs.
4. First experimental demonstration of Negative Capacitance CNFETs (NC-CNFETs), combining the benefits of CNTs, back-gate geometries, and new physics (negative capacitance ferroelectrics).
5. Experimentally reveal the underlying cause behind excess off-state leakage current in CNFETs, and demonstrate a path for overcoming it (leveraging the same back-gate FET geometries used for contributions 1-4). We experimentally implement our approach on CNFETs fabricated across wide range of technology nodes (from 180 nm node to >1 μm node), and show a >60× improvement in off-state leakage current in CNFETs.

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1. Srimani, Tathagata, Gage Hills, Mindy D. Bishop, Max M. Shulaker, "*30 nm Contacted Gate Pitch Back-Gate Carbon Nanotube FETs for Sub-3 nm Nodes*". 2018 (submitted)

2. Srimani, Tathagata, Gage Hills, Jianqiang Lin, Christian Lau, Dimitri Antoniadis, Jesus A. del Alamo, Max M. Shulaker, *"Gate Geometry Engineering for Carbon Nanotube Field-Effect Transistors"*. 2018 (submitted)

3. Srimani, Tathagata, Gage Hills, Mindy D. Bishop, Ujwal Radhakrishna, Ahmad Zubair, Rebecca S. Park, Yosi Stein, Tomas Palacios, Dimitri Antoniadis, and Max M. Shulaker, *"Negative Capacitance Carbon Nanotube FETs"*. *IEEE Electron Device Letters* 39, no. 2 (2018): 304-307.

Chapter 1: Introduction

1.1 Background

Physical and equivalent scaling of silicon complementary metal-oxide semiconductor (CMOS) technology has been a major driving force for improving computing energy efficiency for decades. This progress has had dramatic impact in all of our lives: from enabling self-driving cars to genome sequencing to the "internet-of-everything" (IOE). Yet as these applications demand increasingly energy-efficient computing, progress in computing is coming to an abrupt halt. Continued scaling of silicon-based FETs is growing increasingly challenging, and the benefits afforded by scaling (e.g., Dennard Scaling [Dennard 1974]) no longer follow their historical trends. Therefore, continuing with "business as usual" is insufficient – *new innovation is required.*

As evolving today's technology is insufficient for meeting the computing demands of future applications [Sabry 2015], alternative approaches and technologies are being explored. For example, emerging one-dimensional (1D) and two-dimensional (2D) semiconductors are exciting emerging nanomaterials, promising improved carrier transport and electrostatic control versus bulk semiconductor materials (such as silicon). Single-walled carbon nanotubes (SWCNTs, or CNTs), are one such promising 1D nanomaterial with excellent electrical, thermal and physical properties [Riichiro 1998, Wei 2009]. CNTs are nanocylinders made of a single atomically-thin sheet of carbon atoms with a diameter of ~1 nm. Carbon nanotube field-effect transistors, CNFETs, are formed by multiple CNTs in parallel forming the channel whose conductance is modulated by a metal gate. Figure 1.1 shows the schematic of a single CNT and a CNFET. Gate and source/drain contacts are defined by traditional lithography. Owing to their ultra-thin body thickness (~1 nm diameter of the CNT), CNFETs exhibit excellent electrostatic control and simultaneously high carrier transport [Hills 2015]. Due to these benefits, CNFETs are projected to achieve an order of magnitude benefit in energy-delay product (EDP) compared to silicon CMOS for digital VLSI circuits [Chang 2012; Wei 2009;

Tulevski 2014]. Importantly, CNFETs can be fabricated at low processing temperatures (<400°)[a] [Shulaker 2013; Shulaker 2017; Patil 2009], and therefore naturally enable monolithic three-dimensional (3D) integration (whereby layers of circuits are fabricated sequentially and directly vertically overlapping one-another, all over the same starting substrate [Shulaker 2017]. Such monolithic 3D integration enables new paradigms in designing heterogeneous nanosystems [Shulaker 2017], allowing fine-grained integration of sensing, logic and memory at the nanoscale.

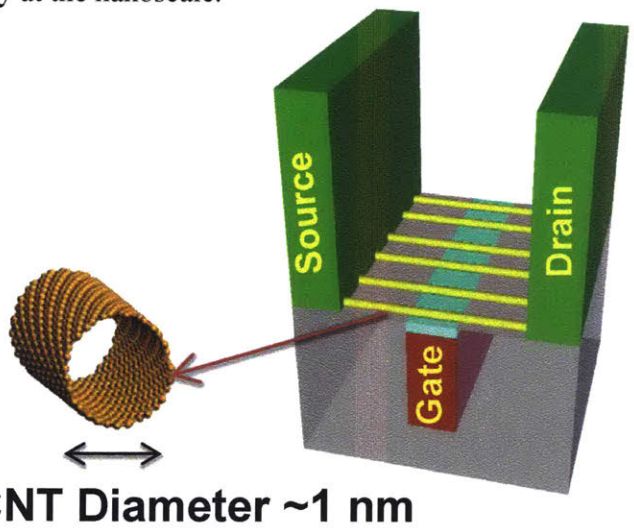

Figure 1.1 Schematic of carbon nanotube field-effect transistor (CNFET) with multiple parallel CNTs (nanocylinders made with atomically thin sheet of carbon atoms with diameter ~ 1 nm) bridging the source to drain contact. Conductance of the CNTs are modulated by the gate to turn the transistor on or off.

Moreover, CNFETs are a rapidly maturing nanotechnology, and the technology has progressed substantially over the past decade. CNFETs are unique among emerging nanotechnologies as complete CNFET digital systems [Shulaker 2013, Shulaker 2014a], highly-scaled CNFETs with sub-10 nm channel lengths [Franklin 12], and complementary p- and n-type CNFETs operating at scaled supply voltages of <400 mV [Wei 2013] have all been experimentally shown. However, prior to this thesis, the projected benefits and works related to CNFETs have been restricted to improvements resulting from an alternative channel material (the CNT itself). In this thesis, we demonstrate that by co-optimizing the fabrication, device structure, and design of CNFETs for digital VLSI circuits, the benefits afforded by CNFETs can increase dramatically (the specific

[a] While CNTs are synthesized at high temperature (>800 °C), they can be transferred to arbitrary substrates through either layer transfers or by solution-based processing at room temperature. This decouples the high-temperature processing of the CNTs from the monolithic 3D IC.

contributions are detailed below). Importantly, this work is both applicable to a broad range of emerging 1D and 2D nanomaterials, and guides future research directions on emerging nanotechnologies for high-performance digital logic VLSI.

1.2 Contributions

In this thesis, we focus on leveraging the unique properties of CNTs to enable additional benefits that have not been previously explored or demonstrated. To do so, this work spans a range of disciplines, from nanofabrication, to semiconductor device physics, to digital VLSI circuit analysis. We demonstrate that by co-optimizing many layers of the stack, EDP benefits afforded by CNTs can increase by >100% while simultaneously enabling new opportunities (such as scaling FETs to record scaled dimensions). To highlight this, this works focuses on co-optimizing the foundational level of the stack, nanofabrication of the devices themselves, with device geometries, digital VLSI circuit EDP, and new physics; this work even leverages the same nanofabrication to overcome one of the key remaining obstacles facing CNFETs today (increased off-state leakage currents). Specifically, this work shows the following:

1) By leveraging the low-temperature (<200 °C) solution-based processing of CNTs, the CNT channel can be fabricated on-top of the gate stack with a back-gate geometry. This is in stark contrast to silicon FETs today, where the silicon is below the gate stack in a top-gate geometry; since silicon often requires >1000 °C processing temperatures, processing silicon over the gate stack would damage or destroy the gate and gate dielectric. While substantial work today focuses on realizing increasingly advanced CNFET geometries (such as top-gate and gate-all-around), we show that back-gate FET geometries enable device scaling opportunities beyond the limits of top-gate FETs, simultaneously with improved energy efficiency. We experimentally fabricate CNFETs and CNFET digital logic with the world's smallest contacted gate pitch to-date of 30 nm (contacted gate pitch, CGP, a key metric determining the area of a FET), and show that back-gate CNFETs improve EDP of digital VLSI circuits by 1.6× vs. top-gate CNFETs and 2.2× vs. gate-all-around CNFETs, analyzed using complete physical designs of commercial processor cores.

2) Despite these benefits, CNFETs are often subject to substantial off-state leakage current (I_{OFF}) which results in increased leakage power and potential incorrect logic functionality. To realize the benefits described above, we investigate and address this substantial obstacle. We reveal the underlying physics of off-state leakage behavior in CNFETs through experiments and experimentally-calibrated simulations. We show this off-state leakage current is due to parasitic leakage currents (stemming from gate-induced drain leakage (GIDL), such as parasitic schottky barrier leakage). Moreover, we experimentally demonstrate a path for mitigating this leakage by engineering the *same back-gate CNFET geometries described above* with asymmetric gates (e.g., gates that overlaps the source but not the drain). We experimentally demonstrate our approach for CNFETs implemented across a wide range of technology nodes (from 180 nm node to >1 μm node), achieving a >60× improvement in off-state leakage current while our calibrated models show potential benefits exceeding 10^6×.

3) The low-temperature fabrication of CNFETs also enables heterogeneous integration of CNTs with other emerging nanomaterials. For instance, we demonstrate that ferroelectric materials can be embedded within the gate stack beneath the CNTs, allowing negative capacitance effects to be exploited within CNFETs. We experimentally demonstrate, for the first time, negative capacitance (NC) CNFETs (NC-CNFETs), combining the benefits of both CNT channels and negative capacitance effects (utilizing negative capacitance effects from the ferroelectric materials embedded within the back-gate stack). We demonstrate NC-CNFETs that achieve below sub-60 mV/decade sub-threshold slope [Salahuddin 2008] of 55 mV/decade at room temperature. The average I_{ON} (on current) of these NC-CNFETs improves 2.1× versus baseline CNFETs, (i.e., without negative capacitance) for the same I_{OFF} (off current). Thus, this work demonstrates a promising path forward for future generations of energy-efficient electronic systems. By co-optimizing fabrication, devices, and materials, emerging nanotechnologies can provide substantial benefits that have not yet been previously explored.

1.3 Outline

Chapter 2 presents back-gate CNFETs as a path for scaling beyond the limits of conventional top-gate and gate-all-around FETs with simultaneous energy efficiency benefits for digital VLSI circuits. Chapter 3 addresses excess leakage current in CNFETs, and presents a path for overcoming it leveraging the same device structure described in Chapter 2. Chapter 4 demonstrates how the same device structure used in Chapter 2 and Chapter 3 enables CNFETs to naturally exploit negative capacitance effects, and shows the first experimental demonstration of a NC-CNFET. Chapter 5 concludes this thesis.

Chapter 2: Engineering Device Geometries for Improved Scaling and Energy Efficiency

2.1 Background

As scaling FET contacted gate pitch (CGP) becomes increasingly challenging, paths for continued scaling to 3 nm technology nodes and beyond remain unclear [Liebmann 2016, ITRS]. Additionally, larger parasitic capacitances due to thinning spacers between the gate and source/drain degrade energy efficiency [Kuhn 2012], further limiting CGP scaling [Bardon 2016]. This has motivated a search for emerging nanotechnologies to supplement or replace silicon FETs. For instance, carbon nanotubes (CNTs) can be used to form CNT FETs (CNFETs), which promise an order of magnitude EDP benefit for digital VLSI systems compared to silicon CMOS [Wei 2009, Tulevski 2014].

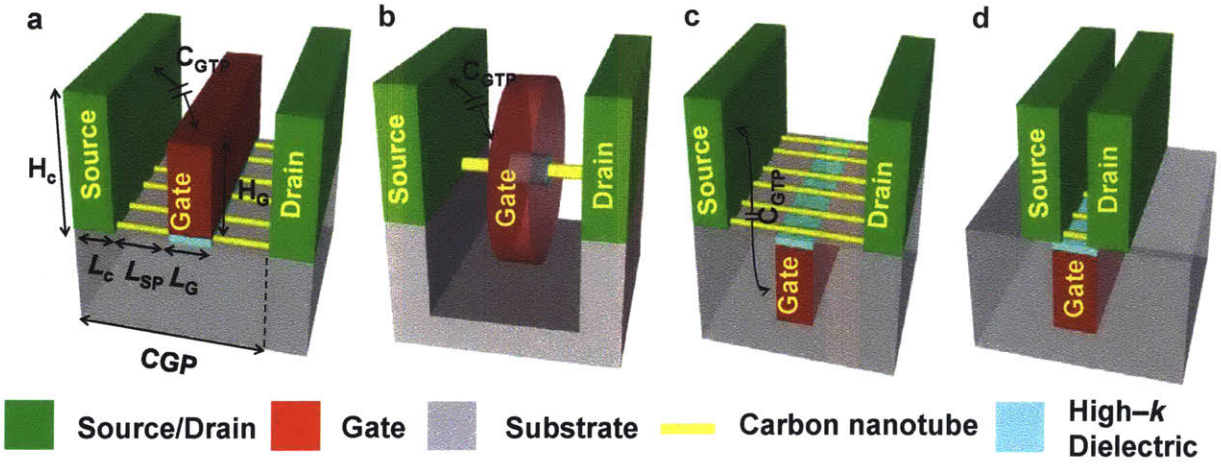

Fig. 2.1: Different FET geometries (illustrated with CNTs as the FET channel). (a) Conventional top-gate FET geometry. (b) Gate-all-around FET geometry. (c) Back-gate FET geometry. (d) Back-gate FET with negative L_{SP}

Fig. 2.1 shows schematics of three different CNFET geometries: top-gate, gate-all-around (GAA) and back-gate FETs. Despite significant efforts to realize increasingly sophisticated FET geometries (such as gate-all-around (GAA) [Franklin 2012, Chen 2008, Franklin 2013]), here we show that back-gate FET geometries provide major advantages that have not been exploited for highly scaled technologies: (1) back-gate FETs enable physical scaling beyond the limits of both top-gate and gate-all-around FET geometries, and (2) back-

gate FETs provide significant additional EDP benefits owing to reduction in parasitic capacitances compared to top-gate and GAA FETs.

2.2 Back-Gate FET Geometry Benefits

First, back-gate FETs enable physical scaling beyond both top-gate and GAA FETs for further reduced CGP, enabling more highly-scaled technology nodes. CGP corresponds to the gate pitch between two or more FETs connected in series with a shared source/drain contact; it is equal to the sum of the source/drain contact length (L_C), the physical gate length (L_G), and the two spacer regions ($2L_{SP}$) that separate the gate from the source/drain (Eq. 1).

Eq. 1: $$CGP = L_C + L_G + 2L_{SP}$$

For back-gate FETs, the spacer regions are not necessary to avoid unintended electrical contact between the gate and the source/drain (i.e., electrical shorts), since the back-gate is on a physically separate plane beneath the source/drain [Tulipe 2008, Doris 2015]. Therefore, there can be intentional overlap between the gate and the source and drain (which mathematically corresponds to $L_{SP} < 0$ in Eq. 1, shown in Fig. 2.1d). Thus, CGP can be reduced by decreasing L_{SP} (e.g., below zero) – even without improving fabrication techniques for scaling L_C and L_G.

2.3 Experimental Demonstration: 30 nm CGP CNFETs & Digital Logic

As an experimental demonstration, we fabricate back-gate CNFETs and digital logic from FETs that fit within a record-scaled CGP = 30 nm (Fig. 2.2). We use CNFETs because (1) the CNTs can be deposited over the pre-fabricated gate stack at room temperature (e.g., through solution-based processing [Cao 2013], in contrast to silicon channels which can require temperatures >1000 °C) [Vinet 2011, Sabry 2015], and (2) CNFETs are a leading and rapidly maturing contender for energy-efficient computing as high-performance devices and complete digital systems have been experimentally demonstrated [Wei 2009, Tulevski 2014, Sabry 2015, Shulaker 2017]. The fabrication flow for a back-gate CNFET is shown in Fig. 2.3. To achieve a

CGP of 30 nm, the CNFETs are patterned with L_C = 20nm, L_G=18nm, and L_{SP}=-4nm (i.e., 4 nm intentional overlap of the back-gate with the source and the drain), with a physical channel length (L_{CH}=CGP-L_C) of 10 nm. Scanning electron microscopy (SEM) and transmission electron microscopy (TEM) images of the fabricated devices are shown in Fig. 2.4. Importantly, this CGP scaling is achieved without additional scaling of L_G and L_C. This highlights how this approach can decouple the conflicting constraints on L_C and L_G (longer Lc and L_G can result in improved contact resistance and electrostatic control) from the constraints imposed by needing to aggressively scale CGP (ideally scaling both L_C and L_G). Fig. 2.5 shows electrical characterization of typical CNFETs and the measured voltage transfer curve from a CNFET inverter fabricated from 30 nm CGP CNFETs, illustrating functional operation. This digital logic comprises of FETs with the most-scaled CGP ever realized to date (Fig. 2.2).

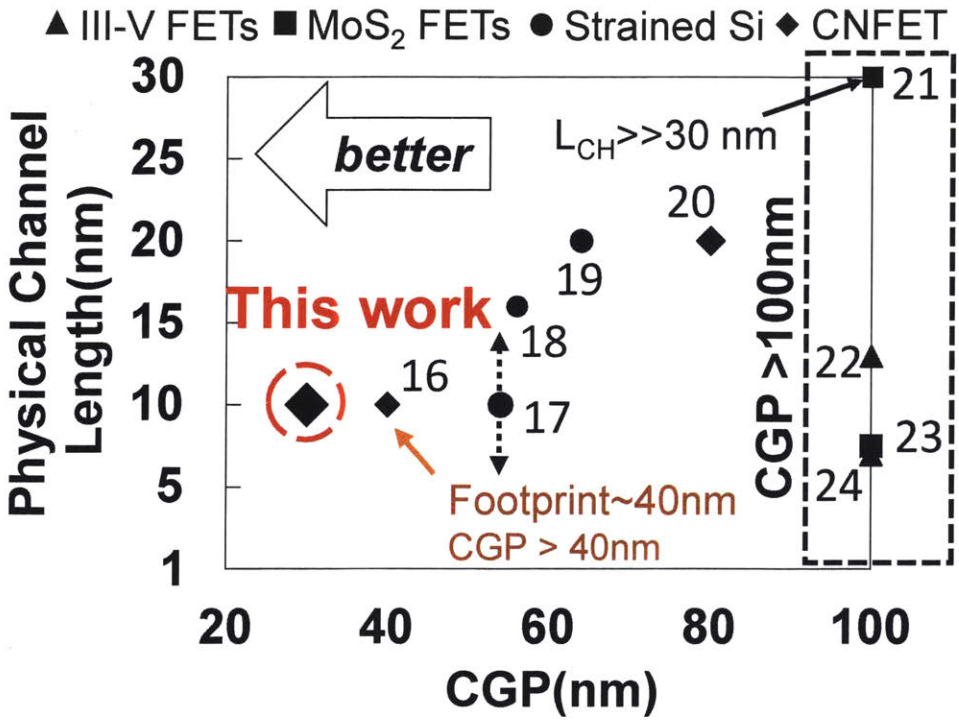

Fig. 2.2: Benchmarking current work with respect to contacted gate pitch across best reported scaled technologies in literature, references [16]-[24] are [Cao 2017, Mistry 2017, Narasimha 2017, Seo 2014, Qiu 2017, Desai 2016, Hahn 2017, Nourbakhsh 2016, Zhao 2017] respectively . [16] reports footprint, [17] doesn't report L_G or L_{eff} , [18] reports L_{eff}, [19] reports the gate length, [20-24] CGP data extracted from SEMs reported in respective papers.

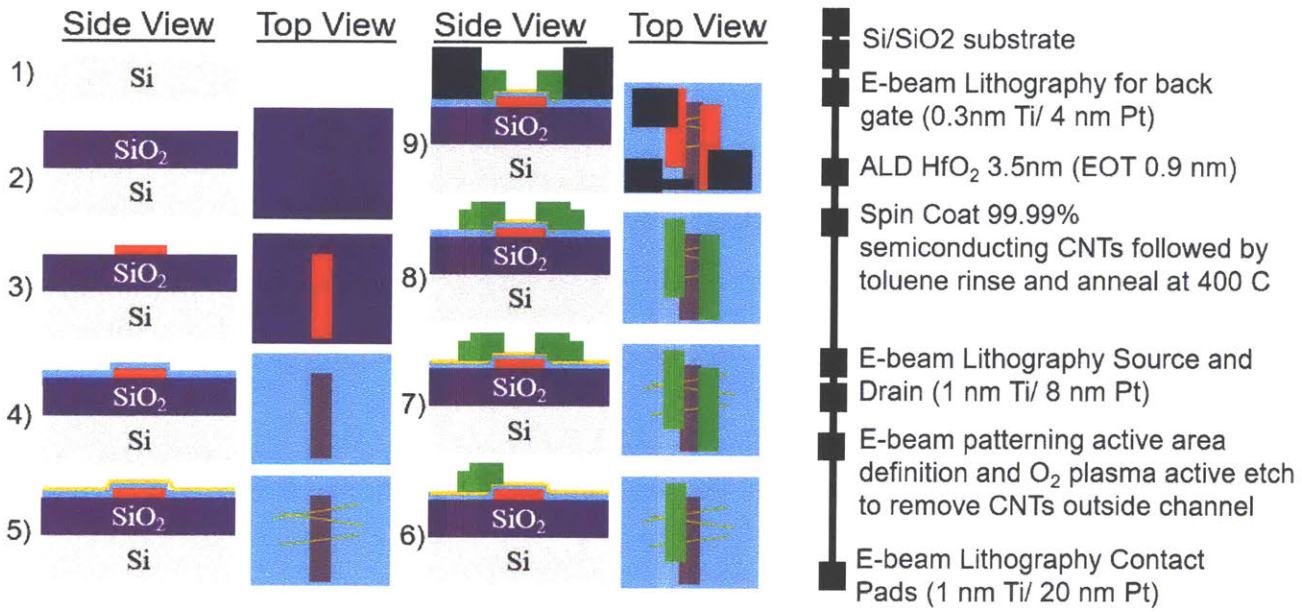

Fig. 2.3: Process flow of back-gate CNFETs. While back-gates are not embedded within the substrate, a conventional damascene process can be used to achieve the reduced parasitics for back-gate FET geometries. E-beam photoresist thickness (< 40nm) limits the metal thickness in our experimental demonstration to <10 nm.

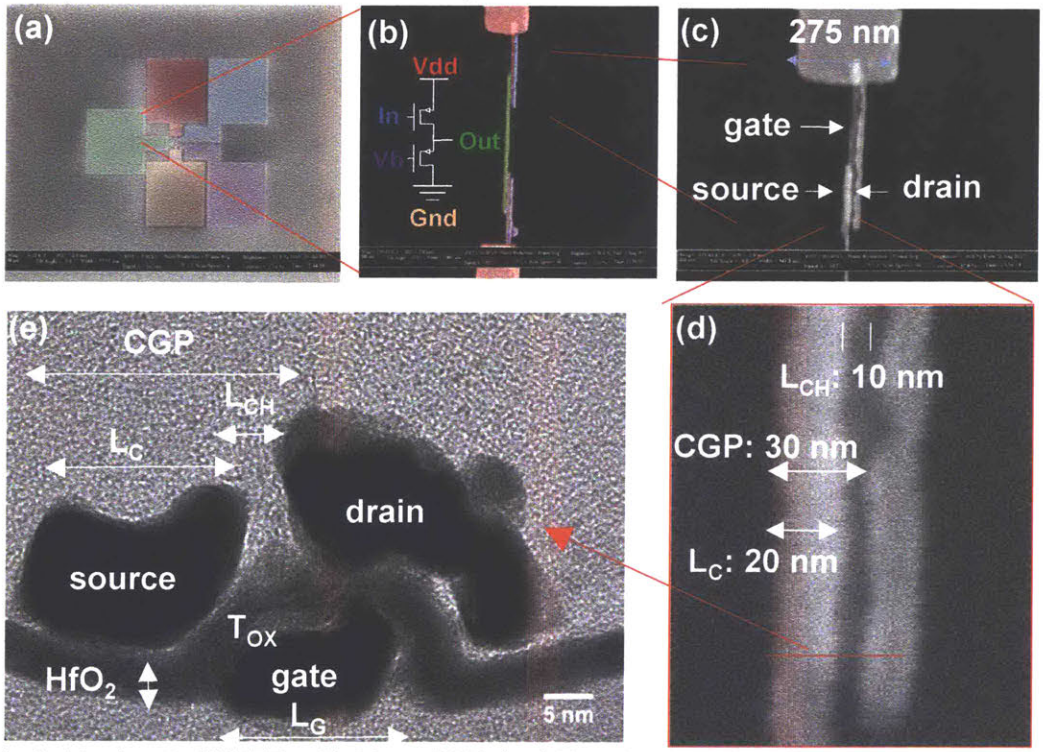

Fig. 2.4. Fabricated back-gate CNFETs with 30 nm CGP. (a-d) Top view scanning electron microscopy (SEM) images of typical 30 nm CGP back-gate CNFETs and CNFET digital logic (inverter). (a) Probe pad layout for the CNFET inverter (false colored). (b) Magnified view of a typical CNFET inverter, false colored to match the inverter schematic in (b), and the pads in (a). the image in (b) shows an inverter before the pads shown in (a) are deposited, since the

pads cover some of these features. (c) Magnified view of a typical back-gate CNFET comprising a CNFET inverter (shown in (b)). (d) Magnified view of the CNFET channel region. L_C is 20 nm and L_{CH} is 10 nm, resulting in a 30 nm CGP. The L_G is 18 nm, and overlaps both with the source (left contact) and drain (right contact) by ~4 nm. (e) Cross-section transmission electron microscopy (TEM) image of a back-gate CNFET with nominal 30 nm CGP.

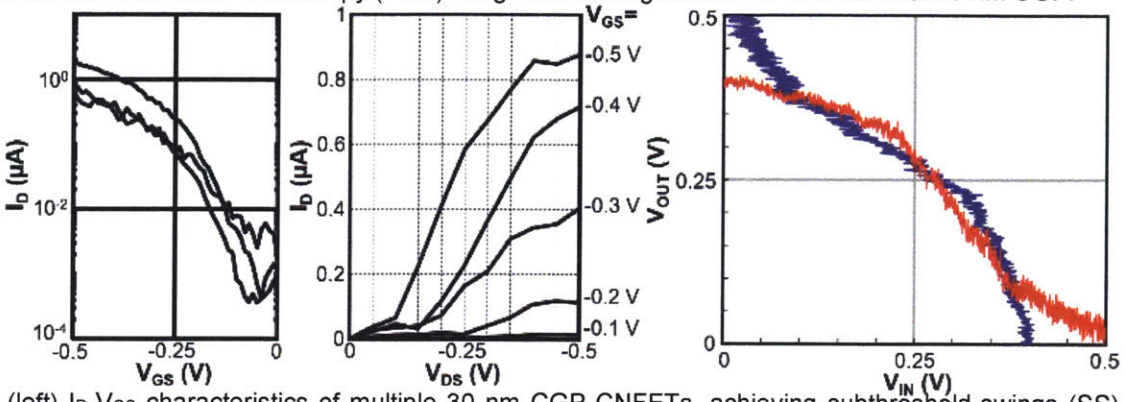

Fig. 2.5: (left) I_D-V_{GS} characteristics of multiple 30 nm CGP CNFETs, achieving subthreshold-swings (SS) of ~125 mV/dec (at V_{DS}=-0.5V). (middle) I_D-V_{DS} characteristic of sample 30 nm CGP CNFET. (right) Voltage transfer curve of a 30 nm CGP CNFET inverter, implemented using depletion load PMOS logic with V_{OH} = 0.4V V_{OL}= 0.05V respectively.

Importantly, the benefits of back-gate CNFETs extend beyond enabling continued scaling. Back-gate FET geometries simultaneously reduce parasitic capacitances (e.g., gate –to source/drain capacitance), resulting in additional EDP benefits for digital VLSI circuits. The reduced parasitic capacitances are due to decreased electrical coupling of the gate beneath the source/drain. As shown in Fig. 2.6, the parasitic capacitances for back-gate FETs is further reduced as CGP continues to scale (for the parameters in Table 2.1), resulting in major EDP benefits for digital VLSI circuits. To quantify these EDP benefits, we analyze physical designs of VLSI digital circuits from the processor core of OpenSPARC T2 [OpenSparc] and a 32-bit commercial processor core (Fig. 2.7). These processor cores incorporate many effects present in realistic VLSI circuits that do not appear in small circuit benchmarks *e.g.*, physical placement and routing congestion, wire parasitics, and buffer insertion to meeting circuit-level timing constraints [Hills 2015]. Due to reduced parasitic capacitances, back-gate CNFETs offer an average of 1.6× EDP benefit vs. top-gate CNFETs and 2.2× vs. GAA CNFETs. Importantly, these benefits are *in addition* to the substantial EDP benefits that top-gate CNFETs offer vs. Si FETs [Wei 2009, Tulevski 2014].

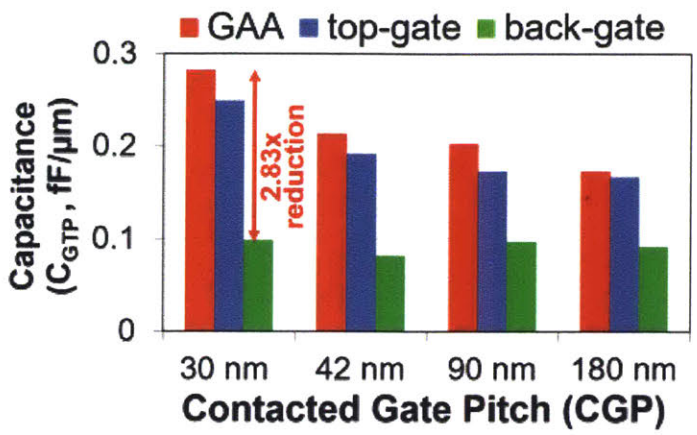

Table 2.1

CGP (nm)	30	42	90	180
L_G (nm)	9	9	24	45
L_{SP} (nm)	6	12	20	45
L_C (nm)	9	9	26	45
H_G (nm)	20	30	40	90
H_C (nm)	40	60	80	180
T_{OX} (nm)	2	2	3	4
K_{SPACER}	5.5	5.5	5.5	5.5
K_{OX}	10.3	10.3	10.3	10.3

Fig. 2.6: (left) Parasitic capacitances (gate-to-plug capacitance, C_{GTP} (Fig. 2.1) for back-gate vs. top-gate and GAA FET. Back-gate FETs reduces parasitics by >2.5× vs. top-gate and by >2.8× vs. GAA for a 30 nm CGP (suitable for a sub-3 nm node). Benefits of parasitic reduction increases as CGP scales. Intrinsic parasitics are determined using TCAD Sentaurus (Synopsys) and verified using COMSOL Multiphysics (COMSOL, Inc.) (with a discrepancy of <0.3% across all simulations). (right) Table 2.1: Device parameters used for analysis. CGP values of 30 nm, 42 nm, 90 nm, and 180 nm correspond to 3 nm, 7 nm, 22 nm, and 45 nm technology nodes, respectively [ITRS, Mistry 2017].

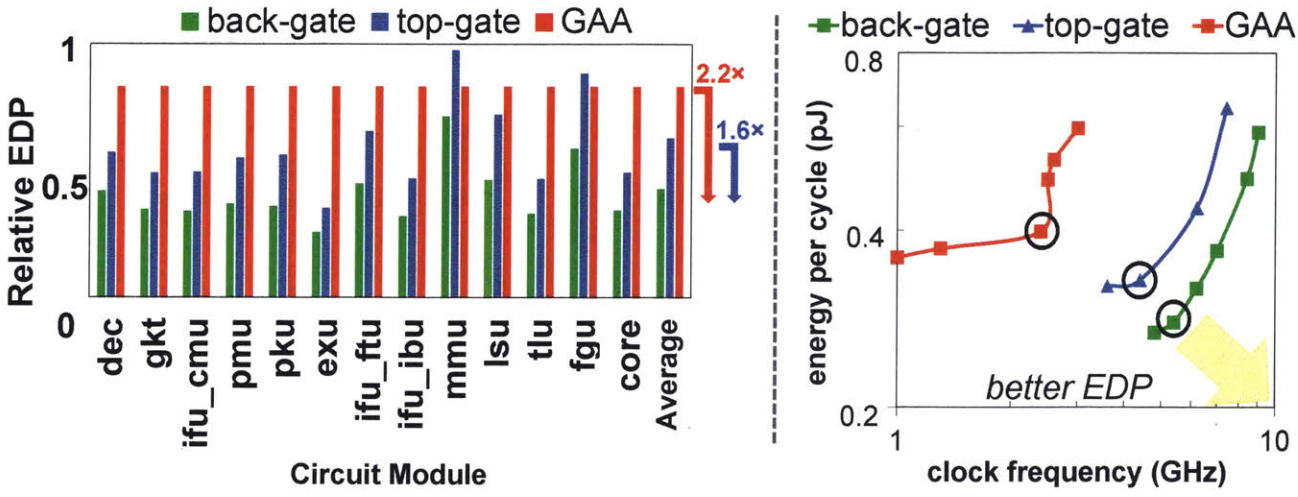

Fig. 2.7: (left) Optimized EDP (normalized with respect to the optimized EDP for the GAA CNFET for each module) across modules from the OpenSparc T2 core and a 32-bit commercial processor core. Average EDP benefit of back-gate vs. GAA is 2.18×, and 1.6× vs. top-gate. (right) Total energy vs. frequency of the 32-bit commercial processor core, showing the pareto-optimal EDP trade-off curves for back-gate, top-gate, and GAA CNFETs. Left figure is extracted from these EDP trade-off curves. All simulations are done with respect to a 30nm CGP device with

parameters listed in Table 2.1, Fig. 2.6. Importantly, EDP benefits are maintained even with low-k spacers (e.g., with a k=4.4 spacer [Yakimets 2017], EDP benefits decrease by <10% (dec module of OpenSparcT2). Moreover, for many existing standard cell libraries, the same physical layouts can be used for FETs with back-gate geometries without any adjustments to the locations of FETs or to the metal routing within standard library cells (specifically for standard cell layouts in which vias to contact FET gates are located outside of the active region of the FETs).

2.4 Additional Considerations

The EDP benefits resulting from reduced parasitics (above) outweigh potential gains stemming from improved electrostatic control for GAA geometries (*e.g.*, the subthreshold-swing (SS) for the back-gate CNFET can degrade from ~60 mV/decade to ~100 mV/decade, while still maintaining EDP benefits compared to GAA CNFETs with nearly ideal SS approaching 60 mV/decade as demonstrated in Fig. 2.8)

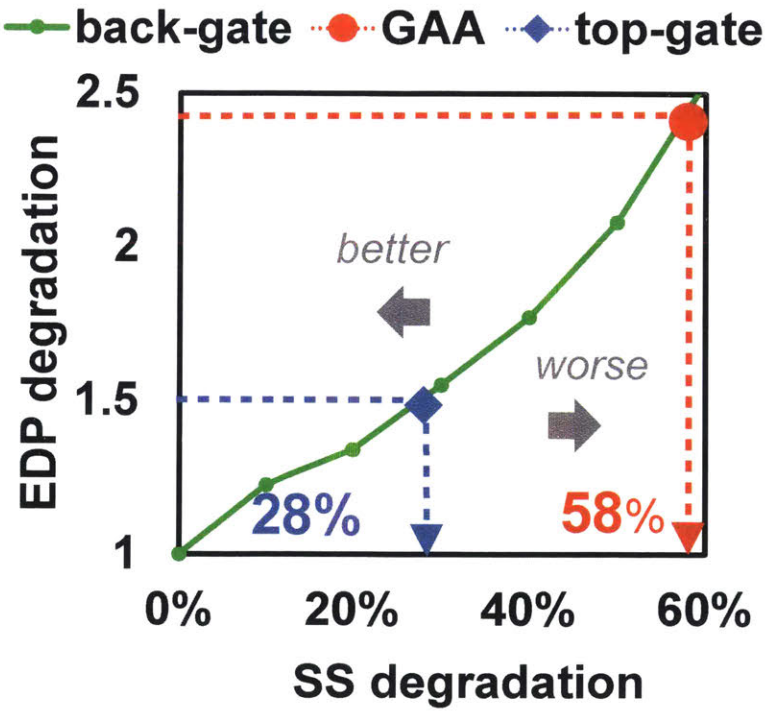

Fig. 2.8: EDP benefits resulting from reduced parasitics outweigh potential gains stemming from improved electrostatic control for GAA geometries. Subthreshold swing (SS) can degrade by > 58% (resulting in SS = 100mV/dec), while still maintaining the EDP benefits compared to GAA CNFETs with assumed ideal SS approaching 60 mV/dec. Importantly, experimental demonstrations of CNFETs with L_{CH} = 9nm have leveraged back-gate geometries and reported a SS better than 100 mV/dec (94 mV/dec), highlighting feasibility of this approach [Franklin 2012a].

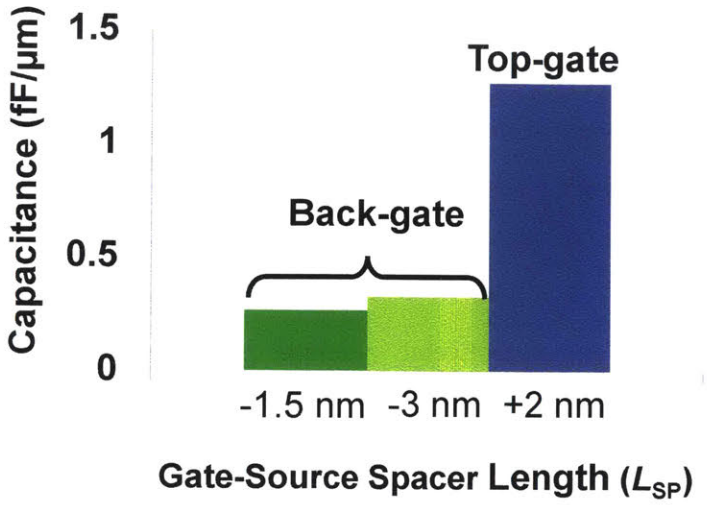

Table 2

CGP (nm)	15	15	15
L_G (nm)	9	9	5
L_{SP} (nm)	-1.5	-3	+2
L_C (nm)	9	9	6
H_G (nm)	15	15	15
H_C (nm)	30	30	30
T_{OX} (nm)	2	2	2
K_{SPACER}	5.5	5.5	5.5
K_{OX}	10.3	10.3	10.3

Fig. 2.9: Paths for realizing 15 nm CGP. Extraction of parasitic capacitance (C_{GTP}) for the top-gate FET, as well as back-gate FETs assuming a 3 nm overlap between the gate and source/ drain and 1.5 nm overlap between the source/ drain. Even with overlap, back-gates will yield >3× reduced parasitic capacitances at scaled nodes. Table 2.2 shows device parameters used for Fig. 9.

In addition to showing scalability to a 30 nm CGP, this approach allows scaling to sub-20 nm CGP, using technology parameters that have already been achieved experimentally (Fig. 2.9). For instance, a 9 nm L_G [Franklin 2012a], a 9 nm L_C [Cao 2015], and an overlap of the gate and the source and drain ($-L_{SP}$) of 3 nm would result in a CGP of 15 nm. Importantly, even when assuming an overlap of the gate with the source and drain (the key to achieving a scaled CGP) for back-gate FETs, the parasitics can still be less compared to a conventional top-gate FET at the same CGP (Fig. 2.9). The overlap of 3 nm is chosen because (1) it enables 15 nm CGP given experimentally realized dimensions for L_C and L_G and (2) it exceeds the projected lithographic overlap accuracy [ITRS], ensuring that some section of the gate will be under the entire channel to maintain electrostatic control. For such aggressively scaled sub-20 nm CGPs, EDP benefits degrade compared to 30 nm CGP, though still maintain EDP benefits compared to 30 nm CGP top-gate CNFETs (Fig. 2.10).

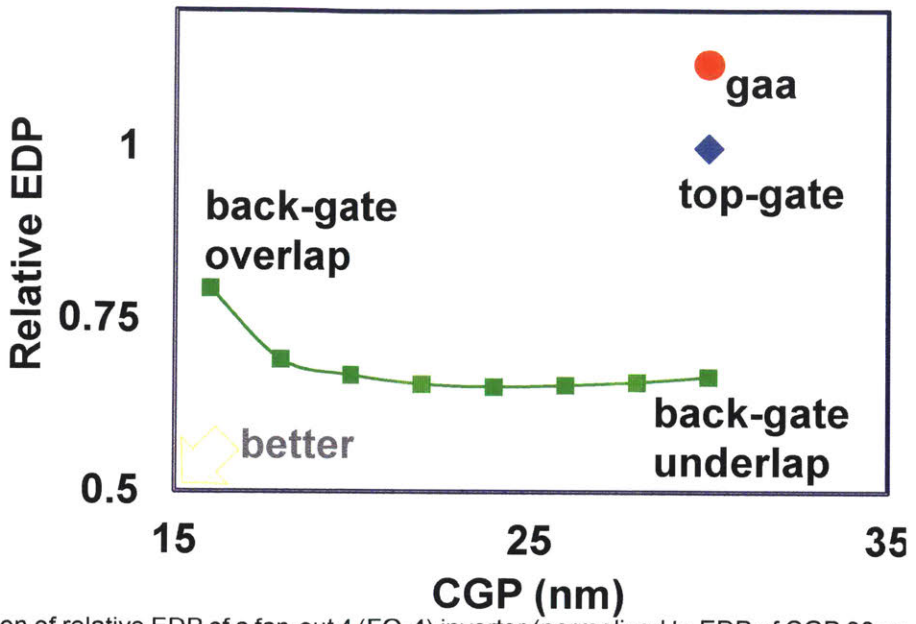

Fig. 2.10: Comparison of relative EDP of a fan-out 4 (FO-4) inverter (normalized to EDP of CGP 30nm top-gate CNFET) vs CGP of back-gate CNFETs (all devices have contact length of 9nm and gate length of 9nm, L_{SP} is varied to reduce CGP).

2.5 Conclusion

We experimentally demonstrate record-scaled 30 nm CGP FETs and digital logic, leveraging back-gate CNFETs. We rigorously quantify the benefits of back-gate CNFETs by analyzing physical designs of digital VLSI circuits, showing that this approach provides additional EDP benefits vs. top-gate and GAA CNFETs due to reduced parasitic capacitances. Furthermore, this approach is applicable to a wide range of FETs using emerging channel materials (such as 1D and 2D nanomaterials) provided that: 1) they can be fabricated at low temperatures (*e.g.*, <400 °C, including channel deposition and subsequent FET processing), and 2) the channel is nanometer-thin for ideal electrostatic control using the back-gate. Thus, we demonstrate significant benefits of back-gate FETs, illustrating that they should be seriously considered for future highly-scaled and energy-efficient digital electronics.

Chapter 3: Gate geometry engineering for improved CNFETs

3.1 Background

While back-gate CNFETs promise substantial energy efficiency benefits for digital VLSI circuits (as discussed in Chapter 2), experimental demonstrations of CNFETs often exhibit significant off-state leakage current. Excess off-state leakage current results in increased leakage power dissipation and potential incorrect logic functionality in digital circuits; therefore, this off-state leakage current must be addressed in order the realize the benefits promised by CNFETs. Here, we provide insight into the underlying cause behind this leakage current, experimentally demonstrating that it stems from gate-induced drain leakage (GIDL). Moreover, we demonstrate a path for mitigating this GIDL current by leveraging the same back-gate geometries discussed above, but with *asymmetric* gates: back-gate CNFETs whose gate overlaps the source but not the drain. We experimentally demonstrate this approach reduces off-state leakage current by >60× at the same bias voltage (implemented across a wide range of CNFETs with channel length spanning 180 nm to > 1μm), while our calibrated models show potential benefits exceeding 10^6×. This reduced leakage current due to the asymmetric gates translates to additional energy-efficiency benefits for CNFETs. Thus this work addresses a key challenge facing CNFET-based electronics and is similarly applicable to a wide range of emerging 1D and 2D nanomaterials.

Fig. 3.1a shows the schematics and measured electrical transfer characteristics (I_D-V_{GS}) of a typical back-gate CNFET. All CNFETs in this work are fabricated as back-gate CNFETs, using >99.9% pure semiconducting CNTs [Nanointegris]). CNTs dispersed in solution are deposited at room temperature over a pre-fabricated high-k metal gate stack (defined by electron-beam lithography). Following deposition of the CNTs, source and drain contacts are aligned to the pre-fabricated gate stack and lithographically defined. CNTs outside of the channel region of the CNFETs are removed by etching with oxygen plasma. A detailed process flow is shown in appendix, Fig. A1.1.

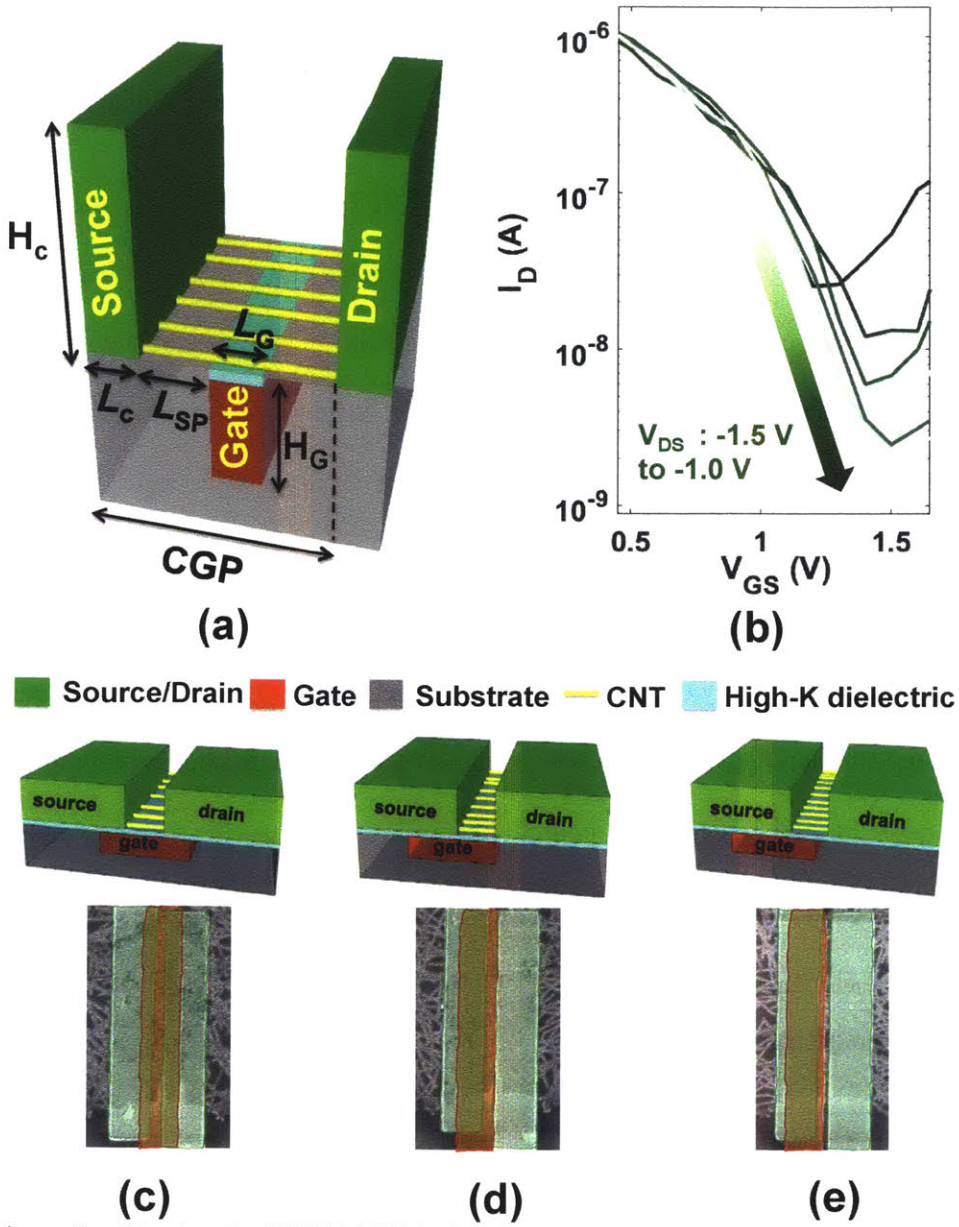

Figure 3.1. (a) Schematic of back-gate CNFET. LCH is the physical channel length, Lsp is (use definition from text), etc.. (b) Experimentally measured I_D-V_{GS} characteristics for a transistor with L_{CH}=180nm (measured at room temperature). Device parameters listed in Table 1. (c-e). Schematics of symmetric vs asymmetric CNFETs, together with matching scanning electron microscopy (SEM) images of fabricated CNFETs. (c) Symmetric back-gate CNFET with the gate overlapping the source and drain, (d) Asymmetric back-gate CNFET with the same gate length and contacted gate pitch (CGP) as (c), but with the gate laterally shifted to achieve zero overlap between the gate and drain, (e) Asymmetric back-gate CNFET with the same gate length and contacted gate pitch (CGP) as (c), but with the gate laterally shifted to achieve an intrinsic CNT region between the gate and drain.

3.2 Leakage Current in CNFETs

Although CNFETs are a rapidly maturing contender for energy efficient computing [Wei 2009, Shulaker 2017, Tulevski 2014, Chang 2012, Sabry 2015], measurements of experimental CNFETs often exhibit significant off-state leakage current. This leads to increased leakage power dissipation and potential incorrect logic functionality. To understand this off-stage leakage behavior, we characterize CNFETs across a range of different biasing conditions (gate potential, V_{GS}, and drain potential, V_{DS}) and physical geometries (channel lengths, L_{CH}). Fig. 3.2a-e shows the I_D-V_{GS} characteristics of CNFETs with L_{CH} spanning 2 μm down to 180 nm. As is typical, all of the CNFETs demonstrate exponential rise in off-state leakage current with increasing V_{DS} [Brady 2016, Qiu 2017]. While this off-state leakage current is often attributed to short channel effects[b] (such as drain-induced barrier lowering, DIBL), short channel effects cannot be the predominant source of the increased off-state leakage current due to: (1) increasing off-state leakage current does not occur in tandem with degrading inverse subthreshold slope[c] ; in contrast, inverse subthreshold slope remains constant, and (2) increasing off-state leakage current with increasing V_{DS} occurs independent of the CNFET channel length (and occurs even at large channel lengths of >1 μm). Rather, this increased off-state leakage current is indicative of Gate-Induced Drain Leakage (GIDL, Fig. 3.3). GIDL occurs at large gate-to-drain bias, when there is sufficient energy-band bending near the drain of the channel that valence band electrons can tunnel into the conduction band (referred to as band-to-band tunneling, BTBT, illustrated in appendix A5). In schottky barrier FETs [Zhang 2002, Lin 2001, Tsui 2005, Husain 2009] (such as CNFETs where the conduction of the FET is determined by the height of the schottky barrier of the metal to the semiconducting channel), this GIDL behavior is caused by parasitic schottky barrier tunneling [Zhang 2002, Lin 2001, Tsui 2005, Husain 2009] near the drain end of the channel (appendix A5). Illustrated in Fig. 3.3a, parasitic schottky barrier tunneling occurs when a large gate-to-drain bias reduces the schottky barrier

[b] Short-channel effects such as drain-induced barrier lowering (DIBL), velocity saturation, hot carrier injection, etc., degrade electrical characteristics in MOSFETs and occur when the channel length is comparable to the depletion width of source and drain junctions. [Veeraraghavan 1989]

[c] Inverse sub-threshold slope is defined as the inverse of rate of change of I_D with V_{GS} in transfer characteristics.

tunneling width, resulting in exponentially increasing electron injection through the schottky barrier (even when the FET is biases in the off-state). These tunneling current resulting from GIDL result in the exponentially increasing off-state leakage current at large gate-to-drain biases.

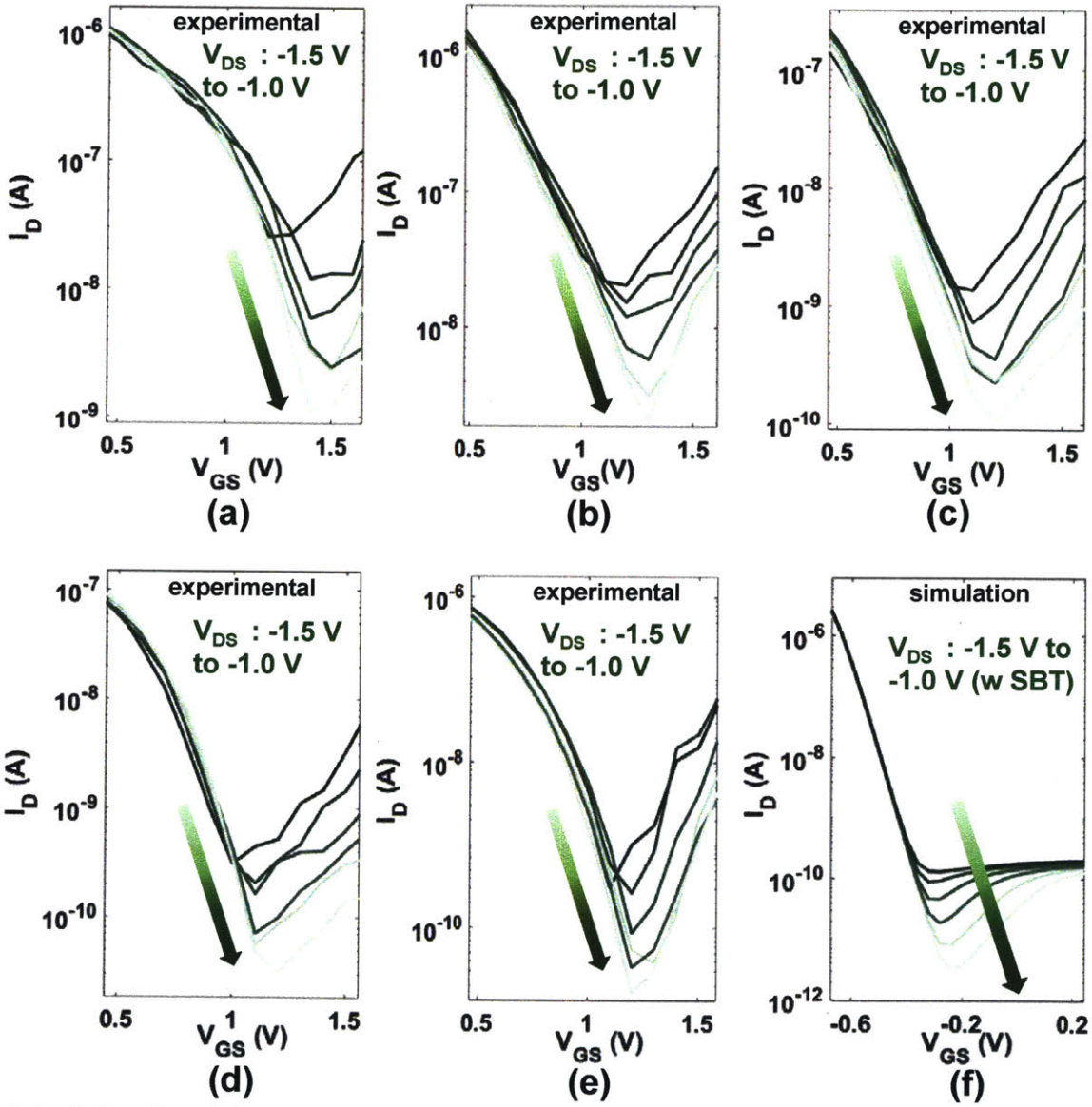

Figure 3.2. (a-e) Experimental room temperature I_D-V_{GS} plots for CNFETs fabricated with a range of different channel lengths (L_{CH}). From (a) through (e), the channel lengths are: 180 nm, 500 nm, 1 μm, 1.5 μm, and 2 μm, respectively. The V_{DS} varies from -1.8 V to -0.1 V (dark green to light green curves), and Table 3.1 lists the device parameters. (f) Simulated I_D-V_{GS} of a CNFET with L_{CH} =180nm using TCAD Sentaurus. The simulated device structure has the same dimensions as the experimental device shown in figure 2a with L_{CH} = 180nm [experimental parameters listed in Table 3.1, device parameters used listed in Table 3.2]. The simulated CNFET exhibits the same trends in I_{OFF} as the measured CNFETs.

While GIDL has been studied extensively in bulk semiconductors (such as silicon, silicon-germanium, and III-V compound semiconductors), this GIDL-induced leakage behavior exhibited by CNFETs has not been previously discussed or incorporated into device-level models [Lee 2015, Deng 2007, Wei 2009, Luo 2013]. To investigate the detailed physics responsible for this excess off-state leakage current, we develop a CNFET model in TCAD sentaurus [Sentaurus] which includes the effect of this GIDL-induced leakage behavior[d] (Supplemental Information). Fig. 3.2f shows the I_D-V_{GS} characteristics of the back-gate CNFET device model from Sentaurus Device. Our simulations (Fig. 3.2f) closely match experimental I_D-V_{GS} characteristics (Fig. 3.2a), with exponential rises of I_{off} with increasing gate-to-drain baises. Thus, it indicates GIDL is responsible for this excess off-state leakage current.

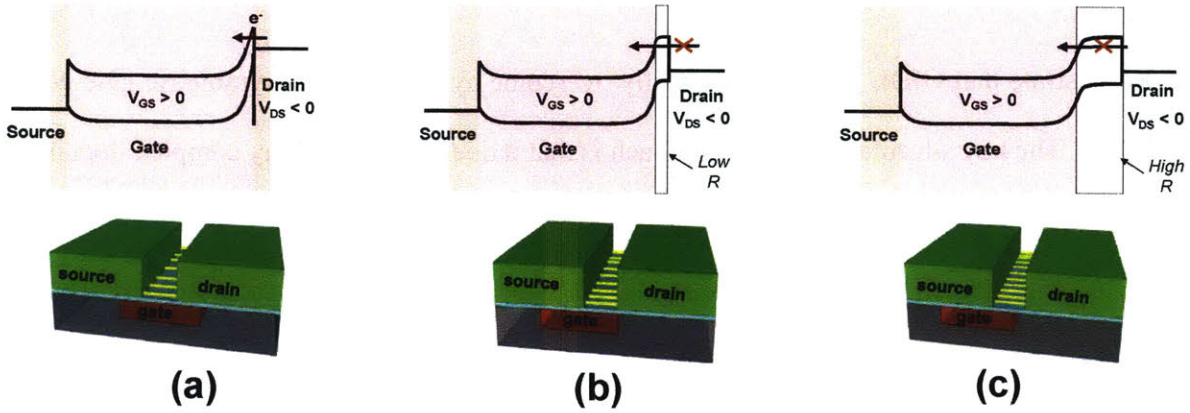

Figure 3.3. (a-c) Energy band diagrams for a symmetric, asymmetric gate CNFET (with a thin intrinsic CNT region) and asymmetric gate CNFET (with a large intrinsic CNT region). The energy-band diagrams are shown for $V_{GS} > 0$ V and $V_{DS} < 0$ V to highlight the presence (or lack there-of) of GIDL (e.g., the difference in tunneling width through the schottky barrier and consequently lower I_{OFF} for the asymmetric CNFETs).

3.3 Asymmetric Back-Gate CNFETs

With understanding of the source of off-state CNFET leakage current, we next propose and experimentally demonstrate a path for overcoming it. Several approaches for overcoming GIDL have been pursued with current silicon and III-V based technologies, all with the aim of reducing the electric field near the drain. For

[d] Sentaurus device [Sentaurus] solves a system of coupled poisson, electron and hole continuity equations in presence of Hurkx tunneling model [Hurkx 1992], to estimate the parasitic schottky barrier tunneling near the drain end and model this GIDL like behavior (more discussion in supplementary information).

instance, FETs with relaxed access regions (*i.e.*, extension regions) or, undoped spacer regions [Zhang 2002, Lin 2001, Lin 2013, Kerber 2013, Chen 1992, Yuan 2008, Lee 2013, Choi 2003] limit the electric field near the drain end of the channel (appendix A5), thereby suppressing this excess off-state leakage current. However, these techniques suffer from several drawbacks: they require complicated dopant profile engineering [Lin 2013, Kerber 2013, Chen 1992, Yuan 2008, Lee 2013, Choi 2003] accomplished through interstitial doping [Beyer 1977], and increase the total device footprint area due to the additional spacer regions between the gate and the drain (defined by contacted gate pitch[e] (CGP) [Lin 2001, Lin 2013, Lee 2014]). Moreover, carbon nanotubes cannot be doped using interstitial doping [Appenzeller 2005] as it damages the pristine CNT lattice, making these previous techniques non-applicable to CNFETs.

Here we demonstrate that GIDL can be successfully overcome by engineering asymmetric gate geometries within CNFETs. The key advantages of this approach is that it does not require any complex dopant profiles nor does it impact the total device footprint area. Figures 1c-e illustrate a range of CNFETs with different gate geometries. Fig. 3.3a shows a conventional CNFET with a *symmetric* gate geometry whereby the gate spans the entire CNT channel, overlapping equally with the source and drain electrodes [Shulaker 2013, Shulaker 2017]. It is this overlap in the gate and drain that results in large electric fields in the schottky barrier near the drain contact (Fig. 3.3a), leading to excess off-state leakage current. In contrast, Fig. 3.3b-c illustrate CNFETs with *asymmetric* gate geometries, whereby the gate is shifted away from the drain towards the source. With enough lateral shift, the gate eventually does not overlap at all with the drain, resulting in an intrinsic section of CNTs self-aligned to the drain contact. This section of intrinsic CNT prevents the high electric field near the drain even at large gate-to-drain biases, suppressing GIDL-induced leakage (Fig. 3.3b-c). Importantly, this approach is accomplished without any additional processing steps as it is implemented entirely during the lithographic patterning of the gate and drain which occurs regardless.

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[e] Contacted Gate Pitch or CGP is defined as the sum of the source/drain contact length (L_C), the physical gate length (L_G), and the two spacer regions ($2L_{SP}$) that separate the gate from the source/drain (Eq. 1, Fig. 3.1).

Eq. 1: $CGP = L_C + L_G + 2L_{SP}$

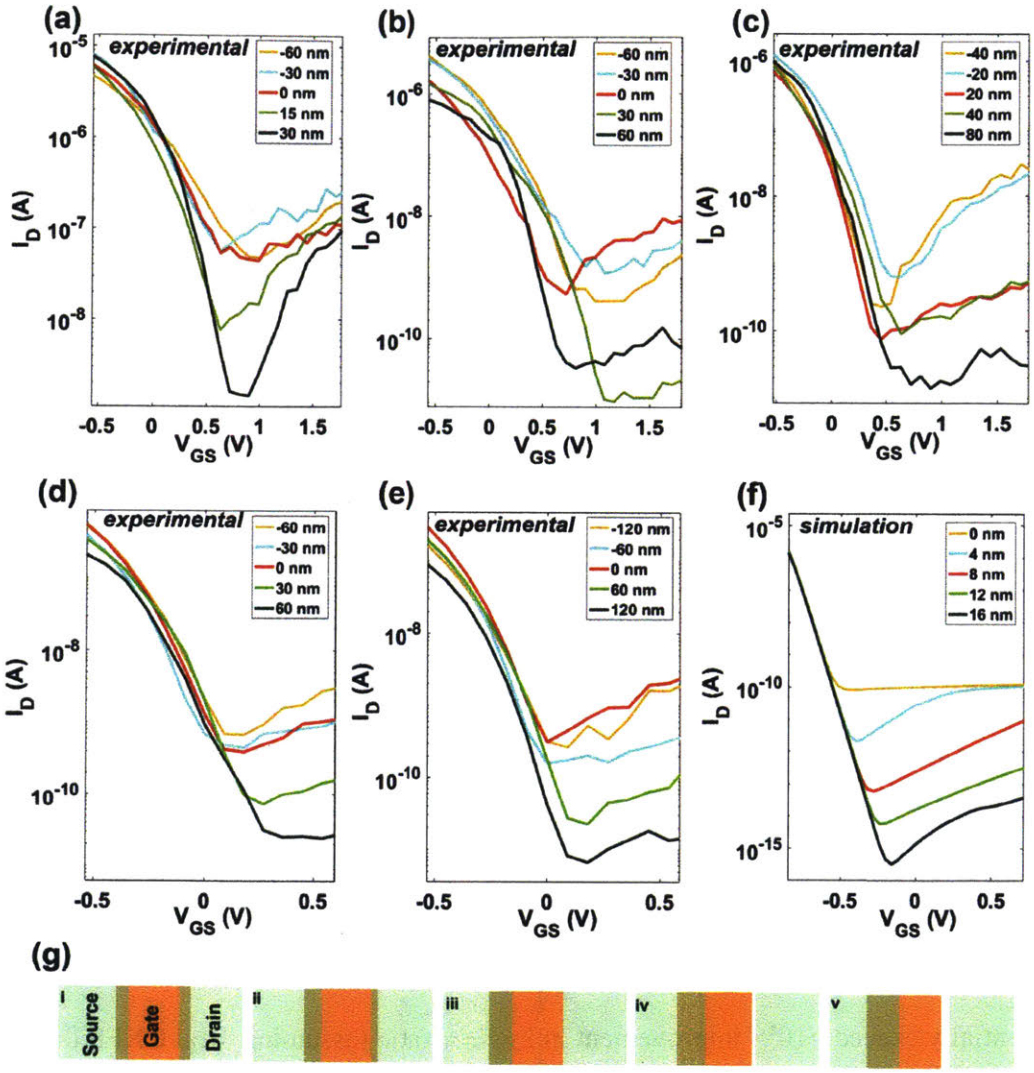


Figure 3.4. (a-e) Experimental I_D-V_{GS} characteristics of back-gate CNFETs with varying L_{SP} [defined in Figure 1a], showing an average reduction of I_{off} by ~60×, and with average improvement in I_{on}/I_{off} by ~30×. Similar to Fig. 3.2, from (a) through (e), the channel lengths are: 180 nm, 500 nm, 1 μm, 1.5 μm, and 2 μm, respectively. (f) Simulated I_D-V_{GS} characteristics of the symmetric vs progressively asymmetrically back-gate CNFETs with varying L_{SP}. Table 3.2 lists the device parameters used for the device model. See Supporting Information for additional information on the simulations. (g) Schematic of symmetric vs asymmetric back-gate CNFETs for the different CNFETs plotted in (a) through (e).

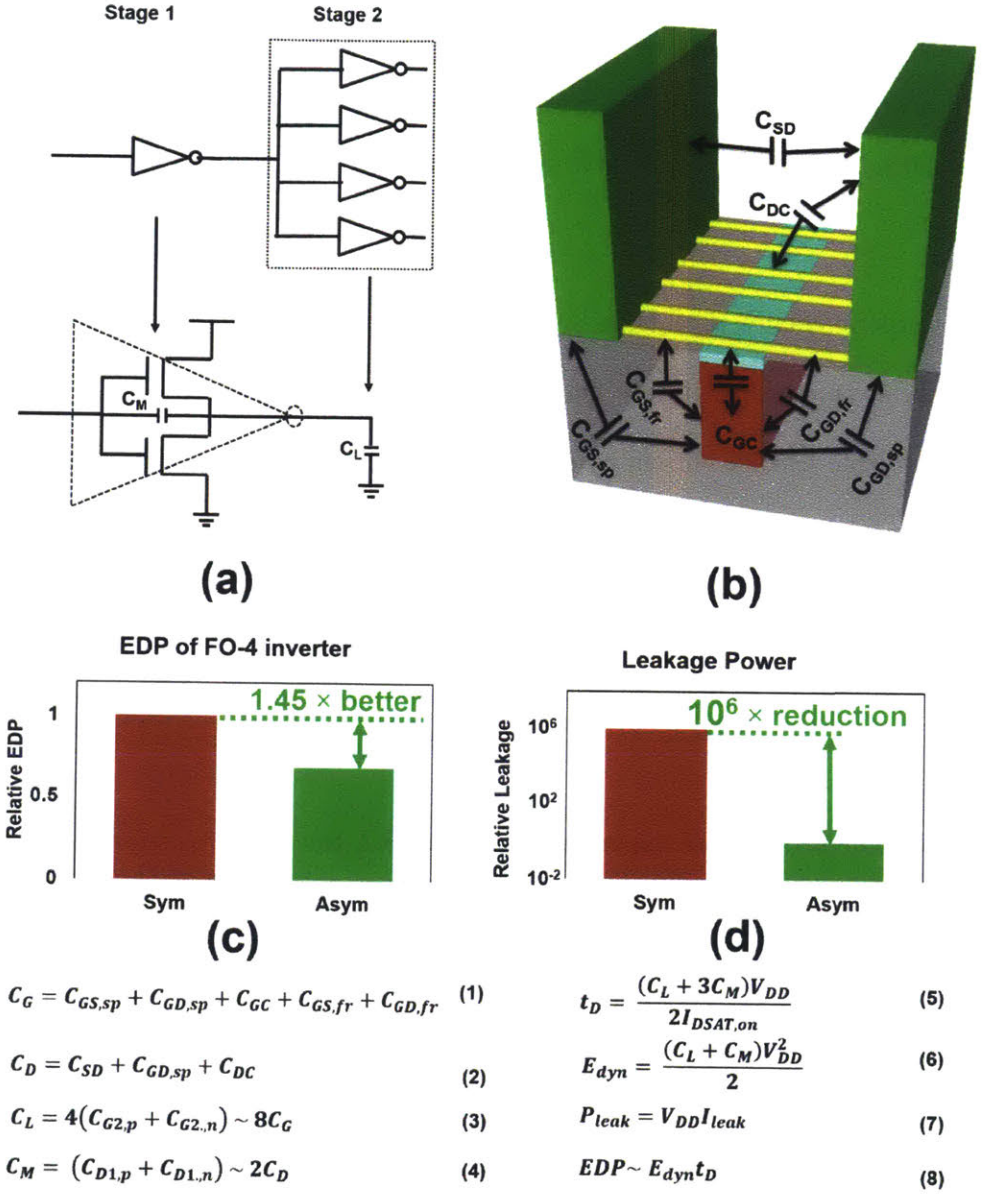
Scanning electron microscopy (SEM) images of fabricated CNFETs ranging from symmetric gate CNFETs to CNFETs with varying degrees of asymmetry in the gate structure (*i.e.*, varying amounts of lateral shifts

away from the drain) are shown in Fig. 3.1c-e. The varying amounts of lateral shifts are introduced during lithographic patterning of the gate, and are quantified by the length of the intrinsic CNT region (L_{SP}, Fig. 3.1a) separating the gate and drain. Similar to Fig. 3.3, we measure the experimental I_D-V_{GS} characteristics for CNFETs with varying channel lengths (L_{CH} = 2 μm down to 180 nm). Fig. 3.4 shows typical I_D-V_{GS} characteristics for these devices, including both symmetric and asymmetric CNFETs. As illustrated in Fig. 3.4, all symmetric CNFETs (and all CNFETs where there is no CNT intrinsic region) suffer from substantial GIDL-induced off-state leakage current. In stark contrast, asymmetric gate CNFETs (with $L_{SP} > 0$ near the drain), have reduced off-state leakage current: the average I_{OFF} reduction exceeds 60× compared to symmetric gate CNFETs, demonstrating the benefits of this approach. Importantly, having large ungated intrinsic CNT regions near the drain introduces additional channel resistance which degrades on-state current (I_{ON}). However, the overall I_{ON}/I_{OFF} ratio, a key metric for device performance, improves by over an order of magnitude: the 60× reduction in I_{OFF} corresponds with an average I_{ON} degradation of <2×, resulting in an overall benefit in I_{ON}/I_{OFF} by >30× (supplemental information). Additionally, we replicate these results with our CNFET model that captures GIDL, simulating matching symmetric and asymmetric gates as our experimental CNFETs in Fig. 3.4. Our simulation results validate the experimental data (Fig. 3.4a), predicting substantial decreases in off-state leakage current at a minor cost in on-state current. In fact, the model predicts gains can potentially exceed $>10^6$× improvement in I_{ON}/I_{OFF} ratio (assuming ideal CNFET performance).

3.4 Additional Benefits : Energy Efficiency

Moreover, the asymmetric gate geometry also affects the parasitic capacitances of the CNFETs. As the gate laterally shifts further from the drain towards the source, the parasitic source capacitance increases while the parasitic drain capacitance decreases (Fig. 3.5). To analyze the circuit-level impact of these asymmetric gates, we analyze a fan-out 4 inverter (Fig. 3.5a) using extracted device parameters from the TCAD Sentaurus simulations. Due to the reduced parasitic drain capacitance (the effect of which is amplified as the impact this capacitance has on the circuit is amplified due to the Miller Effect [Sedra 1998, Rabaey 2002, Andreev

2006]), the asymmetric CNFETs actually yield a slight (~1.45×) benefit in energy-delay product (EDP, a metric of energy-efficiency) versus symmetric CNFETs[f].



$$C_G = C_{GS,sp} + C_{GD,sp} + C_{GC} + C_{GS,fr} + C_{GD,fr} \quad (1)$$

$$C_D = C_{SD} + C_{GD,sp} + C_{DC} \quad (2)$$

$$C_L = 4(C_{G2,p} + C_{G2,n}) \sim 8C_G \quad (3)$$

$$C_M = (C_{D1,p} + C_{D1,n}) \sim 2C_D \quad (4)$$

$$t_D = \frac{(C_L + 3C_M)V_{DD}}{2I_{DSAT,on}} \quad (5)$$

$$E_{dyn} = \frac{(C_L + C_M)V_{DD}^2}{2} \quad (6)$$

$$P_{leak} = V_{DD}I_{leak} \quad (7)$$

$$EDP \sim E_{dyn}t_D \quad (8)$$

Figure 3.5. (a) Schematic of a FO-4 (fan-out 4) inverter with highlighted load capacitance and miller capacitances. (b) Schematic of a back-gate CNFET, highlighting parasitic source and drain capacitances (C_{GS} and C_{GD} respectively). (d) Energy-delay product (EDP) of a FO-4 inverter design with symmetric and asymmetric gate CNFETs. EDP defined in Equation 8. Equations 1-7 are used to calculate dynamic energy, delay and leakage power (considering miller

[f] Here, we analyze the impact for fan-out 4 inverters, although digital systems would also account for Miller Effect in other combinational and sequential logic gates. However, it is important to note that we show there is not an EDP degradation due to the change in capacitances for asymmetric FETs.

capacitances [Sedra 1998, Rabaey 2002, Andreev 2006]). Improvement in the miller capacitances (Fig. 3.5c) for asymmetric CNFETs lead to a 1.45× improvement in EDP. (e) Comparison of simulated leakage power of a FO-4 inverter for the symmetric vs asymmetric gate technologies. Fig. 3.5(c-e) are calculated using extracted device parameters from Sentaurus device simulations for a symmetric and asymmetric back-gate CNFET. For the symmetric back-gate CNFET, we assume 120 nm gate overlap with the source and drain, whereas for the asymmetric back-gate CNFET, the gate is offset from the drain by 16 nm (e.g., L_{SP} = 16 nm).

3.4 Conclusion

In this work, we experimentally reveal the significant impact of GIDL on CNFETs, and provide an experimentally-calibrated model that closely matches our measured results. Moreover, we demonstrate a path for mitigating this off-state leakage current by engineering CNFET geometries with asymmetric gates. We experimentally demonstrate this approach reduces off-state leakage current by >60× while our calibrated models show potential benefits exceeding 10^6×. Thus, this work addresses a key challenge facing CNFET-based electronics, and demonstrates a promising path towards realizing energy efficient CNFET VLSI digital circuits.

Table 3.1. Device Parameters used in experiment

L_{CH}(μm)	0.09	0.18	0.5	1	1.5	2
L_G (μm)	0.33	0.42	0.74	1.24	1.74	2.24
L_C (μm)	0.5	0.5	2	3	3	3
H_G (nm)	15	15	15	15	15	15
H_C (nm)	25	25	25	25	25	25
T_{OX} (nm)	10	10	10	10	10	10
Width(μm)	2	2	2	2	2	2

Table 3.2. Device Parameters used in simulation.

L_{CH}(μm)	0.18
L_G (μm)	0.42
L_C (μm)	0.5
H_G (nm)	15
H_C (nm)	25
T_{OX} (nm)	10
K_{SPACER}	5.5
K_{OX}	10.3

Chapter 4: Negative Capacitance Carbon Nanotube FETs

4.1 Background

While scaling FETs have improved energy efficiency of digital VLSI circuits for decades (e.g., Dennard scaling [Dennard 1974]), continued scaling is resulting in diminishing returns [Bardon 2016]. For instance, circuit supply voltage (V_{DD}) is no longer scaling according to Dennard Scaling, in part due to room temperature sub-threshold slope (SS) theoretical limit of 60 mV/decade as a result of Boltzmann statistics of carriers (which is in itself difficult to achieve due to short channel effects) [Kuhn 2012, Jan 2015]

To overcome these challenges, multiple orthogonal paths are being pursued. One promising option, as discussed above, is to replace today's silicon-based FET channels with ultra-thin body nanomaterials, such as CNTs used to realize CNFETs (Fig. 4.1a), which offer superior electrostatic control vs silicon-based FETs, simultaneously with superior carrier transport [Tans 1998]. Another promising option is to introduce new materials into the FET gate stack, e.g. ferroelectric (FE) materials that exhibit negative capacitance (NC) effects which can act as an internal step-up voltage transformer in the gate dielectric leading to voltage amplification from V_G to internal channel potential Ψ_S. This stems from the stored energy in phase transition of unstable ferroelectric oxides stabilized by a standard positive gate dielectric capacitances. This allows the circuit drive voltage (V_{DD}) to decrease, thus lowering energy consumption while maintaining high effective gate-to-source voltage ($V_{GS,eff}$) for high drive current and high on-off ratio [Salahuddin 2007, Zhirnov 2008]. Here we show that NC can be combined with carbon nanotubes to realize NC-CNFETs, as a promising path towards future generations of energy efficient digital VLSI systems.

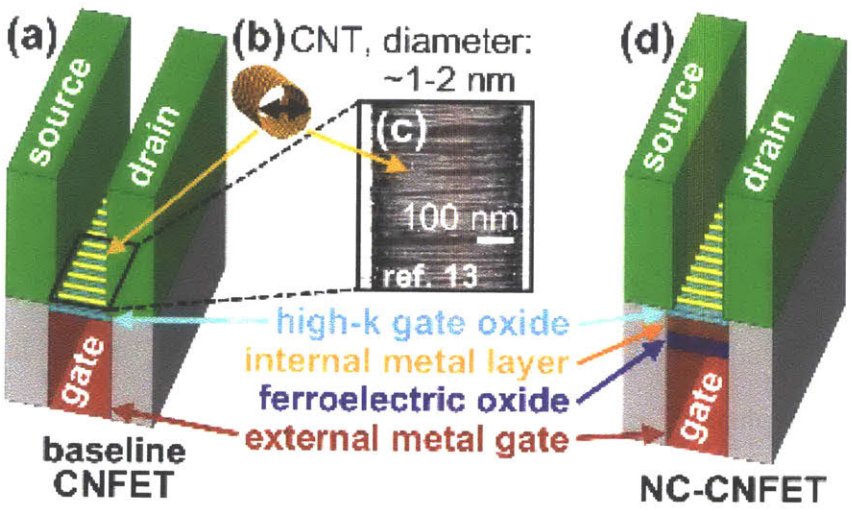


Figure 4.1. (a) Schematic of a baseline CNFET. (b) CNT. (c) SEM of CNFET channel region. (d) Schematic of NC-CNFET

The schematic of an example NC-CNFET is shown in Fig. 4.1d (Fig 4.1a: baseline CNFET: without negative capacitance). The gate stack (from bottom to top) consists of an external metal gate, a ferroelectric oxide, an internal metal layer, and a high-k gate oxide. Multiple parallel CNTs comprise the FET channel, whose conductance is modulated by the voltage of the internal metal layer, this layer serves to average the non-uniform charge in the NC-CNFET channel from source-to-drain under non-zero bias conditions, and presents an average charge to stabilize the ferroelectric capacitance in the negative capacitance state [Nourbakhsh 2017, Khan 2017]. The source, drain and gate regions are defined using traditional photolithography.

Here, we experimentally demonstrate the first NC-CNFETs. For 100 single CNT CNFETs (i.e CNFETs with a single CNT in the channel region), we show that our NC-CNFETs improve SS from an average of 70 mV/decade (for the baseline CNFETs) to an average of 55mV/decade (for the NC-CNFETs), contributing to a 2.1× improvement in I_{ON} versus baseline CNFETs.

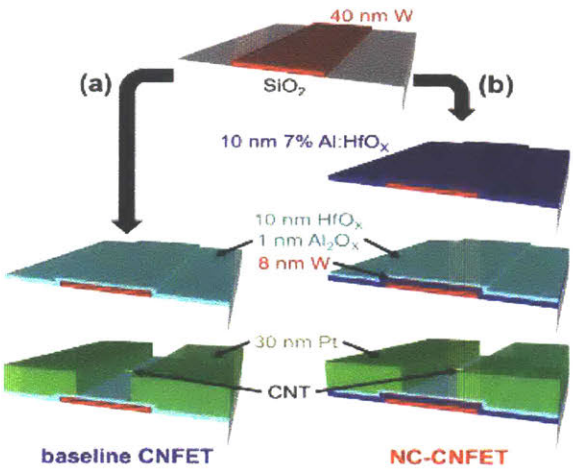


Figure 4.2. (a) Fabrication flow for (a) baseline CNFET & (b) NC-CNFET. The NC-CNFET gate stack consists of 40nm tungsten (for the external metal gate), followed by 10nm of ~7% aluminum doped hafnium oxide (7% Al:HfO_X, deposited through atomic layer deposition). The Al:HfO_X exhibits ferroelectric behavior [Nourbakhsh 2017]. Next, 8nm tungsten is deposited for the internal metal layer, followed by 10nm of high-K HfO_X and 1nm of aluminum oxide (Al_2O_X). The HfO_X deposited over the ferroelectric oxide ensures stable operation (by adding a series positive capacitance with the unstable NC ferroelectric oxide [Khan 2017, Khan 2011]). The 1nm Al_2O_X provides an ideal surface for the subsequent transfer of the CNTs over the channel region (after the fabrication of the gate stack) [Shulaker 2013, Shulaker 2017, Shulaker 2014b]. Finally, platinum electrodes are deposited for source/drain.

4.2 Fabrication Process

Fig. 4.2 illustrates the process flow for baseline CNFETs (Fig. 4.2a) and NC-CNFETs (Fig. 4.2b). We use a back-gate FET geometry (where the semiconducting channel of the FET is deposited over a pre-fabricated gate-stack), as it decouples the high temperature processing (>700 ◦C anneal) required for the ferroelectric material within the gate-stack from the CNTs used as the channel [Nourbakhsh 2017]. The starting substrates for both baseline CNFETs and NC-CNFETs are silicon wafers with 800nm silicon oxide (thermally grown). For the back-gate, 40nm of tungsten is defined through a liftoff process. For the NC-CNFET, a 10nm ferroelectric dielectric is ~7% aluminum-doped hafnium oxide (7% Al:HfO_X), deposited using atomic layer deposition (ALD) at 200 ◦C, followed by a subsequent 800 ◦C anneal for 10 minutes. This ferroelectric

dielectric has been extensively studied [Nourbakhsh 2017]. Fig. 4.3 shows the polarization versus electric field (P-E) hysteresis loop of capacitors fabricated with 10nm 7% Al:HfO_X and 10nm HfO_X. Al:HfO_X exhibits hysteresis unlike HfO_X confirming the ferroelectricity of this ALD grown thin film. The 8nm tungsten deposited over the ferroelectric dielectric is an internal metal layer, and serves to average the non-uniform charge in the NC-CNFET channel from the source-to-drain under non zero bias conditions. This presents an average charge to stabilize the ferroelectric capacitance in the negative capacitance state [Nourbakhsh 2017, Khan 2017].

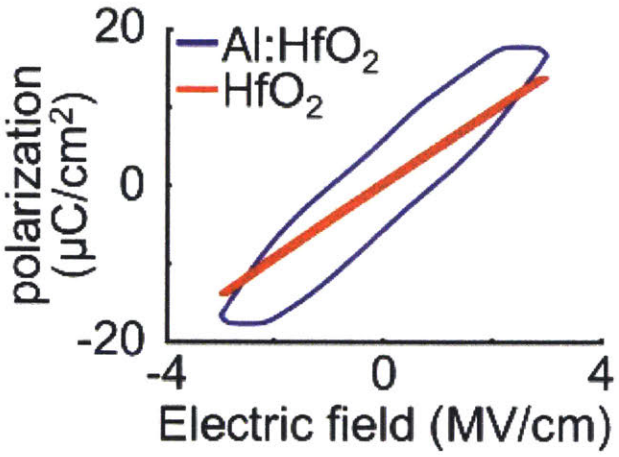


Fig. 4.3 Polarization versus electric field hysteresis for capacitors made from 10nm 7% Al:HfO_X and 10nm HfO_X. The 7% Al:HfO_X dielectric shows hysteresis loop confirming ferroelectricity

For both wafers (NC and baseline CNFETs), the remaining processing is identical. A 10nm layer of HfO_X is deposited by ALD (over the ferroelectric gate stack for NC-CNFET and over bare tungsten metal gate for the baseline CNFET). The HfO_X deposited over the ferroelectric oxide adds a series positive capacitance over the NC stack and ensures stable operation [Khan 2017, Khan 2011]. Following the hafnium oxide dielectric, 1nm Al_2O_X is deposited through ALD, which provides an ideal surface for the subsequent transfer of CNTs over the back-gates [Shulaker 2013, Shulaker 2017, Shulaker 2014b]. Chemical Vapor Deposition (CVD) grown single wall CNTs are transferred over the back-gates using the process described in [Shulaker 2014b]. Importantly, the transfer process is performed at low temperature (< 120 ◦C), and avoids damaging the

ferroelectric gate stack. The metal source and drain electrodes (0.5nm titanium for adhesion followed by 40nm platinum) are lithographically patterned and deposited through a lift-off process. Finally, mis-positioned CNTs outside the channel region of the FETs are removed by oxygen plasma.

4.3 NC-CNFET Experimental Demonstration

We provide the results from 100 CNFETs: 50 baseline CNFETs and 50 NC-CNFETs. The channel length of the CNFETs are 1 μm, and the width is chosen to achieve ~1 CNT per FET (to compare the performance of each single CNT channel). Each CNFET is first measured to determine if it has a semiconducting or a metallic CNT in the channel bridging the source and drain metal contacts (we define metallic CNTs as CNT that will result in CNFETs with I_{ON}/I_{OFF} <100; for energy-efficiency circuits, metallic CNTs can be removed using techniques described in [Hills 2015]). After measuring all of the CNFETs we image each CNFET (using SEM) to confirm that only a single semiconducting CNT is within the channel of the CNFET. Scanning electron microscopy (SEM) and cross-section transmission electron microscopy (TEM) images of a typical fabricated NC-CNFET are shown in Fig. 4.4 (in the TEM, individual CNTs are not visible due to the CNTs being perpendicular to the cross section).

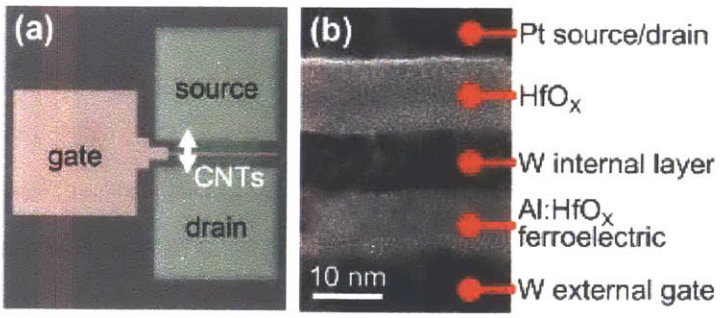


Fig. 4.4. NC-CNFET SEM (a) and cross-section TEM (b)

Fig. 4.5a shows I_D-V_{GS} curves from 50 single CNT baseline CNFETs and 50 single CNT NC-CNFETs. The distributions of SS and I_{ON}/I_{OFF} are shown in Fig. 4.6a and Fig. 4.6b respectively. The average SS improves

from 70 mV/decade to 55 mV/decade for NC-CNFET. Due to improvement in SS, for NC-CNFETs I_{ON} improves by 2.1× for the same I_{OFF}.

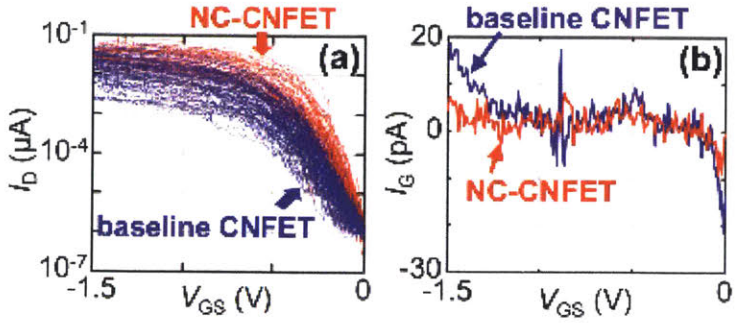


Fig. 4.5. Experimental measurements from 50 single CNT baseline CNFETs and 50 single CNT NC-CNFETs (V_{DS} = 50 mV). (a) I_D-V_{GS} (b) gate leakage (I_G) for one typical baseline CNFET and one typical NC-CNFET. Gate leakage is negligible (<30 pA)

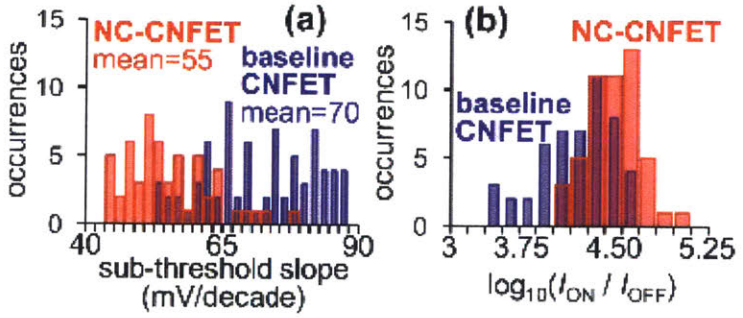


Fig. 4.6. Distributions of performance metrics for baseline CNFETs and NC-CNFETs (extracted from electrical characteristics [Fig. 4.5]) (a) Distribution of SS (SS is calculated over a 60 mV V_{GS} range). Mean SS improves from 70 mV/decade in baseline CNFETs to 55 mV/decade for NC-CNFETs (b) Distribution of I_{ON}/I_{OFF} (I_{ON} measured at V_{GS} = -1.5 V and I_{OFF} measured at V_{GS} = 0 V). Mean I_{ON}/I_{OFF} improves by 2.1× for NC-CNFETs compared to baseline CNFETs, for the same I_{OFF}.

These results experimentally verify the effectiveness of the ferroelectric oxide to amplify the voltage of the external metal gate onto the internal metal layer and achieve sub-60 mV/decade operation. Importantly, gate leakage (I_G, which must be limited for stable negative capacitance operation [Khan 2017]) is negligible ($|I_G|$ < 30 pA) for both baseline CNFETs and NC-CNFETs (shown in Fig 4.5b).

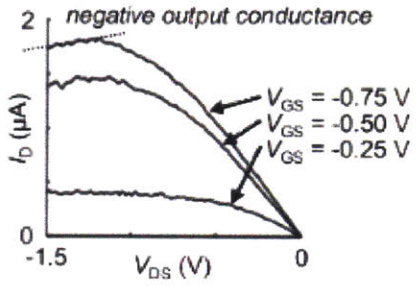


Fig. 4.7. I_D-V_{DS} output characteristic of a typical NC-CNFET. Note the negative output conductance at high bias, e.g. for V_{DS} = -1.5 V with V_{GS} = -0.75 V

Fig. 4.7 shows a typical I_D-V_{DS} characteristic of a NC-CNFET. Importantly, while the NC-CNFET exhibits the expected saturation current as the magnitude of V_{DS} increases, it also exhibits negative output conductance (Fig. 4.7). This negative output conductance at high V_{DS} magnitude (which has been observed in NCFET experimental demonstrations and is consistent with the expected behavior in the compact model as shown in Fig. 4.8c [Radhakrishna 2017]) introduces a fundamental trade-off for NC-FETs: due to non-monotonic relationship between I_D and V_{DS} in NC-FETs [Radhakrishna 2017], there can be hysteresis in logic gates made from NC-FETs (illustrated in Fig. 4.8) [Gupta 2017, Dutta 2017]. This is typically undesirable for digital logic circuits as it can lead to various circuit problems (e.g. incorrect logic functionality). Thus, the positive and negative capacitance portions of the gate stack must be carefully co-optimized to maximize energy efficiency benefits while minimizing the hysteric effect on logic gates.

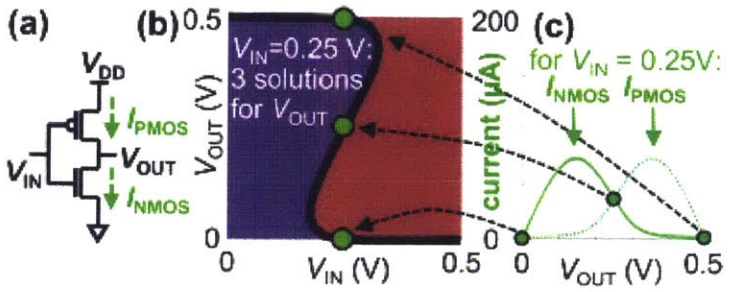


Fig. 4.8. Illustration of multiple solutions for DC convergence of logic gates built using NC-FETs, using a new SPICE-compatible compact model that combines the Virtual Source CNFET model [Lee 2015] with the NC gate stack from

the MIT Virtual Source Negative Capacitance (MVSNC) model [Radhakrishna 2017] (simulation result shown for an inverter built using NC-CNFETs with 5nm FE oxide thickness) (a) Inverter schematic, indicating input voltage (V_{IN}), output voltage (V_{OUT}), PMOS current (I_{PMOS}) and NMOS current (I_{NMOS}). (b) Inverter voltage transfer curve (indicated by the thick black line), illustrating that multiple values of V_{OUT} can lead to DC convergence for a single value of V_{IN} (DC convergence: $I_{PMOS} = I_{NMOS}$). The multiple solutions for DC convergence can result in hysteresis in logic gates (i.e. V_{OUT} can depend on previous values of V_{IN}), e.g. as discussed in [Hills 2017,Gupta 2017]. The shaded blue region indicates values of (V_{IN},V_{OUT}) for which $I_{PMOS}>I_{NMOS}$ (and vice versa for the shaded red region). The green markers in (b) represent the three possible values of V_{OUT} for fixed V_{IN} = 0.25 V such that $I_{PMOS} = I_{NMOS}$; these correspond to the green markers in (c), showing the values for which I_{PMOS} (dotted line) and I_{NMOS} (solid line) are equal.

4.4 Conclusion

We have experimentally demonstrated the first NC-CNFETs, which achieve an average SS of 55 mV/decade (compared to 70 mV/decade for baseline CNFETs), and improve average I_{ON} by 2.1× versus baseline CNFETs (for the same I_{OFF}). This work experimentally demonstrates a path for combining the benefits of both CNT channels with negative capacitance effects, for future generations of energy-efficient electronic systems.

Chapter 5: Concluding Remarks

Emerging nanotechnologies, such as CNTs, promise significant EDP benefits for digital VLSI design [Wei 209, Tulevski 2014]. Yet prior works and projected benefits related to CNFETs have been restricted to improvements resulting from an alternative channel material (the CNT itself). In this thesis, we demonstrate that by co-optimizing the fabrication, device structure, and design of CNFETs for digital VLSI circuits, the benefits afforded by CNFETs can increase dramatically.

By leveraging the unique low-temperature fabrication of CNFETs, we fabricate back-gate CNFETs to experimentally demonstrate record-scaled 30 nm CGP CNFETs and digital logic. We rigorously quantify the benefits of back-gate CNFETs by analyzing physical designs of digital VLSI circuits, showing that this approach provides additional EDP benefits vs. top-gate and GAA CNFETs due to reduced parasitic capacitances. Thus, we demonstrate significant benefits of back-gate FETs (both for scaling and for EDP), illustrating that they should be seriously considered for future highly-scaled and energy-efficient digital electronics.

Moreover, we use these same back-gate FET geometries to address and overcome excess off-state leakage current in CNFETs: a major challenge facing CNFETs today. The key to this approach is engineering asymmetric back-gates (*e.g.*, gates that overlaps the source but not the drain). We experimentally demonstrate this approach reduces off-state leakage current by >60× (implemented across a wide range of technology nodes from the 180 nm node to the >1 μm node), while our calibrated models show potential benefits exceeding 10^6×. We further illustrate this approach affords additional energy-efficiency benefits (due to both the reduced off-stage leakage current as well as the asymmetric gate geometry). Thus, this work addresses a key challenge facing CNFET-based electronics (while simultaneously providing additional energy-efficiency benefits), and is applicable to a wide-range of emerging one-dimensional and two-dimensional nanomaterials.

Additionally, we have experimentally demonstrated the first NC-CNFETs, combining the benefits of both CNT channels with negative capacitance effects, for future generations of energy-efficient electronic systems.

Thus, this work illustrates how coordinated advances across the stack – from nanofabrication to device geometries to digital VLSI circuit analysis – can be combined to realize benefits far greater than the sum of their individual benefits. While this work represents an important step forwards for CNT-based electronics, CNTs are solely a case study. The same approaches (and even same techniques and processes discussed in this thesis) are applicable to a wide range of emerging 1D and 2D nanomaterials. Therefore, while this work represents a major departure from conventional silicon CMOS, it represents an exciting path for realizing the next generation of energy-efficient computing systems. With continued progress, such technologies promise to enable future applications that will continue to benefit our lives for decades to come.

Appendix:

A.1: Process Flow for baseline CNFETs

The starting substrate for the back-gate CNFETs is silicon (resistivity of ~100 ohm-cm) with 800 nm thermal oxide. To pattern the metal gate, the wafer is coated with a single layer PMMA positive photoresist (~200 nm 495k PMMA A4), and electron-beam (ebeam) lithography is used to define the gate electrode. PMMA is patterned with room temperature development at 21 °C using 3:1 IPA:MIBK. Electron beam (ebeam) evaporation is used to deposit 10 Å of Titantium followed by 15 nm Platinum, followed by lift-off. The area dose for e-beam lithography is carefully optimized by simulating the electron back-scattering effects in a stack of PMMA-SiO_2 and PMMA-HfO_2 in TRACER. Atomic layer deposition (ALD) is used to deposit 10nm HfO_2 over the gate metal. Following gate-stack fabrication, photolithography is done using positive photoresist SPR to pattern contact holes to the gate metal electrodes, and a dry Cl_2-based plasma etch is used to etch through the HfO_2. The SPR is stripped in remover 1165 followed by oxygen plasma. To prepare the wafer for CNT deposition, the surface is functionalized with hexamethyldisilazane (HMDS, a common photoresist adhesion promoter). The wafer is then submerged in a solution of toluene containing >99.9% pure semiconducting CNTs (modified Nanointegris supplied IsoSol-S100) for 10 hours. To disperse CNTs in toluene, the CNTs go through several sonication steps to wrap the CNTs in a polymer to disperse them within the toluene, followed by several ultracentrifugation steps to remove non-dispersed CNTs and excess polymer. The source and drain are defined and patterned similar as the gate electrode. A last photolithography step using bilayer resist (SPR+PMGI SF5 lift off layer), ebeam evaporation, and lift-off is performed to define larger probe pads and interconnect wires. After CNFET fabrication, SPR is patterned to cover the transistor channel regions, and oxygen plasma removes all excess CNTs (*e.g.*, CNTs outside of the transistor channel region, and therefore not protected by the SPR).

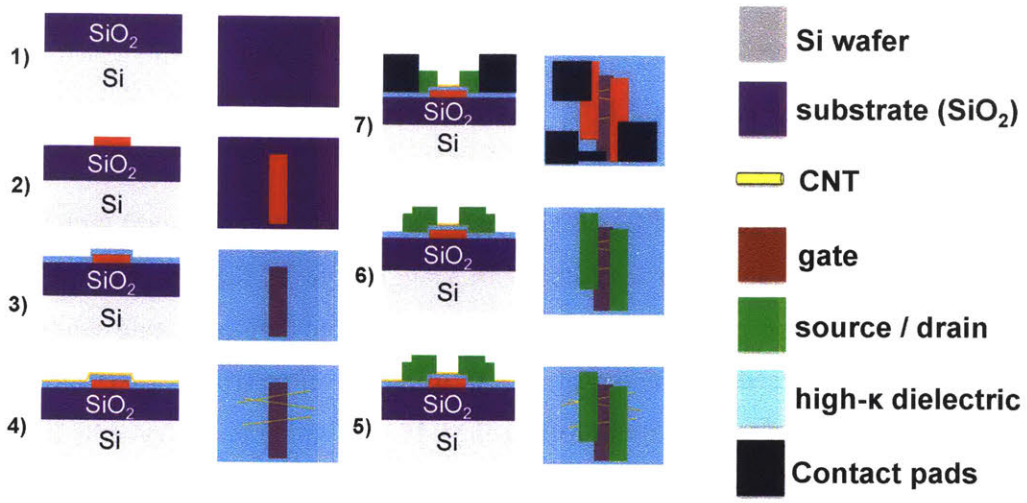


Figure A1.1. Process flow of back-gate CNFETs. (1) Si/SiO_2 substrate. (2) electron-beam(e-beam) lithography patterning, e-beam metal evaporation and liftoff for back-gate (1 nm Ti/ 15 nm Pt). (3) 10 nm HfO_2 gate dielectric (eot ≈ 2.5 nm). (4) Submerge die in purified >99.9% pure semiconducting CNTs dispersed in toluene solution. (5) source/drain patterning through e-beam lithography patterning, e-beam metal deposition and liftoff (1 nm Ti/ 25 nm Pt). (6) oxygen plasma etch to remove CNTs outside of transistor channel region. (7) probe pad deposition defined through photolithography (maskless aligner), e-beam metal evaporation and liftoff (10 nm Ti/ 40 nm Pt).

The starting substrate for the back-gate 30 nm CGP CNFETs are silicon substrates (resistivity of ~100 ohm-cm) with 800 nm thermal oxide. To pattern the metal gate, the wafer is coated with a single layer PMMA positive photoresist (~45 nm PMMA A1), and electron-beam (ebeam) lithography is used to define the gate electrode (LG ~18 nm). PMMA is patterned with cold development at -3.5 °C. Electron beam (ebeam) evaporation is used to deposit 3 Å of Titantium followed by 4 nm Platinum, followed by lift-off in heated 1-methyl pyrrolidone at 60 C in a water bath. The area dose for e-beam lithography is carefully optimized by simulating the electron back-scattering effects in a stack of PMMA-SiO_2 and PMMA-HfO_2 in TRACER[26]. Following gate-stack fabrication, PMMA and ebeam lithography is again used to pattern contact holes to the gate metal electrodes, and a dry Cl_2-based plasma etch is used to etch through the HfO_2. The PMMA is stripped in hot acetone followed by oxygen plasma. To prepare the wafer for CNT deposition, the surface is functionalized with HMDS. The wafer is then submerged in a solution of 1,2-Dichloroethane (DCE) containing >99.9% pure semiconducting CNTs for 10 minutes. To disperse CNTs in DCE, the CNTs go through several sonication steps to wrap the CNTs in a polymer to disperse them within the DCE, followed by several ultracentrifugation steps to remove non-dispersed CNTs and excess polymer. Following CNT deposition, the wafer is rinsed in hot Toluene for 60 minutes, followed by vacuum annealing at $<10^{-5}$ Torr for >30 minutes. The source and drain are defined and patterned similar as the gate electrode, but are done in two separate steps to increase minimum resolution. A last ebeam lithography step, ebeam evaporation, and lift-off is performed to define larger probe pads and interconnect wires. After CNFET fabrication, PMMA is

patterned to cover the transistor channel regions, and oxygen plasma removes all excess CNTs (*e.g.*, CNTs outside of the transistor channel region, and therefore not protected by the PMMA).

A.2: Physical Design Flow for EDP analysis

The physical design flow for VLSI circuits is as follows. We quantify circuit-level performance metrics for physical designs for each VLSI-scale circuit module (*i.e.*, from the OpenSparc T2 processor core and for the 32 bit commercial processor core) at the 5 nm node (details in Table S1) across multiple device-level performance metrics, including (but not limited to): supply voltage (V_{DD} = 375 mV to 500 mV), sub-threshold slope (*SS*) degradation (from 0% to 25%), and accounting for CNFET-level parasitics using a commercially-available 3D field solver [TCAD Sentaurus] and interconnect simulator [Raphael] to model extrinsic elements based on the CNFET geometry and material properties (*e.g.*, on the dimensions and resistivity of the source/drain metal contact plugs). For each combination of parameters (*e.g.*, for each V_{DD}, *SS*, top-gate vs. bottom-gate), we perform the following design flow to quantify relative EDP (*e.g.*, as in Fig. 7) for all VLSI circuit modules:

1. *Standard cell library characterization*: using standard cell layouts (derived from the 15 nm node Nangate Open Cell Library [Nangate]) are used to extract standard cell parasitics, and then the extracted netlists are used in conjunction with the experimentally calibrated compact transistor models [Lee 2015] to characterize power and timing (using Cadence Spectre [Spectre]) for each standard library cell

2. *Synthesis*: using Synopsys Design Compiler [Design Compiler], synthesize each circuit module over a range of target clock frequencies (from 1 GHz to 10 GHz), since operating clock frequency after optimizing circuit EDP can vary depending on the device-level parameters (*e.g.*, V_{DD}).

3. *Placement & routing*: using Synopsys IC Compiler [IC Compiler], perform placement & routing for each synthesized netlist (for each target frequency), allowing for physical circuit optimization such as buffer insertion to meet circuit timing constraints.

4. *Power/timing analysis*: perform power and timing analysis for each physical design (using Synopsys PrimeTime [PrimeTime]) placed & routed above, over several *retargeted* clock frequencies spanning the range from 0.1 GHz up to 10 GHz in 0.1 GHz increments (*i.e.*, readjust the timing constraints in steps 2 and 3 targeting a different clock frequency), since it is potentially more energy efficient to operate at a separate clock frequency than that was specified during synthesis and place & route.

A.3: Non-self-aligned back-gate CNFET

The back-gate structure is not a self-aligned structure. Therefore, the back-gate may be misaligned to the source and drain contacts. This misalignment can lead to increased parasitic capacitances. To analyze the effect of the overlay misalignment, we extract the capacitance of a CNFET with a 30 nm CGP, assuming different overlay misalignment (Figure A3.1a). Given a 6 nm overlay inaccuracy between the gate and source and drain contacts, the input capacitance of the CNFET changes by only <12% (Figure A3.1b).

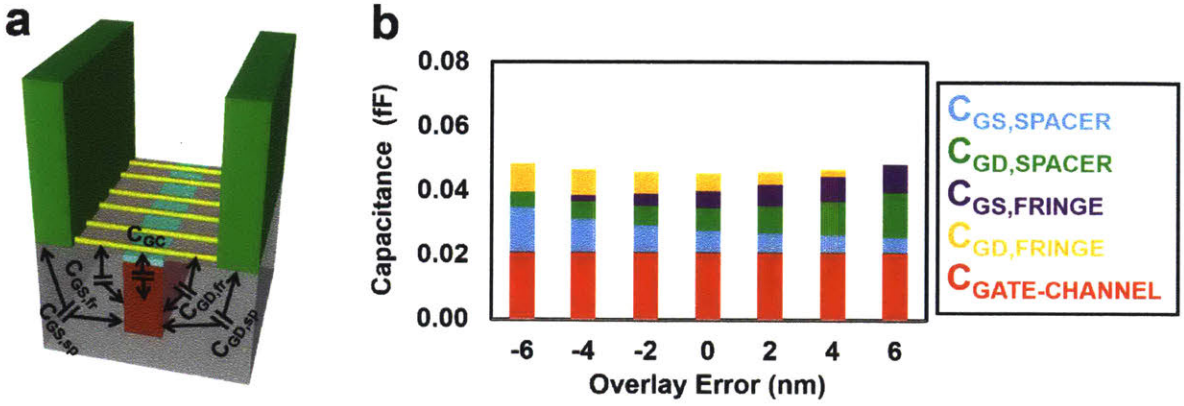


Figure A3.1: (a) Schematic of back-gate CNFET, with labelled input capacitances. (b) The input capacitance of a CNFET changes by <12% given a 6 nm mis-alignment inaccuracy in either direction (for a highly-scaled 30 nm CGP CNFET).

A.4: Additional considerations for designing asymmetric back-gate CNFETs

Figure A4.1 shows the average reduction in I_{OFF} across multiple CNFETs, for a given L_{SP} (sample size: 30 CNFETs). All CNFETs have 180 nm channel length.

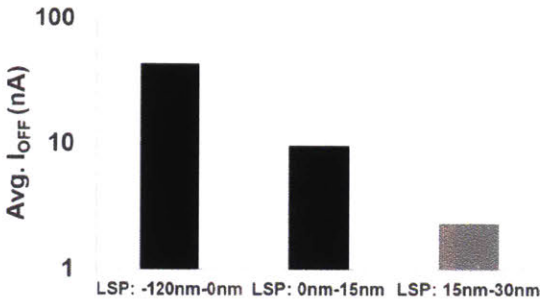


Figure A4.1. Averaged I_{OFF} with varying L_{SP} (defined in Figure 1a), sample size = 30 CNFETs.

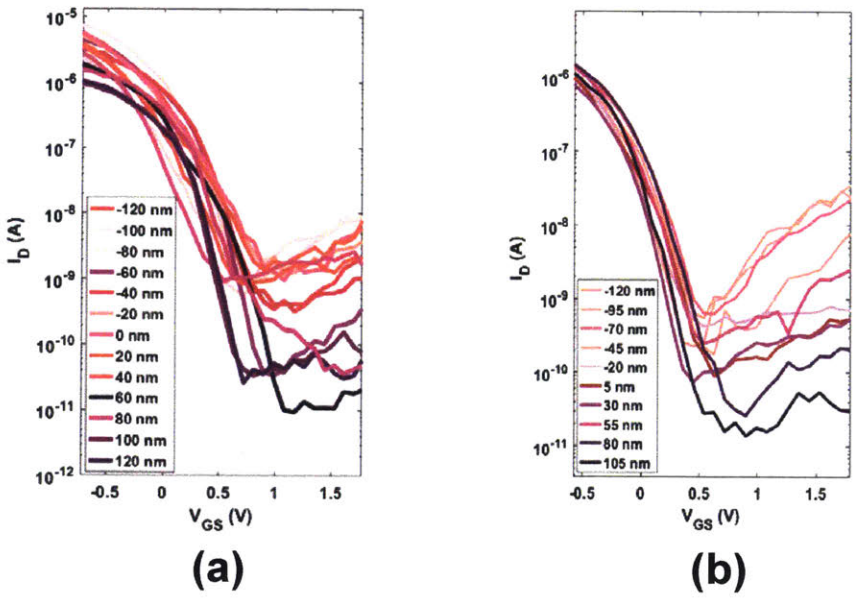


Figure A4.2. Experimental I_D-V_{GS} characteristics for CNFETs with L_{CH} of 500nm (a) and 1μm (b), sweeping over more detailed L_{SP}.

To solve for the electrical transport in CNFETs and intrinsic parasitic capacitances, simulations are performed with TCAD Sentaurus. Devices parameters used for these simulations are listed in Table 3.2 For I-V transport simulation, CNFET is approximated as a 2D MOSFET with an extremely thin semiconductor (t = 2 nm) defining the CNT channel (with CNT material properties as reported in virtual-source CNFET compact

model [Lee 2015]). Platinum is used to define the source, drain and gate electrode and HfO_2 is used to define the gate dielectric. For the sentaurus device model defining the device transport physics we use simple Hurkx tunneling model which calculates tunneling current using WKB approximation. For the capacitance simulation, quasistationary coupled poisson electron and hole equations are solved for a small applied ac voltage and lumped capacitances C_G and C_D (defined in Figure 3.5b, equations 1-2) is extracted as dQ_G/dV_G and dQ_D/dV_G respectively.

A.5: Gate-Induced Drain Leakage (GIDL)

In MOSFETs, gate-induced drain leakage mainly originates from band-to-band tunneling (BTBT) near the gate-drain overlap region, at large gate-to-drain bias. When high voltage is applied even when the transistor is off ($V_{GS}<0$ for a NMOSFET & $V_{GS}>0$ for a PMOSFET), a deep-depletion region is formed in the gate/drain overlap region (Fig. A5.1a). Thus valence band electrons tunnel to the conduction band through BTBT (for NMOS, Fig. A5.1b, for PMOS electrons tunnel from conduction band to valence band, Fig. A6.1c). Thus, electron-hole pairs generated through BTBT are collected by the drain and substrate separately, increasing the leakage current. From tunneling current models [Chan 1987], GIDL-induced current can be represented as:

$$I_{D,GIDL}=AE_S e^{\frac{B}{E_S}} \quad \text{.....(eq. A5.1)}$$

A and B are constants, E_S is vertical electric field at the channel surface (in the overlap region), $E_S = \frac{V_{DG}-C}{3T_{OX}}$, C is a constant., T_{OX} is the oxide thickness, V_{DG} is the gate-to-drain bias voltage

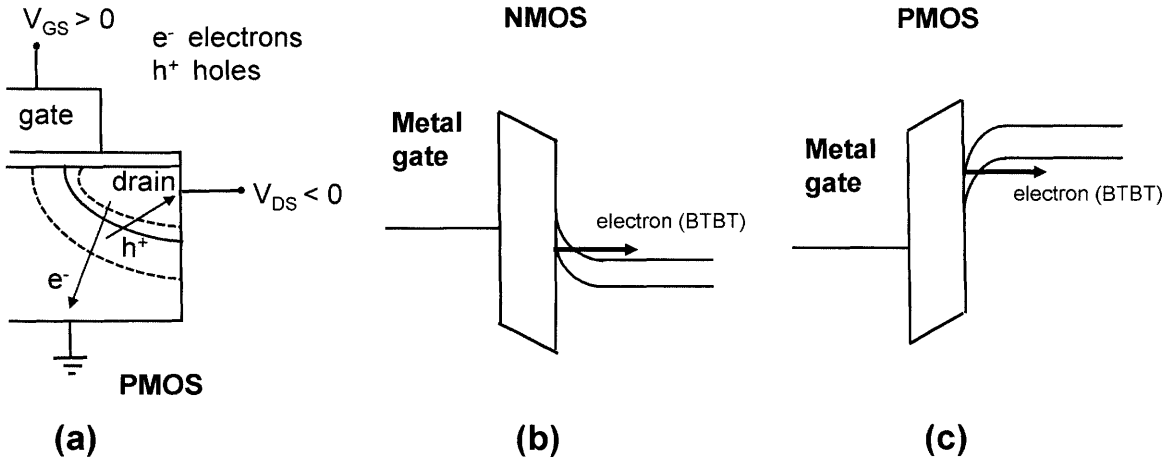


Figure A5.1: a. formation of deep-depletion region in PMOSFET at off-state ($V_{GS} > 0$), showing tunneling of electrons to the substrate, increasing the leakage current. b-c. band diagrams of NMOS and PMOS at off-state showing band-to-band tunneling of electrons causing GIDL.

Possible means to reduce this GIDL-induced current relies on reduction of E_S (evident from equation A5.1). MOSFETs with relaxed access regions or undoped spacer regions can limit this electric-field near the gate-drain overlap region, suppressing excess GIDL-induced current (Fig. A5.2).

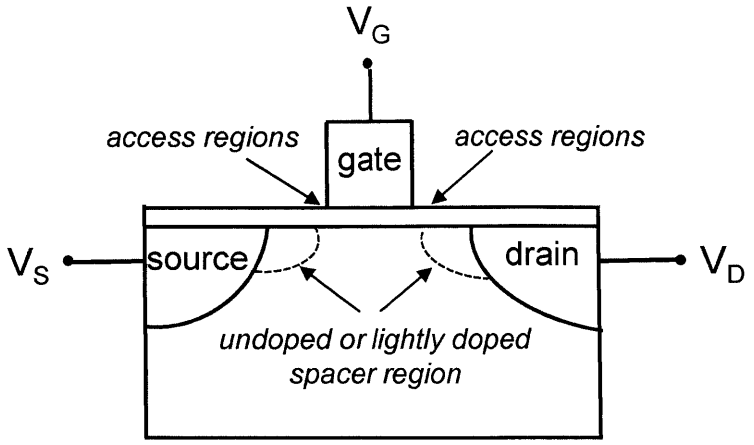


Figure A5.2: FETs with long access regions (or, extension regions) or undoped/lightly doped spacer regions limit the high electric field near the gate/drain overlap region and are used to overcome GIDL-induced leakage current.

In a schottky-barrier FETs, high gate-to-drain bias induces band bending (Fig. A5.3 , equation A5.2) in the drain metal-semiconductor schottky barrier near the gate/drain overlap region, causing electrons to tunnel from the metal contact to the semiconducting channel leading to excess off-state leakage current.

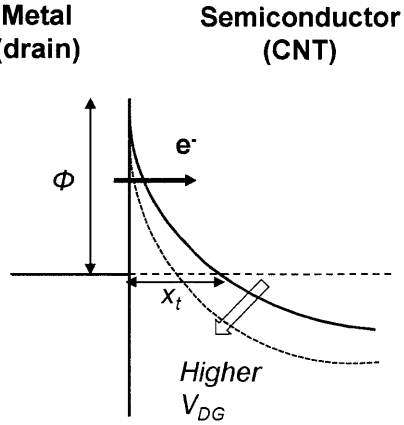


Figure A5.3: Band diagram of the Schottky barrier near the gate/drain overlap region. Increasing gate-to-drain bias (V_{DG}) decreases schottky barrier tunneling width (x_t) increasing tunneling of electrons across the schottky barrier, causing excess off-state leakage current.

Tunneling probability across a schottky barrier [Calvet 2001] can be mathematically expressed as (equation A5.2):

$$P = \exp\left(-\frac{4\sqrt{2m^* q}\,(\Phi)^{3/2}}{3hE}\right) \quad \text{.....(equation A5.2)}$$

Where, E = vertical electric field across the schottky barrier E is proportional to gate-drain bias voltage near the gate/drain overlap region (thus, higher V_{DG} exponentially increases the tunneling probability of electrons across the schottky barrier causing excess off-state leakage current), h = reduced Planck's constant, m* = electron effective mass, q = charge of electron, Φ= schottky barrier height

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