High-Resolution Transmission Electron Microscopy of III-V FinFETs

by

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ABSTRACT

III-V materials have great potential for integration into future complementary metal–oxide–semiconductor technology due to their outstanding electron transport properties. InGaAs n-channel metal-oxide-semiconductor field-effect transistors have already demonstrated promising characteristics, and the antimonide material system is emerging as a candidate for p-channel devices. As transistor technology scales down to the sub-10-nm regime, only devices with a 3D configuration can deliver the necessary performance. III-V fin field-effect transistors (finFETs) have displayed impressive characteristics but have shown degradation in performance as the fin width is scaled to the sub-10-nm regime. In this work, we use high-resolution transmission electron microscopy (HRTEM) in an effort to understand how interfacial properties between the channel and high-k dielectric affect device performance.

At the interface between the channel material, such as InGaSb or InGaAs, and the high-k gate dielectric, properties of interest include defect density, interdiffusion between the semiconductor and dielectric, and roughness of the dielectric - semiconductor interface. Using HRTEM, we can directly study this interface and try to understand how it is affected by different processing conditions and its correlation with device characteristics.

In this thesis, we have analyzed both InGaAs and InGaSb finFETs with state-of-the-art fin widths. Analysis of TEM images was combined with electrical data to correlate interfacial properties with device performance. We compared the materials properties of InGaAs and InGaSb and also explored the impact of processing steps on interfacial properties.

Thesis supervisor: Jesús A. del Alamo
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Table of Contents

List of Figures

CHAPTER 1. INTRODUCTION

1.1 Introduction to III-V finFETs

Silicon complementary-metal-oxide-semiconductor technology has maintained the path of Moore's law for the past fifty years. However, the silicon transistor is tipped to offer diminishing returns at the 7nm node and beyond due to leakage currents and short-channel effects [1]. III-V compound semiconductors have recently emerged as one of the most promising family of materials to replace silicon as the channel material [2], [3]. InGaAs has demonstrated outstanding electron mobility that as already enabled the fabrication of record-breaking high electron mobility transistors (HEMT) and heterojunction bipolar transistors (HBT) [4].

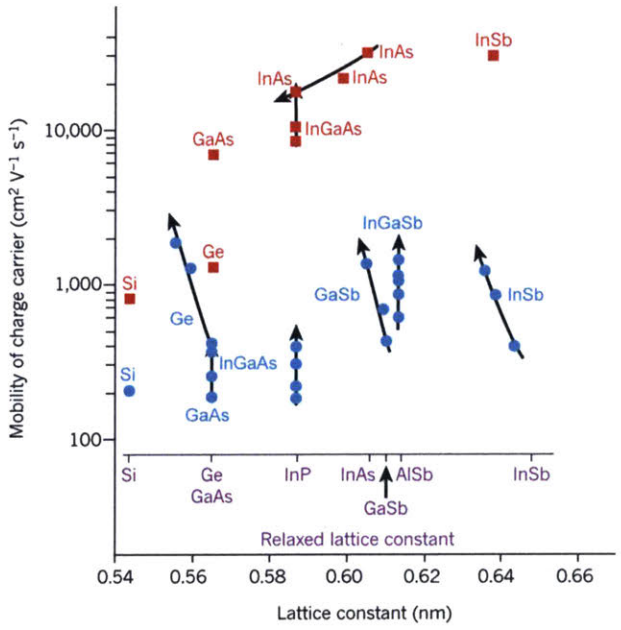

Figure 1. III-V semiconductor compositional space and corresponding carrier mobilities [2].

Besides their outstanding carrier transport properties, III-V compound materials can also span a wide range of lattice constants, effective masses, and bandgaps by varying the composition. Figure 1 shows a plot of the electron and hole mobility of some of the most

important III-V compound semiconductors and their corresponding lattice constants. InGaAs, which has a high electron mobility and can be lattice-matched to InP, was investigated as a channel material for n-type devices in this thesis. Figure 1 shows that InGaAs and other III-V materials have higher electron mobility than Si and Ge. InGaSb has a higher hole mobility than Si and Ge and was therefore investigated as a channel material for p-type devices in this thesis.

Novel III-V metal-oxide-semiconductor field-effect transistor (MOSFET) prototypes with superior electronic characteristics have been demonstrated [5], [6]. Their fabrication fueled further confidence in the potential of the III-V material system. The planar MOSFET's scaling potential, however, is limited. As CMOS technologies scale beyond the 7nm node, only three-dimensional transistor structures can attain the footprint that will comply with Moore's Law transistor density goals.

As its name suggests, the finFET is a transistor architecture where the conducting channel resides in a thin 'fin' of semiconductor. Figure 2 illustrates the finFET architecture. The finFET, like a typical transistor, has a source, gate, and drain. The gate wraps around the fin-shaped channel on either side. This geometry yields a high degree of electrostatic control and enables scaling of the gate length to very small dimensions. The finFET structure is used in today's state-of-the-art silicon transistors and the most advanced CMOS nodes [7], [8].

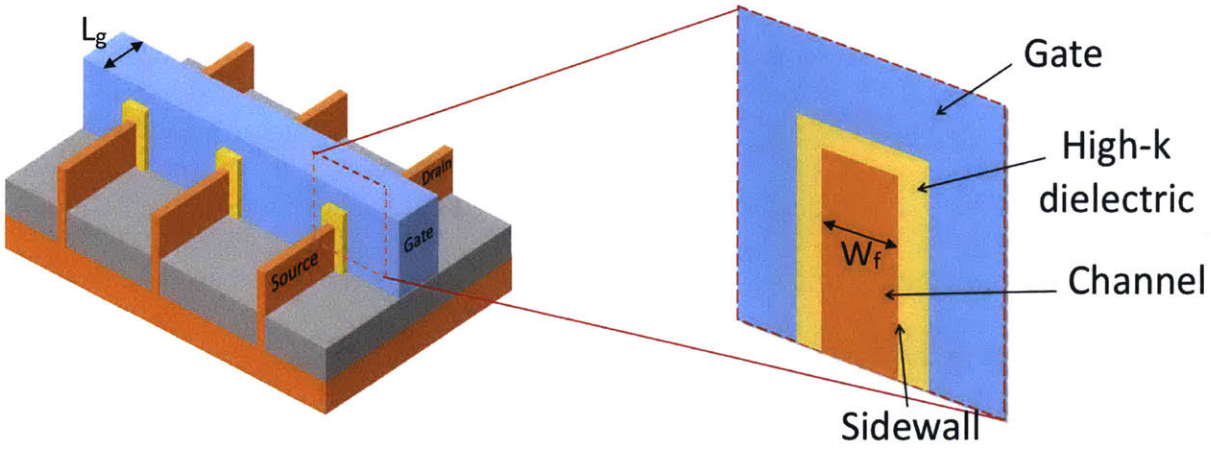

Figure 2. Diagram of finFET and a fin cross-section.

Though impressive III-V MOSFETs have been demonstrated, III-V finFETs still lag behind Si finFETs in performance [9]. III-V finFETs present several materials-related challenges that are explored in this thesis. FinFET performance depends heavily on the quality of the fin, and in order to be inserted into the CMOS roadmap, these transistors must sport a fin width (W_f) less than 10nm and have an aspect ratio greater than five, meaning the channel is at least five times as high as it is wide. The devices studied in this thesis were fabricated using a process that involves reactive ion etching and digital etch, which in combination yields fins with sub-10nm widths. However, as the III-V finFET fin width is scaled down to 10nm, severe ON-current degradation is observed [9]. This degradation in performance is largely related to the quality of the high-k dielectric/channel interface at the fin sidewalls. In this thesis, we use TEM and electrical characteristics to understand properties of the high-k dielectric/channel interface for both p- and n-type devices, with the goal of improving performance of sub-10nm width finFETs.

1.2 Need for both N- and P-type devices

The success of modern CMOS is not possible without the matched performance of both p- and n-type transistors. Similar to the case of Si, the performance of p-type III-V transistors lags behind the performance of n-type III-V transistors [2], largely due to the fact that holes generally have higher effective masses than electrons. This disparity between p-type and n-type devices has long been an issue impeding progress on III-V CMOS, and so this thesis explores both p-type and n-type devices. In this thesis, InGaSb is used as the channel material in the p-type devices, and InGaAs as the channel material in the n-type devices. The goal of this work is to examine the quality of the interfaces that both InGaAs and InGaSb form with the high-k dielectric material through TEM, and then correlate interfacial properties with electrical performance.

1.3 Previous work

The III-V finFET entered published literature relatively recently. The first well-behaved InGaAs finFET was demonstrated in the literature in 2009, with a fin width of 40nm [10]. InGaSb finFETs are an even more recent topic of study; the first InGaSb finFET was demonstrated in 2015 [11]. These InGaSb fins had fin widths (W_f) as small as W_f = 30nm. To meet the demands of current transistor density goals, the literature has since progressed to smaller and smaller fin widths. In December 2017, Intel published TEM images of Si finFETs with fin width W_f = 7nm [12]. The III-V finFETs studied in this work had record fin widths as low as W_f = 5nm.

Electrical characteristics have been used extensively to investigate the materials properties in these III-V finFETs. In InGaAs finFETs, subthreshold characteristics have been used to deduce the presence of sidewall interface states that limit the electrostatic control of the channel by the gate. Samples of W_f = 7nm that were processed to have better sidewall definition had significantly higher transconductance (g_m) than other W_f = 7nm samples, demonstrating the importance of the channel/high-k dielectric interface in device performance [9]. In Figure 3, sample C had a thicker adhesion layer for the HSQ fin mask than sample B, which yielded better sidewall definition and better performance.

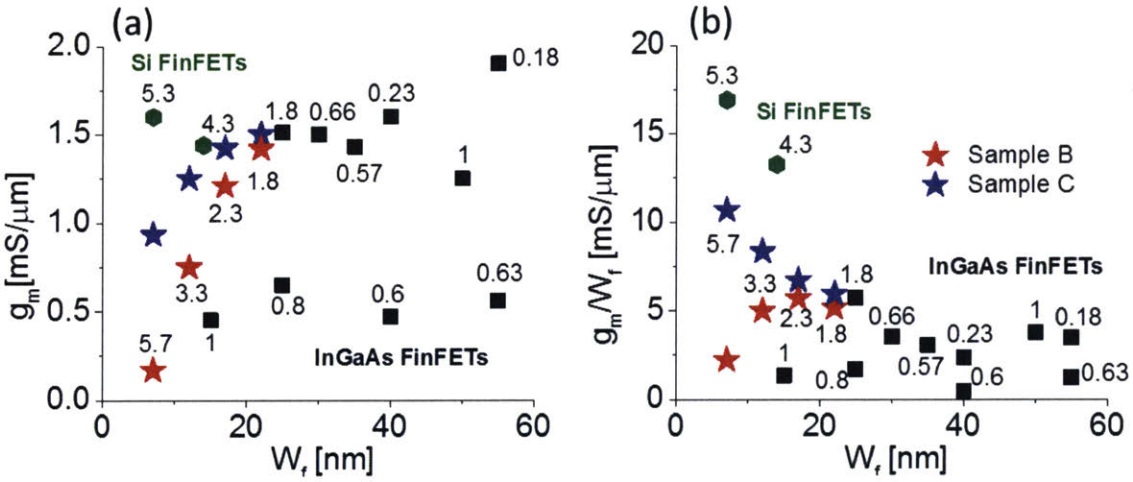

Figure 3. Benchmark of maximum g_m vs. W_f for InGaAs finFETs and state-of-the-art Si finFETs. (a) g_m normalized by gate periphery. (b) g_m normalized by fin footprint [9].

To the author's knowledge, no in-depth study of III-V finFETs using TEM has been performed. TEM allows us to directly see the channel/high-k dielectric interface. TEM analysis in conjunction with electrical measurements allows us to better understand how interfacial properties affect carrier transport in III-V finFETs, and how device performance can be improved. The next section details the methods used to prepare samples for our TEM study.

CHAPTER 2. METHODS

In this chapter, we give a background of the instruments used to carry out the TEM study: FIB and TEM. Additionally, we highlight methods that were used to optimize FIB and TEM for our finFET samples.

2.1 Focused Ion Beam (FIB)

The FIB was essential to prepare cross-sectional samples for TEM. This section details how FIB works and describes the technique used to prepare TEM samples.

A FIB instrument operates much like a scanning electron microscope (SEM). Both can be used to create a specimen image; FIB uses a focused Ga^+ beam and SEM uses a focused electron beam. Operation of the Ga^+ beam begins with a liquid metal ion source (LMIS) of Ga in contact with a tungsten needle. The Ga wets the needle and flows to the tip. An extraction field greater than $>10^8$ V/cm pulls the Ga into a sharp cone of radius 5 – 10nm. Ions are then emitted as a result of field ionization and then accelerated down the FIB column. Accelerating voltages ranging from 5 to 50 keV are typically used in FIB instruments. Ga is used as the ion beam source because (i) it has a low melting point, and (ii) Ga can be focused to a very fine probe size <10nm in diameter to enable high-resolution imaging [13]. Figure 4 shows a schematic of how the ion beam is produced in the chamber.

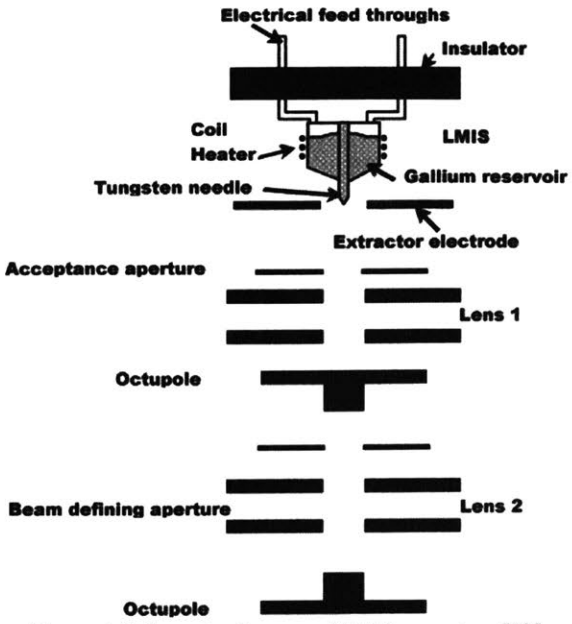

Figure 4. Schematic diagram of FIB lens system [13].

In contrast to the electron beam in SEM, the ion beam in FIB carries much more kinetic energy. The ion beam can therefore perform several useful functions in addition to imaging. FIB can be used to cut and micromachine samples, as well as to assist in deposition of metals [14].

2.1.1 Using FIB to cut samples

When ions collide with the solid sample, the ion kinetic energy is transferred to the solid through both inelastic and elastic interactions. In inelastic interactions, the ion energy is lost to the electrons in the sample, which are then ionized and emitted from the sample. In the elastic interactions, the ion energy is transferred to the atoms in the sample and results in displacement of the sample's atoms and sputtering from the surface. Because of this sputtering behavior, FIB can be used to precisely remove material from a sample. In the

case of TEM sample preparation, FIB is used to mill trenches around the area of interest, to cut through material, and to thin the sample down to a thickness appropriate for TEM.

2.1.2 Using FIB to assist in chemical vapor deposition

In conjunction with a gas-injection system (GIS), FIB can be used to perform local chemical vapor deposition (CVD) [14]. A needle is brought to within 100 - 200μm of the sample surface. A suitable gas is injected from the needle and adsorbs at the sample surface. The Ga^+ beam decomposes the gas and subsequently leaves behind a deposited layer of metal. The byproduct is removed by the vacuum system. The electron beam can also be used to assist in CVD but deposits metal much slower than the ion beam. For TEM sample preparation, the injected gas used is $C_9H_{16}Pt$ and deposits Pt on the sample. Pt deposition is used to protect the sample and to weld objects together.

2.1.3 FIB – induced damage

The ion beam's high kinetic energy enables it to be used for micromachining of samples, but is also its major drawback. Samples are susceptible to damage from the ion beam. As the ion dose increases, regions of displaced atoms overlap and a damaged surface layer forms. This damage can take the form of amorphization, point defect creation, dislocation formation, or other unusual effects [14]. Systematic investigations of FIB damage are still progressing in the literature [15].

In this work, in order to minimize the damaging effect of the ion beam, ion beam images were taken only when necessary during sample preparation. Additionally, towards the end of the sample preparation, only very low accelerating voltages were used to mill the sample. Though high ion beam dosages were avoided, high enough dosages were necessary to complete steps before drift of the beam caused unexpected damage. Consideration of damage from the ion beam was also necessary during analysis of TEM images.

The next section details how FIB was used to prepare cross-sectional TEM samples. An instrument outfitted with both an SEM and FIB as well as a gas injection system (GIS) and an Omniprobe was used.

2.1.4 Overview of cross-sectional TEM sample preparation

Samples were prepared for TEM using FIB. Specifically, the FEI Helios Nanolab 600 Dual Beam System in MIT's Center for Materials Science and Engineering was used. First, the Pt protection layer was deposited. Trenches were then milled on both sides of the sample. An Omniprobe was used to lift out the sample and transfer it to a PELCO FIB Lift-Out TEM Grid. Finally, the sample was thinned until it was semi-transparent to the electron beam. The final desired thickness for a TEM sample was sub-100nm. Figure 5 illustrates a brief outline of the sample preparation steps.

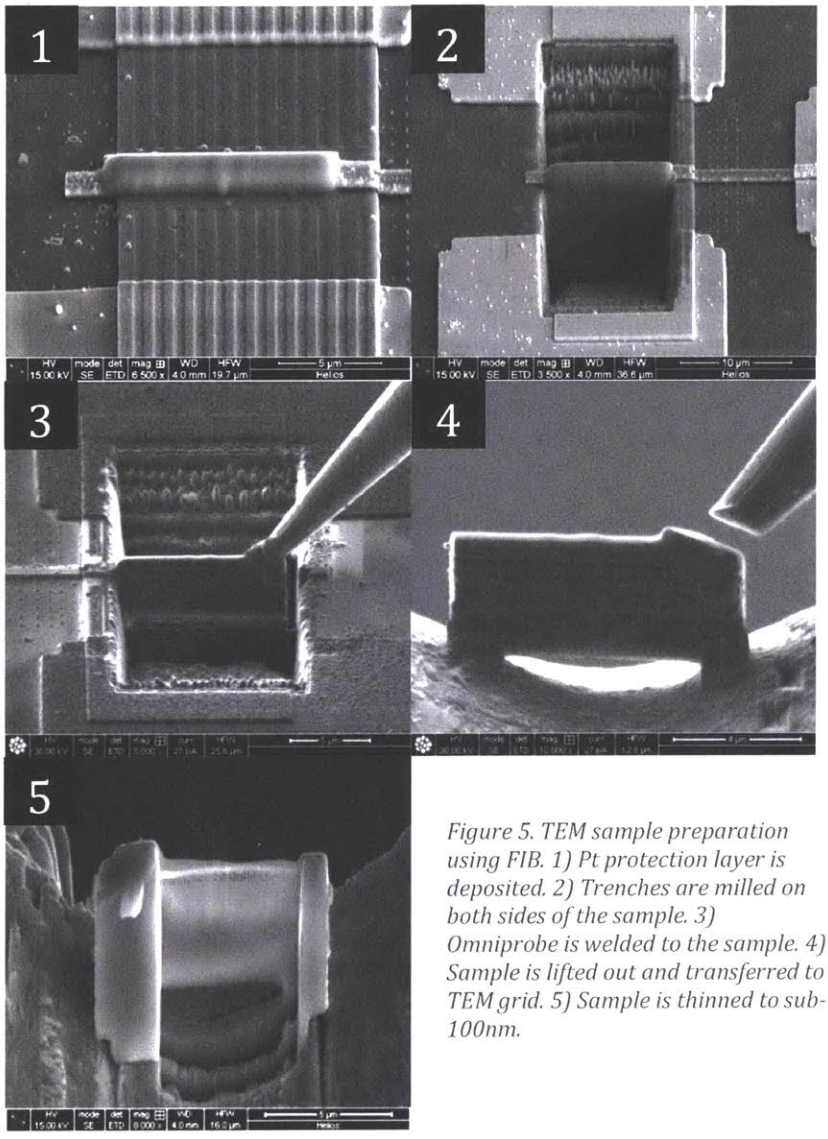

Figure 5. TEM sample preparation using FIB. 1) Pt protection layer is deposited. 2) Trenches are milled on both sides of the sample. 3) Omniprobe is welded to the sample. 4) Sample is lifted out and transferred to TEM grid. 5) Sample is thinned to sub-100nm.

2.1.5 Step-by-step cross-sectional TEM sample preparation

Consistent preparation of good TEM samples was crucial to this project. This section gives an in-depth description of the TEM sample preparation steps in the FIB. Over the course of many FIB sessions, modifications were made to previously used procedures to improve the sample preparation process in light of challenges specific to finFET samples.

1. Find the eucentric height of the sample and align the electron beam with the ion beam.
2. Insert GIS and deposit a Pt protection layer of ~2μm width and ~2μm height across the length of interest, using the electron beam to assist the deposition (Figure 5, step 1). Other procedures typically call for a layer of 1μm height, but since the area of interest (the fins) in our sample is on the surface, a thicker layer is necessary to protect the fins. Additionally, other procedures use ion beam to deposit the protection layer, but we use the electron beam to avoid damaging the fins.
3. Tilt the sample to 52 degrees and mill trenches on either side of the protection layer. Then, over-tilt the sample by 1.5 degrees on either side and mill a cleaning cross section on the exposed sides (Figure 5, step 2). This over-tilt step is necessary to cut completely vertical samples since the intensity of the ion beam profile decreases at high incidence angles.
4. Tilt the sample to 7 degrees and perform an L-cut.
5. Tilt the sample to 0 degrees and insert the Omniprobe and GIS. Carefully lower the Omniprobe to the sample surface.
6. Adjust the ion beam to a low dosage, around 30 keV accelerating voltage and 28 pA current. Weld the Omniprobe to the sample using the ion beam. Turn on the

electron beam and focus the beam onto the sample to also weld using the electron beam (Figure 5, step 3). This additional welding glues the sample and the probe more strongly.

7. Cut the sample on the remaining attached side in parallel with a second L-cut to prevent redeposition of the sample.
8. Lift out the sample to the top of the screen by moving the Omniprobe up and take out GIS. Manually bring the stage down and move the stage to the TEM grid position. Other procedures directed for the Omniprobe to be taken out and re-inserted, but the sample was often lost in that step.
9. Manually bring the stage back up and insert GIS. Lower the sample down to the grid surface.
10. Weld the sample to the grid at a low ion beam dosage (Figure 5, step 4).
11. Cut the Omniprobe from the sample at 30 keV and 2.3nA. Lower ion beam dosages sometimes detached the sample from the grid before the omniprobe was fully cut from the sample.
12. Thin the sample down from either side using the ion beam. Over-tilt the sample 2.5 degrees on either side at the beginning of the thinning process. Decrease the ion beam current, starting from 93pA, and decrease the over-tilt as the sample gets thinner (Figure 5, step 5).
13. To clean the sample, reduce the ion beam accelerating voltage and mill the sample on either side for several minutes. This cleaning step helps remove Ga impurities and phases on the sample surface without damaging the sample.

2.2 High Resolution Transmission Electron Microscopy (TEM)

Samples were analyzed using high-resolution TEM. In TEM, an electron beam, focused by electromagnetic lenses, is passed through the sample. After interacting with the sample the electrons are projected onto a screen at the bottom of the microscope and create an image of the sample. The image is then captured with an internal camera. Figure 6 shows a diagram of how the image is created for the two basic operations in TEM: diffraction mode, where the diffraction pattern is projected onto the screen, and image mode, where the image is projected onto the screen.

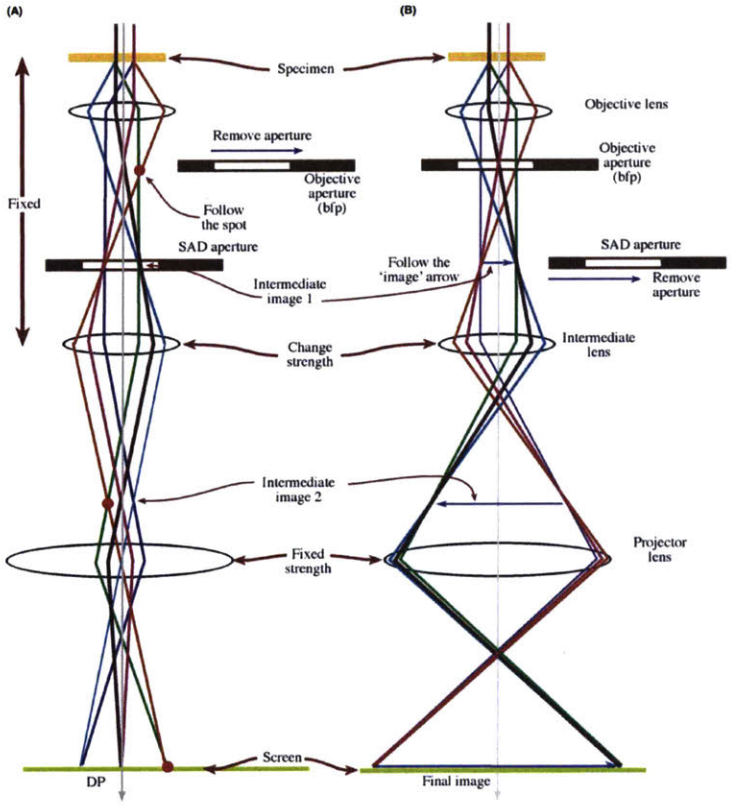

Figure 6. Schematic of electron beam path in TEM chamber for (A) diffraction mode and (B) image mode [16].

The instrument used for this work was the JEOL 2010 FEG Analytical Electron Microscope in MIT's Center for Materials Science and Engineering.

To achieve high resolution, a double-tilt TEM sample holder was used. This sample holder tilted in both the x and y directions and allowed for crystal orientation alignment. Additionally, live Fast Fourier Transform was monitored and used to better focus the beam during imaging.

2.2.1 Preliminary TEM images of GaAs

Prior to TEM study of finFETs, we took TEM images of GaAs grown on Si plan-view samples prepared by sanding and ion milling. These images, in Figure 7, were a preliminary demonstration that TEM could be used to identify defects and dislocations in III-V materials.

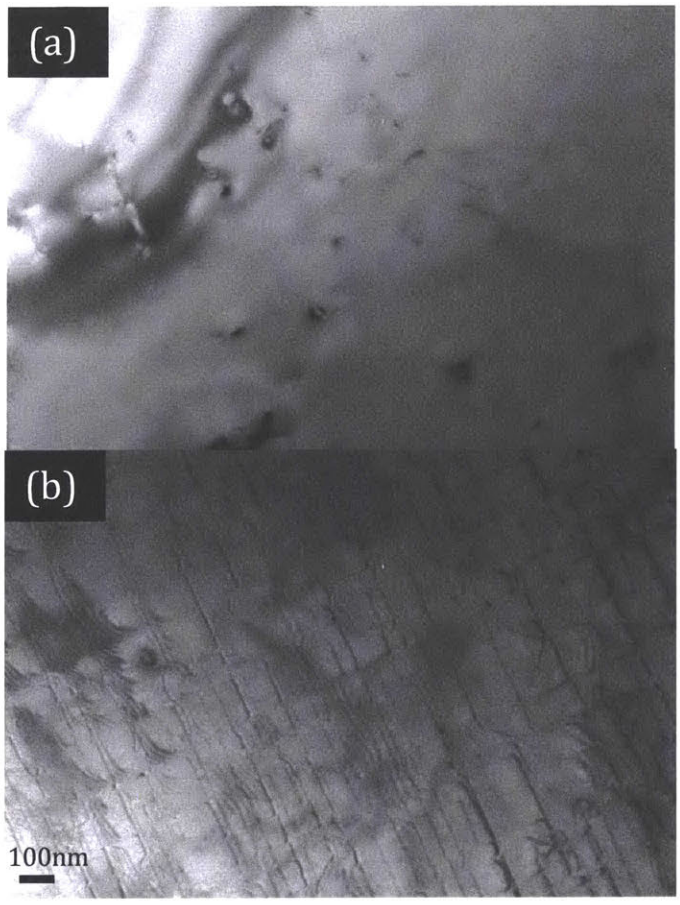

Figure 7. TEM images of plan-view sample of GaAs grown on Si, showing various defects. (a) Inclusions. (b) Misfit dislocations.

TEM reveals the internal structure of a sample at the atomic level. The next chapter shows how TEM was used to study interfacial properties between the channel and high-k dielectric in III-V finFETs as well as to obtain exact dimensions of sample features. These properties were then analyzed alongside electrical characteristics to understand charge transport in novel III-V finFETs.

CHAPTER 3. EXPERIMENTAL RESULTS

In the previous chapter, we gave background on how TEM samples were prepared and imaged. In this chapter, we use TEM images to demonstrate successful fabrication of InGaAs finFETs with W_f = 5nm and InGaSb with W_f = 10nm. We combine analysis of TEM images with electrical characteristics to understand the role of channel/high-k dielectric interfacial properties in device performance.

3.1 Study of InGaAs and InGaSb FinFETs

3.1.1 Demonstration of InGaAs finFETs

Self-aligned InGaAs finFETs were fabricated and studied [17]. In these devices, the InGaAs fins were etched by reactive ion etching and thinned down by several cycles of digital etch, and the high-k dielectric was immediately deposited by atomic layer deposition (ALD). The high-k dielectric consisted of one monolayer of Al_2O_3 and 3nm HfO_2. Figure 8 illustrates the expected fin cross-section.

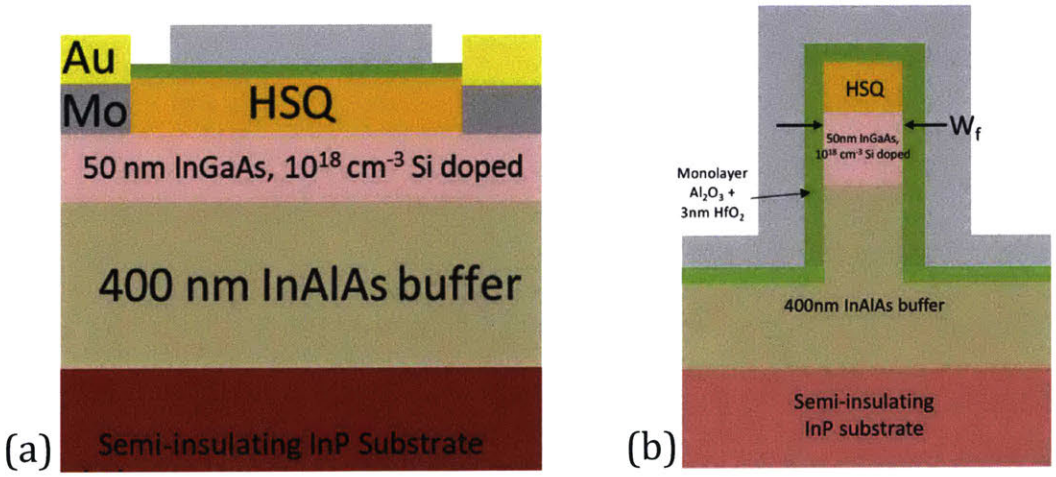

Figure 8. Expected InGaAs finFET cross sections (a) along the fin and (b) across the fin.

After fabrication, a cross-sectional TEM sample was prepared using the steps outlined in section 2.1.5 and imaged. Figure 9 shows that fins were successfully fabricated with a clear, defined channel/high-k dielectric interface.

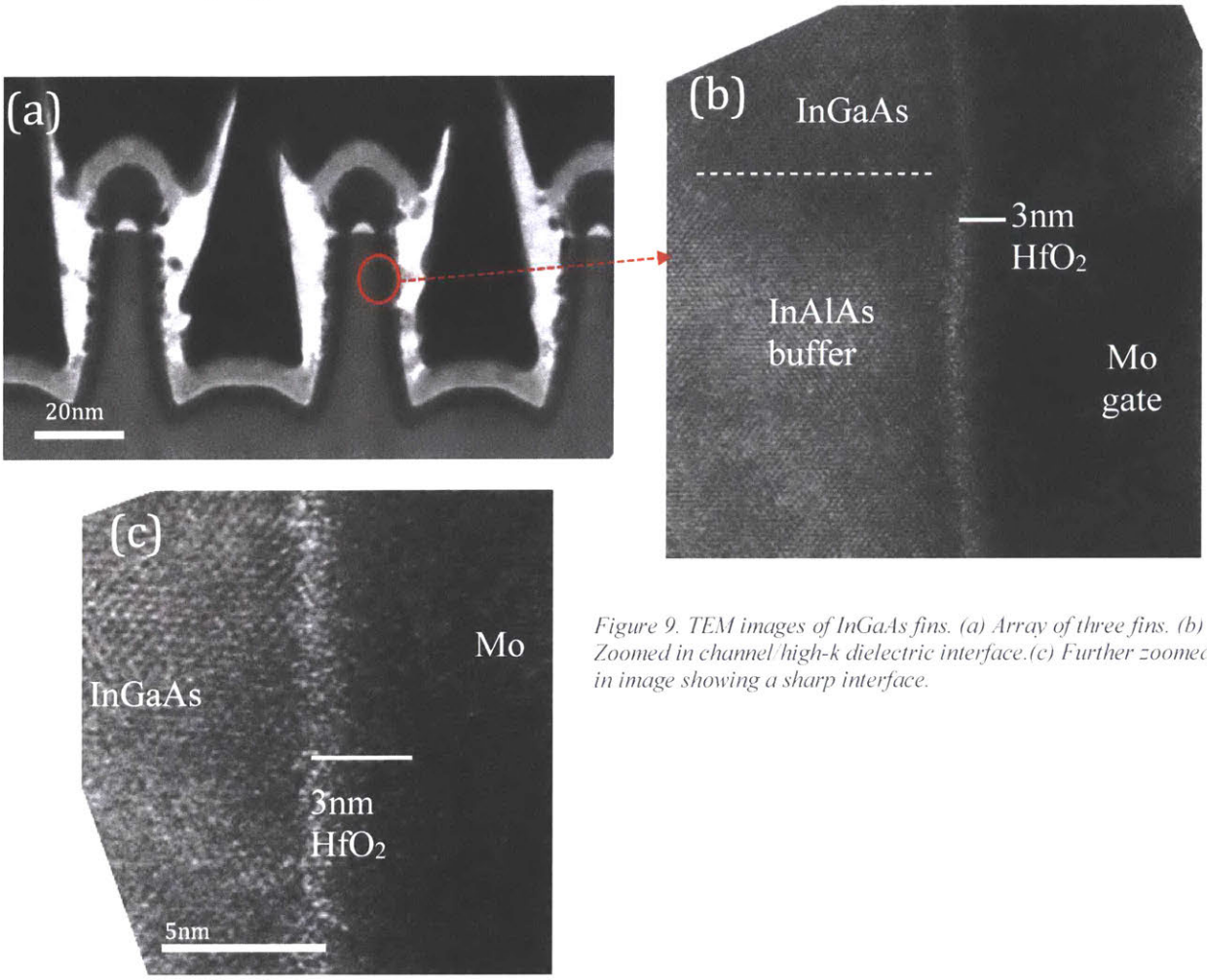

Figure 9. TEM images of InGaAs fins. (a) Array of three fins. (b) Zoomed in channel/high-k dielectric interface.(c) Further zoomed in image showing a sharp interface.

3.1.2 Demonstration of InGaSb finFETs

Self-aligned InGaSb finFETs were also fabricated and studied [18]. Similar to the case of InGaAs devices, digital etch was used to thin the fins, and ALD was then immediately used to deposit the high-k dielectric, 3nm Al_2O_3, at 175°C. However, InGaSb presents additional challenges in the digital etch step. Conventional digital etch using acids dissolved in water

fails with antimonides do to their high reactivity. For these InGaSb devices, a digital etch procedure from a recent work was used [19]; exposure in oxygen plasma was combined with 10% HCl:IPA etch. Figure 10 shows a schematic of the expected device cross-sections along and across the fin.

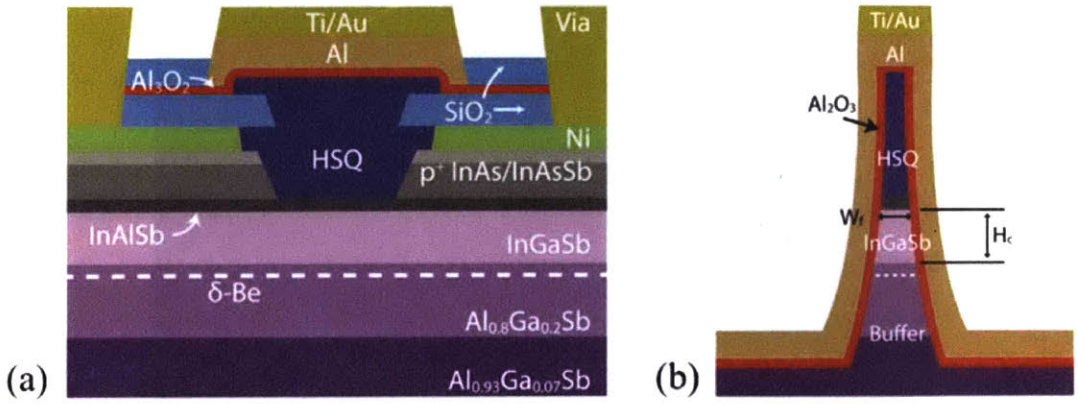

Figure 10. Expected InGaSb finFET cross sections (a) along the fin and (b) across the fin.

Cross-sectional TEM samples both along and across the fin were prepared and imaged. Figure 11 shows TEM images that demonstrate successful fabrication of the InGaSb finFET.

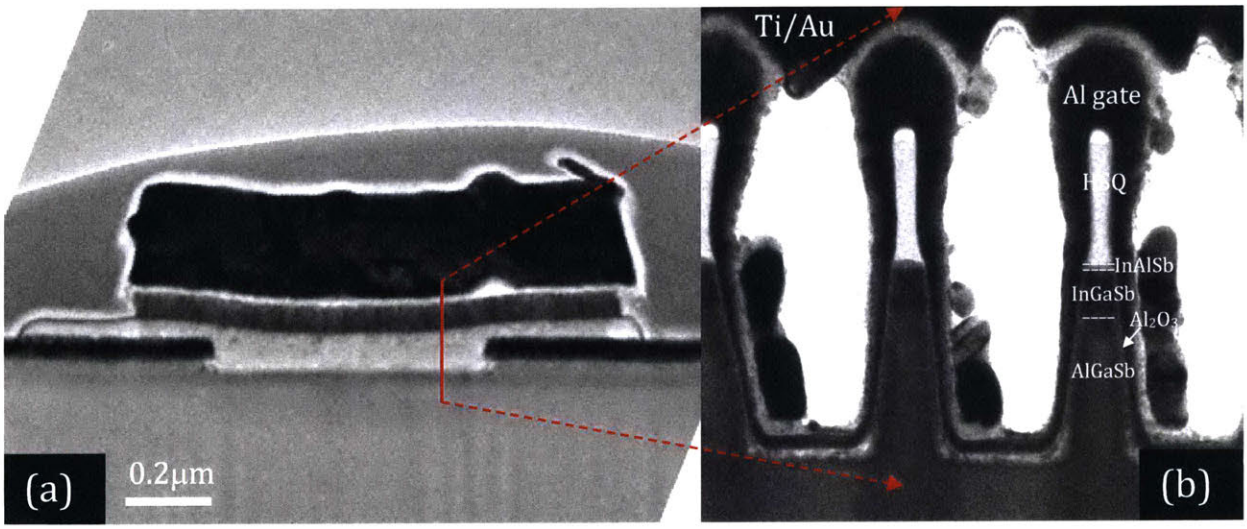

Figure 11. TEM images of InGaSb finFET fin cross sections (a) along the fin and (b) across the fin.

The digital etch step enabled fabrication of fins as thin as 10nm with aspect ratio 2.3, as shown in Figure 11. These are the thinnest InGaSb fins fabricated to date.

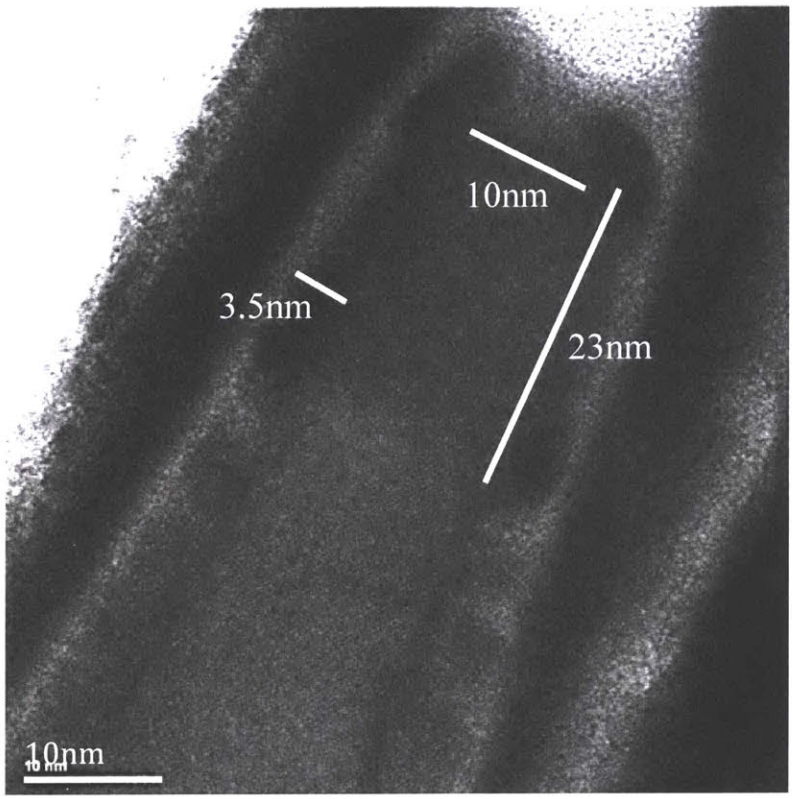

Figure 12. TEM image of InGaSb fin with W_f ~ 10nm.

3.1.3 Comparison of InGaAs and InGaSb finFETs

High-resolution TEM images showed that InGaAs forms a much better interface with the high-k dielectric than InGaSb. Figure 13 shows that the dielectric layer in the InGaSb device is uneven, and also reveals interdiffusion between the channel and dielectric.

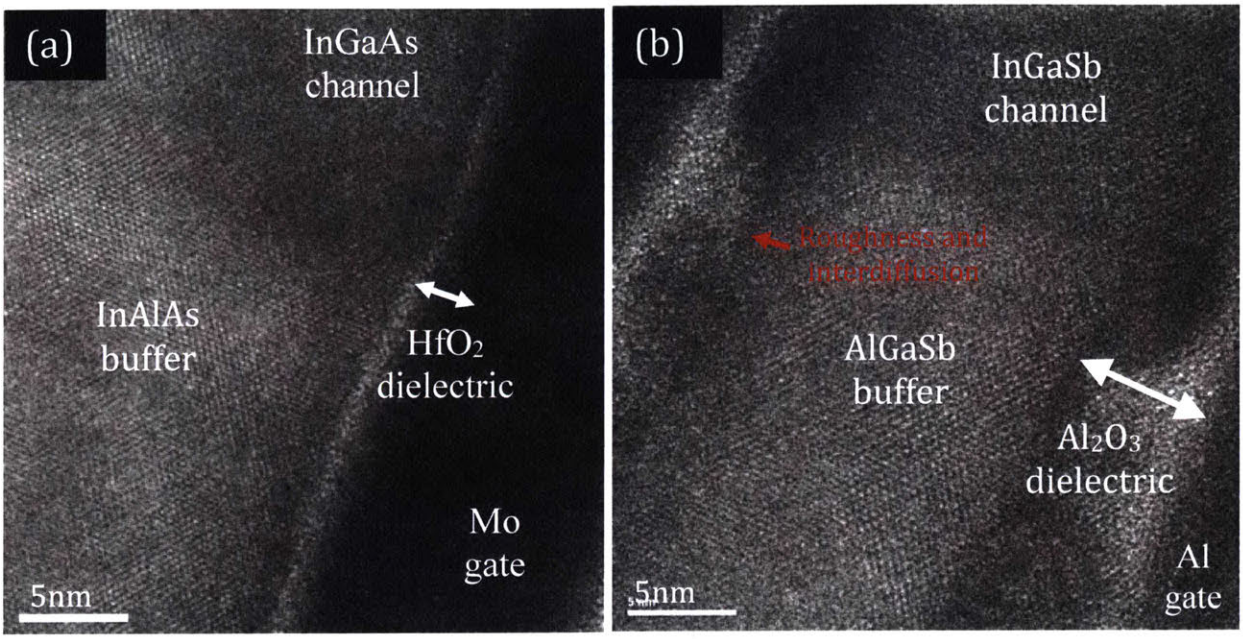

Figure 13. Side-by-side TEM image comparison of (a) InGaAs finFET and (b) InGaSb finFET.

The rough channel/high-k dielectric interface in the InGaSb device is likely due to reactivity of antimonides. The digital etch step used for these devices improved performance compared to devices without digital etch [20], but further work is needed to better passivate the channel prior to deposition of the high-k dielectric.

Electrical characteristics in Figure 14 reflect the superior quality of the InGaAs channel/high-k dielectric interface. I_D-V_{DS} curves demonstrate good saturation behavior for InGaAs finFETs. The devices also achieve a minimum subthreshold swing $S_{lin} \sim 100$

mV/dec, which approaches the ideal S_{lin} = 60 mV/dec. The low S_{lin} indicates that there are minimal trap states present in the device.

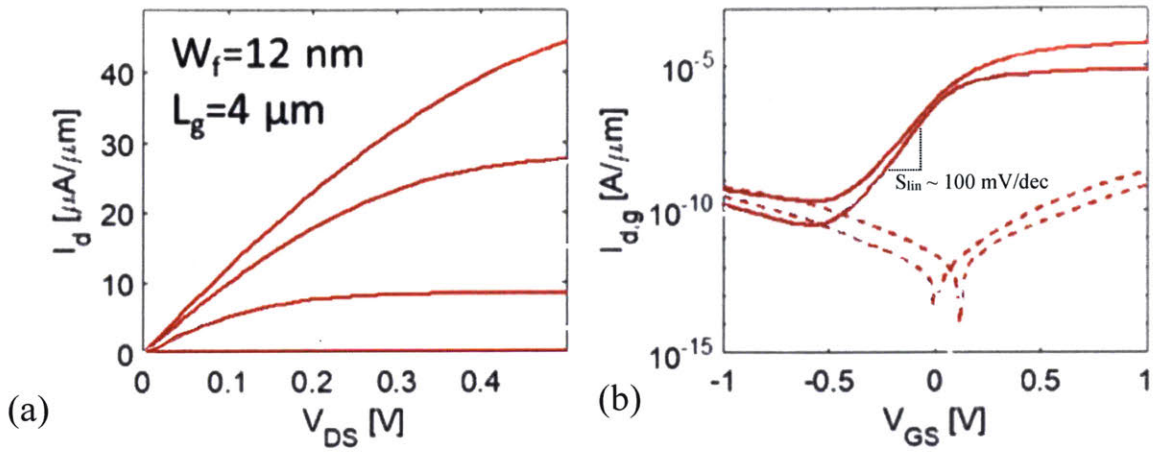

Figure 14. Electrical characteristics for InGaAs finFET with W_f = 12nm and L_g = 4 µm. (a) Output I_D - V_{DS} curves. (b) Subthreshold characteristics.

Figure 15 shows electrical characteristics of the most aggressively scaled InGaSb single-fin device with W_f = 10nm and L_g = 20nm. The characteristics display inadequate gate control of the channel current; the output characteristics show that the device does not achieve good saturation. The high subthreshold swing, S_{lin} = 260 mV/dec indicates the presence of many interface trap states, which cause poor turn-off behavior. These trap states are expected due to the poor interface quality shown in the TEM images above. Figure 16 shows that a longer-channel device has better saturation, but a similarly high subthreshold swing, Slin = 290 mV/dec.

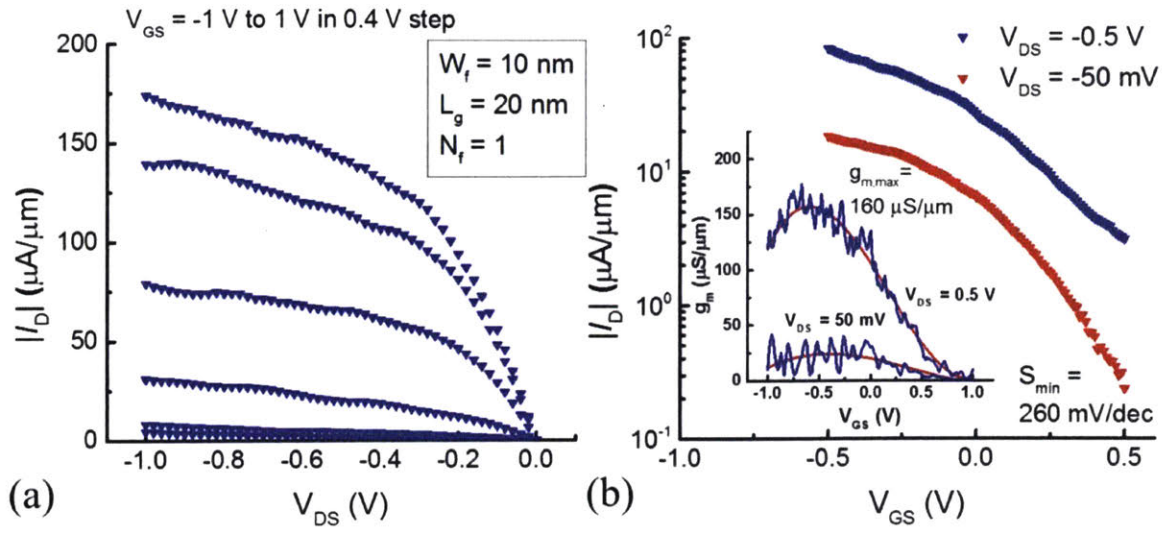

Figure 15. Electrical characteristics for aggressively scaled InGaSb finFET. (a) Output characteristics. (b) Subthreshold characteristics with inset transconductance characteristics.

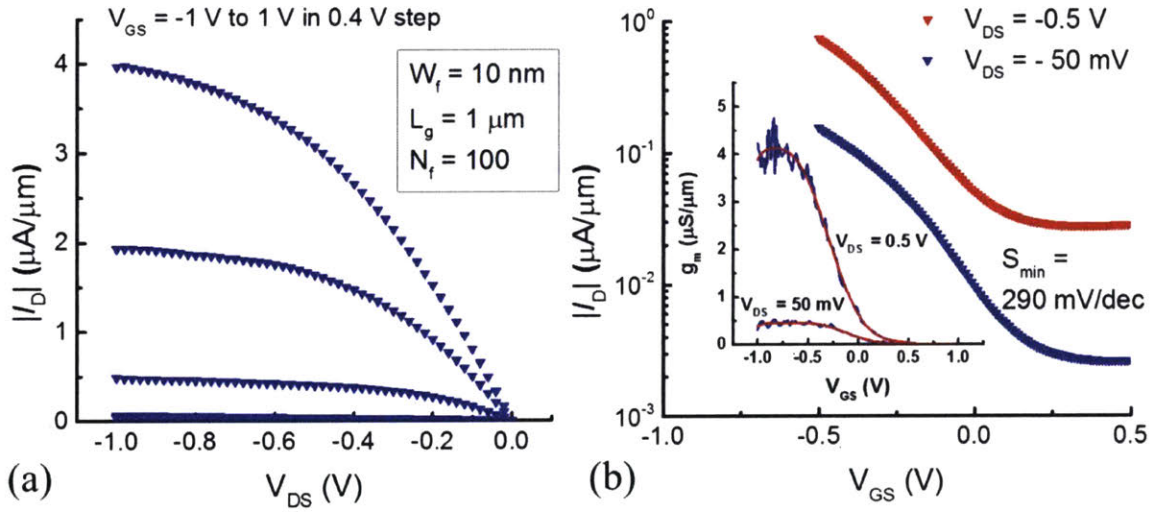

Figure 16. Electrical characteristics for InGaSb long-channel array finFET. (a) Output characteristics. (b) Subthreshold characteristics with inset transconductance characteristics.

3.2 Study of the effect of acid type used in digital etch

Digital etch is a self-limiting etching process that consists of dry oxidation of the semiconductor surface followed by wet etch of the oxide by an acid. Since digital etch is the last step before the high-k dielectric is deposited over the fins, it plays a crucial role in surface preparation and holds the key for further improvements to device transport and electrostatics. In this section, we compare two identical sets of InGaAs FinFETs that underwent digital etch using two different wet etch acids: HCl and H_2SO_4. The expected fin cross section was shown in a previous section, in Figure 8.

To closely analyze fin dimensions, test structures that consisted of fins of varying fin widths in groups of four were imaged. Figure 17 shows a TEM image of some of these test structures. High-resolution TEM showed that the fin shape and dimensions for both digital etch processes were nearly identical (Figures 18,19,20). Both HCl and H_2SO_4 worked well to remove all the oxidized semiconductor. Additionally, both HCl and H_2SO_4 allowed for a defined interface between the semiconductor and high-k dielectric, shown in Figure 21. No apparent differences in interface quality were seen in the TEM images. Both sets of devices displayed a slight bump at the channel/buffer junction but otherwise had smooth channel/dielectric interfaces.

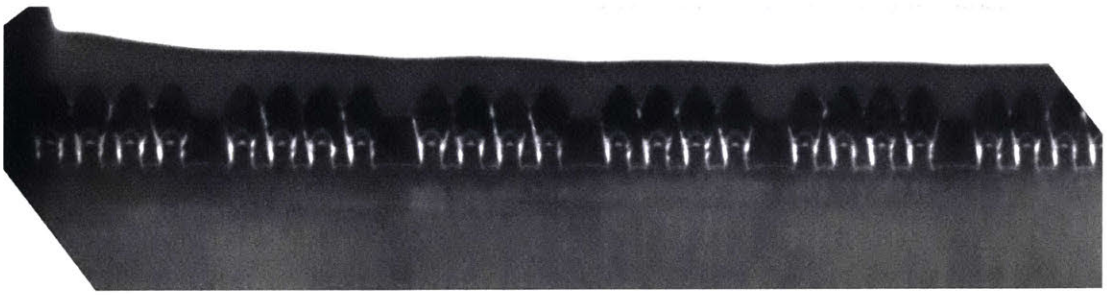

Figure 17. TEM image of fin test structures of varying fin width.

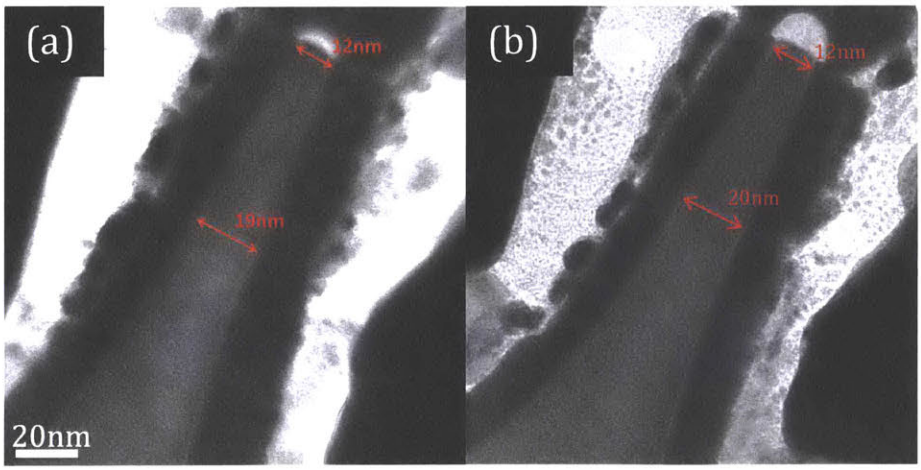

Figure 18. Side-by-side TEM comparison of test structure 1 for (a) HCl and (b) H_2SO_4 digital etch.

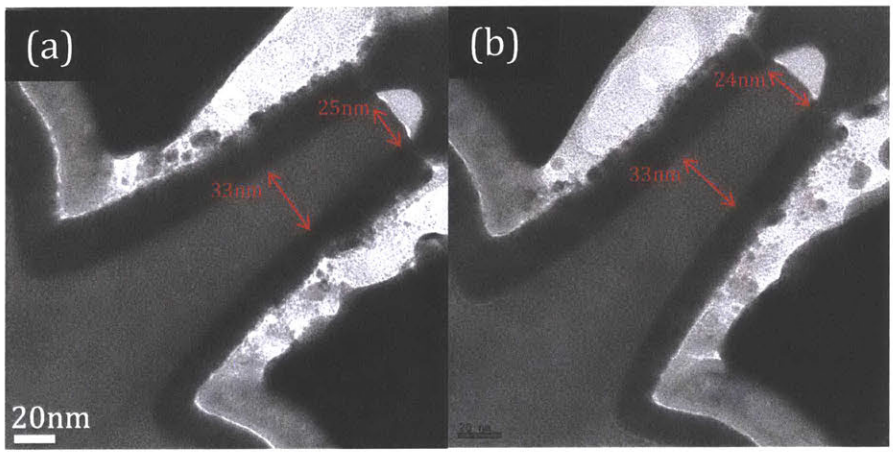

Figure 19. Side-by-side TEM comparison of test structure 3 for (a) HCl and (b) H_2SO_4 digital etch.

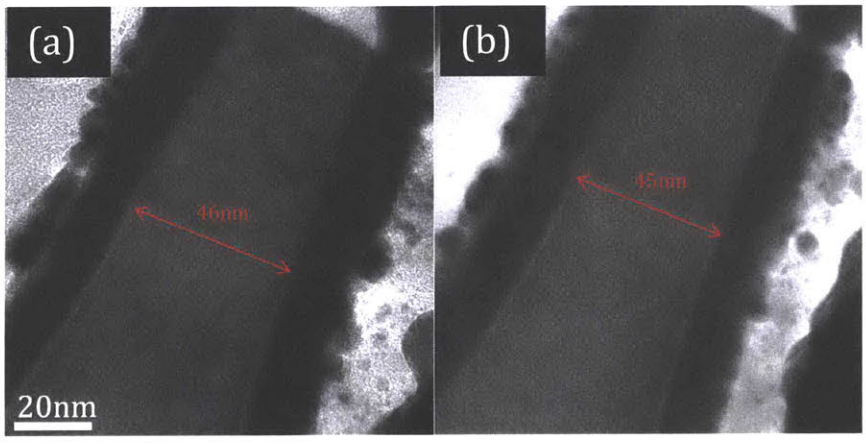

Figure 20. Side-by-side TEM comparison of test structure 6 for (a) HCl and (b) H_2SO_4 digital etch.

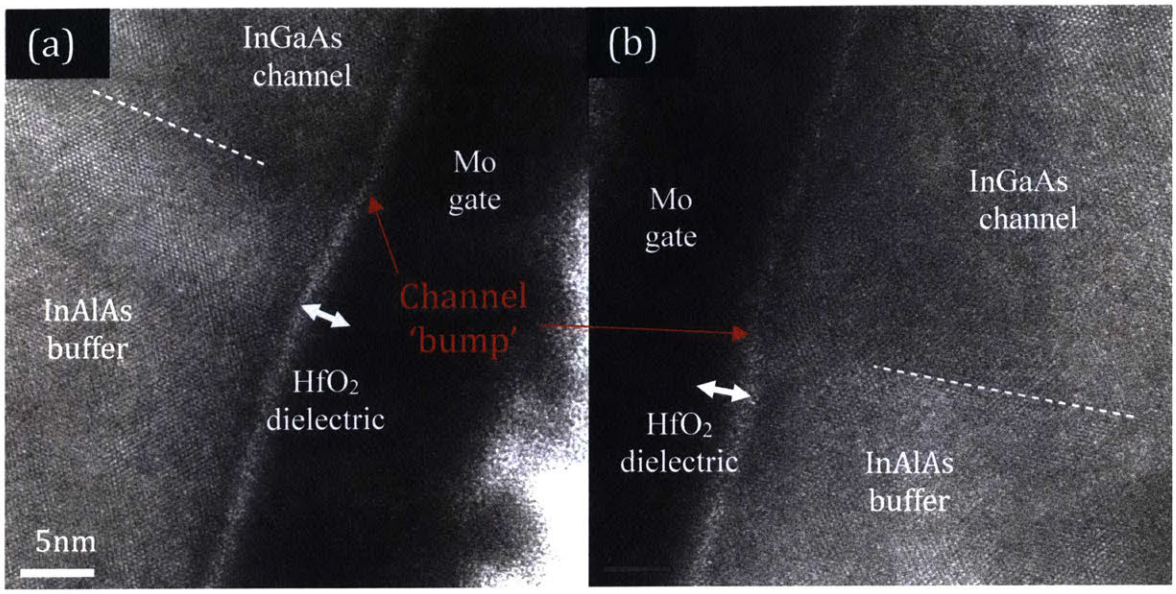

Figure 21. Side-by-side TEM comparison of the semiconductor/high-k dielectric interface for (a) HCl and (b) H_2SO_4 digital etch.

Though differences were not identified in the high-resolution TEM images, the electrical characteristics revealed distinctions between the two sets of devices. Representative characteristics are shown in Figure 22.

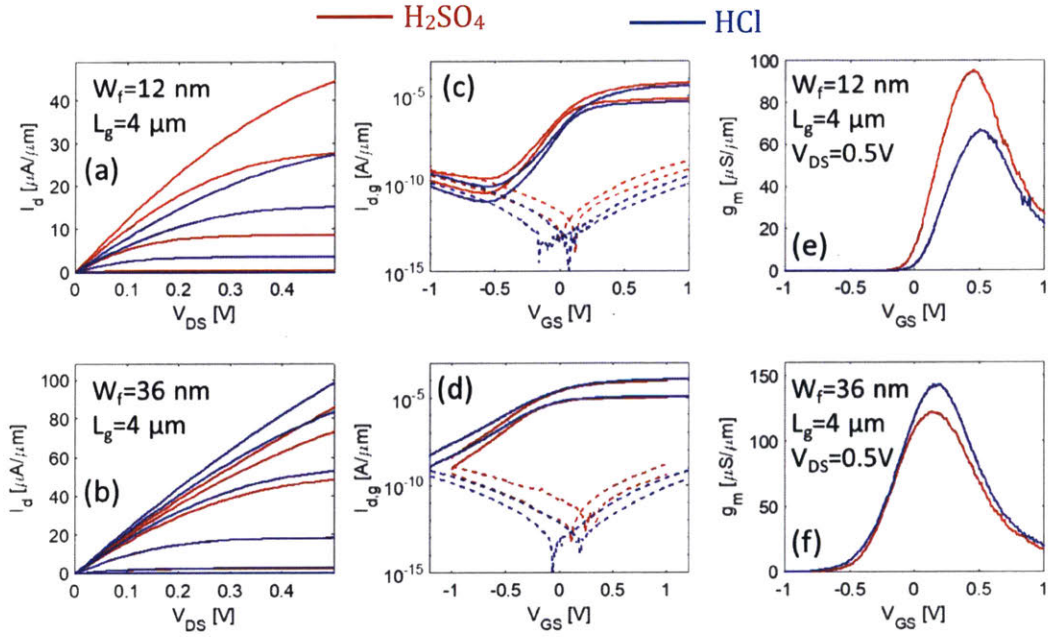

Figure 22. Electrical characteristics for InGaAs finFETs processed with HCl and H_2SO_4. (a), (c), and (d) are for W_f = 12nm. (b), (d), and (f) are for W_f = 36nm.

The characteristics in Figure 22 show that the H_2SO_4 devices perform better for smaller fin widths, but the HCl devices perform better for larger fin widths. In the ON state characteristics, the H_2SO_4 devices reach higher transconductance than analogous HCl devices for W_f = 12nm (Figure 22e), and vice versa for W_f = 36nm (Figure 22f). In the OFF state, HCl devices have lower gate leakage overall (Figures 22c,d), but have a smaller slope in the forward $I_{d,g}$ - V_{GS} curve in Figure 22d, indicating a larger subthreshold swing.

Plots of the subthreshold swing and transconductance over fin width in Figure 23 provide additional insight on why the device performance correlates with fin width.

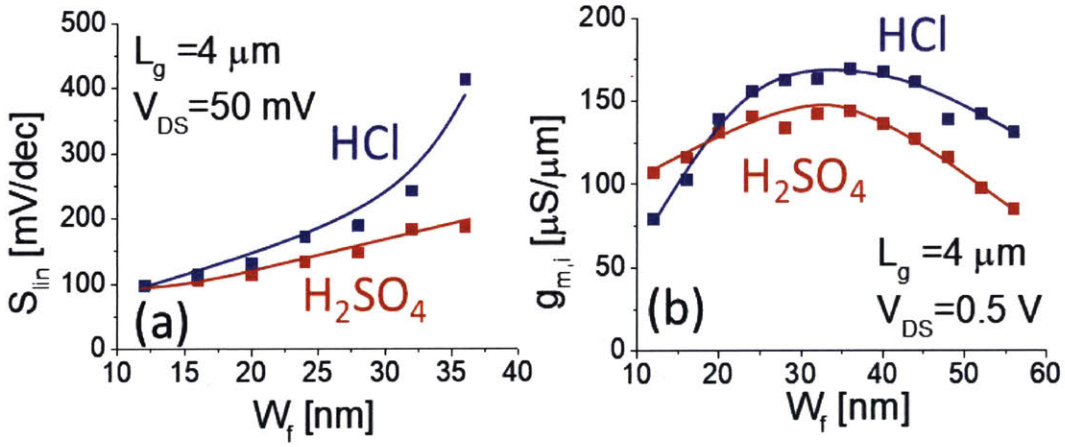

Figure 23. Additional comparisons of HCl and H_2SO_4 devices. (a) S_{lin} over W_f. (b) $g_{m,i}$ over W_f.

Figure 23a shows that the subthreshold swing for the HCl devices is consistently larger than that of the H_2SO_4 devices over varying fin widths. A higher subthreshold swing indicates a higher density of interface trap states at the semiconductor/high-k dielectric interface. Differences between the two sets of samples are theorized to be due to a chlorine ion's smaller size than that of a sulfate group. The higher density of interface states (D_{it}) in

HCl devices could be explained by a chlorine ion's smaller size than that of a sulfate group; the chlorine ion is more likely to remain on the surface after digital etch. The presence of the chlorine ion has been shown to then result in interface states near the conduction band [21].

Figure 23b illustrates the peculiar trend that the intrinsic transconductance is higher in H_2SO_4 devices for low fin width, but higher in HCl devices as fin width increases. Because there is a higher D_{it} in the HCl devices, fewer electrons go to the conduction band. Having fewer charge carriers then increases the mobility. Since the transconductance is a metric of current, both the number of charge carriers and the mobility contribute to the transconductance. The higher mobility in the HCl devices enables higher transconductance for wide fins; but for aggressively scaled fins with $W_f < 20nm$, the carrier concentration in the fin becomes comparable to D_{it} and, as a result, the intrinsic transconductance of the H_2SO_4 devices (with a lower D_{it} toward the conduction band) prevails.

In summary, TEM images confirmed that InGaAs readily forms a good quality interface with an ALD-deposited high-k dielectric. InGaAs device performance depends heavily on the residual molecules left on the semiconductor surface after digital etch.

3.3 Study of W_f = 5nm InGaAs finFETs

The good channel/high-k dielectric interface quality in InGaAs devices enabled the fabrication of self-aligned InGaAs finFETs with fin width as low as 5nm [22]. These highly scaled devices displayed record performance that approaches the performance of state-of-the-art Si finFETs. Figure 24 illustrates the expected fin cross section based on the process flow.

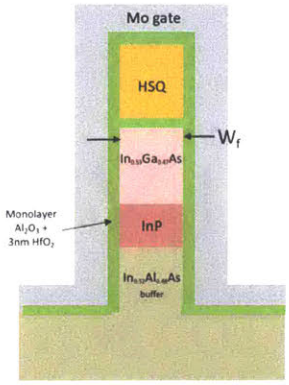

Figure 24. Expected fin cross section for InGaAs finFET.

After fabrication, a cross-sectional TEM sample was prepared. High-resolution TEM revealed that 5nm fin widths were achieved, seen in Figure 25b. Notches in the Mo gate shape are possibly due to damage from the ion beam during TEM sample preparation.

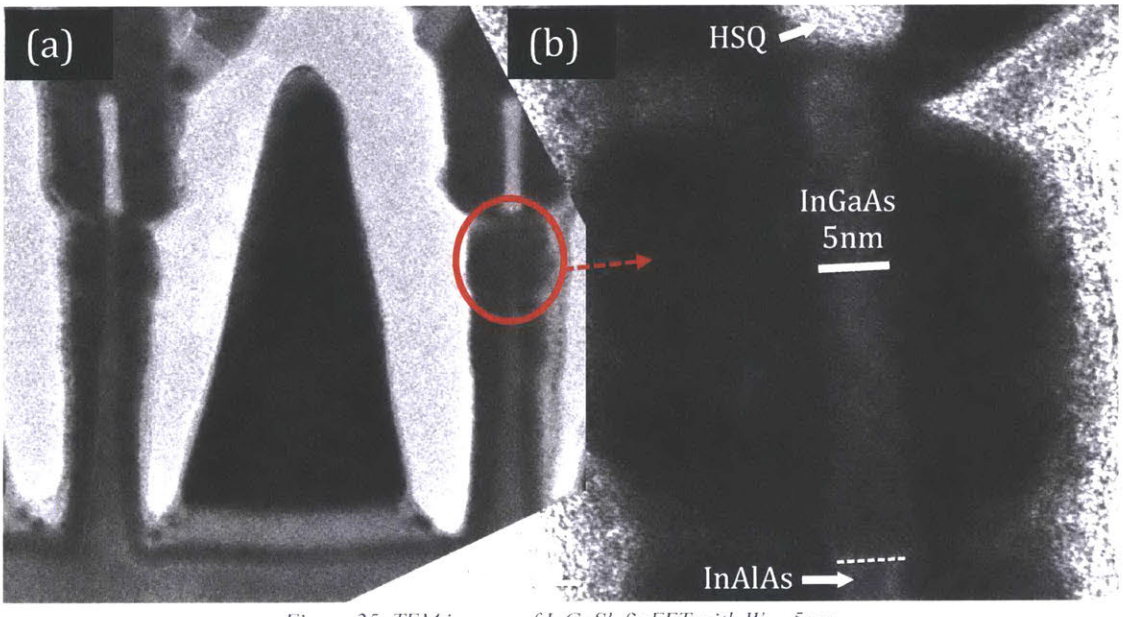

Figure 25. TEM images of InGaSb finFET with W_f ~ 5nm.

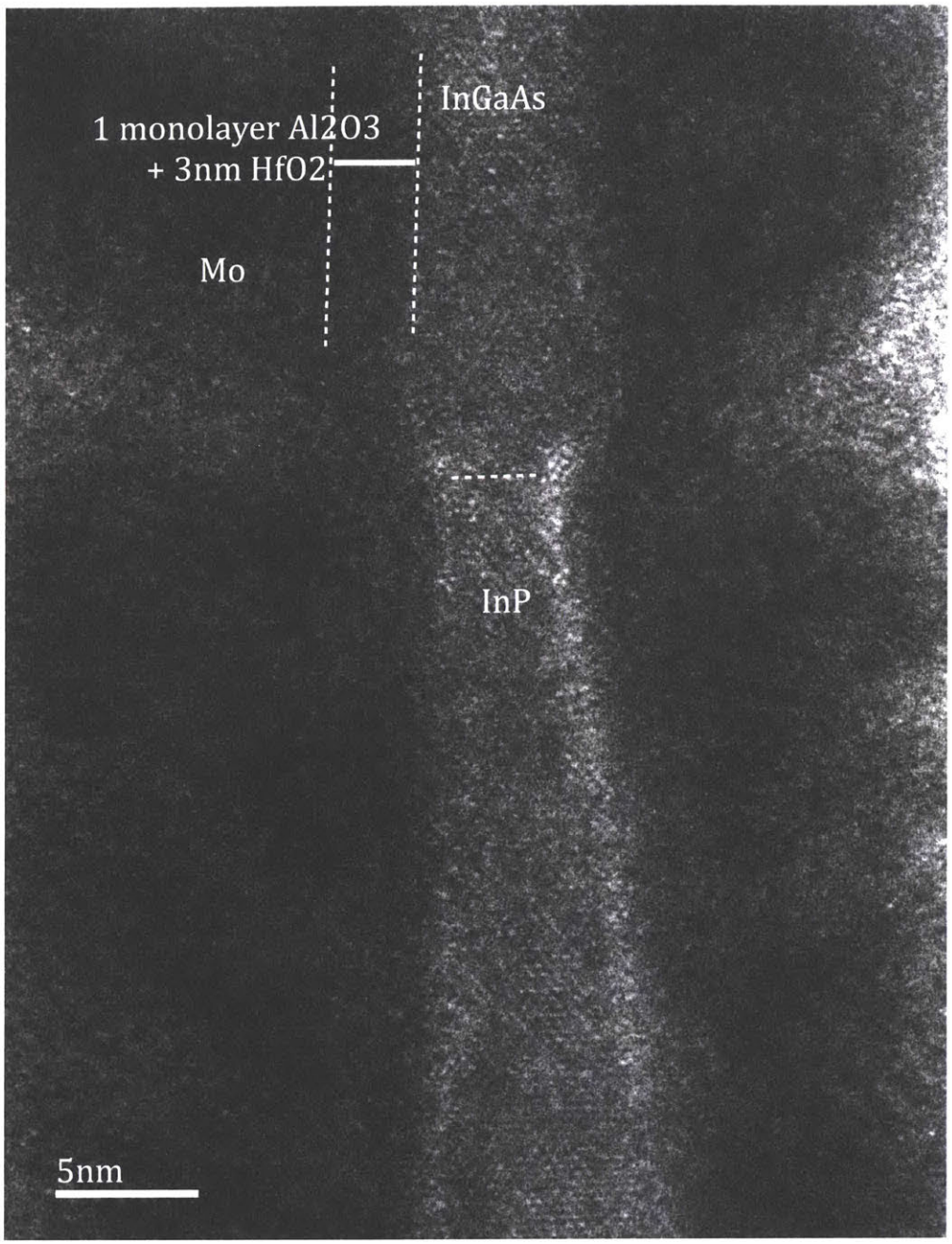

Figure 26. TEM image of InGaAs/high-k dielectric interface.

Figure 26 shows a high-resolution TEM image of a 5nm-wide fin. The channel/high-k dielectric interface is defined but not sharp, and suggests evidence of reaction. The fin shape is slightly uneven and the fin width is not completely uniform.

Electrical characteristics in Figure 27 confirm that these highly scaled InGaAs devices were fabricated with good but imperfect interfacial quality. The devices demonstrate good sidewall control in OFF state characteristics. The subthreshold swing, S_{lin} = 65 mV/dec, approaches the ideal 60 mV/dec. For W_f < 20nm, however, there is a strong dependence of mobility on fin width, indicating the presence of sidewall roughness scattering.

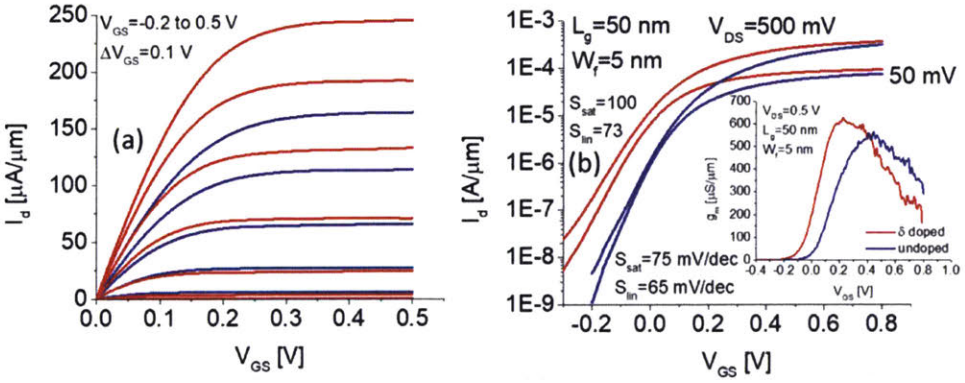

Figure 27. Electrical characteristics for W_f = 5nm device. (a) Output characteristics. (b) Subthreshold characteristics with inset transconductance characteristics.

To further analyze carrier mobility in these InGaAs finFETs, devices with delta-doped fins were also fabricated and tested. Delta-doped fins include a Si delta-doping $4x10^{12}$ cm^{-2} layer in the buffer region. The comparison between electrical characteristics for delta-doped fins and undoped fins revealed that the channel/high-k dielectric interface can still be further improved.

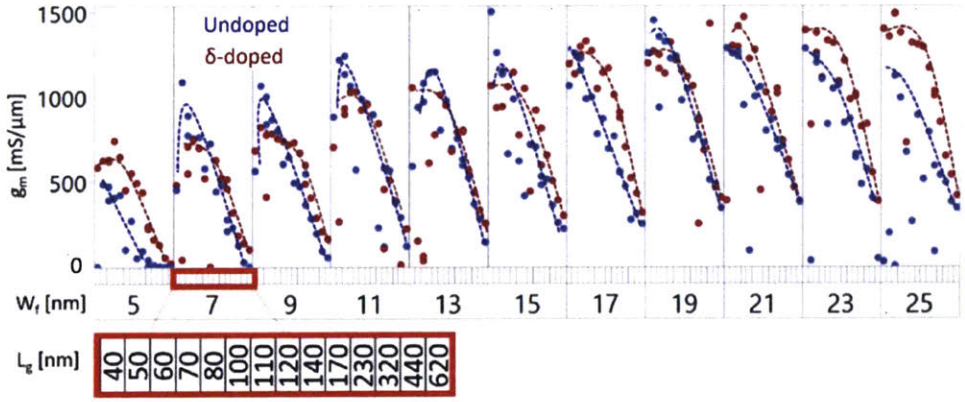

Figure 28. Comparison of g_m for undoped and δ - doped fins across different W_f and L_g.

For the ON state, doped fins demonstrated better performance across nearly all fin widths (Figure 28). Simulations have shown that the presence of the delta-doping layer causes charge distribution to remain highly crowded against the bottom interface, while in undoped fins, electrons pile up against the sidewalls, where interface roughness and scattering is worse [22]. Interface imperfections in these devices were severe enough to cause a clear decrease in performance for undoped fins.

In summary, TEM images demonstrated the successful fabrication of InGaAs finFETs with W_f = 5nm. TEM images showed that the semiconductor/high-k dielectric interface was defined but uneven. Electrical characteristics confirmed that sidewall roughness and scattering had a significant effect on carrier mobility and that interfacial properties are good but can be further improved.

3.4 Preliminary work on all-around gate finFETs fabricated by ALD-ALE

Early stage work has been done to fabricate novel all-around gate III-V finFETS by atomic layer deposition (ALD) combined with atomic layer etching (ALE). This ALD-ALE process was pioneered by the George research group at the University of Colorado - Boulder, and allows the fin etching process and deposition of the high-k dielectric to occur in the same chamber [23].

Electrical characteristics of transistors fabricated by this technique have not yet been obtained, but preliminary TEM images show that an all-around gate has been achieved with excellent channel/high-k dielectric interface quality (Figures 29,30,31). Fins are as thin as ~3nm. Additionally, Figure 31b shows that etching cleanly follows the crystal structure. These images suggest potential for very good devices.

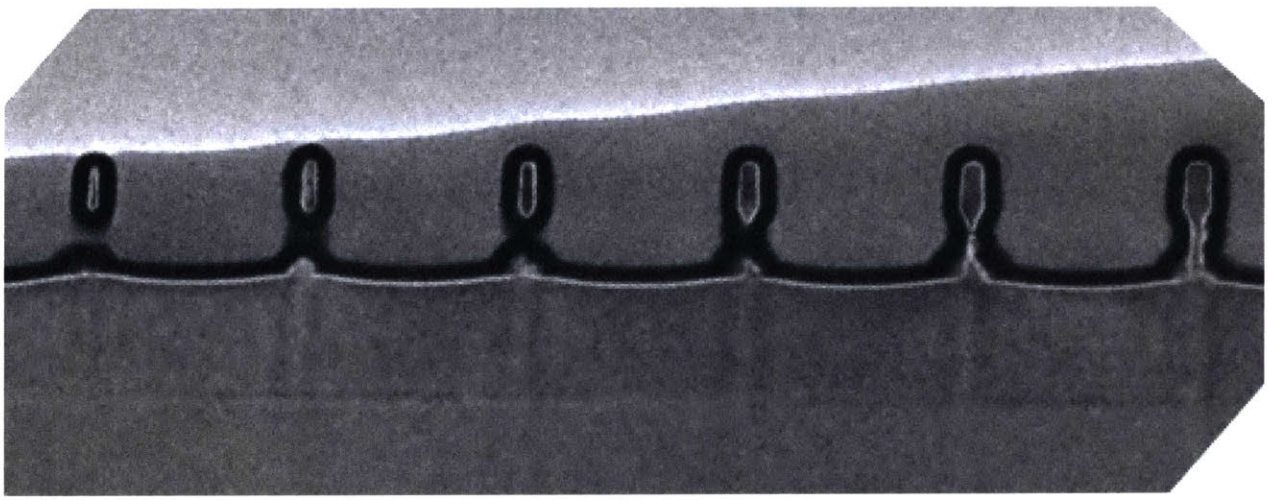

Figure 29. TEM image of III-V fin test structure fabricated by ALD-ALE.

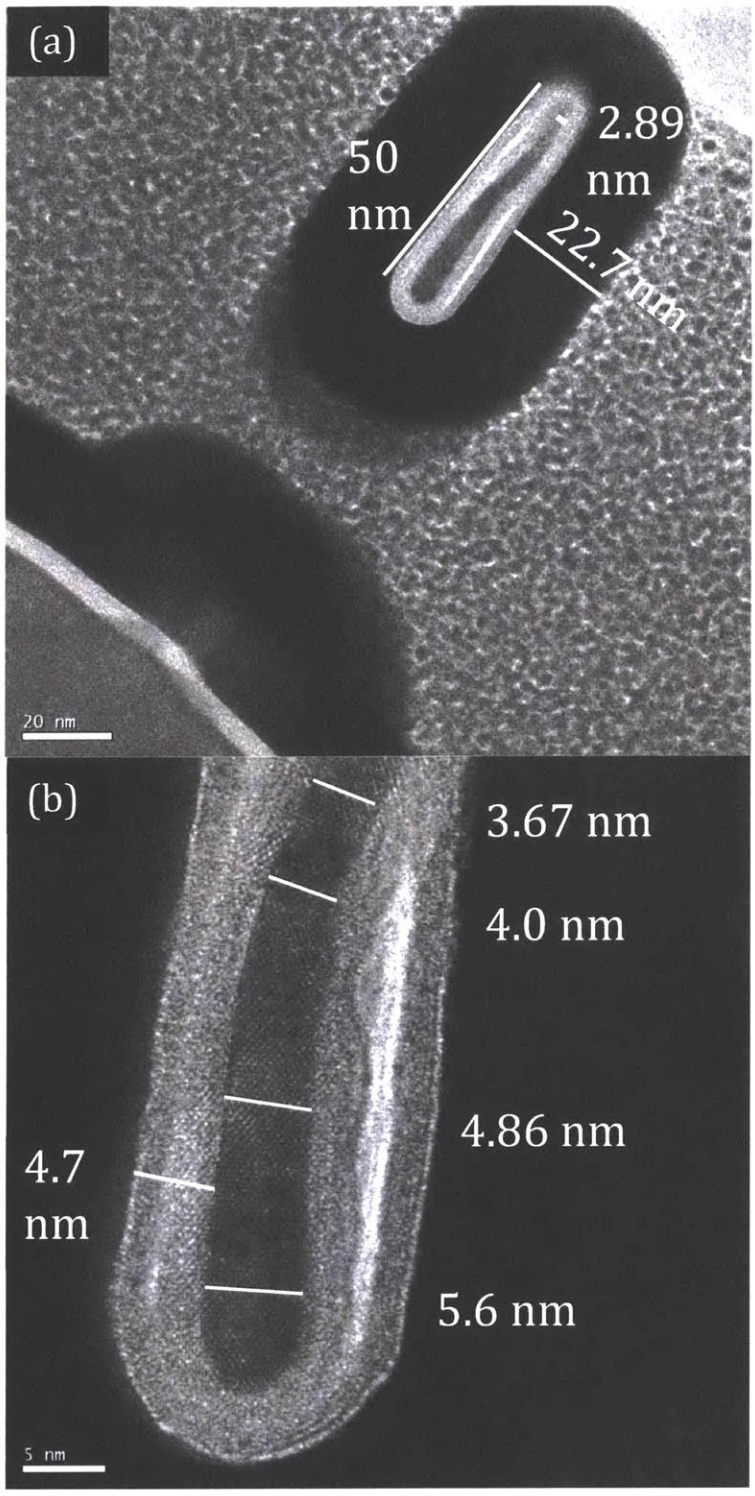

Figure 30. Zoomed in TEM images of test structure 1. W_f is as small as ~3nm.

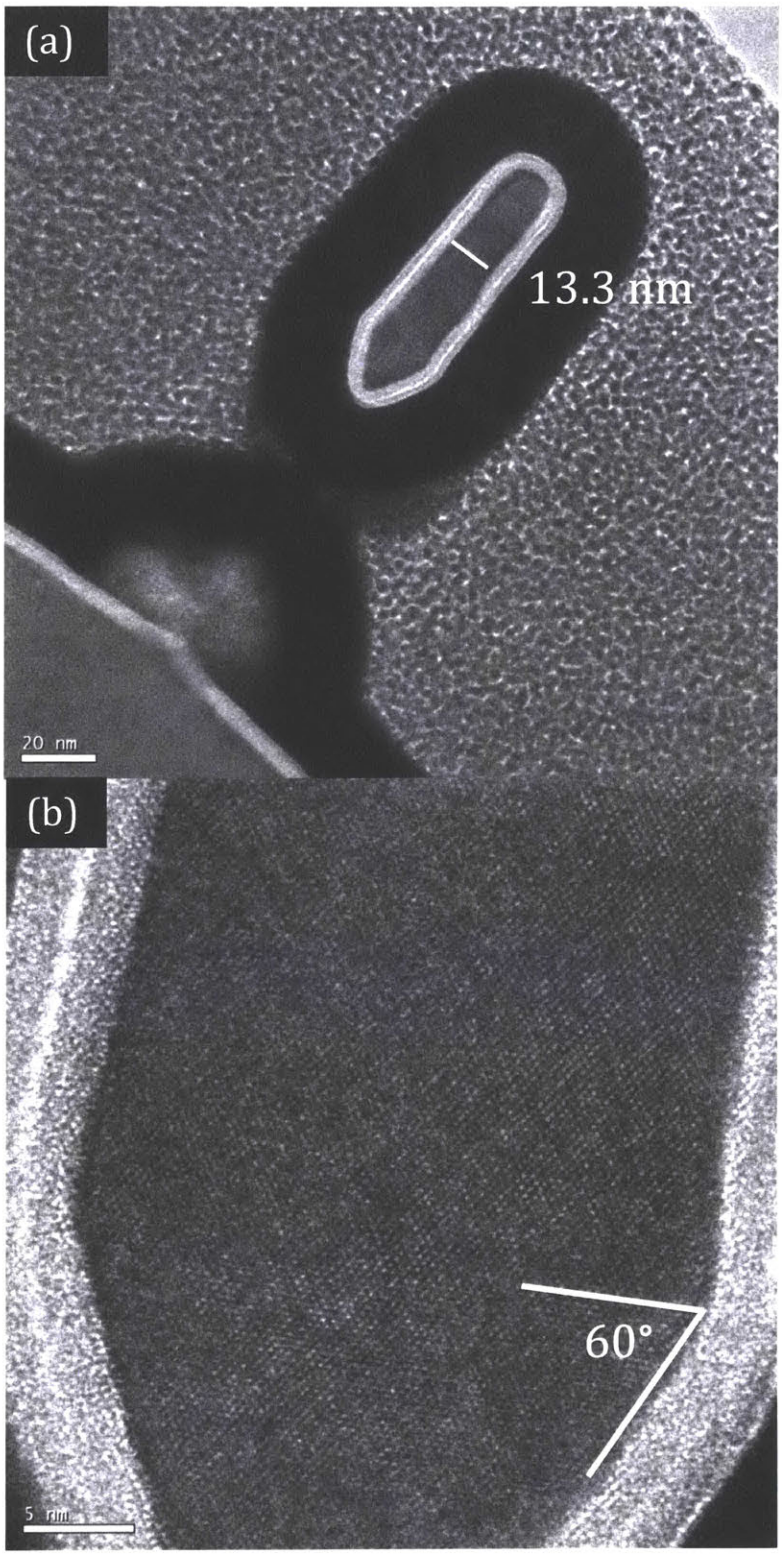

Figure 31. Zoomed in TEM images of (a) test structure 3 (b) test structure 5.

CHAPTER 4. CONCLUSIONS AND FUTURE WORK

4.1 Conclusions

In this thesis work, high-resolution TEM was used to study the channel/high-k dielectric interface in InGaAs and InGaSb channel finFETs. Comparison of InGaAs and InGaSb finFET images showed that InGaAs readily forms a smoother interface than InGaSb does with the high-k dielectric due to the high reactivity of antimonides. Further channel passivation techniques in addition to digital etch are necessary to improve InGaSb devices. Comparison of samples processed using different acids in digital etch demonstrated that while both HCl and H_2SO_4 etch away oxide well, residual molecules create trap states that affect device performance. TEM images also demonstrated successful fabrication of an InGaAs finFET with W_f= 5nm. Electrical characteristics were analyzed along with TEM for all these samples to confirm the importance of interfacial properties identified in TEM images.

Additionally, preliminary TEM images of novel all-around gate structures fabricated by ALD-ALE demonstrate promise of transistors fabricated using this technique. In the final section of this thesis, we provide suggestions for future work.

4.2 Suggestions for future work

To further characterize the channel/high-k dielectric interface, analysis could be performed on the sidewall prior to deposition of the high-k dielectric. Atomic force microscopy (AFM) was explored as a technique to characterize sidewall roughness, but this

work was not completed. Challenges that held this work back were to (i) knock fins over so that the sidewall could be probed horizontally and (ii) achieve a good enough resolution to find noticeable differences in sidewall roughness. If these problems are solved, AFM could be readily used to quantify sidewall roughness in finFETs.

To better analyze and compare TEM images, image processing tools could be used. Recent work in the literature has been done to extract quantitative information from microscopy images [24]. Image processing techniques could be used to find information in TEM images overlooked by the human eye, and to compare images. This additional information would enhance our analysis and understanding of interfacial properties.

Appendix

The work in this thesis has been published in the following:

W. Lu, I. P. Roh, D.-M. Geum, S.-H. Kim, J. D. Song, **L. Kong**, J. A. del Alamo, "10-nm Fin-Width InGaSb p-Channel Self-Aligned FinFETs Using Antimonide-Compatible Digital Etch," *2017 IEEE International Electron Device Meeting*, Dec 2017.

A. Vardi, **L. Kong**, W. Lu, X, Cai, X, Zhao, J, Grajal, J. A. del Alamo, "Self-Aligned InGaAs FinFETs with 5-nm Fin-Width and 5-nm Gate-Contact Separation," *2017 IEEE International Electron Device Meeting*, Dec 2017.

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