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Article

# A Compact Operational Amplifier with Load-Insensitive Stability Compensation for High-Precision Transducer Interface

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**Abstract:** High-resolution electronic interface circuits for transducers with nonlinear capacitive impedance need an operational amplifier, which is stable for a wide range of load capacitance. Such operational amplifier in a conventional design requires a large area for compensation capacitors, increasing costs and limiting applications. In order to address this problem, we present a gain-boosted two-stage operational amplifier, whose frequency response compensation capacitor size is insensitive to the load capacitance and also orders of magnitude smaller compared to the conventional Miller-compensation capacitor that often dominates chip area. By exploiting pole-zero cancellation between a gain-boosting stage and the main amplifier stage, the compensation capacitor of the proposed operational amplifier becomes less dependent of load capacitance, so that it can also operate with a wide range of load capacitance. A prototype operational amplifier designed in 0.13- $\mu\text{m}$  complementary metal-oxide-semiconductor (CMOS) with a 400-fF compensation capacitor occupies 900- $\mu\text{m}^2$  chip area and achieves 0.022–2.78-MHz unity gain bandwidth and over 65° phase margin with a load capacitance of 0.1–15 nF. The prototype amplifier consumes 7.6  $\mu\text{W}$  from a single 1.0-V supply. For a given compensation capacitor size and a chip area, the prototype design demonstrates the best reported performance trade-off on unity gain bandwidth, maximum stable load capacitance, and power consumption.

**Keywords:** analog integrated circuits; operational amplifiers; transducer interface circuit; Internet of Things (IoT) device

## 1. Introduction

The internet of things (IoT) is a new paradigm, which connects any physical objects embedded with ambient computational intelligence to each other such that these objects can recognize others and exchange collected data [1–3]. With the advent of the Internet of Things, there has been an increasing demand on the transducers that are able to perform diverse functions such as sensors, actuators, and radio frequency identification tags, for a wide variety of applications including communication, imaging, display, finance, data centers, transportation, health-care, and biomedical devices [4–10].

Capacitive micromachined ultrasonic transducers (CMUTs) [11–13], piezoelectric transducers [14–16], and electro-neural stimulators [17–21], in particular, need to drive nonlinear capacitive load with a large impedance variation. With such a variable capacitive load, in order to achieve an extremely high-resolution control (e.g., 16-bit resolution) to the extent well beyond the present state-of-the-art, which is typically implemented with less than 6–8-bit resolution [22–24], the electronic interface circuitry of such transducers requires a precision high-gain operational amplifier. However, it is

challenging to design an internally compensated high-gain operational amplifier particularly when the amplifier needs to drive a very wide-range of load capacitance but an available chip area for the amplifier is limited [25–43].

A sufficient direct-current (DC) voltage gain can be generated by multi-stage amplifiers [32–41]. However, multi-stage operational amplifiers suffer from stability problems with variable capacitive loads. Although frequency compensation techniques are commonly used in multi-stage amplifiers to improve feedback stability [25–41], these conventional compensation techniques do not allow a wide range of load capacitance. In addition, a compensation capacitor occupies a large chip area, especially when a high capacitive load exists. The pseudo single-stage (PSS) amplifier [42], which in fact is a multi-stage amplifier, was recently introduced to improve the feedback stability by decreasing its first-stage gain to reduce the compensation capacitor size.

In this paper, we present a gain-boosted two-stage operational amplifier, whose compensation capacitance size is less sensitive of load capacitance compared to the previously reported operational amplifiers. Compared to the PSS amplifier, rather than decreasing the first-stage gain [42], the proposed amplifier alternating-current-couples the first-stage and adds a gain-boosting stage to the second-stage input, which provides a higher flexibility in frequency compensation and also allows low-power operation and a higher unity-gain frequency. The compensation capacitor size of a prototype operational amplifier is up to four orders of magnitude smaller than the load capacitance. By combining the conventional Miller compensation with a pole-zero cancellation technique, compared to the previously reported high-gain operational amplifiers, the proposed operational amplifier allows the smallest compensation capacitor size for a given load capacitance [38–43].

The remainder of this paper is organized as follows. Section 2 reviews the previously known operational amplifier stability compensation techniques. Section 3 presents the operation and architectural analysis of the proposed operational amplifier with a novel stability compensation technique. The detailed circuit implementation and pole-zero cancellation analysis are given in Section 4. Simulation results and performance comparison with the present state-of-the-art are presented in Section 5. Concluding remarks are stated in Section 6.

## 2. Review on Stability Compensation Topologies

### 2.1. Conventional Miller Compensation

Miller compensation, which has been extensively used in integrated operational amplifiers, deals with stability issues in frequency response by introducing capacitor  $C_f$  in series with resistance  $R_f$  between the input and output stage. Figure 1a illustrates the architecture of a two-stage amplifier using conventional Miller compensation [25,44]. Its transfer function from the input  $V_{in}$  to the output  $V_{out}$  is

$$\frac{V_{out}(s)}{V_{in}(s)} = g_{m1} r_{o1} g_{m2} r_{o2} \times \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \left(1 + \frac{s}{\omega_{p2}}\right)}, \quad (1)$$

where the dominant pole  $\omega_{p1}$ , second pole  $\omega_{p2}$  and zero  $\omega_z$  are given as

$$\omega_z = -\frac{g_{m2}}{C_f (1 - g_{m2} R_f)}, \quad (2)$$

$$\omega_{p1} = \frac{1}{r_{o1} C_f (1 + g_{m2} r_{o2})}, \quad (3)$$

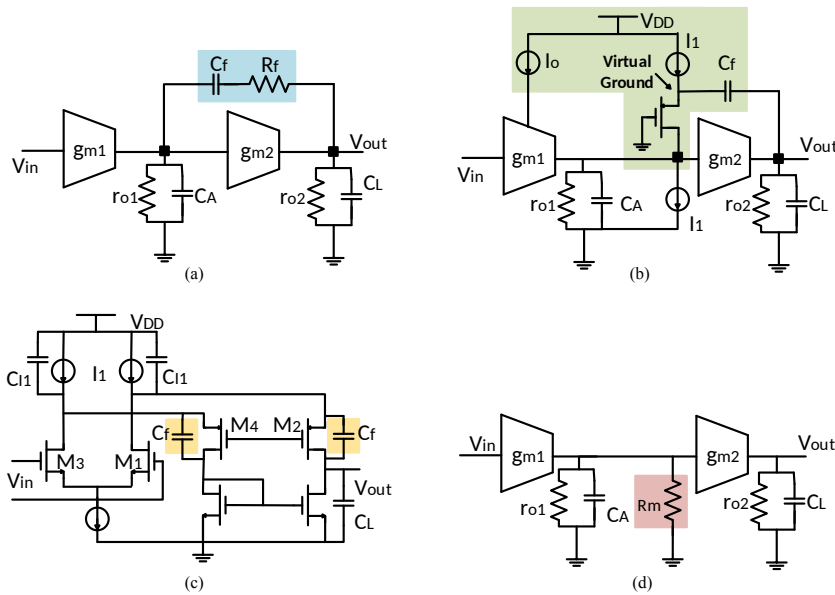
$$\omega_{p2} = \frac{g_{m2} C_f}{C_A C_L + C_A C_f + C_L C_f}, \quad (4)$$

the pole splitting that the output pole is transferred to the second pole is achieved by the Miller compensation [25,44]. The zero can be moved to left half plane by increasing the compensating

resistance value  $R_f$ . Assuming that intrinsic capacitance  $C_A$  is much smaller than load capacitance  $C_L$  and compensation capacitance  $C_f$ , the unity gain frequency  $\omega_u$  is  $g_{m1}/C_f$ , results in

$$\frac{\omega_{p2}}{\omega_u} = \frac{g_{m2} C_f}{g_{m1} C_L}. \quad (5)$$

To avoid the unity gain frequency higher than  $\omega_{p2}$ , which may cause stability issues, the compensating capacitance must be designed larger than  $C_L g_{m1}/g_{m2}$ . Therefore, the conventional Miller compensation topology meets tremendous challenges in driving large capacitive load with a limited footprint.



**Figure 1.** (a) Conventional Miller frequency compensation [25]. (b) Ahuja frequency compensation [26]. (c) Conventional feedforward frequency compensation [27]. (d) Pseudo single-stage amplifier [42]. (Diagrams were redrawn with simplification in order to facilitate the comparison among different compensation techniques.)

## 2.2. Ahuja Compensation

An improved compensation technique was introduced by Ahuja. It utilizes the current transformer providing virtual ground to eliminate feed-forward path in Miller compensation [26], as shown in Figure 1b. The dominant pole  $\omega_{p1}$  is lightly changed from (3) to

$$\omega_{p1} = \frac{1}{r_{o1} C_f g_{m2} r_{o2}'}, \quad (6)$$

while the second pole  $\omega_{p2}$  now is

$$\omega_{p2} = \frac{g_{m2} C_f}{C_A (C_L + C_f)}, \quad (7)$$

which is higher than (4) [27]. The unity gain frequency  $\omega_u$  is still given by  $g_{m1}/C_f$ . As a result, the ratio between the second pole  $\omega_{p2}$  and unity gain frequency  $\omega_u$  is augmented to

$$\frac{\omega_{p2}}{\omega_u} = \frac{g_{m2}}{g_{m1}} \frac{C_f}{C_A} \frac{C_f}{C_f + C_L}. \quad (8)$$

Compared to the conventional Miller compensation, a smaller compensating capacitance is required to drive a same load capacitance for a given phase margin. It copes better with heavy capacitive load [26,45]. However, this reduction is still heavily restricted by the capacitive load.

### 2.3. Conventional Feedforward Compensation

The feedforward compensation technique is introduced to obtain high-frequency performance by implementing pole-zero cancellation [46,47]. Its principle in a folded-cascode amplifier is illustrated in Figure 1c. Assuming poles are widely spread, the positions of zeros and poles are approximately given by

$$\omega_z = \frac{g_{m2}}{(C_f + C_{BD2})}, \quad (9)$$

$$\omega_{p1} = \frac{1}{r_o C_1}, \quad (10)$$

$$\omega_{p2} = \frac{g_{m2}}{\left[ C_2 + C_3 + C_f + \frac{(C_f + C_{BD2})(C_2 + C_{BD1})}{C_1} \right]}, \quad (11)$$

where  $C_1 = C_L + C_{GD2}$ ,  $C_2 = C_{I1} + C_{GS1}$ ,  $C_2 = C_{BD1} + C_{BD2}$ , and the  $r_o$  is the output impedance of this amplifier [27]. For the amplifier without  $C_f$ , the zero is much higher than the second pole as  $C_{BD2}$  is normally much smaller than the capacitors of the second pole. By inserting the feedforward capacitance  $C_f$ , the zero  $\omega_z$  shifts to lower frequency and is practical to cancel the second pole  $\omega_{p2}$ . However, due to the parasitic capacitances, mismatch between the zero and the second pole always exists. It should be noted that the second pole also shifts to lower position, because of  $C_f$ , even though with a minor degree. Consequently, a relatively large  $C_f$  is needed to alleviate this mismatch. This limitation can be relieved by adding a resistance  $R_f$  in series with  $C_f$  [27].

### 2.4. Pseudo Single-Stage Amplifier

The single-stage amplifier only have one high-impedance node at its output, that is why it can drive a large load capacitance without any stability issues. For the pseudo single-stage amplifier, an introduced intermediate resistance  $R_m$  is paralleled with first-stage output impedance  $r_{o1}$ , as shown in Figure 1d, it significantly reduces the output impedance of first stage. Its dominant pole  $\omega_{p1}$  and second pole  $\omega_{p2}$  are obtained as

$$\omega_{p1} = \frac{1}{r_{o2} C_L}, \quad (12)$$

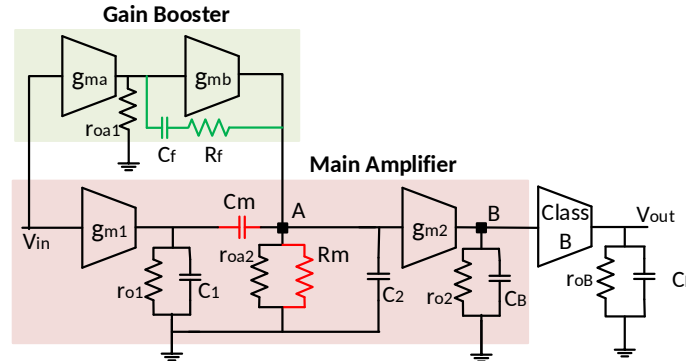
$$\omega_{p2} = \frac{1}{(r_{o1} || R_m) C_A}, \quad (13)$$

because of the small  $R_m$ , the second pole is much higher than the dominant pole [42]. This two-stage amplifier has a frequency response similar to a single-stage amplifier without compensation capacitance. However, this topology is implemented at the expense of insufficient DC voltage gain. This problem can be alleviated by adding a gain booster to the schematic.

In summary, there are mainly two problems existing in these previous frequency compensation topologies. First, the size of compensation capacitor is tightly limited by the load capacitance. Specifically, for a 1-nF load capacitance, the compensation capacitance needed to address stability issues is conventionally larger than 10 pF, which occupies a large proportion of the chip area. In addition, these techniques are required to be optimized based on the single specific load capacitance. As a result, the wide range of load capacitance cannot be driven. In next section, a novel two-stage operational amplifier is introduced to solve these two problems by combing Miller compensation and pole-zero cancellation.

### 3. Proposed Architecture

The proposed operational amplifier architecture is illustrated in Figure 2. It consists of a main amplifier, a gain booster, and a Class-B output stage.



**Figure 2.** Architecture of the proposed gain-boostered two-stage operational amplifier with load-insensitive stability compensation.

In the main amplifier, the first stage transconductance  $g_{m1}$  is alternating-current (AC) coupled to the second stage transconductance  $g_{m2}$  through the capacitor  $C_m$ , the voltage gain at point A is generated by the gain booster. The transfer function from the input  $V_{in}$  to the point A  $V_A$  is

$$\frac{V_A(s)}{V_{in}(s)} = g_{ma} \left[ r_{oa1} \parallel \frac{\left( R_f + \frac{1}{sC_f} \right)}{1 + g_{mb}(r_{oa2} \parallel r_{o1} \parallel R_m)} \right] \times g_{mb} \left[ R_m \parallel r_{oa2} \parallel r_{o1} \parallel \frac{1}{s(C_2 + C_1 \parallel C_m)} \right], \quad (14)$$

where  $g_{ma}$  and  $g_{mb}$  are the transconductance,  $r_{oa1}$  and  $r_{oa2}$  are the output impedance, of the first and second stage of gain booster, respectively.  $r_{o1}$  is the output impedance of the first stage, and  $R_m$  is the inter-stage load impedance, in main amplifier. Because of the Miller effect, the impedance of  $C_f$  in series with  $R_f$  is amplified by  $[1 + g_{mb}(r_{oa2} \parallel R_m)]$ , where  $g_{mb}(r_{oa2} \parallel R_m)$  is the DC voltage gain of the second stage of gain booster. The voltage gain between A and B is

$$\frac{V_B(s)}{V_A(s)} = g_{m2} \left( r_{o2} \parallel \frac{1}{sC_B} \right), \quad (15)$$

where  $r_{o2}$  is the output impedance of the second stage of main amplifier. Therefore, the overall transfer function from the input  $V_{in}$  to the output  $V_{out}$  is obtained as

$$\begin{aligned} \frac{V_{out}(s)}{V_{in}(s)} &= \frac{V_A(s)}{V_{in}(s)} \times \frac{V_B(s)}{V_A(s)} \times \frac{V_{out}(s)}{V_B(s)} \\ &= g_{ma} \left[ r_{oa1} \parallel \frac{\left( R_f + \frac{1}{sC_f} \right)}{1 + g_{mb}(r_{oa2} \parallel r_{o1} \parallel R_m)} \right] \times g_{mb} \left[ R_m \parallel r_{oa2} \parallel r_{o1} \parallel \frac{1}{s(C_2 + C_1 \parallel C_m)} \right] \\ &\quad \times g_{m2} \left( r_{o2} \parallel \frac{1}{sC_B} \right) g_{mB} \left( r_{oB} \parallel \frac{1}{sC_L} \right), \end{aligned} \quad (16)$$

where  $g_{mB}$  and  $r_{oB}$  is the transconductance and output impedance of the Class-B output stage, respectively. Compared to other capacitors in this function,  $C_B$  is much smaller and negligible. This function is approximated to

$$\frac{V_{out}(s)}{V_{in}(s)} \simeq g_{ma} r_{oa1} g_{mb} (r_{oa2} \parallel R_m) g_{m2} r_{o2} g_{mB} r_{oB} \times \frac{\left( 1 + \frac{s}{\omega_{zg}} \right)}{\left( 1 + \frac{s}{\omega_{pg}} \right) \left( 1 + \frac{s}{\omega_{p1}} \right) \left( 1 + \frac{s}{\omega_{p2}} \right)}, \quad (17)$$

where

$$\omega_{zg} = \frac{1}{C_f R_f'} \tag{18}$$

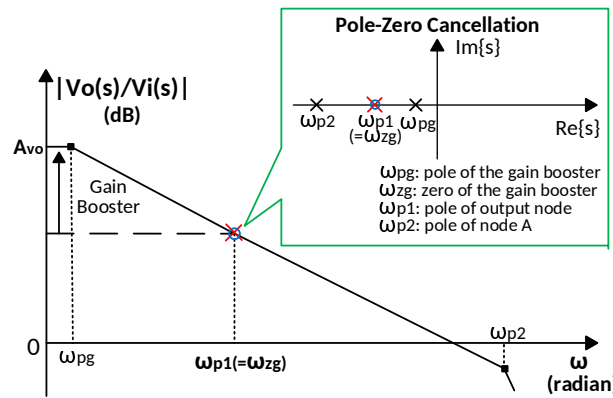
$$\omega_{pg} = \frac{1}{r_{oa1} C_f g_{mb} (r_{oa2} || R_m)} \tag{19}$$

$$\omega_{p1} = \frac{1}{r_{oB} C_L} \tag{20}$$

$$\omega_{p2} = \frac{1}{(R_m || r_{o1} || r_{oa2}) (C_1 || C_m + C_2)} \tag{21}$$

Note that  $\omega_{pg}$  is the dominant pole introduced by the gain booster, and  $\omega_{zg}$  is the zero of the gain booster.  $\omega_{p1}$  is the amplifier output node pole, and  $\omega_{p2}$  is the pole from node A, and  $g_{mB}$  is the transconductance of the Class-B output stage.

Figure 3 illustrates the frequency response of the proposed amplifier. The DC gain is boosted by  $g_{ma} r_{oa1}$ . The gain booster not only increases the DC gain of the main amplifier, but also moves the dominant pole from  $\omega_{p1}$  to  $\omega_{pg}$ , which is independent of  $C_L$ , as shown in Equation (19). However, the extra pole from the gain booster output node reduces the overall phase margin. The Miller compensation by  $C_f$  and  $R_f$  in the gain booster alleviates this problem. The zero of the gain booster  $\omega_{zg}$  is designed to cancel the output node pole,  $\omega_{p1}$ , by choosing a suitable  $C_f$  and  $R_f$ . The pole-zero cancellation enable the proposed work to drive a wide range of load capacitance. The compensation capacitor size comparison between the pseudo single-stage (PSS) amplifier amplifier and this work is given in Table 1. Compared to a PSS amplifier, by taking advantage of Miller compensation, the proposed amplifier reduces the compensation capacitor size by ten times while providing the same DC gain and unity gain bandwidth (UGBW).



**Figure 3.** The gain booster provides a dominant pole  $\omega_{pg}$  and the zero of the gain booster  $\omega_{zg}$  cancels the main amplifier output node pole  $\omega_{p1}$ , thereby making the second pole  $\omega_{p2}$  independent of the load capacitance  $C_L$ .

**Table 1.** Compensation capacitor size comparison between the PSS amplifier and this work.

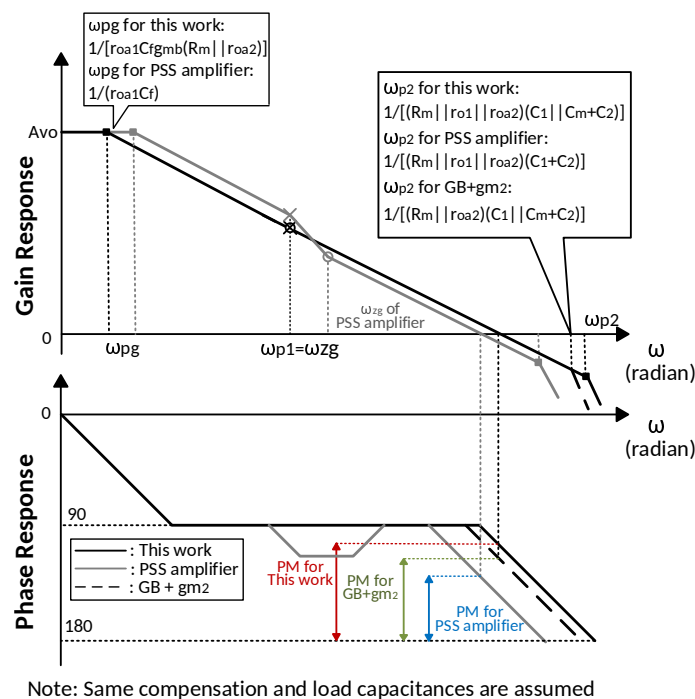
	PSS Amplifier [42]	This Work
Second Pole	$1/[(C_1 + C_2)(r_{o1}    r_{oa2}    R_m)]$	$1/[(C_1    C_m + C_2)(r_{o1}    r_{oa2}    R_m)]$
UGBW	$A_v / (C_f r_{oa1})$	$A_v / [C_f r_{oa1} g_{mb} (r_{oa2}    R_m)]$
$C_f$	1	$\approx 1 / [g_{mb} (r_{oa2}    R_m)] \approx 0.1$

Note: The same second pole location and unity-gain bandwidth (UGBW) are assumed.

The stability of the operational amplifier is dominated by its phase margin, which is the difference between the phase and 180° at the unity-gain cut-off frequency. For a two-pole system, assuming poles are widely spread, its phase margin (PM) is given as

$$\begin{aligned}
 PM &= 180^\circ - \frac{180^\circ}{\pi} \tan^{-1} \left( \frac{\omega_u}{\omega_{p1}} \right) - \frac{180^\circ}{\pi} \tan^{-1} \left( \frac{\omega_u}{\omega_{p2}} \right) \\
 &\simeq 90^\circ - \frac{180^\circ}{\pi} \tan^{-1} \left( \frac{\omega_u}{\omega_{p2}} \right),
 \end{aligned}
 \tag{22}$$

where the  $\omega_{p1}$  and the  $\omega_{p2}$  are the dominant and second pole respectively, the  $\omega_u$  is the unity gain frequency. For the proposed work, the phase margin is primarily determined by the pole from the node A,  $\omega_{p2}$ , as shown in (21), which is not affected by the load capacitance  $C_L$ . The capacitance at node A is much smaller than the compensation capacitance and load capacitance. The gain booster and  $R_m$  raise the second pole location from  $1/(C_A r_{o1})$  to  $1/[C_A(r_{o1} || r_{oa2} || R_m)]$  where  $C_A$  is approximately but less than  $(C_1 + C_2)$  and  $C_m$  is designed to be much larger than  $C_1$  and  $C_2$ . Then the ratio between the second pole and the unity gain frequency is increased, which broadens the phase margin. Compared to the design without  $g_{m1}$ , the proposed amplifier moves  $\omega_{p2}$  higher from  $1/(C_A(r_{oa2} || R_m))$  to  $1/[C_A(r_{o1} || r_{oa2} || R_m)]$ . The comparison about frequency response bode plots among this work, the PSS amplifier [42] and the design without  $g_{m1}$  is shown in Figure 4. With same compensation and load capacitance, this work achieves a larger phase margin and wider unity gain bandwidth.



**Figure 4.** Frequency response for this work, the PSS amplifier [42] and the design without the first stage of main amplifier (GB+  $g_{m2}$ ).

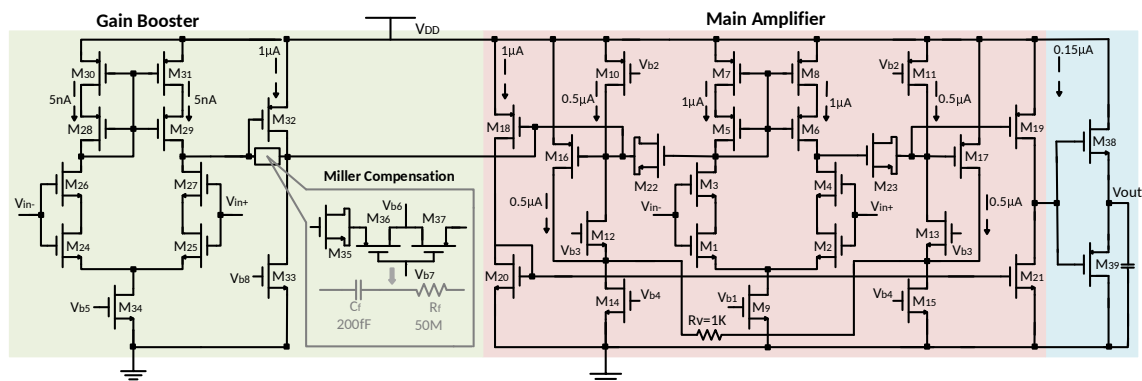
While the two-stage amplifier implementing conventional Miller compensation has a second pole determined by the load capacitance, as shown in Equation (4), the dominant and second pole of this work, which are shown in EquationS (19) and (21), are both independent of the load capacitance. As a result, this work can maintain a sufficient phase margin with various load capacitance, and this frequency compensation topology is less sensitive to the load capacitance compared to the conventional Miller compensation.



## 4. Circuit Implementation and Analysis

### 4.1. Circuit Implementation

Figure 5 shows the circuit of the proposed operational amplifier. Its transistor size is shown in Table 2. The composite cascode [48] is used as input stage in both the main amplifier and the gain booster in order to obtain sufficient DC voltage gain. Compared to the single transistor with doubled length, the composite pair can provide higher gain. A previous work indicated that the voltage gain exceeding 80 dB per stage can be achieved by the composite cascode configuration with transistors operating in weak or moderate inversion domain [49]. A Class-B output stage is implemented to provide a fast settling time by improving the amplifier slew rate.



**Figure 5.** Schematic of the proposed gain-boosted two-stage operational amplifier with load-insensitive stability compensation.

**Table 2.** Transistors size of the proposed work.

Device	Size ( $\mu\text{m}/\mu\text{m}$ )	Device	Size ( $\mu\text{m}/\mu\text{m}$ )	Device	Size ( $\mu\text{m}/\mu\text{m}$ )
M <sub>1</sub> , M <sub>2</sub>	1.7/2.5	M <sub>3</sub> , M <sub>4</sub>	6.55/0.17	M <sub>5</sub> , M <sub>6</sub>	4/0.13
M <sub>7</sub> , M <sub>8</sub>	0.13/0.14	M <sub>9</sub>	3.3/0.2	M <sub>10</sub> , M <sub>11</sub>	5/1
M <sub>12</sub> , M <sub>13</sub>	20/1	M <sub>14</sub> , M <sub>15</sub>	7.5/1	M <sub>16</sub> , M <sub>17</sub>	0.2/0.24
M <sub>18</sub> , M <sub>19</sub>	0.15/0.16	M <sub>20</sub>	0.15/2.52	M <sub>21</sub>	0.15/1.35
M <sub>22</sub> , M <sub>23</sub>	5/5	M <sub>24</sub> , M <sub>25</sub>	0.13/26	M <sub>26</sub> , M <sub>27</sub>	0.13/0.38
M <sub>28</sub> , M <sub>29</sub>	0.15/0.3	M <sub>30</sub> , M <sub>31</sub>	0.15/12.05	M <sub>32</sub>	0.15/0.16
M <sub>33</sub>	0.32/0.17	M <sub>34</sub>	0.2/0.2	M <sub>35</sub>	10/5
M <sub>36</sub> , M <sub>37</sub>	0.29/0.13	M <sub>38</sub>	0.7/0.13	M <sub>39</sub>	0.8/0.13

Design parameters of the proposed amplifier are shown in Table 3. The inter-stage load resistance  $R_m$  can be realized by a negative feedback loop as

$$R_m = \frac{1}{g_{mv}} + \frac{2}{g_{mf} R_v g_{mv}}, \quad (23)$$

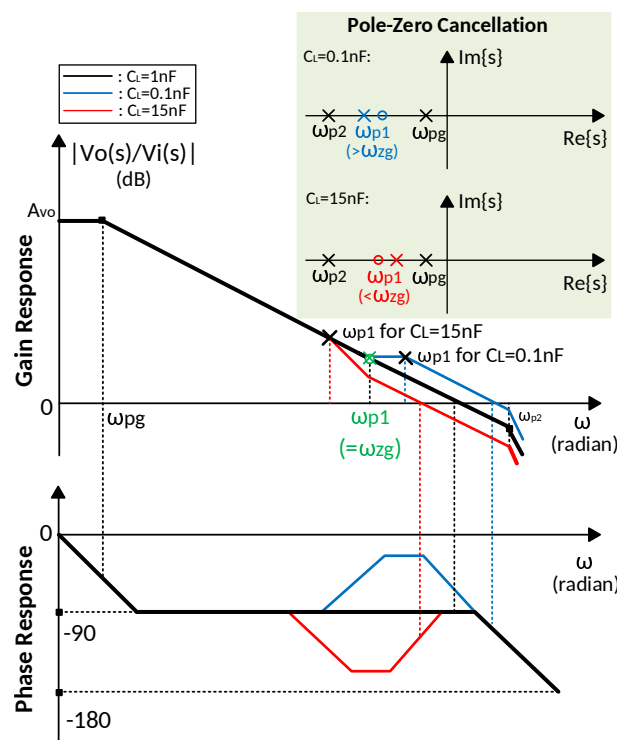
where the  $g_{mv}$  is the transconductance of M<sub>16</sub> and M<sub>17</sub>, and the  $g_{mf}$  is the transconductance of M<sub>12</sub> and M<sub>13</sub> [42]. The  $R_m$  is optimized though choosing suitable  $g_{mv}$  and  $g_{mf}$  to make the second pole  $\omega_{p2}$  much higher than unity gain frequency to obtain sufficient phase margin.  $R_f$  is replaced by floating tunable CMOS resistors to reduce the chip area [50]. The bias circuit for this work is illustrated in Figure A1 and Table A1.

**Table 3.** Design parameters of the proposed work.

Transconductance	Value ( $\mu\text{S}$ )	Transconductance	Value ( $\mu\text{S}$ )
$g_{m1}$	13.1	$g_{m2}$	15.0
$g_{ma}$	0.094	$g_{mb}$	13.2
Capacitance	Value (fF)	Capacitance	Value (fF)
$C_m$	100	$C_f$	200
Resistance	Value ( $\text{M}\Omega$ )	Resistance	Value ( $\text{M}\Omega$ )
$R_m$	20	$R_f$	50

#### 4.2. Pole-Zero Cancellation and Sensitivity Analysis

In order to drive a wide range of load capacitance,  $\omega_{zg}$  is designed to cancel  $\omega_{p1}$  with a load capacitance in-between 0.1 nF and 15 nF, as shown in Figure 6. The  $\omega_{zg}$  is designed lower than the output node pole  $\omega_{p1}$  with minimum load capacitance, which is 0.1 nF. With the increase of load capacitance, the  $\omega_{p1}$  gets lower and the precise pole-zero cancellation occurs. Then as the load capacitance further increases, the  $\omega_{p1}$  get smaller than the  $\omega_{zg}$ , and the precise pole-zero cancellation condition is broken, as a result, the phase margin become worse. To prevent a large degradation in the amplifier phase margin, the zero is designed to cancel the  $\omega_{p1}$  with 1-nF load capacitance. Since a precise pole-zero cancellation is difficult to realize, especially when the load capacitance has a large variation, the pole-zero doublet of  $\omega_{p1}$  and  $\omega_{zg}$  may degrade the settling time.



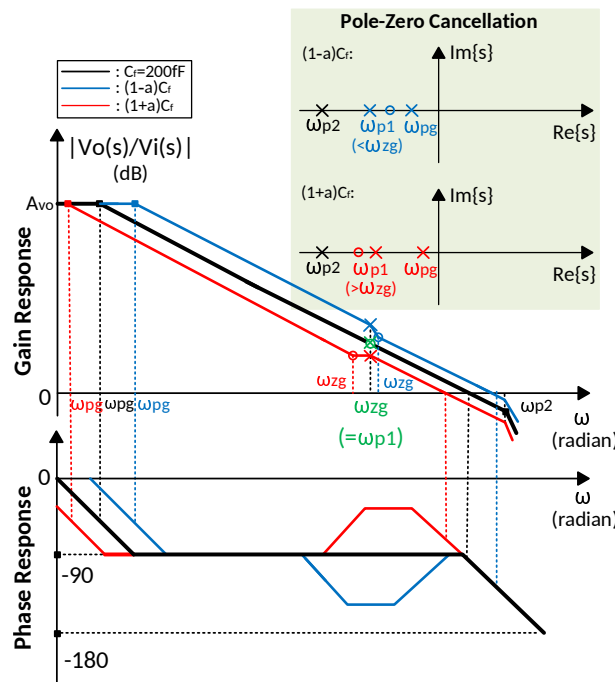
**Figure 6.** Bode plots of pole-zero cancellation with a 0.1–15-nF load capacitance, precise pole-zero cancellation occurs at  $C_L = 1$  nF.

The effect of Miller compensation capacitance variation on the precise pole-zero cancellation is illustrated in Figure 7. The variation on  $C_f$  causes a change on both zero and pole introduced by the gain booster, then the unity gain frequency is also changed, while the second pole is fixed. For a +10% change, both  $\omega_{zg}$  and  $\omega_{bg}$  is decreased by 10%, while the ratio between second pole and unity gain frequency is enlarged result in wider phase margin. In contrast, for a –10% variation, both  $\omega_{zg}$  and

$\omega_{bg}$  in increased by 10%, and phase margin is degenerated. The change on the unity gain frequency is approximately obtained as

$$\Delta\omega_u \simeq \frac{1}{1+a} \left[ \frac{1}{C_f R_f} - \frac{1}{r_{oa1} C_f g_{mb}(r_{oa2} || R_m)} \right], \tag{24}$$

where  $a$  is the variation on  $C_f$ . Because the unity gain frequency  $\omega_u$  is much higher than  $\omega_{p1}$ , which is  $1/(C_f R_f)$ , compared to  $\omega_u$ ,  $\Delta\omega_u$  is negligible. Consequently, the pole-zero cancellation is insensitive to the variation on Miller compensation capacitance.



**Figure 7.** Bode plots of pole-zero cancellation over variations on Miller compensation capacitance for 1-nF load capacitance.

### 4.3. Common-Mode Rejection Ratio Analysis

The common-mode rejection ratio (CMRR) of the differential amplifier reflects its ability of rejecting identical signal components on both inputs. The CMRR is defined as

$$CMRR = \frac{|A_{DM}|}{|A_{CM}|}, \tag{25}$$

where  $A_{DM}$  is the differential-mode gain and  $A_{CM}$  is the common-mode gain. It determines the attenuation applied to the noise from environment. The high CMRR is crucial for the instruments which usually work in noisy environment.

For the proposed amplifier, its common-mode rejection ratio at low frequency is typically determined by the first stage of the gain booster. Assuming that the intrinsic gain of the transistor  $g_m r_o$  is much larger than one, the differential-mode gain of this stage is approximately obtained as

$$A_{DM,gb1} \simeq g_{m25} (g_{m27} r_{o27} r_{o25} || g_{m29} r_{o29} r_{o31}), \tag{26}$$

while its common-mode gain is approximated as

$$A_{CM,gb1} \simeq \frac{1}{2g_{m31} r_{o34}}, \tag{27}$$

Then the CMRR of the proposed work at DC is

$$\begin{aligned} \text{CMRR} &= \frac{|A_{\text{DM,gb1}}|}{|A_{\text{CM,gb1}}|} \\ &= \frac{1}{2g_{m31}r_{o34}} \times g_{m25}(g_{m27}r_{o27}r_{o25} \parallel g_{m29}r_{o29}r_{o31}) \\ &= 104 \text{ dB}, \end{aligned} \quad (28)$$

which is close to the simulated CMRR of 109 dB.

## 5. Simulation Results and Discussion

The proposed amplifier is designed using a 130-nm CMOS technology with a total area of 0.00090 mm<sup>2</sup>. Its layout is shown in Figure 8. The proposed amplifier without bias circuit occupies 0.00073-mm<sup>2</sup> chip area. The total stability compensation area is 100 μm<sup>2</sup>.

The stability simulation with 0.05–17 nF load capacitance over Miller compensation capacitance variations are shown in Figures 9 and 10 and Tables 4 and 5. For the prototype amplifier, the maximum phase margin is achieved when load capacitance  $C_L$  is 2.5 nF, which is 91°. The phase margin larger than 70° with a load capacitance of 0.2–12 nF and it becomes less than 65° when the load capacitance exceeds the 0.1–15-nF range. With the 30% variation on Miller compensation capacitance, the largest change in phase margin is less than 8% and demonstrates a good tolerance on process variation.

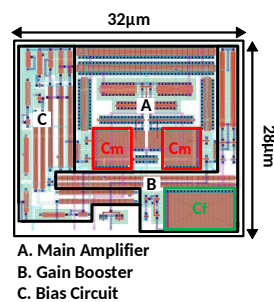


Figure 8. Layout of the proposed amplifier in 130-nm technology.

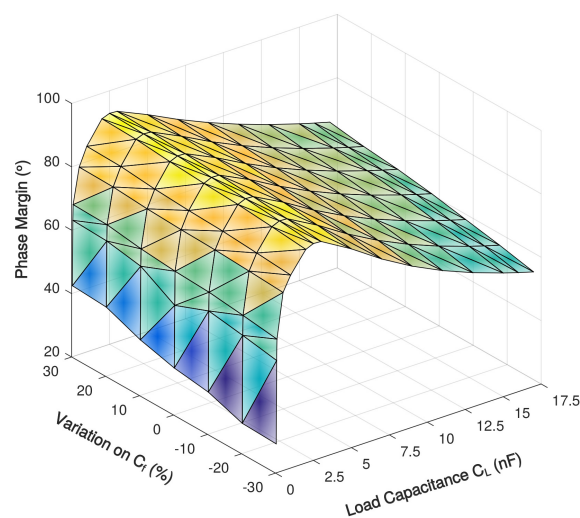
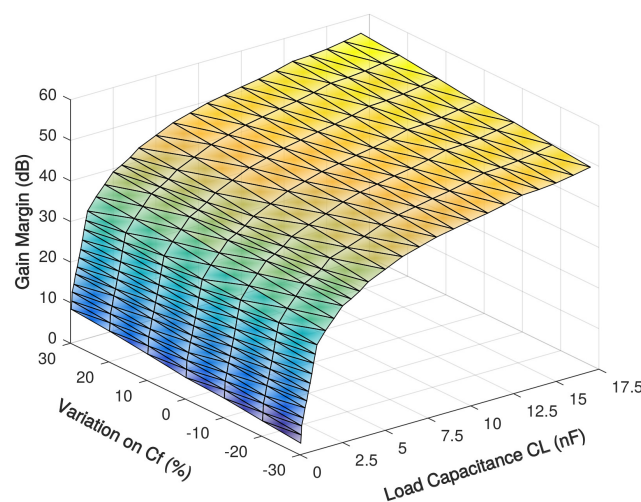


Figure 9. Simulated phase margin of the proposed amplifier with 0.05–17 nF load capacitance over Miller compensation capacitance variations.

**Table 4.** Phase margin over variations on Miller compensation capacitor.

$C_L$ (nF)	This Work	70% $C_f$	80% $C_f$	90% $C_f$	110% $C_f$	120% $C_f$	130% $C_f$
0.08	59.5°	55.5°	57.2°	58.8°	60.7°	62.7°	63.0°
0.1	65.2°	62.1°	63.5°	64.7°	66.2°	67.7°	67.9°
0.2	73.7°	71.0°	72.2°	73.1°	74.8°	76.0°	77.4°
0.5	77.7°	76.2°	76.8°	77.4°	78.1°	78.9°	79.1°
1	82.9°	80.8°	81.7°	82.5°	83.6°	84.6°	84.9°
2.5	90.9°	88.4°	89.5°	90.3°	91.7°	92.2°	92.9°
7	80.9°	76.3°	78.1°	79.5°	82.0°	82.8°	83.7°
12	70.2°	65.2°	66.6°	68.5°	71.5°	72.3°	73.1°
15	65.8°	59.1°	61.4°	63.3°	66.9°	68.0°	69.5°
16	63.9°	58.8°	60.0°	61.9°	65.5°	66.5°	68.1°

**Figure 10.** Simulated gain margin of the proposed amplifier with 0.05–17 nF load capacitance over Miller compensation capacitance variations.**Table 5.** Gain margin over variations on Miller compensation capacitor.

$C_L$ (nF)	This Work	70% $C_f$	80% $C_f$	90% $C_f$	110% $C_f$	120% $C_f$	130% $C_f$
0.08	8.9 dB	5.0 dB	7.1 dB	8.5 dB	10.6 dB	11.4 dB	12.5 dB
0.1	10.9 dB	6.2 dB	8.4 dB	10.1 dB	11.2 dB	12.0 dB	13.8 dB
0.2	11.2 dB	7.1 dB	9.0 dB	10.8 dB	11.9 dB	13.0 dB	14.8 dB
0.5	13.6 dB	9.7 dB	11.0 dB	12.8 dB	14.2 dB	15.4 dB	16.1 dB
1	28.3 dB	25.4 dB	26.6 dB	27.9 dB	29.4 dB	30.5 dB	31.2 dB
2.5	36.2 dB	32.0 dB	33.4 dB	35.6 dB	37.0 dB	37.8 dB	38.9 dB
7	45.2 dB	41.9 dB	43.1 dB	44.5 dB	46.4 dB	47.7 dB	48.2 dB
12	49.6 dB	46.8 dB	47.6 dB	48.9 dB	51.2 dB	52.1 dB	53.0 dB
15	51.3 dB	48.4 dB	49.3 dB	50.7 dB	52.4 dB	53.0 dB	54.1 dB
16	52.0 dB	48.2 dB	49.6 dB	51.3 dB	53.2 dB	54.1 dB	55.9 dB

The simulated frequency response with a 2.5-nF load capacitance is shown in Figure 11, demonstrating 130-kHz unity-gain frequency and over 100-dB gain at DC. The frequency response of the amplifier without the gain booster is separately simulated, which is labeled as  $g_{m1} + g_{m2}$ , showing a significant DC gain drop as expected from the AC coupling between  $g_{m1}$  and  $g_{m2}$ . In addition, the frequency response of the amplifier without the first stage of the main amplifier ( $g_{m1}$ ) is also simulated, which is labeled as  $GB + g_{m2}$ , showing 16° degradation in the phase margin. It also shows that the first stage transconductance allows the overall amplifier to provide a sufficient gain at the

frequencies higher than 50 kHz. Figure 12 shows the comparison of simulated frequency response among this work, the pseudo single-stage (PSS) amplifier and the design without  $C_m$  using total compensation capacitance of 400-fF. Because the 400-fF compensation capacitance is far from sufficient for the PSS amplifier to implement pole-zero cancellation, its phase margin is degenerated severely.

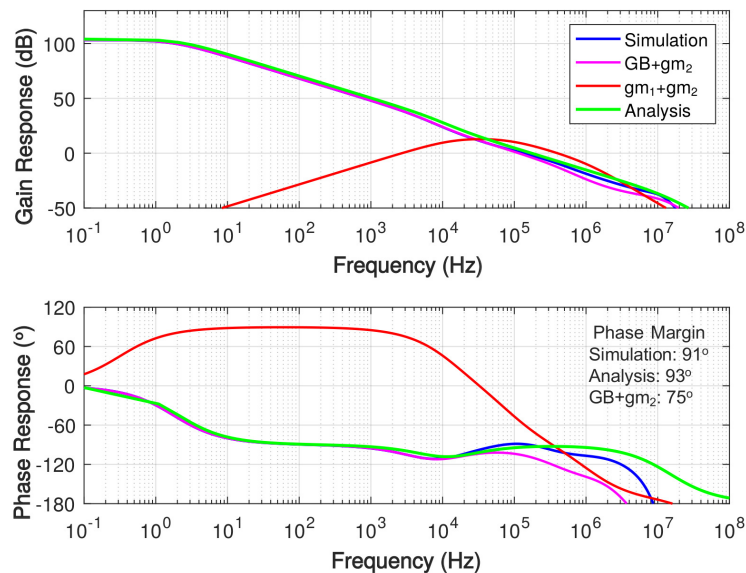


Figure 11. Simulated frequency response of the proposed amplifier with 2.5-nF load capacitance.

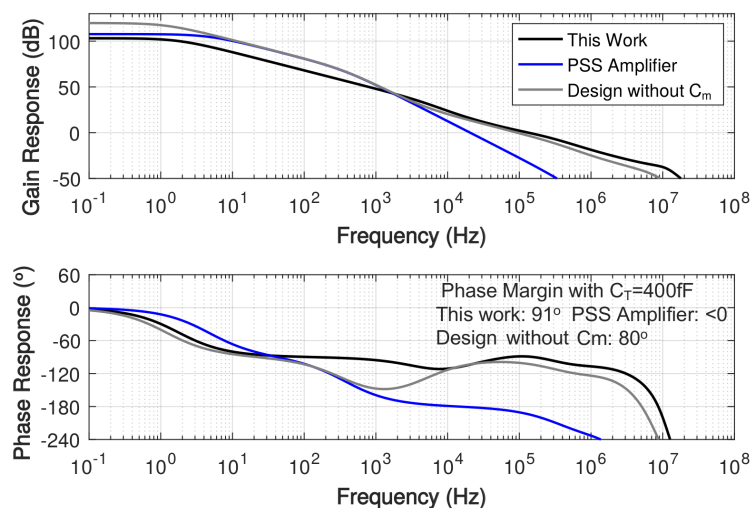
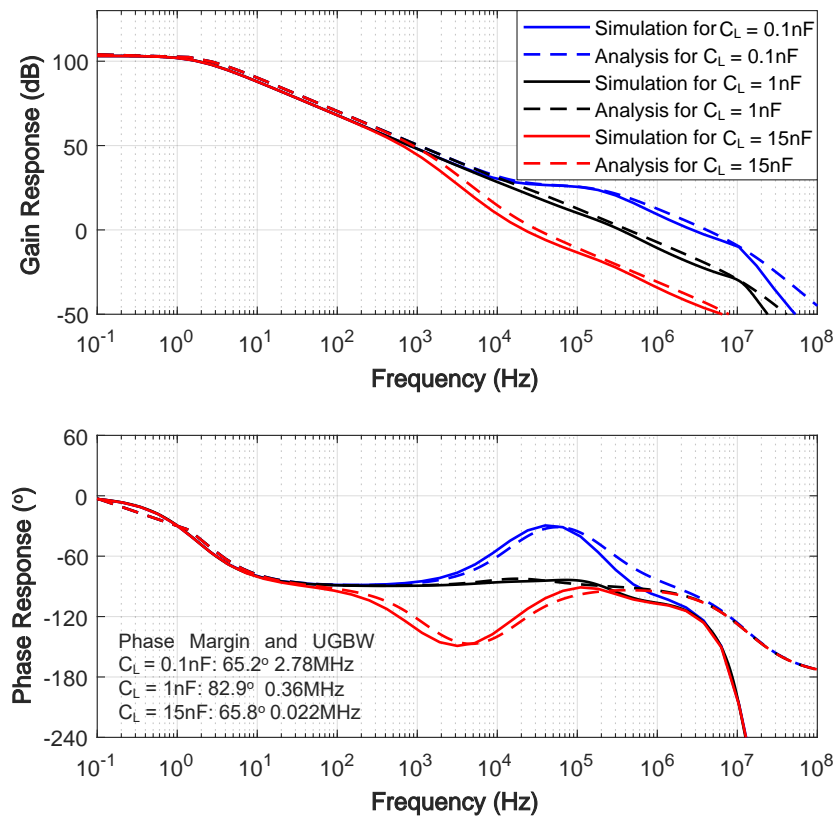


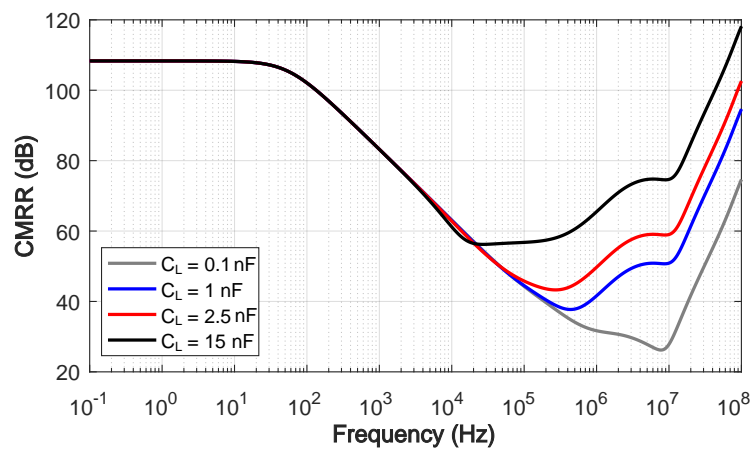
Figure 12. Comparison of simulated frequency response among this work, the PSS amplifier [42] and the design without  $C_m$  with 2.5-nF load capacitance and 400-fF total compensation capacitance.

Figure 13 illustrates the simulated frequency response of the proposed amplifier with 0.1-nF, 1-nF and 15-nF load capacitances, respectively. The precise pole-zero cancellation occurs when load capacitance is 1 nF. The frequency response for 0.1-nF load capacitance shows that the pole of the gain booster,  $\omega_{gz}$  is lower than the output node pole  $\omega_{p1}$ , while  $\omega_{gz}$  is higher than  $\omega_{p1}$  when load capacitance is 15 nF. The broken pole-zero cancellation reflected in Figure 13 accords with the analysis in previous section.



**Figure 13.** Simulated frequency response of the proposed amplifier with 0.1-nF, 1-nF and 15-nF load capacitance.

The simulated common-mode rejection ratio (CMRR) is given in Figure 14, which is 109 dB at DC. At low frequency, the high CMRR is mainly contributed by the first stage of the gain booster, which is a differential composite cascode amplifier, since the first and second stage of the main amplifier are AC coupled by  $C_m$ . With the increase of frequency, the first stage of the main amplifier begins to make a difference to the CMRR. Owing to this, the proposed work obtains a sufficient CMRR at high frequency.



**Figure 14.** Simulated common-mode rejection ratio of the proposed amplifier with 0.1–15-nF load capacitance.

Under a transient simulation setup illustrated in Figure 15, a step response simulation with various load capacitance is shown in Figure 16, and the simulated 1% settling time with variation on Miller compensation capacitor  $C_f$  is shown in Figure 17. The 1% settling time is damaged due to exceeding  $-80^\circ$  phase margin when driving 1–7-nF load capacitance. With the diminution of  $C_f$ , the phase margin decreases, then the 1% settling time is improved.

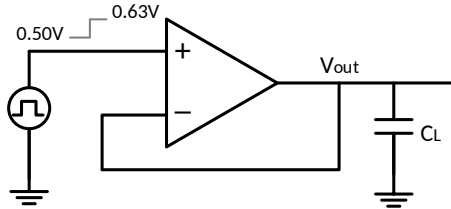


Figure 15. Test-bench circuit for step response simulation.

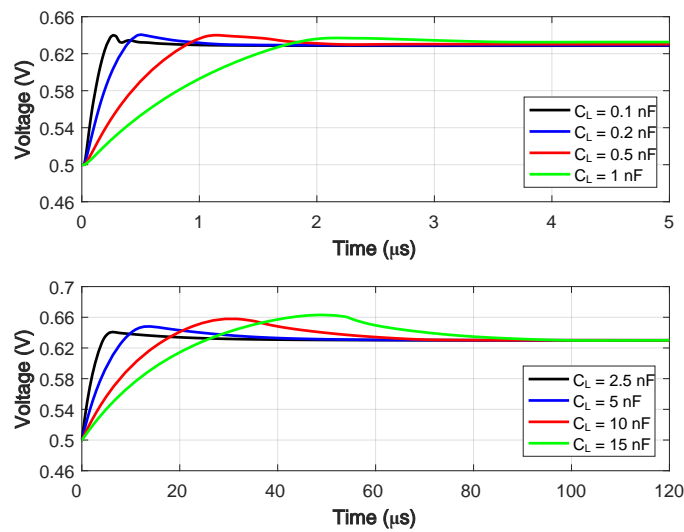


Figure 16. Simulated step response of the proposed amplifier with various load capacitance.

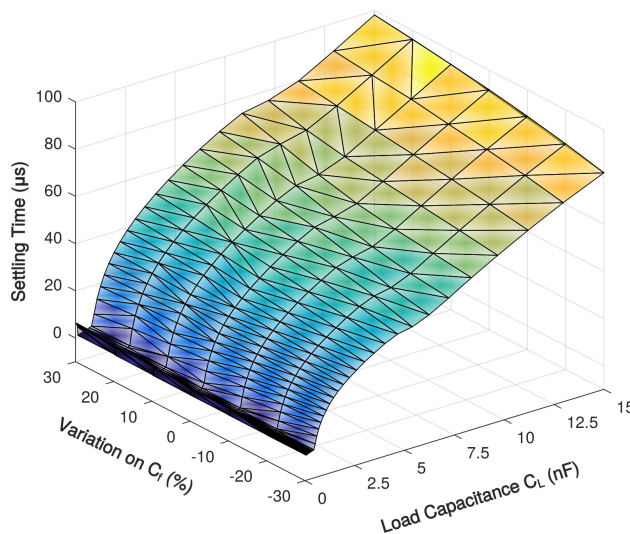


Figure 17. Simulated 1% settling time of the proposed amplifier with 0.1–15-nF load capacitance over Miller compensation capacitor variations.



The input common-mode range (ICMR) and output swing of the proposed amplifier are shown in Figure 18. The input common range is from 0.49 V to 0.64 V, and the output bias voltage swings between 0.34 V and 0.68 V. Considering that the Class-B output stage may cause the distortion of output signal, the simulated total harmonic distortion (THD) with 40-mVpp differential input when load capacitance is 0.1 nF, 1 nF and 15 nF is shown in Figure 19. The largest total harmonic distortion is  $-114$  dB, while the DC voltage gain is 103 dB.

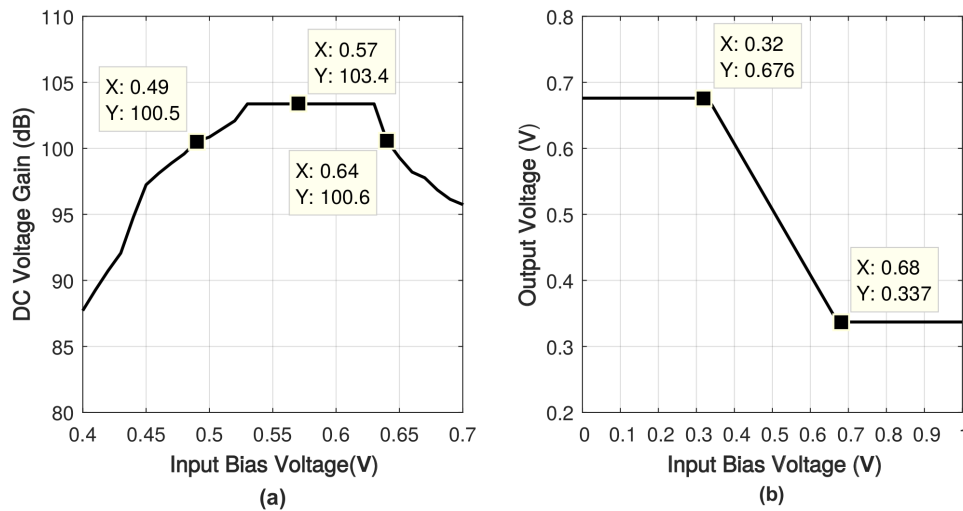


Figure 18. Simulated (a) input common-mode range (b) output swing of the proposed amplifier.

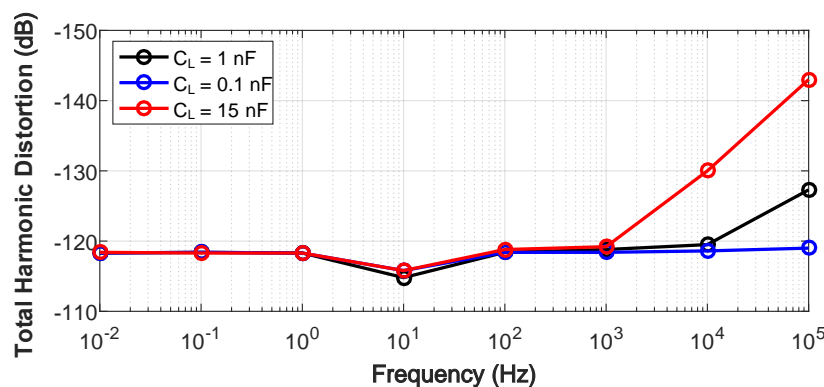
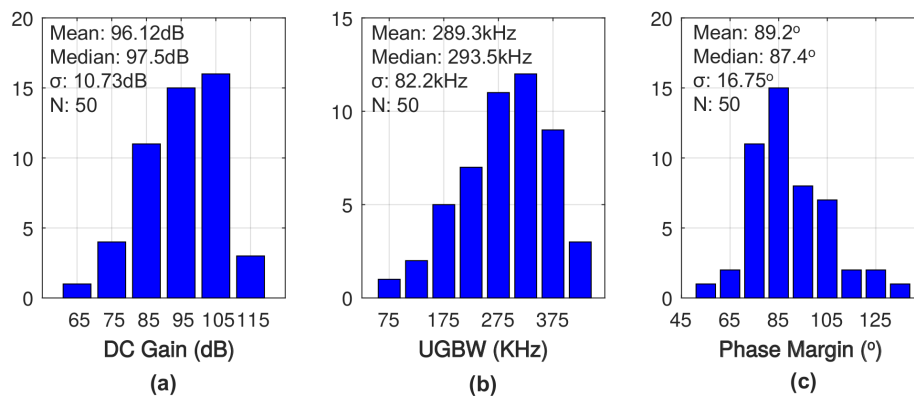


Figure 19. Simulated total harmonic distortion of the proposed amplifier with 0.1-nF, 1-nF and 15-nF load capacitance.

Monte Carlo simulations with 50 samples for DC gain, unity gain bandwidth and phase margin with 1-nF load capacitance are shown in Figure 20. The median performance of 97.5-dB gain, 293.5-kHz unity gain frequency, and  $87.4^\circ$  phase margin is obtained with a standard deviation of 10.7 dB, 82.2 kHz, and  $16.8^\circ$ . Considering the limited number of samples, the median performance of the Monte Carlo simulation well matches the simulation results with typical case model. Figure 20c shows that the prototype remains stable with  $2\sigma$  variation. In addition, the corner simulation performed with one  $\sigma$  process variation presents 110.3-dB gain, 329.9-kHz unity gain bandwidth and  $82^\circ$  phase margin at high side and 95.5-dB gain, 227.3-kHz unity gain bandwidth and  $93^\circ$  phase margin at low side, which also matches the statistical distributions from the Monte Carlo simulation.

Table 6 compares the simulated performance of the prototype design with the state-of-the-art. Compared to previous works, this work utilizes the smallest compensation capacitance, which is 400 fF, and demonstrates the highest ratio between load capacitance and total compensation capacitance,

which is 37,500. In addition, it also presents the best reported performance trade-off on the unity gain bandwidth, load capacitance, and power consumption for a given chip area, as shown in Figure 21.



**Figure 20.** Monte Carlo simulation for (a) DC voltage gain (b) unity gain bandwidth and (c) phase margin of the proposed amplifier with 1-nF load capacitance.

**Table 6.** Performance summary and Figure-of-Merit (FoM) comparison.

	[38]	[39]	[40]	[41]	[42]	[43]	This work		
Load Capacitance $C_L$ (nF)	0.15	0.5	0.5	1	1.5	1.5	0.1	1	15
$C_{L,max}/C_{L,min}$	N/A	1.6	N/A	15	150	12	150		
Gain (dB)	>100	>100	>100	>100	≈100	>100	103		
Phase Margin (°)	58	70	52	83	87	75	65	83	66
Gain Margin (dB)	22	N/A	8	10	35	N/A	11	28	51
UGBW(MHz)	2.85	4	2	1.37	0.12	3.46	2.78	0.36	0.022
Slew Rate (V/μs)	1.03	2.2	0.65	0.59	5.87	1.46	0.78	0.083	0.006
1% Settling Time (μs)	2.25	0.6	1.23	1.28	4.3	0.57	0.82	11.72	91.82
Power (μW)	45	260	20.4	144	7.4	69.6	7.6		
$V_{DD}$ (V)	1.5	2	1.2	2	1.1	1.2	1		
Technology (nm)	350	350	65	350	180	180	130		
Chip Area (mm <sup>2</sup> )	0.02	0.014	0.0088	0.016	0.0021	0.013	0.00096		
Total Compensation Capacitance $C_T$ (pF)	2.02	2.20	1.15	2.64	1.23	1.52	0.40		
$C_L/C_T$	74	227	435	378	1220	987	250	2500	37,500
$FoM_L$ ( $(V/\mu s \cdot pF)/\mu W$ )	3.5	4.2	15.9	4.1	1190	31.5	10.3	10.9	11.8
$FoM_S$ ( $(MHz \cdot pF)/\mu W$ )	9.5	7.7	49.0	9.5	24.3	74.5	36.6	47.3	43.4
LC- $FoM_L$ ( $(V/\mu s)/\mu W$ )	1.7	1.9	13.8	1.5	967.5	20.7	25.8	27.3	29.5
LC- $FoM_S$ ( $MHz/\mu W$ )	4.7	3.5	42.6	3.6	19.8	48.7	91.5	118.3	108.5
$FoM_1$ ( $(V/\mu s \cdot pF)/\mu W/mm^2$ )	175	300	1806	256	566,602	2423	11,453	12,110	13,110
$FoM_2$ ( $(MHz \cdot pF)/\mu W/mm^2$ )	475	550	5568	594	11,583	5730	40,667	52,555	48,221

$FoM_L = (SlewRate \cdot C_L)/Power$   $FoM_S = (UGBW \cdot C_L)/Power$  [37]. LC- $FoM_L = (SlewRate \cdot C_L)/(Power \cdot C_T)$   
 LC- $FoM_S = (UGBW \cdot C_L)/(Power \cdot C_T)$  [41].  $FoM_1 = (SlewRate \cdot C_L)/(Power \cdot ChipArea)$   $FoM_2 =$   
 $(UGBW \cdot C_L)/(Power \cdot ChipArea)$  [51].

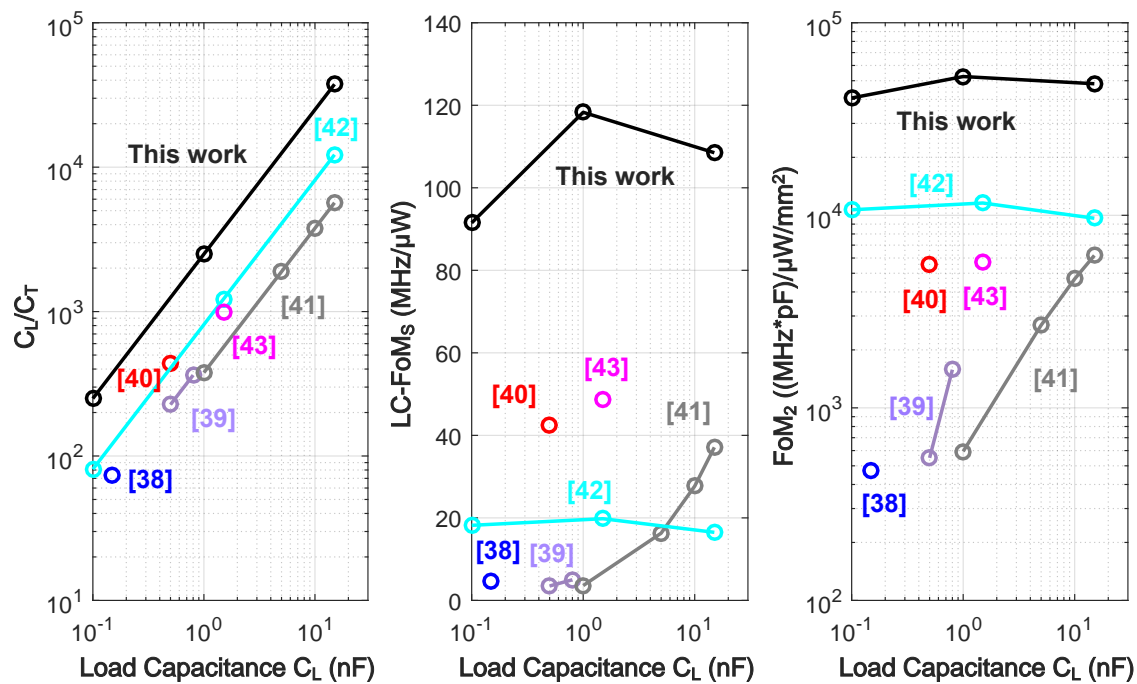


Figure 21. Benchmark of  $C_L/C_T$ , LC-FoM<sub>s</sub> and FoM<sub>2</sub> [38–43].

## 6. Conclusions

Transducers with nonlinear capacitive input impedance need an operational amplifier, which is stable for a wide range of load capacitance. Such an operational amplifier in a conventional design requires a large area for compensation capacitors, increasing costs and limiting applications. In order to address this problem, we present a gain-boosted two-stage operational amplifier, whose frequency response compensation is less sensitive to the load capacitance compared to the conventional Miller frequency compensation. The proposed amplifier cancels the output node pole of the main amplifier stage by the zero of the gain booster, so that a sufficient phase margin can be achieved without using a large compensation capacitor. A prototype CMOS amplifier designed with the proposed architecture uses two-to-four orders of magnitude smaller compensation capacitor compared to the load capacitance. This advantage in the compensation capacitor area requirement extends the applications of the proposed operational amplifier beyond the transducer interface circuits and may benefit general analog integrated circuit applications. The prototype CMOS operational amplifier demonstrates the highest performance trade-off to date when considering unity-gain bandwidth, load capacitance, power consumption, and chip area, which can enable an a compact low-cost transducer interface with unprecedentedly high resolution for emerging applications. It should be also noted that the proposed operational amplifier design technique can be used not only with monolithically integrated transducer interface circuits but also with transducer interface circuits assembled by discrete off-the-shelf components.

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**Author Contributions:** Z.Y. refined the initial circuit topology, designed the prototype, performed the simulations, analyzed the data, and wrote the paper; S.C. conceived the topology and wrote the paper; X.Y. reviewed the prototype design and provided technical advice on the simulations and writing.

**Conflicts of Interest:** The authors declare no conflict of interest.

## Abbreviations

The following abbreviations are used in this manuscript:

AC	Alternating Current
CMOS	Complementary Metal-Oxide-Semiconductor
CMRR	Common-Mode Rejection Ratio
FoM	Figure-of-Merit
DC	Direct Current
ICMR	Input Common-Mode Range
PM	Phase Margin
PSS	Pseudo-Single Stage
UGBW	Unity Gain Bandwidth

## Appendix A

The bias circuit implemented in this work is illustrated in Figure A1 and Table A1.  $I_1$  is the supply independent biasing current, which is 50 nA when  $V_{DD}$  is 1 V.

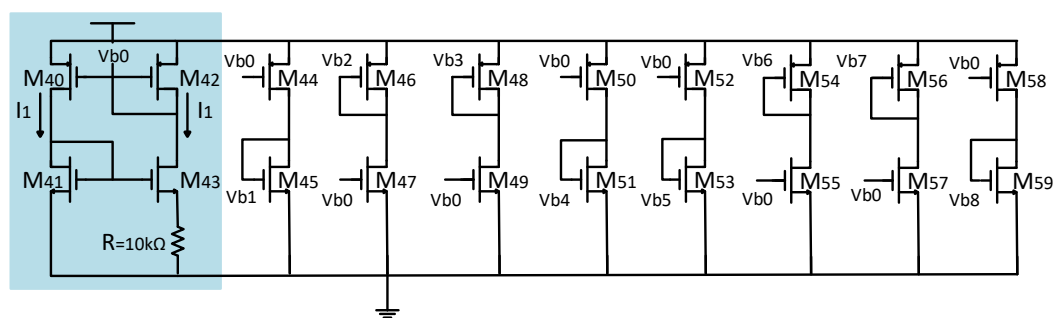


Figure A1. Bias circuit for the proposed work.

Table A1. Transistors size of the bias circuit.

Device	Size ( $\mu\text{m}/\mu\text{m}$ )	Device	Size ( $\mu\text{m}/\mu\text{m}$ )	Device	Size ( $\mu\text{m}/\mu\text{m}$ )
M <sub>40</sub> , M <sub>42</sub>	0.13/3.47	M <sub>41</sub>	0.13/12.54	M <sub>43</sub>	0.13/11.82
M <sub>44</sub>	0.13/3.47	M <sub>45</sub>	1.0/0.34	M <sub>46</sub>	0.13/0.71
M <sub>47</sub> , M <sub>49</sub>	0.13/12.54	M <sub>48</sub>	0.13/0.53	M <sub>50</sub>	0.13/3.47
M <sub>51</sub>	0.13/0.41	M <sub>52</sub>	0.13/3.47	M <sub>53</sub>	0.8/0.34
M <sub>54</sub>	0.13/0.53	M <sub>55</sub>	0.13/12.54	M <sub>56</sub>	0.13/0.24
M <sub>57</sub>	0.13/12.54	M <sub>58</sub>	0.13/3.47	M <sub>59</sub>	0.13/0.53

## References

- Islam, S.M.R.; Kwak, D.; Kabir, M.H.; Hossain, M.; Kwak, K.S. The Internet of Things for health care: A comprehensive survey. *IEEE Access* **2015**, *3*, 678–708.
- Kortuem, G.; Kawsar, F.; Sundramoorthy, V.; Fitton, D. Smart objects as building blocks for the Internet of things. *IEEE Internet Comput.* **2009**, *14*, 44–51.
- Lee, H.; Choi, J. A compact all-textile on-body SIW antenna for IoT applications. In Proceedings of the 2014 International Conference on Intelligent Computing Applications, San Diego, CA, USA, 9–14 July 2017; pp. 825–826.
- Tseng, C.-W.; Chen, T.-C.; Huang, C.-H. Integrating transducer capability to GS1 EPCglobal identify layer for IoT applications. *IEEE Sens. J.* **2015**, *15*, 5404–5415.
- Chew, Z.J.; Ruan, T.; Zhu, M.; Bafleur, M.; Dilhac, J.M. Single piezoelectric transducer as strain sensor and energy harvester using time-multiplexing operation. *IEEE Trans. Ind. Electron.* **2017**, *64*, 9646–9656.

6. Vikulin, I.; Gorbachev, V.; Gorbacheva, A.; Krasova, V.; Polakov, S. Economical transducers of environmental parameters to a frequency for the end devices of IoT. In Proceedings of the 2017 2nd International Conference on Advanced Information and Communication Technologies, Lviv, Ukraine, 4–7 July 2017; pp. 35–40.
7. Khyam, M.O.; Alam, M.J.; Lambert, A.J.; Garratt, M.A.; Pickering, M.R. High-precision OFDM-based multiple ultrasonic transducer positioning using a robust optimization approach. *IEEE Sens. J.* **2016**, *16*, 5325–5336.
8. Wang, N.; Zhang, Z.; Li, Z.; He, Q.; Lin, F.; Lu, Y. Design and characterization of a low-cost self-oscillating fluxgate transducer for precision measurement of high-current. *IEEE Sens. J.* **2016**, *9*, 2971–2981.
9. Yang, X.; Lee, H.-S. Design of a 4th-order multi-stage feedforward operational amplifier for continuous-time bandpass delta sigma modulators. In Proceedings of the 2016 IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, Canada, 22–25 May 2016; pp. 1058–1061.
10. Chung, S.; Abediasl, H.; Hashemi, H. A monolithically integrated large-scale optical phased array in silicon-on-insulator CMOS. *IEEE J. Solid-State Circuits* **2018**, *53*, 275–296.
11. Ergun, A.S.; Hung, Y.; Zhuang, X.; Oralkan, O.; Yarlioglu, G.G.; Khuri-Yakub, B.T. Capacitive micromachined ultrasonic transducers: Fabrication technology. *IEEE Trans. Ultrason. Ferroelect. Freq. Control* **2005**, *52*, 2242–2258.
12. Boulme, A.; Ngo, S.; Zhuang, X.; Minonzio, J.G.; Legros, M.; Talmant, M.; Laugier, P.; Certon, D. A capacitive micromachined ultrasonic transducer probe for assessment of cortical bone. *IEEE Trans. Ultrason. Ferroelect. Freq. Control* **2014**, *61*, 710–723.
13. Kim, D.; Kuntzman, M.; Hall, N. A rotational capacitive micromachined ultrasonic transducer (RCMUT) with an internally-sealed pivot. *IEEE Trans. Ultrason. Ferroelect. Freq. Control* **2014**, *61*, 1545–1551.
14. Okano, T.; Izumi, S.; Katsuura, T.; Kawaguchi, H.; Yoshimoto, M. Multimodal cardiovascular information monitor using piezoelectric transducers for wearable healthcare. In Proceedings of the 2017 IEEE International Workshop on Signal Processing Systems, Lorient, France, 3–5 October 2017.
15. Coskun, M.B.; Fowler, A.G.; Maroufi, M.; Moheimani, S.O.R. On-chip feedthrough cancellation methods for microfabricated AFM cantilevers with integrated piezoelectric transducers. *J. Microelectromech. Syst.* **2017**, *26*, 1287–1297.
16. Cummins, G.; Gao, J.; McPhillips, R.; Watson, D.; Desmulliez, M.P.Y.; McPhillips, R.; Cochran, S. Optimization and characterisation of bonding of piezoelectric transducers using anisotropic conductive adhesive. In Proceedings of the 2017 IEEE International Ultrasonics Symposium, Washington, DC, USA, 6–9 September 2017.
17. Chi, Y. M.; Jung, T.-P.; Cauwenberghs, G. Dry-contact and noncontact biopotential electrodes: Methodological review. *IEEE Rev. Biomed. Eng.* **2010**, *3*, 106–119.
18. Williams, I.; Constandinou, T. G. An energy-efficient, dynamic voltage scaling neural stimulator for a proprioceptive prosthesis. *IEEE Trans. Biomed. Circuits Syst.* **2013**, *7*, 129–139.
19. Rattay, F. Analysis of models for extracellular fiber stimulation. *IEEE Trans. Biomed. Eng.* **1989**, *37*, 676–682.
20. Merrill, D.R.; Bikson, M.; Jefferys, J.G.R. Electrical stimulation of excitable tissue—Design of efficacious and safe protocols. *J. Neurosci. Methods* **2005**, *141*, 171–198.
21. Van Dongen, M.; Serdijn, W. *Design of Efficient and Safe Neural Stimulators*; Springer: Cham, Switzerland, 2016.
22. Yip, M.; Jin, R.; Nakajima, H. H.; Stankovic, K. M.; Chandrakasan, A. P. A fully-implantable cochlear implant SoC With piezoelectric middle-ear sensor and arbitrary waveform neural stimulation. *IEEE J. Solid-State Circuits* **2015**, *50*, 214–229.
23. Chen, K.; Lee, H.-S.; Chandrakasan, A.P.; Sodini, C.G. Ultrasonic imaging transceiver design for CMUT: A three-level 30-V<sub>pp</sub> pulse-shaping pulser With improved efficiency and a noise-optimized receiver. *IEEE J. Solid-State Circuits* **2013**, *48*, 2734–2745.
24. Ha, S.; Akinin, A.; Park, J.; Kim, C.; Wang, H.; Maier, C.; Mercier, P. P.; Cauwenberghs, G. Silicon-Integrated High-Density ElectroCortical Interfaces. *Proc. IEEE* **2017**, *105*, 11–33.
25. Gray, P.R.; Meyer, R.G. MOS operational amplifier design—a tutorial overview. *IEEE J. Solid-State Circuits* **1982**, *17*, 969–982.
26. Ahuja, B.K. An improved frequency compensation technique for CMOS operational amplifiers. *IEEE J. Solid-State Circuits* **1983**, *18*, 629–633.

27. Sansen, W.; Chang, Y.Z. Feedforward compensation techniques for high-frequency CMOS amplifiers. *IEEE J. Solid-State Circuits* **1990**, *25*, 1590–1595.
28. Saxena, V.; Baker, R.J. Indirect compensation techniques for three-stage fully-differential op-amps. In Proceedings of the 2010 53rd IEEE International Midwest Symposium on Circuits and Systems, Seattle, WA, USA, 1–4 August 2010; pp. 588–591.
29. Eschauzier, R.G.H.; Kerklaan, L.P.T.; Huijsing, J.H. A 100-MHz 100-dB operational amplifier with multipath nested Miller compensation structure. *IEEE J. Solid-State Circuits* **1992**, *27*, 1709–1717.
30. Palmisano, G.; Palumbo, G. A compensation strategy for two-stage CMOS op amps based on current buffer. *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.* **1997**, *44*, 257–262.
31. Palumbo, G.; Pennisi, S. Design methodology and advances in nested-Miller compensation. *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.* **2002**, *49*, 893–903.
32. Leung, K.N.; Mok, P.K.T.; Ki, W.-H. Three-stage large capacitive load amplifier with damping-factor-control frequency compensation. *IEEE J. Solid-State Circuits* **2000**, *35*, 221–230.
33. Leung, K.N.; Mok, P.K.T. Analysis of multistage amplifier-frequency compensation. *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.* **2001**, *48*, 1041–1056.
34. Peng, X.; Sansen, W. Nested feed-forward G<sub>m</sub>-stage and nulling resistor plus nested-Miller compensation for multistage amplifiers. In Proceedings of the IEEE 2002 Custom Integrated Circuits Conference, Orlando, FL, USA, 15 May 2002; pp. 329–332.
35. Peng, X.; Sansen, W. AC boosting compensation scheme for low-power multistage amplifiers. *IEEE J. Solid-State Circuits* **2004**, *39*, 2074–2079.
36. Grasso, A.D.; Palumbo, G.; Pennisi, S. Advances in reversed nested Miller compensation. *IEEE Trans. Circuits Syst. I* **2007**, *54*, 1459–1470.
37. Peng, X.; Sansen, W.; Hou, L.; Wang, J.; Wu, W. Impedance adapting compensation for low-power multistage amplifiers. *IEEE J. Solid-State Circuits* **2004**, *46*, 445–451.
38. Peng, X.; Sansen, W. Transconductance with capacitances feedback compensation for multistage amplifiers. *IEEE J. Solid-State Circuits* **2005**, *40*, 1514–1520.
39. Guo, S.; Lee, H. Dual active-capacitive-feedback compensation for low-Power large-capacitive-load three-stage amplifiers. *IEEE J. Solid-State Circuits* **2011**, *46*, 452–464.
40. Chong, S.; Chan, P. Cross feed forward cascode compensation for low-power three-stage amplifier with large capacitive load. *IEEE J. Solid-State Circuits* **2012**, *47*, 2227–2234.
41. Yan, Z.; Mak, P.; Law, M.; Martins, R. A 0.016-mm<sup>2</sup> 144-μW three-stage amplifier capable of driving 1-to-15 nF capacitive load with > 0.95-MHz GBW. *IEEE J. Solid-State Circuits* **2013**, *48*, 527–540.
42. Hong, S.W.; Cho, G.H. A pseudo single-stage amplifier with an adaptively varied medium impedance node for ultra-high slew rate and wide-range capacitive-load drivability. *IEEE Trans. Circuits Syst. I* **2016**, *63*, 1567–1578.
43. Qu, W.; Singh, S.; Lee, Y.; Son, Y.S.; Cho, G.H. Design-oriented analysis for miller compensation and its application to multistage amplifier design. *IEEE J. Solid-State Circuits* **2017**, *52*, 517–527.
44. Black, W.C.; Allstot, D.J.; Reed, R.A. A high performance low power CMOS channel filter. *IEEE J. Solid-State Circuits* **1980**, *15*, 929–938.
45. Dasgupta, U. Issues in ‘Ahuja’ frequency compensation technique. In Proceedings of the 2009 IEEE International Symposium on Radio-Frequency Integration Technology, Singapore, 9–11 December 2009; pp. 326–329.
46. Gray, P.; Meyer, R. Recent advances in monolithic operational amplifier design. *IEEE Trans. Circuits Syst.* **1974**, *21*, 317–327.
47. Apfel, R.J.; Gray, P. A fast-settling monolithic operational amplifier using doublet compression techniques. *IEEE J. Solid-State Circuits* **1974**, *9*, 332–340.
48. Comer, D.J.; Comer, D.T.; Singh, R.P. A high-gain, low-power CMOS op amp using composite cascode stages. In Proceedings of the IEEE International Midwest Symposium on Circuits and Systems, Seattle, WA, USA, 1–4 August 2010; pp. 600–603.
49. Comer, D.J.; Comer, D.T.; Petrie, C.S. The utility of the active cascode in analog CMOS design. *Int. J. Electron.* **2004**, *91*, 491–502.

50. Tajalli, A.; Lelebici, Y.; Brauer, E.J. Implementing ultra-high-value floating tunable CMOS resistors. *Electron. Lett.* **2008**, *44*, 349–350.
51. Yan, Z.; Mak, M.K.; Law, M.K.; Martins, R.P.; Maloberti, F. Nested-current-mirror rail-to-rail-output single-stage amplifier with the enhancements of DC gain, GBW and slew rate. *IEEE J. Solid-State Circuits* **2015**, *50*, 2353–2366.



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