Multi-Source Energy Harvesting for Lightweight Applications

by

Alexander Oliva

S.B., Massachusetts Institute of Technology (2016)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Master of Engineering in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 2018

Author .....
Department of Electrical Engineering and Computer Science
December 21, 2017

Certified by .....
Jeffrey H. Lang
Professor of Electrical Engineering
Thesis Supervisor

Certified by .....
Paul A. Ward
Charles Stark Draper Laboratory
Thesis Supervisor

Accepted by .....
Christopher J. Terman
Chairman, Master of Engineering Thesis Committee

Multi-Source Energy Harvesting for Lightweight Applications

by

Alexander Oliva

Submitted to the Department of Electrical Engineering and Computer Science
on December 21, 2017, in partial fulfillment of the
requirements for the degree of
Master of Engineering in Electrical Engineering and Computer Science

Abstract

This thesis analyzes, designs and tests circuit topologies for simultaneous energy harvesting from solar and 915-MHz RF energy sources. An important design objective is to minimize system weight while maximizing output power and operating time for applications in the sub-170-mg and single-mW ranges. The resulting energy harvesting system uses a unique approach of categorizing the harvesters as primary and auxiliary harvesters due to the power levels of each in relation to the high load demand. This work results in a 162-mg supercapacitor-powered system capable of powering a 2-V load at up to approximately 2-3 mW and a 150-mg battery-powered system capable of powering a 2-V load at up to 6 mW. The auxiliary RF harvester uses a fully-integrated charge pump to impedance-match to a rectenna with greater than 94% matching. The parasitic models developed for the RF harvester show errors less than 1.4% in the measured system.

Thesis Supervisor: Jeffrey H. Lang
Title: Professor of Electrical Engineering

Thesis Supervisor: Paul A. Ward
Title: Charles Stark Draper Laboratory

Acknowledgments

This thesis work would not have been possible without the help of several people along the way.

Chris Salthouse provided great mentoring in the first half of this thesis work, providing me with the resources and advice that I needed to succeed.

Paul Ward was a valuable resource for the second half of my master's studies and was very eager to help review my work and offer suggestions for improvement.

The DragonflEye Team at Draper was a wonderful group to work with, full of intelligent and inspiring people striving to do great research. Joe Register and Jesse Wheeler were excellent leaders that kept the project moving forward.

Draper in general provided excellent resources, organized many helpful events among the Draper Fellows, and is the reason I was able to work on such an interesting and multifaceted project.

Elliot Greenwald's assistance in ASIC design was invaluable. I would have never been able to complete several important aspects of my research without his patience and guidance.

Prof. Jeffrey H. Lang was an excellent mentor, providing support and advice in all areas of this research project. He has been an incredible and inspiring advisor over the past 16 months. I am truly thankful for his support, ideas, and suggestions throughout this work.

Lastly, to all my family and friends, thank you for all your support over the last year and a half. Completing graduate school goes far beyond developing technical skills, and you made it possible and enjoyable.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Background and Motivation

Powering systems from batteries comes with the challenges of battery replacement, battery weight, and proper battery disposal. Recent efforts in ambient energy harvesting and wireless power transfer have opened the opportunity to replace single-use batteries with long-lasting solar, RF, vibration, and thermal energy harvesters. However, even energy harvesters can sometimes suffer from heavy weight when using larger rechargeable batteries or supercapacitors. Weight minimization is particularly important in certain systems, such as in robotic aerial vehicles, wearable electronics, and medical devices.

Another application of lightweight electronics is in neural recorders and optogenetic stimulators for use in insects and other small animals. By studying organisms during free behavior, researchers are able to understand and even manipulate organisms' neural systems. Such efforts have improved insect tracking systems for environmental studies and neural stimulators for controlling insect movement. The latter even allows for opportunities such as exploring areas unfit for humans (e.g. small spaces, disaster areas).

When using electronic circuits to wirelessly study animals, the animals must be able to support the weight of the measurement system. With a growing interest in studying smaller, flying insects, electronics are required to decrease in size, weight, and

consequently power consumption. Therefore, the ability to provide higher quantities of information and higher accuracy is limited to keep output power low enough such that batteries can power the system for a usable amount of time. Many systems use an ambient energy harvesting or wireless power transfer approach in order to power systems endlessly without the need to replace batteries. However, the harvested energy can be very low, still placing restrictions on output power. Combining energy harvesters for various energy sources can often be done, but this increases the weight and complexity of the design. This thesis proposes and investigates methods to minimize system weight while maximizing output power and operating time for a specific dragonfly measurement and optogenetic stimulation system by combining solar and RF energy in a power harvesting and management circuit.

The purpose and unique challenge of this design is to create an incredibly lightweight system capable of running sensors and stimulators at the milliwatt level. The project studies various energy storage methods to allow system operation during moments without ambient or transferred energy. It also examines circuit methods to minimize weight, such as using fully-integrated switching converters, using inductor-less voltage regulators, and reusing discrete inductors. This thesis aims to create a sub-170-mg system capable of powering a 2-V load in the 1-10 mW range using a multi-source solar and RF energy harvester. This is completed for the benefit of and use in the DragonflEye project at the Charles Stark Draper Laboratory in Cambridge, MA.

1.2 Literature Review

Much work has already been done in the realm of energy harvesting. This section summarizes findings in previous animal neural recording and stimulation systems, harvester weights, solar and RF harvester methods, and multi-source harvesting. It also discusses how this thesis builds on these findings.

1.2.1 Weight Analysis of Previous Works

Table 1.1 shows a list of previous wireless recording and stimulation systems developed for use on various land and air animals. Many of the systems used on aerial insects were used on moths [14, 31, 41, 55, 56]. This is likely due to the fact that moths are relatively large flying insects and are therefore more likely to support a higher electronic payload. In fact, the lightest of the moth-oriented systems was 400 mg. Of all the systems shown, the lightest weighed 170 mg, where 76% of the weight consisted of the battery [26]. Both [26] and [44] used a 130-mg silver oxide 337 battery, the lightest of all the batteries in Table 1.1. By replacing the battery with an energy harvester and reusable energy storage element capable of providing the 1 mW of output power needed, the system weight in [26] could have been greatly reduced. While this particular system was successfully demonstrated on a dragonfly, the heavy weight could very well have fatigued the dragonfly, affecting its behavior and resultant neural recordings. Hence, this thesis and the DragonflEye project aim to create a system less than 170 mg, resulting in a system lighter than that of [26].

Table 1.2 shows a comparison of various energy harvesters for various energy sources. Figure 1-1 plots the data of both tables along with the goal of this thesis project. Blue circles and the blue line represent power that can be input to power management circuitry from energy harvesters in Table 1.2; orange asterisks represent power consumed by the systems in Table 1.1, power that must be output from power management circuitry; the green star represents the estimated power consumption and an example weight of the DragonflEye optogenetic stimulator and approximately what is estimated for the lightest system developed in Chapter 3. Figure 1-1 illustrates how this thesis works to develop a system that is lighter than current systems and capable of outputting power above most. This is essential for increasing data rates, improving sensors, and allowing more complex stimulators. Harvesters in [22] and in [27], the latter of which is discussed in terms of specific power, fall within the goal's weight limit, but the solar harvester in [32] can also scale down within this weight limit by using smaller cells. However, only the solar power harvested in [27]

Table 1.1: Comparison of previously developed wireless recording and stimulation systems for various animals.

Work	**Power Consumed (mW)**	**Area (mm x mm)**	**Total Mass (mg)**	**Battery Life (min)**	**Battery Weight (mg)**	**Animal**	**Purpose**	**Year**
Kuwana [31]	-	12 x 7	400	30	-	Moth	Record	1999
Mohseni [41]	2	10 x 10	740	180	230	Moth	Record	2001
Mohseni [42]	2.2	17 x 12	1100	-	-	Marmoset	Record	2005
Yeager [56]	0.036	22 x 17	1600	NA*	0	Moth	Record	2009
Tsang [55]	2.6†	6.8 x 10.2	461.7	180	250.8	Moth	Stimulate	2010
Daly [14]	2.5	15 x 26	1000	972†	320	Moth	Stimulate	2010
Harrison [26]	1	6 x 5	170	300	130	Locust; Dragonfly	Record	2011
Fan [20]	22.5†	16 x 17	4500	360	-	Mouse	Record	2011
Morrison [44]	1.07	2 x 2	522	1320	130	Human	Record	2012
Mann [37]	3†	100 mm^2	280	4	-	Locust	Stimulate	2014

* energy transferred wirelessly through RF

† estimated/calculated from provided data

Table 1.2: Comparison of previously developed energy harvesters.

Work	**Energy Harvester**	**Harvester Power (μW)**	**Harvested From**	**Weight (mg)**	**Area (mm^2)**	**Year**
Law [32]	Thin GaInP/GaInAs/Ge Triple-Junction Solar Cell	500,000	AM0 Solar Energy	240	50	2006
Jean [27]	Vapor-Deposited Parylene Substrate, Organic Solar Cell	6 $^{mW}/_{mg}$	AM0 Solar Energy	-	278 $^{mm^2}/_{mg}$	2015
Ghafouri [22]	Thermoelectric Generator with Bi2Te3/Sb2Te3 Thermocouples	0.8	Beetle's body heat	14	8	2008
Chang [11]	Magnetic-Induction-Based Vibrational Energy	900	*Manduca sexta* moth's wingbeats (25 Hz)	1280	2.85	2009
Aktakka [3]	Non-Resonant Piezoelectric for Vibrational Energy	45	Green June Beetle's wingbeats (85-105 Hz)	200	36	2011
Gudan [23]	2.4-GHz RF Energy	0.0107*	2.4-GHz transmitter	-	100	2014

* at -17.1 dBm; estimated/calculated from provided data

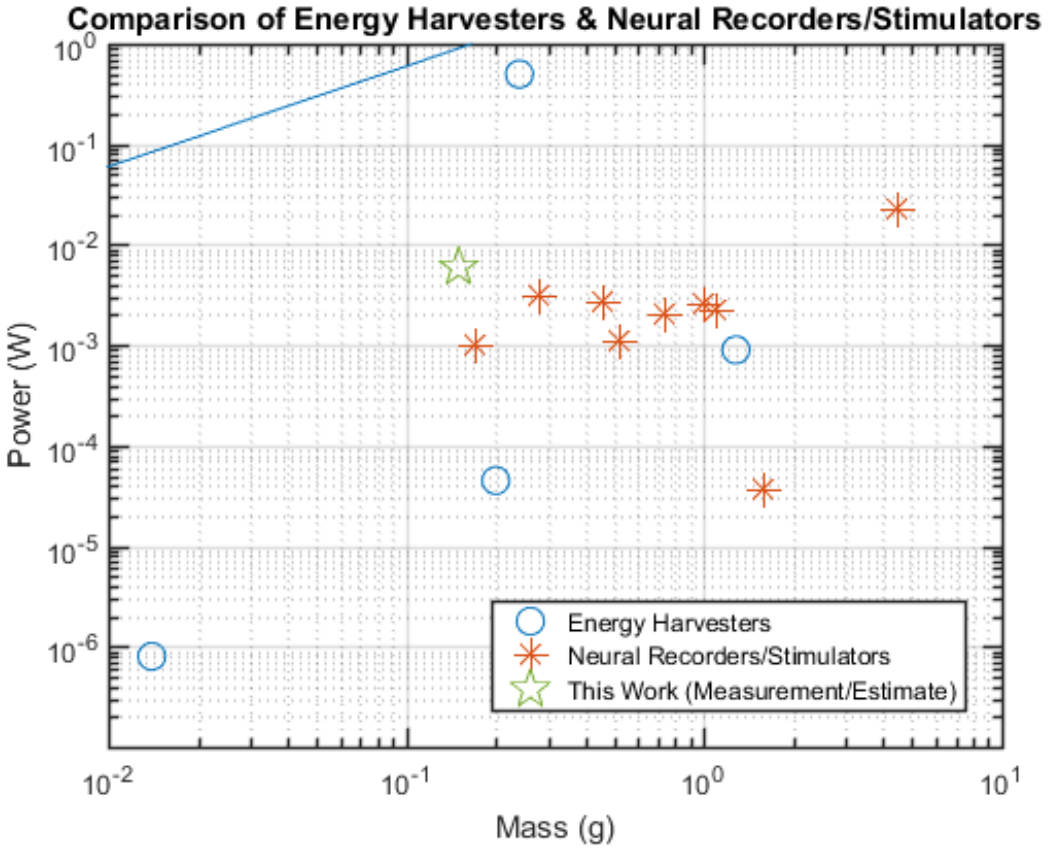


Figure 1-1: Harvested power of various harvesters (blue circles and line), power consumed by various neural recording and stimulation systems (orange asterisks), and goal of this thesis project (green star), vs. mass.

and in [32] is sufficient to meet the power demands of the DragonflEye system. From this, it becomes clear that solar harvesters provide the most power for a reasonable weight for this project. While magnetic-induction-based vibrational energy harvesters can produce power comparable to that of this project (0.9 mW), the weight to do so is beyond that which a dragonfly can handle [11]. Thermoelectric generators have no moving parts, allowing for much lighter construction, but in [22], the devices needed to be implanted during the pupa stage of the beetles' development and also do not produce enough energy to benefit this thesis. The RF energy harvester used in [23] only produces 10.7 nW of harvested power, but its received power was 19.5 μW (-17.1 dBm). The DragonflEYE project will use a 915-MHz, 10-W transmitter a few meters away to perform backscatter communication. The Friis model estimates that half-wave dipole receiving and transmitting antennas between a distance of 1

m and 10 m at this frequency would result in 18.2 mW (12.6 dBm) to 182.0 μW (-7.4 dBm) of received power, respectively. While this an ideal calculation, it does show that significantly more power can likely be received on the wireless DragonflEye system than that received in [23]. While a solar energy harvester will be used in this system because of its power-to-weight ratio, RF energy will also be harvested because a backscattering antenna will already be present on the system. This results in an interesting problem of multi-source power harvesting and management.

1.2.2 Solar Harvesters

An enormous number of maximum power point tracking (MPPT) algorithms for solar cells have been proposed because of their nonlinear current-voltage (I-V) behavior (Figure 1-2) and their dependence on irradiance and temperature [1, 2, 4, 8, 12, 15, 16, 19, 25, 28, 29, 33, 34, 38, 40, 45, 50, 54]. Figure 1-2 illustrates how solar cells must operate at a specific I-V point in order to extract the maximum amount of power possible, which is achieved by MPPT controllers. These algorithms include the perturbation and observation (P&O), incremental conductance (INC), fractional open circuit voltage (FOCV), fractional short circuit current (FSCC), fuzzy logic, and neural network methods. Each has various advantages and disadvantages regarding efficiency, complexity, convergence time, and so on. In this thesis, the desire to minimize die space and power consumption of the control system limits the choice to algorithms that can be performed in a relatively simple manner. This discourages the use of several methods performed using microcontrollers and the use of complex methods such as the neural network method [40], while it encourages the use of simpler digital designs [15]. While limiting power consumption would generally suggest digital control circuitry, constructing analog MPPT circuits at 25-μW power consumption with 99.7% tracking efficiency has been shown to be possible [1]. This leaves a few possible algorithms that meet the stated criteria.

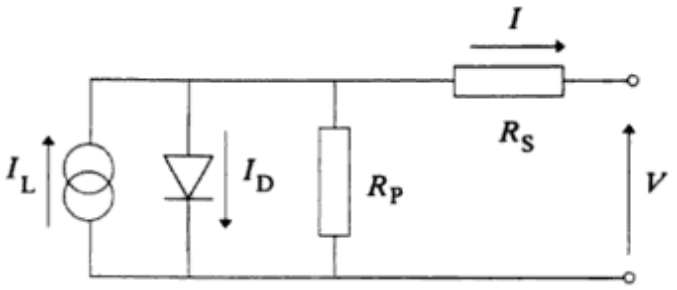
The FOCV method is one of the simplest methods to keep the solar cell operating near the maximum power point (MPP). The FOCV method works by assuming the output voltage at the MPP occurs at a fixed fraction of the open circuit voltage. It

involves periodically disconnecting the solar cell to measure its open circuit voltage followed by long intervals of reconnecting the solar cell to the DC-DC converter. The converter's duty cycle sets the solar cell's loaded voltage to that of the estimated MPP [45]. This method suffers from power loss during the open circuit measurement interval and MPP inaccuracy by assuming a linear relationship between the MPP and the open circuit voltage. However, consistent operating points within 5% of the MPP over various input powers have been reported [54]. In order to respond quickly to changing environmental conditions that move the MPP, the controller must sample the open circuit voltage more frequently, resulting in higher power loss [2]. One advantage of the FOCV method is that it only requires the measurement of the solar cell voltage, greatly simplifying the control system. If properly designed, it also converges quickly under varying weather conditions [45].

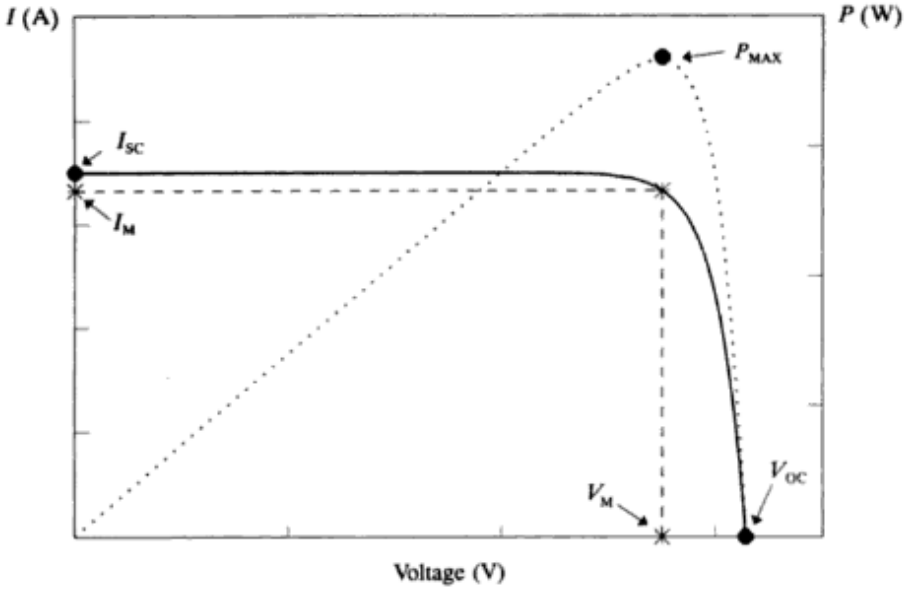
The P&O method measures the solar cell output power, rather than the open circuit voltage of the solar cell. This method constantly changes the DC-DC converter duty cycle to hill-climb up the P-V curve [15]. Once the MPP is found, the controller continues to oscillate around it. This method has experimentally been shown to be the most efficient, as it reliably operates around the MPP [8], and it has the advantage of not needing to disconnect the solar cell from the circuit. However, it has the problem of responding slowly to irradiance level changes and requires measurement of both the output voltage and current.

The INC method follows the slope of the P-V curve up to the MPP by comparing the incremental and instantaneous conductances [50]. Some studies have shown it to have an advantage over the P&O method by responding quickly to changes in irradiance level [8,45], while another study has shown the opposite [19]. This method also tends to be more complex in its implementation [45].

Chapter 3 discusses which MPPT algorithm was chosen for this application based on the performance of the solar cell used.



(a) Typical solar cell circuit model [35].



(b) Typical solar cell current-voltage (I-V) and power-voltage (P-V) curves [35].

Figure 1-2: Solar cell model characteristics.

1.2.3 RF Harvesters

Numerous work has also been completed on harvesting RF energy through antennas. As RF power is received as an AC signal, a rectifier must be used to convert received power to DC. A very simple way to do so is to use a series of diode voltage-doubling rectifiers to both rectify and step up the received voltage. Much work has already been done using this approach, with as many as 7 stages and over frequencies ranging from hundreds of kHz to single GHz [6, 9, 17, 23, 30]. The benefit of such a circuit is it requires little to no control system; diodes simply rectify the signal and step up the voltage based on their nonlinear conduction properties. The challenges of the design is the more diodes that are used, the more losses occur through the non-zero voltage drops of the diodes. The use of low forward-voltage Schottky diodes improves efficiency, but high quality integrated Schottky diodes are not widely available in all integration processes. This requires either a very specific and likely costly integrated circuit process or several heavier discrete components.

Yet another problem rectifiers face is the requirement of impedance matching networks between the antenna and the rectifier for high power transfer with non-optimal loads and to minimize the effects of the power harvester on other uses of the antenna (e.g. backscatter communication). To address this problem, several works have attempted to impedance-match varying loads by inserting a regulator between the rectifier and the load. In the case of inductor-based switching regulators, various buck, boost, and buck-boost circuits have been used to emulate a constant and optimal impedance at the rectifier output [21, 43, 46]. While the high efficiency of inductor-based switching converters and the capability of impedance matching provide excellent results, inductors of usable values are almost always off-chip, adding significant weight to the system. An alternative approach is to use a configurable switched-capacitor charge pump to impedance match to the antenna-rectifier (rectenna) circuit as charge pumps can be fully integrated at high operating frequencies. One attempt attained efficiencies over 80% with this approach [39]. However, the system had a maximum theoretical gain of 6 with 12 capacitors of 150 pF each, occupying a large

area. The system also required a sample-and-hold circuit, periodically disconnected the source from the charge pump, consumed 20 μW of power, and operated with very low input frequencies (less than 500 Hz). As a result, this design would simply not work with the 915-MHz input frequency for the DragonflEye system. This thesis builds on these attempts by designing an impedance-matching charge pump requiring very low-power, simple controls. This charge pump can attain a theoretical ideal gain of 21 with only 6 integrated capacitors.

For this application, an inductor-based RF harvester is highly undesired. Furthermore, avoiding the necessity of integrating high performance Schottky diodes is preferred. Chapter 4 explores a lightweight method of using a discrete rectifier and a fully-integrated charge pump to self-impedance-match to the rectenna.

1.2.4 Multi-Source Harvesters

After deciding upon solar and RF harvester methods, the problem of creating a power management circuit to handle power from two sources still remains. One technique is simply to harvest from various sources each with a different DC-DC switching converter joining to one common filter capacitor on the system [18]. This method has the advantage of allowing independent control of each harvester component and needing only a single energy storage capacitor, but the demonstrated system in [18] requires a space-consuming and heavy inductor for each converter. Another method is to have a single inductor that is shared between various sources [47] and the load [51]. Such a system requires a more complex control algorithm, especially if high transients on the load are possible. Furthermore, energy that enters the entire system must be converted twice: once to store charge onto an intermediary capacitor, and again to remove charge from the intermediary capacitor to power the load. If the intermediary capacitor has a large series resistance, then the efficiency is degraded even further. This limits the maximum amount of output power the system can provide for a given input power. Chapter 2 examines a method of only using a single inductor while avoiding the efficiency losses from storing energy on an intermediary capacitor.

1.3 Overall Summary

Various applications require very lightweight systems, which often come at the cost of reducing system performance to limit power consumption. This thesis proposes and analyzes a system that can provide higher output power at a lower weight than other systems in the field of neural stimulators and recorders. Drawing from previous research, this work uses a well-established MPPT algorithm discussed in future chapters. It also expands on previous work on RF harvesters by developing a new method of harvesting RF energy in a very lightweight manner. The overall power management circuit provides a method of maximizing possible output power without requiring several heavy inductors.

Chapter 2

System Overview

Designing a system to provide high output power while limiting total weight introduces a large number of design trade-offs. This chapter analyzes several different system topologies and how weight, complexity, and efficiency considerations all led to the chosen system architecture of the succeeding chapters.

2.1 Approaches to Harvesting Solar and RF Energy

When attempting to harvest from various sources, two main methods exist: (1) providing each source with a separate electrical harvester [18] and (2) sharing a single electrical harvester between multiple DC or rectified sources [7, 47, 51, 53]. Sharing a harvester usually comes in the form of sharing an inductor. Although inductor sharing reduces weight while allowing each source to be efficiently harvested with a switching converter, it also comes with a few challenges. Firstly, passing an inductor from source to source could cause issues regarding the initial inductor current, potentially requiring zero-crossing detector circuitry to pass an energy-free inductor. Passing an inductor less frequently as in [47] decreases the frequency of having to detect or refresh the inductor current, but the sources are then left unconnected for longer. This could be resolved by having a larger capacitor in parallel with each source, but this may cause a relatively large ripple on the capacitor, another source of losses. Larger capacitors are also typically heavier and are more sensitive to frequency. Secondly,

each harvester could have a different control scheme for harvesting. For example, an FOCV MPPT algorithm for a solar harvester and a matched-impedance algorithm for an RF harvester could operate very differently, complicating a shared-inductor control system.

Alternatively, each source can be provided with a separate harvester, which does not necessarily have to include multiple inductors. While it is commonly known that inductor-based switching regulators are more efficient than switched-capacitor (SC) circuits at high loads, SC charge pumps can be fully integrated. This offers a low-weight approach to energy harvesting. In the case of running a high-power load with both a high-power source and a low-power source, the high-power source must provide the majority of power to the load. In order to maximize output power, it is imperative to have an inductor-based switching regulator for the high-power source (e.g. solar). It is therefore likely acceptable to have a lower efficiency but fully integrated SC charge pump for the low-power source (e.g. RF). Because of the benefits of weight with a slight trade-off of maximum output power, it was determined to use an inductor-based boost converter for the solar harvester and an SC converter for the RF harvester.

2.2 Solar MPPT and Output Voltage Regulation

As the vast majority of power delivered to the load will come from the solar cell, this section examines only the power flow of energy harvested from the solar cell independent of the RF harvester. Because of the nonlinear I-V curve of solar cells as demonstrated in Chapter 1, solar harvesters operating at the MPP with a regulated output traditionally require two converters, one to harvest solar energy at the MPP and another to regulate the stored voltage to a fixed output [24, 48]. This is because a single canonical switching converter cannot both extract maximum power from the input and regulate its output. For highest efficiency, each converter could be its own inductor-based switching regulator. However, as previously stated, this creates additional weight. Instead, two candidate topologies are examined: a shared-inductor

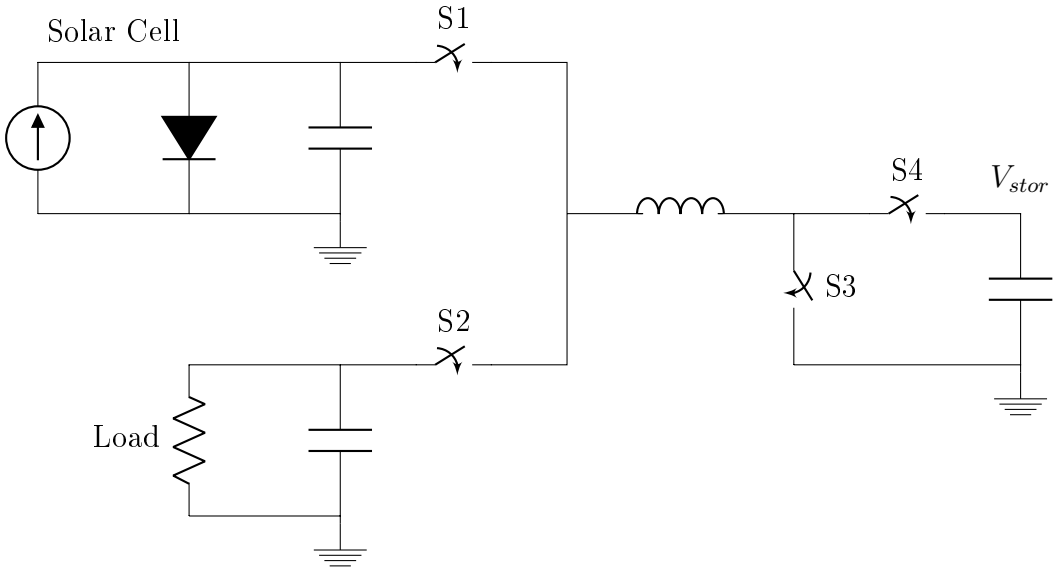


Figure 2-1: Schematic of inductor-sharing for harvesting energy and regulating output voltage.

topology as in [51] and a boost-converter to a low-dropout regulator (LDO).

An example of a shared-inductor harvester and output regulator is shown in Figure 2-1. The system operates by periodically switching between energy-harvesting and output-regulation modes. S1 remains closed and S2 remains open when the circuit acts as a boost converter by switching S3 and S4 for harvesting energy from the solar cell. The harvested energy is stored on the capacitor at the node labeled V_{stor}. When regulating the output load voltage, S2 remains closed and S1 remains open while the circuit acts as a buck converter by switching S3 and S4 while drawing power from the V_{stor} capacitor. In this way, energy from the solar cell must first be stored into the capacitor at V_{stor} and then be removed from it to power the load. If all components are ideal, this topology is lossless. However, the circuit must have a method of retaining substantial energy during moments without ambient energy. As a result, a supercapacitor is often placed at V_{stor}. Supercapacitors have nonnegligible series resistance, introducing a large nonideality into the model of Figure 2-1.

In order to simplify the analysis of the effect of adding a series resistor to the capacitor at V_{stor}, the shared-inductor system is modeled as in Figure 2-2. The left circuit represents the system in energy-harvesting mode where energy is stored

onto V_{stor}, and the right circuit represents the system in output-regulation mode where energy is taken from V_{stor} and deposited into the load. The converters are still assumed to be lossless, and as such they are modeled as constant-power sources as seen by their values in Figure 2-2. A constant-power source is modeled as a current source whose value changes with the voltage across it. The switching effects of S3 and S4 in Figure 2-1 are ignored, which is a valid approximation assuming the switching frequency is sufficiently high and a low equivalent-series-resistance (ESR) capacitor of a high enough value is placed in parallel with the supercapacitor at V_{stor}. The losses in the circuit are entirely determined by the supercapacitor's series resistance and are found to be

$$P_{loss} = \frac{E_{loss}}{T} = \frac{\frac{T}{2}\left(\frac{P_{in}}{V_{stor}}\right)^2 R_{sc} + \frac{T}{2}\left(\frac{P_{out}}{V_{stor}}\right)^2 R_{sc}}{T} = \frac{R_{sc}}{2V_{stor}^2}\left(P_{in}^2 + P_{out}^2\right) \tag{2.1}$$

where P_{loss} is the power lost in the circuit, E_{loss} is the energy lost in the circuit, T is the period of switching between stages, P_{in} is the input power harvested from the solar cell, P_{out} is the output power consumed by the load, V_{stor} is the voltage at the V_{stor} node labeled in Figures 2-1 and 2-2, and R_{sc} is the supercapacitor's series resistance. This equation assumes the system spends equal time in energy-harvesting mode as it does in load-regulation mode. The efficiency is only affected by the R_{sc} losses and is therefore

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}} = 1 - \frac{R_{sc}}{V_{stor}^2}\left(P_{in} + \frac{P_{out}^2}{P_{in}}\right) \tag{2.2}$$

where η is the efficiency. As can be seen from Equation (2.2), the efficiency will only approach 1 as both the input and output powers approach 0 or as V_{stor} approaches infinity. Both are impractical for a physical implementation of this circuit.

A further drawback to this design is the frequency sensitivity of supercapacitors. As this system requires the supercapacitor to constantly charge and discharge at a certain frequency, the measured capacitance could fall dramatically.

Another topology is to use an LDO instead of a buck converter to regulate the

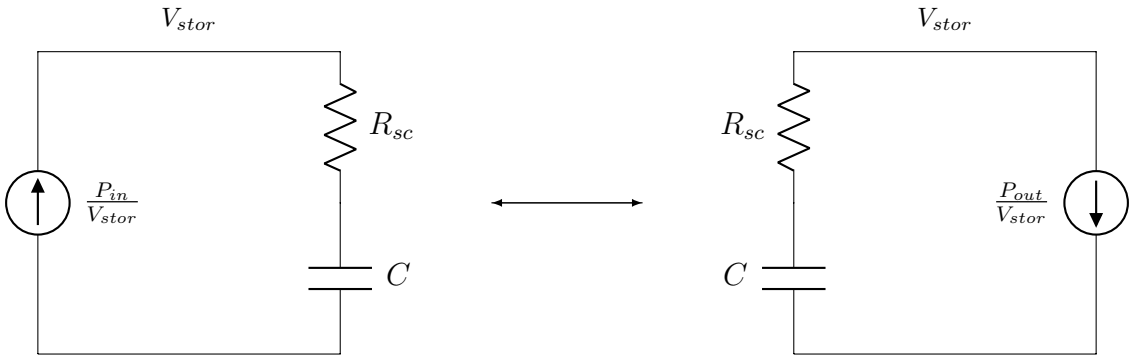


Figure 2-2: Simplified schematic of shared-inductor circuit in Figure 2-1, where the left circuit represents energy-harvesting mode and the right circuit represents output-voltage-regulation mode.

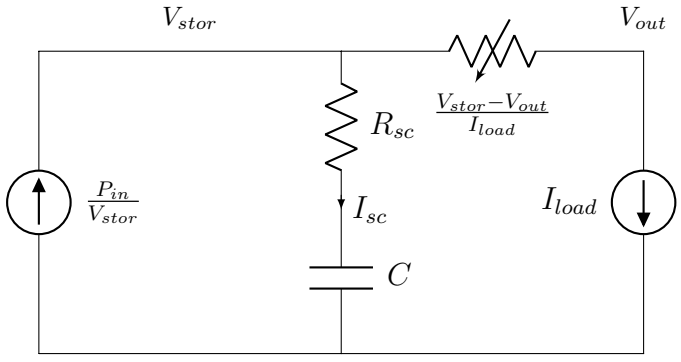


Figure 2-3: Schematic of system with inductor-based energy harvester and LDO-based output voltage regulator.

output voltage. This circuit is shown in Figure 2-3, where the energy harvester switching converter is replaced by a constant-power source. The LDO functions by varying a resistor-like element to control the output voltage based on the V_{stor} voltage and the output current. The system does not alternate between various modes, as no inductor is shared. To begin calculating the losses in the supercapacitor's series resistor, the current in the supercapacitor is found to be

$$I_{sc} = \frac{P_{in}}{V_{stor}} - I_{load} \tag{2.3}$$

where I_{sc} is the current into the supercapacitor and I_{load} is the output load current. The variable resistor in the LDO introduces further losses to the system, where the losses are dependent on the value of the LDO variable resistor shown in Figure 2-3. By using Equation (2.3), the total losses in the system are found to be

$$P_{loss} = I_{sc}^2 R_{sc} + I_{load}^2 \frac{V_{stor} - V_{out}}{I_{load}} \tag{2.4}$$

$$P_{loss} = \left(\frac{P_{in}}{V_{stor}} - I_{load} \right)^2 R_{sc} + I_{load} \left(V_{stor} - V_{out} \right) \tag{2.5}$$

In steady state, the current into the supercapacitor is 0, and thus the input current and load currents are equal. The steady state value of V_{stor} is found to be

$$V_{stor,\,ss} = \frac{P_{in}}{I_{load}} \tag{2.6}$$

where $V_{stor,\,ss}$ is the steady state value of V_{stor}. P_{loss} in steady state becomes

$$P_{loss,\,ss} = I_{load} \left(V_{stor,\,ss} - V_{out} \right) = P_{in} - P_{out} \tag{2.7}$$

where $P_{loss,\,ss}$ is the steady state value of P_{loss}. Since no current flows into the supercapacitor in steady state, the efficiency is simply

$$\eta_{ss} = \frac{P_{out}}{P_{in}} \tag{2.8}$$

where η_{ss} is the steady state efficiency. As can be seen from Equations (2.7) and (2.8), the efficiency can theoretically reach 1 and the loss can reach 0 as the output power approaches the input power. This varies dramatically from the shared-inductor efficiency in that there is no theoretical limit on the input and output powers for the efficiency to reach 1. This allows for potentially high efficiency at a high load. However, with higher loads, $V_{stor,\,ss}$ decreases. This is the opposite of the theoretical shared inductor topology, where as long as the output power is less than the input power, V_{stor} will continually rise. Table 2.1 summarizes the advantages and disadvantages of each topology.

In the end, the LDO-based design was chosen because it has a higher efficiency as output power increases and thus allows higher possible output power for a given input power compared to the shared-inductor design. Maximizing output power was particularly important for the DragonflEye application. The next section describes how the disadvantage of lower energy storage capabilities was addressed.

2.3 Energy Storage Architecture

While using an LDO-based output voltage regulator could limit maximum stored energy, one option is to remove the energy storage function from the capacitor at V_{stor} and to simply use it as a buffer capacitor for load transients. Then, an energy storage element could remain fully charged and idle until the harvested power drops below the output power. This can be completed by using a lightweight, low-ESR ceramic capacitor at V_{stor} and using either a supercapacitor or a battery as the energy storage element. Chapter 3 examines the results of systems with both a supercapacitor and a battery.

Charging circuitry must be added to allow a voltage step-up from V_{stor} to the charging voltage of the storage element. The system is designed such that during startup (discussed in detail in Chapter 3) the energy storage element is sufficiently charged before turning on the output load voltage. Once the system has turned on the output load voltage, the system will only charge the energy storage element

	Advantages	Disadvantages
Shared-Inductor	• Energy stored on V_{stor} will continually increase as long as output power is less than input power	• Higher losses at steady state with high load • Efficiency decreases as load increases • Higher switching and conduction losses (2 more switches, S1 and S2) • Potentially complex controls • High operating frequency sensitivity of supercapacitors
LDO	• Efficiency increases as load increases • Lower switching and conduction losses (2 fewer switches, no S1 or S2) • Simpler controls	• Energy stored on V_{stor} inversely proportional to load current

Table 2.1: Shared-inductor versus LDO approaches to regulating output voltage.

further if there is a large surplus of harvested energy compared to the load energy. In both cases, the efficiency of the charger has no effect on the maximum possible output power of the load. Thus, the natural choice for the charger in this lightweight application would be a fully integrated, inductorless SC charge pump.

When discharging the energy storage element to power the load, efficiency matters much more than when charging. This is because the discharging efficiency determines how long the system can last in the absence of solar power, whereas charging occurs when there is an excess of harvested solar power. A more efficient discharger using a buck converter allows longer operating time. However, because an additional inductor will add more weight, the inductor must be borrowed from the energy harvester. This means that while efficiently discharging the energy storage element with a buck converter, no energy can be harvested from the solar cell. The alternative is to use a linear regulator. This is less efficient but allows solar energy to still be harvested during discharge. Chapter 3 examines circumstances in which one discharger may be more appropriate than the other for battery- and supercapacitor-powered systems.

The controls for such a design can be approached in a variety of ways. Since the charger will turn on when there is a surplus of harvested power and the discharger will turn on when there is a deficiency of harvested power, one method of designing the controls is to measure and compare harvested power and output power. This method would, however, require two voltage and two current measurements. This type of approach could therefore be very expensive in terms of power consumption. A simpler alternative is to monitor V_{stor}. Since

$$P_{out} = V_{load} I_{load} \tag{2.9}$$

where V_{load} is constant, then by using Equation (2.6), it is clear that

$$V_{stor,\,ss} \propto \frac{P_{in}}{P_{out}} \tag{2.10}$$

This shows that the value of $V_{stor,\,ss}$ is an appropriate indicator of the amount of excess energy being harvested. However, this is only true in steady state, and in

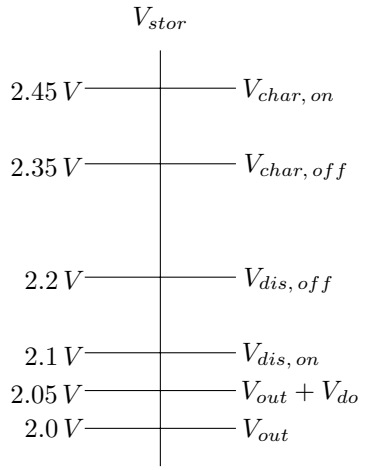


Figure 2-4: Example thresholds on V_{stor}, where V_{char} and V_{dis} indicate threshold voltages to turn on or off charger and discharger for energy storage element (respectively), V_{out} is the output voltage, and V_{do} is the dropout voltage for the LDO.

fact will only work with an excess of harvested energy. If the harvested energy is less than the output power, the voltage at V_{stor} will fall below the output voltage, and the LDO will no longer be able to regulate the output. If the capacitor at V_{stor} is sufficiently large, then when changing from an excess to a deficiency of harvested energy, the voltage at V_{stor} will drop slowly. A minimum V_{stor} threshold slightly higher than the dropout voltage of the LDO can be set to determine when the stored energy discharger should be turned on to charge up V_{stor}. The discharger can then be turned off once V_{stor} has risen sufficiently. The same can be done in the opposite direction for the charger. When V_{stor} exceeds a certain threshold indicating a large enough surplus of harvested energy, the charger can turn on. Once V_{stor} has fallen below this value the charger will turn off. Hysteresis should be added for both the charger and discharger thresholds for stable operation. Example thresholds on V_{stor} are shown in Figure 2-4. The system operates normally between $V_{dis,\,on}$ and $V_{char,\,on}$ until one of the thresholds is crossed. Note that $V_{dis,\,on}$ should be slightly higher than $V_{out} + V_{do}$ in order to account for propagation delays in the control circuitry.

2.4 RF Energy Harvesting

As previously discussed, the majority of power to the load will come from the solar cell. In this sense, the RF harvester can be thought of as an auxiliary source to alleviate demands on the solar harvester. This is because at the expected high output powers, the system can not rely on the RF harvester alone. When there is no solar energy, the system then relies on the energy in the energy-storage element and not on the RF harvester, though the RF harvester can alleviate demands on the power output from the energy-storage element as it would to the solar cell. Furthermore, the RF harvester as a low-power source uses an SC charge pump-based design. In the high-level design, there are several places to which the charge pump could output power: the energy storage element, the V_{stor} node, or the output node. Outputting power to the energy storage element would allow it to be charged even when there is not a large excess of harvested solar power. However, if using a battery, a constant-voltage or constant-current type charger might need to be used, creating a more complex harvester. Furthermore, the energy storage element is the highest voltage in the system, and generally the larger the difference between the charge pump input and output voltages, the less efficient the charge pump becomes. Outputting at V_{stor} has the benefit of being at a lower voltage, but any energy flowing from the RF harvester to V_{stor} must be converted again through the LDO to reach the load, thus elongating the power path and limiting efficiency and usable power. This leaves the output load voltage as the most reasonable place to deposit harvested power. It has the lowest voltage of the three nodes, and as the power consumed by the load will likely be higher than the power provided by the RF harvester, the RF harvester sees a fixed output voltage and alleviates power demands on the solar harvester. This increases the maximum possible load power when both the RF and solar harvesters are providing power.

The other benefit to having a fixed output voltage is that designing the SC charge pump for impedance matching over various input powers is dramatically simplified compared to a charge pump with a variable output or a charge pump whose controller

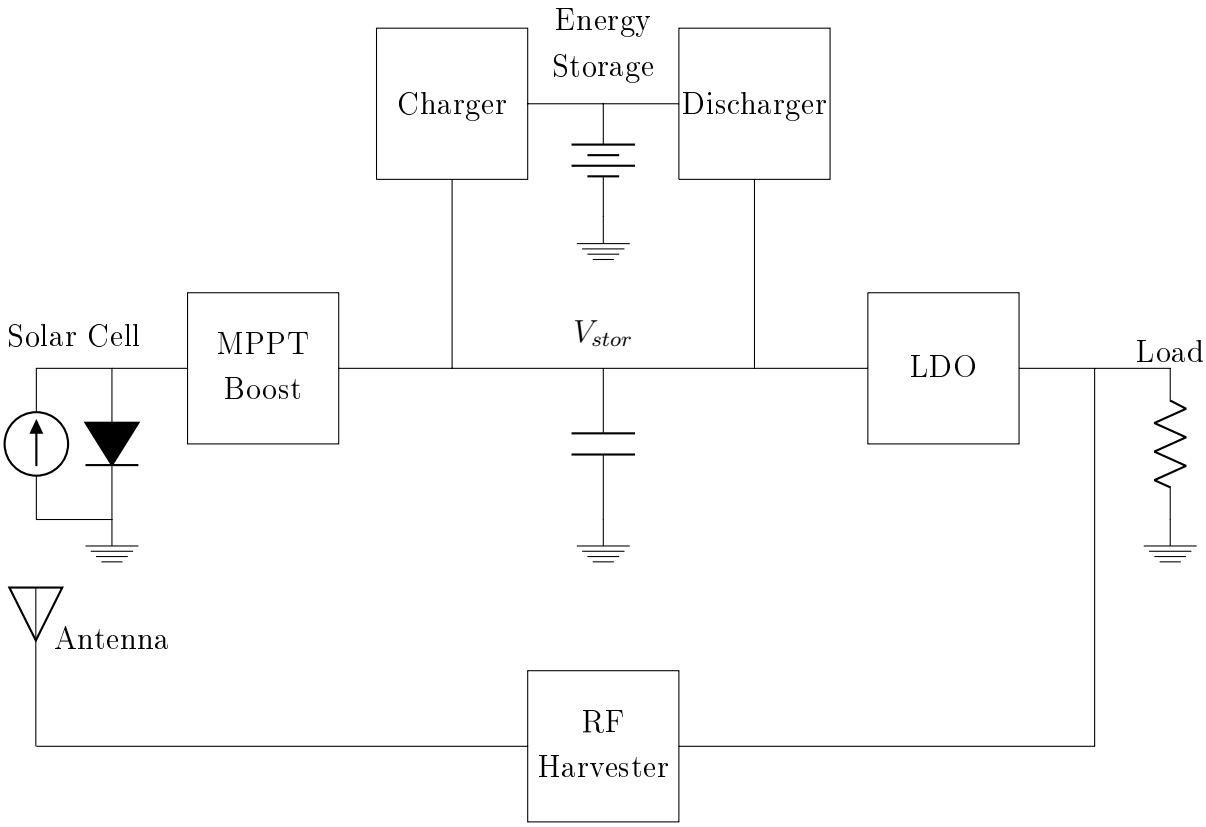


Figure 2-5: Top-level diagram of energy harvesting system.

must on its own provide a regulated output. The RF harvester therefore functions as an auxiliary energy harvester for alleviating demands on the solar harvester. In fact, the design concept is flexible enough that with slight modifications to the controller, the RF harvester can function as an auxiliary harvester for most systems with a fixed output voltage.

2.5 Complete Top-Level System Design

Figure 2-5 illustrates the entire system comprising an MPPT boost converter solar harvester, an SC charge pump-based RF harvester, an energy storage unit composed of a charger and discharger, and an LDO output voltage regulator. The following chapters describe the design in further detail with results of a discrete implementation of battery- and supercapacitor-based systems.

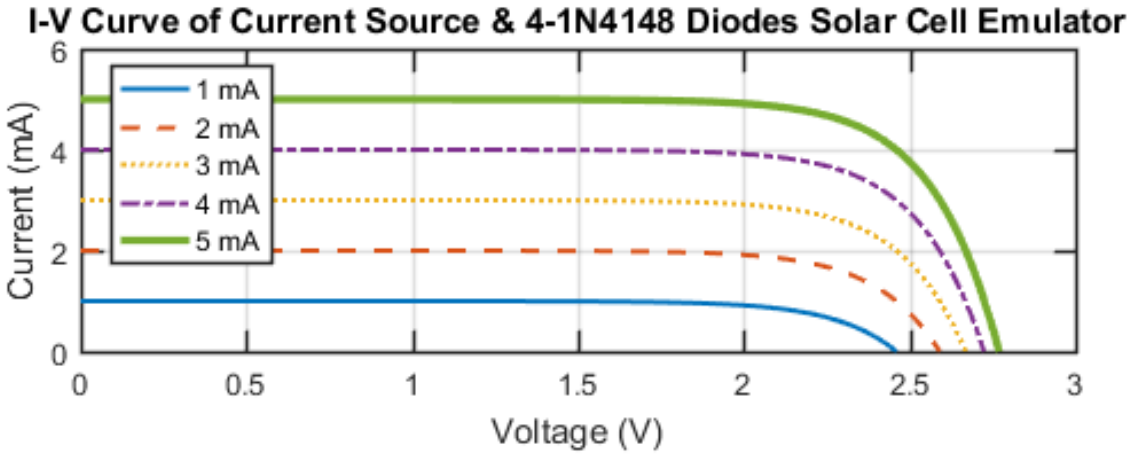
Chapter 3

Solar Harvester and Energy Storage Architecture

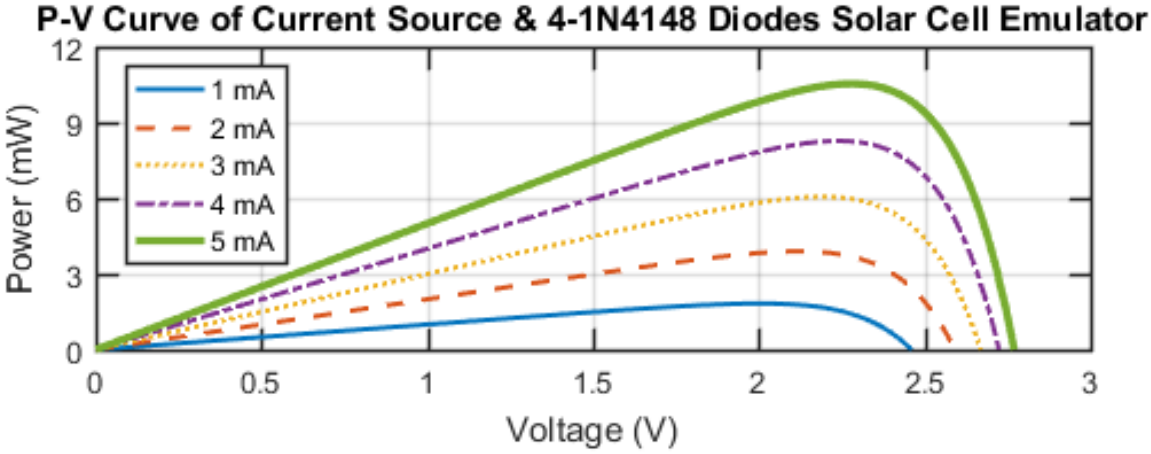
Two discrete-component implementations of the system described in the previous chapter were built and tested, one using a supercapacitor as the energy storage element and the other using a battery. A solar harvester IC was used for the discrete systems with details shown in Section 3.1. The following sections describe the complete systems with the energy storage architectures. This chapter ignores the contributions from the RF harvester since the majority of the load power will come from the solar cell and since the RF harvester does not contribute to the stored energy.

3.1 Solar Harvester

In order to facilitate easier testing and analysis of the presented system, a solar cell was emulated using a current source in parallel with 4 series 1N4148 diodes. This is the same as the model shown in Figure 1-2, with an R_p of infinity and an R_s of 0. The resulting I-V and P-V curves for various input currents for the built emulator are shown in Figure 3-1 with specific values shown in Table 3.1. Figure 3-2 shows the I-V and P-V curves of the actual solar cell to be used, a C3P5 triple-junction solar cell on a Germanium substrate by Spectrolab with a weight of approximately 35 mg, with specific values shown in Table 3.2



(a) Measured I-V curve of physical solar cell emulator.

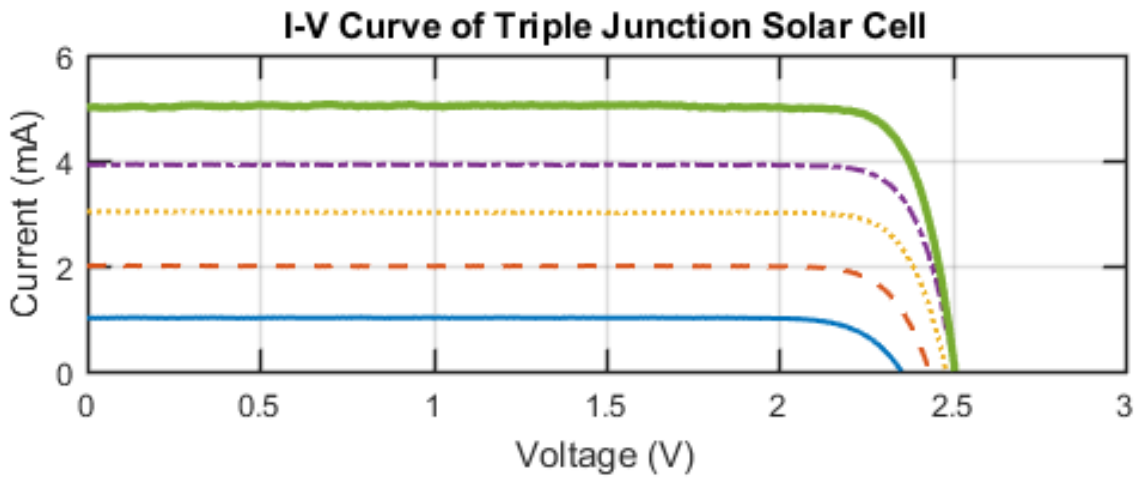


(b) Measured P-V curve of physical solar cell emulator.

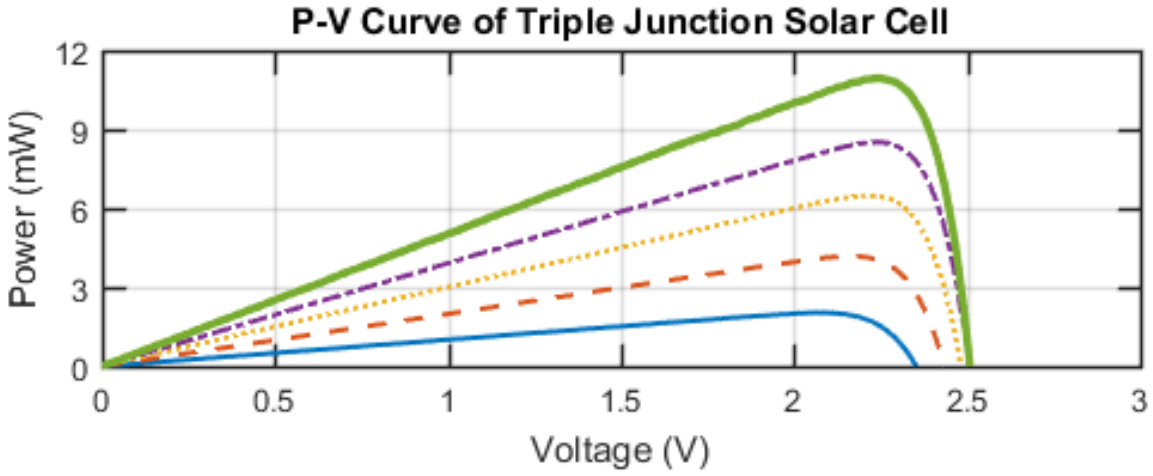
Figure 3-1: Measured I-V and P-V curves of solar cell emulator made of current source in parallel with 4 series 1N4148 diodes, tested over 5 different current source values.

Current (mA)	1	2	3	4	5
V_{oc} (V)	2.460	2.591	2.669	2.724	2.770
V_{mpp} (V)	2.00	2.12	2.19	2.24	2.28
I_{mpp} (mA)	0.9157	1.838	2.765	3.692	4.620
P_{mpp} (mW)	1.831	3.898	6.056	8.271	10.53
V_{mpp}/V_{oc}	81.3%	81.8%	82.1%	82.2%	82.3%

Table 3.1: Open-circuit voltage (V_{oc}); MPP voltage, current, and power (V_{mpp}, I_{mpp}, and P_{mpp}, respectively); and MPP-voltage-to-open-circuit-voltage ratio of solar cell emulator for various input currents.



(a) Measured I-V curve of physical solar cell.



(b) Measured P-V curve of physical solar cell.

Figure 3-2: Measured I-V and P-V curves of triple-junction solar cell on Ge substrate over various input irradiance levels.

V_{oc} (V)	2.353	2.435	2.482	2.505	2.508
V_{mpp} (V)	2.075	2.165	2.220	2.240	2.245
I_{mpp} (mA)	0.983	1.935	2.921	3.802	4.878
P_{mpp} (mW)	2.039	4.190	6.485	8.516	10.950
V_{mpp}/V_{oc}	88.2%	88.9%	89.4%	89.4%	89.5%

Table 3.2: Open-circuit voltage (V_{oc}); MPP voltage, current, and power (V_{mpp}, I_{mpp}, and P_{mpp}, respectively); and MPP-voltage-to-open-circuit-voltage ratio of measured triple-junction solar cell on Ge substrate over various input irradiance levels.

As can be seen, both the emulator and actual solar cell demonstrated almost constant ratios of the MPP voltage to the open-circuit voltage. This, combined with the fact that a very simple and low-power MPPT algorithm was preferred, led to the choice of using the FOCV MPPT algorithm described in Chapter 1. As a result, the BQ25504 Texas Instruments IC was used in this system. It samples the solar cell's open-circuit voltage for approximately 256 ms every 16 seconds. In an ASIC design of this system, a much shorter disconnection period is preferred, as a smaller ceramic capacitor at V_{stor} will power the system during this time. However, this IC still functioned well in the discrete implementation of the systems.

3.2 Supercapacitor-Based System

This section examines the previously presented system with a supercapacitor as the energy storage element. The particular supercapacitor used is XH414HG-IV01E by Seiko Instruments, with a nominal capacitance of 80 mF and a mass of 60 mg.

A simplified schematic of this system is shown in Figure 3-3. The block labeled "MPPT Boost" represents the BQ25504 chip mentioned in Section 3.1; bypass capacitors are shown immediately to its left and right. The capacitor directly below the V_{stor} label represents a 22-μF storage capacitor on V_{stor}. While a large capacitor will allow the V_{stor} voltage to vary more slowly and allow the use of slower and lower-power comparators and controls, a larger capacitor usually weighs more. As a balance between the two parameters, this system is designed around a 22-μF 0402 ceramic capacitor at V_{stor} with an approximate mass of 3.5 mg. The supercapacitor with its equivalent series resistance is shown immediately below the node labeled V_{sc}. The charger and its control circuitry are shown to the left of the supercapacitor, made of two comparators, an OR gate, an SC voltage doubler, and a diode. The buck converter discharger is shown to the right, made of two FETs and an inductor. The LDO is labeled and outputs to the load in parallel with a bypass capacitor. Signals to and from the FPGA are also labeled and are level shifted with external circuitry if needed (e.g. resistor dividers, high-speed comparators; not labeled). Lastly, the main

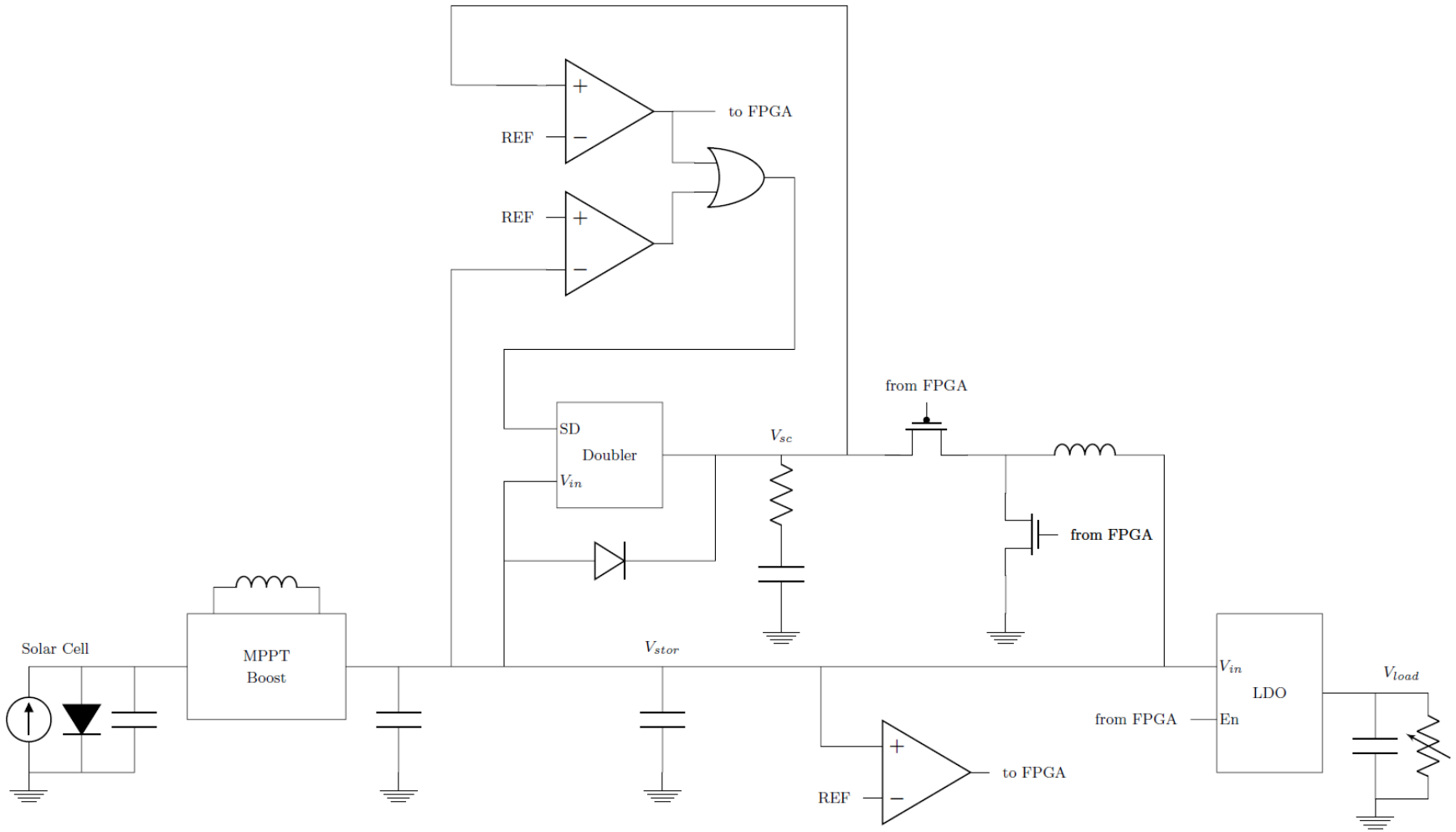


Figure 3-3: Schematic of supercapacitor-powered system.

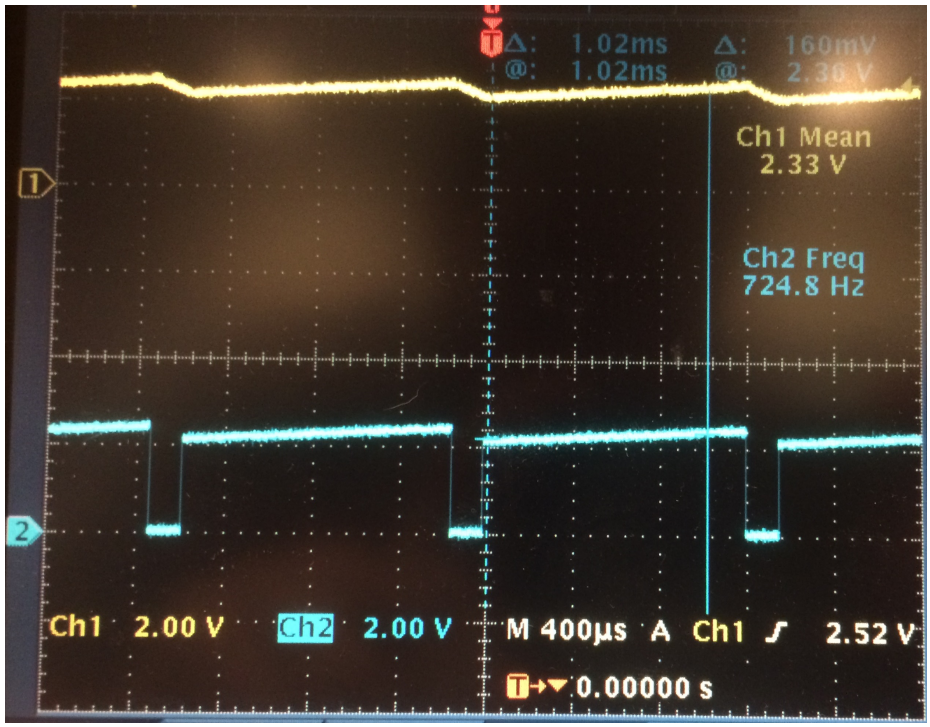
low-power comparators are also shown where used. The following sections describe the charger, discharger, and full system in further detail.

3.2.1 Charger

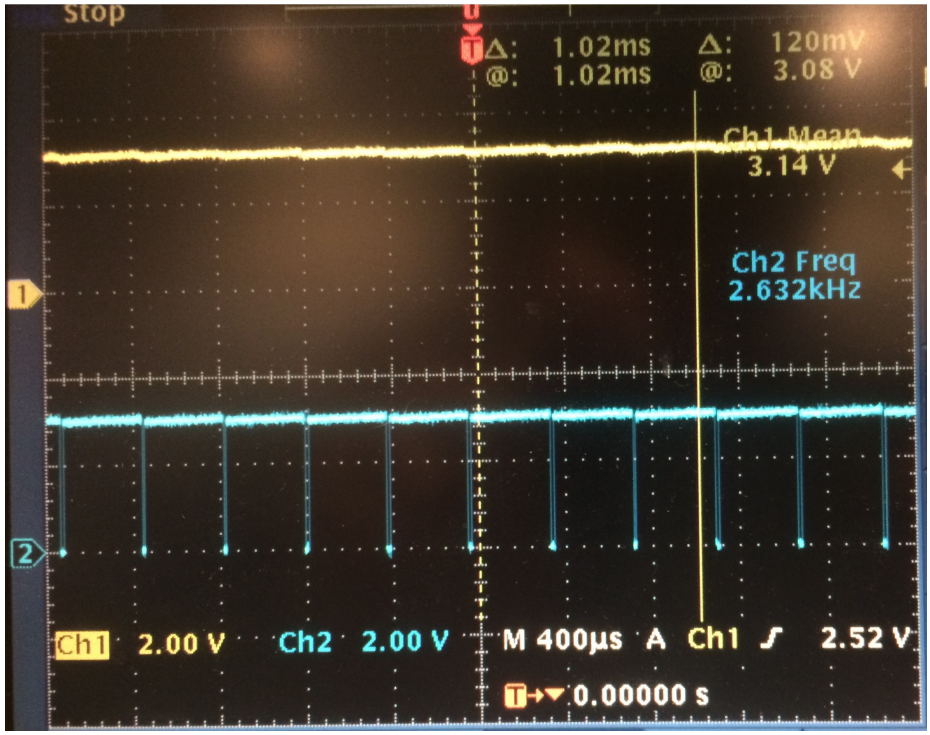
As discussed in Chapter 2, the charger will comprise an SC voltage doubler. An IC requiring a diode for start-up was used (LM2767M5/NOPB), as shown in Figure 3-3. Also shown are the very simple controls used for the charger. One comparator with hysteresis monitors V_{stor} to turn on the charger at approximately 2.35 V and turn it off at approximately 2.25 V. Another monitors the voltage at V_{sc}, the supercapacitor voltage, as this voltage should not exceed 3.3 V for this specific supercapacitor. An OR gate is used to shutdown the voltage doubler using its shutdown (SD) pin if required by either comparator.

In order to independently test the supercapacitor charger, a current source was placed on the V_{stor} node with its 22-μF capacitor and connected only to the charger and not to the boost converter, discharger, or load. The behavior of the charger and its controller is shown in Figure 3-4a. As expected, V_{stor} increases due to the current source until the charger comparator at V_{stor} detects V_{stor} to be high enough to charge the supercapacitor. Then, the doubler shutdown signal falls low, and V_{stor} decreases until the comparator detects that V_{stor} is too low to continue charging the supercapacitor. After the supercapacitor is fully charged, the waveform abruptly changes to that of Figure 3-4b, and the current source attached at V_{stor} reaches its set voltage limit. Because of the high series resistance of the supercapacitor, V_{sc} varies noticeably between when the charger turns on or off, explaining moments of charging in Figure 3-4b, even though the supercapacitor is fully charged.

Table 3.3 shows the time it took to fully charge the supercapacitor depending on the current source placed on V_{stor}. When testing the system with a current source into V_{stor}, the supercapacitor would charge through the doubler's start-up diode before the control circuitry would even turn on. As a result, the times in Table 3.3 indicate when the charger-shutdown signal first fell to when the fully-charged signal first turned on.



(a) Typical charging waveforms.



(b) Charging waveforms after supercapacitor is fully charged.

Figure 3-4: Waveforms while charging supercapacitor and after charging is completed. V_{stor} (yellow, channel 1) and voltage doubler active-high shutdown signal (blue, channel 2).

Table 3.3: Charging times for various V_{stor} input currents for supercapacitor charger.

Input Current (mA)	0.5	1	2	3	4	5
Charge Time (s)	563	253	115	72	46	30

3.2.2 Discharger

In order to allow the system to run without ambient energy for as long as possible, a buck converter was used for the supercapacitor discharger. For this particular discrete implementation, a 1-mH inductor switching at a fixed frequency of 200 kHz was used. In an integrated converter, the switching frequency would likely be on the order of 1 MHz or higher, allowing the inductor to be much smaller. A larger inductor and lower switching frequency were used in the discrete system to limit switching losses that would be much more controlled in the integrated system. The discharger operated at a fixed 90% duty cycle when on. In order to estimate the efficiency of such a discharger, a fixed voltage source (V_{in}) was placed at the input of the buck converter and tested over a wide range of load currents at the buck converter output. The efficiency was then recorded, including the effects of the gate drivers' currents powered from V_{in}. The tests were repeated for six different values of V_{in}, representing V_{sc} as the supercapacitor discharges. The results are shown in Figure 3-5. SPICE simulations indicate that the discharger current into V_{stor} for various supercapacitor voltages occurs on the order of 10 mA, which happens to be where the efficiency is greater than 95% according to the measured data. These results therefore suggest that using a buck converter at a fixed 90% duty cycle, while simple, is a very efficient method of discharging the supercapacitor to charge V_{stor}.

The discharger was controlled by the lowest comparator on V_{stor} shown in Figure 3-3. The discharger turned on at a fixed 90% duty cycle whenever V_{stor} fell below 2.09 V and turned off when V_{stor} rose above 2.18 V. Figure 3-6 shows the results of the discharger powered by a fully charged supercapacitor with the controller and a 1-mA

load on V_{stor}. Figure 3-6a shows the system with 300 nF of bypass capacitors needed at V_{sc} for the discrete system. V_{sc} demonstrated a significant amount of ringing when the discharger turned on. Figure 3-6b shows the same system with an additional 4.7-μF capacitor added to prevent ringing at V_{sc}. While adding an additional bypass capacitor corrected the ringing, it had negative effects on the operation time of the system.

In order to understand how operation time was affected by the load current on V_{stor}, tests were conducted with a constant current load on V_{stor}. The supercapacitor was charged at 3.3 V until its current draw reached 5 μA. Then, the load was turned on, and the discharger controller began to operate. The time the discharger lasted

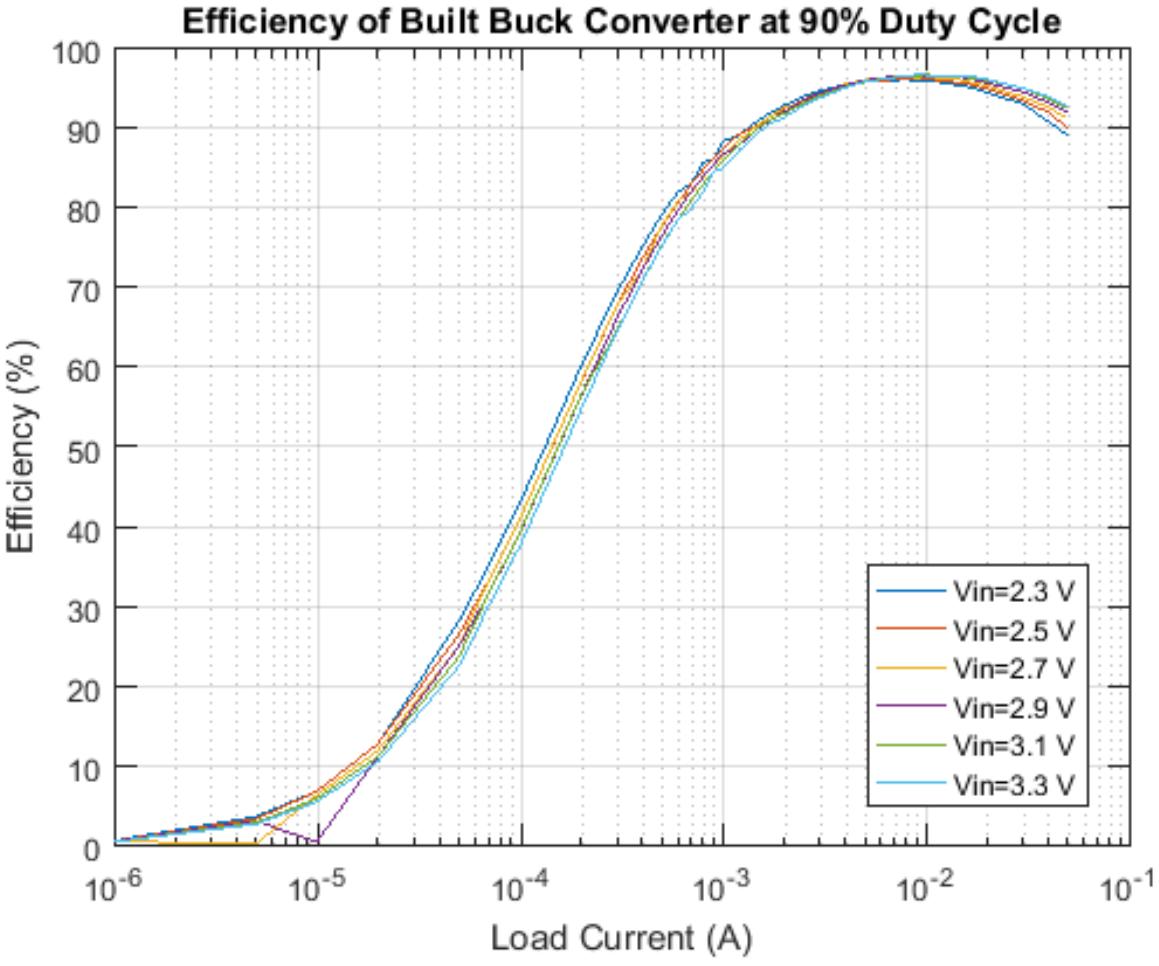
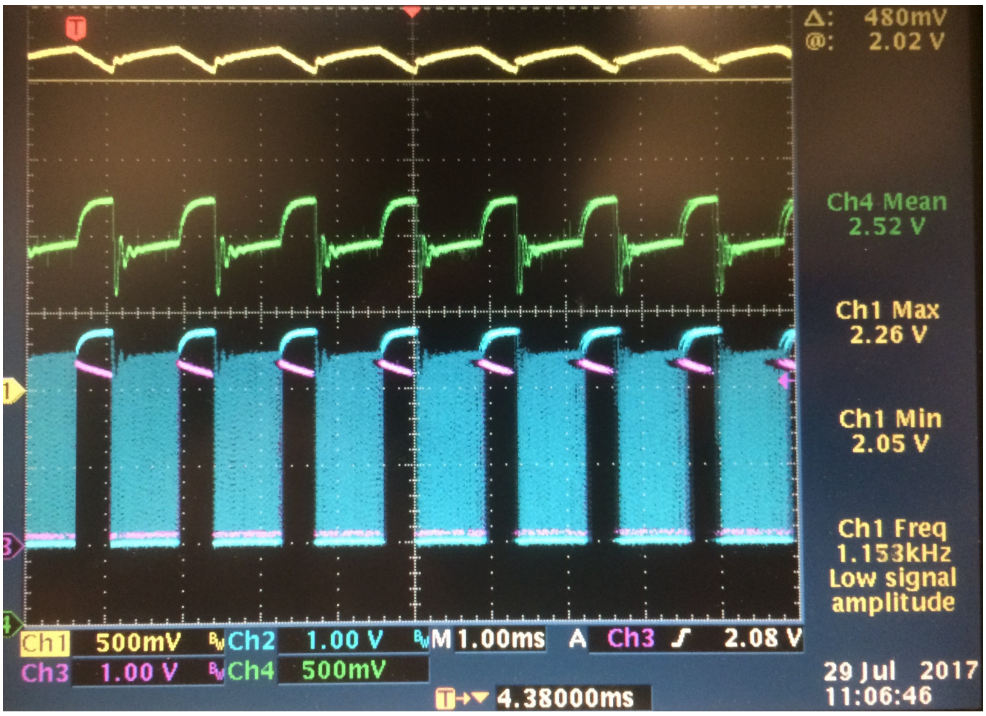
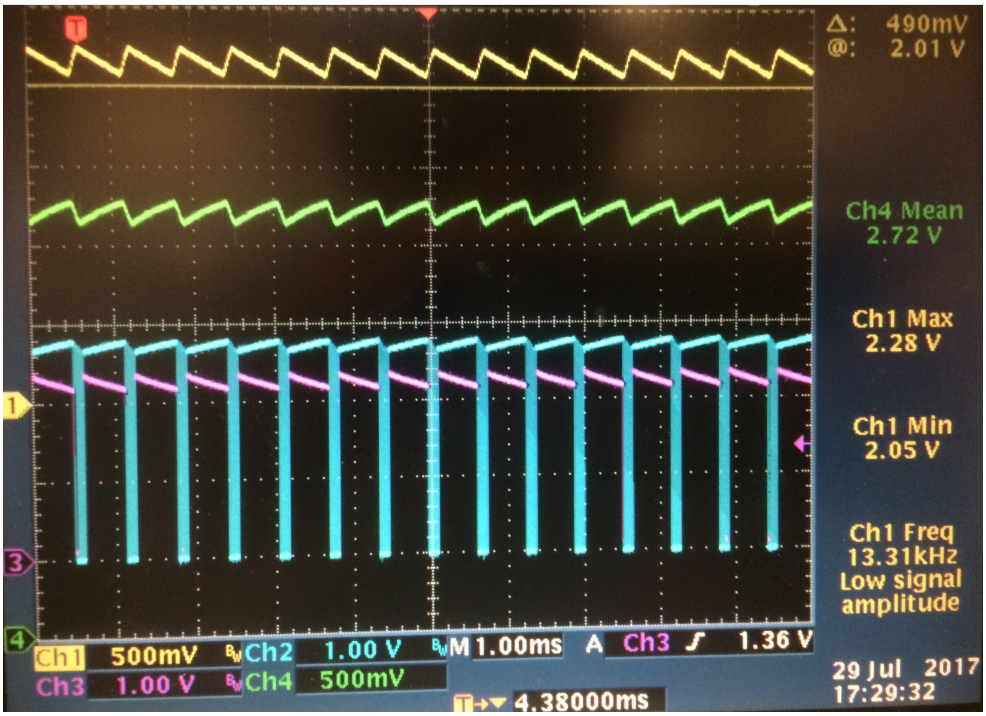


Figure 3-5: Efficiency of built and measured buck converter running at 90% duty cycle for various load currents. Tested over various input voltages, demonstrating minimal differences in behavior. Includes gate driver power losses powered by V_{in}.



(a) 300 nF in parallel with supercapacitor.



(b) 300 nF plus 4.7 μF in parallel with supercapacitor.

Figure 3-6: Waveforms of buck converter discharger on supercapacitor with and without a 4.7-μF capacitor in parallel with supercapacitor. V_{stor} (yellow, channel 1), PFET gate (cyan, channel 2), V_{stor} comparator (pink, channel 3), V_{sc} (green, channel 4).

was determined to be the time it took for V_{stor} to drop below 2.01 V. At a certain moment during each test, the buck converter began to operate continuously, rather than switch on and off as shown in Figure 3-6. This indicates the discharger could not cause V_{stor} to reach the turn-off threshold. Figure 3-7a shows how operation time decreases with increasing load current. It also illustrates how the addition of a larger bypass capacitor decreases operation time. This is due to the $C(\Delta V)^2$ losses from the ripple on V_{sc} seen in Figure 3-6. Once the system turned off after V_{sc} could no longer charge V_{stor}, V_{sc} would slowly rise. The voltage to which it would rise depended on the load current, as can be seen in Figure 3-7b. As the current draw on V_{sc} was constantly pulsing, the AC components of the current draw likely limited the amount of current the supercapacitor could provide. This explains why for higher load currents the system would not last very long and why the open-circuit voltage would rise higher after the system shut off: the supercapacitor could not provide high AC current demands but still held the charge it would otherwise dissipate.

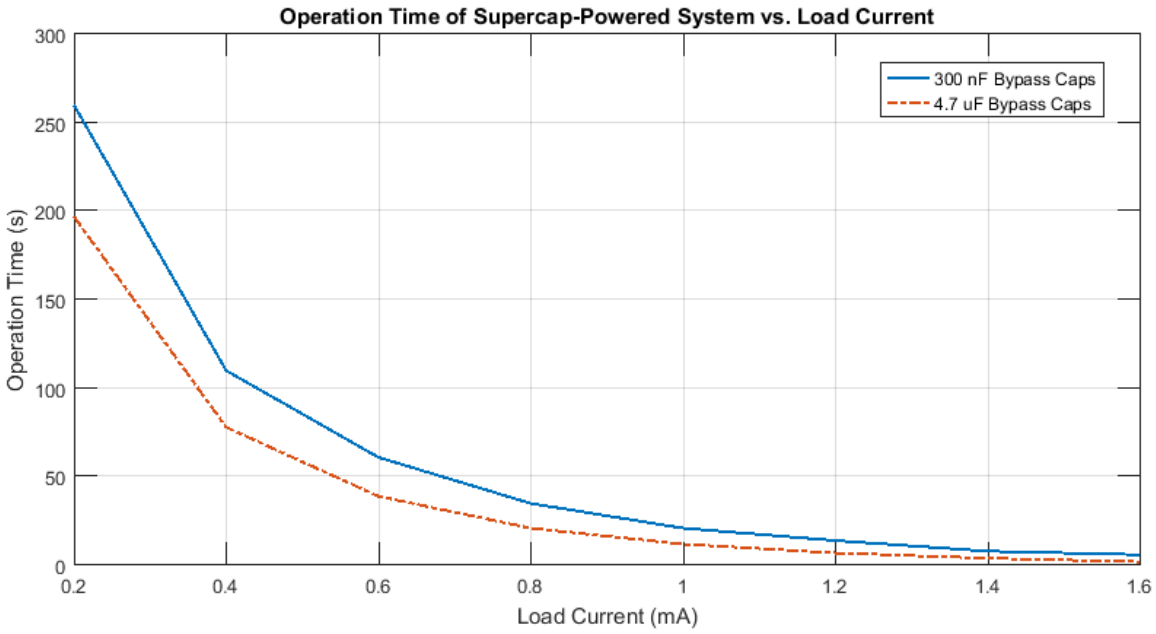
Alternatively, the DC current demands on the supercapacitor also had dramatic effects on the effective capacitance of the supercapacitor. In order to understand such effects, the supercapacitor was again fully charged, and then discharged using a DC current source. During discharge, V_{sc} was sampled every 400 ms. By line-fitting to the resulting curve, the effective capacitance was determined to be

$$C_{eff} = \frac{I_{diss}}{dV/dt} \tag{3.1}$$

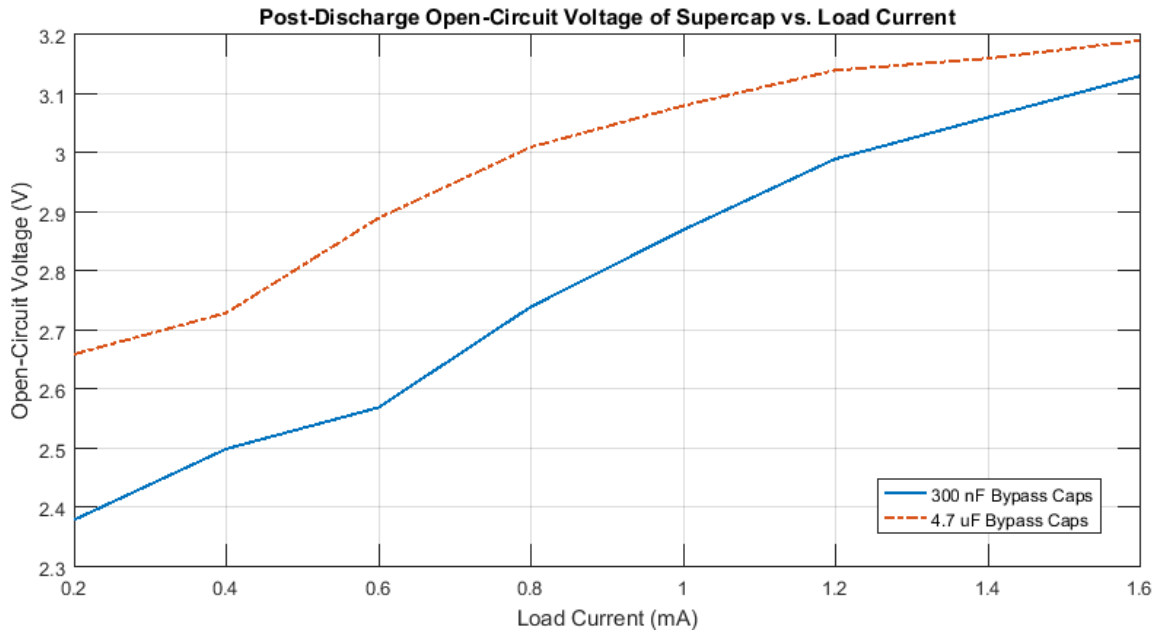
where C_{eff} is the effective capacitance, I_{diss} is the DC current source on the supercapacitor, and dV/dt is the time rate of change of the supercapacitor voltage. The results are shown in Figure 3-8a. The initial resistance was also found to be

$$R_o = \frac{(3.3\,V) - V_{sc,o}}{I_{diss}} \tag{3.2}$$

where R_o is the initial resistance of the supercapacitor, 3.3 V is the charging voltage, and $V_{sc,o}$ is the initial supercapacitor voltage when the DC load current turns on. These results are shown in Figure 3-8b.

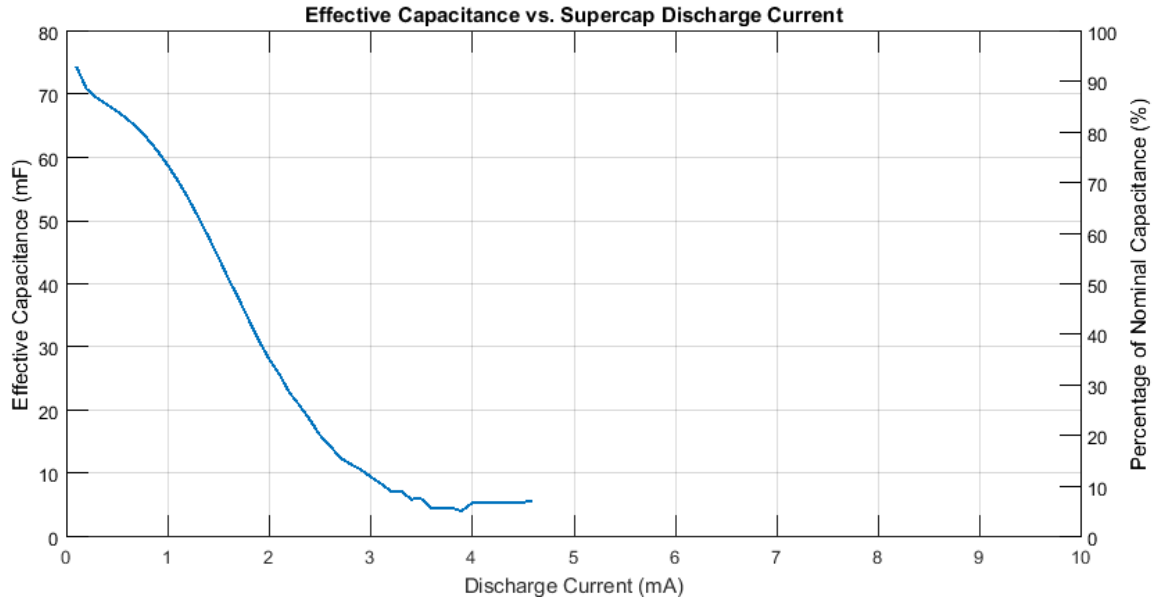


(a) Discharge time.

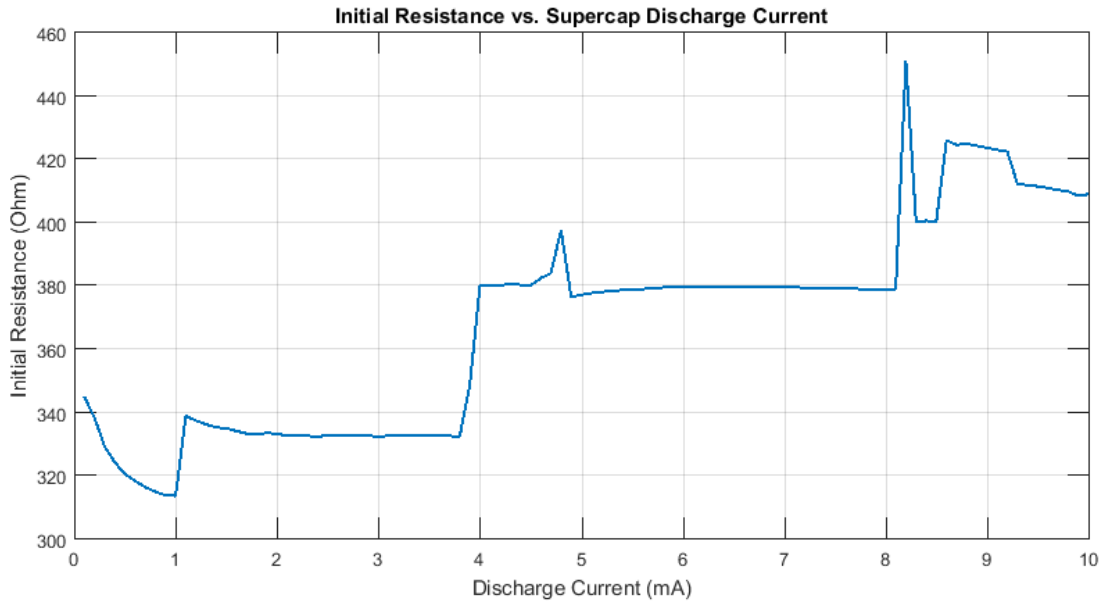


(b) Post-discharge supercapacitor open-circuit voltage.

Figure 3-7: Discharge time of charged supercapacitor using built controller over various loads, and supercapacitor open-circuit voltage after being discharged.



(a) Effective capacitance.



(b) Initial resistance.

Figure 3-8: Effective capacitance and initial resistance of supercapacitor versus DC discharge rates, averaged over three measurements.

Ultimately, the presented discharger results indicate that the use of this specific supercapacitor (XH414HG-IV01E) is unable to support high load currents for extended periods of time without ambient or transferred energy. However, it can sustain very brief demands in a highly efficient manner.

3.2.3 Complete System

After completing and characterizing the energy storage system, the entire system was built as in Figure 3-3 and tested. The physical setup is shown in Figure 3-10. The controls were coded following the state machine shown in Figure 3-9 using a Spartan 6 XC6SLX9 FPGA on a Mojo V3 development board. It should be noted that in this discrete implementation the controls for the supercapacitor charger are completely independent of FPGA inputs, as shown by the discrete OR gate in Figure 3-3. However, the FPGA does take the supercapacitor-maxed signal as an input, where the supercapacitor-maxed signal is the output from the comparator comparing V_{sc} to 3.3 V. The state machine operates by first counting how long the supercapacitor-maxed signal has been high. Then, after the supercapacitor has been determined to be sufficiently charged, the state machine switches to normal operation, where the 2-V output turns on and the charger may operate in the case of a high enough V_{stor} voltage. When the comparator on V_{stor} falls low, the discharger turns on until the comparator outputs high, in which case the system switches back to normal operation. This very simple state machine with minimal inputs and outputs allows for a low-power, low-area control system, especially in an integrated solution.

Figure 3-11 shows a complete system for a 1-mA resistive load on the 2.0-V output. The labeled points are as follows:

1. solar cell model's current source turns on at 5 mA;
2. cold-start ends, charging phase begins;
3. solar cell model's current source changes to 2 mA;
4. supercapacitor has been sufficiently charged, so 2.0-V load turns on;

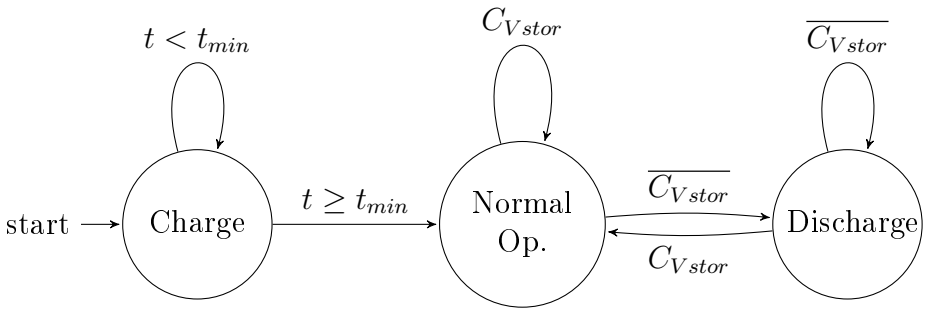


Figure 3-9: Finite state machine for supercapacitor-powered system where t is time comparator has indicated the supercapacitor is fully charged, t_{min} is minimum charge time before turning on 2.0-V output, and C_{Vstor} is output of discharger comparator on V_{stor}.

5. solar cell model's current source changes to 1.5 mA, and no charging occurs at all during this period;

6. solar cell model's current source changes to 5 mA in order to charge up supercapacitor further and quickly;

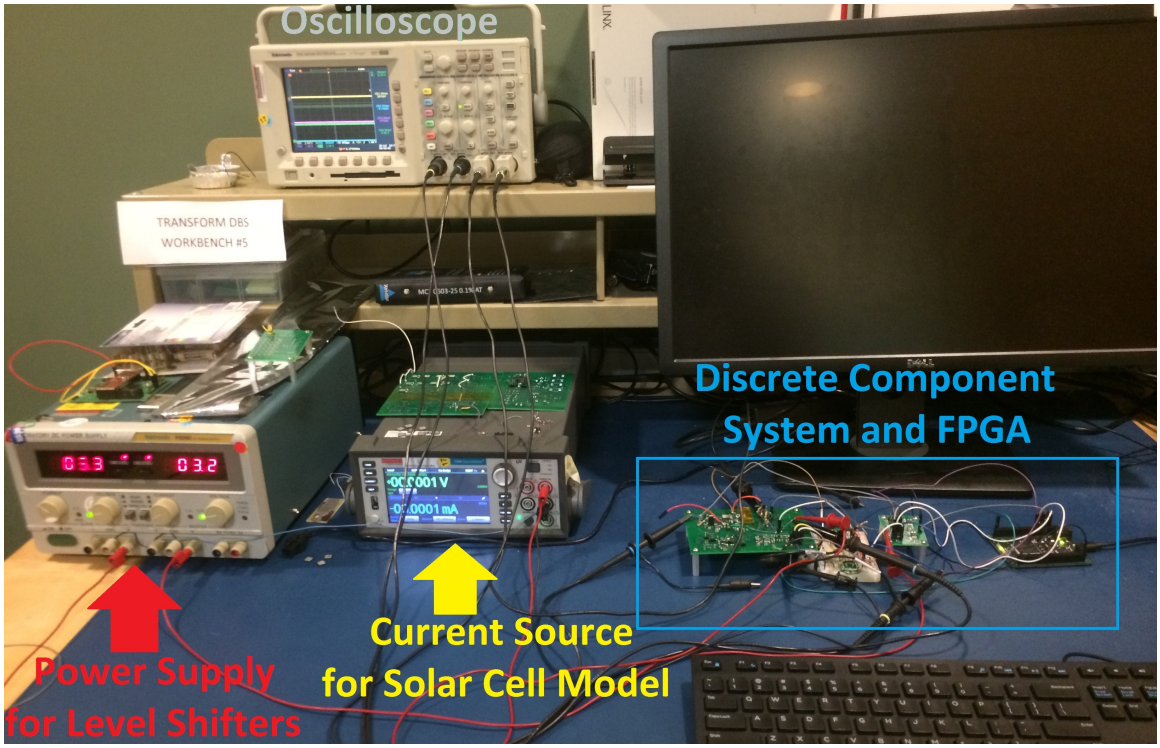
7. V_{stor} voltage maxes out, and supercapacitor charges unintentionally through SC voltage doubler's start-up diode;

8. solar cell model's current source shuts off, and system becomes entirely supercapacitor-powered;

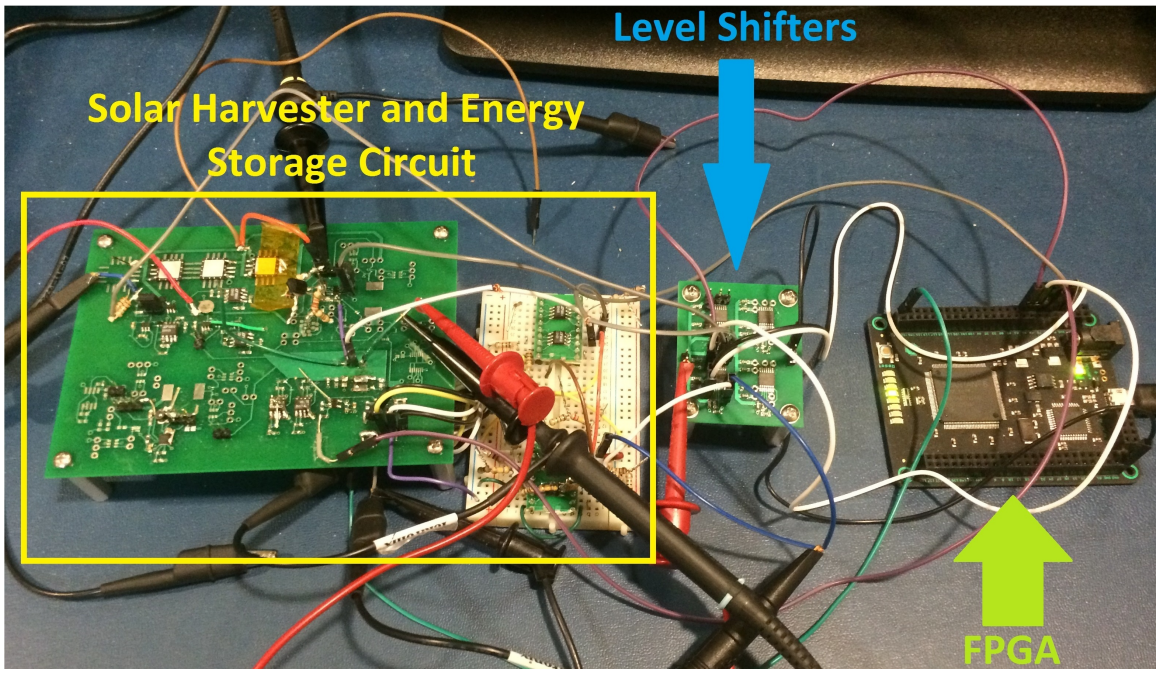
9. 2.0-V output begins to fall below 2.0 V, marking the end of system operation.

Several characteristics of the operating waveforms should be noted. Firstly, at point 1, 5 mA was used because the BQ25504's cold-start would not operate with a lower current input. This was likely due to the quiescent current draw of the charger at low supply voltages. The solution would be to incorporate an undervoltage-lockout circuit or to use a voltage doubler that draws negligible amounts of undervoltage current.

For visibility, the supercapacitor was not charged for very long (points 3 to 4), which is why it is forced to charge further at point 6. During this same period (points 3 to 4), V_{stor} dips below 2.0 V while sampling the solar cell's open-circuit voltage. However, the BQ25504 chip still remains operable, and the 2.0-V output has not been



(a) Test bench setup.



(b) Solar harvester, energy storage, and FPGA circuits.

Figure 3-10: Photographs of test bench setup and closeup of the discrete component system for both the supercapacitor- and battery-powered systems.

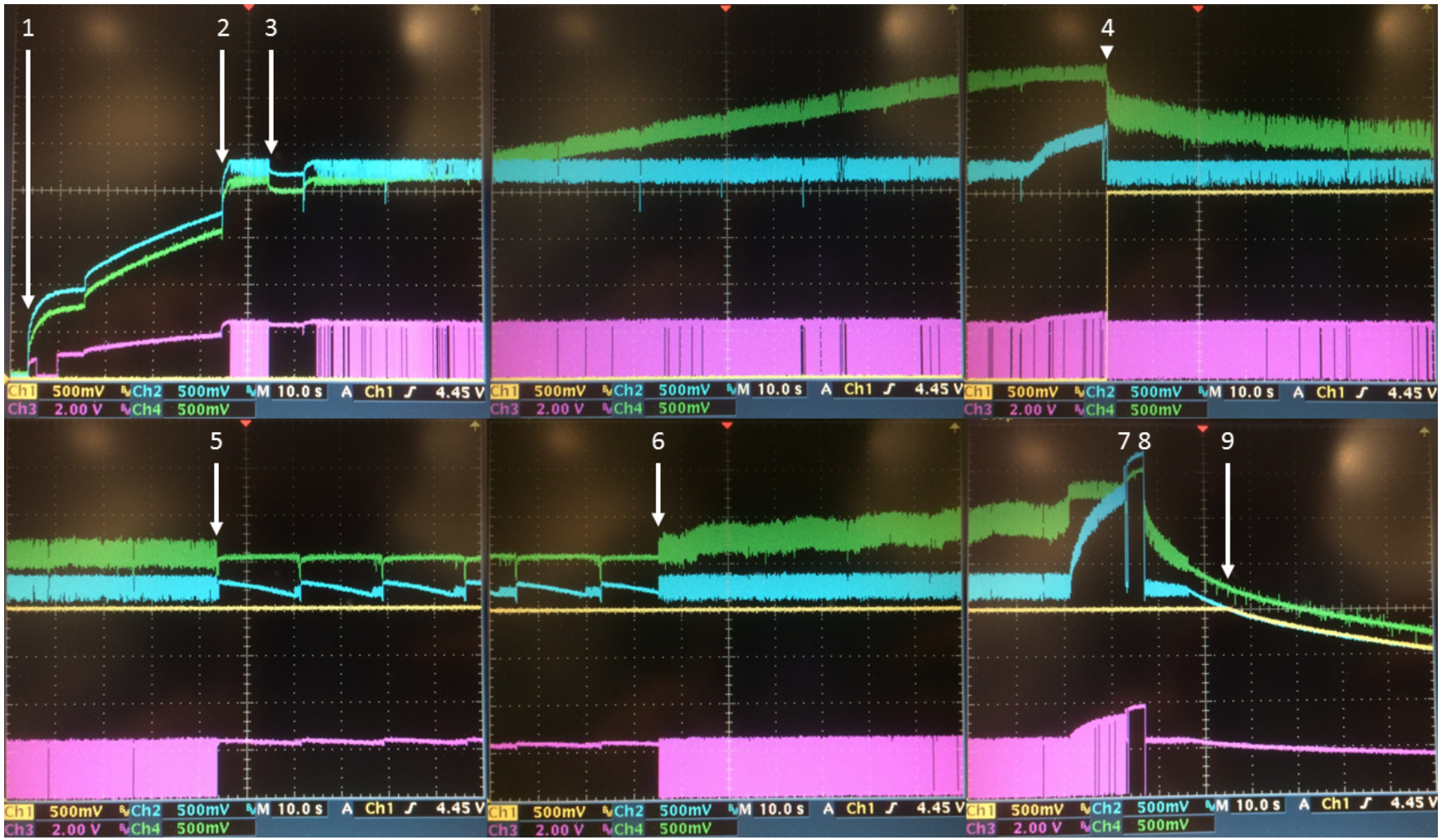


Figure 3-11: Supercapacitor-powered system operation for 1-mA load. 2-V output (yellow, channel 1), V_{stor} (cyan, channel 2), supercapacitor charger shutdown signal (pink, channel 3), V_{sc} (green, channel 4).

turned on yet to even be affected. After V_{stor} turns on, the state machine allows the supercapacitor discharger to prevent V_{stor} from falling too low for the load during the MPPT's open-circuit voltage sampling. In an integrated design, the best solution would be to use a fast enough circuit with a low solar-cell-disconnection time such that V_{stor} would not fall dramatically for the expected loads.

The input power at point 5 is high enough to power the load, but not high enough to increase V_{stor} enough to charge the supercapacitor, as shown by channel 3 remaining high. However, during this period, V_{sc} is seen to drop momentarily several times, representing the discharger maintaining V_{stor} high enough to power the load when the MPPT controller disconnects and samples the solar cell open-circuit voltage.

Lastly, at point 7, the charger shutdown signal is high, indicating that the supercapacitor should not be charging because it had been fully charged already. However, the waveform demonstrates how V_{sc} increases regardless. This occurs because V_{stor} is receiving a very large excess of input power, and the supercapacitor charges through the diode. This can be solved by using a precision shunt regulator in the integrated circuit to dissipate unnecessary power when the supercapacitor is fully charged. A shunt regulator is preferred to turning off or tuning the MPPT algorithm in order to keep control components modular and simple.

Overall, this plot illustrates how the designed topology is able to maintain the highest possible amount of energy in a supercapacitor while allowing it to be efficiently accessed in moments of low harvested energy. The system maintains a fixed 2.0-V output during operation, until the supercapacitor and harvested power are no longer high enough to power the load.

3.2.4 Weight Analysis

As the entire system was developed around weight minimization, an approximation of the total weight is important. Table 3.4 summarizes the approximate weights of the major components in an integrated solution. Several of the components used in the discrete system can be fully integrated. In particular, many of the bypass capacitors were used because of long distances in the PCB layout, and the voltage doubler's

capacitor and start-up diode can also be integrated at higher operating frequencies. One aspect that was ignored in the discrete system is the power supply for the digital controls. This will consist of an LDO powered by V_{stor}, which will likely require a discrete 100-nF 0201 bypass capacitor. Another 100-nF capacitor will be used in parallel with the supercapacitor. The 4.7-μF capacitors will be used for the solar cell boost converter input and for the 2.0-V load. The 22-μF capacitor will be used on V_{stor} and the 100-μH inductor for the switching converters. The packaged ASIC is estimated to be 33 mg based on the weight of the BQ25504 MPPT IC that was used. The flexboard and the solder are estimated to be 20 mg. In total, the system is estimated to be approximately 162 mg.

3.2.5 Design Discussion

Several key design tradeoffs and characteristics of the system should be noted. Firstly, placing the supercapacitor at V_{stor} versus maintaining the supercapacitor at a higher voltage as in this system resulted in different charging times. When using the solar cell model's current source at 5 mA, this system completed cold-start in 42 s and took an additional 58 s to charge the supercapacitor up to 3.3 V. The system with a supercapacitor on V_{stor} takes 50 s to complete cold-start but only an additional 21 s to charge up to 3.3 V. Cold-start is faster in this system because the supercapacitor

Component	**Footprint**	**Mass (mg)**	**Quantity**	**Total Mass (mg)**
solar cell		35	1	35
100-nF cap.	0201	1	2	2
4.7-μF cap.	0201	1	2	2
22-μF cap.	0402	3.5	1	3.5
100-μH ind.	0603	6.9	1	6.9
supercap.		60	1	60
ASIC		33	1	33
Flexboard		20	1	20
Total				**162.4**

Table 3.4: Masses of main components in supercapacitor-powered system.

is not charged to the normal operation threshold before the BQ25504 chip begins normal operation, but it takes longer in normal operation because the voltage doubler introduces a large inefficiency into the power path. When placing the supercapacitor at V_{stor}, the boost converter and supercapacitor charging losses are the only sources of inefficiencies.

Another important note is that the discrete system did not demonstrate inductor-sharing; the BQ25504 chip was provided with its own 22-μH inductor, while the buck discharger used a separate 1-mH inductor. This was done in order to use a separate MPPT IC and because inductor-sharing has been previously demonstrated in several works [7, 47, 51, 53].

Furthermore, the supercapacitor datasheet indicates that charging the supercapacitor with a large voltage ripple may decrease its capacitance [52]. This effect is largely dependent on the amount of harvested power from the solar cell.

This design also displays a few sensitivities. A fast discharger and a slow comparator on V_{stor} could cause V_{stor} to charge so high before the comparator detects it that it can turn the charger on. This is essentially inefficiently passing energy back and forth to the supercapacitor. This could potentially cause instability issues as well. However, a simple solution would be the incorporate the charger into the state machine to prevent the charger from turning on when the discharger is on. Also, as previously stated, the supercapacitor is extremely sensitive to frequency and discharge current. The benefit of using a supercapacitor is that it can be used for other applications requiring a high power-density source at a higher voltage (e.g. LEDs), and that this system is highly efficient for very short demands at the load. Lastly, careful attention must be paid to the order in which the FETs of the buck converter are turned on. The PFET must be turned on first. Otherwise, the inductor will initially begin to charge backwards and cause a drop in V_{stor} when turning the buck converter on.

Several improvements can also be made to the system. In particular, a buck converter discharger with a different controller may be used to match the supercapacitor charge state and the load demands. As was previously mentioned, the supercapacitor discharger at a certain point during testing switched on and did not turn off,

indicating that the 90% duty cycle was not high enough to recharge V_{stor} past the threshold. A different controller could address that problem by increasing the duty cycle. Furthermore, instead of using a doubler charge pump, a 3/2 charge pump could be more efficient. Since V_{sc} only goes as high as 3.3 V and charging begins when V_{stor} is approximately 2.3 V, this provides less of a difference between the charger's output and gained input.

Overall, the discrete implementation of the supercapacitor design functions well as a source-independent energy storage and power management system while maintaining a low weight of approximately 162 mg.

3.3 Battery-Based System

Another possible system is a battery-powered system. Rechargeable batteries charged by harvested energy allow for the high energy density of batteries without having to replace the system each time the batteries are depleted. This section describes the design and results of the proposed system. The schematic of the battery-powered system is shown in Figure 3-12.

3.3.1 Battery Performance Tests

Rechargeable Cymbet CBC050 batteries were chosen for this system because of their very light weight of 16 mg each. However, the batteries have a capacity of 50 μAh, which could have proven problematic at higher discharge rates. In order to support as high a load as possible, the batteries were cycle-tested to determine their behavior at various C-rates. Battery cycle-tests consisted of charging a single fresh CBC050 battery with a 4.1-V source, as per the datasheet, until the charging current into the battery reached 10 μA [13]. Then, a constant current load was switched on, until the voltage on the battery reached a minimum discharge voltage threshold. The process was repeated a total of 50 times with the same discharge current. Thirteen cycle-tests were completed for loads of 100 μA to 1.3 mA spaced at intervals of 100 μA. Appendix A provides clearer individual plots for each of the tests. Figure 3-13 shows

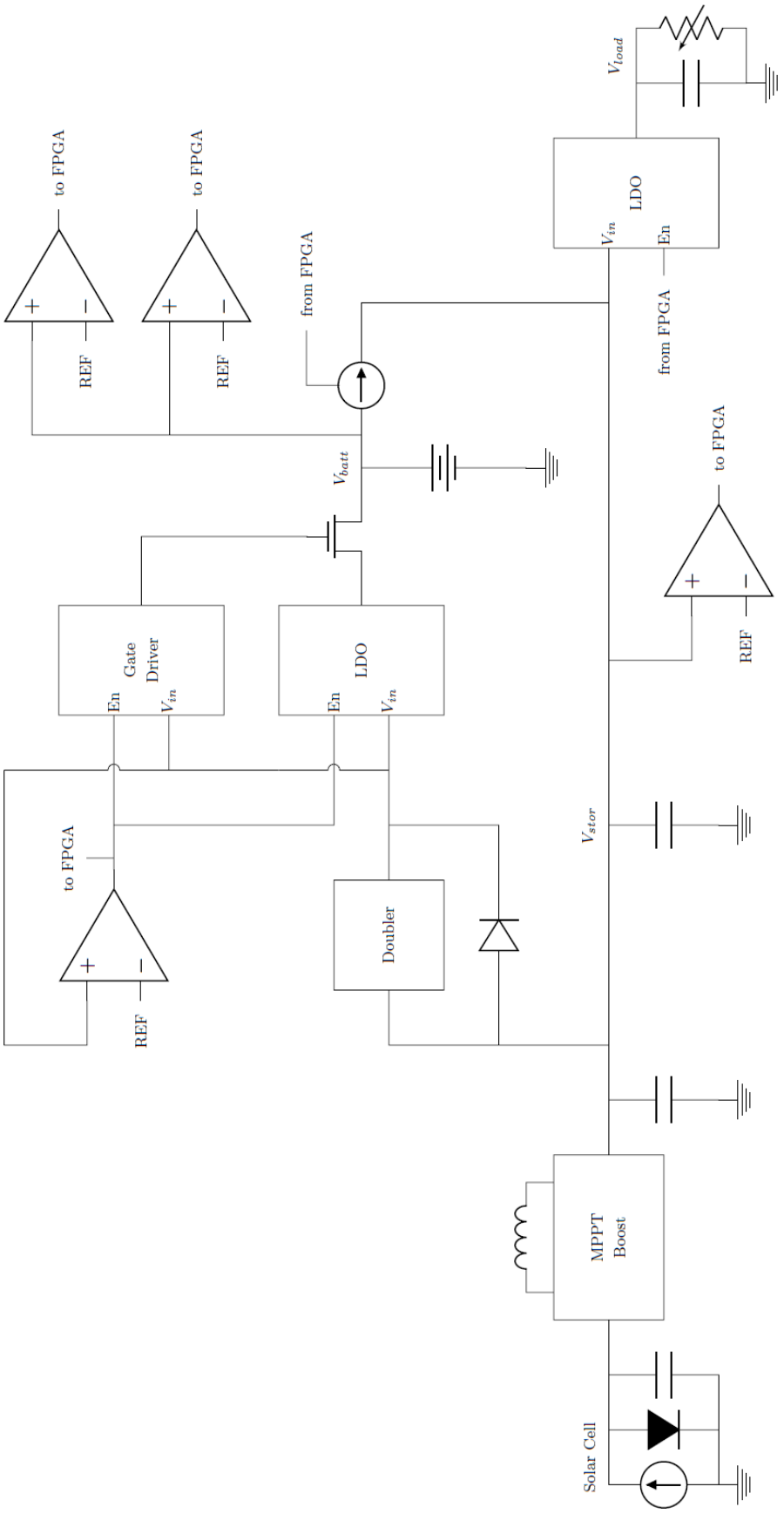


Figure 3-12: Schematic of battery-powered system.

the results of all 13 tests laid together. Figure 3-13a shows the normalized amount of time it took for the batteries to discharge for each cycle; 3-13b shows the normalized amount of work the battery completed over the discharge cycle; 3-13c shows the normalized average output power of the battery during the cycle, which is simply the work divided by the discharge time for a given cycle. All curves are normalized to the value of the initial discharge cycle. The curves for 100-μA to 900-μA discharge currents are represented as thin, black lines. These figures highlight how the behavior changes for discharge currents of 1.1 mA and above, suggesting 1 mA to be a safe limit on the maximum discharge rate. As can be seen, the curves for the 1-mA discharge are similar to those less than 1 mA, following the general trend of a gradual decrease over cycles. The curves for a discharge current of 1.1 mA began to show inconsistent behaviors starting at about cycle 33. The curves for a discharge current of 1.2 mA were much lower than the others. Finally, the curves for a discharge current of 1.3 mA began to increase after about 30 cycles. These last three cycles-tests therefore indicated the batteries were likely degrading from the high output current levels.

To further illustrate the degradation behaviors, Figure 3-14 illustrates the minimum normalized values among the 50 discharge cycles as a function of the discharge current. Figures 3-14a and 3-14b show the 1-mA discharge rate to perform around the knee of the curves, whereas Figure 3-14c shows an approximately linear decrease in minimum normalized average output power over discharge current.

Figures 3-15 and 3-16 show the same curves as Figure 3-13 but with actual values as opposed to normalized ones. Figure 3-15a also illustrates the initial battery resistance. The initial battery resistance is determined as the apparent initial discharge resistance from a Thevenin equivalent model of the battery, where the voltage source is 3.8 V, the output voltage according to the datasheet, and the resistance is determined as

$$R_o = \frac{(3.8\,V) - V_{batt,o}}{I_{load}} \tag{3.3}$$

where R_o is the initial battery resistance, $V_{batt,o}$ is the initial battery discharge voltage, and I_{load} is the discharge load current. This curve is useful in developing an

approximate Thevenin model of the battery.

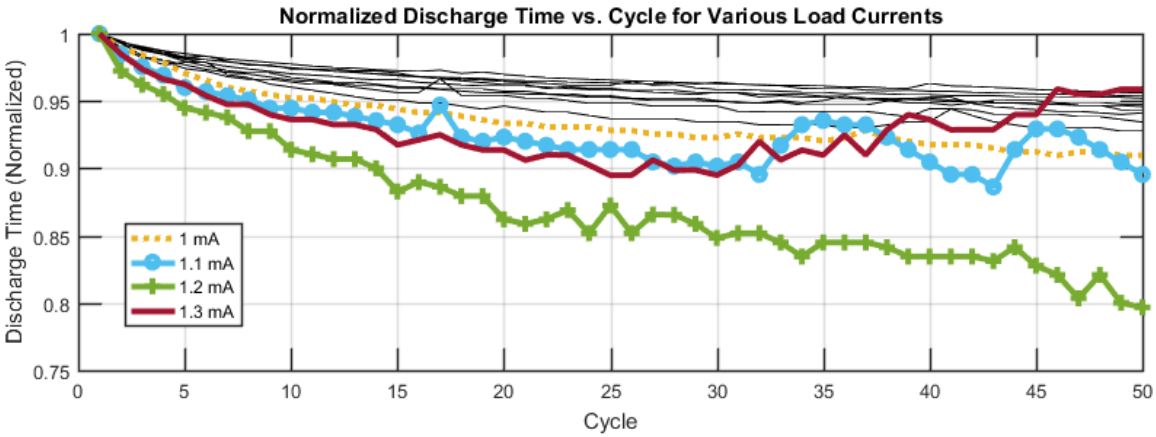
Overall, these tests suggest that by maintaining the discharge current to within 1 mA per battery, or a discharge rate of 20C, the battery could reliably source just under 3 mW of average power for at least 50 cycles, and likely more. This is therefore chosen as the maximum operating current for the batteries for the rest of the design.

3.3.2 Charger

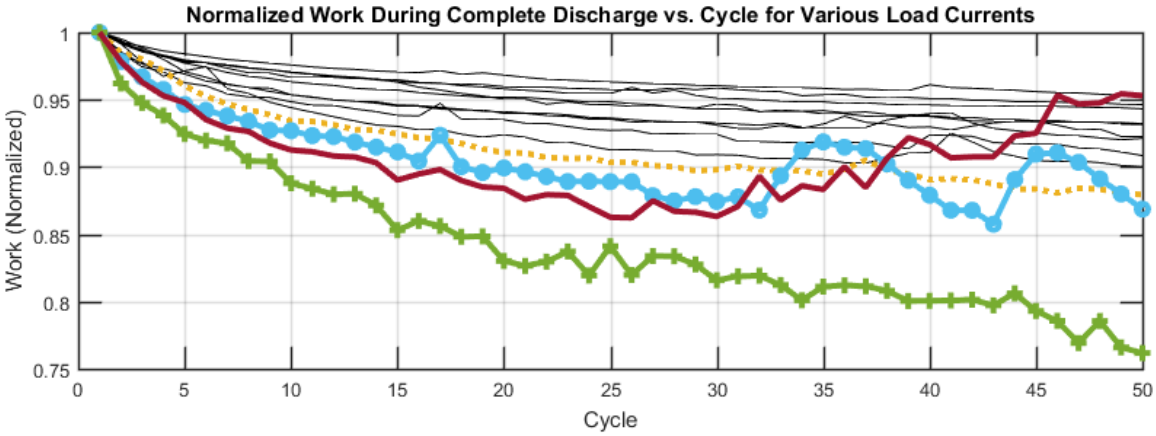
The charger used in this system is shown to the left of the battery at the V_{batt} node in Figure 3-12. Since the CBC050 batteries used must be charged with a constant 4.1-V voltage source, a simple voltage doubler could not be used as in the supercapacitor-powered system. Rather, a voltage doubler was attached to a 4.1-V LDO in order to provide a constant voltage output. An NFET was then attached to the output of the LDO in order to create a high impedance switch with low leakage when the NFET was turned off. A gate driver IC was used to bring the NFET gate high when turning the switch on, powered by the doubled V_{stor} voltage.

The battery charger was tested similarly to the supercapacitor charger. A current source was attached to V_{stor} and one or more batteries were attached to the output of the charger. Figure 3-17 shows the result of using a 600-μA current source limited at 2.5 V. As the batteries charged further, their current draw decreased, meaning the current draw into the charger also decreased. At a certain point, the charger began to draw less than 600 μA and the current source railed to 2.5 V. This is shown in Figure 3-17 when the current into V_{stor} begins to fall. For comparison, the current draw of a single battery attached to a 4.1-V source is also shown. While the battery draw eventually approached near-zero current draw, the charger did not, indicating a quiescent current draw around 180 μA while the charger was on. This could be lowered in an ASIC, but as the charger only operates in moments of excess input power, this current draw is less important than optimizing other parts of the design.

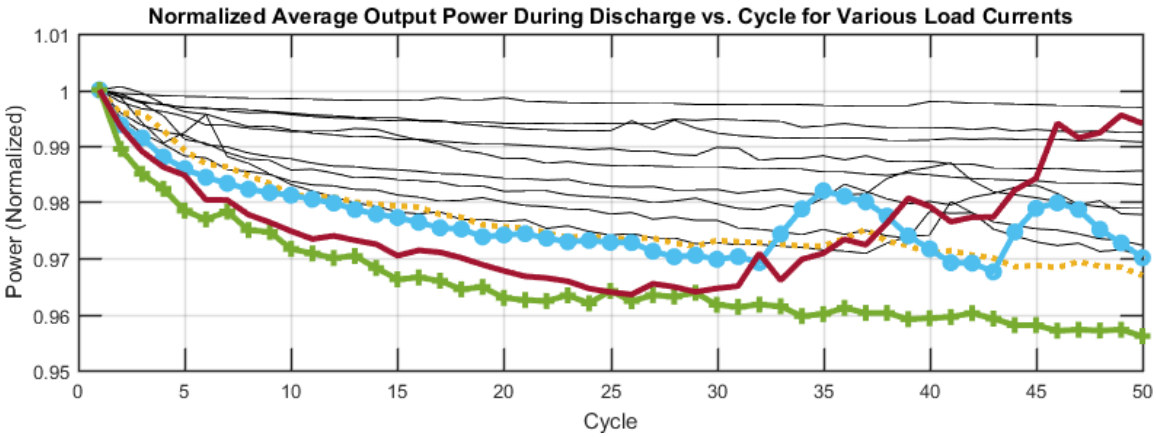
Figure 3-18 shows the operation of the charger charging 3 CBC050 batteries. Blips in the V_{batt} waveform indicate moments of charging the batteries. A higher input current into V_{stor}, would charge the batteries for longer periods at a time.



(a) Normalized discharge time.

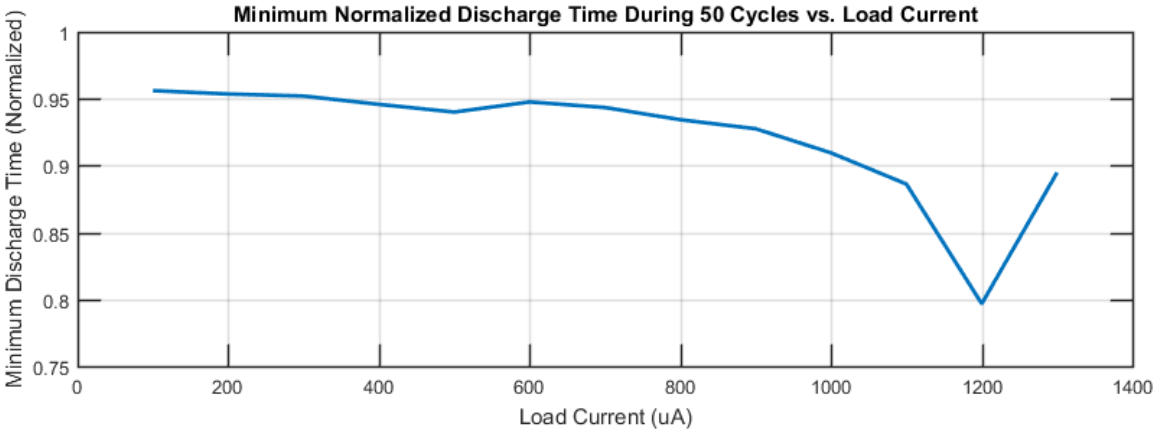


(b) Normalized work during complete discharge.

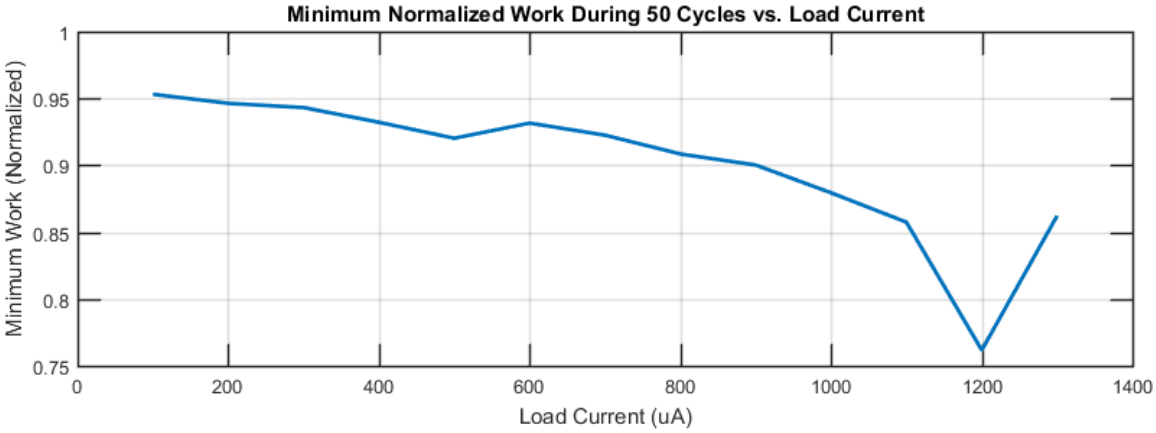


(c) Normalized average output power over complete discharge.

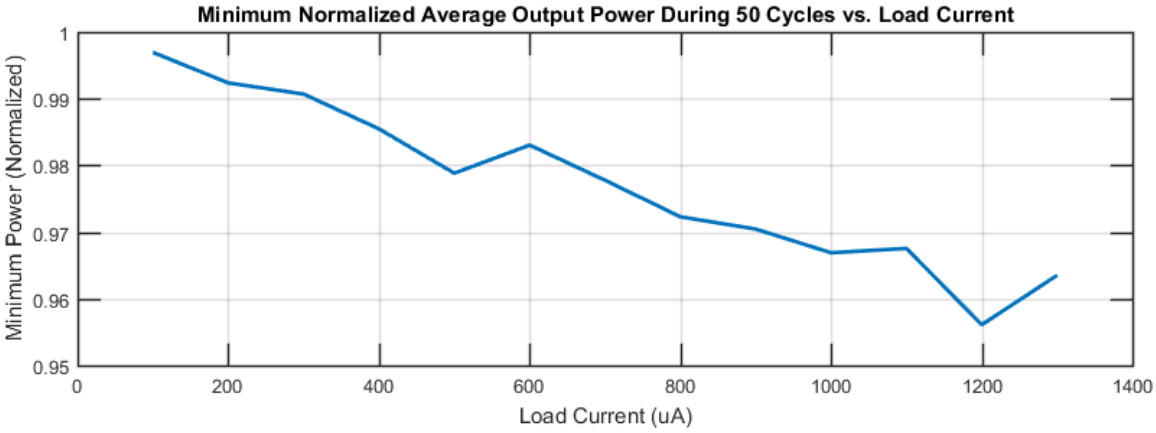
Figure 3-13: Results of 13 different cycle-tests comparing normalized discharge time, normalized work completed by battery, and normalized average output power over cycles. Thin, black curves represent discharge rates of 100 μA to 900 μA.



(a) Minimum normalized discharge time.

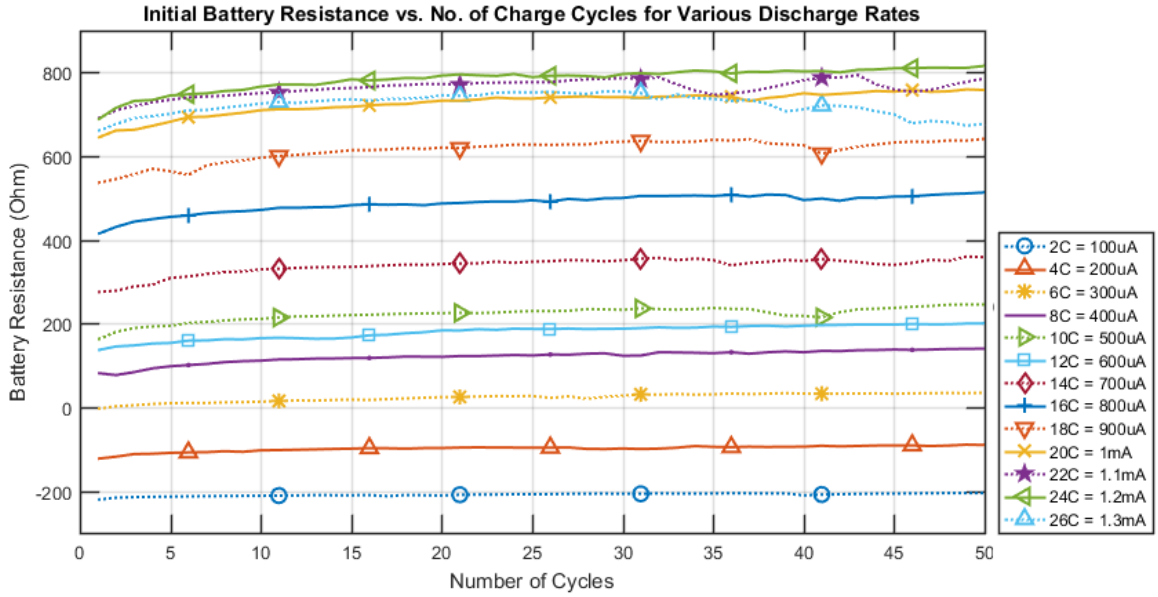


(b) Minimum normalized work during complete discharge.

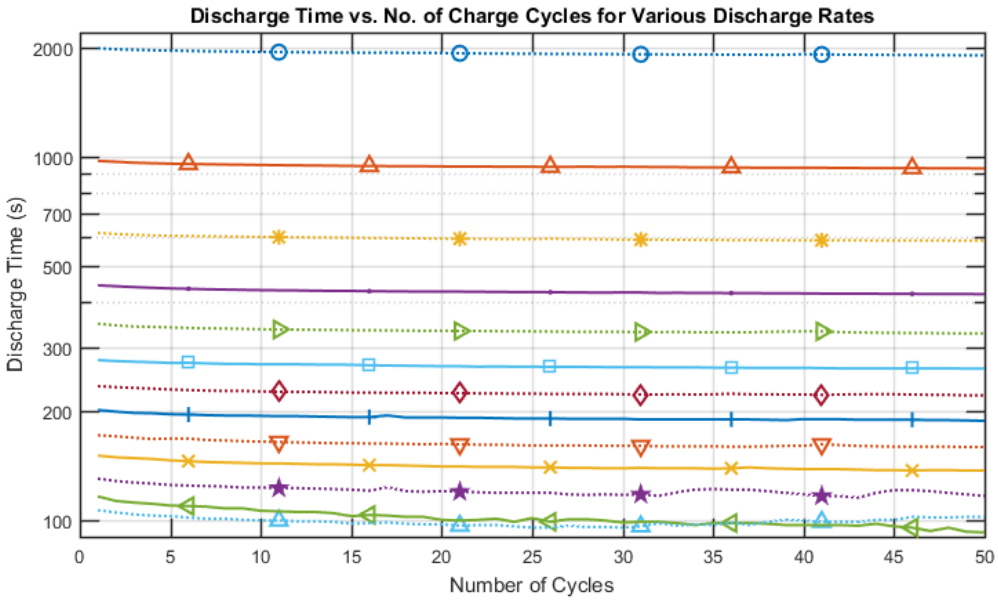


(c) Minimum normalized average output power over complete discharge.

Figure 3-14: Minimum normalized values during the 50 test cycles for each of the 13 discharge load currents from Figure 3-13.

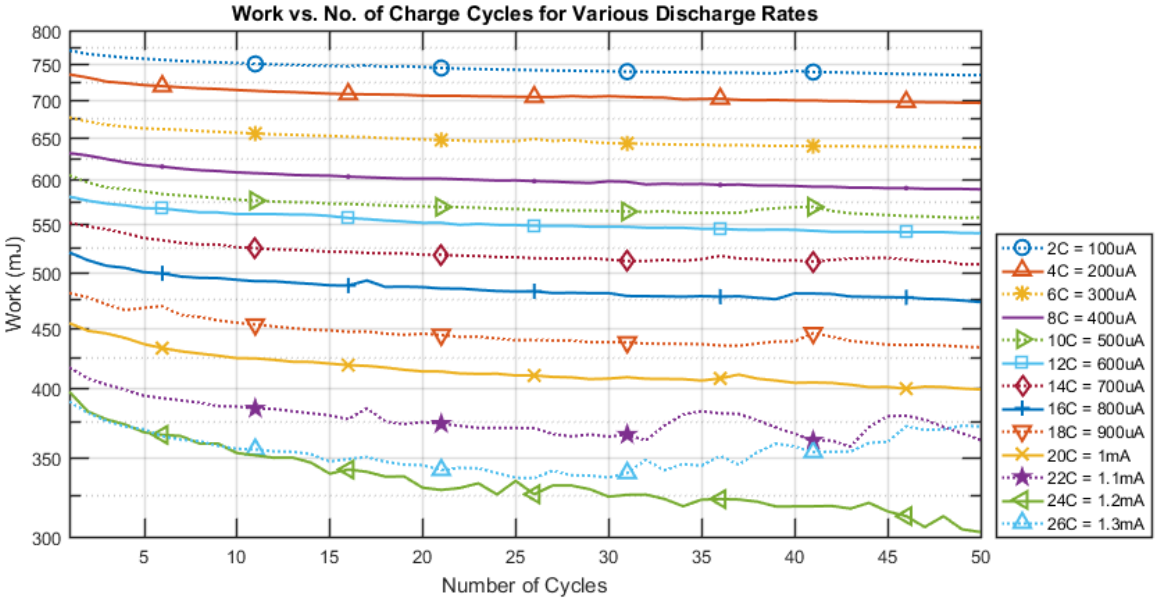


(a) Initial battery resistance.

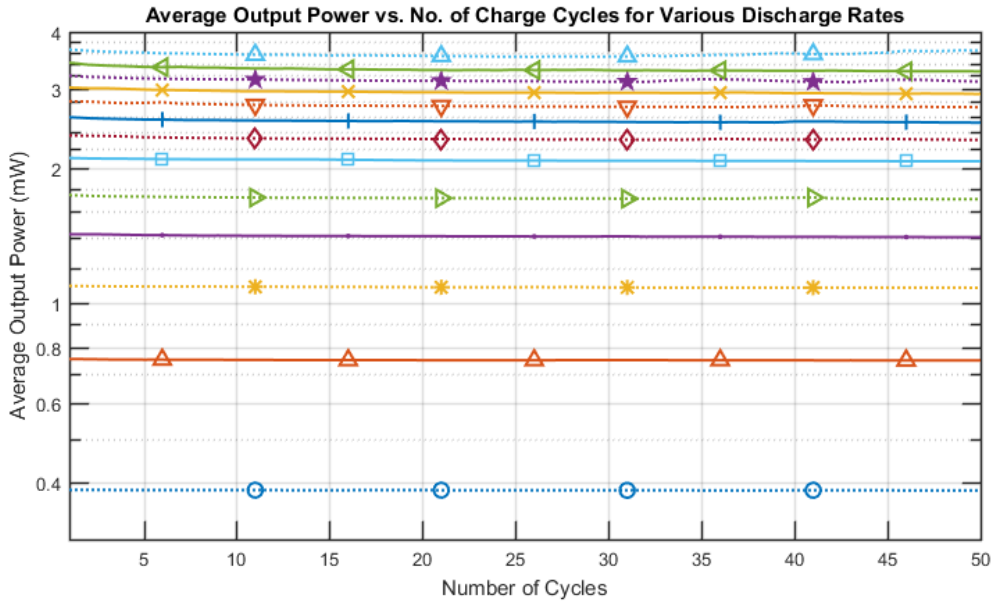


(b) Discharge time.

Figure 3-15: Actual values of initial battery resistance and discharge time for all 13 cycle-tests.



(a) Work during complete discharge.



(b) Average output power over complete discharge.

Figure 3-16: Actual work and average output power for all 13 cycle-tests.

3.3.3 Discharger

While the most energy efficient method of discharging the batteries to charge up V_{stor} would be to use a buck converter, this poses a few problems for the CBC050 batteries. As discussed, the biggest constraint in using a buck converter is that it requires an additional discrete inductor, adding more weight to the system. The previously proposed solution reuses the inductor from the solar harvester for the buck converter. This would require the batteries to fully support the load during this period of time, as the solar harvester would then be powered off. In order to remain within the weight of the supercapacitor in the previous section, up to 3 CBC050 batteries can be used. Each has a mass of 16 mg, for a total of 48 mg, while the

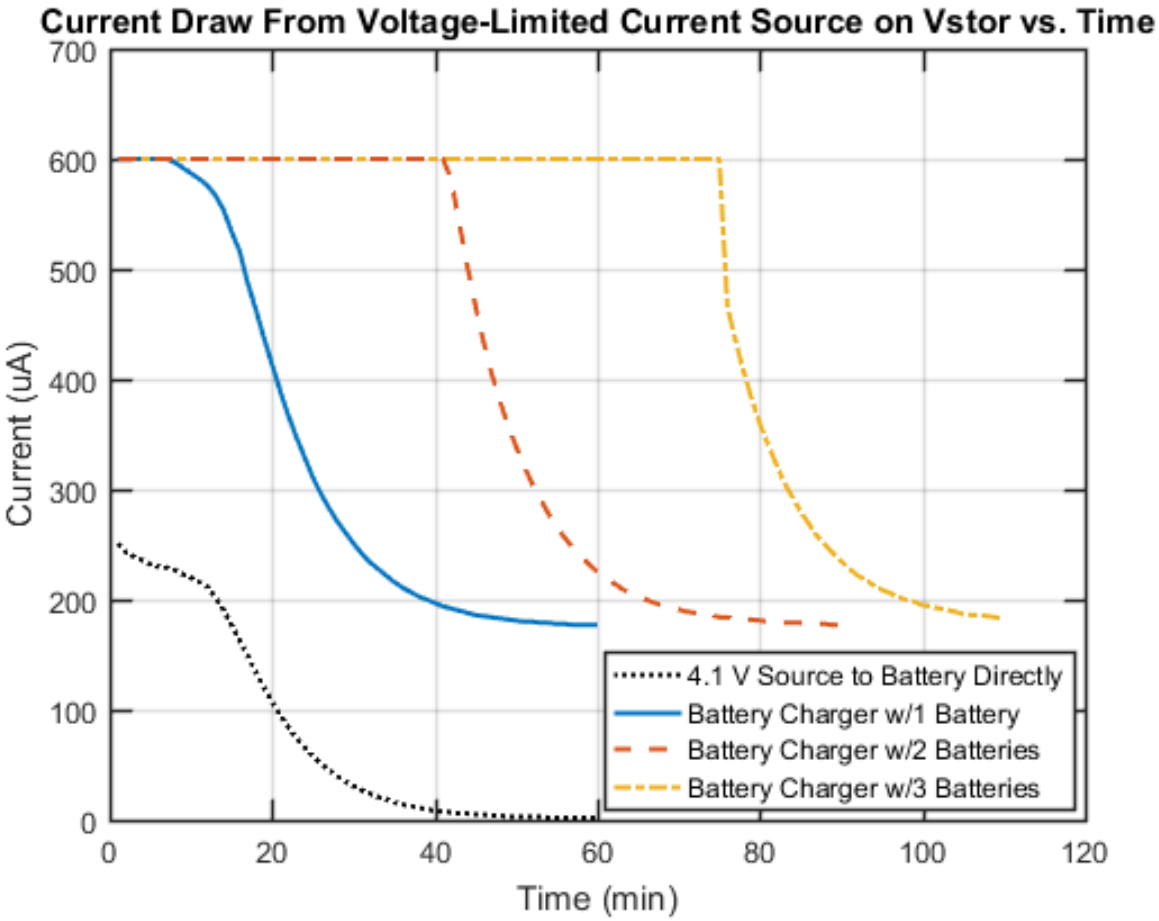


Figure 3-17: Current supplied into V_{stor} by 600-μA current source limited to 2.5 V for battery charger charging 1, 2, and 3 new CBC050 batteries. Normal charge with 4.1-V source shown for comparison.

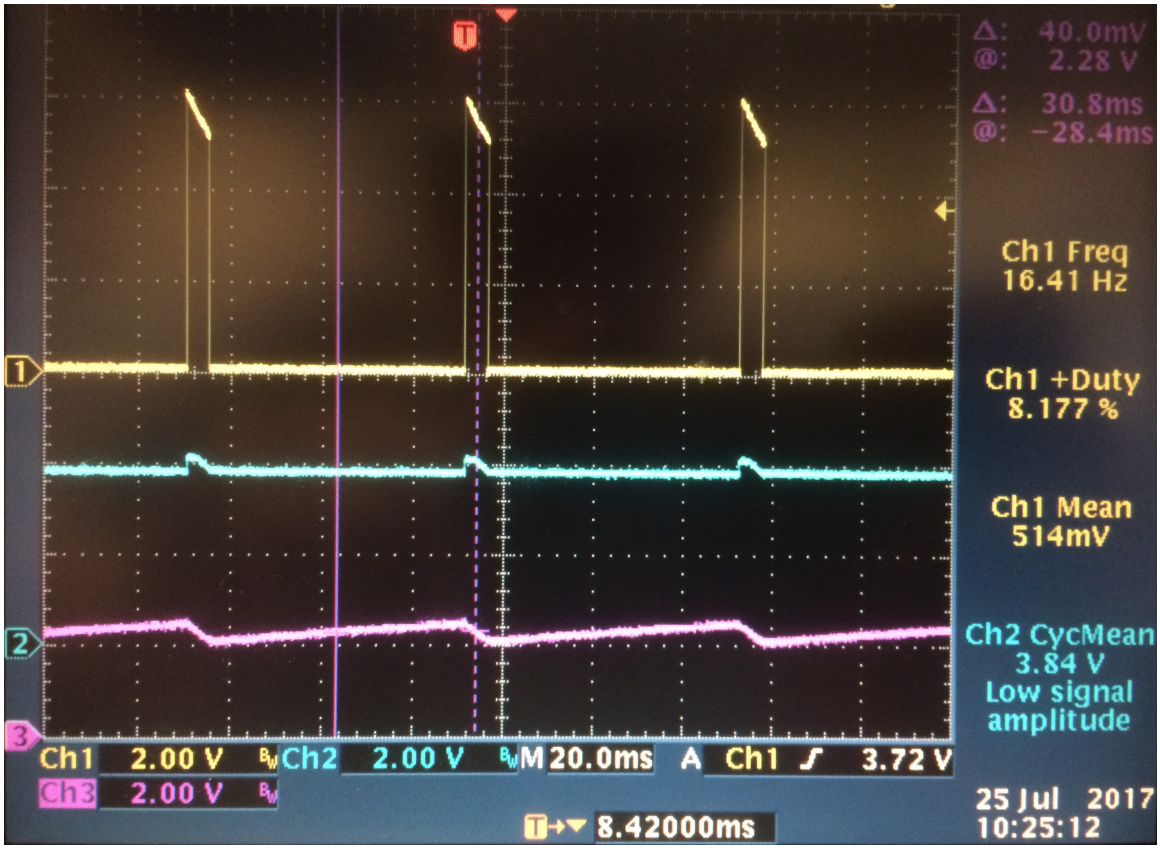


Figure 3-18: Typical charging waveform for battery charger charging 3 CBC050 batteries. Charge enable signal (yellow, channel 1), V_{batt} (cyan, channel 2), V_{stor} (pink, channel 3).

supercapacitor has a mass of 60 mg.

It is estimated that frequencies on the order of 1 MHz will be used for the switching converters in the ASIC, a balance between minimizing switching losses and minimizing inductor size. Figure 3-19a shows the schematic of batteries represented as a voltage source with a series resistance followed by an ideal buck converter. Estimating from Figure 3-15a, a single battery discharging at 1 mA demonstrates approximately 700 Ω of series resistance, so three parallel batteries could be represented as a 3.8-V source with 233 Ω of series resistance. Assuming a duty cycle of 50%, the inductor current appears as in Figure 3-20a. This shows that the batteries exceed the maximum safe discharge current of 3 mA, 1 mA per battery. In order to limit the current, a 340-Ω resistor is added in series with the batteries, as shown in Figure 3-19b. The maximum current through the battery will occur when the inductor appears as a short-circuit,

Inductance (μH)	22	47	100
Efficiency	69.7%	70.9%	74.0%

Table 3.5: Simulation results of battery with current-limiting resistor to buck converter at 75% duty cycle.

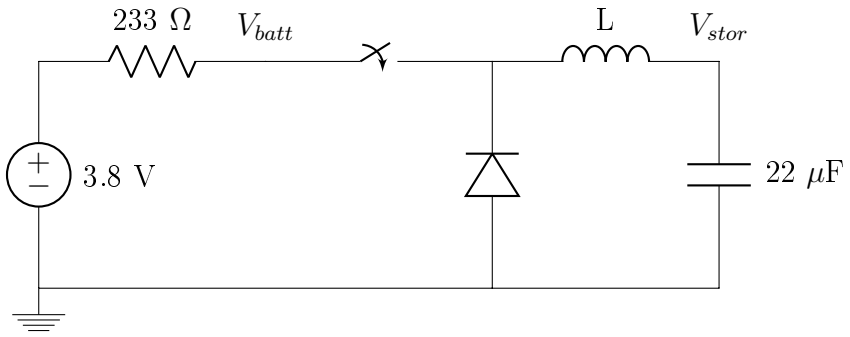
so 340 Ω is chosen as the limiting resistor when V_{stor} is 2.1 V. Figure 3-20b shows how the resistor safely limits the battery discharge current below 3 mA. Since the purpose of the buck converter is to charge V_{stor} above 2.1 V to a certain threshold and since the buck converter input will experience a large voltage drop across the battery's internal resistance and the current-limiting resistor, the actual duty cycle will likely need to be closer to 75% or higher. Table 3.5 shows efficiency results for a SPICE simulation with an ideal switch, diode, and inductor at a 75% duty cycle for three realistic inductances for the inductor to remain below approximately 10 mg. The efficiency is calculated as the average power into V_{stor} divided by the average power out of the V_{batt} node. This shows that in order to current-limit the batteries, a large price is paid in efficiency as compared to a buck converter's 100% theoretical efficiency. Note that using a more accurate current limiting circuit as opposed to a resistor will not improve efficiency in any way; it will simply maintain the maximum current closer to 3 mA as the battery's internal voltage varies.

One solution to low efficiency is to use a current monitor to control the buck converter's high side switch based on the inductor current. If the inductor current reaches the maximum allowable battery current draw, the switch could be turned off, at which point the battery stops providing current. Then, the inductor dissipates through a freewheeling diode or low-side switch until the current reaches a minimum value. The process is repeated until V_{stor} has been sufficiently charged. The problem with this system is that while the average buck converter's input current is less than its average output current (current into V_{stor} under ideal conditions), the instantaneous battery output current is the limiting factor. While the high-side switch is on, the current through the battery is equal to the inductor current. As a result, in order to

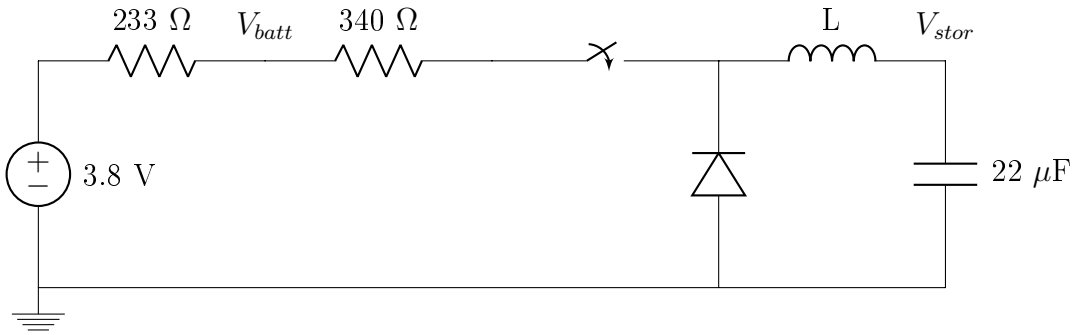
charge up V_{stor} the condition

$$I_{load} < \frac{I_{max} + I_{min}}{2} \tag{3.4}$$

exists, where I_{load} is the average load current on V_{stor}, I_{max} is the maximum battery and inductor current, and I_{min} is the minimum inductor current. As a result of having theoretically 100% efficiency, the maximum allowable load current is reduced. While I_{min} can be chosen close to I_{max}, the tradeoff is then the switching frequency becomes much higher. With an I_{max} of 3 mA, I_{min} of 2 mA, I_{load} of 2 mA, and a 100-μH inductor, simulation shows the switching frequency to be around 8 MHz. In this case, the maximum load current is 2.5 mA. In fact, the maximum load current will always be lower than the full 3 mA that 3 CBC050 batteries can provide.

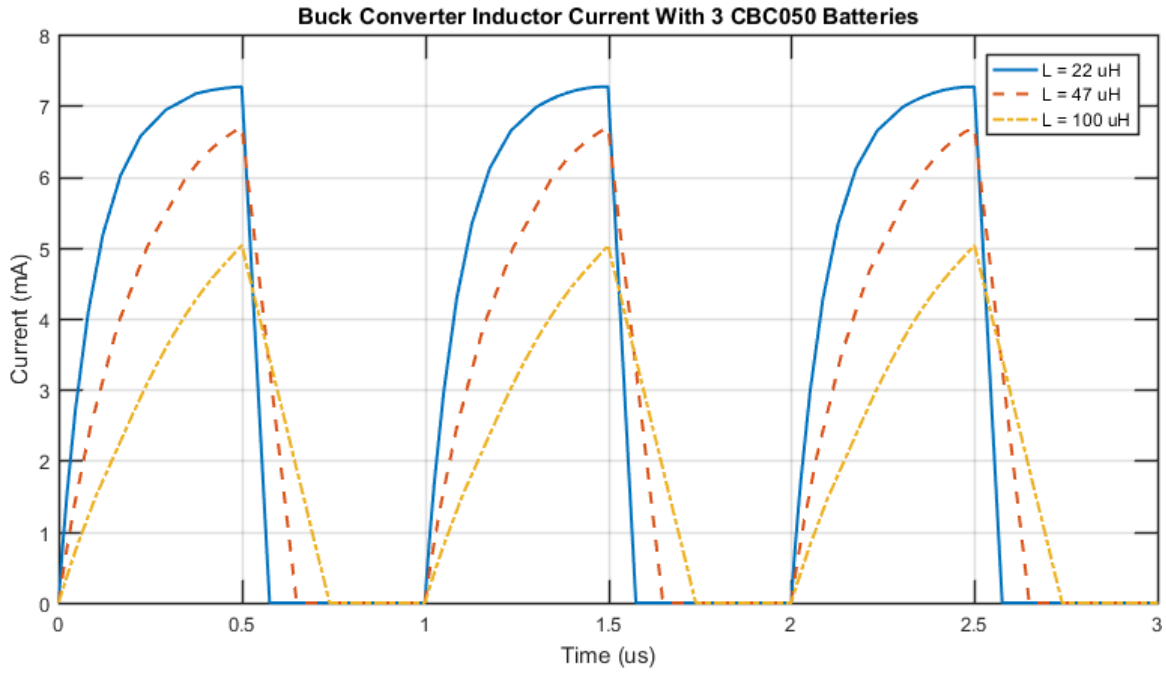


(a) Battery to buck converter.

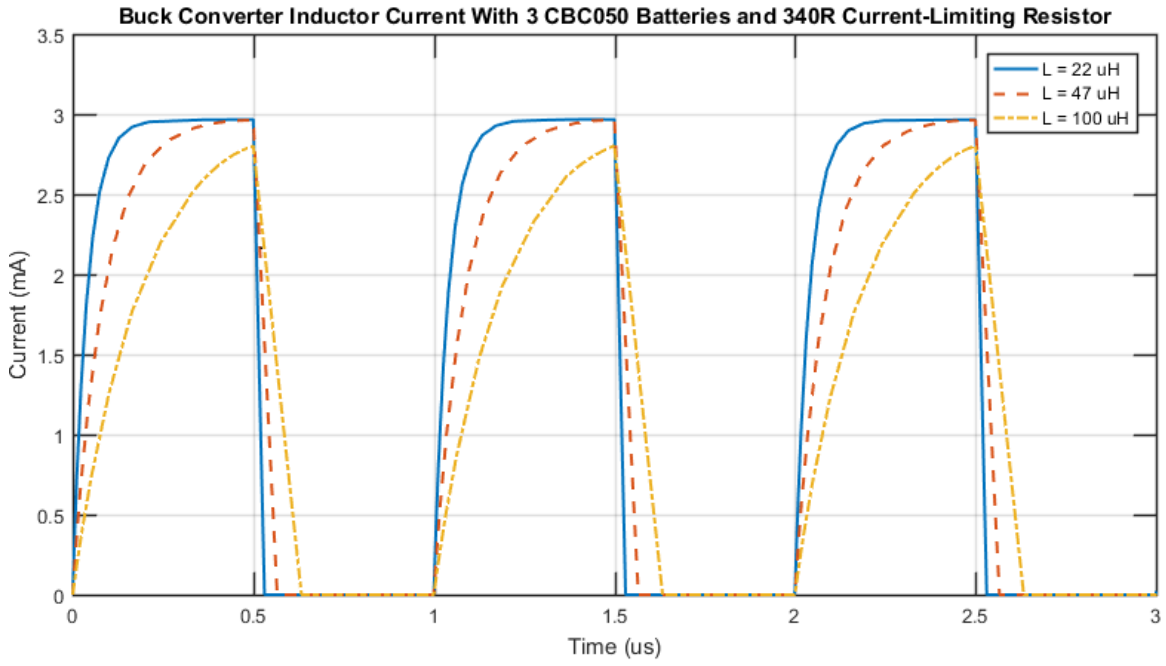


(b) Battery to buck converter with current-limiting resistor.

Figure 3-19: Schematic of battery to buck converter with and without a current-limiting resistor. 3.8-V source and 233-Ω resistor represent 3 CBC050 batteries.



(a) Inductor current of Figure 3-19a.



(b) Inductor current of Figure 3-19b.

Figure 3-20: Inductor currents of Figure 3-19 for various inductor values.

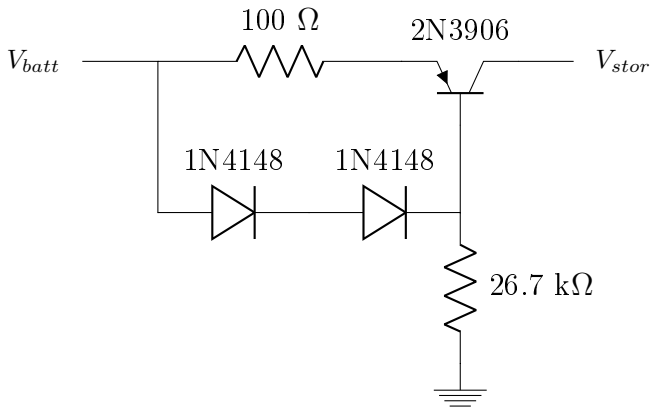


Figure 3-21: Current-source circuit used in physical implementation of discrete battery discharger.

An alternative is to simply use a current source circuit from the batteries to the V_{stor} node. Assuming 1 mA is drawn from each battery, a series resistance of 700 Ω suggests that V_{batt} during discharge will be 3.1 V, which is also suggested by the discharge profiles in the top-left plot of Figure A-10 in Appendix A. The ideal efficiency of the current source discharger is

$$\eta = \frac{V_{stor}}{V_{batt}} \tag{3.5}$$

where η is the efficiency. This is the efficiency of any ideal linear regulator. Input power is defined at the V_{batt} node, ignoring losses from the battery's internal resistance. In the case where V_{stor} is 2.1 V, the efficiency is $\frac{2.1\,V}{3.1\,V} = 67.7\%$. This is quite comparable to efficiencies of the buck converters with current limiters in Table 3.5. In fact, this is because when the buck converter current-limits, the system essentially reduces to a linear regulator. The quiescent losses associated with the current source can be quite small, whereas the buck converter can have much larger losses due to gate-drive capacitance, switch resistance, and inductor resistance. Therefore, it is very possible that a physical current source-discharger may be more efficient than a current-limited buck converter under these conditions. Methods to improve the buck converter efficiency by eliminating the current-limiting resistor are discussed in Section 3.3.6.

In the discrete implementation, the standard circuit shown in Figure 3-21 was used as a current source. Values were tuned such that approximately 3 mA of current were drawn from V_{batt}, for use with 3 CBC050 batteries. The exact current source circuit does not particularly matter, and a different circuit would certainly be used in an integrated CMOS implementation. In order to control the current source, a comparator monitored the V_{stor} node. An LTC1440 comparator was used with hysteresis to turn off at 2.09 V and turn on at 2.21 V. The comparator's output simply determined whether the current source was on or off, where a logic high turned off the current source and vice versa. In this way, the current source would charge up the V_{stor} capacitor to 2.21 V if it detected its voltage had fallen to 2.09 V.

To test this, 3 CBC050 batteries were placed at the discharger input. Figure 3-22 shows an oscilloscope screenshot for an I_{diff} of 1 mA for the designed I_{batt} of 3 mA

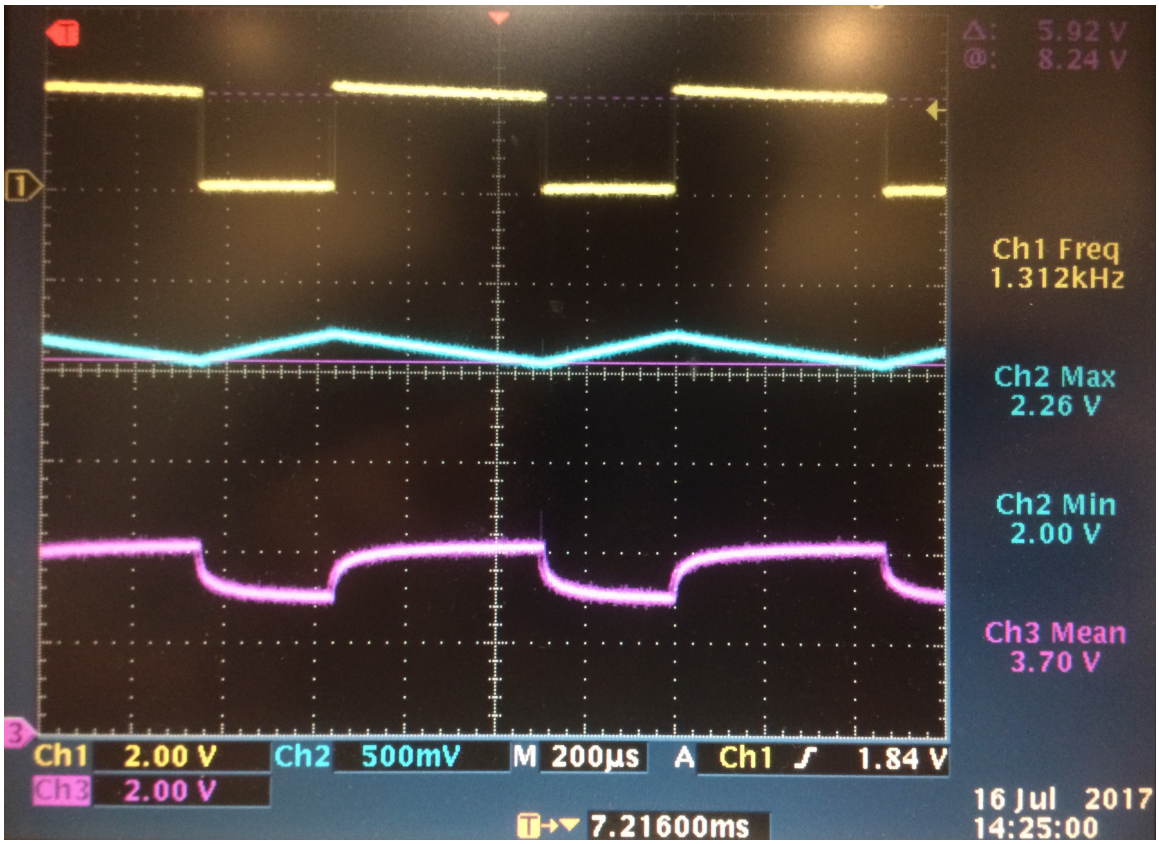


Figure 3-22: Constant-current discharger with 3 CBC050 batteries and controller. I_{diff} is 1 mA. V_{stor} comparator output (yellow, channel 1), V_{stor} (cyan, channel 2), V_{batt} (pink, channel 3).

using these batteries. I_{diff} is defined as

$$I_{diff} = I_{load} - I_{boost} \tag{3.6}$$

where I_{boost} is the input current from the MPPT boost converter solar harvester. I_{diff} is used in analyzing the battery discharger instead of I_{load} because the discharger does not reuse the inductor; therefore, the solar harvester continues sourcing power to V_{stor} even when the discharger is on. As expected, when the comparator on V_{stor} falls low causing the batteries to discharge, the V_{batt} voltage drops due to the batteries' internal resistance. When the comparator switches high, the battery voltage rises as it stops sourcing current. In order to protect the batteries from being over-depleted, another LTC1440 comparator was added at the V_{batt} node, comparing against 3.18 V. Each time the battery discharger shuts off, the FPGA controller waits 80 μs and then checks the V_{batt} comparator. If the comparator is low, it is determined that the batteries have been fully dissipated and the entire system shuts off. As a method to check for a low battery voltage, the open-circuit voltage is used instead of the discharging voltage because the latter depends heavily on the battery's source impedance which changes over time.

In the case that V_{stor} never reaches the 2.21-V threshold to turn on the V_{stor} comparator, it is possible for the battery to not exit a discharge phase to be checked and to deplete enough to be damaged. To address such problem, an LTC1540 comparator is added to monitor if V_{batt} falls below 2.36 V. If so, the discharger shuts off.

In order to understand the effects of the discharger on CBC050 batteries, cycle-tests using the discharger were completed. The discharger was designed for 3 CBC050 batteries, therefore discharging at approximately 3 mA. The batteries were charged using a 4.1-V source, and then discharged using the current source discharger for an I_{diff} of 1 mA. This was repeated 31 times. Then, the tests were repeated for an I_{diff} of 1.5 mA, 2 mA, 2.5 mA, and 1 mA. This was repeated three times in the stated order, for a total of 43 cycle-tests using the 3-mA discharger. The discharge curves for all cycle-tests with an I_{diff} of 1 mA are shown in Figure 3-23. The open-circuit maximum

voltage and the discharging minimum voltage represent the maximum and minimum of the V_{batt} curve as shown in Figure 3-22, respectively. These curves are sampled every 30 seconds. The SourceMeter voltage is an approximately averaged measurement of V_{batt} sampled every 400 ms, and it illustrates how V_{batt} drops dramatically after a critical point but rises back to around its nominal 3.8-V output after the discharger is shutoff by the control system. Figure 3-24 shows how the discharge time decreases over cycles. The 12 additional cycle-tests testing an I_{diff} of 1.5 mA, 2 mA, and 2.5 mA in Table 3.6 were conducted to show how the value of I_{diff} does not significantly affect the discharge time variation, but rather the number of cycles does. After 43 discharges, the 1-mA discharge time was still above 93% of its initial discharge time.

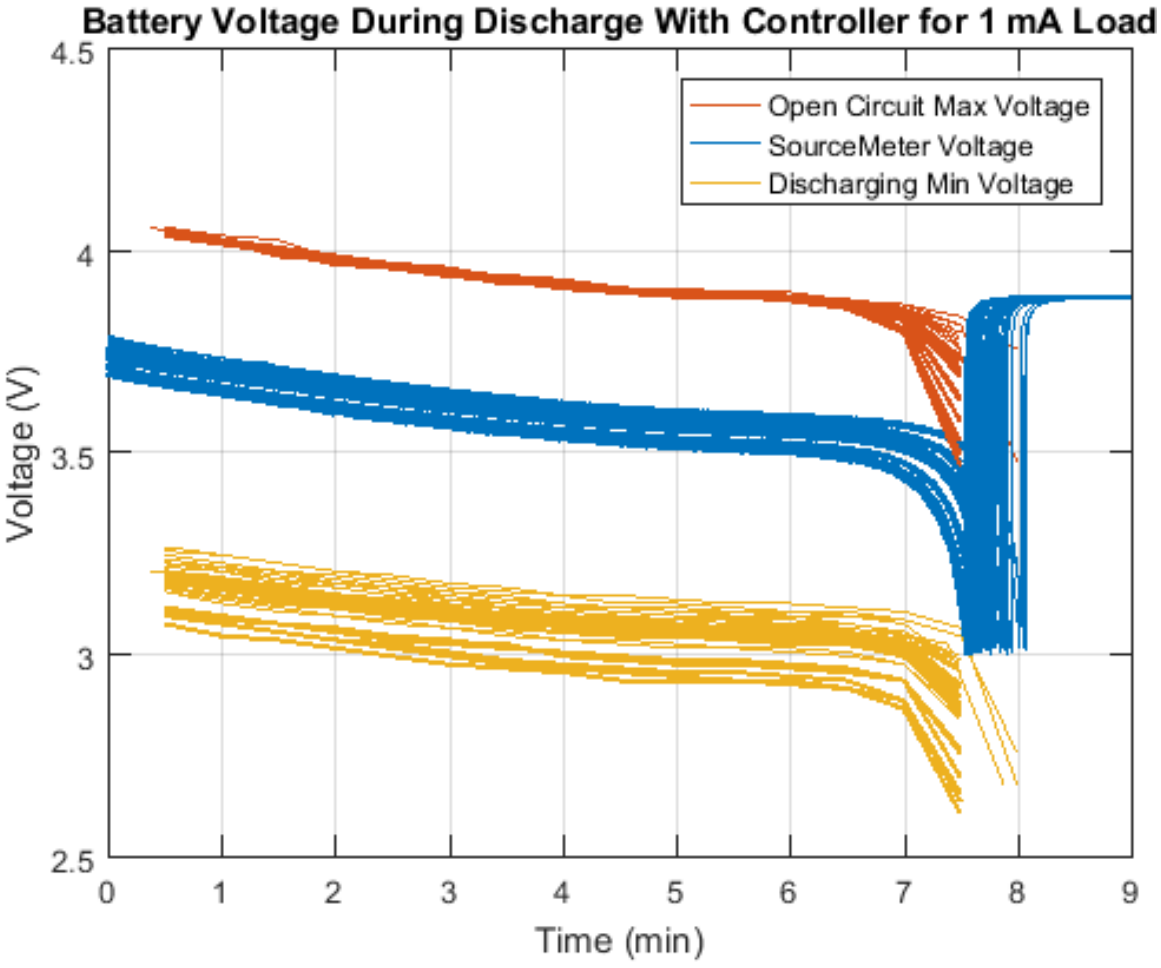


Figure 3-23: Open-circuit maximum voltage, voltage as measured by SourceMeter, and discharging minimum voltage during battery discharge over time with controller for 34 charge-discharge cycles. I_{diff} is 1 mA.

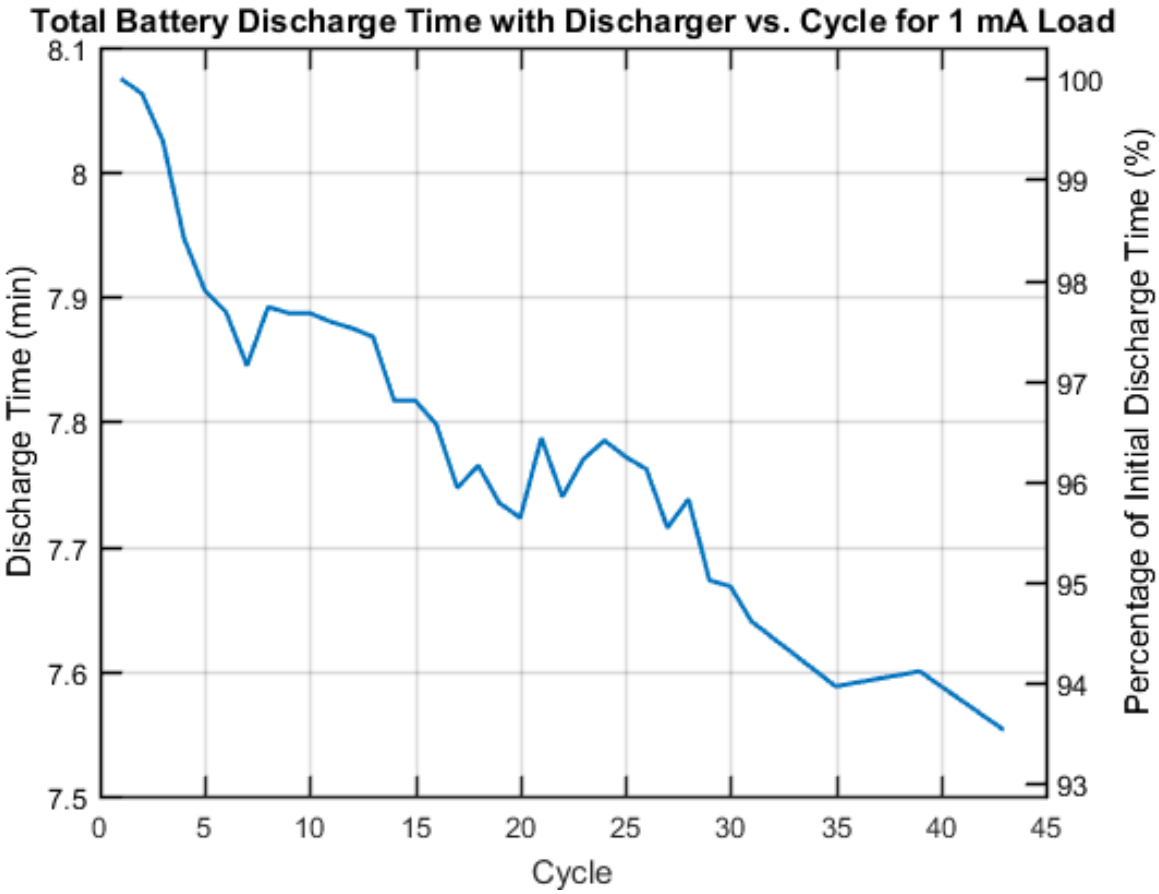


Figure 3-24: Discharge time for batteries at 1 mA I_{diff} with controller over 43 cycles. I_{diff} is 1.5 mA for cycles 32, 36, and 40; 2 mA for cycles 33, 37, and 41; and 2.5 mA for cycles 34, 38, and 42; these are not shown.

$\mathbf{I_{diff}}$ **(mA)**	**Time (min) <Cycle>**		
1.5	5.06 <32>	5.01 <36>	5.01 <40>
2.0	3.69 <33>	3.64 <37>	3.64 <41>
2.5	2.99 <34>	2.91 <38>	2.90 <42>

Table 3.6: Discharge time for batteries in same test as Figures 3-23 and 3-24, but for cycles where I_{diff} is not 1 mA; cycle numbers in brackets.

3.3.4 Complete System

After completing the charger and discharger for the battery-powered system, the entire controller was programmed into the FPGA. The state machine is shown in Figure 3-25. As with the supercapacitor-powered system, the battery-powered system first charged the battery sufficiently before turning on the load. In the discrete system,

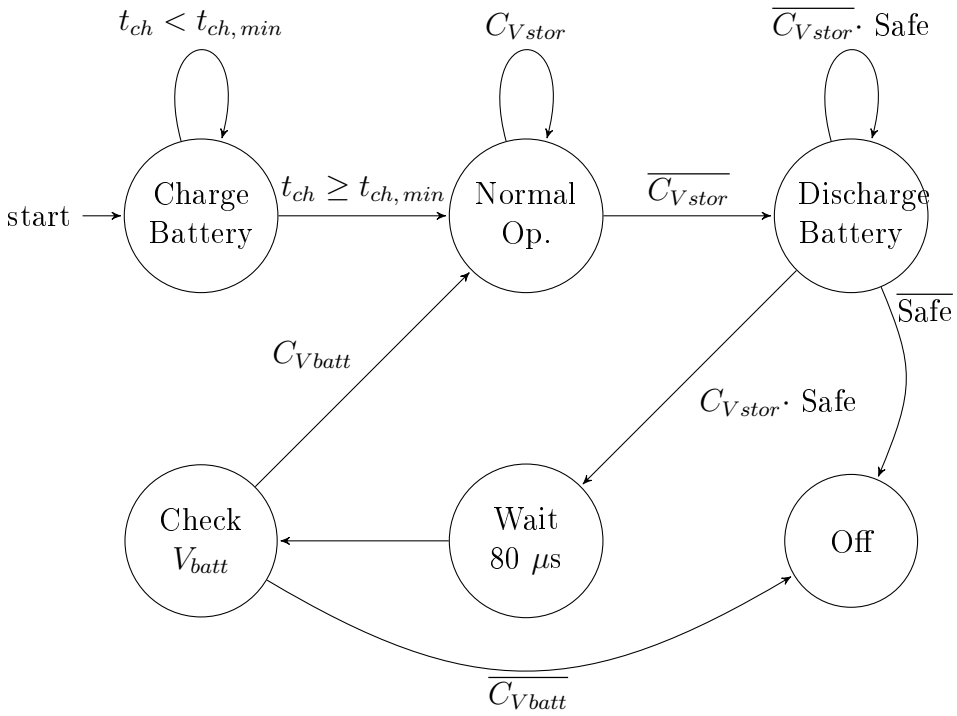


Figure 3-25: Finite state machine for battery-powered system where t_{ch} is time that battery has charged, $t_{ch,min}$ is minimum battery charge time before turning on 2-V output, C_{Vstor} is output of comparator on V_{stor}, C_{Vbatt} is output of LTC1440 comparator on V_{batt}, and Safe is output of LTC1540 comparator checking that battery discharger has not latched.

this was done by simply counting how long the battery-charging signal was on. After the battery was charged, the state machine switched to the controller described in the previous subsection, where the charger was separately governed by the circuitry shown in Figure 3-12. Unlike the supercapacitor-powered system, the battery-powered system had an "off" state in order to prevent damaging the batteries, whereas the supercapacitor-system did not as it is not damaged by low charge voltage.

The behavior of the state machine controlling the system is shown in Figure 3-26. The harvested power is represented as a current source into V_{stor}, rather than the BQ25504 IC. Before time (1), there is no current input into V_{stor}, and the system is off. At time (1), the current source turns on and sources 1 mA of current into V_{stor}, representing the solar harvester's operation. Between (1) and (2) the battery charger turns on and off depending on the voltage on V_{stor}, and the FPGA counts how long the battery has been charged. In Figure 3-26, for demonstration purposes, the

batteries are charged for 10 seconds before moving on to normal system operation. At time (2), the system FPGA determines the batteries have been charged for the equivalent of 10 seconds and enables the 2-V output. The LDO current draw is around 1.1 mA. This current draw in addition to the controls current is higher than the current being input by the current source. As a result, the system oscillates between discharging the battery and normal operation, as described in the previous subsection. At time (3), the current sourced into V_{stor} increases to 2 mA. This is an excess of power compared to the load, so the system oscillates between charging the battery and normal operation. At time (4), the current into V_{stor} becomes 0 mA, and the system again oscillates between discharging the battery and normal operation. As the batteries discharge, the battery voltage droop becomes apparent in Figure 3-26. At time (5), the state machine determines the batteries have been dissipated down to the set threshold, and the system shuts off, as seen in the drop of the 2-V load. Note that the 10-second charge time is not representative of what would be programmed in the integrated solution, and also explains the short duration of the batteries in Figure 3-26. Figure 3-17 demonstrates how in reality useable charge times for three batteries could be near an hour. In an ASIC design, a better approach would be to measure when the current into the batteries during charging drops below a certain

		States and Outputs				
Period	**V_{stor} Input Current (mA)**	**2.0-V Output Enabled**	**Normal Operation**	**Battery Charging**	**Battery Discharging**	**Off**
before (1)	0					X
(1) to (2)	1		X	X		
(2) to (3)	1	X	X		X	
(3) to (4)	2	X	X	X		
(4) to (5)	0	X	X		X	
(5) onward	0					X

Table 3.7: Input current into V_{stor} and resulting states and outputs for points in Figure 3-26.

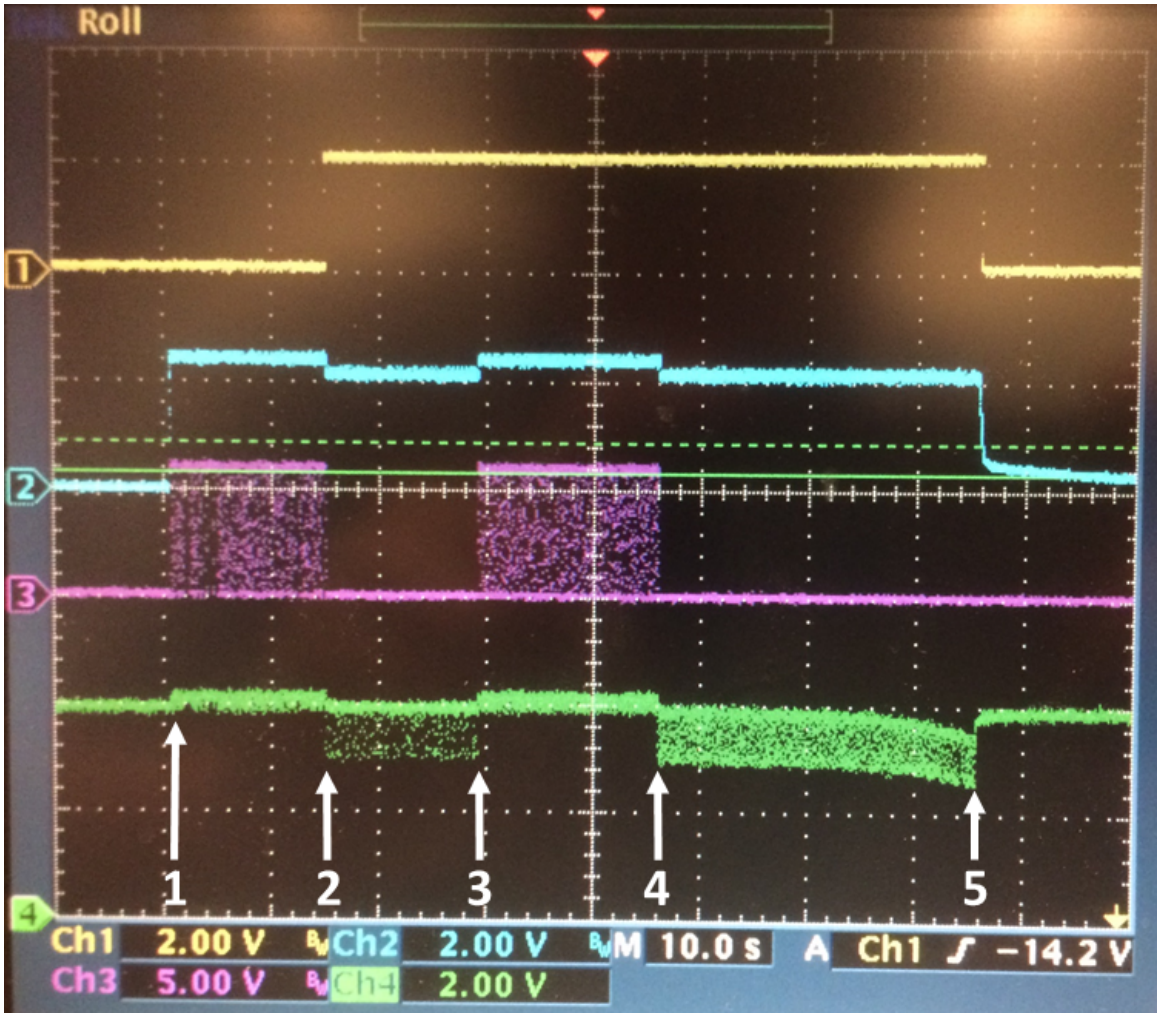


Figure 3-26: Battery-powered system operation for approximately 1-mA load with current source representing I_{diff}. 2-V output (yellow, channel 1), V_{stor} (cyan, channel 2), battery charger enabled signal (pink, channel 3), V_{batt} (green, channel 4).

threshold, such as 2 μA.

Following the demonstration of the complete control system, the current source into V_{stor} was replaced with the BQ25504 solar harvester IC and the solar cell model circuit. The results of this system are shown in Figure 3-27. The labeled points are as follows:

1. solar cell model's current source turns on at 3 mA;

2. battery charged enough according to timer, and 2.0-V load turns on;

3. solar cell model's current source changes to 1 mA;

4. solar cell model's current source changes to 2 mA;

5. solar cell model's current source shuts off;

6. system shuts off because batteries sufficiently depleted.

One benefit of this system is cold-start for the BQ25504 IC occurs very quickly because the capacitor on V_{stor} is very small compared to a supercapacitor and the energy storage component is not charged through the voltage doubler's diode.

Overall, this plot illustrates how the designed battery-powered topology, like the supercapacitor-powered system, is able to maintain the highest possible amount of energy in the battery. While it does not make use of a highly efficient discharger like the supercapacitor-powered system, it does allow the system to continue harvesting solar energy during moments of low solar energy or high load demands. This system therefore does not need the complex circuitry needed for inductor-sharing. It also operates with higher continuous load currents and lasts longer than the supercapacitor-based system.

3.3.5 Weight Analysis

A weight estimation was also developed for the battery-powered system. Table 3.8 summarizes the approximate weights of the major components in an integrated solution. Like the supercapacitor-based system, several of the components used in the discrete system can be fully integrated. As with the supercapacitor-based system, a 100-nF 0201 bypass capacitor will be needed for the control voltage rail that was ignored in the discrete system. Another will likely be needed for the input of the LDO in the battery charger. The 4.7-μF capacitors will be used for the solar cell boost converter input and for the 2.0-V load. The 22-μF capacitor will be used on V_{stor} and the 100-μH inductor for the switching converter. The packaged ASIC is estimated to be 33 mg, just like in the supercapacitor-powered system. In total, the system is estimated to be 150 mg.

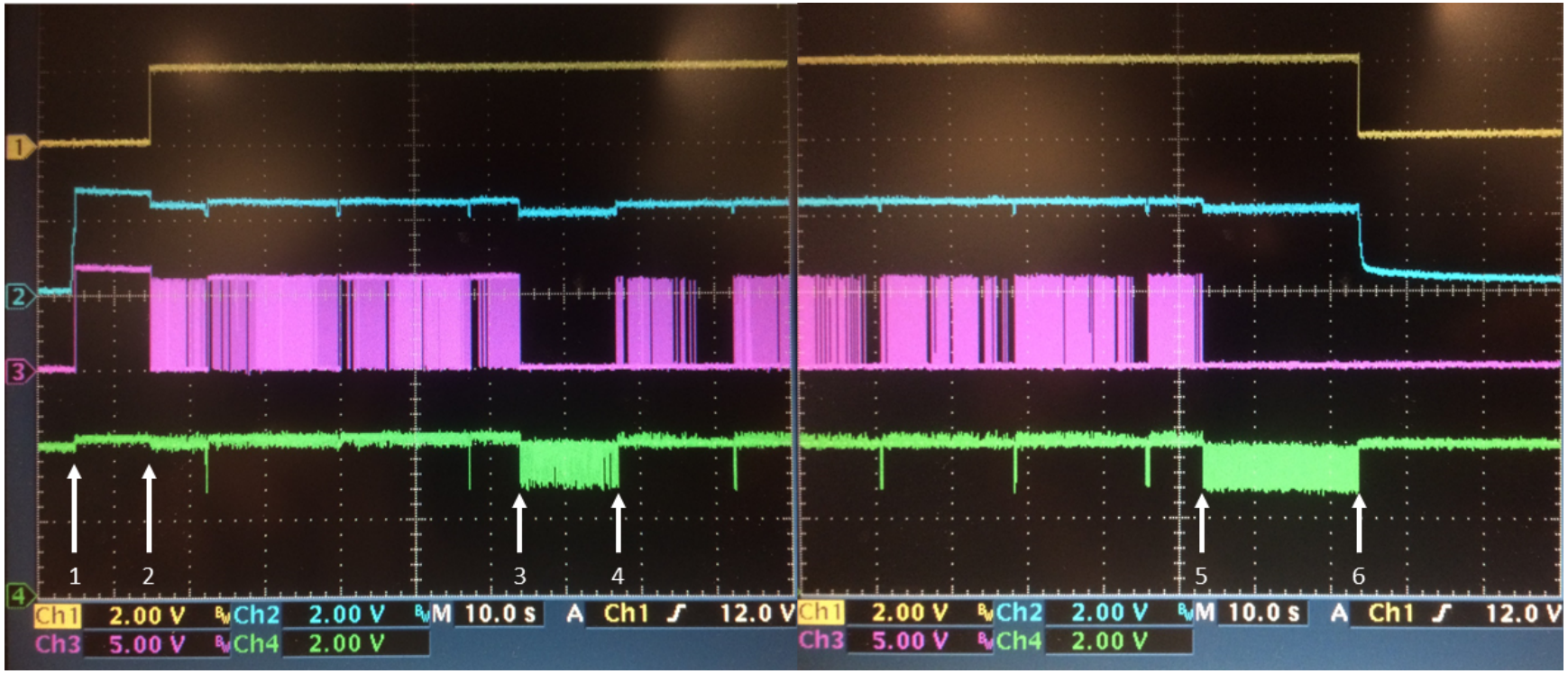


Figure 3-27: Battery-powered system operation for approximately 1-mA load with BQ25504. 2-V output (yellow, channel 1), V_{stor} (cyan, channel 2), battery charger enabled signal (pink, channel 3), V_{batt} (green, channel 4).

Component	Footprint	Mass (mg)	Quantity	Total Mass (mg)
solar cell		35	1	35
100-nF cap.	0201	1	2	2
4.7-μF cap.	0201	1	2	2
22-μF cap.	0402	3.5	1	3.5
100-μH ind.	0603	6.9	1	6.9
CBC050		16	3	48
ASIC		33	1	33
Flexboard		20	1	20
Total				**150.4**

Table 3.8: Masses of main components in battery-powered system.

3.3.6 Design Discussion

Several characteristics of the battery-powered system should be noted. The CBC050 batteries are generally not capable of delivering bursts of high power. In order to minimize weight, this system used a very lightweight 22-μF ceramic capacitor on the V_{stor} node. One possibility to provide high current pulses to the load would be to add a 7.5-mF supercapacitor (CPX3225A752D) to the V_{stor} node, which would add 24 mg of mass but dramatically increase current pulse capabilities. A combination of two CBC050 batteries plus the 24-mg supercapacitor leads to a total weight of 56 mg, still less than the supercapacitor. The problem with that change is the two batteries can only supply a maximum average current output of 2 mA during periods of no harvested power.

As shown in Figure 3-24, the batteries degraded almost 7% after 43 full discharges. While this is acceptable for many applications, it may not be for others. Possible degradation of batteries could have been improved by having a higher minimum open-circuit V_{batt} cutoff threshold in the discharger controller. The lower threshold, while it provided for longer runtime, could have played a large role in battery degradation.

Similarly, the batteries could have been discharged at rates less than 1 mA per battery.

A buck converter was not used for the battery-powered system because of the effects of limiting the instantaneous battery current. However, the batteries were never tested to see if a high ripple current waveform with an average current draw below 1 mA per battery would be acceptable. In the case of a buck converter, the current out of the battery would appear in pulses according to the duty cycle. Further testing of the batteries could possibly show pulses to be acceptable.

Another option for using a buck converter with the batteries is to stack the CBC050 batteries to get a higher voltage. If using 3 series batteries instead of 3 parallel batteries, for example, then the buck converter's duty cycle could be very low while still being able to charge up V_{stor}. By adding a high enough capacitor in parallel with the series-connected batteries, the current draw through the batteries could be maintained approximately at 1 mA. This would allow for the very high energy density of the batteries while still discharging them efficiently. The major problem associated with this method is that high voltage transistors would need to be used.

This system was sensitive to a few things. Firstly, very high value ceramic capacitors, including all tested 22-μF capacitors, had very poor responses to low frequency RMS voltage waveforms. In testing the battery discharger, the RMS values of these waveforms were such that the capacitance decreased from its nominal value dramatically, often greater than 50%. Even with this, the capacitor worked well during testing. However, this could prove problematic with certain high-transient loads that need a 22-μF capacitor at V_{stor} over a 4.7-μF capacitor, for example. Secondly, the system was particularly sensitive to comparator speed. The comparator used at V_{stor} must be fast enough that the system can respond in time to the expected transients.

The battery-powered system exhibited several advantages over the supercapacitor-powered system but lacked the ability of having a flexible energy storage element due to the sensitive charge and discharge specifications of the CBC050 batteries. Overall, each system demonstrated advantages and disadvantages over the other, and both demonstrated energy harvesting and energy storage systems with advantages over a simple supercapacitor at V_{stor}.

Chapter 4

RF Energy Harvester

For all proposed system topologies, the RF harvester works independently of the solar harvester. As an auxiliary harvester that harvests mainly low energy levels, there are a few constraints that must be met. Firstly, the RF harvester should consume a very small area to minimize weight and allow more area for the primary solar harvester and the power management circuits. Secondly, its control circuitry must consume very low power in order to effectively harvest lower energy levels. Lastly, the charge pump should minimize its effects on other functions the antenna may serve, such as backscatter communication. These targets are discussed throughout this chapter.

The RF harvester first rectifies a 915-MHz input signal used for the backscatter communication in the DragonflEye project. It is assumed that high performance Schottky diodes are not available in the ASIC process. As a result, the rectifier must comprise discrete components. A 1-stage Cockcroft-Walton charge pump is used to limit weight, requiring two RF diodes and two discrete capacitors. This results in a theoretical unloaded DC voltage of twice the input amplitude.

Using just one rectifying stage will likely not produce usable voltages, so in order to increase them, an active switched capacitor voltage multiplier (charge pump) is used. The benefit of switched capacitor circuits is that at higher operating frequencies they can be integrated into the ASIC, reducing their weight contribution. There are several switched capacitor circuits one can choose from. The Fibonacci multiplier has been shown to have the largest gain per number of capacitors [36]. Since each

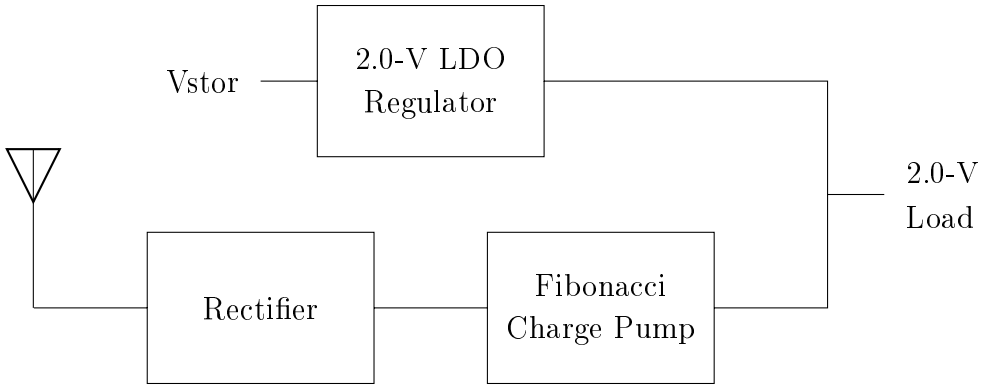


Figure 4-1: RF harvester block diagram showing rectifier-to-charge pump path and the use of a 2.0-V LDO to fix the output voltage.

capacitor can occupy a large area on the ASIC, minimizing the number of capacitors is desirable. The Fibonacci multiplier was therefore chosen as the switched capacitor circuit to be used in this design.

By carefully choosing capacitor and switching frequency values and by designing a controller to turn on a variable number of stages of the charge pump, the Fibonacci switched capacitor multiplier can be approximately impedance-matched to the antenna and rectifier over most input power values. This eliminates the need for discrete impedance matching inductors and capacitors, further decreasing the RF harvester's weight.

Lastly, in order to maximize efficiency by limiting the number of power converters in the power path, the charge pump outputs directly to the 2.0-V load. The 2.0-V load is maintained by the low-dropout regulator (LDO) from the V_{stor} node, as seen in Figure 4-1. The fixed output voltage also allows for easier impedance matching of the charge pump to the rectifier. In order to maintain the output at 2.0 V, the power consumed by the load must be greater than the power output from the RF harvester, meaning the LDO must provide some positive amount of power to the load.

This chapter examines the design and operation of the rectifier, the charge pump, the rectifier-charge pump combination, and the entire RF harvester in tandem with the LDO.

4.1 RF Rectifier

The first step in designing the RF harvester was to examine and characterize the RF rectifier. A simple Cockcroft-Walton RF doubler rectifier was used. This was chosen as opposed to a ladder of diode doublers in order to limit the amount of external components, at the cost of a low rectified voltage. SMSA7630-061 diodes were chosen because of their very low forward voltage drop (0.180 V typical) and their very light weight (less than 1 mg each). In order to eliminate the need for a matching network requiring even more discrete components, the rectifier impedance was examined to directly impedance-match the charge pump to the rectifier. While a typical antenna may not have a source impedance of 50 Ω, most signal generators do. Since a signal generator was used for testing purposes, the system was designed to match to a 50-Ω source impedance before the rectifier. When matching to a different source impedance, the steps described in the rest of this chapter can be followed in the same fashion.

Both ideal diodes and SMSA7630-061 SPICE models found in the datasheet were swept over various loads and for various input voltage amplitudes. The schematic is shown in Figure 4-2. Figures 4-3 through 4-6 show the resulting current versus voltage (I-V) (top) and power versus voltage (P-V) (bottom) curves for ideal diode-based simulations, SMSA7630-061 model-based simulations, and real measurements of the circuit using SMSA7630-061 diodes. As can be seen, the I-V curves look fairly linear followed by tails at higher voltages. Thevenin equivalent models were fit to the approximately linear portions for the simulations and are also shown in the figures. The large decreases in the curves from using ideal diodes to real diodes demonstrate the dramatic effect real diode characteristics have on the rectifier performance. Table 4.1 shows the values at the maximum power point of the P-V curves, indicating a matched impedance at those points. The matched load impedances of the ideal simulations are independent of the input voltage, as expected. For ideal diodes, the optimal load impedance with no leakage currents or source inductance is shown in [49]

to be

$$R_{load,\,opt} = \frac{\pi^2}{2}\sqrt{R_s^2 + \frac{1}{(\omega C_s)^2}} \tag{4.1}$$

where $R_{load,\,opt}$ is the optimal load for matching to the Cockcroft-Walton rectifier, R_s is the source impedance, ω is the input signal's angular frequency, and C_s is the stage capacitor between the source and the diodes. By applying the values shown in Figure 4-2 to Equation 4.1, one would expect the matched load impedance with ideal diodes to be 246.7 Ω. Simulations were sampled at 50-Ω intervals so 250 Ω is listed as the optimal impedance in Table 4.1. Simulations and measurements using SMSA7630-061 diodes were very dependent on the input voltage. Measured matched loads range from 411 Ω to 1277 Ω. In order to match to a specific value, 600 Ω was chosen as a middle value more closely matched to higher input powers than to lower ones. This data fully characterizes the RF rectifier and Section 4.3 demonstrates matching the charge pump to this 600-Ω value.

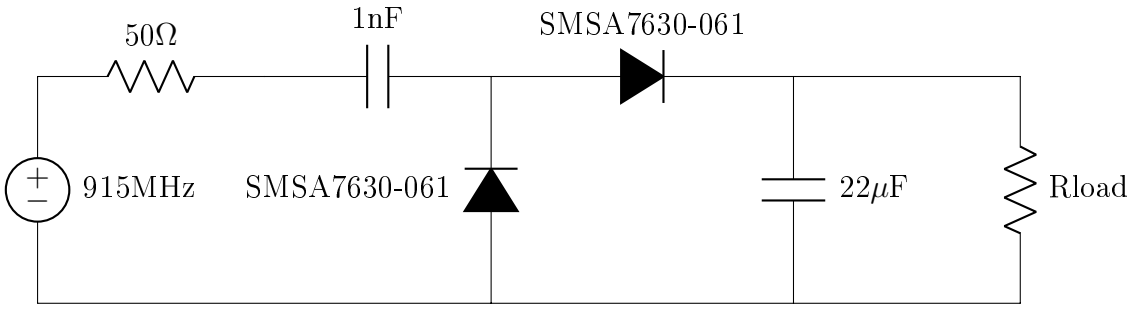
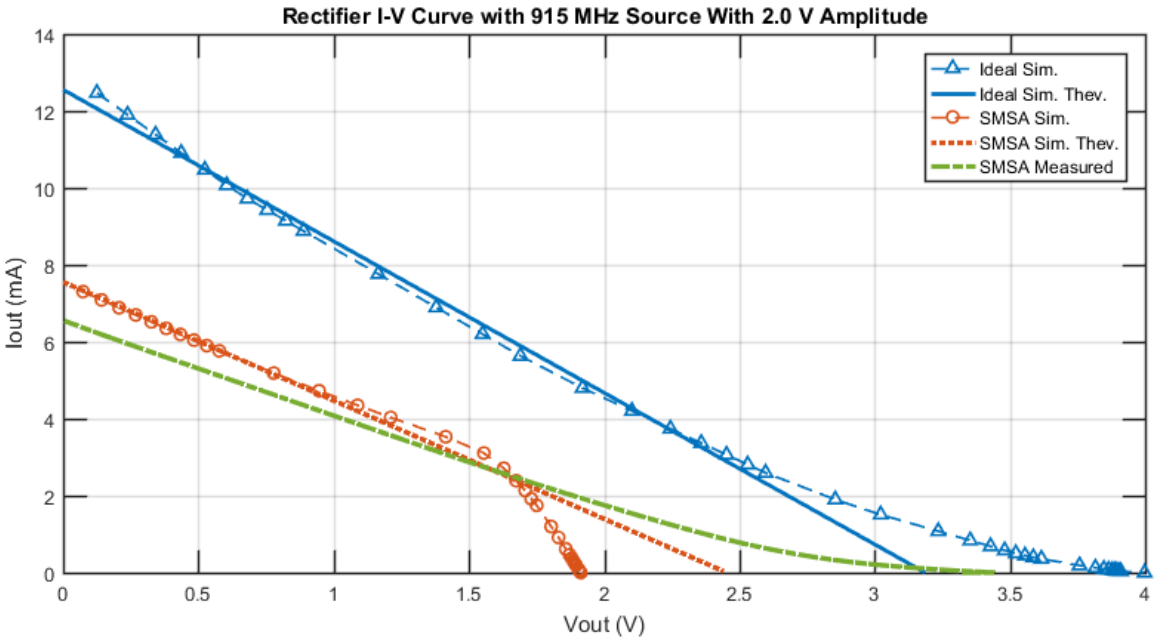


Figure 4-2: Schematic of RF rectifier.



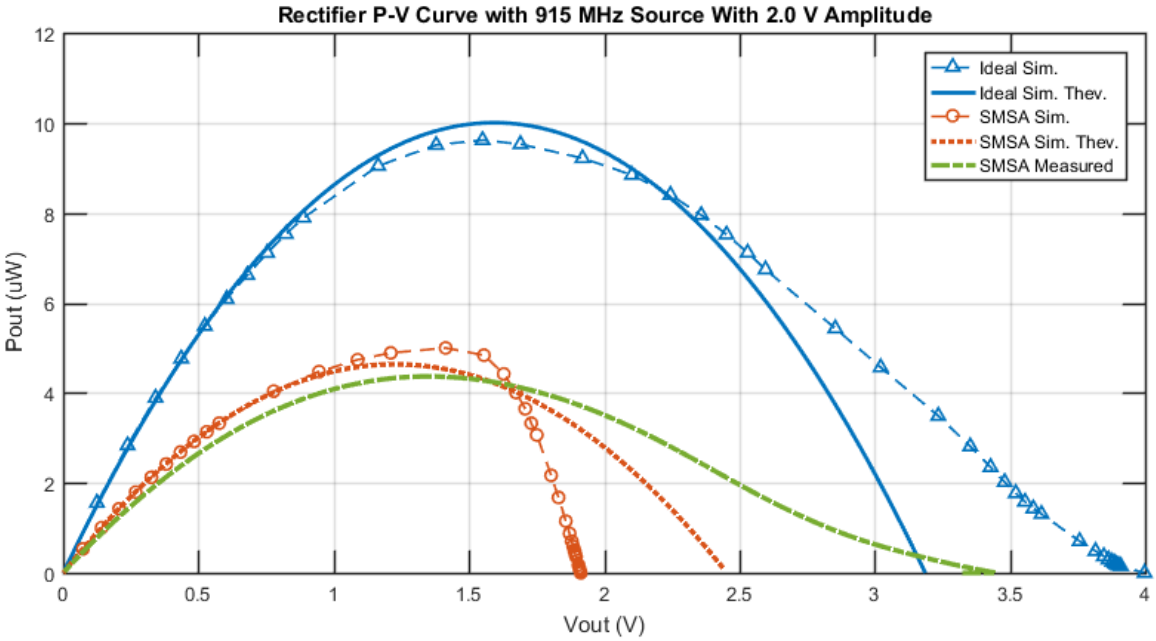


Figure 4-3: Simulation and measurement results of rectifier with 2.0-V input voltage amplitude.

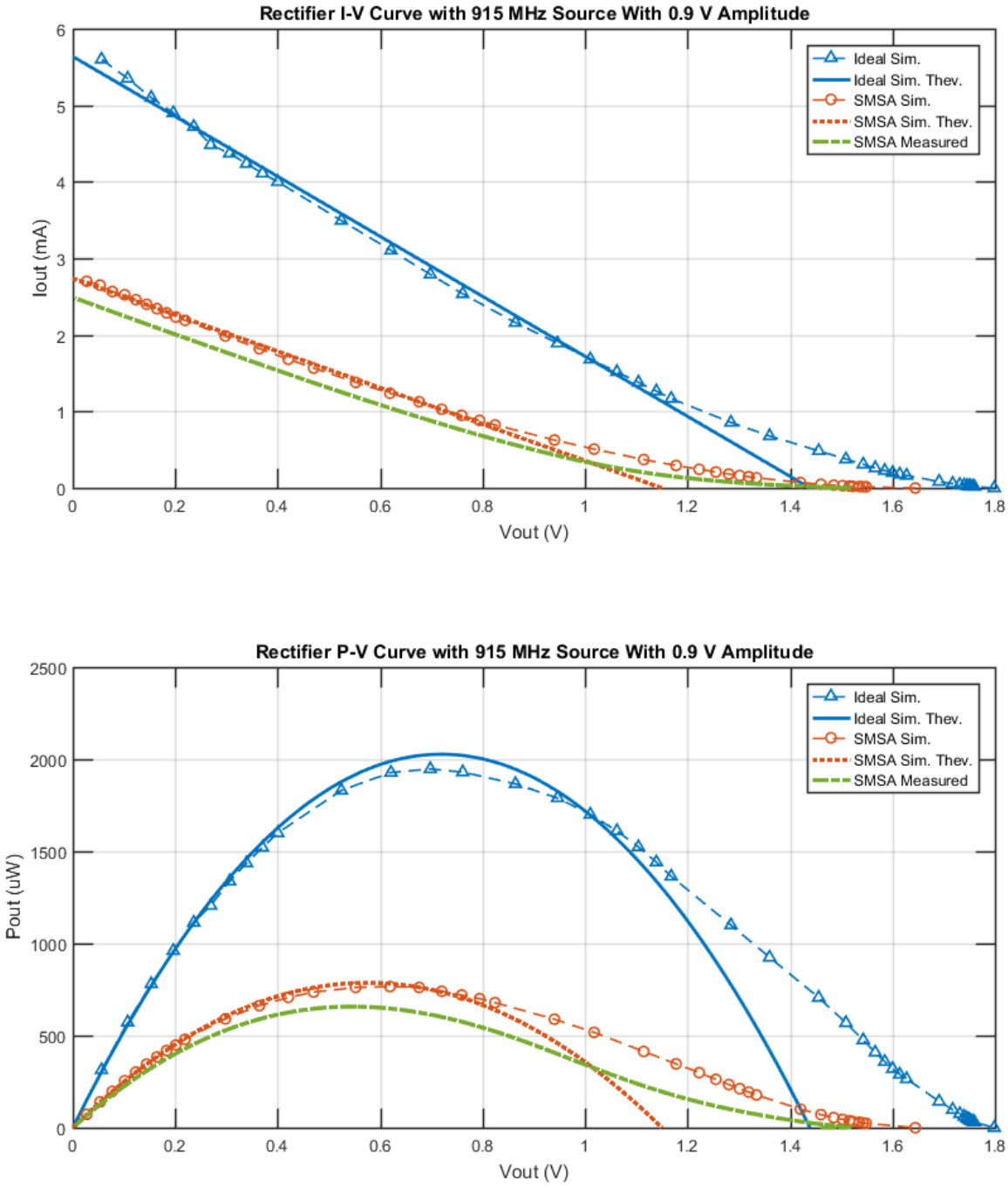


Figure 4-4: Simulation and measurement results of rectifier with 0.9-V input voltage amplitude.

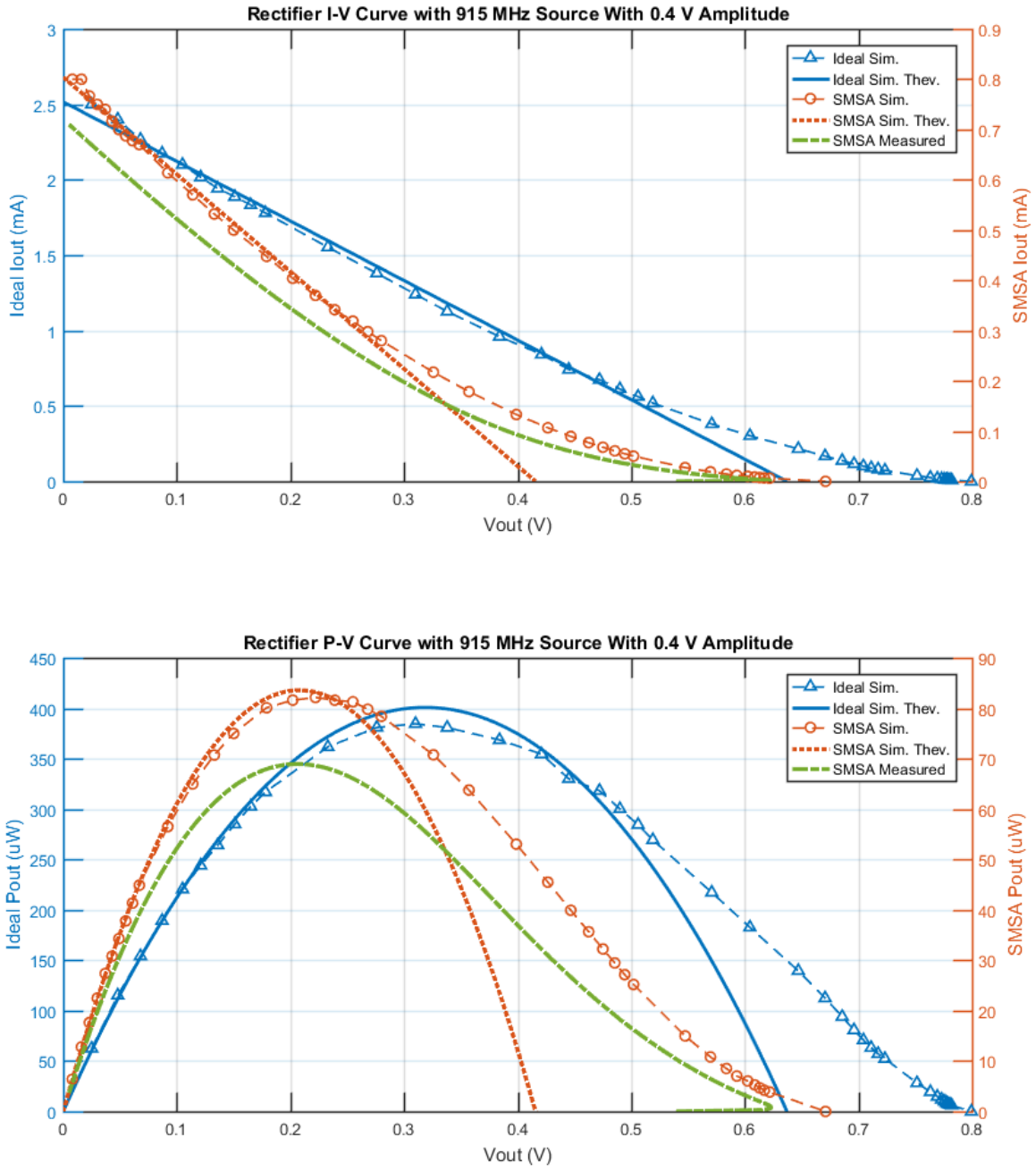


Figure 4-5: Simulation and measurement results of rectifier with 0.4-V input voltage amplitude. For readability, the SMSA7630-061 diode-based data is shown on the right axis.

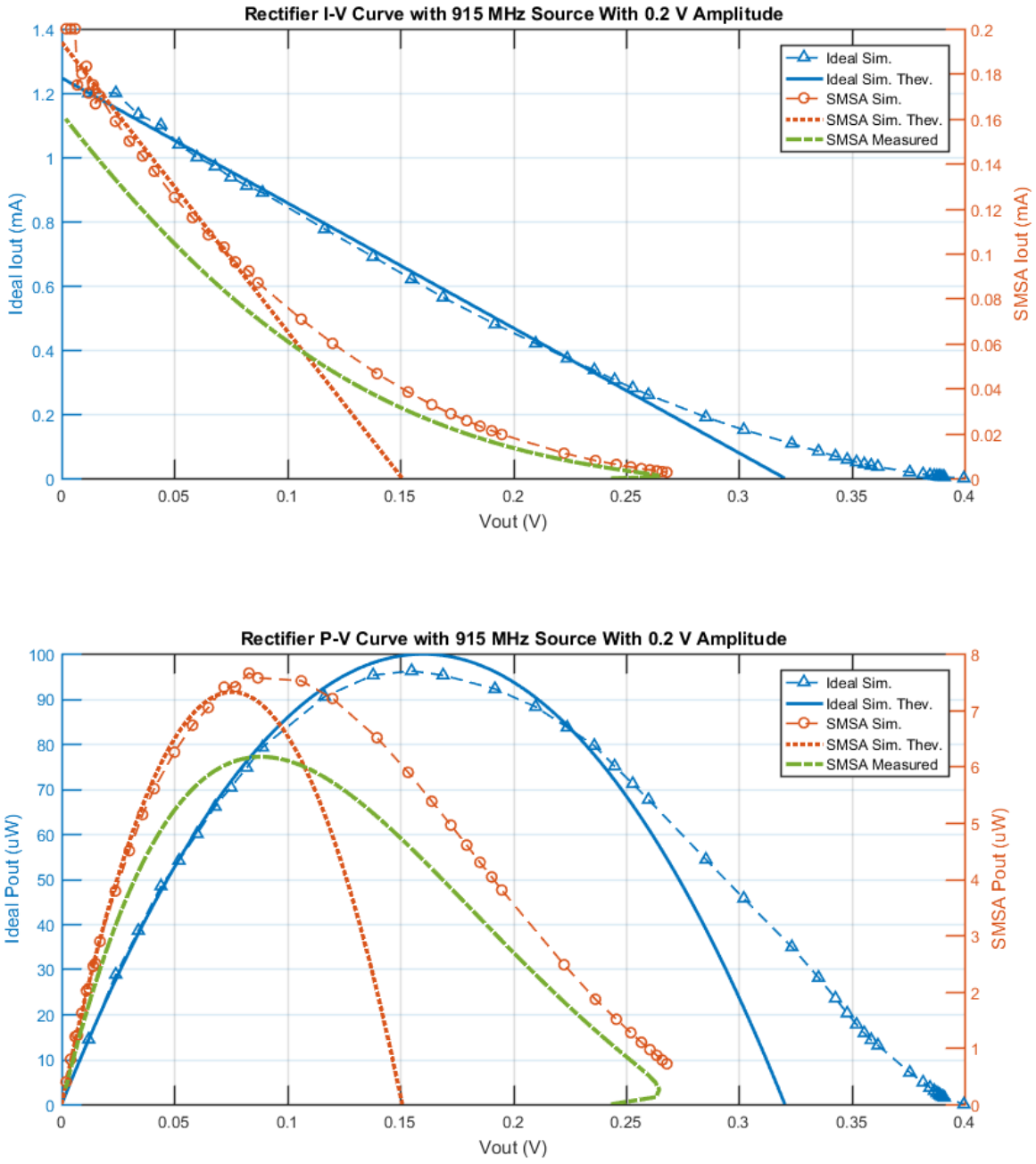


Figure 4-6: Simulation and measurement results of rectifier with 0.2-V input voltage amplitude. For readability, the SMSA7630-061 diode-based data is shown on the right axis.

Table 4.1: Matched impedance characteristics for rectifiers.

Voltage Source Amplitude (V)		$V_{matched}\,(V)$	$I_{matched}\,(\mu A)$	$R_{load,\,matched}\,(\Omega)$	$P_{matched}\,(\mu W)$
2.0 (10 dBm)	**Ideal Sim.**	1.551	6202	250	9616
	SMSA Sim.	1.414	3535	400	4998
	SMSA Meas.	1.340	3259	411	4367
0.9 (3.06 dBm)	**Ideal Sim.**	0.6977	2791	250	1947
	SMSA Sim.	0.6190	1238	500	766.3
	SMSA Meas.	0.5469	1202	455	657.4
0.4 (-3.98 dBm)	**Ideal Sim.**	0.3101	1240	250	384.6
	SMSA Sim.	0.2220	370.0	600	82.14
	SMSA Meas.	0.2067	333.5	620	68.95
0.2 (-10 dBm)	**Ideal Sim.**	0.1551	620.2	250	96.16
	SMSA Sim.	0.0830	92.22	900	7.654
	SMSA Meas.	0.08877	69.49	1277	6.169

4.2 Charge Pump

Following the rectifier, a charge pump is used to bring the rectified voltage to a usable value. When designing and analyzing charge pumps, several previous works have focused on output resistance and voltage gain [5], [10]. This is because a very low output resistance decreases voltage droop for higher output currents. This work, however, designs around input resistance and efficiency in order to impedance-match to the rectifier. It also takes a unique approach by locking the charge pump output to a fixed voltage to combine power from two different sources. Such an approach also simplifies the input resistance analysis.

As previously stated, there are many different switched capacitor charge pump topologies that can be used. The Fibonacci charge pump can achieve the highest gain with the lowest number of capacitors, meaning it would consume the lowest ASIC area when integrated and therefore weigh the least. Still, this topology is not without its challenges. With a fixed output voltage, the input resistance can vary widely over the valid range of input voltages. Furthermore, the larger the difference between the input and output voltages, the less efficient the charge pump becomes. To address both problems, using a variable number of stages can keep the input resistance within a certain range and the efficiency above a specific threshold. Luckily, the controller for such a solution is computationally simple, where the number of enabled stages depends only on the input voltage. In testing, 1- through 6-stage charge pumps were used, with the switches constructed as in Figure 4-7. The analysis results for each stage are shown in Table 4.2. All derivations and schematics showing the operation

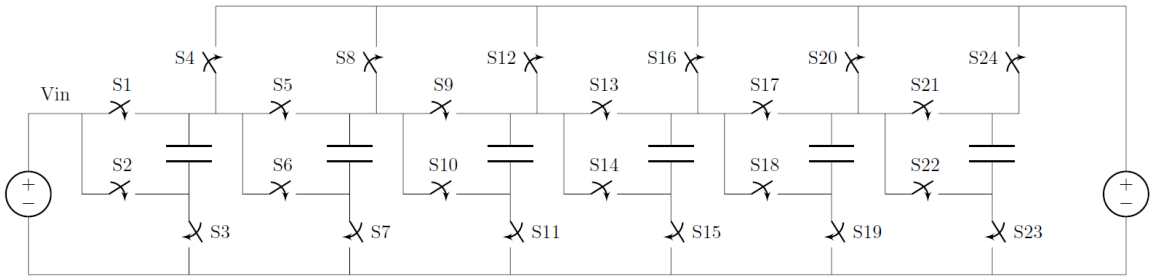


Figure 4-7: Schematic of the built Fibonacci charge pump with a configurable number of enabled stages, from 1 to 6 stages.

Table 4.2: Summary of ideal characteristics for 1- through 6-stage Fibonacci charge pumps.

No. of Stages	$\boldsymbol{I_{out}}$	$\frac{\boldsymbol{I_{in}}}{\boldsymbol{I_{out}}}$	$\boldsymbol{R_{in}}$	$\boldsymbol{\eta}$
1	$Cf(2V_{in} - V_{out})$	2	$\frac{1}{4Cf} \cdot \frac{2V_{in}}{2V_{in}-V_{out}}$	$\frac{V_{out}}{2V_{in}}$
2	$\frac{1}{2}Cf(3V_{in} - V_{out})$	3	$\frac{2}{9Cf} \cdot \frac{3V_{in}}{3V_{in}-V_{out}}$	$\frac{V_{out}}{3V_{in}}$
3	$\frac{1}{6}Cf(5V_{in} - V_{out})$	5	$\frac{6}{25Cf} \cdot \frac{5V_{in}}{5V_{in}-V_{out}}$	$\frac{V_{out}}{5V_{in}}$
4	$\frac{1}{15}Cf(8V_{in} - V_{out})$	8	$\frac{15}{64Cf} \cdot \frac{8V_{in}}{8V_{in}-V_{out}}$	$\frac{V_{out}}{8V_{in}}$
5	$\frac{1}{40}Cf(13V_{in} - V_{out})$	13	$\frac{40}{169Cf} \cdot \frac{13V_{in}}{13V_{in}-V_{out}}$	$\frac{V_{out}}{13V_{in}}$
6	$\frac{1}{104}Cf(21V_{in} - V_{out})$	21	$\frac{104}{441Cf} \cdot \frac{21V_{in}}{21V_{in}-V_{out}}$	$\frac{V_{out}}{21V_{in}}$
n	$\frac{1}{F_n \cdot F_{n+1}}Cf(F_{n+2}V_{in} - V_{out})$	F_{n+2}	$\frac{F_n \cdot F_{n+1}}{F_{n+2}^2 Cf} \cdot \frac{F_{n+2}V_{in}}{F_{n+2}V_{in}-V_{out}}$	$\frac{V_{out}}{F_{n+2}V_{in}}$

F_0	F_1	F_2	F_3	F_4	F_5	F_6	F_7	F_8
0	1	1	2	3	5	8	13	21

of the various charge pumps are provided in Appendix B.

To illustrate the theoretical ideal behaviors of the charge pump, Figure 4-8 shows various plots of a 1-stage ideal Fibonacci charge pump with the output voltage fixed at 2.0 V and a fixed Cf value. As Table 4.2 suggests, the output current is linear with V_{in}, and thus the input current is too because it is a scaled version of the output current. The input power, the product of input current and the input voltage, becomes quadratic, while the output power remains linear since the output voltage is fixed. In order for the input to provide positive power to the load, $V_{in}F_{n+2}$ must be greater than V_{out}, where values of F are shown in Table 4.2. This is why Figure 4-8 sweeps V_{in} from 1 V to 2 V. One important quality to note is that efficiency approaches 1 as output power and input power approach 0. Therefore, efficiency should not be the

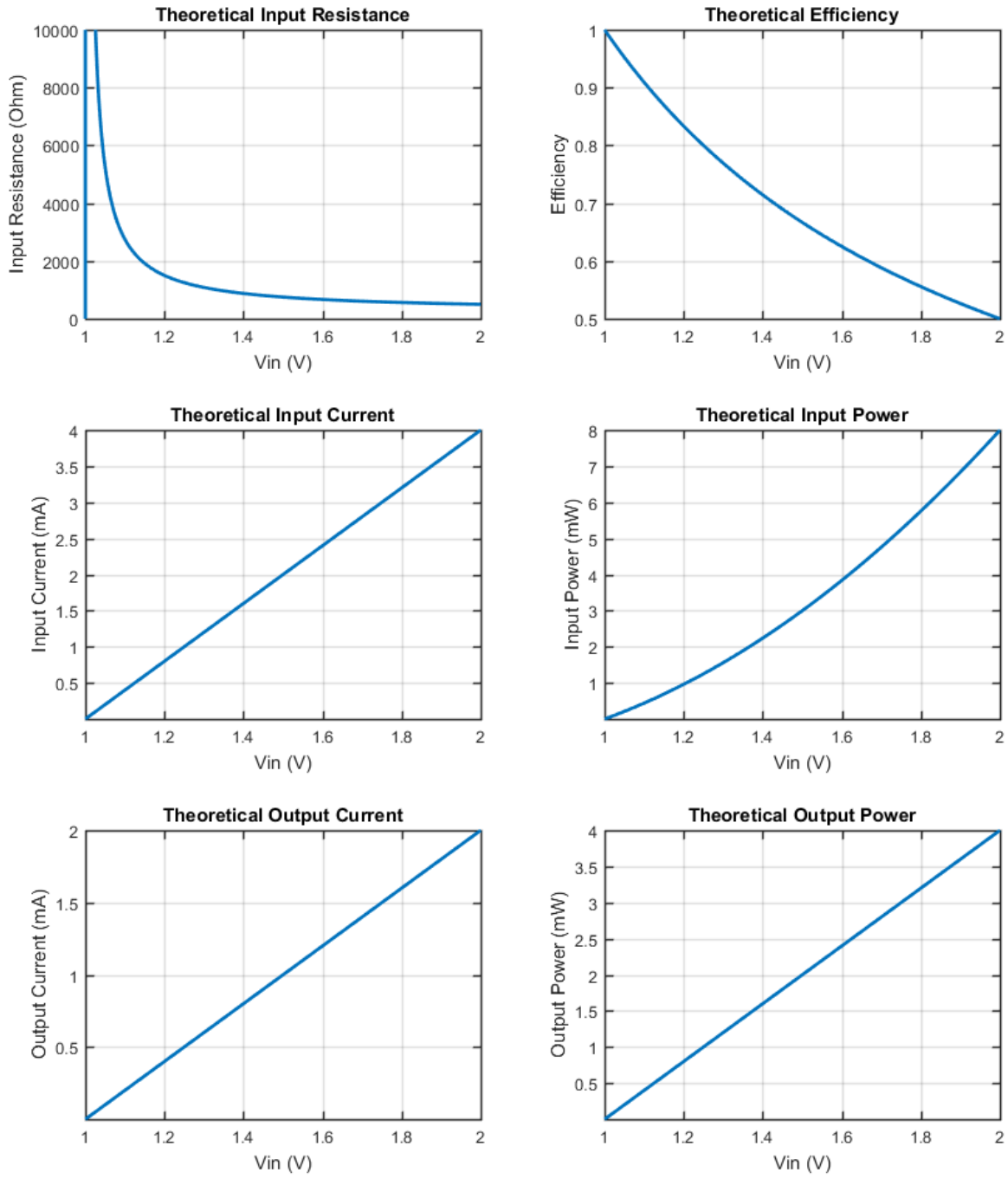


Figure 4-8: Theoretical ideal behavior of 1-stage Fibonacci charge pump with output voltage fixed at 2.0 V. Cf equals 0.001 Ω^{-1}.

sole determinant of the charge pump design.

In order to impedance-match the charge pump to the rectifier, the input resistance can be set to a desired range by changing the product Cf. As described by the equations of Table 4.2, increasing the switching capacitor size or increasing switching

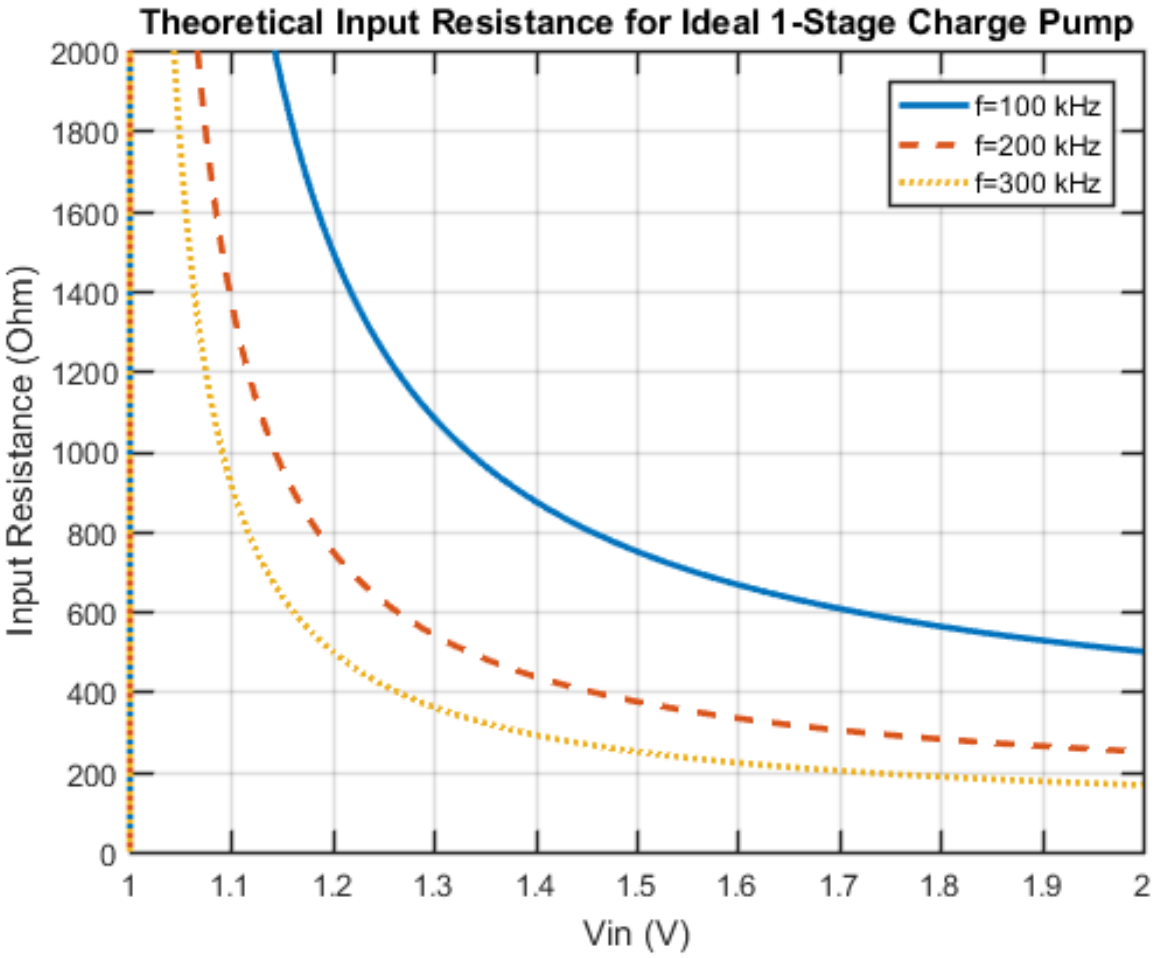


Figure 4-9: Theoretical ideal input resistance of 1-stage Fibonacci charge pump with output voltage fixed at 2.0 V over various switching frequencies.

frequency pushes the input resistance curve downward, decreasing the input resistance at a specific operating point. Both of these come at a cost, however. A larger C requires larger area, and a larger f increases gate capacitance losses in the switches. If either of these is acceptable, then the charge pump can be properly matched to the rectifier. Conveniently, this has no effect on ideal efficiency. Figure 4-9 illustrates how varying the switching frequency affects the input resistance.

Appendix B Section B.2 derives a model for the parasitic switch losses, summarized in Table B.4 by how many stages are enabled. The parasitics model assumes that the input is not affected at all by the losses; rather, the losses are simply subtracted from the output. Interestingly, according to this model, the efficiency is only affected by the parasitic capacitance and is independent of the switching frequency.

This is because according to the model

$$P_{out,\,with\,p} = P_{out,\,ideal} - P_{p,\,total} \tag{4.2}$$

where $P_{out,\,with\,p}$ is the theoretical output power incorporating parasitic loss, $P_{out,\,ideal}$ is the theoretical output power in the ideal case without parasitics, and $P_{p,\,total}$ is the total theoretical parasitic loss. From this, the efficiency becomes

$$\eta_{with\,p} = \frac{P_{out,\,with\,p}}{P_{in}} = \frac{P_{out,\,ideal} - P_{p,\,total}}{P_{in}} = \eta_{ideal} - \frac{P_{p,\,total}}{P_{in}} \tag{4.3}$$

where $\eta_{with\,p}$ is the theoretical efficiency including parasitics and P_{in} is the theoretical input power. From Tables 4.2 and B.4 it is known that

$$\frac{P_{p,\,total}}{P_{in}} \propto \frac{C_p f}{C f} = \frac{C_p}{C} \tag{4.4}$$

where C_p is the parasitic capacitance, C is the switched capacitor capacitance, and f is the operating frequency. This shows that $\eta_{with\,p}$ is proportional to the ratio of C_p and C, independent of f. Figure 4-10 illustrates the theoretical efficiency curve with parasitics and how a larger switching capacitor improves efficiency for the same parasitic capacitance.

After analyzing the charge pump topology, a configurable-stage Fibonacci charge pump as shown in Figure 4-7 was built and tested. In an ASIC design, capacitor values of 200 pF and switching frequencies of 5 MHz are attainable. Since the ideal charge pump formulas are dependent on the product Cf and never solely on one variable or the other, a discrete system was built and tested with 10-nF capacitors and a switching frequency of 100 kHz. This was done because switching losses in the discrete system are far greater than a completely integrated system. Note that the Cf product for both of these combinations is the same. TS3A4751PWR analog multiplexers were used for switches, with an estimated 25 pF of parasitic capacitance across each switch. In order to prevent damaging amounts of current surges, 47-Ω resistors were added in series with each switching capacitor. So long as the RC time constant is much lower

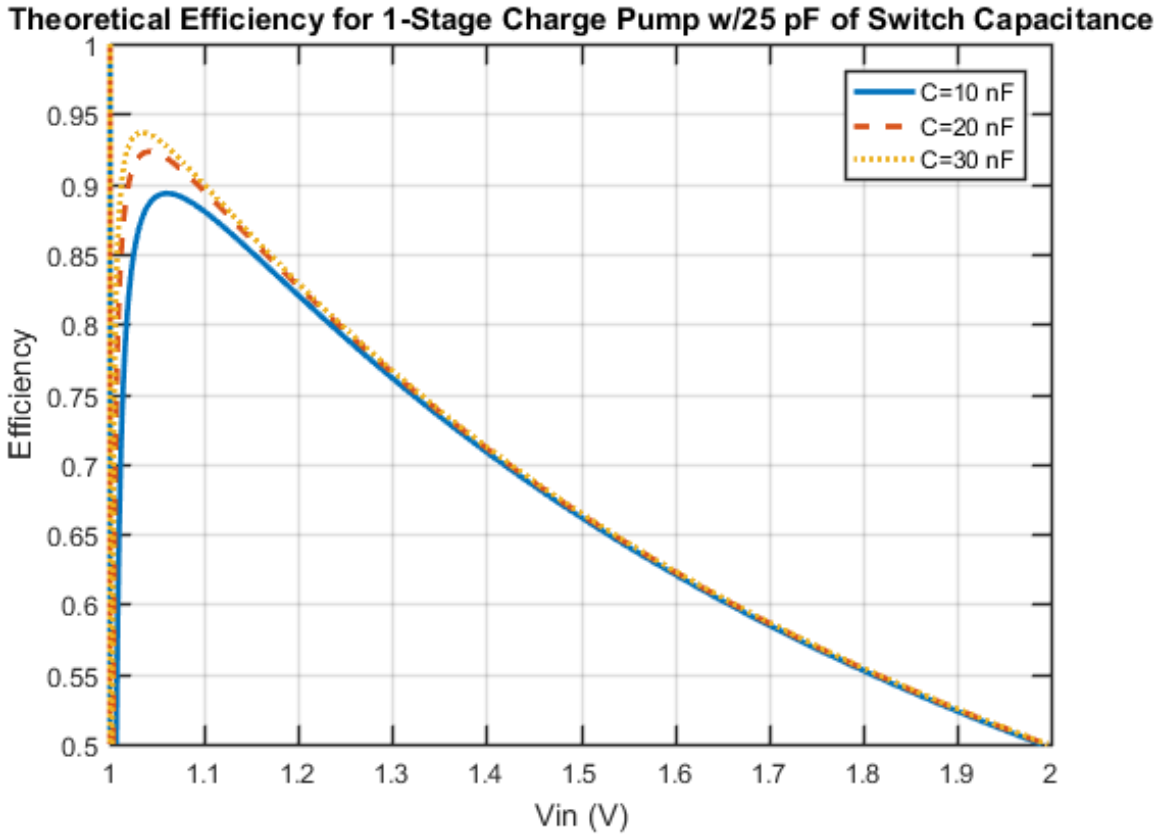


Figure 4-10: Theoretical efficiency of 1-stage Fibonacci charge pump with output voltage fixed at 2.0 V for over various C values. C_p equals 25 pF.

than the swiching period, the resistance should have no effect on energy transfer. Figure 4-11 shows the theoretical ideal behavior of the designed charge pump; Figure 4-12 shows the theoretical behavior including parasitic capacitances of 25 pF; Figure 4-13 shows the actual measured behavior of the built discrete system; and Figure 4-14 shows the error when comparing the theoretical behavior with parasitics to the actual measured system. All plots include curves for 1- through 6-stage charge pumps with 2.0-V loads, with the exception of the bottom plot of Figure 4-14. This plot compares the measured unloaded voltage gains with the theoretical unloaded voltage gains with parasitics. Plots of this behavior and all other measured behaviors for individual stages are found in Appendix C. Due to input voltage limits on the multiplexer, a 3.0-V power supply was separately used to control the switches. Data on the current draw from the power supply is also included in Appendix C. Figure 4-14 displays errors referenced to the theoretical predictions typically within a $\pm 10\%$ bound except for edge cases. Large spikes in errors typically represent input voltage regions where the measurements and predicted behaviors become very small. One example is the output power errors. Around the minimum operating input voltage for each stage, the theoretical output powers approach 0, so small errors in measurement and theory are magnified. In any case, the charge pump would normally not be operated around these regions because of the small amounts of output power.

One interesting observation when using the TS3A4751PWR analog multiplexers was that when using charge pumps with multiple stages enabled, turning on all switches at the same time severally impaired the charge pump performance. The input power rose dramatically from what was expected, and the unloaded output voltage gain was drastically limited. When turning switches on and off sequentially rather than simultaneously, this corrected the problem. Take for example a sequential 3-stage charge pump using the switch labels in Figure 4-7. During the first phase, switches S1 and S3 were turned on first, followed by a pause. Then, S6 was turned on, followed by a pause. Lastly, S9 and S11 were turned on. Turning off the switches was done in the opposite fashion: first S9 and S11, pause, then S6, pause, and lastly S1 and S3.

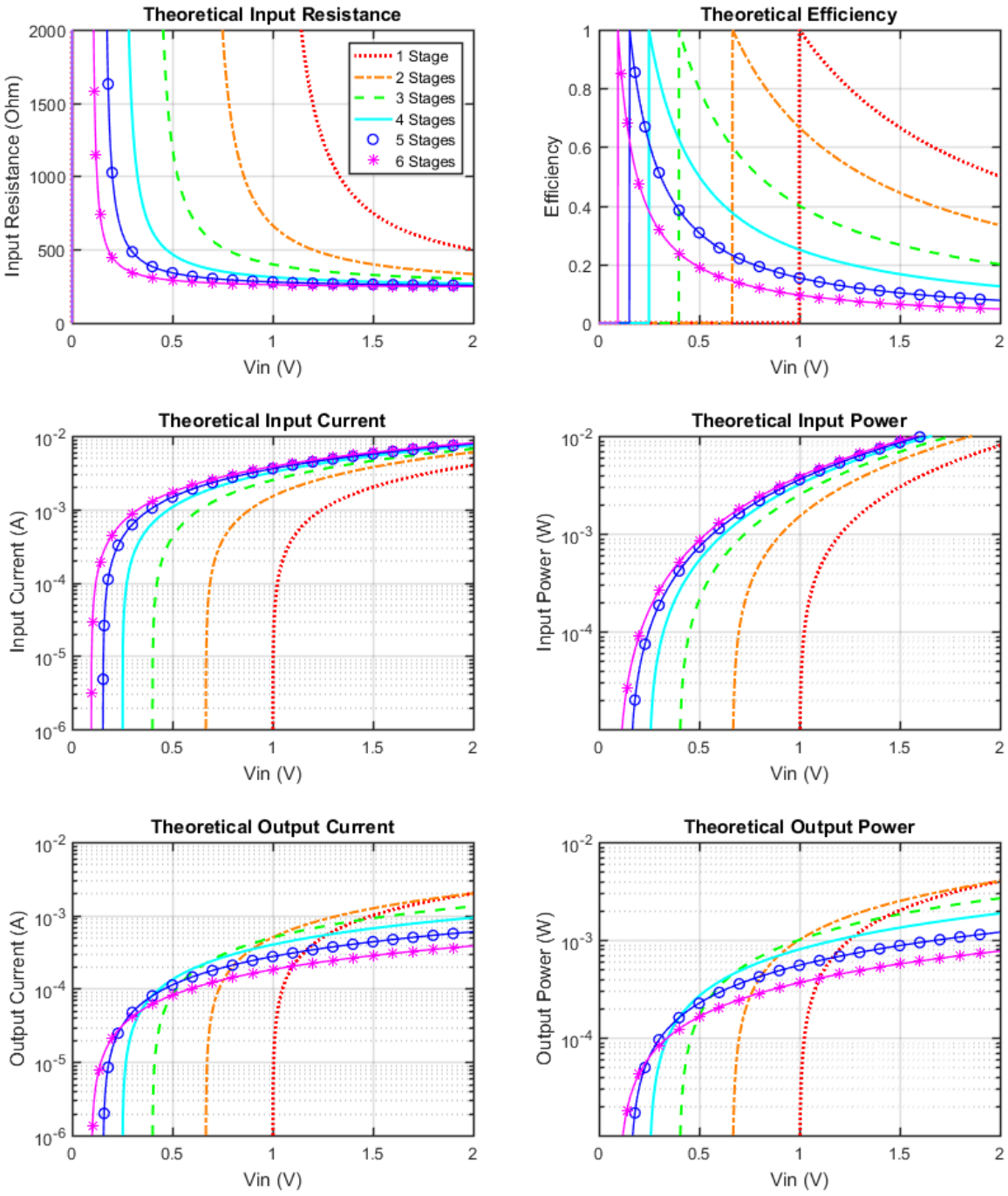


Figure 4-11: Theoretical ideal behavior of 1- through 6-stage charge pumps.

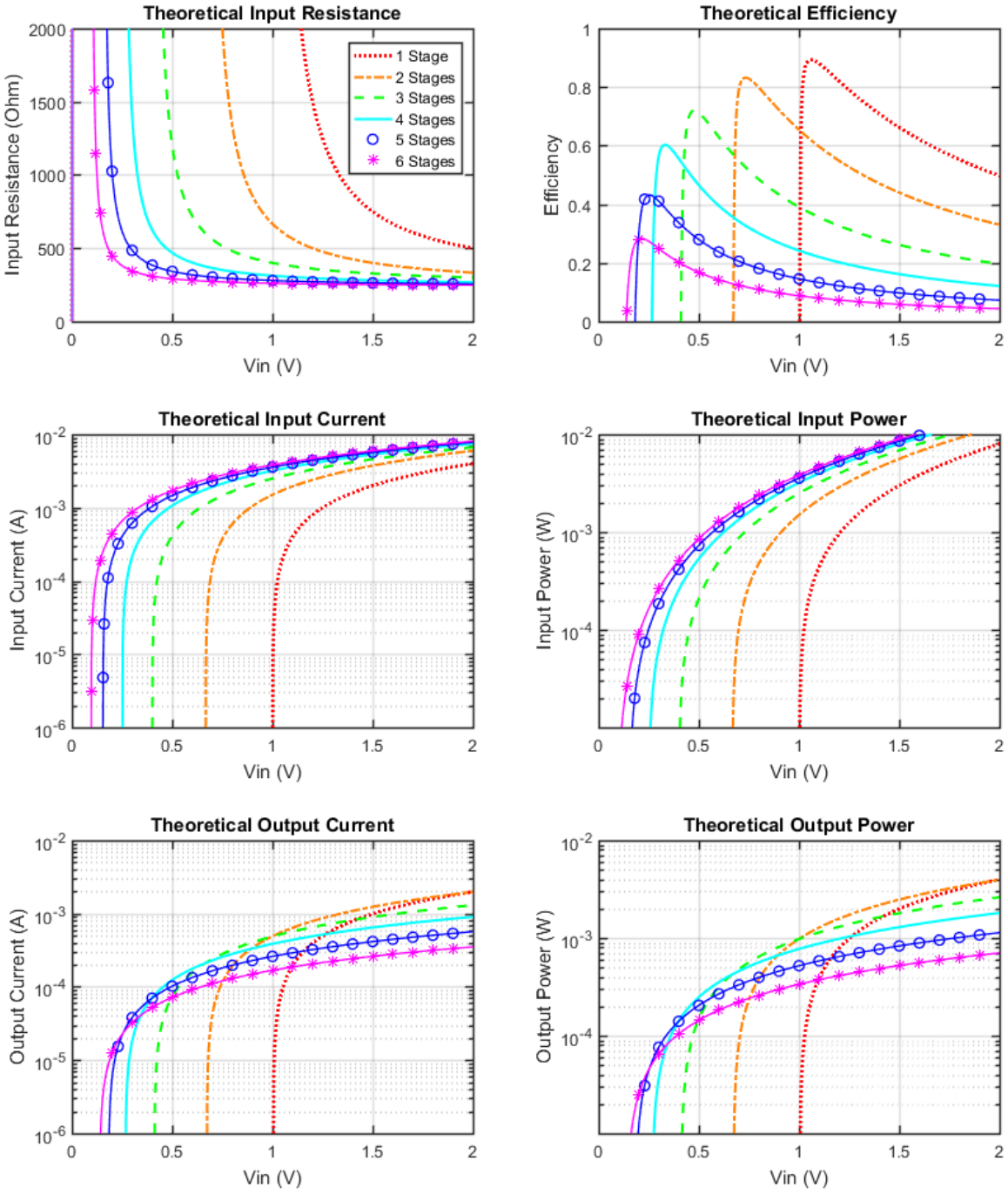


Figure 4-12: Theoretical behavior incorporating parasitics of 1- through 6-stage charge pumps.

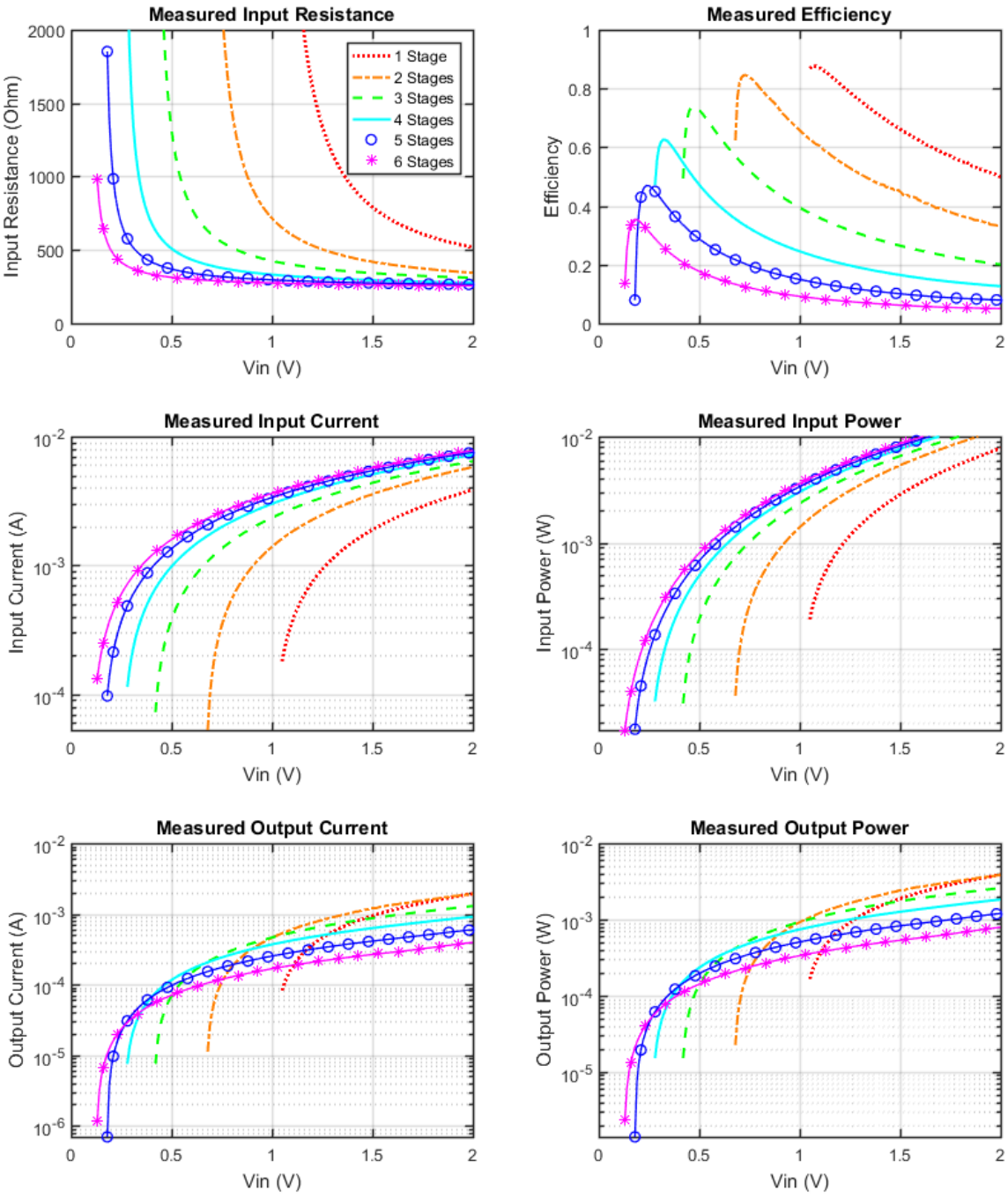


Figure 4-13: Measured behavior of 1- through 6-stage charge pumps.

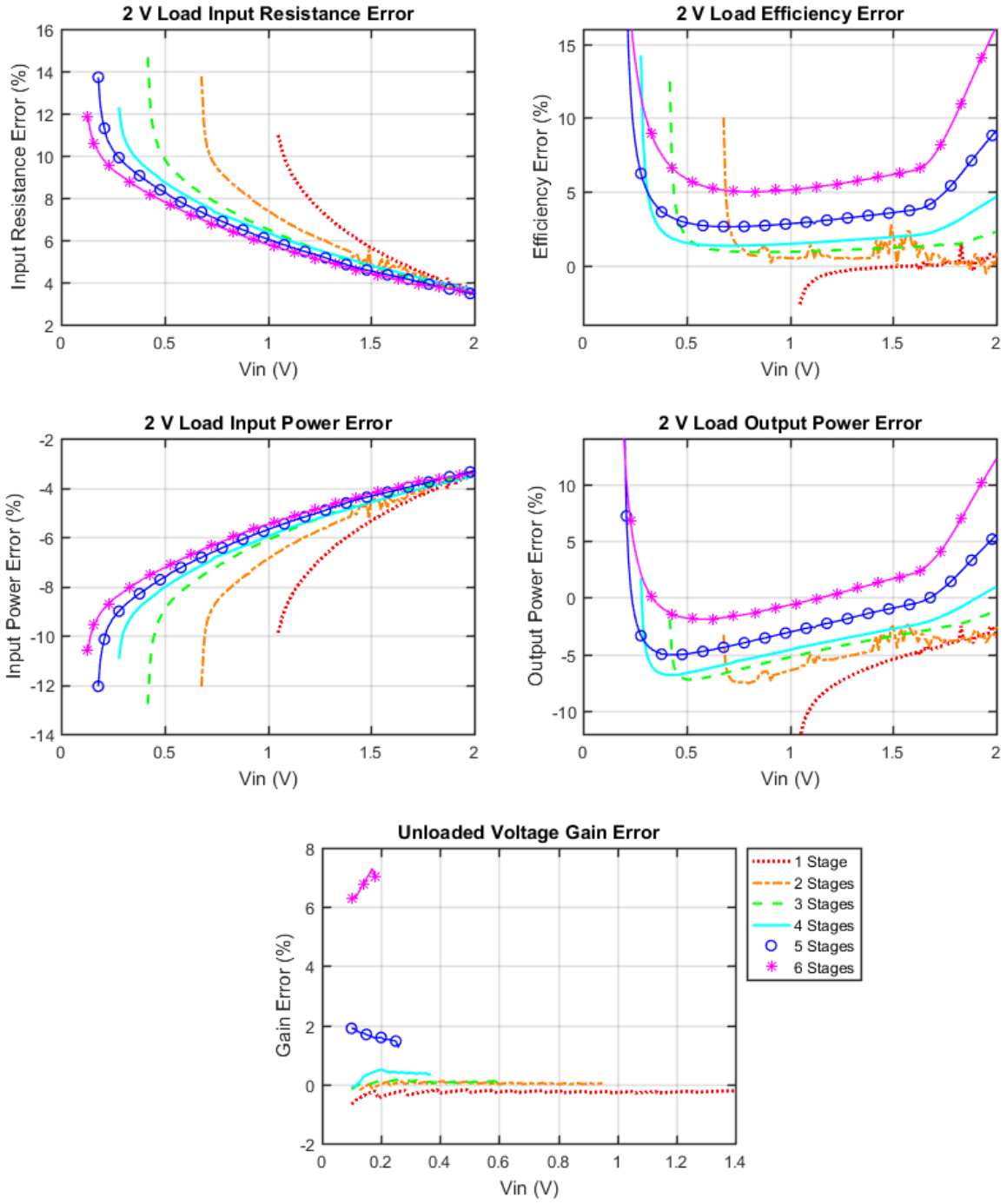


Figure 4-14: Errors of measured behavior referenced to theoretical behavior incorporating parasitics of 1- through 6-stage charge pump.

4.3 Complete RF Harvester

After establishing that the configurable charge pump functions as predicted with the application of a fixed output voltage and a rectified DC input voltage, the charge pump's Cf value and the controller needed to be determined. Before this, however, it needed to be verified that the charge pump's input impedance actually looked resistive. By having an almost purely resistive charge pump, the charge pump's impedance could be matched to the resistor values measured in Section 4.1. The RF rectifier-to-charge pump circuit was simulated and compared to an RF rectifier-to-resistor circuit, with transient results shown in Figure 4-15. In the top three plots, a section of the waveforms for a 6-stage Fibonacci charge pump attached to a 2.0-V voltage source load is examined. During this period of time, the input voltage to the charge pump (the RF rectified voltage) averaged 193.9 mV. Using the R_{in} equation of Table 4.2, this resulted in an estimated input impedance of 463.56 Ω. In Fig 4-15, the bottom three plots show the rectifier to a resistor of this value. The waveforms match very well, indicating that the charge pump behaves very resistively with a large enough filtering capacitor at the charge pump input. The simulation was run with a 300-nF capacitor for faster simulations, but a larger capacitor was used in the physical system, which only decreased any reactive component of the charge pump's impedance.

Then, the controller had to be designed. For very low power dissipation, it was decided to control the charge pump using six nanopower comparators with specific thresholds to switch the charge pump from one number of enabled stages to another depending on which comparators were high. Determining these thresholds was not so simple, however. One technique would be to examine the "Theoretical Output Power" plots of Figures 4-11 through 4-13 and choose the intersection points between various stages as the switching voltages. While this would deliver maximum power to the load from a voltage source input to the charge pump, this would not necessarily be the case for a voltage source with a typical source resistance. The Thevenin resistances of the simulated SMSA7630-061 rectifier, for example, ranged from 400 Ω to 900 Ω

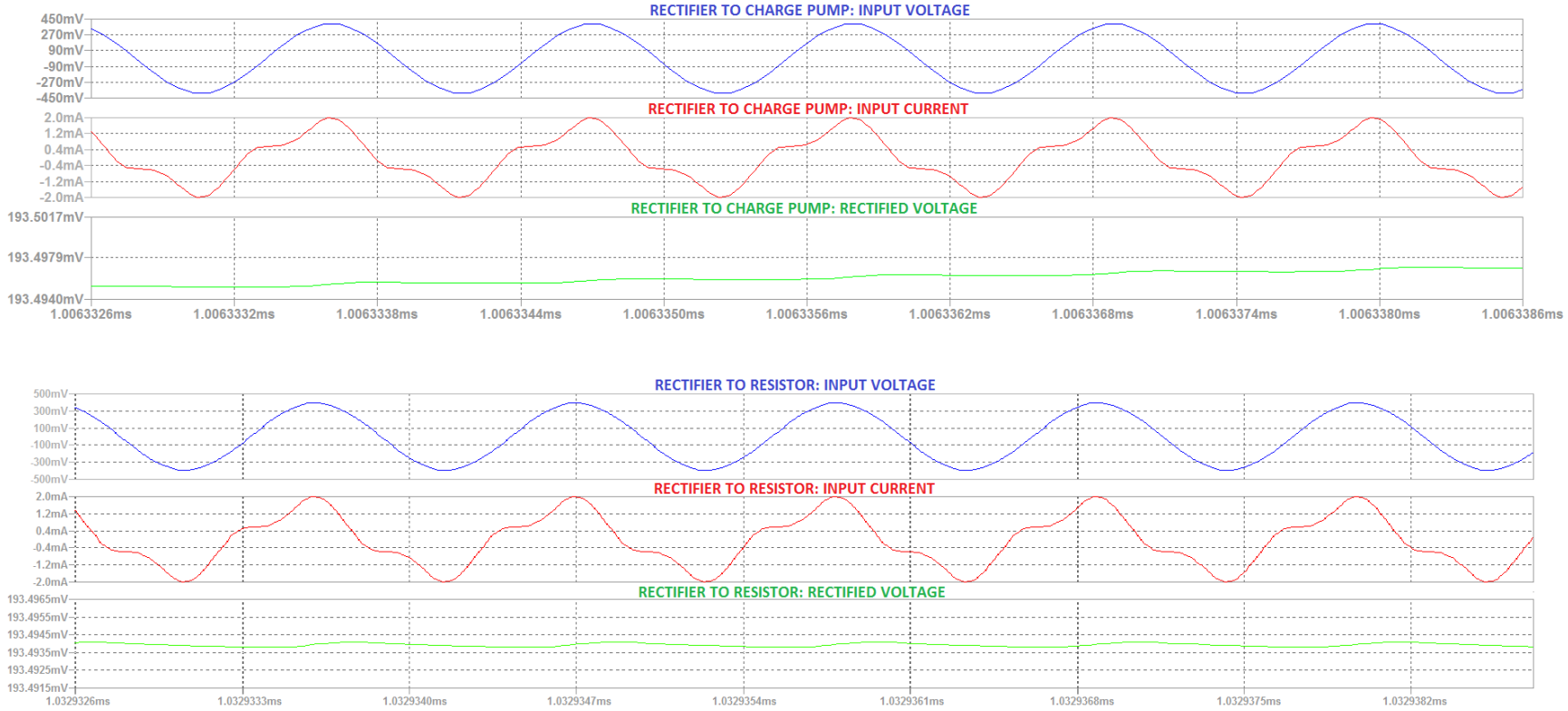


Figure 4-15: Simulated input voltage, input current, and rectified voltage for the RF rectifier to a 6-stage charge pump (top 3 plots) and the RF rectifier to an equivalent resistor (bottom 3 plots).

Table 4.3: Intersection points of rectifier and charge pump I-V curves in Fig 4-16.

No. of Stages	1	2	3	4	5	6
$\boldsymbol{V_{in}\,(V)}$	1.2353	0.9730	0.8000	0.6854	0.6195	0.5762
$\boldsymbol{P_{out}\,(\mu W)}$	941.2	919.0	666.7	464.3	302.7	194.2

over the tested values. Take for example a 1.8-V voltage source with a 600-Ω load. Figure 4-16 shows its I-V curve plotted against the charge pump load lines. The thick, black line labeled "System" represents the system with threshold voltages determined by the intersection points of the output power curve in Figure 4-11. By looking at where the "Input I-V" curve intersects the "System" curve, it is seen that by using this controller, the charge pump would operate at 3 enabled stages with this input. Table 4.3 shows the output power to the 2.0-V load for the operating points for this input with each number of enabled stages. The maximum output power occurs using 1 enabled stage, not 3. This suggests that with the source impedances the charge pump will see with the SMSA7630-061 RF rectifier, this type of controller will not necessarily lead to the best results.

Instead what was done was to choose the threshold voltages by setting a maximum allowable input resistance, R_{max}, and examining the average input impedance over all operating input voltages. There were then two parameters to vary: the Cf product and R_{max}. The threshold voltages were chosen in the following way. First, for a 1-stage charge pump, the input impedance of the charge pump was examined as the input voltage was decreased. When the input impedance equaled R_{max}, that input voltage was determined to be the threshold voltage between a 1-stage charge pump and a 2-stage charge pump. Then, the input voltage continued to be decreased, and the input impedance of the 2-stage charge pump was examined. When the input impedance again reached R_{max}, that input voltage was determined to be the threshold voltage between a 2-stage charge pump and a 3-stage charge pump. This process was repeated up until the input voltage for the 6-stage charge pump reached R_{max}. Any

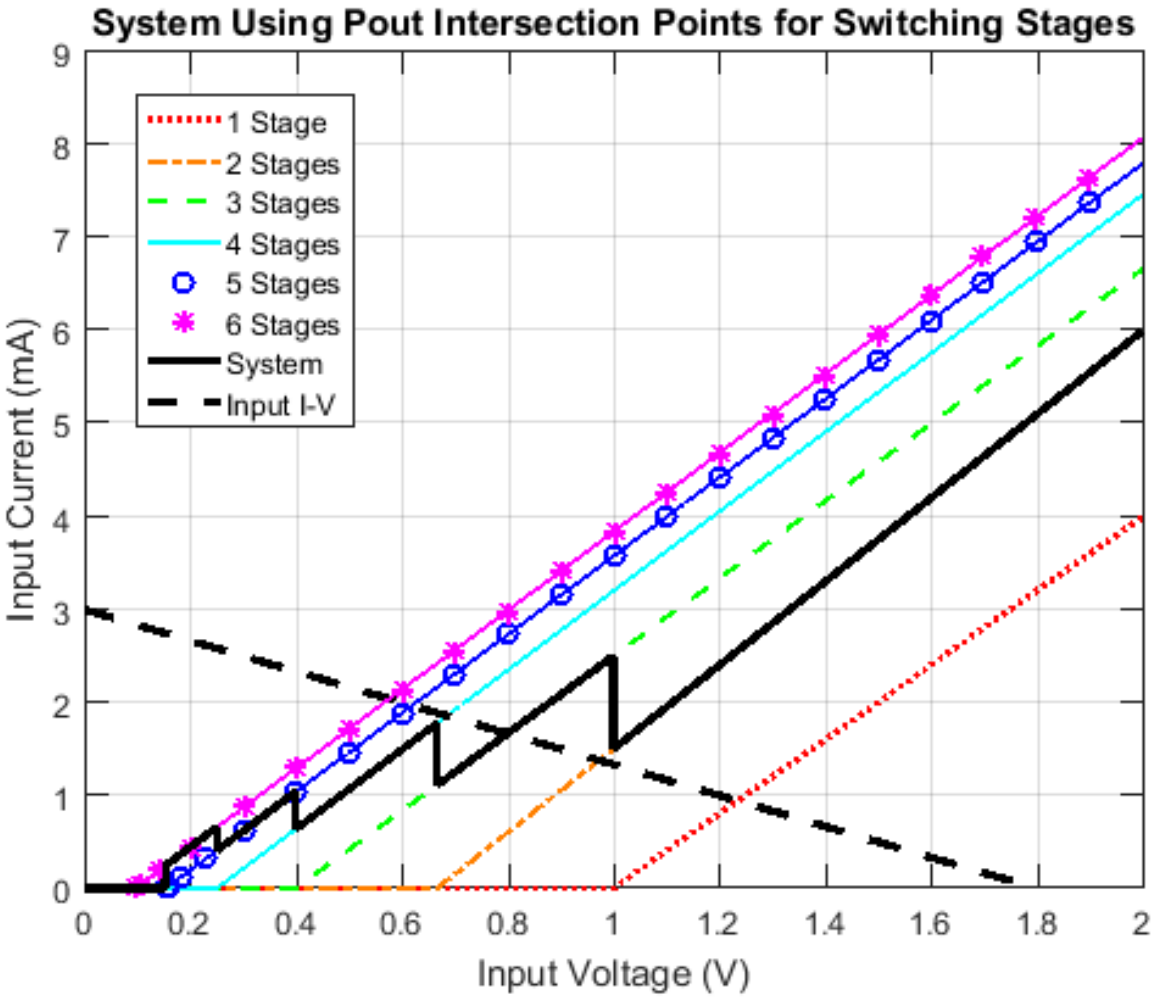


Figure 4-16: Charge pump load lines of various enabled stages against input of 1.8 V with 600-Ω source impedance, and the ideal theoretical system load line with thresholds chosen solely based on output power.

input voltage lower than this simply did not turn on the charge pump. The input resistance for the designed system can be seen in the top-left plot of Figure 4-17.

Since increasing Cf pushes the input resistance curve downward but does not affect the efficiency curve, this allows for higher average efficiencies with the same R_{max} value. However, by simply increasing Cf and maintaining a similar R_{max} value, the range of input resistances becomes larger, regardless of what the average input impedance is. This means the charge pump may perform very well with one input power but poorly with another. Therefore, keeping the range of input impedances small is also important. In the built system, an R_{max} of 900 Ω and a Cf of 10 nF times 100 kHz were chosen. This resulted in an average impedance of 597.2 Ω, very close to the goal of 600 Ω from Section 4.1. All theoretical ideal plots of the built system are shown in Figure 4-17. It is important to note that this analysis is the same regardless of parasitics because it is assumed that the parasitic losses only affect the output power and efficiency, not the input resistance and input power.

This method provides a simple and flexible way of choosing threshold values that function over a wide range of input powers with varying rectifier impedances. However, it is still worth examining the precise equations that govern output power. Figure 4-18 shows the model of the rectenna to the charge pump, where the charge pump is modeled by a variable input impedance and a variable output current. The charge pump outputs current to a fixed output voltage. Its output current and input impedance equations can be found in Table 4.2 and are repeated here following the notation of Figure 4-18.

$$I_{out} = \frac{1}{F_n F_{n+1}} Cf(F_{n+2}V_{CP} - V_{out}) \tag{4.5}$$

$$R_{CP} = \frac{F_n F_{n+1}}{F_{n+2}^2 Cf} \cdot \frac{F_{n+2}V_{CP}}{F_{n+2}V_{CP} - V_{out}} \tag{4.6}$$

The charge pump input voltage V_{CP} can be found by a simple voltage divider equation.

$$V_{CP} = \frac{R_{CP}}{R_{CP} + R_{RF}} V_{RF} \tag{4.7}$$

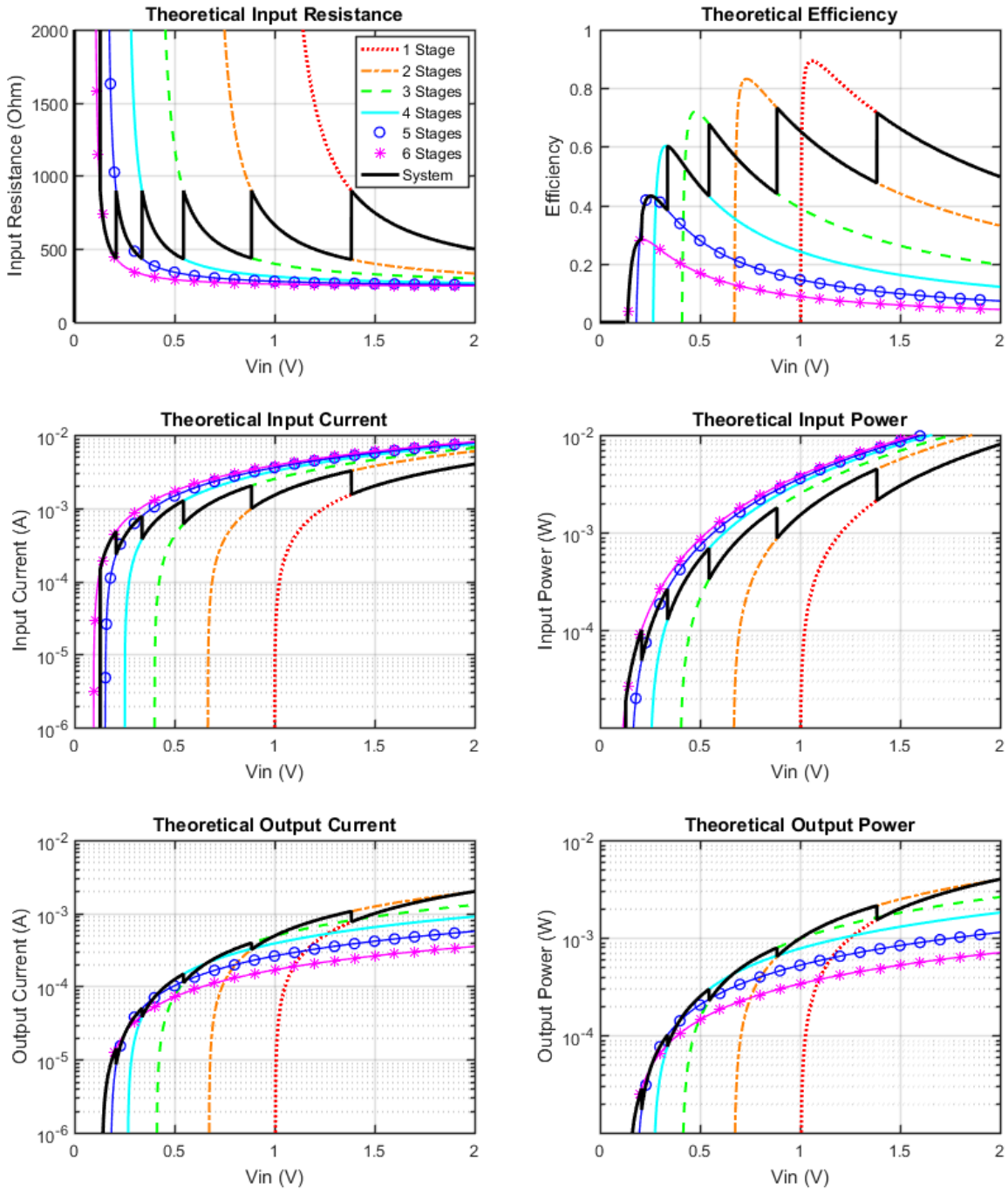


Figure 4-17: Theoretical behavior with parasitics of charge pump as in Fig 4-12 but also with the system changes in number of enabled stages based on input voltage. Maximum input resistance is 900 Ω and the average input resistance is 597.2 Ω.

By substituting Equation (4.7) into Equation (4.6) and solving for R_{CP}, R_{CP} is found to be

$$R_{CP} = \frac{F_n F_{n+1} V_{RF} + F_{n+2} C f V_{out} R_{RF}}{F_{n+2} C f (F_{n+2} V_{RF} - V_{out})} \tag{4.8}$$

$$\lim_{Cf \to \infty} R_{CP} = \frac{V_{out} R_{RF}}{F_{n+2} V_{RF} - V_{out}} \tag{4.9}$$

Similarly, by substituting Equation (4.6) into Equation (4.7) and solving for V_{CP}, V_{CP} is found to be

$$V_{CP} = \frac{R_{RF} F_{n+2} C f V_{out} + F_n F_{n+1} V_{RF}}{F_n F_{n+1} + R_{RF} F_{n+2}^2 C f} \tag{4.10}$$

$$\lim_{Cf \to \infty} V_{CP} = \frac{V_{out}}{F_{n+2}} \tag{4.11}$$

By substituting Equation (4.10) into Equation (4.5), the output power is found to be

$$P_{out} = V_{out} I_{out} = \frac{C f V_{out} (F_{n+2} V_{RF} - V_{out})}{F_n F_{n+1} + R_{RF} F_{n+2}^2 C f} \tag{4.12}$$

$$\lim_{Cf \to \infty} P_{out} = \frac{V_{out} (F_{n+2} V_{RF} - V_{out})}{F_{n+2}^2 R_{RF}} \tag{4.13}$$

By using Equation (4.8) for R_{CP} and Equation (4.12) for P_{out}, the efficiency is found to be

$$\eta = \frac{P_{out}}{V_{RF} I_{in}} = \frac{P_{out}}{V_{RF} \frac{V_{RF}}{R_{RF} + R_{CP}}} = \frac{V_{out}}{F_{n+2} V_{RF}} \tag{4.14}$$

Equation 4.12 shows that the output power is theoretically greatest when Cf is infinity, also seen in Figure 4-19. However, C is constrained by the integrated circuit area, and increasing f increases parasitic switching losses. Therefore, simply increasing Cf without bound will not maximize output power. Furthermore, while increasing Cf theoretically maximizes output power, it does not mean the charge pump is impedance-matched to the rectenna. While maximizing the output power may be the only goal in some applications, the antenna can sometimes be used for other applications in addition to energy harvesting. One example is using the antenna for backscatter communication. In this case, minimizing load variation is important to minimize interference with the backscatter communication circuitry.

The output power can also be plotted for a fixed Cf and R_{RF}. Figure 4-20 shows the output power and input resistance into the charge pump for an infinite Cf product. In this system, the threshold voltages can be chosen to follow the output power curve, since this analysis does take into account the rectenna Thevenin resistance. However, assuming Cf is high enough that it approximates the limit-behavior, there are two problems with this method. Firstly, the impedance of the rectenna changes with received RF power, so the threshold voltages would also change. Secondly, the input resistance into the charge pump ranges from 371 Ω to 1.066 kΩ. This is much larger than the system designed in Figure 4-17 (434 Ω to 900 Ω). Therefore, for this application, the previous method with a resulting system curve as shown in Figure 4-17 is appropriate.

After designing the input voltage thresholds, the controller was simulated using logic statements in SPICE. Comparator outputs were sampled every 3 μs, in order to avoid possible instability caused by transients from switching to a different number of enabled charge pump stages. In the actual FPGA implementation, the comparators were sampled every 1 ms. The Thevenin equivalent for the SMSA7630-061 simulated rectifier with a 0.9-V RF source is plotted against the designed charge pump system in Figure 4-21. This plot predicts an operating rectified voltage of 0.6726 V, which would produce 454.3 μW of output power to the 2.0-V load. When the controller was simulated in SPICE, at steady-state, the system operated at an average rectified input voltage of 0.6705 V and an average output power of 453.6 μW to the load. Figure 4-22 shows the transient plots for the system starting at turn-on up to steady-state. The system gradually changes from a 6-stage charge pump to a 3-stage charge pump when it finally reaches steady-state at the operating point predicted in Figure 4-21.

The actual controller was built using a Spartan 6 XC6SLX9 FPGA on a Mojo V3 development board and 6 LTC1540 nanopower comparators to compare the rectified voltage against 6 thresholds. The FPGA sampled 6 digital inputs from the comparators every microsecond and output 24 digital signals to the 6 TS3A4751PWR ICs that composed the charge pump. The values of the expected voltage thresholds from the system shown in Figure 4-17 and the measured thresholds for the built system

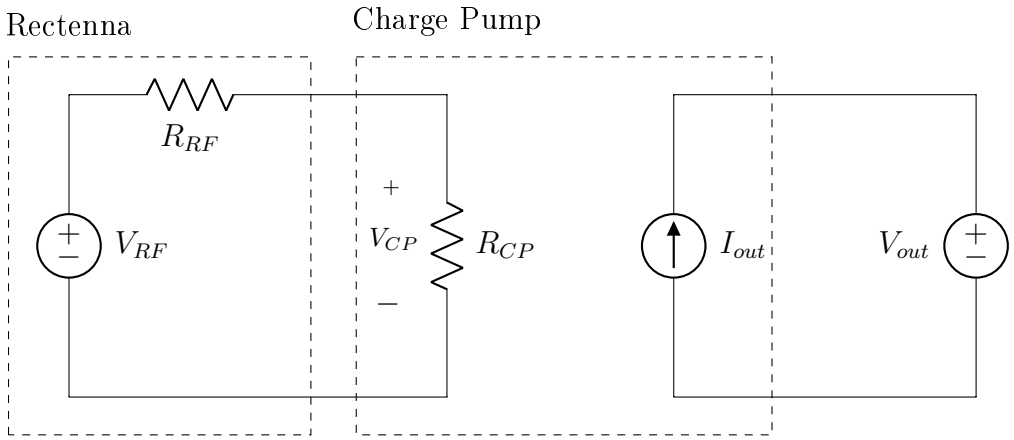


Figure 4-18: Thevenin equivalent of rectenna (V_{RF} and R_{RF}) to model of charge pump (R_{CP} and I_{out}) to locked output voltage (V_{out}).

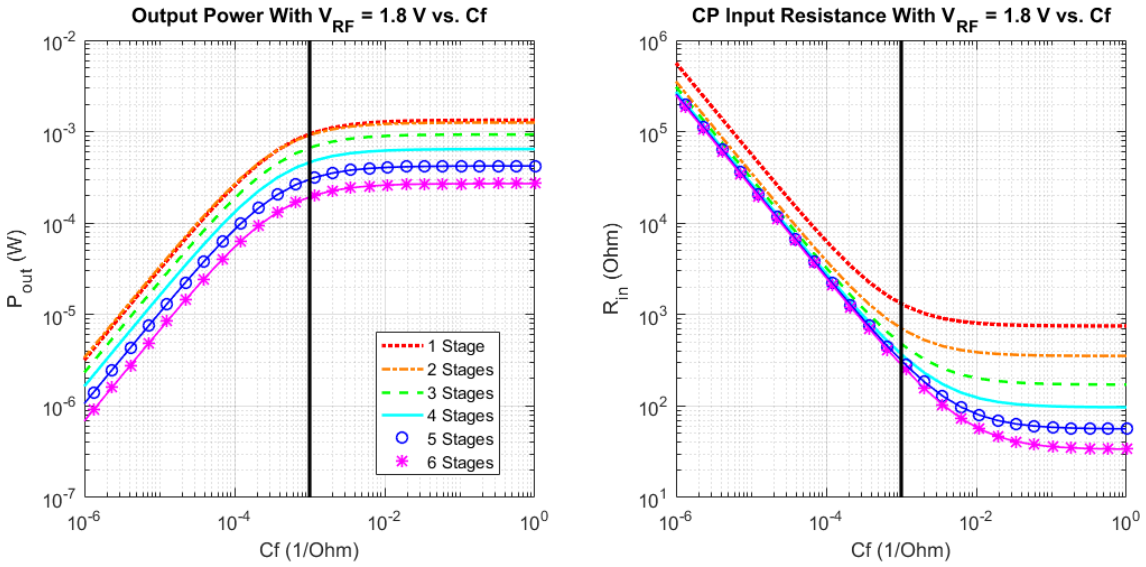


Figure 4-19: Output power and charge pump input resistance vs. Cf product for a V_{RF} of 1.8 V and R_{RF} of 600 Ω.

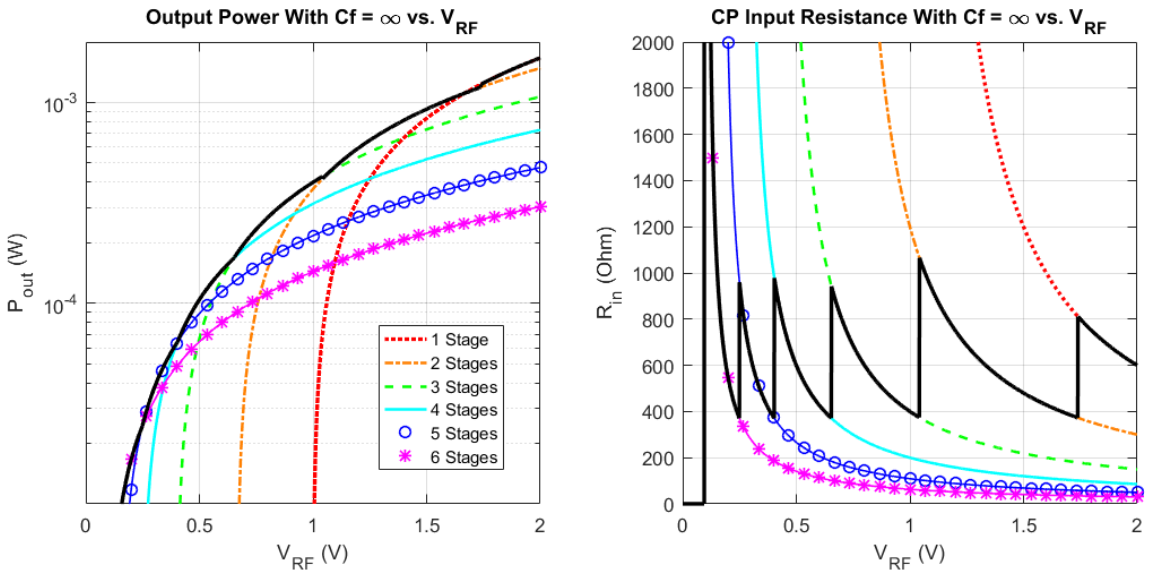


Figure 4-20: Output power and charge pump input resistance vs. V_{RF} for infinite Cf product and R_{RF} of 600 Ω.

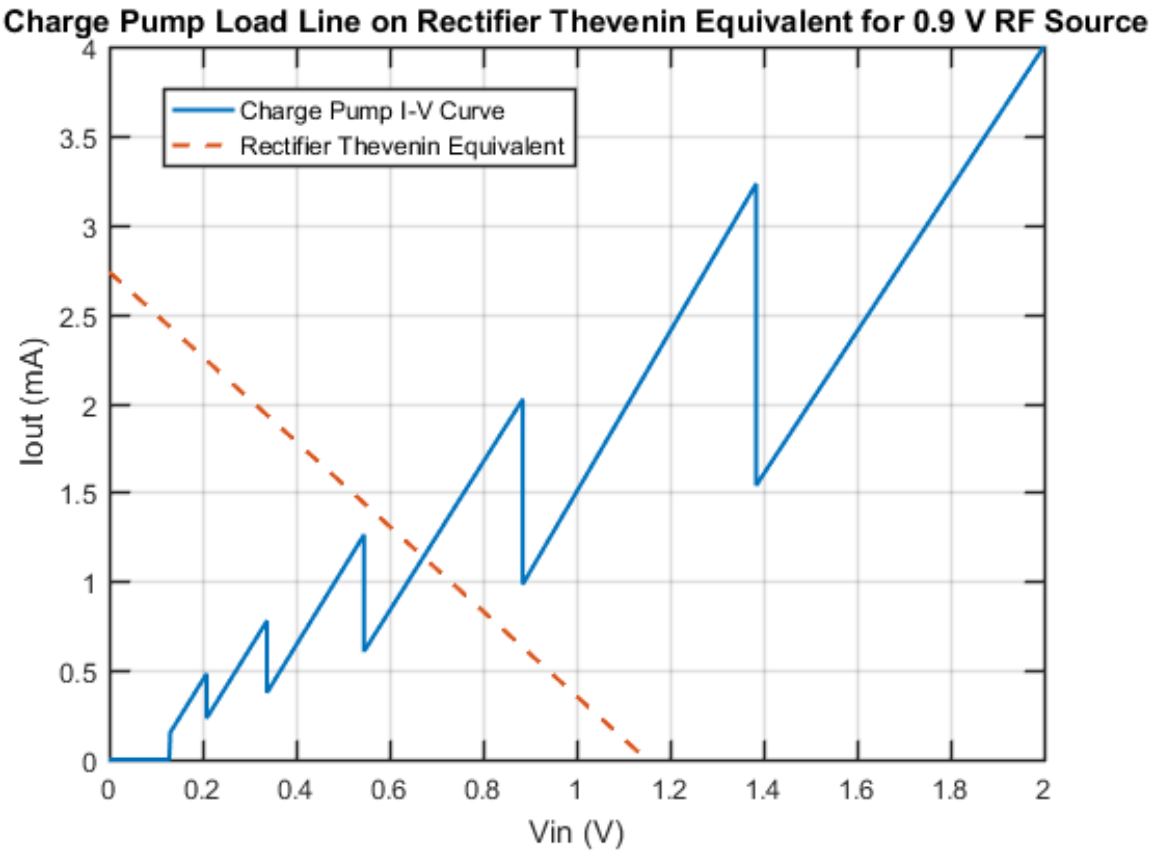


Figure 4-21: Predicted steady-state operating point of 0.6726-V rectified voltage determined by imposing system-level charge pump I-V curve onto Thevenin equivalent of 0.9-V amplitude RF source.

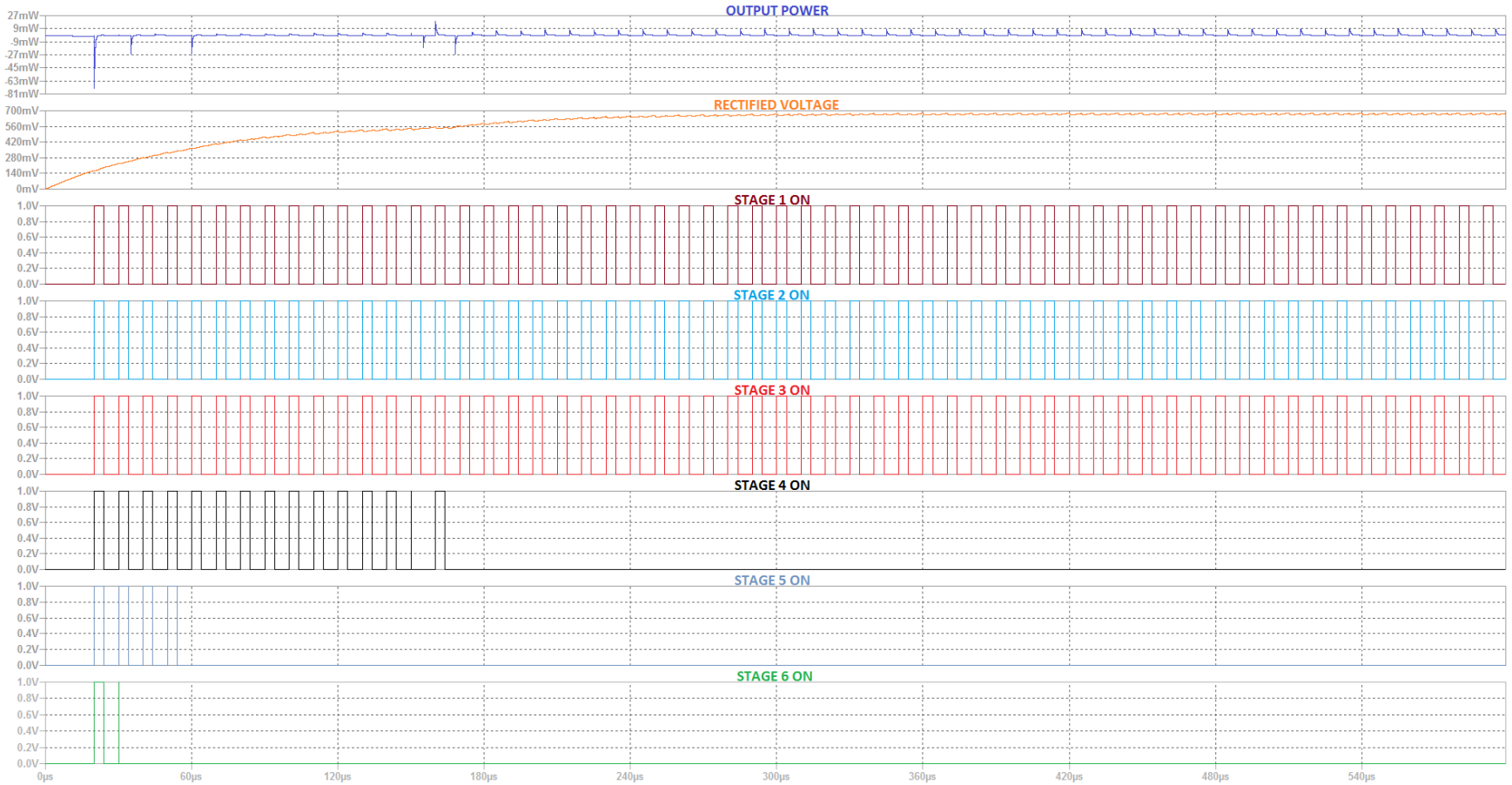


Figure 4-22: Transient results of SPICE simulation of 0.9-V amplitude RF source into rectifier-charge pump circuit. Oscillating "STAGE ON" signals indicate how many stages are enabled at a specific point in time.

Table 4.4: Expected vs. measured comparator trigger voltages for charge pump controller.

Comparator	1	2	3	4	5	6
Expected Threshold Voltage (V)	1.388	0.887	0.548	0.338	0.209	0.130
Measured Threshold Voltage (V)	1.380	0.885	0.550	0.337	0.202	0.133

are shown in Table 4.4. All differences are less than or equal to 8 mV, indicating that the built controller behaves very closely to the designed controller.

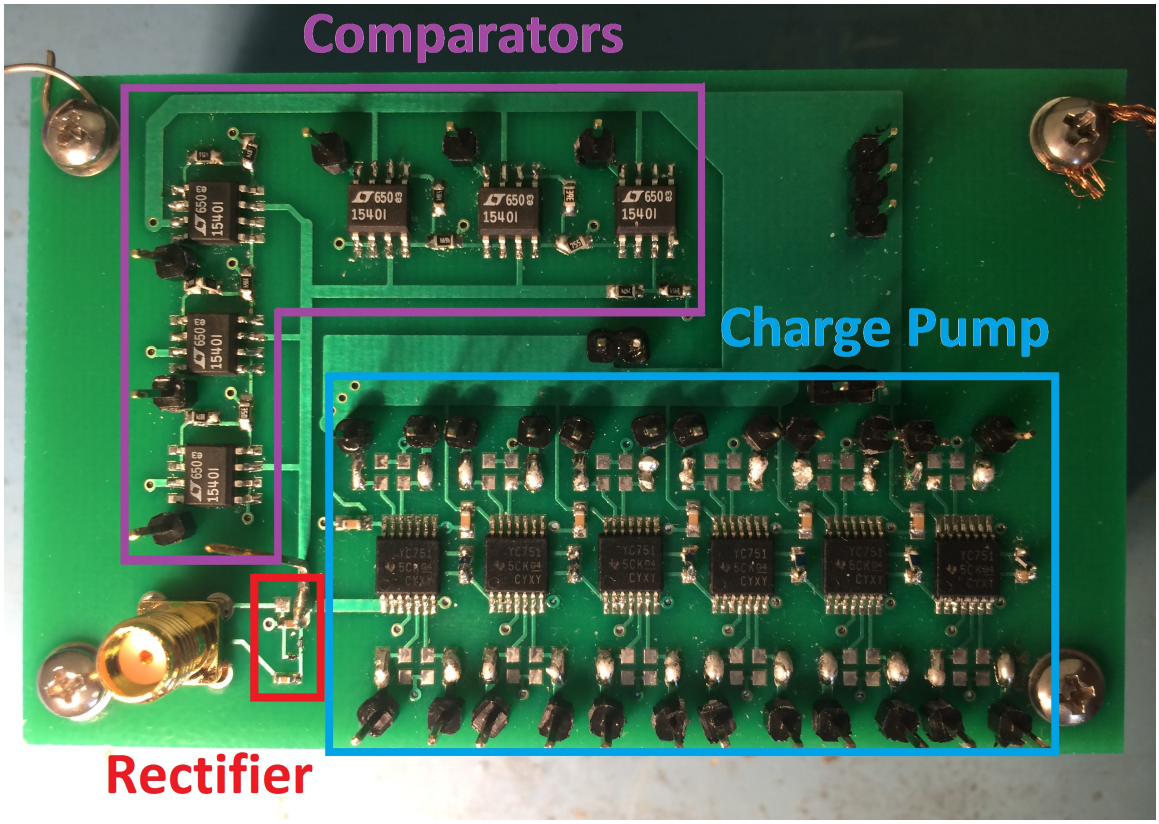
After having the charge pump designed around the RF rectifier and its expected input voltages, simulating the system and its controller, and having a physical controller that behaved very closely to the ideal, the entire system could then be physically tested with various input powers. The built charge pump is shown in Figure 4-23a, and the complete RF Harvester system is shown in Figure 4-23b. In the top plot of Figure 4-24, the system I-V load line of the charge pump is plotted against the measured SMSA7630-061 rectifier I-V curves with 2.0-V, 0.9-V, 0.4-V, and 0.2-V RF input voltage amplitudes discussed in Section 4.1. Note that a log-Y plot is used due to the large range of currents. The bottom plot illustrates the measured charge pump output power to the 2.0-V load with the operating points marked. The 0.4-V RF source intersects the charge pump load line at 3 different points, while the 0.2-V RF source intersects the charge pump load line at a point on the cusp of the charge pump turn-off threshold. This suggests that the 0.4-V RF source could operate at any of the three intersection points (though the middle point would only occur in transition between the outer two points), and that the 0.2-V RF source will likely not produce any usable output power if it turns the charge pump on at all. Table 4.5 shows how much power can actually be delivered to the charge pump based on measurements of the actual rectifier, the power delivered to the charge pump from the rectifier in the measured complete system, the percentage of how much power that could be delivered

Table 4.5: Power delivered to the charge pump from the rectifier in the built system with the controller (P_{CP}) vs. the measured maximum power that actually can be delivered to the charge pump during exact matching ($P_{CP,max}$) for different input powers.

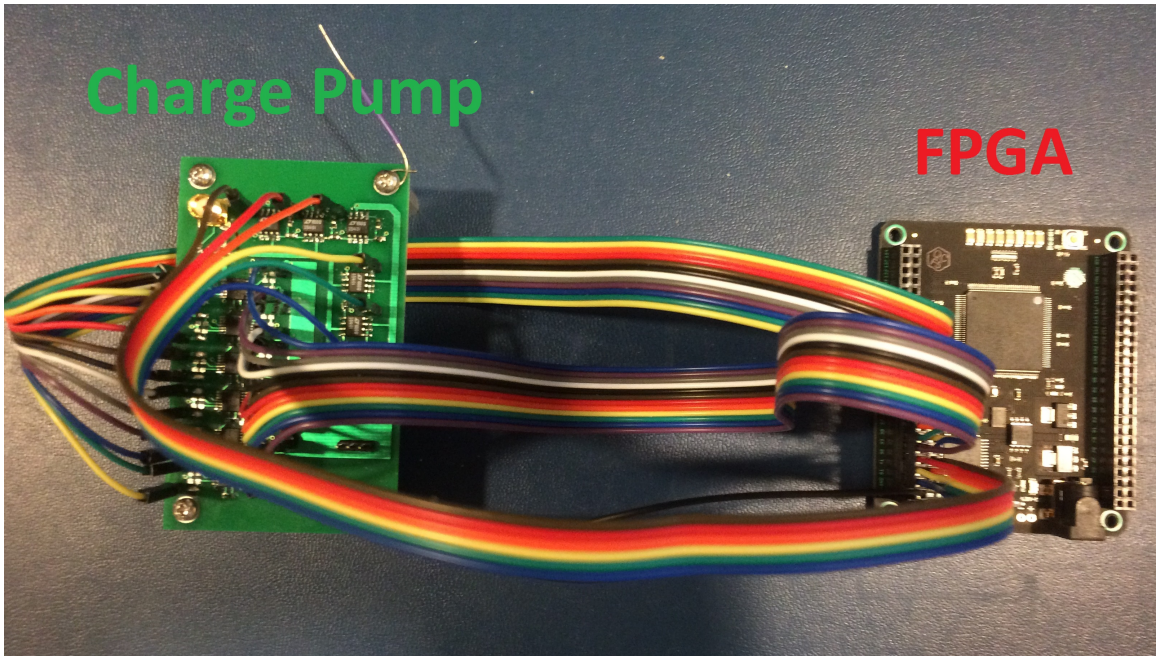
Amplitude	2.0	0.9	0.4
RF Power (dBm)	10	3.06	-3.98
RF Power (mW)	10	2.023	0.4
Measured $P_{CP,max}$ (mW)	4.367	0.6574	0.06895
System P_{CP} (mW)	4.12	0.6284	0.0674
% to $P_{CP,max}$	94.34%	95.59%	97.75%
P_{out} to 2.0-V Load (mW)	2.52	0.374	0.0318

to the charge pump actually is, and how much power is delivered to the 2.0-V load. If the charge pump was perfectly matched to the rectifier's impedance, then the "System P_{CP}" entry would be exactly that of "Measured $P_{CP,max}$" and the "% to $P_{CP,max}$" entry would be 100%. The "% to $P_{CP,max}$" row therefore indicates how closely the charge pump controller impedance-matches to the rectifier. With the exception of the 0.2-V RF source, the charge pump is matched at least 94%, indicating that the controller does an exceptional job matching the charge pump to the RF rectifier over various input powers. As stated, the 0.2-V RF source was on the cusp of the charge pump's turn-off voltage, and thus minute amounts of power were actually drawn. In order to minimize disturbances on the system, the input power to the charge pump was not physically measured. Instead, the rectified voltage was measured, and the input power to the charge pump was extracted from the middle-right plot of Figure 4-13. However, the output power to the 2.0-V load was actually measured.

Table 4.6 shows, for an RF source input into the complete RF harvester, the error between the output power to the load expected from the intersection points of Figure 4-24 and the output power to the load actually measured. The 0.4-V RF source was assumed to have been operating at the 5-stage intersection point. These results suggest that using a load line approach to estimate where the RF rectifier will operate



(a) PCB of configurable Fibonacci charge pump with the rectifier, charge pump, and comparators labeled.



(b) Interfacing between charge pump PCB and FPGA. PCB outputs comparator values to FPGA, and FPGA sends charge pump clock signals back to charge pump.

Figure 4-23: Physical discrete RF harvester PCB and interface to FPGA.

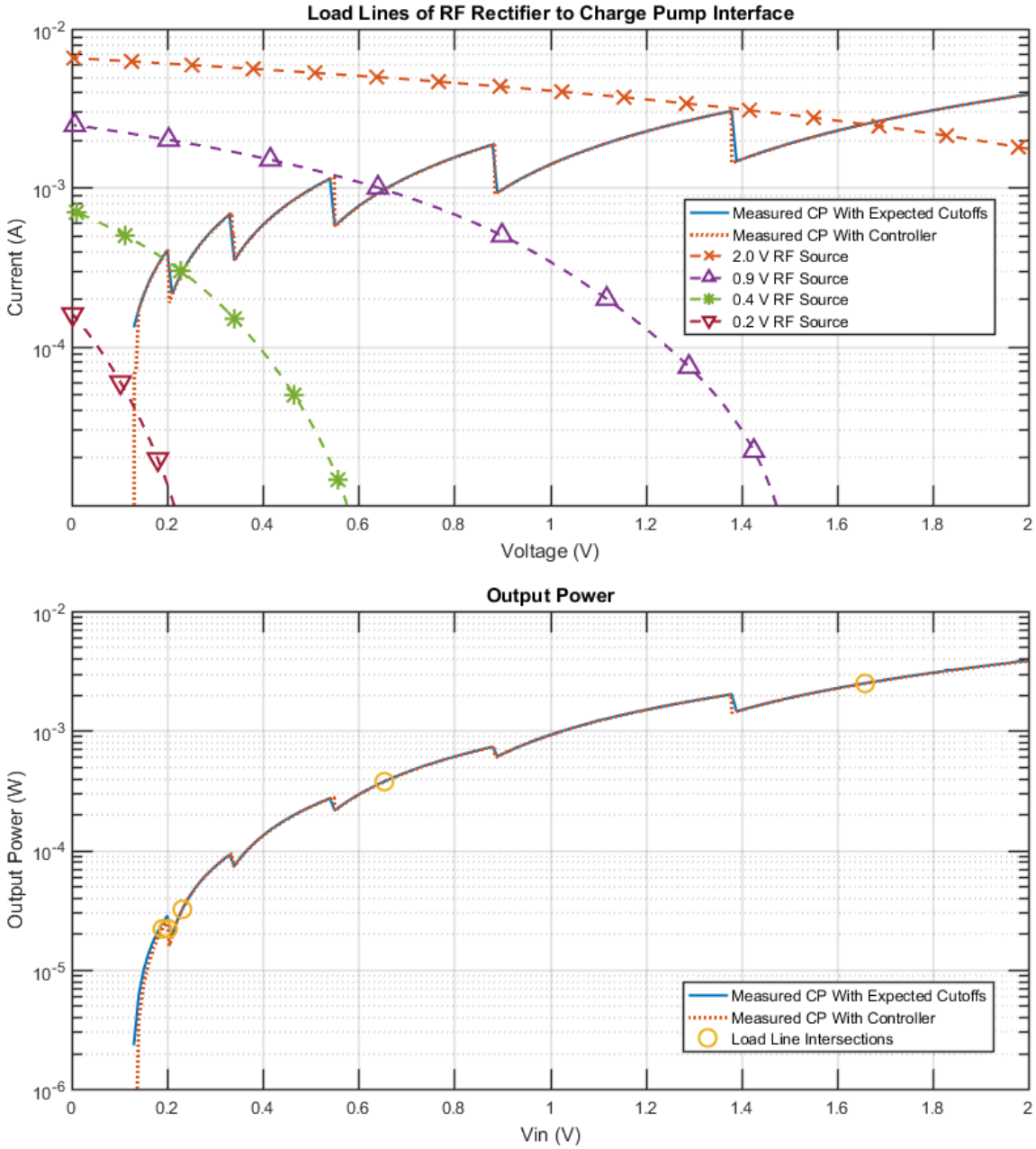


Figure 4-24: Measured charge pump load lines across measured rectifier for 4 different power inputs (top). Resulting output powers at marked intersection points (bottom). Log-Y plots used for large range of currents and powers. 0.4-V RF source contains 3 operating points with the charge pump.

Table 4.6: Expected output power to 2.0-V load in entire system based on simulated SMSA7630-061 rectifier vs. measured.

RF Voltage Amplitude (V)	**Expected P_{out} (μW)**	**Measured P_{out} (μW)**	**Error**
2.0	2487	2520	1.33%
0.9	374.2	374	-0.05%
0.4	31.91	31.8	-0.34%

with the charge pump produces very accurate predictions and that the overall system behaves very closely to its design.

4.4 Performance of Charge Pump within Entire Multi-Source Harvesting Architecture

Lastly, to check how the RF harvester will actually behave with an LDO replacing the voltage source, the RF-charge pump output was attached to a 500-Ω load powered by a 2.5-V voltage source attached to a 2.0-V LDO. The 2.5-V voltage source represents an arbitrary voltage on V_{stor} provided by the solar harvester as discussed in Chapter 3. The expected output current from the charge pump is just what was measured previously when the charge pump output was attached to a 2.0-V source. The output current of the 2.5-V source with the RF harvester is expected to be the current draw from the 2.5-V source without the RF harvester minus the expected current provided by the RF harvester. Table 4.7 shows the results of the experiment and the associated error. The LDO behaves very closely to an actual 2.0-V source, suggesting that the RF harvester in the entire multi-source harvester will behave very closely to what is predicted.

Table 4.7: Performance of RF harvester when replacing 2.0-V voltage source load with a resistive load and a 2.0-V LDO.

RF Voltage Amplitude (V)	**2.5-V Source Current Output w/o RF Harvester (mA)**	**2.5-V Source Current Output w/RF Harvester (mA)**	**Measured Current Decrease of 2.5-V Source (mA)**	**Expected Current Decrease of 2.5-V Source (mA)**	**Error**
2.0	4.045	2.7875	1.2575	1.26	-0.20%
0.9	4.045	3.8558	0.1892	0.187	1.18%
0.4	4.045	4.0291	0.0159	0.0159	0.00%

4.5 Summary and Design Discussion

The results presented in this chapter demonstrated very positively an impedance-matching charge pump that outputs current to a fixed-voltage output created for a multi-source energy harvester. The errors of the charge pump behavior were typically contained within a 10% bound, the controller impedance-matched to the RF rectifier to at least 94% for the tested values, and the RF harvester in a multi-source environment behaved as predicted with errors less than 1.2% for tested values. This section discusses design choices and how different parameters can be changed for different applications.

LTC1540 nanopower comparators were used for the controllers with resistor dividers around 10 MΩ each, so the power supply current draw was dominated by the analog multiplexers. As a result of using nanopower comparators, the comparators had relatively slow response times. In the tested system, a 22-μF ceramic capacitor was placed at the rectified voltage node. By using a large capacitor, slower nanopower comparators were appropriate. This prevented the charge pump's input voltage from changing so quickly that the controller could not respond in time. Having a quickly varying input voltage to the charge pump is especially dangerous if it drops below the

minimum input voltage for the current number of enabled stages. This would cause the output voltage to source power to the charge pump input, resulting in negative efficiency. The cusp of this occurs when the efficiency equals 100%. Therefore, the slower the comparators and the slower they are sampled, the larger the capacitor on the rectified voltage node must be.

As the efficiencies for higher numbers of stages are more affected by parasitic capacitances, having the lowest number of stages possible, and therefore the lowest fixed output voltage possible, results in best performance. In this particular system, since there is a 1.8-V rail available, it would be more efficient to use that as the output of the charge pump. However, since the 1.8-V rail is anticipated to not consume very much control power, in order to demonstrate use with a large range of RF input powers, the 2.0-V main output rail was used. This is because the RF harvester's output power must be less than the power draw of the load on the rail in order for an LDO to mimic a constant voltage output.

If it turns out that the Cf product cannot be integrated because the capacitors are too large or the frequency results in too high of losses, then one option is to add another RF multiplier stage. This would allow the optimal impedance of the rectifier to increase and thus the Cf product to decrease, meaning the frequency could be lower and still be impedance-matched. This would likely further degrade efficiency, however, since it would add more non-ideal diode drops. The specific effects on efficiency would need to be tested further if such an option is chosen.

Along the lines of using another RF multiplier stage, if the application finds that a higher number of charge pumps particularly affected by parasitics are consistently being used, simply adding another RF multiplier stage could allow the charge pump to operate with a lower number of stages. This would be beneficial because, as seen in the top-right plot of Figure 4-13, the efficiencies due to parasitics have greater effects on charge pumps with a higher number of stages. When the system efficiency curve starts to operate over the humps seen in these plots, the effectiveness of certain input voltages of these stages is negatively affected.

One of the most important contributions of the proposed RF harvester is its very

low area. By using a Fibonacci charge pump, the system uses the minimum number of integrated capacitors possible. Perhaps more importantly, it works without the use of a discrete impedance-matching network. This is substantial since most discrete inductors use 0603 packages or larger. Furthermore, because the system is designed around a range of impedances and since the threshold voltages are not near the minimum-operating-voltages of each stage, the system is not particularly sensitive to small variations in C or f.

Chapter 5

Conclusion

5.1 Summary

This thesis proposed, analyzed, and tested a combined solar and RF power harvesting and management circuit. Its motivation was to minimize system weight while maximizing output power and operating time for a specific dragonfly measurement and optogenetic stimulation system. The purpose and unique challenge of this design was to create an incredibly lightweight system capable of running sensors and stimulators at the milliwatt level. The project studied various energy storage methods to allow system operation during moments without ambient or transferred power. It also examined circuit methods to minimize weight, such as using fully-integrated switching converters, using inductor-less voltage regulators, and reusing discrete inductors. This thesis created a 162-mg supercapacitor-powered system capable of powering a 2-V load at up to approximately 2-3 mW, and a 150-mg battery-powered system capable of powering a 2-V load at up to 6 mW using a multi-source solar and RF energy harvester. The multi-source harvesting system used a unique approach of categorizing the harvesters as primary and auxiliary harvesters due to the power constraints on each in relation to the high load demand.

In Chapter 1, previous work on animal neural stimulators and recorders, solar MPPT harvesters, RF harvesters, and multi-source harvesters was investigated and discussed. The results showed a limitation on the weight-to-output-power relation

on current neural recorders and stimulators that this project, when developed as an integrated circuit, is predicted to exceed. These specific weight estimates were discussed in Chapter 3.

In Chapter 2, the overall system architecture was defined. It was determined to use an inductor-based boost converter for the solar harvester and an SC converter for the RF harvester in order to minimize weight with only a minor decrease in maximum output power. The theoretical efficiencies of shared-inductor-based and LDO-based converters were derived, showing the LDO-based design to theoretically have a higher maximum output power for a given input power (Chapter 2.2). In order to use a very low-power and low-area controller, a simple hysteretic controller based on outputs of comparators on V_{stor} was described for the LDO-based design (Chapter 2.3). The RF harvester was approached as an auxiliary, low-power harvester for the high-power load and is most naturally placed at the output voltage to maximize output power and efficiency (Chapter 2.4).

In Chapter 3, an FOCV MPPT method was chosen for its simplicity and compatibility with the solar cells that will be used (Chapter 3.1). In Chapter 3.2, the supercapacitor-based system was developed and discussed. The system was built with a highly efficient buck converter discharger (Chapter 3.2.2). For simplicity, the buck converter was run at a fixed duty cycle to charge up V_{stor}. The discharger system in general showed degraded capacitance with high load currents. However, the system retained a higher capacitance for low currents. The full system was then developed and shown to operate over a wide range of input powers (Chapter 3.2.3). It made use of modular and very simple controllers to limit power consumption and area in an integrated design. The total system was estimated to have a mass of 162 mg without the RF harvester (Chapter 3.2.4).

In the latter part of Chapter 3, the battery-powered system was analyzed. Lightweight, rechargeable CBC050 batteries were cycle-tested (Chapter 3.3.1). The results showed 1 mA/battery (20C discharge rate) to be an appropriate maximum discharge current for the batteries. A system with three batteries was able to last around 8 min for an I_{diff} of 1 mA and about 2.9 min for an I_{diff} of 2.5 mA (Chapter 3.3.3). After 43

discharge cycles, the batteries still performed at 93% of their original discharge time. The current-source discharger, while less efficient, allowed the system to continue harvesting while discharging the batteries and did not need several power switches and more complex controls for inductor-sharing. Like the supercapacitor-powered system, the battery-powered system was shown to operate over a wide range of input powers and used a simple and modular control system (Chapter 3.3.4). The fully integrated system was estimated to have a mass of 150 mg without the RF harvester (Chapter 3.3.5).

In Chapter 4, the RF harvester was developed and analyzed. As an auxiliary harvester that harvests mainly low energy levels, there were a few constraints placed on the system. Firstly, the RF harvester had to consume a very small area to minimize weight and allow more area for the primary solar harvester and the power management circuits. Secondly, its control circuitry had to consume very low power in order to effectively harvest lower energy levels. Lastly, the charge pump had to minimize its effects on other functions the antenna may serve, such as backscatter communication. A self-impedance matching Fibonacci charge pump was chosen to minimize the number of capacitors and thus area and weight (Chapter 4.2). Though the charge pump could be integrated, the rectifier was designed to be made of discrete Schottky diodes, as the integration process did not have high-quality diodes (Chapter 4.1). A 50-Ω source generator was used to represent the receiving antenna. The RF rectifier was determined to have a matched impedance of approximately 600 Ω as a middle value between the various input powers. The charge pump system was very simple with the number of enabled stages changing by monitoring the input voltage with a series of comparators (Chapter 4.3). The threshold voltages for the charge pump were chosen by keeping the input impedance below a maximum level and tuning Cf to keep the average input impedance at 600 Ω. The charge pump successfully and very accurately harvested energy from three tested input powers (10.0 mW, 2.0 mW, and 0.4 mW), with a rectenna match greater than 94% for all three tested input powers. Lastly, the RF rectifier output voltage source was replaced by an LDO to demonstrate the harvester's behavior in a multi-source harvester (Chapter 4.4).

5.2 Conclusions

Several conclusions were drawn from the analyses and tests conducted as part of this thesis. These are particularly important for development of an ASIC implementation and future work in improving the system, as well as illustrating the benefits of this system.

In Chapter 2, an analysis of ideal harvesting circuit topologies showed that the LDO-based design could theoretically output higher power to the load for a given input power than the shared-inductor design could. Another advantage to the LDO-based system is that in steady-state, the LDO-based design showed no AC current waveform on the V_{stor} capacitor or supercapacitor. As the capacitance value of supercapacitors and high value ceramic capacitors tend to be highly dependent on frequency, the LDO-based design was much more immune to this problem than the shared-inductor design that by definition creates an AC waveform on the V_{stor} capacitor.

Regarding the supercapacitor-powered system in Chapter 3.2.2, the buck converter showed substantial ringing on the supercapacitor voltage, which was likely due to the series resistance of the capacitor. When designing the inductor-sharing discharger system in an integrated circuit, care must therefore be taken to properly model the supercapacitor for accurate simulations. Next, even with a very simple control system of using a fixed 90% duty cycle, this system demonstrated very high efficiencies and properly charged V_{stor} when the supercapacitor was sufficiently charged. This simple controller is desirable because it will likely use less power and consume less area in an ASIC than a more complex controller. One of the most important findings of this section was how sensitive this system was to the AC current imposed on the supercapacitor. For extended periods of harvested power deficiency compared to the output power, this control system could cause the current draw on the supercapacitor to look like an AC waveform with a fundamental frequency in the approximate range of 1-20 kHz. Supercapacitors' frequency dependence could dramatically inhibit the operating time of this system during harvested power deficiency. Furthermore, DC

current draw tests showed that the effective capacitance on the specific supercapacitor used (XH414HG-IV01E) decreased dramatically with increased load current. Overall, this specific discharger system is unable to support loads greater than 1.5 mA for reasonable amounts of time. One important positive quality of this system is that supercapacitors are able to sustain very short and infrequent pulses of current, which could easily damage batteries. With LEDs in particular, this system retains the supercapacitor at a higher voltage that could be necessary for providing pulses to optogenetic stimulators.

The battery-powered system of Chapter 3.3 also made important conclusions, particularly for the discharger of Chapter 3.3.3. This section showed that using parallel CBC050 batteries with a safe amount of discharge current in a buck converter is problematic because limiting the current with a current-limiting resistor greatly reduces the efficiency of the buck converter. By using a current-monitoring system to keep the buck converter efficiency at the ideal 100%, the maximum output load current is limited. A simple current source maximizes possible output power and allows the solar harvester to still operate while the discharger operates, further increasing the maximum possible output power. Therefore, partially decreasing operation time allows higher load power. Still, with an I_{diff} of 1 mA, the system was still able to operate for over 8 min. Next, as the battery tests illustrate that the internal battery resistance changes over time, monitoring the battery depletion by monitoring the open-circuit voltage is a much better indicator than monitoring the loaded voltage. However, if the battery discharger remained on for too long (e.g. when $I_{diff} \approx I_{batt}$) then another comparator is needed to monitor the loaded voltage to shut off the system. This prevented the batteries from over-depleting. Degradation of the batteries was 7% after 43 full discharges, using total discharge time in the system as a metric. To choose between a longer discharge time or less degradation over cycles, the battery discharge threshold and the discharge current can simply be tuned to empirically determined values.

Some conclusions were common to both the supercapacitor-powered system and the battery-powered system. Modularizing the system allowed for a few independent,

low-power, simple control systems as opposed to a single large and complex controller. In both the battery-powered system and supercapacitor-powered system, the charger, discharger, and MPPT converter all operated separately. As discussed in Chapter 3.2.3, the addition of a precision shunt regulator at V_{stor} to protect the system from overly high input powers would also be an independent entity. The weight analyses of Chapter 3.2.4 and 3.3.5 showed that the system weight was dominated by the solar cell, packaged ASIC, supercapacitor or batteries, and flexboard. Having an unpackaged ASIC would dramatically reduce weight but may not be possible for the application. Since the chargers of Chapters 3.2.1 and 3.3.2 only operate in times of excess energy, their efficiency is less important than optimizing other parts of the design. Improving efficiency in these components simply decreases charge time. Lastly, during cold start in the supercapacitor-powered system, the solar cell had to have a relatively high input power to overcome the quiescent current draw of the circuitry at under-voltage levels (Chapter 3.2.3). If the system needs to be able to start up with low input-power levels, then care should be taken to address under-voltage current draw of the components on V_{stor}. While this same effect was not noticed in the battery-powered system, it could very well become a problem with a different transistor-level architecture in the integrated circuit.

Some of the most innovative findings of this thesis work were in the RF harvester of Chapter 4. A fundamental idea in the RF harvester was that locking the output voltage using an LDO simplified the impedance-matching calculations to be able to very accurately predict the charge pump impedance by merely monitoring the rectified voltage. These formulas for input resistance and as well as for parasitic analysis were developed in Appendix B. The parasitic losses from the switches' input capacitances are shown to improve with increasing C values and is theoretically independent of f (Chapter 4.2). Therefore, increasing the capacitor size in the integrated circuit will improve the efficiency closer to the ideal and will also decrease f for a constant Cf product, decreasing gate losses. However, this does not take into account the parasitics that are unique to integrated circuits (e.g. top- and bottom-plate capacitances). The errors between measurements and the theoretical models with parasitics

show errors within a 10% bound, typically much less, as shown in Figure 4-14. This suggests a valid parasitic model.

As seen in Chapter 4.3, the method developed for choosing a maximum input resistance value and tuning Cf to create a matched average input impedance does not theoretically provide the maximum output power, though it does provide the maximum input power to the charge pump. In fact, increasing Cf theoretically always increases output power monotonically up to a limit. However, the range of the input impedance for a large Cf is larger than the method developed. Since backscatter communication will also be used on the line, minimizing the charge pump's input resistance variation is important. Next, for three different receiving antenna powers, the built discrete charge pump and controller system harvested greater than 94% of maximum power able to be harvested from the rectifier. Furthermore, by using a load-line approach by laying the measured rectenna I-V plot along the measured I-V plot of the charge pump input, the resulting errors in the predicted operating points and the measured operating points were less than 1.4%. This indicates that the load-line approach will very accurately predict the behavior of the RF harvester for a given rectenna input power. For these three tested input powers (10 mW, 2.0 mW, and 0.4 mW), the powers input to the charge pump were 4.12 mW, 0.6 mW, and 0.07 mW, respectively. At the output, this produced 2.5 mW, 0.4 mW, and 0.03 mW of output power, respectively. This shows that the rectifier in fact produces the most losses in the RF harvester and suggests that the RF harvester in this thesis has an advantage over RF harvesters made with long strings of diode-doublers.

The latter parts of Chapter 4 also made important conclusions on this system. The differences in behavior between using a 2.0-V LDO at the charge pump output and using a 2.0-V voltage source was less than 1.2%, indicating that the method of harvesting with the charge pump output power less than the load power behaved very accurately to what was intended and predicted (Chapter 4.4). The discussion of Chapter 4.5 pointed out that as the efficiencies for higher numbers of stages are more affected by parasitic capacitances, having the lowest number of stages possible, and therefore the lowest fixed output voltage possible, results in best performance. Lastly,

the RF harvester was not particularly sensitive to small changes in Cf because the system is based on an averaged impedance method.

5.3 Future Work

The work completed in this thesis can be continued in a variety of ways. Firstly, several minor adjustments and verifications in the design could be made. For example, inductor-sharing in the supercapacitor-powered system was not implemented in the discrete system for simplicity and the initial proof-of-concept. The system would need to be tested further with inductor-sharing to understand how the system dynamics would change. This would be best to simulate at the integrated circuit design phase, as the system dynamics would be very dependent on the operating frequency, actual inductor value used, and parasitics. In the discrete system, larger inductors and lower switching frequencies were used to reduce switching losses that would be more controlled in an IC. Second, even with the BQ25504's 256 ms disconnection period in its MPPT algorithm, the 22-μF capacitor on V_{stor} was able to sustain the quiescent current draw of the other components on V_{stor} before the output voltage was enabled and the discharger could turn on. After the output voltage turned on, however, the discharger would turn on during every MPPT disconnection period. In the ASIC, it would be best to sample as quickly as possible in order to sustain the load power from V_{stor} without needing to turn on the discharger. Lastly, though not necessary, the charger in Chapter 3.2.1 could have been made more efficient by using a charge pump with a gain closer to the final value of the supercapacitor. Since the maximum voltage of the supercapacitor is 3.3 V, a 3/2 charge pump from V_{stor} around 2.2 V could have been more efficient for quicker charging.

Several improvements could be made regarding the buck converter in both systems. In the supercapacitor-powered system, a buck converter discharger with a different controller may be developed to match the supercapacitor charge state and the load demands. As was previously mentioned in Chapter 3.2.2 and 3.2.5, the supercapacitor discharger at a certain point during testing switched on and did not turn off, indicating

that the 90% duty cycle was not high enough to recharge V_{stor} past the threshold. A different controller could address that problem by increasing the duty cycle as the supercapacitor depletes. Additionally, as mentioned in Chapter 3.3.6, another option for using a buck converter with the batteries is to stack the CBC050 batteries to get a higher voltage. If using three series batteries instead of three parallel batteries, for example, then the buck converter's duty cycle could be very low while still being able to charge up V_{stor}. By adding a high enough capacitor in parallel with the series-connected batteries, the current draw through the batteries could be maintained approximately at 1 mA. This would allow for the very high energy density of the batteries while still discharging them efficiently. The major problem associated with this method is that high voltage transistors would be required.

One of the most promising continuations of this research would be to combine the battery-powered system and the supercapacitor-powered system while still meeting the set power and weight goals. As discussed in Chapter 3.3.6, using two CBC050 batteries and a lighter supercapacitor than the one tested in Chapter 3.2 would allow the high energy density of batteries while still allowing pulses of current. Potential supercapacitors are the CPX3225A752D at 7 mF and 24 mg or the CPH3225A at 11 mF and 25 mg, both by Seiko Instruments. The energy storage elements together would have a mass of 56-57 mg, support higher current pulses, and supply on average 2 mA of load current.

The RF harvester could also be further continued. As the rectifier was the largest source of losses in the RF harvester, one method of improving overall efficiency could be to only use a single-stage half-wave rectifier. This would only use one diode and perhaps improve the efficiency of the RF rectifier. One problem with this is the input voltage into the charge pump would theoretically be half, and so for the same output voltage, the charge pump would not be able to harvest as low of input powers. As a result, another possible improvement is to develop a system that would change the number of rectifier stages in order to harvest higher power levels more efficiently with a "shorter" rectifier (e.g. half-wave) while still being able to harvest lower powers by switching to a "longer" rectifier (e.g. full-wave). Lastly, the RF rectifier charge pump

would need to be developed in an integrated circuit. The effects of the gate driver losses could then by analyzed and controlled, and additional parasitics only seen in the integrated circuit could be analyzed.

Several improvements in areas outside of circuit design and energy harvesting could also benefit this system. For example, improving the supercapacitor frequency response would allow the supercapacitor-powered system to last longer and likely support a higher average load current compared to that of Figure 3-7a. Innovation in IC packaging technology and flexboard technology could also greatly minimize weight contributions from these components.

Appendix A

Measured CBC050 Characteristics

The CBC050 test results mentioned and described in Section 3.3.1 are shown here. Each page shows 50 overlaid discharge profiles (top-left), the discharge time over each cycle (top-right), the work performed by the battery over each cycle (bottom-left), and the average output power by the battery over each cycle (bottom-right).

The discharge cutoff voltages mentioned in Section 3.3.1 are determined to be

$$V_{cutoff} = (3.0\,V - I_{diss} \cdot 500\,\Omega) \cdot 1.1 \tag{A.1}$$

where V_{cutoff} is the discharge cutoff voltage and I_{diss} is the discharge current on the battery. The CBC050 datasheet lists 3.0 V as the minimum discharge voltage. In order to create a limit for much higher discharge currents, the battery is assumed to have a 500-Ω source impedance, and it is assumed the internal battery voltage in a Thevenin model must not drop below 3.0 V. The cutoff is then conservatively raised 10%. This method is used simply to create an analytical expression for the cutoff thresholds in the cycle-tests.

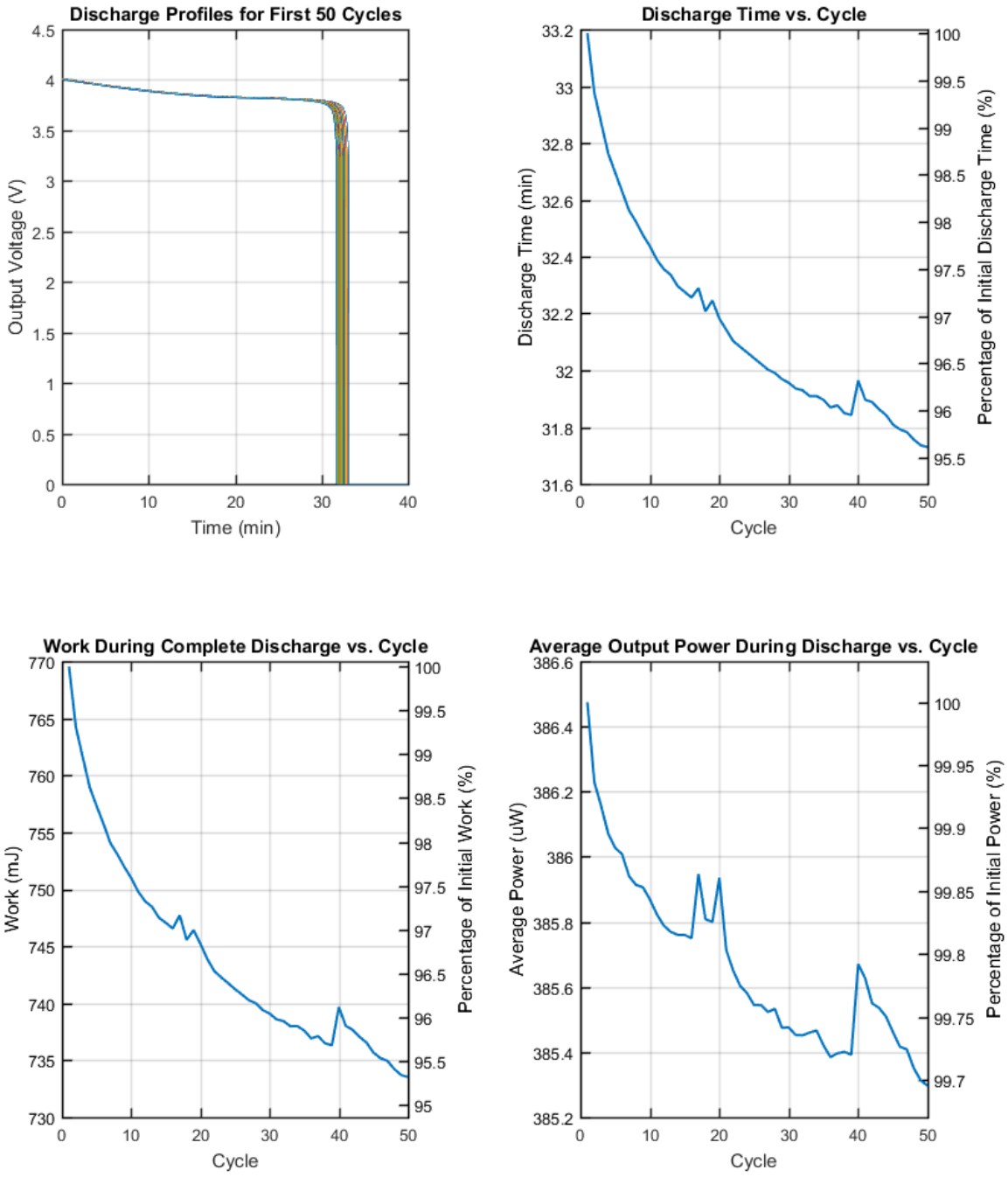


Figure A-1: Measured characteristics of CBC050 with 100-μA discharge current.

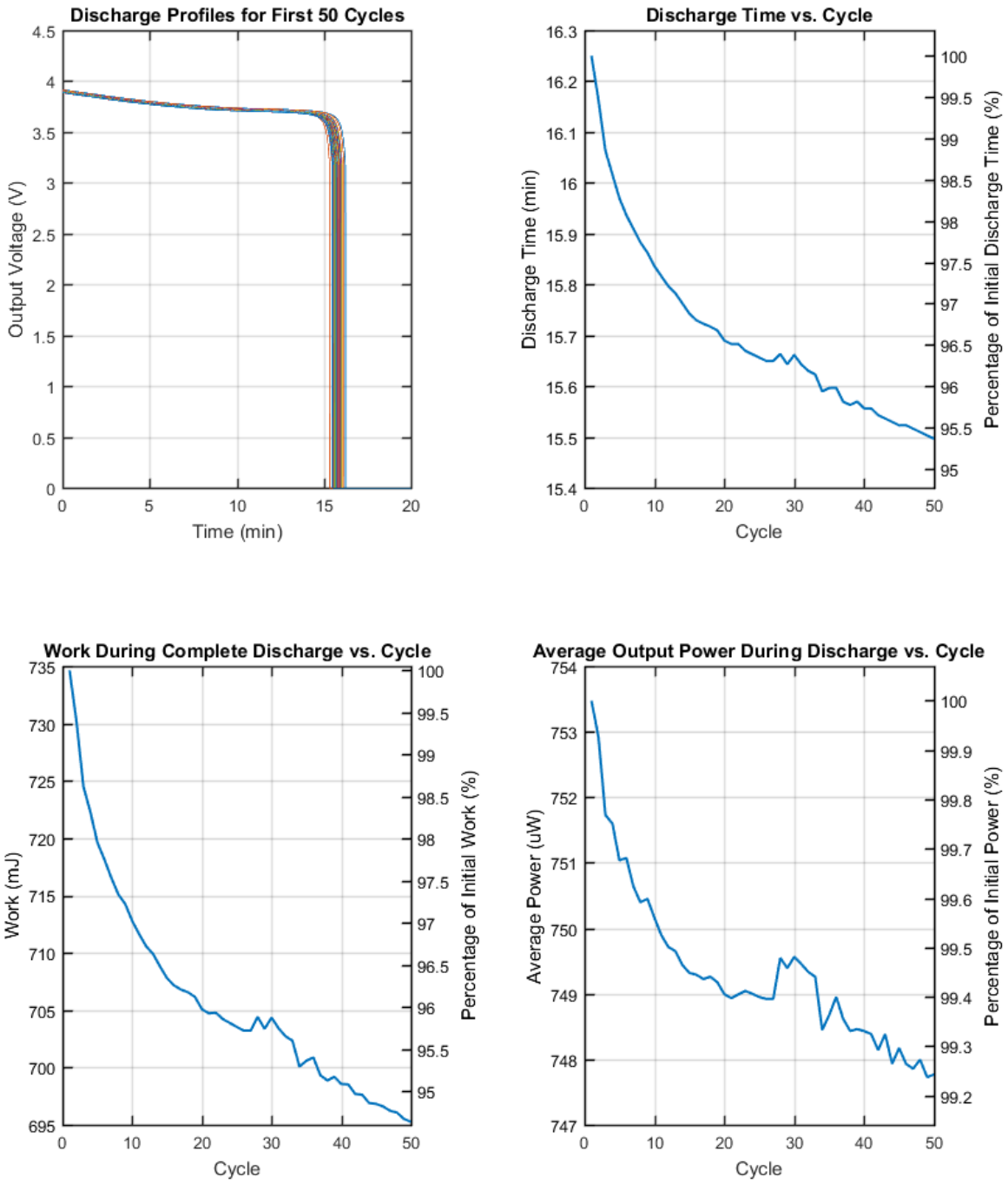


Figure A-2: Measured characteristics of CBC050 with 200-μA discharge current.

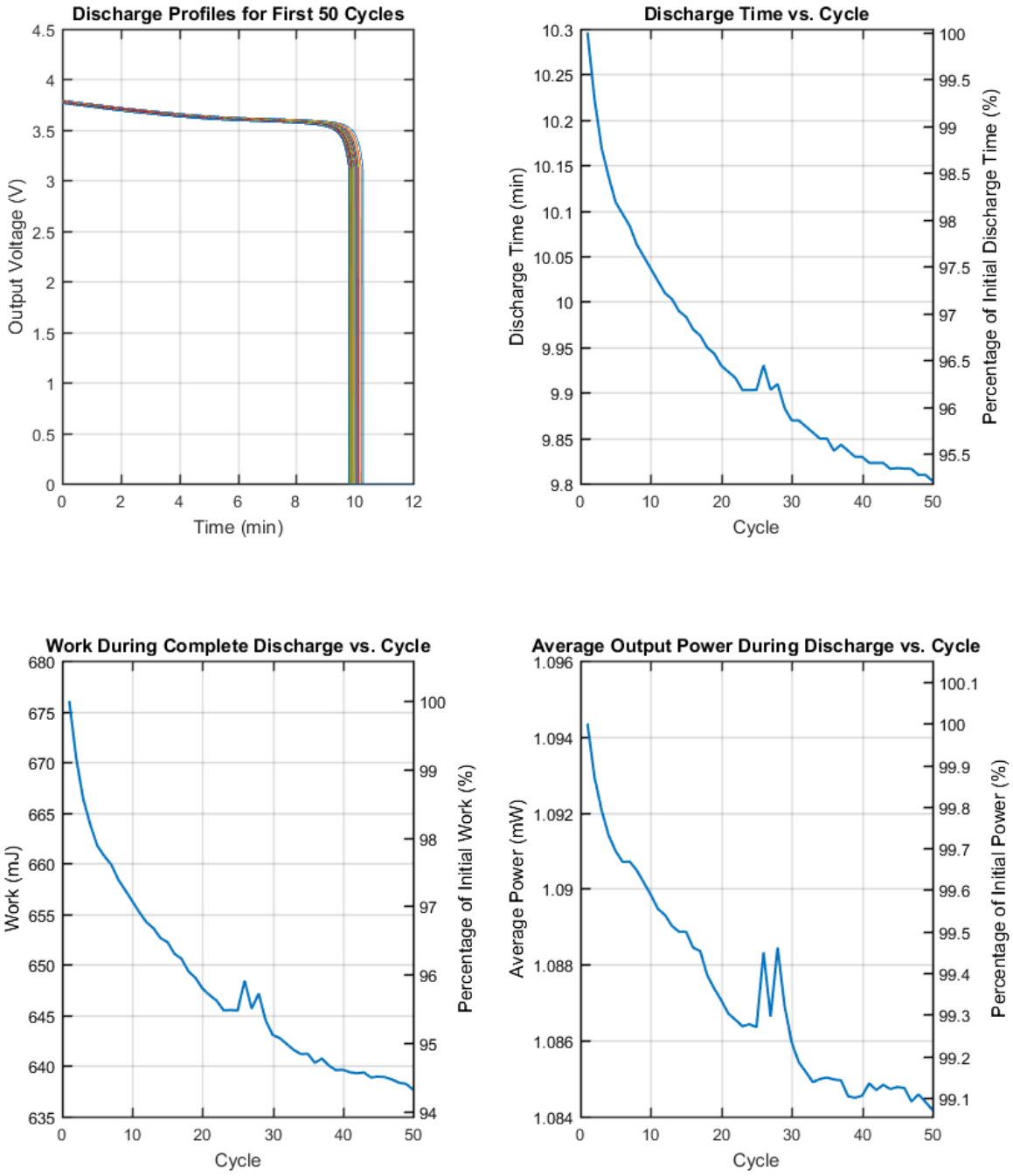


Figure A-3: Measured characteristics of CBC050 with 300-μA discharge current.

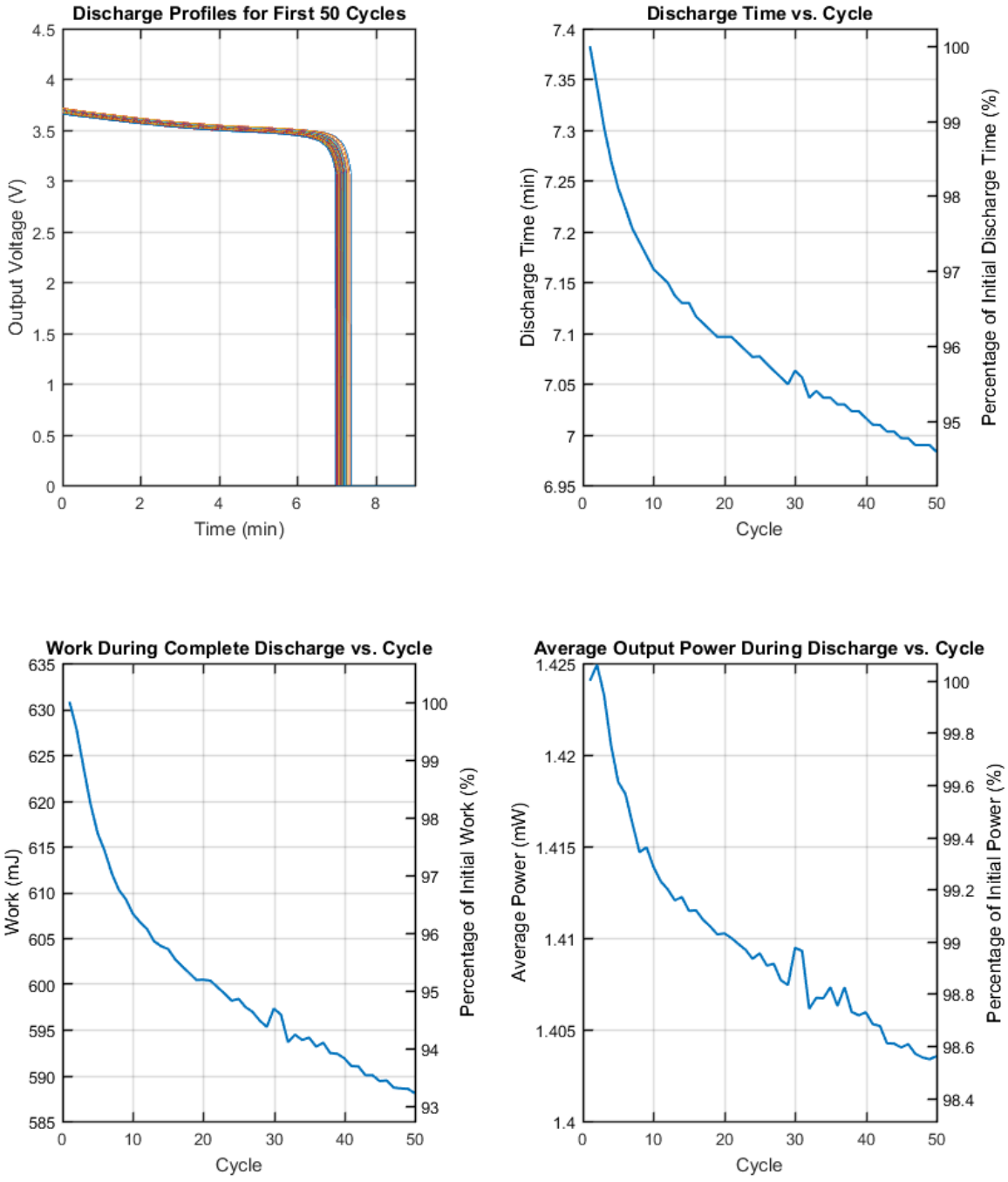


Figure A-4: Measured characteristics of CBC050 with 400-μA discharge current.

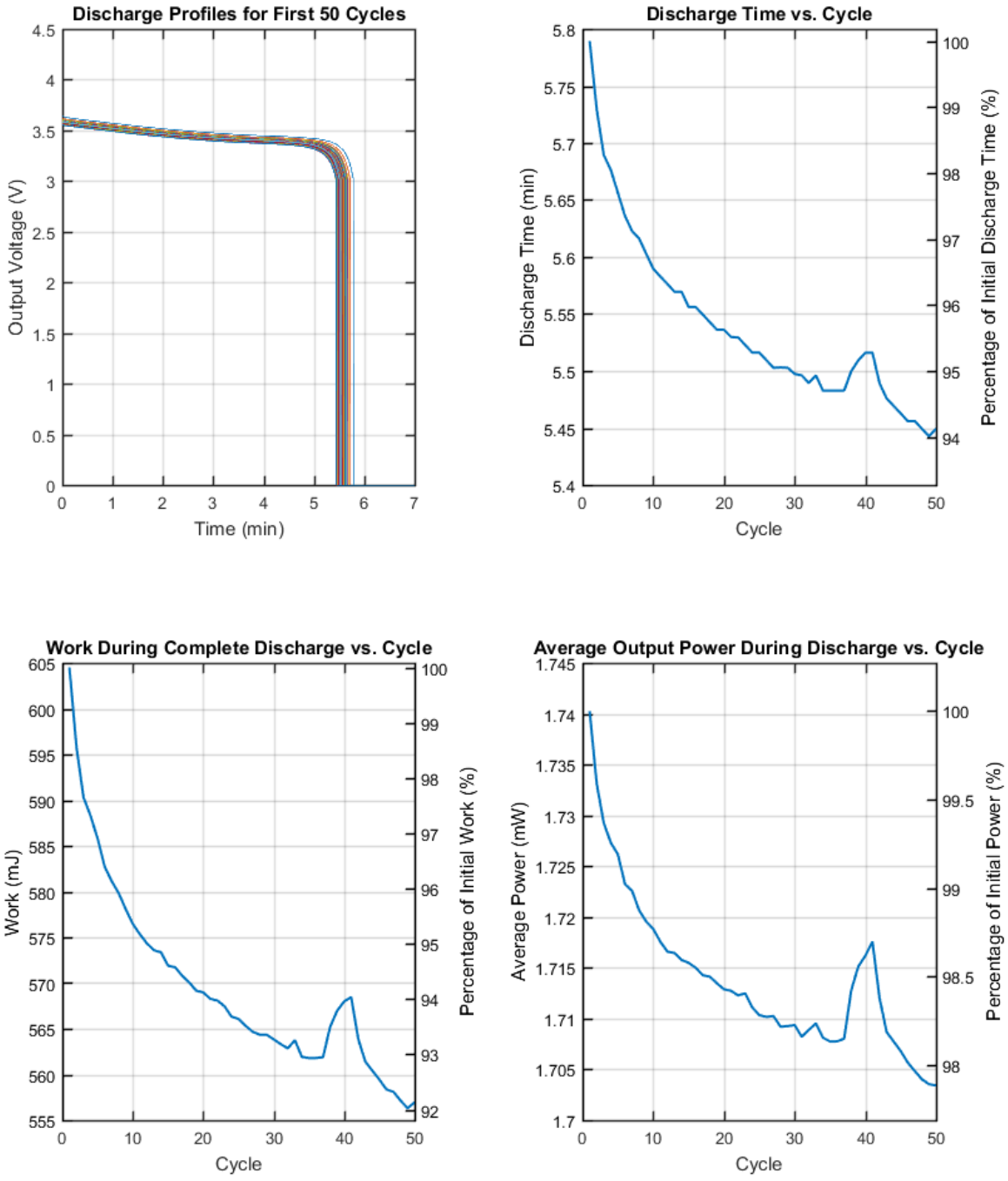


Figure A-5: Measured characteristics of CBC050 with 500-μA discharge current.

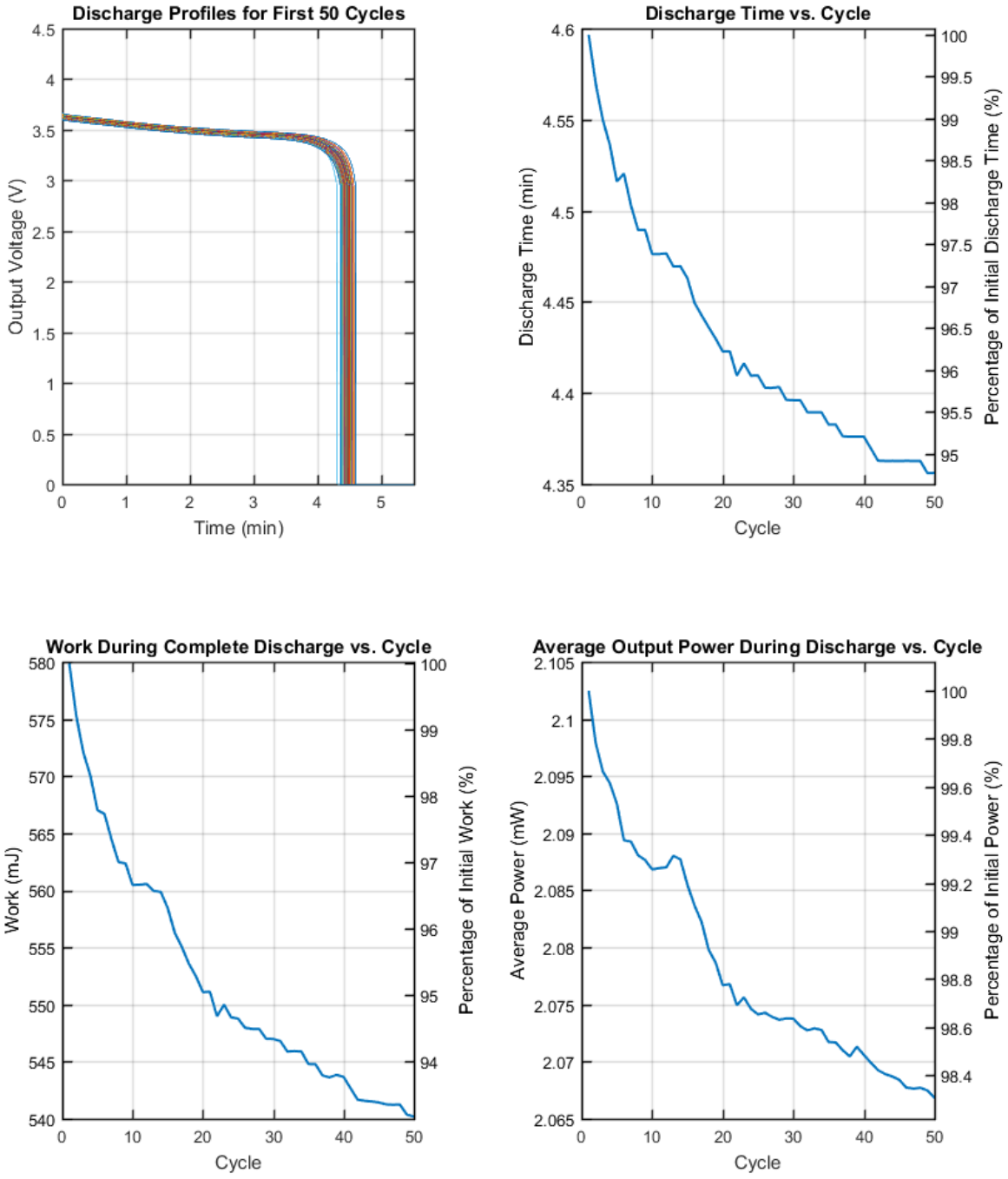


Figure A-6: Measured characteristics of CBC050 with 600-μA discharge current.

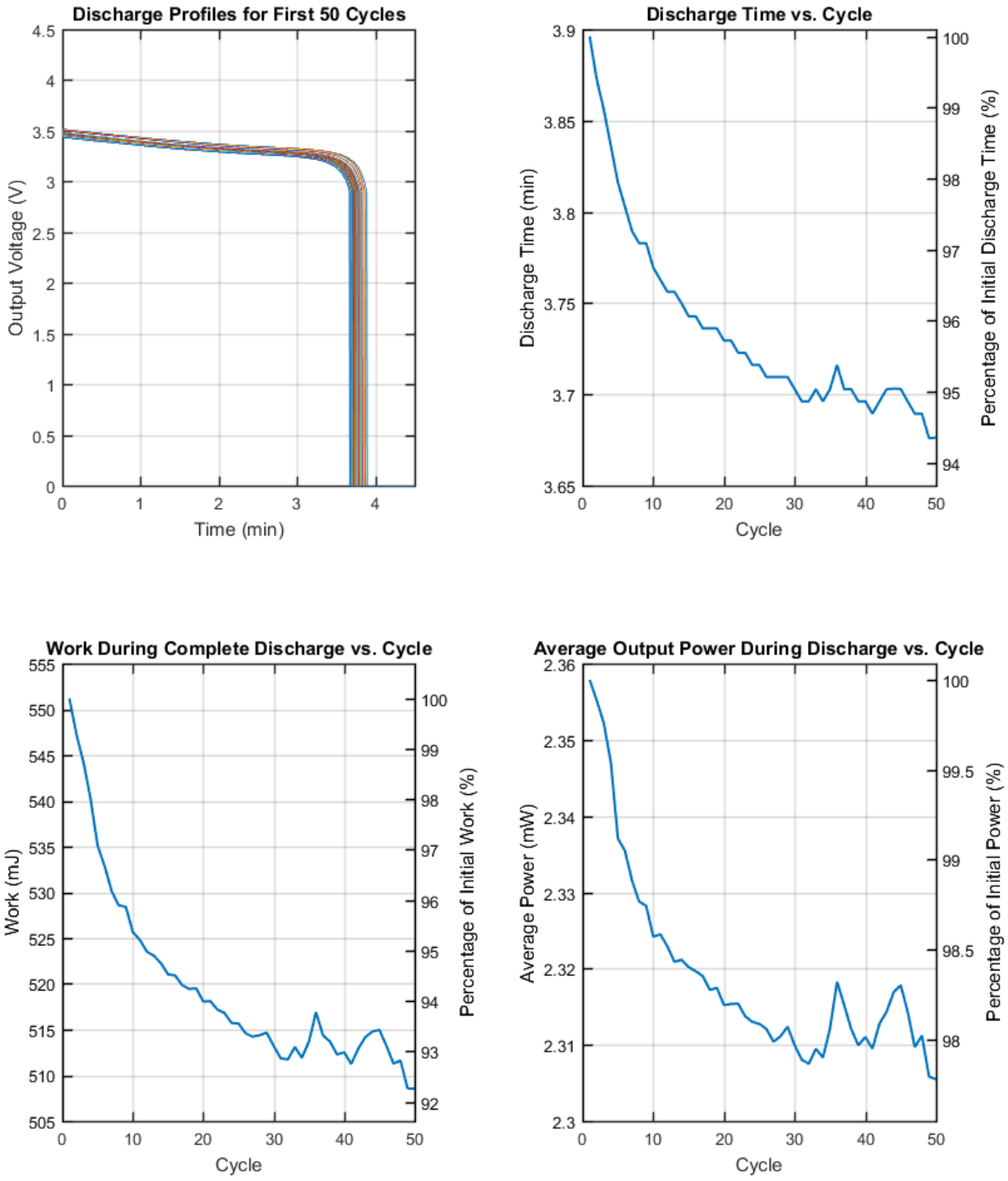


Figure A-7: Measured characteristics of CBC050 with 700-μA discharge current.

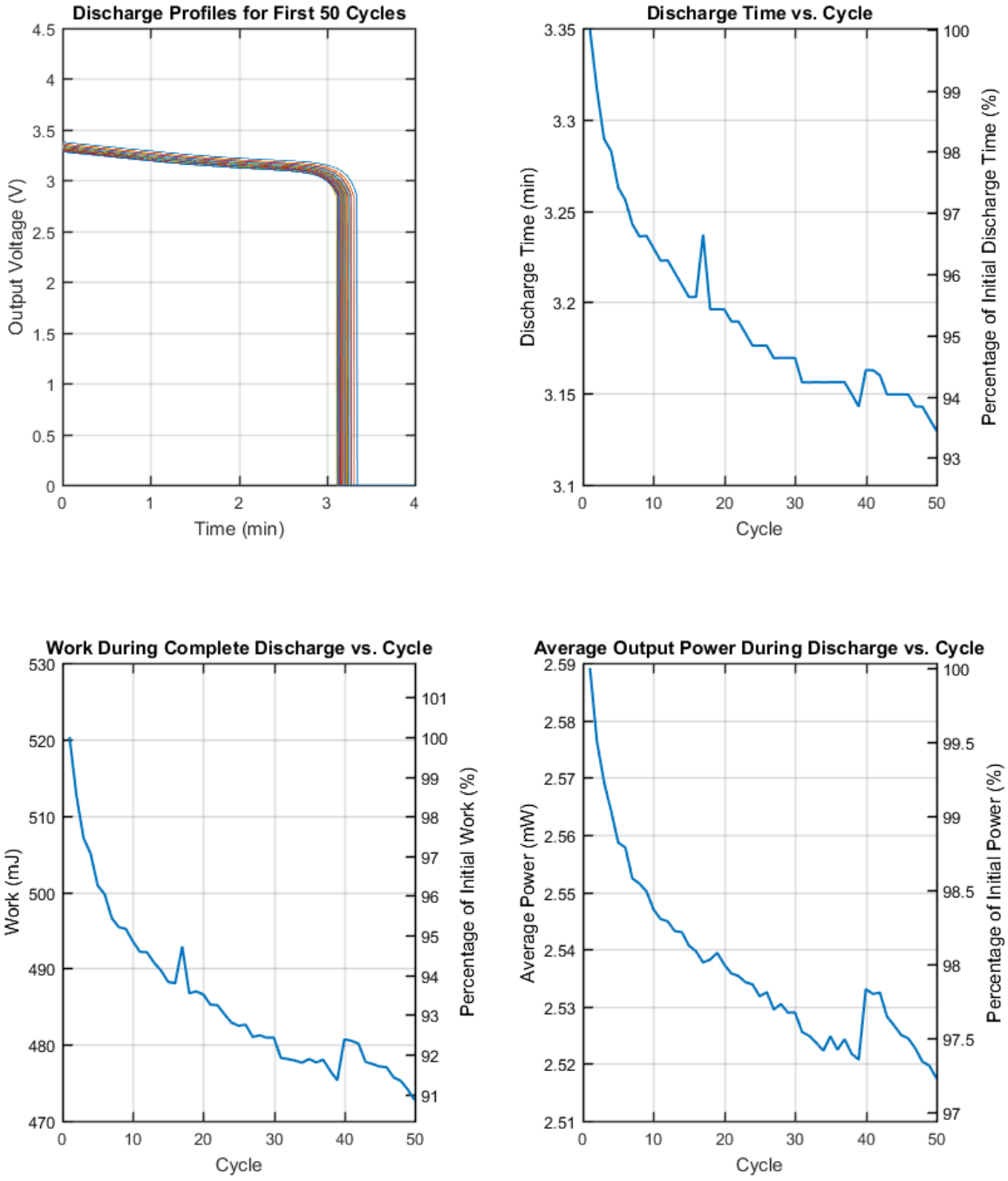


Figure A-8: Measured characteristics of CBC050 with 800-μA discharge current.

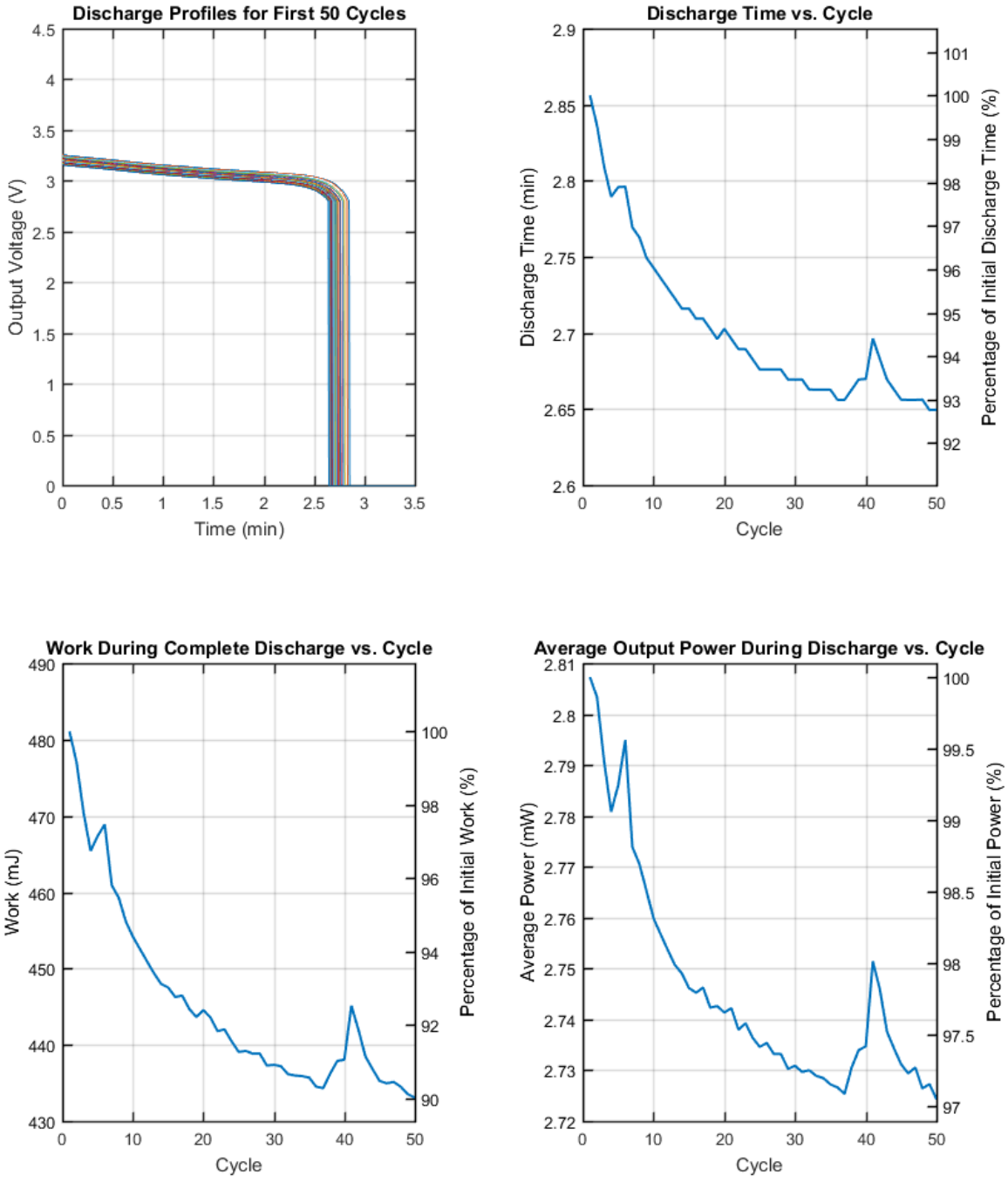


Figure A-9: Measured characteristics of CBC050 with 900-μA discharge current.

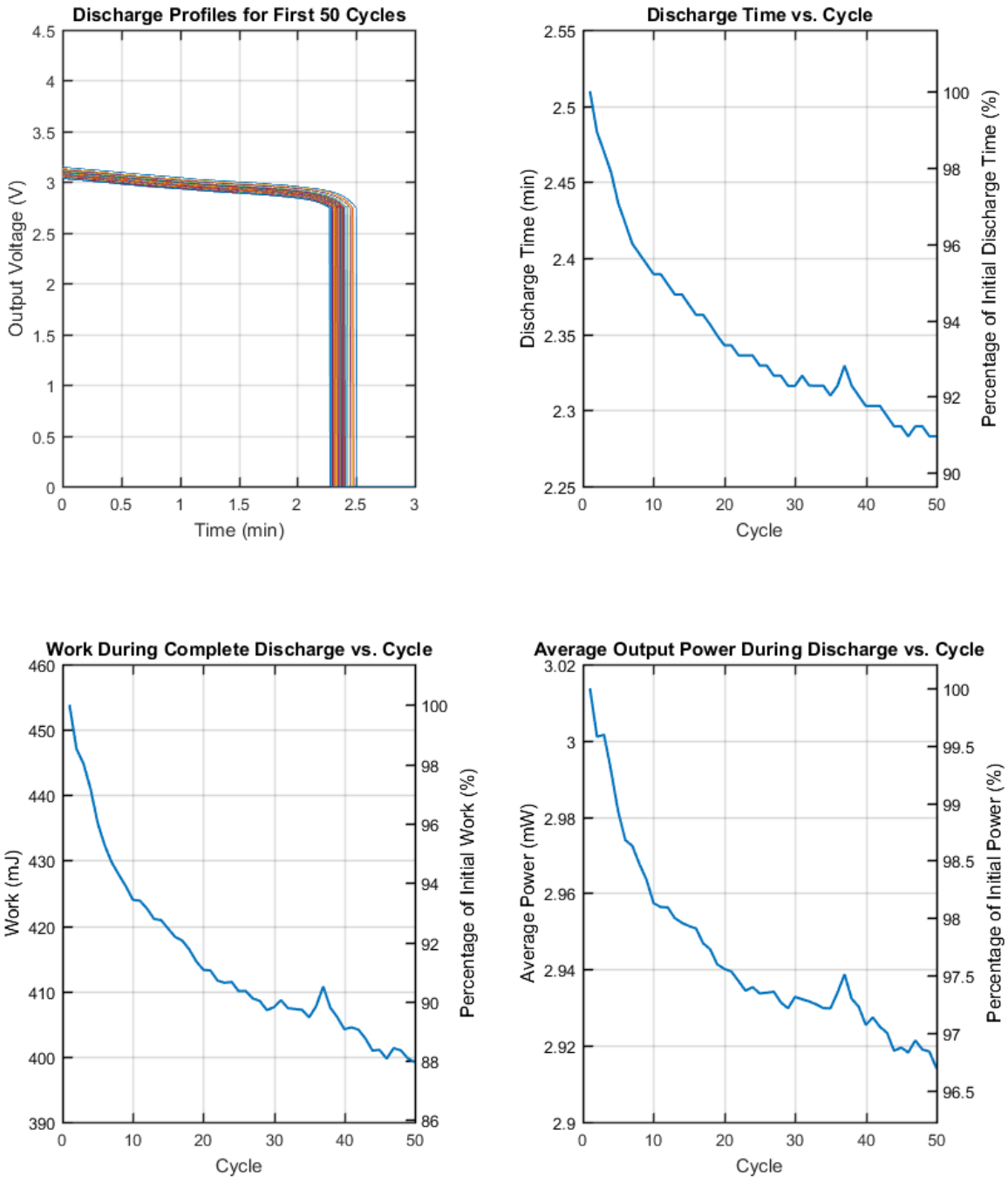


Figure A-10: Measured characteristics of CBC050 with 1000-μA discharge current.

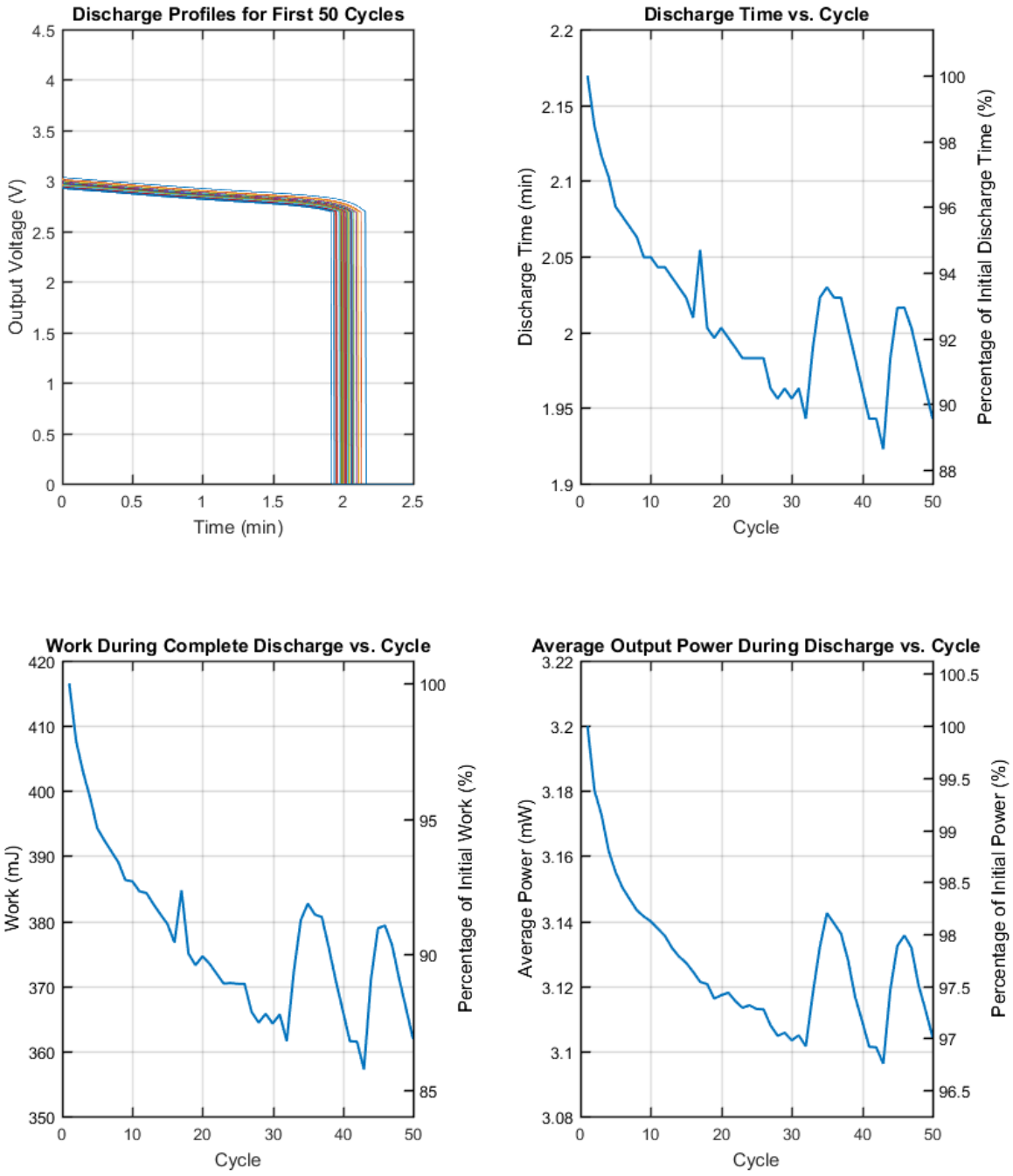


Figure A-11: Measured characteristics of CBC050 with 1100-μA discharge current.

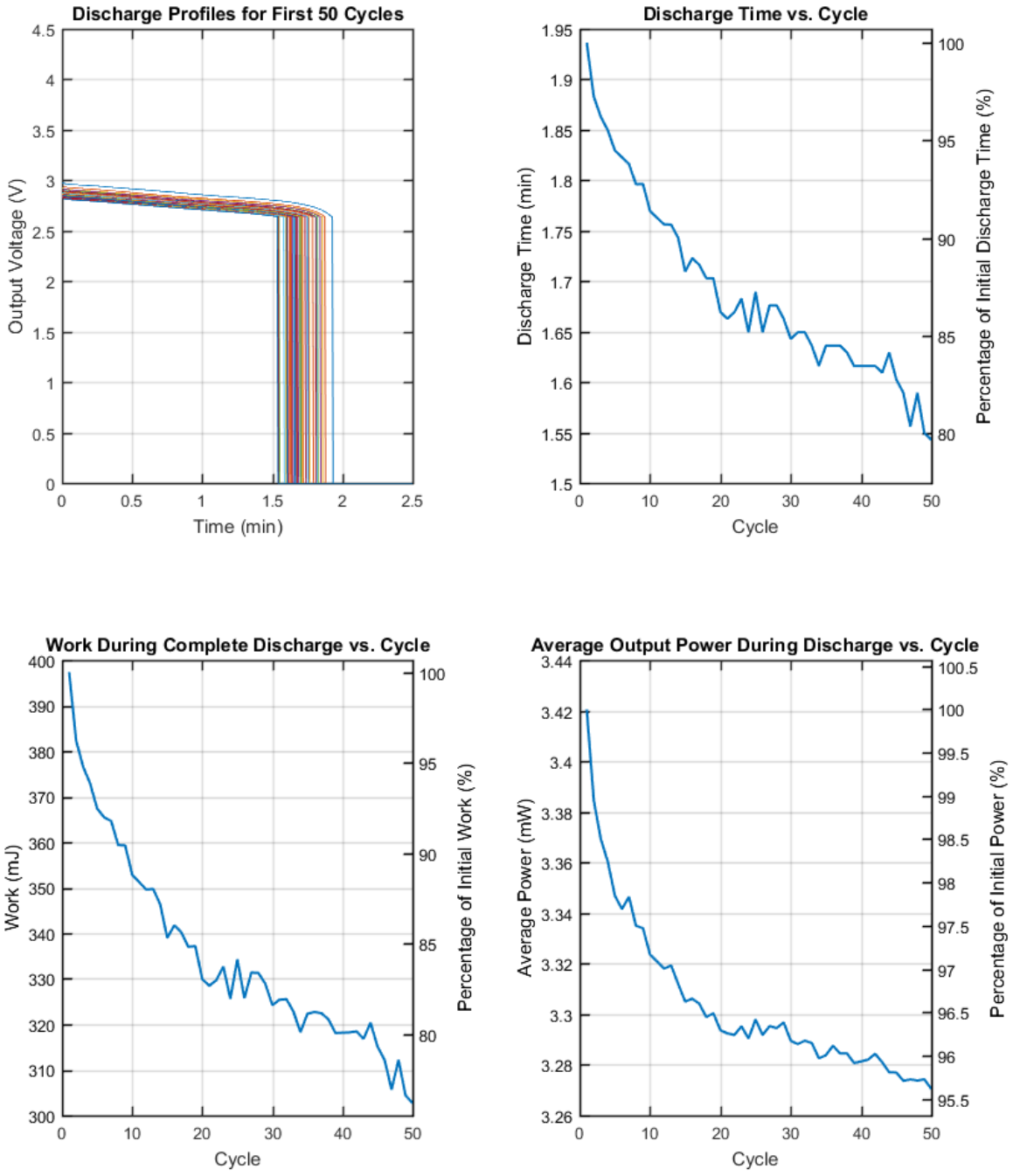


Figure A-12: Measured characteristics of CBC050 with 1200-μA discharge current.

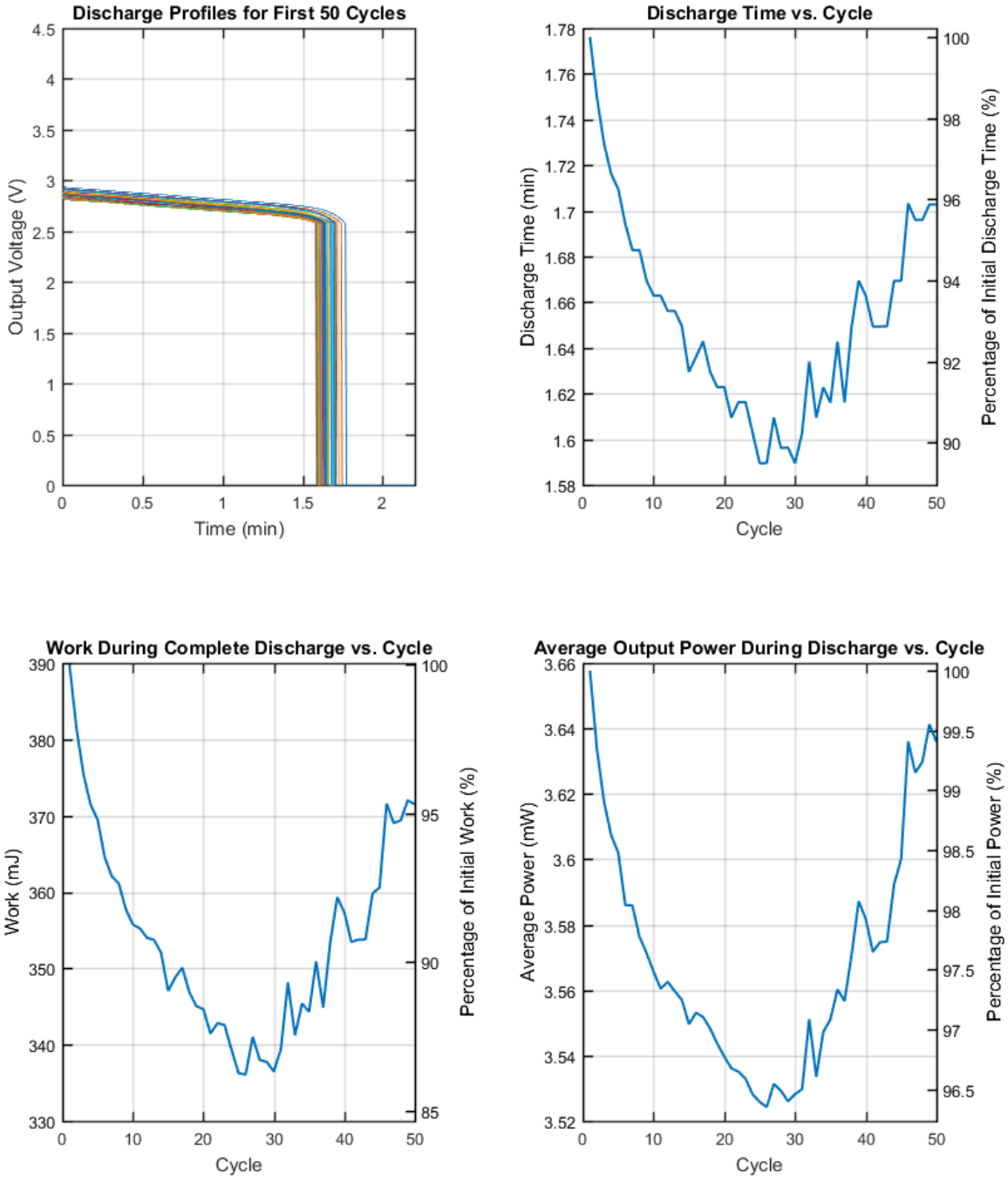


Figure A-13: Measured characteristics of CBC050 with 1300-μA discharge current.

Appendix B

Derivations of Fibonacci Charge Pump Characteristics

Chapter 4 extensively uses the ideal and parasitic theoretical behavior of the Fibonacci charge pump for 1 through 6 stages. This appendix derives these behaviors. Schematics are also included for each number of enabled stages, illustrating open and closed switches for each of the charge pump's two phases. All switching capacitors are assumed to have a capacitance C, and all parasitic capacitors are assumed to have a capacitance C_p.

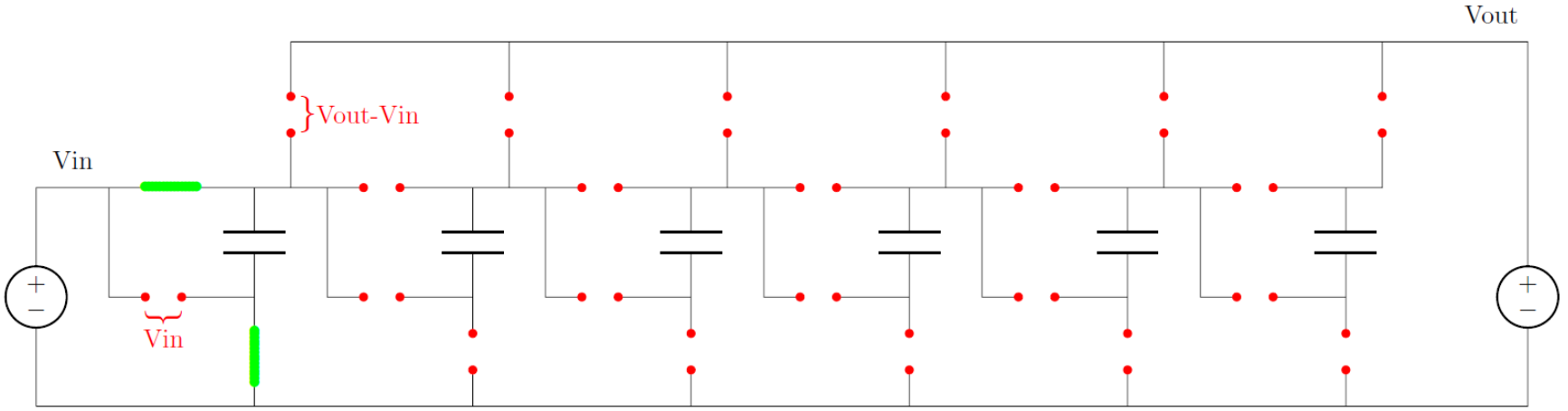
B.1 Ideal Characteristics

B.1.1 1 Stage

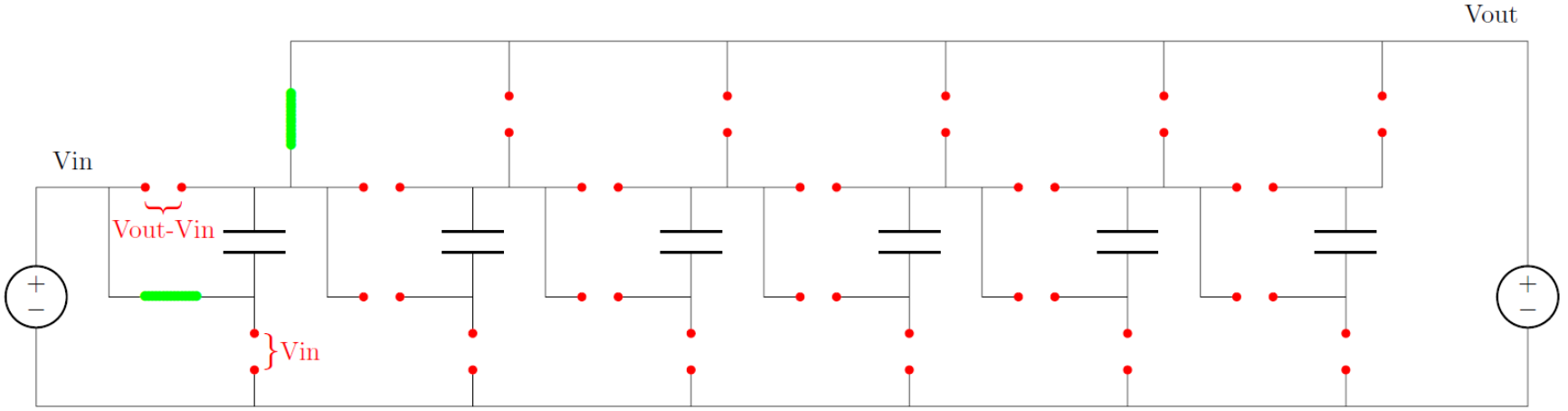
Figure B-1 shows the two phases of a 1-stage Fibonacci charge pump. The charge from the input source during 1 complete switching cycle is

$$\Delta q_{in} = -C(V_{out} - V_{in} - V_{in}) + C(V_{in} - V_{out} + V_{in}) = C(4V_{in} - 2V_{out}) \tag{B.1}$$

$$\Delta q_{in} = C\left(\frac{4}{1}V_{in} - \frac{2}{1}V_{out}\right) \tag{B.2}$$



(a) Phase one.



(b) Phase two.

Figure B-1: Both phases of Fibonacci charge pump when 1 stage is enabled.

The charge to the output source during 1 complete switching cycle is

$$\Delta q_{out} = -C(V_{out} - V_{in} - V_{in}) = C\left(\frac{2}{1}V_{in} - \frac{1}{1}V_{out}\right) \tag{B.3}$$

From Equations (B.2) and (B.3), the input-output charge and current relations are determined to be

$$2\Delta q_{out} = \Delta q_{in} \tag{B.4}$$

$$2I_{out} = I_{in} \tag{B.5}$$

Average output current is defined as

$$I_{out} = \Delta q_{out} \cdot f \tag{B.6}$$

and substituting in Equation (B.3) results in

$$I_{out} = C\left(\frac{2}{1}V_{in} - \frac{1}{1}V_{out}\right) f \tag{B.7}$$

which is the relationship between input voltage, output voltage, and output current. By substituting Equations (B.5) and (B.7) into the definition of input resistance, the input resistance is found to be

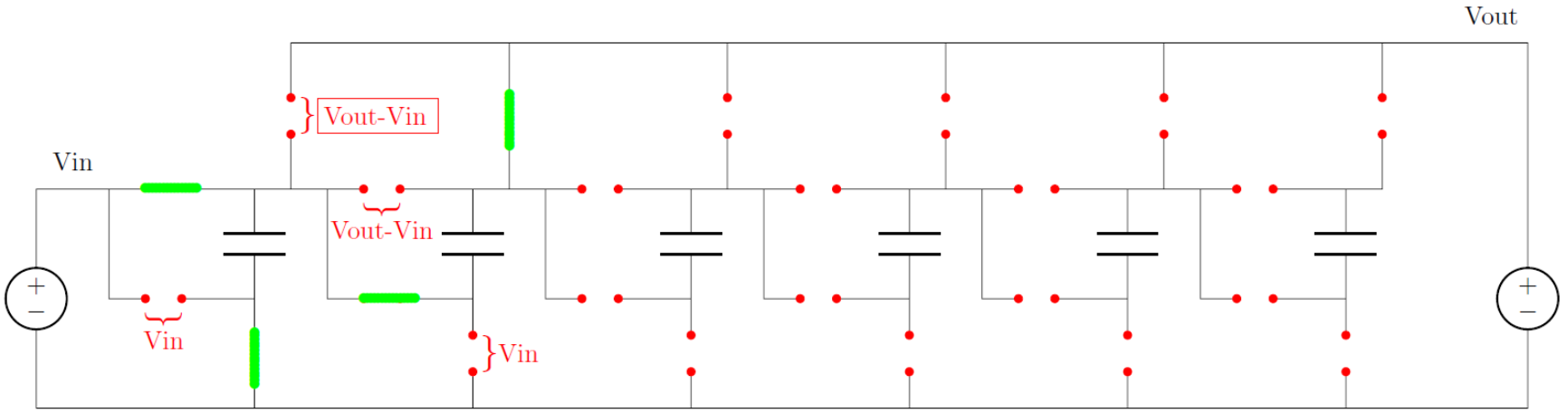
$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{2I_{out}} = \frac{V_{in}}{2Cf(\frac{2}{1}V_{in} - \frac{1}{1}V_{out})} = \frac{1}{4Cf} \cdot \frac{2V_{in}}{2V_{in} - V_{out}} \tag{B.8}$$

Using Equation (B.4) and the definition of efficiency shows the efficiency to be

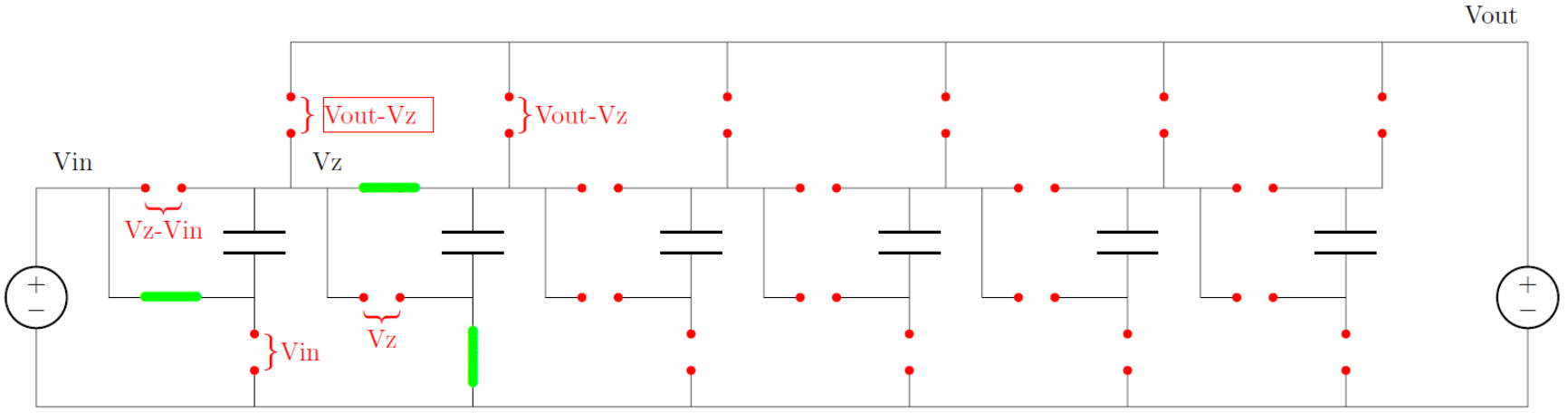
$$\eta = \frac{\Delta q_{out} V_{out}}{\Delta q_{in} V_{in}} = \frac{V_{out}}{2V_{in}} \tag{B.9}$$

B.1.2 2 Stages

Figure B-2 shows the two phases of a 2-stage Fibonacci charge pump. For 2 stages and higher, the first step for solving the characteristics is to solve for the intermediary



(a) Phase one.



(b) Phase two.

Figure B-2: Both phases of Fibonacci charge pump when 2 stages are enabled.

node voltages. This is done using KCL at each node where charge transfer ($\Delta Q = C\Delta V$) is examined instead of current. Performing this on node V_z results in

$$C(V_z - V_{in} - V_{in}) + C(V_z - V_{out} + V_{in}) = 0 \tag{B.10}$$

and rearranging shows that

$$V_z = \frac{1}{2}V_{in} + \frac{1}{2}V_{out} \tag{B.11}$$

The charge from the input source during 1 complete switching cycle is

$$\Delta q_{in} = -C(V_z - V_{in} - V_{in}) - C(V_{out} - V_{in} - V_z) + C(V_{in} - V_z + V_{in}) \tag{B.12}$$

$$\Delta q_{in} = C(5V_{in} - V_{out} - V_z) = C\left(\frac{9}{2}V_{in} - \frac{3}{2}V_{out}\right) \tag{B.13}$$

The charge to the output source during 1 complete switching cycle is

$$\Delta q_{out} = -C(V_{out} - V_{in} - V_z) = C\left(\frac{3}{2}V_{in} - \frac{1}{2}V_{out}\right) \tag{B.14}$$

From Equations (B.13) and (B.14), the input-output charge and current relations are determined to be

$$3\Delta q_{out} = \Delta q_{in} \tag{B.15}$$

$$3I_{out} = I_{in} \tag{B.16}$$

Substituting Equation (B.14) into Equation (B.6) results in

$$I_{out} = C\left(\frac{3}{2}V_{in} - \frac{1}{2}V_{out}\right) f \tag{B.17}$$

which is the relationship between input voltage, output voltage, and output current. By substituting Equations (B.16) and (B.17) into the definition of input resistance, the input resistance is found to be

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{3I_{out}} = \frac{V_{in}}{3Cf(\frac{3}{2}V_{in} - \frac{1}{2}V_{out})} = \frac{2}{9Cf} \cdot \frac{3V_{in}}{3V_{in} - V_{out}} \tag{B.18}$$

Using Equation (B.15) and the definition of efficiency shows the efficiency to be

$$\eta = \frac{\Delta q_{out} V_{out}}{\Delta q_{in} V_{in}} = \frac{V_{out}}{3V_{in}} \tag{B.19}$$

B.1.3 3 Stages

Figure B-3 shows the two phases of a 3-stage Fibonacci charge pump. Solving for the intermediary node voltages using KCL results in

$$V_x : C(V_x - V_{in} - V_z) + C(V_x - V_{out} + V_z) = 0 \tag{B.20}$$

$$V_z : C(V_z - V_{in} - V_{in}) + C(V_z - V_x + V_{in}) - C(V_{out} - V_z - V_x) = 0 \tag{B.21}$$

These can be represented in matrix form as

$$\begin{bmatrix} 2 & 0 \\ 0 & 3 \end{bmatrix} \begin{bmatrix} V_x \\ V_z \end{bmatrix} = \begin{bmatrix} V_{in} + V_{out} \\ V_{in} + V_{out} \end{bmatrix} \tag{B.22}$$

$$\begin{bmatrix} V_x \\ V_z \end{bmatrix} = \begin{bmatrix} \frac{1}{2}V_{in} + \frac{1}{2}V_{out} \\ \frac{1}{3}V_{in} + \frac{1}{3}V_{out} \end{bmatrix} \tag{B.23}$$

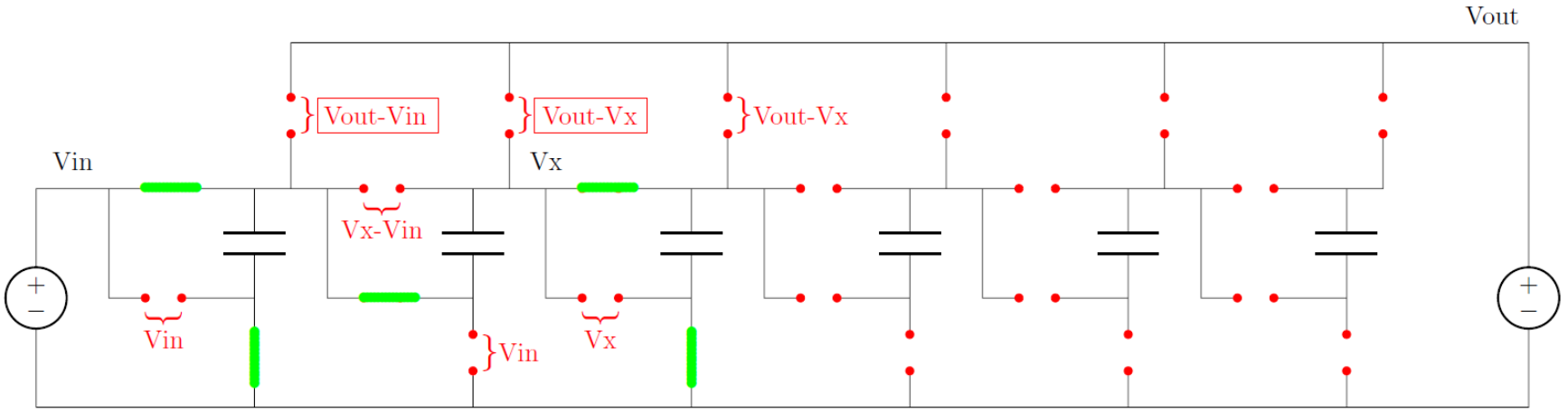
The charge from the input source during 1 complete switching cycle is

$$\Delta q_{in} = -C(V_z - V_{in} - V_{in}) - C(V_x - V_{in} - V_z) + C(V_{in} - V_z + V_{in}) \tag{B.24}$$

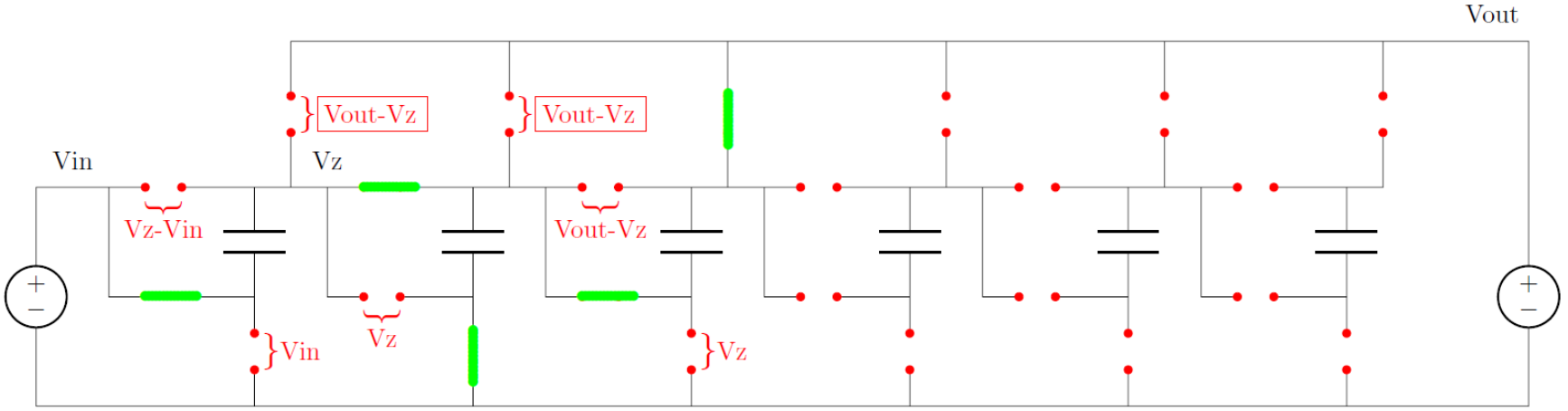
$$\Delta q_{in} = C(5V_{in} - V_x - V_z) = C\left(\frac{25}{6}V_{in} - \frac{5}{6}V_{out}\right) \tag{B.25}$$

The charge to the output source during 1 complete switching cycle is

$$\Delta q_{out} = -C(V_{out} - V_z - V_x) = C\left(\frac{5}{6}V_{in} - \frac{1}{6}V_{out}\right) \tag{B.26}$$



(a) Phase one.



(b) Phase two.

Figure B-3: Both phases of Fibonacci charge pump when 3 stages are enabled.

From Equations (B.25) and (B.26), the input-output charge and current relations are determined to be

$$5\Delta q_{out} = \Delta q_{in} \tag{B.27}$$

$$5I_{out} = I_{in} \tag{B.28}$$

Substituting Equation (B.26) into Equation (B.6) results in

$$I_{out} = C\left(\frac{5}{6}V_{in} - \frac{1}{6}V_{out}\right)f \tag{B.29}$$

which is the relationship between input voltage, output voltage, and output current. By substituting Equations (B.28) and (B.29) into the definition of input resistance, the input resistance is found to be

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{5I_{out}} = \frac{V_{in}}{5Cf(\frac{5}{6}V_{in} - \frac{1}{6}V_{out})} = \frac{6}{25Cf} \cdot \frac{5V_{in}}{5V_{in} - V_{out}} \tag{B.30}$$

Using Equation (B.27) and the definition of efficiency shows the efficiency to be

$$\eta = \frac{\Delta q_{out}V_{out}}{\Delta q_{in}V_{in}} = \frac{V_{out}}{5V_{in}} \tag{B.31}$$

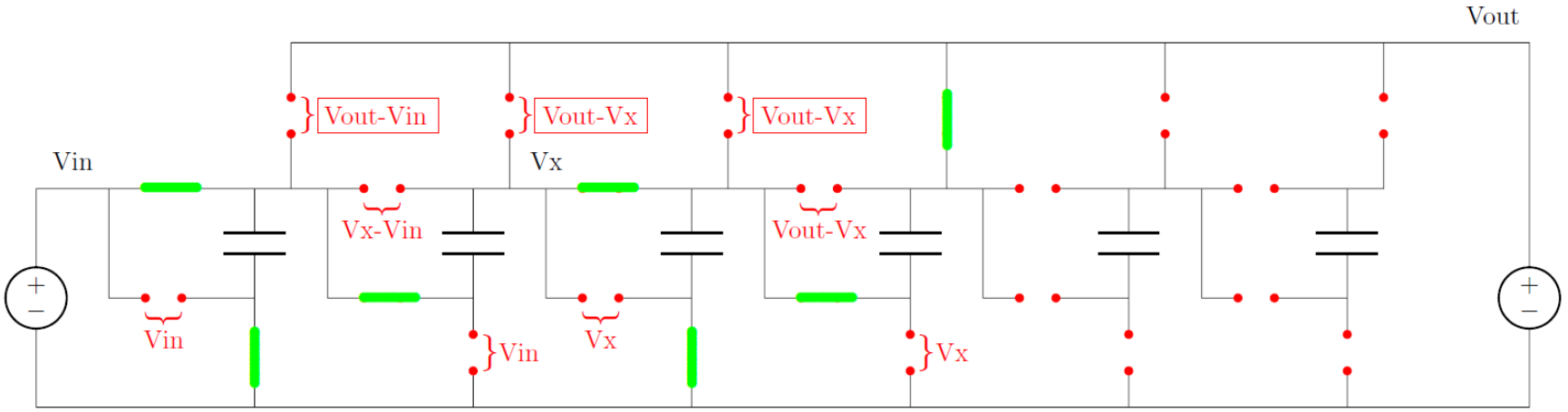
B.1.4 4 Stages

Figure B-4 shows the two phases of a 4-stage Fibonacci charge pump. Solving for the intermediary node voltages using KCL results in

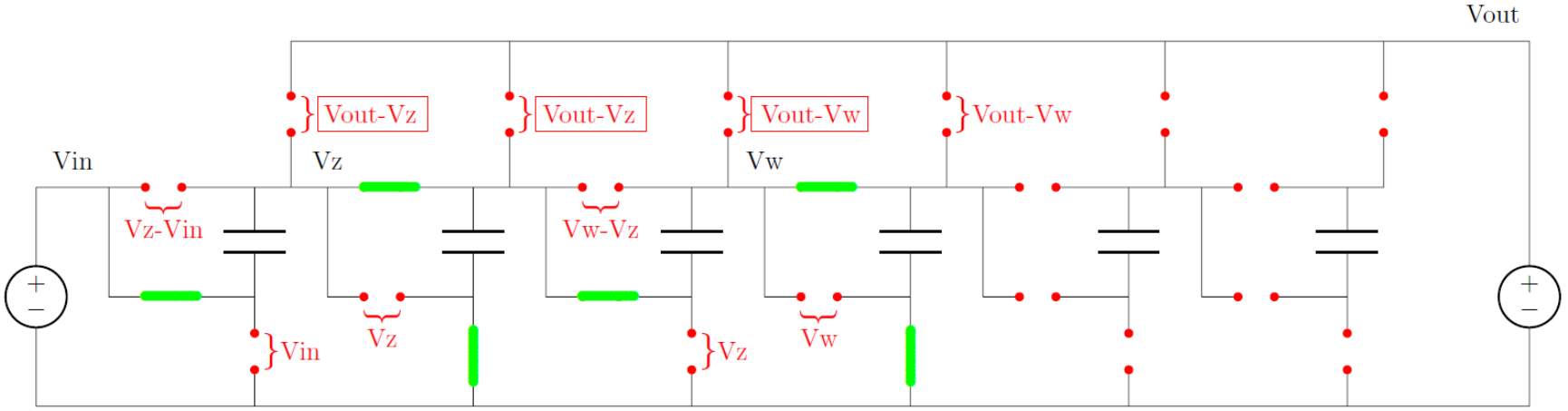
$$V_x : C(V_x - V_{in} - V_z) + C(V_x - V_w + V_z) - C(V_{out} - V_x - V_w) = 0 \tag{B.32}$$

$$V_z : C(V_z - V_{in} - V_{in}) + C(V_z - V_x + V_{in}) - C(V_w - V_z - V_x) = 0 \tag{B.33}$$

$$V_w : C(V_w - V_z - V_x) + C(V_w - V_{out} + V_x) = 0 \tag{B.34}$$



(a) Phase one.



(b) Phase two.

Figure B-4: Both phases of Fibonacci charge pump when 4 stages are enabled.

These can be represented in matrix form as

$$\begin{bmatrix} 3 & 0 & 0 \\ 0 & 3 & -1 \\ 0 & -1 & 2 \end{bmatrix} \begin{bmatrix} V_x \\ V_z \\ V_w \end{bmatrix} = \begin{bmatrix} V_{in} + V_{out} \\ V_{in} \\ V_{out} \end{bmatrix} \tag{B.35}$$

$$\begin{bmatrix} V_x \\ V_z \\ V_w \end{bmatrix} = \begin{bmatrix} \frac{1}{3}V_{in} + \frac{1}{3}V_{out} \\ \frac{2}{5}V_{in} + \frac{1}{5}V_{out} \\ \frac{1}{5}V_{in} + \frac{3}{5}V_{out} \end{bmatrix} \tag{B.36}$$

The charge from the input source during 1 complete switching cycle is

$$\Delta q_{in} = -C(V_z - V_{in} - V_{in}) - C(V_x - V_{in} - V_z) + C(V_{in} - V_z + V_{in}) \tag{B.37}$$

$$\Delta q_{in} = C(5V_{in} - V_x - V_z) = C\left(\frac{64}{15}V_{in} - \frac{8}{15}V_{out}\right) \tag{B.38}$$

The charge to the output source during 1 complete switching cycle is

$$\Delta q_{out} = -C(V_{out} - V_x - V_w) = C\left(\frac{8}{15}V_{in} - \frac{1}{15}V_{out}\right) \tag{B.39}$$

From Equations (B.38) and (B.39), the input-output charge and current relations are determined to be

$$8\Delta q_{out} = \Delta q_{in} \tag{B.40}$$

$$8I_{out} = I_{in} \tag{B.41}$$

Substituting Equation (B.39) into Equation (B.6) results in

$$I_{out} = C\left(\frac{8}{15}V_{in} - \frac{1}{15}V_{out}\right) f \tag{B.42}$$

which is the relationship between input voltage, output voltage, and output current. By substituting Equations (B.41) and (B.42) into the definition of input resistance,

the input resistance is found to be

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{8I_{out}} = \frac{V_{in}}{8Cf(\frac{8}{15}V_{in} - \frac{1}{15}V_{out})} = \frac{15}{64Cf} \cdot \frac{8V_{in}}{8V_{in} - V_{out}} \tag{B.43}$$

Using Equation (B.40) and the definition of efficiency shows the efficiency to be

$$\eta = \frac{\Delta q_{out} V_{out}}{\Delta q_{in} V_{in}} = \frac{V_{out}}{8V_{in}} \tag{B.44}$$

B.1.5 5 Stages

Figure B-5 shows the two phases of a 5-stage Fibonacci charge pump. Solving for the intermediary node voltages using KCL results in

$$V_x : C(V_x - V_{in} - V_z) + C(V_x - V_w + V_z) - C(V_y - V_x - V_w) = 0 \tag{B.45}$$

$$V_y : C(V_y - V_x - V_w) + C(V_y - V_{out} + V_w) = 0 \tag{B.46}$$

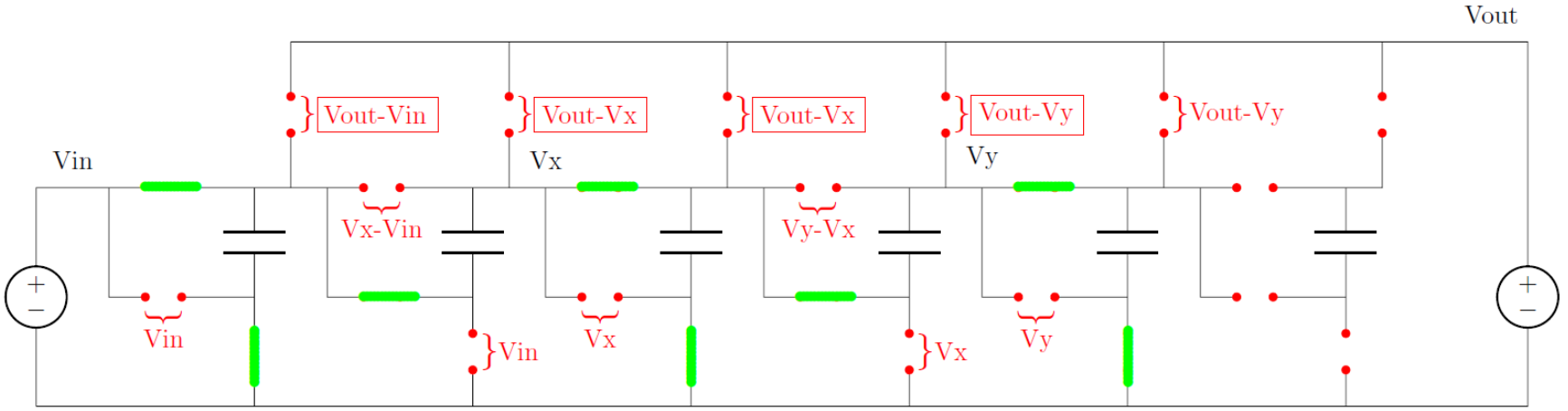
$$V_z : C(V_z - V_{in} - V_{in}) + C(V_z - V_x + V_{in}) - C(V_w - V_z - V_x) = 0 \tag{B.47}$$

$$V_w : C(V_w - V_z - V_x) + C(V_w - V_y + V_x) - C(V_{out} - V_w - V_y) = 0 \tag{B.48}$$

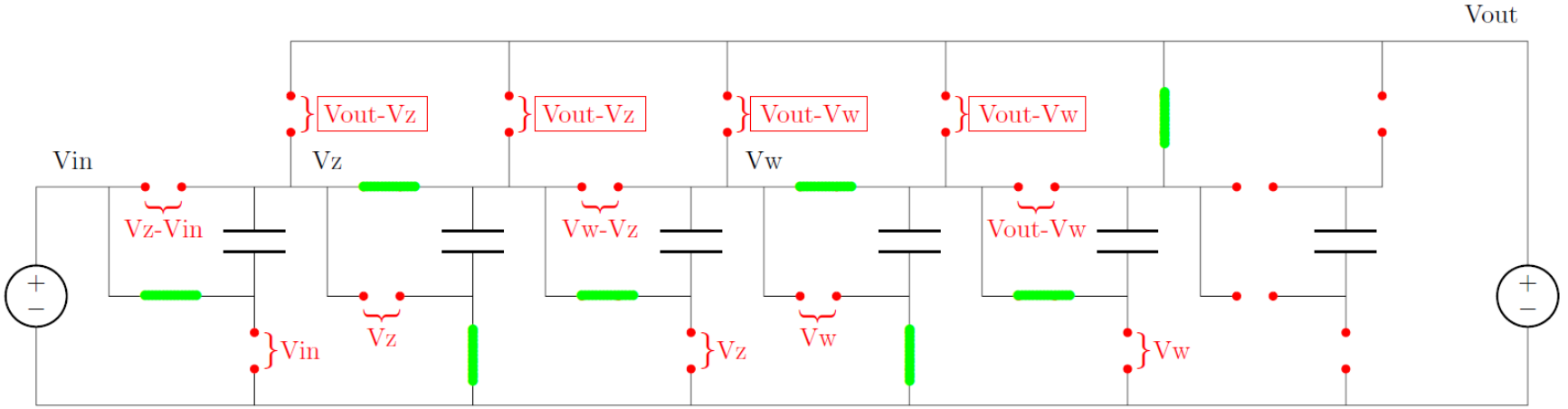
These can be represented in matrix form as

$$\begin{bmatrix} 3 & -1 & 0 & 0 \\ -1 & 2 & 0 & 0 \\ 0 & 0 & 3 & -1 \\ 0 & 0 & -1 & 3 \end{bmatrix} \begin{bmatrix} V_x \\ V_y \\ V_z \\ V_w \end{bmatrix} = \begin{bmatrix} V_{in} \\ V_{out} \\ V_{in} \\ V_{out} \end{bmatrix} \tag{B.49}$$

$$\begin{bmatrix} V_x \\ V_y \\ V_z \\ V_w \end{bmatrix} = \begin{bmatrix} \frac{2}{5}V_{in} + \frac{1}{5}V_{out} \\ \frac{1}{5}V_{in} + \frac{3}{5}V_{out} \\ \frac{3}{8}V_{in} + \frac{1}{8}V_{out} \\ \frac{1}{8}V_{in} + \frac{3}{8}V_{out} \end{bmatrix} \tag{B.50}$$



(a) Phase one.



(b) Phase two.

Figure B-5: Both phases of Fibonacci charge pump when 5 stages are enabled.

The charge from the input source during 1 complete switching cycle is

$$\Delta q_{in} = -C(V_z - V_{in} - V_{in}) - C(V_x - V_{in} - V_z) + C(V_{in} - V_z + V_{in}) \tag{B.51}$$

$$\Delta q_{in} = C(5V_{in} - V_x - V_z) = C\left(\frac{169}{40}V_{in} - \frac{13}{40}V_{out}\right) \tag{B.52}$$

The charge to the output source during 1 complete switching cycle is

$$\Delta q_{out} = -C(V_{out} - V_w - V_y) = C\left(\frac{13}{40}V_{in} - \frac{1}{40}V_{out}\right) \tag{B.53}$$

From Equations (B.52) and (B.53), the input-output charge and current relations are determined to be

$$13\Delta q_{out} = \Delta q_{in} \tag{B.54}$$

$$13I_{out} = I_{in} \tag{B.55}$$

Substituting Equation (B.53) into Equation (B.6) results in

$$I_{out} = C\left(\frac{13}{40}V_{in} - \frac{1}{40}V_{out}\right) f \tag{B.56}$$

which is the relationship between input voltage, output voltage, and output current. By substituting Equations (B.55) and (B.56) into the definition of input resistance, the input resistance is found to be

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{13I_{out}} = \frac{V_{in}}{13Cf(\frac{13}{40}V_{in} - \frac{1}{40}V_{out})} = \frac{40}{169Cf} \cdot \frac{13V_{in}}{13V_{in} - V_{out}} \tag{B.57}$$

Using Equation (B.54) and the definition of efficiency shows the efficiency to be

$$\eta = \frac{\Delta q_{out} V_{out}}{\Delta q_{in} V_{in}} = \frac{V_{out}}{13V_{in}} \tag{B.58}$$

B.1.6 6 Stages

Figure B-6 shows the two phases of a 6-stage Fibonacci charge pump. Solving for the intermediary node voltages using KCL results in

$$V_x : C(V_x - V_{in} - V_z) + C(V_x - V_w + V_z) - C(V_y - V_x - V_w) = 0 \tag{B.59}$$

$$V_y : C(V_y - V_x - V_w) + C(V_y - V_p + V_w) - C(V_{out} - V_y - V_p) = 0 \tag{B.60}$$

$$V_z : C(V_z - V_{in} - V_{in}) + C(V_z - V_x + V_{in}) - C(V_w - V_z - V_x) = 0 \tag{B.61}$$

$$V_w : C(V_w - V_z - V_x) + C(V_w - V_y + V_x) - C(V_p - V_w - V_y) = 0 \tag{B.62}$$

$$V_p : C(V_p - V_w - V_y) + C(V_p - V_{out} + V_y) = 0 \tag{B.63}$$

These can be represented in matrix form as

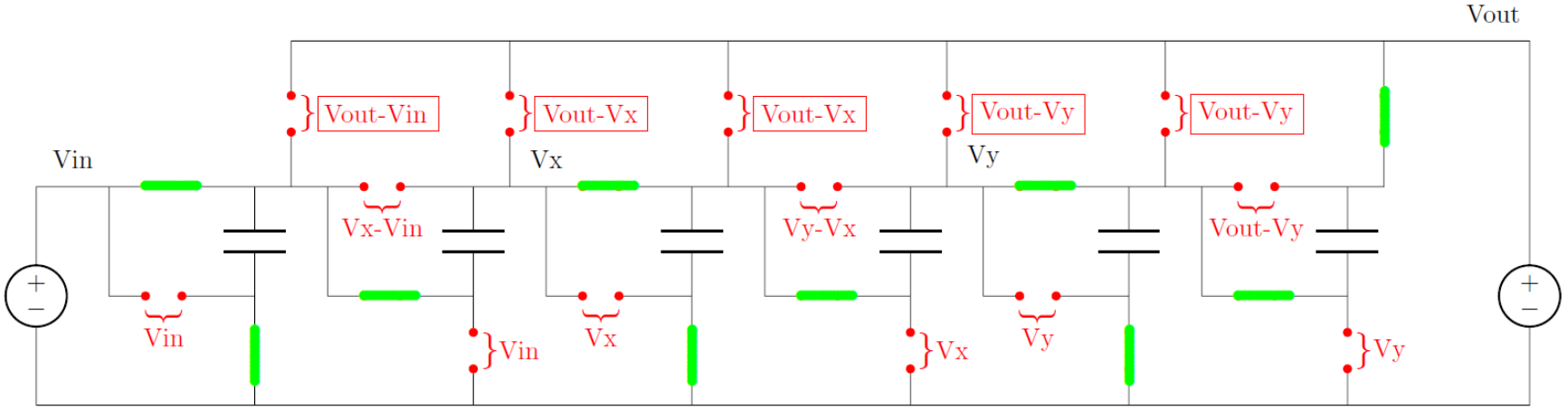
$$\begin{bmatrix} 3 & -1 & 0 & 0 & 0 \\ -1 & 3 & 0 & 0 & 0 \\ 0 & 0 & 3 & -1 & 0 \\ 0 & 0 & -1 & 3 & -1 \\ 0 & 0 & 0 & -1 & 2 \end{bmatrix} \begin{bmatrix} V_x \\ V_y \\ V_z \\ V_w \\ V_p \end{bmatrix} = \begin{bmatrix} V_{in} \\ V_{out} \\ V_{in} \\ 0 \\ V_{out} \end{bmatrix} \tag{B.64}$$

$$\begin{bmatrix} V_x \\ V_y \\ V_z \\ V_w \\ V_p \end{bmatrix} = \begin{bmatrix} \frac{3}{8}V_{in} + \frac{1}{8}V_{out} \\ \frac{1}{8}V_{in} + \frac{3}{8}V_{out} \\ \frac{5}{13}V_{in} + \frac{1}{13}V_{out} \\ \frac{2}{13}V_{in} + \frac{3}{13}V_{out} \\ \frac{1}{13}V_{in} + \frac{8}{13}V_{out} \end{bmatrix} \tag{B.65}$$

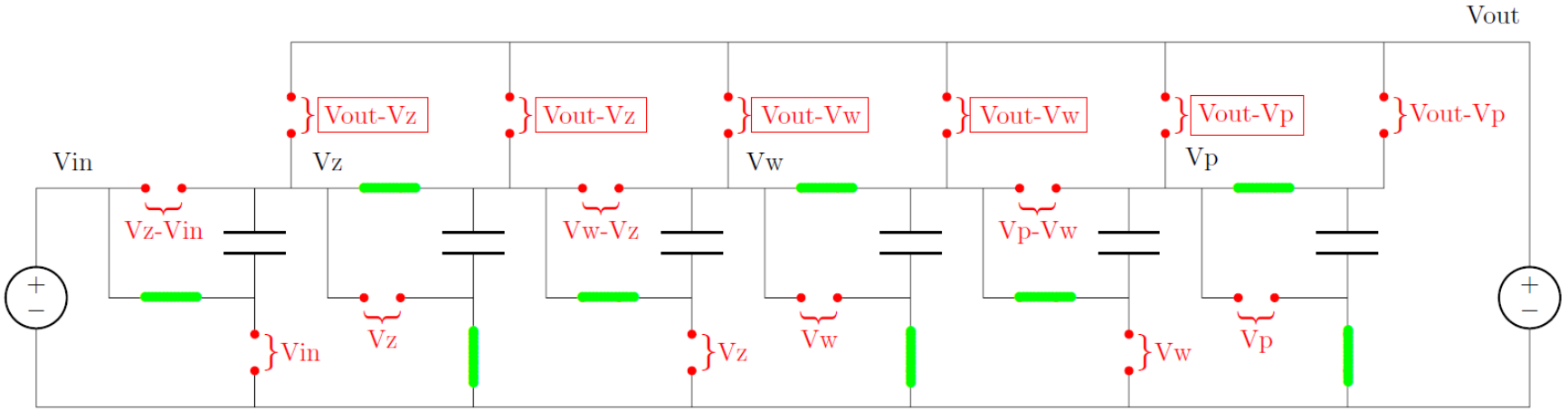
The charge from the input source during 1 complete switching cycle is

$$\Delta q_{in} = -C(V_z - V_{in} - V_{in}) - C(V_x - V_{in} - V_z) + C(V_{in} - V_z + V_{in}) \tag{B.66}$$

$$\Delta q_{in} = C(5V_{in} - V_x - V_z) = C\left(\frac{441}{104}V_{in} - \frac{21}{104}V_{out}\right) \tag{B.67}$$



(a) Phase one.



(b) Phase two.

Figure B-6: Both phases of Fibonacci charge pump when 6 stages are enabled.

The charge to the output source during 1 complete switching cycle is

$$\Delta q_{out} = -C(V_{out} - V_y - V_p) = C\left(\frac{21}{104}V_{in} - \frac{1}{104}V_{out}\right) \tag{B.68}$$

From Equations (B.67) and (B.68), the input-output charge and current relations are determined to be

$$21\Delta q_{out} = \Delta q_{in} \tag{B.69}$$

$$21I_{out} = I_{in} \tag{B.70}$$

Substituting Equation (B.68) into Equation (B.6) results in

$$I_{out} = C\left(\frac{21}{104}V_{in} - \frac{1}{104}V_{out}\right)f \tag{B.71}$$

which is the relationship between input voltage, output voltage, and output current. By substituting Equations (B.70) and (B.71) into the definition of input resistance, the input resistance is found to be

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{21I_{out}} = \frac{V_{in}}{21Cf(\frac{21}{104}V_{in} - \frac{1}{104}V_{out})} = \frac{104}{441Cf} \cdot \frac{21V_{in}}{21V_{in} - V_{out}} \tag{B.72}$$

Using Equation (B.69) and the definition of efficiency shows the efficiency to be

$$\eta = \frac{\Delta q_{out}V_{out}}{\Delta q_{in}V_{in}} = \frac{V_{out}}{21V_{in}} \tag{B.73}$$

B.2 Parasitic Losses

The previous analysis assumed no parasitic effects. This section incorporates the source-drain capacitances of the switches into the model. It is assumed that when opened, each switch's parasitic capacitor becomes fully charged, and when closed, each fully discharges. Therefore, the losses are assumed to be C_pV^2f for each capacitor, where C_p is the parasitic capacitance, V is the voltage developed across the

capacitor, and f is the operating frequency. Figures B-1 through B-6 show the voltages developed across each open switch during each phase. By inputting the values derived for intermediary nodes, the theoretical voltage across each switch can be determined for any given input and output voltage. Then, all of these losses can be summed to determine the total losses from the switches in the power path. The result for the 6-stage charge pump is:

$$P_{p,\,power\,path} = \sum_i C_p V_i^2 f = C_p f \left(\frac{24737}{5408} V_{in}^2 + \frac{23}{2704} V_{in} V_{out} + \frac{8673}{5408} V_{out}^2 \right) \tag{B.74}$$

Note that this equation sums only the unboxed parasitic capacitors in the previous figures. These are capacitors that turn on and off completely during each cycle and are referred to as the power path parasitic capacitors.

Because the actual charge pump has a configurable number of stages, every switching capacitor also has a switch directly connected to the output. Although these switches when unused never close to fully discharge the capacitor, they do change voltage during each phase. Again using the 6-stage charge pump as an example, each parasitic switch capacitor attached from the main, non-parasitic capacitor to the output experiences voltage changes of

$$\Delta V_{S4} : (V_{out} - V_{in}) - (V_{out} - V_z) = V_z - V_{in} \tag{B.75}$$

$$\Delta V_{S8} : (V_{out} - V_x) - (V_{out} - V_z) = V_z - V_x \tag{B.76}$$

$$\Delta V_{S12} : (V_{out} - V_x) - (V_{out} - V_w) = V_w - V_x \tag{B.77}$$

$$\Delta V_{S16} : (V_{out} - V_y) - (V_{out} - V_w) = V_w - V_y \tag{B.78}$$

$$\Delta V_{S20} : (V_{out} - V_y) - (V_{out} - V_p) = V_p - V_y \tag{B.79}$$

where the nomenclature of the switches follows that of Figure 4-7. When replacing the intermediary voltages with their solved values, the sum of the losses becomes

$$P_{p,\,output\,switches} = \sum_i C_p V_i^2 f = C_p f \left(\frac{1165}{2704} V_{in}^2 - \frac{235}{1352} V_{in} V_{out} + \frac{265}{2704} V_{out}^2 \right) \tag{B.80}$$

Note that this equation sums only the boxed parasitic capacitors, capacitors that remain completely off during each phase and that are attached from the output to some node in the power path. They are referred to as the output switches parasitic capacitors. Table B.4 at the end of this section shows the results for all types of losses for all 6 stages. Note that the 1-stage charge pump has no unused output switches attached to nodes in the power path. All power losses are of the form shown at the top of Table B.4, so the results are listed in terms of the coefficients γ, δ, and ϵ.

In the 1-, 2-, 3-, 4-, and 5-stage charge pumps, there are unused switches reserved for higher-stage charge pumps. In Figures B-1 through B-6, these are represented as unlabeled red dots. These open switches contribute some amount of parasitic capacitance. In the 5-stage case, the sixth charge pump is attached to node V_y, as seen in Figure B-5. This unused stage is shown in Figure B-7a, with the parasitic capacitors labeled C_p and the main switching capacitor labeled C. The switching capacitor is assumed to be very large compared to the parasitic capacitances and uncharged. Therefore, it can be shorted and ignored in this analysis. Just as in the analysis for the output switches, the losses in these capacitors are dependent only on changes in voltage. Since in the RF harvester the output is held at a constant voltage, it can be shorted to calculate the equivalent capacitance. Figure B-7b illustrates the simplified schematic. For the 5-stage charge pump, the losses due to unused stages is

$$P_{p,\,unused\,stages} = C_p(V_{out} - V_y)^2 f = C_p f \left(\frac{1}{25}V_{in}^2 - \frac{4}{25}V_{in}V_{out} + \frac{4}{25}V_{out}^2\right) \tag{B.81}$$

For the 1-, 2-, 3-, and 4-stage charge pumps, the unused stages are attached recursively. Figure B-8 is a schematic of the unused stages for a 1-stage charge pump. It can be seen that the schematic with its simplifications can reduce to Figure B-9, where C_{prev} is the unused-stages capacitance of the 2-stage charge pump. The equivalent parasitic capacitance for unused stages becomes

$$C_{p,\,eq} = (2C_p)||(2C_p + C_{prev}) = \frac{4C_p^2 + 2C_pC_{prev}}{4C_p + C_{prev}} \tag{B.82}$$

Since C_{prev} can be written as αC_p, α_n can be written as:

$$\alpha_n = \frac{4 + 2\alpha_{n+1}}{4 + \alpha_{n+1}} \tag{B.83}$$

where the numbering of n has been matched to the number of used stages out of the six available. The same process can be applied to other stages, and the results are shown in Tables B.1 and B.4.

In order to test the accuracy of these assumptions and analyses, several test cases were simulated in SPICE and compared to the theoretical predictions. The tests assumed that the parasitic losses had no effect on input power and were simply subtracted from the output power. The following values were used: C = 10 nF, C_p = 25 pF, V_{out} = 2 V, and f = 100 kHz. The results are shown in Tables B.2 and B.3. The errors between the theoretical analysis and SPICE simulations were very low, always less than 1.5%, suggesting a valid parasitics model.

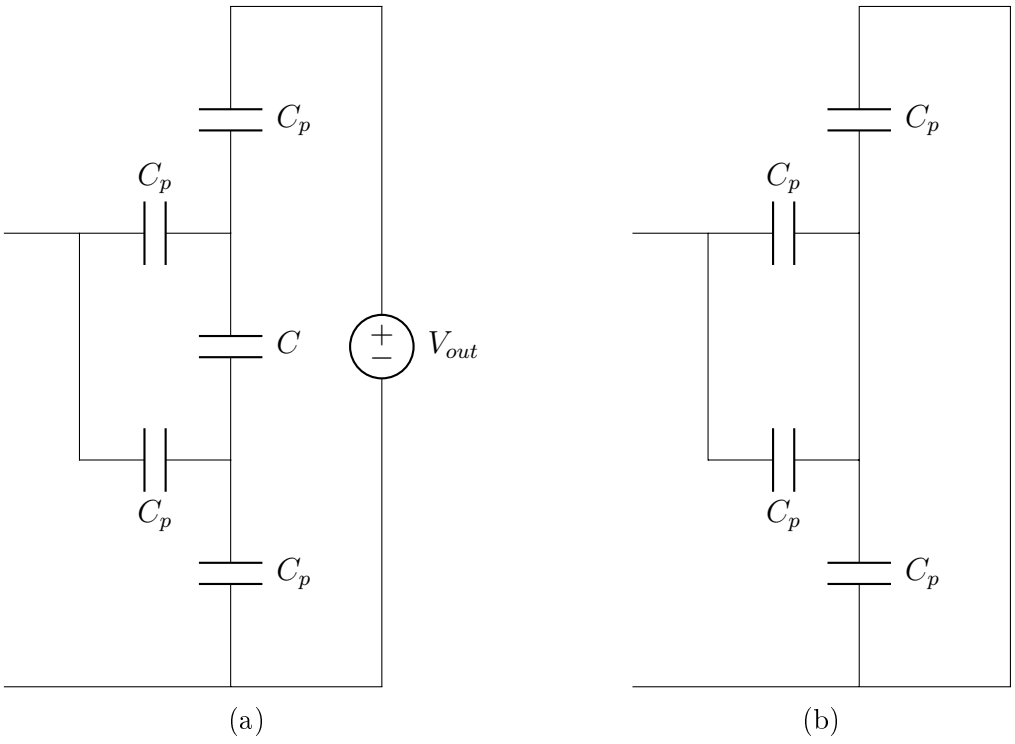


Figure B-7: (a) Unused sixth stage attached to 5-stage charge pump and (b) its simplified circuit

Table B.1: Parasitic losses from unused charge pumps for each stage.

No. of Stages	$\boldsymbol{\alpha}$	$\boldsymbol{P_{p,\,unused\,stages}}$
1	$^{110}/_{89}$	$\frac{110}{89}C_p(V_{out}-V_{in})^2 f$
2	$^{21}/_{17}$	$\frac{21}{17}C_p(V_{out}-V_z)^2 f$
3	$^{16}/_{13}$	$\frac{16}{13}C_p(V_{out}-V_x)^2 f$
4	$^{6}/_{5}$	$\frac{6}{5}C_p(V_{out}-V_w)^2 f$
5	1	$C_p(V_{out}-V_y)^2 f$

Table B.2: Theory vs. SPICE on charge pump input power with 2-V load.

No. of Stages	**Vin (V)**	$\mathbf{P_{in}}$ **Theory** ($\boldsymbol{\mu W}$)	$\mathbf{P_{in}}$ **SPICE** ($\boldsymbol{\mu W}$)	$\mathbf{P_{in}}$ **Error**
1	1.2	960	959.5	0.05%
2	0.8	480	479.305	0.14%
3	0.6	500	501.55	0.31%
4	0.4	256	256.605	0.25%
5	0.3	182.25	185.86	0.33%
6	0.2	88.846	89.14	0.33%

Table B.3: Theory vs. SPICE on charge pump output power with 2-V load.

No. of Stages	**Vin (V)**	$\mathbf{P_{out}}$ **Theory** ($\boldsymbol{\mu W}$)	$\mathbf{P_{out}}$ **SPICE** ($\boldsymbol{\mu W}$)	$\mathbf{P_{out}}$ **Error**
1	1.2	787.622	787.25	0.05%
2	0.8	382.888	382.495	0.10%
3	0.6	314.659	316.42	0.56%
4	0.4	142.237	141.695	0.38%
5	0.3	76.073	76.85	1.02%
6	0.2	24.955	25.3225	1.47%

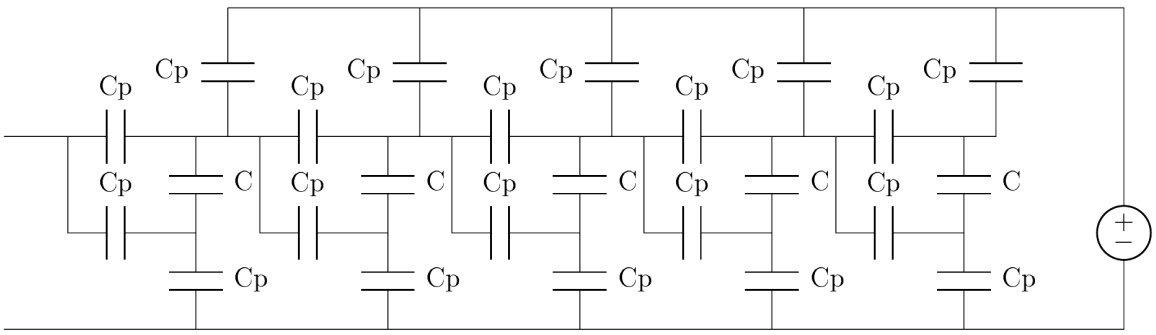


Figure B-8: Unused stages attached to 1-stage charge pump.

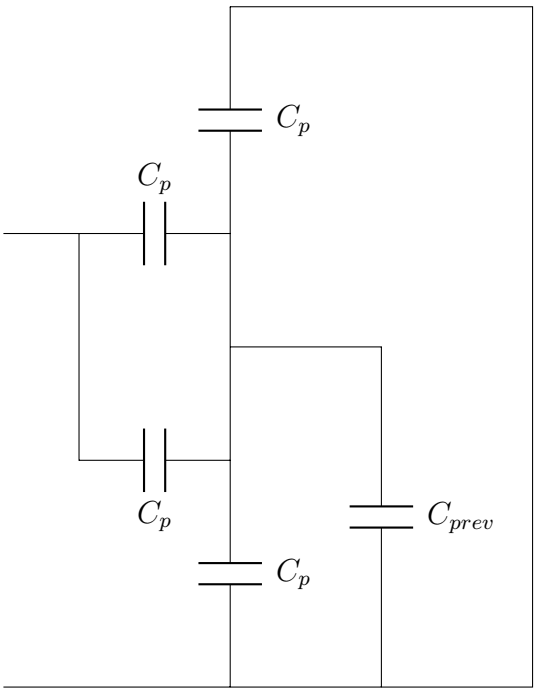


Figure B-9: Recursive model of unused stages.

Table B.4: Summary of parasitic losses from switch capacitance.

No. of Stages	$P_p = C_p f(\gamma V_{in}^2 - \delta V_{in} V_{out} + \epsilon V_{out}^2)$											
	$P_{p,\,power\,path}$			$P_{p,\,output\,switches}$			$P_{p,\,unused\,stages}$			$P_{p,\,total}$		
	γ	δ	ϵ	γ	δ	ϵ	γ	δ	ϵ	γ	δ	ϵ
1	4	4	2	0	0	0	$^{110}/_{89}$	$^{220}/_{89}$	$^{110}/_{89}$	$^{466}/_{89}$	$^{576}/_{89}$	$^{288}/_{89}$
2	$^{19}/_{4}$	$^{5}/_{2}$	$^{7}/_{4}$	$^{1}/_{4}$	$^{1}/_{2}$	$^{1}/_{4}$	$^{21}/_{68}$	$^{21}/_{34}$	$^{21}/_{68}$	$^{361}/_{68}$	$^{123}/_{34}$	$^{157}/_{68}$
3	$^{163}/_{36}$	$^{17}/_{18}$	$^{55}/_{36}$	$^{17}/_{36}$	$^{7}/_{18}$	$^{5}/_{36}$	$^{4}/_{13}$	$^{8}/_{13}$	$^{4}/_{13}$	$^{69}/_{13}$	$^{76}/_{39}$	$^{77}/_{39}$
4	$^{1021}/_{225}$	$^{64}/_{225}$	$^{319}/_{225}$	$^{86}/_{225}$	$^{74}/_{225}$	$^{29}/_{225}$	$^{6}/_{125}$	$^{24}/_{125}$	$^{24}/_{125}$	$^{621}/_{125}$	$^{302}/_{375}$	$^{652}/_{375}$
5	$^{733}/_{160}$	$^{1}/_{16}$	$^{253}/_{160}$	$^{189}/_{400}$	$^{43}/_{200}$	$^{41}/_{400}$	$^{1}/_{25}$	$^{4}/_{25}$	$^{4}/_{25}$	$^{163}/_{32}$	$^{7}/_{16}$	$^{59}/_{32}$
6	$^{24737}/_{5408}$	$-^{23}/_{2704}$	$^{8673}/_{5408}$	$^{1165}/_{2704}$	$^{235}/_{1352}$	$^{265}/_{2704}$	0	0	0	$^{27067}/_{5408}$	$^{447}/_{2704}$	$^{9203}/_{5408}$

B.3 Effect of Parasitics on Unloaded Voltage Gain

While the unloaded gains in the ideal cases are very straightforward to derive, predicting the unloaded gains with parasitics is less so. It was derived that the output current can be represented as

$$I_{out} = Cf(\alpha V_{in} - \beta V_{out}) \tag{B.84}$$

and that the total parasitic loss can be represented as

$$P_{p,\,total} = C_p f(\gamma V_{in}^2 - \delta V_{in} V_{out} + \epsilon V_{out}^2) \tag{B.85}$$

By assuming the parasitic losses can simply be modeled as a load on the output, then

$$P_{p,\,total} = V_{out} I_{p,\,total} \tag{B.86}$$

By equating Equations (B.85) and (B.86) and by substituting $I_{p,\,total}$ with the expression for I_{out} in Equation (B.84), the expressions combine to

$$\frac{C_p f(\gamma V_{in}^2 - \delta V_{in} V_{out} + \epsilon V_{out}^2)}{V_{out}} = Cf(\alpha V_{in} - \beta V_{out}) \tag{B.87}$$

Solving for the gain gives the final result of

$$\frac{V_{out}}{V_{in}} = \frac{\alpha C + \delta C_p \pm \sqrt{(\alpha C + \delta C_p)^2 - 4\gamma C_p(\epsilon C_p + \beta C)}}{2(\epsilon C_p + \beta C)} \tag{B.88}$$

This model was also compared against SPICE. The results are shown in Table B.5. Values of $C = 10$ nF, $C_p = 25$ pF, and $f = 100$ kHz were used. Again, very low errors between the model and SPICE simulations suggest an accurate parasitics model.

Table B.5: Theory vs. SPICE on charge pump unloaded voltage gain.

No. of Stages	**Vin (V)**	**Theoretical Unloaded Gain w/o Parasitics**	**Theoretical Unloaded Gain w/Parasitics**	**SPICE Unloaded Gain w/Parasitics**	**Error**
1	1.2	2	1.9935	1.9900	0.17%
2	0.8	3	2.9748	2.9738	0.04%
3	0.6	5	4.8687	4.8665	0.05%
4	0.4	8	7.5154	7.4808	0.46%
5	0.3	13	10.974	10.987	0.12%
6	0.2	21	14.526	14.566	0.28%

Appendix C

Measured Charge Pump Characteristics

Chapter 4 discusses several of the experimental results of the Fibonacci charge pump. This appendix contains figures illustrating several behaviors of individual charge pumps for 1 through 6 stages. These behaviors are

- the supply current draw from the 3-V power supply, with both no load and a 2-V load;
- the unloaded voltage gain, with ideal theoretical, theoretical-with-parasitics, and measured behaviors;
- the unloaded input resistance, which would ideally be infinite;
- the input resistance with a 2-V load, with both theoretical and measured behaviors;
- the input power with a 2-V load, with both theoretical and measured behaviors;
- the output power with a 2-V load, with ideal theoretical, theoretical-with-parasitics, and measured behaviors;
- the supply power with a 2-V load;

- and the efficiency, with ideal theoretical, theoretical-with-parasitics, measured-excluding-power supply, and measured-including-power supply behaviors.

Note that according to the theoretical model presented in Appendix B, parasitics only affect the output behaviors: unloaded voltage gain, output power, and efficiency.

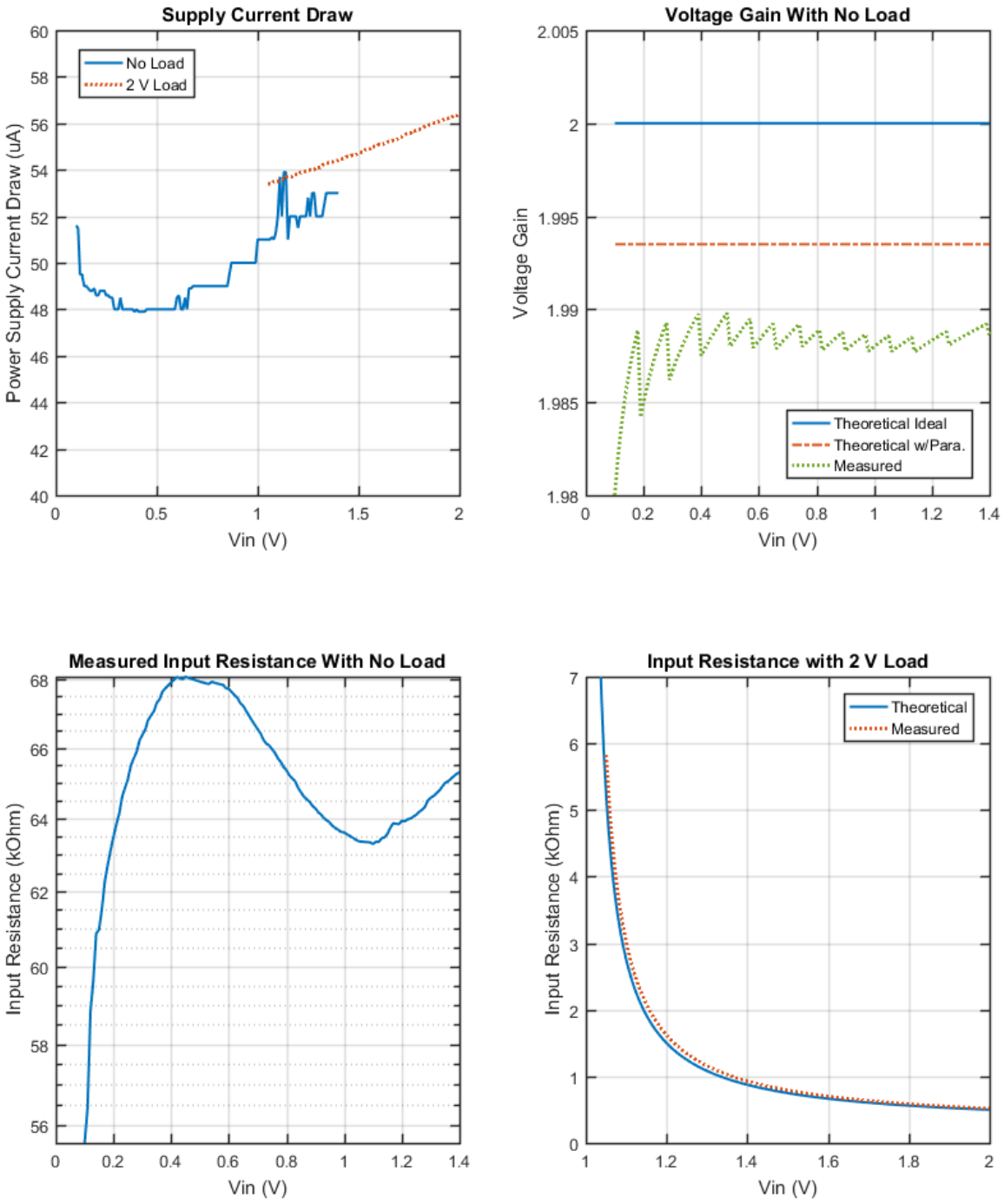


Figure C-1: Measured characteristics of 1-stage charge pump.

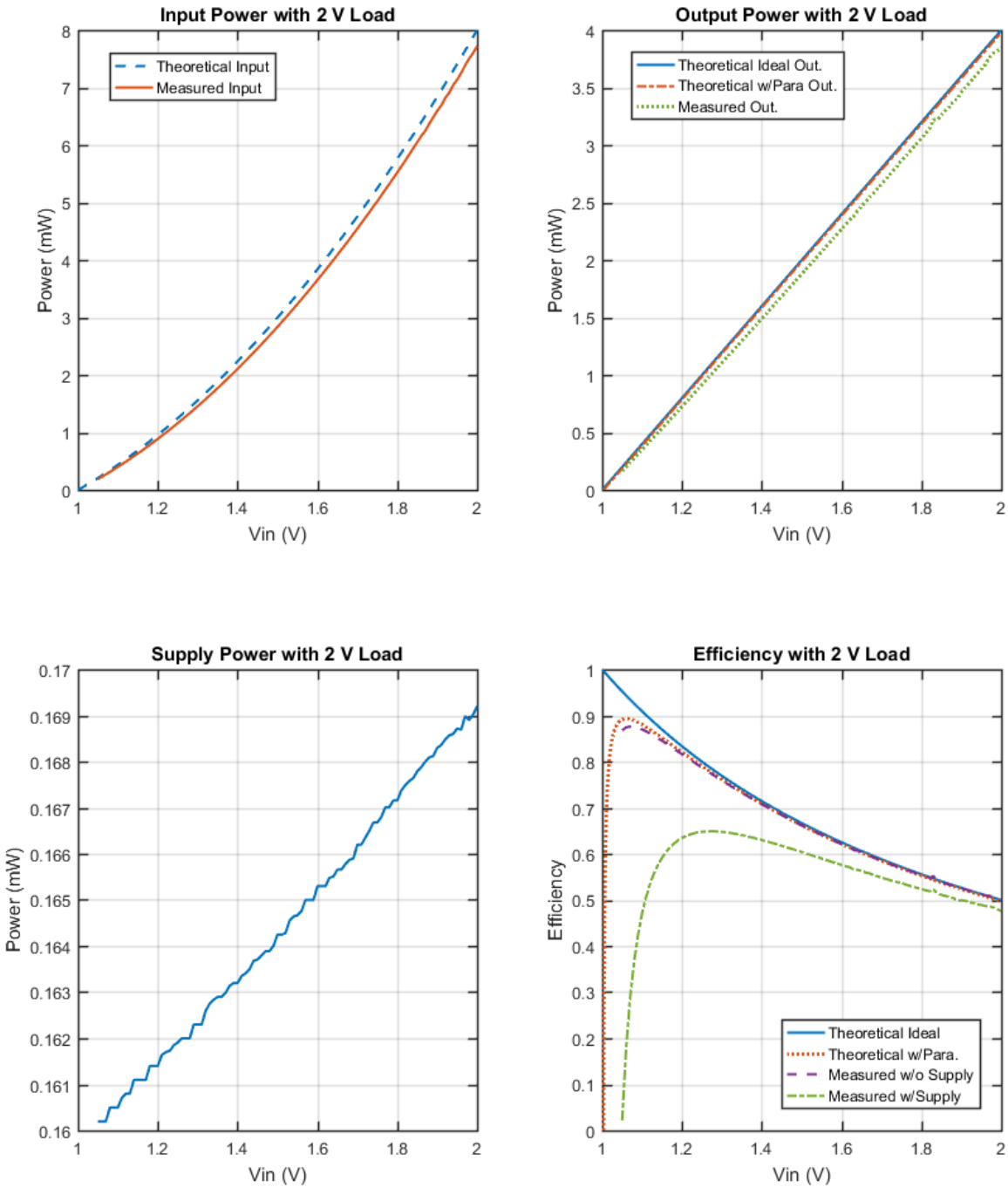


Figure C-2: Measured characteristics of 1-stage charge pump (cont.).

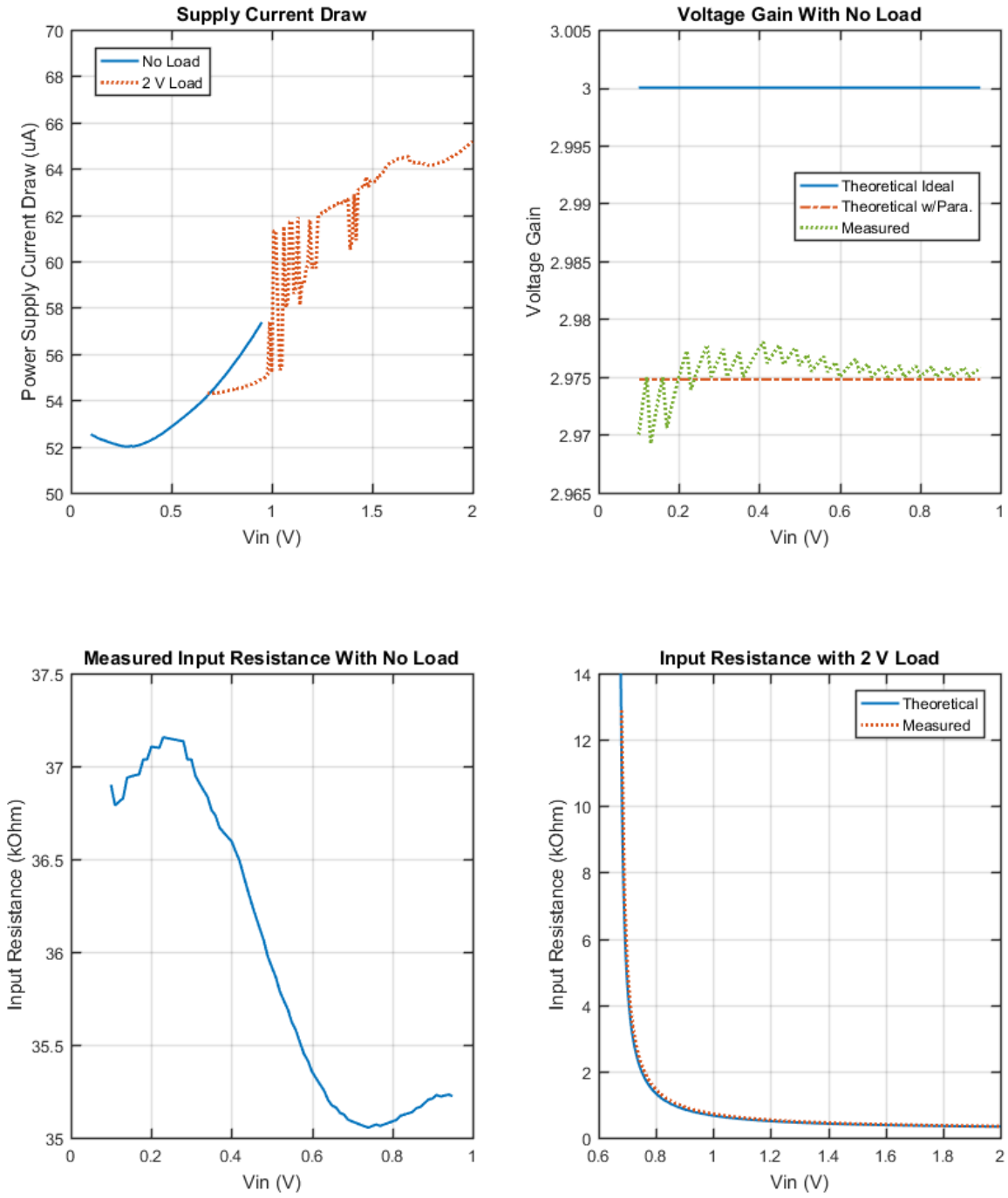


Figure C-3: Measured characteristics of 2-stage charge pump.

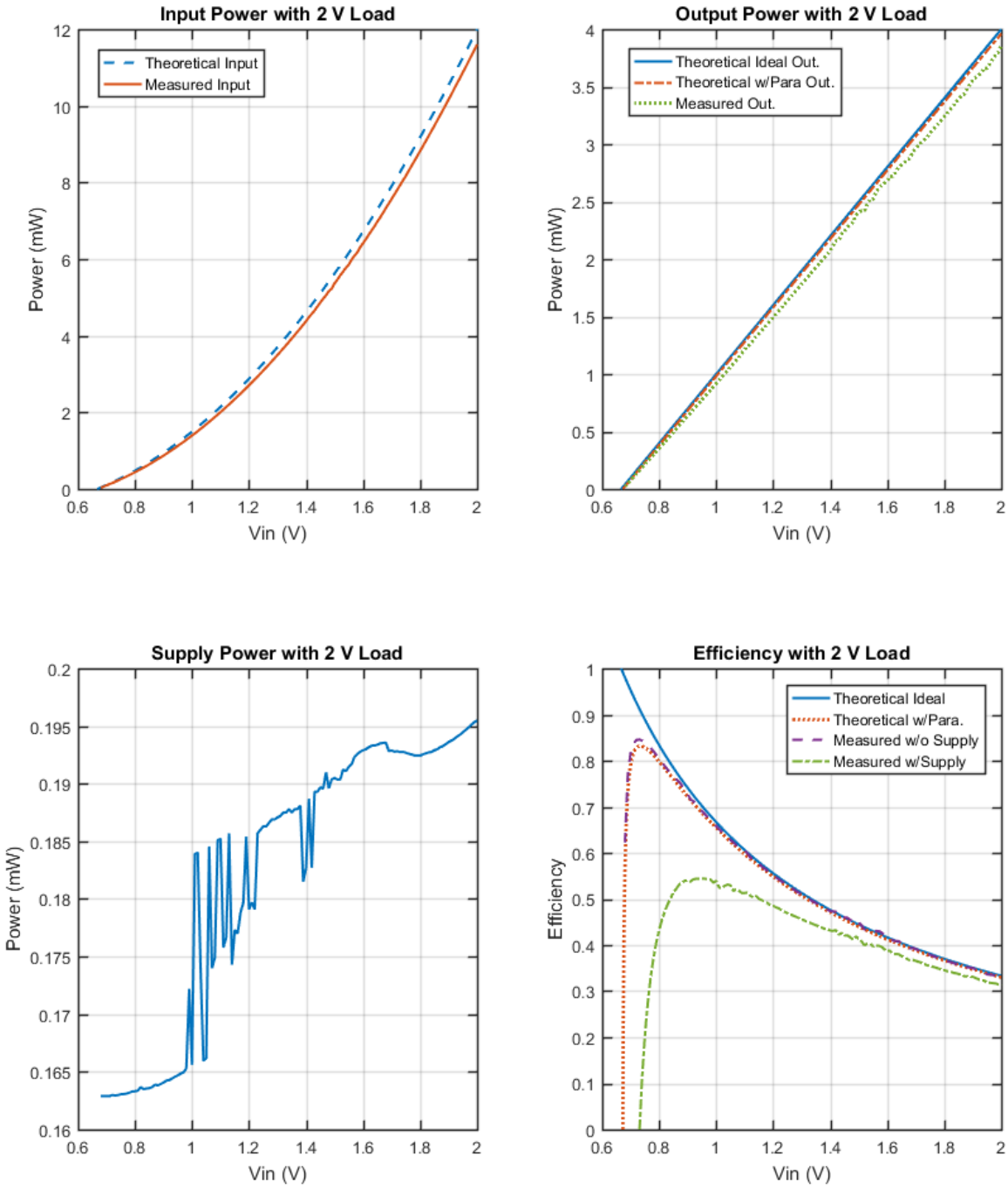


Figure C-4: Measured characteristics of 2-stage charge pump (cont.).

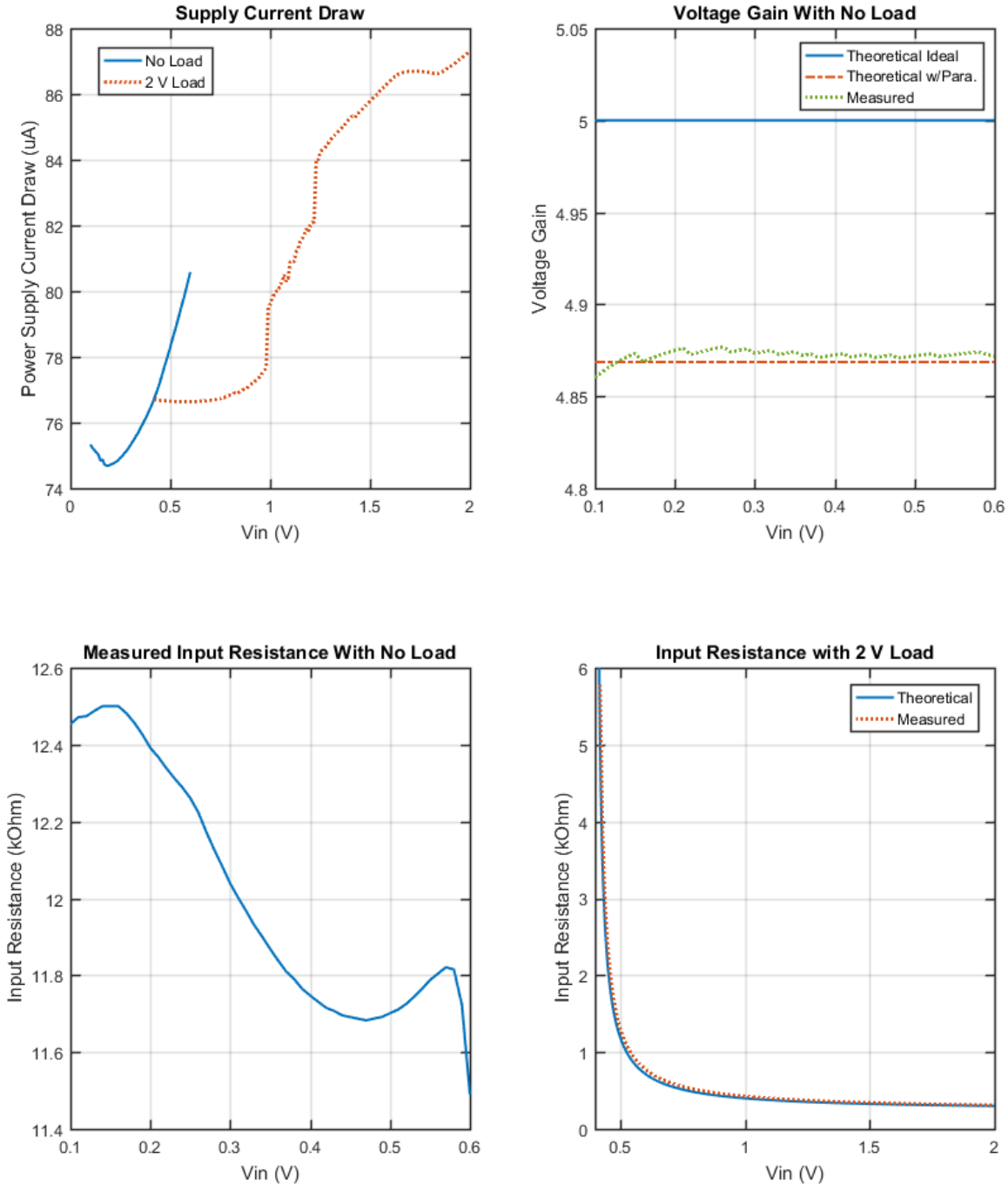


Figure C-5: Measured characteristics of 3-stage charge pump.

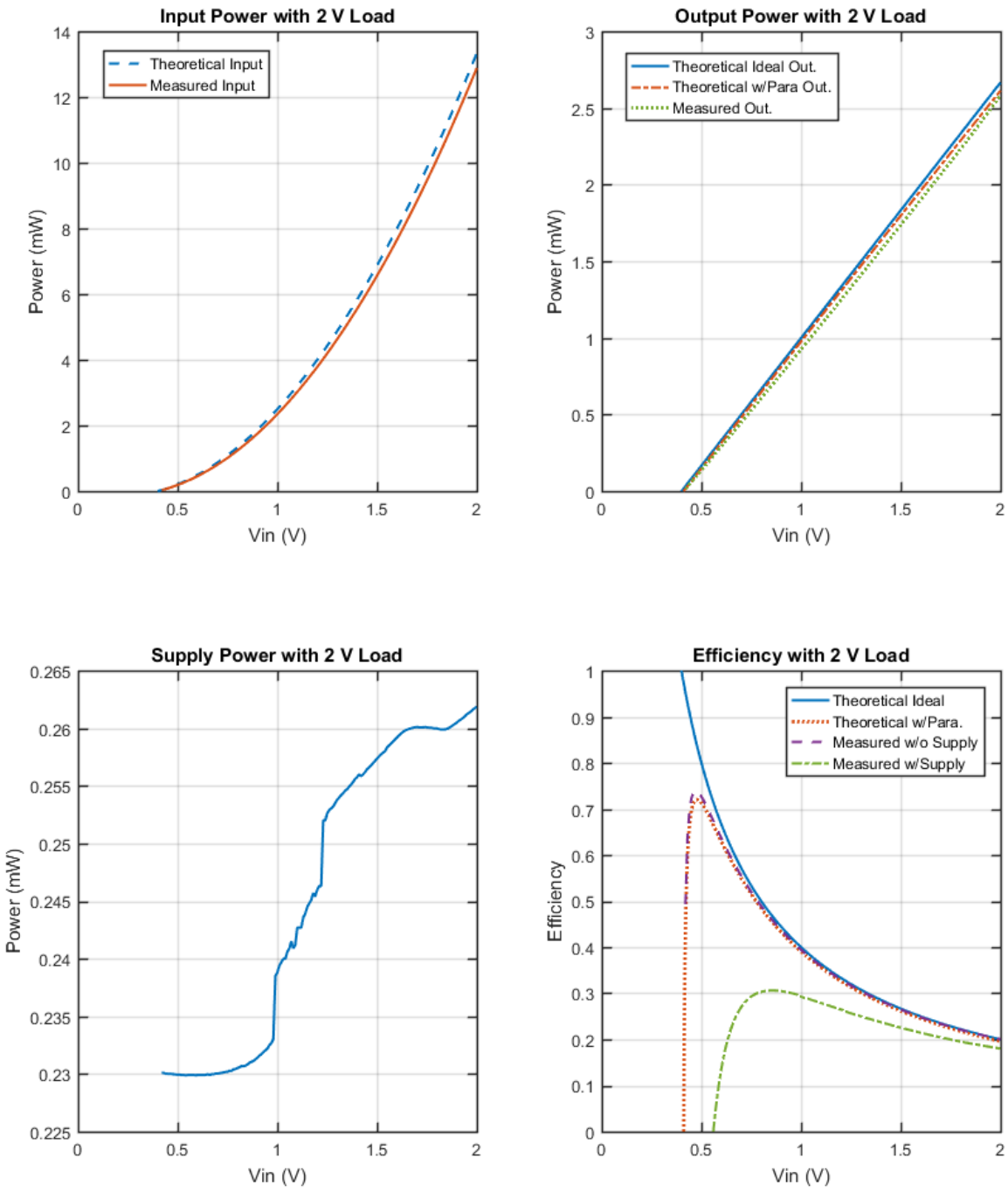


Figure C-6: Measured characteristics of 3-stage charge pump (cont.).

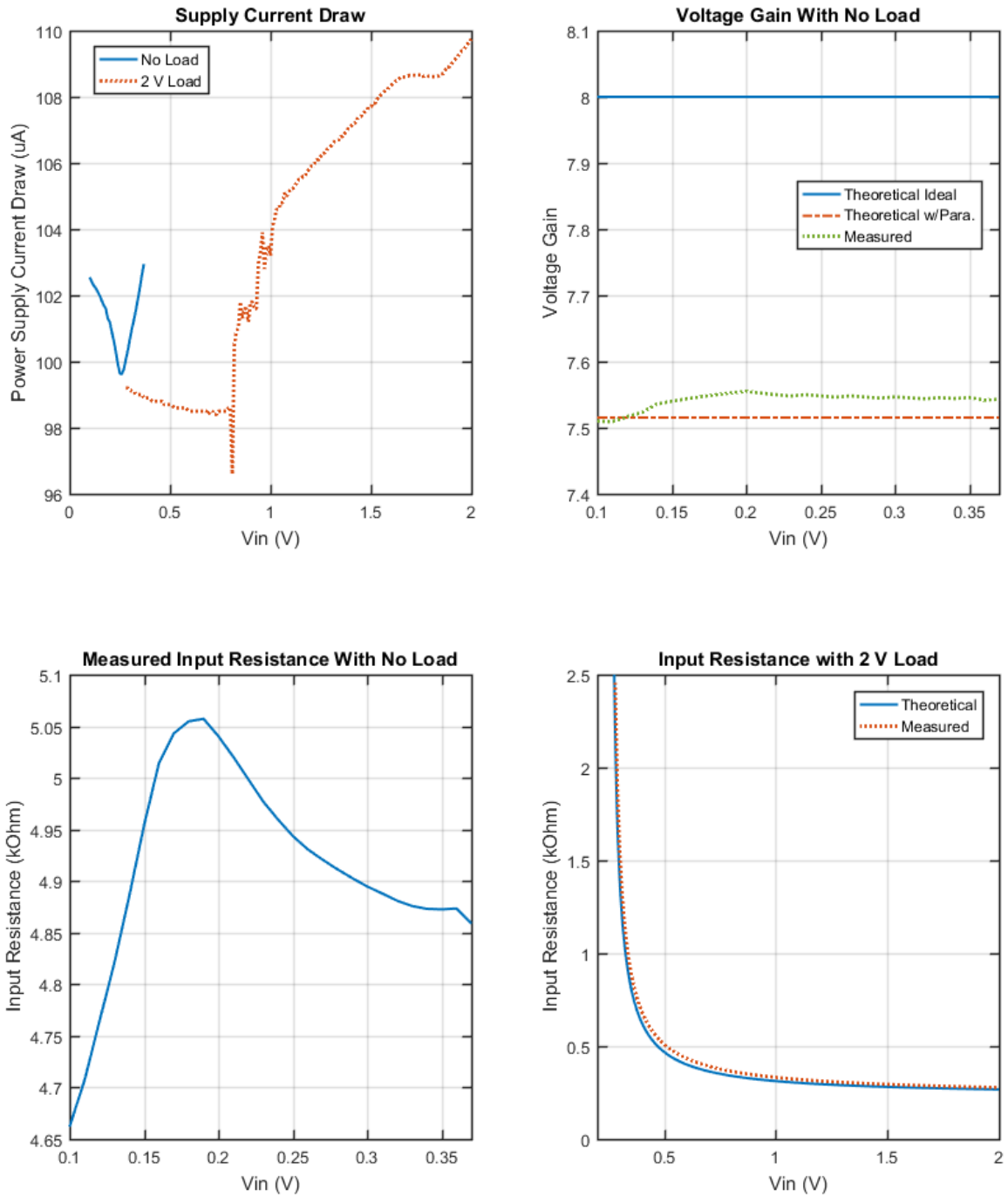


Figure C-7: Measured characteristics of 4-stage charge pump.

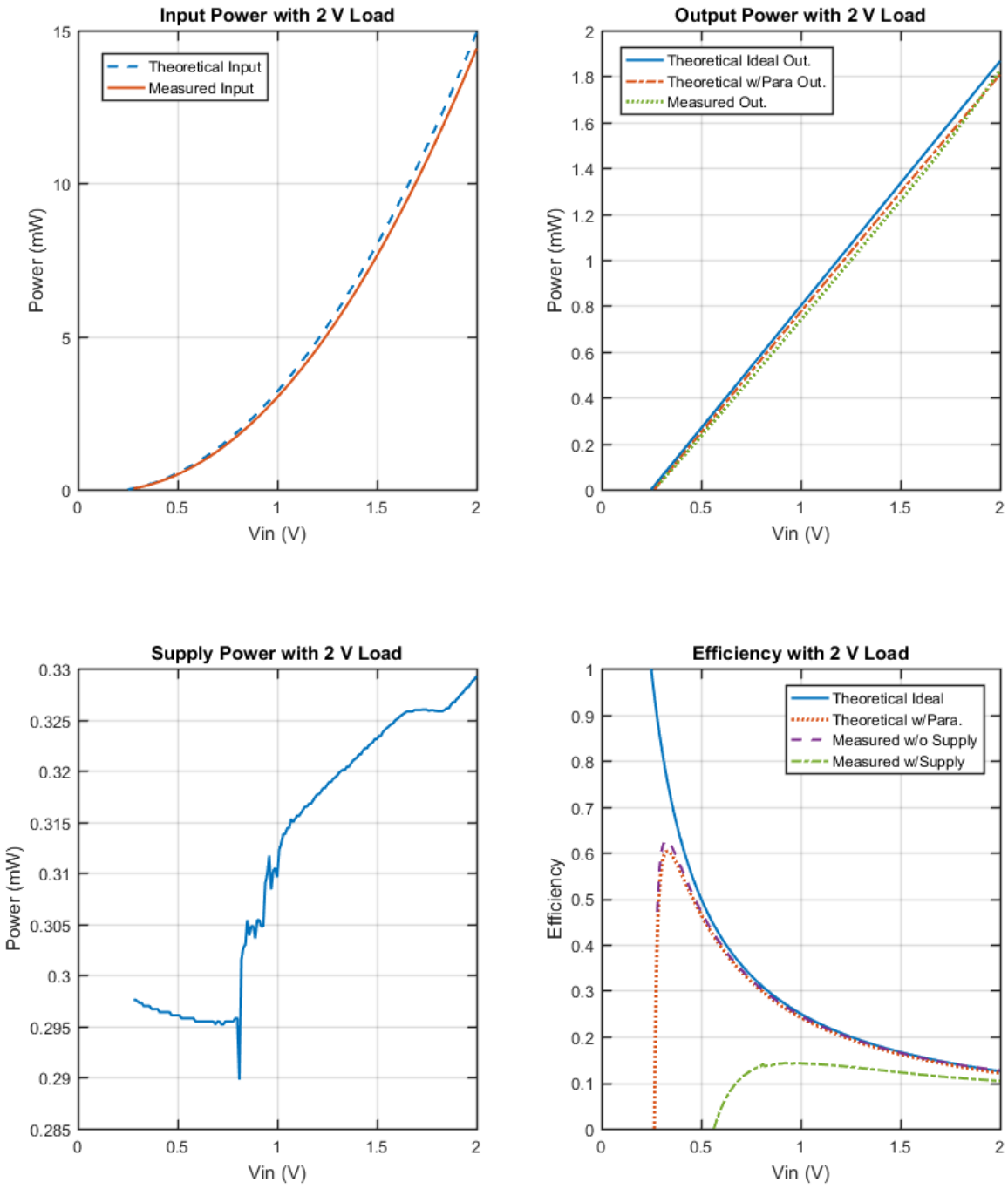


Figure C-8: Measured characteristics of 4-stage charge pump (cont.).

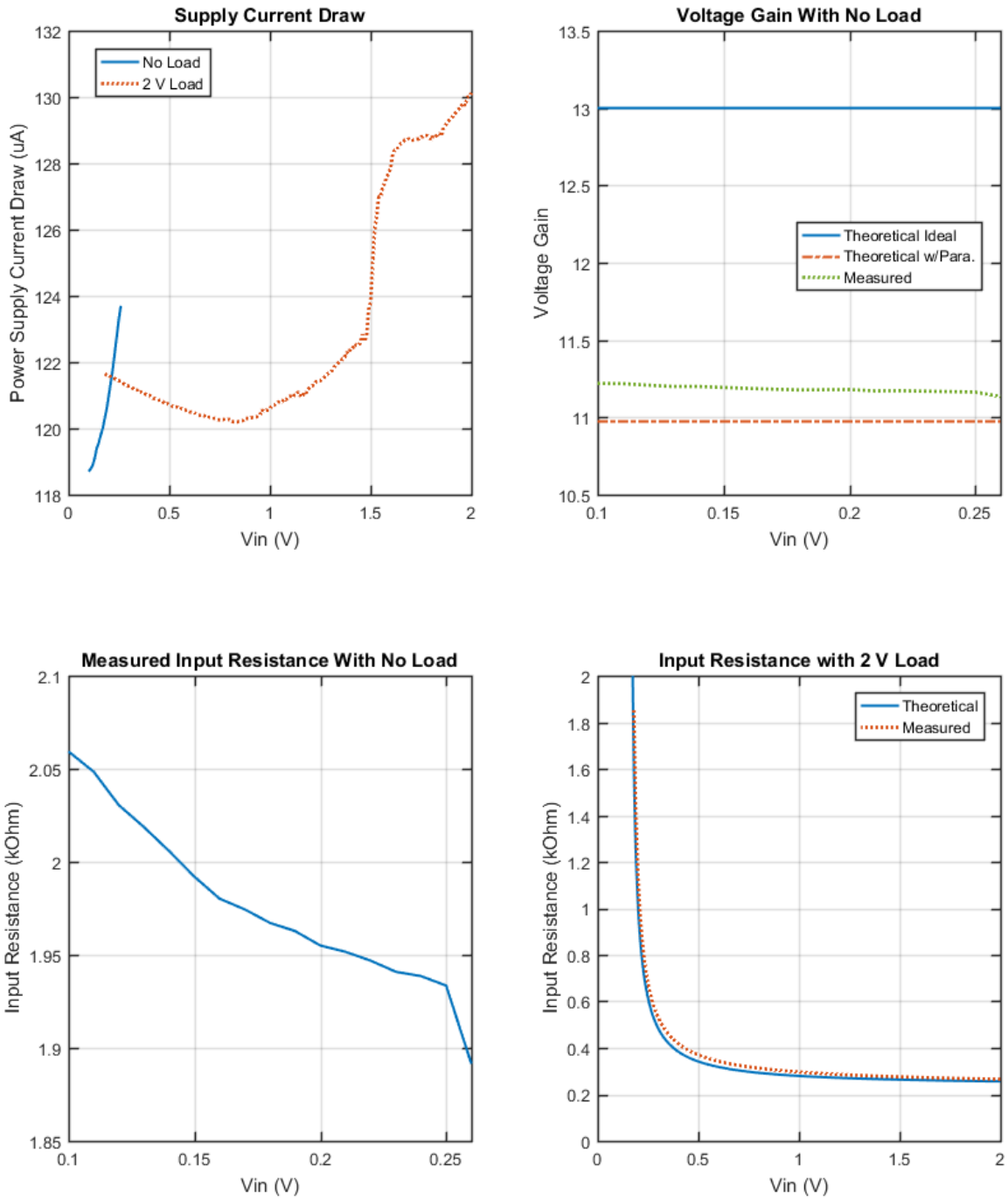


Figure C-9: Measured characteristics of 5-stage charge pump.

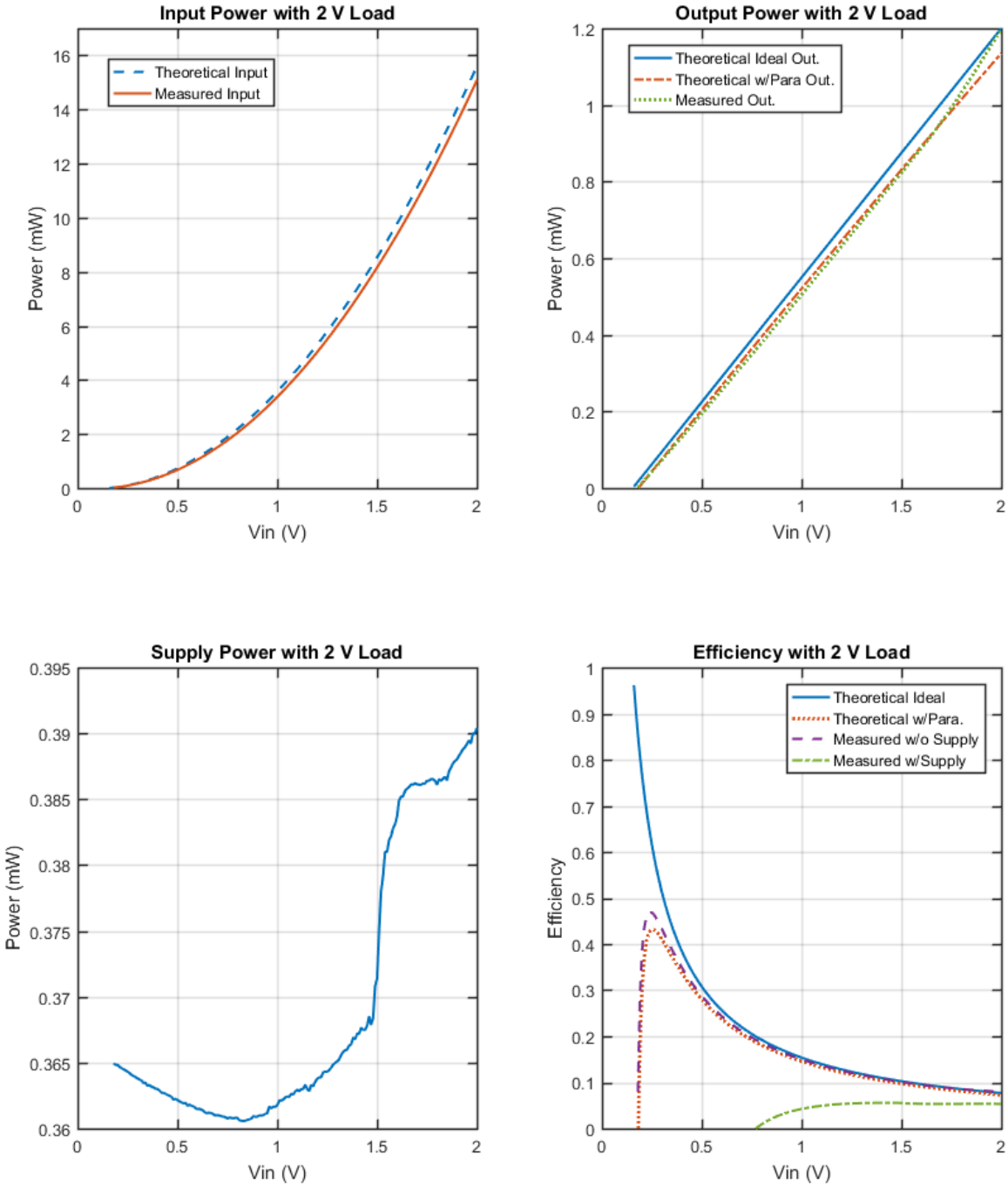


Figure C-10: Measured characteristics of 5-stage charge pump (cont.).

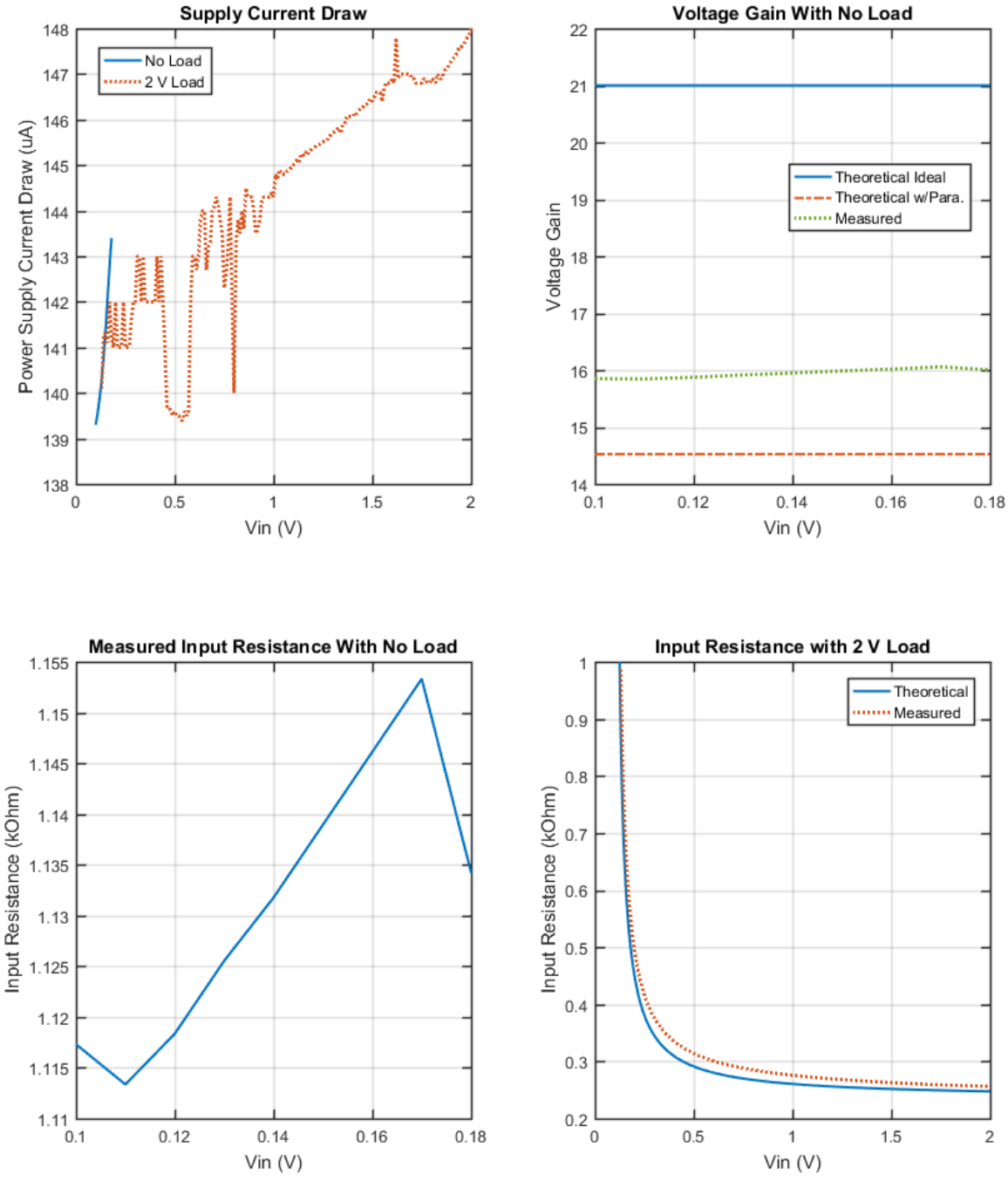


Figure C-11: Measured characteristics of 6-stage charge pump.

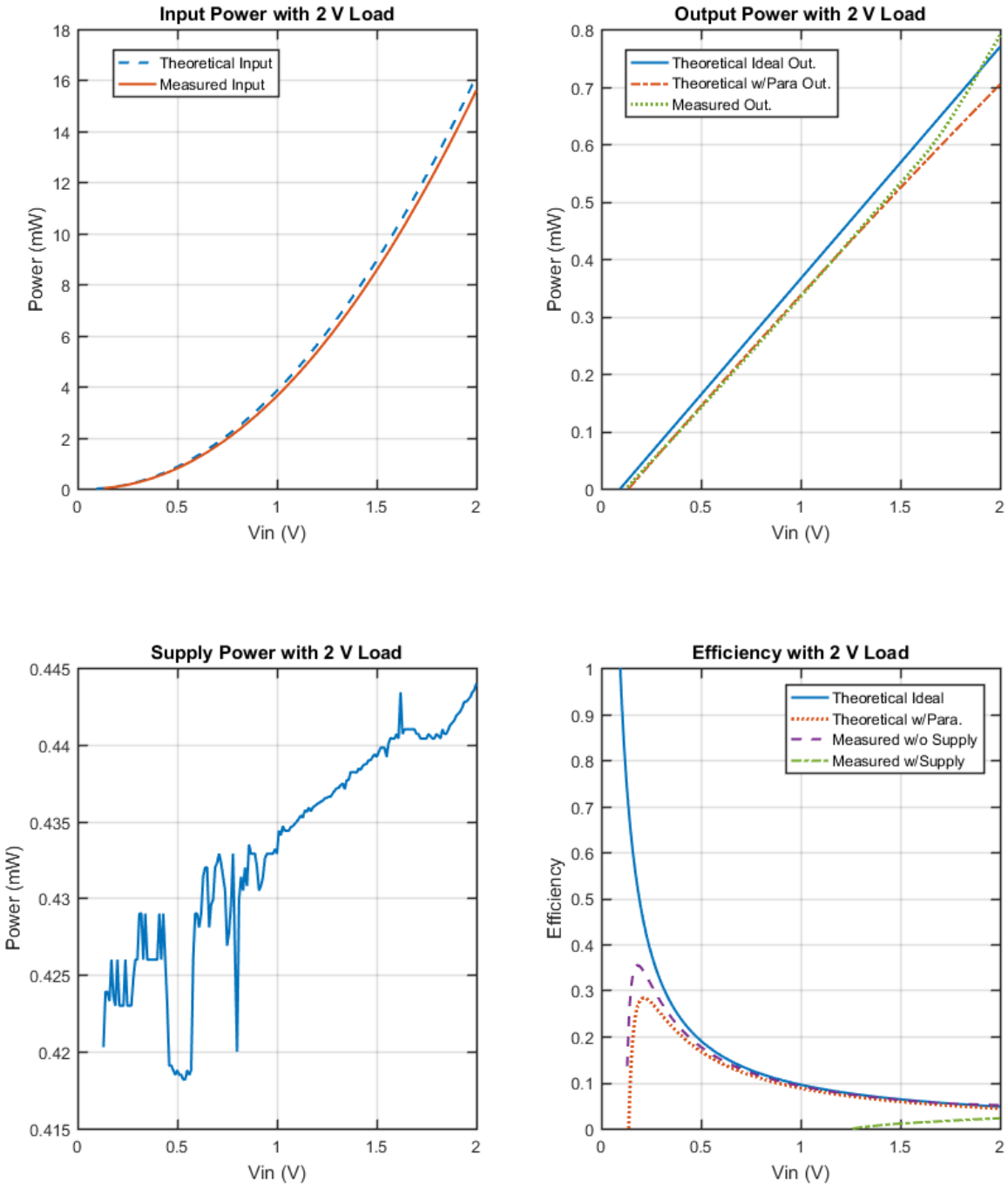


Figure C-12: Measured characteristics of 6-stage charge pump (cont.).

Bibliography

[1] A. A. Abdelmoaty, M. Al-Shyoukh, Y. C. Hsu, and A. A. Fayed. A mppt circuit with 25 μW power consumption and 99.7% tracking efficiency for pv systems. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 64(2):272–282, Feb 2017.

[2] J. Ahmad. A fractional open circuit voltage based maximum power point tracker for photovoltaic arrays. In *2010 2nd International Conference on Software Technology and Engineering*, volume 1, pages V1–247–V1–250, Oct 2010.

[3] E. E. Aktakka, H. Kim, and K. Najafi. Energy scavenging from insect flight. *Journal of Micromechanics and Microengineering*, 21(9):1–11, Aug 2011.

[4] C. Alippi and C. Galperti. An adaptive system for optimal solar energy harvesting in wireless sensor network nodes. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 55(6):1742–1750, July 2008.

[5] Y. Allasasmeh and S. Gregori. A performance comparison of dickson and fibonacci charge pumps. In *2009 European Conference on Circuit Theory and Design*, pages 599–602, Aug 2009.

[6] P. Aminov and J. P. Agrawal. Rf energy harvesting. In *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)*, pages 1838–1841, May 2014.

[7] S. Bandyopadhyay and A. P. Chandrakasan. Platform architecture for solar, thermal, and vibration energy combining with mppt and single inductor. *IEEE Journal of Solid-State Circuits*, 47(9):2199–2215, Sept 2012.

[8] M. Berrera, A. Dolara, R. Faranda, and S. Leva. Experimental test of seven widely-adopted mppt algorithms. In *2009 IEEE Bucharest PowerTech*, pages 1–8, June 2009.

[9] D. Bouchouicha, M. Latrach, F. Dupont, and L. Ventura. An experimental evaluation of surrounding rf energy harvesting devices. In *The 40th European Microwave Conference*, pages 1381–1384, Sept 2010.

[10] A. Cabrini, L. Gobbi, and G. Torelli. Voltage gain analysis of integrated fibonacci-like charge pumps for low power applications. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 54(11):929–933, Nov 2007.

[11] S. C. Chang, F. M. Yaul, A. Dominguez-Garcia, F. O'Sullivan, D. M. Otten, and J. H. Lang. Harvesting energy from moth vibrations during flight. In *Proc. International PowerMEMS Conference*, pages 57–60, Dec 2009.

[12] I. Y. W. Chung and Y. C. Liang. A low-cost photovoltaic energy harvesting circuit for portable devices. In *2011 IEEE Ninth International Conference on Power Electronics and Drive Systems*, pages 334–339, Dec 2011.

[13] Cymbet Corporation. *EnerChip Bare Die*, 2016. Rev. 6.

[14] D. C. Daly, P. P. Mercier, M. Bhardwaj, A. L. Stone, Z. N. Aldworth, T. L. Daniel, J. Voldman, J. G. Hildebrand, and A. P. Chandrakasan. A pulsed uwb receiver soc for insect motion control. *IEEE Journal of Solid-State Circuits*, 45(1):153–166, Jan 2010.

[15] D. Das. Fpga based implementation of mppt of solar cell. In *2012 National Conference on Computing and Communication Systems*, pages 1–5, Nov 2012.

[16] S. Dhar, R. Sridhar, and G. Mathew. Implementation of pv cell based standalone solar power system employing incremental conductance mppt algorithm. In *2013 International Conference on Circuits, Power and Computing Technologies (ICCPCT)*, pages 356–361, March 2013.

[17] N. M. Din, C. K. Chakrabarty, A. Bin Ismail, K. K. A. Devi, and W.-Y. Chen. Design of RF Energy Harvesting System for Energizing Low Power Devices. *Progress In Electromagnetics Research*, 132:49–69, September 2012.

[18] C. Ding, S. Heidari, Y. Wang, Y. Liu, and J. Hu. Multi-source in-door energy harvesting for non-volatile processors. In *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 173–176, May 2016.

[19] M. A. Elgendy, B. Zahawi, and D. J. Atkinson. Assessment of the incremental conductance maximum power point tracking algorithm. *IEEE Transactions on Sustainable Energy*, 4(1):108–117, Jan 2013.

[20] D. Fan, D. Rich, T. Holtzman, P. Ruther, J.W. Dalley, A. Lopez, et al. A wireless multi-channel recording system for freely behaving mice and rats. *PLoS ONE*, 6(7):e22033, July 2011.

[21] M. Fu, T. Zhang, X. Zhu, and C. Ma. A 13.56 mhz wireless power transfer system without impedance matching networks. In *2013 IEEE Wireless Power Transfer (WPT)*, pages 222–225, May 2013.

[22] N. Ghafouri, H. Kim, M. Z. Atashbar, and K. Najafi. A micro thermoelectric energy scavenger for a hybrid insect. In *2008 IEEE Sensors*, pages 1249–1252, Oct 2008.

[23] K. Gudan, S. Chemishkian, J. J. Hull, S. J. Thomas, J. Ensworth, and M. S. Reynolds. A 2.4ghz ambient rf energy harvesting system with -20dbm minimum input power and nimh battery storage. In *2014 IEEE RFID Technology and Applications Conference (RFID-TA)*, pages 7–12, Sept 2014.

[24] N. J. Guilar, R. Amirtharajah, P. J. Hurst, and S. H. Lewis. An energy-aware multiple-input power supply with charge recovery for energy harvesting applications. In *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, pages 298–299,299a, Feb 2009.

[25] R. Gules, J. D. P. Pacheco, H. L. Hey, and J. Imhoff. A maximum power point tracking system with parallel connection for pv stand-alone applications. *IEEE Transactions on Industrial Electronics*, 55(7):2674–2683, July 2008.

[26] R. R. Harrison, H. Fotowat, R. Chan, R. J. Kier, R. Olberg, A. Leonardo, and F. Gabbiani. Wireless neural/emg telemetry systems for small freely moving animals. *IEEE Transactions on Biomedical Circuits and Systems*, 5(2):103–111, April 2011.

[27] J. Jean, A. Wang, and V. Bulovic. In situ vapor-deposited parylene substrates for ultra-thin, lightweight organic solar cells. *Organic Electronics*, 31:120–126, Apr 2016.

[28] H. Kim, S. Kim, C. K. Kwon, Y. J. Min, C. Kim, and S. W. Kim. An energy-efficient fast maximum power point tracking circuit in an 800-uw photovoltaic energy harvester. *IEEE Transactions on Power Electronics*, 28(6):2927–2935, June 2013.

[29] H. Kim, Y. J. Min, C. H. Jeong, K. Y. Kim, C. Kim, and S. W. Kim. A 1-mw solar-energy-harvesting circuit using an adaptive mppt with a sar and a counter. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 60(6):331–335, June 2013.

[30] S. Kitazawa, H. Ban, and K. Kobayashi. Energy harvesting from ambient rf sources. In *2012 IEEE MTT-S International Microwave Workshop Series on Innovative Wireless Power Transmission: Technologies, Systems, and Applications*, pages 39–42, May 2012.

[31] Y. Kuwana, N. Ando, R. Kanzaki, and I. Shimoyama. A radiotelemetry system for muscle potential recordings from freely flying insects. In *Proceedings of the First Joint BMES/EMBS Conference. 1999 IEEE Engineering in Medicine and Biology 21st Annual Conference and the 1999 Annual Fall Meeting of the Biomedical Engineering Society (Cat. N*, volume 2, pages 846 vol.2–, Oct 1999.

[32] D. C. Law, K. M. Edmondson, N. Siddiqi, A. Paredes, R. r. King, G. Glenn, E. Labios, M. H. Haddad, T. D. Isshiki, and N. H. Karam. Lightweight, flexible, high-efficiency iii-v multijunction cells. In *2006 IEEE 4th World Conference on Photovoltaic Energy Conference*, volume 2, pages 1879–1882, May 2006.

[33] Z. Liang, R. Guo, and A. Huang. A new cost-effective analog maximum power point tracker for pv systems. In *2010 IEEE Energy Conversion Congress and Exposition*, pages 624–631, Sept 2010.

[34] O. Lopez-Lapena, M. T. Penella, and M. Gasulla. A new mppt method for low-power solar energy harvesting. *IEEE Transactions on Industrial Electronics*, 57(9):3129–3138, Sept 2010.

[35] Eduardo Lorenzo et al. *Solar Electricity. Engineering of photovoltaic systems*, section 2, pages 75–80. PROGENSA, Sevilla, Spain, first edition, Nov 1994.

[36] M. S. Makowski and D. Maksimovic. Performance limits of switched-capacitor dc-dc converters. In *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE*, volume 2, pages 1215–1221 vol.2, Jun 1995.

[37] K. Mann, T. L. Massey, S. Guha, J. P. van Kleef, and M. M. Maharbiz. A wearable wireless platform for visually stimulating small flying insects. In *2014 36th Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, pages 1654–1657, Aug 2014.

[38] M. A. S. Masoum, H. Dehbonei, and E. F. Fuchs. Theoretical and experimental analyses of photovoltaic systems with voltageand current-based maximum power-point tracking. *IEEE Transactions on Energy Conversion*, 17(4):514–522, Dec 2002.

[39] D. Maurath, M. Ortmanns, and Y. Manoli. High efficiency, low-voltage and self-adjusting charge pump with enhanced impedance matching. In *2008 51st Midwest Symposium on Circuits and Systems*, pages 189–192, Aug 2008.

[40] S. Messalti, A. G. Harrag, and A. E. Loukriz. A new neural networks mppt controller for pv systems. In *IREC2015 The Sixth International Renewable Energy Congress*, pages 1–6, March 2015.

[41] P. Mohseni, K. Nagarajan, B. Ziaie, K. Najafi, and S. B. Crary. An ultralight biotelemetry backpack for recording emg signals in moths. *IEEE Transactions on Biomedical Engineering*, 48(6):734–737, June 2001.

[42] P. Mohseni, K. Najafi, S. J. Eliades, and Xiaoqin Wang. Wireless multichannel biopotential recording using an integrated fm telemetry circuit. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 13(3):263–271, Sept 2005.

[43] Y. Moriwaki, T. Imura, and Y. Hori. Basic study on reduction of reflected power using dc/dc converters in wireless power transfer system via magnetic resonant coupling. In *2011 IEEE 33rd International Telecommunications Energy Conference (INTELEC)*, pages 1–5, Oct 2011.

[44] T. Morrison, M. Nagaraju, B. Winslow, A. Bernard, and B. P. Otis. A 0.5 cm^3 four-channel 1.1 mw wireless biosignal interface with 20 m range. *IEEE Transactions on Biomedical Circuits and Systems*, 8(1):138–147, Feb 2014.

[45] A. F. Murtaza, H. A. Sher, M. Chiaberge, D. Boero, M. De Giuseppe, and K. E. Addoweesh. Comparative analysis of maximum power point tracking techniques for pv applications. In *INMIC*, pages 83–88, Dec 2013.

[46] T. Paing, J. Shin, R. Zane, and Z. Popovic. Resistor emulation approach to low-power rf energy harvesting. *IEEE Transactions on Power Electronics*, 23(3):1494–1501, May 2008.

[47] Y. K. Ramadass. *Energy processing circuits for low-power applications*. PhD dissertation, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, June 2009.

[48] Y. K. Ramadass and A. P. Chandrakasan. A batteryless thermoelectric energy-harvesting interface circuit with 35mv startup voltage. In *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, pages 486–487, Feb 2010.

[49] N. M. Roscoe and M. D. Judd. Optimization of voltage doublers for energy harvesting applications. *IEEE Sensors Journal*, 13(12):4904–4911, Dec 2013.

[50] A. Safari and S. Mekhilef. Simulation and hardware implementation of incremental conductance mppt with direct control method using cuk converter. *IEEE Transactions on Industrial Electronics*, 58(4):1154–1161, April 2011.

[51] S. Saggini and P. Mattavelli. Power management in multi-source multi-load energy harvesting systems. In *2009 13th European Conference on Power Electronics and Applications*, pages 1–10, Sept 2009.

[52] Seiko Instruments Inc. *Micro Battery Product Catalogue*, 2016.

[53] C. Shi, B. Miller, K. Mayaram, and T. Fiez. A multiple-input boost converter for low-power energy harvesting. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 58(12):827–831, Dec 2011.

[54] F. Simjee and P. H. Chou. Everlast: Long-life, supercapacitor-operated wireless sensor node. In *ISLPED'06 Proceedings of the 2006 International Symposium on Low Power Electronics and Design*, pages 197–202, Oct 2006.

[55] W. M. Tsang, A. Stone, Z. Aldworth, D. Otten, A. I. Akinwande, T. Daniel, J. G. Hildebrand, R. B. Levine, and J. Voldman. Remote control of a cyborg moth using carbon nanotube-enhanced flexible neuroprosthetic probe. In *2010 IEEE 23rd International Conference on Micro Electro Mechanical Systems (MEMS)*, pages 39–42, Jan 2010.

[56] D. J. Yeager, J. Holleman, R. Prasad, J. R. Smith, and B. P. Otis. Neuralwisp: A wirelessly powered neural interface with 1-m range. *IEEE Transactions on Biomedical Circuits and Systems*, 3(6):379–387, Dec 2009.