Dielectric Reliability in GaN Metal-Insulator-Semiconductor High Electron Mobility Transistors

by

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Abstract

GaN Metal Insulator Semiconductor High Electron Mobility Transistors (GaN MIS-HEMTs) show excellent promise as high voltage power transistors that can operate efficiently at high temperatures and frequencies. However, current GaN technology faces several obstacles, one of which is Time-Dependent Dielectric Breakdown (TDDB) of the gate dielectric. Under prolonged electrical stress, the gate dielectric suffers a catastrophic breakdown that renders the transistor useless.

Understanding the physics behind gate dielectric breakdown and accurately estimating the average time to failure of the dielectric are of critical importance. TDDB is conventionally studied under DC conditions. However, as actual device operation in power circuits involves rapid switching between on and off states, it is important to determine if estimations done from DC stress results are accurate. Due to the rich dynamics of the GaN MIS-HEMT system such as electron trapping and carrier accumulation at the dielectric/AlGaN interface, unaccounted physics might be introduced under AC stress that may cause error in DC estimation. To this end, we characterize TDDB behavior of GaN MIS-HEMTs at both DC stress conditions and more accurate AC stress conditions. We find that TDDB behavior is improved for AC stress compared to DC stress conditions at high stress frequencies. At 100 kHz, the average dielectric breakdown time is twice the average dielectric breakdown time under DC stress conditions.

Furthermore, the impact of tensile mechanical stress on TDDB under DC stress is investigated. This is an important concern because of the piezoelectric nature of GaN and the substantial lattice mismatch between Si, GaN and AlGaN that results in high mechanical strain in the active portion of the device. If mechanical stress significantly impacts TDDB, designers will have to work with further constraints to ensure minimal stress across the dielectric. To address this, we have carried out measurements of TDDB under $\varepsilon = 0.29\%$ tensile strain. We find that TDDB in both the On-state and Off-state stress conditions are unaffected by this mechanical stress.

Through measurements done in this thesis, we gather further insight towards understanding the physics behind TDDB. Through AC stress we find that the dynamics of the GaN MIS-HEMTs prolong dielectric breakdown times. Through mechanical stress we find that modulation of the 2-Dimensional Electron Gas and dielectric bond straining have minimal impact on TDDB.

Thesis supervisor: Jesús A. del Alamo
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Contents

Chapter 1 Introduction........13

1.1 Benefits of GaN Based MOSFETs........13

1.2 GaN Metal Insulator Semiconductor High Electron Mobility Transistor........15

1.3 Thesis Goal........17

1.4 Thesis Layout........18

Chapter 2 Physics of Time-Dependent Dielectric Breakdown........19

2.1 Introduction........19

2.2 The Percolation Model........19

2.3 Weibull Distribution........20

2.4 TDDB Stress Conditions........21

2.5 E-model and 1/E-model........23

2.6 Summary........27

Chapter 3 Device Characteristics and Experimental Methodology 29

3.1 Introduction........29

3.2 Device under Study........29

3.3 Device Characteristics........30

3.4 Measurement Equipment........34

3.4.1 AC TDDB Setup........34

3.4.2 Mechanical Stress TDDB Setup........35

3.4.3 Substrate Thinning for Mechanical Stress Characterization........36

3.5 Summary........39

Chapter 4 TDDB under AC stress........41

4.1 Introduction........41

4.2 AC TDDB vs DC TDDB for Si........42

4.3 Low Frequency AC TDDB........43

4.4 High Frequency AC TDDB........46

4.5 Acceleration Factor Versus Stress Frequency........50

4.6 Summary........52

Chapter 5 DC TDDB under Mechanical Stress........53

5.1 Introduction........53

5.2 Transfer and Output Characteristics Change........53

5.3 On-state TDDB under mechanical stress *57*
5.4 Off-state TDDB under mechanical stress *62*
5.5 Summary *67*
Chapter 6 Conclusions and Suggestions for Future Work **69**
6.1 Conclusions *69*
6.2 Suggestions for Future Work *70*

List of Figures

Figure 1-1 Comparison of material properties between Si and GaN. 13
Figure 1-2 Theoretical on-resistance at a given breakdown voltage for Si, GaN, and SiC. Reprinted with permission from [4]. 14
Figure 1-3 Left) GaN tetrahedral under no stress. Polarization for a complete tetrahedral is balanced to zero. Right) AlN/GaN tetrahedral under stress. Polarization is no longer balanced, resulting in a piezoelectric polarization. Reprinted with permission from [5]. 15
Figure 1-4 Band diagram of GaN HEMT. Unbalanced piezoelectric polarization is balanced by electrons that gather at the AlGaN/GaN interface. Reprinted with permission from [5]. 16
Figure 2-1 Percolation model adapted from [10]. Hard breakdown occurs when an overlapping path of defects is formed. 19
Figure 2-2 Hard breakdown time statistics from 4 different stress voltages. Reprinted with permission from [12].. 20
Figure 2-3 Extrapolation of the 4 T63 values from figure 2-2 to lower electric fields. Adapted from [12]. 21
Figure 2-4 Left) schematic of stress conditions and electric field distribution under On-state TDDB. Right) schematic under Off-state TDDB. 22
Figure 2-5 Typical gate current evolution during On-state TDDB... 23
Figure 2-6 Local bond structure within SiO2 dielectric. Amorphous nature of the dielectric prevents constant bond angle of 109º impossible from [13]... 24
Figure 2-7 Oxygen vacancy leading to a weak Si-Si bond. From [13].. 24
Figure 2-8 a) Local SiO2 structure with oxygen vacancy under a local electric field. b) Same structure after defect formation. There is a hole trap associated with the Si atom labeled 2 and an electron trap with Si labeled 1. From [13]. 25
Figure 2-9 Schematic of the anode hole injection model. Electrons tunnel to the anode, generating a hot hole while thermalizing. This hole tunnels back to the cathode, generating electron traps in the process. 26
Figure 3-1 Simplified cross section of the devices under study. Type A: no field plate, thick gate dielectric to test behavior of gate dielectric under integrated field plate, B: no field plate, thin gate dielectric, C: integrated field plate, thin gate dielectric. This is the standard gate dielectric of the

full device, and D: all field plates and thinnest dielectric. This is the standard device design for a lower voltage device. 30
Figure 3-2 Transfer and output characteristics of a typical Type A device. 32
Figure 3-3 Transfer and output characteristics of a typical Type B device. 32
Figure 3-4 Transfer and output characteristics of a typical Type C device. 33
Figure 3-5 Transfer and output characteristics of a typical Type D device. 33
Figure 3-6 Diagram of stress setup and gate current measurement during AC stress using the MPSMU. 34
Figure 3-7 Summarized table of voltage stress values applied to each device type in the study of the impact of mechanical stress on TDDB. 36
Figure 3-8 Cross section after the chip is mounted upside down on a 6-inch wafer. The trench prevents any resist to remain after processing. 36
Figure 3-9 Left: 254 um thick chip. Right: 40 um thick chip after substrate etching. 37
Figure 3-10 Approximation of strain from radius of curvature [24]. 38
Figure 3-11 Probe contact for 40 um process thinned chips. 39
Figure 4-1 Oscilloscope trace of actual waveforms used in AC TDDB for 1 Hz and 10 kHz. The sharp transition allows for accurate estimation of stress time. 41
Figure 4-2 Weibull failure distribution comparison between DC stress and 1 Hz 50% duty cycle AC stress. V_{GS} = 8.5 V for DC, 8.5V/-8.5V for AC, V_{DS} = 0V. Body is left floating. Data comes from one die. 43
Figure 4-3 Weibull failure distribution comparison between DC stress and 1 Hz 50% duty cycle AC stress. V_{GS} = 8.5 V for DC, 8.5V/-8.5V for AC, V_{DS} = 0V. Body is left floating. Data comes from three dies. 45
Figure 4-4 Weibull failure distribution comparison between 1 Hz 50% duty cycle AC stress between three dies. V_{GS} = 8.5V/-8.5V for AC, V_{DS} = 0V. Body is left floating. Each dataset comes from one die. 45
Figure 4-5 Gate leakage current versus time for DC stress and 50 % DC AC 1 Hz bipolar AC stress. V_{GS} = 8.5 V for DC, 8.5V/-8.5V for AC, V_{DS} = 0V. Body is left floating. Data comes from three dies. 46

Figure 4-6 Weibull failure distribution comparison between DC stress and 100 kHz 45% duty cycle AC stress. V_{GS} = 8.5 V for DC, 8.5V/0 V for AC, V_{DS} = 0V. Body is left floating. Data comes from six dies. 46
Figure 4-7 Weibull failure distribution comparison between DC stress and 100 kHz 45% duty cycle AC stress. V_{GS} = 8.5 V for DC, 8.5V/-8.5V for AC, V_{DS} = 0V. Body is left floating. Data comes from three dies. 47
Figure 4-8 Weibull failure distribution comparison between DC stress and 1 kHz 45% duty cycle AC stress. V_{GS} = 8.5 V for DC, 8.5V/0V (top) or 8.5V/-8.5V (bottom) for AC unipolar and bipolar respectively, V_{DS} = 0V. Body is left floating. Data comes from three dies. 48
Figure 4-9 Weibull failure distribution comparison between DC stress and 10 kHz 45% duty cycle AC stress. V_{GS} = 8.5 V for DC, 8.5V/0V (top) or 8.5V/-8.5V (bottom) for AC unipolar and bipolar respectively, V_{DS} = 0V. Body is left floating. Data comes from three dies. 49
Figure 4-10 Acceleration parameter versus stress frequency for unipolar and bipolar AC TDDB. Duty cycle is fixed at 45%. 50
Figure 4-11 Gate to channel capacitance C_{GG} evolution over stress time at various measurement frequencies. The drop in capacitance at a given stress time with increasing frequency correspond to less electron accumulation in the conduction band edge of the AlGaN/dielectric interface [10]. 51
Figure 4-12 Band diagram of GaN MIS-HEMT with positive gate bias. At the beginning of a pulse, electrons have not responded to the changing stress. Voltage is dropped across both the dielectric and the AlGaN (left). Given enough time, a steady state will be reached where there is electron accumulation in the AlGaN conduction band (right). 52
Figure 5-1 Transfer and Output curves of Type A device under 0.29% tensile strain (red) versus no strain (blue). Measurement conditions are same as Figure 3-2. 55
Figure 5-2 Transfer and Output curves of Type B device under 0.29% tensile strain (red) versus no strain (blue). Measurement conditions are same as Figure 3-3. 55
Figure 5-3 Transfer and Output curves of Type C device under 0.29% tensile strain (red) versus no strain (blue). Measurement conditions are same as Figure 3-4. 56
Figure 5-4 Summary of transfer characteristics with mechanical stress from flat → tensile. Type A is an average of 15 devices each, Types B and C are averages of 4 devices each. 57

Figure 5-5 Gate current versus time for flat Type A devices under On-state conditions. V_{GS} = 128 V, V_{DS} = 0 V, V_{BS} = 0 V. Devices come from multiple dies. 57

Figure 5-6 Gate current versus time for 0.29% tensile strain Type A devices under On-state conditions. V_{GS} = 128 V, V_{DS} = 0 V, V_{BS} = 0 V. Devices come from multiple dies.................... 58

Figure 5-7 Gate current versus time for On-state stress conditions on unbent chip. V_{GS} = 128 V, V_{DS} = 0 V, V_{BS} = 0 V. Devices come from a single die. 59

Figure 5-8 Gate current versus time for 0.29% tensile strain Type A devices (red) under On-state conditions versus unbent devices (blue). V_{GS} = 128 V, V_{DS} = 0 V, V_{BS} = 0 V. Devices come from multiple dies... 59

Figure 5-9 Type A device TDDB failure plot. V_{GS} = 128 V, V_{DS} = 0 V, V_{BS} = 0 V. 61

Figure 5-10 Type C device TDDB failure plot. V_{GS} = 24 V, V_{DS} = 0 V, V_{BS} = 0 V.................... 61

Figure 5-11 Unbent Type A device TDDB failure plot. V_{DG} = 325 V and V_{BS} = 0 V. Black is under dark, blue is under 3.5 eV UV illumination. Devices are interspersed between multiple dies..... 62

Figure 5-12 Gate current versus time for flat Type A devices under dark (black) and UV illumination (blue). V_{DG} = 325 V and V_{BS} = 0 V. 63

Figure 5-13 Gate current versus time for flat and tensile Type A devices. V_{DG} = 325 V, V_{BS} = 0 V. 63

Figure 5-14 Type A device TDDB failure plot for flat versus 0.29% tensile strain under dark. V_{DG} = 325 V, V_{BS} = 0 V. Devices come from multiple dies. 64

Figure 5-15 Type A device TDDB failure plot for flat versus 0.29% tensile strain under 3.5 eV UV illumination. V_{DG} = 325 V and V_{BS} = 0 V. Devices come from multiple dies. 65

Figure 5-16 Gate leakage current for Type A devices in Figure 5-15. Devices come from multiple dies. 65

Figure 5-17 Amplitude of weights associated with each exponential for Off-state. Top, unbent Type A device. Bottom, tensile Type A device. 66

Chapter 1 Introduction

Silicon (Si) based metal-oxide-semiconductor field effect transistors (MOSFETs) are the long running standard devices used for electrical power control. Such devices power a diverse area of commercial and consumer use ranging from the automobile and space industry to personal computers and home power converters. Thanks to the large investment and industry built around it, silicon technology enjoys lower costs and thoroughly researched technology.

However, while the world demand for electrical power continues to grow, the rate of improvement of Si based devices has stalled as they asymptotically approach theoretical limits. Gallium nitride (GaN) based MOSFETs offer the next step to enhance the performance and efficiency of electrical power management systems in the future.

1.1 Benefits of GaN Based MOSFETs

First GaN based devices appeared in 2004 as depletion-mode high electron mobility transistors (HEMTs) [1]. Fabricated by Eudyna Corporation in Japan, Eudyna designed these GaN HEMTs to be used at radio frequencies (RF) while taking advantage of a phenomenon discussed in 1975 by T. Mimura *et al* [2] and in 1994 by M. A. Khan *et al.* [3] where a two-dimensional electron gas (2DEG) at the interface between aluminum gallium nitride (AlGaN) and GaN would lead to a substantially higher mobility than in bulk AlGaN or GaN.

So why is GaN considered so promising as the next step in material of choice for power management? GaN has distinct advantages over Si in three areas: 1. Band gap (E_g), 2. Critical Field (E_{crit}), 3. On-Resistance (R_{ON}).

Parameter	Units	Si	GaN
Band Gap (E_g)	eV	1.12	3.39
Electron Mobility (μ_n)	$cm^2/V\ s$	1400	1000
Critical Field (E_{crit})	MV/cm	0.23	3.3
Thermal Conductivity (λ)	W/cm K	1.5	1.3

Figure 1-1 Comparison of material properties between Si and GaN.

The band gap of GaN at 3.4 eV is significantly higher than Si at 1.1 eV. The larger bandgap for GaN implies that carrier generation is more difficult. Two implications from this is that intrinsic leakage current is lower and that the device can operate at higher temperatures necessary for space or automotive applications.

Another consequence of the large bandgap of GaN is that its critical field at 3.3 MV/cm is much larger than in Si at 0.23 MV/cm and as a result, GaN can withstand a substantially larger electric field and voltage before breakdown from impact ionization. Therefore, for a particular voltage across the drain and the source, GaN FETs can have much smaller device dimensions leading to spatial and performance efficiency.

The on-resistance is almost directly proportional to the length of the drift region that is designed in a power transistor to support the high electric field. This means that with GaN having a higher critical field and therefore a smaller required length at a given voltage constraint, GaN has a substantially smaller on-resistance compared to Si. This leads to increased performance efficiency. Plotting the ON resistance versus breakdown voltage in Figure 1-2, we see that at the theoretical limit GaN outperforms Si by more than 3 orders of magnitude and SiC by an order of magnitude at a given breakdown voltage.

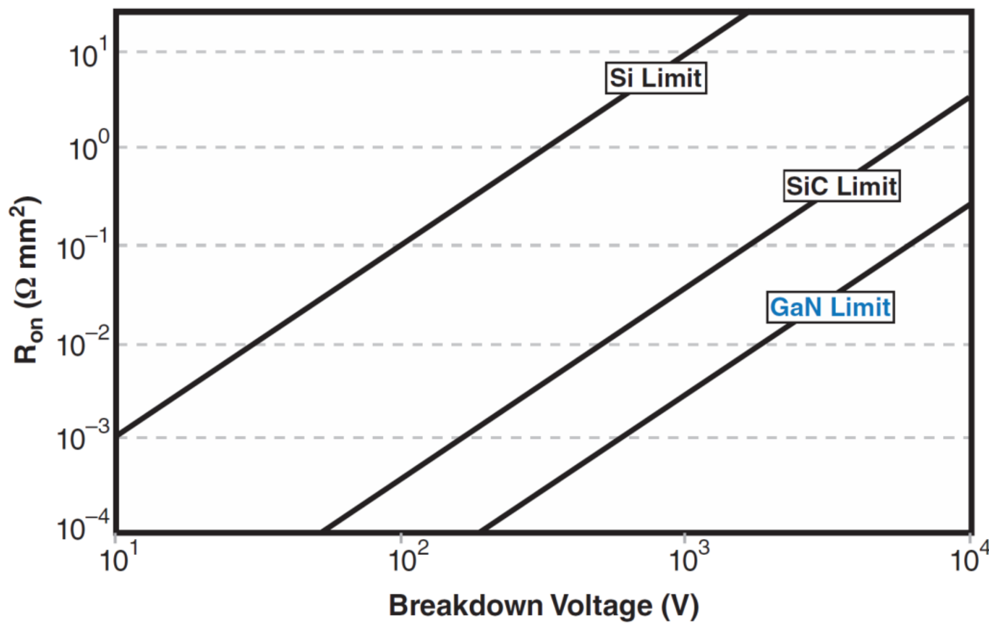


Figure 1-2 Theoretical on-resistance at a given breakdown voltage for Si, GaN, and SiC. Reprinted with permission from [4].

1.2 GaN Metal Insulator Semiconductor High Electron Mobility Transistor

In addition to the above-mentioned benefits, the piezoelectric nature of GaN allows for a high electron concentration at the AlGaN/GaN interface. This can support a large current drive. In addition, the electron mobility of the 2DEG is enhanced from about 1000 $cm^2/V \cdot s$ to 1500~1600 $cm^2/V \cdot s$. This allows GaN transistors to have comparable mobility to Si. To understand this phenomenon, we first look at the crystalline structure of GaN and AlGaN tetrahedral.

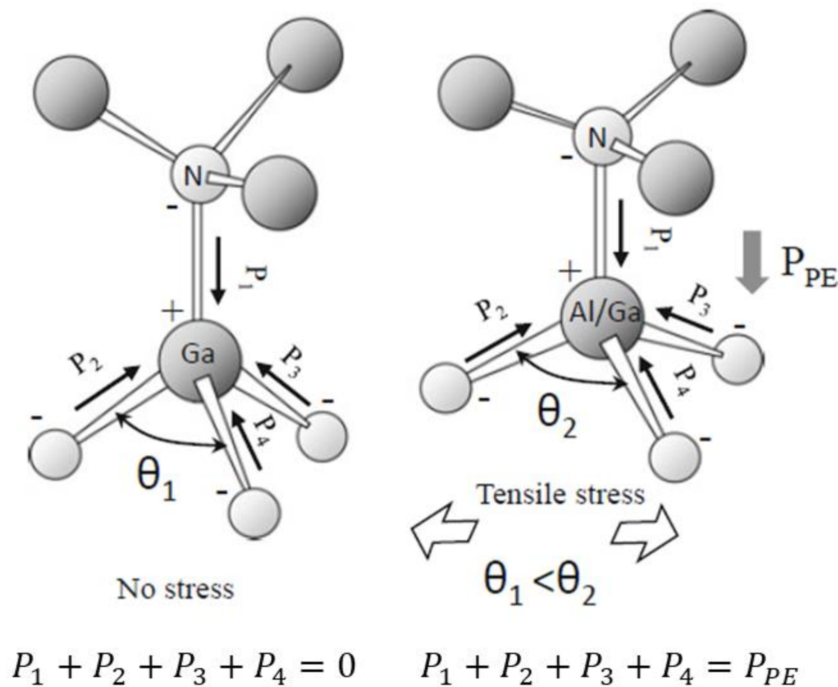


Figure 1-3 Left) GaN tetrahedral under no stress. Polarization for a complete tetrahedral is balanced to zero. Right) AlN/GaN tetrahedral under stress. Polarization is no longer balanced, resulting in a piezoelectric polarization. Reprinted with permission from [5].

As Figure 1-3 shows, Ga-N and Al-N ionic bonds are polarized as the nitrogen atom has a greater affinity for the electron. In a relaxed GaN crystal, the tetrahedral structure balances out the polarized bond resulting in net zero polarization within the bulk of the crystal. However, the asymmetry at the cut face of the crystal results in spontaneous polarization, P_{SP}, due to hanging bonds. When AlGaN and GaN layers are grown in a heterostructure, their lattice mismatch causes

the smaller AlGaN lattice to be stretched or become under tensile strain. Then, as Figure 1-3 shows, the interface develops a piezoelectric polarization as bonds are no longer symmetrically oriented.

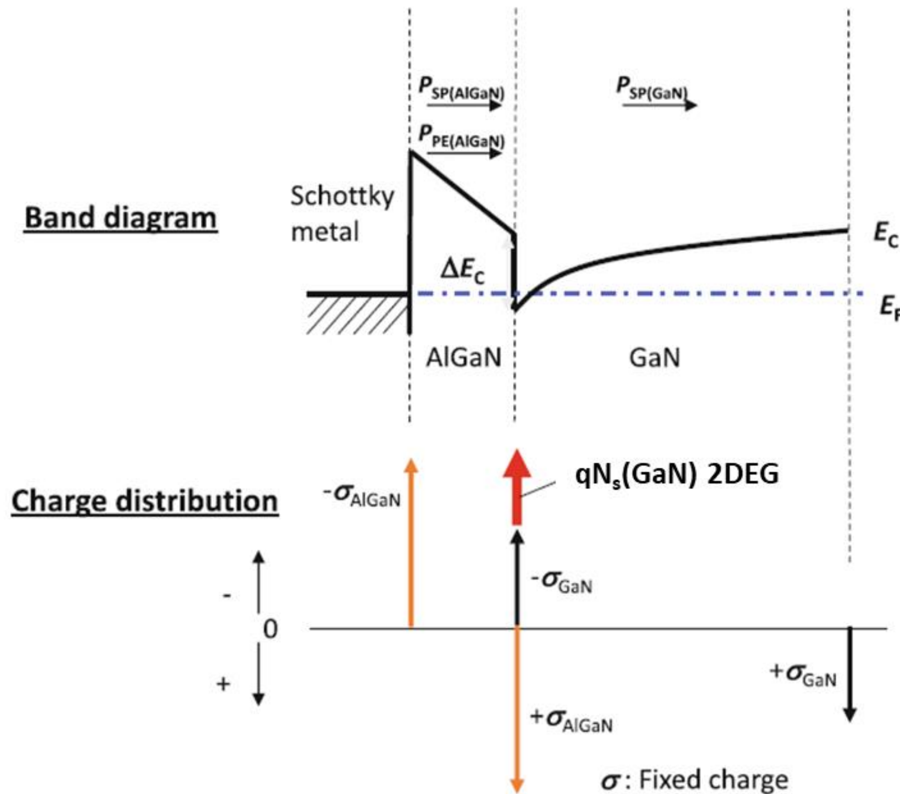


Figure 1-4 Band diagram of GaN HEMT. Unbalanced piezoelectric polarization is balanced by electrons that gather at the AlGaN/GaN interface. Reprinted with permission from [5].

The combination of the spontaneous polarization and piezoelectric polarization, labeled P_{PE}, leads to an uncompensated positive charge at the AlGaN/GaN interface. Electrons gather at this interface to screen the positive charge (Figure 1-4). This is the source of the 2DEG. As there are little to no dopants that act as scattering centers at the interface, high electron mobility is achieved at the 2DEG. GaN transistors with such a layout is referred to as High Electron Mobility Transistors (HEMTs).

While the large bandgap of AlGaN is sometimes enough to act as a barrier to prevent conduction between the 2DEG and the Schottky metal, for better control of gate leakage current in a power transistor, a dielectric is grown atop the AlGaN. With the addition of the dielectric the transistor is finally referred to as the GaN Metal Insulator Semiconductor High Electron Mobility Transistor (GaN MIS-HEMT).

However, adding a gate dielectric introduces a number of reliability concerns [6]. Of key interest for commercial applications is the phenomenon known as time dependent dielectric breakdown (TDDB). In essence, under prolonged electrical stress, the dielectric suffers a catastrophic breakdown that renders the transistor useless. Details of the physics behind TDDB will be discussed in chapter 2.

As devices are designed to survive for a long period of time, estimating the dielectric time to failure within a reasonable timeframe first requires applying extreme stress conditions to break the dielectric. Then, the time to failure is extrapolated to estimate device reliability at operating conditions.

The extreme stress conditions are set to mimic device operating conditions albeit at an elevated temperature or a large voltage. However, in most studies the voltage is held constant even though actual operation involves switching constantly, often at a very high frequency. This is in part due to easier instrumentation setup as well as less ambiguity in the physics involved.

1.3 Thesis Goal

Contributing towards an understanding of TDDB in GaN MIS-HEMTs is the goal of this thesis. First, the accuracy of TDDB measurements under DC conditions is investigated. These measurements are compared with results from AC stress conditions which better represent the operational conditions of the transistors. As many dynamic behaviors exist in the GaN system like electron trapping [7] and dielectric/AlGaN electron occupation [8], TDDB measurements under DC conditions may not be enough to successfully capture reliability behavior. In addition, TDDB measurements under DC conditions but with changing mechanical stress are also investigated. Due to the piezoelectric nature of GaN, mechanical stress and strain is inherently critical to the design of GaN MIS-HEMTs. Modifying the design of a transistor even slightly can cause large mechanical stress changes. If TDDB behavior is to change with changing mechanical stress, DC measurements will be severely limited in scope as even slightly modifying the transistor design would require a completely new set of measurements.

By investigating the changes in TDDB behavior with these varying stress conditions, the relevant variables that are responsible for TDDB in GaN MIS-HEMTs will be extracted. To quantitatively

see these changes, dielectric failure distribution plots as well as gate leakage current with stress accumulation will be looked in detail.

1.4 Thesis Layout

In chapter 2, a detailed description of time dependent dielectric breakdown is given. Typical behavior as well as leading models explaining dielectric degradation is discussed.

In chapter 3, experimental setup including instruments used, values of electrical and mechanical stress conditions, and processing steps used to induce the mechanical stress are given.

In chapter 4, results from comparing TDDB under DC and AC stress conditions are presented.

In chapter 5, results from comparing TDDB under DC conditions with changing mechanical stress are presented.

Finally, in chapter 6, the conclusions of this thesis are provided, as well as suggestions for further work.

Chapter 2 Physics of Time-Dependent Dielectric Breakdown

2.1 Introduction

In this chapter we discuss the basic physics of time-dependent dielectric breakdown (TDDB). Hard breakdown through the percolation model of defects is described. Typical plots relevant to TDDB are shown. Finally, the nature of defects is discussed under the thermochemical E-model and the anode hole injection 1/E-model.

2.2 The Percolation Model

There is wide acceptance in literature that dielectric breakdown follows the percolation model [9]. According to this model, under electrical stress defects are generated at random inside the insulator. Once enough defects are generated to create a conducting path through the insulator, ohmic conduction through the path causes catastrophic breakdown inside the dielectric, also called *hard breakdown*.

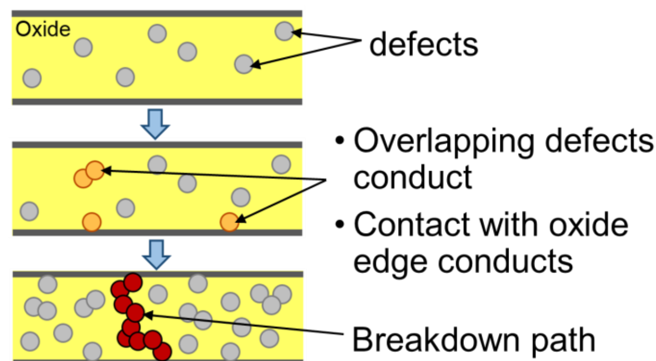


Figure 2-1 Percolation model adapted from [10]. Hard breakdown occurs when an overlapping path of defects is formed.

The percolation model depends on an aging process in which defects are generated at random at a certain rate over time. The statistical distribution that is very well suited for describing this effect is the Weibull distribution. Indeed, TDDB studies on a wide array of substrates and dielectrics

have shown that *hard breakdown time* (T_{HBD}), or the stress time until hard breakdown, follows the Weibull distribution.

2.3 Weibull Distribution

In essence, the Weibull statistical distribution is described by $\ln(-\ln(1-F)) = \beta\ln(t) - \ln(\alpha)$ where F is cumulative frequency, t time, and β and α are two parameters [11] that describe the tightness and shape of the statistical distribution. A typical Weibull distribution is shown in Figure 2-2.

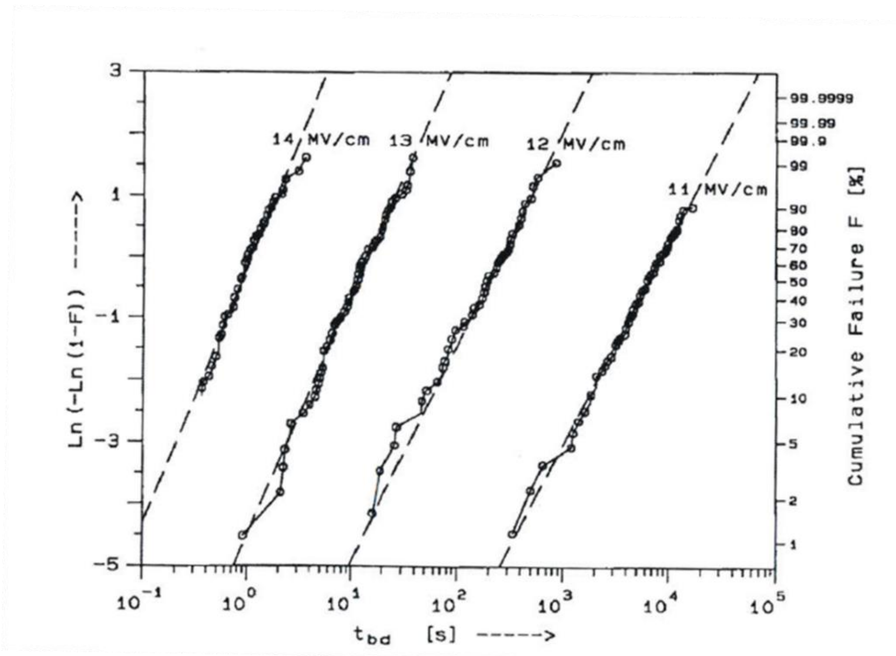


Figure 2-2 Hard breakdown time statistics from 4 different stress voltages. Reprinted with permission from [12].

As evidenced by Figure 2-2, increasing the stress voltage leads to a leftward shift of the Weibull fit. This corresponds to a drop in the hard breakdown times of the devices under test for that voltage. This is critical as time constraints encourage using extreme stress conditions to accelerate hard breakdown. A near constant shift of the Weibull fit with fixed step increase of the stress voltage allows for estimating the device lifetime at typical operating voltages. In fact, taking the x intercept (where the y axis = 0 or the cumulative frequency is 63%), T_{63}, of each stress conditions and extrapolating allows us to determine stress conditions needed to allow for the dielectric to survive a target duration.

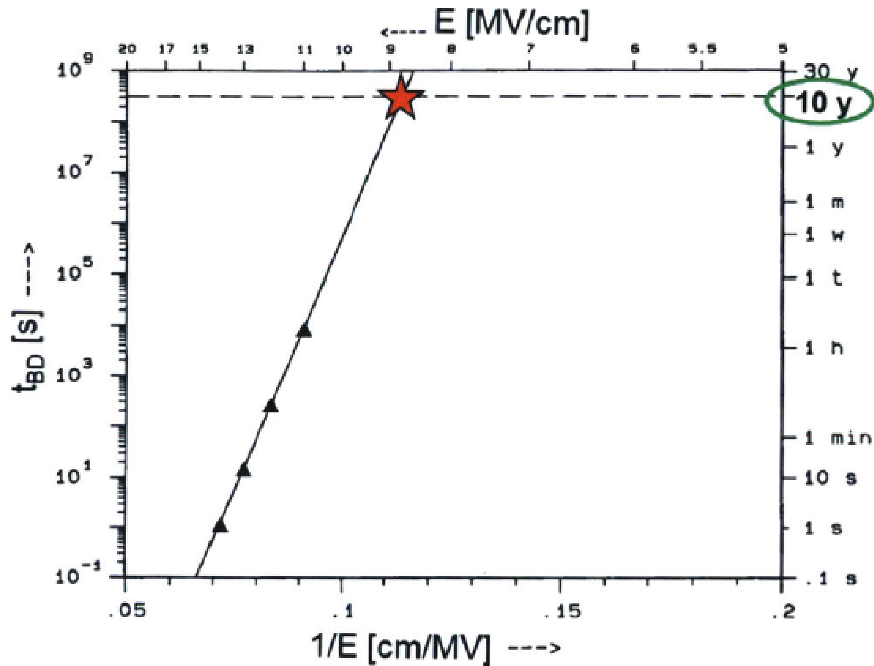


Figure 2-3 Extrapolation of the 4 T63 values from figure 2-2 to lower electric fields. Adapted from [12].

In Figure 2-3, the four T_{63} values from Figure 2-2 are extrapolated to lower stress conditions. In this manner, we can then predict that an electric field magnitude of approximately 9 MV/cm or lower should be used to ensure that the dielectric can survive for 10 years on average.

2.4 TDDB Stress Conditions

As evidenced by Figure 2-3, applying larger electrical stress than typical operational ranges is critical to ensure data collection within a reasonable timeframe. However, this electrical stress still should be applied to mimic actual operational conditions as much as possible. To this end, two different stress configurations are used to extract TDDB data: On-state and Off-state.

In On-state TDDB, also called forward bias TDDB, the stress conditions are set to mimic conditions when the transistor is turned on. Therefore, there is a positive voltage on the gate. While in actual operation there is a drain source bias to drive current, for simplicity, both drain and the source is held at zero volts during On-state TDDB.

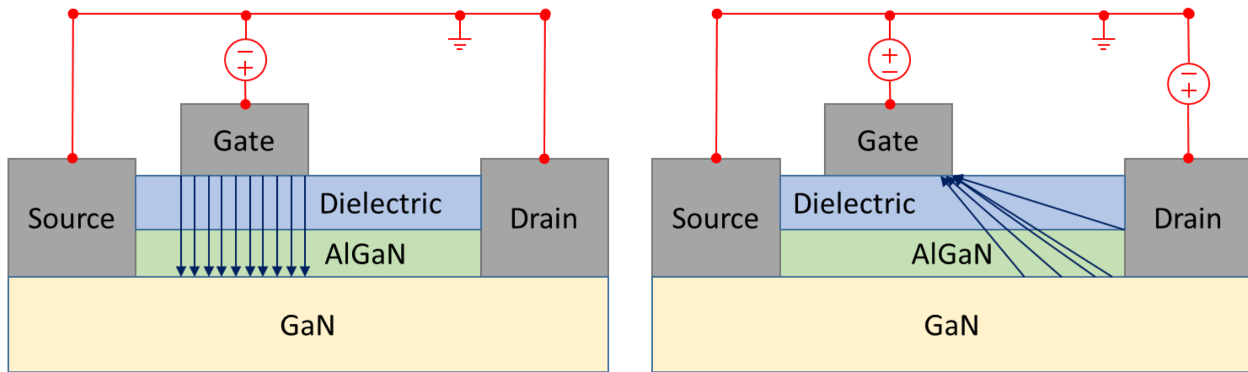


Figure 2-4 Left) schematic of stress conditions and electric field distribution under On-state TDDB. Right) schematic under Off-state TDDB.

As shown in left of Figure 2-4, holding the source and drain at zero volts allows for the electric field distribution to be more uniform across the dielectric. This results in a simpler picture of the physics involved as the electric field can be more easily calculated.

In Off-state TDDB, also called reverse bias TDDB, stress conditions are set to mimic device conditions when the transistor is turned off and is blocking a large voltage. The gate is held at a negative voltage below threshold, and there is a large voltage between drain and the source. This leads to an electric field peak under the gate towards its drain edge shown by the diagram on the right in Figure 2-4 as the channel is now depleted.

For power devices such as our high voltage MIS-HEMTs, Off-state TDDB conditions is of more interest. The devices must be able to block large voltage reliably while turned off and therefore accurate modelling of blocking capability is critical to commercial deployment.

Figure 2-5 shows the typical gate leakage current under On-state TDDB measurement conditions. Due to the large number of curves, there is some gate leakage current deviation between devices through stress indicating device to device variation. At the beginning of stress, there is a slight decrease in gate leakage current. This is thought to be a result of electrons being trapped between the channel and the gate, leading to reduced tunneling or thermionic emission current [6]. During stress, gate leakage current increases steadily. This is attributed to stress-induced leakage current (SILC) where defect formation increases the tunneling current [6]. Finally, the leakage currents jump sharply in the end, indicating catastrophic or hard breakdown.

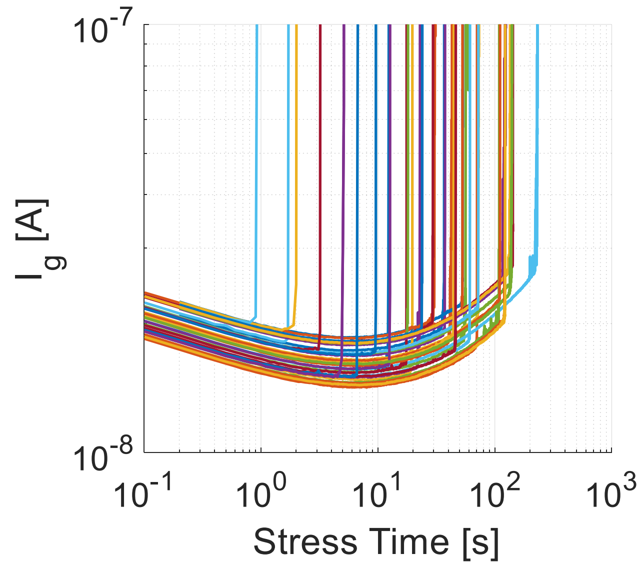


Figure 2-5 Typical gate current evolution during On-state TDDB.

The nature of defects that lead to hard breakdown is still under discussion. A complete understanding of the physics behind TDDB requires defect formation and conduction through defects to be understood. In the next section, simplified summaries of two leading models explaining defect formation are presented.

2.5 E-model and 1/E-model

The E-model predicts that the time to failure TF is described by the relation

$$\ln(TF) \propto \frac{\Delta H_o}{k_B T} - \gamma * E \tag{2.1}$$

Where ΔH_o is activation energy, E is electric field across dielectric, γ is the field acceleration parameter, k_B is the Boltzmann constant, and T is the temperature.

While the model started out empirically to fit the various lifetime extrapolations, it has since been described by the, so called, thermochemical model.

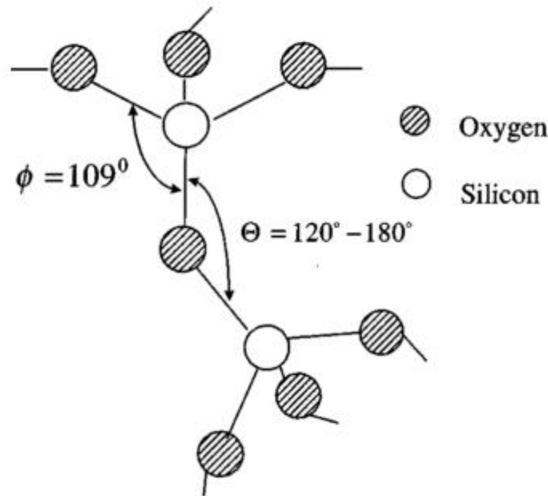


Figure 2-6 Local bond structure within SiO2 dielectric. Amorphous nature of the dielectric prevents constant bond angle of 109º impossible from [13].

The thermochemical model was formulated to investigate TDDB in SiO_2 dielectric [13]. Crystalline SiO_2 is tetrahedral with a bonding angle of 109º. As Figure 2-6 shows, the amorphous nature of the oxide makes maintaining a bond angle of 109º impossible for every bond. Instead, this angle can be anywhere between 120º to 180º. Furthermore, bond angles larger than 150º are reported to be rare [14]. Instead, oxygen vacancies result, leading to very weak Si-Si bonding as shown in Figure 2-7. These Si-Si bonds, which can be detected with electron spin resonance techniques, [15] and the weak Si-O bonds with angles greater than 120º are thought to be the culprits behind defect formation.

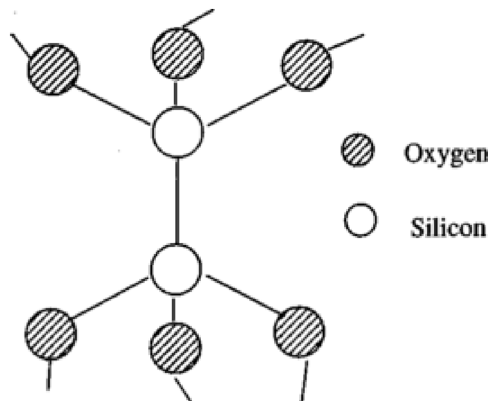


Figure 2-7 Oxygen vacancy leading to a weak Si-Si bond. From [13].

Si-O bonding has a covalent bonding energy of 1.4 eV and ionic bonding energy of 3.8 eV. This results in the Si-O covalent bonding being polar with electrons strongly pulled towards the oxygen atom. Within a perfect tetrahedral, all the Si-O dipoles cancel each other out, leading to net zero dipole moment. However, in amorphous SiO_2 there is no net cancellation, leading to formation of dipole moments.

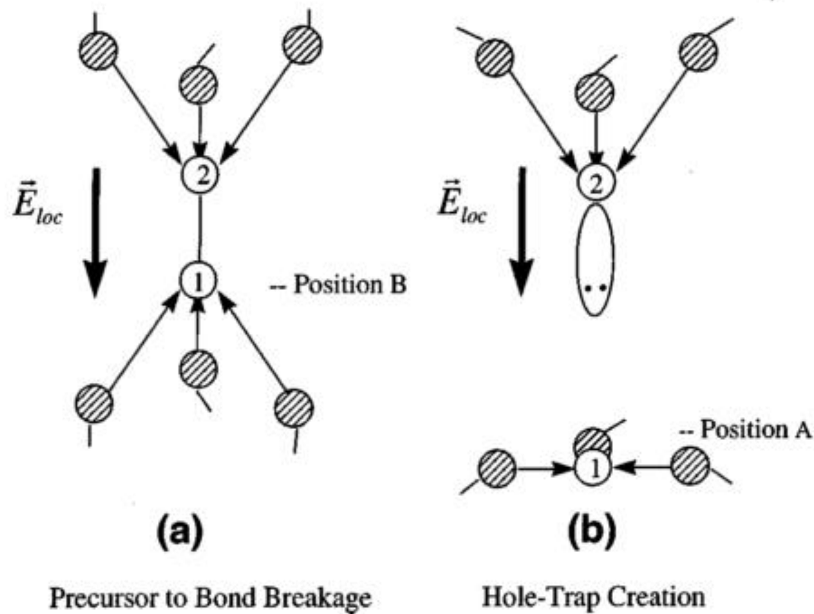


Figure 2-8 a) Local SiO2 structure with oxygen vacancy under a local electric field. b) Same structure after defect formation. There is a hole trap associated with the Si atom labeled 2 and an electron trap with Si labeled 1. From [13].

Figure 2-8a shows the structure from Figure 2-7 under an external electric field (E_{loc}). The sum of the dipole moments in the top pseudo-tetrahedral results in the moment pointing parallel to the applied electric field. On the other hand, the bottom pseudo-tetrahedral has its dipole moment pointed antiparallel. Therefore, under external electrical stress the bottom tetrahedral is energetically favored to collapse into a planar structure as shown in Figure 2-8b. This collapse is thought to happen when the thermal energy distribution provides energy large enough to overcome the activation energy.

In other words, the external electric field acts as a catalyst to break bonds weakened by oxygen vacancies (Si-Si bonding) or large bond angles (Si-O bonding). Ultimately, the defects in the thermochemical E model are broken bonds that also act as hole or electron traps.

The 1/E model instead claims that the lifetime dependence on electric field is instead

$$\ln(TF) \propto \frac{1}{E} \tag{2.2}$$

Where TF is the mean time to failure and E is the applied electrical field across the dielectric.

The inverse dependence of electric field has been proposed by Schuegraf and Hu to be a result of hole injection from the anode during stress [16]. Holes have been found to be able to generate electron traps at both the bulk and interface of SiO_2. Furthermore, hole transport has been measured before hard breakdown, hinting the role of holes in breakdown [17] [18] [19] [20].

In the anode hole injection model (Figure 2-9), some of the electrons tunneling across the dielectric transfer all of their energy to deep valence band electrons at the anode. These electrons can impact ionize and create highly energetic holes. These holes tunnel back through the dielectric towards the cathode. Some of the holes are trapped in the dielectric and generate electron traps [21] which ultimately lead to broken bonds. Due to the generation of electron traps, tunneling current increases further hole generation. This positive feedback ultimately leads the electron trap density to reach a critical value and leads to catastrophic dielectric breakdown. The 1/E dependence in the model then comes from the electron tunneling current needed to generate holes which can be described by Fowler-Nordheim (FN) Tunneling.

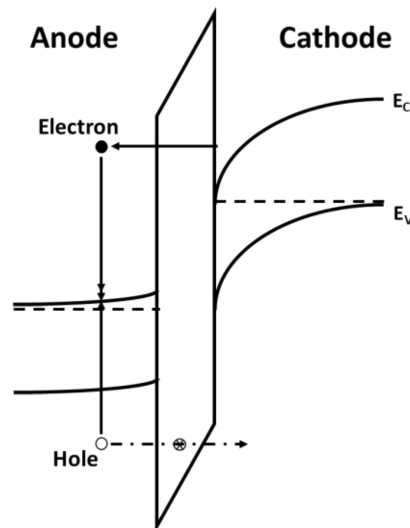


Figure 2-9 Schematic of the anode hole injection model. Electrons tunnel to the anode, generating a hot hole while thermalizing. This hole tunnels back to the cathode, generating electron traps in the process.

The principles behind the thermochemical E-model carry over to our SiN dielectric. The silicon nitride dielectrics used in this study are also amorphous. Therefore, one can expect suboptimal bond angles between the Si-N as well as nitrogen vacancies [22] that lead to Si-Si bonding. Si-N bonding is also slightly polar which translates to the thermochemical E model being relevant. On the other hand, the anode hole injection 1/E-model is less clear on its relevance to the GaN MIS-HEMT system. As the gate material is metal, it is unclear where holes can be generated.

At any rate, in both the E-model and the 1/E-model, the defects enhance SILC, thereby increasing gate leakage current. Once made, the defects act as "stepping stones" for tunneling carriers in a process known as trap assisted tunneling (TAT).

2.6 Summary

An overview of TDDB and the proposed physical models explaining defect formation was provided. In both the thermochemical E-model and the anode hole injection 1/E-model, defects are attributed to broken bonds within the dielectric. While in the thermochemical model, bond breakage is thought to be enhanced by the external electric field and hole trapping is a result of bond breakage, the anode hole injection model considers hole trapping a precursor of defect formation.

In the next chapter, an overview of the experimental setup including measurement equipment, device descriptions, and stress conditions are provided. Processing steps used to induce large strain across the channel are detailed as well.

Chapter 3 Device Characteristics and Experimental Methodology

3.1 Introduction

In this chapter, we discuss the devices under study and details of the experimental methodology. First, electrical transfer and output characteristics of the devices under measurement are presented. For AC TDDB, frequency, duty cycle, and stress bias values are discussed. Finally, electrical stress values as well as methods for introducing mechanical stress are presented.

3.2 Device under Study

Industry provided devices are used for all the measurements. There are a total of 4 different device structures studied. All of the devices are GaN MIS-HEMTs grown on 6-inch (111) Si. The 2DEG is formed by growing AlGaN on top of GaN. SiN dielectric is placed above the AlGaN to form the gate dielectric. The drain is preferentially further from the gate than the source to allow for a large voltage drop between the gate and the drain for high voltage applications. In three of the device structures, there are no field plates to allow for more simplified investigations of Off-state or reverse-biased TDDB. The last device structure, which comes from a different product design, has source field plates but has a much thinner dielectric. This allows for the smaller voltage to be used to accelerate stress which is necessary due to the limited voltage capabilities of the function generator used for AC stress. Simplified cross sections of the device structures are presented in Figure 3-1.

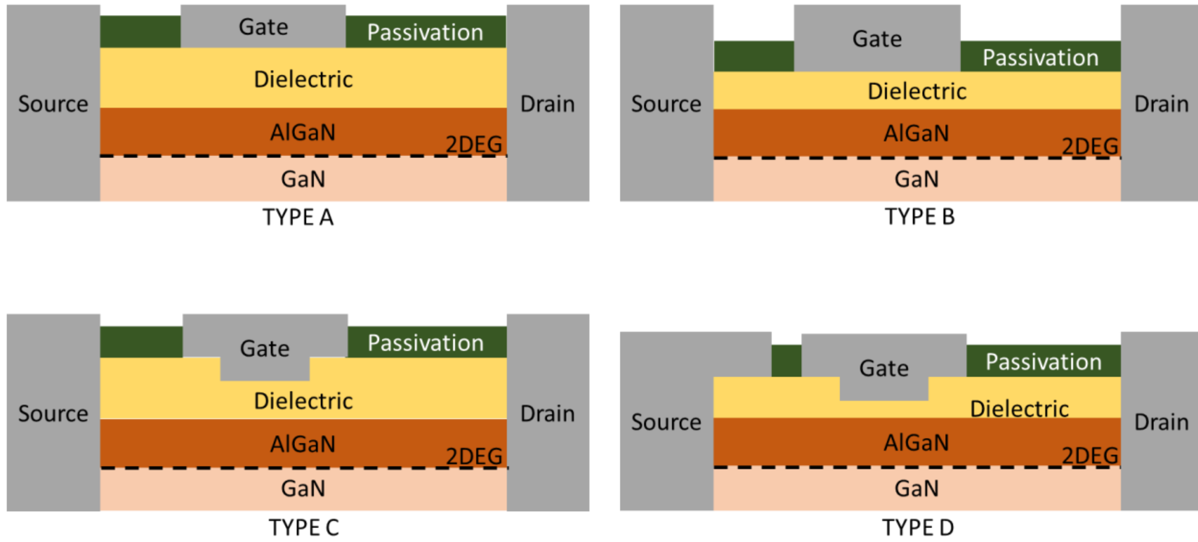


Figure 3-1 Simplified cross section of the devices under study. Type A: no field plate, thick gate dielectric to test behavior of gate dielectric under integrated field plate, B: no field plate, thin gate dielectric, C: integrated field plate, thin gate dielectric. This is the standard gate dielectric of the full device, and D: all field plates and thinnest dielectric. This is the standard device design for a lower voltage device.

Type D devices are studied for AC measurements while Type A, B, and C are all used for mechanical stress studies. For mechanical stress, most of the measurements are done on Type A. Devices under this type have a gate placed where an integrated gate field plate would be. This leads to very large dielectric thickness and therefore a larger than usual threshold voltage. However, we still use these devices as they are the most common in the wafer, allowing for effective statistical comparisons necessary for interpreting TDDB data.

From henceforth, gate voltage will be described by the gate overdrive, defined as

$$V_{GT} = V_{GS} - V_T \tag{3.1}$$

Where V_T is the threshold voltage.

3.3 Device Characteristics

Figure 3-2 through 3-5 show the transfer and output curves of the four device types. The transfer and output characteristics of Type A devices (Figure 3-2) show a well-behaved transistor. In the transfer sweep, gate voltage is swept from $V_T - 4$ to $V_T + 6$ V while the drain voltage is held at

0.05 V and 0.5 V (for each curve). For the output sweep, the drain voltage is swept while the gate voltage is increased from $V_T + 2$ to $V_T + 7$ V in 1 V increments. The body is left floating.

Similarly, transfer and output sweep of a Type B device shows a well behaved transistor. The transfer sweep drain bias is held at 0.05 V and 0.5 V as before. For the output sweep, the drain voltage is swept while the gate voltage is increased from $V_T + 2$ to $V_T + 7$ V in 1 V increments. The saturation towards the larger gate voltage bias in the output characteristic plot is due to the source measurement unit compliance. The body is left floating.

Transfer and output characteristics of Type C devices are very similar to Type B devices. As Type C devices are in essence a combination of Type A and Type B devices, the electrostatics through the gate stack will be similar to that of Type B devices, resulting in this shared output and transfer characteristics. As we will see later, the Off-state breakdown voltage behavior will be similar between Type A and Type C devices, reflecting the impact of the electrostatics of the integrated gate field plate. The measurement conditions are identical to Type B devices.

Finally, the transfer and output curves of a Type D device reveal a very well behaving transistor with excellent subthreshold swing. For the transfer sweep, V_{DS} is held at 0.5 and 0.05 V while V_{GS} is swept from $V_T – 2$ V to $V_T + 3$ V. For the output curve measurement, V_{GS} is held from $V_T – 0.5$ V to $V_T +3.5$ V in 1 V intervals while V_{DS} is swept from 0 to 5 V. The body is left floating.

Clearly, the device characteristics and performance plots show that the transistors are nearly ideal in behavior. However, reliability issues like TDDB limit widespread commercial deployment of these devices. In the next section, we address the experimental setup used to assess the validity of DC lifetime estimate and the impact dielectric traps have on dielectric reliability.

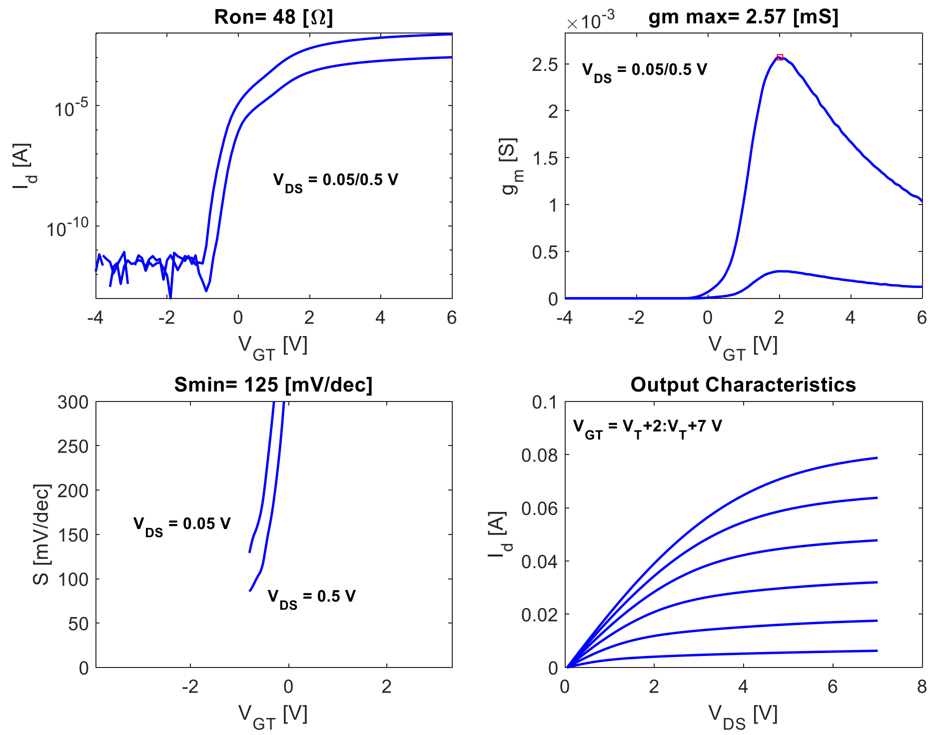


Figure 3-2 Transfer and output characteristics of a typical Type A device.

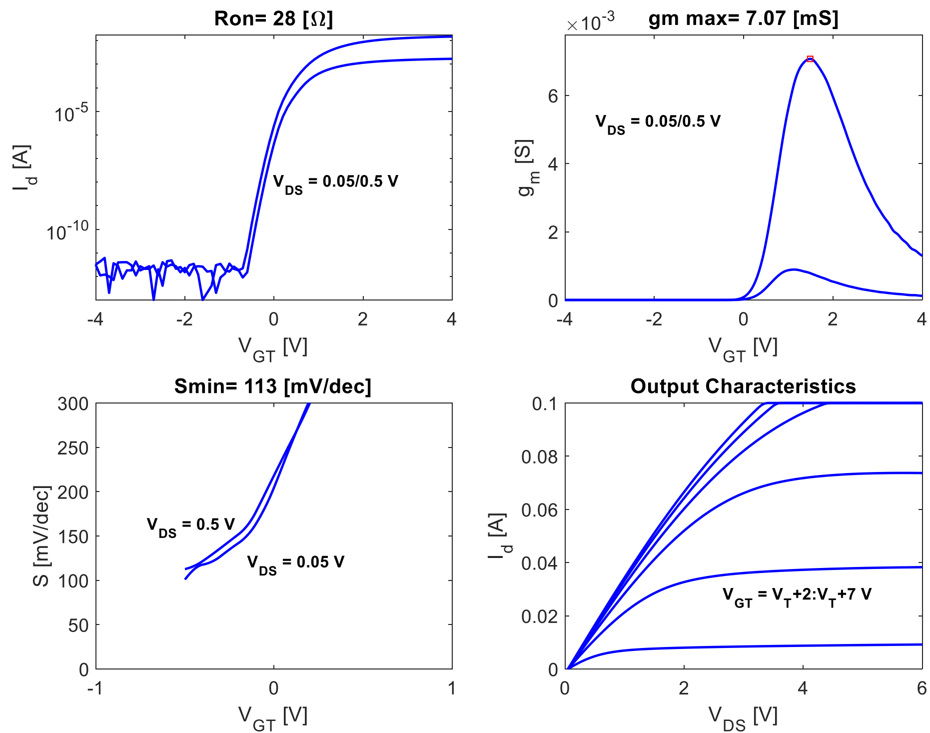


Figure 3-3 Transfer and output characteristics of a typical Type B device.

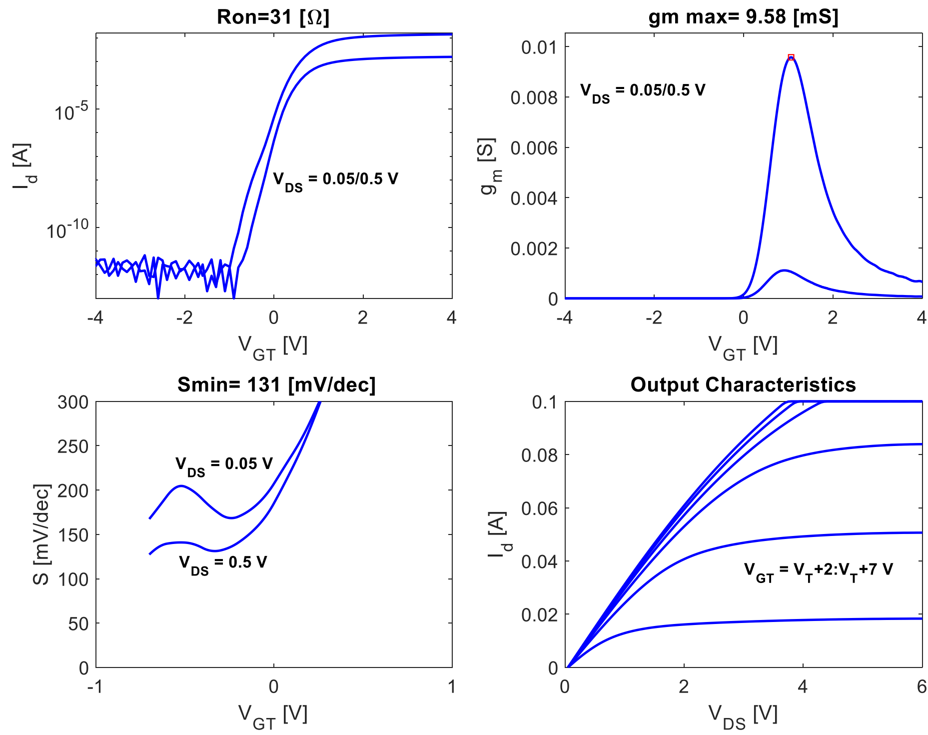


Figure 3-4 Transfer and output characteristics of a typical Type C device.

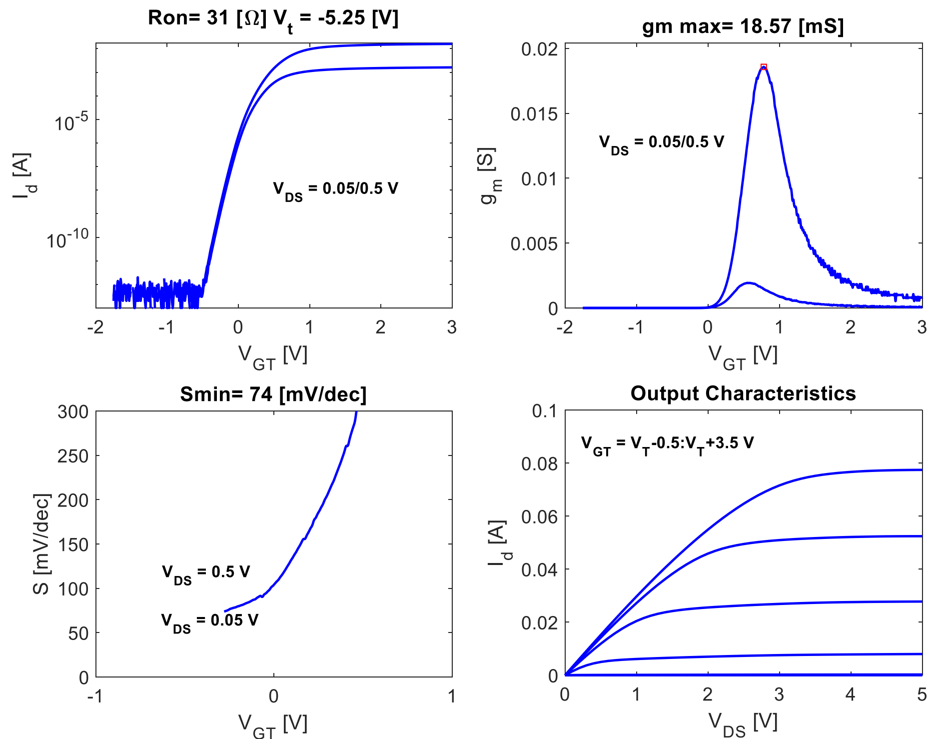


Figure 3-5 Transfer and output characteristics of a typical Type D device.

3.4 Measurement Equipment

All measurements are done on Keysight's B1500A Semiconductor Device Parameter Analyzer (SDPA) or B1505B Power Device Analyzer (PDA).

3.4.1 AC TDDB Setup

The B1500A SDPA is used primarily for AC TDDB measurements. The drain and source terminals of Type D devices are connected to two High Resolution Source Measurement Units (HRSMUs) installed inside the B1500A. The gate terminal is connected to either the Medium Power Source Measurement Unit (MPSMU) or the High Voltage Semiconductor Pulse Generator Unit (HV-SPGU). The body is left floating.

The MPSMU is limited in the frequency it can apply due to its lower slew rate (V/sec). However, the gate current can be measured (Figure 3-6) while the gate AC bias is applied. On the other hand, the HV-SPGU supports a large frequency (up to 1 MHz) with the tradeoff being that the gate current cannot be measured continuously. In this instance, the breakdown condition must be monitored through the drain or the source terminal.

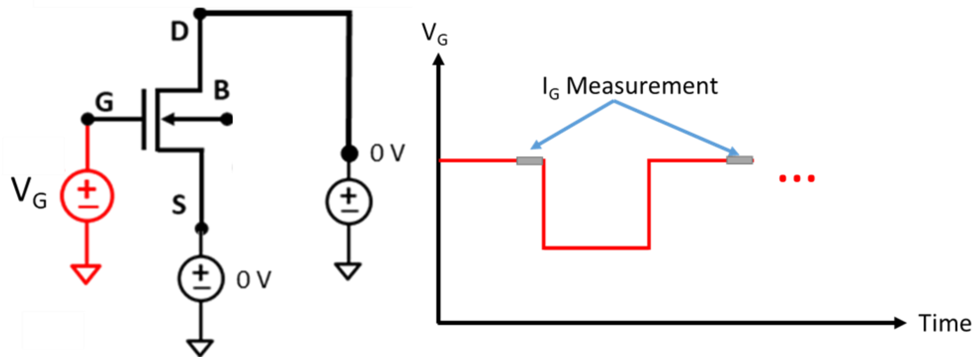


Figure 3-6 Diagram of stress setup and gate current measurement during AC stress using the MPSMU.

To simplify the relevant physics during TDDB, we choose to compare the results between DC and AC stress for On-state or forward-bias TDDB. As discussed previously in chapter 2, On-state TDDB's more uniform distribution of the electric through the dielectric under the gate metal allows for a simpler picture of the physics involved.

Therefore, following the stress conditions for On-state TDDB, the source and drain are held at 0 V while AC stress (or DC stress as reference) is applied to the gate. The gate is stressed with a stress bias of 8.5 V. With an AC voltage across the gate, four parameters can be altered in comparison to DC: 1. Waveform shape, 2. Frequency, 3. Duty cycle, and 4. Recovery voltage.

First, a square wave is chosen for the waveform shape. TDDB is known to have an exponential dependence on electric field [13]. An application of a sine wave for example makes accurate extraction of actual stress duration difficult as the voltage is constantly changing. A square wave allows for a definite determination of the stress time (when voltage is high) and better mimics conditions presented in DC TDDB.

Second, frequency is logarithmically swept from 1 Hz to 100 kHz. This sweeping allows for studying the evolution of TDDB behavior with frequency change. TDDB statistics are collected and compared between DC and AC at these frequencies to determine when the departure in behavior, if any, becomes definite.

Third, the duty cycle is chosen to be 50%. The ramp rate is chosen to ensure there is minimal overshooting in the waveform. The 50% duty cycle allows for equal stress and recovery duration.

Finally, the recovery voltage (low voltage portion of the square wave) can be changed. Since electron trapping occurs during stress due to the large positive bias across the gate, relaxation may partially empty the electron traps. The relaxation bias can be modulated to become more negative so that the electrons are more energetically encouraged to be detrapped [23].

3.4.2 Mechanical Stress TDDB Setup

All mechanical stress measurements are done with the B1505 PDA. The Power Device Analyzer's High Voltage Source Measurement Unit (HVSMU) allows for application of a very large voltage (up to 2000 V) that is necessary for Off-state measurements. Here, the source and gate terminals are each connected to High Power Source Measurement Units (HPSMU) which allow for application of up to 200 V. The drain terminal is connected to the HVSMU. Finally, the body is kept at 0 V with respect to the source by an electrical connection through the chuck holding the wafer. The chuck is connected to a Medium Power Source Measurement Unit.

The stress conditions of the 3 device types and 2 stress conditions are summarized below in Figure 3-7.

On-state	Type A	Type B	Type C
V_{GS} [V]	128	24	24
V_{DS} [V]	0	0	0
V_{BS} [V]	0	0	0

Off-state	Type A	Type B	Type C
V_{DG} [V]	325	150	350
V_{BS} [V]	0	0	0

Figure 3-7 Summarized table of voltage stress values applied to each device type in the study of the impact of mechanical stress on TDDB.

Mechanical stress is induced by substrate thinning. The next section details the steps used to thin the substrate as well as strain and stress calculations.

3.4.3 Substrate Thinning for Mechanical Stress Characterization

First, industry provided 6-inch wafers have a total thickness of 254 um thickness. They were then diced into 2 cm by 3 cm using a die saw tool at the Microsystems Technology Laboratories (MTL) at MIT. In the same cleanrooms, AZ4620 photoresist was spin coated onto a 6-inch Si wafer. A circular trench was then made by scraping off the photoresist at a fixed radius from the center of the wafer. This was done so that when the chips were mounted to the wafer upside-down, active areas of the chip would be less exposed to possibility of photoresist residue. A cross section of this process is shown in Figure 3-8.

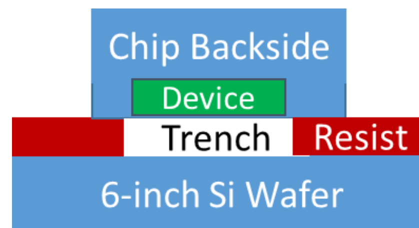


Figure 3-8 Cross section after the chip is mounted upside down on a 6-inch wafer. The trench prevents any resist to remain after processing.

Once the chips were mounted upside down (Si substrate facing top), the photoresist was cured at 95 degrees Celsius for one hour. Afterwards, the wafer underwent Deep Reactive Ion Etching

(DRIE) using SPTS Pegasus at MTL. Chips were etched in an SF_6 and O_2 environment (10:1 ratio) in a 5 minute etch/ 3 minute rest cycle repeated 3 times (15 minutes total).

Once etched, the chips were placed in an acetone bath for 3 hours at room temperature. This released the chip from the carrier Si wafer. After the acetone bath, the chips underwent further cleaning inside warm *N*-Methyl-2-pyrrolidone solution for 1 hour. The chips were then finally cleaned by rinsing under acetone, methanol, and isopropyl alcohol.

The result of the processing step can be seen in Figure 3-9. The chips were thinned to a final thickness of 40 um, becoming translucent and extremely bent.

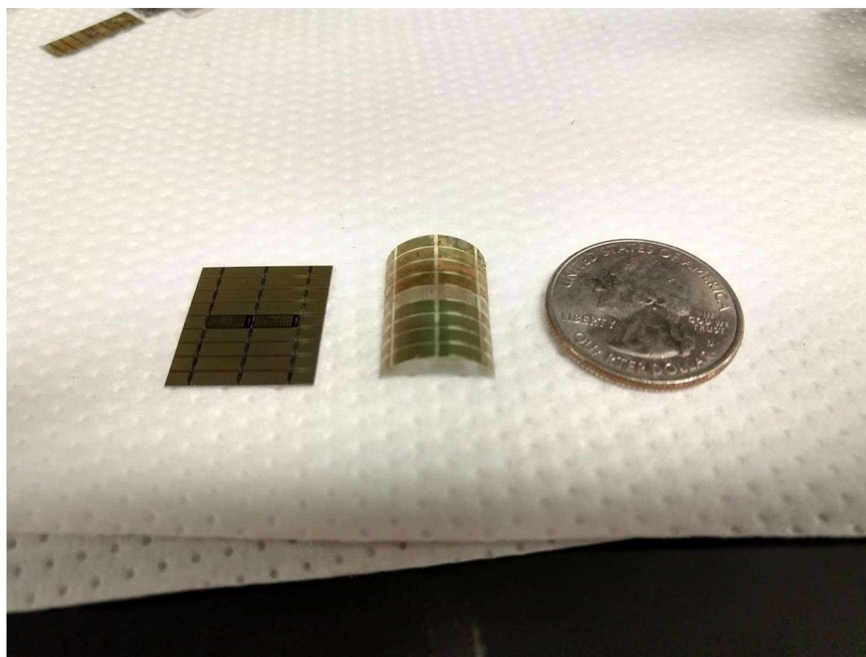


Figure 3-9 Left: 254 um thick chip. Right: 40 um thick chip after substrate etching.

Since the chips showed natural bending in the channel direction due to uncompensated stress, they were mounted on a metal cylinder to allow for device characterization (Figure 3-11). Strain was calculated by measuring the radius of curvature (metal cylinder) and knowing that the dielectric is approximately 20 um away from the neutral axis of the bent chip.

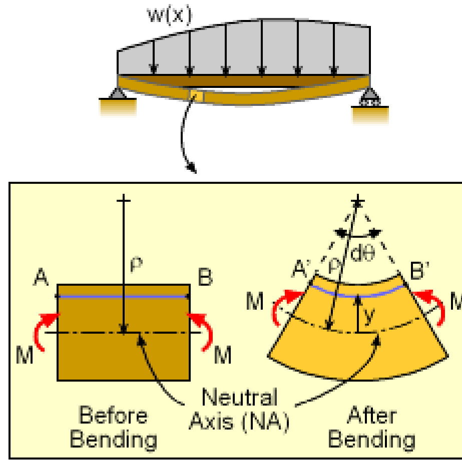


Figure 3-10 Approximation of strain from radius of curvature [24].

Since strain is

$$\boldsymbol{\varepsilon} = \frac{\boldsymbol{\Delta L}}{\boldsymbol{L}} \approx \frac{\boldsymbol{A'B'} - \boldsymbol{AB}}{\boldsymbol{AB}} \tag{3.1}$$

And from Figure 3-10,

$$\boldsymbol{A'B'} = (\boldsymbol{\rho} - \boldsymbol{y})\boldsymbol{d\theta} \tag{3.2}$$

$$\boldsymbol{AB} = \boldsymbol{\rho d\theta} \tag{3.3}$$

We can get an expression for the strain and the stress at the top of the bending surface by combining (3.1), (3.2) and using the Young's Modulus.

$$\boldsymbol{\varepsilon} = \frac{(\boldsymbol{\rho} - \boldsymbol{y})\boldsymbol{d\theta} - \boldsymbol{\rho d\theta}}{\boldsymbol{\rho d\theta}} = -\frac{\boldsymbol{y}}{\boldsymbol{\rho}} \tag{3.4}$$

$$\boldsymbol{\sigma} = \boldsymbol{E\varepsilon} \tag{3.5}$$

The metal cylinder used has a radius of 70 mm. Then, the strain is calculated to be $\varepsilon = 0.29\%$ and in the channel direction. While the exact value is unknown, Young's Modulus of silicon nitride is reported to be between 100-300 GPa. Using the median value of 150 GPa, the expected stress across the dielectric is approximately E = 435 MPa.

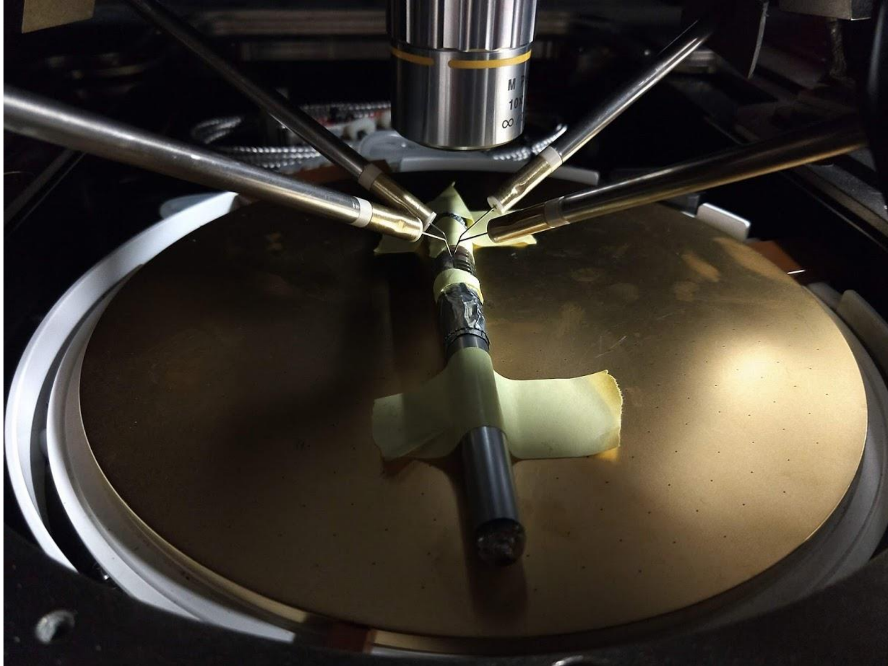


Figure 3-11 Probe contact for 40 um process thinned chips.

3.5 Summary

We have introduced the devices under study which show nearly ideal electrical characteristics. Electrical stress conditions for both AC and mechanical stress measurements were discussed as well as methodologies for applying mechanical stress.

In the next chapter, we discuss the results from investigating whether TDDB behavior changes significantly under AC stress compared to DC stress. Studying the change allows us to, 1. Determine whether time to failure approximations done from DC is accurate or at least conservative, and 2. Offer a glimpse toward the underlying physics behind TDDB.

Chapter 4 TDDB under AC stress

4.1 Introduction

While dielectric reliability projections under DC stress conditions are useful due to simple measurement methods, there is ambiguity on the accuracy of the estimates. In actual power circuits, devices undergo rapid switching between forward and reverse-biased conditions in the kHz to MHz range. As the GaN MIS-HEMT hosts a wealth of dynamic processes such as electron trapping [25] and electron accumulation in the SiN/AlGaN interface [10], it is yet unclear what impact the constantly changing electric field will have on the dielectric reliability. Presently, there is very little research verifying the accuracy of dielectric reliability estimations from just using DC stress, especially in the GaN system.

In this chapter, we investigate whether reliability estimation using DC stress is accurate. To achieve this, we compare TDDB under DC On-state conditions with TDDB under AC On-state conditions. For DC measurements, the source and drain are held at ground while the gate is held at 8.5 V to accelerate damage in the dielectric. For AC measurements, the gate is cycled between 8.5 V and a much lower recovery voltage of either -8.5 V or 0 V in a square waveform while the source and drain is again held at ground. Unless otherwise specified, the duty cycle of the square wave is at 50%. In both cases, the body is left floating. Figure 4-1 shows the oscilloscope trace of the gate voltage waveform at 1 Hz and 10 kHz. Stress time calculation is straight forward as the waveform shows a sharp transition between stress voltage and recovery voltage. For 1 kHz and above, stress time is actually 45% of the period due to the limited slew rate.

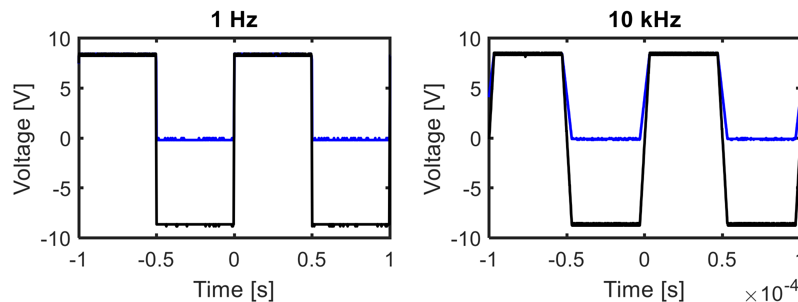


Figure 4-1 Oscilloscope trace of actual waveforms used in AC TDDB for 1 Hz and 10 kHz. The sharp transition allows for accurate estimation of stress time.

4.2 AC TDDB vs DC TDDB for Si

In literature, AC TDDB studies done on Si substrates show a widely changing behavior that depends on the dielectric material and the frequency used.

Hirano et al. found that sub-1Hz AC TDDB unipolar and bipolar measurements for HfSiON gate n-type MOSFETs show very little T_{63} change compared to DC TDDB. However, they found substantial improvement of the Weibull slope ß when applying bipolar stress. This improvement appears to increase with longer recovery time (decreasing duty cycle) [26]. They attribute this improvement to changes to defect size due to modulation of electron and hole trapping/detrapping.

On the other hand, Kerber et al. measured 100 Hz bipolar AC TDDB measurements for n-MOSFET on SOI substrate with Hafnium-based high-k dielectrics. They report an order of magnitude reduction in hard breakdown times compared to DC stress conditions [23]. They attribute this degradation to electron detrapping in the dielectric that leads to a stronger electric field.

Lee et al. support this finding by showing that 1 kHz bipolar AC TDDB measurements show a reduction in hard breakdown times compared to DC stress conditions for Hafnium-based dielectric on Si [27]. However, they also show that further increasing the frequency of the bipolar stress to 100 kHz results in an improvement compared to DC. They further report that poly-Si/SiON n-type MOSFETs also show improving TDDB behavior (increasing hard breakdown times) with increasing unipolar and bipolar stress frequency. They attribute the improvement in poly-Si/SiON to less hole generation during high voltage and detrapping of generated holes during low voltage periods. For the Hafnium-based dielectric MOSFETs, they hypothesize that at low frequencies the interlayer between the substrate and the dielectric is quickly damaged by hole generation but at high frequencies there is not enough time per stress cycle for hole generation.

Finally, Schwab et al. found that bipolar AC TDDB measurements ranging from 0.1 Hz to 10 kHz show hard breakdown times improvement compared to DC for metal insulator metal capacitors with SiN dielectric [28]. However, they found that the improvement largely depended on the processing of the nitride. Nitrides that are silicon rich tended to perform better under AC conditions than DC. They suggest that this improvement is due to stronger electron trapping on both sides of the dielectric under bipolar stress that leads to a weakened electric field in the dielectric.

Just from these 4 reports, it is immediately clear that change in TDDB behavior with AC stress compared to DC stress is difficult to predict. The change is dependent on the dielectric and stress frequencies. As mentioned before, the GaN system used in this thesis has further complications added due to the complex gate stack. Therefore, verifying the accuracy of TDDB measurement results from DC stress conditions with that of AC is of utmost importance.

4.3 Low Frequency AC TDDB

We first start with 1 Hz AC TDDB bipolar stress. This stress condition mimics the transition of the gate voltage between on and off state but has a low frequency to allow for the behavior to be close to DC stress conditions. As a bonus, gate leakage current can be measured for AC stress as this low frequency can be applied with a traditional source measurement unit.

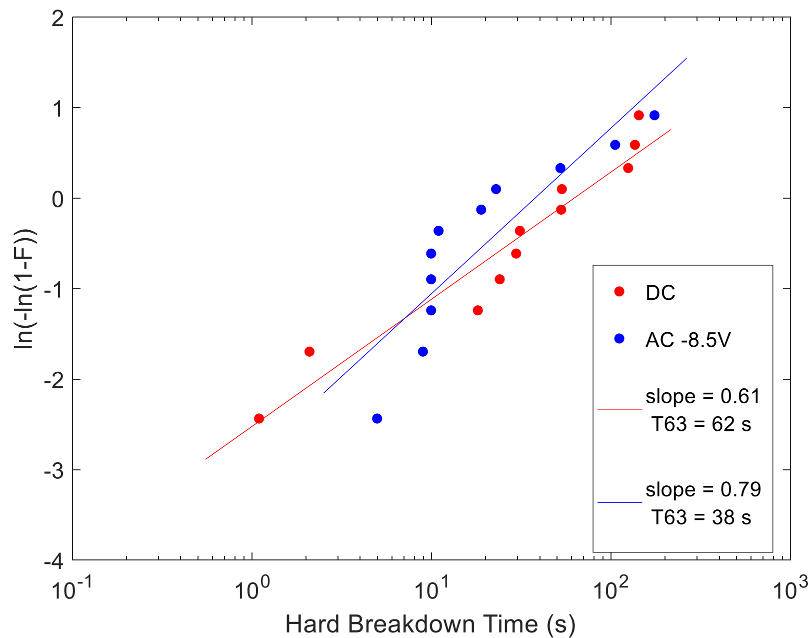


Figure 4-2 Weibull failure distribution comparison between DC stress and 1 Hz 50% duty cycle AC stress. V_{GS} = 8.5 V for DC, 8.5V/-8.5V for AC, V_{DS} = 0V. Body is left floating. Data comes from one die.

Figure 4-2 shows a TDDB measurement comparison between DC and bipolar AC stress at 1 Hz with a recovery voltage of -8.5 V (symmetric gate voltage). While there seems to be some degradation in the overall breakdown times for AC (T_{63} = 49s) compared to DC (T_{63} = 65s), the limited sample size makes a conclusion difficult. As the number of devices per die is limited,

accurate collection of data requires measuring multiple dies. However, one must practice caution when doing this. In fact, Figure 4-4 graphs the Weibull failure distribution for AC stress conditions from 3 different dies. Even though identical stress conditions are used, there is considerable die to die variation.

To minimize the impact of die to die variation, samples are interspersed such that both stress conditions are represented in each die. Therefore, die to die variation is suppressed and the overall statistics become much clearer thanks to the larger sample size.

Data accumulated over three dies in this manner are plotted in Figure 4-3. There is a definite lack of change between DC and AC stress conditions at this low 1 Hz frequency. In addition to the DC and symmetrical AC bipolar stress, an additional stress condition of 8.5V/-3 V bipolar AC stress is added for comparison. This is done to investigate the impact of weakening the recovery stress magnitude. The Weibull slope ß and y-intercept T_{63} is nearly identical between DC, AC 8.5V/-8.5V, and AC 8.5V/-3V (ß = 0.85, 0.90, 0.91 and T_{63} = 62, 57s, 62s). This result is not surprising as pausing the stress has been shown to not impact the overall TDDB behavior [29]. As pausing is similar to low frequency AC stress with cycling between long DC stress and pauses, we expect TDDB behavior to not change significantly.

The gate leakage currents corresponding to Figure 4-3 are plotted in Figure 4-5. It is important to note that AC measurements before 1 s is inaccurate as the 1 Hz data takes a measurement every second. Comparing the current evolution past the one second mark shows that SILC and HBD are remarkably similar between the two. Thus, we can conclude that at this low frequency there is no change in the physics involved in TDDB.

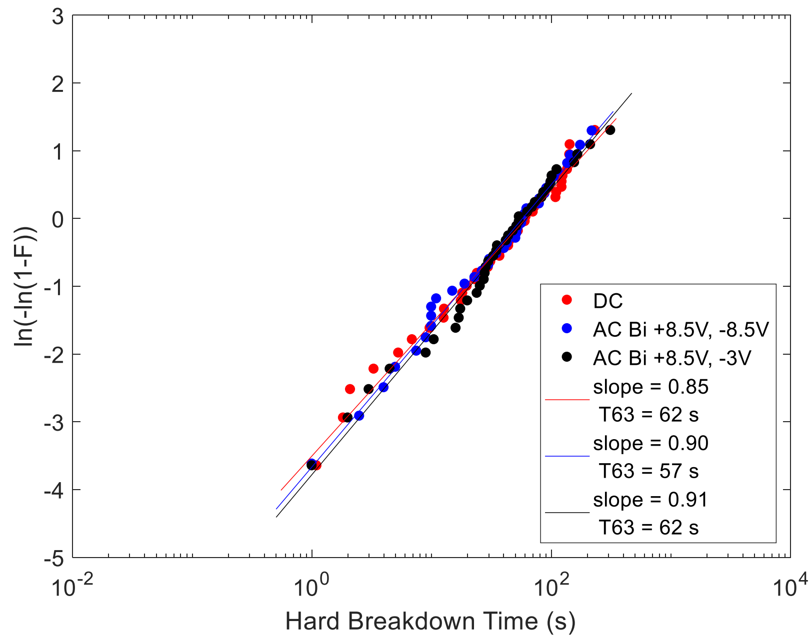


Figure 4-3 Weibull failure distribution comparison between DC stress and 1 Hz 50% duty cycle AC stress. V_{GS} = 8.5 V for DC, 8.5V/-8.5V for AC, V_{DS} = 0V. Body is left floating. Data comes from three dies.

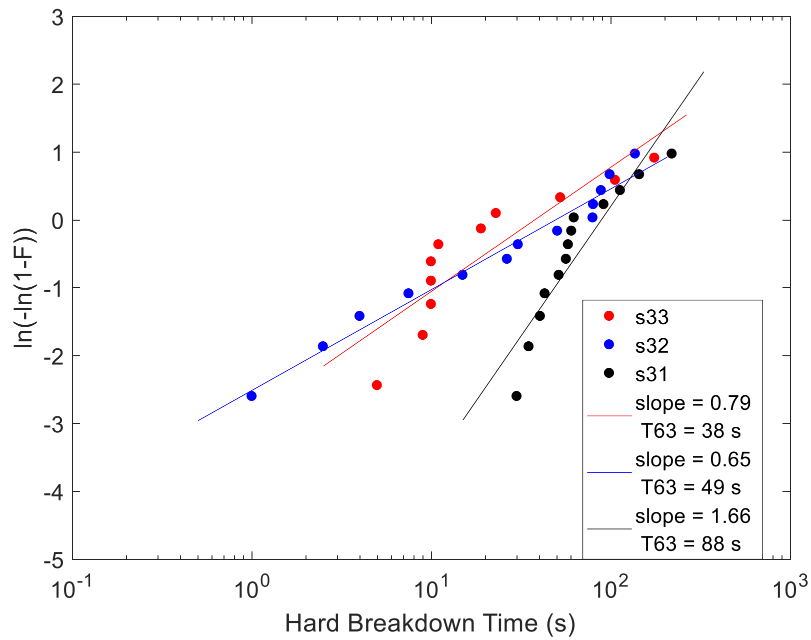


Figure 4-4 Weibull failure distribution comparison between 1 Hz 50% duty cycle AC stress between three dies. V_{GS} = 8.5V/-8.5V for AC, V_{DS} = 0V. Body is left floating. Each dataset comes from one die.

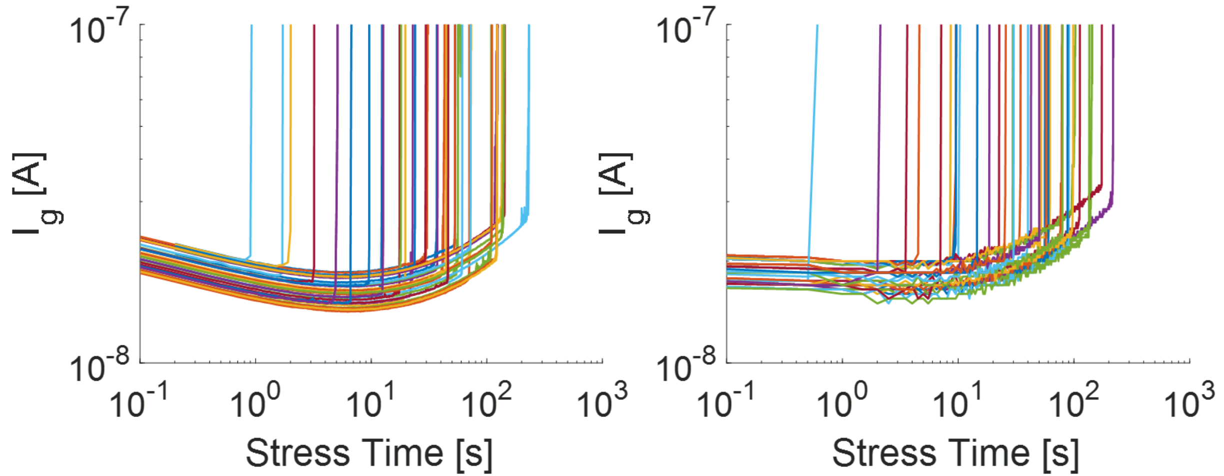


Figure 4-5 Gate leakage current versus time for DC stress and 50 % DC AC 1 Hz bipolar AC stress. V_{GS} = 8.5 V for DC, 8.5V/-8.5V for AC, V_{DS} = 0V. Body is left floating. Data comes from three dies.

4.4 High Frequency AC TDDB

As devices stressed under 1 Hz do not show any change in TDDB behavior compared to DC, we now move on to higher frequencies. Ultimately, the target frequency is between 100 kHz and 1 MHz as the devices used in the thesis are targeted to operate at that range.

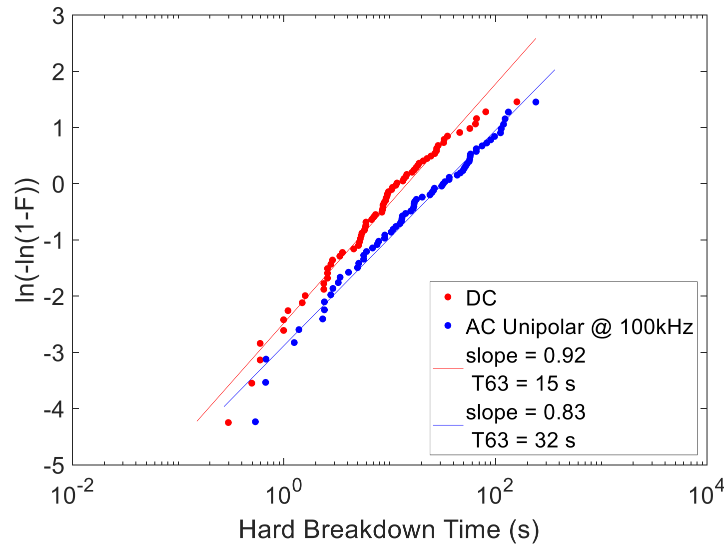


Figure 4-6 Weibull failure distribution comparison between DC stress and 100 kHz 45% duty cycle AC stress. V_{GS} = 8.5 V for DC, 8.5V/0 V for AC, V_{DS} = 0V. Body is left floating. Data comes from six dies.

Increasing the stress frequency to 100 kHz stress shows a very clear increase in the hard breakdown distribution for AC stress compared to DC as shown in Figure 4-6. Comparing the T_{63} times of 32s for AC unipolar stress and 15s for DC stress show a factor of two increase in the overall hard breakdown time. Clearly, there is a frequency dependence on the behavior of AC stress. This behavior is repeated for symmetrical AC bipolar stress (8.5V/-8.5V) in Figure 4-7.

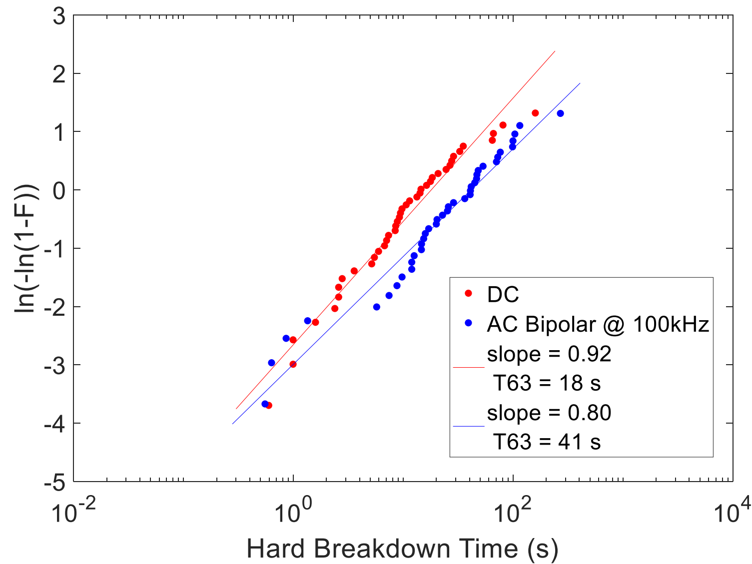
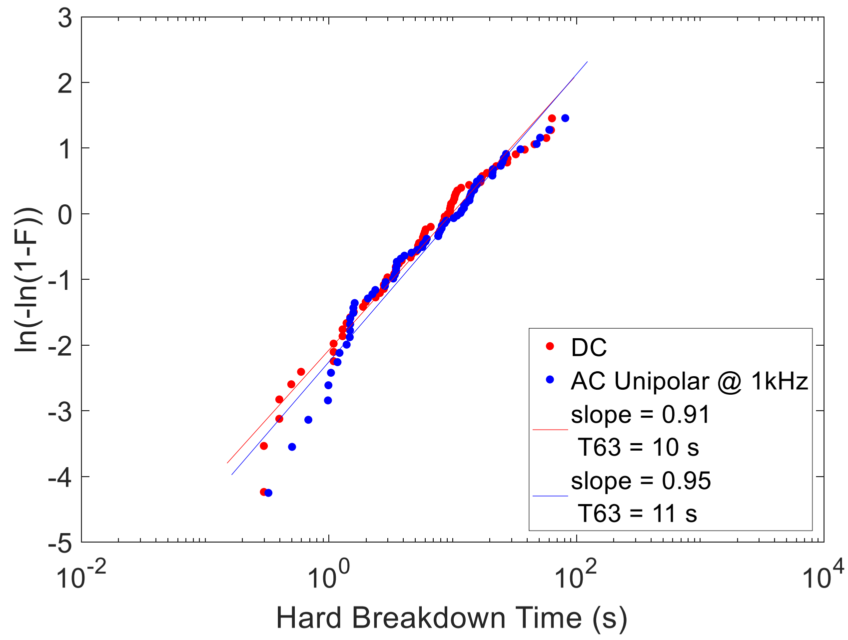


Figure 4-7 Weibull failure distribution comparison between DC stress and 100 kHz 45% duty cycle AC stress. V_{GS} = 8.5 V for DC, 8.5V/-8.5V for AC, V_{DS} = 0V. Body is left floating. Data comes from three dies.

There must then be a transition frequency in which the improvement for AC TDDB becomes clear. To get a rough estimate of this frequency, we repeat TDDB measurements for 1 kHz and 10 kHz.

As Figure 4-8 shows, there is very little change in TDDB for AC stress at 1 kHz for unipolar stress. However, as stress frequency is increased to 10 kHz in Figure 4-9, there is a distinguishable improvement. In fact, the ratio of the T_{63} between AC and DC from 1 kHz to 10 kHz increases from 1.1 to 1.45 for unipolar stress.



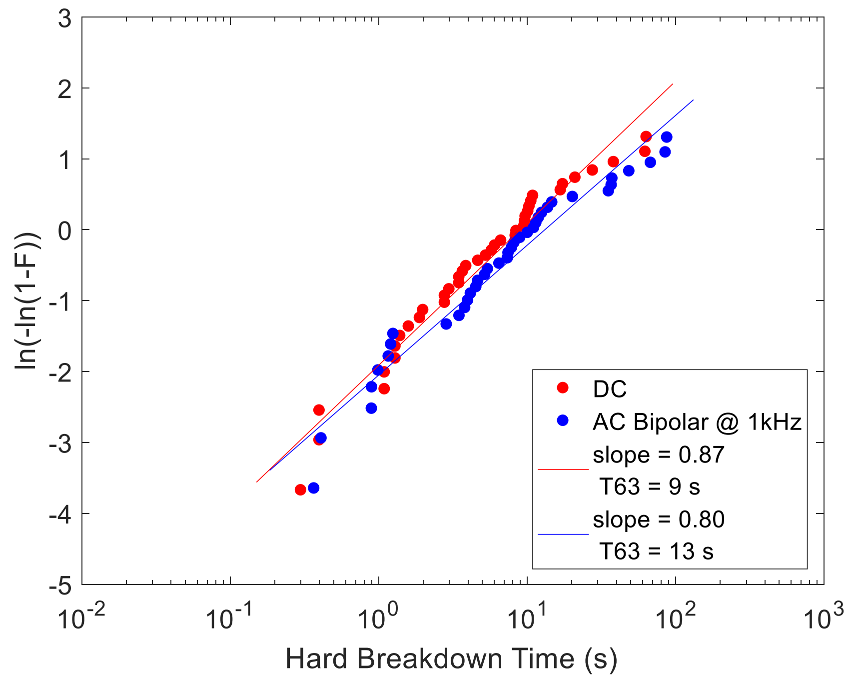
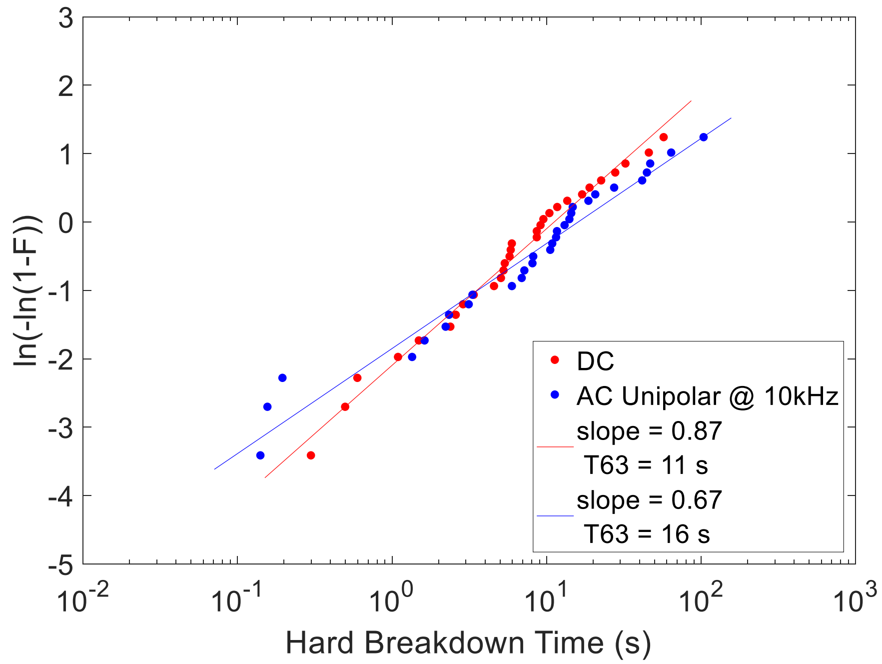


Figure 4-8 Weibull failure distribution comparison between DC stress and 1 kHz 45% duty cycle AC stress. V_{GS} = 8.5 V for DC, 8.5V/0V (top) or 8.5V/-8.5V (bottom) for AC unipolar and bipolar respectively, V_{DS} = 0V. Body is left floating. Data comes from three dies.



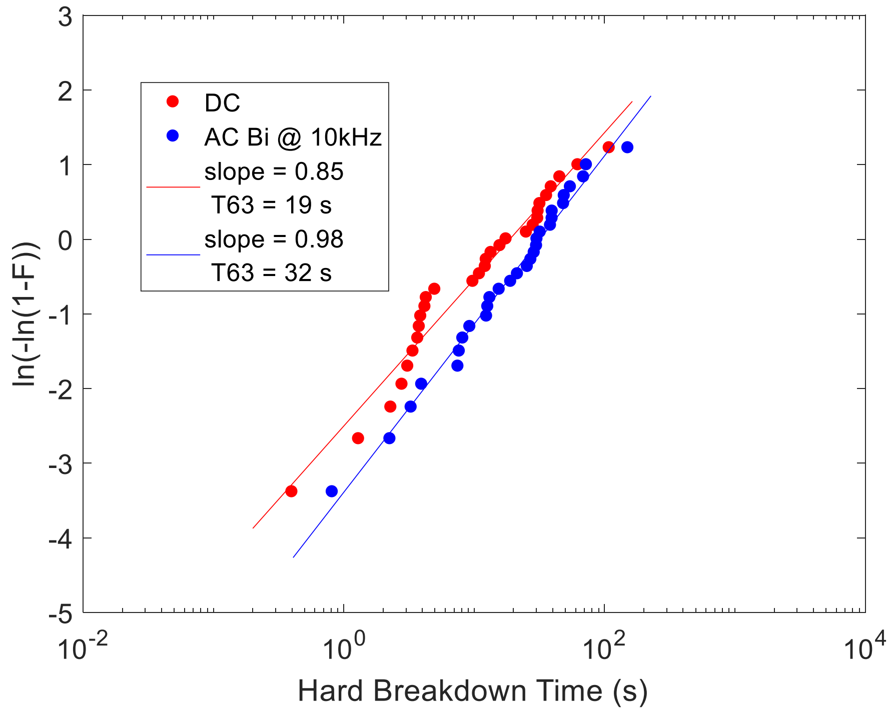


Figure 4-9 Weibull failure distribution comparison between DC stress and 10 kHz 45% duty cycle AC stress. V_{GS} = 8.5 V for DC, 8.5V/0V (top) or 8.5V/-8.5V (bottom) for AC unipolar and bipolar respectively, V_{DS} = 0V. Body is left floating. Data comes from three dies.

4.5 Acceleration Factor Versus Stress Frequency

We define this ratio of the T_{63} between AC and DC as the acceleration factor α. In Figure 4-10, we take the acceleration factors calculated from Figure 4-3 to Figure 4-9 and plot them versus frequency for both unipolar and bipolar measurement results. We see that there is a very definite change in the TDDB improvement versus frequency of AC stress that becomes noticeable at a frequency of ~10 KHz.

The natural question is then where this improvement comes from. Earlier in the chapter, two possible explanations for improving hard breakdown times with increasing frequency were given. Schwab et al. suggest that increased electron trapping occurs for bipolar stress. Indeed, the acceleration factor plot shows slightly improved behavior for bipolar stress compared to unipolar stress. On the other hand, as the devices studied in this thesis are not capacitors, bipolar stress does not necessarily result in electron injection/trapping from both sides of the dielectric. As discussed before, Lee et al. hypothesize that decreased hole generation and improved hole detrapping during AC stress lead to this improved reliability. However, it is difficult to reconcile this theory with the lack of a hole generating mechanism in GaN MIS-HEMT's metal gate.

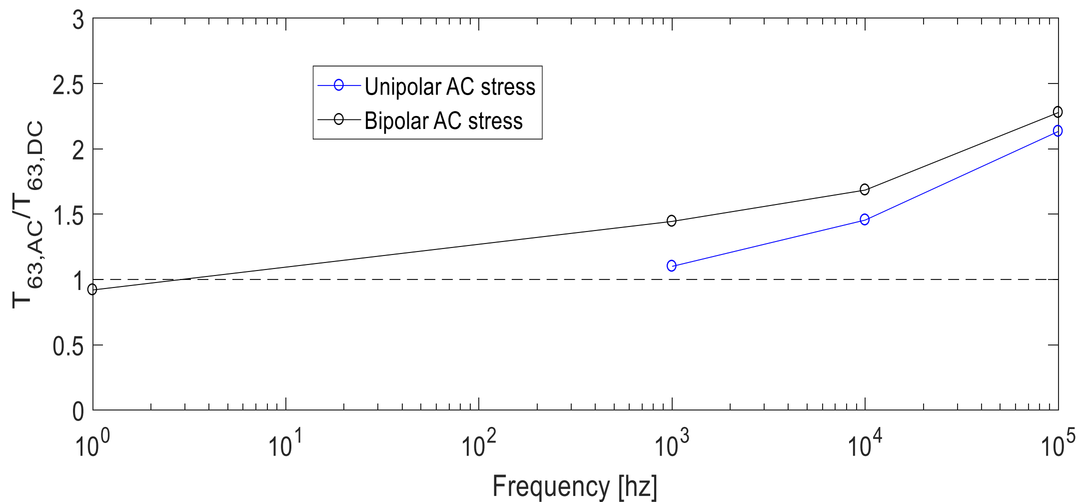


Figure 4-10 Acceleration parameter versus stress frequency for unipolar and bipolar AC TDDB. Duty cycle is fixed at 45%.

While more work needs to be done to understand the reason for the improvement, a property unique to the GaN MIS-HEMT system may suggest a possible explanation. Huang found that the gate to channel capacitance (C_{GG}) at a large constant positive gate voltage drops in magnitude with

increasing frequency for devices with Al_2O_3 dielectrics [8]. Warnock verified this behavior for devices more similar to ones used in this thesis [10]. As Figure 4-10 shows, at $V_{GT} = 0$ V the gate to channel capacitance jumps. This is consistent with electron accumulation in the 2DEG. C_{GG} then saturates until $V_{GT} > 11$ V at which point electron accumulation in the AlGaN/dielectric interface causes the capacitance to jump once more. However, as the right of Figure 4-11 shows, this jump becomes more suppressed with higher gate voltage frequency.

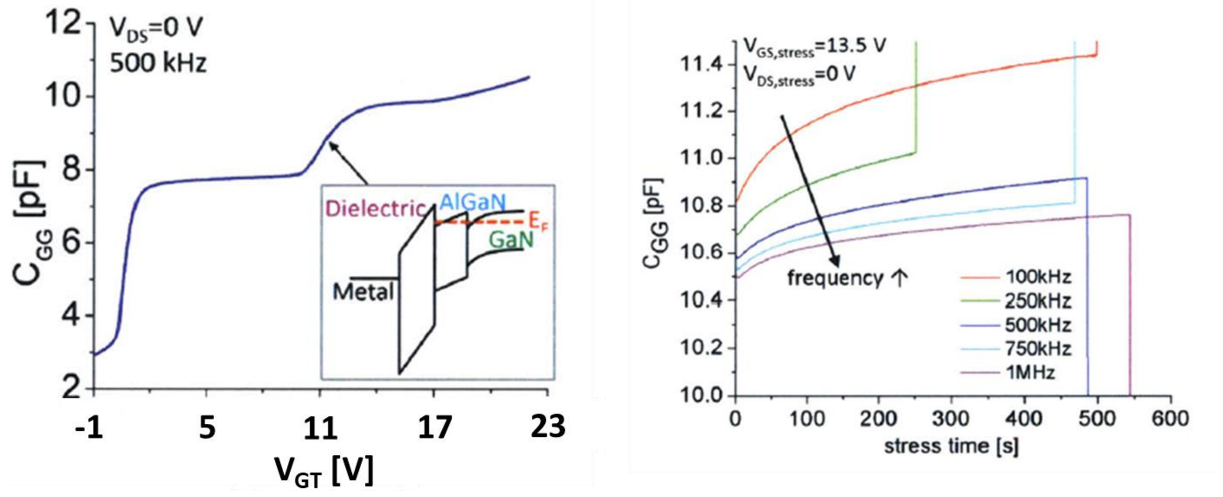


Figure 4-11 Gate to channel capacitance C_{GG} evolution over stress time at various measurement frequencies. The drop in capacitance at a given stress time with increasing frequency correspond to less electron accumulation in the conduction band edge of the AlGaN/dielectric interface [10].

This is consistent with a decreasing ability to modulate the electron concentration in the conduction band at the AlGaN/dielectric interface as the frequency increases. Under steady state with large positive gate bias, electrons have little trouble getting to the inversion layer at the AlGaN/dielectric interface (Figure 4-12). This is most likely done by overcoming the barrier that separates the interface from the 2DEG at the AlGaN/GaN interface. However, this is a relatively slow process. If the gate voltage changes rapidly, the electron concentration at the dielectric/AlGaN interface can't follow and hence, the 2DEG at the AlGaN/GaN interface is modulated. This results in a lower electric field across the dielectric and an increased dielectric breakdown time. This is a situation not too dissimilar to "deep depletion" in MOS capacitor structures.

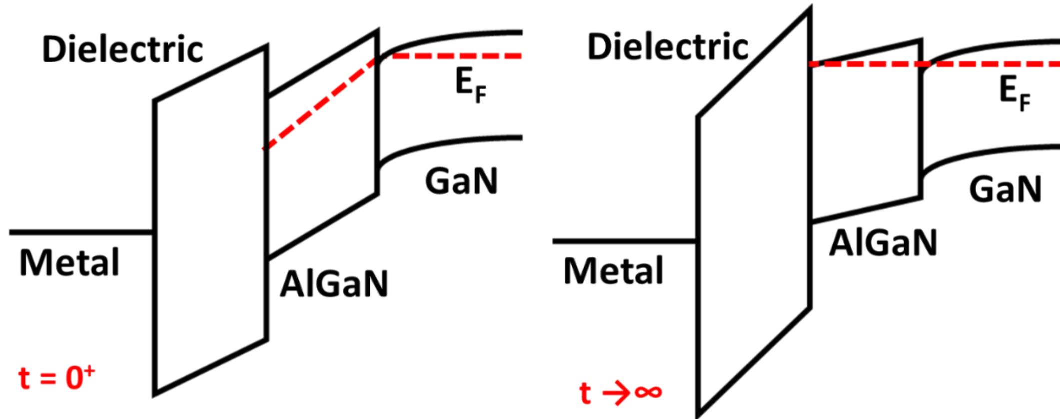


Figure 4-12 Band diagram of GaN MIS-HEMT with positive gate bias. At the beginning of a pulse, electrons have not responded to the changing stress. Voltage is dropped across both the dielectric and the AlGaN (left). Given enough time, a steady state will be reached where there is electron accumulation in the AlGaN conduction band (right).

While the transition frequency at which the AlGaN conduction band population begins to be impeded must be measured for the devices studied in this thesis, this behavior explains the frequency dependence observed in the study. This explanation also fits the result that bipolar stress consistently shows improved hard breakdown times compared to unipolar. Applying a negative V_{GS} further encourages electrons that managed to accumulate at the dielectric/AlGaN interface to return to the 2DEG, ensuring a lower electric field across the dielectric and therefore higher hard breakdown time. If verified, this unique property of the GaN/AlGaN stack can lead to longer hard breakdown times than expected from DC measurements.

4.6 Summary

We find that at 1 Hz, there is no discernable difference between TDDB measurements under DC and AC stress. We also find that at much higher frequencies (>1 kHz), time to breakdown becomes frequency dependent and increases as the frequency increases. We find that the magnitude of the recovery bias (i.e. unipolar or bipolar) makes a difference in the enhancement of time to breakdown. Finally, we hypothesize that this frequency and recovery voltage dependence arises from the dynamical behavior of AlGaN conduction band population under high frequency stress. In the next chapter, we discuss results from studying TDDB with external mechanical stress.

Chapter 5 DC TDDB under Mechanical Stress

5.1 Introduction

In this chapter, we examine the results from applying DC voltage in both on and off conditions on dielectric reliability under different mechanical stress. Transfer characteristics are examined to see what changes, if any, arise from the modulation of the 2-Dimensional Electron Gas (2DEG) from the application of mechanical stress. Change in TDDB is measured with flat and tensile mechanical stress. Finally, timescales associated with electron trapping during DC voltage is calculated to investigate any changes in trap dynamics.

Before we can measure TDDB, we must first investigate whether the 2DEG is affected since piezoelectric charge of the AlGaN/GaN system should change with mechanical strain. For this, we first measure the transfer and the output curves of the devices with different mechanical strain and extract the threshold voltage, ON resistance, and transconductance.

5.2 Transfer and Output Characteristics Change

First, we discuss the expected behavior of threshold voltage, ON resistance, and transconductance with strain. As discussed in chapter 2, without any bending, GaN and AlGaN lattice mismatch causes additional piezoelectric polarization on top of the already present spontaneous polarization. Adding additional mechanical stress by bending changes the piezoelectric polarization. Even though the stress is roughly the same between the AlGaN and GaN layers due their small thickness compared to the Si substrate, the difference in piezoelectric coefficients between the two layers mean that polarization changes at different rates between the two layers.

With an application of tensile stress, 2DEG density has been measured to increase [30]. Increase in 2DEG density translates to a more negative threshold voltage. This can be intuitively understood by noting that now a greater negative gate voltage is needed to deplete a 2DEG with larger sheet charge density. Therefore, we expect our devices to show a negative change in threshold voltage

with tensile mechanical stress and positive change in threshold voltage with compressive mechanical stress.

However, the change in ON resistance and transconductance with the application of mechanical stress is less clear. Shockley's derivation of classical transistor behavior [31] shows that the transconductance in the saturation regime and ON resistance in the linear regime scale as:

1.1

$$g_m = \sqrt{2\frac{W}{L}\mu_e C_{ox} I_D} \tag{5.1}$$

$$R_{on} = \frac{1}{\frac{W}{L}\mu_e C_{ox}(V_{GS} - V_T)} \tag{5.2}$$

Where W is the width of the device, L is the channel length, C_{ox} is the dielectric capacitance, I_D is the drain current, μ_e is the electron mobility, V_{GS} is the gate to source voltage, and V_T is the device threshold voltage. Equation (5.2) omits R_S, the source resistance, and R_D, the drain resistance.

In both ON resistance and transconductance, there are several parameters that can change with mechanical stress/strain. First, it is reported that some dielectrics such as HfSiON show permittivity change with mechanical stress, leading to changes in oxide capacitance [32]. Also, mobility is shown to change with mechanical stress [33] [34]. Evidently, changes in transconductance and ON resistance are difficult to predict; therefore, threshold voltage change will be used as the primary indicator for changes to the 2DEG.

With the devices under tensile stress at strain of 0.29%, we report typical transfer and output characteristics of devices of Type A, B, and C in Figure 5-1 to Figure 5-3.

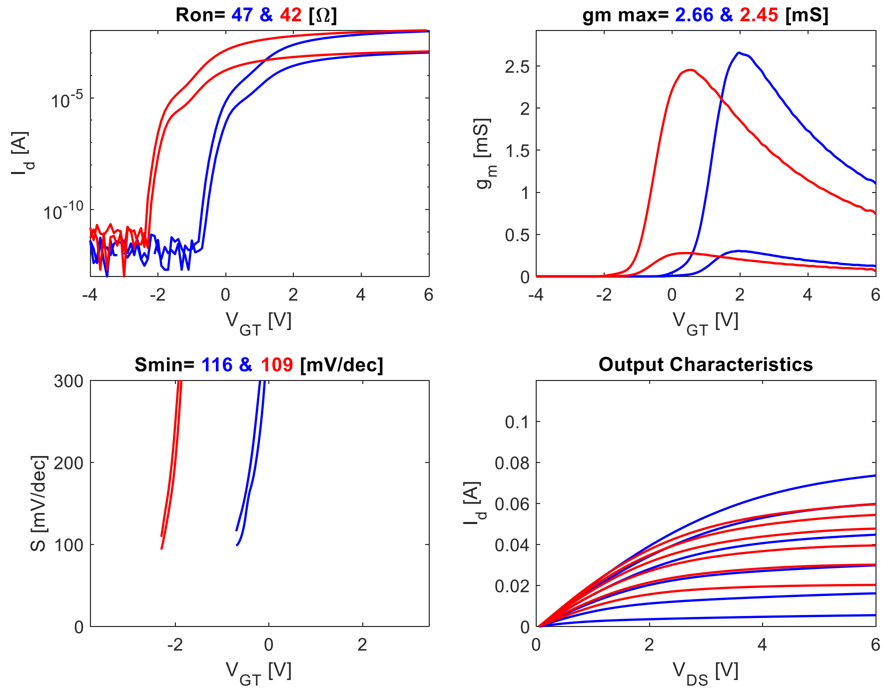


Figure 5-1 Transfer and Output curves of Type A device under 0.29% tensile strain (red) versus no strain (blue). Measurement conditions are same as Figure 3-2.

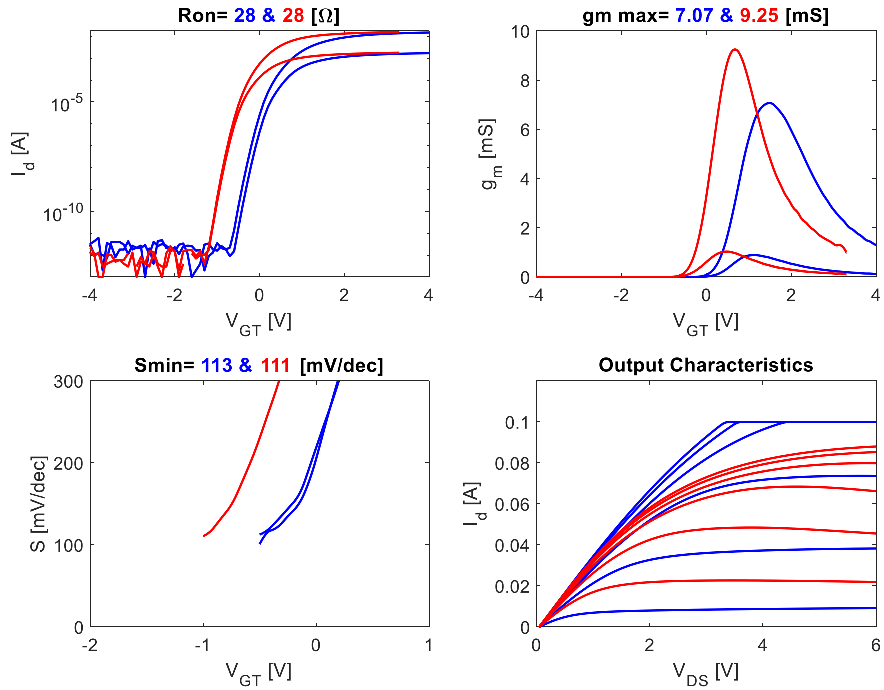


Figure 5-2 Transfer and Output curves of Type B device under 0.29% tensile strain (red) versus no strain (blue). Measurement conditions are same as Figure 3-3.

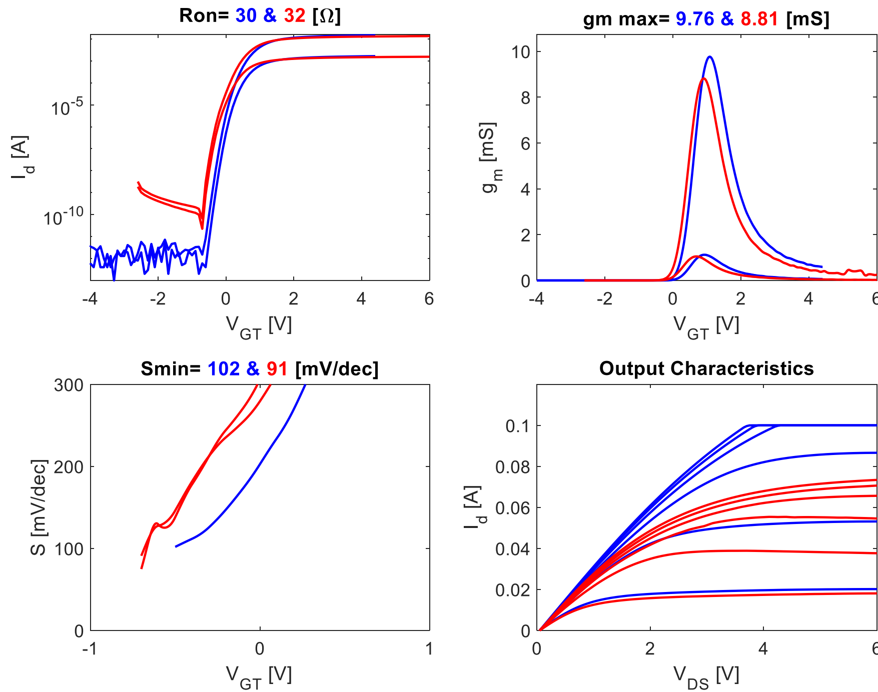


Figure 5-3 Transfer and Output curves of Type C device under 0.29% tensile strain (red) versus no strain (blue). Measurement conditions are same as Figure 3-4.

In all three transfer curves, despite the extreme thinning and the resulting bending, devices function fairly well. Comparing these curves to the typical device characteristics presented in chapter 3, we can see that there indeed tends to be a negative shift in threshold voltage with mechanical stress. While the behavior of transconductance and subthreshold swing is less clear, output characteristics show a constant drop in drain current across all devices for tensile mechanical stress. This is very likely due to problems during processing. Micrographs of typical device post processing shows a layer of iridescent film as well as burnt on photoresist residue that is thought to introduce significant contact resistance at high current values. There is great difficulty in making probe contacts on the thinned device. Abrupt contact often leads to microcracks in the [111] direction of the Si substrate that would sometimes render the device useless. These non-idealities coupled with device to device variations on electrical properties suggest a more definite investigation requires a statistical study.

Figure 5-4 summarizes the behavior of the transfer characteristic averages for all device types under mechanical stress. As predicted, in all three device types, the threshold voltage consistently shifts negative. In contrast, the behavior of transconductance and ON resistance is less clear.

Nevertheless, this definite threshold voltage change is indicative of 2DEG modulation under mechanical stress. We can now collect DC TDDB data to study the impact that 2DEG modulation and/or dielectric bond straining from mechanical stress have on dielectric reliability.

Device Type	ΔV_T (V)	Δg_m (mS)	ΔR_{on} (Ω)
Type A	-0.90	-0.17	5
Type B	-0.57	0.32	-0.4
Type C	-0.20	-0.69	2.7

Figure 5-4 Summary of transfer characteristics with mechanical stress from flat → tensile. Type A is an average of 15 devices each, Types B and C are averages of 4 devices each.

5.3 On-state TDDB under mechanical stress

First, we look at the gate leakage current change with mechanical stress on Type A devices.

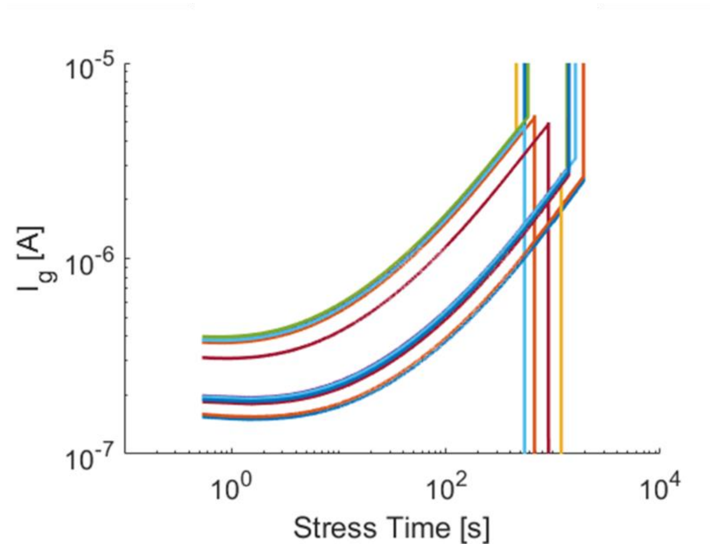


Figure 5-5 Gate current versus time for flat Type A devices under On-state conditions. V_{GS} = 128 V, V_{DS} = 0 V, V_{BS} = 0 V. Devices come from multiple dies.

Figure 5-5 shows the evolution of the gate leakage current for flat Type A devices under On-state conditions discussed in chapter 3. In the early stages of the experiment, there is a slight decrease in current, a characteristic signature of electron trapping in the AlGaN or dielectric that reduces the electric field across the gate stack [29]. As damage accumulates, there is an order of magnitude increase in leakage current (SILC) until the dielectric finally breaks down catastrophically. While

at hard breakdown, the gate current generally jumps up indicating the formation of an ohmic path across the dielectric, under On-state conditions in Type A devices we often see a collapse of the current. This is attributed to the device design where the gate is connected by a thin metal via to the pad. It is suspected that at hard breakdown the large energy dissipation is destroying this metal via, leading to the collapsed current. Indeed, micrographs reveal extensive damage for devices broken in this manner.

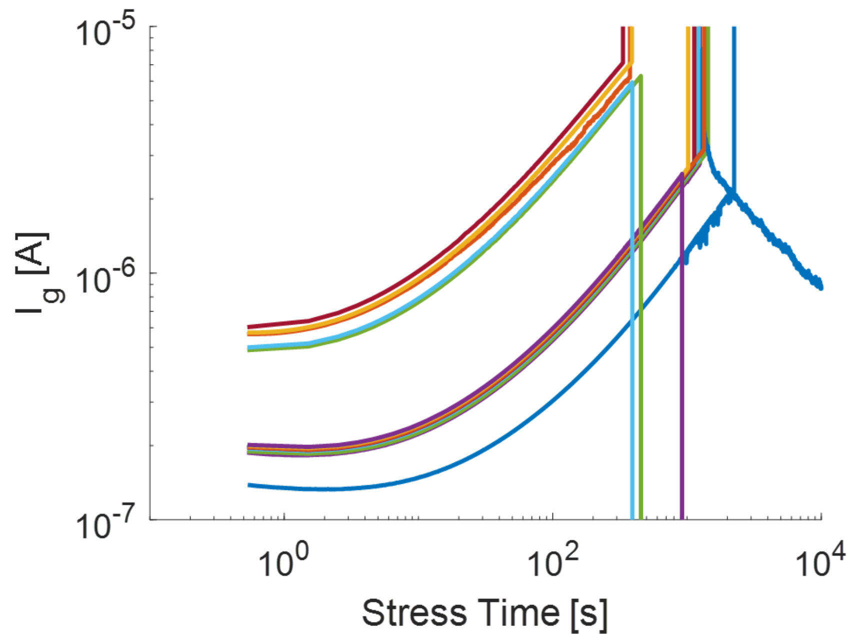


Figure 5-6 Gate current versus time for 0.29% tensile strain Type A devices under On-state conditions. V_{GS} = 128 V, V_{DS} = 0 V, V_{BS} = 0 V. Devices come from multiple dies.

When the devices are bent under 0.29% tensile strain, a similar behavior is observed (Figure 5-6). Here, we see a slight indication of trapping followed by SILC due to defect formation and ultimately hard breakdown. In both cases, there is large device to device variation both in initial gate leakage current and time to breakdown. This is due to the data being collected from multiple dies due to limited device availability per die. However, in addition to die to die variations, for On-state stress there is significant current variation within a die (Figure 5-7).

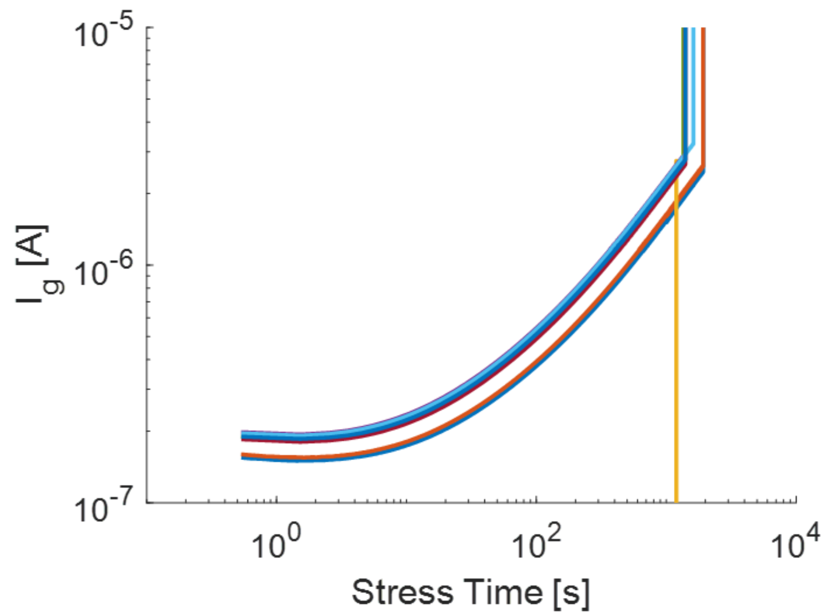


Figure 5-7 Gate current versus time for On-state stress conditions on unbent chip. V_{GS} = 128 V, V_{DS} = 0 V, V_{BS} = 0 V. Devices come from a single die.

Overlaying the gate current for tensile stress and no stress reveals that there is no discernible trend with mechanical stress (Figure 5-8). In fact, device to device variations are more significant than any change stemming from the change in mechanical stress.

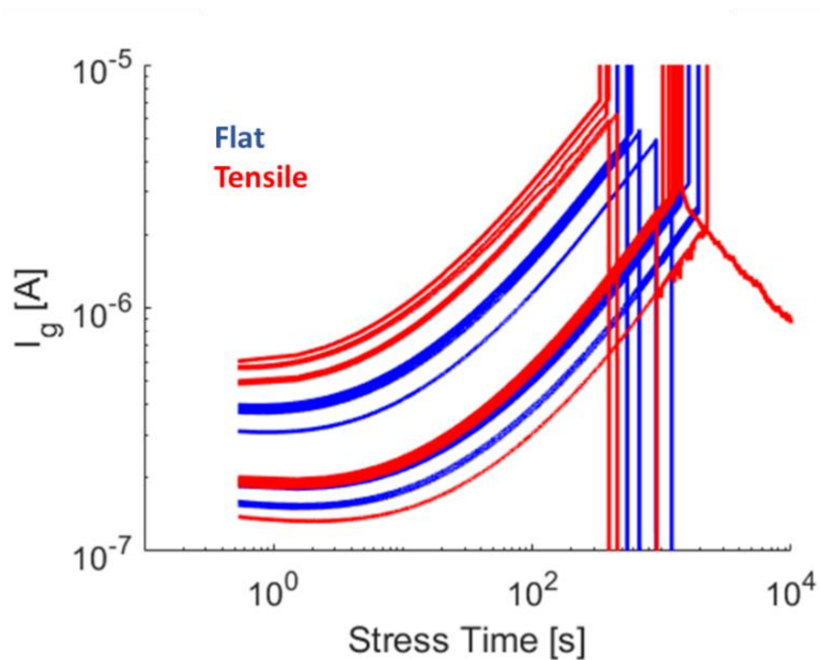


Figure 5-8 Gate current versus time for 0.29% tensile strain Type A devices (red) under On-state conditions versus unbent devices (blue). V_{GS} = 128 V, V_{DS} = 0 V, V_{BS} = 0 V. Devices come from multiple dies.

Plotting the hard breakdown times in a Weibull plot (Figure 5-9), we observe that there is no significant change for dielectric reliability in the On-state with mechanical stress.

The relatively large Weibull slopes of 1.92 and 1.64 indicate a tight grouping and a well-behaved breakdown distribution. The x intercept (y = 0) or $T_{63\%}$ of 1270 s for flat and 1221 s for tensile stress indicate very similar breakdown times. Therefore, we can conclude that even with this large tensile strain there is no change in On-state TDDB with mechanical stress.

The same behavior is observed for Type C devices. Looking at the TDDB failure plot in Figure 5-10, we see that despite the very small number of data points there is no observed drastic change in TDDB behavior.

The lack of On-state TDDB is contrary to literature results on HfSiON or SiO_2 on a Si system [32] [35] which shows dramatic (orders of magnitude) changes in TDDB with mechanical stress far less than our value of nearly 450 MPa. The changes in the above two dielectrics are attributed to either a strained dielectric bond or enhanced trap formation. Since there is no discernable change, we conclude that 2DEG modulation, strained dielectric bonds, and trap modulation do not impact TDDB for a SiN on GaN system.

It is still worthwhile to investigate Off-state TDDB under mechanical stress. Not only is the reverse biased condition more relevant to actual device application, the possibility of using UV illumination as demonstrated by Warnock [29] allows eliminating trap modulation as a variable. With UV illumination, we can focus TDDB change on just 2DEG modulation and dielectric bond straining.

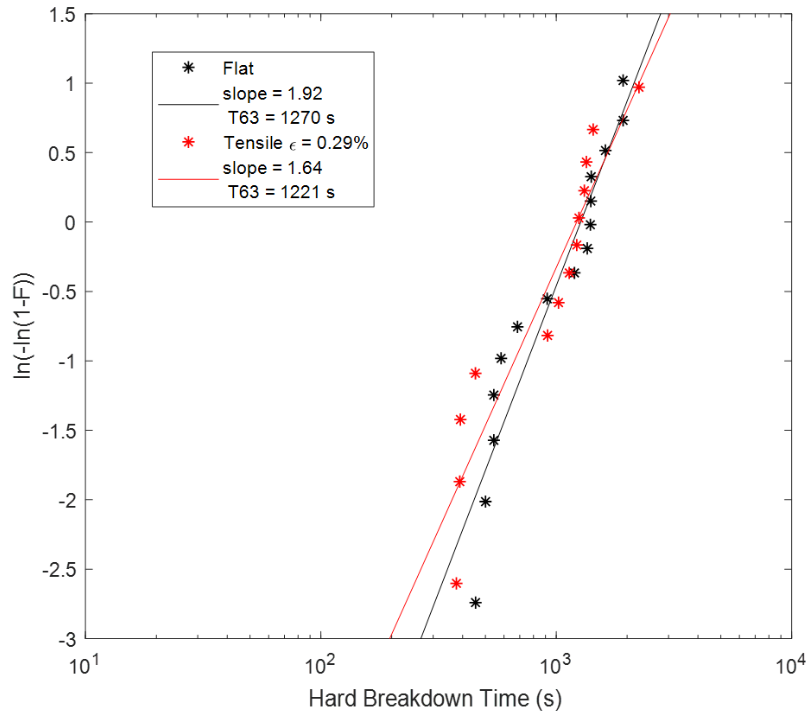


Figure 5-9 Type A device TDDB failure plot. V_{GS} = 128 V, V_{DS} = 0 V, V_{BS} = 0 V.

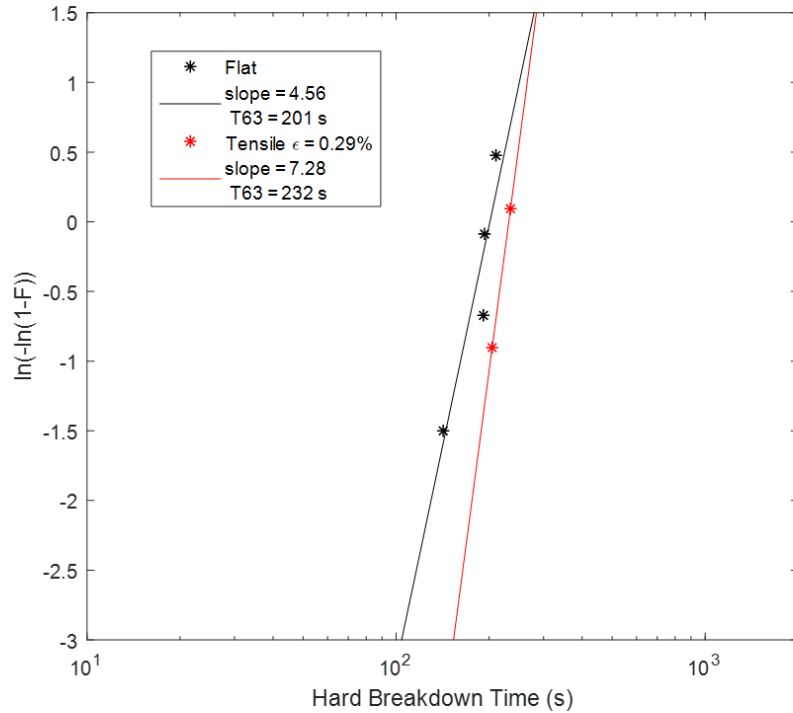


Figure 5-10 Type C device TDDB failure plot. V_{GS} = 24 V, V_{DS} = 0 V, V_{BS} = 0 V.

5.4 Off-state TDDB under mechanical stress

Before we carry out Off-state TDDB stress measurements, we must first verify that trapping effects are significant at this stress condition. To do this, following the approach in [29], we verify that application of UV light changes the breakdown voltage in Off-state (Figure 5-11).

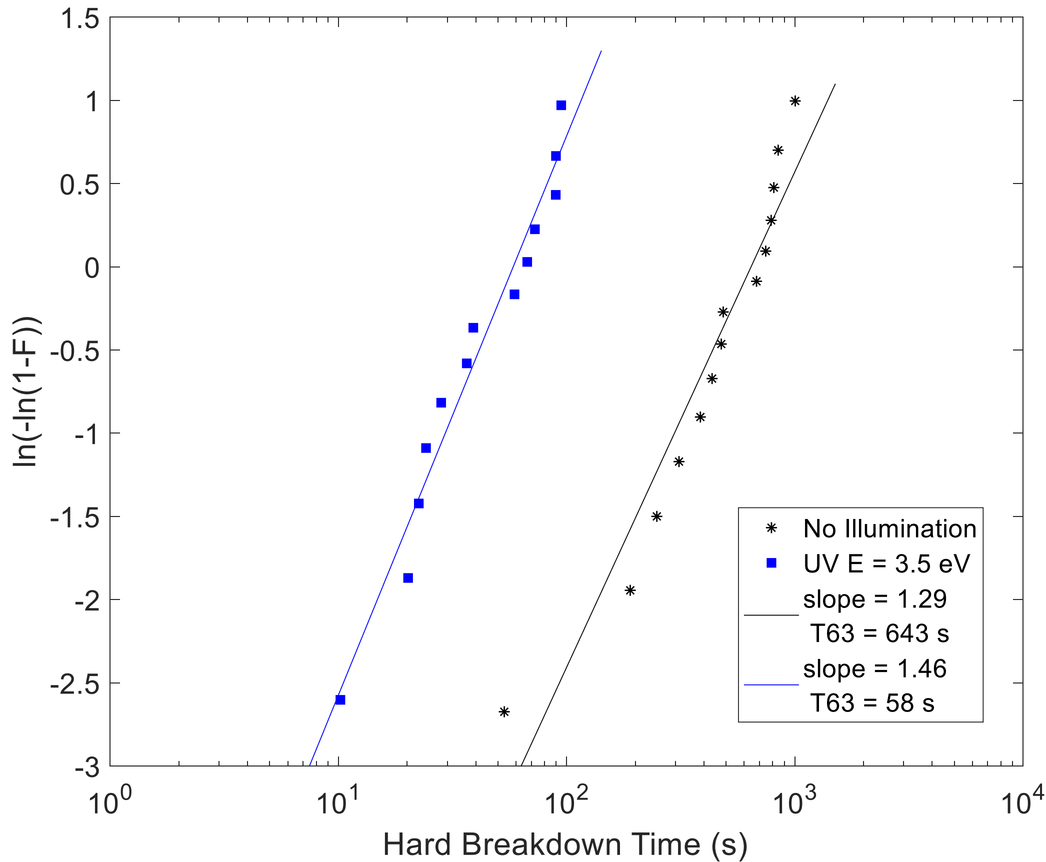


Figure 5-11 Unbent Type A device TDDB failure plot. V_{DG} = 325 V and V_{BS} = 0 V. Black is under dark, blue is under 3.5 eV UV illumination. Devices are interspersed between multiple dies.

Collecting the hard breakdown times for Off-state TDDB under dark and under UV at 3.5 eV, we can see that for identical stress conditions devices under UV illumination tends to break much faster. This is because electron traps can no longer weaken the electric field in the dielectric.

Furthermore, gate leakage currents between devices tested under dark and under UV illumination (Figure 5-12) show that devices under UV lack the current drop at the beginning of the experiment. This indicates that UV light is successful in continuously detrapping electrons. Consequently, the

electric field is stronger in UV illuminated device under the same voltage condition resulting in the measured SILC and faster breakdown.

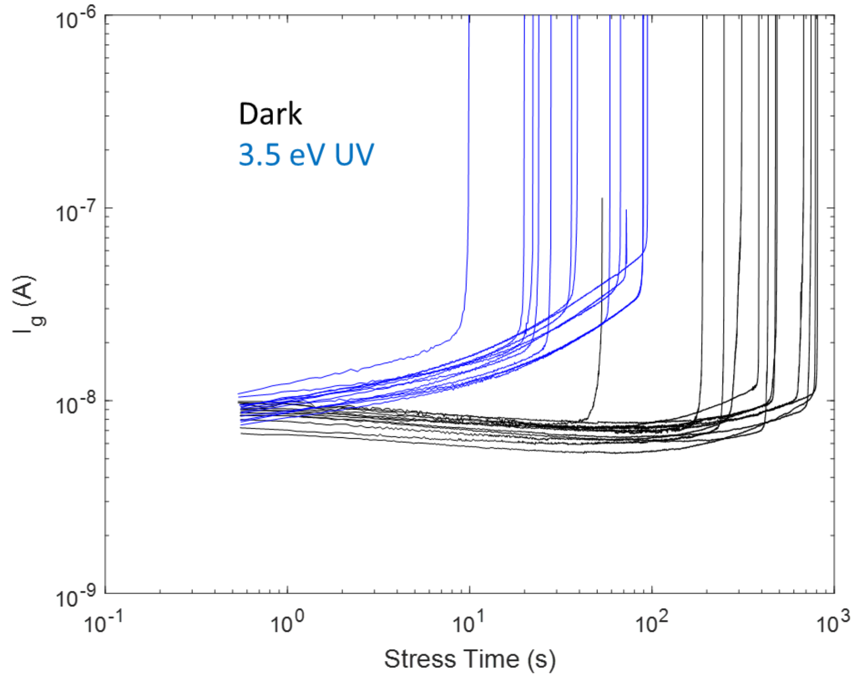


Figure 5-12 Gate current versus time for flat Type A devices under dark (black) and UV illumination (blue). V_{DG} = 325 V and V_{BS} = 0 V.

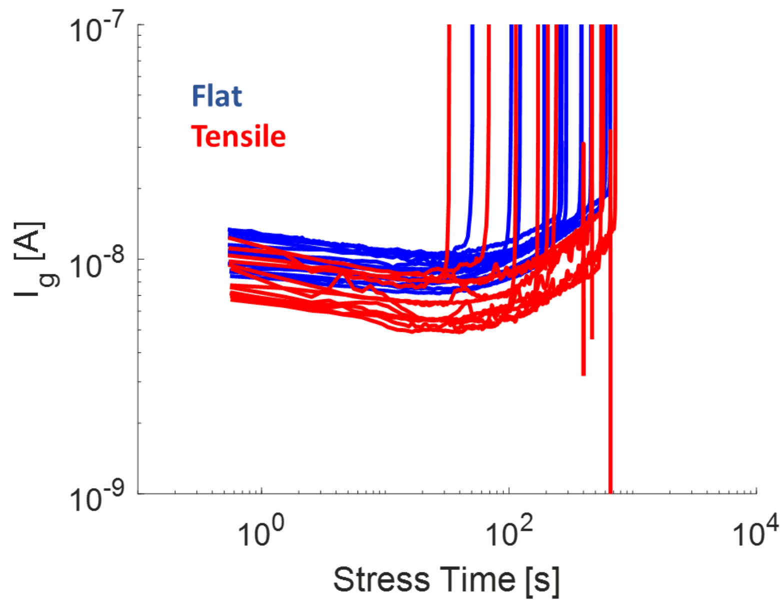


Figure 5-13 Gate current versus time for flat and tensile Type A devices. V_{DG} = 325 V, V_{BS} = 0 V.

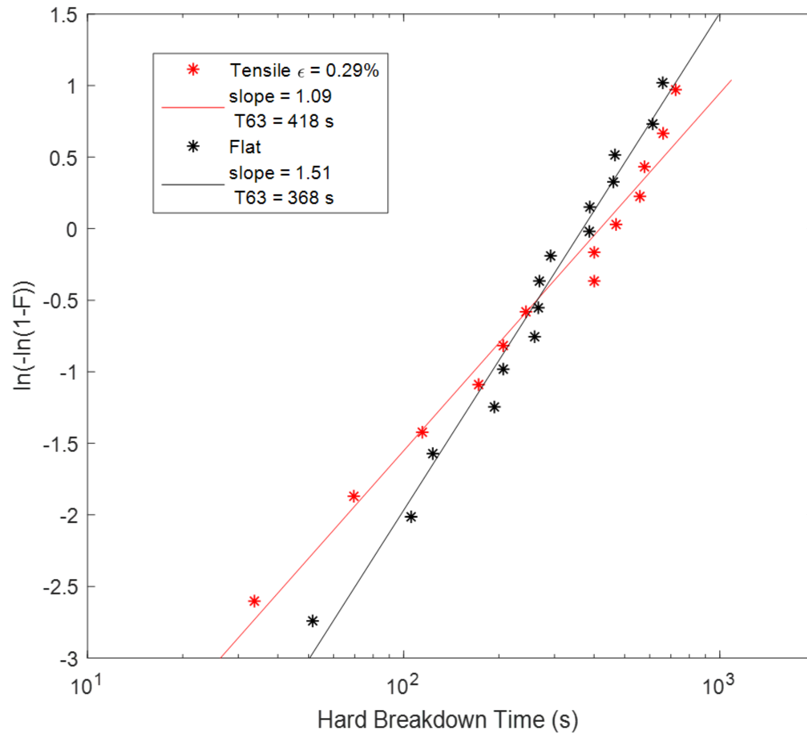


Figure 5-14 Type A device TDDB failure plot for flat versus 0.29% tensile strain under dark. V_{DG} = 325 V, V_{BS} = 0 V. Devices come from multiple dies.

In addition, gate leakage current plots show that any change that may be present is insignificant compared to device to device variation (Figure 5-13). Similar current levels through the entire experiment duration indicate that trap densities are not significantly changed by the application of mechanical stress.

Now that we have established UV illumination is able to detrap electrons successfully in Off-state, we can filter out trapping effects to study the impact of mechanical stress on TDDB due to the 2DEG and the dielectric bond straining. First, we report the Type A device TDDB failures for unbent and 0.29% tensile strain devices in Figure 5-14. There is again no significant change in the TDDB behavior. The combination of the 2DEG, trapping effects, and dielectric bond straining is shown to cause no change in TDDB behavior despite the large mechanical stress.

As UV has been shown to filter out trapping effects before, we can now do the same measurement but with under UV illumination. As Figure 5-15 shows, this again results in no change between flat and 0.29% tensile strain devices. Therefore, the combination of 2DEG change and dielectric straining causes no change in TDDB behavior with mechanical stress.

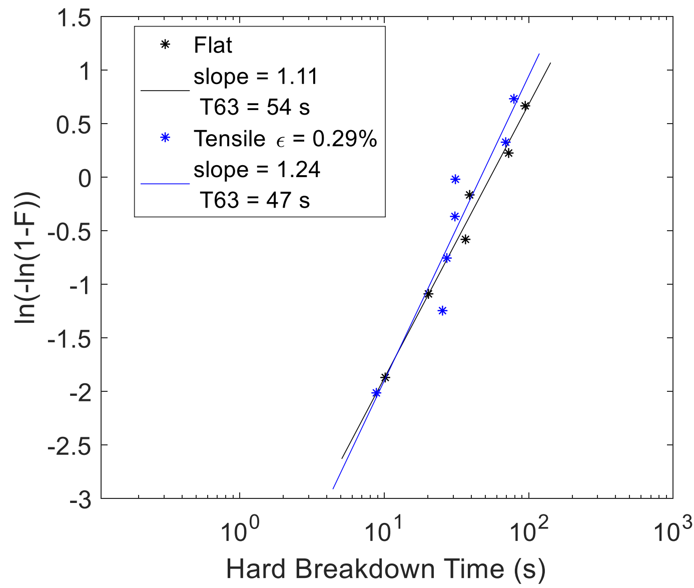


Figure 5-15 Type A device TDDB failure plot for flat versus 0.29% tensile strain under 3.5 eV UV illumination. V_{DG} = 325 V and V_{BS} = 0 V. Devices come from multiple dies.

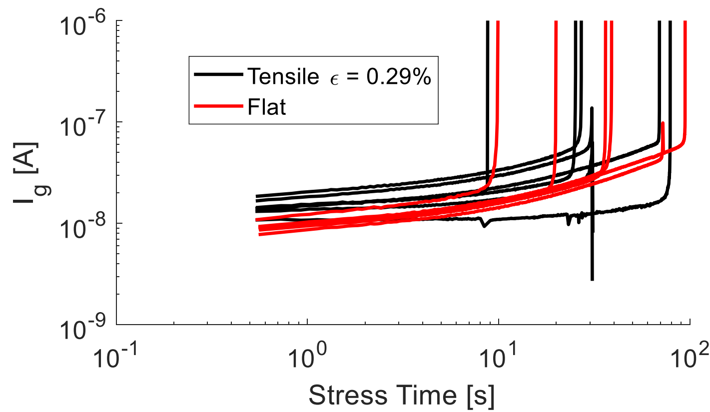


Figure 5-16 Gate leakage current for Type A devices in Figure 5-15. Devices come from multiple dies.

The gate leakage currents (Figure 5-16) for the devices in Figure 5-15 also paint a similar picture. There is no large change with mechanical stress. Instead, device to device variation is more noticeable. Due to the UV illumination, both stress conditions show no trapping effect.

As trapping effects are severe in Off-state TDDB gate leakage currents, we can leverage Off-state TDDB measurements in dark conditions to verify whether mechanical stress impacts trap occupation.

To see if trap occupation is affected by the application of mechanical stress, we use the method described by Joh in [7] to extract the relevant time constants that describe the decreasing gate

leakage current at the beginning of TDDB measurements. In essence, the method approximates the decreasing gate current as a sum of negative exponentials.

$$\boldsymbol{I_g = \sum_i a_i e^{-\frac{t}{\tau_i}}} \tag{5.3}$$

Computer calculation of the weights of each exponential, a_i, reveals that the timescales of note are unchanged between flat Type A devices and tensile Type A devices. In Figure 5-17, a positive amplitude implies that a_i is positive and therefore reflects a decreasing current. A negative amplitude reflects current increase through defect formation (SILC).

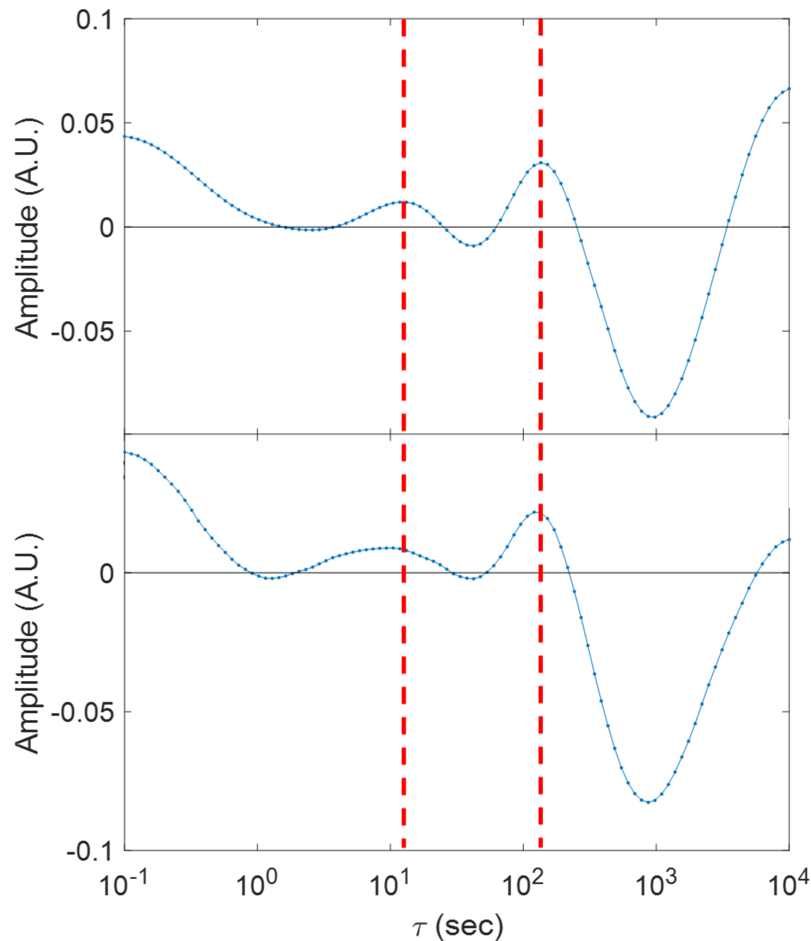


Figure 5-17 Amplitude of weights associated with each exponential for Off-state. Top, unbent Type A device. Bottom, tensile Type A device.

The relevant time constants, approximately 15 seconds and 150 seconds, are relatively unchanged with mechanical stress. Therefore, even trap occupation is unchanged with mechanical stress.

5.5 Summary

We find in this chapter that mechanical stress has no discernible impact on TDDB in both On-state and Off-state. While 2DEG is definitely changed with mechanical stress, its impact along with strain dielectric bonds appear to be minimal on TDDB. Furthermore, trap generation and occupation appear both unchanged with mechanical stress. These results are significantly different from reported results on different dielectrics in Si systems, demonstrating a more robust dielectric and/or substrate.

Chapter 6 Conclusions and Suggestions for Future Work

In this thesis, we characterized TDDB of GaN MIS-HEMTs under various stress conditions with two objectives in mind: 1. To verify whether measurements done under DC stress are accurate even though actual operation involves constant switching, and 2. To determine if TDDB in GaN MIS-HEMTs is sensitive to mechanical stress. We summarize our key findings and provide suggestions for future work here.

6.1 Conclusions

We find that On-state TDDB measurements done under DC stress conditions yield a conservative estimate. At low frequencies, there is very little change between AC and DC stress conditions to measure TDDB. However, as frequency increases past the 10 kHz range, AC stress conditions result in significantly higher hard breakdown times. As this frequency approaches operational conditions, the hard breakdown time improves by around a factor of two. Within the small range studied here, we find that the magnitude of the recovery voltage (voltage value at the low point of square wave) impacts the enhancement in the time to breakdown. Finally, we hypothesize that this improvement with increasing frequency is attributed to the difficulty of populating with electrons the dielectric/AlGaN interface under fast pulsed conditions.

We also find that both On-state and Off-state TDDB measurements under DC stress conditions are insensitive to adding tensile mechanical strain in the channel direction for strain levels below $\varepsilon = 0.29\%$. We see a definite modulation of the 2DEG that results in threshold voltage shifts upon the application of mechanical stress. By studying the gate leakage current evolution in the Off-state under dark, we find that mechanical strain does not significantly impact electron trap generation/occupation. Finally, Off-state TDDB measurements under UV exposure demonstrate that any modulation of the 2DEG or bond straining from bending in the dielectric does not change the overall TDDB behavior.

In conclusion we find that DC TDDB estimates are conservative with respect to actual operational use as it comes to the impact of AC pulsing and the application of mechanical strain. Therefore, lifetime extrapolations from DC stress experiments underestimate the time to failure under realistic operating conditions. This conservative approach to reliability predictions might result in an unnecessary trade-off with performance.

6.2 Suggestions for Future Work

There are several directions that can be pursued to further the understanding of the physics of TDDB in GaN MIS-HEMTs and to increase the confidence in the estimation of failure times. Here, suggestions for further work in both AC voltage stress and mechanical stress are listed.

1. Gate to channel capacitance measurements with increasing frequency can be found to determine if AlGaN conduction band population begins to be inhibited around the same frequency range observed for TDDB improvement under AC stress.
2. AC measurements can be collected at more frequencies to better plot the acceleration factor versus frequency plot. This will improve understanding of the transition frequency in which AC measurements begin to significantly outperform DC measurements in terms of hard breakdown time.
3. Drain to body breakdown with changing mechanical stress can be investigated. While no longer TDDB, drain to body breakdown is still a reliability concern that can change with mechanical strain. In an unthinned wafer, large stress is accumulated in the substrate/GaN buffer to prevent wafer warping. This stress can be mimicked with external mechanical stress.
4. TDDB change from mechanical stress applied transverse to the channel direction should be investigated.
5. Impact of compressive mechanical stress can be studied.
6. Gate current evolution with high frequency AC stress should be measured. Changes to trapping at beginning of stress, SILC, and gate current levels can shed more light towards why TDDB improves under AC.

7. High frequency capacitance measurements during AC stress can be investigated. For example, 4 MHz CV measurement while AC stress at 100 kHz can offer a direct investigation on how charges are reacting to the AC stress.
8. True AC TDDB where device is cycled between On-state conditions and Off-state conditions should be explored. This would offer the most accurate time to failure estimation.
9. Temperature dependence of the change between DC and AC stress conditions should be measured.

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