Miniaturization of Ac-Dc Power Converters for Grid Interface

by

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Abstract

In this thesis we present a two-stage ac/dc grid-connected converter for computer applications. Also known as off-line power supplies, these converters have to meet various demanding specifications such as a wide input voltage range (typically 0-376 V), large voltage step down (typical output voltages range from 12-48 V), harmonic current limits and galvanic isolation. The focus of this work is in the reduction in volume of ac/dc converters while keeping efficiency constant or improving it, which is challenging to achieve while meeting all the specifications. The thesis breaks down the converter in subsystems and explores architectural and topological trade-offs, modeling, component selection and control methods. The performance of each individual subsystem is experimentally verified.

The first stage of the converter is a step-down power factor correction (PFC) converter. This stage interacts with the grid and draws the necessary ac power from the line and rectifies it. Following the PFC is a capacitor bank, which is used to both buffer the ac power from the line and to provide hold-up energy to the output. The capacitor selection process is detailed in the thesis. The second stage of the converter provides isolation and regulation to the output. Two different approaches to the second stage converter are presented: using commercially available, "plug and play" converters and developing a custom converter. The full system is evaluated with both solutions and is compared to other state of the art converters. The final prototype achieves an efficiency of 95.33% at full power (250 W) and 230 Vac input, and a power density of 35 W/in^3.

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Chapter 1: Introduction

Due to historical reasons the transmission and distribution of electric power over the grid is done using ac waveforms. However, many of today's loads are electronic devices that require dc voltages, such as laptops, personal computers, mobile phones, and LED lights. Ac to dc converters are used to transform power from the grid to a form power useful for an electronic load. These converters, present in nearly all modern grid-connected electronic devices, tend to be a bottleneck in the miniaturization of electronics. Owing to the desire for miniaturization and the large amount of energy processed through such converters, decreasing their volume while maintaining or improving performance is a problem of present practical importance.

The two main types of power converters used today are linear and switching converters. Linear converters provide regulation by dissipating excess power. They are useful in low power applications (e.g. < 3 W) because of their simplicity and low noise output. In higher power applications their low efficiency becomes unacceptable. On the other hand, switching converters provide ideally lossless power conversion at the cost of higher complexity and size. This thesis focuses on the miniaturization of switching power converters, with a focus on isolated ac/dc conversion from universal input voltages to low-voltage dc outputs.

An important approach towards miniaturizing power converters is increasing the switching frequency of the converter [1]. The passive components of a power converter, such as capacitors and inductors, are used to store energy every switching cycle. The energy that needs to be stored each cycle is reduced by increasing the switching frequency of the converter, and - at least over some frequency range - the required size of energy storage elements is reduced. High frequency

circuits also enable higher control-loop bandwidth, faster response to transients and reduced size of input and output filters.

Despite the benefits of higher frequencies, there are a number of challenges that inhibit their use. There is a limit to how high the frequency can be increased before frequency-dependent losses become excessive. The main mechanisms of frequency-dependent losses include transistor switching losses, gating losses, magnetic core losses and magnetic winding losses (including skin and proximity effects) [1]. Likewise, sensing and control become increasingly difficult as frequency is increased. These factors are further constrained by the characteristics of available devices, components and materials and are heavily influenced by the selected power conversion architecture and topology.

In addition to switching frequency, there are many other factors that limit miniaturization of grid-interface power converters for single-phase systems. A chief one is the need for twice-line-frequency energy buffering and holdup in the face of power interruptions, as the energy storage needed to ride through line voltage crossings and/or provide holdup during line dropout is a function of output power and the line frequency, and doesn't depend on the switching frequency [2,3]. The wide operating range (in input voltage and power) required of ac-dc converters operating under "universal input voltage" requirements (e.g., 85 Vac-264 Vac) likewise makes it difficult to miniaturize converters for this application, as does the need to meet strict EMI constraints, meet ac line current waveform requirements for high power quality, and provide good thermal management for inevitable losses.

Achieving miniaturization demands designs that can address these challenges while mitigating high-frequency losses and which can best utilize available semiconductor devices, passive components and controls. This thesis explores new architectures and design approaches to increase the performance of universal-input grid interface ac/dc converters. Specifically, the thesis focuses

on design techniques for high power factor, high efficiency and high energy density single phase isolated ac/dc power converters in the range of hundreds of watts, such as suitable for computer power supplies and similar applications. The new topologies, circuits and controls considered are expected to contribute to substantial miniaturization and to permit improved performance in multiple applications.

1.1 Challenges and requirements of ac/dc converters

Single-phase power factor correction (PFC) converters in the hundreds of watts range typically need to meet the EN61000-3-2 Class D [4] harmonic current specification (shown in table 1.1), operate over universal input voltage and provide hold-up transient energy to the output. Meeting the EN61000-3-2 specification requires precise control of the converter input current in order to provide a waveform with low harmonic content. The "universal input" ac voltage range required for many such grid-interface converters is often defined from 86 to 264 Vac RMS which translates to instantaneous voltages between 0 and 372 V. This is a fairly wide input voltage range and it is difficult to make the converter operate efficiently at all operating points, particularly as a converter needs to operate over much of the line cycle to meet line harmonic specifications. Finally, such ac-dc converters take pulsating power and deliver constant dc power. There needs to be a place in the converter to buffer the inevitable twice-line-frequency power pulsations. In addition to this, ac-to-dc converters for computer applications are expected to be able to deliver full load power during a transient event in which the ac line is disconnected; a typical hold up time is one full line cycle (20 ms in the case of a 50 Hz ac input) at full output power. The converter needs to have an energy storage element to provide said energy and this usually takes a substantial amount of overall converter volume.

Table 1.1. EN61000-3-2 Harmonic current requirements for Class D equipment (such as single-phase ac-input computer power supplies over 75 W) [4]

Harmonic order *n*	**Maximum permissible harmonic current per watt mA/W**	**Maximum permissible harmonic current A**
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
13 < n < 39	3.85/*n*	0.15*15/*n*

Power converters for applications such as computers are also required to provide galvanic isolation and electromagnetic interference (EMI) filtering and meet stringent efficiency standards (e.g. 80 Plus [5]). Galvanic isolation is needed both to meet grounding requirements and for protection of the user in case of an electric power surge, such as caused by lightning striking the power line [6,7]. Switching converters have the potential to produce substantial EMI and thus EMI injection into the grid needs to be strictly limited [8,9], and output filtering is often likewise required, each of which can add substantially to converter volume. Market efficiency standards, such as the 80 Plus requirements for computer power supplies, are increasingly of interest to decrease energy waste. As an example, Table 1.2 illustrates that a computer power supply can be certified 80 Plus Platinum if, with an input of 230 V ac, it has an efficiency greater than 90% at 20% load, 94% at 50% load and 90% at 100% load, and operates with a power factor greater than 0.9 at 50% load. Simultaneously meeting all these requirements while achieving high power density is a challenge [10-12].

Various designs found in the literature and commercially [13-18] meet the aforementioned specifications while achieving various levels of performance in terms of efficiency and power

density. Figure 1.1 shows a scatter plot of full-load efficiency vs power density for these sample designs. These designs have similar design specifications to the one prototyped in this thesis. One can see a trade-off between efficiency and power density. The observed trade-off is reasonable because in general having bigger components (e.g. FETs, board traces, windings, etc.) can be used to reduce conduction loss and magnetic core loss. Of note is that converter [14] is 80 PLUS platinum certified. Table 1.3 shows the individual converter data that was used to generate Fig. 1.1.

Table 1.2. 80 PLUS certification requirements for computer and server power supply units [3]. Redundancy is typically used in data centers.

	115V Internal Non-Redundant				**230V Internal Redundant**			
% of Rated Load	**10%**	**20%**	**50%**	**100%**	**10%**	**20%**	**50%**	**100%**
80 PLUS	---	80%	80%	80% / PFC 0.90	---	---	---	---
80 PLUS Bronze	---	82%	85% / PFC 0.90	82%	---	81%	88% / PFC 0.90	81%
80 PLUS Silver	---	85%	88% / PFC 0.90	85%	---	85%	90% / PFC 0.90	85%
80 PLUS Gold	---	87%	90% / PFC 0.90	87%	---	88%	92% / PFC 0.90	88%
80 PLUS Platinum	---	90%	92% / PFC 0.95	89%	---	90%	94% / PFC 0.95	91%
80 PLUS Titanium	90%	92% / PFC 0.95	94%	90%	90%	94% / PFC 0.95	96%	91%

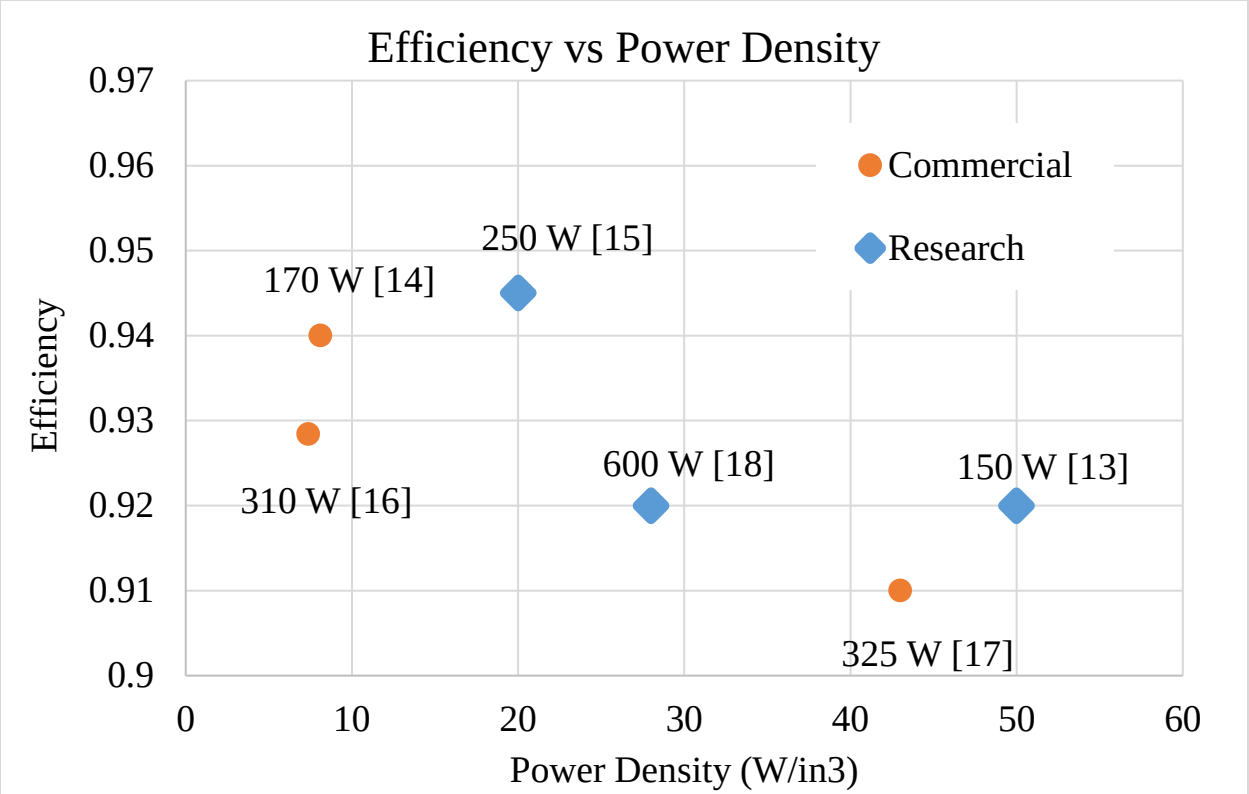


Figure 1.1. Full load **e**fficiency vs power density for different converters.

Table 1.3. Data from various converters, both from research and commercial. This data was used to generate the plot in Fig. 1.1. The densities with stars are estimated as a value was not presented in the publication.

	[13]	**[14]**	**[15]**	**[16]**	**[17]**	**[18]**
Output Power (W)	150	170	250	310	325	600
Density (W/in^3)	50	8.1	20*	7.381	42.97	28
Efficiency	0.92	0.94	0.945	0.928	0.92	0.92
Output Voltage (V)	12	12	48	28	24	24
Universal Input	yes	yes	yes	yes	yes	yes

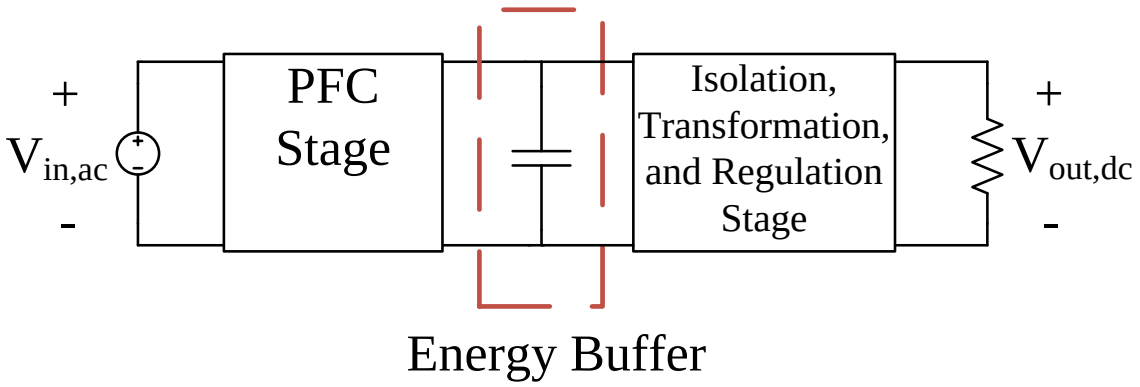


Figure 1.2. Typical architecture for a two stage, single phase ac/dc converters

1.2 Typical ac/dc converters

Ac/dc converters broadly address two challenges: (1) drawing energy from the ac line with acceptable waveform quality while providing sufficient energy buffering to handle line zero crossings and holdup requirements, and (2) providing isolation, voltage transformation, and regulation of the dc output. There are two main types of circuit architectures used to solve this problem: single-stage designs, e.g. [19-21], which accomplish both of these functions with one power stage, and two-stage designs [22-24] which split these functions up among multiple stages. (There are also design variants that are somewhere in between a single stage and two full cascaded stages, such that one of the stages does not process all the power (e.g., [22]) but for purposes here we'll treat such designs as two stage designs.) Single-stage converters typically have fewer components and the design and control schemes are simpler [10,12]. Power is only processed once, but the energy processing limits of single-stage designs tend to hurt their achievable performance (e.g., in terms of waveform quality, volume, etc.). On the other hand, the two stage approach provides more flexibility and control handles that enables system-wide tradeoffs which can result in high-performance converters. In this type of converter, power is processed twice, so it is imperative that the tradeoffs are well understood and the components and topology carefully

selected so that the circuit offers an overall increase in performance. Broadly speaking, single-stage designs are most often found in low-power systems where component count tends to drive cost and performance requirements are somewhat relaxed, while two (or more) stage designs are dominant in high-power and high-performance systems.

In this thesis a two stage PFC circuit architecture is explored that is suitable for high-frequency (multi-MHz) operation while providing high efficiency and power density. Figure 1.2 shows a simplified view of the general architecture of the converter. The front end is the power factor correction (PFC) stage that manages drawing energy from the line with high waveform quality and providing energy buffering for twice-line-frequency ripple and holdup. The 2nd stage is an isolation and regulation stage that provides voltage step down, galvanic isolation, and regulated control of the output. The energy buffering capacitors are placed between the two stages.

1.3 PFC stage

The PFC stage is typically the front end of an ac/dc converter. Its main purpose is to extract current from the line at high power factor, making the ac/dc converter look close to a resistive load. Because the line voltage is sinusoidal, a perfect power factor of 1 is achieved if the current drawn is also sinusoidal and in phase with the voltage (i.e., the converter looks like a resistor to the line). However, international standards for computer power supplies such as EN61000-3-2 [4] and 80 PLUS [5] allow for some harmonic content. The "relaxed" constraints enables the use of distorted (non-sinusoidal) current drawn from the line, which in turns gives the designer a variety of options in topology and control scheme selections. [10, 12, 22, 25]. In particular, the ability to draw some degree of harmonic currents allows reduction in the required energy storage for twice line frequency buffering, permits a broader range of topologies to be used (e.g., ones that may not be able to draw current over the full line cycle), and provides greater flexibility in control.

In typical commercial ac/dc converters the PFC stage consists of a line-frequency rectifier followed by a boost-type converter [10,12,26] or a "bridgeless" design in which the boost converter is integrated with the rectifier [11,19]. This converter has several useful characteristics: it has one magnetic component, it has a common-referenced switch, and, most importantly, it can operate to draw current from the line over the full line cycle. In short it is a very popular topology because of its low component count, simple control scheme and high power factor. One drawback of the boost-type PFC is the high output voltage, which must be higher than the peak input voltage (i.e. higher than 373 V in an universal input design). This requires switches and energy storage at the output that is rated for relatively high voltage compared to the ultimate output voltage of the system. Moreover, operating at this high output voltage will also increase the step down ratio of the second stage, which hurts its achievable size and efficiency. On the other hand buck-type PFC converters [10,12,23] offer the opposite trade-offs: lower device stress and lower second stage step-down ratio but also lower achievable line waveform quality and power factor, as such a PFC stage can only operate over the parts of the line cycle where the instantaneous line voltage is higher than the output voltage of the PFC stage. Other types of converters (e.g., flyback or buck-boost stages) can split this difference, providing intermediate characteristics [23, 26], though some such designs can impose quite high stresses [19,27].

1.4 Energy buffering capacitors

Energy buffering for twice-line frequency power pulsations and holdup is usually accomplished with capacitors, as other energy storage forms typically yield some combination of larger volume, higher cost and/or worse efficiency, with high-voltage electrolytic capacitors dominating this space. Nevertheless, such capacitors can take up to 30 to 40 % of a high-power-density ac/dc converter’s total volume. Their size is determined by three constraints: the energy

that needs to be stored and delivered every half line cycle, the energy needed for hold-up time requirements and the temperature rise due to the current flowing through it. In single-phase ac/dc converters the input power drawn from the line is necessarily pulsating while constant power is delivered to the load. As illustrated in Fig. 1.3, energy is stored when the instantaneous input power drawn from the line is higher than the output power and this energy is then delivered when the output power is higher than the instantaneous input power. The element (usually a capacitor) that provides this intermediate energy storage is this energy buffer. Because energy is typically stored and delivered two times in a line cycle, this process is called twice line-frequency energy buffering. The amount of energy needed, the allowed ripple on the capacitor voltage and the average capacitor voltage all affect the sizing of the capacitors.

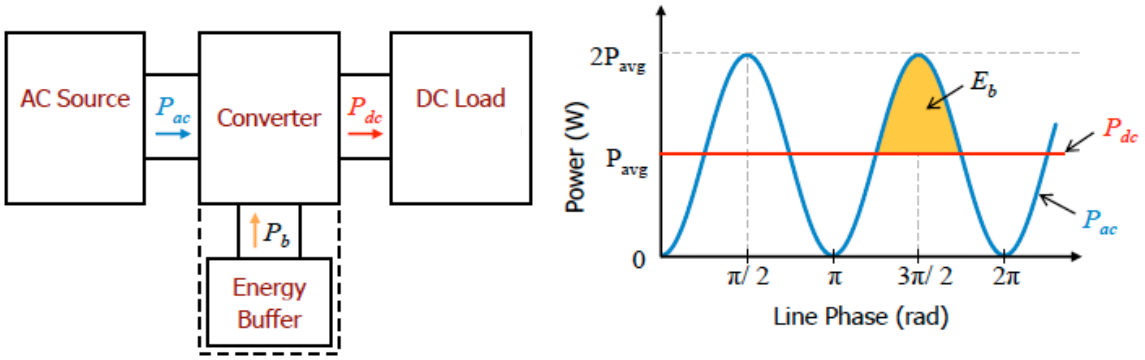


Figure. 1.3. Energy buffering in single phase ac to dc converters. Waveform on the right shows the case of unity power factor, where the peak power processed by the circuit is twice the average power delivered to the load.

Hold-up time also affects capacitor size. Hold-up time is the time the ac/dc converter needs to deliver (typically full) output power with the ac input disconnected. This is a transient event (e.g., typically associated with short line faults or brownout) and is a specification that many power supplies, especially those powering computers or servers, need to meet. The idea is that if there is a temporary dropout on the line voltage then the load will not be affected, or if there is a supply cut-off then this gives time for an uninterruptible power supply to take over the supply demands.

The capacitor energy requirement can be summarized as follows: for a given converter design the capacitor energy requirement will be dominated by either line energy buffering or hold-up time. Finally, all capacitors have equivalent series resistance (ESR) which will dissipate power as heat, imposing an RMS current limit on the capacitor for steady-state (twice line frequency) buffering.

1.5 Isolation and regulation stage

The second stage in Fig. 1.2 takes the energy from the first stage (including the energy buffer) and delivers it to the output. Typically this would be done with a step-down isolated dc/dc converter. The converter provides regulation of the output voltage and incorporates a transformer that provides isolation [6,7]. (Capacitive isolation is possible [28,29], but not generally favorable for volume or efficiency, and the transformer also helps to provide necessary voltage transformation.) The converter should also be able to handle a range of input voltages corresponding to that provided from the PFC stage during a hold-up time transient event.

1.6 Thesis Outline

In the following chapters, details about the particular 2-stage conversion architecture explored in this thesis will be discussed along with the design approach for the proposed system. Chapter 2 offers a high-level overview of the system, and explains trade-offs and the reasoning behind the chosen topology and architecture. This chapter also explores how each subsystem improves system-level performance: extract power with high power factor, increase converter efficiency and reduce converter volume. The selection of the PFC stage, its operation and key elements are detailed here too. Chapter 3 focuses on the building block of the PFC power stage, the resonant-transition inverter buck converter. Operation, modeling, component selection and performance

evaluation are the focus of this chapter. Chapter 4 talks about the selection criteria for the energy buffering capacitors, and also offers a study on the usable energy density of commercially available electrolytic capacitors. The selection of the energy buffering capacitor is a vital part of our design, as not only it affects converter volume but also sets constraints on the power factor, line harmonics, PFC stage output voltage and second stage step-down ratio and device rating. Chapter 5 describes one possible implementation of the second stage: using commercially available, "plug and play" converters that provide regulation and isolation. Various converters are analyzed based on datasheet values and full system performance is evaluated with the highest performing converter. Chapter 6 proposes a custom second stage converter that is believed will outperform the commercially available ones. Details on operation, component selection, topological variants and performance evaluation are shown here. This custom converter is designed to provide very high efficiency at a nominal input voltage, but is also able to work transiently over a wide input voltage range during a hold-up time event. Chapter 7 focuses on improvement of the light-load efficiency of dual active bridge (DAB) converters. A model is developed and is used to create a control law that improves light-load efficiency. Chapter 8 details the full system performance of the prototype using the custom converter. This chapter also includes various incremental improvements to the system and a comparison with state of the art converters found in literature and commercial ones. Finally, Chapter 9 concludes the thesis.

Chapter 2: Single-Phase Two-Stage PFC Converter Overview

As was described in the previous chapter, a two-stage architecture is selected for developing our miniaturized ac/dc converter. Many architectural approaches were considered; an analysis and trade-off evaluation between the different approaches will be described in detail in this chapter.

2.1 PFC Stage

A general approach to reducing converter size is to increase the switching frequency. To realize a multi-MHz switching converter that operates with a high input voltage (e.g. 372 V from the grid), it is imperative that soft switching techniques are implemented. Zero voltage switching (ZVS) capable converters typically use the circuit inductance to resonate with the device capacitance to allow the switch to turn on at a lower voltage (ideally zero). This resonant event is an important part of the switching cycle period, and the speed of the resonance is related to the natural frequency ($\omega_O = \frac{1}{\sqrt{L*C}}$) of the device capacitance C and the circuit inductance L and to the characteristic impedance of the resonance ($Z_O = \sqrt{\frac{L}{C}}$). By consequence, for a fixed characteristic impedance both L and C have to be reduced simultaneously in order to increase switching frequency. In increasing the resonant frequency, the first constraint that is hit will be the device capacitance C. The value of C is limited by size of the device needed to carry the circuit currents. Moreover, typical off-line converters operate with high input voltage and relatively low input current which tends to make characteristic impedance high for typical topologies, and in turn limits how much the value of

inductance L can be reduced.

One way to make a significant improvement in frequency is to use a (*i*) circuit architecture that enables reduced circuit voltages (and characteristic impedances) such as using stacked converters and (*ii*) associated topology that features a relatively low required characteristic impedance (i.e. the resonant, ZVS converter operates with a smaller voltage than the ac input, and furthermore has relatively high ac current for a given voltage). In the next sub-sections we will cover these approaches in detail.

2.1.1 Converter-stacking architectures

Converter stacking architectures can be used in various ways to the designer's advantage. Power converters with stacked inputs have often been used when dealing with high input voltages. For example, in [22,30]. Indeed some designs explicitly use modules with series stacked inputs and parallel outputs in order to reduce voltages on individual modules and effect voltage transformation. This technique is useful in reducing subsystem characteristic impedance, modifying transformer turns ratio, utilizing lower voltage devices, reducing CV^2 energy stored in device capacitance and many other applications. Other converters such as multi-cell converters [31] and single stage point-of-load converters (POL) [32] also utilize input series output parallel (ISOP) configurations.

For our system, the idea is to use a stacking converter architecture to reduce the required characteristic impedance of each converter. Figure 2.1 shows an example of converter stacking in a grid-connected application. In this configuration, the converters will split the input voltage equally between them (i.e. 0-186 V at the input port of each dc/dc converter if connected to a 240 Vac line, or 0-93 V if connected to a 120 Vac line). However, it is difficult to design the converters

to operate efficiently over both sets of input voltage. A reconfigurable input would mitigate this effect, making the range of input voltage the same whether the input is 120 Vac or 240 Vac. Lastly, depending on the topology of the converter the outputs can be connected in series, in parallel or can be kept as two separate outputs. If left as separate outputs the converter will store energy in two sets of energy buffering capacitors, otherwise only a single capacitor bank is needed.

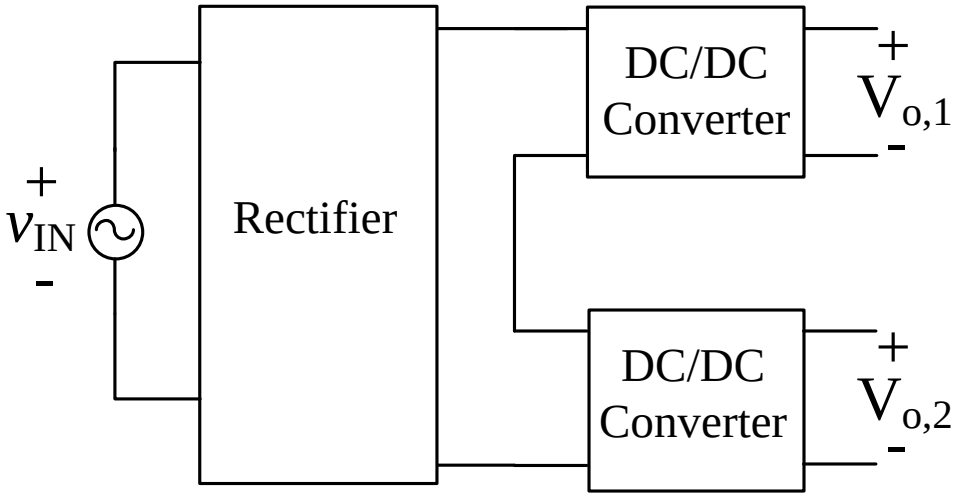


Figure 2.1. Diagram showing a possible PFC stage with two converters with their inputs stacked in series and each with their own output. This configuration thus reduces the operating voltage of each converter but one must manage multiple outputs (and potentially multiple places to store twice-line-frequency energy). Depending on the specifics of the design, the two outputs can be connected in series, parallel or kept separate.

2.1.2 Low characteristic impedance topologies

Topologies with low characteristic impedance are those with low inductance and/or high capacitance. Because we want to operate at high frequency, we have to minimize the L and C product. Thus the topologies we are interested in are the ones with low inductance and high inductor current ripple, which enable minimum-sized magnetics. In these category are the well-known discontinuous conduction mode (DCM) family of topologies and resonant-pole-based topologies. The resonant-pole-based topologies [33,34,35] are synchronous converters that

maintain ZVS using the inductor current ringing. However the added complexity of controlling multiple switches synchronously at megahertz frequencies (plus the additional component count) was deemed unfavorable for this design. On the other hand, there are various single-switch topologies that operate in DCM and would be useful for this application [36,37]. In DCM topologies one gets guaranteed ZCS at turn on but only gets ZVS if specific conditions are met. One has to deal with the voltage across the switch ringing naturally, and whether it makes it all the way to zero depends on circuit parameters.

A very high performance soft switching DCM dc/dc converter topology suitable for this application is the resonant transition inverted (RTI) buck converter, shown in Fig. 2.2. This converter's waveforms are very similar to those of the "Quasi-Square-Wave" ZVS buck converter [36]. This is a variable-frequency converter that can operate on the multi-megahertz range with a single grounded switch. The active switch having its control signal referenced to a fixed potential greatly simplifies the driving circuitry, which can be a limiting factor in driving circuits at megahertz switching frequencies [1]. This converter, like many other ZVS topologies, has a limited operating range that guarantees soft switching. In this case, ZVS (or near-ZVS with acceptable losses) is maintained for up to ~2.5:1 input-to-output step down conversion. This means that for a peak input of 186 V, ZVS can be achieved if the output voltage is ~75 V. This topology has been used in previous designs as part of a step-down PFC converter [22] and as a regulator [37].

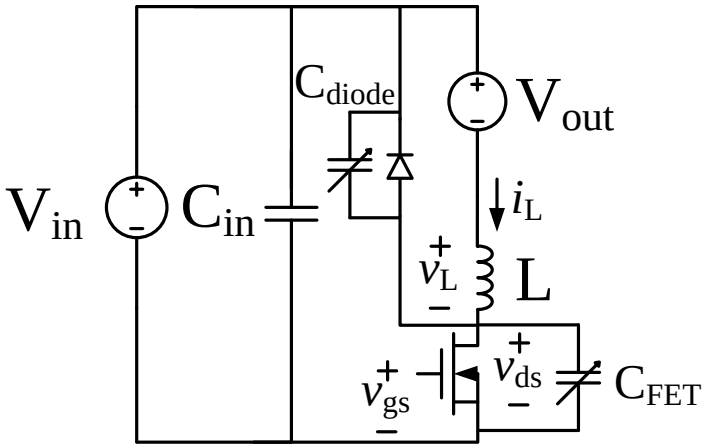


Figure 2.2. Resonant transition buck converter. This particular implementation is the inverted version. This is a candidate topology for the dc/dc converter used as the PFC building block. More details found in Chapter 3.

2.1.3 Step-down PFC

Boost-type PFCs are the most widely-used PFC converter. They are well regarded because they can operate over the complete line cycle (providing ideally unity power factor) and they have a single switch referenced to ground. On the other hand, buck PFCs [38-41] cannot operate over the complete line cycle (only during the portions where the instantaneous input voltage is larger than the output voltage), thus adding distortion to the line current. However, if properly designed this distortion is acceptable under the EN6100-3-2 standard. An advantage of the buck PFCs is that they provide "help" in the system-wide step-down conversion which can be leveraged to improve the design of the second stage, while the boost PFCs increases the voltage to about ~400 V and the second stage has a larger step down. A larger step-down ratio typically leads to poorer efficiency. Finally, the RTI buck topology has a switch referenced to a stable voltage, minimum sized inductor due to the high current ripple and ZVS over a reasonable input voltage range. For all these reasons, a step-down PFC using the resonant transition buck converter is selected as the main power stage of the front end. Component selection, performance evaluation and other details of the RT buck are found in Chapter 3.

A last note on the step-down PFC is the relationship between achievable power factor and converter output voltage. Figure 2.3 shows the typical waveforms of line current and voltage in a buck PFC, where current does not start flowing until the line voltage reaches the value of the buck converter's output voltage. From this waveform, an expression relating the power factor with the angle ϕ (when conduction starts, in radians) can be derived:

$$p.f. = \sqrt{\frac{\pi - 2\phi + \sin(2\phi)}{\pi}} \quad (2.1)$$

Lastly, we can relate the angle ϕ to the converter output voltage by the following equation:

$$\phi = \arcsin\left(\frac{V_O}{V_{PK}}\right) \quad (2.2)$$

Figure 2.4 shows a plot of the power factor as a function of ϕ, while Fig. 2.5 shows the power factor as a function of converter output voltage. For an output voltage of ~75 V, the expected

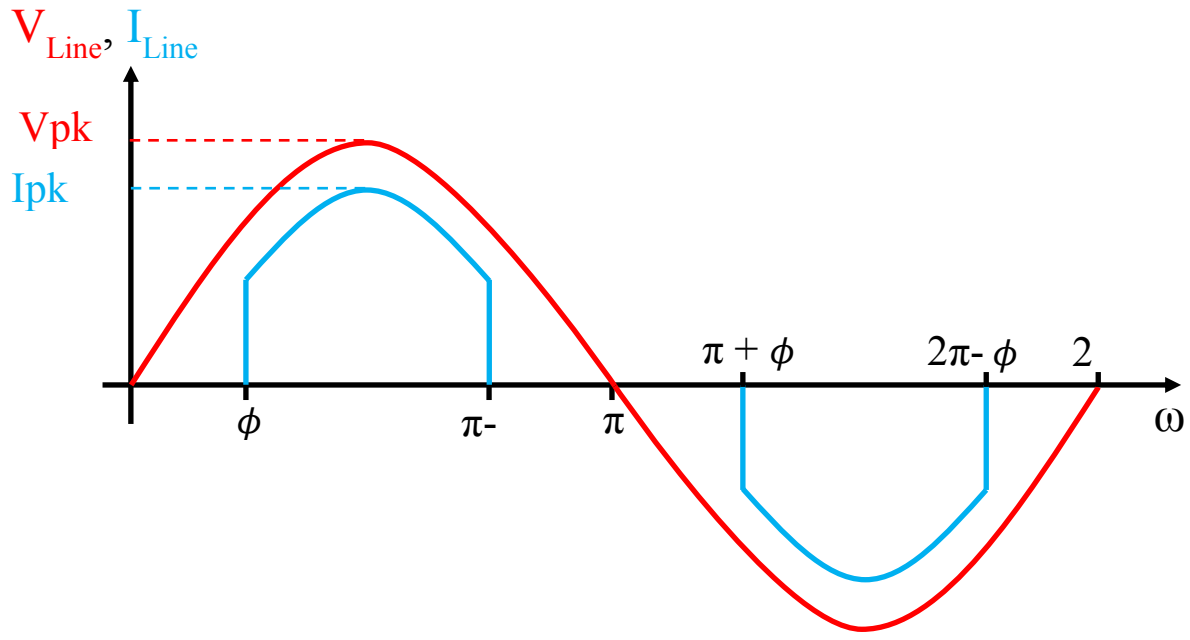


Figure 2.3. Typical line voltage and current for buck PFC. At the angle ϕ the line voltage reaches the output voltage of the buck converter and conduction begins.

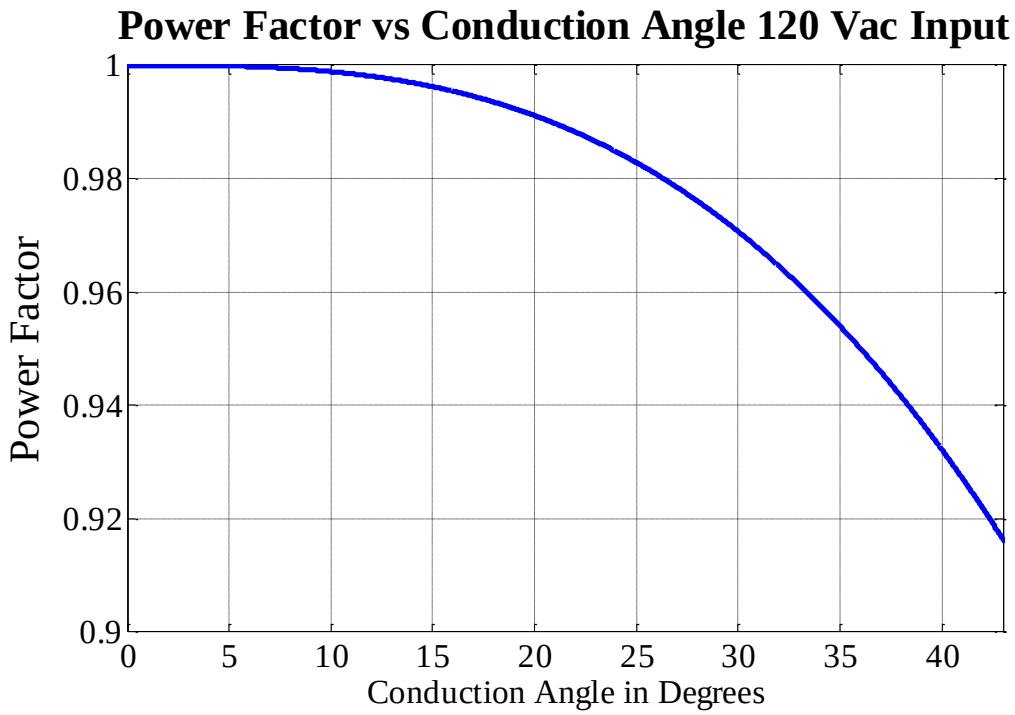


Figure 2.4. Power factor at the ac input port of a buck PFC as a function of conduction angle ϕ. The input is 120 Vac.

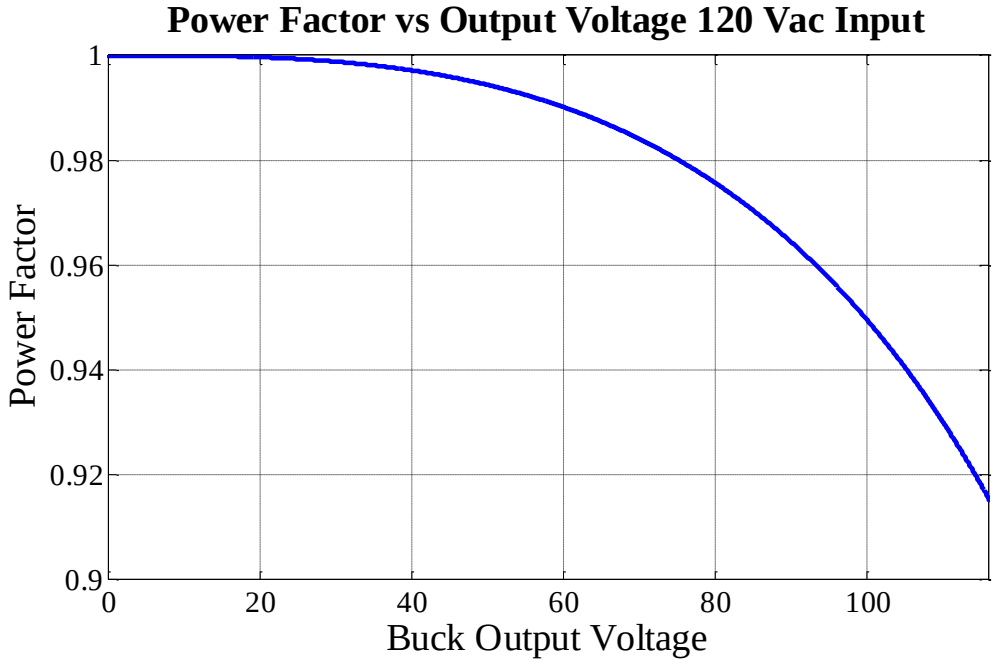


Figure 2.5. Power factor at the ac input port of a buck PFC as a function of buck converter output voltage. The input is 120 Vac.

power factor is above 0.97. This is a reasonable power factor with little harmonic content. In conclusion, if we fix the outputs to ~75 V per converter (which means their input voltage range is 75 to 186 V when stacked) we gain two benefits: >0.95 power factor and guaranteed ZVS (or near-ZVS) over the complete input voltage range.

2.1.4 Reconfigurable inputs

A key consideration in "universal input" power converters is the very wide input range, and the fact that there are multiple broad ac voltage ranges that one must operate under: 100 Vac / 120 Vac (in Japan and the US) and 240 Vac (in Europe). (Furthermore, one must typically operate down to 15% of nominal line voltage and up to +10% of nominal line voltage, giving an "overall" input range of 85 - 264 Vac rms.) This wide range imposes a significant design penalty on most converters that limits achievable frequency and miniaturization, as one is forced to operate at both "high voltage/low current" and "low voltage / high current" conditions. This wide range hurts design from multiple perspectives: one must over-rate switches and components in both current and voltage, one must seek topologies that can provide high-efficiency operation (e.g., ZVS switching) over much wider input ranges and conversion ratios, and one must be able to realize controls that address these different operating ranges. For example, with the architecture shown in Fig. 2.1, the peak input voltage of each dc/dc converter nominally would be 186 V with a 240 Vac input (e.g. European voltages) and 93 V with a 120 Vac input (e.g. USA voltages) and a mere 60 V with a 100 Vac low-line input of 85 Vac. This low maximum input voltage represents a challenge.

One way to solve this problem is to add a switch network after the rectifier which is capable of reconfiguring the inputs of the dc/dc converters depending on the input ac voltage. An example, high-level implementation of this approach is shown in Fig. 2.6. The way this configuration

network works is that if the system is connected to “high-line” voltage (200-240 Vac), the step-down converters are connected in series. This would effectively split the voltage equally between them and their peak input voltage would be 186 V. (This configuration has the same outcome as in Fig. 2.1). On the other hand if the system is connected to a “low-line” voltage (85-132 Vac), the configuration network would connect these converters in parallel. Consequently the peak input voltage would still be 186 V for each converter. (The lowest peak voltage at 85 Vac would be 120 V.) The goal of the reconfigurability is that the step-down converters see the same input voltage range regardless of the line voltage they are connected to, and reduces the overall input voltage range. As explained above, this helps in selecting switches, designing magnetics and miniaturization. The configuration network would trigger once (after the microcontroller senses the peak line voltage magnitude) and stays that way for the duration of system operation.

2.1.5 Architectural variants with reconfigurable inputs

There are various ways to realize reconfiguration of the PFC conversion stages as suggested in Fig. 2.6, each of which has benefits and limitations. Multiple approaches leveraging resonant transition buck PFC cells were considered, and the best of these was adopted for further

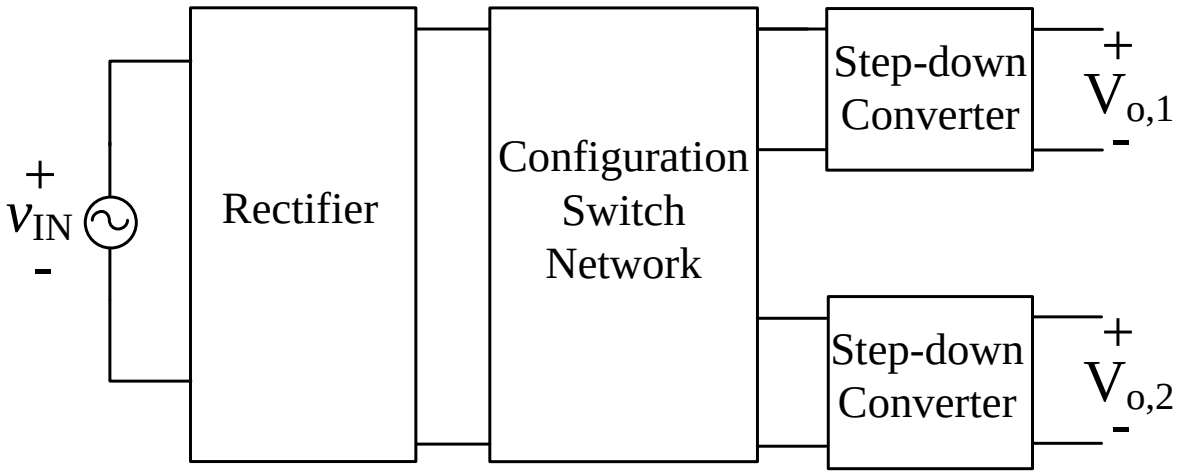


Figure 2.6. PFC stage block diagram. The configuration switch network triggers once and consists of low frequency, low on-resistance switches. The purpose of the switch network is to keep the peak input voltage of the dc/dc converters to be 186 V regardless of whether the line input is 120 Vac or 240 Vac.

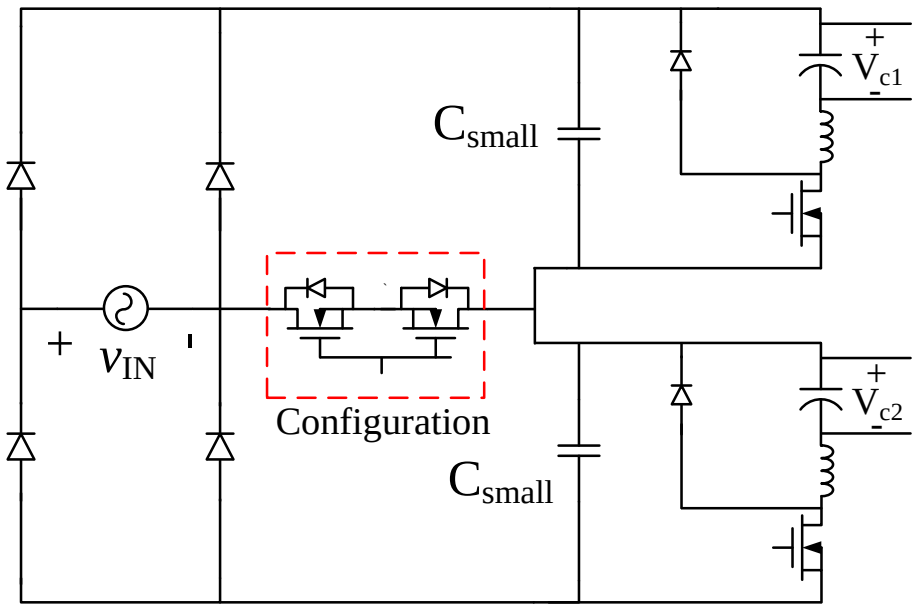
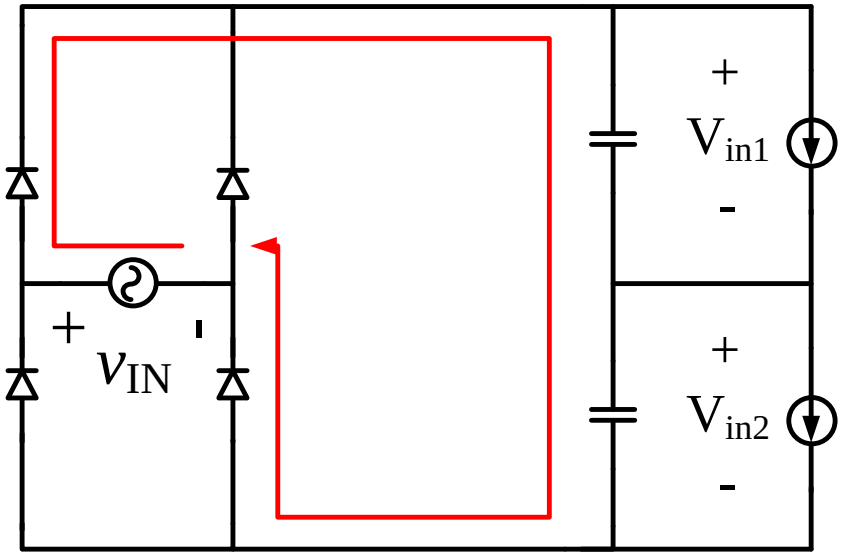
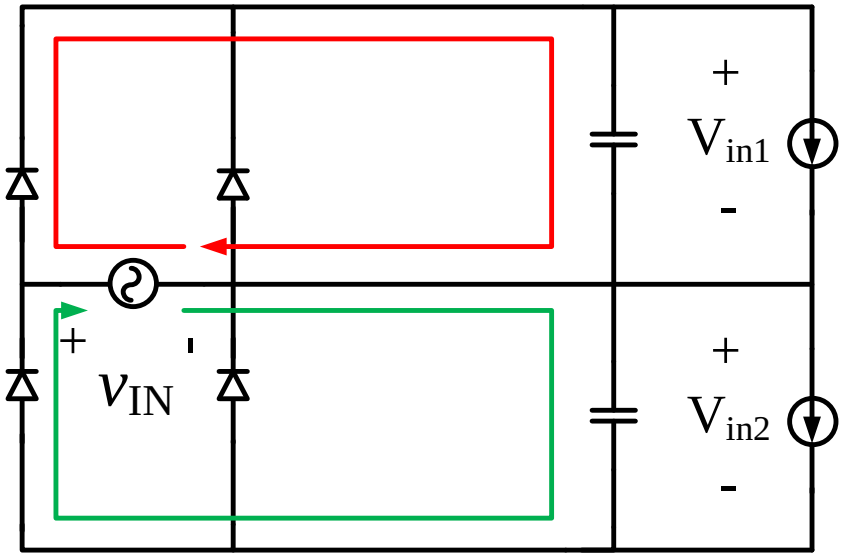


Figure 2.7. A first implementation approach for a reconfigurable PFC front end as indicated in Fig. 2.6. The dc/dc converters used is the one from Fig. 2.2. The rectifier is implemented as a diode bridge but this can also be a FET bridge. The configuration switch stays off when the input ac voltage is 240 Vac and the rectifier works as a full bridge rectifier while splitting the voltage equally among the two stacked converters. At 120 Vac, the switch closes and the rectifier works as a half wave rectifier. Each converter would operate once every half cycle. This converter has two outputs.

development. One possible implementation of a reconfigurable buck PFC design is shown in Fig. 2.7. Here the dc/dc converters are implemented using the circuit from Fig. 2.2. The configuration switch network is a single switch (bidirectional blocking, bidirectional carrying) that remains open if the input voltage is 240 Vac, and closes if the input is 120 Vac. This ensures that the input voltage range of each dc/dc converter stays the same regardless of the ac line voltage. This switch is simple to use and only triggers once, so a "big", low resistance FET is adequate here; a solid-state relay or latching mechanical relay is also a possibility. When the switch is open, both buck converters conduct simultaneously as illustrated in Fig. 2.8(a). (In this figure the converters are modeled as current sources, which is accurate for modeling line-frequency behaviors.) When the switch is closed, each converter only operates for half the cycle, as shown in Fig. 2.8(b). This means that for the same dc power delivered to the load, the converters process twice the peak



(a)



(b)

Figure 2.8. Operation of the PFC converter shown in Fig. 2.7. The buck converters are modeled as current sources for simplicity. In (a) the configuration switch is open (240 Vac input) and both converters conduct simultaneously. Both converters split the input voltage between them. In (b) the configuration the configuration switch is closed (120 Vac input) and each converter operate for one half of the line cycle. For the positive half of the line voltage, the top converter conducts (indicated by the red line) while for the negative half the bottom converter conducts (indicated by the green line). Because each converter only operates half the time, in this mode each converter has to process twice the power as compared to the high voltage mode.

power each in comparison to the 240 Vac mode. This behavior is undesirable because (i) each converter needs to be able to handle twice the peak current (this negatively impacts magnetics and switches) and (ii) the energy buffering capacitors at the output of each converter will only be charged once per cycle leading to double the voltage ripple for the same capacitance. Both of these disadvantages tend to increase the volume of the system (e.g. using bigger switches or more switches in parallel to compensate for the higher currents and doubling the capacitance to achieve the same voltage ripple).

One way to mitigate this effect is to add a voltage-balancing circuit at the input of the dc/dc converters, such as that shown in Fig. 2.9. This circuit would make sure both converters can operate simultaneously during 120 Vac mode by sloshing charge between C_{top} and C_{bot} continuously. Switches "A" would all turn on first and connect $C_{flying,2}$ across C_{top} and $C_{flying,1}$ across C_{bot}. Then switches "A" turn off and switches "B" turn on connecting $C_{flying,1}$ across C_{top} and $C_{flying,2}$ across C_{bot}. This happens at a much higher frequency than the like frequency (e.g. tens of kilohertz) to

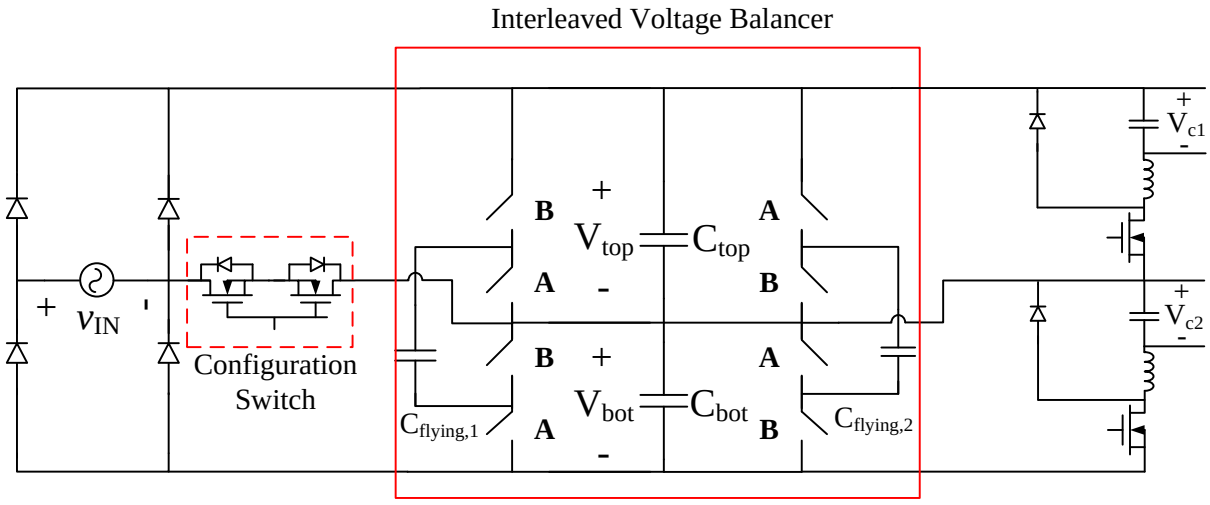


Figure 2.9. Buck PFC converter with the voltage-balancing circuit. This circuit will only operate during the 120 Vac mode when the configuration switch is closed. The circuit is an interleaved switch capacitor network that takes energy from C_{top} and delivers it to C_{bot} during the positive half of the voltage line cycle, and does the opposite operation during the negative half of the cycle.

ensure C_{top} and C_{bot} have always the same voltage. However this additional circuit needs to process half the power of the circuit (which incurs extra loss), and adds 8 switches (that need drivers and control signals). This approach was deemed too complicated and lossy to be useful.

Another possible architectural variant on the PFC stage is shown in Fig. 2.10. This version of the system uses a non-inverted and an inverted versions of the RT buck (from Fig. 2.2) stacked in such a way that their outputs add. This means the PFC converter has a single output of 150 V, as opposed to the two outputs of 75 V each from Fig. 2.7. Otherwise, the operation of this converter is the same as described above for Fig. 2.7. Being able to have an output of 150 V allows the usage of a higher energy dense capacitor for energy buffering. As will be discussed in Chapter 4, energy buffering capacitors can take up to 30 to 40% of full system volume so being able to use the highest energy dense capacitors is a desired feature. However there are a few drawbacks to this implementation. First, it suffers of the same problem as the last one: without a balancing circuit, each converter will have to be rated to process double the peak power in 120 Vac mode. This will probably offset the volume advantage gained from storing the energy at 150 V. Furthermore, this circuit has one high-side switch which adds to the complexity of driving it at HF [1]. Finally, the 150 V output means the second stage has a higher step down ratio (when compared to 75 V) and also needs to use higher voltage devices. These will have a negative impact on the performance of the second stage. Overall, compared to a design that can operate with the same power in both modes, the architecture with the single configuration switch is not very appealing.

Figure 2.11 shows a different implementation approach towards a reconfigurable system. In this case, the reconfiguration switch network utilizes three “big and slow” unidirectional switches with low ohmic loss with states that are set only once for the duration of the converter operation. If switches S1 and S3 are on, the converter inputs are connected in parallel (for 120 Vac operation).

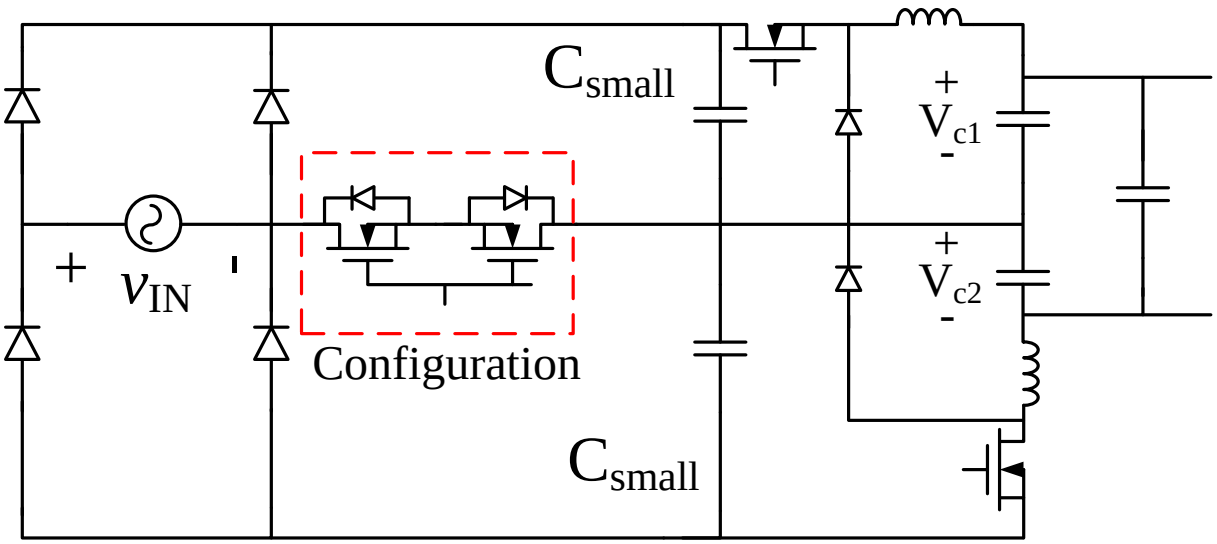


Figure 2.10. A circuit implementation of Fig. 2.6. This is a variation on the circuit shown in Fig. 2.7. This variation uses a non-inverted resonant transition buck (top) stacked over an inverted resonant transition buck. This converter has a single output at twice the voltage of the previous iteration (~160 V).

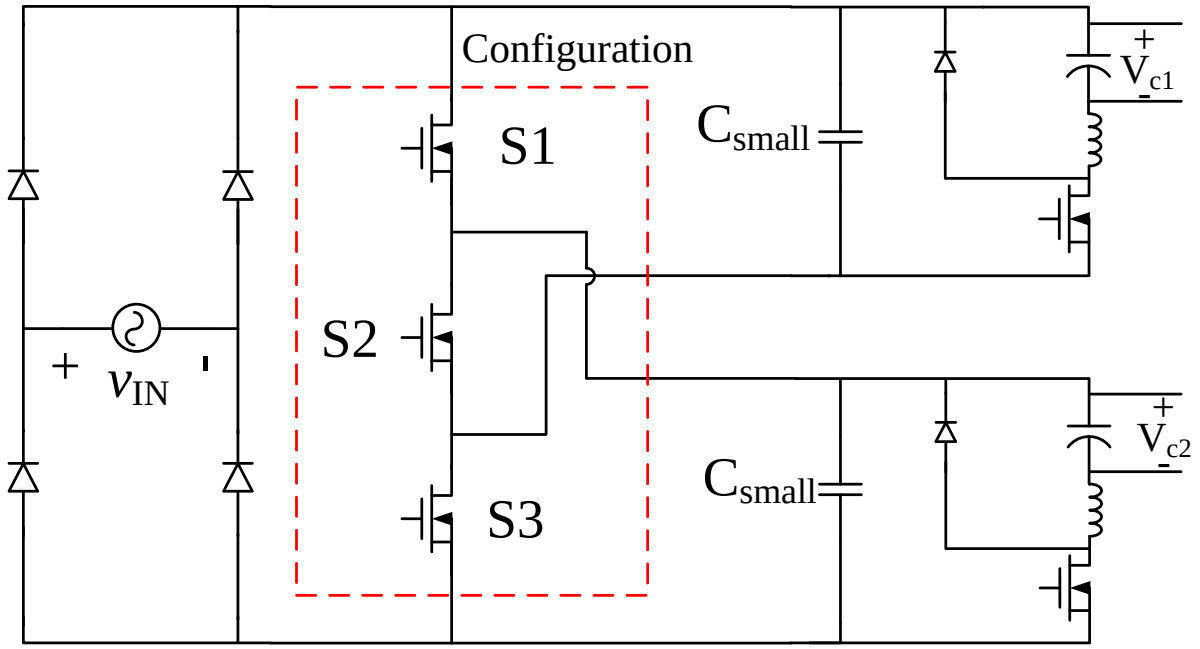


Figure 2.11. A circuit implementation of Fig. 2.6. Here the configuration switch network consists of three switches: S1, S2 and S3. If the ac line input is 240 Vac, S1 and S3 remain open and S2 closes. This connects the inputs of the dc/dc converters in series and they share the voltage. If the ac line input is 120 Vac, S1 and S3 close and S2 remains open. This connects the inputs of the dc/dc converters in parallel, and they each have the same voltage across them.

If switch S2 is on, the inputs of the converters are connected in series (for 240 Vac operation). This ensures that they have the same input voltage range and process the same peak instantaneous power regardless of line voltage magnitude. The main benefits over the single switch configuration is that both converters will always operate simultaneously regardless of input voltage without the need for a balancing circuit. One of the limitations, compared to the architecture previously discussed (Fig. 2.10), is that the outputs need to be kept separate and energy stored at 75 V in two places. (This three switch configuration will not work with the 150 V output version of the PFC). In turn forces the second stage to have a power combining capability.

After evaluating all the options presented here, the PFC converter architecture to be implemented is the one shown in Fig. 2.11. The two converters operating in unison (lower peak power processed and lower buffer capacitor ripple) and the low component count (higher efficiency and less complexity) outweigh the use of 150 V buffer capacitors.

2.2 Second Stage

The second stage converter draws energy from the first stage and the energy buffer capacitors and delivers it to the load. The second stage has to provide galvanic isolation and regulate the load voltage to a constant value as the load current changes. In the proposed architecture, the second stage is a multi-input, single output system, as shown in Fig. 2.12. It effectively will also serve as a “power combiner” because the PFC stage has two outputs (and two energy storage capacitors for holdup and energy buffering) but the system has only one load. The second stage needs to also be able to deliver full power over a full line cycle in a hold-up time transient event. Consequently, to help reduce the size of the energy storage capacitors, it must be able to operate to deliver power with substantial droop in the energy storage capacitor voltages at its inputs during a transient "holdup" event.

In this thesis two implementations of the second stage are considered. The first approach seeks to exploit commercially available, off-the-shelf telecom converters. The benefit of this approach is that it can reduce the overall system design time, enable different design versions (e.g., different output voltages) to be accommodated by changing out the second stage converters used, and can leverage the large amount of engineering optimization and economies of scale associated with such converters. However, this approach imposes challenges, because one needs to supply a single output with two standard single-input converters. The second approach is the development of a custom high-power-density two-input single output converter that is designed specifically for the required function. As will be seen, through custom design, one can achieve higher performance (combinations of efficiency and power density) than is achievable with the first approach. These solutions are discussed in detail in chapters 5 and 6, respectively.

Figure 2.13 shows the full system architecture. The PFC stage consists of a rectifier (and the EMI filter, not shown), a configuration switch network and two stacked step-down converters. The intermediate stage is the energy buffering capacitors, and the second stage is an isolated two-input, single-output converter. The rest of the thesis develops this architecture and explains each part in detail.

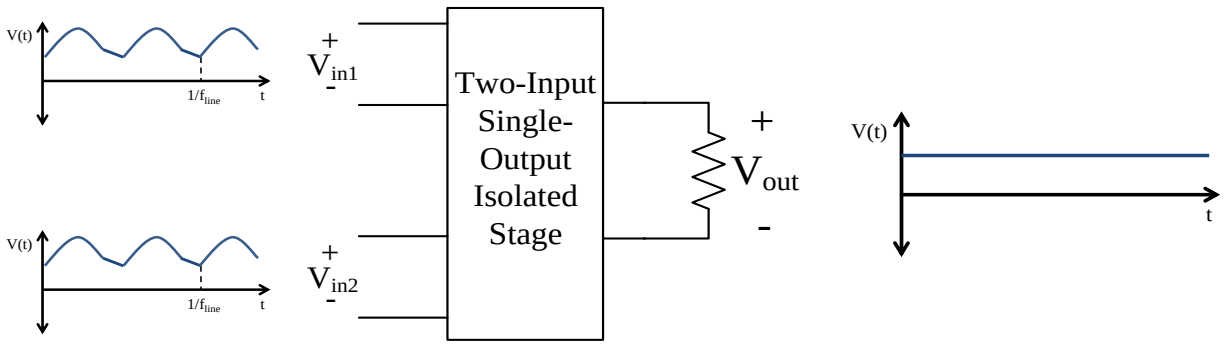


Figure 2.12. Second stage block diagram and input and output waveforms. The second stage takes energy from the energy buffering capacitors, so its input voltage waveform has the twice line-frequency ripple. It has to deliver clean dc power to the load. The capacitor selection is important because the amount of ripple present at the input will affect the performance of the second stage. Also during a hold-up time event, the input voltage will start to droop and the second stage converter needs to deliver full power over a full line cycle period (20 ms).

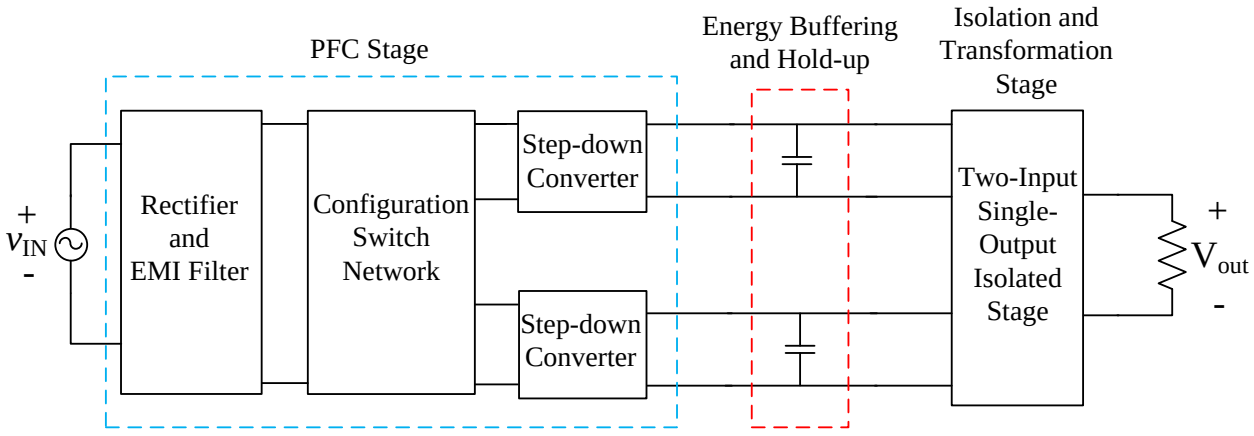


Figure 2.13. Full system architecture block diagram. The PFC stage functionality was discussed here and expanded on in chapter 3. The energy buffering capacitor sizing criteria is discussed in chapter 4. The second stage implementation is discussed in chapters 5 and 6.

Chapter 3: Resonant-Transition Inverted Buck Converter Design, Component Selection and Performance Evaluation

In this chapter, the building block of the proposed PFC converter, the Resonant-Transition Inverted (RTI) buck converter, is explored in detail. The operation of the converter is discussed along with the component selection criteria. The various steps taken to improve the efficiency of the converter developed in this thesis are also explained. The chapter closes with evaluation of the performance of the prototype converter with a dc input. (The performance of the full PFC system is explored in Chapter 8.)

3.1 Step-down converter operation

The topology used in this step down converter is the resonant transition inverted (RTI) buck converter, shown in Fig. 3.1 [22,37]. The general waveforms of this converter (shown in Fig. 3.2-3.4) largely correspond to that of the "Quasi-Square-Wave" buck converter [36], albeit with different control techniques [22,37]. The converter is "inverted" from the usual buck converter in the sense that it has "common positive" terminals of the input and output voltages, rather than a common ground. As described in detail below, this converter effectively operates at the edge of discontinuous conduction mode (DCM) so the inductor current reaches zero every cycle, but it also incorporates resonance between the buck inductor and the combination of the switch and diode capacitances to provide partial or complete zero-voltage turn-on of the transistor. (The device and diode capacitances provide snubbing for "zero voltage" transistor turn off.).

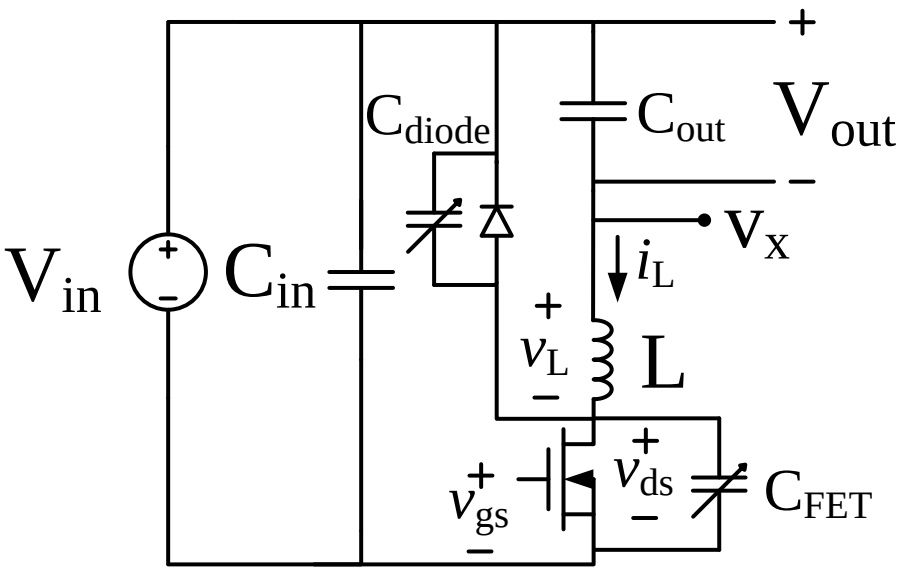


Figure. 3.1. The resonant transition inverted buck converter. This topology provides ZVS (or near ZVS) operation. It operates with large inductor current ripple and with an extremely low characteristic impedance, enabling high-frequency operation with a small magnetic component. It is used as a core building block of the PFC system as described in Chapter 2.

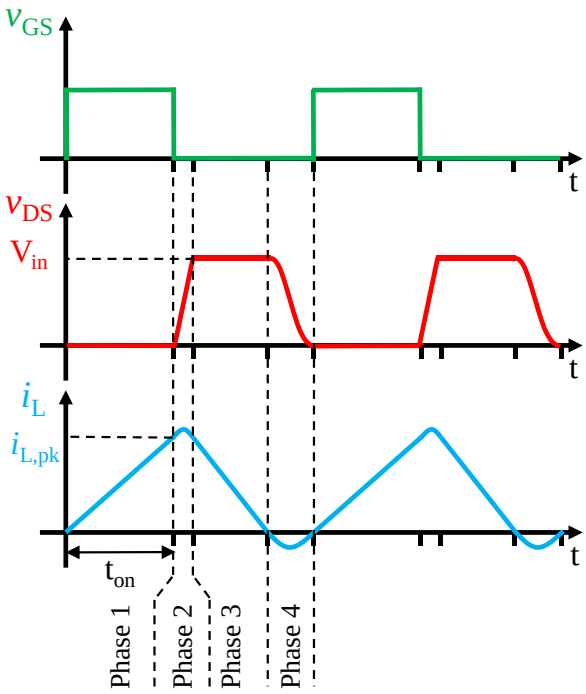


Figure 3.2. RTI buck converter idealized waveforms. This waveforms occur when Vin = 2Vout.

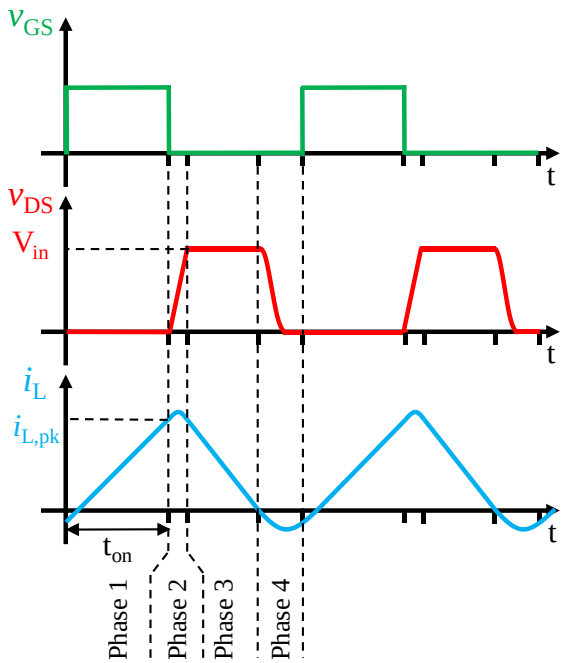


Figure 3.3. RTI converter idealized waveforms. Here the switch voltage reaches zero before the switch turns on and the FET body diode conducts. The switch turns on with non-zero current flowing through it.

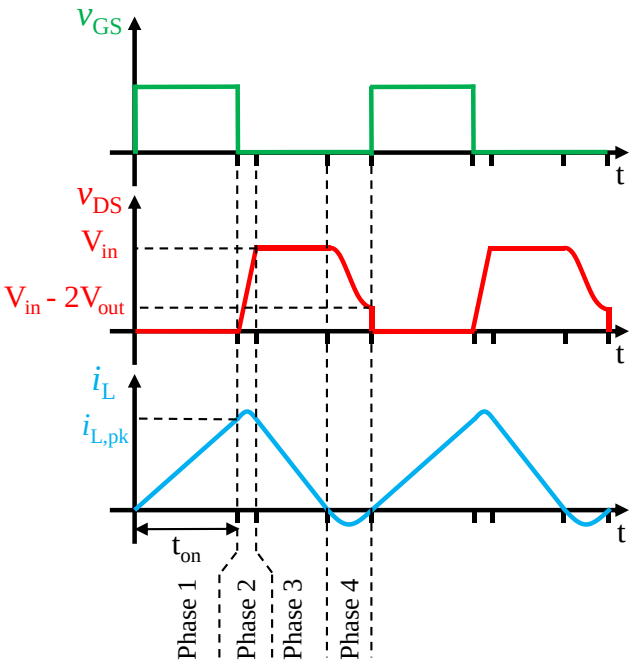


Figure 3.4. RTI converter idealized waveforms. Here the switch turns on with some voltage (Vin-2Vout) across it. This happens when the input voltage is higher than twice the output voltage.

Figure 3.2 shows the idealized waveforms of the converters, which may be divided into 4 phases. Phase 1 starts when the transistor turns on. A constant voltage is placed across the inductor ($v_L = V_{in} - V_{out}$) such that inductor current grows linearly with time with slope $(V_{in}-V_{out})/L$. After a specified on time (corresponding to a desired peak inductor current and average output current), the switch is turned off, with the transistor and diode capacitance providing snubbing for "Zero Voltage" turn-off of the switch, and phase 2 begins. In phase 2 the first resonant transition happens: the parallel combination of the diode and FET capacitances ring with the buck inductor, such that the switch voltage increases. Eventually the switch drain voltage V_DS is clamped to the input voltage by the diode turn on, and phase 3 begins. In phase 3 the diode conducts and a negative constant voltage appears across the inductor ($v_L = -V_{out}$). The inductor current ramps down at a rate ($dv_L/dt = -V_{out}/L$). When the inductor current reaches zero, the diode stops conducting (providing ZCS turn off of the diode), and phase 4 (the second resonant transition phase) begins. During phase 4, the inductor resonates with the parallel combination of the switch and diode capacitances. The drain voltage decreases and the inductor current goes negative, pulling charge out of the switch capacitance, resonantly discharging it. Phase 4 ends when the transistor turns on, initiating phase 1.

Ideally, switch turn on (starting phase 1) should occur either when (1) the transistor drain voltage just reaches zero, or (2) the transistor drain voltage reaches a valley minimum. In the first case, shown in Fig. 3.3, inductor current will be less than or equal to zero when the transistor is turned on. If the transistor is not turned on by the time the transistor drain voltage reaches zero, the body diode (or effective body diode) of the transistor will conduct, clamping the switch diode voltage near zero until the transistor turns on. In the idealized circuit, this scenario occurs if the input voltage is less than twice the output voltage.

In the second case (shown in Fig. 3.4), the transistor is turned on under at least some drain voltage, though this drain voltage is greatly reduced from the input voltage (which we refer to as "valley switching" or with the imperfect description of "partial ZVS"). With perfect "valley switching", the transistor is turned on when the inductor current is zero, and when transistor has zero dv/dt. In the idealized circuit, this scenario occurs if the input voltage is more than twice the output voltage.

The time duration of each phase in a cycle is dependent on input and output voltage, peak inductor current, $i_{L,pk}$, buck inductance value L and switch and diode parasitic capacitance. The circuit can be analyzed in a piece-wise fashion and equations can be derived for each phase. A full period of the converter is [42]:

$$T = \frac{Li_{L,pk}}{V_{in} - V_{out}} + \frac{C_{eq}V_{in}}{i_{L,pk}} + \frac{Li_{L,pk}}{V_{out}} + \pi\sqrt{LC_{eq}} \qquad (3.1)$$

C_{eq} is the parallel combination of diode and FET capacitance, $i_{L,pk}$ is the peak inductor current at the end of phase 1, V_{in} is the input voltage, and V_{out} is the output voltage. Each term in (3.1) represents the duration of each phase from 1 to 4, respectively. The input voltage of the converter changes with the ac line voltage as does the peak inductor current, which means over a line cycle the frequency of the converter varies. In the final design the frequency ranges from 1.2 MHz to 4 MHz.

3.2 Suitability for high-frequency operation

This topology offers many advantages that aid in achieving high switching frequency operation and miniaturization. First, the RTI buck converter can maintain ZVS up to a 2:1 step down ratio [37]. The drain to source voltage v_{ds} in phase 4 is [42]:

$$v_{ds} = V_{in} - V_{out} + V_{out} \cos\left(\frac{t}{\sqrt{LC_{eq}}}\right) \qquad (3.2)$$

Equating (3.2) to zero yields that to maintain ZVS, V_{in} has to be less than or equal to twice V_{out}. This range can be extended moderately with full ZVS because of the non-linear nature of device capacitance, and can operate with high efficiency with "valley switching" even in the absence of true ZVS, enabling voltage ranges of ~2.5:1 to be achieved at high efficiency [37]. Moreover, by virtue of its step-down operation the voltage stress on the switch is minimized.

Additionally, because this topology operates in DCM with high inductor current ripple, it enables the use of a very small inductor in both value and size. (Of course, to achieve high system performance, the inductor was carefully designed to maximize efficiency while keeping volume low [43-45].) The operating frequency of a converter may be limited in part by the duration of the resonance used to achieve ZVS, as seen in (3.1). By utilizing a design that resonates the full buck inductor with the sum of the device capacitances, one can achieve a reduced effective characteristic impedance and as small a magnetics size as possible. This also works to limit the switching frequency range as current is varied. All in all, the reduced value of inductance due to the high-ripple current goes a long way in the miniaturization of this converter.

Finally, because the inverted buck configuration is utilized, the source of the transistor is referenced to a steady voltage (or “logic common” in the case of the bottom converter in the stack) which makes the converter easier to drive at HF.

3.3 High-Speed Control Circuit

To achieve the desired operation providing ZVS or near-ZVS turn on of the transistor and effective control over converter output current, a high-speed control circuit is utilized [22,26,37]. This circuit, (shown on Fig. 3.5) regulates switching based on two thresholds using a pair of comparators: an indirect peak-current threshold turn-off (comparator 1) and a ZVS threshold turn-on (comparator 2). Each of these actions will be explained in detail.

Phase 1 begins when the transistor turns on. At this time, the voltage across C_{C1} is zero and the outputs of comparators 1 and 2 are both low. (The switch turns on only when the output of both comparators is low due to the NOR logic gate). When the transistor is on, capacitor C_{C1} is charged through the resistance R_{C1}. The voltage applied to this RC network is the voltage across the inductor, V_X ($V_X = V_{in}$-V_{out}). The voltage that builds up across C_{C1} is (approximately) proportional to the time integral of V_X. This is a valid approximation because the voltage V_X will be much bigger than the logic level (5 V) voltage that is allowed to build up in C_{C1}. In turn this allows us to approximate the current through R_{C1} as constant (V_X / R_{C1}). Finally the voltage across C_{C1} can be approximated as:

$$V_{CC1} = \frac{V_{in} - V_{out}}{R_{C1}C_{C1}} t_{ON} \qquad (3.3)$$

where t_{ON} is the switch on time. The voltage V_{CC1} is compared to a reference voltage v_{Iref} (set by the microcontroller) and the comparator flips state (and the FET turns off) after V_{CC1} is greater than v_{Iref}. In other words, by modulating the value of v_{Iref} we can control the peak inductor current (and average output current) of the circuit. The value of t_{ON} can be expressed as:

$$t_{ON} = \frac{R_{C1}C_{C1}}{V_{in} - V_{out}} v_{Iref} \qquad (3.4)$$

After comparator 1 output flips to high, phase 2 begins. In phase 2, the switch drain to source voltage v_{ds} increases to V_{in} and the comparator 2's output flips to high. This discharges (resets) the voltage in capacitor C_{C1} which consequently flips the output of comparator 1 to low.

No changes occur to the control circuit in phase 3 because C_{C1} is still held to ground potential by the open drain inverter. Phase 4 begins when the voltage v_{ds} starts decreasing after the inductor current goes negative. Phase 4 ends when v_{ds} (stepped down by the voltage divider R_{C2} and R_{C3}) is lower than the reference voltage v_{ZVS} (set by the microcontroller). At that instant, the output of comparator 2 goes to low, the open drain inverter opens (which allows C_{C1} to charge again) and the FET turns on. The cycle starts again in phase 1. Of note is that this control scheme does not allow body diode conduction because reference v_{ZVS} has to be a finite number greater than zero and the FET will turn on immediately after v_{ds} reaches the desired value during ring-down.

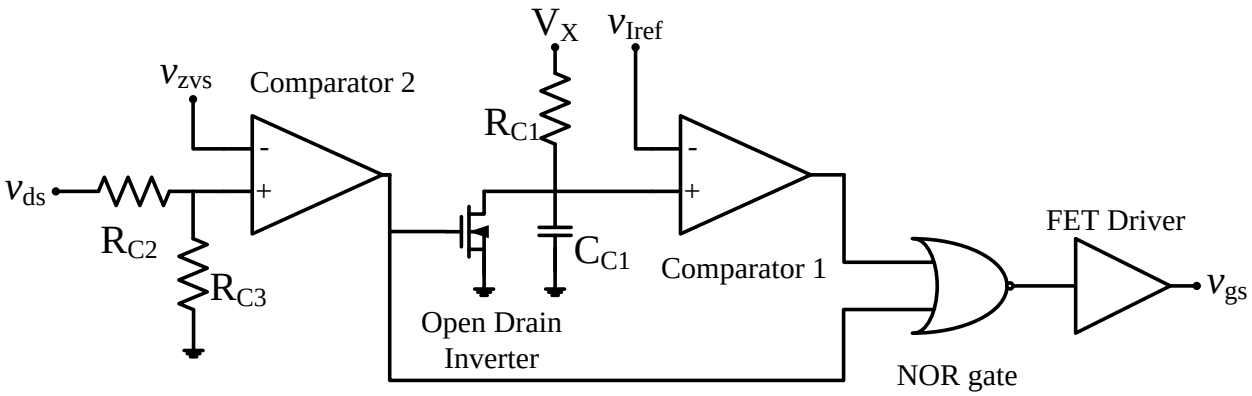


Figure 3.5. Control circuit for the RTI Buck converter. In the prototype system, these components are implemented with discrete components selected for their short propagation delays. Vx is the difference between input and output voltage, which is the same as inductor voltage when the switch is on. v_{ds} is the drain to source voltage of the switch while v_{gs} is the gate to source voltage of the same switch. v_{ZVS} and v_{Iref} are reference voltages coming from the microcontroller. v_{ZVS} is used used to determine the "valley" voltage at which the switch turns on. This value varies over the line cycle as the instantaneous input voltage to the dc/dc converter changes. v_{Iref} is used to control the on time of the switch which is used to regulate the output.

One important aspect of selecting the components in the control circuit is the propagation delays. For example, a switching cycle with a frequency of 4 MHz has a period of 250 ns. Any significant propagation delay would affect the maximum achievable frequency. The comparators used (the ADCMP601 from Analog Device) have ~3.5 ns of delay. The NOR gate (the 74LVC1G27 from Texas Instrument. This is a three-input logic gate, where the third input is used as a general "enable" toggle.) has a delay of ~2 ns. The delay may also affect the turn-on and turn-off timings of the switch. This can be compensated for by adjusting the values of v_{Iref} and v_{ZVS} slightly.

In the next section, we will describe the component selection process in detail. Each component will have its own subsection: transistor, diode and inductor.

3.4 Converter Design Specifications

Because of the stacked architecture and the output voltage of 75 V (discussed in Chapter 2), each RTI buck converter input voltage range is ~75 V to 186 V. This means the FET and diode have to be rated to handle greater than 200 V of blocking voltage. Each RTI buck converter will also process half of the output constant power load or 125 W each. However the peak power processed during a line cycle is higher. For a unity power factor converter, the peak power is twice the dc power delivered, and the peak power increases as power factor is reduced. Peak power as a function of conduction angle ϕ (defined in Chapter 2, Fig. 2.3) in radians is:

$$P_{peak} = \frac{2\pi P_{dc}}{(\pi - 2\phi + \sin(2\phi))} \quad (3.5)$$

where P_{dc} is the constant output power delivered. For an input voltage of 186 V peak (upper bound) and output voltage of 75 V, the conduction angle is 0.415 radians (23.78º), which translates to a

peak power processed of 258 W per converter. For the lower bound on input voltage (85 Vac or 120 V peak) the peak power processed is 283.8 W per converter. (The conduction angle is 0.6751 radians or 38.68º with a power factor of 0.9385). Accounting for converter losses (using a conservative estimate of 90% efficiency at full load), each converter should be rated for a peak power processed of 315 W. Consequently the peak, instantaneous current drawn by each converter is ~2.5 A. LTSPICE simulations were used to determine the current ratings of each component in all corner cases.

In the next section, the component evaluation process is described.

3.5 Component Evaluation Process

Component selection was done in several steps. First, through simulation, the corner cases of operation were evaluated and the final component specifications were obtained. The simulations were done using LTSpice to identify RMS and peak values of circuit voltages and currents. The second step was to use datasheet values of components to downselect to a handful of candidate components to be used in the converter. Many of the component characteristics have not been specified by the manufacturers at the switching frequencies required for operation in our HF converter system, hence their performance differ from that seen in the datasheet (e.g., [46]). As a consequence, a test system implemented on a printed circuit board (testing PCB) was developed which has “flexible” footprints to allow components to be readily swapped in and tested. (Appendix A has further details on the testing PCB). Thus, step three, was to use this tester PCB to experimentally evaluate the performance of each component and select the ones providing the best combination of efficiency and size. This flexible test PCB also allowed us to compare performance with varying numbers or parallel semiconductor devices to see how performance changed with device area.

Figure 3.6 shows a schematic of the tester PCB setup. The circuit performance was evaluated using a dc input and the load is a zener bank. The zener bank (comprising 25x 1N3336B zener diodes connected in parallel mounted on a heat sink [47]) acts as a constant voltage load. The constant voltage load is a good approximation of the load when the converter operates under closed loop control, and it facilitates performing sweeps in output power by modulating transistor on time as opposed to changing the load at each data point. In the next subsections, details of component selection are shown.

3.5.1. MOSFET selection

Based on our initial design specification and backed up with evaluations based on LTSpice simulation, we found that the FET should be able to block more than 200 V, conduct ~8.5 A peak and ~3.5 A average. Of course, it was desired that the transistor package should be as small as possible (within thermal limits) to reduce loop inductance. For evaluating FETs that meet this specifications, we look at the high frequency figure of merit C_{OSS}*R_{ON} of each FET (as developed in [48]). This is selected as an appropriate figure of merit because increases in either parameter degrades performance: An increase in C_{OSS} degrades achievable switching frequency (but also limits the switching frequency of the converter as discussed in Chapter 2), while increases in R_{ON} increases conduction loss. Ideally, to first order this product should also be constant for a given device family, independent of device area.

C_{OSS} is the output capacitance of the FET as defined in the datasheet. This is a voltage-dependent parameter, and for this evaluation the value of capacitance at half of the rated voltage is used. R_{ON} is the on-resistance of the switch between drain and source. Usually this includes

channel resistance, metal contact resistance and bond wires (if applicable). The channel resistance component of R_{ON} is dependent on the gate voltage, and all components of it are temperature dependent. For purposes of this evaluation, R_{ON} is selected at the rated gate voltage and at 25 ºC (approximate room temperature).

Figure 3.7 shows a plot of the figure of merit vs rated voltage for various FETs, with specific data for each FET included in Table 3.1. The low voltage GaN FETs manufactured by EPC showed the best performance (i.e. lowest figure of merit). The EPC2025 (300 V rated voltage) and was selected to be tested in the buck converter. It has a figure of merit of 6.6 pF*ohms and a 2 mm by 2 mm flip chip package. This FET fit all of the desired specifications. Data on the performance of the FET is shown in Figs. 3.8 and 3.9. Figure 3.8 plots efficiency vs output power for 2, 3 and 4 EPC2025 FETs in parallel, while Fig. 3.9 shows a temperature rise vs output power curve. All tests were done using the maximum step-down ratio (i.e. from 186 V input to 72 V output). In the latter plot, the overall lowest temperature rise (and thus, lowest FET loss) is provided by the 3 FET configuration. Based on this evaluation, 3x EPC2025 in parallel were used in the final implementation of the resonant-inverter buck converter.

3.5.2. Diode selection

A similar process was used to select the buck converter's diode. The selection criteria was a diode rated to block more than 200 V, carry an average current exceeding 3.5 A, and provide fast switching and low reverse recovery (preferably a Schottky). It was also desirable to have a diode with low forward voltage to the extent possible. The selection of commercially-available Schottky diodes with blocking voltages greater than 200 V is very limited. Table 3.2 shows the diodes evaluated in the test setup for use in the buck converter. All three are Schottky diodes, one of them Si and the other two SiC. The diode selected for use in the final circuit is the Si Schottky diode

MBRB40250TG because it provides the lowest loss at full power. This diode has the lowest forward voltage of all three according to the datasheet. Unfortunately it has a bigger package (TO-220) than the C3D1P7060Q but the 14% less loss is very valuable to achieving high system efficiency, and was deemed to be reason enough to select it.

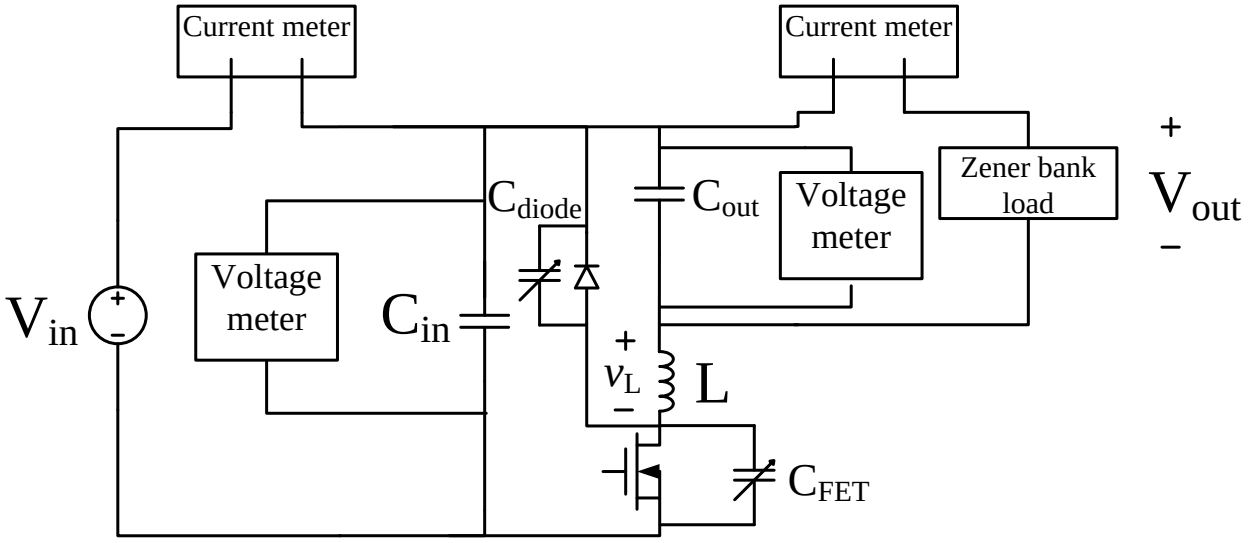


Figure 3.6. Test setup block diagram. This type of setup allows us to measure efficiency at various dc operating points. The tester board is built with flexibility in mind so that footprints allow for swapping components. More details on the tester board can be found in Appendix A.

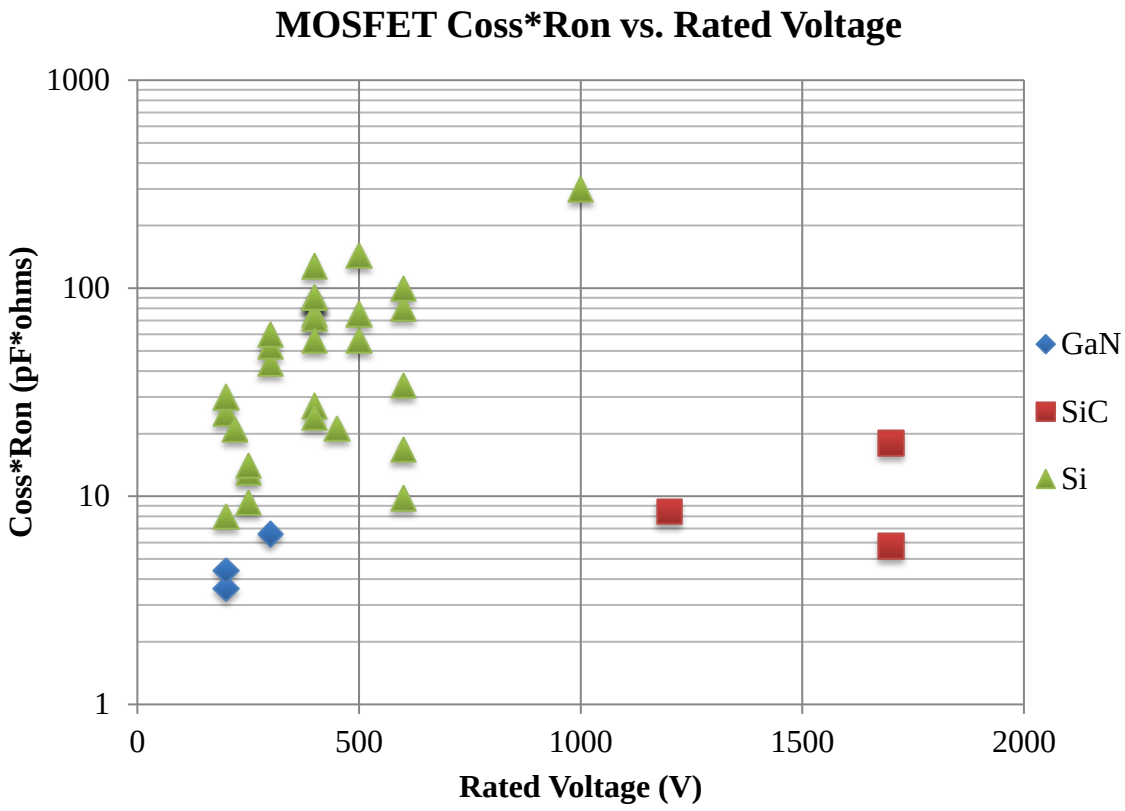


Figure 3.7. FET high frequency figure of merit vs rated voltage. Detailed data associated with this scatter plot is shown in Table 3.1.

Table 3.1 List of FETs evaluated to generate the chart in Fig. 3.7.

MOSFET	Voltage Rating (V)	Coss (pF) @ half of rated voltage	Rds (ohm) @ Rated gate voltage and 25 C	Coss*Ron (pF*ohms)	Note:
EPC2012	200	60	0.06	3.6	GaN
EPC2010	200	220	0.02	4.4	GaN
EPC2025	300	55	0.12	6.6	GaN
C2M1000170D	1700	18	1	18	SiC
GA08JT17-247	1700	25	0.23	5.75	SiC
SCT2280KE	1200	29	0.29	8.41	SiC
IXFA4N100Q	1000	100	3	300	Si
FQD12N20L	200	100	0.25	25	Si
FDD5N60NZ	600	40	2	80	Si
FCD9N60NTM	600	28	0.35	9.8	Si
FDB14N30	300	150	0.29	43.5	Si
FDB12N50TM	500	120	0.625	75	Si
TK13A60D	600	110	0.31	34.1	Si
STQ3NK50	500	45	3.2	144	Si
PSMN130-200D	200	100	0.08	8	Si
PML340SN	220	55	0.38	20.9	Si
FDD7N20TM	200	50	0.6	30	Si
FDD7N60NZ	600	80	1.25	100	Si
IRFR12N25D	250	50	0.26	13	Si
AOD7S60	600	28	0.6	16.8	Si
AON7460	300	66	0.8	52.8	Si
FDD3N40	400	25	3	75	Si
FDD6N50	500	70	0.8	56	Si
FDS2734	250	80	0.117	9.36	Si
FDT3N40	400	24	3	72	Si
FQD6N40C	400	70	0.8	56	Si
FQP3N30	300	30	2	60	Si
IRF720	400	50	1.8	90	Si
IRFR320	400	50	1.8	90	Si
RCD040N25	250	14	1	14	Si
SiHF6N40D	450	25	0.85	21.25	Si
SiHF710S	400	25	3.6	90	Si
SiHFR320	400	50	1.8	90	Si
STD3N40K3	400	8	3.4	27.2	Si
STN3N40K3	400	8	3	24	Si
STP5NK40Z	400	80	1.6	128	Si

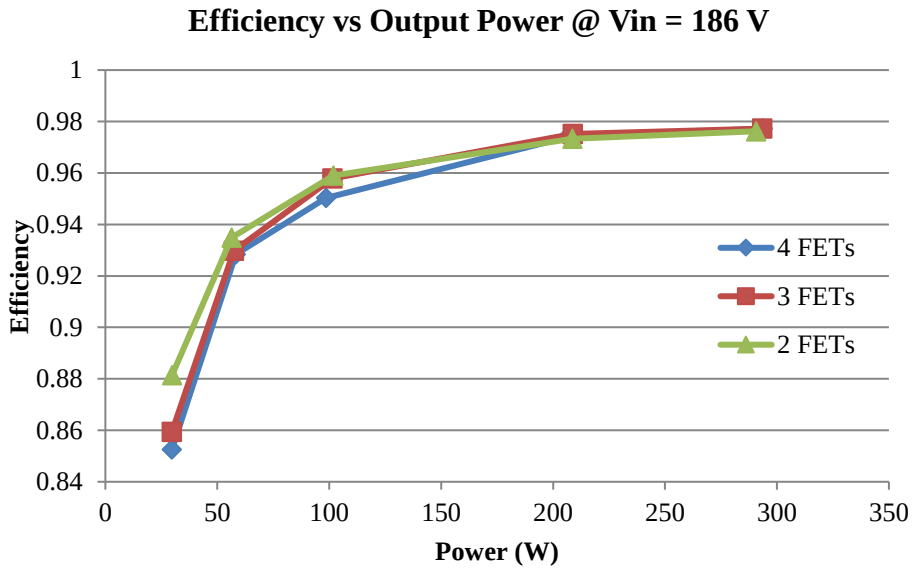


Figure 3.8. EPC2025 performance data. Efficiency vs output power for 2, 3 and 4 FETs in parallel. More FETs in parallel lead to better performance at high power (due to low total R_{ON}) but on the other hand lower efficiency at low power due to increased switching losses (i.e. higher total C_{OSS}). The input voltage is 186 V, the output voltage is 68 V (Zener bank average voltage over all operating points. Inductor used: 2 parallel windings making 9 turns each of 100/40 litz wire on Micro Metals P4840-102. Diode used: 6x C3D1P7060Q in parallel.

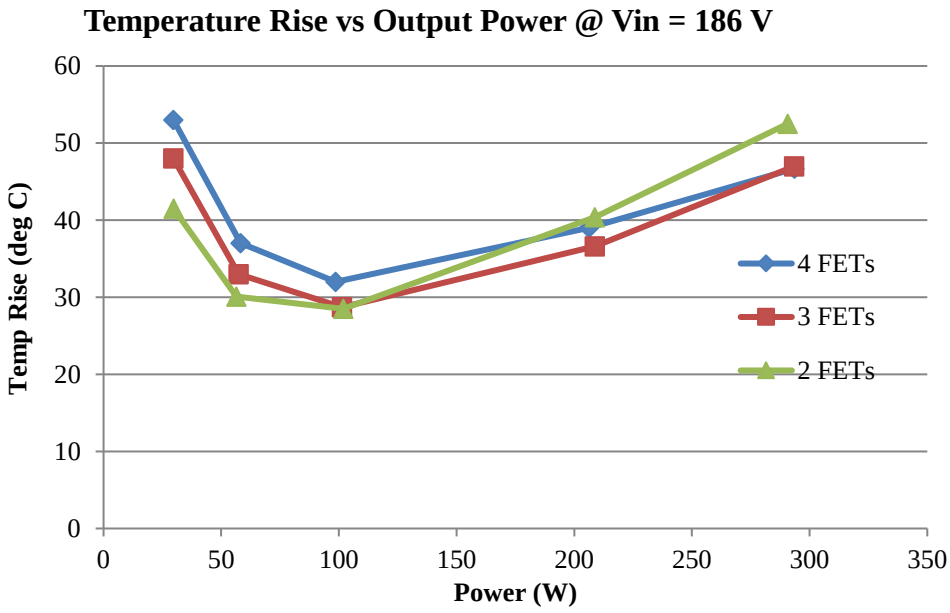


Figure 3.9. EPC2025 performance curve. FET Temperature rise vs output power for 2, 3 and 4 FETs in parallel. The 3 FET configuration has the lowest temperature rise across all operating points. The input voltage is is 186 V, the output voltage is 68 V (Zener bank average voltage over all operating points). Inductor used: 2 parallel windings making 9 turns each of 100/40 litz wire on Micro Metals P4840-102. Diode used: 6x C3D1P7060Q in parallel.

Table 3.2. Diodes evaluated in the test board and their resulting impact on overall efficiency. The test circuit is shown in Fig. 3.6 and the operating conditions are as follows: input voltage of 186 V, output voltage 69 V, output power 300 W. Inductor used: 2 parallel windings making 9 turns each of 100/40 litz wire on Micro Metals P4840-102. FETs used: 4x EPC 2025 in parallel.

Diode	V block (V)	Typical V fwd (V) @ 1 A and 125 C	Capacitance at half rated voltage (pF)	Diode type	Package	Circuit efficiency
MBRB40250TG	250	0.4	110	Si Schottky	TO-220	0.9798
C3D1P7060Q	600	1.5	7	SiC Schottky	QFN	0.9764
C3D10060G	600	0.75	40	SiC Schottky	TO-220	0.9750

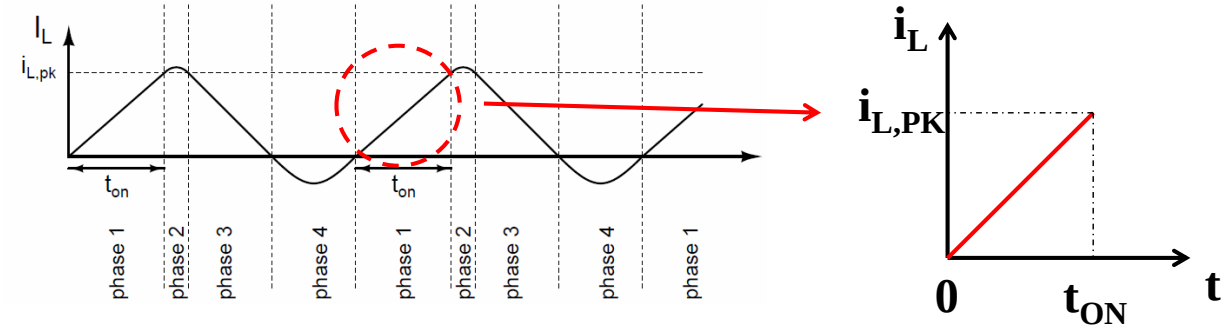


Figure 3.10. Inductor current waveform and zoom in on phase 1 (inductor current ramp-up). The transistor on time t_{ON} is modulated to vary the power delivered to the load.

3.5.3 Inductor Value Selection

The inductor design is critical to achieving high power density and high efficiency. Figure 3.9 shows the inductor current waveform for the case where the input voltage is exactly twice the output voltage, such that the drain voltage rings exactly down to zero and the transistor is turned on at zero voltage and zero dv/dt. This case is the only one considered because we are trying to find a minimum value of inductance and, thus, a minimum value of t_{ON}. In the case where the

transistor turns on with non-zero dv/dt, the inductor current is negative and takes longer to reach the desired peak current thus yielding a higher t_{ON}. The average inductor current is approximately proportional to the peak inductor current and to transistor on time. This also means the power delivered to the output can be directly modulated by the transistor on time.

As described in Eqn. (3.1), converter operating frequency is closely related to power / current delivery to the output and to inductor size. There is a close link between the on time of the transistor, the inductance, and the peak and average current delivered to the converter output. Interestingly, a key constraint in practically selecting the inductor in the converter is providing sufficient inductance such that one can realize the desired lowest peak (and average) current into the converter output with an achievable minimum on time. This occurs owing to control limitations in synthesizing very short transistor on times. The inductance value of the RTI buck converter is selected based on the following equation derived from the inductor current ramp-up phase:

$$L = \frac{(V_{IN,MAX} - V_O)}{i_{L,PK,MIN}} * t_{ON,MIN} \qquad (3.6)$$

where L is inductance, $V_{IN,MAX}$ is the maximum input voltage (186 V), V_O is the output voltage (72 V), $i_{L,PK,MIN}$ is the peak inductor current needed at minimum output power (0.85 A peak for 30 W), and $t_{ON,MIN}$ is the minimum transistor on time considered feasible for realizing minimum power delivery. The minimum on time was selected to be around 20 ns, which includes driver rise time. Following this analysis the inductance was selected as 3 μH.

3.5.4 Inductor Design

The inductor was designed using an iterative approach. A certain combination of core material, core geometry, air gap and winding configuration is selected that achieves 3 μH of inductance, while also providing a maximum of ~3 W (~1% of peak power processed) loss under operating conditions of peak power (~300 W) and yielding a maximum inductor temperature rise of 100º C above 25º C ambient. The expected operating frequency range is 1.2 MHz to 4 MHz; the low end of the frequency range is expected for ~8 A peak current, and the high end of the frequency range is expected for 0.85 A peak current. However, initial loss calculations showed that the 8 A, 1.2 MHz operating point (high power) dominated the inductor losses over the 0.85 A, 4 MHz operating point (low power). Thus, the inductor is only evaluated at high power. The inductor is also checked that it does not saturates and that the winding fits in the window area of the core. The designs considered here all have litz wire winding.

The design algorithm is as follows. An inductor is synthesized by selecting a core material, core geometry, litz wire winding, number of turns and air gap with the goal of achieving a 3 μH inductance. The core materials considered were 4F1, 3F4, 3F45 from Ferroxcube and 67 from Fair-Rite. These materials were chosen because they have high performance at the ~1 MHz range. The core geometries considered were selected from the list in table 3.3. The litz winding considered was 40 AWG with 100 strands (However, the litz wire used in the final design was improved further. This will be explained shortly. For future work, the litz wire improvement step could be incorporated directly to the algorithm.). The number of turns considered were from 1 to 10, with the air gap adjusted accordingly to obtain the desired inductance.

After an inductor is synthesized, the design is checked for core saturation and realizable winding area. If the inductor passes the check, the winding losses are calculated. Afterwards, core

losses are calculated. The sum of core and winding losses are the total inductor loss. Finally, the total loss is used to estimate the temperature rise of the inductor. In the next step, the number of turns is increased and the loss and temperature rise are recalculated. After reaching 10 turns (i.e. 10 different inductors), another core geometry is selected. With this new core size, inductors are designed again for 1 through 10 turns. This process continues until all the core geometries in Table 3.3 are covered. Afterwards a new core material is selected and the process begins anew, cycling through the number of turns (1 to 10) and core geometries again. After all four core materials are covered, the best design based on volume, loss and temperature rise is chosen. Availability of core material and geometry is also another limiting factor. Figure 3.11 shows a flowchart of the algorithm. A Matlab script is written that executes the algorithm. It is included in Appendix B.

In the following subsections the models for winding loss, core loss and temperature rise are discussed.

Table 3.3 List of core geometries considered in synthesizing buck inductors.

Core Geometries
E14, E18, E22, E32, E38, E43, E58, E64
EQ13, EQ20, EQ25, EQ30, EQ38
EILP14/3.5/5, EILP18/4/10, EILP22/6/16, EILP32/6/20, EILP38/8/25, EILP43/10/28

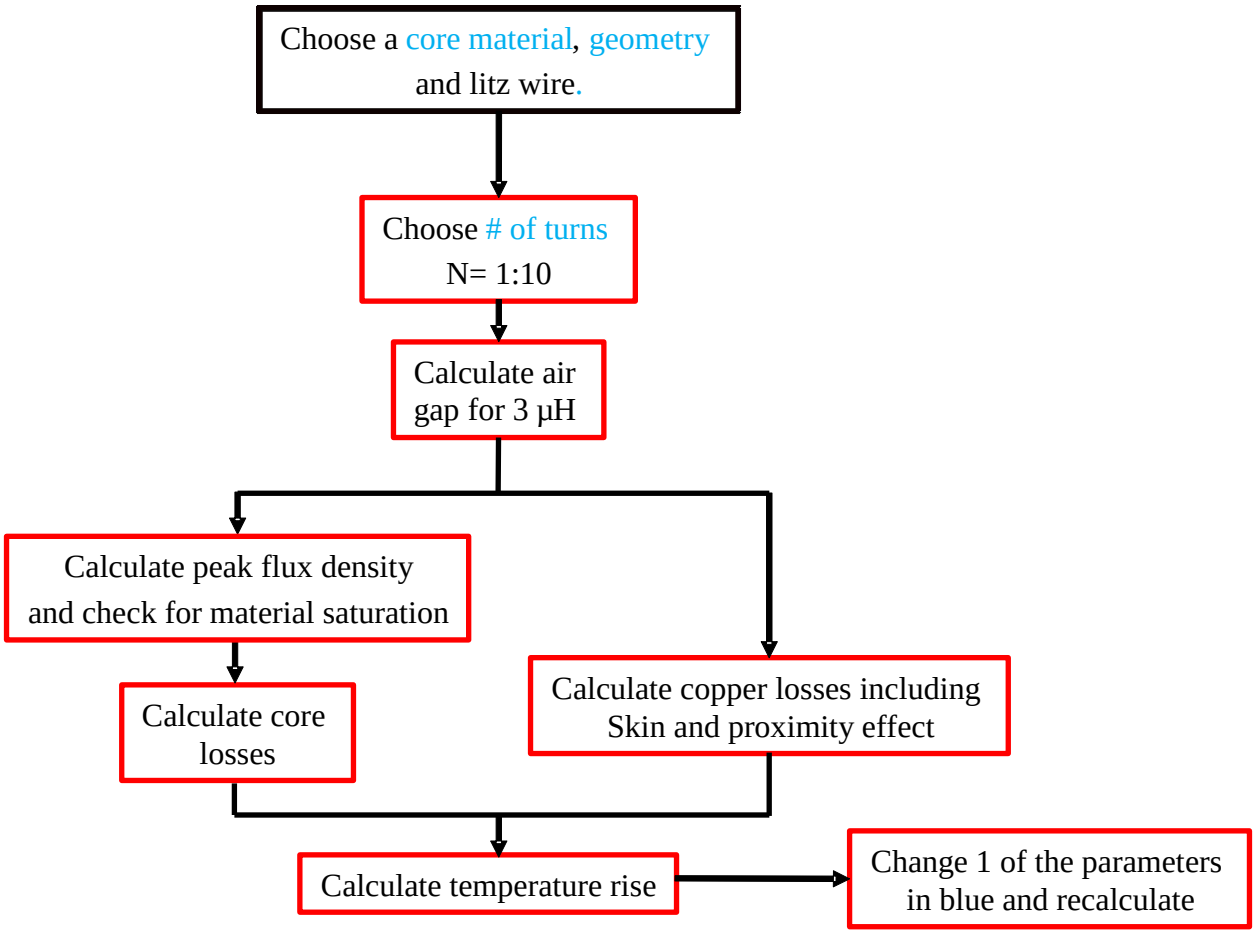


Figure 3.11. Flowchart for the inductor design algorithm. The algorithm loops first through the number of turns, then the core geometry and finally through core material.

3.5.4.1 Winding Loss

The winding losses are estimated using the following equation:

$$P_{winding} = {I_{avg}}^2 * R_{dc} + \frac{1}{2} * \sum_{m=1}^{x} {I_m}^2 * R_{ac,m} \qquad (3.7)$$

where I_{avg} is the average (dc) component of the inductor current, $R_{dc}$is the dc resistance of the litz wire, I_m is the Fourier coefficient of the *m*th harmonic, and $R_{ac,m}$ is the equivalent ac resistance

of the *m*th harmonic. The dc resistance of the litz wire is calculated using the classic resistance calculation equation:

$$R_{dc} = \frac{n\,\rho\,l}{A_s n_s} \qquad (3.8)$$

where n is the number of turns, ρ is the resistivity of copper, l is the length of one turn (which depends on core geometry), A_s is the cross-sectional area of a single strand and n_s is the number of strands.

The Fourier coefficients are calculated for the fundamental and the next 9 harmonics (for a total of 10 frequencies). The Fourier coefficients were calculated using an LTSpice simulation waveform of the inductor current at the desired operating point. The LTSpice waveform file was exported to Matlab and the 10 coefficients were calculated numerically. Including harmonics in the winding loss calculations increases the accuracy of the model.

The value of R_{ac} is calculated by first finding the ac resistance factor. The ac resistance factor is calculated using the well-known Dowell's equation [49]. Dowell's equation is useful in this litz wire model because the way the inductor is wound all turns wrap around each other. In other words, the turns form layers on top of each other. This is illustrated in Fig. 3.12. (More on inductor construction shortly.) All the core geometries considered are planar cores where this type of winding configuration can be readily used. The ac resistance factor is:

$$F_R = \frac{R_{ac}}{R_{dc}} = \frac{\Delta * (\sinh(2*\Delta) + \sin(2*\Delta))}{(\cosh(2*\Delta) - \cos(2*\Delta))} + \left(\frac{2}{3}\right) * \frac{(n^2 - 1) * (\sinh(\Delta) - \sin(\Delta))}{(\cosh(\Delta) + \cos(\Delta))} \qquad (3.9)$$

where Δ is ratio between wire (strand in the litz-wire case) diameter and skin depth δ. Skin depth δ is defined as:

$$\delta = \sqrt{\frac{2\rho}{\mu\omega}} \qquad (3.10)$$

μ is the permeability of the conductor and ω is the frequency in radians per second of the inductor current. With this model, we can use Eqn. (3.7) to estimate the winding losses. In the next subsection we discuss the core loss model.

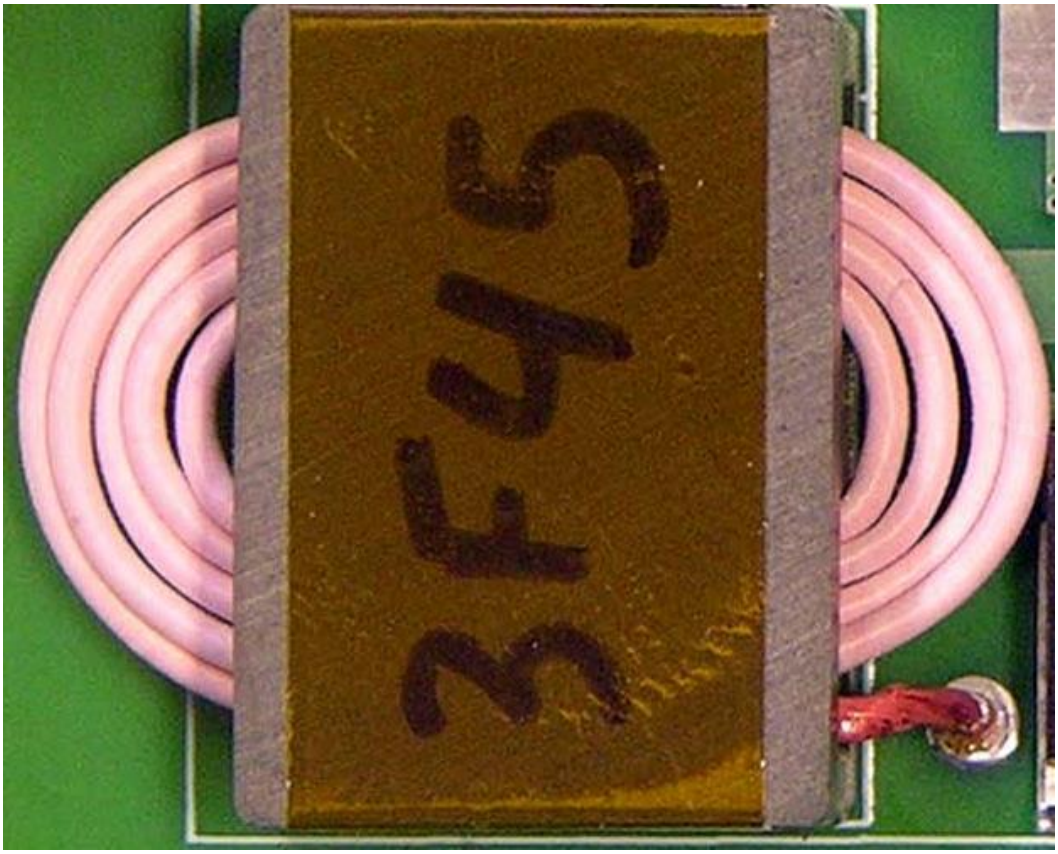


Figure 3.12. Inductor top view. The litz wire wraps around each turn forming layers. The losses can be modeled using Dowel's equation.

3.5.4.2 Core Loss

The core loss is calculated using the following equation:

$$P_{core} = V_{core} * K * {B_{pk}}^{\alpha} \qquad (3.11)$$

where V_{core} is the volume of the core, K is a constant usually with units of watts per cm^3 (this unit for K fixes the units of V_{core} to cm^3), B_{pk} is the core peak flux density in Tesla, and α is a unitless constant found experimentally. The values of K and α are material and frequency dependent. Datasheets of the core materials have experimentally-generated curves (by the manufacturers) that plot loss density as a function of peak flux density for different frequencies. The values of K and α are derived from a curve fitting of these plots. For each of the 4 core materials tested here (4F1, 3F4, 3F45 and 67) the values of K and α can be found in table 3.4.

One of the drawbacks of this method is that these loss density curves are generally created using sinusoidal excitation of the core. The buck inductor designed here, as well as many other power converters, have non-sinusoidal waveforms. It is well known that these non-sinusoidal excitations cause extra loss compared to the sinusoids of the same frequency, or even to the sum of the losses contributed by each harmonic [44,50-53]. Given that the triangular waveform used in the buck inductor has a higher ac ripple (~8 A peak) compared to dc content (~4 A average), a conservative approach was used here to calculate core losses: the peak field used in Eqn. (3.11) is the one generated by a sinusoidal current with the same amplitude as the peak inductor current. In other words:

$$B_{pk} = \frac{n i_{L,pk}}{\mu l_c} \qquad (3.12)$$

Table 3.4 List of core material parameters at 1 MHz sinusoidal excitation. These parameters are used in Eqn. (3.11) with K in units of watts/cm^3. Parameter α is unitless but the value in the table is for B_{pk} in milliteslas.

Core Material	K	α
4F1	0.7661	2.0457
3F4	0.0138	2.7287
3F45	0.0107	2.6149
67	0.0973	2.441

where l_c is the mean magnetic core length of the inductor. With all parameters defined, we can calculate core loss using Eqn. (3.11).

After calculating winding and core losses, the total losses in the inductor is the sum of both. Temperature rise is the final parameter to be calculated.

3.5.4.3 Temperature Rise

If we knew the thermal resistance of each core, the product of the thermal resistance from core to ambient and the total loss would tell us the temperature rise. Unfortunately that information is not readily available. The following formula provides a reasonable approximation for the temperature rise of a core in free standing air [54]:

$$T_{rise} = 0.75 * \frac{(P_{core} + P_{winding})^{0.833}}{SA} \qquad (3.13)$$

where SA is the surface area of the core in cm^2 and the sum of P_{core} and $P_{winding}$ is in milliwatts. The 0.75 factor accounts for conduction time of the buck converter: the conduction angle is roughly 23º so 134º out of every 180º (or ~75% of the period) are spent conducting. This is a conservative estimate because the total loss utilized here only happens at peak of line.

After running the algorithm, the top 3 cores are picked and tested in the RTI buck converter. Model verification is found in section 3.5.7.

3.5.5 Inductor Testing

Three inductors were constructed and tested. All three use the same core material (3F45) and the same litz wire (40/100) albeit with different number of turns. The E22 core was wound with 5 turns, the EQ25 with 7 and the EQ30 with 6. When constructing them, the air gap was formed using kapton tape across all legs of the core. The distributed air gaps were built using the impedance analyzer to measure inductance. More layers of kapton tape were added until the desired 3 μH of inductance were reached. Table 3.5 shows the inductor parameters and the experimental results. The calculated temperature rise for E22 and EQ25 are within 15% of the measured one. The converter efficiency with each inductor is very similar but the E22 stands out. In addition it boasts a small temperature rise and the smallest volume of the three. The E22-3F45 with 5 turns was selected for the final design.

The algorithm yields good designs but a sweep of different litz wires will help improve the efficiency further. In the next section we will consider additional litz wire options.

Table 3.5. List of inductors tested on the RTI buck tester board. All cores materials are 3F45 from Ferroxcube. Each inductor has an airgap that fixes the inductance to 3 μH. Each one is wound with 100 strands of 40 AWG litz wire. The best inductor design was the E22 core with 5 turns. Test conditions: input voltage 186 V, output power 300 W.

Core	Turns of 40/100 litz wire	Calculated Pwinding (W)	Calculated Pcore (W)	Calculated Temp rise (deg C)	Experimental Temp rise (deg C)	Experimental Buck Converter Efficiency
E22	5	0.339	1.38	27.02	23.5	0.9758
EQ25	7	0.625	0.638	19.35	22	0.9739
EQ30	6	0.429	1.7839	26.2	17	0.9734

3.5.6 Litz Wire Improvements

All the inductors designed above use 40 AWG 100 strands litz wire. We would like to explore other litz wire options for the E22-3F45 core, 5 turns design. We will use our model for winding losses, Eqn. (3.7), to find the losses with different wires. Figure 3.13 shows the winding losses of the inductor for different litz wire configurations. For the wires selected in this plot, the dc resistance is kept constant which means that the number of strands increase as the wire thickness decreases.

For strand diameter smaller than 46 AWG there are diminishing returns and the cost of litz wire increases very quickly. For cost and availability reasons, litz wire with 450 strands and gauge 46 AWG was selected for the final design. The new strand diameter is around 0.48 of a skin depth (at a fundamental frequency of 1.2 MHz) and this helps reduce the ac resistance of the winding. Lastly, a spacer (made of spare PCB FR-4 material) was added between the airgap and the winding. The spacer separates the winding by 62 mils from the distributed airgap, significantly reducing the magnetic field impinging on the wire and causing additional proximity-effect loss. The 62 mils spacer is chosen because now the E core can be placed in a PCB and the board itself can be used as the spacer (Typical 4 layer PCBs are made 62 mils thick.). The litz wire is placed on the top layer of the board away from the fringing fields. Figure 3.14 shows further details of the inductor.

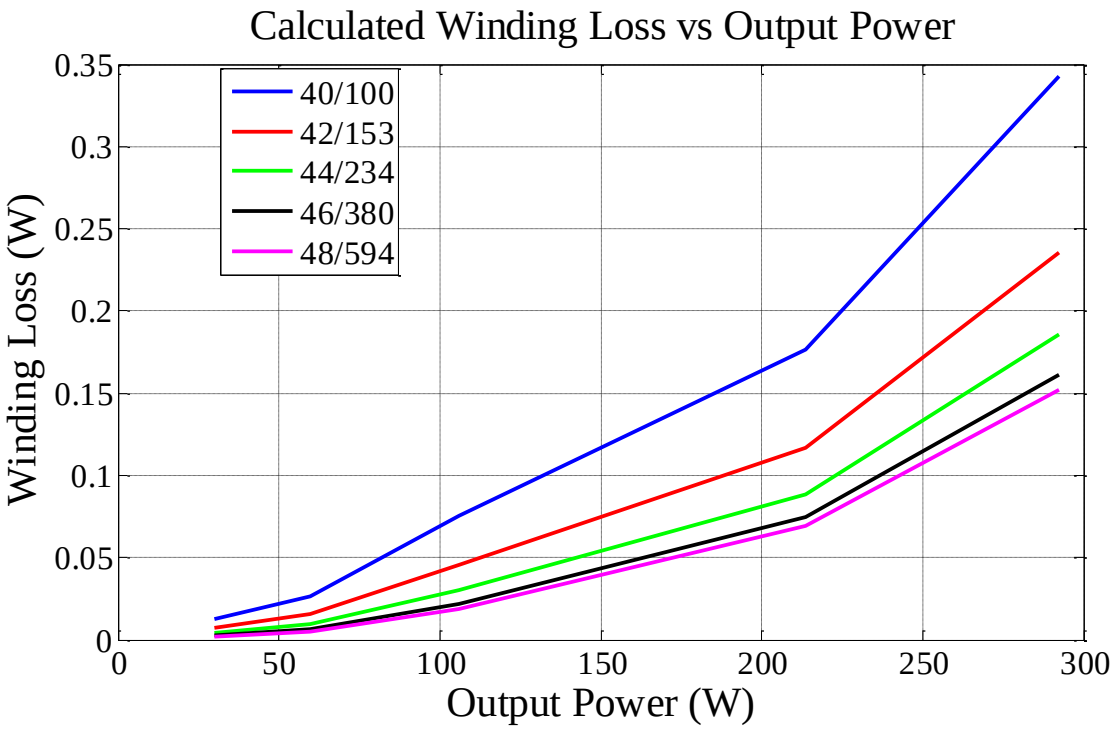


Figure 3.13. Calculated inductor winding loss as a function of output power in the RTI buck converter with a fixed inductor (E22 geometry, 5 turns). The 40/100 litz is used as the base comparison. The other 4 wires listed have the same dc resistance as 40/100. A litz winding of 46/450 was used in the final design.

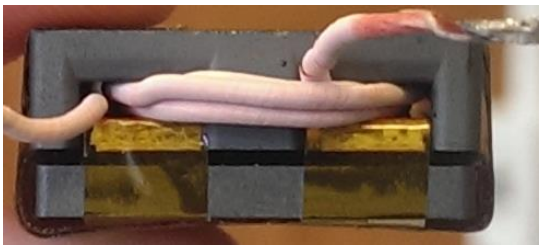


Figure 3.14. Inductor detail picture. The distributed airgap is around 32 mils (enough to obtain 3 µH of inductance). Kapton tape is used to set the airgap. The spacer separates the airgap and winding by 62 mils.

3.5.7 Model verification

Some experiments were conducted in order to verify our model. First, three different inductors are compared in the RTI buck. All three have the same core (E22-3F45) and same inductance (3 μH) but the windings are different: one has 40/100 wire with no spacer, another has 46/450 with no spacer and the last one has 46/450 with 62 mil spacer (All the spacers mentioned here are used to keep the winding away from the fringing fields near the distributed air gap). The results are shown in Fig. 3.15.

The no-spacer windings are compared first. As the model predicted, the 46/450 wire (97.65% efficient at 300 W) is more efficient than the 40/100 wire (97.62% efficient at 300 W). This difference in efficiency (0.03% or ~ 0.1 W) is in the same order of magnitude as the loss-saving we expect to get from Fig. 3.13 (~0.18 W). On the other hand, adding a spacer increased the efficiency of the converter significantly (97.92% efficient at 300 W). This hints that the proximity-effect loss is exacerbated due to the fringing fields impinging on the copper.

The second experiment conducted compares two inductors where everything is the same (E22-3F45 core, 3 μH inductance, 46/450 litz wire and 62 mil spacer) except the number of turns and the air gap. (The air gap is distributed among the three legs and adjusted using the impedance analyzer to measure inductance). One of them has five turns and the other has four turns. The results are in Fig. 3.16. As the algorithm predicted, for E22-3F45 the 5 turn inductor is less lossy than the 4 turn one.

In the next section, the RTI buck converter final performance evaluation is discussed.

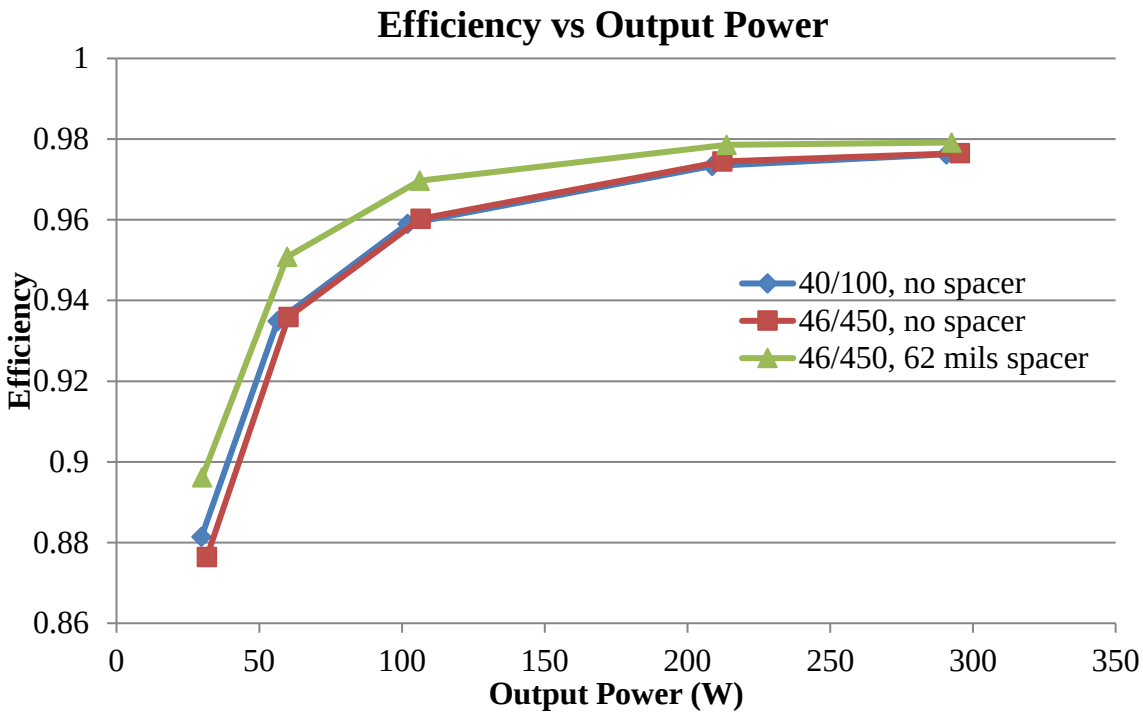


Figure 3.15. Experimental data. Efficiency vs output power for three winding configurations. The same design is used: E22-3F45 with 5 turns and 3 µH of inductance. As the model predicted, the 46/450 wire (97.65% efficient at 300 W) is more efficient than the 40/100 wire (97.62% efficient at 300 W). Adding a spacer increased the efficiency significantly (97.92% efficient at 300 W). This RTI buck used for this test had 2x EPC2025 in parallel and 1x of the MBRB40250TG diode. Input voltage 186 V, output voltage 69.3 V at 300 W and 67.5 V at 30 W (variations due to the zener load).

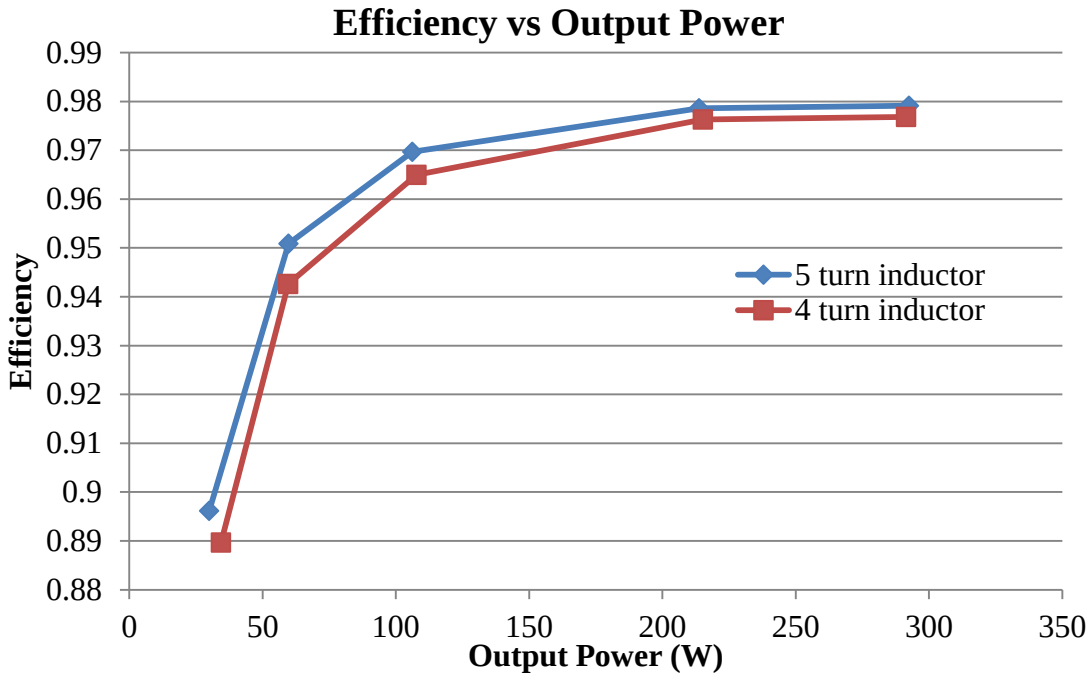


Figure 3.16. Experimental data. Efficiency vs output power for two different inductors. Both use E22-3F45 cores, 46/450 wire with a 62 mil spacer and have 3 µH of inductance. Their difference is in the number of turns and the air gap. As the algorithm predicted, the 5 turn inductor is more efficient than the 4 turn one.This RTI buck used for this test had 2x EPC2025 in parallel and 1x of the MBRB40250TG diode. Input voltage 186 V, output voltage 69.3 V at 300 W and 67.5 V at 30 W (variations due to the zener load).

3.6 Other Design Considerations

Various smaller but important design choices will be discussed here. Some of the topics include PCB layout, gate driver design and sensing signals.

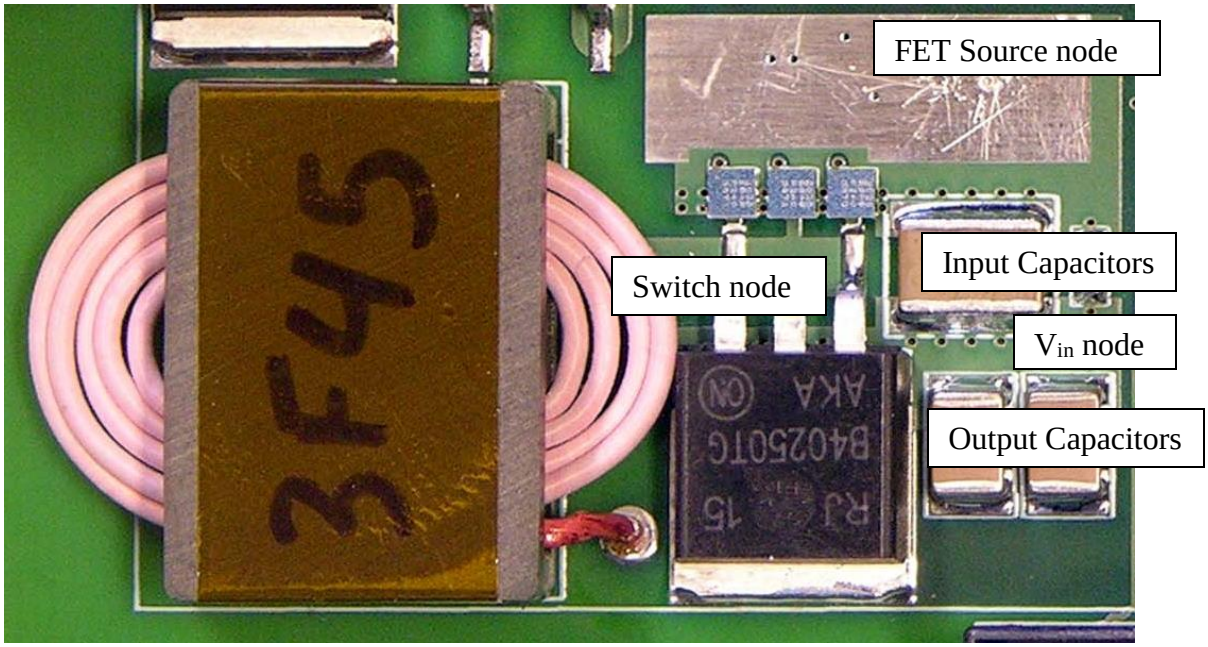
3.6.1 PCB Layout

High-frequency circuits are very sensitive to component layout on a PCB. The inductance of current loops must be kept low. A loop with high rate of change in current (high di/dt) that has inductance across it will suffer extra losses in switching devices due to excess ringing at device turn-off or turn-on. It also may cause increased EMI or noise for surrounding circuitry. To achieve

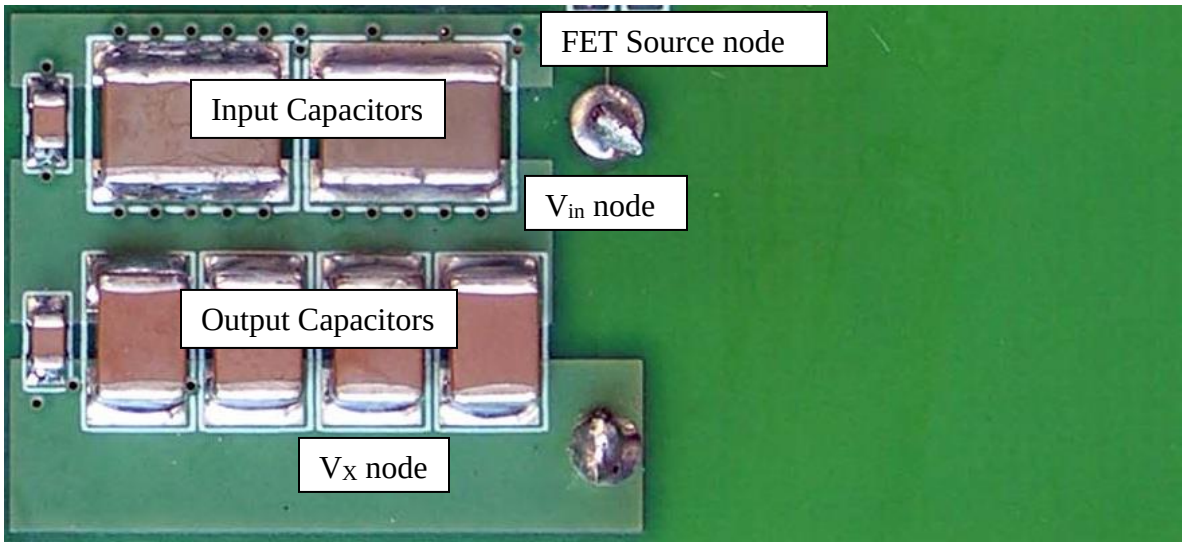
low inductance in a current loop we need to reduce the physical distance that current must travel in the PCB. In the RTI buck converter (with the layout shown in Fig. 3.17), particular attention is given to the current loops that contain the switches. When the FET is on, the current builds up in the inductor and travels from the switch node to the FET source node, through the input capacitors into the V_{in} node, then through the output capacitors and back to the inductor. (These nodes are highlighted in Fig. 3.17). Similarly, when the diode is conducting the current travels from the switch node to the V_{in} node through the diode, then through the output capacitors (through vias) to finally reach the inductor (and switch node) again. The times that both switches are open (phases 2 and 4) current flows through the inductor and the parasitic capacitances of both switches. As we can see from this description, it is very important to have the capacitors and the switches be as close to each other as possible, and make clever use of vias (and the multiple layers) in the PCB to minimize current travel path.

An important observation is that there are multiple capacitors in parallel in both sides of the board connected by vias, and they are placed tightly as close as possible to the FET and the diode. These are all the input and output bypass capacitors.

Another important aspect of the layout is minimizing the inductance on the current loop formed between the FET's gate and source terminals and the gate driver. The principles are the same: the distance between the driver and the FET should be minimized. If there are multiple FETs in parallel, place the driver in a symmetric way such that the current sourced (and sinked) by the driver splits evenly.



(a)



(b)

Figure 3.17. Layout on a PCB of the RTI buck converter. Fig. 3.17(a) shows the top side, while (b) shows the bottom. The nodes and capacitors relevant to the current path discussion are labeled.

3.6.2 Gate driver

The gate driver is a very important component in a high frequency power converter. The driver needs to source (and sink) the current needed to turn on (and turn off) the switch. A MOSFET, for example, needs a certain amount of gate charge to be able to turn on properly and provide a path for the current with low channel resistance. In a MHz range converter, we want to deliver the full amount of charge as fast as possible (high dq/dt). Thus, a high current driver is desired for driving a MOSFET in a high frequency converter.

The MOSFET selected for the final design (EPC 2025) needs 5 V at the gate. Thus, when evaluating a gate driver, we focus on the characteristics at 5 V of supply voltage. The driver's datasheet should have information on recommended layout patterns, pad size, maximum driving capacitance and how to select the bypass capacitor. The bypass capacitor should be placed as close as possible to the driver.

In our personal experience, the GaN FETs from EPC have a very sensitive gate terminal: voltage overshoots of more than a couple of volts can harm the switch. Consequently it is advised that during layout, enough space is left for gate resistors (for both the source and sink paths). These resistors usually range from a few ohms to below 1 ohm. The actual value of the resistor was chosen experimentally by looking at the gate waveform during RTI buck operation. If the overshoot exceeds the recommended operating voltage, the ringing can be damped and the switching action slowed down by placing the correct resistor. Finally, one should select the driver with the appropriate propagation delays and rise and fall times for the application. In our case, we want to minimize all values of delays and rise times. The driver used for the RTI buck is the UCC27511 from Texas Instrument.

3.6.3 Sensing signal

The high-speed control circuit, discussed in section 3.3, has to sense two signals from the RTI buck converter: the V_{in}-V_{out} voltage (called V_X in Figs. 3.1 and 3.5) and the drain to source voltage of the FET. The voltage V_X ranges from zero to about 110 V. The changes in magnitude will only affect the on-time of the FET, but it does not needs to be stepped down to logic level voltages because we are only interested in its time integral. More importantly it changes with twice line-frequency speeds (100 to 120 Hz). This makes it relatively easy to sense. On the other hand, the drain to source voltage of the FET changes at MHz frequencies, and has a peak value of 186 V. There are two things to consider here: we are interested in the actual value of v_{ds} so it needs to be stepped down to logic level voltages (5 V), and this signal changes very fast and we want to measure it accurately. One way to do this is to use a resistive and capacitive voltage divider. This network, shown in Fig. 3.18, provides a voltage step down and filters the signal. The resistors R_{C2} and R_{C3} are selected with a step down ratio of 5/200 or 1/40 to step down the voltage to a level safe for the comparator ($1/40 = R_{C3} / (R_{C2} + R_{C3})$). The resistor values are chosen big enough such that only a small amount of power is dissipated in them. The capacitors are selected with the same ratio between them ($1/40 = 1/C_{C3} / (1/C_{C2} + 1/C_{C3})$). The capacitance value should be selected such that it filters high frequency noise. A cut off frequency of 10 to 20 MHz should be sufficient for the 1-4 MHz signal we are measuring.

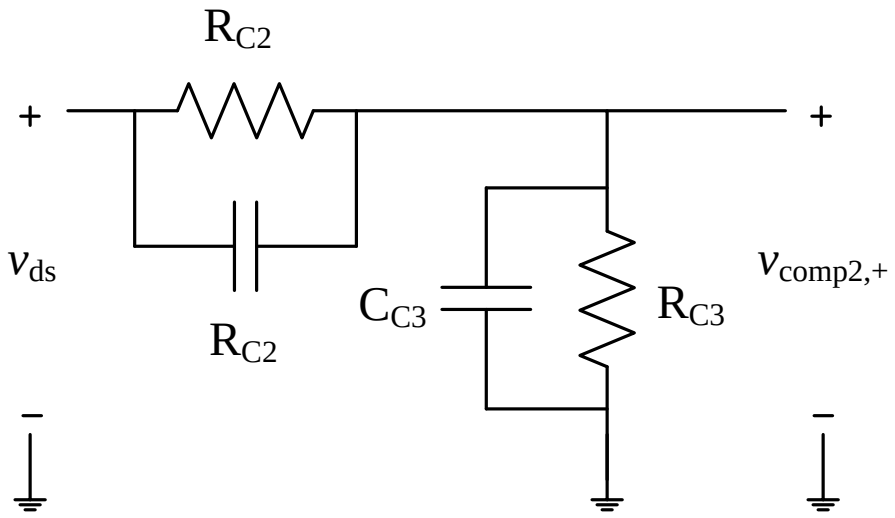


Figure 3.18. Resistive and capacitive voltage divider network used to sense the FET's drain to source voltage.

3.7 Performance Evaluation

The final component selection for the RTI buck converter used in the prototype system is summarized in table 3.6. Figure 3.19 shows the converter experimental waveforms. These waveforms are in very good agreement with the ideal waveforms found in Fig. 3.4. Figure 3.20 shows the efficiency of the RTI buck converter at various operating points. The efficiency at peak output power of 300 W and 186 V input is 98.16 %. Table 3.7 shows the shows the estimated instantaneous efficiency of the converter over a line cycle using data extracted from Fig. 3.20, and illustrates that 98% efficiency is expected over a reasonably wide range of operating conditions.

Table 3.6. Finalized part list for RTI buck converter. The MOSFET used is the GaN EPC 2025. The diode is a Schottky Barrier Diode MBRB40250TG. The inductor was hand wound. The core was an E-22 core made of 3F45 material from Ferroxcube. The litz wire used is 46/450 and has a 62 mils spacer between airgap and winding. The distributed airgap length is an estimated. The way the inductor is built is by adding air gap until 3 uH of inductance is obtained.

Part	Name
MOSFET	3x EPC2025
Diode	MBRB40250TG
Inductor	E-22-3F45, 5 turns of 46/450 litz wire, distributed ~32 mils airgap, 62 mil spacer between airgap and winding

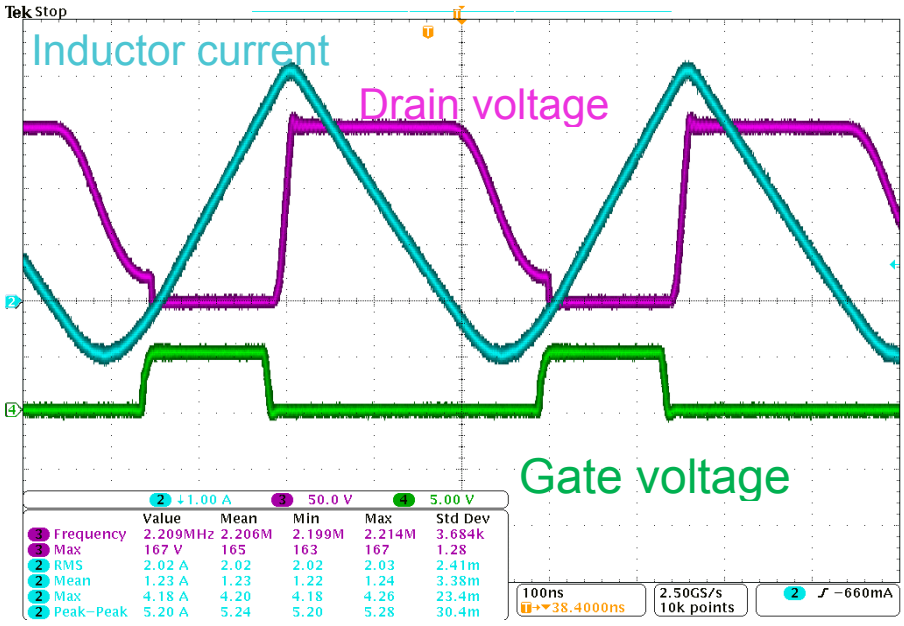


Figure 3.19. RTI buck experimental waveforms. Green is switch gate to source voltage (5 V/div), purple is switch drain to source voltage (50 V/div), and blue is inductor current (1 A/div). Operating point: input voltage 150 V, output voltage 68 V, output power 82 W.

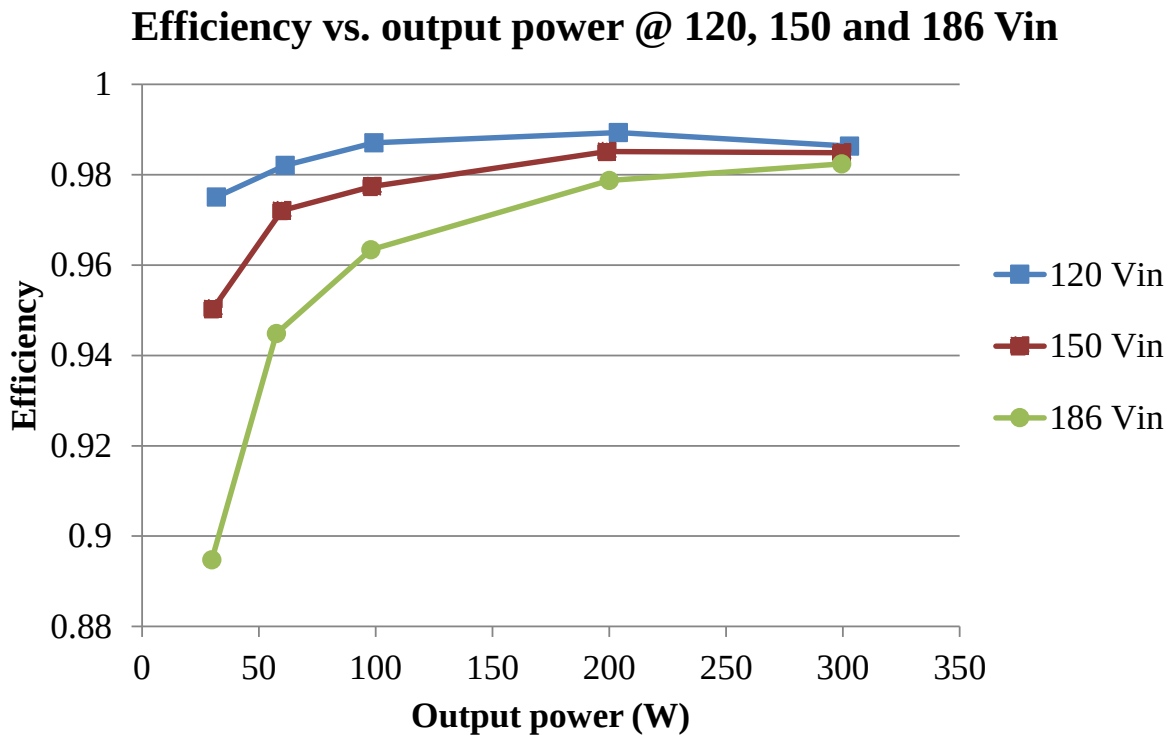


Figure 3.20. Efficiency vs output power for various input voltages of the RTI buck converter final, optimized design. The output voltage is 69 V. Components shown on table 3.6.

Table 3.7. RTI buck efficiency over a line cycle along with the instantaneous power. The efficiency over a line cycle is estimated based on the steady-state data extracted from Fig. 3.20. The average efficiency over a line cycle of a single RTI buck converter at full power is greater than 98%.

Vin (V)	Pout (W)	Efficiency
186	300	0.9816
150	197	0.9802
120	124.8	0.9874

Chapter 4: Energy Buffering Capacitor Selection

As mentioned in the introduction, the energy buffering capacitor(s) in an isolated ac/dc PFC converter system for computer applications can take up as much as 30 to 40% of the full system volume. Therefore capacitor sizing is central to all the decisions made about the ac/dc converter when power density is a metric of interest. In this chapter we will discuss the main concerns of buffer capacitor selection, and establish capacitor sizing and selection for the proposed converter system.

4.1. Twice line frequency energy buffering

Ac/dc converters for computer applications take energy from a sinusoidally-varying voltage source so necessarily must draw pulsating power, yet at the same time are desired to deliver constant power to the load. As shown in Fig. 4.1, for part of the line cycle the instantaneous input power from the ac source will be higher than the average (output) and lower for other parts. In order to avoid fluctuation in output power (especially during line voltage zero crossings), additional energy drawn from the ac source is stored during one portion of the line cycle and utilized to support the load during another portion. This process is called twice line-frequency energy buffering. The amount of energy that needs to be buffered in a unity power factor converter is [55]:

$$E_b = \frac{P_{dc}}{\omega_{line}} \tag{4.1}$$

where P_{dc} is the average power delivered to the load and ω_{line} is the line frequency in radians per second. There are two points to note in equation (4.1). First, this energy storage requirement is true only for a converter drawing perfectly sinusoidal current in phase with the voltage (that is, with

unity power factor) and delivering constant power . Thus this is an absolute minimum of energy buffered for unity power factor and constant output voltage. However, for a given allowed amount of line harmonic currents drawn, this energy storage requirement can be reduced somewhat. For example, considering the EN61000-3-2 class D line harmonic requirements [4], this energy storage requirement can be reduced up to between 44 and 61% depending on what harmonic current draw is achievable [25]. At the same time, improperly drawn harmonic currents and/or fundamental phase shifts can WORSEN the required energy buffering. (For first-order calculations, we consider the requirements of (4.1).) Second, the energy needed to be buffered only depends on the line frequency and is independent of the converter switching frequency. This is important to note because increasing switching frequency is a common method that reduces passive component size, but does not benefit component sizing with respect to the twice line-frequency energy buffering requirement.

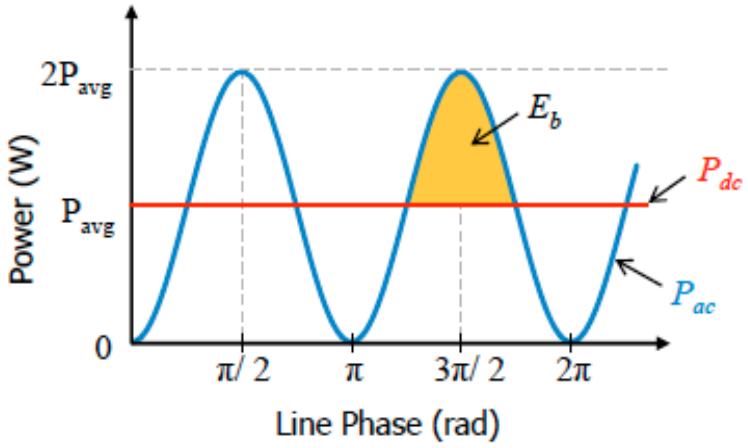


Figure 4.1. Power vs line phase. The blue waveform shows the pulsating, ac input power and the red waveform shows the dc output power.

4.2 Hold-up time energy requirement

Another important function of energy storage in the converter is to provide hold-up time. Ac-dc converters for many computer applications (including servers) must provide sufficient internal energy storage to ride through a temporary drop-out of the ac line voltage. During a hold-up transient event, the ac input may be disrupted (e.g., zero input voltage) temporarily yet the converter must be able to provide full output power is delivered. In many computer applications the hold-up time duration is specified as a full line cycle (20 ms for 50 Hz line frequency), yielding sufficient time for recovery of the line or transition to an uninterruptible power supply (UPS). The energy buffering capacitors are used as the source to deliver energy during a hold-up transient event. The amount of energy stored in the capacitors has to be enough to satisfy both twice-line-frequency energy buffering and hold-up energy requirements.

There is another trade-off between hold-up energy and the second stage converter. During a hold-up time event, the energy buffering capacitors are allowed to discharge as energy is taken out of them and delivered to the load by the second stage, without the usual steady-state requirements on allowed capacitor voltage ripple and RMS current. Thus, one may typically discharge the holdup capacitors to any extent permissible by the second stage (e.g., to the extent that the capacitor voltage is within the allowable operating range of the second stage.). The wider the input voltage range of the second stage, the more the energy buffering capacitors may be allowed to discharge during a holdup event, and the greater the portion of capacitor peak energy storage may be used. A wider allowed discharge range thus reduces capacitor size if the capacitor sizing is limited by holdup requirements. However, operating over a wide input voltage range on a converter typically comes at the cost of efficiency, so the second stage topology and design have to be chosen carefully in conjunction with the capacitor size to achieve high overall performance.

It is important to note that not all ac/dc converters have hold-up energy requirements; in fact this is a characteristic that is most common in computer servers and high reliability computer power supplies. Applications that involve charging a battery, for example in laptops, cellphones, and electric vehicles, do not require hold-up energy because the batteries can keep the system powered in case of a line dropout.

4.3. Energy buffering capacitors

Historically, energy buffering has been realized using capacitors, as they tend to provide the best tradeoffs in terms of both accessible energy per unit volume and cost at 100-120 Hz frequencies and typical power levels. Most typically, electrolytic capacitors have been used (which by far provide the best energy storage per cost), through some designs have leveraged film or ceramic capacitors [22,56,57,58]. As described in more detail below, the capacitors with the best combination of energy density and cost for the proposed design are electrolytic capacitors.

One way to define the energy buffering capability of a given capacitor is by finding its usable energy density - that is, the amount of the total energy storage that can be used in practice to buffer energy within an allowable voltage swing (e.g., over a half line cycle). For a linear (constant) capacitor, usable energy density may be defined as:

$$E_U = \frac{1}{2} C \left(V_{max,r}^2 - V_{min,r}^2 \right) \quad (4.2)$$

where C is the capacitance, $V_{max,r}$ is the maximum value of the voltage ripple (usually the rated 'working' voltage of the capacitor) and $V_{min,r}$ is the minimum value of the voltage that is

acceptable (either from an operating perspective or a loss perspective). Another useful quantity to define is ripple ratio R_C:

$$R_C = \frac{V_{max,r}}{V_{nom}} - 1 \qquad (4.3)$$

where V_{nom} is the nominal voltage or average voltage that the energy is stored at. Equation (4.3) applies to capacitors charged with square-wave current (and thus have a triangular voltage waveform). The capacitors in PFC converters are charged by quasi-sinusoidal currents (the current charging the capacitor is zero near line-voltage zero crossings in a buck PFC as explained in Chapter 2), and their voltage waveforms are not triangular. However for a small ripple the voltage waveform can be approximated as triangular. Figure 4.2 shows a LTSpice simulation time domain waveforms. The red curve is the typical buck PFC energy buffering capacitor current and the capacitor green is the voltage. The voltage can be approximated as a triangular waveform. Here V_{nom} is 71 V and $V_{max,r}$ is 74.3 V, which yields R_C of 0.046 or 4.6% ripple.

From Eqn. (4.2) one can see that there are two ways to increase the useable energy storage capability of a capacitor: increase its value of capacitance or increase the allowable voltage swing $\Delta V = V_{max,r} - V_{min,r}$ across it. Given a given dielectric and allowed field strength, increasing the capacitance value, with all else held constant, increases the size of the capacitor. On the other hand, increasing the allowed voltage ripple ΔV increases the amount of useable energy without increasing volume. However, a high voltage ripple could unacceptably increase the resistive losses in an electrolytic capacitor (i.e. the RMS value of capacitor current increases). Likewise, a converter drawing energy from this capacitor (e.g., the second stage converter in our system) has

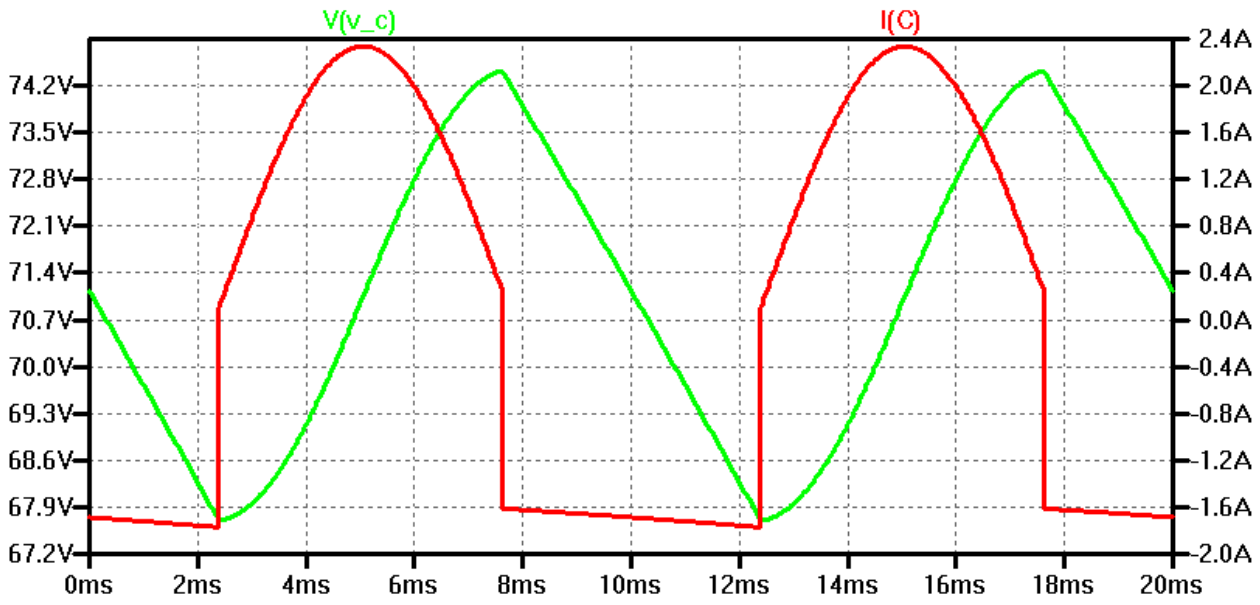


Figure 4.2. LTSpice time domain simulation. Red shows a typical current waveform for a buck PFC charging an energy buffering capacitor. In green is the capacitor voltage. The capacitor being charged is 1.2 mF and this network is connected to a constant power load of 120 W. The average voltage is 71 V.

to operate over a wider input voltage range for larger allowed capacitor ripple, which can compromise its achievable size and performance. These trade-offs between capacitor volume and second stage converter size and performance are key in this design.

Figure 4.3 shows a plot of the usable energy density of commercially-available electrolytic capacitors vs rated voltage for different allowed ripple ratios R_C. From this plot one can see that - for a given allowed percentage ripple - the highest energy density electrolytic capacitors are 400 V – 450 V capacitors; storing energy at other voltage levels is disadvantageous in terms of achievable capacitor size. It is likely the origin of this phenomenon is historical as opposed to reflecting underlying physics: the peak "high line" ac line voltage for 240 Vac is in the vicinity of 375 V. Consequently, most commercial ac/dc converters (e.g., including simple bridge rectifiers and boost-type PFC converters) yield outputs that store energy at voltages in the vicinity of 400 V.

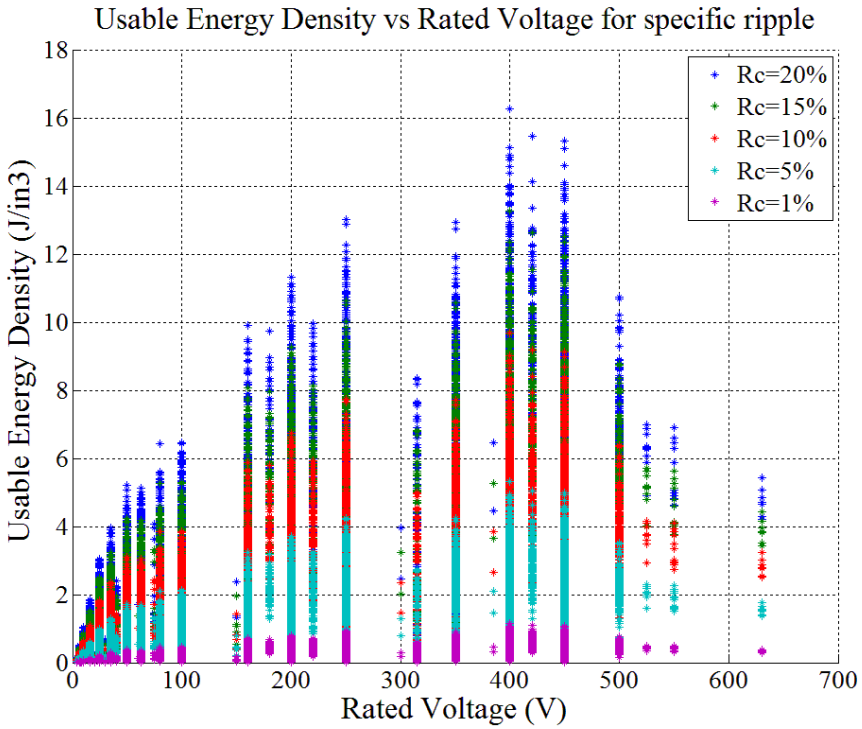


Figure 4.3. Usable energy density for electrolytic capacitors at different voltage ripple ratios vs. rated voltage for different capacitor voltage ripple ratios R_C. Usable energy density is the usable energy E_U per unit capacitor volume, as limited by how much voltage ripple is allowed every cycle. In practice, the maximum allowed ripple is limited by the allowed capacitor RMS current and/or the application design limits. Data for this plot was obtained in October 2014 from Digikey (an electronics distributor) for over 1000 capacitors. Credit to Ali Al Shehab [47] for gathering the data, analyzing it and producing this figure.

Thus manufacturers have historically been incentivized to optimize capacitors for working voltages near 400 V.

4.4 Storage Voltage Selection

An important decision, which is tied to the architectures and topologies of the ac/dc converter, is selecting the operating voltage of the buffer capacitors. While storing the energy at 400 V would benefit us in terms of capacitor size, storing at a lower voltage has system-level advantages. First, a lower capacitor voltage would decrease the step-down ratio and input voltage of the second stage

converter. Typically a lower step-down ratio and input voltage leads to smaller magnetics and higher efficiency.

Second, using a step-down PFC topology inherently increases the harmonic content in the line current. The converter can only operate during the portion of the line cycle where the input voltage is higher than the output. The higher the buck PFC output voltage (i.e. the energy buffering capacitor voltage), the lower the power factor of the system. Figure 4.4 (repeated here from Chapter 2, Fig. 2.5) shows the power factor of a buck PFC as a function of the output voltage of the buck. At ~75 V, the maximum power factor achievable is ~0.98, while at 150 V it is ~0.75. A power factor of 0.75 is undesired for this ac-dc converter.

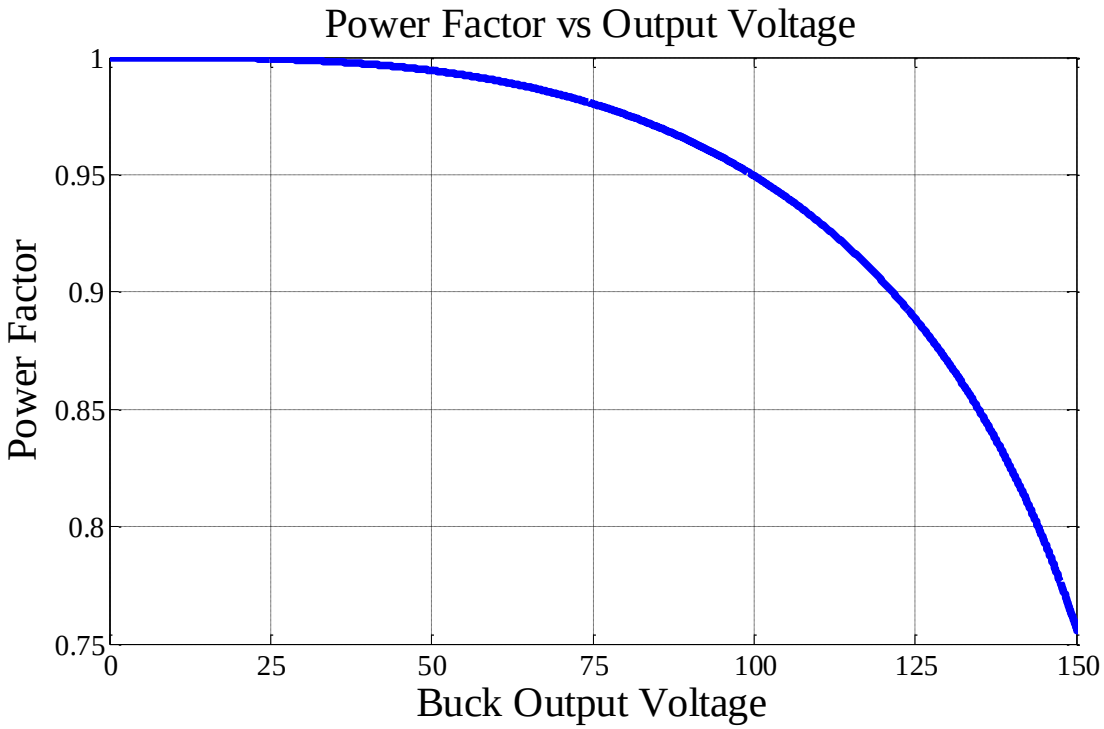


Figure 4.4. Power factor at the ac input port of a buck PFC as a function of buck converter output voltage. The input is 120 Vac. Expanded (x-axis ends at a higher voltage) from Fig. 2.5.

From Fig. 4.3, the next capacitors after 150 V rated ones are 100 V and 80 V rated ones. With a desired, final output voltage of 24 V, the second stage would have to step-down ~4:1 if using 100 V as energy storage or ~3:1 if using 80 V. The difference between them in terms of usable energy density is minimal (~0.2 J/in^3), but the difference in step down ratio can make a notable impact. For example, a lower step down ratio can help lower transformer turns ratio which is very advantageous in designing high-frequency magnetics. For this reasons, it was decided to use capacitors rated at 80 V with an average voltage of ~72 V across them.

4.5 Capacitor selection

The energy buffering capacitors are chosen selecting the minimum volume capacitance that meets the intersection of the following constraints: *i)* the twice-line-frequency energy buffering requirement, *ii)* the hold-up time energy requirement, and *iii)* the capacitor RMS current limit. Each of these constraints is explained in more detail as follows:

i) Capacitance selection constraints: allowed voltage ripple

This requirement varies with topology and application. In this case the ripple (R_C) is limited by the input voltage range on the second stage converter. From here one can determine the minimum capacitance C_{ripple} needed to maintain the capacitor voltage ripple below an allowed amount, and relate it to the amount of energy needed to be buffered every half cycle:

$$C_{ripple} = \frac{E_{buff}}{2R_C {V_{nom}}^2} \qquad (4.4)$$

where E_{buff} is the twice line cycle energy buffered. The minimum value of E_{buff} is found with Eqn. (4.1). However because of the reduced conduction time, the energy buffered in buck PFCs is higher. For a converter that draws line current like that shown in Fig. 4.5 (taken from Chapter 2, Fig. 2.3), it can be shown that the energy buffered every half cycle is:

$$E_{buff} = \frac{P_{dc}}{\omega_{line}}\left(\frac{\pi - \phi}{\pi - 2\phi}\right) \tag{4.5}$$

where ϕ is the angle at which the buck converters start conducting (i.e. when the line voltage is equal to the buck output voltage). As discussed in Chapter 2, a conduction angle of 26º was chosen for a buck output of ~72 V.

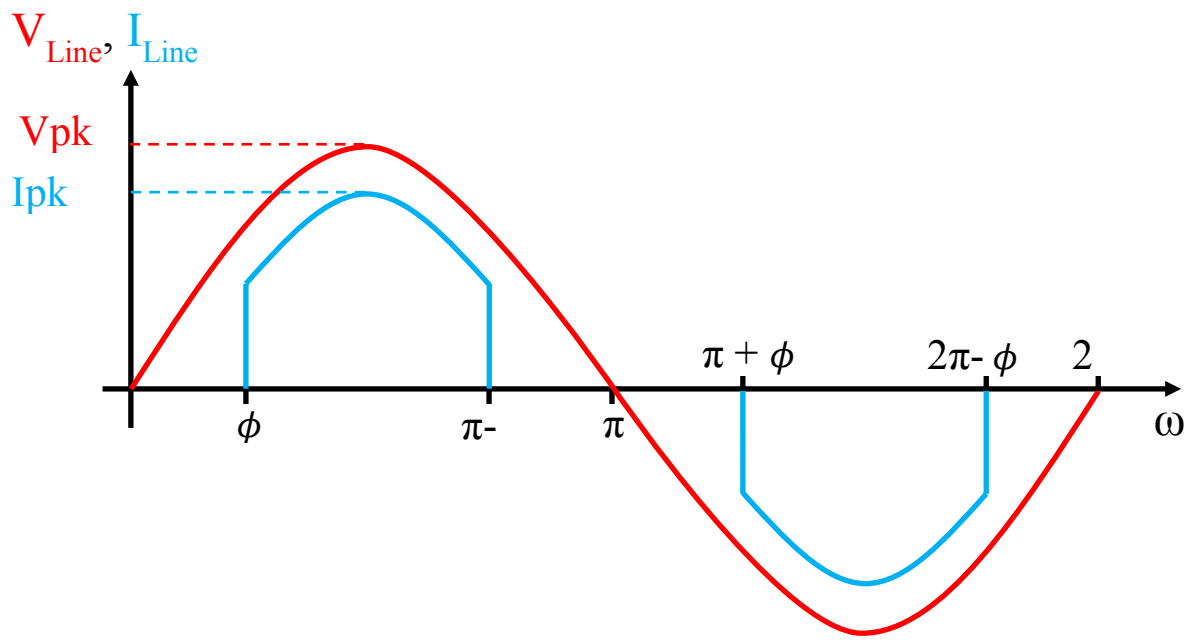


Figure 4.5. Typical line voltage (red) and current (blue) for a buck PFC. At the angle ϕ the line voltage reaches the output voltage of the buck converter and conduction begins. Taken from Chapter 2, Fig. 2.3.

ii) Capacitance selection constraints: hold-up time requirement

The second stage converter needs to be able to deliver full dc power P_{dc} to the load during a transient event where the ac input power is cut-off for a duration $t_{hold-up}$. (In the prototype system, $t_{hold-up}$ is 20 ms, or one line cycle at 50 Hz line frequency, and the nominal rated power is 250 W or 125 W per stacked converter.) The amount of capacitance $C_{hold-up}$ needed to provide constant dc power to the load during time $t_{hold-up}$ is:

$$C_{hold-up} = \frac{2P_{dc}t_{hold-up}}{(V_{nom}(1-R_C))^2 - {V_{min}}^2} \tag{4.6}$$

where V_{min} is the minimum allowed voltage of the second stage converter.

iii) Capacitor selection constraints: RMS current rating

Electrolytic capacitors typically offer both very low cost and very high peak energy density when compared to other families of capacitors (such as ceramic, mica, porcelain, tantalum, etc.), and thus are widely used for energy buffering in PFC converters. These benefits come with limitations, however: electrolytic capacitors have high equivalent series resistance (ESR) and thus are thermally limited in the amount of RMS current they can carry to support transfer of energy every half cycle. It is typical practice from manufacturers to specify the capacitor's rated RMS current for various frequencies. The required specification of RMS current of the capacitor varies with application and topology because it is dependent on the capacitor current waveform.

Figure 4.6 shows a simplified model of the energy buffering capacitor useful to calculate its RMS current rating. The input current source I_{in} is the current from the PFC converter. This current has a dc and ac component. The current source $I_{out,dc}$ is the current drawn by the second stage,

which is assumed constant. The ac component of I_{in} flows through the energy buffering capacitor. The RMS current of the capacitor is:

$$I_{cap,ac,RMS} = \sqrt{\frac{1}{T}\int_0^T (\mathrm{I_{in}} - \mathrm{I_{out,dc}})^2 dt} \tag{4.7}$$

where T is the period of the current waveform (typically 16.67 ms or 20 ms).

4.6 Application of constraints

Now we apply these constraints to the design to size our energy buffering capacitors. In the design, there are two PFC converter submodules, each with their own output. The energy buffering capacitors are split equally between the two PFC stage outputs. Each of the two submodules process half the rated power (125 W each) and buffer half the energy at its output; the second stage will to combine power from the two PFC stages and energy buffer to supply the single output. The second stage converter to be used in this design has an input voltage range (for each input) of 35-75 V. As described in more detail in Chapter 5 (for a second stage realized with commercial

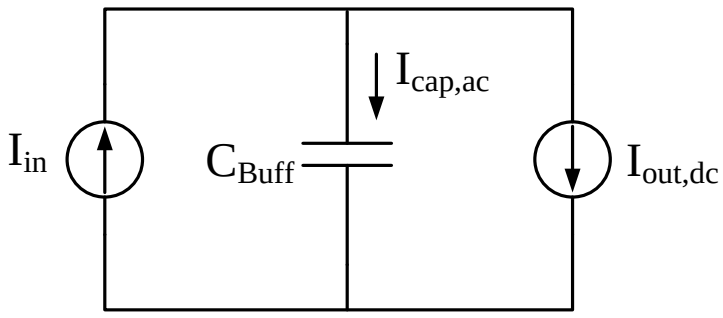


Figure 4.6. Simplified model of energy buffering capacitor. Only the ac component of the input current flows through the capacitor. The capacitor RMS current is the RMS value of $I_{in} - I_{out,dc}$.

telecom converters), this operating range is selected because it provides good second-stage efficiency while being able to leverage a significant fraction of the peak energy storage capability of the capacitors. However, in Chapter 6 we develop a custom second-stage design which operates highly efficiently over an input voltage range of 69-75 V in periodic steady state operation, and during a transient event can operate down to the specified minimum input voltage of 35 V (albeit at reduced efficiency). For the present sizing calculation (used for capacitor selection and relevant to both designs), we simply assume an operating range of 35-75 V for the second stage input voltages.

Identifying all the values needed, this translates to V_{max} of 75 V, V_{nom} (or average) of 72 V and V_{min} (or minimum allowed during a hold-up event) of 35 V. The value of the ripple ratio R_C is 4.16%, found with Eqn. (4.3). As per equation (4.5), the twice-line-frequency energy that we need to buffer E_{buff} is 0.478 J per capacitor bank. The full dc power P_{dc} for each converter is 125 W. The hold-up time $t_{hold-up}$ is 20 ms (full 50 Hz line cycle).

Plugging in the values above into Eqn. (4.4), the capacitance needed for energy buffering C_{ripple} is 1.106 mF. Doing likewise for Eqn. (4.6), the capacitance needed to store hold-up energy $C_{hold-up}$ is 1.357 mF. This analysis reveals that this ac/dc converter is limited by the hold-up capacitance. The value of capacitor RMS current rating, per capacitor, found using Eqn. (4.7) is 1.68 A at 100 Hz.

From the analysis above, the best energy buffering capacitance to place at the output of EACH of the two PFC submodules will be the smallest capacitor or combination of capacitors rated for 80 V with an RMS current rating greater than 1.68 A at 100 Hz and an equivalent capacitance greater than 1.357 mF, and that we should operate our PFC output around a nominal voltage of

approximately 72 V. The energy buffering capacitor bank chosen as the best candidate comprises two of the EKYB800ELL681MK40S (each rated for 80 V, capacitance of 0.68 mF and RMS current capacity of 1.47 A) in parallel at each PFC output. Even though this capacitor bank does not have the smallest volume fitting all the requirements, it was chosen because it limits the height of the circuit to the diameter of the capacitor (0.5 inches). Because we are optimizing for box volume in our power density calculations, it is very important to factor the height of the components and its result for the system.

4.7 Experimental verification

The above calculations reveal the requirements on the capacitor. As described above, it is the holdup constraint that sets the capacitor size in the prototype design. The hold-up energy storage requirement would be met by the proposed capacitors and was verified through an experiment. Figure 4.7 shows a block diagram of the experimental setup. A capacitor bank (2 of EKYB800ELL681MK40S in parallel) is charged from a dc power source to 72 V and the input of a commercial isolated converter (SynQor SQ60120ETA20) is connected in parallel with the capacitor bank. The converter extracts a constant 120 W as long as its input voltage remains above ~32 V. A mechanical switch is used to disconnect the source from the system allowing the capacitor to be the only source of energy for the converter. This setup is shown in Fig. 4.8. Figure 4.9 shows the capacitor voltage waveform from the experiment. The capacitor voltage droops from 72 V to 30 V before the isolated converter stops operating. However, if we find the point where the capacitor voltage reaches ~36 V, the hold-up time is 20 ms.

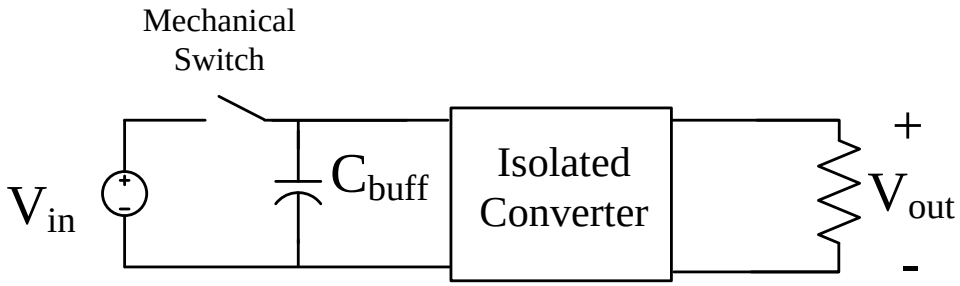


Figure 4.7. Block diagram of experimental setup for testing hold-up time capabilities of the capacitor bank. Figure 4.8 shows a photo of the bench setup. The load is a 1.2 Ω resistor. The converter is the SynQor SQ60120ETA20.

Figure 4.8. Experimental setup for testing hold-up time. The capacitance used is 2x EKYB800ELL681MK40S. The converter used is the SynQor SQ60120ETA20, which regulates its output voltage to 12 V. The capacitors are charged to an initial voltage of 72 V and the load resistor is selected as 1.2 Ω to set the constant output power drawn to 120 W. (Note: for this early test, a nominal rated total output power of 240 W was used instead of 250 W.)

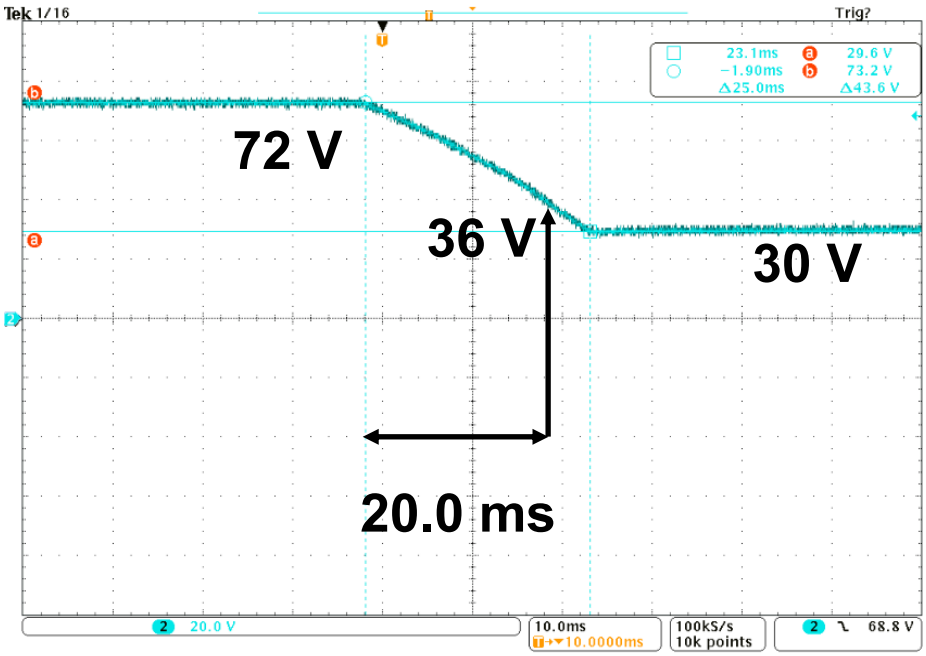


Figure 4.9. Capacitor voltage waveform during a hold-up time event using the setup in Fig. 4.7. The capacitor starts at 72 V and delivers 120 W for 25 ms before the converter stops operating. However at 20 ms, the capacitor voltage is ~36 V, as predicted.

Chapter 5: Second-Stage Design Based on Commercially Available Converters

The second stage of the ac/dc converter needs to have three main characteristics: (i) draw energy equally from two inputs and combine power to supply a single output, (ii) provide galvanic isolation and regulate the output voltage, and (iii) be able to operate transiently over a wide input voltage while supplying power to the output during a hold-up time event. A first strategy for implementing the second stage is addressed in this chapter. In this first strategy, we utilized commercially-available (and mass manufactured) telecom "brick" converters to implement the second stage. Typical telecom "brick" converters are usually specified for a nominal 48 V input with various input ranges (e.g., 36-75 V, 36-60 V and 18-75 V) and are able to provide regulation. There are many manufacturers of such converters (such as General Electric, SynQor, Vicor, Murata, etc.) and they come in a variety of rated powers, input voltage range, efficiency, output voltages and power densities, and in multiple standardized form factors. These converters are useful because they are compatible with the PFC stage we have developed here and can easily be swapped in case (1) a different output voltage rating or characteristic is desired or (2) some functions of one family are more desirable than that of others. For example, not all of them have the ability to connect their single-ended output in series or parallel. In this chapter we discuss the different commercial converters available and present experimental results of the full system operating with the commercial second stage connected to our PFC stage.

5.1. Second stage isolated converters selection

A major trade-off among second-stage converters, for this application, is the input voltage range vs efficiency. Typical converters available for the telecom space have input voltage ranges of 36-75 V "2:1 input range", and some are available for a wider 18-75 V "4:1 input range". (These typical ranges have emerged to cover the battery range requirements of "48 V" battery backed up systems, among other applications. Other input ranges are also available, but less common.) A 4:1 input voltage range converter provides a lower voltage threshold during hold-up, effectively reducing the capacitance requirement for the transient event (as explained in chapter 4). On the other hand, 4:1 voltage range converters typically have overall lower efficiency than 2:1 input voltage range (e.g., 36-75 V) converters. This lower efficiency comes from the fact that manufacturers must optimize their designs to work "well" over a wider operating range and meet thermal specifications at all corner points.

The telecom "brick" converter voltage ranges considered for the proposed PFC architecture include designs for 18-75 V (4:1 input voltage range) and 36-75 V (2:1 input voltage range). Because of the energy buffer capacitor sizing considerations described in Chapter 4, second-stage converters in the proposed system will operate near their maximum allowed voltage (around 69-75 V) during steady state operation and only operate transiently at lower voltages during hold-up time events. Ideally, therefore the selected second-stage converters would have the highest efficiency in the vicinity of 69-75 V input.

Tables 5.1 and 5.2 show efficiency data from manufacturer's datasheets for a selection of 4:1 and 2:1 input voltage range converters, respectively; these data were compiled in July, 2015, reflecting the best available commercial converters at that time. All the data shown are for the converter operating at 75 V input and 120 W output, regardless of rated values, in keeping with

the requirements of our application. We considered designs providing either 12 V or 24 V output, such that the individual converters would be connected with outputs in series or parallel to provide the desired 24 V system output. The peak efficiency of the 4:1 input voltage range converters is 91% (Power-One converter UIE48T10120) and of the 2:1 input voltage range converters is 95.0% (General Electric EBVW020A0B). The difference in efficiency is very significant to the overall design, as we target full system efficiencies in excess of 90%. For example, using the 4:1 converter with highest efficiency the PFC stage would need to be 99% efficient to achieve a full system efficiency of 90%. The 2:1 input voltage range converters were chosen in the end for their higher efficiency. Specifically, two of the GE EBVW020A0B converter were used, one connected to each of the second-stage inputs (at the energy buffering capacitors), as illustrated in Fig. 5.1. Their outputs were connected in parallel to achieve 250 W of output power at 24 V.

Of note is that connecting the outputs of these two GE converters in parallel was not a trivial effort, particularly for the "series-connected" input case. A slight shift in the output voltages would cause an imbalance in the load sharing of the two converters and this would in turn cause an instability in the PFC stage; one of the energy buffering capacitors would over charge. In order to run them successfully in (output) parallel, the output voltage trim ("adjust") feature of each converter was used (following datasheet recommendations). Controlling the "adjust" pin in closed loop allowed both converters to share the load properly and maintain stability of the PFC stage. This "trim adjust" technique was developed by Mr. David Otten who collaborated on this project.

Table 5.1. Isolated telecom brick converters with 4:1 input voltage range. All the data is taken from manufacturer's datasheets.

Manufacturer	Part Number	Rated Power (W)	Volume (in^3)	Power Density @ 120 W (W/in^3)	Efficiency at 75 V and 120 W	Output DC Voltage (V)
SynQor	IQ36240QTx05	120	1.8324	65.49	89%	24
Ericsson	PKB 5113W PI	120	0.8073	148.64	90%	12
Power-One	UIE48T10120	120	0.9068	132.34	91%	12
General Electric	EHHD010A0B	120	0.7245	165.63	90%	12
Murata	UNE-12/10-Q48-C	120	0.8073	148.64	90%	12

Table 5.2. Isolated telecom brick converters with 2:1 input voltage range. All the data is taken from manufacturer's datasheets.

Manufacturer	Part Number	Rated Power (W)	Volume (in^3)	Power Density @ 120 W (W/in^3)	Efficiency at 75 V and 120 W	Output DC Voltage (V)
SynQor	SQ60120ETA20	240	1.03086	116.4	93.50%	12
General Electric	EBVW020A0B	240	1.1003	109.06	95.0%	24
Murata	RBE-12/20-D48NB-C	240	0.828	144.93	92.50%	12
Delta Electronics	E48SH12010	120	0.7659	156.67	92.50%	12

5.2 Full system performance with commercial isolated converters

A schematic of the full ac/dc converter using the commercial second stage converters connected in parallel is found in Fig. 5.1. The fully assembled board (top side) is shown in Fig. 5.2; full schematics are provided in Appendix C (reference to an appendix with a full schematic and BOM and layout files.). This converter system had overall dimensions of 3.8 in x 4.575 in x 0.5 in (height), providing an overall power density of 28.76 W/in^3.

The circuit has been tested at all operating points with General Electric's EBVW020A0B isolated converters implementing the second stage, thus demonstrating complete PFC and isolated voltage conversion down to 24 V.

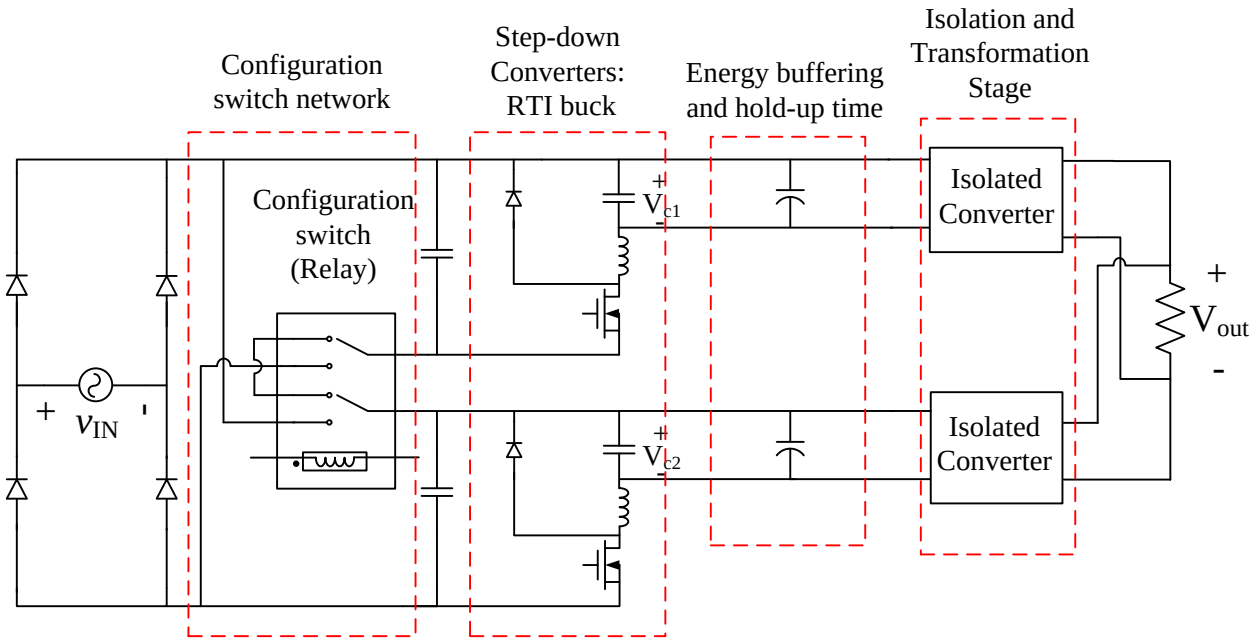


Figure 5.1. Detailed circuit of the input PFC stage. Two RTI buck converters, each with its own output, are stacked with inputs in series or parallel depending upon the ac line voltage. The energy buffering capacitors are placed at the output of each RTI buck converter. Each converter will process 125 W. The relay is used to connect the converters in input series for 120 $V_{ac,rms}$ input voltage and in input parallel for 240 $V_{ac,rms}$.

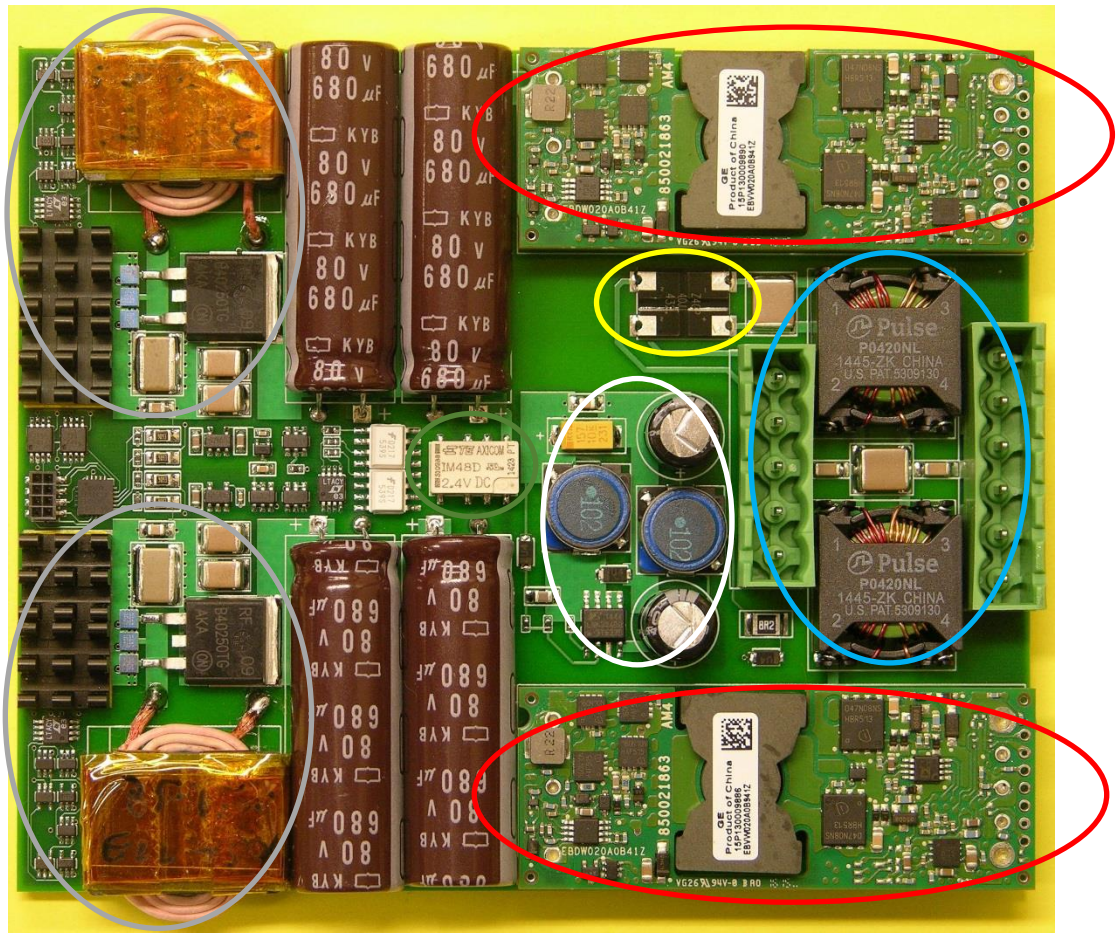


Figure 5.2. Full system board of the prototype converter utilizing a second stage based on commercial telecom converters. Top side of the board. Yellow circle: Line-frequency diode bridge. Blue: EMI filter. Orange: configuration switch network (4 pole relay). Gray: RTI buck converters (including HF control circuit). Red: second stage isolated converters. White: Power supply for control circuit (hotel power). Board layout by: Mr. David Otten.

Figures 5.3 and 5.4 show plots of efficiency and power factor vs output power for the "pfc module inputs in series" configuration of the system (used for ac line voltages of 180-240 $V_{ac,rms}$). The peak overall efficiency (from ac input to dc output) is 91.76% with 0.9577 power factor at 240 $V_{ac,rms}$ input and 257 W output. Figures 5.5 and 5.6 show sample waveforms of input voltage and current along with efficiency and power factor calculations near rated output power for 240 $V_{ac,rms}$ and 200 $V_{ac,rms}$ input voltages, respectively. Figures 5.7 and 5.8 show plots of efficiency and power factor vs output power for the "parallel" configuration of the system (used for ac line

voltages of 85-130 $V_{ac,rms}$). The peak efficiency and power factor are 90.31% and 0.9664, respectively. Figures 5.9 and 5.10 show sample waveforms for operation in parallel mode near rated power at 130 $V_{ac,rms}$ and 120 $V_{ac,rms}$ respectively. All these tests were performed with a single phase AC Power Source, the Agilent 6812B. The measurements were taken with the Yokogawa WT18000 Digital Power Analyzer. The load used is the Agilent 6060B System DC Electronic Load. Figure 5.11 shows a block diagram of the test setup.

Based on the measured results, it was concluded that using commercial converters is not very well advised for this application despite the notional attractiveness in doing so (leveraging high-volume commercial converters, providing flexibility in outputs and ease of reconfiguration, etc.). First, even with the best available commercial telecom converter efficiencies (95%), overall efficiency was lower that desired. Secondly, design with these converters was not as simple and as flexible as anticipated: getting the two converters to work with parallel outputs was a challenge, especially for the PFC modules in input-series configuration. Also there is the possibility of greater integration, better control handling, and increases in efficiency and power density by designing a custom second stage; this is the topic of the following Chapter 6.

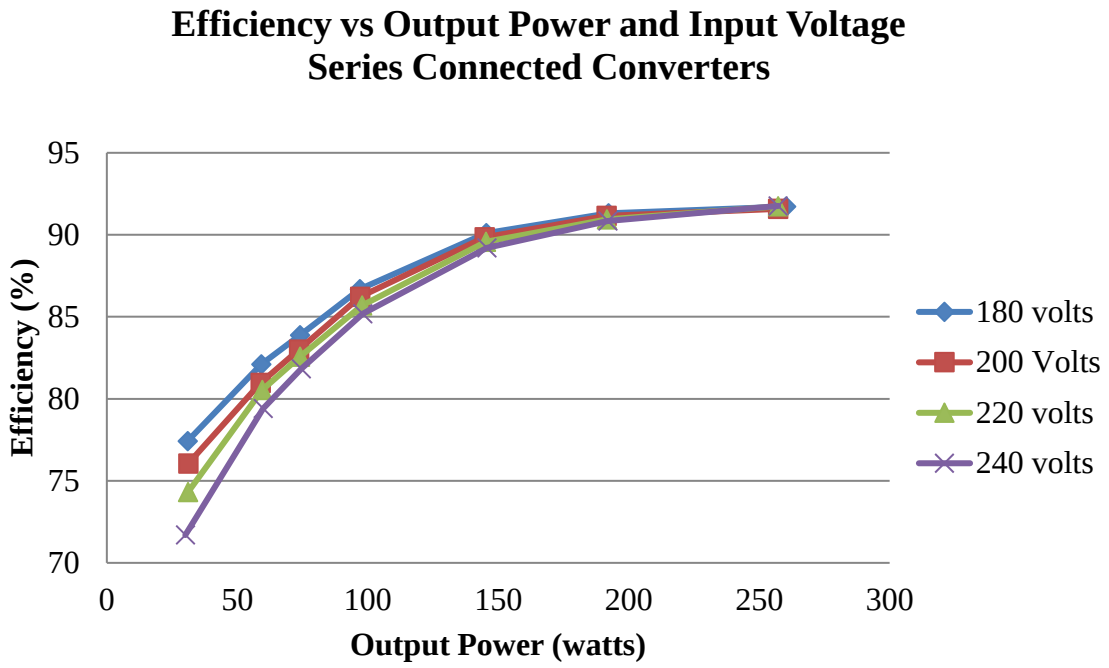


Figure 5.3. Efficiency vs output power from ac line to 24 V dc output across average output power, parameterized in ac line voltage. The data shown here are for the input-series connection of the PFC stage modules (i.e. for input voltages from 180-240 $V_{ac,rms}$) at 60 Hz. Peak efficiency is 91.76 % at 240 $V_{ac,rms}$ input and 257 W output.

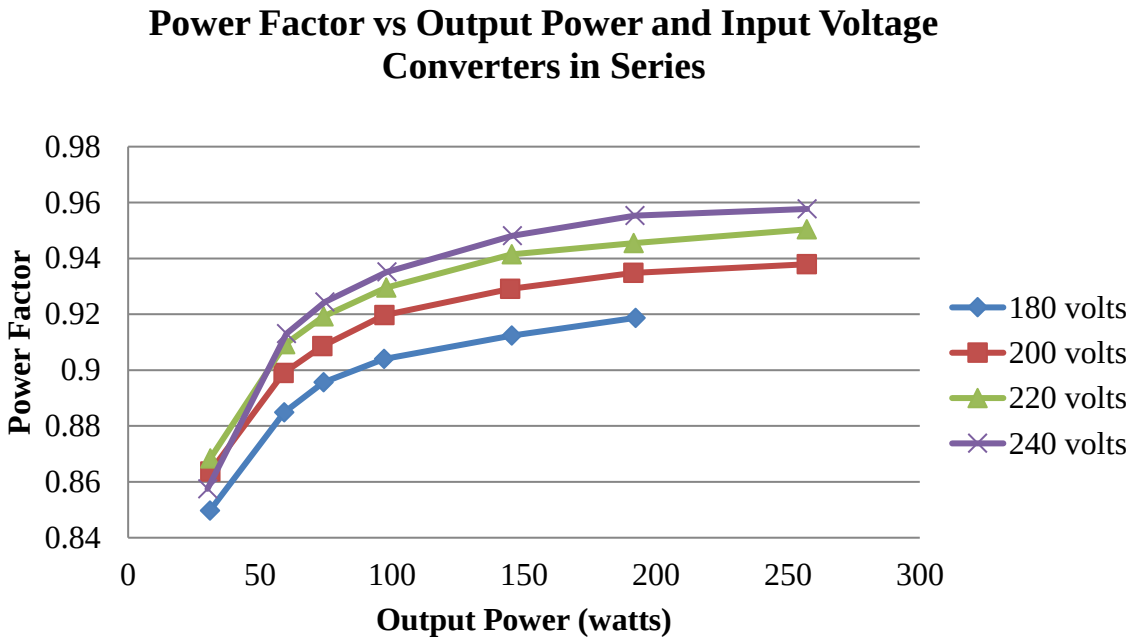


Figure 5.4. Power factor vs output power from ac line voltage to 24 V dc output across average output power, parameterized in ac line voltage. The data shown here are for the series input connection of the PFC converter modules (i.e. for input voltages from 180-240 $V_{ac,rms}$) at 60 Hz. Peak power factor is 0.9577 at 240 $V_{ac,rms}$ input and 257 W output.

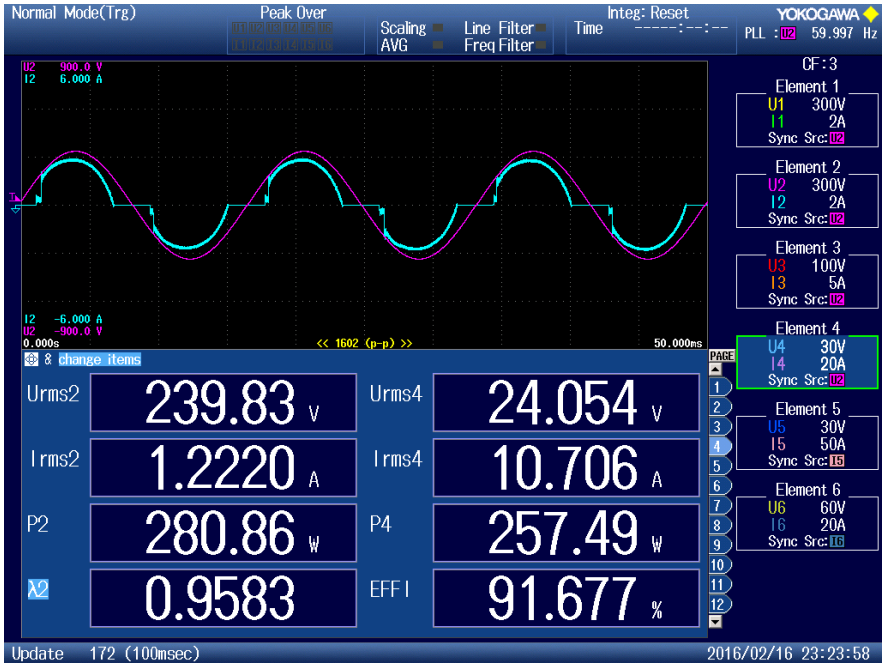


Figure 5.5. Screenshot from data measured using the Yokogawa Digital Power Analyzer. Pink: line voltage. Blue: Line current. Operating conditions: 240 $V_{ac,rms}$ input, 24 V dc output, 257.49 output power, 91.68% efficiency and 0.9583 power factor.

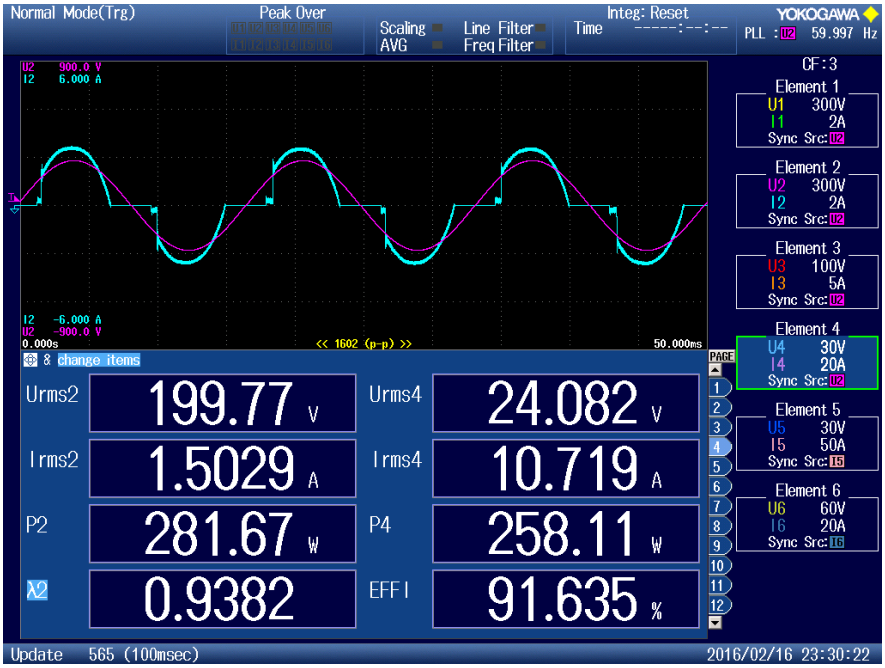


Figure 5.6. Screenshot from data measured using the Yokogawa Digital Power Analyzer. Pink: line voltage. Blue: Line current. Operating conditions: 200 $V_{ac,rms}$ input, 24 V dc output, 258.11 output power, 91.64% efficiency and 0.9382 power factor.

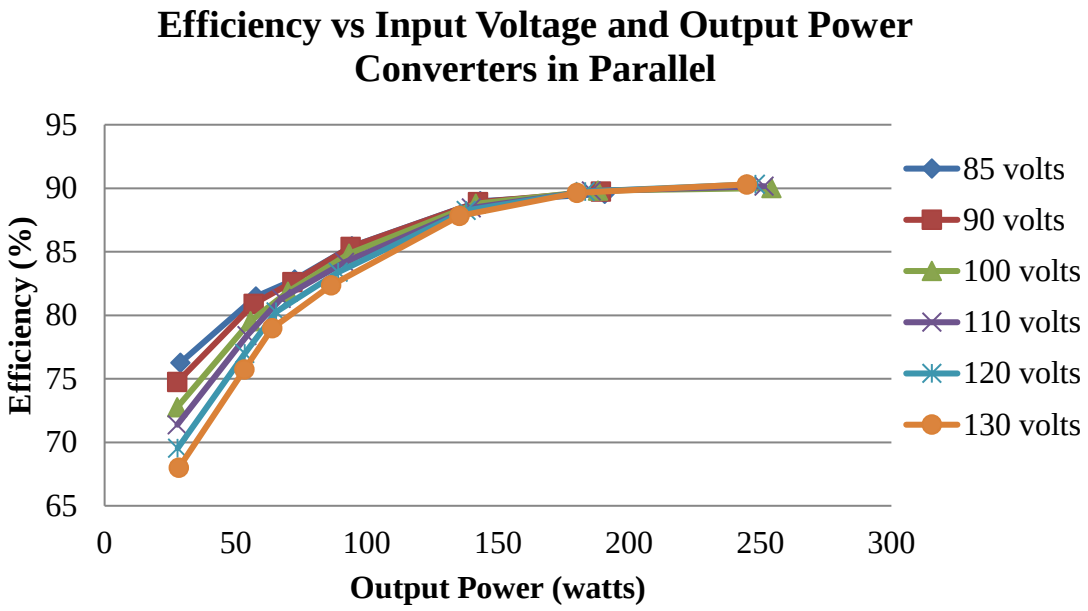


Figure 5.7. Efficiency vs output power from ac line voltage to 24 V dc output across average output power, parameterized in ac line voltage. The data shown here are for the parallel input connection of the PFC converter modules (i.e. for input voltages from 85-130 $V_{ac,rms}$) at 60 Hz. Peak efficiency is 90.31% at 120 $V_{ac,rms}$ input and 248.15 W output.

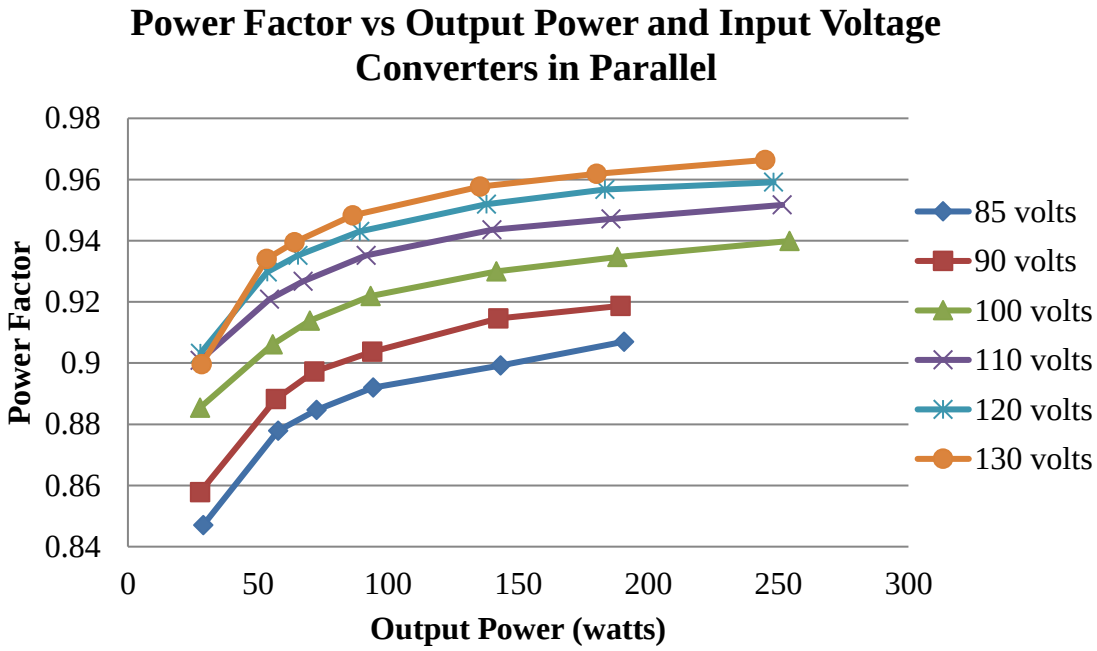


Figure 5.8. Power factor vs output power from ac line voltage to 24 V dc output across average output power, parameterized in ac line voltage. The data shown here are for the parallel input connection of the PFC converter modules (i.e. for input voltages from 85-130 $V_{ac,rms}$) at 60 Hz. Peak power factor is 0.9664 at 130 $V_{ac,rms}$ input and 244.94 W output.

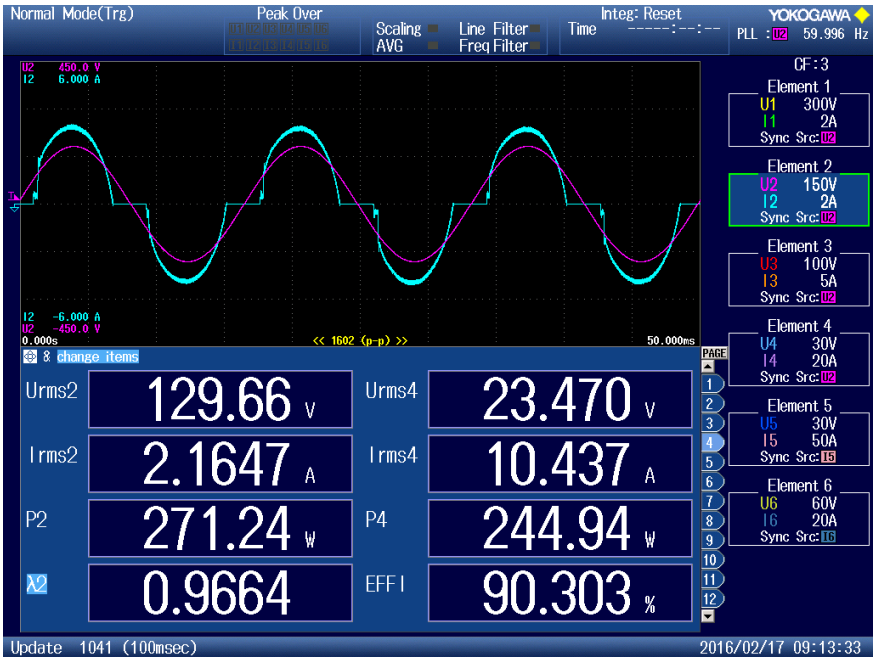


Figure 5.9. Screenshot from data measured using the Yokogawa Digital Power Analyzer. Pink: line voltage. Blue: Line current. Operating conditions: 130 $V_{ac,rms}$ input, 23.47 V dc output, 244.94 output power, 90.30% efficiency and 0.9664 power factor.

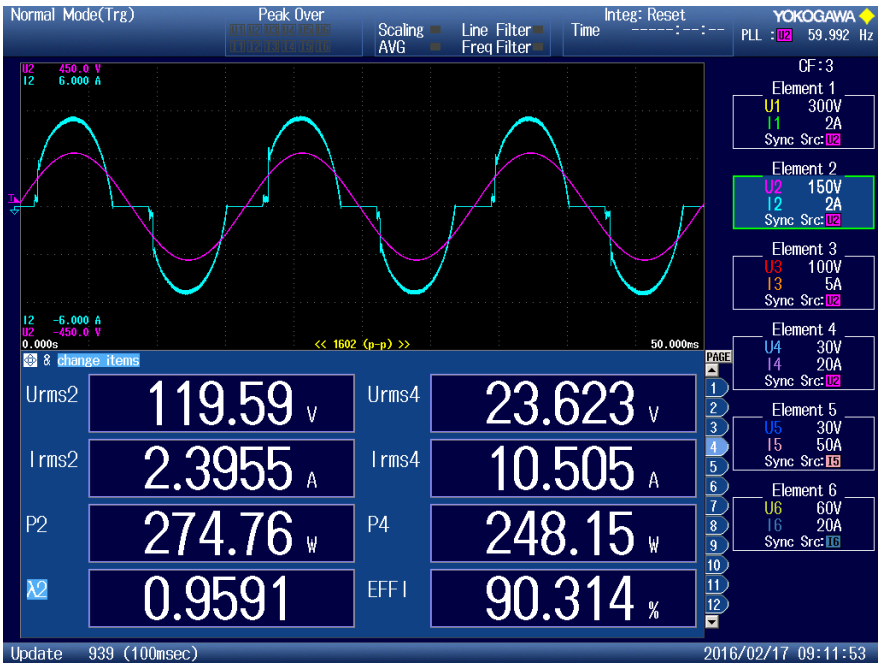


Figure 5.10. Screenshot from data measured using the Yokogawa Digital Power Analyzer. Pink: line voltage. Blue: Line current. Operating conditions: 120 $V_{ac,rms}$ input, 23.62 V dc output, 248.15 output power, 90.31% efficiency and 0.9591 power factor.

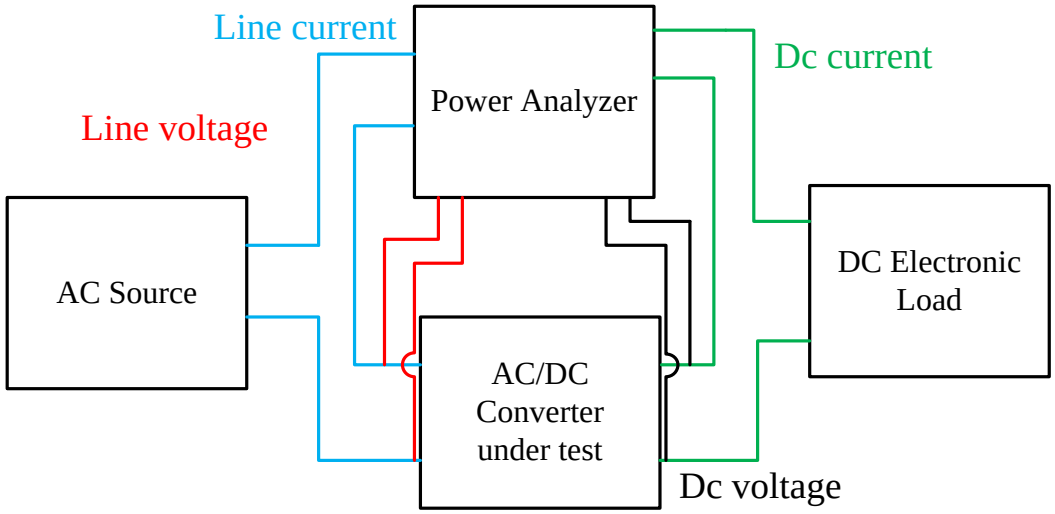


Figure 5.11. Test setup block diagram. The power analyzer reads ac input voltage and current, and the dc output voltage and current. The source used is the Agilent 6812B. The power analyzer used is the Yokogawa WT18000. The load used is the Agilent 6060B.

Chapter 6: Second Stage Converter Design, Component Selection and Performance Evaluation

The previous chapter described the use of commercial telecom "brick" converters to implement the second stage, which provides isolation, voltage conversion and regulation from the two PFC stage outputs to the system output. In this chapter we develop a custom second stage converter that serves this function, but achieves a much higher performance level. The converter requirements are the same: two inputs which are power combined to support a single output, provision of isolation and regulation of the output, and the ability to draw energy from the PFC stage over a wide input voltage range during a hold-up time event as the energy buffer capacitors discharge.

6.1 Topology selection approach

We desire a second stage design that operates from two matched-voltage inputs and provides a single output, as shown in Fig. 6.1. The converter should operate with maximum efficiency near the nominal output voltage (24 V) and the nominal design input voltage (~72 V) with modest

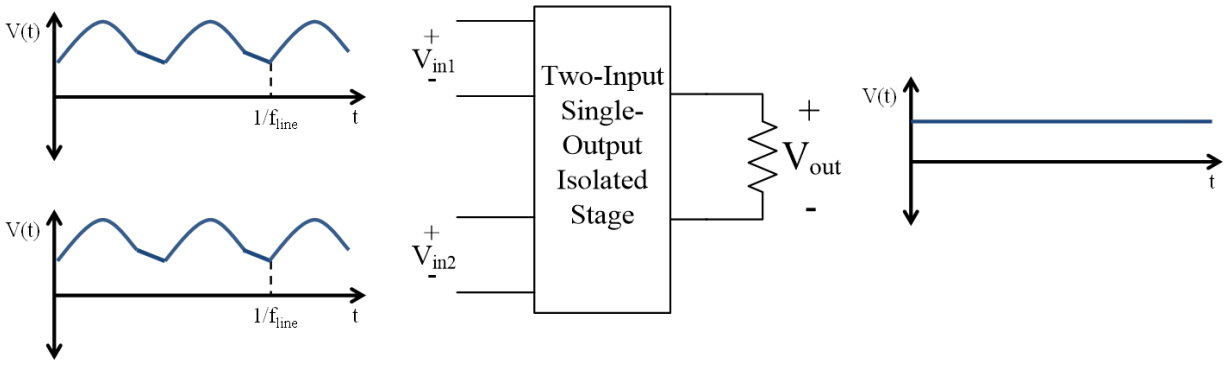


Figure 6.1. Diagram representing the functionality of the dc/dc isolation stage. The converter has two identical inputs with a dc value (72 V) and a small ripple at twice line frequency (+/- 6%). The output voltage is dc at 24 V. The converter should be able to keep the output power constant over a line cycle during a transient event.

voltage range in steady state (nominally, 69 V - 75 V) but needs to be operable (transiently) down to low input voltages (e.g., 36 V) during holdup events. It is also highly desirable if the stage can naturally balance voltage between the two inputs, as this eliminates the need to utilize an explicit voltage balancing circuit to maintain energy balance among the two energy buffer capacitors.

A power stage providing high efficiency and power density was desired, suggesting the use of relatively high switching frequencies and Zero-Voltage Soft Switching. The analysis and downselect for the second stage structure focused on three inter-related aspects: 1) the type of ac "tank" or impedance network used; 2) the types of inverters and rectifiers to be used (e.g., full-bridge, half-bridge, stacked-bridge, full-wave half-bridge, resonant, etc.); and 3) The means of achieving voltage balancing among the two inputs. Each of these considerations are addressed here separately.

We only considered converters providing zero-voltage switching (ZVS) in order to achieve high operating frequency and small size. Among such converters, we considered both resonant converters and "active bridge" converters. In terms of the type of "tank" network or intermediate energy storage / filtering network, many options are possible, with the type of tank network also inter-related with how power is controlled. Typical resonant converters (e.g., series-, parallel-, LCC series/parallel, LLC) with diode rectifiers operate dominantly under frequency control (e.g., [59-65]), though active rectifier varieties can also incorporate phase-shift control between the inverter and rectifier (e.g., [66]). For resonant converters we focused on use of frequency as the dominant control variable, while for "active bridge" converters (e.g., [61]) we focused on phase shift between inverter and rectifier as the dominant control variable. Because of the relatively low output voltage, we further only considered designs with "synchronous rectification", or actively-controlled rectifier devices, in order to achieve high efficiency.

Among resonant converters (which utilize sinusoidal or quasi-sinusoidal intermediate waveforms), the series-resonant converter (e.g., [59,66]) has the benefit of few magnetic components, with the resonant inductor potentially being able to be incorporated into the transformer, and with no additional inductor required for the rectifier (i.e., a voltage-loaded rectifier). (Thus, a single magnetic component can potentially be used.) However, a key disadvantage for the present purpose is that this converter has the highest "power factor" of transferring energy through the tank – and hence lowest conduction loss – when it is operated near its maximum input-to-output voltage gain (i.e., operated near the resonant frequency with fundamental ac voltage and current waveforms nearly in phase in the ac tank and a normalized voltage gain near unity.) Unfortunately, for the design under consideration, maximum conversion gain is only required during rare "holdup" events, so the converter must be designed to operate at a "suboptimal" operating point (with higher conduction losses) for its normal operating condition. For this reason, the series-resonant converter was not considered further.

The traditional LCC parallel and series-parallel converters (e.g., [61]) do not have the above limitation on operating point, but were not considered owing to their use of "current loaded" rectifiers, requiring an additional inductor on the low-voltage, high-current side. Other higher-order resonant converters, such as the ICN- and RCN-based converters (e.g., [63-65]) also typically require larger numbers of magnetic components, and the advantages these designs bring (operating effectively across wide input and/or output voltage ranges) were deemed to be relatively unimportant in this application. While a large number of variants exist with high tank order (e.g., see [67]), many of these are not particularly advantageous in the proposed application owing to high component count and failure to absorb key parasitics into the system operation.

The LLC converter, however, offers a small number of magnetic components, including the ability to absorb the key resonant magnetics into the transformer for a single-magnetic-component design (e.g., [60,68,69]). While the "full-wave center-tapped" rectifier variant of the LLC converter commonly-used for voltage step down was considered to become undesirable when moving into the HF frequency range (owing to issues arising from leakage inductance between the secondaries), a full-bridge or voltage doubler synchronous rectifier version appears to be quite viable. Moreover, as this tank structure can maintain good efficiency over a relatively wide input-voltage range and power level, the LLC converter was considered to be perhaps the best among the common resonant converter topologies.

The "active-bridge" class of converters has several benefits. Key among these is that this converter can operate at extreme high efficiency and power density for a designated voltage conversion ratio, and is capable of delivering full power at significantly lower input-to-output voltage conversion ratios (by increasing phase shift). This is well-suited to the operating requirements of the proposed system, in which one operates near a specified voltage conversion ratio under normal circumstances, but may need to operate at much higher conversion ratios during a holdup transient event (only). One reason for this high performance near the specified nominal voltage conversion ratio is that when operated with low phase shift (for a voltage conversion ratio close to the design condition), the current waveforms are approximately trapezoidal and energy transfer is provided at both the fundamental frequency and the third harmonic, yielding lower rms currents for a given power level than with many resonant converters. (i.e., the approximately trapezoidal current waveform provides high power transfer per unit conduction loss.) Moreover, unlike resonant converters where there is some resonant impedance cancelling or voltage attenuation used to provide the frequency selectivity used for frequency control, none is required

in active bridge converters; this tends to providing better utilization of the magnetics for energy storage. Lastly, as with the LLC converter it is possible to utilize a single magnetic component implementing a "leakage transformer" (e.g. [30]).

An advantage of the "active bridge" class of designs relative to resonant designs is that the resonant converters exhibit a high degree of sensitivity to the timing of the active rectifier relative to the active inverter, and this sensitivity becomes increasingly important at higher frequencies. (The sinusoidal nature of the intermediate ac waveforms with switching near the current zero crossing means that a small timing error can yield a large current error at the switching instant.) In particular, because most resonant converter designs seek to operate the active rectifier to behave like diodes, very careful control of rectifier timing becomes increasingly important and difficult as frequency moves into the multi-MHz range. (The design of [70] addresses this problem, for example, but at the expense of regulation capability.) By contrast, the current slopes at the switching instant tend to be smaller in an active bridge converter, and the timing of the rectifier with respect to the inverter is already under active control. In consideration of this last aspect along with the strengths of the dual active bridge converter in terms of conduction loss, it was decided that a dual-active bridge structure utilizing a single magnetic component offered the best opportunity for both high density and efficiency, and so a preliminary downselect to this class of topology was made (pending detailed design and testing to confirm its strengths in this case and identify any weaknesses.)

Since a goal is to build a two-input second stage, a question arises of how to combine power and how to realize voltage balancing among the two inputs. One approach, illustrated in Fig. 6.2 (a), is to utilize two transformer windings and two inverters, and utilize energy transfer through the windings to maintain voltage balance. The two primary windings are wound across the same

core leg (i.e. they share the same flux) which helps with load balancing. A second approach, illustrated in Fig. 6.2 (b) is to utilize two transformer windings but use switched-capacitor energy transfer to maintain voltage balance between the two inputs. (This is done in the dc-dc converter of [71] for example.) A third strategy (Fig. 6.3), is to use a single transformer winding, with capacitor connected, synchronously-driven inverters to combine power from the two inverters and provide switched-capacitor energy transfer to maintain voltage balance among them. This type of energy transfer is used in so-called "multitrack" converters [13,71]. Given that the second and third strategies require a more accurate degree of timing between the two inverters, and given the benefit of distributing current among multiple windings at HF for efficiency reasons, it was decided to implement the first approach (with the second as a backup if energy transfer between inputs via the transformer were insufficiently efficient.)

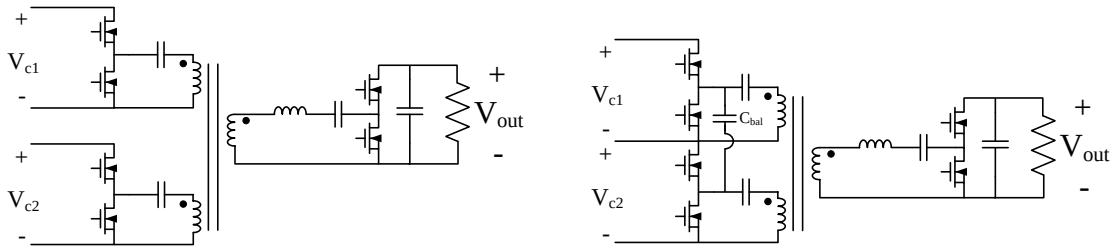


Figure 6.2 (a) A first example implementation of a customized second stage having two inputs (of equal voltage) and an isolated output, utilizing a magnetic core with a single magnetic flux path. The two inverters can be switched synchronously. Different tank structures (e.g., DAB, series resonant, LLC, …) may be utilized to achieve high efficiency and power density, and different inverter or rectifier topologies (e.g., a full-bridge rectifier or center-tapped full-wave rectifier) can likewise be used. **(b)** A second example implementation of a customized second stage (shown with the two inverters stacked as for the second PFC stage design). Capacitor C_{bal} allows efficient voltage balance between V_{c1} and V_{c2}, and enables equal current balance of the transformer windings for high efficiency.

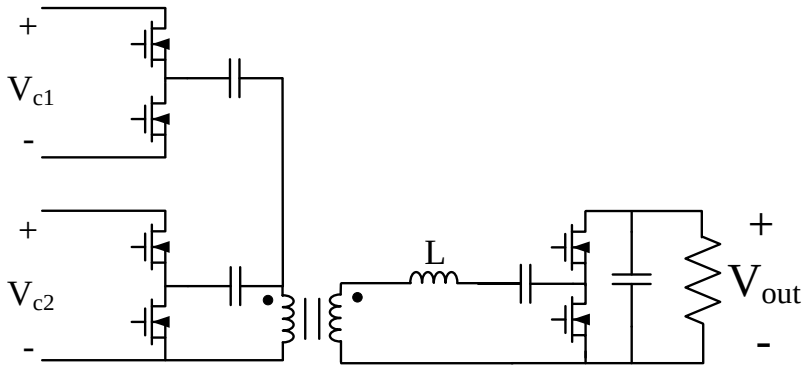


Figure 6.3. A third possible implementation of the customized second stage converter. This implementation has the benefit of only needing a two-winding transformer winding and uses capacitors to couple both input inverters. With proper timing, voltage balancing is provided for the two input branches.

A last question is the selection of inverter and rectifier structures (e.g., half-, full-, stacked bridges, etc.). For operational simplicity and avoidance of design sensitivity, it was decided to not consider resonant inverters and rectifiers (which have low component counts and simple single-switch drive, but have relatively high stresses and frequency sensitivity [46,72]). Half bridge inverters and stacked-bridge inverters offer a lower dc-to-ac gain than full-bridge inverters [30,69] by a factor of two. Likewise, half-bridge (voltage doubler) rectifiers offer a higher ac-to-dc gain than full-bridge rectifiers. (The more recently-developed concept of "Variable-Inverter-Rectifier-Transformer" or VIRT designs further increases opportunities in shaping conversion ratios by co-design of inverter, transformer and rectifier structures [73], though was not considered for this project at the time the proposed design was developed.) The inverter and rectifier topologies can thus be selected to change the required transformer turns ratio. In the case of high numbers of turns on both the primary and secondary, changing the transformer turns ratio is not a major advantage. However, in HF designs, which may have very few turns, selecting the appropriate turns ratio can have a significant effect on how easily a transformer design can be implemented. Consequently, we decided to select the specific inverter and rectifier topologies to yield a desirable number of

turns on the transformer for good implementation of the "leakage transformer" as a single, compact and efficient magnetic component. This thus resulted in the "downselected" converter that was fully developed, the one shown in Fig. 6.2 (a).

6.2 Circuit operation

Here we consider topology in Fig. 6.2 (a) (with half bridge rectifier) and its variant in Fig. 6.4 (with full bridge rectifier). They operate similarly, but each one requires a different turns ratio due to the different gain from the rectifier. The operation of this converter is similar to that of a dual active bridge (DAB) [61,62]. The rectifier (right side of the transformer) is phase shifted with respect to the half bridge inverters (left side of the transformer). This phase shift between the primary and secondary voltages creates a trapezoidal current using the transformer's leakage inductance. Figure 6.5 shows idealized waveforms of the converter, referencing the variables highlighted in Fig 6.4, and assuming the two dc input voltages are identical and the switching of the two inverters are identical. The output power of the converter is described in the following equation:

$$P_o = \frac{N * V_{in} * V_O}{2 * \omega * L} * \Phi * \left(1 - \frac{abs(\Phi)}{\pi}\right) \qquad (6.1)$$

where N is the 1:N turns ratio of the transformer, V_{in} and V_O are the input and output voltages, ω is the switching frequency in radians, L is the equivalent inductance referred to the secondary (including transformer leakage and any additional inductance) and Φ is the phase shift (in radians) between the inverters and the rectifier.

It is important that the difference between the (transformer-scaled) magnitudes of $v_{p,n}$ and v_s (from Fig. 6.4) is minimized to reduce the transformer RMS current. If there is a voltage imbalance,

the transformer input and output current waveform distort from a pure trapezoidal wave and transformer RMS current increases for the same output power. This behavior is shown in Fig. 6.6. Thus the circuit operates very efficiently for a fixed input voltage (with low ripple) but, by controlling the phase shift, it is still capable of delivering power across a wide input voltage range.

Another important characteristic of this converter is its zero-voltage switching (ZVS) capability for both the inverter and the rectifier. During the switch dead time part of the cycle, transformer current charges one switch capacitance voltage and discharge its counterpart so that the incoming FET turns on at a reduced voltage. With sufficient current, the switch voltage will discharge all the way to zero. The minimum switch current needed for ZVS is given by [62]:

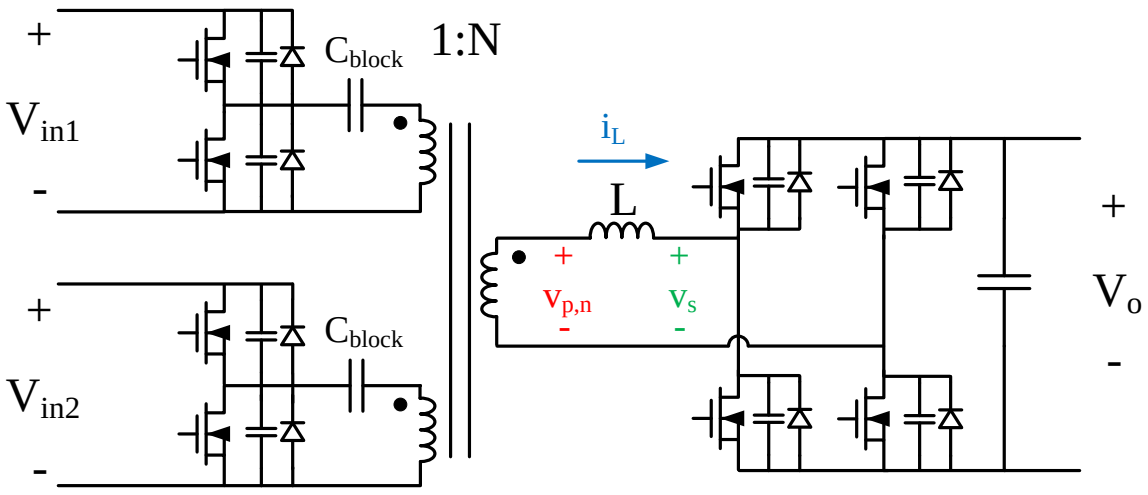


Figure 6.4. Two-input single-output isolated dc-dc converter. The inverters consist of 2 half bridges while the rectifier is a full bridge. The converter works similar to a dual active bridge converter [61,62]. The inductance shown is the leakage inductance of the transformer referred to the secondary.

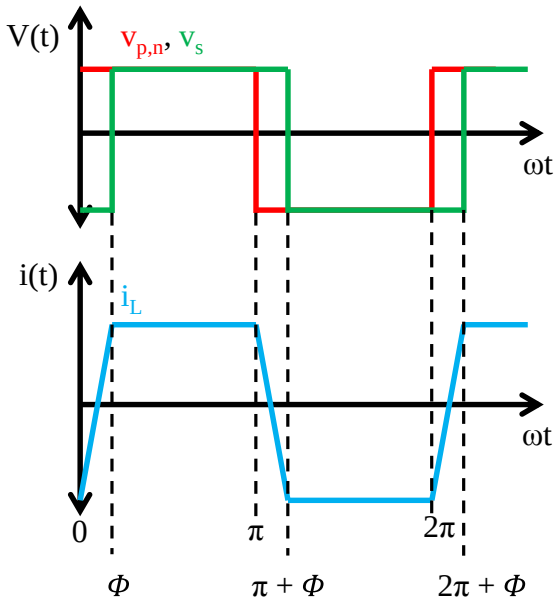


Figure 6.5. Idealized converter waveforms. The red waveform is the primary voltage referred to the secondary, $v_{p,n}$ from Fig. 6.4, the green waveform is the secondary winding voltage, v_s from Fig. 6.4, and the blue waveform is the secondary current, i_L. Φ is the phase shift. The trapezoidal current minimizes rms currents for very high efficiency.

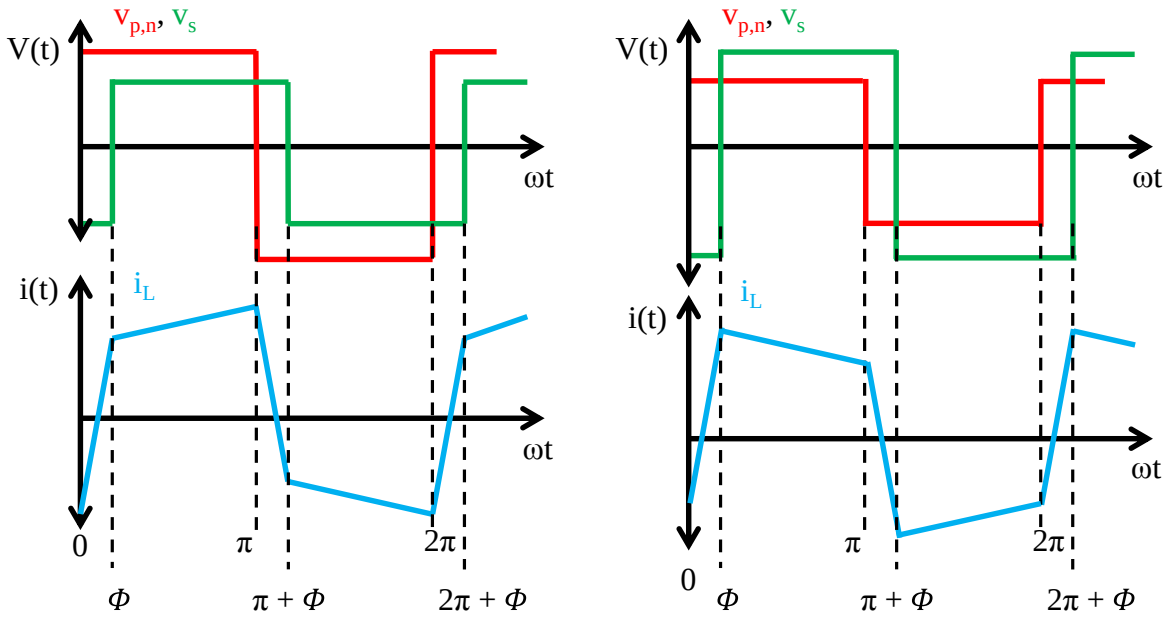


Figure 6.6. Converter waveforms for input and output voltage imbalance. On the left, $N * V_{in} > V_o$ and on the right $N * V_{in} < V_o$. The voltage imbalance causes increased transformer RMS current for a given output power.

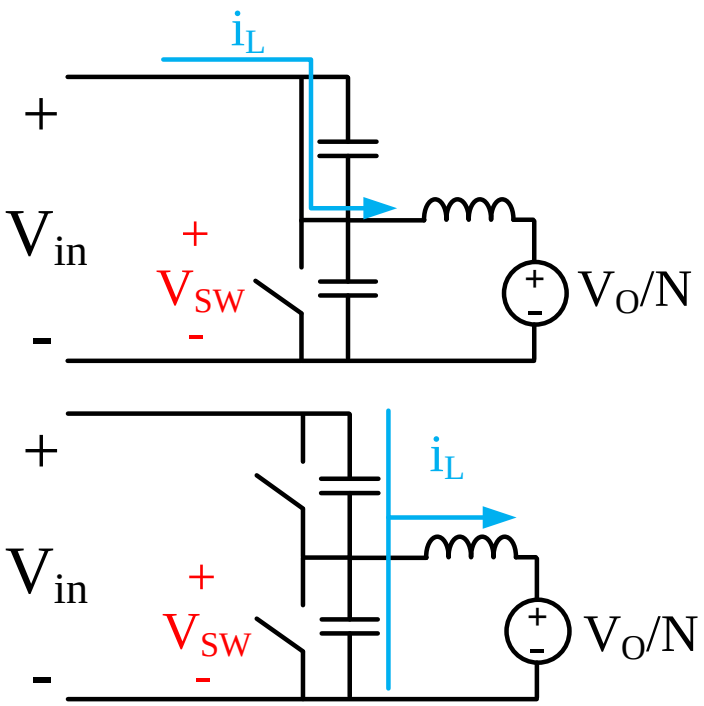


Figure 6.7. Figure detailing the transition from switches conducting (top) into dead time (bottom). During dead time, the parasitic capacitance and the inductance resonate.

$$I_{SW,min} = \frac{2*\sqrt{V_{in}*V_O/N}}{Z_O} \qquad (6.2)$$

where Z_O is the characteristic impedance of the transformer equivalent inductance and the switch equivalent capacitance ($Z_O = \sqrt{L_{eq}/C_{eq}}$). This equation is valid for both the inverter and rectifier switches with appropriate values of L_{eq} and C_{eq}. As a consequence of this minimum current, ZVS is lost at light loads. The load range for ZVS can be extended by increasing magnetizing current at the cost of efficiency during heavy loads.

Up to now, the presence and effect of finite magnetizing inductance and magnetizing current has not been considered. The magnetizing current is a function of the magnetizing inductance, switching frequency and input voltage and is independent of the load. The magnetizing current flows only through the inverter and primary windings of the transformer. Therefore it can be useful

to extend primary-side switches ZVS range: as long as the sum of the primary-referred load current and the magnetizing current is higher than the minimum needed for ZVS, soft switching can be achieved.

The magnetizing current of the transformer can be changed by adding an air gap to the transformer. This reduces the magnetizing inductance and increases the magnetizing current. However, extending the ZVS range comes at a cost: full load efficiency is reduced because more current (that does not reach the load) will flow through the inverter switches and primary winding, increasing the conduction loss. For this design, we did not add any air gap to the transformer for two reasons: first, because we want to maximize full load efficiency and, second, after analysis, simulations and experiments it was found that no thermal limits were reached due to loss of ZVS. Magnetizing inductance was maximized so that the magnetizing current is minimized. However, there is another method used to increase light load efficiency, developed in Chapter 7, that uses a new control method and does not sacrifices heavy-load efficiency.

The performance of the proposed second-stage topology with two different rectifier configurations (Figs. 6.2 (a) and 6.4) has been investigated in detail. The half bridge rectifier itself provides a voltage step up factor of 2 (i.e., operating as a voltage doubler), thus reducing the number of turns needed on the secondary of the transformer by half when compared to the full bridge version (Fig. 6.4). Having less turns reduces ac winding resistance. On the other hand, half the turns on the secondary means the secondary RMS current is doubled. The two variants are analyzed and compared to select the optimal one for this application.

The transformer dominates the size of this circuit and special attention is given to its design. Copper and core losses have been minimized by using the appropriate litz wire and core material. A Matlab code (found on Appendix D) was developed that sweeps through all transformer

parameters (i.e. core material, core geometry, litz wire type, number of turns, and switching frequency) and calculates winding and core losses. From here one can select the best design for the application. Winding losses are calculated using the model for ac resistance found in [45], and core losses are calculated from the core material datasheet. This algorithm for transformer design is very similar to the one discussed in chapter 3 for inductor design , and is detailed in the next section of this chapter.

First, the two circuit variants are analyzed. The losses on the FETs were calculated and the difference between half bridge and full bridge losses was found to be negligible compared to the transformer losses. Thus, the selection of the rectifier configuration was based on transformer losses alone. Figure 6.8 shows the transformer losses for both circuit variants. From this plot it is clear that the full bridge rectifier has lower transformer loss. Considering a full window area of copper, the conduction losses would be the same in both cases if only dc resistance is taken into account. However, proximity and skin effects increase the loss at the frequencies of interest. For each transformer design there is an optimal litz wire configuration that minimizes ac resistance. It was found that in all realizable designs the full bridge rectifier transformer (3:2 turns ratio and 12 A RMS of secondary current) had lower losses than the half bridge transformer (3:1 turns ratio and 24 A RMS secondary current). Thus, despite its increased component count, the full-bridge rectifier configuration was selected and employed. In the next section we discuss the modeling of transformer losses.

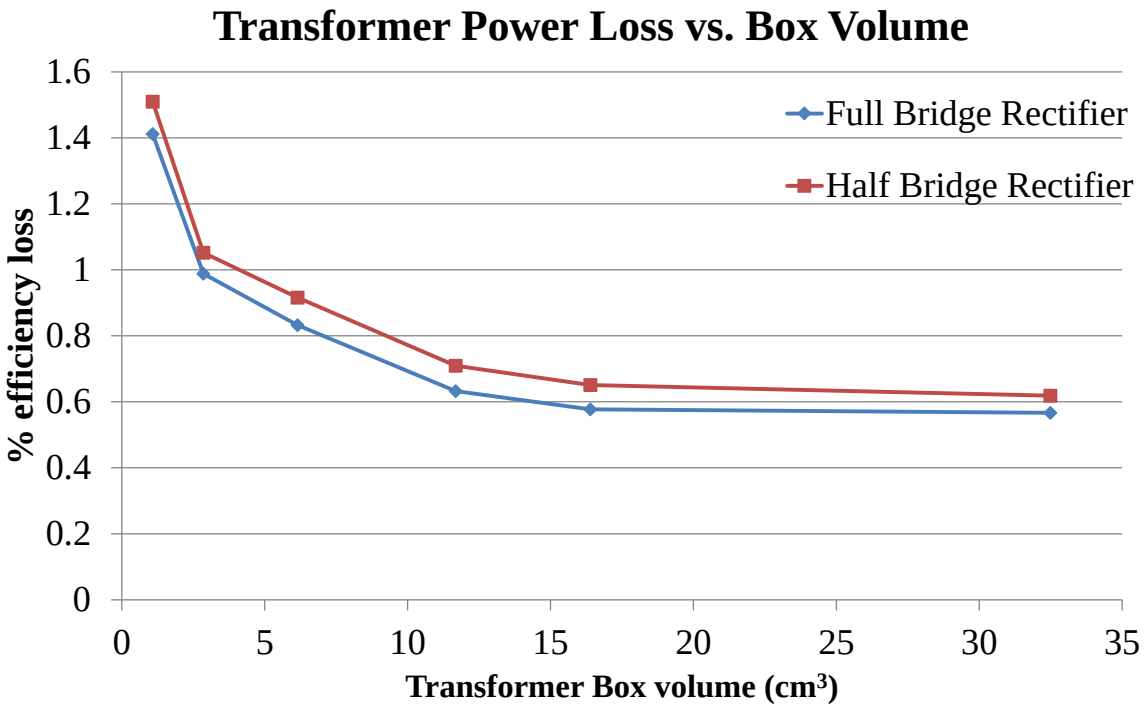


Figure 6.8. Transformer power loss vs. box volume vs. rectifier configuration. This plots shows the difference in transformer losses for the two rectifier variants. The transformer losses are the sum of winding and core losses. In this example, the transformer loss is evaluated at 250 W (full power), with a switching frequency of 500 kHz and utilizing N49 core material from Epcos. The turns ratio for the full bridge design is 3:2 and for the half bridge is 3:1.

6.3 Transformer loss calculation

Transformer loss is divided into winding loss and core loss. Details on how these are calculated are below:

6.3.1 Winding loss

Winding loss is calculated using the method described in [45]:

$$P_{Wind} = F_r {I_{ac,RMS}}^2 R_{dc} \qquad (6.3)$$

where *Fr* is the ac resistance factor, $I_{ac,RMS}$ is the RMS value of the winding current, and R_{dc} is the dc resistance of the wire. Fr is defined as:

$$F_r = 1 + \frac{\pi^2 \omega^2 \mu_o^2 N^2 n^2 d_c^6}{768 \rho_c^2 b_c^2} \quad (6.4)$$

where ω is the radian frequency of the current, n is the number of strands, N is the number of turns, d_c is the diameter of the copper in each strand, ρ_c is the resistivity of the copper conductor (used the resistivity of copper at 125º C, 2.5e-8 Ω-m), and b_c is the breadth of the core window area (in this case, the height of the E core leg). The assumptions made in order for this equation to be useful are: strand diameter is small compared to a skin depth, each litz wire strand is treated as a "layer", each strand conducts equal amounts of current (This assumption is equivalent to assuming that the bundle-level construction has been chosen properly to control bundle-level proximity and skin effects [45].), and the strands of all litz bundles are uniformly distributed in the window, as they would be in a single winding using nN turns of wire the diameter of the litz strands. Equation (6.4), as described in [45], also assumes the full window area of your core is utilized and that no air gap is present (which would create undesirable fringing fields).

The value of $I_{ac,RMS}$ is found by taking the fundamental component of the current waveform. From this fundamental component, the RMS value is extracted for use in Equation (6.3). The winding loss is calculated separately for the primary and secondary windings, and also includes the magnetizing current. The value for ω is taken as the fundamental frequency of the transformer current.

During nominal operation, the converter must supply 250 W to the 24 V load, which translates to an output current of 10.5 A. The full bridge rectifier must deliver a constant 10.5 A, which in turn translates to a transformer secondary current of a square wave with 10.5 A of amplitude. The primary current can be calculated by adding the magnetizing current and the secondary current

referred to the primary side. The magnetizing current is approximated as a triangle wave with peak value of:

$$I_{mag} = \frac{V_{in}}{4L_{mag}} * \frac{T}{2} \quad (6.5)$$

where V_{in} is the input voltage to the dc/dc converter, T is the period of the switching cycle, and L_{mag} is the magnetizing inductance. Once the primary and secondary currents are calculated a fundamental frequency approximation is made and the winding loss is calculated according to (6.3).

6.3.2 Core loss

To calculate core loss, we utilize a simple approximation of the core flux using the volts-seconds applied to the transformer, and apply Steinmetz equations loss calculations. We first obtain Steinmetz parameters using the power loss density vs peak flux density curves available in each material's datasheet (for sinusoidal excitation). (For some materials, we rely on data measured in our own group [44].)

For example, Ferroxcube material 3F45 has a power loss density (in kW/m^3) vs peak flux density (in mT) for sinusoidal excitations shown at 2, 1 and 0.5 MHz frequencies. From each data plot one can extract Steinmetz parameters for calculating core loss. The Steinmetz formula used is:

$$P_{core} = V_c K {B_{pk}}^y \quad (6.6)$$

where V_c is the magnetic core volume, B_{pk} is the peak flux density, and K and y are constants that depend on the magnetic material composition, its temperature and drive frequency. Tables for the core materials and core loss parameters used are provided in Appendix E.

The peak flux density of the transformer is:

$$B_{pk} = \frac{V_{in}}{N_p * A_e} * \frac{T}{2} \quad (6.7)$$

where V_{in} is the input voltage to the dc/dc converter, T is the period of the switching cycle, N_p is the number of turns on the primary winding, and A_e is the cross sectional area of the core. In calculating core loss, we approximate the core flux waveform as a sinusoid having the same peak flux density as the core flux (i.e., approximate the triangular flux density as a sinusoid of the same peak value.)

By adding the core and winding loss, we estimate power dissipation. Furthermore, if we estimate the core thermal resistance using Eqn. (3.13), we can use this power loss to estimate temperature rise.

6.4 Transformer design algorithm

This algorithm is very similar to the one used in Chapter 3 to evaluate inductor designs. The flowchart is shown in Fig. 6.9. The script goes through a pre-defined list of transformer parameters: core material, core geometry, litz wire type (strand diameter and number of strands), number of turns, and switching frequency. (The lists of parameters are shown in Table 1.) It selects one of each parameter and synthesizes a transformer. The transformer losses are evaluated and the temperature rise is estimated. Then one parameter is changed, a new transformer is synthesized and all calculations are done again. This continues until all possible combinations of parameters are evaluated. The script is able to evaluate the performance of many transformers in a relatively short amount of time. The final transformer design is selected based on loss and volume constraints. The only constant among all transformer design is the turns ratio of 3:2.

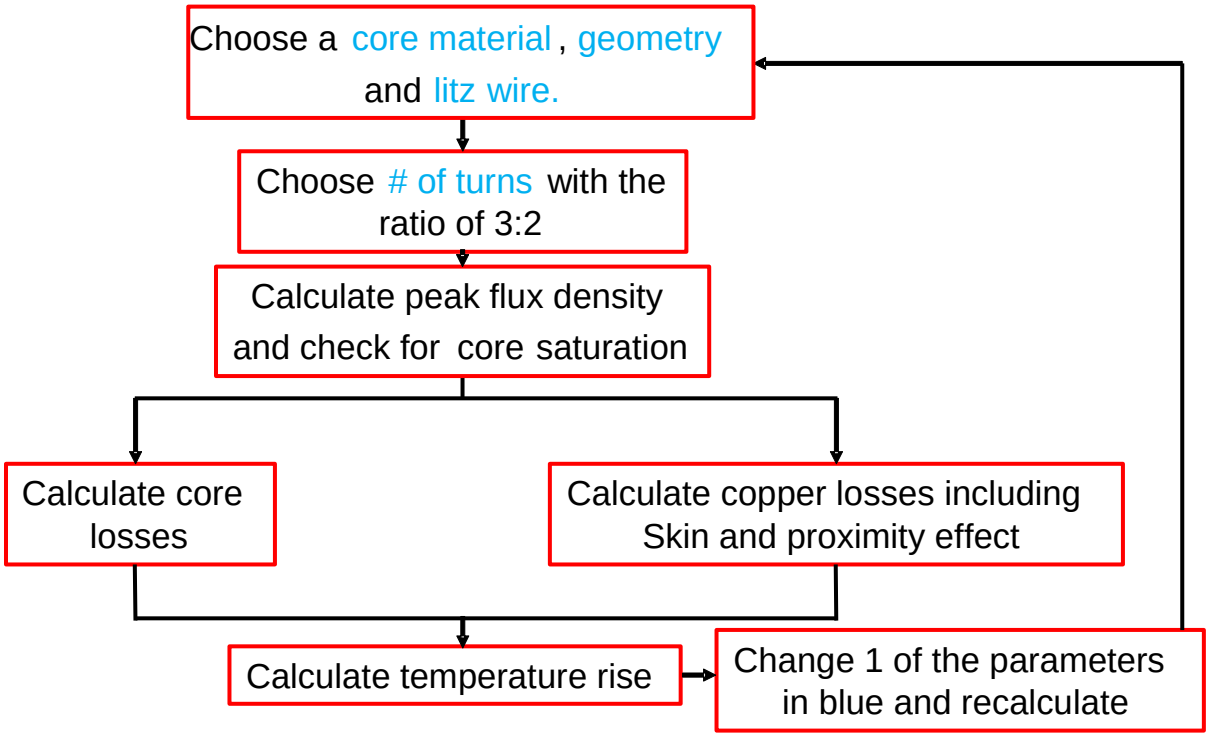


Figure 6.9. Flowchart showing the transformer design algorithm. The algorithm synthesizes transformers by selecting one of each: core material, geometry, litz wire and number of turns. Then the transformer losses are calculated and the temperature rise is estimated. Finally the algorithm changes one of the parameters (e.g. number of litz wire strands), synthesizes a new transformer and recalculates all parameters. The code finishes running after it has gone through all the pre-defined values.

Table 6.1. List of parameters used to synthesize various transformers using the algorithm described in Fig. 6.9.

Core material	**Geometry**	**Litz wire gauges (AWG)**	**Litz wire strands**	**Switching frequency (Hz)**
3F45, DMR51, 3F5, N49 and 3C96	E18, E22, E32, E38, E43, E58	40, 42, 44, 46, 48, 50, 52	from 10 strands to 1000 in steps of 10.	300k, 500k, and 1 MHz

6.5 Transformer design

As stated above, a Matlab script (provided in Appendix D) using the algorithm and loss calculations detailed in the previous sections was developed to calculate transformer losses for different designs. The relevant results from the script can be seen in Fig. 6.10. There are various designs that are predicted to yield 1 % efficiency loss at full load (i.e. less than 2.5 W of dissipation). The switching frequency of the converter is selected taking into account transformer loss and light load operation of the converter.

Based on modeling and testing of multiple prototype transformers, a design using the DMR51 core material with the shape E22 was selected for our transformer, which will be operating with a switching frequency of 1 MHz. (Operating at 1 MHz also helps us reduce the leakage inductance required to deliver our desired output power.) The construction of the transformer can be seen in Fig. 6.11. Two E22 core-halves were used (as opposed to the typical E-I pair) because the extra window area provided space for more copper in the high-current secondary, lowering overall ac resistance. Of note is that the extra height added by the second E shape is still under the dominating height, the energy buffering capacitors. A Litz wire winding, 1000 strands of 48 AWG, or (48/1000) was used for the transformer, with both primaries having 3 turns each and the secondary having 2 turns of two 48/1000 Litz wires in parallel, all wrapped around the center post. Each winding is wound in a single layer of either 3 turns (primaries) or 2 turns (secondary). There is Kapton tape (with thickness of 1 mil, ~6 kV of insulation) between each primary and the secondaries. There is no spacer used in the transformer. Note that the construction technique, with the two primaries on the outside and the secondary on the inside, yields complete interleaving, justifying the loss model used above.

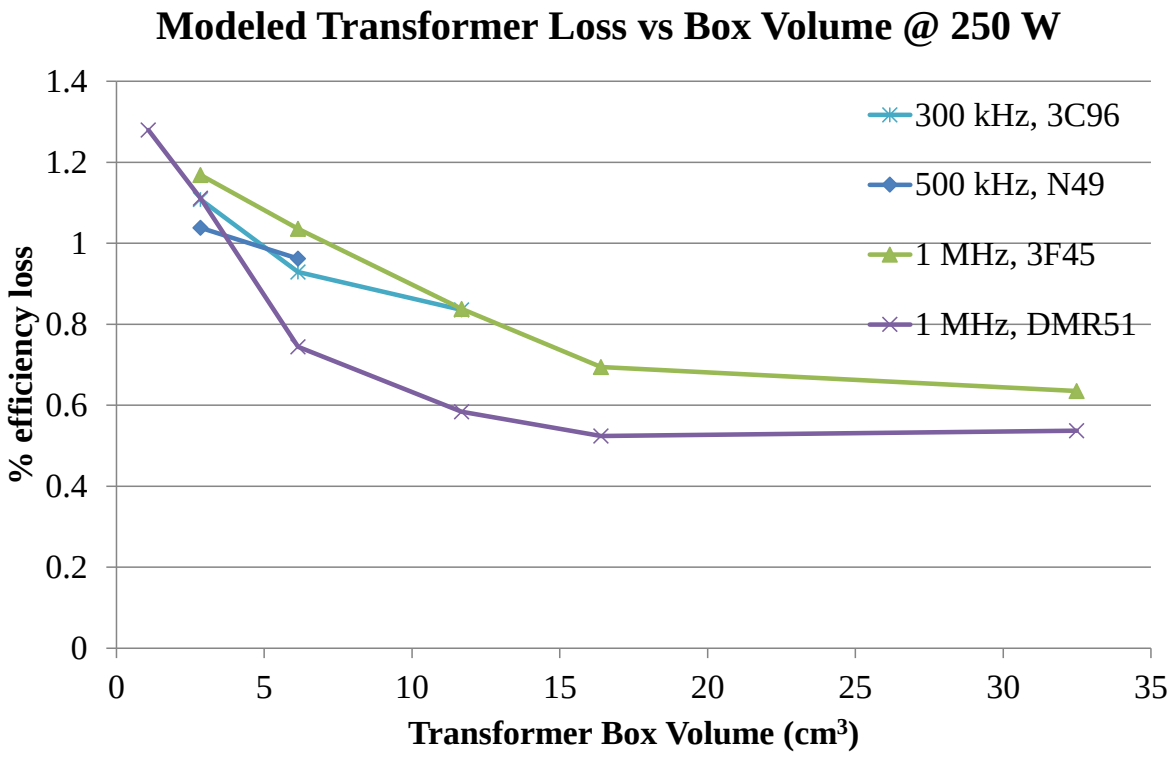


Figure 6.10. Modeled Transformer power loss vs. box volume for different materials and operating frequencies. Each data point on the x axis corresponds to a different core geometry; in order: E18, E22, E32, E38, E43, and E58 planar core with I plate. Operating conditions: 36 V peak on primaries (square wave), primary current 4 A RMS (on each primary), 11 A RMS on secondary. Circuit conditions: Input voltage 72 V, output voltage 24 V, 250 W output power.

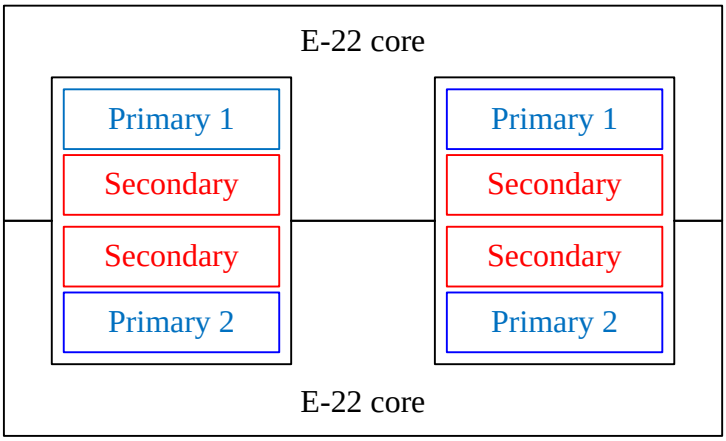


Figure 6.11. Diagram of transformer construction. The magnetic material consists of two E-22 cores of DMR51 material. The windings are wound with 48/1000 litz wire. Each primary has three turns. The two secondary windings are connected in parallel, and each has two turns. Each winding is wound on a single layer, making a "race track" pattern resembling a planar winding. There is 1 mil thick Kapton tape between primary 1 and secondary, and primary 2 and secondary.

Table 6.2. List of the synthesized inductors evaluated in Fig. 6.10. These are a selection of feasible designs taken from the results of the algorithm.

Core material	Size	Primary litz wire gauge (AWG)	Primary Litz wire strands	Secondary litz wire gauge (AWG)	Secondary litz wire strands	Switching frequency (Hz)	Number of turns
3C96	E22	52	800	48	930	300k	6:4
3C96	E32	50	1000	48	1000	300k	6:4
3C96	E38	48	670	46	1000	300k	6:4
N49	E22	52	860	48	860	500k	6:4
N49	E32	50	1000	48	1000	500k	6:4
N49	E58	46	1000	44	1000	500k	3:2
3F45	E22	50	1000	48	1000	1 M	3:2
3F45	E32	50	1000	48	1000	1M	3:2
3F45	E38	48	1000	48	1000	1M	3:2
3F45	E43	48	1000	46	1000	1M	3:2
3F45	E58	48	1000	46	1000	1M	3:2
DMR51	E18	52	1000	52	1000	1M	6:4
DMR51	E22	50	1000	48	1000	1M	3:2
DMR51	E32	50	1000	48	1000	1M	3:2
DMR51	E38	48	1000	48	1000	1M	3:2
DMR51	E43	48	1000	46	1000	1M	3:2
DMR51	E58	48	1000	46	1000	1M	3:2

6.6 Component Selection

This section details the component selection procedure for this converter. The process is very similar to the one used for the RTI buck converter selection (Chapter 3). A tester board was built and various components tested for efficiency; the design of this tester board is fully documented in Appendix F.

6.6.1 Inductance selection

The first step in designing the converter is to select a leakage inductance value that satisfies the operating conditions of the circuit. There are conflicting design goals in selecting the leakage inductance. Figure 6.12 shows a plot of the output power of the converter as a function of phase

shift for various inductance values (referred to the secondary). The family of curves was generated using equation (6.1) with an input voltage of 72 V, output of 24 V, turns ratio of 3:2 (three of each primary and two on the secondary) and a switching frequency of 1 MHz. This plot sets an upper bound on the inductance values: if the inductance is too high, the desired output power can't be reached. Moreover, as shown in Eqn. (6.1), a smaller inductance reduces the phase-shift Φ needed to attain a given power, reducing the phase-shift between transformer current and voltage and improving the power factor at which energy is transferred across it (and potentially the efficiency at which the transformer operates.) Of note is that if the inductance is too low, the control of the converter becomes slightly more difficult because each step in phase shift would cause larger deviations in output power.

At the same time, from equation (6.2), neglecting the effects of transformer magnetizing inductance, the square root of this inductance is inversely proportional to the minimum current needed to achieve ZVS of the converter. Thus the inductance should be as high as possible to extend the power range (to lower values) over which the switches can soft switch.

To balance the above considerations, the inductance value selected to be 250 nH (referred to the secondary), resulting in a phase-shift range of 0 to 55º to control power between zero and maximum at the nominal operating voltage. The transformer as designed has an equivalent secondary-referred leakage inductance of ~60 nH. Additional external leakage inductance was added to increase the total value. A single rod core of 61 material, part 3061990871 (from Fair-Rite) was split in two equal parts and each section was wound with 5 turns of 48/1000 litz wire (for illustration, a photo of this construction is provided in Fig. 6.13). One of each of the resulting inductors was placed on the primary side of the transformer (one inductor for each primary

winding). Each inductor was about ~270 nH, which when referred to the secondary (through a 3:2 turns ratio) was close enough to the desired value.

The resulting magnetizing inductance referred to the secondary is ~8 µH. Using Eqn. 6.5 we can calculate the maximum magnetizing current to be 1.1 A. This current can help extend ZVS range in the inverter switches. If we calculate the minimum current needed for ZVS in the inverter using Eqn. (6.2) (using the capacitance of the EPC2016C shown in table 6.3, and ~500nH of inductance when referred to the primary) it is ~2.2 A. Without the presence of magnetizing current, (and assuming perfectly trapezoidal currents) perfect ZVS can be maintained down to roughly 63% of the output power (2.2 A per inverter is equivalent to 6.6 A at the secondary, which in turns is 160 W). If we assume that the magnetizing current splits evenly across both primaries, this adds roughly 0.55 A to each primary current. Recalculating values, the new minimum load that maintains inverter-side ZVS is 120 W or 48% of full load. The magnetizing currents extends ZVS in the inverter switches by ~15% lower loads.

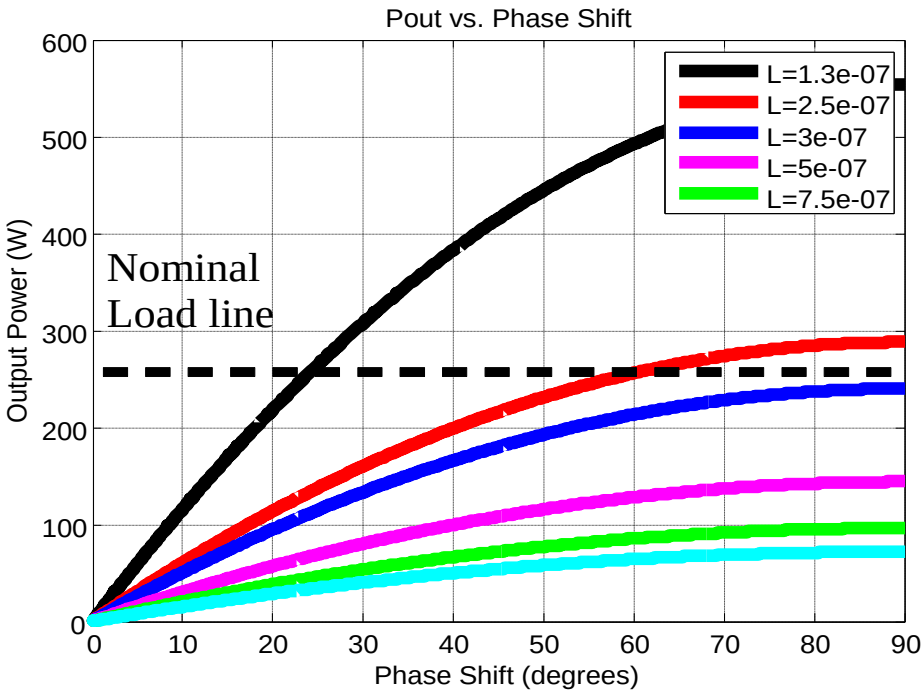


Figure 6.12. Output power vs phase shift for various inductance values. The inductance is the equivalent of the leakages referred to the secondary. This family of curves are generated using equation (6.1) with the following values: N = 2/3, Vin = 72 V, Vo = 24 V and $\omega = 2*\pi*1e3$. The nominal load line shows 250 W of output power.

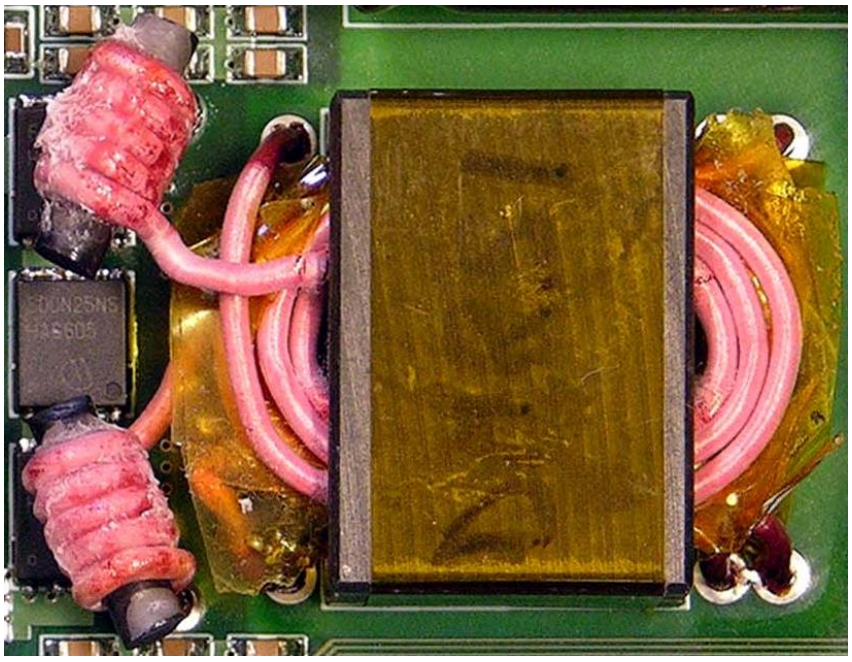


Figure 6.13. Photo of the transformer construction with the additional leakage inductance. The same wire used on the transformer (48/1000) was used to wind the additional leakage. The inductors are suspended above the PCB, adding nothing to the box volume of the system.

6.6.2 Switches

The switches were selected also in a similar manner to that of the RTI buck shown in Chapter 3. The inverter FETs need to block 80 V and carry 3.5 A RMS, while the rectifier FETs need to block 24 V and carry 10.5 A RMS. For the inverter we consider FETs rated at 100 V and 200 V, and for the rectifier 40 V and 60 V devices. A comparison between FETs is made using datasheet values to find a good trade-off between on resistance (R_{on}) and output capacitance (C_{oss}). The full list of devices considered are in tables 6.3 and 6.4. A handful are selected for testing on our tester board using simulation results. The simulation uses LTSpice and we input the on resistance and capacitance information shown in the tables. The simulation gives us an good estimate of the conduction and switching losses of each device.

The FETs selected for evaluation on the tester board are shown in Table 6.5, are tested in the tester board. The board, shown in Fig. 6.14, is used to experimentally determine the efficiency for different FETs configurations. Full details of this board, including schematics, bill of material, and PCB layout files, are documented in Appendix F. This board uses the LM5113 half bridge driver from TI. There are a total of 4 divers, one for each complimentary pair of FETs.

Figure 6.16 shows the results of testing the devices in Table 6.5. The EPC2016C (inverter) and the EPC2024 (rectifier) were chosen as the FETs used in the final design.

After selecting the pair of FETs to be used (EPC2016C in the inverter and EPC2024 on the rectifier), these were tested in different parallel configurations (i.e., different numbers of FETs used in parallel in the inverter and rectifier), with the results shown in Fig. 6.16. In the full system layout (which will be discussed in Chapter 8), the configuration with only 1 FET on each switch was used, as this yielded the best performance as indicated in Fig. 6.16.

Table 6.3. Inverter-side candidate FETs. All are GaN devices. These devices were tested in an LTSpice simulation that include their on resistance and output capacitance.

	Vds (V)	Rds_on @ 125 C (ohms)	Coss @ 50 V (pF)	Figure of merit (ohms * pF)	I_D @ 25 C (A)	Qg (nC)	footprint (mm^2)
EPC2001C	100	0.01155	425	4.90875	36	9	6.69936
EPC2016C	100	0.02512	210	5.2752	18	4.5	3.55003
EPC2007C	100	0.0486	110	5.346	6	2.2	1.85007
EPC2033	150	0.01225	600	7.35	31	10	11.96
EPC2012C	200	0.17	80	13.6	5	1	1.57241
EPC2019	200	0.085	145	12.325	8.5	1.8	2.6277
EPC2010C	200	0.04375	320	14	22	3.7	5.80013

Table 6.4. Rectifier-side candidate FETs. All are GaN devices. These devices were tested in an LTSpice simulation that include their on resistance and output capacitance.

	Vds (V)	Rds_on @ 125 C (ohms)	Coss @ 18 V (pF)	Figure of merit (ohms * pF)	I_D @ 25 C (A)	Qg (nC)	footprint (mm^2)
EPC2014C	40	0.0256	152	3.8912	10	2	1.85007
EPC2015C	40	0.00644	770	4.9588	53	11.2	6.69936
EPC2020	60	0.00374	1500	5.61	90	20	13.915
EPC2031	60	0.004212	1450	6.1074	31	17	11.96

Table 6.5. Candidate FETs to be tested in the tester board. The top two are inverter FETs, and the bottom are rectifier FETs. C_{oss} was evaluated at half of the operating voltage of each FET (36 V for the inverter devices and 12 V for the rectifier devices).

	Vds (V)	Rds_on @ 2 A, 125 C (ohms)	Coss @ 36, 12 V (pF)	Figure of merit (ohms * pF)
EPC2012 C	200	0.11	90	9.9
EPC2016C	100	0.02	235	4.7
EPC2015C	40	0.00644	830	5.3452
EPC2024	40	0.0024	2100	5.04

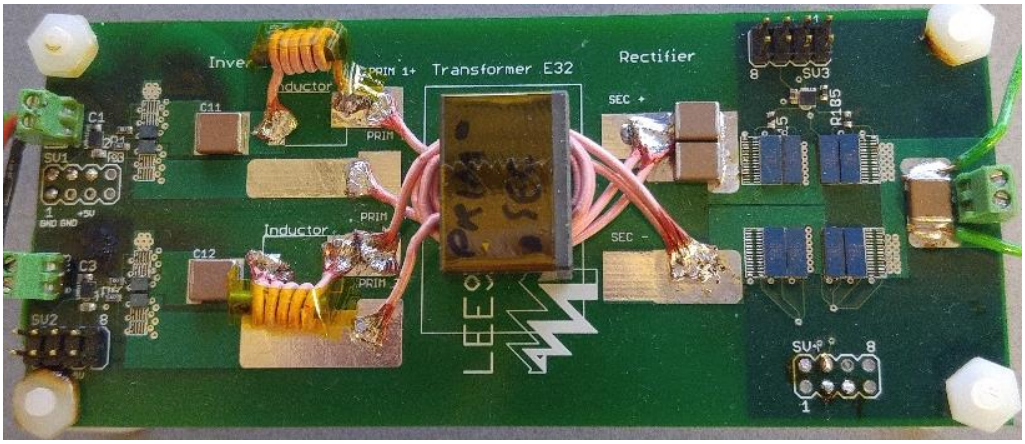


Figure 6.14. Custom 2nd stage converter tester board. 2 input, single output DAB converter. Full details, including completed schematics, bill of materials, and PCB layout files, are documented in Appendix F. The board uses two E cores size E22 as the transformer using core material DMR51 from Hengdian Group DMEGC Magnetics. The transformer is wound PSSP (top to bottom) using 1000/48 Litz wire as indicated in Figs. 6.11 and 6.13 above. The transformer has 3 turns for each primary and two turns of secondary (with the secondary comprising two parallel Litz wires). The additional leakage inductance provided in series with each primary is approximately 270 nH, made by winding 5 turns of the same Litz wire around a rod core section (with 3mm diameter and 11mm of length) of mix 61 from Fair-Rite. The operating frequency used for testing is 1 MHz.

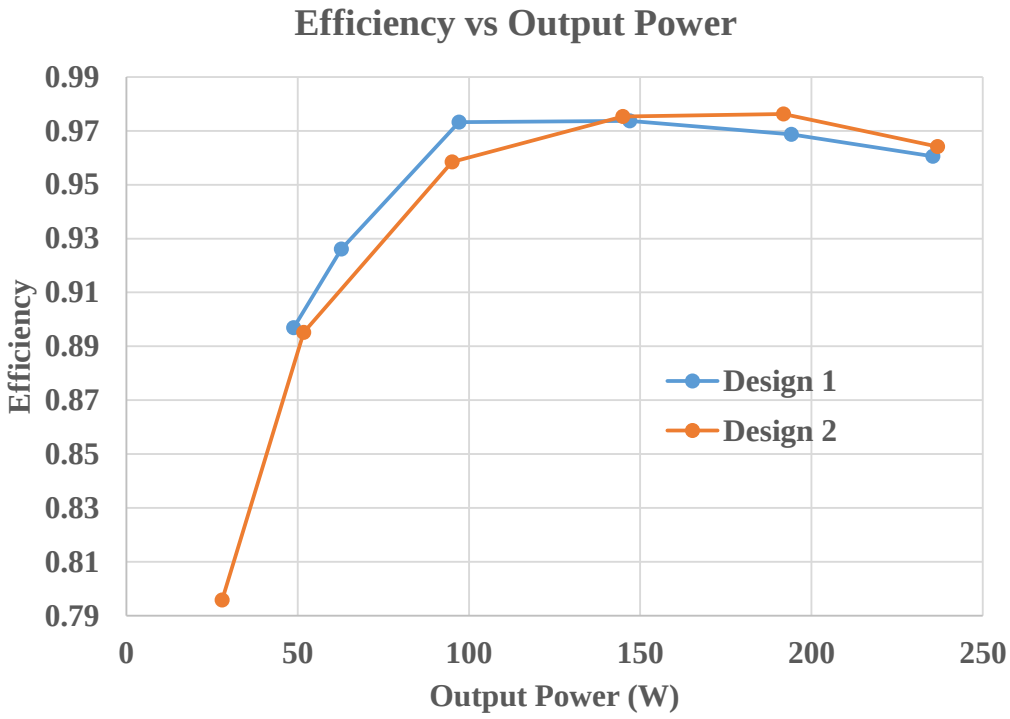


Figure 6.15. Experimental results from testing the FETs in Table 6.5. The blue line ("Design 1") uses EPC2012C on the inverter and EPC2015C on the rectifier. The orange line ("Design 2") uses EPC2016C on the inverter and EPC 2024 on the rectifier. The "Design 2" pair were selected based on having higher efficiency at high load.

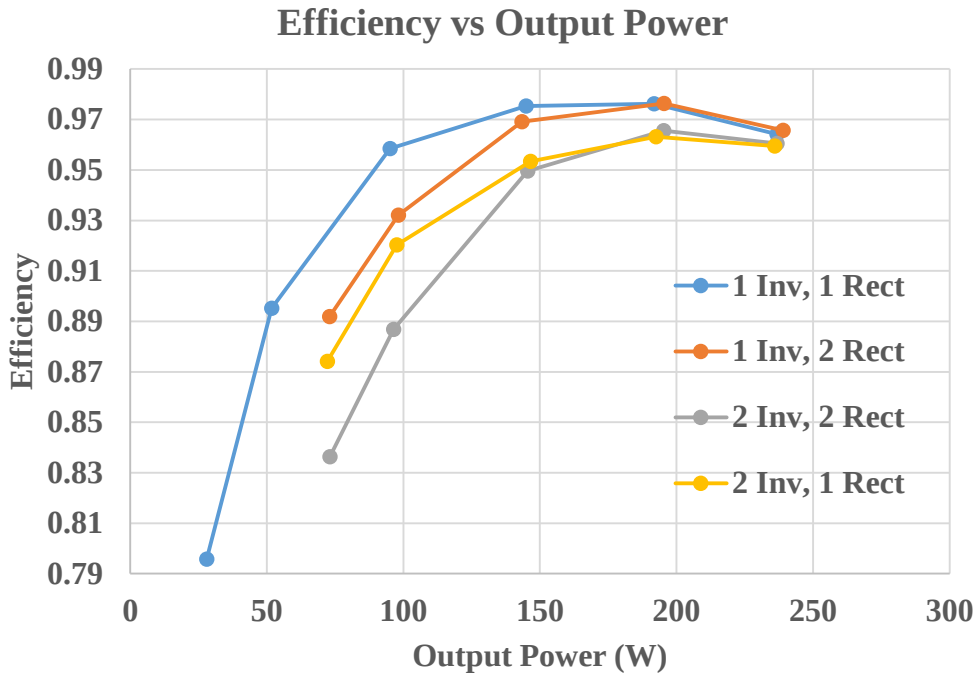


Figure 6.16. Efficiency vs output power curve for different parallel configurations of FETs. The circuit to be implemented in the integrated board consists of only 1 FET on each side (blue curve). The FETs used in the inverter is the EPC2016C, and the one used in the rectifier is the EPC2024. V_{in} = 72 V, V_o = 24 V, f_s = 1 MHz

6.7. Final experimental performance

A summary of the parts used in the second-stage (isolated) converter is found in Table 6.6. Figure 6.17 shows the final efficiency of the converter, as tested in the Test Board of Appendix F, for 72 V on each input and 24 V on the output. The efficiency at full power (250 W) is 96.4%. The peak efficiency is 97.6% at 192 W. This converter (without optimization) has a footprint of approximately 4.33 in x 1.45 in and a height 0.5 in, for a power density of approximately 80 W/in^3. (This is greatly improved in the final design through layout.) Importantly, this design achieves much higher performance than the design based on commercial telecom brick converters (described in the previous chapter) in terms of both footprint and board area. In the next chapter a control scheme that improves light-load efficiency is introduced.

Table 6.6. Parts list for the isolated dc/dc converter.

Part	Description	Parameters
Inverter FETs	EPC2016C	Coss = ~220 pF
Rectifier FETs	EPC2024	Coss = ~2050 pF
Transformer	core: DMR51 2x E22; turns: 3 on each primary, 2 on secondary (2 paralleled Litz wires for secondary); wire: 1000/48 Litz on each winding;	leakage inductance= ~60 nH, magnetizing inductance = ~8 uH, (all referred to secondary) 3:2 turns ratio
External leakage inductors on inverter side	core: 1 rod core 3061990871 from Fair-Rite split in two; turns: 5 wire: 1000/48 Litz	Primary external leakage 1 = ~280 nH Primary external leakage 2 = ~260 nH

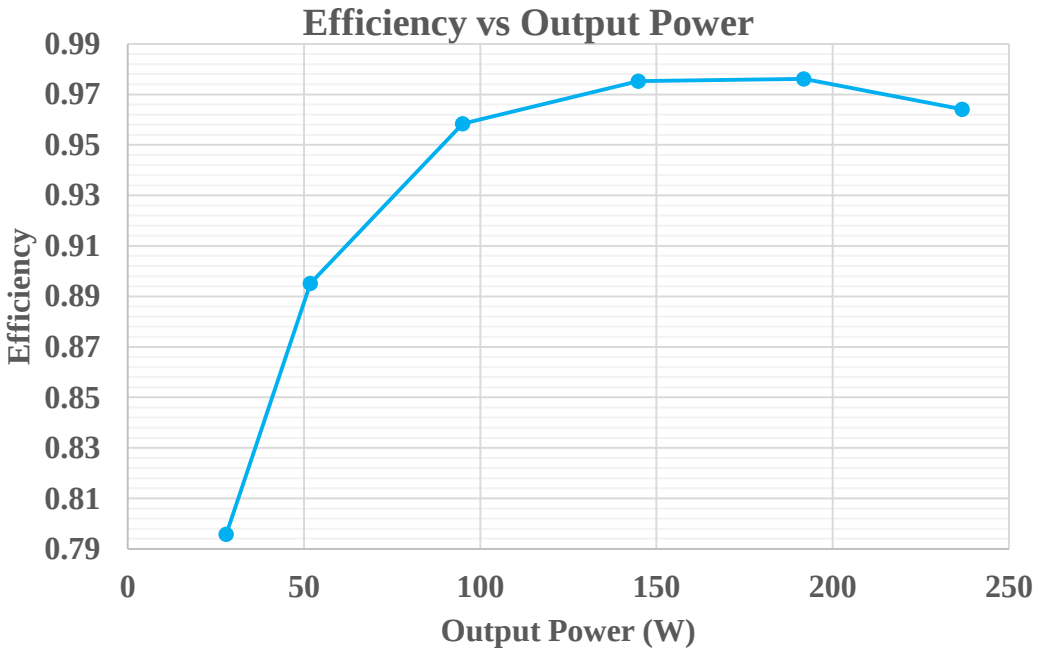


Figure 6.17. Final efficiency vs output power curve for the isolated dc/dc converter. Input voltage 72 V, output voltage 24 V, switching frequency 1 MHz. The components are found on Table 6.6.

Chapter 7: Light Load Efficiency Improvements in Dual Active Bridge (DAB) Converters

In the previous chapter the design of a custom isolated converter was introduced that draws power from a pair of (nominally identical) inputs, and delivers it to a load, providing transformation, galvanic isolation, and regulation of the output. As described there, this converter was based on the Dual Active Bridge (DAB) converter architecture, which provided a number of advantages in the target application. One of the disadvantages of this converter (and of DAB converters in general) is that it loses soft zero-voltage switching (ZVS) at light loads. There is not enough current (and associated energy storage) provided by the transformer (owing to either leakage or magnetizing current) to fully discharge and charge the switch capacitances during transistor dead time. Moreover, at low currents the switching dead times needed to provide some degree of switching loss reduction are on the same order (or larger) than the "phase shift times" (the time delay associated with the phase shift phi used to provide power control), making the power control equation (6.1) itself become inaccurate (as the model underpinning its derivation is not accurate). While conducting experiments it was found that extremely long dead-times were used - longer than the time delays associated with conventional phase-shift control - then ZVS soft switching could be maintained, albeit with very different control relations. In particular, if dead time is increased to values that are significantly larger than the phase shift time, the switch capacitance voltages can be made to oscillate in a manner that preserves soft switching. This presents an opportunity to extend ZVS range in terms of power. However at very low phase shift time and comparatively-large dead times, modulating dead time greatly affects output power. While the transfer function between phase shift and output power in the DAB (at high power

levels) is very well known (and used in Chapter 6), the relation between dead time and output power in DAB-type converters has not been explored well.

Various techniques exist that aim to increase light-load efficiency is DAB converters [70,74-78]. One popular technique is Dual-Phase-Shift (DPS) [75,76,77] control. The goal of this technique is to reduce the circulating (reactive) currents during light-load operation by adding an additional phase shift (i.e. another control variable). This new phase shift D_2 is between the switches that during single-phase-shift control operate simultaneously (e.g. between S1 and S2, S3 and S4, etc. from Fig. 7.1). This scheme imposes a three-level voltage on the inductor, effectively reducing transformer current (and thus, output power) with lower reactive power than compared to single-phase-shift control. Another control technique [78] has the converter operate in three different switching patterns or "modes" depending on the output power. This is demonstrated to improve light-load efficiency, but suffers of having a controller compute extensive calculations, which may not be suitable for compact HF designs.

Other control techniques require additional components for sensing [79,80] or for energy "sloshing" [62,70]. However, additional components adds to the complexity, cost and volume of the converter. Others utilize adaptive techniques where the dead time is adjusted while another variable in the circuit is used to control power delivery (usually phase shift or duty cycle) [81,82].

For purposes of the discussions in this chapter, dead time is considered to be the same value among all switches (both inverter and rectifier switches). Figure 7.1 shows the classic DAB topology. Figure 7.2 shows the switch timing diagram over a converter switching cycle, for both small dead times (i.e. typical DAB operation with phase shift control) and high dead time (and small phase shift). We will refer to these signals throughout the discussion.

This chapter explores the use of dead time control to provide regulation in the DAB at light loads, instead of conventional phase shift control. This is done to preserve ZVS and efficiency at light load compared to conventional approaches. The approach does not sacrifice efficiency under high load and requires no hardware changes to the power stage. We show that dead time control can maintain high efficiency even at <10% of output power. While this approach has been proposed before [74], it has only been explored empirically, and a detailed model of the output modulation due to variations in dead time (with fixed phase shift) has not been previously developed. Here, we present a general model that can be used for prediction of dead time control characteristics in the DAB and design and control of DAB converters using this approach. We validate the proposed model and control approach with SPICE simulations and with experimental results.

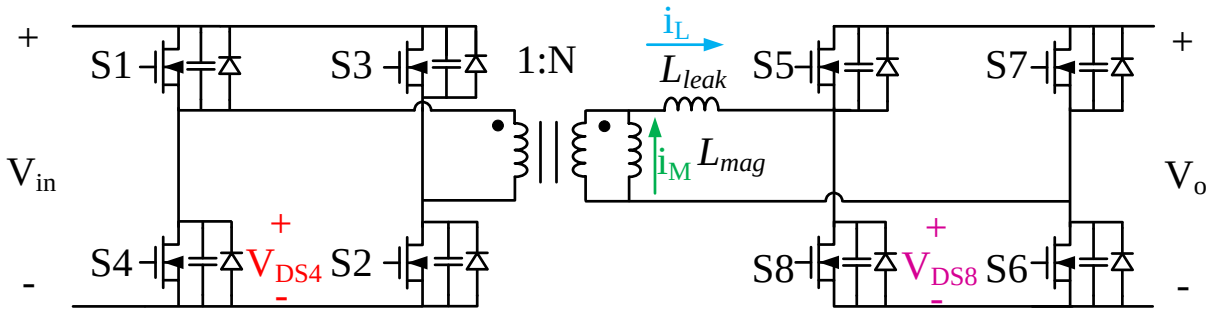


Figure 7.1. DAB converter schematic. All inductances are referred to the secondary. The FET parasitic capacitances and body diodes are explicitly shown. The colored variables and labels (FET voltages and inductor currents) match the colors of their waveforms in Fig 7.3.

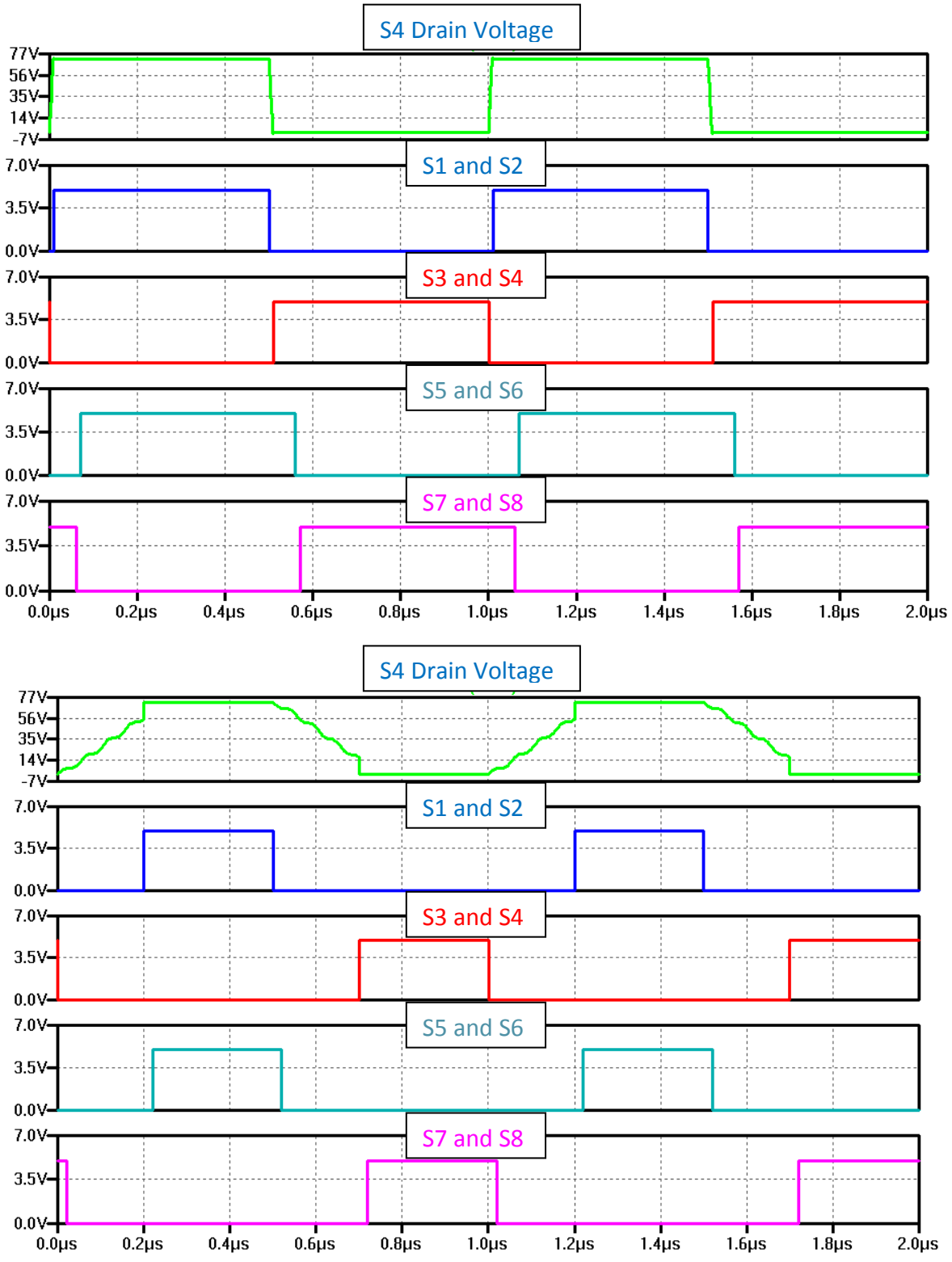


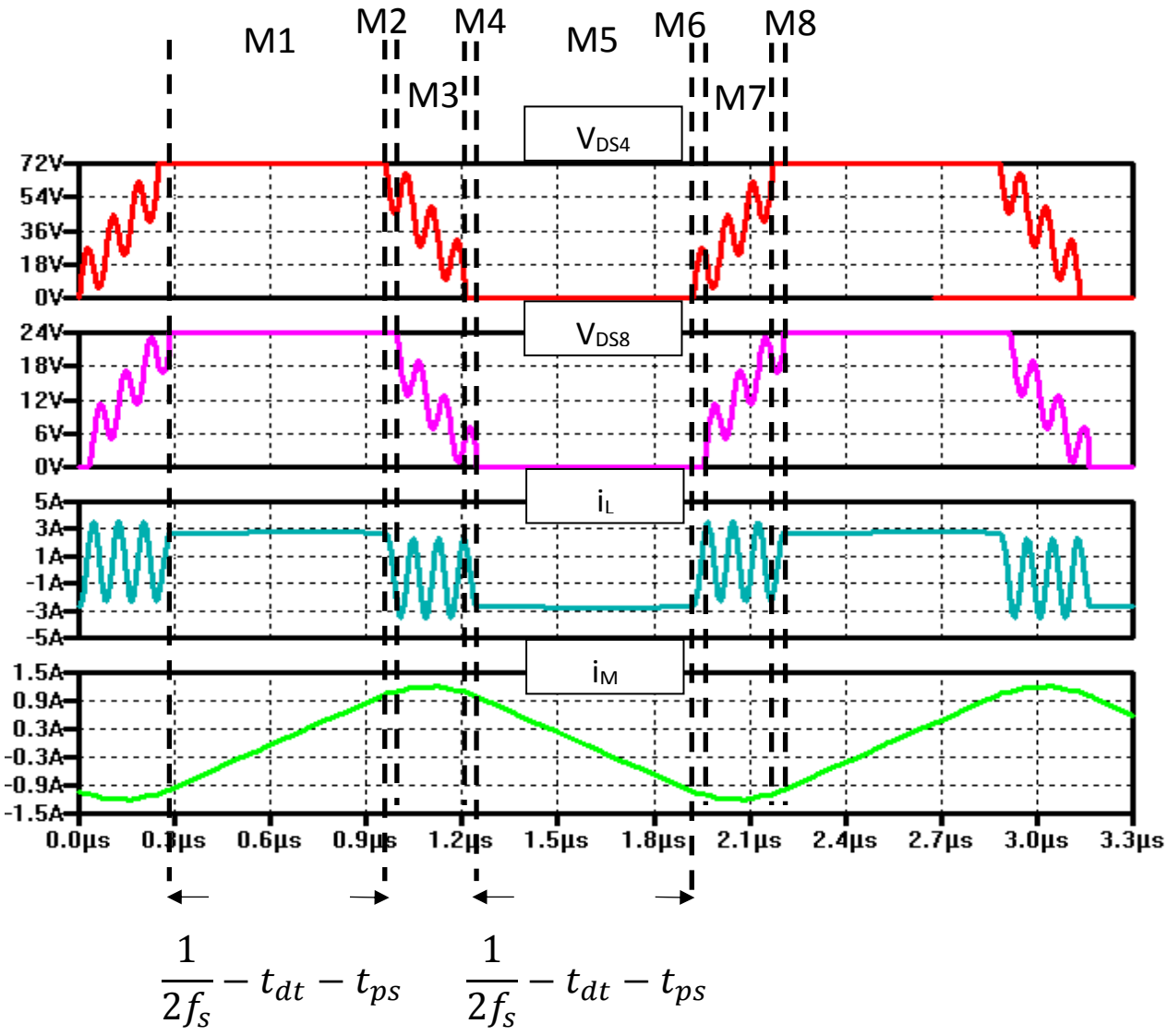
Figure 7.2. Switch timing diagram for the DAB converter in Fig. 7.1. The top figure shows the switch timings for typical (i.e. low dead time) operation. The dead time is set to 1% of the period. The bottom figure shows the timings for high-dead time operation. The dead time here is 20% of the period.

7.1 Modeling and control of the DAB converter

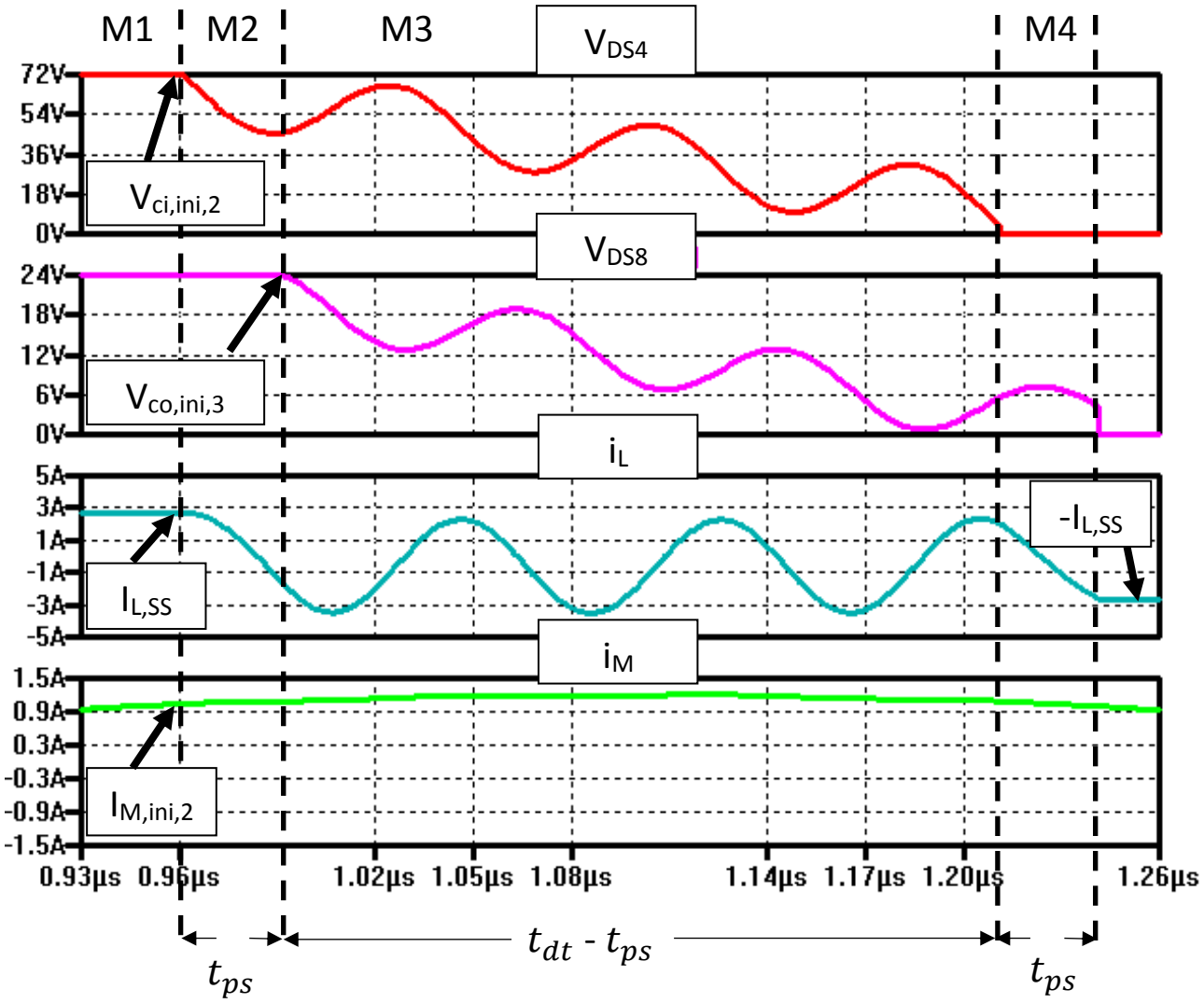
Fig. 7.1 shows a typical DAB converter. For purposes of our analysis, the converter output can be treated as a constant voltage V_O because it is assumed the converter will operate in closed loop with the output voltage changing only on a time scale that is slow compared to the switching period. Figure 7.3 shows LTSPICE simulation waveforms of the converter operating under high dead time (i.e. dead time much bigger than phase shift). When the circuit operates with high dead time, the incoming switch capacitance is allowed to discharge completely and ZVS can be recovered even in light load situations. Modulating dead time also affects output power; thus, it is necessary to understand the effect of dead time both on ZVS and output power control in order to use it for control at light loads.

One goal of this analysis is to find the relationship between the output power and switch dead time in the DAB converter for a fixed phase shift value. As illustrated in Fig. 7.3, with appropriate (and large) dead times, ZVS operation can be maintained under light-load conditions. Based on this relation, dead time control (with fixed phase shift) can be used to modulate output power during light load operation while maintaining high efficiency. As will be seen, the relationship between dead time and output power is complicated, so accurate modeling is valuable in selecting a control law.

The following analysis assumes the circuit is lossless, all leakage is referred to the secondary, the switches have linear capacitance, the transformer magnetizing inductance value is finite but much bigger than the total DAB leakage inductance, and $V_{in} * N = V_O$ so that the DAB inductance current is constant outside of the phase shift and dead time periods. Also this analysis assumes that in light load the dead time period of the converter will correspond to a longer duration than the phase shift delay.


M1
M2
M3
M4
M5
M6
M7
M8
V_{DS4}
V_{DS8}
i_L
i_M
72V
54V
36V
18V
0V
24V
18V
12V
6V
0V
5A
3A
1A
-1A
-3A
-5A
1.5A
0.9A
0.3A
-0.3A
-0.9A
-1.5A
0.0µs
0.3µs
0.6µs
0.9µs
1.2µs
1.5µs
1.8µs
2.1µs
2.4µs
2.7µs
3.0µs
3.3µs
$\frac{1}{2f_s} - t_{dt} - t_{ps}$
$\frac{1}{2f_s} - t_{dt} - t_{ps}$

(a)



(b)

Figure 7.3. SPICE simulation time domain waveforms of the DAB converter operating with high dead time. From the top: inverter FET S4 voltage, rectifier FET S8 voltage, leakage current i_L referred to secondary, and magnetizing current i_M referred to secondary. All 8 modes (individual conduction periods) are shown in 7.3(a), and the main 4 modes are shown in more detail in 7.3(b) along with relevant initial conditions ($V_{Ci,ini,2}$, $V_{Co,ini,3}$, $I_{L,SS}$, $I_{M,ini,2}$) and mode duration times. Simulation parameters and operating point associated with Fig. 7.1: 72 V input, 24 V output, N=1/3, fs=520 kHz, phase shift = 30 ns, dead time = 250 ns, L_{LEAK}= 82 nH, L_{MAG}=8020 nH, Po=45 W, FET capacitance of each inverter switch is 235 pF (representative of EPC2016C devices) and 2100 pF for each rectifier switch is (representative of EPC2024 devices). In M1, switches S1, S2, S5 and S6 are closed. In M2, switches S1 and S2 open while S5 and S6 remain closed. In M3, all switches are open. In M4, switches S3 and S4 close. In M5, switches S3, S4, S7 and S8 are closed. In M6, switches S3 and S4 open while S7 and S8 remain closed. In M7, all switches are open. In M8, switches S1 and S2 close.

The switching cycle of the DAB converter in high dead time operation (light load) can be divided into 8 modes; only 4 will be discussed as the other 4 are symmetric. The relevant modes are shown in detail in Fig. 7.2(b). Expressions for the leakage current, magnetizing current and switch capacitances voltages are derived for all 4 modes and are shown in the Derivation section at the end of the chapter.

The upcoming discussion about the operating modes of the circuit in Fig. 7.1 uses a simplified circuit for modeling purposes. The simplification treats the switches as open or close: when the switches are open, they are modeled as a constant capacitor with value of the switch output capacitance (i.e. C_{OSS}). In this case, the value of C_{OSS} is taken as the value of capacitance when the voltage across it is half of V_{in} for the inverter side FETs, or half of V_O for the rectifier side FETs. When the switches are closed, they are modeled as a short circuit. Finally, all values of voltages and currents are referred to the secondary. This simplification allows us to reduce the circuit of Fig. 7.1 into a set of linear time invariant (LTI) circuits that represent the dynamics of the system in a piece-wise function. The model circuits are shown in Fig. 7.4. We can map the values of the capacitances, inductances and switch voltages in the model to the real values from the topology shown in Fig. 7.1. The mapping is shown in Table 7.1. The model assumes the capacitor that is ringing starts charged, so the capacitor voltage represented is always the voltage of the FETs that were off in the previous mode (i.e. the capacitors that are charged to the input voltage for the inverter FETs or to the output voltage for the rectifier FETs). To find the voltage of the complementary switch, one can use $(V_{in} - v_{DSX})$ for the inverter FETs or $(V_o - v_{DSX})$ for the rectifier FETs where X is the number of the FET whose complementary pair is of interest from Table 7.1. Of note is that to model the relationship between dead time and output power, information from only modes 1-4 is sufficient.

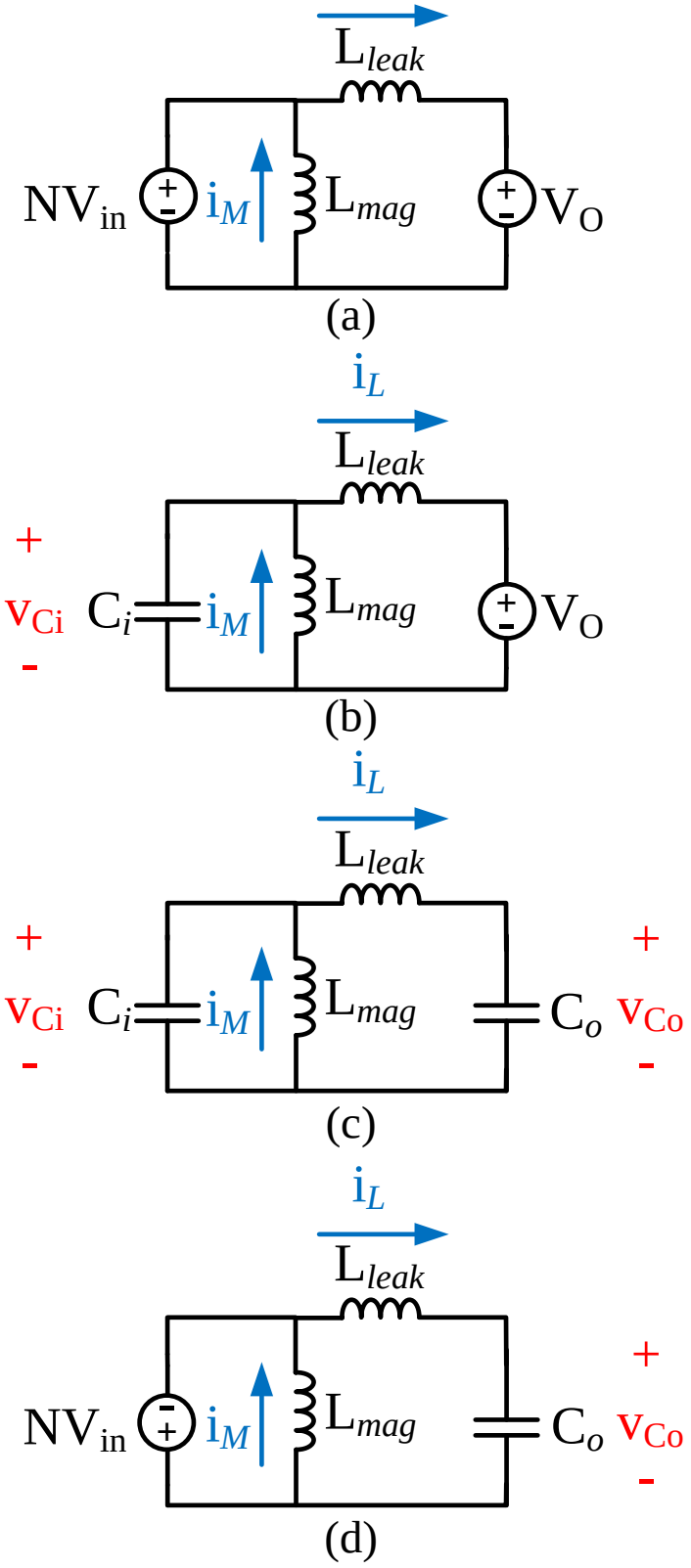


Figure 7.4. Simplified, equivalent resonant circuits for, top to bottom: (a) mode 1, (b) mode 2, (c) mode 3 and (d) mode 4.

Table 7.1. Mapping of parameters between model and real circuit. This is only valid for the circuit in Fig. 7.1. The complementary inverter switch voltage (e.g. V_{DS1} and V_{DS4} are complementary) can be found by using ($V_{in} - V_{DSX}$) where X is the number of the switch found in this table. For the rectifier side complementary switch voltage, use ($V_O - V_{DSX}$).

Name	Model Parameter	Real Circuit Parameter
Inverter capacitance	C_i	C_{OSS} / N^2
Rectifier capacitance	C_o	C_{OSS}
Secondary referred leakage inductance	L_{leak}	L_{leak}
Secondary referred magnetizing inductance	L_{mag}	L_{mag}
Drain to Source voltage on S3 and S4	v_{Ci} in modes 2,3	$N*V_{DS3}$, $N*V_{DS4}$
Drain to Source voltage on S1 and S2	v_{Ci} in modes 6,7	$N*V_{DS1}$, $N*V_{DS2}$
Drain to Source voltage on S7 and S8	v_{Co} in modes 3,4	V_{DS7}, V_{DS8}
Drain to Source voltage on S5 and S6	v_{Co} in modes 7,8	V_{DS5}, V_{DS6}

In mode 1 (on-time mode), the switches S1, S2, S5 and S6 are on such that the source delivers direct energy to the load. The voltage across all the FETs is constant, as is the current through the DAB leakage inductance L_{leak}. However the current through the magnetizing inductance L_{mag} rises linearly. The simplified circuit referred to the transformer secondary is shown in Fig. 7.4(a).

Mode 2 (1st phase shift mode), starts when the inverter side switches S1 and S2 turn off and the source is disconnected from the circuit. The inverting bridge switch capacitances and the leakage and magnetizing inductances form a resonant circuit, shown in Fig. 7.4(b). Here the inverter side capacitances of switches S1 through S4 are represented by C_i, a single equivalent capacitance (defined in Table 7.1) which starts discharging from an initial voltage V_{in} as the transformer and DAB inductances resonate with them. From the Derivation section at the end of the chapter, Mode 2 leakage current i_L is equation (D.1), magnetizing current i_M is (D.2) and inverter switch capacitance voltage v_{Ci} is (D.3). In Mode 2, v_{Ci} (from Fig. 7.4(b)) represents the switch drain voltage for S3 and S4 (from Fig. 7.1). Mode 2 lasts for the phase shift time set by the controller.

Mode 3 (dead time mode) starts when the rectifying bridge switches S5 and S6 turn off and the load is disconnected from the circuit. The net inverter switch capacitance C_i, equivalent rectifier capacitance C_o (defined in Table 7.1), leakage inductance L_{leak} and magnetizing inductance L_{mag} form a resonant circuit (shown in Fig. 7.4(c)) that has two resonant frequencies. For the case where the magnetizing inductance is far larger than the leakage inductance, these resonances may be approximated as one "fast" resonance that is dominantly between the capacitors (in series) and the leakage inductance and another "slow" resonance that is dominantly between the capacitors (in parallel) and the magnetizing inductance. The "fast" resonant frequency can be approximated as:

$$f_{leak,m3} = \frac{1}{2\pi\sqrt{L_{leak} * \left(\frac{C_i * C_O}{C_i + C_O}\right)}} \quad (7.1)$$

where C_i is the equivalent inverter capacitance referred to the secondary and C_o is the equivalent rectifier capacitance. The "slow" resonant frequency can be approximated as:

$$f_{mag,m3} = \frac{1}{2\pi\sqrt{L_{mag} * (C_i + C_O)}} \quad (7.2)$$

The magnetizing current can be considered nearly constant during this mode and helps ring down the switch capacitance voltage for ZVS turn on of the incoming switches if given enough time, as can be seen in Fig 7.3. The equations for this mode are: leakage current (D.5), magnetizing current (D.6), inverter capacitance voltage (D.7) and rectifier capacitance voltage (D.8).). In Mode 3, v_{Ci} (from Fig. 7.4(b)) represents the switch drain voltage of S3 and S4 (from Fig. 7.1), while v_{Co} represents the switch drain voltage of S7 and S8. Mode 3 lasts for the switch dead time minus the phase shift time.

Mode 4 (2^{nd} phase shift) starts when the inverter side switches S3 and S4 turn on and connect the source in the opposite polarity than in Mode 1. A new resonant circuit is formed between the leakage and magnetizing inductances and the rectifier capacitance, shown in Fig. 7.4(d). The equations for this mode are: leakage current (D.10), magnetizing current (D.11) and rectifier capacitance voltage (D.12). In Mode 4, while v_{Co} represents the switch drain voltage of S7 and S8. This mode lasts for the phase shift time value set in the controller.

The load current is the opposite of the leakage inductance current during modes 1 and 5 (on-time modes) and approximately zero for all other times. The output power can be approximated by finding the average current delivered to the load:

$$I_{O,avg} = \frac{(\frac{1}{f_s} - 2 * (t_{ps} + t_{dt}))}{\frac{1}{f_s}} * I_{L,SS} \quad (7.3)$$

$$P_{O,avg} = V_O * I_{O,avg} \quad (7.4)$$

where f_s is the converter switching frequency in hertz, t_{ps} is the phase shift time in seconds, t_{dt} is the switch dead time and $I_{L,SS}$ is the value of constant leakage inductor current in mode 1. By finding $I_{L,SS}$, one can use (7.3) and (7.4) to find the output power.

There are 4 unknowns in the equations describing the timings (found in the Derivation section): the initial values of inductor currents and capacitor voltages at the start of mode 2 ($I_{L,SS}$, $I_{M,ini,2}$, $V_{ci,ini,2}$, and $V_{co,ini,3}$). The inverter and rectifier capacitor initial voltage values ($V_{ci,ini,2}$ and $V_{co,ini,3}$) are set by the input and output voltages, respectively. The magnetizing current at the beginning of mode 2 can be approximated by:

$$I_{M,ini,2} = \frac{V_{in} * N}{L_{mag}} * \left(\frac{1}{2 * f_s} - t_{dt} - t_{ps}\right) \quad (7.5)$$

This equation approximates the magnetizing current at the beginning of mode 2 as being half of the peak-to-peak swing in the current over the duration in which constant voltage is applied across it by the input voltage.

A final equation is needed to finally solve for $I_{L,SS}$. In periodic steady state, the current in the leakage inductor at the beginning of mode 2 has to be equal in magnitude but opposite in sign to the current at the end of mode 4. This can be seen in the 3rd pane in Fig. 7.3(b). In equation form:

$$I_{L,ini}(0) = I_{L,SS} = -I_{L,ini}(t_{dt} + t_{ps}) \quad (7.6).$$

Using these equations, one can develop a model of the circuit. An analytical solution for output power vs dead time is not available, but a numerical solution is nonetheless useful. The numerical model is solved in a piece-wise fashion using the time duration of the different modes as intervals described by different sets of equations. Equations D.1, D.2 and D.3 are used to describe the circuit variables over a time t_{ps} (mode 2 duration as seen in Fig. 7.3(b)). The final values of mode 2 are used as the initial values of mode 3, which has duration $t_{dt} - t_{ps}$ (as seen in Fig. 7.3(b)) and uses equations D.5 through D.8. In turn the final values of mode 3 are used as the initial conditions of mode 4, which also has duration t_{ps} and uses equations D.10, D.11 and D.12. All initial conditions of mode 2 are known except for $I_{L,SS}$. This variable can be kept through the numerical solutions and at the end solved for using (7.6). The output power can be calculated using (7.3) and (7.4). A Matlab script was used here to readily evaluate all the computations. The script is included in Appendix G. By arranging a sweep of dead time values t_{dt}, one can generate a plot such as the one in Fig. 7.5, which compares the predicted output with that generated by LTSPICE simulations using the simulation model in Appendix H.

Using this model, the output power can be calculated as a function of dead time for a given DAB circuit with the following inputs: switch capacitances, leakage and magnetizing inductance, nominal input and output voltage (as longs as $V_{in} * N = V_O$ holds), switching frequency and phase shift time value.

Figure 7.5 shows a comparison of the model developed here to an LTSPICE simulation. The simulation and the model are in very good agreement.

In the following section, the numerical model is compared to experimental results.

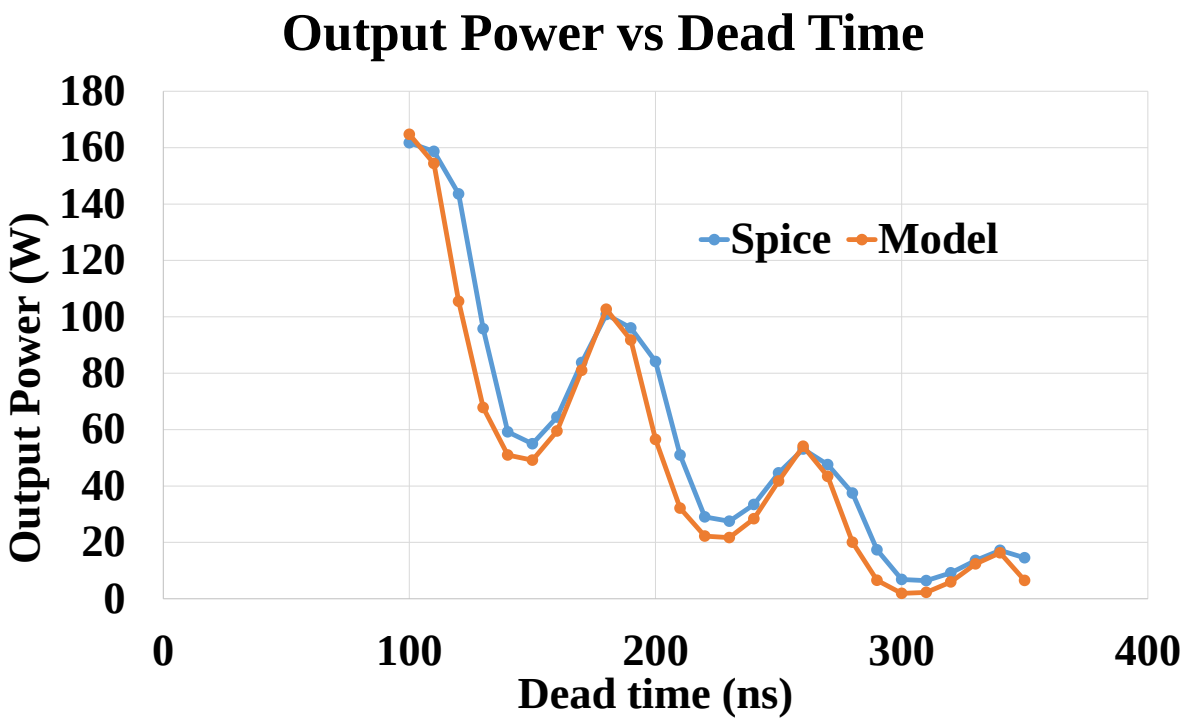


Figure 7.5. Output power vs dead time plot. This plot compares the numerical model developed here to a SPICE simulation at the same operating points. Simulation parameters and operating point: 72 V input, 24 V output, N=1/3, fs=520 kHz, phase shift = 30 ns, L_{leak}= 82.07 nH, L_{mag}=8020.7 nH, rated power of 250 W, inverter total switch capacitance C_i=3735 pF, and rectifier total switch capacitance C_o=4100 pF (all capacitance and inductance values are referred to secondary). These capacitances are representative of using EPC2016C devices for the inverter and EPC2024 devices for the rectifier.

7.2 Experimental verification

The model was verified experimentally using the DAB converter discussed in chapter 6. A simplified schematic is shown in Fig. 7.6 with components detailed in Table 7.2; the full schematic is detailed in Appendix F. This converter's transformer has two primaries and one secondary, and the inverter on each primary is a half bridge inverter. For the circuit in Fig. 7.6, both input voltages are identical (the input ports are connected in parallel in the experiments) and the blocking capacitors have negligible ripple on it (effectively acting as a dc offset in the model which can be easily accounted for). The two primaries and the secondary are wound around the center leg,

sharing the same flux. The two primaries can be effectively seen as two identical circuits in parallel when referred to the secondary. Nevertheless, this converter can be reduced to the simplified circuits shown in Fig. 7.4 and thus can be described accurately with the model developed here. There are minor changes in how to calculate the net values of switch capacitance but the model is useful if the mode transitions happen as described above.

The net value of capacitances C_i and C_o are found by analyzing the circuit in Fig. 7.7. By finding the characteristic equation of the circuit, one can determine the single capacitance values that resonate with the inductance L_{leak}. C_i is $2C_{OSS,i}/N^2$ for a single primary, and twice that value for both primaries. C_O is $C_{OSS,o}$.

Figure 7.8 shows data that compares the model developed here to experimental results. In these experiments the converter is operated at a switching frequency of 1 MHz and at a phase shift of 10 ns. Contrary to "normal" DAB operation, phase shift is held constant and output power is modulated using dead time as described in the introduction.

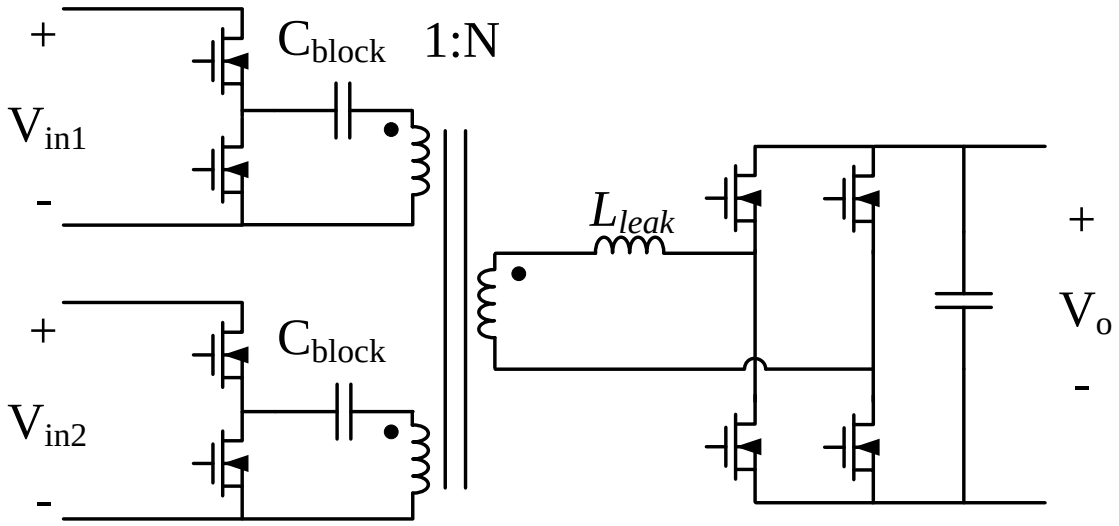


Figure 7.6. DAB converter used for experimental verification of the model. This converter is described in detail in Chapter 6.

Table 7.2. Parts and parameters used in the experimental verification of the model.

Part	Description	Circuit Parameters
Inverter FETs	EPC2016C	C_{OSS} = ~220 pF
Rectifier FETs	2x EPC2024	C_{OSS}= ~2050 pF 2x in parallel
Transformer	core: DMR51 2x E22; turns: 3 on primary, 2 on secondary; wire: 1000/48 Litz on each winding;	leakage inductance= ~50 nH, magnetizing inductance = ~8 uH, (all referred to secondary) 3:2 turns ratio
External leakage inductors on inverter side	core: 1 rod core 3061990871 from Fair-Rite split in two; turns: 5 wire: 1000/48 Litz	Primary external leakage 1 = ~280 nH Primary external leakage 2 = ~260 nH

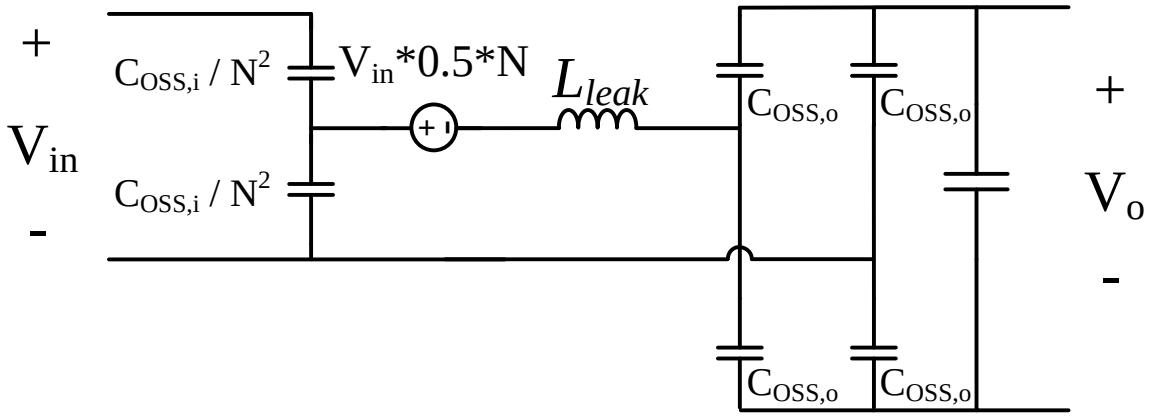


Figure 7.7. Circuit analyzed to find the equivalent capacitances C_i and C_o. This circuit models dead time mode, where all switches are open. The switches are modeled as their output capacitances referred to the secondary. Only one primary is analyzed here. We are ignoring the effects of the magnetizing inductance in this model.

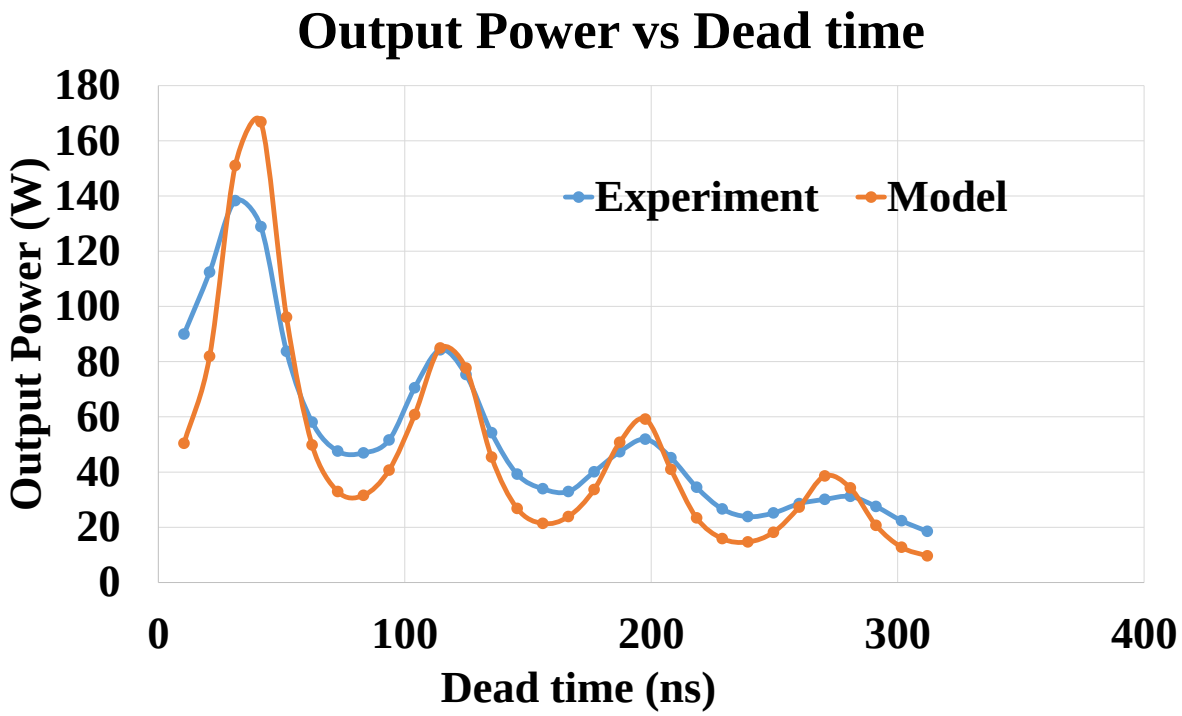


Figure 7.8. Output power vs dead time plot. This plot compares the experimental results to the model. The switching frequency is 1 MHz, the phase shift is fixed at 10 ns, the input voltage is 72 V, output voltage is 24 V, and rated power of 250 W for both experiment and model. The circuit parameters (for model) and parts list (for experiment) are found in Table 7.2.

7.3 Improvements in light load efficiency

Operating with high dead time can be used to significantly increase light load efficiency, as is shown experimentally in [74], and also applied in our earlier work [70]. The orange and blue curves of Fig. 7.7 show experimental results of efficiency vs output power for our prototype DAB converter of Fig. 7.6 using phase shift control and dead time control. It can be seen that for low output power, the dead time control approach can yield higher efficiencies than with phase shift control. (Below, we describe how to map this to a control law that achieves high efficiency across a wide operating range, providing the red curve.)

Our results show that by increasing dead time the FET capacitors are allowed to losslessly charge and discharge which mitigates switching loss, which is a main loss mechanism (along with

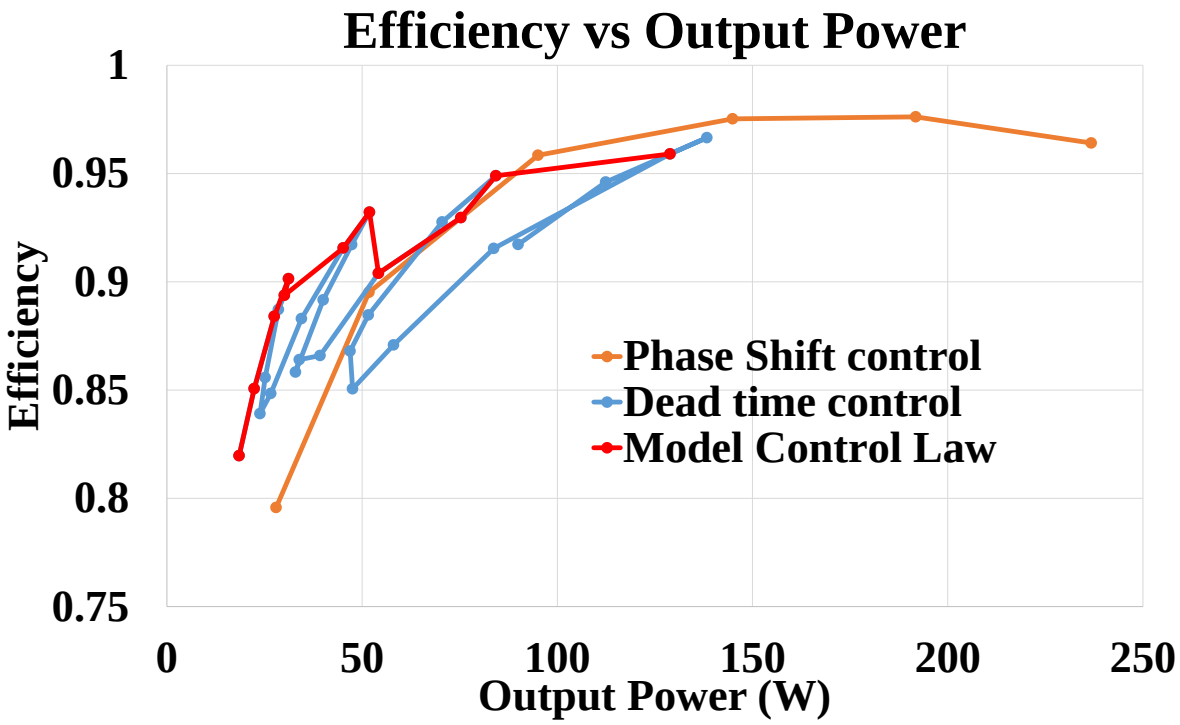


Figure 7.9. Experimental results of efficiency vs output power plot for different control methods. This plot shows the efficiency of the converter when controlled by typical phase shift modulation (orange), by sweeping dead time up to about 30% of period at fixed phase shift (blue), and by following the dead times predicted by the model to achieve high efficiency, using the control law of Fig. 7.11 (red). It can be seen that one can smoothly control power with improved efficiency using the model-predicted controls. The operating conditions and circuit parameters are the same as in Fig 7.8. For phase shift control, dead time is constant at 10 ns, and phase shift time is modulated from 1 to 61 ns. For dead time control, phase shift time is constant at 10 ns, and dead time is modulated from 10.4 ns to 312 ns.

transformer core loss) at light loads, while enabling power control. Figure 7.10 shows an experimental waveform of the drain voltage. Although it is not always possible to achieve true ZVS for a given output power, the turn-on voltage of the switch can be reduced significantly.

From Fig. 7.8 we can see that there are multiple dead times that can provide the same output power; from simulation and empirical results it was found that the most efficient dead time for a given output power is the highest dead time. A high dead time allows for maximum charge/discharge of the switch capacitance (reducing switching loss) and yields a lower volts-seconds applied to the transformer (reducing transformer core loss). The voltage waveform seen

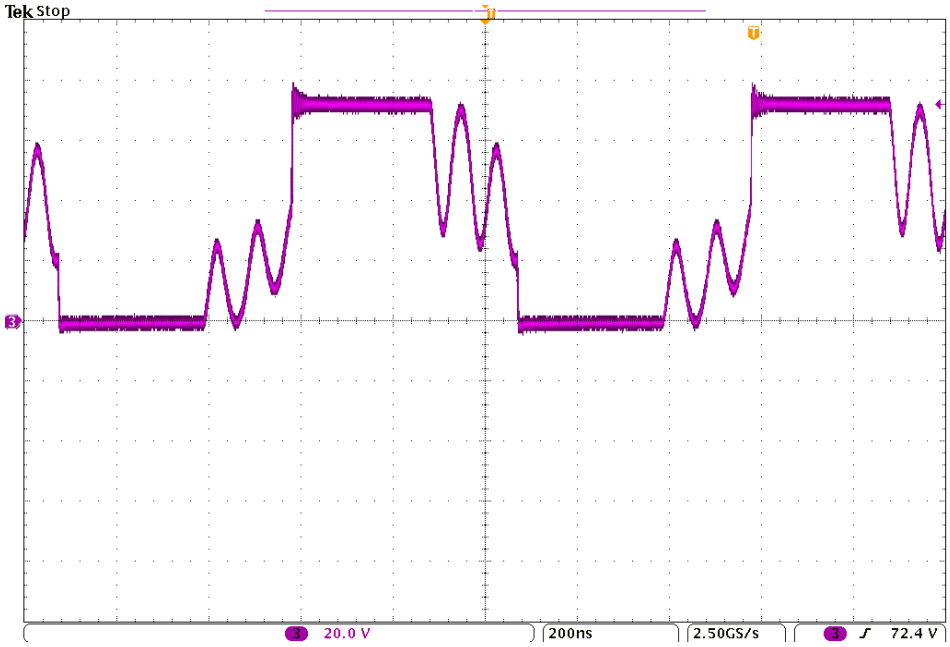


Figure 7.10. Experimental waveform for the drain voltage of the low-side FET in the top inverter in Fig. 7.6. This particular operating point shows a reduction of 10 V in the turn-on voltage across the switch when compared to turning on at the bottom of the first "valley". Operating point: input voltage= 72 V, output voltage = 24 V, output power = 48 W, phase shift time = 10 ns, and dead time = 185 ns.

in Fig. 7.10 is the same applied to one of the primaries of the transformer (minus the dc component). By reducing the on time of the switches, the volt-seconds applied the transformer is reduced (area under the voltage vs time curve) when compared to a 50% duty cycle square wave. This yields a lower flux swing in the core.

An efficient control algorithm is to use phase shift control with a small, fixed dead time down to some load boundary (~40% in our example), and to modulate dead time at fixed phase shift time at lighter loads. The desired effect of the capacitors reaching ZVS or near ZVS occurs only when the dead time is bigger than the phase shift time. For the example converter used in these experiments, phase shift is fixed at 10 ns and dead time is modulated from 52 ns (~33% load) to 300 ns (~8% load).

An effective way to use dead time control is to program the controller to jump between dead time "sections" to maximize efficiency for a given power level. These operating "sections" of dead time are selected based on being the highest dead time useable for a given power level. The numerical model can be used to rapidly create an output power vs dead time curve (such as the one in Fig. 7.8) and graphically select the regions of dead time for efficient operation for a given power level. An example of the way to select the dead time regions of interest is shown in Fig. 7.11. (This method is based on the modeled output power vs efficiency curve.) The red curve in Fig. 7.9 also shows the efficiency vs output power curve for this converter if operated in the regions selected using the method shown in Fig. 7.11. The efficiency is improved greatly compared to the standard phase shift control method for light loads. At around 25 W (10% load), efficiency is improved about ~9%. However there are a few areas where the model captures a suboptimal operating point. This inaccuracy in the model-generated control law is very likely due to the non-linear capacitance of the FETs and magnetic component losses which are phenomena not captured in the model. The inaccuracies of the model can be corrected by using empirical data collected on a given converter. Nevertheless, this model is useful for predicting the behavior of the output power as dead time is modulated, and gives the designer the tools to rapidly determine how changing a parameter in the circuits affects said relation. Of note is that this algorithm increases light load efficiency without any increases in component count, circuit complexity, volume or cost.

The next section shows the details of the equations used to generate the output power vs dead time plot.

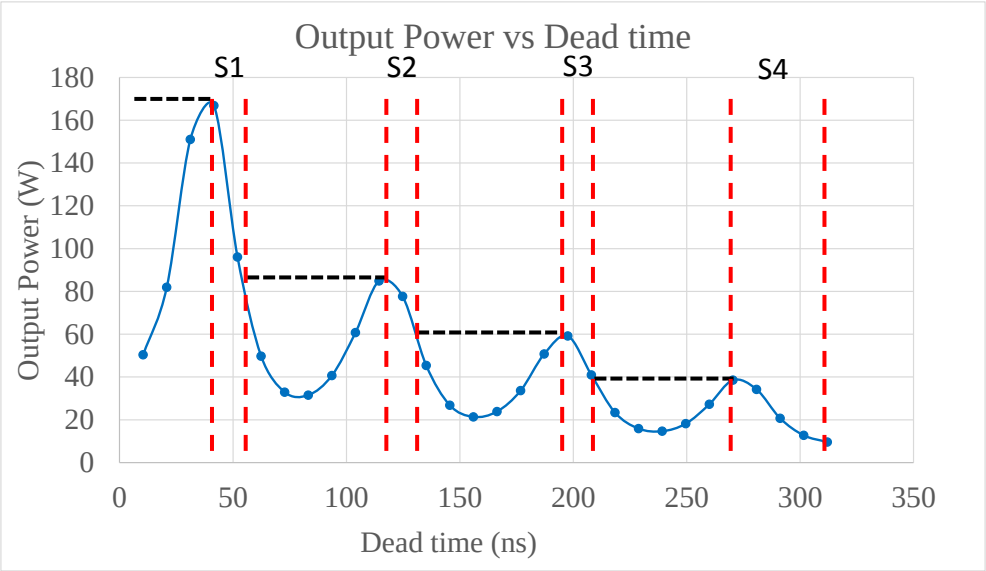


Figure 7.11. Output power vs dead time plot created using the model (a repeat of the one shown in Fig. 7.8). Here the graphical method used to select the operating dead times sections is shown. The sections are divided into S1 to S4. These sections are selected based on the highest dead time for a given amount of output power. S1 can deliver between 165 W to 85 W using the dead times between 35 ns and 60 ns; S2 can deliver between 85 W to 60 W by modulating dead time between 110 ns and 130 ns; S3 can deliver between 60 W to 40 W by utilizing dead times between 190 ns and 210 ns; S4 can deliver between 40 W to ~10 W by using dead times between 270 ns to 310 ns. As seen on this plot, these sections are quasi-linear and can provide a reliable control handle.

7.4 Derivations

Here the set of equations that compose the numerical model are derived. The equations consists of the inductor currents and capacitor voltages in each of modes 2, 3 and 4. The complete circuit is solved numerically by matching the initial conditions of one mode to the final conditions of the previous one. The circuit analyzed for mode 2 operation is shown in Fig. 7.3(b). The leakage inductor current, magnetizing inductor current and inverter capacitance voltage are:

$$I_{L,m2} = -\frac{V_O}{L_{leak}} * t \ + \ \frac{V_O}{L_{leak}} * \left(\frac{L_{mag}}{L_{mag}+L_{leak}}\right) * t \ + \left(\frac{L_{mag}}{L_{mag}+L_{leak}}\right) * \left(I_{L,SS} + I_{M,ini,2}\right) * (\cos(\omega_{m2} * t) - 1) \ + \frac{1}{\omega_{m2} * L_{leak}} * \left(V_{ci,ini,2} - V_O * \left(\frac{L_{mag}}{L_{mag}+L_{leak}}\right)\right) * sin(\omega_{m2} * t) + I_{L,SS} \quad (\boldsymbol{D.1})$$

$$I_{M,m2} = \frac{V_O}{L_{mag}+L_{leak}} * t - \left(\frac{L_{leak}}{L_{mag}+L_{leak}}\right) * \left(I_{L,SS} + I_{M,ini,2}\right) + \left(\frac{L_{leak}}{L_{mag}+L_{leak}}\right) * \left(I_{L,SS} + I_{M,ini,2}\right) * \cos(\omega_{m2} * t) + \frac{1}{\omega_{m2} * L_{mag}} * \left(V_{ci,ini,2} - V_O * \left(\frac{L_{mag}}{L_{mag}+L_{leak}}\right)\right) * sin(\omega_{m2} * t) + I_{M,ini,2} \quad (\boldsymbol{D.2})$$

$$V_{ci,m2} = V_{in} * N - V_{ci,ini,2} + V_O * \left(\frac{L_{mag}}{L_{mag}+L_{leak}}\right) + \left(V_{ci,ini,2} - V_O * \left(\frac{L_{mag}}{L_{mag}+L_{leak}}\right)\right) * cos(\omega_{m2} * t) - \left(\frac{L_{mag} * L_{leak}}{L_{mag}+L_{leak}}\right) * \omega_{m2} * \left(I_{L,SS} + I_{M,ini,2}\right) * sin(\omega_{m2} * t) \qquad (\boldsymbol{D.3})$$

where L_{mag} is the magnetizing inductance, L_{leak} is the leakage inductance, $I_{L,SS}$ is the leakage current at the beginning this mode (initial value), $I_{M,ini,2}$ is the magnetizing current at the beginning of this mode (initial value), $V_{ci,ini,2}$ is the inverter capacitance voltage at the beginning of this mode (initial value), and ω_{m2} is the resonance frequency of the mode 2 circuit defined as:

$$\omega_{m2} = \frac{1}{\sqrt{C_i * \left(\frac{L_{mag} * L_{leak}}{L_{mag} + L_{leak}}\right)}} \qquad (\boldsymbol{D.4})$$

where C_i is the inverter capacitance.

The equations that describe mode 3 (with equivalent circuit shown in Fig. 7.3(c)) are:

$$I_{L,m3} = V_{dc,caps} * \left(\omega_{leak,m3} * C_i - \frac{1}{\omega_{leak,m3} * L_{mag}}\right) * sin\left(\omega_{leak,m3} * t\right) + \left(\frac{-\left(I_{L,ini,3}+I_{M,ini,3}\right)}{C_i} + \frac{I_{M,ini,3}}{C_i+C_o}\right) * \left(\frac{1}{\left(\omega_{leak,m3}\right)^2 * L_{mag}} - C_i\right) * \cos\left(\omega_{leak,m3} * t\right) + \left(V_{ci,ini,3} - V_{dc,caps}\right) * \left(\omega_{mag,m3} * C_i - \frac{1}{\omega_{mag,m3} * L_{mag}}\right) * sin\left(\omega_{mag,m3} * t\right) + \left(-L_{mag} * I_{M,ini,3} + \frac{I_{L,ini,3}+I_{M,ini,3}}{\left(\omega_{leak,m3}\right)^2 * C_i} - \frac{I_{M,ini,3}}{\left(\omega_{leak,m3}\right)^2 * (C_i+C_o)}\right) * \left(\frac{1}{L_{mag}} - \left(\omega_{mag,m3}\right)^2 * C_i\right) * \cos\left(\omega_{mag,m3} * t\right) \quad (\boldsymbol{D.5})$$

$$I_{M,m3} = I_{M,ini,3} + \frac{V_{dc,caps}}{\omega_{leak,m3} * L_{mag}} * sin\left(\omega_{leak,m3} * t\right) + \left(\frac{-\left(I_{L,ini,3}+I_{M,ini,3}\right)}{\left(\omega_{leak,m3}\right)^2 * C_i} + \frac{I_{M,ini,3}}{\left(\omega_{leak,m3}\right)^2 * (C_i+C_o)}\right) * \left(\frac{1}{L_{mag}} - \frac{\cos\left(\omega_{leak,m3} * t\right)}{L_{mag}}\right) + \frac{\left(V_{ci,ini,3} - V_{dc,caps}\right)}{\omega_{mag,m3} * L_{mag}} * sin\left(\omega_{mag,m3} * t\right) + \left(-L_{mag} * I_{M,ini,3} + \frac{I_{L,ini,3}+I_{M,ini,3}}{\left(\omega_{leak,m3}\right)^2 * C_i} - \frac{I_{M,ini,3}}{\left(\omega_{leak,m3}\right)^2 * (C_i+C_o)}\right) * \left(\frac{1}{L_{mag}} - \frac{cos\left(\omega_{mag,m3} * t\right)}{L_{mag}}\right) \quad (\boldsymbol{D.6})$$

$$V_{ci,m3} = V_{dc,caps} * \cos\left(\omega_{leak,m3} * t\right) + \left(\frac{-\left(I_{L,ini,3}+I_{M,ini,3}\right)}{\omega_{leak,m3} * C_i} + \frac{I_{M,ini,3}}{\omega_{leak,m3} * (C_i+C_o)}\right) * \sin\left(\omega_{leak,m3} * t\right) + \left(V_{ci,ini,3} - V_{dc,caps}\right) * cos\left(\omega_{mag,m3} * t\right) + \left(-\omega_{mag,m3} * L_{mag} * I_{M,ini,3} + \frac{\left(I_{L,ini,3}+I_{M,ini,3}\right) * \omega_{mag,m3}}{\left(\omega_{leak,m3}\right)^2 * C_i} - \frac{I_{M,ini,3} * \omega_{mag,m3}}{\left(\omega_{leak,m3}\right)^2 * (C_i+C_o)}\right) * sin\left(\omega_{mag,m3} * t\right) \quad (\boldsymbol{D.7})$$

$$V_{co,m3} = V_{dc,caps} * \cos\left(\omega_{leak,m3} * t\right) + \left(\frac{-\left(I_{L,ini,3}+I_{M,ini,3}\right)}{\omega_{leak,m3} * C_i} + \frac{I_{M,ini,3}}{\omega_{leak,m3} * (C_i+C_o)}\right) * \sin\left(\omega_{leak,m3} * t\right) + \left(V_{ci,ini,3} - V_{dc,caps}\right) * cos\left(\omega_{mag,m3} * t\right) + \left(-\omega_{mag,m3} * L_{mag} * I_{M,ini,3} +$$

$$\frac{(I_{L,ini,3}+I_{M,ini,3})*\omega_{mag,m3}}{(\omega_{leak,m3})^2*C_i} - \frac{I_{M,ini,3}*\omega_{mag,m3}}{(\omega_{leak,m3})^2*(C_i+C_o)}\Big) * sin(\omega_{mag,m3} * t) - L_{leak} * \Big(V_{dc,caps} *$$

$$\Big((\omega_{leak,m3})^2 * C_i - \frac{1}{L_{mag}}\Big) * \cos(\omega_{leak,m3} * t) - \Big(\frac{-(I_{L,ini,3}+I_{M,ini,3})}{C_i} + \frac{I_{M,ini,3}}{C_i+C_o}\Big) * \Big(\frac{1}{\omega_{leak,m3}*L_{mag}} -$$

$$\omega_{leak,m3} * C_i\Big) * \sin(\omega_{leak,m3} * t) + (V_{ci,ini,3} - V_{dc,caps}) * \Big((\omega_{mag,m3})^2 * C_i - \frac{1}{L_{mag}}\Big) *$$

$$cos(\omega_{mag,m3} * t) - \Big(-L_{mag} * \ I_{M,ini,3} + \frac{I_{L,ini,3}+I_{M,ini,3}}{(\omega_{leak,m3})^2*C_i} - \frac{I_{M,ini,3}}{(\omega_{leak,m3})^2*(C_i+C_o)}\Big) * \Big(\frac{\omega_{mag,m3}}{L_{mag}} -$$

$$(\omega_{mag,m3})^3 * C_i\Big) * \sin(\omega_{mag,m3} * t)\Big) \quad (\boldsymbol{D.8})$$

where $I_{M,ini,3}$ is the magnetizing current at the beginning of this mode (initial value), $I_{L,ini}$ is the leakage current at the beginning of this mode (initial value), $V_{ci,ini,3}$ is the inverter capacitance voltage at the beginning of this mode (initial value), C_o is the capacitance of the rectifier FETs, $\omega_{leak,m3}$ is the resonant frequency of the capacitors and leakage inductance in radians and it is defined in (7.1) in hertz, and $\omega_{mag,m3}$ is the resonant frequency of the capacitors and magnetizing inductance in radians and it is defined in (7.2) in hertz; finally $V_{dc,caps}$ is defined as:

$$V_{dc,caps} = \Big(\frac{C_O}{C_i + C_O}\Big) * (V_{ci,ini,3} - V_{co,ini,3}) \quad (\boldsymbol{D.9})$$

where $V_{co,ini,3}$ is the rectifier capacitance voltage at the beginning of this mode (initial value).

The equations that describe mode 4 (with equivalent circuit shown in Fig. 7.3(d)) are:

$$I_{L,m4} = -\omega_{m4} * C_O * (V_{in} * N + V_{Co,ini,4}) * \sin(\omega_{m4} * t) + \ I_{L,ini,4} * \cos(\omega_{m4} * t) \quad (\boldsymbol{D.10})$$

$$I_{M,m4} = -\frac{V_{in} * N}{L_{mag}} * t + I_{M,ini,4} \qquad (\boldsymbol{D.11})$$

$$V_{co,m4} = \left(V_{in} * N + V_{Co,ini,4}\right) * \cos(\omega_{m4} * t) + L_{leak} * \omega_{m4} * I_{L,ini,4} * \sin(\omega_{m4} * t) - V_{in} * N \quad (\boldsymbol{D.12})$$

where the "*ini*" values are the initial conditions of this mode, and ω_{m4} is defined as:

$$\omega_{m4} = \frac{1}{\sqrt{L_{leak} * (C_O)}} \quad (\boldsymbol{D.13})$$

Chapter 8: Full System Performance Evaluation and Comparisons with State of the Art

In the previous chapters we have discussed all subsystems of the proposed ac/dc converter. In this chapter we provide more details about the full system and evaluate it's performance. At the end we will compare to other similar state of the art designs.

8.1 Layout, volume distribution and power density

A simplified representation of the full system is found in Fig. 8.1. Each main subsystem is highlighted in colored rectangles. A photograph of the optimized full system circuit board annotated to illustrate the corresponding circuit blocks is shown in Fig. 8.2. This optimized system was laid out by Mr. David Otten of MIT, who also contributed a variety of aspects to the final design; full system schematics, PCB files and a bill of materials is included in Appendix I. The full converter includes the active line rectifier, EMI filter (on the dc side of the rectifier), PFC converter modules, isolation stage, auxiliary power supply and control circuitry.

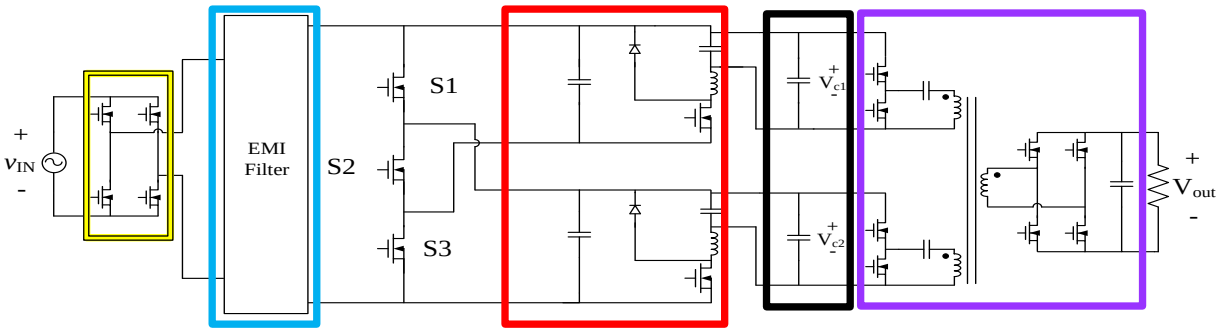


Figure 8.1 Simplified full power stage schematic of the ac/dc converter. Color code: in yellow is the rectifier FET bridge, in blue is the EMI filter, in red are the RTI buck converters, in black the energy buffering capacitors and in purple is the isolated, second stage dc/dc converter.

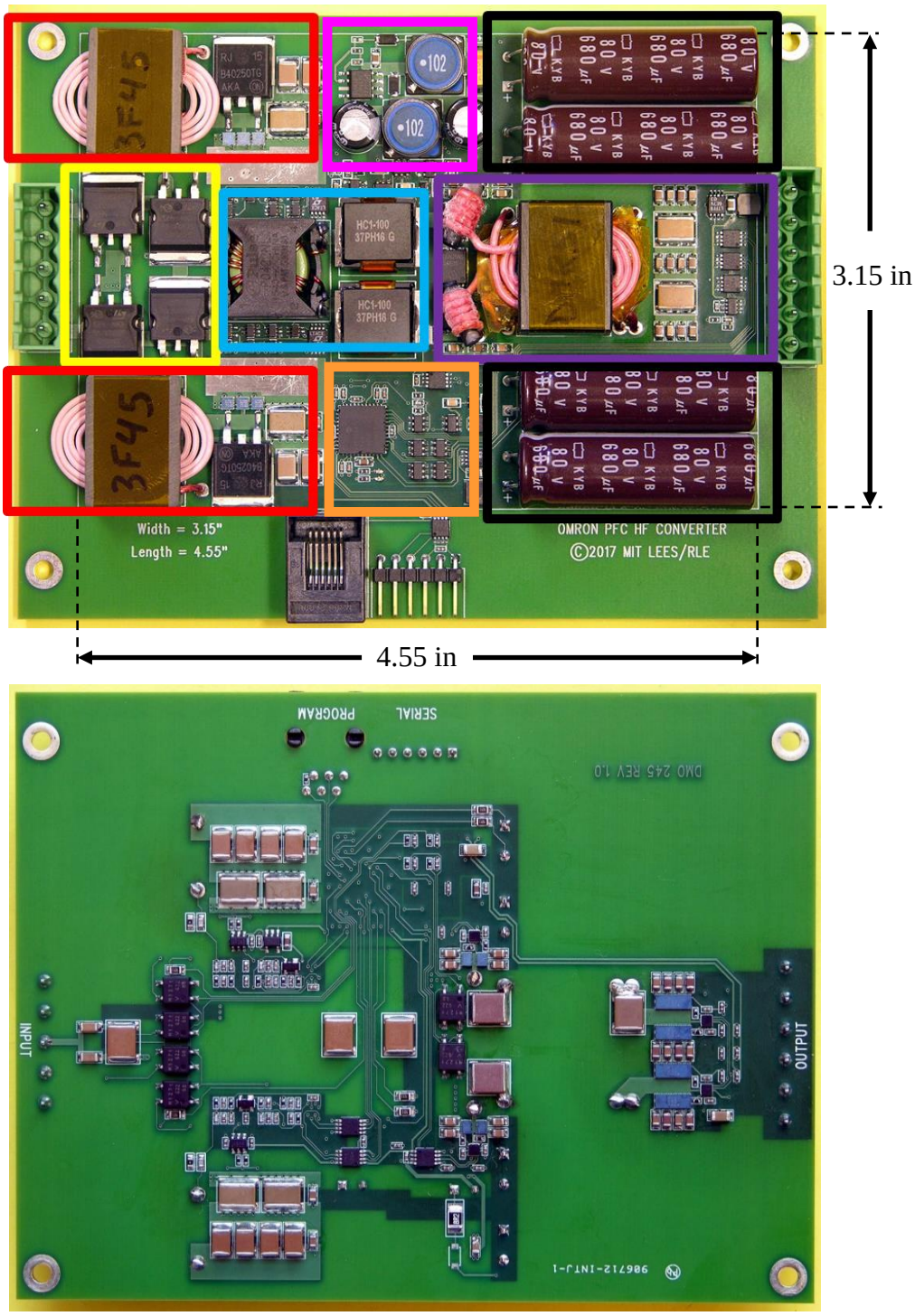


Figure 8.2. Top and bottom sides of the full system PCB; full schematics, BOM, and PCB layouts are provided in Appendix I. There is space for cutouts for the capacitors and magnetics which bring the total board height to 0.5 inches. The height is limited by the diameter of the electrolytic capacitors. Color code: yellow is the rectifier FET bridge, blue is the EMI filter, magenta is the "hotel supply" (on board power supply for controller and drivers), orange is the microcontroller (with peripherals), red are the RTI buck converters, black are the energy buffering capacitors and purple is the isolated, second stage dc/dc converter. The configuration switch network lies underneath the leakage inductance rods (near the transformer primaries). Layout by Mr. David Otten. Width=3.15 in, Length=4.55 in.

Table 8.1. Box volume breakdown of the full system. The total height is 0.5 inches. The major contributors are the buck PFC stage, the energy buffering capacitors and the isolated dc/c converter stage.

Item	Area (in^2)	System Volume Contribution (in^3)	Fraction (%)
EMI Filter	1.216	0.608	8%
Line Rectifier	1.215	0.608	8%
Mode Switch	0.278	0.139	2%
Buck	3.58	1.79	25%
Energy Buffer	3.45	1.725	24%
Control	1.036	0.518	7%
Isolation Stage	2.706	1.353	19%
Control Supply	0.852	0.426	6%
Total	14.333	7.166	100%
Density	34.89	watts/in^3	

This prototype converter, (which has length = 4.55 in, width = 3.15 in, height = 0.5 in, power rating = 250 W) provides a "box volume" power density of 34.9 W/in^3. This very high power density is achieved through the proposed architecture and multi-MHz operation. A breakdown of the volume is shown in Table 8.1. The RTI buck converter, the energy buffering capacitors and the isolation stage dominate the volume of the system.

8.2 Line current shaping and other incremental efficiency improvements

Various incremental improvements were made in the PFC stage when compared to the results shown in chapter 6 (i.e. the difference in efficiency and power density is due to more than just changing the commercial converters for the custom one). The major changes were (1) that the line rectifier was changed from a diode bridge to an active FET bridge, and (2) that additional line current shaping was done to improve system efficiency while maintaining line current waveforms within allowable harmonic specifications. Minor changes include adjusting the operating frequency of the second stage (from 1 MHz to 575 kHz), changing the average voltage on the buffer capacitors as a function of the load (from ~72 V at 100 W load to ~74 V at 250 W load) and adjusting dead time as a function of power in the second stage (as discussed in Chapter 7). It is estimated that these modifications improved the efficiency by ~2%. Many of these improvements were done empirically (i.e. tuning parameters and checking efficiency) by David Otten, however line current shaping was done in a more systematic way that is worth exploring.

8.2.1 Line current shaping

Figure 8.3 shows a screen shot from the Yokogawa power analyzer. The converter is drawing a rough approximation to sinusoidal current from the line, limited by its ability to draw current at low voltage points owing to the use of a buck PFC configuration. Because the PFC stage is a step-down converter, it cannot operate to draw current from the line until the line voltage reaches a certain value, approximately 150 V in this instance. That is the reason for the “clipped” current waveform. There is some additional distortion in the current due to the fact that the “line” current sensors are at the inputs of the step-down converters (i.e. after the EMI filter). While the controller is set to draw a scaled version of the line voltage, the EMI filter plays a role in adding some distortion and phase shift to the current measured by the power analyzer (i.e. the true line current).

Figure 8.3. Line voltage (red), line current (yellow), output voltage (blue) and output current (purple) for the following operating point: input of 230 Vac output voltage of 24 V and output power of 251 W. The power factor is 0.941 and efficiency 95.02%. The line current is set to follow the line voltage. However the current sensor is placed after the EMI filter and thus the controller makes the stacked converter input current sinusoidal. The line current is slightly distorted by the EMI filter.

Figure 8.4 shows the harmonic current (for Fig. 8.3) relative to the Class D limits imposed by the EN-61000-3-2 international standard (discussed in Chapter 1). The harmonic closest to its limit is the 9th, though it is still only slightly above 50% of the allowed current draw. This means we can further distort the line current and still have a compliant waveform. Reviewing the characteristics of the proposed PFC stage (Chapter 3), the RTI buck converters operate with higher efficiency for lower input voltage (i.e. for a lower step-down ratio). This raises the question of whether we can draw more current at lower line voltage (when the converters are more efficient)

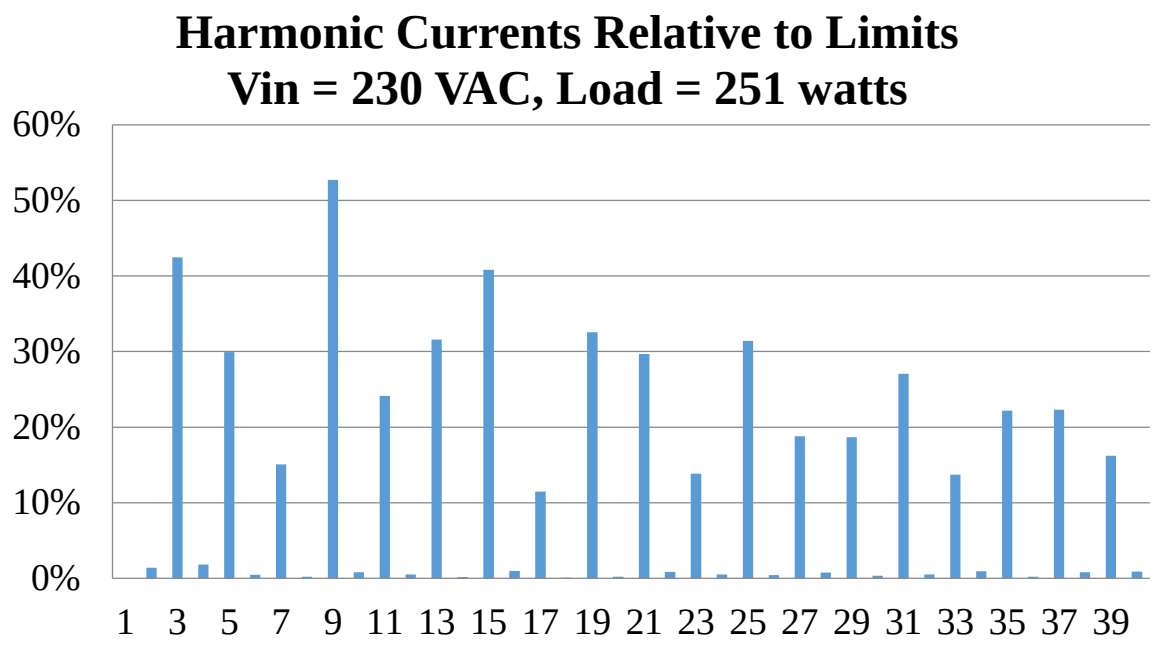


Figure 8.4. Harmonic currents relative to the limits stated by EN61000-3-2 from the current waveform in Fig. 8.3. The 9th harmonic is the closest to its limit. Operating point: input of 230 Vac, 60 Hz, output voltage of 24 V and output power of 251 W. This data was collected by extracting the current waveform data points from the Yokogawa Power Analyzer, and post processing it in Excel to acquire the harmonic information.

and less current during peak of line resulting in an overall efficiency improvement. This type of line distortion technique has sometimes been pursued to reduce twice-line-frequency energy storage [25]; here we use it to improve overall efficiency.

Figure 8.5 shows the power analyzer waveforms for the modified line current, which is selected to draw increased current when the voltage conversion ratio of the RTI buck converter is low (where it exhibits the highest efficiency). This waveform is taken as proportional to the derivative of the line voltage (instead of proportional to the absolute value of line voltage as in Fig. 8.3). The derivate of the line voltage is high at the moment conduction starts and decreases as the line voltage peaks. This control strategy allows us to draw more current at lower line voltage than at peak; in addition to leveraging the high efficiency operating point of the PFC buck converter, this

waveform also flattens the input power drawn during the time that the converter operates (a characteristic in common with the design in [22]). The slight asymmetry in the waveform could also be attributed to the EMI filter between the line and the buck converters. The overall system efficiency with this modified current waveform increased by about 0.2%, corresponding to reduction in total losses by 5%. Figure 8.6 shows the harmonic content of the modified current waveform and it still is within the bounds of EN61000-3-2.

8.2.2 Active bridge rectifier and configuration switch

The active bridge rectifier and the configuration switch played an important role in the high efficiency of the converter. The design and control strategy of the rectifier was done by Mr. David Otten. As shown in Fig. 8.1 (yellow outline), an active rectifier bridge is used at the input of the supply to maximize efficiency. STB32NM50N FETs with a typical on-resistance of 0.1 Ω are used to provide low conduction losses and withstand peak input voltages of 500 V. The gates are driven by Vishay VOM1271 photovoltaic MOSFET drivers with integrated fast turn-off. They are able to turn off the rectifier FETs in under 20 μs though it takes 1-2 ms to turn them on. Because the rectifiers operate at line frequency, this is not a problem. The input voltage is continuously monitored by the controller and compared with the buck converter output voltage. If the input is more than 15 V higher than the output voltage, the appropriate FETs are turned on. If the voltage difference is less than 8 V, they are turned off. When the supply is first powered up and no gate drive signals are supplied, the body diodes of the FETs perform as a conventional full bridge rectifier.

The configuration switch network shown in Fig. 8.1 (switches S1, S2 and S3 between the blue and red outlines) is used to connect the two buck converters in series or parallel. Infineon BSC600N25NS3 FETs with an on-resistance of 60 mΩ and a rated voltage of 250 V are used for

this function. S1 and S2 are also driven by Vishay VOM1271 photovoltaic MOSFET drivers but S3 does not require an isolated drive. When no gate drive signals are present, the two buck converters are connected in series by the body diode of S2. This default condition at power up allows time for the controller to measure the input line voltage and determine if series or parallel operation is required, based on the input line voltage. The appropriate switches are normally turned on when the supply is first started and not changed.

Figure 8.5. Line voltage (red), line current (yellow), output voltage (blue) and output current (purple) for the following operating point: input of 230 Vac output voltage of 24 V and output power of 251 W. The power factor is 0.948 and efficiency 95.236%. This data point is taken including all the software changes that increase efficiency. The converter does not draw peak current when the voltage is maximum.

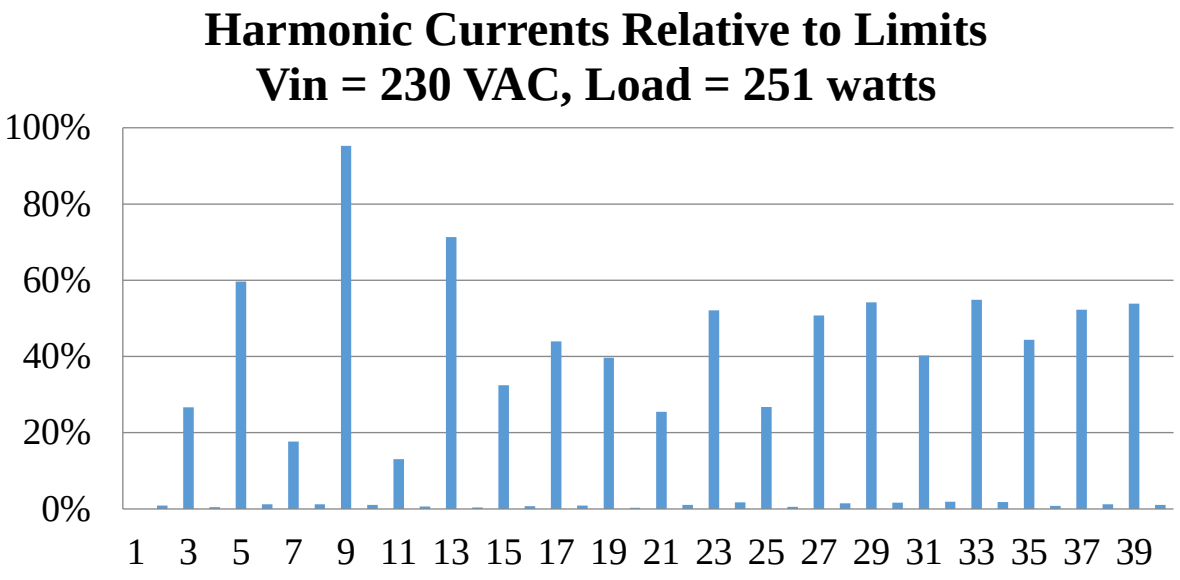


Figure 8.6. Harmonic currents relative to the limits stated by EN61000 from the current waveform in Fig. 8.5. The 9th harmonic is the closest to its limit. Operating point: input of 230 Vac, 60 Hz, output voltage of 24 V and output power of 251 W. This data was collected by extracting the current waveform data points from the Yokogawa Power Analyzer, and post processing it in Excel to acquire the harmonic information.

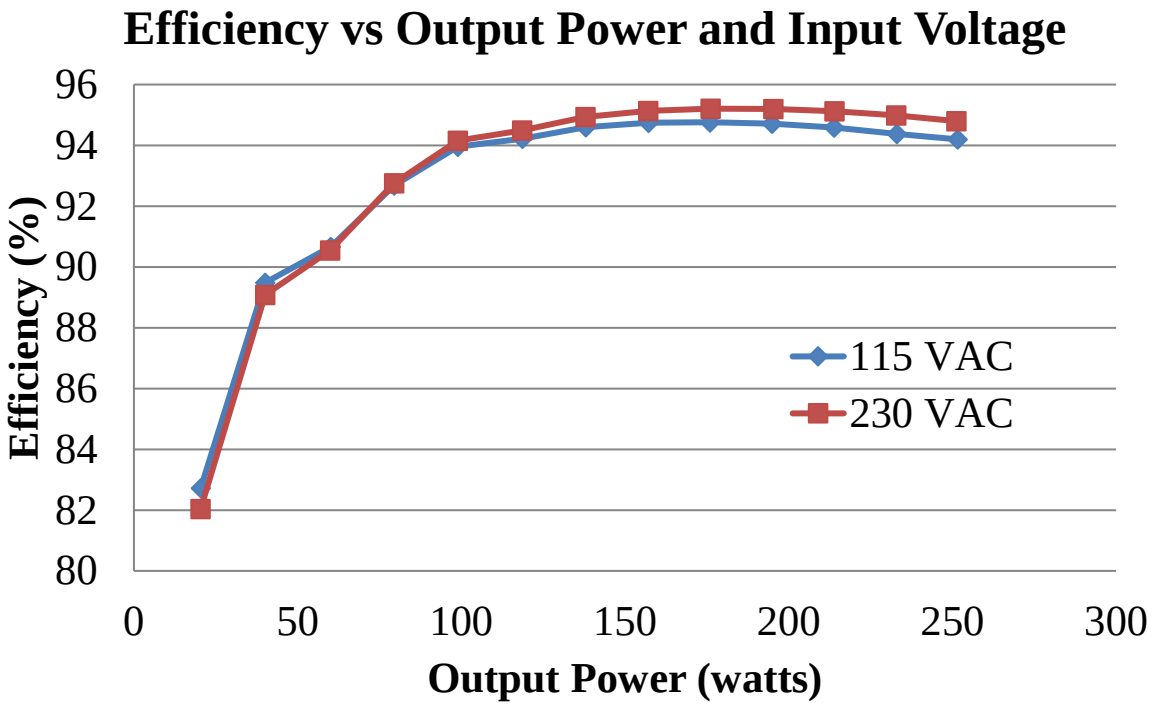


Figure 8.7. Full system efficiency at 115 Vac RMS and 230 Vac RMS, both at 60 Hz input. Only the active bridge rectifier is implemented here out of all the efficiency improvements discussed in section 8.2. Efficiency at full power (250 W) at 230 Vac is 94.80% and at 115 Vac is 94.20%. Output voltage is 24 V.

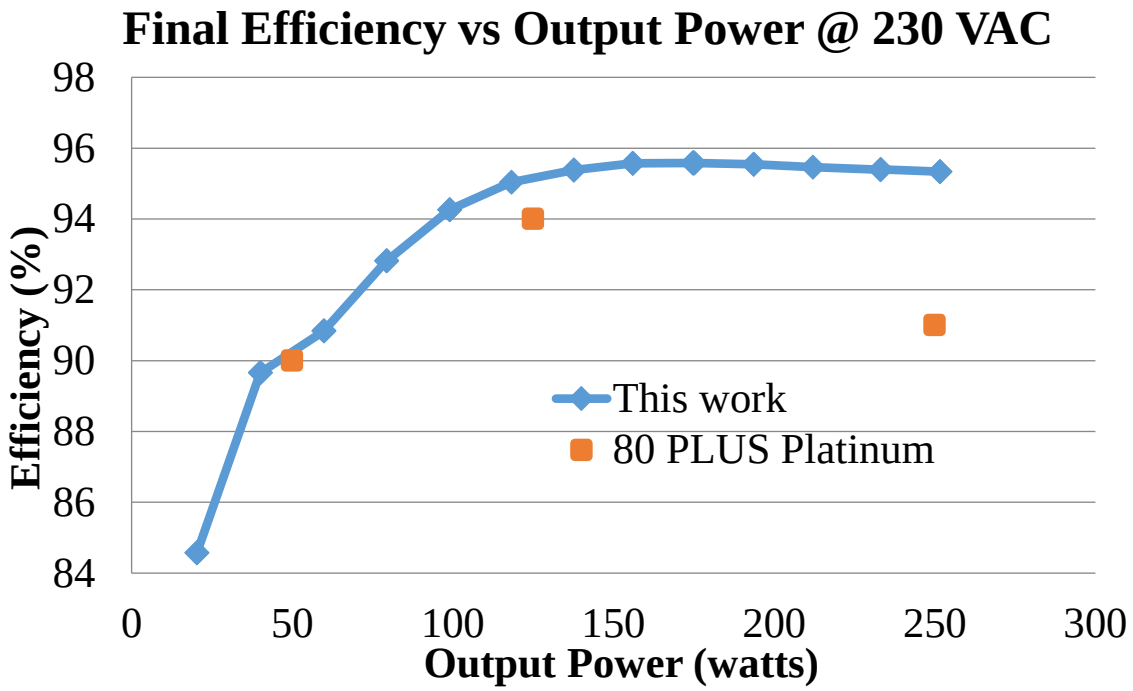


Figure 8.8. Full system efficiency at 230 Vac RMS, 60 Hz input after all empirical adjustments have been implemented. Efficiency at full power and 230 Vac is 95.33%. The output voltage is 24 V. The orange points are the efficiency requirement for 80 PLUS Platinum. The proposed converter meets the 80 PLUS Platinum requirements.

8.3. Full system efficiency

Figure 8.7 shows the full system efficiency at 115 Vac and 230 Vac. It is important to note that this data is taken BEFORE most of the incremental efficiency improvements talked above are implemented. The only improvement taken into account in this plot is the active bridge rectifier. This is the last data taken at “low line” voltage and it is useful to compare system performance across its operating range. (The focus shifted to 230 Vac input because that is the voltage that both EN61000-3-2 and 80 PLUS standards evaluate converter performance at.) One can see that at high power the efficiency at 115 Vac drops compared to 230 Vac. This is because 115 Vac processes twice the line current, which leads to extra loss in the rectifier and the EMI filter. The full power efficiency at 250 W is 94.80% at 230 Vac and 94.20% at 115 Vac.

Fig. 8.8 shows the final full system efficiency at 230 Vac, which is the operating condition relevant to the "80 Plus" efficiency specifications. In this data, all efficiency improvements from section 8.2 have been implemented. The peak efficiency is 95.58% at 175 W and the full power efficiency is 95.33%. In the next section we compare this converter with other state-of-the-art converters.

8.4 Comparison to state of the art

Figure 8.9 shows a full load efficiency vs power density plot for various converters; full details of each plotted point are indicated in Table 8.2. We consider full-load efficiency as an important metric because this is the condition that often determines achievable size reduction owing to thermal constraints. Of the commercial converters [14,16,17] shown, only the 170 W converter from Murata [14] meets the 80 PLUS Titanium rating (the highest tier awarded by 80 PLUS, and one tier higher than our proposed design). This plot suggests that there is a clear trade-off between achievable size and efficiency in ac/dc converters. This is to be expected. For example, one can increase power density by shrinking magnetics size in a design, but such a reduction typically worsens loss (owing to increased core and conductor loss).

Clearly, the proposed conversion approach yields an exceptionally high combination of size and efficiency (considering both full load and “80 PLUS” efficiency metrics). This high performance, which extends the Pareto front in the important metrics of efficiency and power density, is accomplished while meeting the numerous challenges in PFC conversion detailed in Chapter 1 (wide input range, isolation, holdup, etc.). If we were to remove some of these constraints, such as universal input or hold-up time, the proposed approach would be able to achieve still higher power density at constant efficiency, or achieve higher efficiency at constant

power. It may be concluded that the proposed approach is effective for advancing the state of the art in PFC power supplies for computer applications.

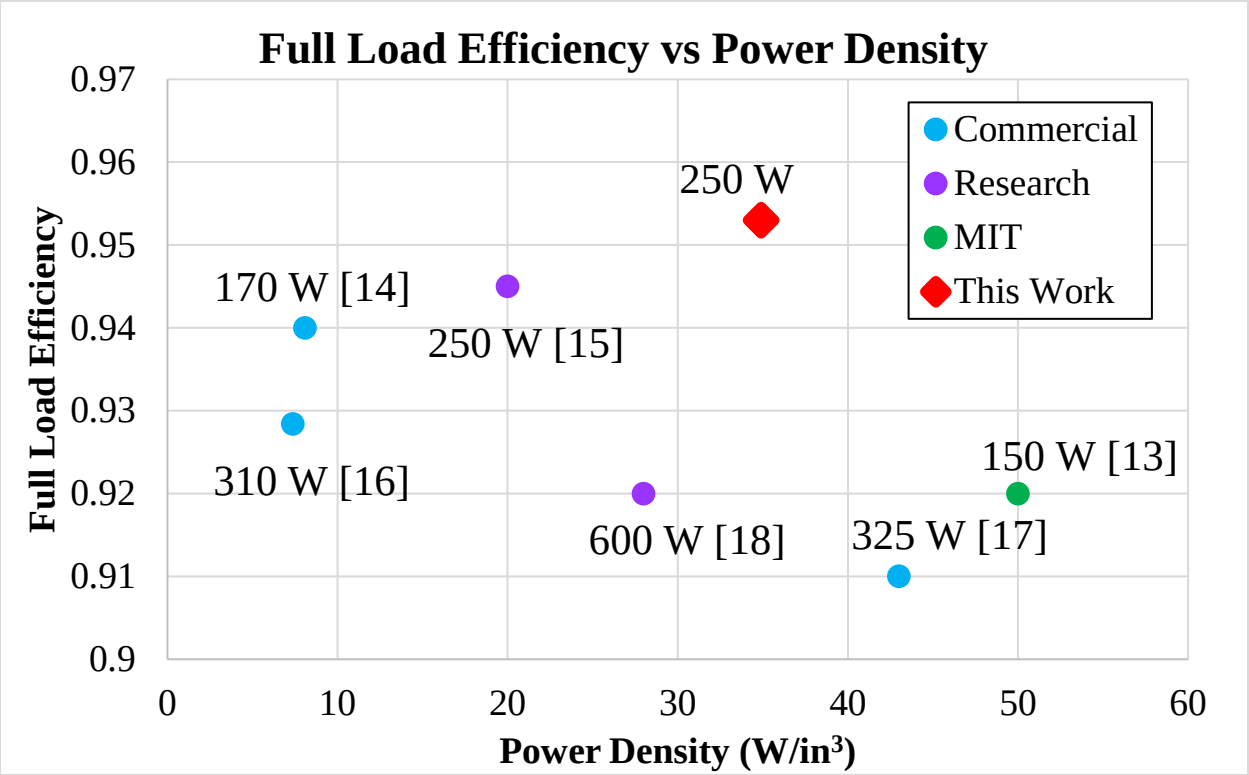


Figure 8.9. Full load efficiency vs power density for comparable, state of the art converters. All the converters featured here have universal input, energy buffering capacitors and similar output voltage and power ratings.

Table 8.2. Data from various converters, both from research and commercial. This data was used to generate the plot in Fig. 8.9. The densities with stars are estimated as a value was not presented in the publication.

	[13]	[14]	[15]	[16]	[17]	[18]
Output Power (W)	150	170	250	310	325	600
Density (W/in^3)	50	8.1	20*	7.381	42.97	28
Efficiency	0.92	0.94	0.945	0.928	0.92	0.92
Output Voltage (V)	12	12	48	28	24	24
Universal Input	yes	yes	yes	yes	yes	yes

Chapter 9: Conclusions and Future Work

This thesis explores topic of miniaturization of ac/dc converters. The thesis explains the requirements and challenges of designing ac/dc converters. Afterwards the thesis breaks down and explains each subsystem in detail, along with topology selection, trade-off analysis and experimental results. The thesis ends with an evaluation of the full system performance and comparison to other converters.

9.1 Thesis summary and contributions

Chapter 1 contains the introduction to the thesis, motivation for this work, background information and what has been already done in the field. This chapter includes a literature review of the state of the art, a breakdown of the key challenges in the design, and a preface to the approach used here.

Chapter 2 contains an overview of the architecture to be used in this work. Multiple approaches towards reconfigurable PFC converters were considered and this chapter includes an analysis of the advantages and disadvantages of each approach. Only one architecture was selected to be prototyped. The final architectural decisions are justified here.

All subsystems in the converter are affected by the architectural choices made here. For example, using stacked converters means there are two outputs to the PFC stage, so this imposes a power combining requirement on the second stage. Subsystem trade-offs need to be understood very well because they are critical to achieve high performance.

Chapter 3 details the PFC power stage building block, the RTI buck converter. Its operation is described along with component selection including inductor loss models. Experimental performance verifications are also presented here.

The RTI buck converter is a very useful topology for miniaturized PFC stages. It can operate with ZVS or near-ZVS over a relatively wide input voltage range; it offers a low characteristic impedance due to its DCM operation which is appropriate for grid-connected converters. It can also operate at the MHz range while processing over 300 W of peak power with greater than 98% efficiency.

Chapter 4 explores the energy buffering capacitor selection criteria: capacitance due to allowed ripple voltage, capacitance due to hold-up time requirement and capacitor RMS current rating. It also contains a study on the usable energy density of over a thousand electrolytic capacitors available in the online retailer Digikey.

A key aspect that affects all parts of the system is the energy buffering capacitor working voltage. This voltage affects the size of the capacitor itself, the converter's maximum achievable power factor, the harmonics injected into the line and sets various constraints on the second stage: step-down ratio, device rating and input voltage range.

Chapter 5 studies using commercially-available isolated converters as the second stage of the PFC converter. The options are analyzed based on efficiency and power density. The experimental performance of the full ac/dc system working with commercial converters is evaluated, along with system power density.

Using commercial second stage converters has various advantages (e.g. mass manufactured, output flexibility, ease of reconfiguration, etc.) but the difficulty in control when paralleling the outputs of two converters and the lower-than-desired efficiency convinced us to design a cutom converter.

Chapter 6 details the operation, design, component selection, and performance evaluation of a custom isolated converter as the second stage of the system. The justification for the topology as well as topological variants are reviewed. This section includes isolation transformer design.

A two input, single output custom converter has several advantages over using two commercial parts. First, there will always be redundancy in each commercial board, for example in control or safety circuitry. Therefore, we can achieve a higher overall power density with a custom design. Second, manufacturers typically will optimize the efficiency of their design over the complete, rated input voltage range. On the other hand, we can design our converter to be extremely efficient at the steady state input voltage and only have a wide input voltage during a hold-up time event (a transient event where efficiency is less of a concern). Finally, the controls are simpler because the selected topology is self-balancing and extracts the same amount of power from each input.

Chapter 7 talks about a control method of the custom converter from Chapter 6 that improves light-load efficiency. A model is developed for general DAB circuits to find the transfer characteristics between output power and switch dead time (for fixed phase shift), and said model is experimentally verified. The control law provides a significant increase in light load efficiency with no additional hardware nor volume costs.

Here we learned of an useful way to control DAB converters at light load: using dead time as a control handle. Dead time is a property of most converters that use complementary, controllable switches (such as half bridges or full bridges) and can be harnessed to deliver low power efficiently.

Chapter 8 presents the full system performance of the ac/dc converter with the custom isolated converter. Volume distribution and power density are also evaluated. The converter developed here is compared to other state-of-the-art converters.

Our final prototype has a full power (250 W) efficiency of 95.33% at 230 Vac, and a power density of 35 W/in^3. It is very competitive with both commercial designs and other research designs, as seen in Fig. 8.9.

The main contributions of this thesis are the topological variant trade-offs, design, modeling and component selection of each subsystem and how all parts are designed with the goal of miniaturization and high performance in mind.

9.2 Future Work

Looking at Table 8.1 (volume breakdown of the system), the limiting parts are the PFC buck stage and the energy buffering capacitors. With the advancement of semiconductors, new GaN switches have competitive figures of merit even at higher blocking voltages. Also new magnetic materials excelling in megahertz frequency range enable better magnetics designs. New switches and magnetic materials could make feasible the development of miniaturized HF boost PFC stages. This would allow the energy buffering capacitors to store energy at a higher voltage, reducing their size notably. However, this could compromise the efficiency of the second stage. With careful design, it could be possible to increase system-level power density without reducing efficiency greatly.

Another direction to take the project into the future is power scaling. Possible ways to scale the output power would be to use these 250 W converters as "modules" and connected them in parallel. This method would most likely decrease the system power density as we need to account for interconnection space. Increasing the power-handling capability of each subsystem would require new switches that can carry higher currents and re-designing the magnetics. At the time it is unclear what the power handling limits of today's components are without the addition of heat sinks or external fans, but it would be an interesting question to explore.

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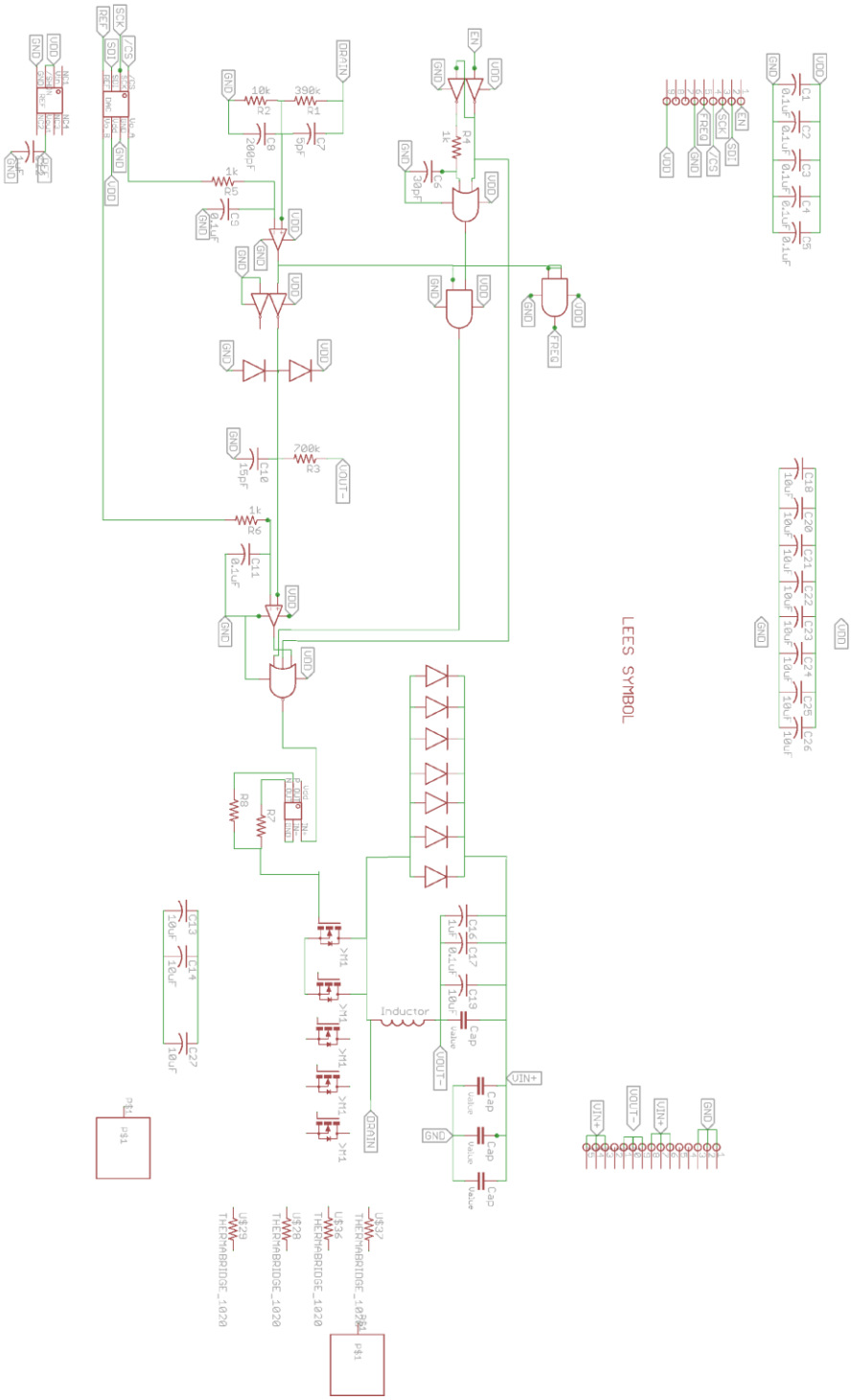
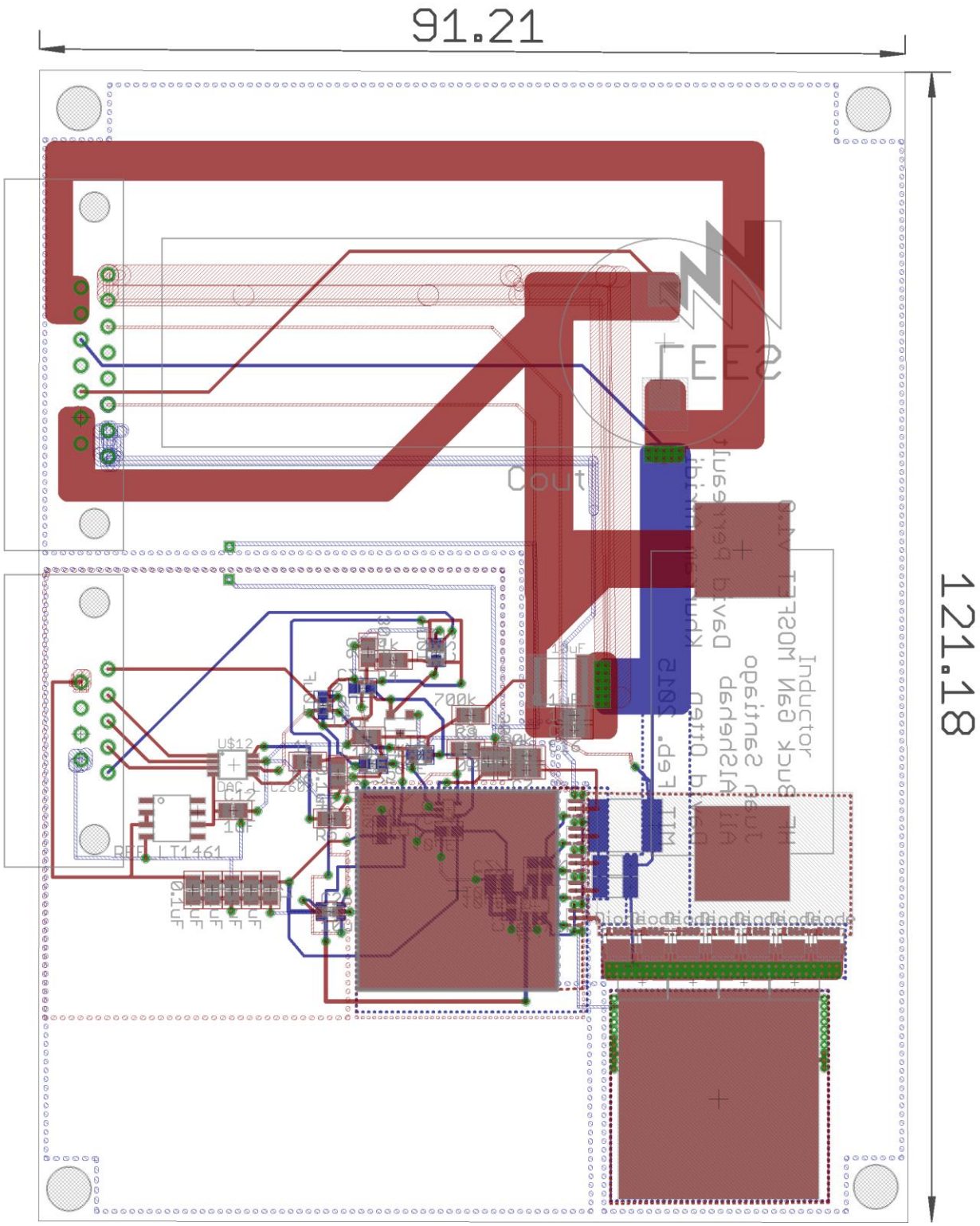
APPENDIX A

RTI Buck converter schematic and PCB files

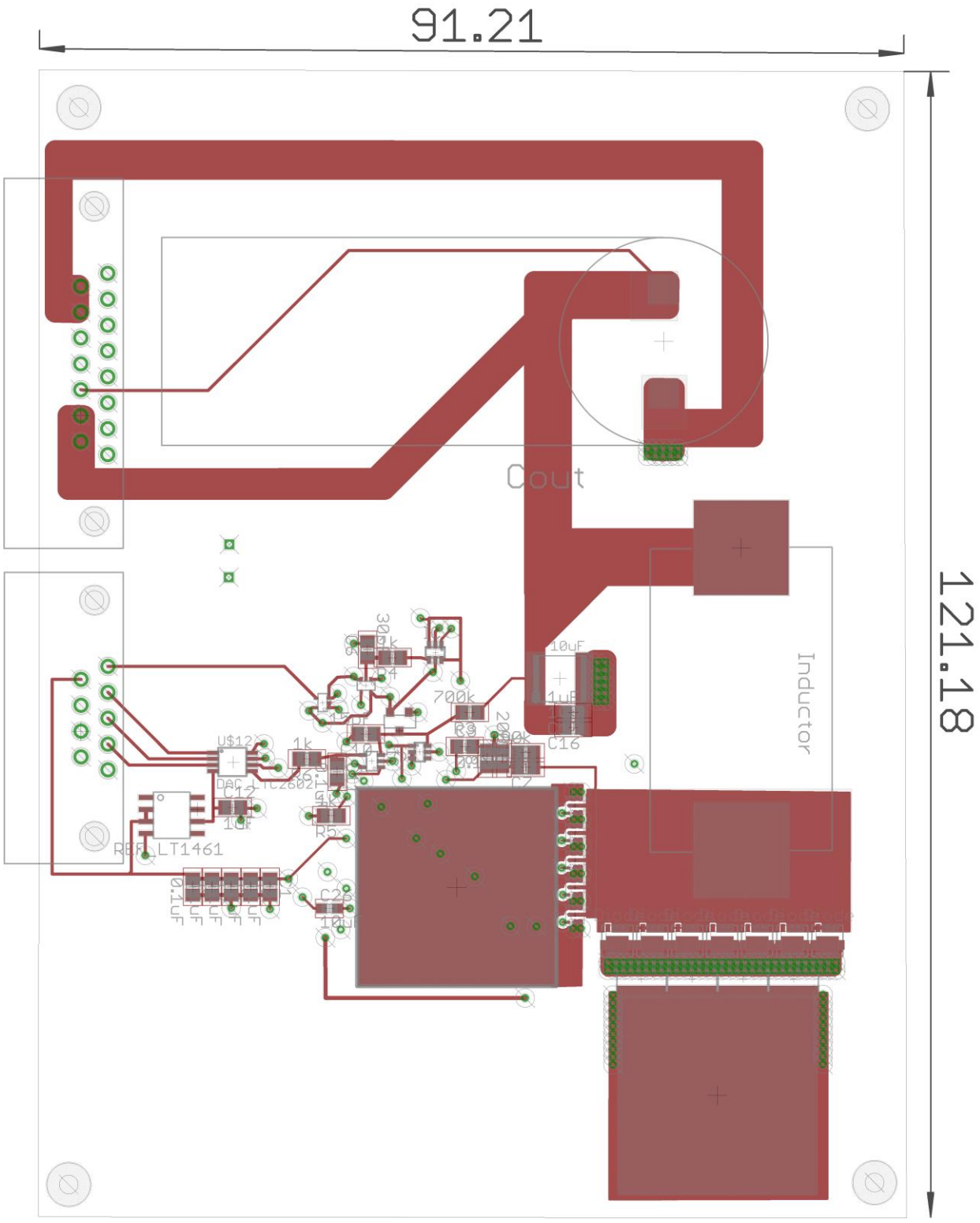
A.1 Schematic



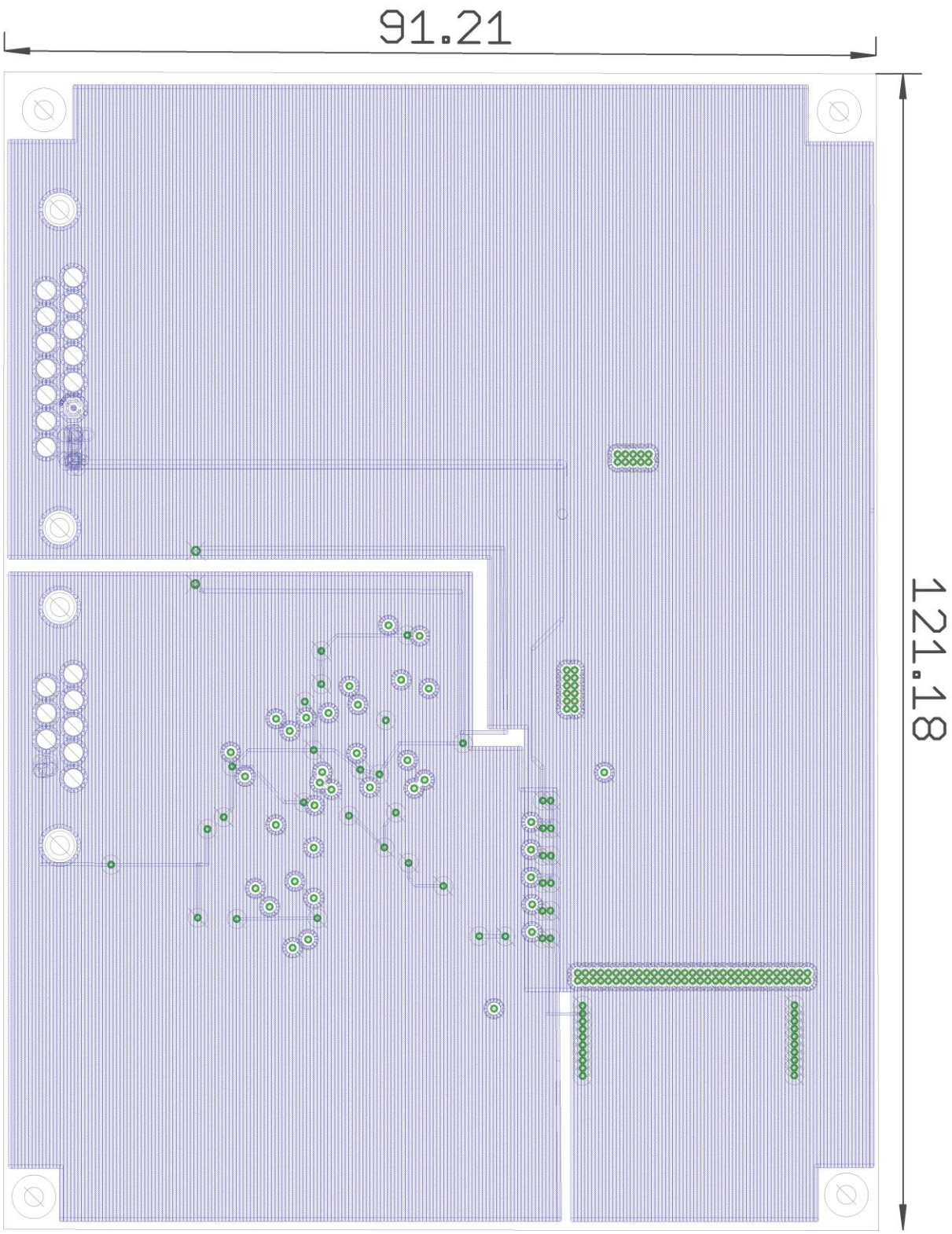
A.2 Layout



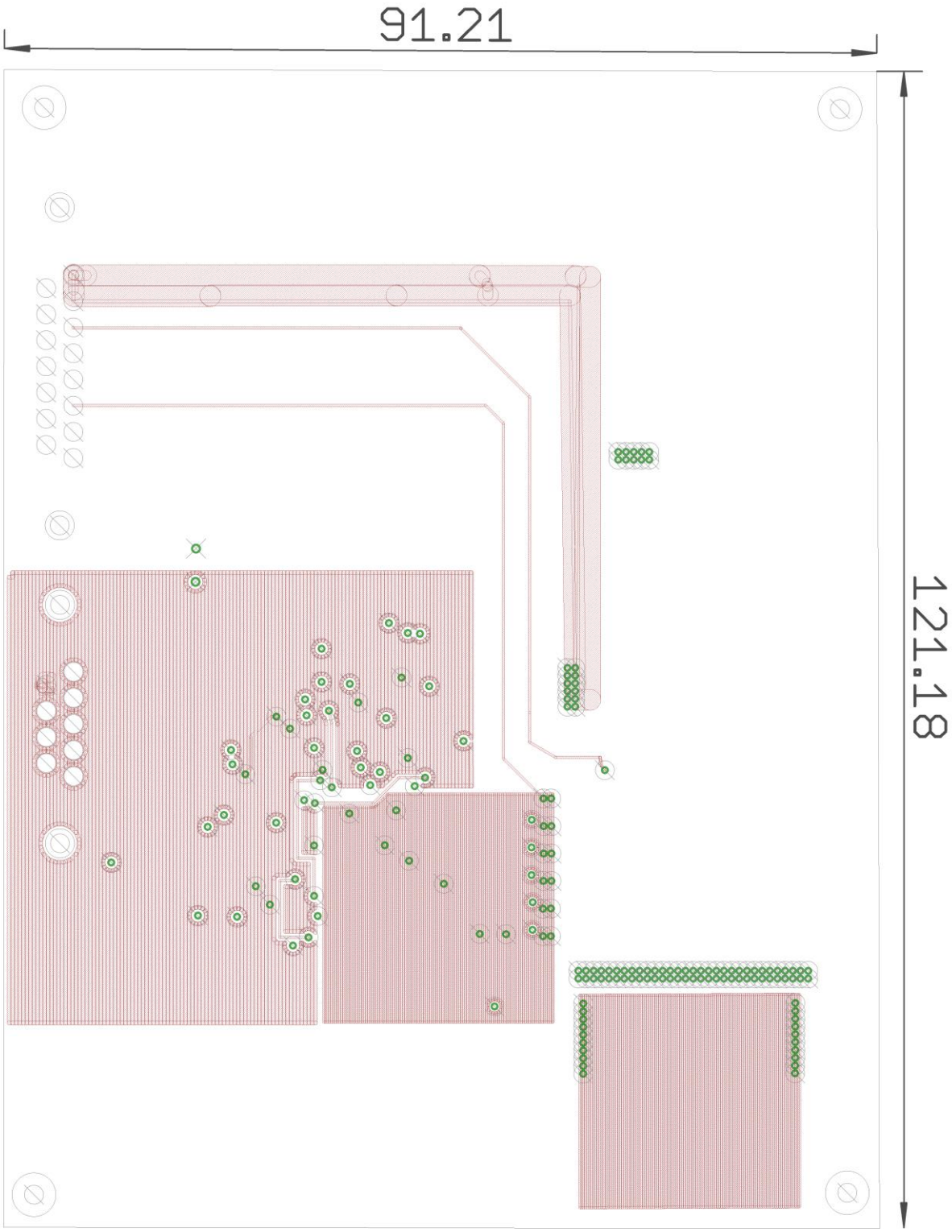
A.3 Top Layer


91.21
121.18
Cout
Inductor
10uF
1uF
C16
700k
1k
DAC
C12
10k
REF
LT1461
C2
10uF

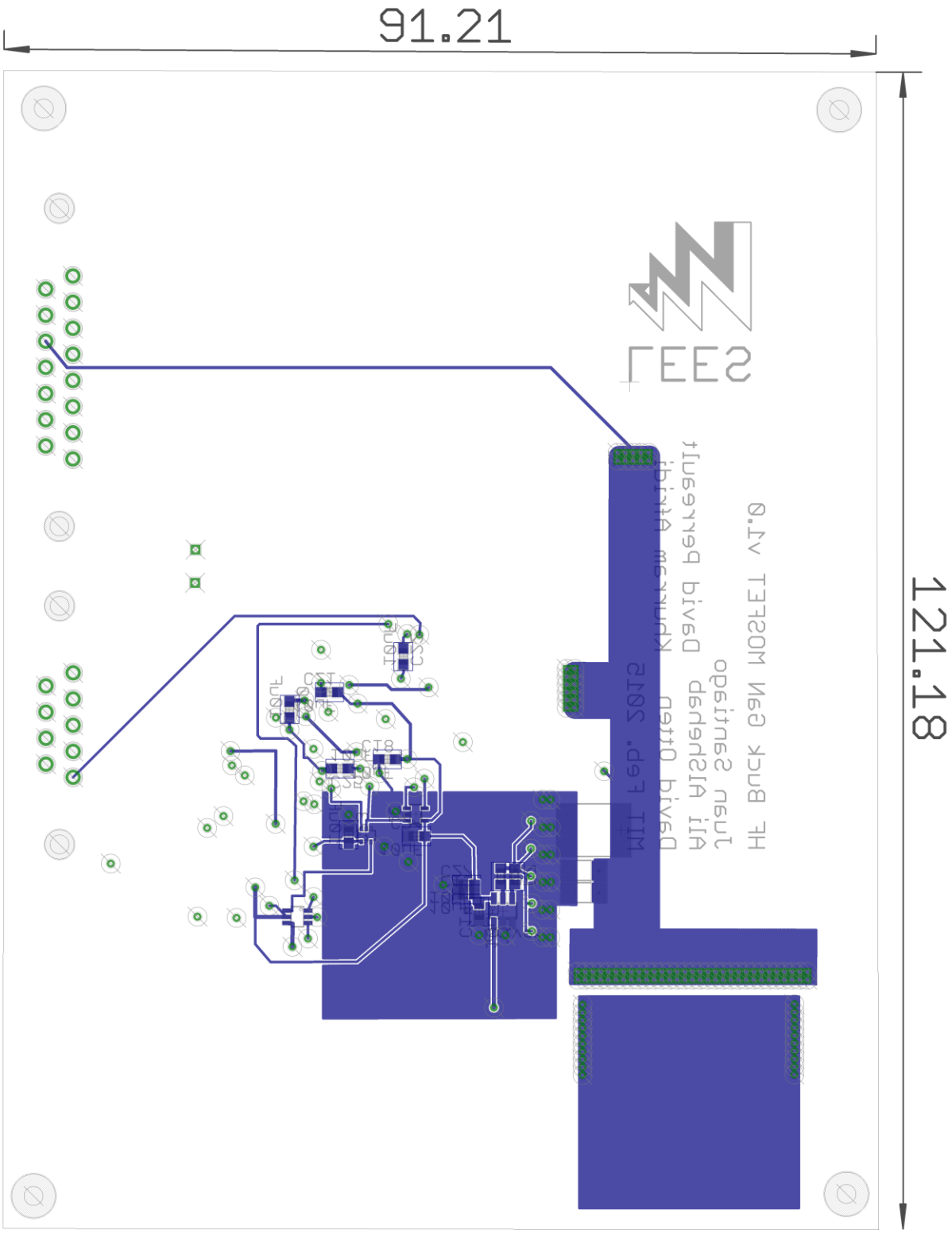
A.4 Inner Layer 2



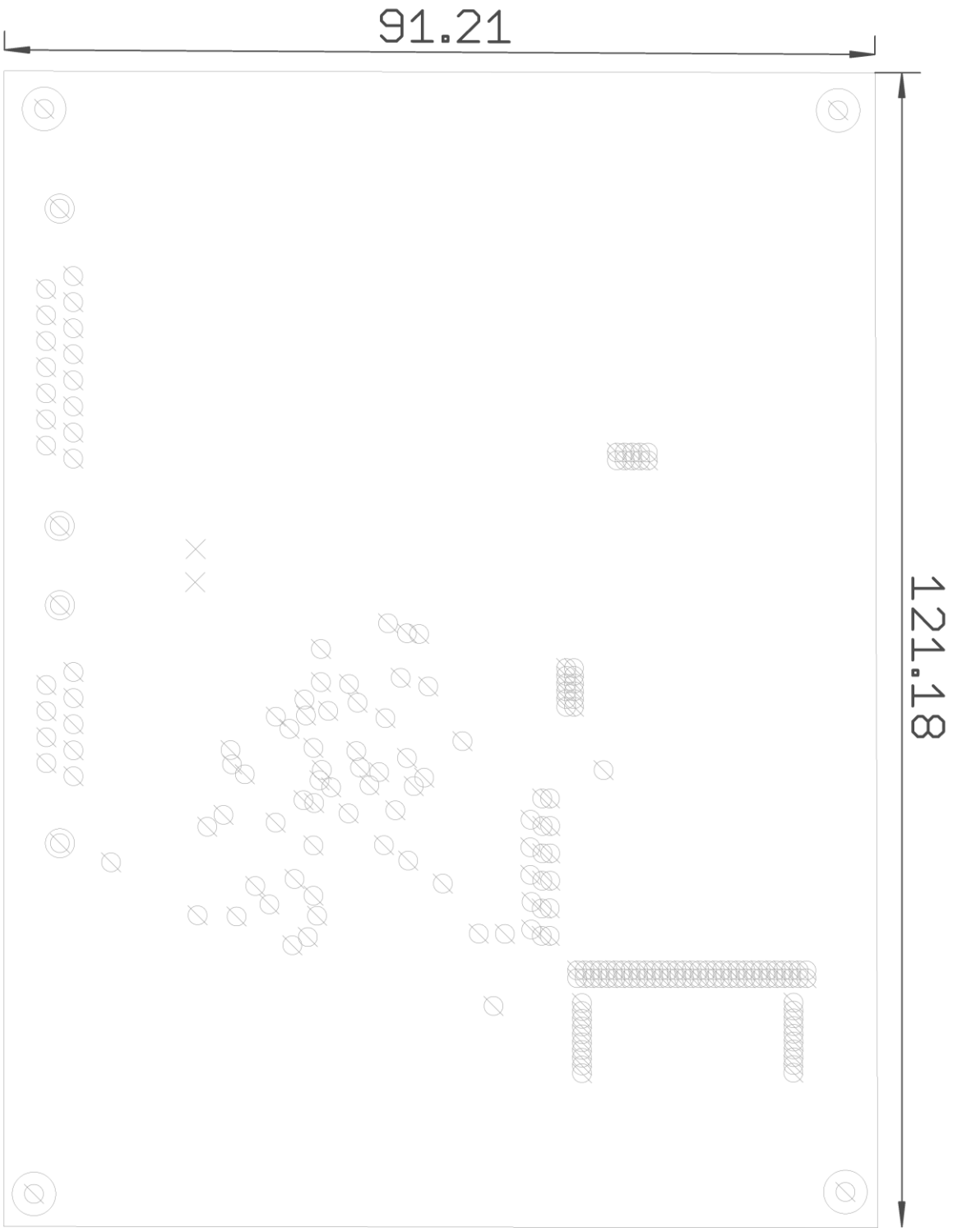
A.5 Inner Layer 3



A.6 Bottom Layer



A.6 Drill file



APPENDIX B

Inductor design Matlab script

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% The script calculates the Core loss, winding loss and temperature rise
% for all feasable planar inductor designs with DCM triangular current
waveforms
% Based on David Perreault's PhD optimization files
%
% Author: Ali S. AlShehab
% Review: Juan A. Santiago
% Date: July 2015
% Edited further by: Juan Santiago Sept 2015 (litz wire analysis)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
clc
clear all
close all

%% To run this code:
% Make sure the core data file is in the same directory as this file. And,
% 1- Choose the core geometry and core type.
% 2- Specify the operating frequency, currents (Irms, Ipk, Iavg)
% 3- Specify the K, y and relative permiability values for the material
%    at frequency of interest
% Steps explained below:

% 1- Choose and load the core geometry and core type. (Comment/Uncomment)
%EQCoredat;             % EQ Cores have a circular center post
PlanarECoredat;      % PlanarE Cores have a rectangular center post
%EILPCoredat;         % EILP Cores have a rectangular center post

Coretype = 1;          % Coretype 1 has a rectangular center post
%Coretype = 2;        % Coretype 2 has a circular center

% 2- Specify the operating frequency, currents (Irms, Ipk, Iavg)
f = 1.3e6;              %Specify operating frequency (Hz)
f_str = '1.3 MHz';      %For plotting purpose
Ipk= 9.08;              %Specify peak current (A)
Irms= 5.1245;           %Choose current RMS (A)
Iavg= 4.246;            %Choose average current  (A)


% 3- Specify the K, y and relative permiability values for the material at
frequency of interest:
K1 = 0.7661; y1 = 2.0457;  % Coefficients of power for 4F1 @ 1MHz
K2 = 1.7385; y2 = 2.0665;  % Coefficients of power for 4F1 @ 5MHz

K3 = 0.0138; y3 = 2.7287;  % Coefficients of power for 3F4 @ 1 MHz
K4 = 7.0863; y4 = 2.0517;  % Coefficients of power for 3F4 @ 4 MHz

K5 = 0.0107; y5 = 2.6149;  % Coefficients of power for 3F45 @ 1 MHz
K6 = 8.248; y6 = 2.2057;   % Coefficients of power for 3F45 @ 4 MHz
```

```
K7 = 0.0973; y7 = 2.441;   % Coefficients of power for 67 @ 1.3 MHz
K8 = 0.6863; y8 = 2.2016;  % Coefficients of power for 67 @ 5 MHz

K = K5; % Choose K value
y = y5; % Choose y value
ur = ur_3F45; % Choose relative permiability of core material: ur_3F4,
ur_F67, ur_3F45, ur_4F1

% 4- Other parameters and specifications:

I_n =[0.4302; 0.0747; 0.0243; 0.0271; 0.0032; 0.0103; 0.0058; 0.0041; 0.0074;
0.0032] .* Ipk; % Fourier Coefficients of waveform

% Applies for DCM triangular current waveform
Bmax = 0.3;                                    % Maximum flux density in T to
prevent saturation
Tmax = 50;                                     % Maximum temperature rise in
deg Celcius
L = 3e-6;                                      % Inductance in H
mu=4*pi*10^-7;                                 % Permeability of free space
(H/m)
p = 2.5e-8;                                    % Resistivity of copper (Ohm-m)
@ 125 deg C
N = 10;                                        % Max number of turns in an
inductor



awg=0.08e-3;                                   %40 awg, diameter of a single
strand in m
nst=100;                                       %number of strands
numw=2;                                        %number of litz wires used in
parallel



%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% End User Input
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

No_of_layers = 1;                              % Max number of layers
d = sqrt(2./(4*pi*10^-7*2*pi.*f*10^8/2.5));  % Skin depth in m
modeltype=1; % 1-D field approx for Fr (Dowell's model)

%% save core data
lg = zeros(numcores,N); %Gap length
ue = zeros(numcores,N); %Effective permiability
Bpk = zeros(numcores,N); %Peak magnetic field
Pcore = zeros(numcores,N); %Core loss
Ptot = zeros(numcores, N); %Lowest total loss
Ptot1 = zeros(numcores, N); %Total Losses using 1 layer
Ptot2 = zeros(numcores, N); %Total Losses using 2 layers
Ptot3 = zeros(numcores, N); %Total Losses using 3 layers
```

```
Ptot4 = zeros(numcores, N); %Total Losses using 3 layers
Pwind = zeros(numcores, N); %Lowest Winding Loss
Pwind1 = zeros(numcores, N); %Winding Losses using 1 layer
Pwind2 = zeros(numcores, N); %Winding Losses using 2 layers
Pwind3 = zeros(numcores, N); %Winding Losses using 3 layers
Pwind4 = zeros(numcores, N); %Winding Losses using 4 layers
No_layers = zeros(numcores,N); %Number of layers
deltaT = zeros(numcores,N); %Temperature rise
designok = zeros(numcores,N); %Design check

%% Loop through available cores and synthesize inductor designs

%Calc Delta(harmonic)
for harmonic = 1:length(I_n)
    Delta_n(harmonic) =awg*sqrt(harmonic*2*pi*1.3e6*pi*4e-7*(1/p)/2);
end



%Loop over all cores
for core =1:numcores

    %Calculate surface area for each core
    if Coretype == 1;
        SA(core)= 10000*(2*(h_core(core)*w_core(core)+
l_core(core)*w_core(core)+l_core(core)*h_core(core)- h(core)*(OD(core)-
ID(core)))+4*h(core)*w_core(core)+ 2*(OD(core)-ID(core))*w_core(core));
    elseif Coretype ==2;
        SA(core)= 10000*(2*(h_core(core)*w_core(core)+
l_core(core)*w_core(core)+l_core(core)*h_core(core)-
h(core)*OD(core))+2*pi*h(core)*(ID(core)/2)+ 2*(OD(core)*w_core(core)-
pi*(ID(core)/2)^2));
    end

    %Loop over different number of turns
    for n= 1:N

        designok(core, n) = 1; % assume this core design works

        %Calc gap
        %lg(core,n) = mu*Ae(core)*(1/Al(core,n) -
le(core)/(Ae(core)*mu*ur(core)));
        lg(core,n) = ((n^2*mu*Ae(core))/L)-(le(core)/ur(core));
        if lg(core,n) < 0
            designok(core, n) = 0;     % design is not ok
            disp([corename{core,:},' @ ',num2str(n),' turns rejected: lg =
',num2str(lg(core,n))]);
        end

        if lg(core,n) > 0.9*h(core)
            designok(core, n) = 0;     % design is not ok
            disp([corename{core,:},' @ ',num2str(n),' turns rejected: lg  =
',num2str(lg(core,n)), ' (larger than 0.5*core height)']);
        end

        % Calc the effective permeability (coefficient)
```

```
        ue(core,n) = ur(core)/(1+ur(core)*lg(core,n)/le(core));
        if ue(core,n) < 0
            designok(core, n) = 0;      % design is not ok
            disp([corename{core,:},' @ ',num2str(n),' turns rejected: ue =
',num2str(Bpk(core,n))]);
        end

        % Calc the peak magnetic field Bpk in Tesla
        Bpk(core,n) = ue(core,n)*mu*n*Ipk/le(core);
        if Bpk(core,n) > Bmax
            designok(core, n) = 0;      % design is not ok
            disp([corename{core,:},' @ ',num2str(n),' turns rejected: Bpk =
',num2str(Bpk(core,n)),...
                ' gauss']);
        end


        %Calc Core Loss
        Pcore(core, n)=(Vc(core)*K*(Bpk(core,n)*1000)^y)/1000;

        %Initialize Factors = Rac(n)/Rdc
        Factors = zeros(length(I_n), 1);

        %Calc turns per layer, dc resistance, and Winding Loss
        for number_of_layers=1:1
             turn_layer = zeros(1,No_of_layers); % This array will contain
the number of turns in each layer
             layer_dc_resistance = zeros(1,No_of_layers); % Array to store
the dc resistance for each layer


             ds=awg*1000; %strand diameter in mm


             if Coretype == 1;
                 dc_resistance=
p*2*(W(core)+ID(core))*n*4/awg^2/nst/pi/numw; %litz wire resistance
rectangular post
             elseif Coretype == 2;
                 dc_resistance= p*ID(core)*n*4/awg^2/nst/numw; %litz wire
resistance circular post
             end


             for harmonic=1:length(I_n) %Factors= Rdc*Rac(n)/Rdc

                   Factors(harmonic) =
dc_resistance*Delta_n(harmonic)*(((sinh(2*Delta_n(harmonic))+sin(2*Delta_n(ha
rmonic)))/(cosh(2*Delta_n(harmonic))-cos(2*Delta_n(harmonic))))+ ...
                            (2/3)*(((n)^2)-1)*((sinh(Delta_n(harmonic))-
sin(Delta_n(harmonic)))/(cosh(Delta_n(harmonic))+cos(Delta_n(harmonic)))));

             end
```

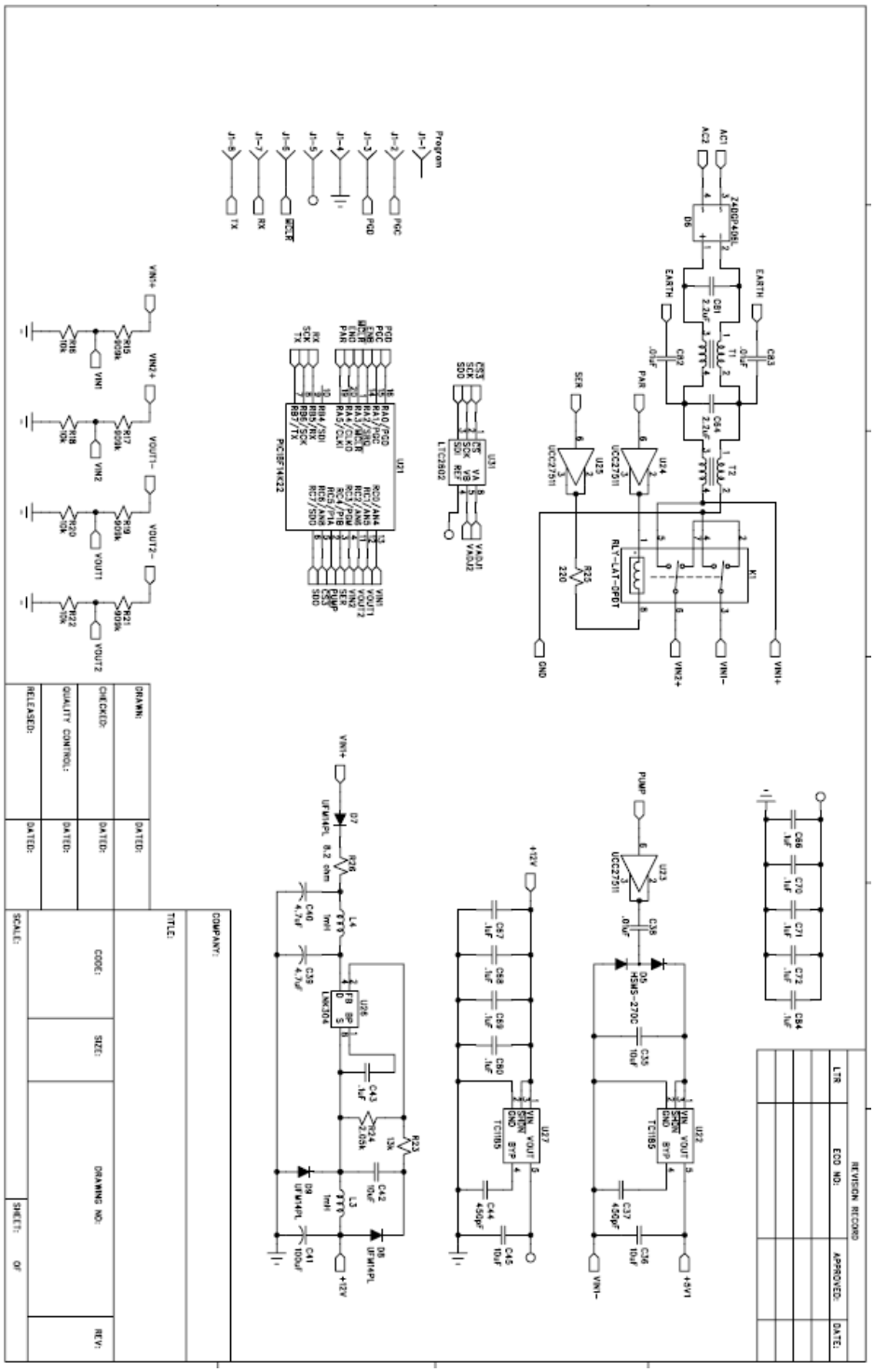
```
            %Calc Winding loss for different number of layers
             if number_of_layers == 1
                Pwind1(core, n)= Iavg^2*dc_resistance +
0.5*sum((I_n.^2).*Factors);
%              elseif number_of_layers == 2
%                  Pwind2(core, n)= Iavg^2*dc_resistance +
0.5*sum((I_n.^2).*Factors);
%              elseif number_of_layers == 3
%                  Pwind3(core, n)= Iavg^2*dc_resistance +
0.5*sum((I_n.^2).*Factors);
%              elseif number_of_layers == 4
%                  Pwind4(core, n)= Iavg^2*dc_resistance +
0.5*sum((I_n.^2).*Factors);
             end

        end

        %Calc Total Loss for different number of layers
        Ptot1(core, n)=Pwind1(core,n)+Pcore(core,n);
%
       [Ptot(core, n), No_layers(core,n)] = min([Ptot1(core, n)]);
        if No_layers(core,n) == 1
            Pwind(core,n)= Pwind1(core, n);
%
        end
        %Calc Total temperature rise
        deltaT(core, n) = (0.55*Ptot(core, n)*1E3/SA(core)).^0.833;
        if deltaT(core, n) > Tmax
           designok(core, n) =0;
           disp([corename{core,:},' @ ',num2str(n),' turns rejected: delta T
= ',...
                 num2str(deltaT(core, n)),' deg C']);
        end

        % Write out the data for the best design and plot Losses for all
        %designs that worked
        if designok(core, n) == 1
            %Display best designs stats
            disp('              ');
            disp([corename{core,:},' : Works!']);
            disp(['f = ',num2str(f), ' Hz']);
            disp(['L = ',num2str(L), ' H']);
            disp(['lg = ',num2str(lg(core, n)), ' m']);
            disp(['N = ',num2str(n)]);
            disp(['No of layers = ',num2str(No_layers(core, n))]);
            disp(['Bpk = ',num2str(Bpk(core,n))]);
            disp(['Pcore = ',num2str(Pcore(core,n)),' Watts']);
            disp(['Pwind = ',num2str(Pwind(core,n)),' Watts']);
            disp(['Ptot = ',num2str(Ptot(core,n)),' Watts']);
            disp(['delta T = ',num2str(deltaT(core, n)),' deg C']);
            disp('              ');

            corenamevalid{core,n} = corename{core,:};
            lgvalid(core,n) = lg(core, n);
            Bpkvalid(core,n) = Bpk(core,n);
            Pcorevalid(core,n) = Pcore(core,n);
```

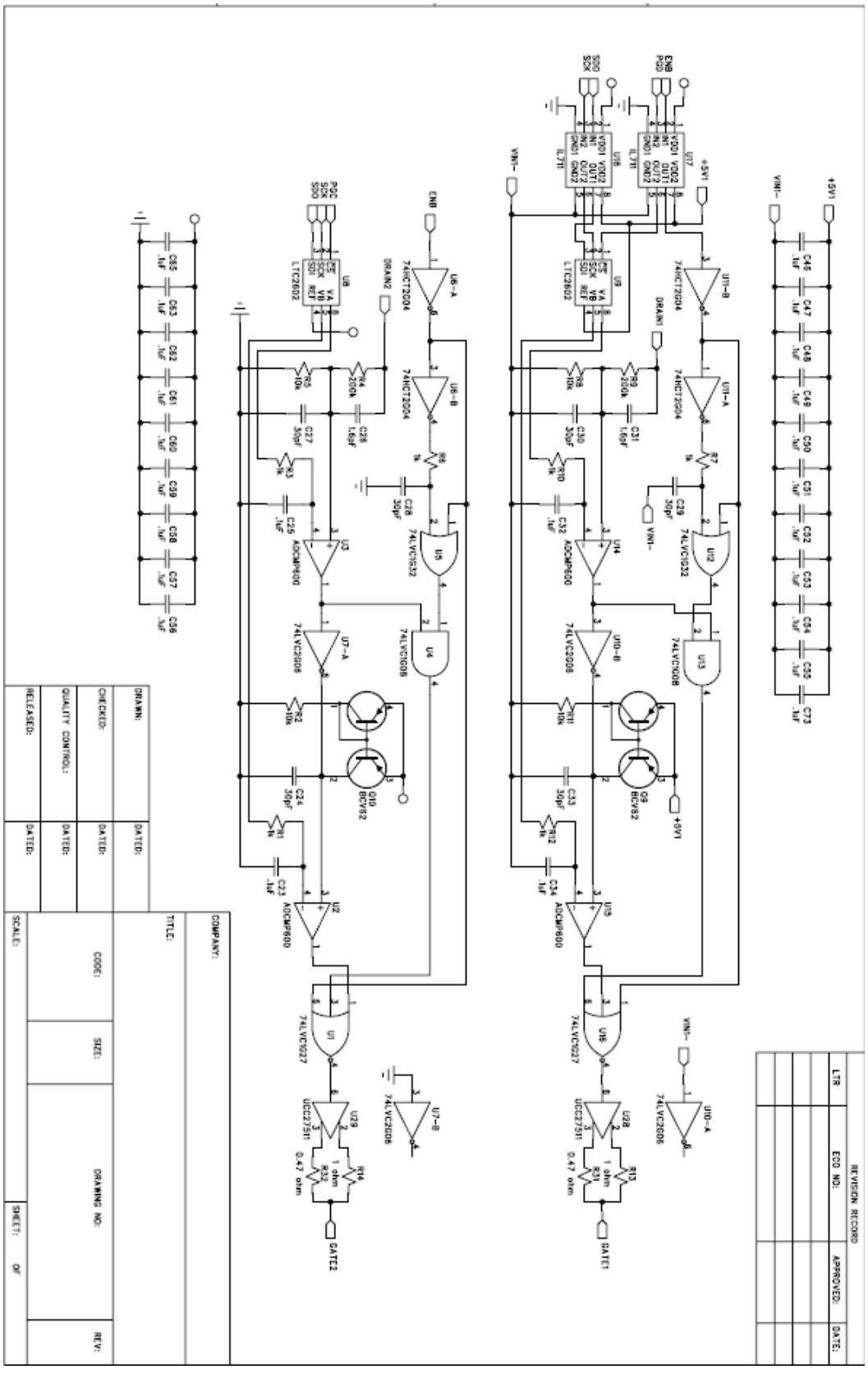
```
            Pwindvalid(core,n) = Pwind(core,n);
            Ptotvalid(core,n) = Ptot(core,n);
            deltaTvalid(core,n) = deltaT(core,n);
            Nvalid(core, n) = n;
        else
            corenamevalid{core,n} = [corename{core,:}, '(Failed)'];
            lgvalid(core,n) = NaN;
            Bpkvalid(core,n) = NaN;
            Pcorevalid(core,n) = NaN;
            Pwindvalid(core,n) = NaN;
            Ptotvalid(core,n) = NaN;
            deltaTvalid(core,n) = NaN;
            Nvalid(core, n) = NaN;

        end
    end


end

for core= 1:numcores
    [Best_Ptot(core), Best_N(core)] = min(Ptotvalid(core,:));
    Best_corename{core}= corenamevalid{core, Best_N(core)};
    Best_Pwind(core)= Pwindvalid(core, Best_N(core));
    Best_Pcore(core)= Pcorevalid(core, Best_N(core));
end
```

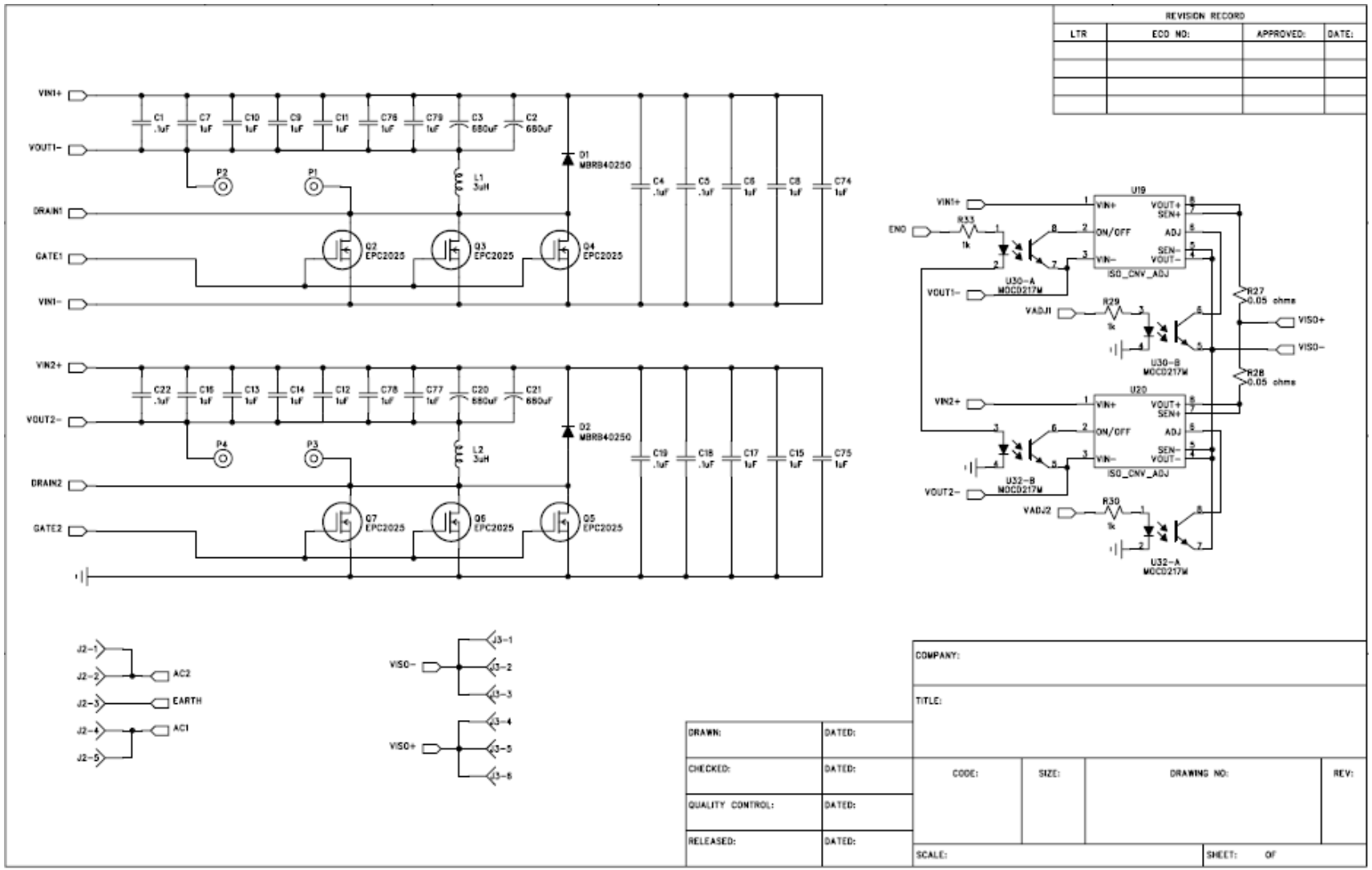
APPENDIX C

Full system with commercial converters

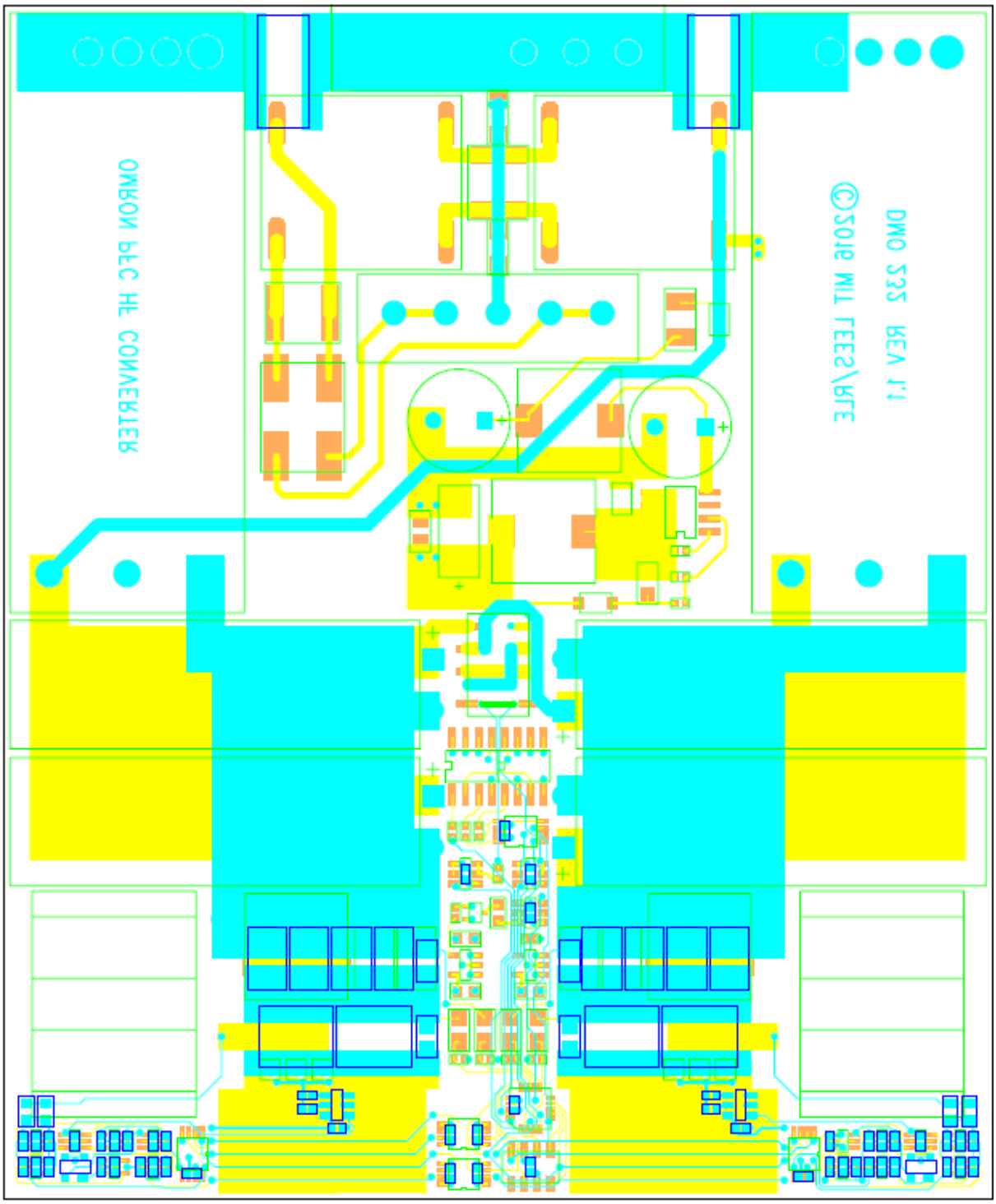
C.1 Schematics



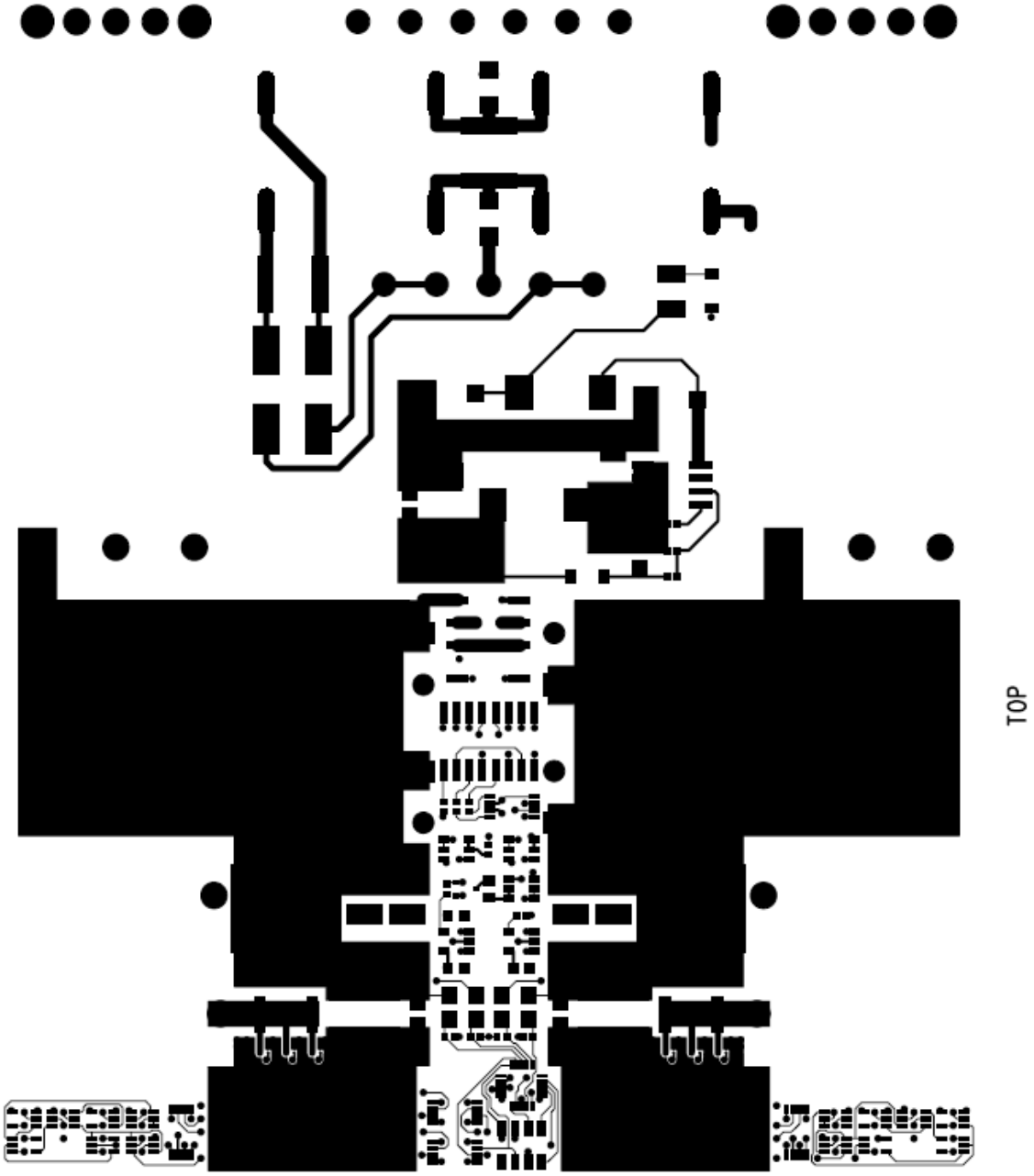



REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
VIN1+
VOUT1-
DRAIN1
GATE1
VIN1-
C1 .1uF
C7 1uF
C10 1uF
C9 1uF
C11 1uF
C76 1uF
C79 1uF
C3 680uF
C2 680uF
P2
P1
L1 3uH
D1 MBRB40250
C4 .1uF
C5 .1uF
C6 1uF
C8 1uF
C74 1uF
Q2 EPC2025
Q3 EPC2025
Q4 EPC2025
VIN2+
VOUT2-
DRAIN2
GATE2
C22 .1uF
C16 1uF
C13 1uF
C14 1uF
C12 1uF
C78 1uF
C77 1uF
C20 680uF
C21 680uF
P4
P3
L2 3uH
D2 MBRB40250
C19 .1uF
C18 .1uF
C17 1uF
C15 1uF
C75 1uF
Q7 EPC2025
Q6 EPC2025
Q5 EPC2025
J2-1
J2-2
J2-3
J2-4
J2-5
AC2
EARTH
AC1
VISO-
VISO+
J3-1
J3-2
J3-3
J3-4
J3-5
J3-6
U19
ISO_CNV_ADJ
U20
ISO_CNV_ADJ
ENO
R33 1k
VADJ1
R29 1k
VADJ2
R30 1k
R27 0.05 ohms
R28 0.05 ohms
U30-A MOCD217M
U30-B MOCD217M
U32-B MOCD217M
U32-A MOCD217M
COMPANY:
TITLE:
DRAWN:
DATED:
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
DATED:
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: OF

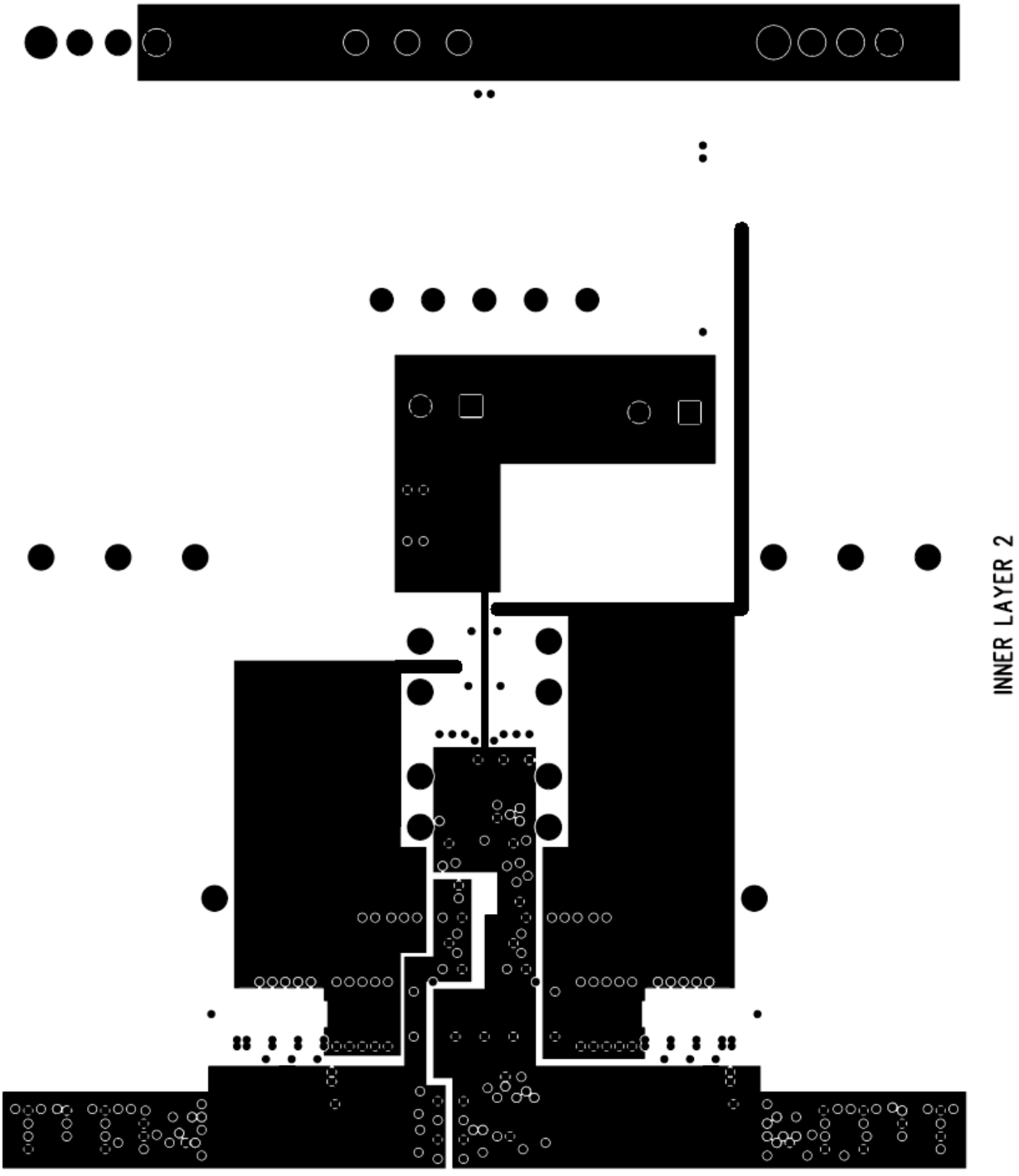
C.2 Layout



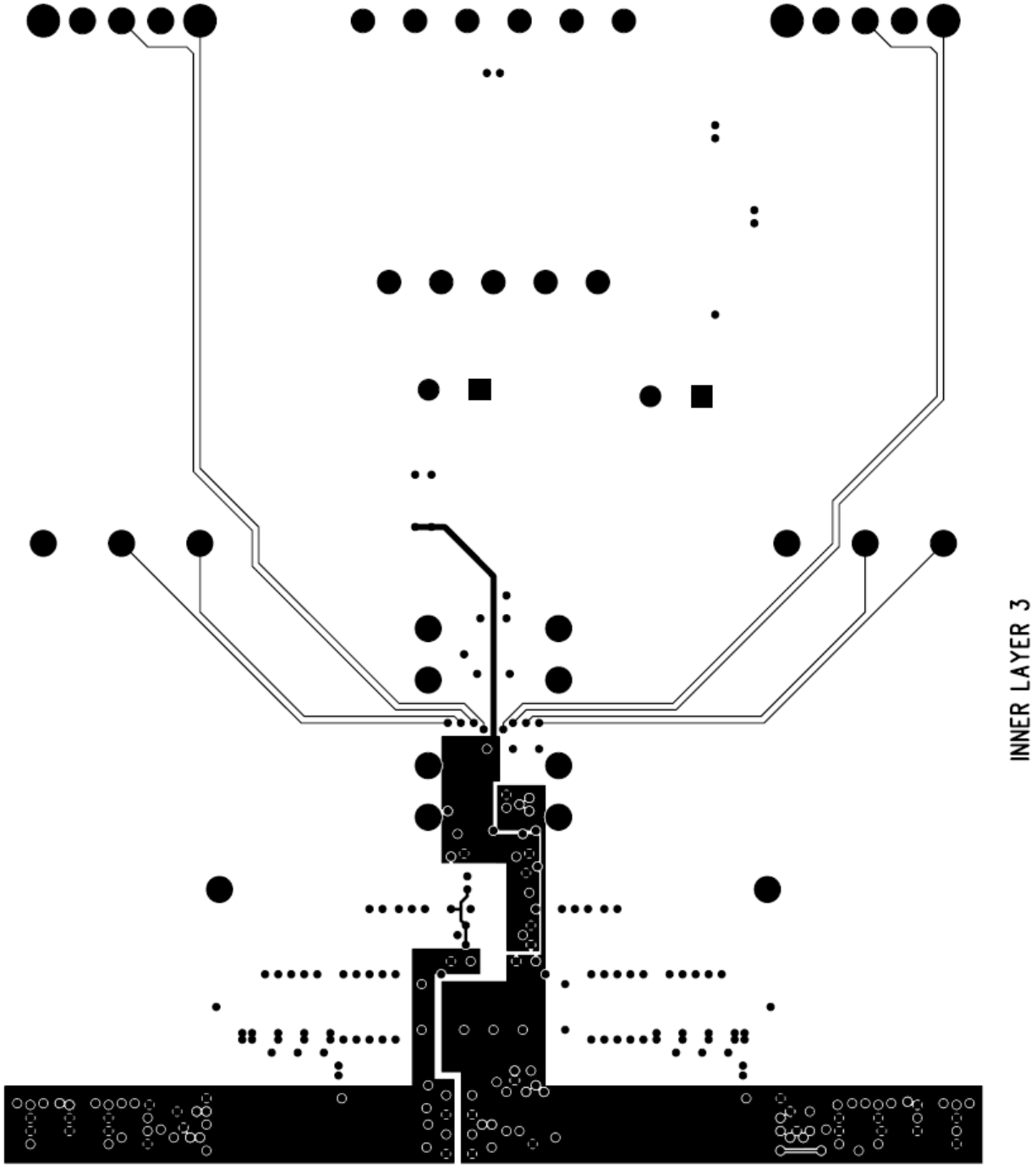
C.3 Top Layer



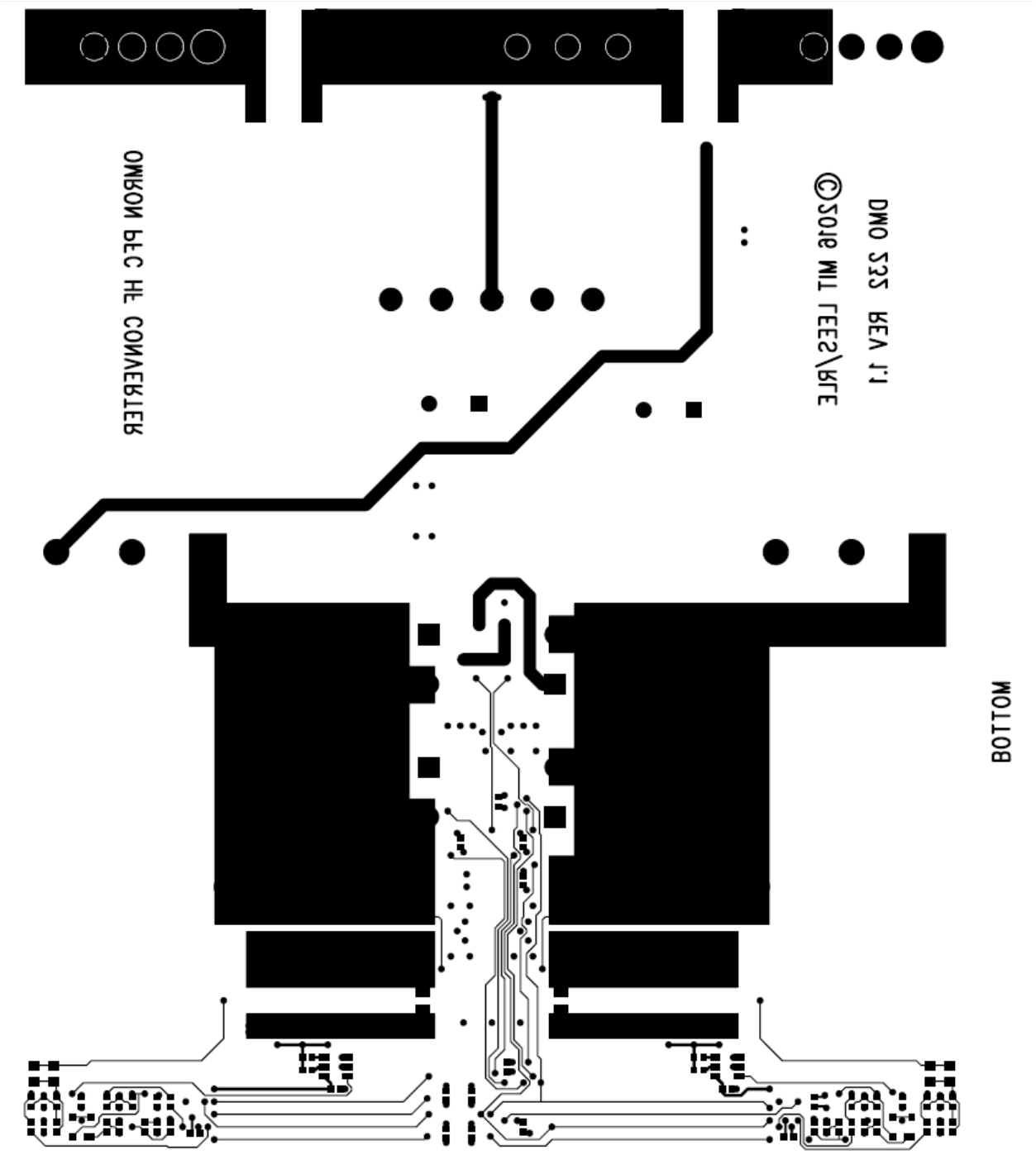
C.4 Inner Layer 2



C.5 Inner Layer 3



C.6 Bottom Layer



APPENDIX D

Transformer design Matlab script

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% The script calculates the Core loss, winding loss and temperature rise
% for all feasable planar inductor designs with DCM triangular current
waveforms
% Based on David Perreault's PhD optimization files
%
% Author: Ali S. AlShehab
% Review: Juan A. Santiago
% Date: July 2015
% Edited further by: Juan Santiago Sept 2016 (trasformer)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
clc
clear all
close all
format long e

%% To run this code:
% Make sure the core data file is in the same directory as this file. And,
% 1- Choose the core geometry and core type.
% 2- Specify the operating frequency, currents (Irms, Ipk, Iavg)
% 3- Specify the K, y and relative permiability values for the material
%    at frequency of interest
% Steps explained below:

% 1- Choose and load the core geometry and core type. (Comment/Uncomment)
%EQCoredat;             % EQ Cores have a circular center post
PlanarECoredat;      % PlanarE Cores have a rectangular center post
%EILPCoredat;         % EILP Cores have a rectangular center post

Coretype = 1;          % Coretype 1 has a rectangular center post
%Coretype = 2;        % Coretype 2 has a circular center

% 2- Specify the operating frequency, currents (Irms, Ipk, Iavg)
f = 1.0e6;               %Specify operating frequency (Hz)
f_str = '1 MHz';      %For plotting purpose
Ipk= 9.08;               %Specify peak current (A)
Irms= 5.1245;            %Choose current RMS (A)
Iavg= 4.246;             %Choose average current  (A)
Vpk=35;
IprimRMS=4;

rect=1; % enable for full bridge rectifier

%rect=2; % enable for half bridge rectifier

if rect==1
   IsecRMS=12; % secondary RMS currrent in A for full bridge rectifier
   t_ratio=3/2; % primary to secondary turns ratio for full bridge rectifier
elseif rect==2
   IsecRMS=24; % secondary RMS currrent in A for half bridge rectifier
   t_ratio=3/1; % primary to secondary turns ratio for half bridge rectifier
```

```
end


% 3- Specify the K, y and relative permiability values for the material at
frequency of interest:

%% 500 kHz coeficients
K1 = 0.02271; y1 = 2.32193;  % Coefficients of power for 3F3 @ 0.5 MHz

K2 = 0.00084; y2 = 2.95936;  % Coefficients of power for 3F35 @ 0.5 MHz

K3 = 0.000314; y3 = 3.189;  % Coefficients of power for N49 @ 0.5 MHz

K4 = 0.0000876; y4 = 3.4512111; % Core loss coefficients for DMR51 @ 500 kHz

K5=0.01135; y5=2.32193; % Core loss coefficients for 3F5 @ 500 kHz


%% 300 kHz coefficients

K6=0.0000607; y6=3.2479275; % Core loss coefficients for 3F35 @ 300 kHz

K7=0.0001638; y7=2.9808912; % Core loss coefficients for 3F5 @ 300 kHz

K12=0.001487; y12=2.63743; % Core loss coefficients for 3C96 @ 300 kHz


%% 1 MHz

K8=0.0089706; y8=2.662965; % Core loss coefficients for 3F45 @ 1 MHz

K9=0.0004508; y9=3.3808218; % Core loss coefficients for DMR51 @ 1 MHz

K14=0.0000980; y14=3.7138309; %% Core loss coefficients for PC200 (N59) @ 1
MHz



%% 750 kHz

K10=0.0057858; y10=2.6818741;   % Coefficients of power for N49 @ 0.75 MHz

%% 1.25 MHz

K11=0.0430719; y11=2.4214638; % Core loss coefficients for 3F45 @ 1.25 MHz

%% 2 MHz

K13=0.1248839; y13=2.3219281; % Core loss coefficients for 3F5 @ 2.0 MHz
```

```
K = K9; % Choose K value
y = y9; % Choose y value

ur_3F45=900;

ur_DMR51=1100;

ur_N49=1500;

ur_3F5=650;

ur_PC200=800;

ur = ur_DMR51; % Choose relative permiability of core material: ur_3F4,
ur_F67, ur_3F45, ur_4F1, etc.

% 4- Other parameters and specifications:

I_n =[1]; % Fourier Coefficients of waveform

% Applies for DCM triangular current waveform
Bmax = 0.3;                                    % Maximum flux density in T to
prevent saturation
Tmax = 100;                                     % Maximum temperature rise in
deg Celcius
L = 3e-6;                                      % Inductance in H
mu=4*pi*10^-7;                                 % Permeability of free space
(H/m)
p = 2.5e-8;                                    % Resistivity of copper (Ohm-m)
@ 125 deg C
N = 6;                                        % Max number of turns in an
inductor



% awg=0.08e-3;                                   %40 awg, diameter of a single
strand in m
% nst=100;                                       %number of strands in primary
% nsts=100;                                      %number of strands in
secondary
% numw=1;                                        %number of litz wires used in
parallel

% awg=0.0635e-3;                                   %42 awg, diameter of a
single strand in m
% nst=144;                                       %number of strands in primary
% nsts=432;                                      %number of strands in
secondary
 numw=1;

% Lits of Litz wires to test
%                    40       42        44        46        48        50
52
```

```
litz_dia= 1e-3*[ 0.07874 , 0.06350 , 0.05080 , 0.03983 , 0.03160 , 0.02505 ,
0.01987]; % diameter in m of a single strand of 40, 42, 44, 46, 48, 50 and 52
AWG
litz_strands= linspace(10,1000,50); % number of trands on a litz wire bundle


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% End User Input
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

No_of_layers = 1;                               % Max number of layers
d = sqrt(2./(4*pi*10^-7*2*pi.*f*10^8/2.5));  % Skin depth in m
modeltype=1; % 1-D field approx for Fr (Dowell's model)

w_model=1; %for using Sullivan's equations for winding losses
%w_model=2; %for using Dowell's equations for winding losses

%% save core data
lg = zeros(numcores,N); %Gap length
ue = zeros(numcores,N); %Effective permiability
Bpk = zeros(numcores,N); %Peak magnetic field
Pcore = zeros(numcores,N); %Core loss
Ptot = zeros(numcores, N); %Lowest total loss
Ptot1 = zeros(numcores, N); %Total Losses using 1 layer
Ptot2 = zeros(numcores, N); %Total Losses using 2 layers
Ptot3 = zeros(numcores, N); %Total Losses using 3 layers
Ptot4 = zeros(numcores, N); %Total Losses using 3 layers
Pwind = zeros(numcores, N); %Lowest Winding Loss
Pwind1 = zeros(numcores, N); %Winding Losses using 1 layer
Pwind2 = zeros(numcores, N); %Winding Losses using 2 layers
Pwind3 = zeros(numcores, N); %Winding Losses using 3 layers
Pwind4 = zeros(numcores, N); %Winding Losses using 4 layers

Pwind_temp=0;
wire_awg_prim=0;
strand_prim=0;
strand_sec=0;
Lmag=0; %magnetizing inductance
Imagpk=0; %peak magnetizing current
ImagRMS=0;

No_layers = zeros(numcores,N); %Number of layers
deltaT = zeros(numcores,N); %Temperature rise
designok = zeros(numcores,N); %Design check

%% Loop through available cores and synthesize inductor designs

%Calc Delta(harmonic)
% for harmonic = 1:length(I_n)
%     Delta_n(harmonic) =awg*sqrt(harmonic*2*pi*f*pi*4e-7*(1/p)/2);
% end
```

```
%Loop over all cores
for core =1:numcores

    %Calculate surface area for each core
    if Coretype == 1;
        SA(core)= 10000*(2*(h_core(core)*w_core(core)+
l_core(core)*w_core(core)+l_core(core)*h_core(core)- h(core)*(OD(core)-
ID(core)))+4*h(core)*w_core(core)+ 2*(OD(core)-ID(core))*w_core(core));
    elseif Coretype ==2;
        SA(core)= 10000*(2*(h_core(core)*w_core(core)+
l_core(core)*w_core(core)+l_core(core)*h_core(core)-
h(core)*OD(core))+2*pi*h(core)*(ID(core)/2)+ 2*(OD(core)*w_core(core)-
pi*(ID(core)/2)^2));
    end

    %Loop over different number of turns
    for n= 1:N

        np=n; % primary turns

        ns=np/t_ratio;% secondary side turns

        designok(core, n) = 1; % assume this core design works

        Pwind_temp=0;
        wire_awg_prim=0;
        wire_awg_sec=0;
        strand_prim=0;
        strand_sec=0;
        copper_area_prim=0;
        copper_area_sec=0;
        Lmag=0; %magnetizing inductance
        Imagpk=0; %peak magnetizing current
        ImagRMS=0;


        % Calc the peak magnetic field Bpk in Tesla
        %Bpk(core,n) = ue(core,n)*mu*n*Ipk/le(core);
        Bpk(core,n)=Vpk/(2*f*n*Ae(core));

        if Bpk(core,n) > Bmax
            designok(core, n) = 0;     % design is not ok
            disp([corename{core,:},' @ ',num2str(n),' turns rejected: Bpk =
',num2str(Bpk(core,n)),...
                ' gauss']);
        end


        %Calc Core Loss
        Pcore(core, n)=(Vc(core)*K*(Bpk(core,n)*1000)^y)/1000;

        %Initialize Factors = Rac(n)/Rdc
        Factors = zeros(length(I_n), 1);
```

```
        num_wire=length(litz_dia);

        %Calc turns per layer, dc resistance, and Winding Loss
        for number_of_layers=1:num_wire

            awgp=litz_dia(number_of_layers);


           for num_wire_sec=1:num_wire

               awgs=litz_dia(num_wire_sec);

            for num_strands=1:length(litz_strands)

                nst=litz_strands(num_strands);

              for num_strands_sec=1:length(litz_strands)

                  nsts=litz_strands(num_strands_sec);

                  turn_layer = zeros(1,No_of_layers); % This array will
contain the number of turns in each layer
                  layer_dc_resistance = zeros(1,No_of_layers); % Array to
store the dc resistance for each layer

                  winding_area_core=(OD(core)-ID(core))/2*h(core); %core
window area (area available for winding) in m2

                  winding_area_prim=2*n*nst*(pi)*(awgp/2)^2;  % winding area
taken by a single primary winding in m2
                  winding_area_sec=2*ns*nsts*(pi)*(awgs/2)^2; % winding area
taken by the secondary winding in m2

                  tot_winding_area= 2*winding_area_prim+winding_area_sec;


               if winding_area_core-tot_winding_area>0

                if Coretype == 1;
                  dc_resistance_prim=
p*2*(W(core)+ID(core))*np*4/awgp^2/nst/pi/numw; %litz wire dc resistance
rectangular post primary
                  dc_resistance_sec=
p*2*(W(core)+ID(core))*ns*4/awgs^2/nsts/pi/numw; %litz wire dc resistance
rectangular post secondary
                elseif Coretype == 2;
                  dc_resistance_prim= p*ID(core)*np*4/awgp^2/nst/numw; %litz
wire resistance circular post
                  dc_resistance_sec= p*ID(core)*ns*4/awgs^2/nsts/numw; %litz
wire dc resistance circular post secondary
                end
```

```
                if w_model == 1; %Fr= Rdc*Rac(n)/Rdc, uses Sullivan's model
from 1999 Trans on PE, "Optimal Choice..."


                    fr_prim=1+power(((pi*2*pi*f*4*pi*1e-
7*np.*nst.*awgp^3.*1)./(p*h(core))),2)./768;

                    fr_sec=1+power(((pi*2*pi*f*4*pi*1e-
7*ns.*nsts.*awgs^3.*1)./(p*h(core))),2)./768;

                elseif w_model == 2; %Fr= Rdc*Rac(n)/Rdc,uses Dowell's
equation model

                 harmonic = 1;


fr_prim=Delta_n(harmonic)*(((sinh(2*Delta_n(harmonic))+sin(2*Delta_n(harmonic
)))/(cosh(2*Delta_n(harmonic))-cos(2*Delta_n(harmonic))))+ ...
                            (2/3)*(((np)^2)-1)*((sinh(Delta_n(harmonic))-
sin(Delta_n(harmonic)))/(cosh(Delta_n(harmonic))+cos(Delta_n(harmonic)))));



fr_sec=Delta_n(harmonic)*(((sinh(2*Delta_n(harmonic))+sin(2*Delta_n(harmonic)
))/(cosh(2*Delta_n(harmonic))-cos(2*Delta_n(harmonic))))+ ...
                            (2/3)*(((ns)^2)-1)*((sinh(Delta_n(harmonic))-
sin(Delta_n(harmonic)))/(cosh(Delta_n(harmonic))+cos(Delta_n(harmonic)))));


                end

            %Calc Winding loss for different number of layers


                 %Pwind1(core, n)= Iavg^2*dc_resistance +
0.5*sum((I_n.^2).*Factors);

                Lmag(end+1)=mu*ur*Ae(core)/(2*le(core))*np*np; %magnetizing
inductance referred to primary
                Imagpk(end+1)=Vpk/Lmag(end)*0.5/f/2; %peak magnetizing
current
                ImagRMS(end+1)=8/(pi*pi*sqrt(2))*Imagpk(end); %RMS on
fundamental magnmetizing current

Pwind_temp(end+1)=IprimRMS^2.*dc_resistance_prim.*fr_prim.*2+IsecRMS^2.*dc_re
sistance_sec.*fr_sec;
                wire_awg_prim(end+1)=awgp ;
                wire_awg_sec(end+1)=awgs;
                strand_prim(end+1)= nst;
                strand_sec(end+1)= nsts;
                copper_area_prim(end+1)=2*n*nst*(pi)*(awgp/2)^2/2;
                copper_area_sec(end+1)=2*ns*nsts*(pi)*(awgs/2)^2/2;
```

```
%Pwind1(core,n)=IprimRMS^2.*dc_resistance_prim.*fr_prim.*2+IsecRMS^2.*dc_resi
stance_sec.*fr_sec;
%               %

               else
                  Lmag(end+1)=mu*ur*Ae(core)/(2*le(core))*np*np; %magnetizing
inductance
                  Imagpk(end+1)=Vpk/Lmag(end)*0.5/f/2; %peak magnetizing
current
                  ImagRMS(end+1)=8/(pi*pi*sqrt(2))*Imagpk(end); %RMS on
fundamental magnmetizing current
                  Pwind_temp(end+1)=1e3;
                  wire_awg_prim(end+1)=awgp ;
                  wire_awg_sec(end+1)=awgs;
                  strand_prim(end+1)= nst;
                  strand_sec(end+1)= nsts;
                  copper_area_prim(end+1)=2*n*nst*(pi)*(awgp/2)^2/2;
                  copper_area_sec(end+1)=2*ns*nsts*(pi)*(awgs/2)^2/2;




               end
              end
             end
            end
         end

         [Pwind1(core,n),index(core,n)]=min(Pwind_temp(2:end));
         best_wire_awg_prim(core,n)=wire_awg_prim(index(core,n)+1);
         best_wire_awg_sec(core,n)=wire_awg_sec(index(core,n)+1);
         best_strand_prim(core,n)=strand_prim(index(core,n)+1);
         best_strand_sec(core,n)=strand_sec(index(core,n)+1);
         best_copper_prim(core,n)=copper_area_prim(index(core,n)+1);
         best_copper_sec(core,n)=copper_area_sec(index(core,n)+1);
         best_Lmag(core,n)= Lmag(index(core,n)+1);       %magnetizing
inductance
         best_Imagpk(core,n)= Imagpk(index(core,n)+1);
         best_ImagRMS(core,n)= ImagRMS(index(core,n)+1);


         %Calc Total Loss for different number of layers
         Ptot1(core, n)=Pwind1(core,n)+Pcore(core,n);
%
        [Ptot(core, n), No_layers(core,n)] = min([Ptot1(core, n)]);
         if No_layers(core,n) == 1
             Pwind(core,n)= Pwind1(core, n);
%
         end
         %Calc Total temperature rise
         deltaT(core, n) = (0.55*Ptot(core, n)*1E3/SA(core)).^0.833;
         if deltaT(core, n) > Tmax
            designok(core, n) =0;
            disp([corename{core,:},' @ ',num2str(n),' turns rejected: delta T
= ',...
```

```
                num2str(deltaT(core, n)),' deg C']);
        end

        % Write out the data for the best design and plot Losses for all
        %designs that worked
        if designok(core, n) == 1
            %Display best designs stats
            disp('              ');
            disp([corename{core,:},' : Works!']);
            disp(['f = ',num2str(f), ' Hz']);
            disp(['L = ',num2str(L), ' H']);
            disp(['lg = ',num2str(lg(core, n)), ' m']);
            disp(['N = ',num2str(n)]);
            disp(['No of layers = ',num2str(No_layers(core, n))]);
            disp(['Bpk = ',num2str(Bpk(core,n))]);
            disp(['Pcore = ',num2str(Pcore(core,n)),' Watts']);
            disp(['Pwind = ',num2str(Pwind(core,n)),' Watts']);
            disp(['Ptot = ',num2str(Ptot(core,n)),' Watts']);
            disp(['delta T = ',num2str(deltaT(core, n)),' deg C']);
            disp(['Optimal wire diameter primary=
',num2str(best_wire_awg_prim(core, n)),' m']);
            disp(['Optimal wire diameter secondary=
',num2str(best_wire_awg_sec(core, n)),' m']);
            disp(['Optimal Strands Primary = ',num2str(best_strand_prim(core,
n)),' ']);
            disp(['Optimal Strands Secondary =
',num2str(best_strand_sec(core, n)),' ']);
            disp(['Primary copper area single winding=
',num2str(best_copper_prim(core,n)),' m2 ']);
            disp(['Secondary copper area single winding=
',num2str(best_copper_sec(core,n)),' m2 ']);
            %disp(['delta T = ',num2str(deltaT(core, n)),' deg C']);
            disp(['Magnetizing inductance referred to primary=
',num2str(best_Lmag(core,n)),' H ']);
            disp(['Peak magnetizing current= ',num2str(
best_Imagpk(core,n)),' A ']);
            disp(['RMS magnetizing current= ',num2str(best_ImagRMS(core,n)),'
A RMS ']);
            disp('              ');

            corenamevalid{core,n} = corename{core,:};
            lgvalid(core,n) = lg(core, n);
            Bpkvalid(core,n) = Bpk(core,n);
            Pcorevalid(core,n) = Pcore(core,n);
            Pwindvalid(core,n) = Pwind(core,n);
            Ptotvalid(core,n) = Ptot(core,n);
            deltaTvalid(core,n) = deltaT(core,n);
            Nvalid(core, n) = n;
        else
            corenamevalid{core,n} = [corename{core,:}, '(Failed)'];
            lgvalid(core,n) = NaN;
            Bpkvalid(core,n) = NaN;
            Pcorevalid(core,n) = NaN;
            Pwindvalid(core,n) = NaN;
            Ptotvalid(core,n) = NaN;
            deltaTvalid(core,n) = NaN;
            Nvalid(core, n) = NaN;
```

```
        end
    end


end

for core= 1:numcores
    [Best_Ptot(core), Best_N(core)] = min(Ptotvalid(core,:));
    Best_corename{core}= corenamevalid{core, Best_N(core)};
    Best_Pwind(core)= Pwindvalid(core, Best_N(core));
    Best_Pcore(core)= Pcorevalid(core, Best_N(core));
end

Best_corename{core}
    Best_N(core)
    Best_Pwind(core)
    Best_Pcore(core)
    min(Ptotvalid(core,:))
```

APPENDIX E

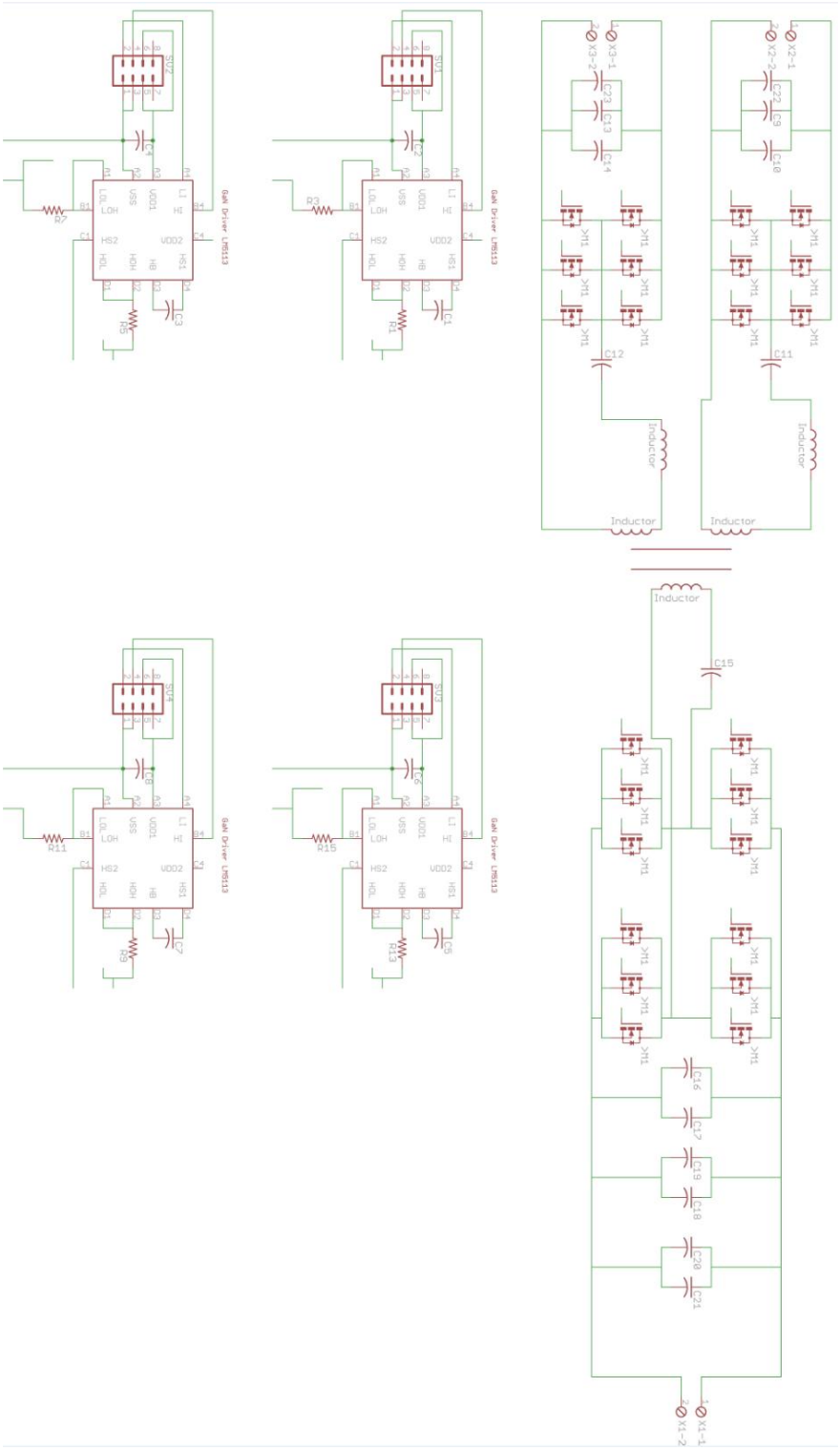
Core loss parameters for transformer design

Core material	Switching frequency (Hz)	K	Y
3C96	300k	1.487e-3	2.637
N49	500k	3.14e-4	3.189
3F45	1M	8.97e-3	2.663
DMR51	1M	4.508e-4	3.38

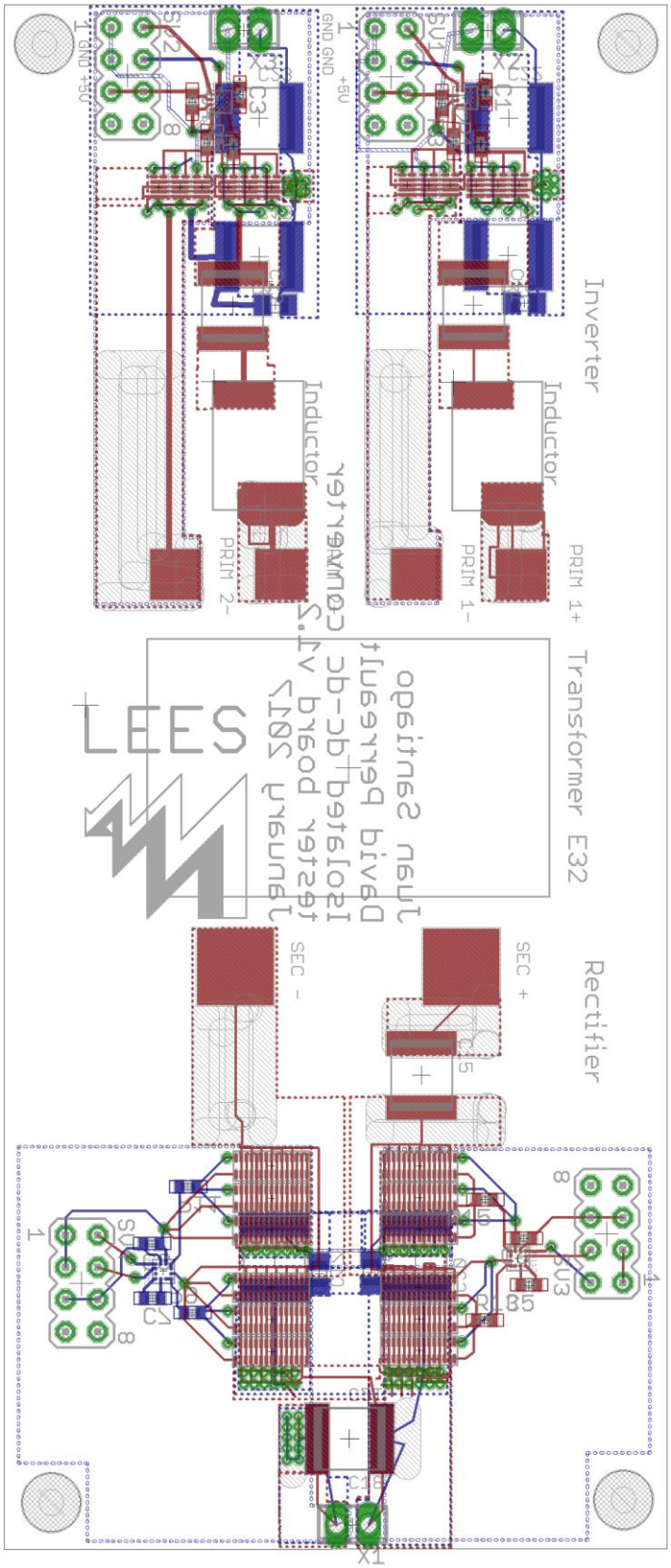
APPENDIX F

Second Stage DAB Tester board

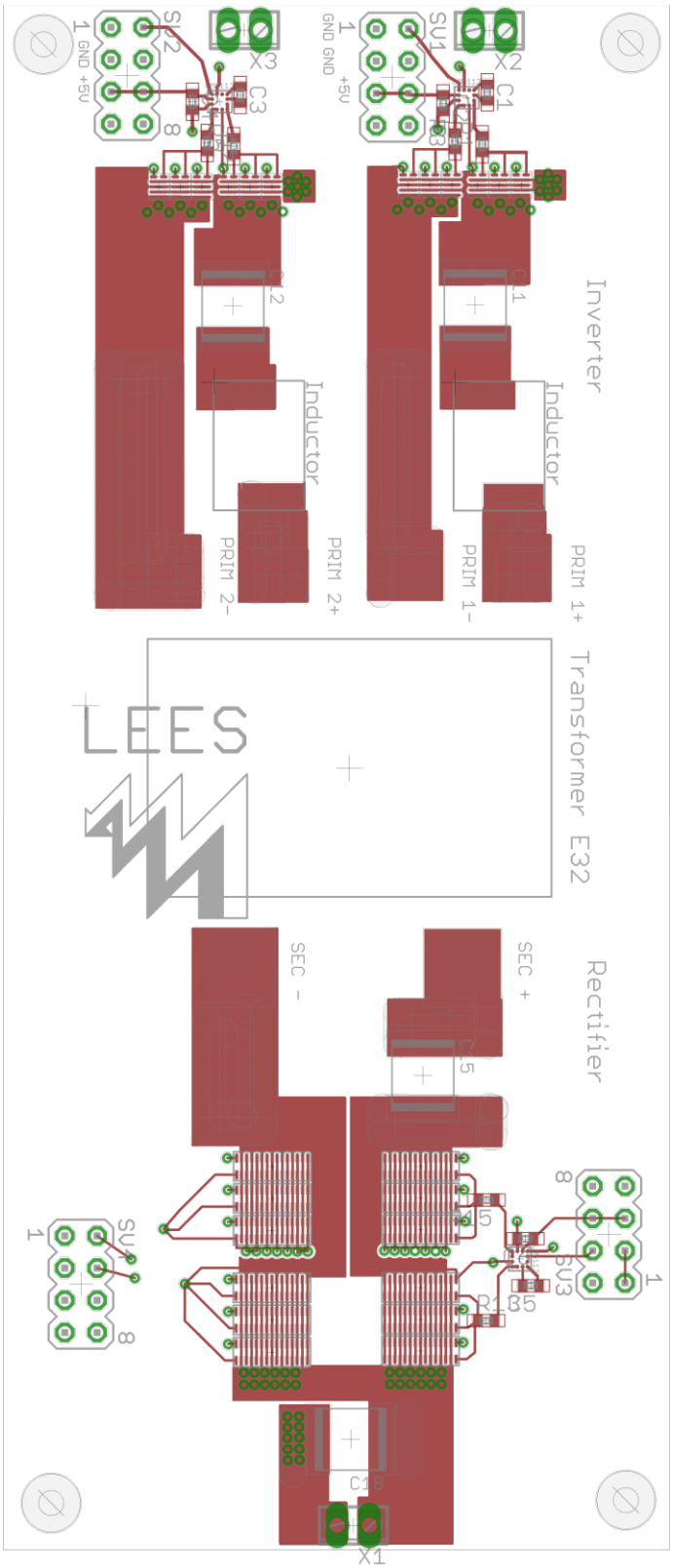
F.1 DAB tester schematic



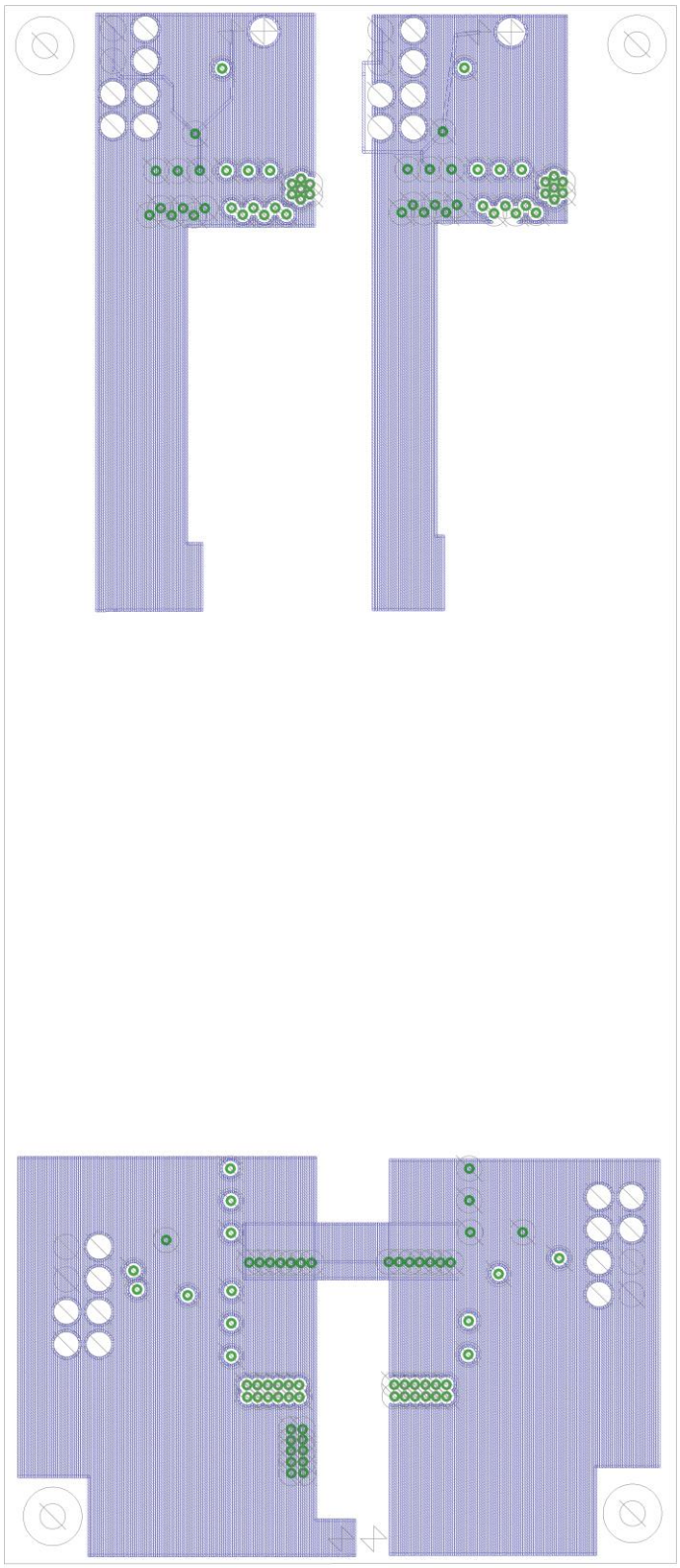
F.2 DAB tester Layout



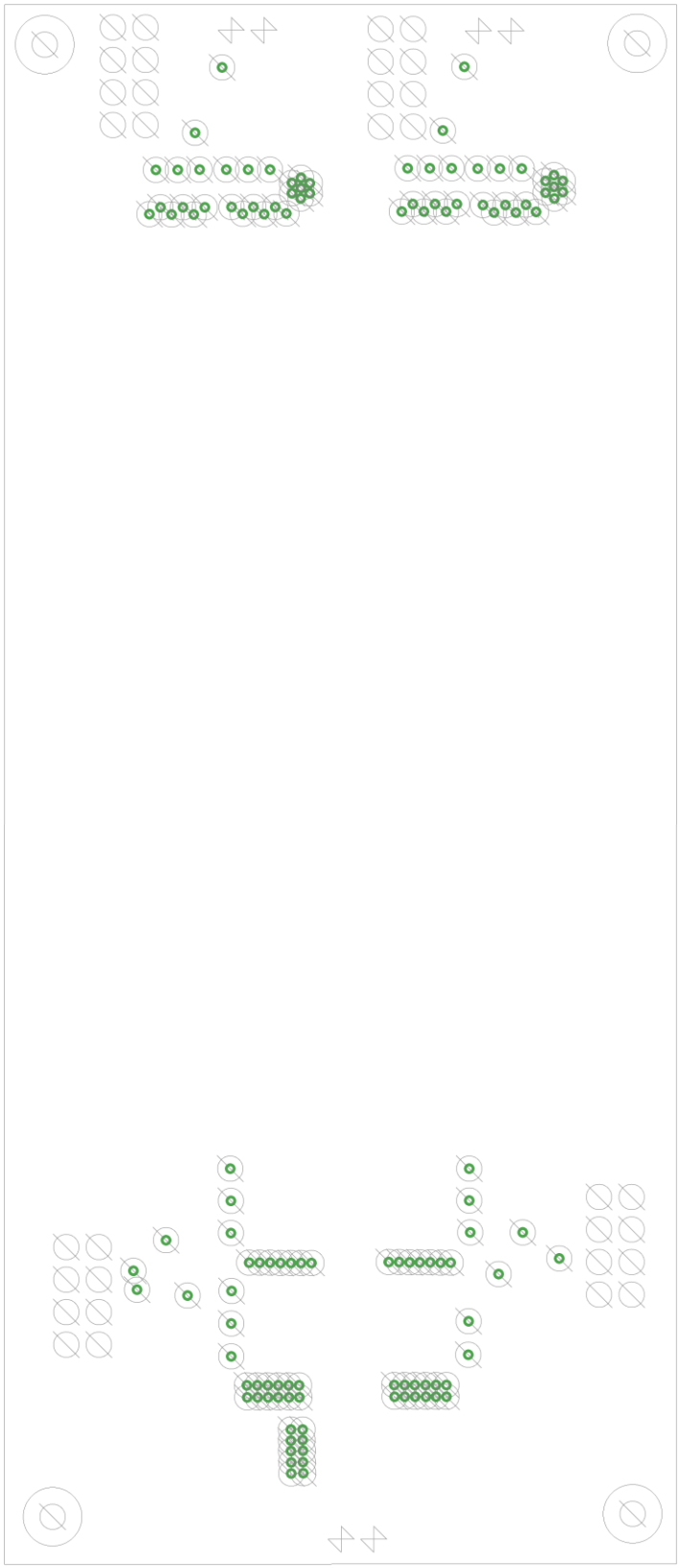
F.3 Top Layer


SV2
X3
C3
SV1
X2
C1
Inverter
Inductor
PRIM 2-
PRIM 2+
PRIM 1-
PRIM 1+
LEES
Transformer E32
SEC -
SEC +
Rectifier
SV4
SV3
X1

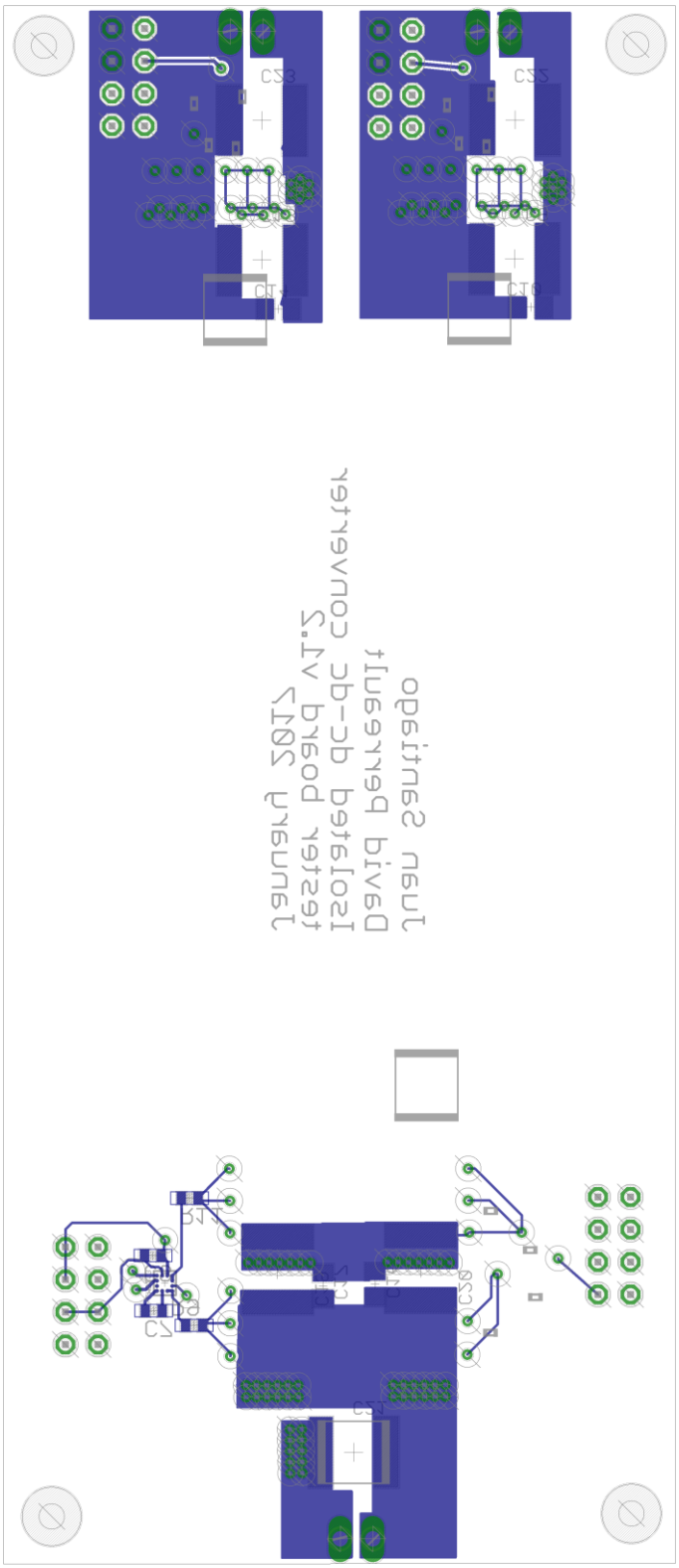
F.4 Inner layer 2



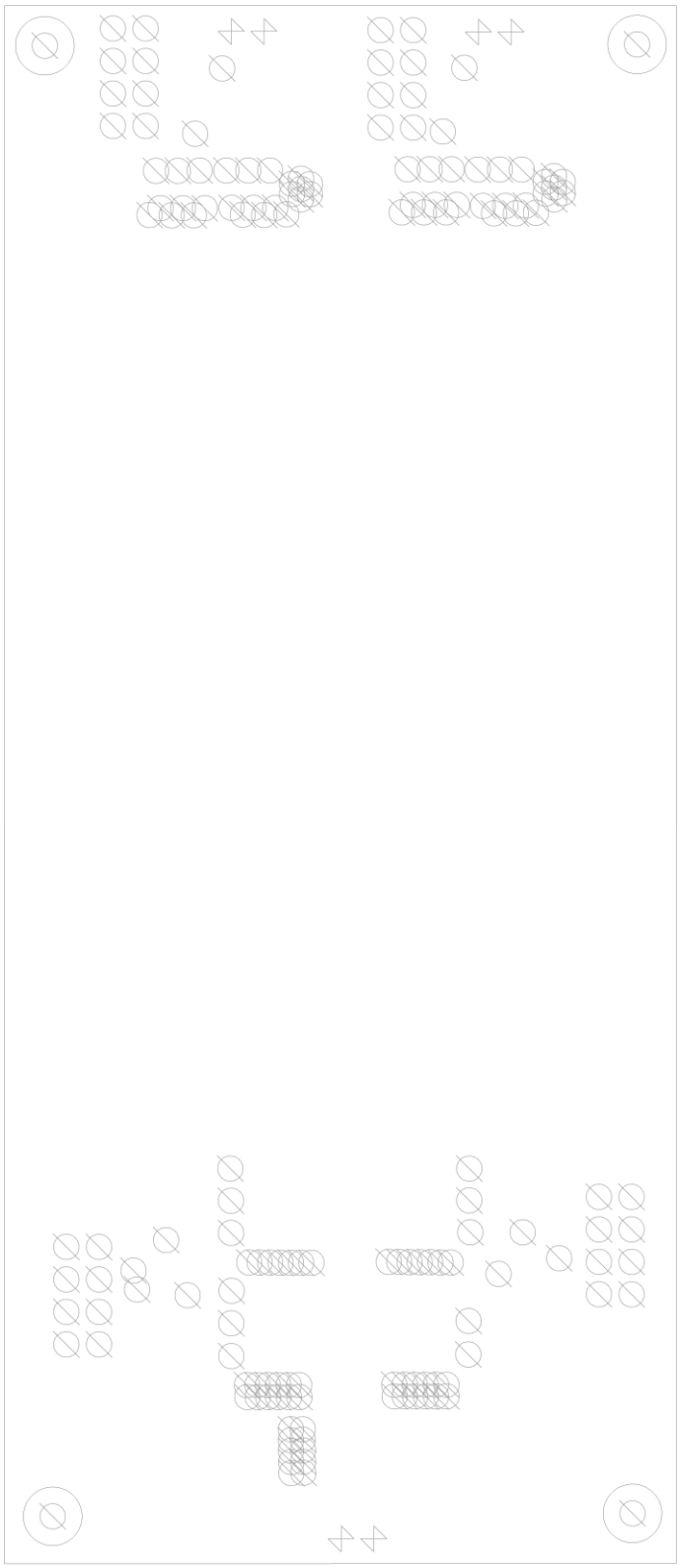
F.5 Inner layer 3



F.6 Bottom layer



F.7 Drill



APPENDIX G

Matlab script for output power vs dead time model

```
%% numerically calculate output power vs dead time

%% plotting Vleak
close all
clear all
format long e

fs=520e3; %frequency in hertz
dead_time=100e-9; %dead time in sec
phi=30e-9; %phase shift in sec

Vin=72; % converter input voltage in volts
Vo=24;  % converter output voltage in volts
n=2/3;  % tranformer turns ratio 1:n
Ci=3735e-12; %inverter switch capacitance referred to secondary
Ci=Cio*2/(n^2) in farads
Co=4100e-12; % rect switch cap referred to secondary in farads
Lmag=8020.7e-9; % magnetizing inductance referred to the seconday in henries
Lleak=82.07e-9; % leakage inductance referred to the seconday in henries
Vci=48; % iverter cap initial voltage referred to the secondary in volts
Vco=24; % rectifier cap initial voltage referred to the secondary in volts


dt=dead_time;
ton=1/(2*fs)-dt;
w_leak=1/sqrt(Lleak*Ci*Co/(Ci+Co));
w_mag=1/sqrt(Lmag*(Ci+Co));
w_ph=1/sqrt(Ci*Lleak*Lmag/(Lmag+Lleak));
w_ph_Co=1/sqrt(Lleak*Co);
Vdc_caps=(Co/(Ci+Co))*(Vci-Vin*n/2-Vco);

t_ton=0:0.1e-9:ton;
t_ph=0:0.1e-9:phi;
t_dt=0:0.1e-9:dead_time-phi;

t1=0:0.1e-9:ton-phi;
t2=0:0.1e-9:phi;
t3=0:0.1e-9:dt-phi;
t4=0:0.1e-9:phi;

%syms('IL','IM')
syms('IL')


%IL=Ileak;
%IM=Imag;
IM=Vin/2*n/Lmag*ton*0.5;


% First phase shift
```

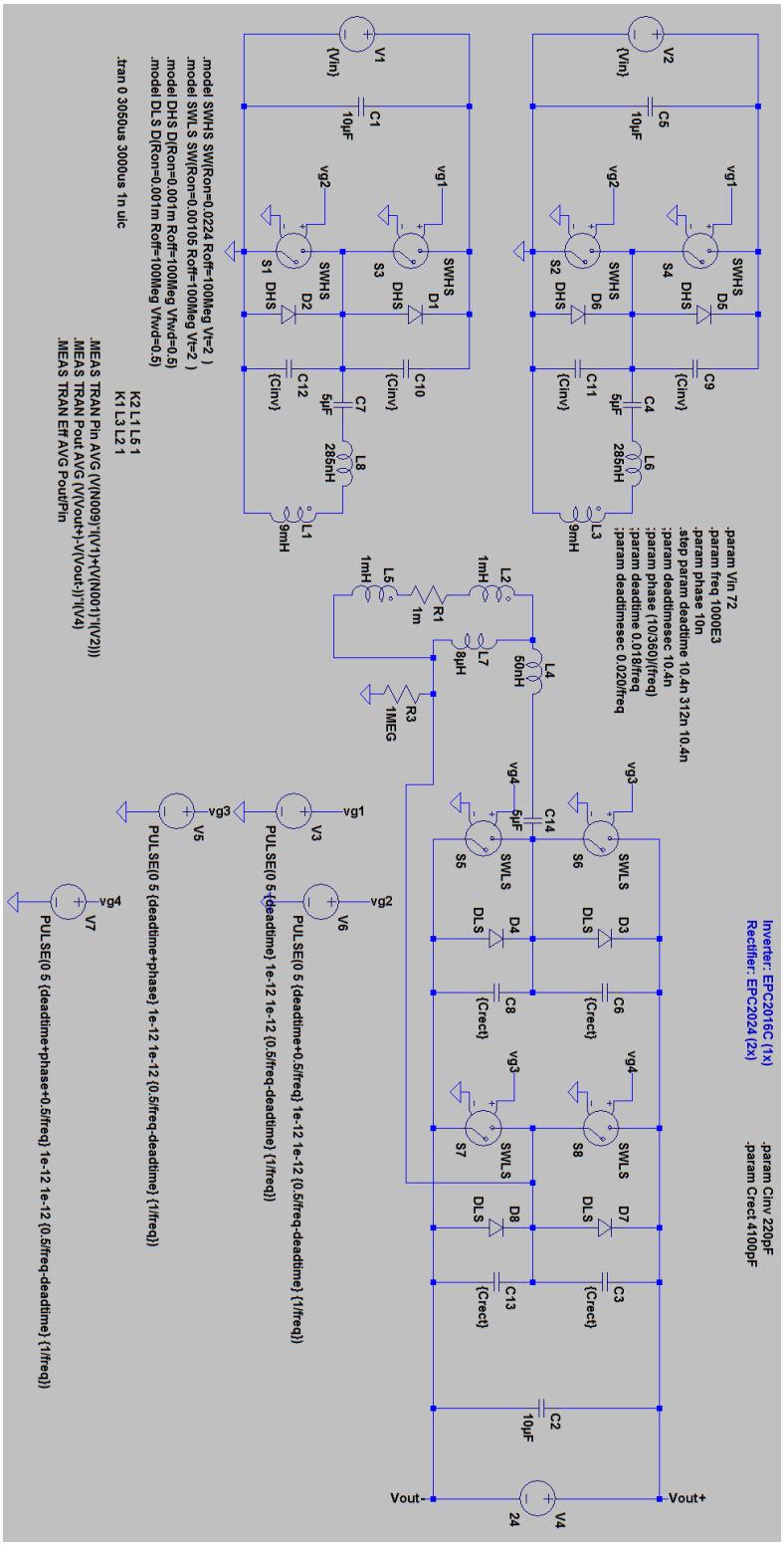
```
Ileak_t_ph=-
Vo*t_ph/Lleak+IL+(Vo*(Lmag/(Lmag+Lleak)))/Lleak*t_ph+(Lmag/(Lleak+Lmag))*(IL+
IM)*(-1+cos(t_ph*w_ph))+1/(w_ph*Lleak)*(Vci-Vin*n/2-
Vo*Lmag/(Lmag+Lleak))*sin(t_ph*w_ph); %verified correct

Vci_t_ph=Vin*n*3/2-Vci+Vo*(Lmag/(Lmag+Lleak))+(Vci-Vin*n/2-
Vo*(Lmag/(Lmag+Lleak)))*cos(t_ph*w_ph)+-
(Lmag*Lleak/(Lmag+Lleak))*(IL+IM)*w_ph*sin(t_ph*w_ph); %verified correct

Imag_t_ph=IM+(Vo*(1/(Lmag+Lleak)))*t_ph+-
(Lleak/(Lleak+Lmag))*(IL+IM)+(Lleak/(Lleak+Lmag))*(IL+IM)*cos(t_ph*w_ph)+1/(w
_ph*Lmag)*(Vci-Vin*n/2-Vo*Lmag/(Lmag+Lleak))*sin(t_ph*w_ph); %verified
correct
Ileak1=Ileak_t_ph;
Imag1=Imag_t_ph;
Vci1=Vci_t_ph;
Vco1=0;
Vco1(1:length(t_ph))=Vo;


Vci=Vci_t_ph(length(Vci_t_ph));
Ileak=Ileak_t_ph(length(Ileak_t_ph));
Imag=Imag_t_ph(length(Imag_t_ph));
%Imag=IM;
Vdc_caps=(Co/(Ci+Co))*(Vci-Vin*n/2-Vco);



% Deadtime minus phi

Imag_t_dt=Imag+Vdc_caps/(w_leak*Lmag)*sin(w_leak*t_dt)-(-
(Imag+Ileak)/(Ci*w_leak^2)+Imag/(w_leak^2*(Ci+Co)))/Lmag*cos(w_leak*t_dt)+(-
(Imag+Ileak)/(Ci*w_leak^2)+Imag/(w_leak^2*(Ci+Co)))/Lmag+(Vci-Vin*n/2-
Vdc_caps)/(w_mag*Lmag)*sin(w_mag*t_dt)-(-
Lmag*Imag+(Ileak+Imag)/(Ci*w_leak^2)-
Imag/((Ci+Co)*w_leak^2))/Lmag*cos(w_mag*t_dt)+(-
Lmag*Imag+(Ileak+Imag)/(Ci*w_leak^2)-Imag/((Ci+Co)*w_leak^2))/Lmag;

Ileak_t_dt=Vdc_caps*(w_leak*Ci-1/(w_leak*Lmag))*sin(w_leak*t_dt)+(-
(Ileak+Imag)/Ci+Imag/(Ci+Co))*(1/(w_leak^2*Lmag)-Ci)*cos(w_leak*t_dt)+(Vci-
Vin*n/2-Vdc_caps)*(Ci*w_mag-1/(Lmag*w_mag))*sin(w_mag*t_dt)+(-
Lmag*Imag+(Ileak+Imag)/(Ci*w_leak^2)-Imag/((Ci+Co)*w_leak^2))*(1/Lmag-
Ci*w_mag^2)*cos(w_mag*t_dt);

Vci_t_dt=Vin*n/2-Vci+Vdc_caps*cos(w_leak*t_dt)+(Imag/(w_leak*(Ci+Co))-
(Ileak+Imag)/(w_leak*Ci))*sin(w_leak*t_dt)+(Vci-Vin*n/2-
Vdc_caps)*cos(w_mag*t_dt)+(-Imag*w_mag*Lmag-
Imag*w_mag/(w_leak^2*(Ci+Co))+(Ileak+Imag)*w_mag/(Ci*w_leak^2))*sin(w_mag*t_d
t);

Vmag_t_dt=Vdc_caps*cos(w_leak*t_dt)+(-
(Ileak+Imag)/(w_leak*Ci)+Imag/(w_leak*(Ci+Co)))*sin(w_leak*t_dt)+(Vci-
Vin*n/2-Vdc_caps)*cos(w_mag*t_dt)+(w_mag*Imag*(-Lmag-
1/((Ci+Co)*w_leak^2))+(Ileak+Imag)/(Ci*w_leak^2)*w_mag)*sin(w_mag*t_dt);
```

```
Vleak_t_dt=Lleak*(Vdc_caps*(w_leak^2*Ci-1/(Lmag))*cos(w_leak*t_dt)+-(-
(Ileak+Imag)/Ci+Imag/(Ci+Co))*(1/(w_leak*Lmag)-
Ci*w_leak)*sin(w_leak*t_dt)+(Vci-Vin*n/2-Vdc_caps)*(Ci*w_mag^2-
1/(Lmag))*cos(w_mag*t_dt)+-(-Lmag*Imag+(Ileak+Imag)/(Ci*w_leak^2)-
Imag/((Ci+Co)*w_leak^2))*(w_mag/Lmag-Ci*w_mag^3)*sin(w_mag*t_dt));

Vco_t_dt=Vmag_t_dt-Vleak_t_dt;

Ileak2=Ileak_t_dt;
Imag2=Imag_t_dt;
Vci2=Vci_t_dt+Vci;
Vco2=Vco_t_dt;

Vci=Vci_t_dt(length(Vci_t_dt))+Vin*n;
Ileak=Ileak_t_dt(length(Ileak_t_dt));
Imag=Imag_t_dt(length(Imag_t_dt));
%Imag=IM;
Vco=Vco_t_dt(length(Vco_t_dt));
Vdc_caps=(Co/(Ci+Co))*(Vci-Vin*n/2-Vco);

% Second phase shift

Ileak_t_ph2=-
Co*w_ph_Co*(Vin*n/2+Vco)*sin(w_ph_Co*t_ph)+Ileak*cos(w_ph_Co*t_ph);

Imag_t_ph2=-Vin*n/(2*Lmag)*t_ph+Imag;

Ileak_ss=Ileak_t_ph2(length(Ileak_t_ph2));

Imag_ss=Imag_t_ph2(length(Imag_t_ph2));
%Imag=IM;

Ileak3=Ileak_t_ph2;
Imag3=Imag_t_ph2;
Vci3=0;
Vci3(1:length(t_ph))=0;

Vco3=(Vin*n/2+Vco)*cos(w_ph_Co*t_ph)+Lleak*w_ph_Co*Ileak*sin(w_ph_Co*t_ph)-
Vin*n/2;


Ileak_plot=[Ileak1 Ileak2 Ileak3];
Imag_plot=[Imag1 Imag2 Imag3];
Vci_plot=[Vci1 Vci2 Vci3];
Vco_plot=[Vco1 Vco2 Vco3];

t_plot=[t_ph t_dt+phi t_ph+dt];

figure
plot(t_plot,Ileak_plot)
grid on
title('Leakage inductor current vs time')
xlabel('time (s)')
```

```
ylabel('Current (A)')
hold on

figure
plot(t_plot,Imag_plot,'g')
grid on
title('Magnetizing inductor current vs time')
xlabel('time (s)')
ylabel('Current (A)')

figure
plot(t_plot,Vci_plot)
grid on
title('Inverter side capacitor voltage referred to the secondary vs time')
xlabel('time (s)')
ylabel('Voltage (V)')
hold on

figure
plot(t_plot,Vco_plot,'g')
grid on
title('Rectifier side capacitor voltage referred to the secondary vs time')
xlabel('time (s)')
ylabel('Voltage (V)')

%
eqn1=vpa(-IL-Ileak_ss);

%
eqns=solve([eqn1==0]);
%
Ileak_sol=eqns;
%
Iout=Ileak_sol;
%

% calculating output power

Po=((1/fs)-2*(dt+phi))/(1/fs)*Iout*Vo
```

APPENDIX H

LT Spice Simulation for verifying dead time model



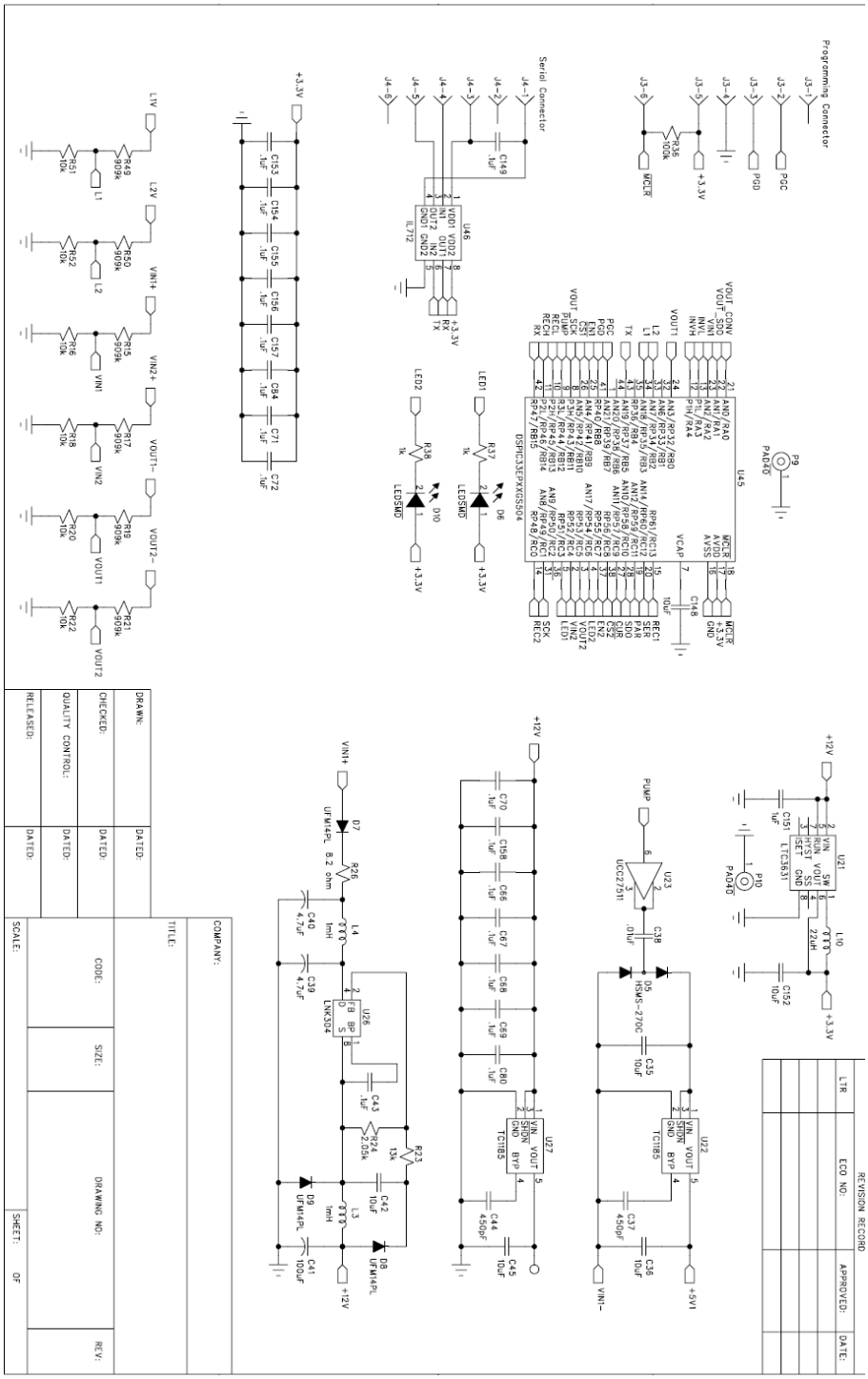
LTSPICE simulation netlist

```
S1 0 N012 vg2 0 SWHS
S3 N012 N009 vg1 0 SWHS
C7 N013 N012 5µF
V1 N009 0 {Vin}
L4 N005 N006 50nH Rser=1m
S5 Vout- N007 vg4 0 SWLS
S6 N007 Vout+ vg3 0 SWLS
V3 vg1 0 PULSE(0 5 {deadtime} 1e-12 1e-12 {0.5/freq-deadtime} {1/freq})
R3 N008 0 1MEG
V4 Vout+ Vout- 24
V5 vg3 0 PULSE(0 5 {deadtime+phase} 1e-12 1e-12 {0.5/freq-deadtime} {1/freq})
C1 N009 0 10µF
C2 Vout+ Vout- 10µF
D1 N012 N009 DHS
D2 0 N012 DHS
D3 N007 Vout+ DLS
D4 Vout- N007 DLS
L1 0 N014 9mH Rser=1m
L5 N008 N011 1mH Rser=1m
R1 N010 N011 1m
V6 vg2 0 PULSE(0 5 {deadtime+0.5/freq} 1e-12 1e-12 {0.5/freq-deadtime}
{1/freq})
V7 vg4 0 PULSE(0 5 {deadtime+phase+0.5/freq} 1e-12 1e-12 {0.5/freq-deadtime}
{1/freq})
C6 Vout+ N007 {Crect}
C8 N007 Vout- {Crect}
C10 N009 N012 {Cinv}
C12 N012 0 {Cinv}
S7 Vout- N008 vg3 0 SWLS
S8 N008 Vout+ vg4 0 SWLS
D7 N008 Vout+ DLS
D8 Vout- N008 DLS
C3 Vout+ N008 {Crect}
C13 N008 Vout- {Crect}
L7 N005 N008 8µH Rser=1m
C14 N007 N006 5µF
L2 N010 N005 1mH Rser=1m
S2 0 N002 vg2 0 SWHS
S4 N002 N001 vg1 0 SWHS
C4 N003 N002 5µF
V2 N001 0 {Vin}
C5 N001 0 10µF
D5 N002 N001 DHS
D6 0 N002 DHS
L3 0 N004 9mH Rser=1m
C9 N001 N002 {Cinv}
C11 N002 0 {Cinv}
L6 N003 N004 285nH Rser=1m
L8 N013 N014 285nH Rser=1m
.model D D
.lib C:\PROGRA~2\LTC\LTSPIC~1\lib\cmp\standard.dio
.model SWHS SW(Ron=0.0224 Roff=100Meg Vt=2  )
.model SWLS SW(Ron=0.00105 Roff=100Meg Vt=2  )
.model DHS D(Ron=0.001m Roff=100Meg Vfwd=0.5)
.model DLS D(Ron=0.001m Roff=100Meg Vfwd=0.5)
```

```
.tran 0 3050us 3000us 1n uic
.MEAS TRAN Pin AVG (V(N009)*I(V1)+(V(N001)*I(V2)))
.MEAS TRAN Pout AVG (V(Vout+)-V(Vout-))*I(V4)
.MEAS TRAN Eff AVG Pout/Pin
.param Vin 72
.param freq 1000E3
.param phase 10n
.step param deadtime 10.4n 312n 10.4n
;param deadtimesec 10.4n
;param phase (10/360)/(freq)
;param deadtime 0.018/freq
;param deadtimesec 0.020/freq
K2 L1 L5 1
K1 L3 L2 1
* Inverter: EPC2016C (1x)\nRectifier: EPC2024 (2x)
.param Cinv 220pF
.param Crect 4100pF
.backanno
.end
```

APPENDIX I

Full system schematic with custom second stage, and active bridge rectifier



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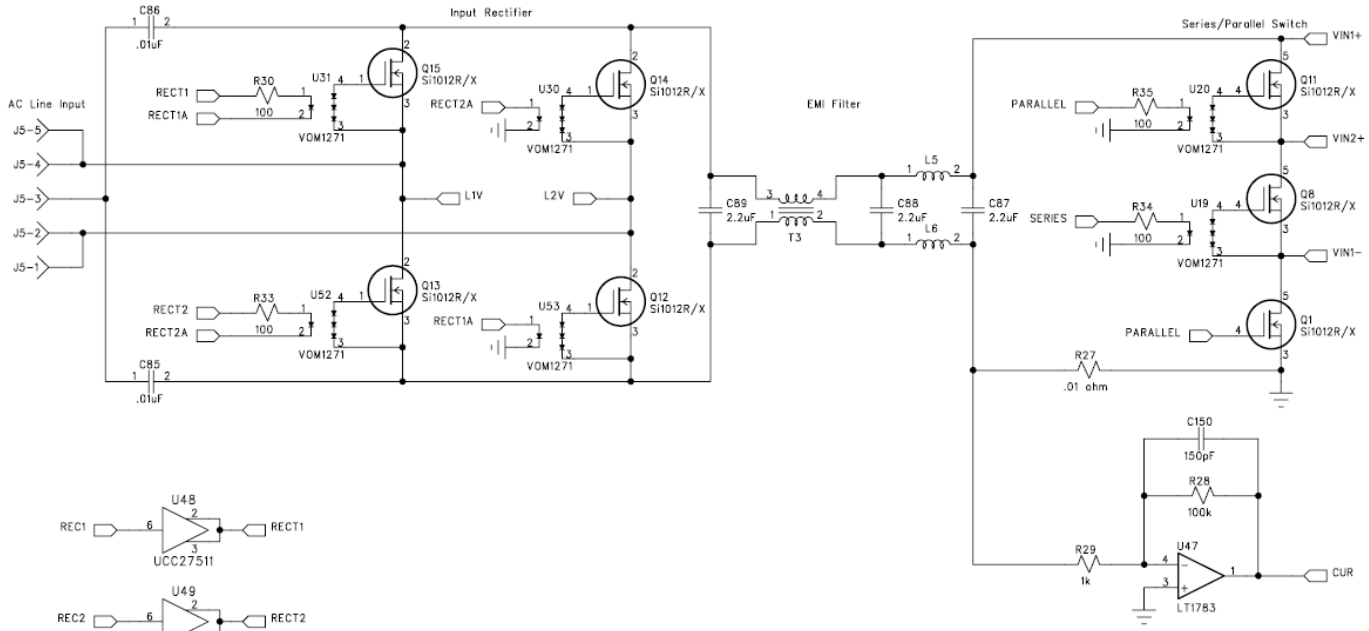

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QUALITY CONTROL:	DATED:				
RELEASED:	DATED:	SCALE:		SHEET: OF	

REVISION RECORD			
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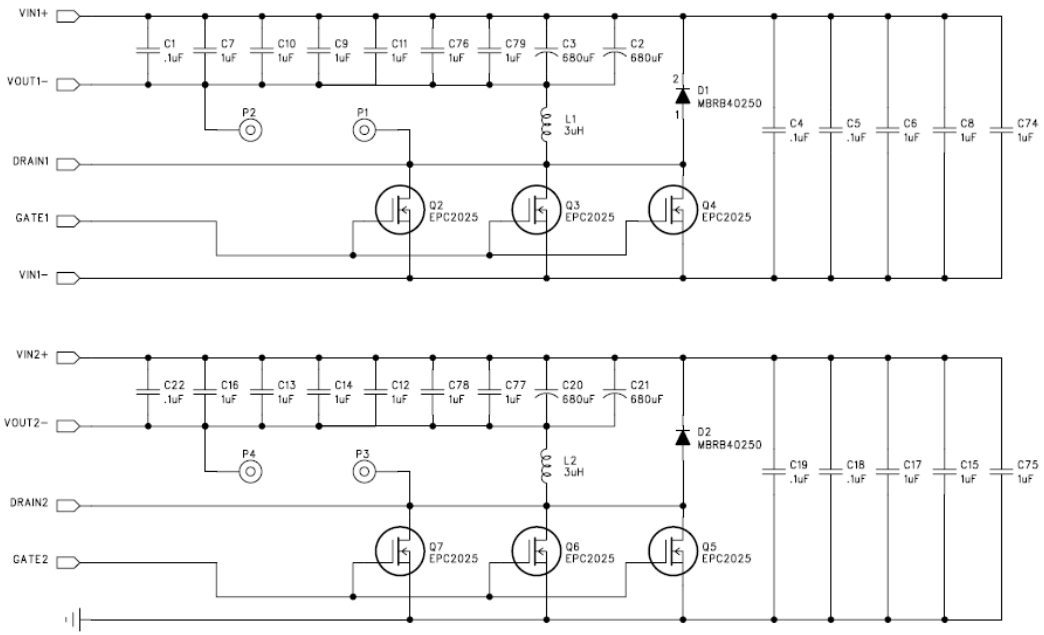

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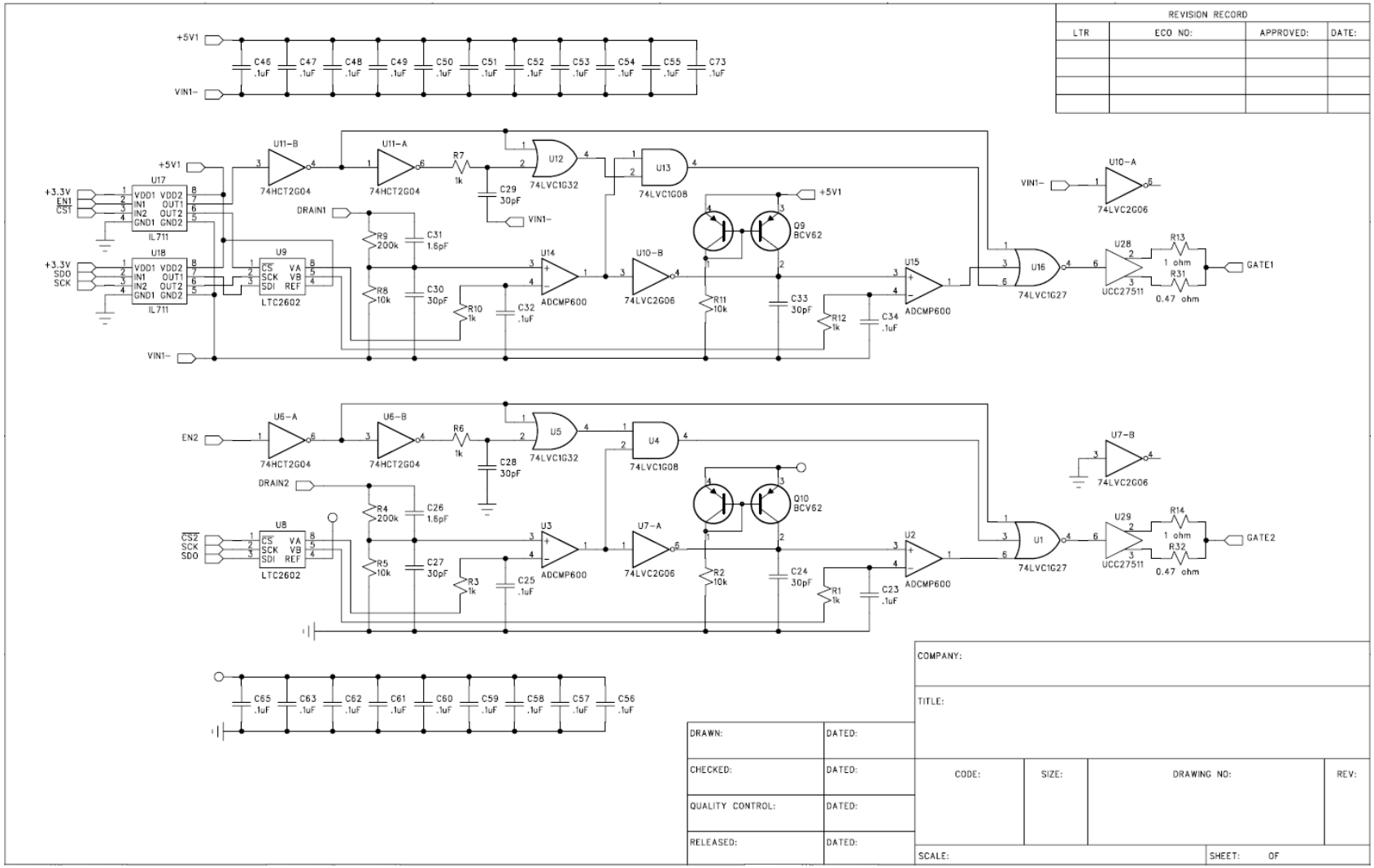
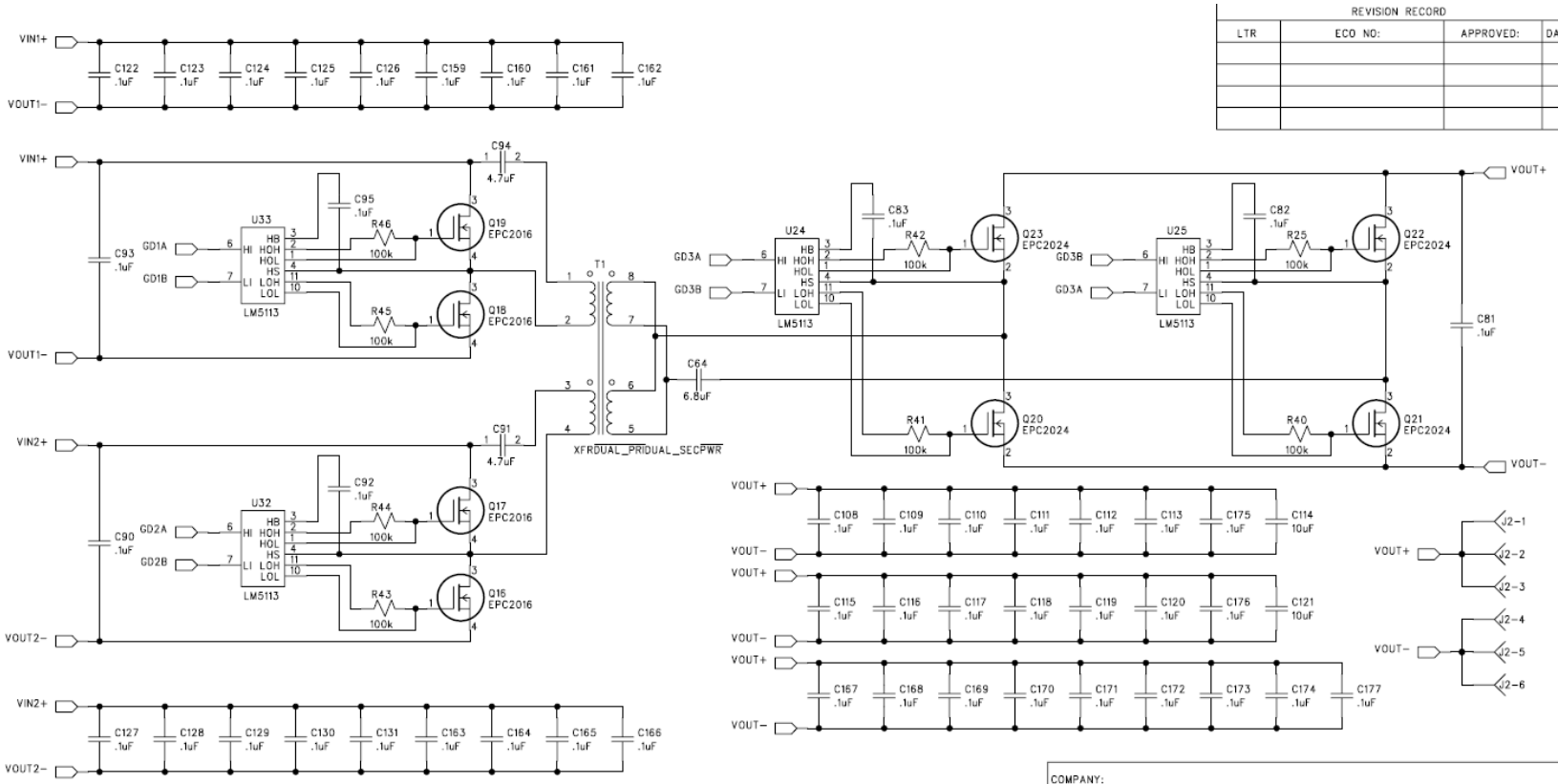

REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
+5V1
VIN1-
C46 .1uF
C47 .1uF
C48 .1uF
C49 .1uF
C50 .1uF
C51 .1uF
C52 .1uF
C53 .1uF
C54 .1uF
C55 .1uF
C73 .1uF
U11-B
U11-A
74HCT2G04
R7 1k
U12
74LVC1G32
C29 30pF
U13
74LVC1G08
U17
IL711
+3.3V
EN1
CS1
U18
SDO
SCK
U9
LTC2602
DRAIN1
R9 200k
C31 1.6pF
R8 10k
C30 30pF
R10 1k
C32 .1uF
U14
ADCMP600
U10-B
74LVC2G06
Q9 BCV62
R11 10k
C33 30pF
R12 1k
C34 .1uF
U15
U16
74LVC1G27
U10-A
U28
UCC27511
R13 1 ohm
R31 0.47 ohm
GATE1
EN2
U6-A
U6-B
R6 1k
C28 30pF
U5
U4
DRAIN2
R4 200k
C26 1.6pF
R5 10k
C27 30pF
R3 1k
C25 .1uF
U3
U7-A
Q10 BCV62
R2 10k
C24 30pF
R1 1k
C23 .1uF
U2
U1
U7-B
U29
R14 1 ohm
R32 0.47 ohm
GATE2
CS2
SCK
SDO
U8
C65 .1uF
C63 .1uF
C62 .1uF
C61 .1uF
C60 .1uF
C59 .1uF
C58 .1uF
C57 .1uF
C56 .1uF
COMPANY:
TITLE:
DRAWN:
DATED:
CHECKED:
QUALITY CONTROL:
RELEASED:
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: OF



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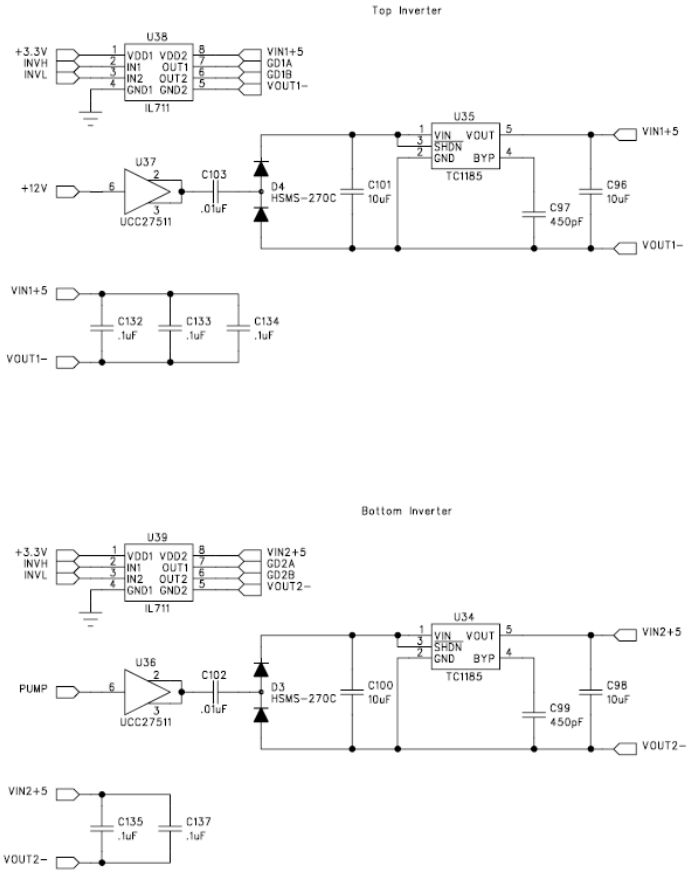
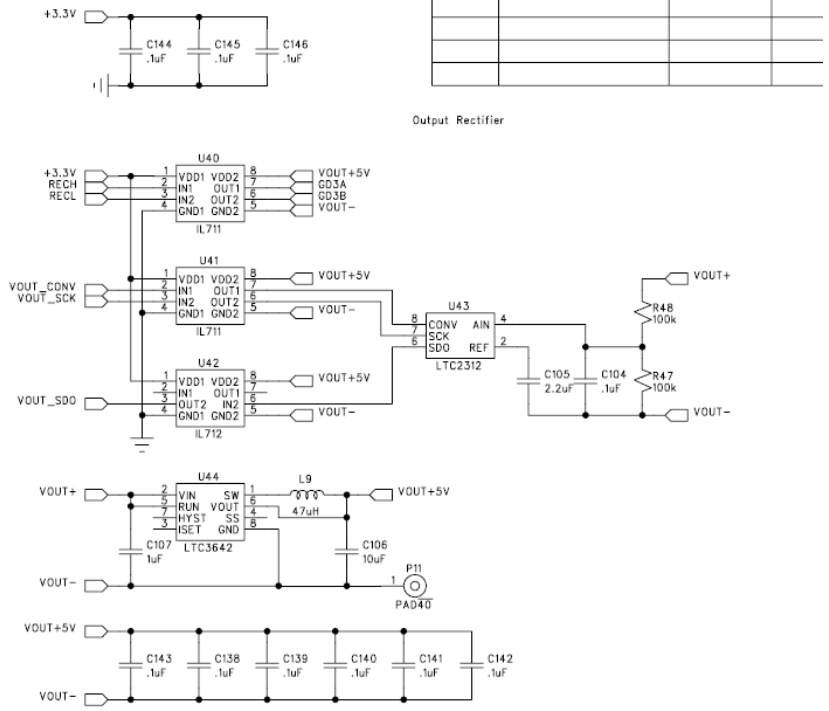
COMPANY:	
TITLE:	
DRAWN:	DATED:
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

CODE:	SIZE:	DRAWING NO:	REV:

SCALE: SHEET: OF





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COMPANY:					
TITLE:					
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CHECKED:	DATED:	CODE:	SIZE:	DRAWING NO:	REV:
QUALITY CONTROL:	DATED:				
RELEASED:	DATED:				
		SCALE:		SHEET: OF	

BOM of Materials for OMRON Supply				
Qty	**Part Name**	**Description**	**Manufacturer**	**Package**
4	ADCMP600	comparator	Texas Instruments	SC70-5
6	IL711	high speed two-channel digital isolator, unidirectional	NVE	MSOP-8
2	IL712	high speed two-channel digital isolator, bidirectional	NVE	MSOP-8
4	LM5113	half-bridge gate driver for GaN FETs	Texas Instruments	DSBGA (12)
4	TC1185	150 mA CMOS LDO with shutdown	Microchip	SOT23-5
2	74HCT2G04	dual inverter	NXP Semiconductors	SC70-5
2	74LVC1G08	2-input AND gate	NXP Semiconductors	SC70-5
2	74LVC1G27	3-input OR gate	NXP Semiconductors	SC70-6
2	74LVC1G32	dual inverter	NXP Semiconductors	SC70-5
2	74LVC2G06	dual inverter	NXP Semiconductors	SC70-6
1	DSPIC33EPXXGS504	16-bit digital signal controller for digital power applications	Microchip	QFN-44
1	LNK304	off-line switcher IC	Power Integrations	8SOP
1	LT1783	operational amplifier	Linear Technology	SOT23-6
1	LTC2312	12-bit 500 ksps Serial Sampling ADC	Linear Technology	TSOT23-8
2	LTC2602	dual 16-bit rail-to-rail DAC	Linear Technology	MSOP-8
1	LTC3631	High Voltage 50 mA Synchronous Step-Down Converter	Linear Technology	MSOP-8
1	LTC3642	High Voltage 50 mA Synchronous Step-Down Converter	Linear Technology	MSOP-8
9	UCC27511	single-channel, high-speed, low-side gate driver	Texas Instruments	SOT23-6
6	VOM1271	photovoltaic MOSFET driver	Vishay	4-SOP
2	LED\SMD	light emitting diode		
3	HSMS-270C	dual diode, schottky, 15V, 750mA	Broadcom Limited	SOT-323
2	MBRB40250TG	diode, schottky, 250V, 40A	ON Semiconductor	D2PAK
3	UFM14PL	diode, general purpose, 400V, 1A	Micro Commerical Components	SOD123FL
2	BCV62	PNP current mirror	NXP Semiconductors	SOT143B

6	EPC2025	eGaN FET, 300V, 6.3A, 120mohm	Efficient Power Conversion	
4	EPC2016C	eGaN FET, 100V, 18A, 16mohm	Efficient Power Conversion	
4	EPC2024	eGaN FET, 40V, 90A, 1.5mohm	Efficient Power Conversion	
3	BSC600N25NS3	N-FET, 250V, 25A, 60mohm	Infineon	TDSON-8
4	STB32NM50N	N-FET, 500V, 22A, 130mohm	STMicroelectronics	D2PAK
2		1.6pF capacitor, 250V, NPO	Johanson Technology Inc	0603
6		30pF capacitor		0402
1		150pF capacitor		0402
4		450pF capacitor		0402
5		.01uF capacitor		0402
110		.1uF capacitor		0402
20		1uF capacitor		
4		2.2uF capacitor		
2		4.7uF capacitor		
1		6.8uF capacitor		
13		10uF capacitor		0603
1		100uF capacitor		
2	400AX4.7MEFC8X9	4.7uF, 400V, 20%, radial electrolytic, 105 degC	Rubycon	
4	EKYB800ELL681MK40S	680uF, 80V, 20%, radial electrolytic, 105 degC	United Chemi-Con	
1	PRL1632-R010-F-T1	.01 ohm resistor, 1%, 1W	Susumu	wide 1206
2		0.47 ohm resistor		0402
2		1 ohm resistor		0402
1		8.2 ohm resistor, 5%, 1/2W	Panasonic	1210
4		100 ohm resistor		0402
9		1k resistor		0402
1		2.05k resistor		0402
10		10k resistor		0402
1		13k resistor		0402

12		100k resistor		0402
2	KTR03EZPF2003	200k resistor, 1%, 1/10W	Rohm	0603
6	KTR10EZPF9093	909k resistor, 1%, 1/8W	Rohm	0805
2	custom inductor	3uH inductor, E22 core, 3F45 material, 5T	MIT	
1	custom transformer	custom transformer, dual 3T primary, dual 2T secondary	MIT	
1	P0422NL	common mode choke, 4.8A, 0.77mH, 40mohm	Pulse Electroinics Corporation	
2	SLF10145T-102MR29-PF	1mH inductor, 290mA, 3.36 ohm	TDK Corporation	
1	NR4018T220M	22uH inductor, 590mA, 432mohm, shielded, wire wound	Taiyo Yuden	
1	NR4018T470M	47uH inductor, 420mA, 780mohm, shielded wirewound	Taiyo Yuden	
2	HC1-100-R	10uH inductor, 12.79A, 5.7mohm	Eaton	
1	68016-106HLF	connector, header, 6 pos, 0.100 R/A 30AU	FCI	
1	0955012661	6 pos 6 pin Modular Jack	Molex	
1	1755778	5 pin header, verticle, 5.08mm	Pheonix Contact	
1	1755765	6 pin header, verticle, 5.08mm	Pheonix Contact	