### **Tunneling Nanoelectromechanical Switches Based On Compressible Self-Assembled Molecules**

**by**

Jinchi Han

B.Eng. Electrical Engineering, Tsinghua University **(2013) M.S.E.** Electrical Engineering, Tsinghua University **(2015)**

Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Engineering and Computer Science

at the

**MASSACHUSETTS INSTITUTE** OF **TECHNOLOGY**

September **2018**

@ Massachusetts Institute of Technology **2018. All** rights reserved.

# Author **........... Signature redacted................**

Department of Electrical Engineering and Computer Science Signature redacted<sup>-August 31, 2018</sup> Certified by .......... Vladimir Bulović Professor of Electrical Engineering and Computer Science Signature redacted Thesis Supervisor Certified by.... **C** Jeffrey H. Lang Io6fessor of Electrical Engineering and Computer Science **Signature red acted** Thesis Supervisor A ccepted **by .......... .................** Leslie **A.** Kolodziejski Professor of Electrical Engineering and Computer Science Chair, Department Committee on Graduate Students **MASSACHUSETTS INSTITUTE**<br>OF TECHNOLOGY OCTI **0 2018** LIBRARIES

 $\label{eq:2} \frac{1}{\sqrt{2}}\sum_{i=1}^n\frac{1}{\sqrt{2}}\sum_{i=1}^n\frac{1}{\sqrt{2}}\sum_{i=1}^n\frac{1}{\sqrt{2}}\sum_{i=1}^n\frac{1}{\sqrt{2}}\sum_{i=1}^n\frac{1}{\sqrt{2}}\sum_{i=1}^n\frac{1}{\sqrt{2}}\sum_{i=1}^n\frac{1}{\sqrt{2}}\sum_{i=1}^n\frac{1}{\sqrt{2}}\sum_{i=1}^n\frac{1}{\sqrt{2}}\sum_{i=1}^n\frac{1}{\sqrt{2}}\sum_{i=1}^n\frac{1$ 

 $\label{eq:2} \frac{1}{\sqrt{2}}\left(\frac{1}{\sqrt{2}}\right)^{2} \left(\frac{1}{\sqrt{2}}\right)^{2}$ 

### **Tunneling Nanoelectromechanical Switches Based On Compressible Self-Assembled Molecules**

**by**

Jinchi Han

Submitted to the Department of Electrical Engineering and Computer Science on August **31, 2018,** in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering and Computer Science

#### **Abstract**

Nanoelectromechanical **(NEM)** switches are investigated as a promising candidate for energy-efficient logic devices. They promise quasi-zero static leakage, large on-off current ratio, small subthreshold slope and high robustness in harsh environments. However, strong van der Waals interaction at the nanoscale usually results in high hysteresis and the risk of stiction failure, thereby bringing about an inevitably high actuation voltage and unfavorable dynamic power consumption in practical device designs. The low switching speed, poor reliability and absence of scalable manufacturing technique also set barriers to the maturation of **NEM** switches to complement or substitute semiconductor transistors for applications with energy constraints.

To accelerate the development of **NEM** switches for digital logic, this thesis presents a novel squeezable **NEM** switch, termed a "squitch", based on direct tunneling through a metal-molecule-metal junction, whose tunneling gap can be electromechanically modulated **by** compressing the molecular layer. **A** sub-5 nm change in the tunneling gap in the absence of direct contact between electrodes leads to at least several orders of magnitude current modulation, enabling a squitch to exhibit a low actuation voltage near 2 V, a low hysteresis and a high switching speed, which support the prospects of squitches as ultra-low power beyond-CMOS devices. **A** scalable and versatile dielectrophoretic trapping technique for fabrication of devices involving nanoparticles in design has also been developed in this thesis as a critical fabrication step.

Thesis Supervisor: Vladimir Bulovi6 Title: Professor of Electrical Engineering and Computer Science

Thesis Supervisor: Jeffrey H. Lang Title: Professor of Electrical Engineering and Computer Science

### **Acknowledgments**

Ever since I joined MIT two years ago, I have received precious support and assistance from my advisors, colleagues and friends. It is a genuine pleasure to express my deep gratitude to those people who have influenced my personal and academic life at MIT.

First, I would like to acknowledge my advisors Prof. Vladimir Bulović and Prof. Jeffrey Lang. Vladimir's insightful guidance, invaluable support and continuous encouragement have always been playing a significant role to the progress of my research. His profound understanding of science and enthusiasm for research inspire me to explore broader research interests and to pursue academic achievements. **I** am also very fortunate and thankful to have the opportunity to be co-advised **by** Jeff. Jeff has influenced me deeply over the past two years with his broad horizon of knowledge and rigorous attitude towards research. **I** am very grateful to Jeff for his great patience in advising me and helping me to develop into a better researcher.

It has been a great honor to be part of the Organic and Nanostructured Electronics Laboratory (ONELab), and **I** have benefited a lot from the enjoyable research atmosphere and the interactions with our lab members, which is critical to development of my research skills and accumulation of my research experience. Especially, **I** would like to thank Dr. Farnaz Niroui for her mentorship and valuable suggestions on my work.

I also received great supports from my friends at MIT. **I** would like to especially thank Zhantao, Jiahao, Juner, Ang-Yu, Haozhe, Pin-Chun, Mayuran, and Matthew for being very helpful to my research and personal life at MIT.

I would like to acknowledge **NSF** Center for Energy Efficient Electronics Science **(E3S)** for supporting my research financially and providing me great opportunities for professional development.

The completion of this thesis is impossible without the training and assistance **I** received from Mark, Kurt, and many research staff in MTL and **CMSE. I** would like to express my thanks to them.

Finally, **I** would like to thank my family for always standing behind me. They

have been encouraging me to chase my dream and reminding me of the importance of perseverance. None of my accomplishments would be possible without their unconditioned love and support. I am grateful to my family forever.

 $\sim$ 

# **Contents**





# **List of Figures**





 $\sim 10^{11}$  km s  $^{-1}$ 

 $\sim$ 

**10**



- **3-13** (a) **A** fabricated four-terminal squitch based on all Au bottom electrodes; **(b)** a fabricated four-terminal squitch based on Au source/drain electrodes and Al gate electrodes. The scale bars correspond to  $1 \mu m$ . 84
- 3-14 (a) Au nanorods nonuniform in length; **(b)** a failed squitch device with multiple short nanorods trapped; (c) a failed squitch device with a single short nanorod trapped; **(d)** a failed squitch device that trapped an aggregate of nanorods from washed suspension; (e) a failed squitch device that trapped an aggregate of nanorods from suspension after **SAM**: (f) a failed squitch device with dislocated nanorod due to significant capillary force when the suspension dries; **(g)** a failed squitch device with nanorod washed away **by** significant capillary force when the suspension dries; The scale bars correspond to  $1 \mu$ m. . . . . . . . . 85
- 4-1 (a) Microscopic image of the testing sample fabricated on quartz substrate **(b) SEM** image of a pair of two-terminal electrodes with a patterned capacitor connected in series. The scale bar corresponds to **100** jim **.. . . . . . . . . . . . . .. . . .. 89** 4-2 Representatives of devices using (a) unfiltered nanorod suspension and **(b)** filtered nanorod suspension. The trapping condition was **1** V, **50** kHz for 2 min. The scale bars correspond to  $1 \mu m$ . . . . . . . . . . . . 90 4-3 Representatives of devices obtained **by** applying (a) **10** kHz, **1** V voltage for 2 min, **(b) 100** kHz, 1 V voltage for 2min, (c) **500** kHz, 1 V voltage for 2min. Unfiltered nanorod suspension was used and the scale bars correspond to 1 **pm. 91** 4-4 (a) **A** device with a single nanorod obtained **by** a **500** kHz, 1 V voltage applied for 2 min; **(b)** a device with two nanorods obtained **by** a **500** kHz, **1.5** V voltage applied for 2 min. Filtered nanorod suspension was used and the scale bars correspond to  $1 \mu$ m. . . . . . . . . . . . . . . . 92 4-5 Successful trapping cases under different conditions. The scale bars correspond to 1 pm **. 93**



**13**

14

 $\mathcal{L}^{\text{max}}_{\text{max}}$  and  $\mathcal{L}^{\text{max}}_{\text{max}}$ 

 $\sim$   $\sim$ 

## **Chapter 1**

## **Introduction**

# **1.1 Nanoelectromechanical Switch - An Ultra-Low Power Emerging Logic Device Beyond CMOS**

For the past few decades, the continuous scaling of conventional semiconductor transistors has brought about enormously enhanced functionality and reduced cost of integrated circuits and systems based on complementary metal-oxide semiconductor **(CMOS)** technologies. However, great challenges that originated from power dissipation, short channel effects, and so on were encountered as the conventional transistor kept shrinking **[1].** After material and structural limitations of Geometrical Scaling were identified, Equivalent Scaling was initiated in the 1990s. Featured technologies such as high-k/metal gate, and FinFET are now able to bring the critical dimension down to **10** nm range [2]. As the effort for extending Moore's law continues, an everincreasing interest in finding alternatives to **CMOS** devices leads to the upsurge of emerging device researches.

Nanoelectromechanical **(NEM)** switches have been investigated as candidate lowpower beyond-CMOS devices for years. For a normally-off type conventional **NEM** switch, the electrodes are physically separated in the OFF-state. As a result, a **NEM** switch features quasi-zero OFF-state leakage and thereby negligible standby power consumption **[3].** When a gate voltage is applied, an electrostatic force on the active element will be induced and then deflect the movable electrode towards the stationary electrode. **If** the voltage is higher than a threshold value, namely the pull-in voltage, the attractive forces including electrostatic force and van der Waals force will overwhelm the restoring force from the movable electrode suspension, consequently leading to a large enough deflection to make the source electrode and the drain electrode in ohmic contact, which corresponds to the ON-state. The transition between the ON-state and the OFF-state usually defines a several orders of magnitude onoff ratio, and the abrupt switching behavior endows **NEM** switches low subthreshold swings, which suggests the potential for low-voltage operation and low dynamic power consumption [4]. Except for the normally-off type, a **NEM** switch can also be configured as the normally-on type, which has the source and drain electrodes initially in contact and relies on an applied gate voltage to pull them apart. With proper combination of these two types of **NEM** switches, basic and complicated logic computation can be achieved with a greatly reduced number of devices compared to conventional **CMOS** technology **[5, 6].** Besides, the transition between ON-state and OFF-state depends on mechanical actuation rather than the diffusion and drift of electrons and holes, which makes the operation less sensitive to temperature [7,8] and various interference (e.g., high dose radiation **[81,** microwaves **[8]** and external electromagnetic fields **[9]).** These fundamental merits make **NEM** switches not only favorable for outdoor sensor networks but also robust in harsh environments with strong interference and extreme temperature encountered in aerospace and defense applications **13, 10].** Moreover, all the aforementioned properties of **NEM** switches perfectly cater to the needs of the thriving Internet of Things (IOT) [4], which adds to their popularity as emerging energy-efficient beyond-CMOS devices.

The drawbacks of **NEM** switches are also distinct, and the ultimate tradeoff for **NEM** switches lies in between device performance and reliability. The special working mechanism of **NEM** switches favors their low-power consumption while at the same time adds uncertainty to their reliable operations. Since the van der Waals force becomes significantly large at the nanometer scale, the source electrode and the drain electrode cannot separate easily when the gate voltage is removed. Therefore, perma-

nent stiction turns out to be one of the prevalent failures for **NEM** switches **[11,** 12]. Even if stiction-free operation is obtainable **by** designing a stiff enough active element, a large hysteresis between ON-to-OFF actuation and OFF-to-ON actuation is usually inevitable for most contact **NEM** switches owing to the effect of van der Waals force at the nanoscale. As a result, though a **NEM** switch can theoretically operate at low voltage due to its excellent subthreshold swing, the actual operation voltage is usually determined **by** hysteresis to ensure reliable operation. Further, slow switching speed compared to **CMOS** devices becomes another weakness of **NEM** switches, considering that mechanical movement is required for switching on and off. In addition, conventional **NEM** switches are usually of much larger dimensions than CMOS-based devices, and scaling as well as integration of **NEM** switches is indeed challenging and still remains an open issue.

This thesis seeks to address some of the aforementioned challenges **by** using selfassembled molecules to make a tunneling **NEM** switch. Compared to conventional **NEM** switches, the electromechanical modulation of the tunneling gap filled **by** compressible molecules allows several orders of magnitude of current change with a **low** actuation voltage. **By** avoiding direct contact between the source electrode and the drain electrode, hysteresis can also be greatly reduced. Prior to the theoretical and experimental study of this novel tunneling **NEM** switch, progress in the field as well as challenges of **NEM** switches will be overviewed in this chapter.

### **1.2 Progress of NEM Switches - State of the Art**

With the rapid advancement of nanotechnology and manufacturing techniques, the performance of **NEM** switches keeps improving **by** innovation of device structure and involvement of novel functional nanomaterials. Nevertheless, most **NEM** switches to date have utilized capacitive structure and functioned **by** mechanically deflecting a movable suspension to contact an opposing electrode despite different configurations and materials used. For such a typical **NEM** switch, stiffness of the active suspending element, the air gap between the suspending electrode and the opposing electrode, and contact materials for low stiction prove to be the most critical design considerations.

When a gate voltage is applied, the charge induced between the active electrode and the gate electrode leads to an electrostatic force proportional to the square of the voltage between the active electrode and the gate electrode. When the gate voltage is small, the active electrode is deflected but not pulled down to the opposing electrode. The deflection is basically decided **by** the force balance among the electrostatic force, the van der Waals force and the elastic restoring force of the strained active element, where the van der Waals force is usually negligible for a large air gap. As the gate voltage increases, new force balance will be established with larger deflection and reduced air gap. However, with the decrease of air gap, the electrostatic force and the van der Waals force increase in inverse proportion to the square and approximately the cube of air gap **[13],** respectively, while the restoring force is only proportional to the deflection. The nonlinearity of the attractive forces results in a critical point of applied voltage, beyond which the resulting attractive force overwhelms the restoring force and the movable electrode keeps accelerating until contact is made with the stationary electrode. At this point, extra supportive force from the stationary electrode helps establish a new force balance in the ON-state. Such a threshold gate voltage, referred to as the pull-in voltage, determines the minimum actuation voltage required to close the **NEM** switch. When the gate voltage is reduced to switch off, the electrostatic force as well as the supportive force from the stationary electrode keeps decreasing, and the **NEM** switch gets ready to open at a specific gate voltage (namely release voltage or pull-out voltage) where the supportive force disappears. Further decrease of the gate voltage will result in acceleration and movement of the active element towards the initial state.

It is evident that a more compliant active element with a shorter separation from the stationary electrode in a **NEM** switch enables a lower pull-in voltage, which is favorable for low-power operation. The side effect is a consequently higher hysteresis since the restoring force in the ON-state is also greatly reduced and the resulting release voltage is smaller. The worst case is that the restoring force is even smaller than the van der Waals force in the ON-state, which means the electrodes will remain

in contact even without any gate voltage applied. For non-memory applications, this is when stiction failure happens. In general, a stiff active electrode with a large enough air gap seems essential to guarantee reliable operation, which comes at an expense of higher operation voltage and power consumption. To date, most researches on **NEM** switches, whether using advanced materials or sophisticated structures, are exploring combinations of stiffness and air-gap thickness, trying to find a "sweet spot" of reliability and device performance. In this section, representatives of **NEM** switches will be introduced and classified **by** structures of electrodes and working principles.

### **1.2.1 NEM Contact Switches Based On Cantilever Nanostructures**

**NEM** contact switches based on cantilever nanostructures have obtained considerable interests ever since the very beginning of researches on **NEM** switches due to their simple structures and ease of fabrication. Typical two-terminal and three-terminal **NEM** switches based on cantilever nanostructures are presented in Figure **1-1** (a). For a cantilever **NEM** switch with a large suspension gap, the effect of van der Waals force is usually negligible and the pull-in happens when the tip deflection reaches one third of the suspension gap. However, van der Waals force will play a significant role in decreasing the pull-in voltage for a switch with a nanometer-scale gap [14].

Pull-in voltage, switching speed and reliability are usually the major concerns for a **NEM** switch. Therefore, a considerable number of researches made improvements from these aspects, and progress for this specific type of **NEM** switches so far has included delicate cantilever structure designs and incorporation of advanced materials or nanoparticles.

In general, a small switching gap between the cantilever and the underlying gate electrode is indispensable to achieve low-voltage actuation. **A 15** nm-thick suspension airgap was made possible with ultra-thin poly-Si as a sacrificial layer and critical point drying technique to prevent the release-related collapse of the cantilever **[15]. A** 13.4 V pull-in voltage, a **3** mV/dec subthreshold slope and a **105** on-off ratio were achieved.



Figure **1-1:** Schematic representation of typical **NEM** switches, including (a) **NEM** switches based on cantilever nanostructures, **(b) NEM** switches based on suspended nanostructures, (c) typical lateral **NEM** switches and a bistable lateral **NEM** switch, **(d) NEM** switches based on vertically aligned nanostructures, and (e) **NEM** switches based on telescoping nanostructures

The pull-in voltage is not low enough because a **300** nm-long, **35** nm-thick titanium nitride (TiN) cantilever was used as the cantilever, which is stiff enough to make hundreds of switching cycles without stiction failure observed. In another work of the TiN cantilever **NEM** switch, a similar pull-in voltage **(13** V) was observed when the airgap was increased to 20 nm and the TiN beam was thinned to **30** nm **[161. A** thin switching gap was also utilized in a **NEM** single-atom switch design. Small deflection of two cantilevers, each with a sharp end to make single-atom gold contact in the ON-state, will either close or open the tiny gap between the tips **[171. A 13.5** V pull-in voltage was reported and such a high threshold was basically due to weak tuning **by** the gate, which was **50** nm underneath the cantilevers. **A** similar working principle was utilized for a **NEM** switch based on interconnected single-walled carbon nanotubes (CNTs) **[181.** When the gate voltage was reduced to less than **-10** V, the induced electrostatic force was strong enough to break the connection between CNTs to switch off.

Effort to reduce the actuation voltage was also made in device structure design. **A NEM** switch based on a cantilever anchored on a suspended torsion bar operated in torsional mode rather than bending mode **[19].** Such a device exhibited a **5.5** V pull-in voltage, which can be reduced to  $\sim$ 1 V level in theory by device optimization.

Except for adjustments of geometries and device structure designs, selection of various nanoparticles for the cantilever nanostructure opens a new opportunity for tuning the mechanical property of the nanoswitch towards enhanced performance. Carbon nanotubes, a type of nanoparticles with well-characterized physical and chemical properties, low mass, good conductivity, and excellent directional stiffness 1201, make very attractive candidates for the cantilever nanostructure and have been the focus of researches for over a decade. **A** number of theoretical works predict that a **CNT** nanorelay is able to work in the **1** V or even sub-1 V regime if the gap thickness can be reduced to a few nanometers level 114,20,211. However, most **NEM** switches based on a **CNT** cantilever reported to date have exhibited pull-in voltages ranging from **5V** to **30** V **[22-25],** which are constrained **by** the large suspension gaps in those devices. The high Young's modulus of **CNT** also allows for **high** operation

speeds for the nanoswitches based on **CNT** cantilevers. **A** switching delay of **10** ns was reported [23], which coincides well with the theoretical predictions [12,20]. These suggest a cantilever-type **CNT** nanoswitch is able to work in a **100** MHz regime. Besides CNT-based cantilevers, a U-shaped NEM switch with  $5 \mu m$  dual Si nanowires was developed, which achieved an average pull-in voltage of 1.12 V but only survived 12 cycles **[261.** Graphene was also utilized as the cantilever nanostructure. Sub-5V pull-in voltage was demonstrated and the switching delay was measured to be **25** ns **[27].**

### **1.2.2 NEM Contact Switches Based On Suspended Nanostructures**

The **NEM** contact switches based on suspended nanostructures usually comprise a double-clamped nanoparticle or ensemble as the active element (Figure **1-1 (b)).** Compared with those based on cantilevers, the **NEM** switches with suspended nanostructures have stiffer active elements, and thereby should exhibit larger actuation voltages [14,28] and higher operating frequencies **[291.**

For the typical double-clamped beam structure, low-dimensional materials were employed as the suspending element in pursuit of enhanced performance. Electrostatic force microscopy enabled characterization of a nanoswitch based on a singlewalled **CNT** bundle **230** nm in length and **27** nm in diameter **[30]. A** 2 V actuation voltage was demonstrated **by** adjusting the pull-in gap to be **6.5** nm. In a pretty recent research, a three-terminal **NEM** switch based on all **2D** materials was developed **[311.** Graphene was used as the suspended beam, and a graphene gate electrode was buried underneath a graphene source electrode with a layer of hexagonal boron nitride **(hBN)** in between as the dielectric layer. Such an all-2D **NEM** switch exhibited a **6** V pull-in voltage with a subthreshold slope of 10.4 mV/dec.

Innovation in device structure design also turns out to be effective to obtain excellent performance of **NEM** switches. **A** large suspended gate electrode employed in a four-terminal nanorelay enabled a low pull-in voltage while small contact dimples

designed to make conducting channels between source and drain led to low hysteresis and high endurance of the device **1321.** Moreover, a recent research revealed that an antistiction molecular layer assembled on the source/drain electrodes allowed for further reduction in hysteresis **[331.** Another interesting design is a so-called pipe clip structure  $[34]$ , which has the lowest to date pull-in voltage  $(400 \text{ mV})$  reported for **NEM** switches without body bias. The success of such a pipe clip device was attributed to the fabricated 4 nm-thick air gap and small contact area between the suspended electrode and the bottom electrode.

Besides the efforts in material and structure design, novel operating principles were also developed. Though these devices may not be classified as contact-mode devices anymore, they are still reviewed here given their same structure with the **NEM** switches based on suspended nanostructures. Semiconductor nanowires have been utilized as suspended elements to make nanoelectromechanical field effect transistors. The gate voltage will induce an electrostatic force on the nanowire to bend it down, and pull-in functions as a mechanical approach for an infinite-gain amplification of the nanowire surface potential **by** the gate voltage **[351.** Such a device based on a Ge-core/Si-shell nanowire achieved a subthreshold slope of **6** mV/dec, which well outperformed conventional semiconductor transistors. Another representative is the capacitive **NEM** switch, which defines the on-off transition **by** changes in device capacitance rather than changes in current. For instance, a **NEM** switch with suspended **CNT** beam exhibited a **33%** tunability in capacitance when a **6** V pull-in voltage was applied **[361.**

### **1.2.3 NEM Contact Switches Based On Lateral Nanostructures**

The lateral **NEM** contact switches work in a similar regime to the aforementioned two types of **NEM** switches except that the active element of a lateral **NEM** switch moves in-plane. **A** typical lateral **NEM** switch is presented in Figure **1-1** (c). Electrostatic force induced makes the cantilever swing to the side gate and thereby connection will be established between the tip of cantilever (the source electrode) and the drain electrode when pull-in happens. An additional pair of gate/drain electrodes are usually added to make bistable lateral **NEM** switches **137,38]** (Figure **1-1** (c)), which are of particular interests for applications as non-volatile memories [39,40. Derivatives of this typical bistable lateral **NEM** switch were also developed, which include Y-shaped layout [411 and clamped-clamped design [39,421. Though actuation voltages of most lateral **NEM** switches reported fell inside **5~50** V range [7,38,41-45], sub-1V lateral switches were predicted possible **by** optimization in geometry design and material selection [38,46], and a 0.8 V pull-in voltage was recently achieved with a 20  $\mu$ m  $\times$  500 nmx **19** nm tungsten nitride cantilever and a **150** nm-thick air gap **[371.**

Lateral **NEM** switch designs based on nanoparticles or ensembles were reported as well. For nanowire-based designs, an ultrathin, long silicon or silicon carbide (SiC) nanowire was double-clamped to make a source electrode and electrostatic force pulled the nanowire to establish contact with a side drain/gate electrode **[8,471. A** tiny airgap was usually inevitable to obtain a low actuation voltage, and both kinds of nanowire lateral **NEM** switches demonstrated 1 V-level actuation voltages. **A** multi-walled **CNT** was also used in a similar structure to make a three-terminal lateral nanoswitch [481, where the **CNT** acted as mask for self-aligned patterning of the side electrodes. The gate electrode on one side repelled the **CNT** (drain) and contact with the source electrode on the other side was established at a pull-in voltage of **3.6** V. In other designs, **CNT** ensembles were employed either as the cantilever for the typical lateral device structure [49] or as the intimate contact of a laterally actuated two-terminal **NEM** switch **[50].**

### 1.2.4 **NEM** Contact Switches Based On Vertically Aligned Nanostructures

**NEM** contact switches can also be designed in a vertical configuration based on metal electrodes or nanoparticles. Triode-structure **NEM** switches based on CNTs are shown in Figure **1-1 (d).** CNTs grown from pre-patterned catalysts are used as the source electrode and the drain electrode, while the gate can be either patterned metal electrodes or another **CNT [51,521.** Both the drain electrode and the gate electrode are connected to positive voltage supplies while the source electrode is grounded. As a result, the drain electrode experiences an attractive force from the source electrode and a repulsive force from the gate electrode. When the gate voltage is large enough, the resulting electrostatic force and van der Waals force overwhelm the elastic restoring force, and drain electrode thereby swings towards the source electrode to make contact. With delicate control of the separation of electrodes, it is possible to make such a vertical nanoswitch operate either in non-memory mode or memory mode **[52].** To maximize the gate control, a self-aligned patterning step with  $\sin x$  as the sacrificial layer enabled fabrication of a gate electrode embracing the drain electrode with a **~30** nm narrow gap, which resulted in a sub-5 V drive voltage **[51].**

Another nanoscale memory device was developed based on a similar design. **A** capacitor on the source electrode was formed by depositing a  $\text{SiN}_x$  dielectric layer and then an outside layer of Cr on the source **CNT** electrode **[531.** The **CNT** drain electrode was still actuated **by** the repulsive force from the gate electrode. Each time the drain electrode contacted the Cr electrode layer, the capacitor on the source electrode was either charged or discharged depending on the bias applied at the drain electrode. In this case, the vertical **NEM** switch can properly work as an erasable non-volatile memory cell.

### **1.2.5 NEM Contact Switches Based On Telescoping Nanostructures**

The idea of telescoping **NEM** switches originates from the low-friction bearing capabilities of multi-walled or double-walled CNTs [54]. The telescoping nanostructure (Figure **1-1** (e)) comprises two open-ended multi-walled or double-walled CNTs with a nanometer-scale gap engineered **by** current-driven breakdown. When a voltage is applied between the adjacent segments, the induced charge on the core shells and that on the outer shell of the same segment have the same polarity, while opposite charge is induced on its adjacent segment. As a result, the inner tube will experience a repulsive force from its outer shell and an attractive force from the adjacent segment, which leads to the sliding of inner tubes and closure of the gap to switch on. When the voltage is removed, the adjacent inner tubes remain in contact due to the van der Waals force. Such a mechanism promises non-volatile memory applications.

**A** unidirectional sliding design of the telescoping **NEM** switch was first experimentally demonstrated with both engineered multi-walled **CNT** and double-walled **CNT,** which showed actuation **by** a sub-5 V voltage and promised a GHz-level operation frequency in theory **[551.** Moreover, the established ON-state of the non-volatile switch can be erased **by** applying a high voltage on the gate electrode.

**A** bidirectional non-volatile switch worked in a similar regime, except that it had electrodes on both sides of the **CNT** with open ends. The van der Waals interaction intratube and the binding energy between the **CNT** and the electrodes created stable energy states on both sides and therefore enabled a non-volatile memory unit with up to three stored digits **[56].** The bidirectional telescoping **NEM** switch was realized **by** Subramanian et al. with a scalable manufacturing method developed **[57].** Multiple bidirectional nanobearings were fabricated simultaneously **by** opening multiple nanogaps of a multi-walled **CNT,** and each pair of opposing **CNT** segments constituted a telescoping device. In this way, a high-density non-volatile memory based on the telescoping nanoswitches was made possible. However, a more sophisticated shell-engineering technique to open the gap is required to ensure consistent actuation voltage from device to device.

#### **1.2.6 Piezoelectric NEM Switches**

Piezoelectric **NEM** switches are actuated **by** induced displacement of the active element that incorporates piezoelectric material rather than **by** an electrostatic force, which makes it intrinsically different from other types of **NEM** switches. Though limited studies of piezoelectric **NEM** switches have been reported, it has shown the best overall performance among all kinds of **NEM** switches so far. Typical topologies utilize cantilever with an embedded piezoelectric actuator. The potential difference between

the gate electrode and the body electrode will induce lateral strain of the piezoelectric film based on the  $d_{31}$  piezoelectric effect, causing a bending motion of the actuator beam stack. As a result, the displaced metal tip either closes the gap to make a conducting channel between the source electrode and the drain electrode (for normally-off switch) or releases to break the connection (for normally-on switch). **A** triple beam configuration was designed to compensate the differences in stresses among the three beams which thus achieved nanometer-level switching gap **[58].** When the source beam and the drain beam also carried actuators, low actuation voltage was achieved **by** simultaneously pulling the three actuators apart. Such a piezoelectric **NEM** switch possessed a **520** mV actuation voltage with a low subthreshold swing of **0.013** mV/dec. Moreover, it is surprising to find the hysteresis to be as low as **8** mV, which indicates a very low surface adhesion between the metal tip and the source/drain electrodes. The low hysteresis also enabled a **10** mV switching with **23** aJ power consumption for each cycle. These superior characteristics make the piezoelectric nanoswitches outperform not only **CMOS** devices but also the majority of **NEM** switches.

#### **1.2.7 Tunneling NEM Switches**

Besides the aforementioned contact **NEM** switches, various tunneling **NEM** switches have also been forwarded. **A** simple tunneling switch can derive from the typical contact-mode switch based on suspended nanostructures. For instance, a tunneling **NEM** switch based on a double-clamped **ALD** Tungsten beam operated **by** bending the suspended beam to tune the tunneling gap, which avoided direct contact of electrodes **159].** In this case, the subthreshold swing was sacrificed in exchange for a greatly enhanced reliability, which was confirmed **by** a lifetime of millions of cycles. Another example for the tunneling device with a similar structure involved single-walled CNTs **[601.** Sub-5 V voltage proved to be enough to achieve a 4 orders of magnitude modulation of the tunneling current, which defined the on-off transition. Besides these derivatives of contact-mode devices, novel designs of tunneling nanoswitches were developed at different scales as well, and a few representatives will be reviewed.

At single-molecule scale, a **NEM** switch operated **by** tunneling of a single **C60** molecule was studied. **A** combination of tunneling, current induced heating and thermal fluctuation resulted in rotation of the **C60** molecule, which led to transition from the face of pentagon carbon atoms to the face of hexagon carbon atoms to contact the electrodes or reversely and subsequent switching between the two states with different conductance **[611.**

At thin-film scale, a monolayer of self-assembled compressible molecules was added into parallel-plate-capacitor structure **[621** or typical lateral **NEM** switch structure **[63].** The molecular layer between metal electrodes defined a metal-molecule-metal junction, which can be electromechanically modulated. Specifically, the induced electrostatic force was able to squeeze the molecules and decrease the tunneling gap, which thereby led to an exponential change in the tunneling current. **A** two-terminal **NEM** switch working in this principle was demonstrated with poly(ethylene glycol) dithiol molecules assembled on twd bottom Au electrodes and a graphene layer as the top floating electrode **[62]. A** sub-2 V actuation voltage as well as a **6** orders of magnitude on-off ratio was achieved, and a nanosecond-level switching time was theoretically predicted. Moreover, the molecular spacer prevented direct contact between electrodes, which effectively reduced the risk of stiction failure. The same idea was also applied to a typical lateral **NEM** switch to make a tunneling three-terminal nanoswitch **[63].**

At macroscopic scale, piezoresistive nanocomposites were used in a tunneling **NEM** switch design [64]. To make the piezoresistive nanocomposites, conductive Ni nanoparticles were doped inside polydimethysiloxane (PDMS). When the nanocomposite was compressed, the tunneling distance between conductive nanoparticles along the percolation pathway was reduced, which brought about exponentially increased tunneling current. Though a 4 orders of magnitude on-off ratio was achieved with **15%** strain, the actuation voltage to achieve such a strain turned out to be considerably high.

## **1.3 Challenges, Limitations, and Prospects of NEM Switches**

In spite of the great progress of **NEM** switches for the past decades in terms of principle design and device performance, great challenges still remain unaddressed and block the maturation of **NEM** switches into viable technologies to make energy-efficient logic units. For instance, a low actuation voltage is usually achieved at the cost of device reliability and a lifetime of billions of cycles usually accompanies with a relatively high threshold voltage **[7,321,** which seems an inevitable tradeoff. Nanoparticles or ensembles allow for superior device performance, while scalable manufacturing techniques for those devices are still in acute needs. Moreover, some obstacles even originate from the intrinsic limitation of **NEM** switches. Compared with **CMOS** devices, **NEM** switches are still not competitive in applications where operating speed rather than power consumption has the highest priority. In this section, perspectives of **NEM** switches will be briefly discussed, which helps understand the critical limitations, challenges and potential applications of **NEM** switches.

### **1.3.1 Failures and Reliability**

Poor reliability has been regarded as a major drawback and thus a critical challenge of **NEM** switches for a long time. To make **NEM** switch a viable technology, prevalent failure modes need to be avoided to greatly extend the lifecycles. In general, **NEM** switches of all kinds risk either structure failure or permanent stiction. In many cases, structure failure is attributed to stress-induced fracture or fatigue **[7,** 24, 47, **65].** In other cases, electrical discharge or high contact resistance will induce transient or accumulative joule heating, which results in surface wear, ablation, and even burnout of electrodes **[15].** Though electrodes may survive structure damage, repetitive switching behavior is likely to generate enough heat to weld the electrodes and thus leads to permanent stiction [26, 39]. At the nanoscale, poor heat dissipation exacerbates these heating-induced issues. For non-memory nanoswitches, another cause

for permanent stiction is excessive electrostatic force and van der Waals force at the nanoscale **[35,37,60].** It is not an issue just for conventional contact **NEM** switches based on metal electrodes with large contact area; nanoswitches based on nanoparticles such as CNTs are also vulnerable to permanent stiction. It has been revealed that stiction-free design window is getting smaller as the device shrinks in size while maintaining a low actuation voltage **[66].**

To avoid structure failure, metals with superior mechanical and thermal properties, such as tungsten, are preferred for electrodes **[321.** Besides, better heat and wear endurance is attainable with protective coating. For instance, deposition of an ultra-thin oxide layer onto the electrode is able to limit the current flow and therefore prevents electrode from burned out **[15].** Coating electrodes with noble metals (e.g., platinum) brings about enhanced hardness of electrodes and wear endurance with cycles of contact, as well as improved resistance to air exposure, corrosion and chemicals [441. To deal with concerns on permanent stiction, a stiff active element in a non-memory design is viable but far from optimal. **A** nanoswitch can be designed to work in a non-contact mode **[251,** but apparently it cannot make a versatile solution. Given the significance of contact interface, great efforts have been made on surface engineering. Carbon-carbon contact becomes more preferable in nanoswitch designs **[12,23,31,501** over metal-metal contact and carbon-metal contact, which are both susceptible to stiction. Intentionally roughening at least one contacting surface helps reduce stiction risk **[13]** while adding more undesirable nonuniformity to device performance from batch to batch. Surface modifications **by** chemical approaches have also been explored **[131.** Particularly, when a monolayer of fluorinated molecules is self-assembled onto the surface of metal electrodes, possibility of stiction is greatly reduced since the surface energy is reduced and direct metal-metal or carbon-metal contact is avoided **[33,621.**

#### **1.3.2 Actuation Voltage and Hysteresis**

Actuation voltage represents the minimum value needed to turn on the switch, and therefore considerable efforts have been made from different aspects to achieve an

actuation voltage as low as possible. However, a high actuation voltage does not necessarily mean a high voltage for switch operation. The idea of employing a **DC** bias at an additional body electrode has been proven effective in reducing the operational voltage of **NEM** switches **by** pre-stressing the active element and therefore moving the IV curve to the left **[32,581.** In this case, the minimum voltage needed for **NEM** switch operation is limited **by** the hysteresis (difference between the pull-in voltage and the release voltage) if a proper body bias is applied to shift the release voltage close to **0** V. **A** low hysteresis, which favors ultra-low power circuit operation, usually requires for a weakened van de Waals interaction when electrodes are in contact. The efforts include miniaturized contact region in design [32-34, **67]** and reduction in surface energy **by** self-assembled anti-stiction coating **[33]** or encapsulation **by** insulating liquid media **[681.** So far, sub-50 mV circuit operation based on **NEM** switches has been successfully demonstrated **[33].**

However, a low hysteresis itself still cannot guarantee low-voltage operation of circuit. When a considerable number of **NEM** switches operate together in a circuit, an identical body bias applied to all nanoswitches is more realistic. **If** the actuation voltage deviates from device to device, the nonuniformity will be added to the actual operation voltage of circuit to ensure reliable switching. For designs with low actuation voltages, the inconsistency among devices is smaller. It explains why **NEM** switches of both low actuation voltage and low hysteresis have been gaining particular interest from scientific community.

#### **1.3.3 Switching Speed**

Compared with **CMOS** devices, the speed of **NEM** switches can be much slower, which is a fundamental limitation originating from the switching mechanism based on mechanical motion. In general, a smaller but stiffer active element has a higher intrinsic frequency, which promises a higher operation speed for the nanoswitch. As a result, most of the high switching speeds reported to date have involved nanoparticles as active elements in device designs. For both vertical and lateral nanoswitches based on single-clamped cantilever, the reported switching delays of **10** ns **[23]** and **25** ns **[27]** for a **CNT** cantilever and a graphene cantilever, respectively, suggested a **100** MHz operation regime, which is much faster than the conventional designs without nanoparticles **[7, 32].** For **NEM** switches based on suspended nanostructures, the higher stiffness of the double-clamped beam enables a higher resonance frequency of the nanostructure **[30, 35][32, 361,** which promises a faster switching speed. **A 2.8** ns delay was experimentally measured for a **CNT** nanoswitch **[601.** On the other hand, stiffer active element usually brings about an undesirable high actuation voltage and issues due to high-voltage operation **169].** Therefore, a combination of a stiff nanoparticle and a body bias constitutes a feasible solution; however, researches on the switching speed of such nanoswitches are still lacking.

#### **1.3.4 Scalable Manufacturing**

Small dimensions and exceptional device performance of **NEM** switches based on nanoparticles or ensembles make them particularly promising; circuit-level operation, however, has not been achieved with these attractive nanoswitches. It is noteworthy that the absence of a universal and scalable manufacturing technique acts as a primary roadblock to further progress in this field **[3].**

For device fabrication, deposition of nanoparticles varies from design to design, but in general, only a few methods are utilized. **A** straightforward idea is that droplets of nanoparticle suspension are first randomly dispensed onto the substrate and metal electrodes are patterned after finding an individual nanoparticle [48, **55].** However, sorting nanoparticles that are stochastically distributed is very demanding, which also brings about huge difficulties for circuit layout. **A** more controlled process was developed to reduce the effort on realignment process for electrode patterning. The affinity between the nanoparticle and specific chemical termination of pre-patterned molecular layer on the substrate is utilized to orient nanoparticles to achieve selfalignment **[70].** Nevertheless, the yield for trapping a single nanoparticle on each spot was not reported, which makes its scalability unclear. Another approach involves nano-manipulators to position individual nanoparticles [12, 24, 54], but such a method is of little practical prospects despite its high precision of positioning. **A**

more realistic approach is catalytic chemical vapor deposition **(CVD).** The catalysts are pre-patterned on the substrate and nanoparticle are directly synthesized on the catalyst to achieve desired position and orientation. The majority of research in this field is related to CNTs, and such a method has been proven to be effective in controlled deposition of individual CNTs **[51-53, 60],** ensembles **[36, 50]** or even arrays at the wafer-scale [49]. However, this catalytic synthesis process is not suitable for nanoparticles (such as many metallic nanoparticles) not compatible with **CVD** process, which makes such a method scalable but not universal. In comparison, **AC** dielectrophoretic trapping makes a versatile method for deposition of nanoparticles **[71,72].** With a proper contrast between the dielectric constant of nanoparticle and that of suspension liquid, a high frequency **AC** electric field will induce a dielectrophoresis force strong enough to trap nanoparticles onto the electrodes. Though the effectiveness of trapping a single nanoparticle has been validated **by** a good number of researches **[18,25,30,57,73],** none has investigated on scaling the dielectrophoretic trapping approach to make multiple devices with individual nanoparticle simultaneously. Therefore, a versatile and scalable method for nanoparticle deposition is of wide interests and in acute demand.

### **1.3.5 Application Prospects**

Regardless of limitations such as poor reliability and low switching speed, the merit of ultra-low power dissipation itself makes all-nanoswitch-based logic circuits attractive candidates for situations where energy consumption is the major concern. Such a motivation gives rise to not only basic logic **(NOT, NAND,** NOR, XOR, etc.) realized **by NEM** switches **151** but also more complex components needed for **VLSI** system, such as latches, adder, memory, and I/O circuits [6, 74]. Compared with CMOS-based components, **NEM** switches are capable of offering a ten-fold or more improvement in energy efficiency **[6].** Moreover, circuit architecture based on single-stage complex gates was proposed to significantly mitigate the low operating speed of **NEM** switches at the circuit-level **by** minimizing the number of mechanical delays on the critical path [74].

Compared with thinking **NEM** switches as substitute for semiconductor devices, the idea of complementing semiconductor transistors seems more realistic at the present stage. Therefore, efforts were made to bring functionality of **NEM** switch into **MOS** devices and circuits. At device level, a suspended gate that can mechanically actuated helps a **MOS** transistor overcome both the large gate leakage and the subthreshold slope limit simultaneously **[751.** At the circuit-level, successful integration of **NEM** switches with nMOS and **CMOS** devices has been achieved **[65,76,77].** Incorporation of **NEM** switches into transistor-based circuits helps block the main leakage path and therefore reduces the stand-by power dissipation **[78].** For staticrandom-access memories (SRAM), replacing two pull-down **MOS** transistors with **NEM** switches results in an **85%** decrease in leakage power **[79].** When **NEM** switches are used for programmable routing in Field Programmable Gate Array **(PFGA),** reduction in both leakage power and critical path delay is attainable **[801.** However, challenges also exist for integration of **NEM** switches with **MOS** devices. Except for the reliability concern, **NEM** switches are required to operate in sub-1 V regime in order to be CMOS-compatible.

### **1.4 Thesis Objectives and Outline**

For a **NEM** switch, the energy consumption per switching cycle and the switching speed are treated as the most significant metrics for evaluation of device performance. Since the static energy loss due to leakage in the OFF-state is typically negligible for **NEM** switches, the energy dissipated during charging and discharging the parasitic capacitors constitutes the major consumption per switching cycle, evaluated **by** the product **of** wiring capacitance and square of actuation voltage for the **NEM** switch. Therefore, a low actuation voltage is critical to obtaining an energy-efficient **NEM** switch. In order to ensure reliable operation, the minimum voltage to actuate a **NEM** switch is approximately the hysteresis plus the product of subthreshold swing and on-off ratio when a proper body bias is applied. It suggests that a low actuation voltage asks for a steep subthreshold slope and a low hysteresis at the same time.

For the switching speed, the mechanical delay for the active element turns out to be the major concern. However, as reviewed above, most **NEM** switches are not able to achieve an outstanding subthreshold swing, a low hysteresis and a high switching speed simultaneously.

This thesis explores an opportunity of using compressible molecules to achieve orders of magnitude modulation in current **by** sub-5 nm displacement, seeking to develop a low-hysteresis **NEM** switch with a low actuation voltage and a high switching speed. To this end, a novel tunneling **NEM** switch has been proposed based on electromechanical modulation of a metal-molecule-metal junction. Self-assembled molecule with a proper chain length is selected to define the nanometer-scale initial thickness of the tunneling gap, in order that negligible leakage current from tunneling is observed. When a voltage is applied between electrodes, an electrostatic force will be induced to squeeze the molecular spacer and thereby to exponentially increase the tunneling current **by** a few orders of magnitude, which is enough to define transition from the OFF-state to the ON-state. When the voltage is removed, initial state of tunneling junction will be recovered due to the restoring force of compressed molecules, turning the switch back to the OFF-state. Such a squeezable nanoswitch is termed as a "squitch".

The proposed squitch promises potentials to address some of the critical challenges that conventional **NEM** switches undergo. First, direct metal-metal contact is avoided in the ON-state **by** employing self-assembled molecules between electrodes in design. As a result, both hysteresis and possibility of stiction failure can be greatly reduced. Second, a sub-5 nm movement of the active electrode during on-off transition is capable of providing adequate modulation of the fabricated nanoscale gap and the tunneling current, which not only allows for a low actuation voltage but also promises a high switching speed. Third, a scalable manufacturing technique for trapping a single nanoparticle on individual devices has been developed, which makes fabrication of the proposed squitches very efficient. Moreover, it is believed that the developed approach is versatile to a good variety of devices, whose fabrication process relies on manipulation of individual nanoparticles.

The remaining contents of this thesis are organized as follows. In chapter 2, a theoretical model of squitches is established, which offers both prediction of characteristics and insights into design considerations towards optimal device performance. Chapter **3** introduces the fabrication process of squitches with efforts in yield control for each step. In chapter 4, effectiveness of the newly-developed scalable trapping technique is experimentally validated, and preliminary results of two-terminal and four-terminal squitches are presented and discussed, which shed light on the challenges remained to be addressed. Chapter **5** summarizes this thesis and future work is provided.
## **Chapter 2**

# **Theoretical Analysis of Statics and Dynamics of A Multi-Terminal Squitch**

### **2.1 Fundamental Concept of A Multi-Terminal Squitch**

#### **2.1.1 Working Principle**

**A** multi-terminal squitch operates **by** electromechanically modulating the width of the metal-molecule-metal junction **by** the applied gate voltage. In particular, a threeterminal squitch (shown in Figure 2-1) has an Au nanorod utilized as the floating electrode and a monolayer of molecules self-assembled on the bottom electrodes, which function as the tunneling barrier between the nanorod and the bottom electrodes. In order to ensure negligible gate leakage during operation, the gate electrode should be recessed **by** a few nanometer. The tunneling gaps of the nanorod-molecule-source junction and the nanorod-molecule-drain junction are defined **by** the thickness of the assembled molecules, which can be electromechanically modulated.

When no gate voltage is applied, the tunneling gap between the nanorod and the bottom source/drain electrode (typically around **5** min) is thick enough to ensure a negligible drain-to-source tunneling current in the OFF-state. The actuation of



Figure 2-1: (a) Schematic of a three-terminal squitch in the OFF-state with zero gate voltage; **(b)** schematic of a three-terminal squitch in the ON-state with a gate voltage equal to the pull-in threshold.

the three-terminal squitch stems from the gate-induced modulation of the tunneling gap, and the compression caused **by** the electrostatic -force induced from the source and the drain is insufficient to cause any significant change to the tunneling gap and the tunneling current, as a small drain voltage is utilized. When a gate voltage is applied, the induced electrostatic force will squeeze the molecules and thereby reduce the width of the tunneling junction. Consequently, the tunneling current will exhibit an exponential increase. The force balance among the electrostatic force, surface adhesive force and the elastic restoring force can be maintained **by** a small reduction in the thickness of molecular layer when a small gate voltage is applied. When the gate voltage reaches a threshold, the overwhelming attractive forces will lead to a collapse of the tunneling gap and a resulting leap in tunneling current, which represents the

transition to the ON-state. This behavior is called "pull-in" and the corresponding threshold gate voltage is defined as the pull-in voltage  $(V_{pi})$ . When the gate voltage is removed, the electrostatic force is drastically reduced and the elastic restoring force helps recover the initial width of the tunneling junction, leading to a transition back to the OFF-state.

In order to design a good squitch, multiple factors must be considered. **A** theoretical model is not only significant for prediction and optimization of device performance, but essential to the comprehension of experimental results as well. Prior to establishing static and dynamic models for the squitch, a few perspectives are discussed to provide basis for the deduction that follows.

#### **2.1.2 Tunneling Current**

The concept of squitches is based on direct tunneling through a self-assembled molecular layer. Therefore, comprehension of the tunneling mechanism across a gap is critical to understanding the device behavior. The electrical conduction based on direct tunneling can **be** described **by** the Simmons model **[81],** and the tunneling current is expressed as

$$
I = \frac{qS}{4\pi^2 \hbar d^2} \left\{ \left( \Phi - \frac{qV_t}{2} \right) \exp \left[ -\frac{2(2m)^{1/2}}{\hbar} \alpha \left( \Phi - \frac{qV_t}{2} \right)^{1/2} d \right] - \left( \Phi + \frac{qV_t}{2} \right) \exp \left[ -\frac{2(2m)^{1/2}}{\hbar} \alpha \left( \Phi + \frac{qV_t}{2} \right)^{1/2} d \right] \right\},
$$
\n(2.1)

where **q** and *m* are the electron charge and the electron mass, respectively, **S** is the area of the gap, *d* is the distance across the gap between the electrodes (i.e., tunneling width),  $V_t$  is the applied voltage,  $\Phi$  is the tunneling barrier height of the molecular layer, and  $\alpha$  is an adjustable parameter that corresponds to the effect of the barrier shape and the electron effective mass.

The values of  $\Phi$  and  $\alpha$  are important for the tunneling behavior and usually determined **by** experiments. For the PEG-thiol molecules used for squitch, these values are selected to be  $\Phi = 1.5$  eV and  $\alpha = 0.4$ , close to the values reported in



Figure 2-2: Dependence of the tunneling current on (a) the voltage across the tunneling junction at different gaps with a barrier height  $\Phi = 1.5$  eV and (b) the tunneling gap with different barrier heights when the voltage across the junction is set as  $V_t = 1$ **V.**

literature [62].

When a gap area of  $0.015 \ \mu m^2$  is assumed, the variation of the tunneling current according to the applied voltage is shown in Figure 2-2 (a). With a constant tunneling gap, the curve describing the dependence of the tunneling current on the voltage across the junction resembles a power function, which is valid for low voltages regardless of the tunneling gap. The variation of the current with the tunneling gap is also simulated according to a constant voltage of 1 V, described **by** Figure 2-2 **(b).** Exponential modulation in the tunneling current **by** variation of the gap is confirmed, and a large tunneling barrier height brings about an increase over more orders of magnitude **by** the same reduction in the gap. With the barrier height selected **(1.5** eV), a 4 nm reduction in the gap leads to an almost **8** orders of magnitude enhancement in the tunneling current, which is outstanding for a **NEM** switch.

#### **2.1.3 Potential of the Floating Electrode**

For a typical three-terminal squitch, three tunneling junctions between the floating Au nanorod and the bottom electrodes form three capacitors  $C_D$ ,  $C_S$ ,  $C_G$  and three resistors *RD, RS, RG* due to tunneling leakage at the source, the drain and the gate,

respectively, as shown in Figure 2-3. The resistance of for a  $1 \mu m$ -long, 60 nm-wide Au nanorod is approximately 10  $\Omega$ , and therefore it is reasonable to assume that the potential along the entire nanorod  $(V_F)$  is constant. It is also assumed that the dielectric constant of the assembled molecules under compression remains unchanged as  $\varepsilon_{rm} = 3$  and the tunneling gaps of  $d_S$  and  $d_D$  are equal. When the recess of the gate is defined as *dr,* the relationship among the gaps at different junctions is described **by**  $d_G = d_S + d_r$ . Therefore, the values of capacitance of the  $C_D$ ,  $C_S$ , and  $C_G$  are given **by**

$$
C_D = \frac{\varepsilon_{rm} \varepsilon_0 S_D}{d_D},\tag{2.2}
$$

$$
C_S = \frac{\varepsilon_{rm} \varepsilon_0 S_S}{d_S},\tag{2.3}
$$

$$
C_G = \frac{\varepsilon_0 S_G}{d_S + d_r - d_{mG} + d_{mG}/\varepsilon_{rm}},\tag{2.4}
$$

where  $\varepsilon_{rm}$  is the relative permittivity of molecules,  $\varepsilon_0$  is the vacuum permittivity,  $d_r$ is the recess at the gate,  $d_{mG}$  is the thickness of molecular layer on the gate, and  $S_D$ , **Ss,** *SG* are the overlap area between the Au nanorod and the drain electrode, the source electrode, the gate electrode, respectively.

The relaxation time (given **by** Equation **2.5)** determines whether the capacitors or the resistors are dominant for the potential of the floating Au nanorod. For the purpose of evaluation, parameters for a three-terminal squitch are selected as  $S_D$  =  $S_S = 0.015 \ \mu \text{m}^2$ ,  $S_G = 0.03 \ \mu \text{m}^2$ ,  $d_{mG} = 5.5 \ \text{nm}$ ,  $d_S = d_D = 5.5 \ \text{nm}$  for the OFF-state and  $d_S = d_D = 1.5$  nm for the ON-state. It should be noticed that these values are chosen arbitrarily but able to be achieved **by** device design and engineering of the molecules. With the selected parameters, the values of capacitance are calculated to be  $C_S = C_D = 7.244 \times 10^{-17}$  F,  $C_G = 3.887 \times 10^{-17}$  F for the OFF-state and  $C_S = C_D = 2.656 \times 10^{-16}$  F,  $C_G = 9.375 \times 10^{-17}$  F for the ON-state. The values of resistance for  $R_S = R_D$  are calculated to be 1.97 TQ in the OFF-state and 13.4 **kQ** in the ON-state according to the currents obtained **by** Equation 2.1, while *RG is* considered significantly larger than  $R<sub>S</sub>$  and  $R<sub>D</sub>$  due to the negligible leakage at the gate. As a result, the relaxation time for the OFF-state is **615** *ps* and that for the



Figure **2-3:** Schematic with definition of variables and diagram of equivalent circuit of a three-terminal squitch.

ON-state is **1.23** ps.

$$
\tau = (C_S + C_D + C_G) \frac{R_S R_D R_G}{R_S R_D + R_D R_G + R_S R_G},\tag{2.5}
$$

**<sup>A</sup>**relaxation time much smaller than the mechanical delay of squitch (typically at the nanosecond-level) will result in a dominant role of resistors for the potential of the floating electrode  $(V_F)$ . In this case,  $V_F$  can be approximated as  $V_D/2$  for small tunneling gaps, considering  $R_S = R_D$  and  $R_G$  is significantly larger. For large tunneling gaps, the relaxation time can be much larger than the mechanical delay. In that case,  $V_F$  will be dominated by the capacitors, calculated by

$$
V_F = \frac{C_D V_D + C_G V_G}{C_S + C_D + C_G},\tag{2.6}
$$

For convenience, the potential of the floating electrode  $(V_F)$  will be assumed constant as  $V_D/2$  to develop the theoretical model for a three-terminal squitch. Though  $V_F$  calculated by Equation 2.6 at large tunneling gaps usually differs from  $V_D/2$ , the deviation is not a concern for evaluating the performance of squitches, considering the tunneling currents are tiny.

#### **2.1.4 Bending of the Au Nanorod**

As the induced electrostatic force is able to bend the suspended Au nanorod, it is necessary to calculate the maximum deflection to ensure that the Au nanorod will not touch the recessed gate electrode and the gate leakage is negligible during operation. The suspended nanorod can be treated as a simply supported beam. The maximum deflection occurs in the center and can be calculated as

$$
y_{max} = \frac{5FL^3}{384EI},\tag{2.7}
$$

where  $F$  is the attractive force imposed on the beam by the gate electrode,  $E$  is the Young's modulus, *L* is the suspended length of the beam and *I* is the moment of inertia. For a Au nanorod with hexagonal cross-section, the moment of inertia is given **by**

$$
I = \frac{(4 - \sqrt{3})D^4}{48},\tag{2.8}
$$

where  $D$  is the width of the beam, i.e., twice the side length of the hexagon. The induced electrostatic force can be calculated **by**

$$
F_e = \frac{\varepsilon_0 S_G}{2(d_S + d_r - d_{mG} + d_{mG}/\varepsilon_{rm})^2} (V_G - V_F)^2.
$$
\n(2.9)

To estimate the maximum deflection of Au nanorod, parameters are assumed the same as those used in the previous section. When a **3** V gate voltage is applied, the squitch is assumed in the ON-state, and the potential of top electrode is **0.5** V when  $V_D$  is 1 V. Since the tunneling gap at the gate is still large, the van der Waals force from the bottom gate electrode is negligible compared to the electrostatic force, i.e.,  $F \approx F_e$ . Therefore, the corresponding maximum deflection in the center of a simply-supported **60** nm-diameter nanorod is less than **3** nm when the suspended length is controlled to be **500** nm. Such a deflection is not sufficient to bring about contact between the nanorod and the bottom gate electrode or noticeable gate leakage because of the recess. On the other hand, the bending even helps reduce the actuation voltage due to the enhanced gate-induced electrostatic force. To reduce the deflection in the center, stiff nanoparticles such as CNTs for the floating electrode are favorable. Besides, the deflection is sensitive to the dimensions of the nanoparticle. For instance, when the diameter of the Au nanorod is increased to 80 nm, the deflection will be reduced to 1 nm. Therefore, uniform Au nanorods are important for making squitches consistent in performance. For convenience, the deflection will not be considered in the models established for squitch.

# **2.2 Static Performance Modeling - Towards A Squitch With Low Actuation Voltage**

In order to establish a theoretical model for the switching mechanism, investigation on the forces that are imposed on the active element is necessary. Apart from the induced electrostatic force and the restoring force from the compressed molecules, adhesive forces at the nanometer-scale play a significant role in the pull-in process. In general, the adhesive forces consist of Casmir force and van der Waals force. Previous work in literature suggests that the Casmir force will dominate when the gap is larger than **10%** of the plasma wavelength of the metal and the van der Waals force is more crucial below that threshold of the gap **182].** As the plasma wavelength of Au is **136** nm **<sup>1821</sup>** and the initial tunneling gap is around **5** nm, it is reasonable to assume that van der Waals force plays a dominant role in the adhesive forces. For convenience, only van der Waals force will be considered in the theoretical model of a squitch. Further, as the gate electrode is recessed, the van der Waals force from the gate electrode should be much smaller than those from the source and drain electrodes and thus is also neglected. In addition, a 1  $\mu$ m-long, 60 nm-wide Au nanord has a mass of 45.17 **fg,** and the trivial effect of gravity on the force balance will not be considered.

For the elastic restoring force, the molecular layer is typically assumed as a linear elastomer when the nonlinearity between the spring constant and the compression is neglected. However, when pull-in happens, the attractive force will overwhelm the restoring force from the compressed molecules, resulting in continuous acceleration of the active element if the molecular spring is assumed linear. For squitches, it is expected that the nonlinearity of the molecules at a large compression is crucial to obtaining and maintaining a stable ON-state. Therefore, the molecular layer is modeled as a nonlinear spring. When the displacement is small, the spring constant increases very slowly. When the compression reaches a threshold, an abrupt change in the spring constant is expected. **A** fractional function can be utilized to model the stiffness, expressed **by**

$$
k_f(d_{S,D}) = \left(\frac{d_0 - d_{thr}}{d_{S,D} - d_{thr}}\right)^p \frac{E_m S_{S,D}}{d_0},\tag{2.10}
$$

where  $d_{S,D}$  and  $S_{S,D}$  are the gap and the area overlap at the source  $(S)$  or drain  $(D)$ , respectively,  $d_0$  is the intial thickness of the molecular layer,  $d_{thr}$  is the threshold value of the gap when abrupt stiffening occurs,  $E_m$  is the Young's modulus of the molecules, and p is the parameter to control the nonlinearity of the spring constant.

The force balance equation is therefore given **by**

$$
F_{eG} + F_{eS} + F_{eD} + F_{vdw} - F_m = 0,
$$
\n(2.11)

where  $F_{eG}$ ,  $F_{eS}$ ,  $F_{eD}$  are the electrostatic forces induced by the gate voltage, the source voltage and the drain voltage, respectively,  $F_{vdw}$  is the van der Waals force, and the  $F_m$  is the restoring force from the compressed molecules. Specifically,

$$
\frac{\varepsilon_0 S_G}{2(d + d_{eq})^2} (V_G - V_F)^2 + \frac{\varepsilon_{rm} \varepsilon_0 S_S}{2d^2} V_F^2 + \frac{\varepsilon_{rm} \varepsilon_0 S_D}{2d^2} (V_D - V_F)^2 \n+ \frac{A_H (S_S + S_D)}{6\pi d^3} - k_f(d)(d_0 - d) = 0,
$$
\n(2.12)

where  $A_H$  is the Hamaker constant,  $E_m$  is the Young's modulus, *d* is the thickness of the tunneling gap at the source (and also the drain), and the equivalent thickness

 $d_{eq} = d_r - d_{mG} + d_{mG}/\varepsilon_{rm}$ . A numerical example will be provided based on the selected parameters as  $\varepsilon_{rm} = 3$ ,  $E_m = 5 \text{ MPa}$ ,  $A_H = 3 \times 10^{-19} \text{ J}$ ,  $d_0 = d_{mG} = 5.5 \text{ nm}$ ,  $d_r = 5$  nm,  $V_D = 0.5$  V,  $d_{thr} = 1.5$  nm,  $S_D = S_S = 0.015$   $\mu$ m<sup>2</sup>,  $S_G = 0.03$   $\mu$ m<sup>2</sup>. The dependence of the tunneling gap on the gate voltage is calculated **by** the developed model and is shown in Figure 2-4.

To understand the numerical results of the variation of tunneling gap for individual device, a single curve with  $p = 0.1$  is first analyzed. In the OFF-state, the tunneling gap is shorter than  $d_0 = 5.5$  nm, indicating that the molecules are pre-compressed. The potential of the floating electrode calculated **by** Equation **2.6** is around **0.25** V when no gate voltage is applied. In the OFF-state, electrostatic forces will be induced in the source, drain and gate regions. As a result, the molecules will be stressed due to attraction **by** both van der Waals force and electrostatic force. When the gate voltage increases from **0** V to **0.25 V,** the voltage between the gate and the floating electrode



Figure 2-4: Dependence of the tunneling gap on the applied voltage at the gate. Different nonlinearities for the molecular layer are represented **by** different parameter p.

**will** be reduced, which leads to a slight release of the top electrode, as observed in Figure 2-4. When the gate voltage is small, the change rate of the attractive force with the displacement of the top electrode (same as compression) can be matched **by** that of the repulsive force, resulting in slow variation of the tunneling gap. The threshold, i.e., pull-in voltage, defines the limit of this equilibrium. **A** gate voltage beyond this threshold will result in attractive forces that overwhelm the repulsive force. The top electrode will accelerate and move towards the bottom electrode until a new stable state (ON-state) is achieved, where the attractive forces are balanced **by** the drastically increased repulsive force due to the abrupt stiffening of molecules. For  $p = 0.1$ , the pull-in happens at  $3.08$  V, where a collapse is observed from Figure 2-4. Further increase in the gate voltage will not bring about further decrease of the tunneling gap because of the stiffened molecules in the ON-state.

The actuation process largely depends on the nonlinearity of the molecular spacer, which can be analyzed **by** comparing the curves with different parameter **p.** When p is large (e.g.,  $p = 0.5 \sim 5$ ), the tunneling gap varies slowly with the increase of gate voltage, but a distinct pull-in process is absent. When parameter **p** is reduced, variation of the tunneling gap gets steeper until clear pull-in behavior is observed when **p** gets down to 0.2. In order to understand the nonlinearity controlled **by** parameter **p,** the equivalent spring constants of the molecular layer are calculated according to different tunneling gaps. As observed in Figure **2-5,** a reduction in **p** will make the elastic property of the molecular spacer closer to that of the typical contact-mode **NEM** switch, which has a spring initially linear and non-compressible upon arrival at the threshold. Therefore, a molecular spring with a smaller **p** is more ideal for **NEM** switch, featured **by** the existence of a pull-in behavior and a steep subthreshold slope, which favors low-voltage operation.

The dependence of the pull-in voltage on the parameters can be investigated **by** the developed theoretical model as well. First, the influence of Young's modulus of the molecules is simulated with  $p = 0.1$ . Figure 2-6 (a) indicates that stiffer molecules correspond to a higher actuation voltage, as expected. The effect of dimensions on the pull-in voltage is studied as well by changing the ratio of overlap area  $S_G/S_D$ ,



Figure **2-5:** Simulated spring constants of the molecular spring at different gaps according to different parameter **p.**

and numerical results are presented in Figure **2-6 (b).** The overlap area at the source is kept consistent with that at the drain. When the overlap at the gate increases, better gate control will be achieved and the squitch can be consequently actuated **by** a lower voltage. The absence of sub-1 V pull-in voltage in Figure **2-6** is attributed to the weakened gate control caused **by** the recess of the gate electrode. If the recess is reduced to 3 nm, a 1.23 V pull-in voltage can be obtained when  $S_G/S_D$  equals 6.

Another important static feature to extract from the IV curve is the subthreshold swing, which decides the rate of change of current with increase in voltage. For squitches, the subthreshold swing is dominated **by** the variation of tunneling gap during the pull-in process, which largely depends on the elastic property of the molecules. To obtain some intuitions, the theoretical IV curves are available when the tunneling gaps are translated into tunneling currents based on the Simmons model (Equation 2.1) with parameters used in Section 2.1.2. The IV curves for three-terminal squitches based on molecules with different elastic properties, represented by  $p = 0.1$ 



Figure 2-6: Dependence of the pull-in voltage on the (a) Young's modulus of the molecules when  $S_G/S_D = 2$  and (b) the overlap area at the gate normalized by molecules when  $S_G/S_D = 2$  and (b) the overlap area at the gate normalized by the overlap area at the drain when  $E_m = 5$  MPa. Other parameters for numerical simulation are  $\varepsilon_{rm} = 3$ ,  $A_H = 3 \times 10^{-19}$  J,  $d_0 = d_{mG} = 5.5$  nm,  $d_r = 5$  nm,  $V_D = 0.5$  $V, d_{thr} = 1.5$  nm,  $S_D = S_S = 0.015$   $\mu$ m<sup>2</sup>.

and  $p = 0.5$ , are shown in Figure 2-7.

Two cases are studied based on molecules with different nonlinear elasticities. When the molecular spring is almost linear above the threshold and noncompressible below the threshold (represented by  $p = 0.1$ ), the elastic system is similar to that for typical contact-mode switches, and a distinct pull-in behavior exists in the IV curve. Near the pull-in voltage, a mere **10** mV change in gate voltage will bring out an almost **5** orders of magnitude change in the tunneling current, which corresponds to an outstanding subthreshold swing (2.14 mV/dec) comparable to those of the contact-mode **NEM** switches. If the molecules have no abrupt stiffening (represented by  $p = 0.5$ , there will be no obvious pull-in behavior and the resulting subthreshold swing can be large. The best subthreshold swing corresponding to a **3** orders of magnitude change in current is around 200 mV/dec. The elastic property of the actual assembled molecules usually lies in between those in the two cases above, and the molecules can be engineered closer to the former, leading towards an abrupt switching behavior at pull-in.

The developed theoretical model also provides some insights into the hysteresis of a squitch. When the voltage is reduced to release the floating electrode, the



Figure **2-7:** IV curves of three-terminal squitches based on molecules with different nonlinear elastic properties, represented by  $p = 0.1$  and  $p = 0.5$ . Parameters for calculation are chosen as  $\varepsilon_{rm} = 3$ ,  $E_m = 5$  MPa,  $A_H = 3 \times 10^{-19}$  J,  $d_0 = d_{mG} = 5.5$ nm,  $d_r = 5$  nm,  $V_D = 0.5$  V,  $d_{thr} = 1.5$  nm,  $S_D = S_S = 0.015$   $\mu$ m<sup>2</sup>,  $S_G = 0.03$   $\mu$ m<sup>2</sup>,  $\Phi = 1.5$  eV and  $\alpha = 0.4$ .

force balance is also represented **by** Equation 2.12, which was developed to analyze the squeezing process. The IV curves for the release process of the three-terminal squitches based on molecules with and without abrupt stiffening, represented **by**  $p = 0.1$  and  $p = 0.5$ , respectively, are simulated and provided in Figure 2-7. A **1.5** V hysteresis is observed for the squitch based on molecules with an ideal elastic property  $(p = 0.1)$ , while no hysteresis exist for the squitch based on molecules that have an elastic property represented **by p = 0.5.** In consequence, the elasticity of the self-assembled molecular spacer turns out to be the key to a low-hysteresis or even hysteresis-free squitch. However, the reduction of hysteresis sacrifices the steepness of subthreshold slope, which seems to be a tradeoff. If the molecules can be engineered

to exhibit different elastic properties for the compression process (e.g,  $p = 0.1$ ) and the release process (e.g.,  $p = 0.5$ ), the hysteresis can be substantially reduced at no cost of the steepness of subthreshold slope. For a hysteresis-free squitch with a **3** V actuation voltage, the energy loss during one switching cycle is estimated to be **90** fJ considering typical wiring capacitance of  $10^{-14}$  F and no additional energy will be lost due to the hysteresis. The energy loss due to static leakage during one switching cycle is nearly **9** orders of magnitude smaller and therefore negligible.

# **2.3 Dynamic Performance Modeling - Towards A High-Speed Squitch**

To study the dynamic performance of a squitch, a theoretical model is established to calculate the switching delays. In the analysis that follows, an actuation voltage equal to the pull-in threshold is applied to turn on the squitch, and then the voltage is completely removed to recover the initial state and thereby turn off the squitch. Oscillation of the tunneling gap near the stable point is predicted before an equilibrium is reached, but it cannot be simulated **by** the established model due to the singularity of the fractional function (Equation 2.10) at the threshold  $d(t) = d_S(t) = d_D(t) = d_{thr}$ . However, when the switching delay is taken to be the time of the first arrival at the corresponding stable position, then the established model is still capable of providing good estimates for the delays. The squeezing process can be represented **by** the differential equation as

$$
m\frac{\mathrm{d}^{2}d(t)}{\mathrm{d}t^{2}}=F_{eG}+F_{eS}+F_{eD}+F_{vdw}-F_{m}, \qquad (2.13)
$$

specifically,

$$
m\frac{\mathrm{d}^{2}d(t)}{\mathrm{d}t^{2}} = \frac{\varepsilon_{0}S_{G}}{2(d(t)+d_{eq})^{2}}(V-V_{F})^{2} + \frac{\varepsilon_{rm}\varepsilon_{0}S_{S}}{2d(t)^{2}}V_{F}^{2} + \frac{\varepsilon_{rm}\varepsilon_{0}S_{D}}{2d(t)^{2}}(V_{D}-V_{F})^{2} + \frac{A_{H}(S_{S}+S_{D})}{6\pi d(t)^{3}} - k_{f}(d(t))(d_{0}-d(t)),
$$
\n(2.14)

where  $m$  is the mass of floating electrode,  $V$  is the voltage applied at the gate electrode, *d(t)* is the time-dependent thickness of the tunneling gap at the source (and also the drain) and the other parameters have been defined in the previous section. The switching delay associated with turning on a squitch can be obtained from the Equation 2.14 when  $V = V_{pi}$ . The time-dependent tunneling gap during the release process can be calculated **by** solving the differential equation

$$
m\frac{\mathrm{d}^2d(t)}{\mathrm{d}t^2} = \frac{\varepsilon_0 S_G}{2(d(t) + d_{eq})^2}V_F^2 + \frac{\varepsilon_{rm} \varepsilon_0 S_S}{2d(t)^2}V_F^2 + \frac{\varepsilon_{rm} \varepsilon_0 S_D}{2d(t)^2}(V_D - V_F)^2 + \frac{A_H(S_S + S_D)}{6\pi d(t)^3} - k_f(d(t))(d_0 - d(t)),\tag{2.15}
$$

which is capable of providing an estimate for the delay associated with turning a squitch off.

Two numerical examples are given based on molecules with different elastic properties as discussed in the previous section. The parameters are selected as  $\varepsilon_{rm} = 3$ ,  $E_m = 5 \text{ MPa}, A_H = 3 \times 10^{-19} \text{ J}, d_0 = d_{mG} = 5.5 \text{ nm}, d_r = 5 \text{ nm}, V_D = 0.5 \text{ V},$  $d_{thr}$  = 1.5 nm,  $S_D = S_S = 0.015 \ \mu \text{m}^2$ ,  $S_G = 0.03 \ \mu \text{m}^2$ . For ideal molecules with abrupt stiffening at the threshold (represented by  $p = 0.1$ ), the actuation voltage is selected as the pull-in voltage  $V = V_{pi} = 3.08$  V, and the variation of the tunneling gaps over time during the switch-on process and the switch-off process is calculated and presented in Figure **2-8** (a). The switch-on delay and the switch-off delay are estimated to be **4.975** ns and **2.830** ns, respectively. Increasing the applied gate voltage can theoretically improve the switch-on delay while no side effect will occur for the switch-off process. For instance, if the actuation voltage is increased to **5** V, the switch-on delay will be reduced to **2.205** ns. As comparison, a three-terminal squitch based on molecules with  $p = 0.5$  is also simulated with  $V = 11.4$  V, and results are shown in Figure **2-8 (b).** The time cost to switch on is calculated to be **0.882** ns, comparable to the delay  $(0.878 \text{ ns})$  for a squitch based on ideal molecules  $(p = 0.1)$ actuated **by** the same voltage. However, the non-ideal molecules enable a switch-off delay of 1.012 ns. The faster speed to switch off arises from a stiffer molecular spring for most of the time under compression compared to  $p = 0.1$ .



Figure **2-8:** Dynamics represented **by** the time-dependent tunneling gaps of threeterminal squitches based on (a) ideal molecules represented by  $p = 0.1$  and (b) nonideal molecules represented by  $p = 0.5$ .

Similar to the dependence of static performance, the dynamics of a squitch are also dependent on a few factors, such as the Young's modulus of molecules, the overlap area, etc. As an example, the dependence on the Young's modulus of molecules is studied and shown in Figure **2-9.** It is evident that a stiff molecular spring exhibits smaller switch-on and switch-off delays, while a large voltage is required to actuate the switch. **A 100** MHz to 2 GHz operating frequency range is predicted based on the numerical results, and the high switching speed stems from the mere 4 nm displacement needed to switch on and off.

Apart from the factors influential to both static and dynamic performance, the mass of the top electrode is also significant but only to the switching speed. **If** the mass of top electrode is reduced **by** an order of magnitude while other parameters hold, the switch-on delay and the switch-off delay for a squitch with **5** MPa molecules  $(p = 0.1)$  will be decreased to 1.574 ns and 0.894 ns, respectively, which corresponds to an over three-fold improvement in the operating frequency. From this perspective, the idea of replacing the Au nanorod **by** lighter nanoparticles such as multi-walled **CNT** is attractive and high-speed squitches with low actuation voltages are thereby promising.



Figure **2-9:** Dependence of the squitch delays and the highest operating frequency on the Young's modulus of the molecules.

### **2.4 Summary**

Theoretical models to describe the statics and dynamics of a three-terminal squitch have been established. Perspectives regarding the electromechanical modulation of the tunneling width and current have been discussed, which act as the basis for the development of the theoretical model. Significant metrics to evaluate device performance, including pull-in voltage, subthreshold swing, and switching delays have been numerically simulated, and their dependence on various factors, e.g., stiffness of molecules, dimensions of electrodes, mass of active element, has been investigated as well **by** the established static and dynamic model. Moreover, the elastic property of the molecules has been proved critical to both statics and dynamics of squitches. This suggest a possible approach to configure the device performance **by** engineering the properties of self-assembled molecules.

The simulation results not only validate the feasibility of the squitch concept, but also indicate the potential of squitches to make low-hysteresis **NEM** switches with low actuation voltages and high switching speeds. It should be pointed out that many parameters utilized for numerical simulation are arbitrary. However, since all the parameters depend either on the device structure or the materials utilized, the actual squitches can be designed to obtain the simulated device performance. For instance, the tunneling gap in the ON-state, which is assumed as **1.5** nm for all the simulation, can be controlled **by** engineering the elastic property of the molecules. In general, compliant molecules with a sufficiently long chain and abrupt stiffening behavior allow for a low actuation voltage, a negligible static leakage, a high **ON**state tunneling current and a steep subthreshold slope, which also defines a large on-off ratio and a low ON-state resistance. Further, a large gate area in design helps decrease the actuation voltage. In order to achieve a high switching speed, a light floating electrode is favorable, which justifies the idea of utilizing nanoparticles such as Au nanorod and **CNT.**

# **Chapter 3**

# **Nanofabrication of A Multi-Terminal Squitch**

### **3.1 Fabrication Process Overview**

The fabrication process of a multi-terminal squitch is a combination of top-down and bottom-up fabrication techniques. The process flow is presented in Figure **3-1.**

In the first fabrication step, the bottom electrodes are patterned **by** electron beam lithography, metal evaporation and a standard lift-off process. Gold (Au) is chosen as the metal to make the bottom electrodes, for its great stability in air and resistance to corrosion and chemicals. Moreover, it favors the subsequent peeling process and the self-assembly process. To fabricate a multi-terminal squitch, a recess of a few nanometers for the gate electrodes is essential, which ensures a negligible gate leakage current at a small sacrifice of gate control. To this end, a patterned ultra-thin sacrificial layer is utilized to define the recess.

In the second fabrication step, a peeling technique is developed to transfer the bottom electrodes from the initial  $Si/SiO<sub>2</sub>$  substrate to a receiving glass substrate with epoxy. The purpose of this step is to obtain planarized bottom electrodes with sub-nanometer roughness, which will contribute to a uniform assembled molecular spacer and an identical thickness of the tunneling gap over the entire junction.

In the third fabrication step, a monolayer of poly-ethylene-glycol **(PEG)** molecules,





Figure **3-1:** Nanofabrication process flow of a multi-terminal squitch.

which have single or double thiol terminations, is self-assembled to the bottom electrodes when the sample is soaked inside PEG-thiol solution.

In the last fabrication step, a synthesized Au nanorod, which will be employed as the top floating electrode, is positioned to bridge the source bottom electrode and the drain bottom electrode **by AC** dielectrophoretic trapping approach. For all these fabrications steps, it is noteworthy that the **AC** dielectrophoretic trapping is the most challenging step and in general not suitable for massive manufacturing of nanoparticle-based devices, for sophisticated control is demanded to position a single nanorod on each device precisely. Herein, a scalable trapping approach will be proposed and its effectiveness will be validated in Chapter 4. It is believed that the novel scalable trapping technique represents a versatile and efficient solution to fabrication of various kinds of devices involving nanoparticles in their design.

This chapter will present the nanofabrication process of a multi-terminal squitch with comprehensive details of each step. The fabrication of a two-terminal squitch is similar except that patterning of the gate electrodes and the sacrificial layer is removed, and therefore it will not be the focus in this chapter. Considering the significance of yield control, typical failure modes will be discussed for each fabrication step in this chapter, and approaches to avoid those failures and thereby ensure a high yield will be highlighted.

### **3.2 Bottom Electrodes Patterning**

Miniaturization of a squitch not only favors high density integration but also promises superior device performance. Besides, the stochasticity in the length of synthesized Au nanorods also asks for shrinking the size of a squitch. Specifically, the longer the nanorods are, the more non-uniform they are in length. Short nanorods contribute to a higher yield for **AC** dielectrophoretic trapping and more consistent performance from device to device. Based on these considerations, the bottom electrodes are designed with a miniaturized active area no larger than 2  $\mu$ m $\times$ 500 nm and gaps between electrodes smaller than 200 nm. In this case, electron beam lithography, which is capable of making sub-10 nm fine features with a sub-10 nm alignment resolution, is utilized to pattern the bottom electrodes.

**<sup>A</sup>**gate recess is significant in the concept of multi-terminal squitches. To this end, a monolayer of graphene is grown **by** chemical vapor desposition **(CVD),** transferred onto the 300nm-Si $O_2/Si$  substrate to act as the sacrificial layer, and patterned before deposition of the electrodes in order to achieve the gate recess. Smooth surfaces of bottom electrodes that face the tunneling gaps are critical to obtaining consistent tunneling junctions and consequently uniform device performance. However, conventional methods to deposit metal electrodes, e.g., evaporation or sputtering, usually bring about a roughness of a few nanometers or even larger, which makes assembling molecules difficult and may even result in local shorting spots between the bottom electrode and the floating top electrode. Though metal electrodes patterned **by** atomic layer deposition **(ALD)** technique usually have much lower roughness, it is not practical to make **100** nm-thick bottom electrodes with **ALD.** For squitch fabrication, electrode roughness is remedied **by** using thermal evaporation for metal deposition and followed **by** a peeling technique developed for subsequently transferring the patterned electrodes onto a receiving substrate. As a result, the electrode surfaces previously in intimate contact with the initial substrate will be exposed and roughness of the transferred electrodes will be determined **by** the substrate roughness (sub-nanometer roughness for a polished Si or  $SiO<sub>2</sub>/Si$  wafer).

To pattern the bottom electrodes, we start with a Si or  $300 \text{ nm } \text{SiO}_2/\text{Si}$  substrate with a monolayer of graphene on top. For the purpose of peeling in the following step, no adhesive layer (e.g., chromium or titanium) is allowed in deposition of bottom electrodes, which makes the Au patterns vulnerable during the lift-off process. To address this issue, an undercut of resist after development can facilitate the lift-off process **by** avoiding metal deposition on the sidewall. Therefore, a combination of poly(methyl methacrylate) (PMMA) and copolymer consisting of methyl methacrylate (MMA) and methacrylic acid **(MAA)** is adopted.

In the first step, alignment marks, large electrode pads and connecting wires are patterned. Copolymer (MMA **(8.5) MAA) EL9** (from MicroChem Inc.) is first spincoated onto the substrate at **2500** rpm for 1 min followed **by** baking at **180 'C** for 2 min. The resulting thickness of copolymer layer is approximately 400 nm. Then another layer of PMMA **950** A4 (from MicroChem Inc.) is spin-coated on top of the copolymer layer at **2500** rpm for 1 min and baked at **180 'C** for another 2 min, leading to a thickness of 250 nm. Elionix **FS-125** is used as the electron beam lithography tool, which operates at **125** keV acceleration with adjustable beam current from **25 pA** to 100 nA. The area dose for exposure is set to  $1400\sim1500 \mu C/cm^2$ . For the large features, **80** nA beam current is selected, which corresponds to a **100** nm beam size. After exposure, the sample is soaked inside a **1:3** methyl isobutyl ketone (MIBK) **:** isopropyl alcohol (IPA) developer for 90s at 20 **'C,** rinsed in IPA and dried with a stream of nitrogen. Since the exposed copolymer dissolves at a higher rate than the

exposed PMMA, a 400 nm-thick undercut layer is therefore formed after development. Then **100** nm-thick Au film is thermally evaporated onto the sample at a rate of **0.5** A/s. After evaporation, the sample is put in acetone for at least **8h,** to complete the lift-off process. When the resist is dissolved **by** acetone, the Au film will be lifted off, leaving **100** nm-thick Au on the patterned region.

The second step of patterning is to selectively etch the graphene monolayer in order to define the recess. After peeling the electrodes, the gate should be a few nanometers lower than the source and drain electrodes. Therefore, the graphene at locations where source/drain electrodes lie should be removed while the graphene on the regions corresponding to the gate electrodes must be protected. **A** single layer of PMMA resist is required for the graphene patterning step. PMMA **950** A4 is spincoated onto the sample at 2000 rpm and baked at **180 'C** for 2 min. The regions to be etched are first exposed **by** electron beam with 2 nA beam current **(2.5** nm beam diameter) and a  $1400\sim1500 \mu C/cm^2$  area dose. After development in 1:3 MIBK:IPA developer, the sample is placed inside an oxygen plasma cleaner to etch the graphene on the exposed regions. Then the sample is put in acetone to strip the resist, rinsed in IPA and dried **by** nitrogen flow.

In the third step, small electrodes including the source, drain and gates will be patterned. Bilayer resist with copolymer and PMMA is dispensed with the same recipe as described in the first step. **A** 2 nA beam current is selected to pattern these small electrodes with gaps less than 200 nm in between. Alignment during ebeam lithography is required to make sure that the source and drain electrodes, patterned **by** metal evaporation and subsequent lift-off process, lie on the etched regions in the previous step. The patterned gate electrodes between the source electrode and the drain electrode therefore have graphene underneath.

The as-patterned bottom electrodes are shown in Figure **3-2** with a few typical designs. As observed in the images, the gaps between electrodes can be made as tiny as 40 nm. The separation between the source electrode and the drain electrode can be miniaturized to 450 min for a four-terminal design (Design **A)** and **300** nmn for a three-terminal design (Design **D).**



Figure **3-2: SEM** images of patterned bottom electrodes. Design **A,** B, **C** represent the bottom electrodes for four-terminal squitches with different overlaps among source, drain and gate. Design **D** represents the bottom electrodes for a three-terminal squitch. The scale bars correspond to 200 nm.

The yield for the patterning the bottom electrodes is usually within the **80%-100%** range, depending on the design and the feature size. For this step, several failure modes should be avoided to achieve a high yield.

First, patterning nanogaps less than **100** nm between electrodes is in general difficult when the bilayer resist is employed for Au patterning. The undercut layer permits the adjacent electrodes to easily short if the gap is designed to be small (as shown in Figure **3-3** (a)).

Second, with the help of the undercut layer, no sonication or heating is needed for the lift-off process. However, extra care is still necessary considering the weak adhesion between evaporated Au and graphene on the substrate. Figure **3-3 (b)** and (c) show examples of failed devices when the container was not shaken gently to lift off the Au film. The electrodes were either torn (Figure **3-3 (b)),** or peeled and then



Figure **3-3: SEM** images of failed bottom electrodes. (a) shorted electrodes; **(b)** torn electrodes; (c) peeled electrodes; **(d)** broken electrodes caused **by** resist residual after development; (e), **(f)** broken gate electrodes due to collapse of suspended resist beam. Insets of (e) illustrate how the failed electrodes form. The scale bars correspond to **500** nm.

resettled on the substrate (Figure **3-3** (c)).

Third, after the sample is developed in an MIBK/IPA solution, it should be rinsed well in clean IPA twice to get rid of undissolved resist particles. Otherwise, the resist residuals will act as undesirable masks during evaporation and therefore result in broken electrodes after lift-off, as presented in Figure **3-3 (d).**

Besides, the copolymer layer between adjacent electrodes (exposed regions) can completely dissolve during development if the gap is small, thereby forming a suspended PMMA beam. The resist suspension is susceptible to collapse when the sample dries, and the longer the gap is designed to be, the more vulnerable the PMMA beam is. In this case, the following metal deposition based on the broken mask will result in failed electrodes as shown in Figure **3-3** (e) and **(f).** To prevent this failure, designs involving sub-100 nm wide gaps with large aspect ratios should be avoided. Otherwise, controlling the flow of nitrogen while drying the sample, i.e., low pressure combined with orientation parallel to the length direction of the suspended PMMA beam, can be critical towards a high yield.

Avoiding the aforementioned failures will ensure the completeness and correct shape of the electrodes. However, it is still not enough to guarantee the success of patterned bottom electrodes. In order to recess the gate, it is required that the source electrode and the drain electrode be deposited on the etched region of graphene. **If** they are shifted, some locations of the gate may not be recessed after the peeling step, which will bring about large gate leakage or even shorting issues. Aligning patterns based on the same set of alignment marks for ebeam exposure in both the graphene patterning step and the small electrodes patterning step should offer an alignment accuracy of sub-10 nm level when Au is used to make marks. However, the subsequent evaporation step will also experience an alignment issue, arising from the employment of bilayer resist.

Figure 3-4 (a) presents an example of a failed device with the alignment issue. It can be observed that the edges of rectangular shadows (region of etched graphene) do not align with the edges of source and drain electrodes. It is attributed to the misalignment between the evaporation target and the sample above it. As illustrated in the inset of Figure  $3-4$  (a), due to the existence of the undercut layer, the misalignment will allow the metal vapor to penetrate underneath the PMMA mask and therefore result in a slight shift of the pattern. The shorter the separation between the target and the sample is, the more deviation the evaporated electrodes will have.

Though the shift is usually no more than 200 nm, it is large enough to destroy a squitch, considering that the gaps between adjacent electrodes are usually **100** nm or less. **A** more straightforward case is presented in Figure 3-4 **(b).** When a **10** nm Cr adhesion layer is deposited underneath **80** nm Au (not the typical case for squitch fabrication), the two layers can be badly misaligned when the two target boats are on different sides, as illustrated in the inset of Figure 3-4 **(b).**



Figure 3-4: **SEM** images of bottom electrodes failed due to pattern shift; (a) misalignment between the evaporated electrodes and the previously etched region; **(b)** misalignment between evaporated Au pattern and the adhesive Cr layer underneath. Insets explain the pattern shift during evaporation due to misaligned target and sample. The scale bars correspond to **500** nm.



Figure **3-5: SEM** images of (a) four-terminal and **(b)** three-terminal bottom electrodes with Au for the source/drain and **Al** for the gates. The scale bars correspond to 200 nm.

In addition, such an evaporation issue demands special consideration when the source/drain electrodes and the gate electrodes are not patterned in the same step. For instance, depositing metal with a good adhesion to epoxy for the gate electrodes is beneficial to device reliability, and deposition of different metals for the electrodes also allows for a selective self-assembly process on the bottom electrodes. In this case, two evaporation steps are inevitable. To prevent the issue of shifted electrodes, a large separation between the target and the sample is favorable. Besides, manual alignment of the sample right above the target before evaporation will be conducive, if possible. Dispensing a thinner undercut layer can also help reduce the shift of electrodes. Figure **3-5** presents successful examples with patterned Au source/drain electrodes and **Al** gate electrodes, whose fabrication involved separate patterning steps and manual alignment between the sample and the target before evaporation.

## **3.3 Bottom Electrodes Transfer by Peeling Technique**

The surface roughness of evaporated electrodes (usually a few nanometers) makes it difficult to assemble a uniform molecular monolayer, and increases the risk of device failure from ohmic contact between the floating electrode and spikes on the bottom electrodes. Therefore, a peeling technique is developed to flip the electrodes and thereby expose the other surface of the evaporated electrodes for use, whose sub1 nm smoothness is defined **by** the initial substrate. For squitch fabrication, the initial substrate has a monolayer of graphene on top of polished  $300 \text{nm-SiO}_2/\text{Si}$ . Though graphene may wrinkle during the transfer process, it will not affect the local smoothness if it adheres well to the substrate. Therefore, sub-nanometer roughness is still guaranteed. Other **2D** materials are also applicable as the sacrificial layer, as long as they can be easily etched without damaging the substrate underneath.

**A** schematic for the peeling step is included in Figure **3-1.** Glass is utilized as the receiving substrate so that the Au electrodes can be peeled **by** UV-cured epoxy. Other transparent dielectric materials such as quartz are appropriate for peeling as well. However, extra care will be required for handling and peeling, for quartz is not as compliant as glass. Besides, epoxy does not have to be UV-curable. In that case, non-transparent substrates can be applied and annealing is required to cure the epoxy instead of **UV** exposure. Whichever type of epoxy is employed, it is better to be solvent-free. Otherwise, bubbles will form inside the epoxy layer after curing, which exacerbates the weak adhesion between electrodes and epoxy. To avoid the bubbles, a porous receiving substrate is preferred and a multi-stage annealing scheme under vacuum condition can be helpful.

For squitch fabrication, **NOA61** from Norland Products, Inc., which has good tolerance for many chemicals after curing, is chosen for the UV-cured epoxy. Though the adhesion between Au and epoxy is in general weak, this approach is effective since such an affinity is still better than that between Au and graphene. For applications without graphene, a self-assembled monolayer **(SAM)** coating is essential to prevent stiction between the epoxy and the substrate. To fabricate a squitch, this step is also beneficial, for there are exposed  $SiO<sub>2</sub>$  regions where the graphene was etched away. Trichloro(1H,1H,2H,2H-perfluorooctyl)silane or 1H,1H,2H,2H-Perfluorodecyltriethoxysilane can be used for vapor-phase **SAM** coating, while the latter demands a much longer time for assembly.

**A** detailed peeling step is presented as follows. Vapor-phase **SAM** assembly is conducted inside a desiccator. The sample with patterned electrodes is put on a glass slide slightly above a 10  $\mu$ L droplet of 1H,1H,2H,2H-Perfluorodecyltriethoxysilane molecule. The desiccator keeps pumping down **by** household vacuum for **30** min to help the droplet evaporate into its vapor phase, after which the desiccator is isolated from the vacuum line and stands alone for another  $30\nu 40$  min to assemble fluorosilane onto the substrate. For the other type of fluorosilane molecule, **5** min pumping plus **5** min isolation should be enough. After **SAM** assembly, it is suggested that the sample should be rinsed inside ethanol and dried **by** nitrogen flow. The purpose of this step is to remove the residual of fluorosilane molecules and to ensure that a monolayer is assembled. Then droplets of epoxy are dispensed on the edge of the sample, and a piece of glass substrate, which is washed **by** detergent, deionized **(DI)** water, acetone and IPA beforehand, is put on top of the sample. Capillary force will make the epoxy spread inside until the gap between the two substrates is filled up **by** epoxy. Then the sample is put inside another desiccator under vacuum for **30** min to 1 h to obtain a uniform epoxy layer. To make sure the epoxy wets the nanogaps between electrodes well, it is required that the flowing direction of epoxy should be controlled along the length direction of the nanogaps. Otherwise, bubbles are likely to be trapped inside the gap, which leads to broken electrodes after peeling (as shown in Figure **3-6).** After spreading the epoxy, the sample is put under a **100** W **UV** lamp for **30** min to cure the epoxy. An extra annealing step at **60 'C** for 2 h is suggested to further enhance the adhesion between epoxy and Au electrodes. The next step is to use a razor blade to separate the laminated sample, starting from the corner. An ultra-thin razor blade is favorable since it can cleave the laminated substrates without causing a large shear stress which may tear the electrodes. After this step, the Au electrodes are transferred onto the glass substrate **by** epoxy.

The ideal case is that graphene is left behind after peeling if its adhesion to the initial substrate is good enough; however, it is more likely that the graphene is partially peeled **by** the epoxy, which will block the subsequent self-assembly of molecules onto the Au electrodes and even short the electrodes. Therefore, an additional etching step is required to remove the residual of graphene attached to the electrodes. The sample is put inside an oxygen plasma cleaner for **30** s, and then rinsed in ethanol and **DI** water to clean the surface of the electrodes. The specific time for plasma treatment



Figure **3-6:** Atomic force microscopy (AFM) image (topology) of broken electrodes after peeling due to existence of bubbles inside the nanogaps.

may vary for different cleaners. The basic rule is that the etching time should be long enough to completely remove the graphene monolayer, while at the same time prevent the sample from overheating.

The developed peeling technique achieves sub-nanometer roughness of the bottom electrodes, which is discernible **by** comparing the atomic force microscopy (AFM) figures of the evaporated bottom electrodes in Figure **3-7** (a) and the peeled bottom electrodes in Figure 3-7 (b). The RMS roughness of the selected region  $(200 \text{ nm} \times$ 200 nm) on the evaporated electrodes is measured to be **2.58** nm, while the roughness for the peeled electrodes in Figure 3-7 (b) is only 0.437 nm. Moreover, a  $\sim$ 6 nm recess at the two gates is observed from the measured height (Figure **3-7** (c)) of the section along the dashed line in Figure **3-7 (b).** Such a large recess is a little unexpected, for the thickness of a monolayer of graphene should be  $0.4 \text{ nm} \sim 1.7$ nm [83]. It is probably because the graphene is not in intimate contact with the underlying substrate but the deposited Au is able to contact the substrate closely.



Figure **3-7:** (a) AFM image (topology) of evaporated bottom electrodes; **(b)** AFM image (topology) of peeled bottom electrodes; (c) height profile of the section along the dashed line on the peeled electrodes.

One explanation for this can be that the affinity between graphene and  $SiO<sub>2</sub>$  is not as high as that between Au and  $SiO<sub>2</sub>$ . Another explanation can be that the wrinkles formed during the transfer process result in tiny gaps between the graphene and the substrate. It is also noticed in Figure **3-7 (b)** that the epoxy region surrounding the electrodes was slightly rougher, because the sample was put into a strong oxygen plasma cleaner to etch graphene residue away. Without this step, the epoxy should have the same roughness as that of the electrodes, since both of them are defined **by** the smoothness of initial substrate. More examples of peeled electrodes with various designs are presented in Figure **3-8.**

**A** more versatile alternative peeling technique, suitable for non-Au electrodes, is also introduced here, which excludes the **SAM** anti-stiction coating and relies on a large enough graphene monolayer (or other **2D** that can be easily etched) as the release



Figure **3-8:** AFM images (topology) of peeled bottom electrodes including (a) design **A** and **(b)** design **C.**

layer. Without any **SAM** pretreatment for the sample, epoxy is directly dispensed **on** the edge of graphene and a glass receiving substrate smaller than the graphene monolayer is put on top. The following steps for spreading, curing and annealing epoxy parallel those introduced for the basic peeling technique. It should be much easier to separate the laminated sample afterwards since the whole receiving substrate with epoxy underneath lies on the graphene area, which makes the top substrate easier to release.

For comparison, samples with **Al** gate electrodes were peeled **by** the basic peeling technique and the alternative peeling technique, shown in Figure **3-9** (a) and **(b),** respectively. It can be observed that the **Al** electrodes were successfully peeled **by** the alternative process instead of the basic process. The failure of the latter is attributed to the extra **SAM** coating step, which inadvertently functionalizes the surface of **Al** electrodes and makes them hard to **peel.** The alternative peeling technique is believed to be capable of transferring all kinds of metallic electrodes and even non-metallic patterns to achieve sub-nanometer surface roughness.

The yield for pattern transfer with the developed basic or alternative peeling technique is usually influenced **by** a few considerations.

First, the electrode material is crucial. Ai is selected for squitch designs because of its good stability and well-characterized features for self-assembly; however, the



Figure **3-9:** Bottom Au source/drain electrodes and **Al** gate electrodes transferred **by** (a) the basic peeling technique and **(b)** the alternative peeling technique.

adhesion between Au and epoxy is usually weak, which is also the case for other noble metals, e.g., Pt. As a result, the electrodes are likely to break at those tiny patterns, where the weak adhesion and limited contact area lead to insufficient adhesive force to detach patterns from the initial substrate. Such an issue can be mitigated **by** using non-noble metals in the design if possible.

Second, the design of the electrodes can be critical. In general, long and thin electrodes are brittle, and connectors with abrupt changes in width should be avoided, for they are vulnerable to shear stress. Besides, epoxy cannot wet a narrow but long nanogap well even under a high vacuum condition, which makes nanogaps with aspect ratios over **50:1** unfavorable in design. Another design consideration is specific for the alternative peeling process. Since epoxy sticks to  $SiO<sub>2</sub>$  without the SAM treatment, the etched graphene region should be designed smaller than the electrodes deposited afterwards in order that epoxy will not directly contact  $SiO<sub>2</sub>$  during the peeling step. It will help reduce the local shear stress and thus ensure the completeness of the tiny electrodes.

Third, bubbles should be minimized in order to obtain a high yield. There are multiple reasons that might lead to bubbles trapped inside the nanogap. In general, bubbles stem either from evaporation of solvent inside epoxy or from trapped air while dispensing the epoxy on the sample. These bubbles can be removed afterwards, with difficulty, when the sample is put inside vacuum to spread the epoxy. The direction
that epoxy flows turns out to be significant. It has been proven that fewer bubbles are trapped inside nanogaps when the epoxy flow is oriented parallel to the length direction of the nanogap compared with a perpendicular orientation. In addition, **SAM** coating is also influential. **If** more than a monolayer is assembled, it will add difficulty to the spreading of epoxy into the nanogaps and therefore bubbles are more likely to be left inside the gap.

With efforts made on all these aspects, the overall yield of the peeling step with the basic process can be controlled within  $60\% \sim 100\%$  range, and that with the alternative process is even higher, over **90%.**

# **3.4 Self-Assembly of Molecular Layer On Bottom Electrodes**

The self-assembly step deposits a monolayer of molecules with a specific chain length onto the bottom electrodes and thereby defines the thickness of the tunneling junction for the squitch. Compared with previous steps, the self-assembly is straightforward, while a few considerations must be discussed to ensure a good assembled molecular spacer.

Since Au is used as electrodes in the squitch, molecules with thiol end groups are used to obtain Au-S bonds. Besides, it is also required that the molecules should not be too stiff to compress. Therefore, **PEG-SH** or **HS-PEG-SH** are selected, considering that PEG-thiol molecules with different molecular weights are commercially available. It should be noticed that PEG-thiol molecules may not constitute good candidates for real applications, since these molecules are sensitive to temperature, light, moisture, etc. and are easily oxidized as well. Though encapsulation is capable of isolating the device from ambient environment  $(O_2, \text{ moisture and light})$ , severe joule heating inside the metal-molecule-metal junction during device operation may degrade or even burn out the PEG-thiol molecules. Though not excellent for applications, PEG-thiol molecules are decent for research purpose and proof of principle.



Figure **3-10:** TEM image of a Au nanorod assembled with a monolayer of **5k** MW **PEG-SH** molecules.

The thickness of the molecular spacer depends on the chain length of PEG-thiol molecule, which is primarily decided **by** its molecular weight (MW). **A** tunneling electron microscopy (TEM) image (Figure **3-10)** of a Au nanorod surrounded **by** a monolayer of **PEG-SH** molecules (MW: **5k)** shows a thickness of **5.5** nm for the assembled molecular layer. However, such a thickness corresponds to a resting molecular layer. Though not well-characterized, the actual thickness of the junction is believed to be slightly smaller, for van der Waals force will pre-compress the molecules. **A** larger molecular weight of **PEG-SH** or **HS-PEG-SH** is able to bring about a larger thickness, but such an increase will be very small for molecular weight over **5k.** It can be attributed to the fact that the chain of large molecule is not straight and that molecules will intertwine during the assembly process. However, assembling molecules on both bottom electrodes and nanorod can effectively bring about increased junction thickness and more densely packed molecules.

**A** standard way to assemble PEG-thiol molecules onto the bottom electrodes is introduced as follows. The sample with peeled bottom electrodes should first be rinsed in ethanol, **DI** water and then dried **by** a stream of nitrogen. Fresh **5** mmol/mL (mM) **PEG-SH** molecules (MW: **5k)** in **DI** water is prepared and stored in a glass vial. The sample after cleaning is then put in and completely soaked **by** the PEG solution. In order to minimize oxygen exposure, dry nitrogen should be backfilled into the vial, which is then sealed **by** parafilm. The self-assembly process usually takes over 12 h, and a longer time usually leads to a denser molecular layer. To terminate **SAM** assem**bly,** the sample should be rinsed in DI water for **15** s before drying with nitrogen flow. The **DI** water is suggested as the solvent for assembly because **PEG** with a molecular weight as high as **10k** can easily dissolve therein. 200 proof ethanol is another solvent option for self-assembly of PEG-thiol molecules, while an extra sonication step is required and a small amount of DI water is usually added to completely dissolve the large PEG-thiol molecules. For **SAM** assembly on Au nanoparticles, additional stirring during assembly is essential to prevent agglomeration of nanoparticles.

For the standard PEG-thiol self-assembly process, two concerns are significant for obtaining well-assembled monolayer.

The first concern is the cleanness of the surface of Au electrodes, which is a prerequisite for **SAM. A** typical problem is that organic nanoparticles may be seen on the peeled electrodes after peeling and plasma cleaning, as shown in Figure **3-11** (a). Such an issue is usually encountered when the sample is put inside a very high vacuum for a long time during the peeling step. In that case, the epoxy tends to penetrate underneath the graphene, and subsequently covers the graphene on top after peeling (Figure **3-11 (b)).** Oxygen plasma treatment that follows will attack the cured epoxy and leave organic nanoparticles attached to the surface of the electrodes. The contaminated surface is found extremely difficult to clean. Extra time of plasma cleaning and an additional rinsing step turn out to be insufficient to remove these particles. To avoid this issue, both vacuum level and time under vacuum for spreading epoxy must be well-controlled, and a good adhesion between graphene and  $Si/SiO<sub>2</sub>$ substrate assists in preventing the penetration of epoxy.



Figure **3-11:** (a) AFM image (topology) of peeled bottom electrodes (after plasma cleaning) contaminated **by** organic nanoparticles; **(b)** AFM image (phase) of the same bottom electrodes after peeling but before plasma cleaning.

Cross-contamination is another concern. **If** a sample is peeled **by** the basic peeling technique introduced above, an anti-stiction **SAM** coating with fluorosilane will be utilized. Since silane compounds can easily contaminate various surfaces, an extra rinsing step with ethanol is essential to make sure that fluorosilane molecules attached to epoxy after peeling get washed away. In comparison, the alternative peeling process is free from such an issue **by** avoiding any usage of silane molecules.

# **3.5 Dielectrophoretic Trapping of Nanoparticles as Top Electrode**

The last step to fabricate a squitch is to position **by** the dielectrophoretic trapping approach a single Au nanorod so as to bridge the source electrode and the drain electrode. To implement such a method, a droplet of nanoparticle suspension is dispensed onto the sample and an **AC** voltage signal is subsequently applied across the electrodes where the nanoparticles are supposed to land. However, it turns out that this straightforward fabrication step is the most challenging one and directly limits the overall yield of the batch of devices on a sample.

In order to achieve consistency in performance among devices, it is required that

a single Au nanorod be precisely positioned across the source electrode and the drain electrode. The dielectrophoresis force induced for a cylindrical-shaped nanoparticle is given **by [71,72]**

$$
\vec{F}_{DEP} = \frac{\pi d^2 l}{8} \varepsilon_1 Re \left( \frac{\varepsilon_p^* - \varepsilon_l^*}{\varepsilon_l^* + (\varepsilon_p^* - \varepsilon_l^*) L} \right) \nabla E^2,\tag{3.1}
$$

$$
\varepsilon_p^* = \varepsilon_p - i\frac{\sigma_p}{\omega}, \quad \varepsilon_l^* = \varepsilon_l - i\frac{\sigma_l}{\omega}, \tag{3.2}
$$

where *d* and *l* are the diameter and the length of the cylindrical nanoparticle, respectively,  $\varepsilon_p^*$  and  $\varepsilon_l^*$  are the complex dielectric constants of the nanoparticle (indexed by *p*) and the surrounding liquid media (indexed by *l*), respectively,  $\sigma_p$  and  $\epsilon_p$  are the corresponding conductivity and real part of dielectric constant of the nanoparticles, respectively,  $\sigma_l$  and  $\varepsilon_l$  are the conductivity and real part of dielectric constant of the liquid media, respectively, *E* is the applied electric field and *L* is a depolarization factor, defined **by**

$$
L \approx d^2/l^2[\ln(2l/d) - 1].\tag{3.3}
$$

It can be observed that the driving force for nanoparticle deposition is not only determined **by** properties of the nanoparticle and the liquid media, but also influenced **by** multiple external factors. For instance, the shapes of electrodes as well as the applied voltage determine the electric field distribution and thereby influence the dielectrophoresis force. The frequency of the applied voltage signal also has an effect on the dielectrophoresis force, considering the frequency-dependent complex dielectric constants of the nanoparticles and the liquid media in Equation **3.2.**

Though the dielectric field across the electrodes may be weakened after a nanoparticle gets trapped, the high resistance of the active area, arising from the two ohmic contacts between the nanoparticle and the electrodes, still maintains a large electric field distribution between electrodes, which leads to continuous trapping of additional nanoparticles onto the same gap over time. **A** typical method to prevent trapping multiple nanoparticle is to employ an external resistor with an appropriate resistance connected in series with the electrodes. Such an idea is illustrated **by** the equivalent

circuit in Figure **3-12** (a). When no nanoparticle is trapped, the resistance of the gap between the trapping electrodes is infinite and reactance of the nanogap is huge. Consequently, all the voltage is applied across the gap between electrodes. After a single nanoparticle bridges the gap, the resistance of the active area is reduced to a value much lower than that of the external resistor. In this case, the majority of the applied voltage is transferred to the external resistor and the electric field across the gap between trapping electrodes is too weak to overcome the Brownian motion of the nanoparticles, which prevents the trapping of a second nanoparticle onto the gap.

Though such a method may be effective for various contact-mode **NEM** switches, it is not suitable for fabrication of squitches, which are intrinsically tunneling devices. For a squitch, after a Au nanorod is trapped onto the electrodes with a self-assembled molecular layer on the surface, the resistance should be well above the gigaohm level considering the noise-level leakage current from tunneling. Though the simultaneous change in capacitance will result in a lower reactance and thus a lower impedance of the active area after trapping, the impedance should still be  $100 M\Omega \sim 1 G\Omega$  level for a typical squitch. Even if a high enough resistance is available, the resistance of the nanoparticle suspension itself will fail such an idea, which will be discussed in detail below.

The equivalent-circuit illustration for tunneling device fabrication with an external resistor is shown in Figure **3-12 (b).** The equivalent capacitance of the active area immersed in nanorod suspension but before trapping a nanorod is calculated to be  $7.08 \times 10^{-17}$  F, when the total width of nanogaps, the thickness of electrodes and the overlap in length between adjacent electrodes are assumed as **500** nm, **100** nm, and **500** nm, respectively. After a Au nanorod is trapped, the total overlap area of the two junctions is assumed to be 1  $\mu$ m × 60 nm, and the tunneling gap is around 5 nm. The relative dielectric constant for the junction should be a weighted average of that for the PEG-thiol molecule  $(\varepsilon_{r-PEG} = 3 \sim 5)$  and that for DI water  $(\varepsilon_{r-DI} = 80)$ , assumed to be 20. The corresponding capacitance of the device immersed in the suspension with a nanorod trapped is calculated to be  $2.13 \times 10^{-16}$  F, 30 times the initial capacitance value. As a result, the impedance for the active area on the device at an applied



Figure **3-12:** Schematic and equivalent circuit representations of dielectrophoretic trapping process for (a) contact-mode devices with external resistors, **(b)** tunneling devices with external resistors and (c) tunneling devices with on-chip capacitors.

frequency of 1 MHz will change from  $2.2$  G $\Omega$  to 73.3 M $\Omega$  after a Au nanorod lands. However, the resistance of 10  $\mu$ L droplet of the Au nanorod suspension dispensed on a glass slide is measured **by** multimeter to be 4.2 **MQ,** while the resistance for the same amount of **DI** water is measured to be 4.3 **MQ.** As a result, the overall resistance of the active area on device immersed inside the droplet of nanoparticle suspension (i.e., parallel branches in the equivalent circuit of Figure **3-12 (b))** remains unchanged at  $\sim$ 4 M $\Omega$ , even though over an order of magnitude change in impedance happens at the gap of electrodes. As a result, the electric field distribution is almost the same before and after trapping a single nanoparticle regardless of any resistance in series, which leaves no design space for the external resistor. To address such an issue, a novel approach for trapping is proposed here, which is not only suitable to contact-mode devices but effective for tunneling devices as well.

In the proposed trapping approach, a patterned capacitor is connected in series with the nanogap between the electrodes for trapping. The capacitor in principle functions in the same way as the external resistor, since the voltage distribution across a branch is decided **by** the impedance of components in series at an applied **AC** voltage. Since the bottom electrodes with nanogaps in between (i.e., the active area) intrinsically form capacitors in series, the voltage distribution is primarily determined **by** the ratio between the capacitance value of the active area and that of the patterned capacitor in series, regardless of the frequency applied. Therefore, over an order of magnitude change in capacitance will provide enough design space for the capacitor in series, which helps trap only a single nanoparticle. The effectiveness of the proposed method for squitch fabrication is discussed **by** equivalent circuit modeling as well. Since the patterned capacitor lies close to the active area, the dispensed nanorod suspension will cover both of them, resulting in a 4 **MQ** resistor in parallel with the whole branch rather than only the active area, as shown in Figure **3-12** (c). Besides, two additional resistors  $R_{\text{DI}-\text{dev}}, R_{\text{DI}-\text{C}}$  (not shown in Figure 3-12 (c)) should be added in parallel with the active area and the patterned capacitor considering the dielectric polarization of **DI** water. These resistances can be evaluated **by**

$$
R_{\text{DI}-\text{dev}} = \frac{\rho_{\text{DI}}\varepsilon_{\text{DI}}}{C_{\text{dev}}}, \quad R_{\text{DI}-\text{C}} = \frac{\rho_{\text{DI}}\varepsilon_{\text{DI}}}{C_{\text{C}}}, \tag{3.4}
$$

where  $C_{\text{dev}}$  and  $C_{\text{C}}$  are the capacitance of the device and the patterned capacitor, respectively,  $\varepsilon_{\text{DI}}$  and  $\rho_{\text{DI}}$  are the dielectric constant and the resistivity of DI water, corresponding to values of  $80 \times 8.854 \times 10^{-12}$  F/m and 18.2 M $\Omega$ -cm, respectively.

 $R_{DI-dev}$  is calculated to be 1.82 T $\Omega$  before trapping a nanorod, which can be neglected compared with the impedance of the active area. Similarly,  $R_{\text{DL-C}}$  can be ignored compared with the impedance of the patterned capacitor. As a result, the proposed approach does not suffer the issue that the conventional method involving an external resistor has. In order to evaluate the effect of the patterned capacitor for trapping, we assume the same change (i.e., **30** times) in capacitance as discussed above. **If** a patterned capacitor is designed to have a capacitance three times as much as that of the active area without nanorod, **75%** of the applied voltage will be on the active area for trapping. After a single nanorod bridges the electrodes, the voltage on the active area will be drastically reduced to only **8.9%** of the source voltage. The greatly weakened electric field and thus reduced dielectrophoresis force prevent trapping more nanorods onto the same spot provided that the voltage for trapping is not too large.

The underlying principle determines that the proposed trapping approach is suitable for the fabrication of both contact-mode and tunneling devices that demand single nanoparticle. Besides, the capacitors can be easily patterned and integrated, making them viable for many processes with which resistor fabrication is not compatible. Moreover, the proposed approach makes nanoparticle-based device fabrication scalable. When arrays of bottom electrodes, each with a patterned capacitor in series, are connected in parallel to the voltage source, the trapping process for each device is independent. Namely, the landing of a nanoparticle on the device in one branch will not affect the voltage distribution on other branches. As a result, hundreds, thousands or even millions of devices in parallel can be trapped simultaneously, which makes the fabrication **highly** efficient. Considering that the patterned capacitors are not part of the eventual circuit, they will be removed (e.g., **by** etching) upon completion of the trapping process. The experimental results of scalable fabrication based on the proposed trapping approach will be presented in the next chapter.

Whatever trapping approaches adopted, conditions are very crucial to the yield. The critical conditions include concentration of the nanoparticle suspension, voltage and frequency of the trapping source, and the trapping time. Since these four factors combined to influence the trapping process, it is difficult to predict the optimal combination of conditions for trapping. In other words, there may be multiple options that lead to the same trapping result. In general, nanoparticles are more likely to be trapped onto the bottom electrodes when the concentration of suspension is high. **A** higher applied voltage brings about stronger electric field, and thus a larger dielectrophoresis force. The frequency is also important. When the other three factors are kept constant, a higher frequency leads to more nanorods trapped along the field orientation due to the increased dielectrophoresis force. **If** the concentration of suspension is high and dielectrophoresis force is large, the trapping time should be limited in order to prevent multiple nanoparticles trapped. Though patterned capacitor is able to greatly reduce the dielectrophoresis force after trapping the first nanoparticle, additional ones may be trapped over time if the applied voltage is so high that the dielectrophoresis force is still large enough to overcome Brownian motion. For squitch fabrication, a relatively long handling time is preferred. Therefore, a diluted nanorod suspension and a long trapping time are utilized. For the voltage source, the applied voltage should be low in order to protect the tunneling junction after trapping, and a high frequency is used to obtain a strong enough dielectrophoresis force. The specifics of the trapping step with detailed conditions are presented as follows.

For squitch fabrication, commercial Au nanorod suspension from Nanopartz, Inc. is utilized. Au nanorods with an average length of  $1 \mu m$  and a concentration of **0.05** mg/mL are encapsulated **by 50** mM cetyltrimethylammonium bromide (CTAB). Therefore, the first step is to remove the CTAB both inside the suspension and on the surface of Au nanorod. To wash the Au nanorods,  $100 \mu L$  original suspension is added into a centrifuge tube and diluted by 200  $\mu$ L DI water. Then the tube is centrifuged at 2000 rpm for **15** min. The supernatant should be carefully removed and 200  $\mu$ L DI water is added into the tube to re-suspend the sediment. The suspension should be mixed well **by** pipette and sonicated for **10** s. Another centrifugation step is optional, which will collect less but cleaner Au nanorods. If self-assembly of **PEG**thiol molecules onto the Au nanorod is necessary, the liquid media in the suspension should be replaced **by** 2 mM PEG-thiol solution and stirring at 200 rpm for **8** h. Then the Au nanorod suspension is washed **by** the same step as described above.

After preparing the Au nanorod suspension, the sample with assembled PEG-thiol molecules on the bottom electrodes is put on the stage of a probe station. The probe tips should be in good contact with the source and drain electrode pads for trapping. **10** puL prepared suspension is dispensed on the sample with micropipette. Then a  $2 V_{\text{pp}}$ , 1 MHz voltage signal, which has been proven as a combination of conditions effective for a wide variety of fabricated devices, is applied and maintained for 2 min before terminating the process. The sample can be dried naturally or **by** a gentle stream of dry nitrogen. After the sample gets totally dried, a careful rinse in **DI** water is suggested to further remove residue of molecules (CTAB or **PEG)** on the sample. After these steps, the fabrication of a squitch is completed. **SEM** images of two fabricated squitch devices are presented in Figure **3-13.** The first one has **All** Au bottom electrodes, and the second one has Au source and drain electrodes and two **Al** gate electrodes.

The yield for dielectrophretic trapping is constrained **by** a few challenges. First, the quality of the nanorod solution is significant for the success of trapping a single nanorod. Though short nanorods can be made relatively consistent, nanorods as long as  $1 \mu m$  are in general nonuniform in length (as observed in Figure 3-14 (a)). If all the nanorods distributed near the bottom electrodes are not long enough, the electric field will not be weakened after the first nanorod gets trapped. As a result, multiple nanorods will be trapped but none will bridge the source electrode and the drain electrode, as shown in Figure 3-14 **(b).** Even though a single nanorod is achieved, it is still likely that the nanorod may not be long enough to make a good squitch, as presented in Figure 3-14 **(c).** Miniaturized bottom electrodes enable shorter and



Figure **3-13:** (a) **A** fabricated four-terminal squitch based on all Au bottom electrodes; **(b)** a fabricated four-terminal squitch based on Au source/drain electrodes and **Al** gate electrodes. The scale bars correspond to 1  $\mu$ m.

thus more uniform nanorods as the top electrodes, but it can be difficult to peel the tiny electrodes and in consequence the overall yield still remains low. To address this issue, length separation with extra sorting steps can be helpful, if possible.

Second, nanorods can agglomerate easily. The nanorods are usually encapsulated **by** CTAB for storage, and the surfactants keep the nanorods monodispersed. However, when nanorod suspension is prepared for trapping, the first step is to remove the CTAB inside the original suspension and also on the surface of nanorod. The nanorods tend to agglomerate during centrifugation, while subsequent washing and sonication are usually incapable of re-suspending the agglomerated nanorods due to lack of surfactants on the nanoparticle. When such nanorod suspension is utilized, an aggregate of nanorods is likely to get trapped onto the bottom electrodes, as shown in Figure 3-14 **(d).** Moreover, if additional **SAM** coating on the nanorod is needed, the agglomeration issue will be exacerbated, for nanorods can also aggregate during the assembly process. As a comparison, **SEM** image of a device made with nanorod suspension after **SAM** assembly is shown in Figure 3-14 (e). To address this issue, the prepared nanorod suspension can be filtered by a syringe filter with a 1.2  $\mu$ m or 1.5  $\mu$ m pore size. It should be noticed that the concentration of nanorods in suspension can be greatly reduced after filtering. Therefore, the suspension should be prepared more concentrated at the beginning.

The third challenge originates from the strong capillary force experienced **by** the



Figure 3-14: (a) Au nanorods nonuniform in length; **(b)** a failed squitch device with multiple short nanorods trapped; (c) a failed squitch device with a single short nanorod trapped; **(d)** a failed squitch device that trapped an aggregate of nanorods from washed suspension; (e) a failed squitch device that trapped an aggregate of nanorods from suspension after **SAM; (f)** a failed squitch device with dislocated nanorod due to significant capillary force when the suspension dries; **(g)** a failed squitch device with nanorod washed away **by** significant capillary force when the suspension dries; The scale bars correspond to 1  $\mu$ m.

nanorod when the suspension dries on the sample. When the edge of suspension moves across the active area of bottom electrodes, the trapped nanorod can be misaligned (Figure 3-14 **(f))** or even washed away (Figure 3-14 **(g)).** Such an issue can be difficult to deal with. One possible solution is to add some ethanol inside the nanorod suspension. The ethanol mixes well with **DI** water, and contact angle of the modified suspension droplet becomes much smaller than that with pure **DI** water as the solvent for suspension. As a result, the capillary force is greatly reduced. However, the ethanol added inside tends to make nanorods agglomerate more easily. It is suggested that the nanorod suspension be freshly prepared with a low concentration before use.

Though the aforementioned approaches are able to increase the possibility of successfully aligning a single nanorod on the electrodes, the improvement in yield is still limited, and a high quality suspension containing monodispersed nanorods with uniform lengths is in acute demand in order to obtain a high yield. The yield for the dielectrophoretic trapping step in the nanofabrication of a multi-terminal squitch is still under estimation.

#### **3.6 Summary**

The process of making a squitch device combines top-down and bottom-up nanofabrications. Except for the electron beam lithography and self-assembly techniques that have been widely used to fabricate nanostructures, novel approaches for pattern transfer and precisely positioning single nanoparticles have been developed. It is noteworthy that these two techniques are not just intended for squitch fabrication but can be versatile to a good variety of devices.

Challenges are encountered in each fabrication step, and considerations that are critical to yield control have been discussed. At present, a high overall yield for squitch fabrication is still challenging. In particular, the precise alignment of a single Au nanorod greatly relies on the quality of the suspension, making the advancement in this field imperative.

# **Chapter 4**

# **Experimental Squitch Results**

### **4.1 Scalability of Squitch Fabrication**

As described in the previous chapter, four separate steps that are required to fabricate a squitch include patterning bottom electrodes using lithography, pattern transfer **by** a peeling technique, self-assembly of the molecular spacer, and positioning of the top electrode with dielectrophoretic trapping. In making the squitch fabrication scalable, the most challenging step is the dielectrophoretic trapping, as manipulation of individual nanoparticles to make a large number of devices at the same time can be demanding. Therefore, a novel scalable trapping approach based on a patterned capacitor connected in series to each device allows for alignment of a single nanoparticle on each pair of electrodes, that is for the batch fabrication of devices. With this newly developed approach, the entire fabrication process of the squitch can be scalable. Moreover, this approach is believed to be versatile, hense applicable to a variety of devices beyond the squitch, which will enable massive production of nanoparticlebased devices in a **highly** efficient way. In this section, the developed dielectrophoretic trapping technique will be applied to arrays of two-terminal devices under different conditions, and experimental results will be presented to verify the effectiveness of the proposed technique and thereby the scalability of the squitch fabrication.

**A** sample with hundreds of pairs of two-terminal electrodes on quartz is prepared in advance to test the proposed trapping approach. To make such a sample, electron

beam lithography technique is used; however, the patterning step is slightly different due to the quartz dielectric substrate in use. First, bilayer MMA copolymer/PMMA resist are spin-coated on quartz substrate in the same way as describe in Chapter **3.** Then a **5~10** nm-thick Cr layer is deposited on top of the resist **by** thermal evaporation; such a metallic layer is utilized to help dissipate charge during the electron beam lithography. In order to make sure the sample is well grounded during lithography, the edge of the Cr layer should be clamped **by** a small clip connected to the stage. A 2 nA beam current and an area dose of 1400  $\mu$ C/cm<sup>2</sup> are adopted for patterning the small two-terminal electrodes. After lithography, the Cr layer should be removed before development. To do so, the sample is put in Cr7, a typical Cr etchant, for **30 s,** rinsed in **DI** water and dried with nitrogen flow. Then the sample is developed in **1:3** MIBK:IPA developer for **90** s. For metal deposition, a **10** nm Cr is evaporated as an adhesion layer underneath **80** nm Au. After evaporation, the sample is put in acetone for over **8** h to finish the lift-off process. The as-fabricated sample is presented in Figure 4-1 (a). There are 540 sets of electrodes patterned on the sample, which are divided into **9** regions to try different trapping conditions. For each region, all the branches, each comprising a set of electrodes and a capacitor in series (as shown in Figure 4-1 **(b)),** are connected in parallel. The capacitance of the capacitor that enables trapping single nanoparticle can be designed within a pretty wide range, typically varying from twice to **9** times the capacitance of the corresponding electrodes for trapping, and a ratio of **5** is mostly adopted.

The Au nanorod suspension is prepared in a similar fashion as that for squitch fabrication. To ensure monodispersed nanorods in the suspension, the Au nanorods are only washed for once, and re-suspended **by** pure **DI** water and no ethanol. For the purpose of comparison, some suspension is taken out and filtered **by** syringe filter with a 1.2  $\mu$ m pore size. The former suspension is referred to as the "unfiltered" suspension and the latter is referred to as the "filtered" suspension for the purpose of comparison. For convenience, electrodes are not peeled and PEG-thiol molecules are not assembled onto the electrodes. As a result, these devices will be in the contact-mode rather than tunneling mode after trapping nanoparticles on them. To test scalability



Figure 4-1: (a) Microscopic image of the testing sample fabricated on quartz substrate **(b) SEM** image of a pair of two-terminal electrodes with a patterned capacitor connected in series. The scale bar corresponds to  $100 \mu m$ .

of the proposed trapping approach, experiments with various combinations of testing frequency and voltage have been conducted. For most conditions, both the unfiltered suspension and filtered suspension were employed for comparison. The testing frequency was varied from **10** kHz to 1 MHz and the peak value of the testing voltage was selected among **0.5** V, 1 V, **1.5** V, 2 V, **3** V. The trapping time was carried out over 2 min for all conditions. After terminating the trapping process, the sample was imaged **by SEM** to check how each device looked. The trapping yield is determined **by** the cooperative effect from factors including nanorod suspension, voltage, frequency, and trapping time. According to the **SEM** images, a few comparisons can be made, which indicates how each factor influences the trapping yield.

**A** first comparison considers the nanorod suspension, and the difference can be observed from Figure 4-2. The left one and the right one correspond to the unfiltered suspension and the filtered suspension, respectively. The other conditions for trapping are consistent, i.e., **50** kHz, **1** V voltage applied for 2 min. Figure 4-2 (a) shows a device with multiple nanorods trapped on the electrodes, which represents the typical case for the sample with unfiltered suspension. In comparison, a good number of devices that trapped a single nanorod (shown in Figure 4-2 **(b))** were obtained



Figure 4-2: Representatives of devices using (a) unfiltered nanorod suspension and **(b)** filtered nanorod suspension. The trapping condition was **1** V, **50** kHz for 2 min. The scale bars correspond to 1  $\mu$ m.

in a single batch fabrication **by** using the filtered suspension. The different results are attributed to the difference in concentration of the nanorod suspension. The prepared unfiltered suspension was concentrated, while the concentration was greatly reduced after filtering. As discussed in the previous chapter, though the electric field was weakened a lot after the first nanorod was trapped **by** using the capacitor in series, it is possible to trap additional nanorods onto the electrodes over time if the dielectrophoresis force is still high enough to overcome the Brownian motion. Such a process may happen slowly, but 2 min can be long enough, especially when the concentration of the suspension is high and many nanorods are thereby distributed close to the electrodes. In comparison, for the filtered suspension that has much lower concentration, a single nanorod is more likely to be trapped. Therefore, a diluted nanoparticle suspension combined with a sufficiently long trapping time is favorable for the scalable trapping approach.

**A** second comparison indicates how trapping frequency influences the dielectrophoretic trapping. Figure 4-3 presents the **SEM** images of three devices with consistent trapping conditions (unfiltered suspension used and 1 V voltage applied for 2 min) but different trapping frequencies. It is observed that an increasing number of nanorods have been aligned along the fringing field with the increase in trapping frequency, which is also partially due to the high concentration of nanorods in the unfiltered suspension. For diluted suspension, the strong dielectrophoresis force induced



Figure 4-3: Representatives of devices obtained **by** applying (a) **10** kHz, **1** V voltage for 2 min, **(b) 100** kHz, 1 V voltage for 2min, (c) **500** kHz, **1** V voltage for 2min. Unfiltered nanorod suspension was used and the scale bars correspond to 1  $\mu$ m.

**by** a high frequency will help attract those sparsely distributed nanoparticles inside suspension onto the electrodes. Therefore, the combination of a diluted nanoparticle suspension and a high frequency for trapping is able to provide both a long handling time and a good trapping yield, which makes it favorable for squitch fabrication.

The influence of voltage on the trapping process is also studied. The trapping frequency and time were set to be **500** kHz and 2 min, respectively, while the voltage was selected as **0.5** V, 1 V and **1.5** V for comparison. According to the results, most devices obtained with a **0.5** V trapping voltage had no nanorod on the electrodes, while a number of devices with single nanorod trapped (Figure 4-4 (a)) were achieved **by** a voltage of **1** V. The yield for these successful devices was further improved when the trapping voltage was raised to **1.5** V. On the other hand, devices with a second nanorod (shown in Figure 4-4 (b)) were observed among the devices obtained **by** a **1.5** V voltage, which was not seen for a **1** V voltage. These results



Figure 4-4: (a) **A** device with a single nanorod obtained **by** a **500** kHz, **1** V voltage applied for 2 min; **(b)** a device with two nanorods obtained **by** a **500** kHz, **1.5** V voltage applied for 2 min. Filtered nanorod suspension was used and the scale bars correspond to 1  $\mu$ m.

demonstrate that a higher voltage leads to an enhanced electric field and therefore a larger dielectrophoresis force for trapping.

For many conditions applied, there are successful devices with a single nanorod trapped and well aligned. Some are presented in Figure 4-5 with the trapping conditions marked on each figure. However, the yield for trapping can be a lot different, making some conditions outperform others.

The best way to find the optimal conditions is to investigate the yields obtained under different conditions statistically. The yields for some trapping conditions are summarized in Figure 4-6.

The cooperative effect from the nanoparticle suspension, trapping voltage and frequency can be identified, and it is noticeable that multiple optimal conditions may coexist. The best yield (20%) is obtained **by** both **1.5** V, **500** kHz and **1** V, **1** MHz, and the latter condition is used for squitch fabrication as well. Besides, devices with misaligned single nanoparticle due to the strong capillary force during drying, like that in Figure 4-7, were not counted. **If** these are seen as successful devices, the yield can be much higher. For instance, the yield for the **1** MHz, **1** V condition will be increased to over 40%. On the other hand, since the misalignment is caused **by** the strong capillary force, the yield is expected to increase **by** adding a certain amount of ethanol into the suspension. As a result, a **50%** yield can be accomplished with some



Figure 4-5: Successful trapping cases under different conditions. The scale bars correspond to 1  $\mu$ m.

optimizations and a better controlled trapping process. It should also be pointed out that only **60** devices were tested for each condition, which makes the statistical yield rough. Besides, the conditions tested are not exhaustive. These ask for a more sophisticated study in the future.

According to the experimental results presented above, the effectiveness of the developed trapping technique has been validated. As simultaneous nanorod positioning for many devices becomes viable, the squitch fabrication process is made completely scalable. More significantly, the proposed technique has opened up an opportunity



Figure 4-6: Statistical trapping yields for different conditions.



Figure 4-7: **A** two-terminal device with a misaligned nanorod due to strong capillary force during drying process. The scale bar corresponds to 1  $\mu$ m.

for the manufacturing of various devices involving nanoparticles to become scalable and **highly** efficient.

### **4.2 Experimental Results of Two-Terminal Squitches**

**A** two-terminal squitch can be seen as a simplified version of a multi-terminal squitch, since it eliminates the gate electrodes. The two terminal squitch works **by** the same principle as the multi-terminal squitch except that the actuation voltage is applied across the source electrode and the drain electrode rather than at the gate electrodes. As a result, the two terminal squitches should have characteristics similar to those of multi-terminal squitches, which makes investigation of two-terminal squitches interesting.

The fabrication of a two-terminal squitch is easier than making a multi-terminal squitch, for the graphene sacrificial layer is unnecessary. The two-terminal electrodes and capacitors in series designed for parallel trapping are patterned **by** electron beam lithography, and subsequently peeled **by** the developed peeling technique. After assembly of PEG-thiol molecules onto the electrodes, the Au nanorods from filtered suspension are trapped and aligned onto devices in parallel **by** a 1 MHz, 2 **Vpp** voltage. The **SEM** image of a fabricated two-terminal squitch is shown in Figure 4-8. Thanks to the peeling technique, the electrodes become much smoother than those unpeeled ones presented in the previous section. The smooth Au surfaces not only facilitate the assembly of PEG-thiol molecules but also bring about more uniform performance for devices from different batches.

To test a two-terminal squitch, an Agilent B1500 semiconductor parameter analyzer is utilized. The voltage is swept from **0** V to **5** V with a step of **50** mV, and then backwards. The compliance is set as  $1 \mu A$  to protect devices from damage caused by testing. Experimental results of devices with PEG-thiol (MW **10k)** are presented in Figure 4-9.

As observed from these results, the three devices except Device 4 exhibit similar IV curves with pull-in voltages around 2 V and release voltages around 1.2 V. For



Figure 4-8: **A** fabricated two-terminal squitch. The scale bar corresponds to **500** nm.

Device 4, the IV curve slightly deviates from the other three, and shows a **2.5** V pullin voltage as well as a 2 V release voltage, which corresponds to a hysteresis of **0.5** V. Compared with existing two-terminal **NEM** switches, low actuation voltages have been achieved **by** the squitches owing to the unique underlying working principle, i.e., modulation of a nanometer-scale tunneling junction rather than deflecting an active element **by** tens of nanometers or even more. In principle, squitches can be made hysteresis-free according to theoretical analysis in Chapter 2. However, the molecular layer may be reconfigured during compression and exhibit different elastic properties for the switch-on process and the switch-off process, which leads to a hysteresis. Even **so,** the sub-1 V hysteresis obtained **by** the compressible molecular spacer also makes squitch outperform most contact-mode **NEM** switches.

Pico-amp level leakage current is observed for all the devices in Figure 4-9, and a **3** orders of magnitude modulation in tunneling current can be extracted if we plot the blue curve in Figure 4-9 (a) on a log-log scale, as shown in Figure 4-9 **(b).** Considering that the compliance is set as  $1 \mu A$ , the actual modulation in current could be better. Since the pull-in happens at the starting point of abrupt change in the current, Devices  $1\sim 3$  show around two orders of magnitude on-off ratios, while



Figure 4-9: (a) Experimental results of two-terminal squitches based on **10k** MW PEG-thiol molecules; **(b)** Experimental result of Device **3** in a log-log plot with a resistive fit.

that for Device 4 is about three orders. It is expected the devices will show higher on-off ratios if the compliance is raised. The best subthreshold swing is measured to be **62.6** mV/dec obtained **by** Device **3.** Though not comparable to some contact-mode **NEM** switches, such a subthreshold swing is outstanding for a tunneling nanoswitch, and it has approached the limit value for semiconductor transistors, i.e., **60** mV/dec. Further improvement is possible according to the theoretical analysis conducted in Chapter 2.

Another batch of samples are fabricated using PEG-thiol molecules with a **5k** molecular weight. The same testing conditions are utilized except that the voltage is swept from **0** V to **3** V and then backwards. The experimental results are shown in Figure 4-10. The three devices also showed similar IV curves, with pull-in voltages around 2.2 V. For Device **1** and Device **3,** the release voltages are around **1.5** V, and therefore sub-1 V hysteresis has been achieved as well. The OFF-state tunneling current is still maintained at pico-amp level, while the on-off ratio and subthreshold swing seem not as good as those from the batch with **10k** MW molecules. This is probably because the PEG molecules with **5k** MW have shorter chain lengths and therefore were more densely packed on the Au surface, which might correspond to an elasticity similar to that described **by** a large parameter **p** in Equation 2.10. Besides,



Figure 4-10: Experimental results of two-terminal squitches based on **5k** MW PEGthiol molecules.

it is noticed that the pull-in voltages from the two batches are similar. This may arise from the similar thickness of molecular spacer and the resulting tunneling gap between the Au nanorod and the respective bottom electrode. This provides evidence to the assumption in Section 3.4 that the molecular layer will not be thickened **by** increasing the molecular weight if the chain is long enough.

IV curves for multiple operating cycles of a fabricated two-terminal squitch with **10** MW molecules are shown in Figure 4-11. **A** distinct pull-in behavior in the IV curve is only observed for the first cycle. For the subsequent cycles, the IV curve gradually moved to the left and no obvious pull-in behavior was observed for these cycles. This is probably attributed to reconfiguration of assembled molecular layer during each operation. After the first cycle, the molecular spacer was compressed and thereby became more densely packed and slightly thinner. For the following cycles, the molecular spacer became more and more compact, which provides higher and higher tunneling current at the same applied voltage and simultaneously increasing



Figure 4-11: Experimental results of a two-terminal squitch based on **10k** MW PEGthiol molecules over cycles of operation.

elastic restoring force at the same compression. Such a change in the elastic property of the molecular layer can be described **by** a larger parameter **p** in Equation 2.10. For the 5th cycle, the compliance was raised to 10  $\mu$ A. An abrupt change in the tunneling current happened at **1.75** V, but it should not be seen as a proper pull-in behavior, considering that the slope was too steep and no release occurred when the voltage was swept down to zero. Ohmic contact between the source electrode and the drain electrode was measured afterwards, suggesting the molecular spacer was destroyed during the 5th sweep. This constitutes a typical stiction failure for the two-terminal squitch and such an irreversible process is probably attributed to the severe joule heating inside the tunneling junction, sufficient to burn out the **PEG** molecules. In this case, a densely packed spacer based on stiff and thermally-stable molecules will be more resilient.

**<sup>A</sup>**similar failure mode is discernible from the IV curves (Figure 4-12) of another two-terminal device with assembled **5k** MW PEG-thiol molecules. **A** pull-in behavior



Figure 4-12: Experimental results of a two-terminal squitch based on **5k** MW PEGthiol molecules over cycles of operation.

is distinct in the first cycle, while the IV curves for the subsequent cycles suggest a potential change from tunneling to ohmic contact at the junction. Different from the stiction failure introduced above, the contact resistance is still high, implying the non-conductive PEG-thiol molecules were not burned out. **A** possible explanation for such an issue is that the characteristics of molecules might be changed during the first run, and the molecular spacer was not as compressible as that in the original state. Such an explanation can be justified **by** the sensitive feature of PEG molecules in use, and the molecules may deteriorate due to heating, accelerated oxidization, effect of moisture during the testing process. In this case, molecules with good heat resistance and stability are favorable, and device encapsulation may be necessary to reduce degradation of device performance over time **by** minimizing the exposure to air and moisture.

## **4.3 Experimental Results of Multi-Terminal Squitches**

Unlike two-terminal squitches, additional gate electrodes add more stochasticity to dielectrophoretic trapping process, resulting in a much lower yield for fabrication of a multi-terminal squitch. In order to test a sample, it is required to either test all the devices in sequence, or test the good devices that are sorted in advance. The latter option is more efficient, particularly when dielectrophoretic trapping for hundreds of devices on a sample simultaneously is enabled **by** the developed scalable trapping technique. However, sorting devices on a sample through a nonintrusive way can be difficult. The critical area of a squitch is usually smaller than  $2 \mu m$  by 500 nm, and a Au nanorod is thinner than **100 nmi.** As a result, it is impossible to check if a single Au nanorod lies on the tiny bottom electrodes **by** optical microscopes. Even under dark field, Au nanorods cannot be easily identified, for the bottom electrodes are also made with Au and the contrast in the critical area is bad. Therefore, the fabricated devices were sorted **by SEM** imaging before testing at the beginning.

To test the sorted devices, the gate voltage is swept from **0** V to **3** V with a step **of 10 mV,** while a **0.1** V **DC** voltage is applied at the drain electrode and the source electrode is grounded. Figure 4-13 (a) provides the experimental result of a sorted device. The IV curve is expected to show exponential increases for the source current and the drain current at small gate voltages, while the gate current maintains at the noise-level. However, the source current and the drain current started from **30**  $\mu$ A. Though pull-in behavior was observed at around 1 V, it cannot conceal the fact that the molecular spacer was damaged before testing. After testing a number of devices, it was found that **SEM** imaging could result in severe damages to the device, since the molecules tend to carbonize when high energy electrons are injected into the metal-molecule-metal junction. Therefore, sorting devices **by SEM** before testing cannot make a viable approach.

Besides, a more perplexing detail from the IV curve is that the gate current also exhibited an abrupt change until compliance was reached. According to the theoretical analysis, a suspended Au nanorod should not have enough deflection in



Figure 4-13: (a) Experimental result of a four-terminal squitch; **(b) SEM** image of the four-terminal squitch before testing; (c) **SEM** image of the four-terminal squitch after testing. The scale bars correspond to  $1 \mu m$ .

the center to contact the recessed gate. However, the high gate current indicates that the bottom gate electrodes and Au nanorod were in contact after the pull-in happened. The device was imaged again to find out what happened during the testing, but no significant difference can be recognized **by** comparing the pre-testing image in Figure 4-13 **(b)** and the post-testing image in Figure 4-13 (c).

Another batch of samples were tested without sorting devices in advance to ensure that the devices were free from damage. The testing conditions are similar to the



Figure 4-14: Experimental results of four-terminal squitches and **SEM** images of these devices after testing. (a) and **(b)** correspond to one squitch device, while (c) and **(d)** correspond to another one. The curve of the gate current  $I_g$  is on top of that of the source current  $I_s$  in (b). The curve of the gate current  $I_g$  is on top of that of the drain current  $I_d$  in (d). The scale bars correspond to 1  $\mu$ m.

previous setting, except that a **0.5** V **DC** voltage is applied at the drain electrode. After testing, the devices were imaged **by SEM.** The measurement results of two devices and their **SEM** images are shown in Figure 4-14. It is noticed from both IV curves that the pull-in happened between the gate electrode and the source/drain electrode, and that the tunneling current at the drain/source electrode was at noiselevel during the voltage sweep. Similar to the previous failed four-terminal squitch, no abnormities were discernible from the **SEM** images of both devices. This confirmed that such a failure mode, i.e., pull-in at the gate electrodes, did not happen **by** accident.

**A** possible interpretation is that the unexpected pull-in originated from the ex-



Figure 4-15: **SEM** image of a squitch with a peeled gate electrode after the Au nanorod on top of the squitch was washed away. The inset provides the corresponding IV curve of the squitch before the nanorod was washed away. The scale bar corresponds to 1  $\mu$ m.

cessive electrostatic force experienced **by** the gate electrodes. Though the deflection of the suspended Au nanorod is small, the counteracting electrostatic force may be large enough to peel the gate electrode towards the suspended Au nanorod in consideration of the poor adhesion between Au and epoxy. In particular, the electrostatic force at the edge of gate electrode can be significantly magnified **by** the fringe effect. As the edge of gate electrode only needs to move a few nanometers to contact the Au nanorod, such a tiny change is usually undetectable from **SEM** images. In this case, the pull-in process should resemble that for contact-mode **NEM** switches, which explains why the subthreshold swings were observed much better than those of the two-terminal squitches. **A** more direct evidence for the speculation is provided in Fig. 4-15, whose inset shows that a similar pull-in occurred at the gate of another squitch. When the Au nanorod on this device was washed away, one of the gate electrodes was peeled, which indicates that this gate electrode was previously in contact with the Au nanorod after testing.

**A** possible solution to this issue is adding some dielectric spacer onto the gate electrodes to prevent direct contact between the suspended nanorod and the gate electrodes. The spacer can be a monolayer of **2D** material or an ultra-thin layer of dielectrics. **h**-BN is known for its ideal dielectric property, and a simple implementation is to replace the graphene **by h-BN,** which does not need to be etched away after peeling. Nevertheless, **h-BN** must still be patterned at the first step to make sure the Au surfaces of the source electrode and the drain electrode are exposed after peeling for the PEG-thiol molecules to assemble on. The difficulty of etching **h-BN** without roughening the underlying surface decreases the suitability of **h-BN** as the dielectric spacer.

**A** more promising idea is to use non-noble materials to fabricate the gate electrodes. After peeling and plasma cleaning to remove graphene residue, the gate electrodes will be oxidized a bit to form an ultra-thin oxide layer as the dielectric spacer. This approach can be easily implemented with small modifications to the original fabrication process. Samples with **Al** gate electrodes have been fabricated, but no pull-in behavior at any electrode was observed even at a **10** V gate voltage. One possible interpretation is that the oxide layers of the gate electrodes were too thick and the gate control was greatly weakened **by** the drastically reduced electrostatic force. Another interpretation is that the surface of gate electrodes became very rough after oxygen plasma treatment. The nanorod was suspended **by** peaks on the gate electrodes. As a result, the suspended nanorod would not be able to squeeze the molecules attached to its two ends no matter how large the electrostatic force was. Even so, the effectiveness of preventing pull-in at the gate electrodes were still validated. When the sample was intentionally exposed under high-energy electrons for a long enough time to make sure the molecular layer was carbonized, the IV curves of devices previously without pull-in were measured again. The source electrode and the drain electrode were shorted after this treatment, while the gate current was still maintained at noise-level during the sweep. Therefore, it is believed that if the thickness of oxide layer is well controlled and surface roughening is minimized, such an approach will enable the success of four-terminal squitches.

#### **4.4 Challenges for Squitches**

Outstanding performance, including an ultralow OFF-state leakage and a small subthreshold swing, of the proposed squitches has been demonstrated **by** the preliminary experimental results of two-terminal squitches. However, great challenges block the route towards reliable operation of a squitch. In this section, failure modes encountered **by** both two-terminal squitches and multi-terminal squitches during operation will be summarized, which may provide some insights into device design towards robust squitches with outstanding performance.

When pure Au is utilized for the gate electrodes, the strong electrostatic force at a large gate voltage applied may peel the edge of the electrode to make contact with the suspended Au nanorod, resulting in an unexpected pull-in at the gate electrodes. This issue is largely due to the poor adhesion between the Au and epoxy. To ensure good adhesion, a large contact area between the gate electrodes and epoxy is recommended. Surface engineering is also capable of enhancing the adhesion of bottom electrodes, e.g., functionalizing Au surface **by** thiolated molecules with end groups that have good affinity with epoxy. Besides, an alternative material for the bottom electrodes may help from different aspects. Adhesion between a non-noble metal and the epoxy is generally better than that for Au, and the native oxide layer can function as a dielectric spacer when the non-noble metal is used for the gate electrodes.

Stiction between the nanorod and the bottom electrodes constitutes another typical failure for squitch operation, which might be caused **by** a poorly assembled molecular layer on the electrodes or excessive joule heating inside the tunneling junction. Besides, the molecular layer tends to reconfigure and its elasticity can be degraded after cycles of operation until it becomes completely non-compressible. Such a failure is also seen as "stiction", even though the high contact resistance makes it different from the typical cases with direct metal-metal contact. These issues are greatly dependent on the self-assembled molecular layer, and stiction-free design requires a well-controlled self-assembly process as well as compressible but robust molecules utilized inside the junction. Besides, designs with good heat dissipation are essential, which helps prevent the molecules from burning out **by** accumulative joule heating.

Except for destruction to the molecules inside junction, the accumulative joule heating is sometimes able to melt the Au nanorod in the middle, leading to the breakdown of a squitch. Such a failure mostly occurs when a high compliance (above 10  $\mu$ A) is selected. Therefore, reducing the compliance for testing to 1  $\mu$ A level can effectively avoid the issue of melted Au nanorod. For reliable operation of squitches, metallic nanoparticles that withstand high temperature are more favorable as the floating electrode.

In summary, the fabrication difficulties introduced in the previous chapter determine the yield for successful devices out of a batch, and the aforementioned challenges decide whether a fabricated squitch can operate reliably. These obstacles must be properly solved before squitches become viable candidates for ultra-low power digital computing.
# **Chapter 5**

### **Summary and Outlook**

### **5.1 Summary**

This thesis explores the opportunities of using electromechanical modulation of metalmolecule-metal junctions as the working principle to make a novel type of tunneling nanoelectromechanical switches (termed "squitches"), seeking to address significant challenges in device performance (e.g., actuation voltage, hysteresis, switching speed), reliability and scalability that conventional **NEM** switches are facing. To this end, a multi-terminal squitch design has been proposed and investigated, which is based on compressible molecules self-assembled between the bottom electrodes and a Au nanorod top electrode. Direct contact between the metal electrodes is avoided, which reduces the risk of stiction failure and promises low-hysteresis operation. Further, a sub-5 nm change in the thickness of the molecular layer is sufficient to make the drain-to-source tunneling current undergo a few orders of magnitude change, which thereby defines the transition between the ON-state and the OFF-state. For the same reason, the squitches promise low actuation voltages and high switching speeds due to the small displacement needed to switch on and off.

**A** theoretical model is established to study the statics and dynamics of a threeterminal squitch. The numerical simulation predicts a sub-i **pA** leakage current in the OFF-state when the molecular layer is designed to be over **5** nm thick. **A** 4 nm reduction in the thickness of the molecules will result in an over **7** orders of magnitude increase in the tunneling current, which defines transition to the ON-state as well as a sub-100  $k\Omega$  ON-state resistance. A 3 V actuation voltage has been demonstrated **by** the parameters selected for simulation, and optimization in the device structure and the molecules is possible to bring the actuation voltage down to sub-1 V level. Moreover, the steep subthreshold slope and the intrinsic low-hysteresis feature promise sub-100 mV operation of squitches when a proper body bias can be applied. **By** virtue of the small displacement needed to switch on and off, a squitch with a Au nanorod as the top floating electrode exhibits the potential to operate in the **100** MHz to 1 GHz regime, while further improvement in the operating frequency without sacrificing the low actuation voltage is possible when a lighter nanoparticle (e.g., a multi-walled **CNT)** replaces the Au nanorod. The excellent static and dynamic performance of squitches predicted in theory supports their prospect as high-speed **NEM** switch candidates for low-power logic applications.

To demonstrate the squitch concept **by** experiment, a detailed nanofabrication process for a multi-terminal squitch has been proposed, which combines top-down and bottom-up fabrication techniques. **A** newly-developed peeling technique provides subnanometer roughness for the surface of the electrodes, which not only favors the selfassembly process to achieve a uniform monolayer of molecules but also contributes to consistent performance from device to device. The thickness of the molecular spacer is defined **by** the molecular chain length, and dielectrophoretic trapping is utilized to position a single nanoparticle as the top floating electrode to complete squitch fabrication. In order to make the entire fabrication process scalable, a large-scale trapping approach has been proposed, which works **by** connecting devices in parallel to enable independent trapping process for each device. Moreover, an on-chip capacitor is connected in series to each device to help prevent trapping multiple nanorods onto the electrodes. The effectiveness and scalability of the proposed technique have been validated **by** the success of trapping Au nanorods onto hundreds of two-terminal electrodes simultaneously with a decent yield of 20%. More significantly, the proposed scalable trapping approach works for both contact-mode devices and tunneling-mode devices (squitches as an example), and therefore represents a versatile nanofabrication technique that makes the manufacturing of nanoparticle-based devices **highly** efficient.

Two-terminal squitches based on Au nanorod and PEG-thiol molecules with different molecular weights have been fabricated for proof of concept. **A** 2 V actuation voltage and a sub-i V hysteresis of a two-terminal squitch have been demonstrated **by** experiments. Besides, the performance from device to device is consistent owing to uniform metal-molecule-metal junctions fabricated **by** the developed peeling technique. The manufacturing of a four-terminal squitch turns out to be much more challenging. Still, successful four-terminal squitches are presented, which are made possible **by** yield control, discussed in detail in Chapter **3,** for each fabrication step. Though a four-terminal squitch with a proper switching behavior is absent in this thesis, the capability of squitches to function as low-power logic unit has been suggested **by** the preliminary results of two-terminal squitches and will be fulfilled after a few challenges are properly addressed in future work.

### **5.2 Outlook**

According to the theoretical and experimental study conducted in this thesis, the maturation of squitches into a viable **NEM** switch technology is subject to a few challenges lying among device design, fabrication and engineering of molecules. **Ad**ditionally, dynamics of the squitches have not been well characterized, which will be another interesting topic for future work.

#### **5.2.1 Improvement for Squitch Design and Fabrication**

First, poor adhesion between Au and epoxy sets a huge block to the reliable operation of a multi-terminal squitch. According to the results of four-terminal squitches, device failure caused **by** the pull-in occurred at the gate electrodes is most likely attributed to the poor adhesion between the gate electrodes and the epoxy. Therefore, gate electrodes made with non-noble materials, which have better adhesion to epoxy, will be involved in future designs. For those squitches, the thickness of an oxide layer formed on the gate electrodes should be controlled in order that low actuation voltage

is still available despite the weakened gate-modulation.

Second, an optimized self-assembly process is acutely needed. According to the results from two-terminal squitches, the IV curves for the first few cycles do not coincide well. The disappearance of pull-in behavior after the first (or the second) run and the gradual shift of IV curve to lower actuation voltages indicate that the molecular spacer is reconfigured during the first few cycles of operation. After compression in each cycle, the molecules are packed more densely and the resulting molecular layer is thinner and exhibits a more nonlinear elasticity. The change in thickness of the molecular layer agrees with the measured shift of IV curve, and the pull-in behavior tends to disappear when the nonlinearity in the elastic property of molecules increases, as analyzed in Chapter 2. Reconfiguration of the molecular spacer under compression also explains the sub-1 V hysteresis observed for fabricated two-terminal squitches. Theoretically, the squitch can be made hysteresis-free according to the prediction in Chapter 2; however, if the molecules during the release process show an elastic property different from that during the compression process, there will be a hysteresis for the equivalent spring constant and a resulting hysteresis for the IV curve. When a more densely packed molecular layer is available due to an optimized self-assembly process, more consistent performance during cycles of operation and a lower hysteresis can be predicted for the next generation of squitches.

Third, the overall yield for multi-terminal squitch fabrication is still limited, which is constrained **by** the yield for dielectrophoretic trapping. Though a decent yield of 20% has been obtained for two-terminal squitches, the more complex field distribution around multi-terminal electrodes as well as the strong capillary force experienced **by** trapped nanoparticles when the suspension dries brings about huge obstacles to a high yield of trapping for multi-terminal squitches. To address this issue, optimization in the shapes of multi-terminal electrodes and a more effective way to reduce the capillary force will be the key to the success of scalable fabrication of squitches with a high overall yield.

Fourth, the limited lifecycle measured for current squitches constitutes another concern. It is believed that the stiction failure occurs due to the accumulated joule heating inside the junction which will degrade or even burn out the molecules. Therefore, heat generation and dissipation inside the junction will be an important issue to study in future work, which may ask for optimization in device design. Besides, encapsulation can be helpful considering the sensitive feature of **PEG** molecules.

#### **5.2.2 Engineering of Molecules**

Instead of protecting the molecules **by** encapsulation and a sophisticated design for heat dissipation, replacing the sensitive molecules with more robust ones seems more straightforward and effective. With molecules resistant to heat as well as moisture and oxygen in the ambient environment, device degradation over time will be less likely and the lifecycle can be greatly extended.

Though good device performance has been demonstrated **by** the fabricated twoterminal squitches, there is still a gap between the experimentally measured results and the excellent properties theoretically predicted. For instance, a 2.14 mV/dec subthreshold slope has been predicted, while the fabricated squitches only show **60** mV/dec. The disparity is probably attributed to the non-ideal elastic property of the PEG-thiol molecules utilized to make squitches. Therefore, optimization of molecules is necessary for future studies before outstanding device performance can be demonstrated. Besides, hysteresis-free squitches are predicted based on the assumption that a small nonlinearity exists in the elasticity of the molecular layer, and it indicates that the hysteresis for squitches can be greatly reduced or even eliminated **by** engineering the elastic property of the molecules.

#### **5.2.3 Dynamics of Squitches**

Investigation into the dynamic performance of squitches will be another focus of future work. Though the squitches are predicted to work in a **100** MHz to 1 GHz regime, the outstanding switching speed has not been demonstrated **by** experiment. **A** rough evaluation of the switching delay is attainable through step-response experiments on squitch devices, while a more accurate measurement for the delay can be obtained **by** connecting squitches into a ring oscillator.

Finally, theoretical analysis indicates that reduction in the mass of floating electrode is able to increase the switching speed of squitches without sacrificing the low actuation voltage. From this perspective, the idea of replacing the nanorod with a multi-walled **CNT** is very attractive, which will be another focus of future work.

# **Bibliography**

- **[11** David **J** Frank, Robert H Dennard, Edward Nowak, Paul M Solomon, Yuan Taur, Hon-Sum Philip Wong, et al. Device scaling limits of si mosfets and their application dependencies. *Proceedings of the IEEE,* **89(3):259-288,** 2001.
- [21 The international technology roadmap for semiconductors 2.0 (itrs2.0, **2015):** Executive report. http://www.itrs2.net/itrs-reports.html.
- **[3]** Owen Y Loh and Horacio **D** Espinosa. Nanoelectromechanical contact switches. *Nature nanotechnology,* **7(5):283,** 2012.
- [41 The international technology roadmap for semiconductors 2.0 (itrs2.0, **2015):** Beyond cmos. http://www.itrs2.net/itrs-reports.html.
- **[51** Hamed F Dadgour, Muhammad M Hussain, Casey Smith, and Kaustav Banerjee. Design and analysis of compact ultra energy-efficient logic gates using laterallyactuated double-electrode nems. In *Design Automation Conference (DA C), 2010 47th ACM/IEEE,* pages **893-896. IEEE,** 2010.
- **[6]** Matthew Spencer, Fred Chen, Cheng **C** Wang, Rhesa Nathanael, Hossein Fariborzi, Abhinav Gupta, Hei Kam, Vincent Pott, Jaeseok Jeon, Tsu-Jae King Liu, et al. Demonstration of integrated micro-electro-mechanical relay circuits for vlsi applications. *IEEE Journal of Solid-State Circuits,* **46(1):308-320,** 2011.
- **[71** Te-Hao Lee, Swarup Bhunia, and Mehran Mehregany. Electromechanical **com**puting at **500** c with silicon carbide. *Science,* **329(5997):1316-1318,** 2010.
- **[8]** Kyu-Man Hwang, Jun-Young Park, Hagyoul Bae, Seung-Wook Lee, Choong-Ki Kim, Myungsoo Seo, Hwon Im, Do-Hyun Kim, Seong-Yeon Kim, Geon-Beom Lee, et al. Nano-electromechanical switch based on a physical unclonable function for **highly** robust and stable performance in harsh environments. *A CS nano,* **11(12):12547-12552, 2017.**
- **[9]** L Magnus Jonsson, **S** Axelsson, Tomas Nord, **S** Viefers, and Jari M Kinaret. High frequency properties **of** a cnt-based nanorelay. *Nanotechnology,* 15(11):1497, 2004.
- **[10] MN** Lovellette, AB Campbell, HL Hughes, RK Lawerence, **JW** Ward, M Meinhold, TR Bengtson, **GF** Carleton, BM Segal, and T Rueckes. Nanotube memories

for space applications. In *Aerospace Conference, 2004. Proceedings. 2004 IEEE,* volume 4, pages **2300-2305.** IEEE, 2004.

- **[11]** Till **JW** Wagner and Dominic Vella. Switch on, switch off: stiction in nanoelectromechanical switches. *Nanotechnology,* **24(27):275501, 2013.**
- [12] Owen Loh, Xiaoding Wei, Changhong Ke, John Sullivan, and Horacio **D** Espinosa. Robust carbon-nanotube-based nano-electromechanical devices: Understanding and eliminating prevalent failure modes using alternative electrode materials. *small,* **7(1):79-86,** 2011.
- **[13]** Roya Maboudian and Roger T Howe. Critical review: Adhesion in surface micromechanical structures. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena,* **15(1):1-20, 1997.**
- [14] Marc Dequesnes, **SV** Rotkin, and NR Aluru. Calculation of pull-in voltages for carbon-nanotube-based nanoelectromechanical switches. *Nanotechnology,* **13(1):120,** 2002.
- **<sup>1151</sup>**Weon Wi Jang, Jeong Oen Lee, Jun-Bo Yoon, Min-Sang Kim, Ji-Myoung Lee, Sung-Min Kim, Keun-Hwi Cho, Dong-Won Kim, Donggun Park, and Won-Seong Lee. Fabrication and characterization of a nanoelectromechanical switch with **15** nm-thick suspension air gap. *Applied Physics Letters,* **92(10):103110, 2008.**
- **[16]** Weon Wi Jang, Jun-Bo Yoon, Min-Sang Kim, Ji-Myoung Lee, Sung-Min Kim, Eun-Jung Yoon, Keun Hwi Cho, Sung-Young Lee, In-Hyuk Choi, Dong-Won Kim, et al. Nems switch with **30** nm-thick beam and 20 nm-thick air-gap for high density non-volatile memory applications. *Solid-State Electronics,* **52(10):1578- 1583, 2008.**
- **[17]** Christian **A** Martin, Roel HM Smit, Herre **SJ** van der Zant, and Jan M van Ruitenbeek. **A** nanoelectromechanical single-atom switch. *Nano letters,* 9(8):2940-2945, **2009.**
- **[18]** Zhuo Chen, Lianming Tong, Zhongyun Wu, and Zhongfan Liu. Fabrication of electromechanical switch using interconnected single-walled carbon nanotubes. *Applied Physics Letters,* **92(10):103116, 2008.**
- **[19]** Wenfeng Xiang and Chengkuo Lee. Nanoelectromechanical torsion switch of low operation voltage for nonvolatile memory application. *Applied Physics Letters,* **96(19):193113,** 2010.
- [20] **JM** Kinaret, T Nord, and **S** Viefers. **A** carbon-nanotube-based nanorelay. *Applied Physics Letters,* **82(8):1287-1289, 2003.**
- [21] **SE** Khadem, M Rasekh, and **A** Toghraee. Design and simulation of a carbon I nanotube-based adjustable nano-electromechanical shock switch. *Applied Mathematical Modelling,* **36(6):2329-2339,** 2012.
- [22] Sang Wook Lee, Seung Joo Park, Eleanor EB Campbell, and Yung Woo Park. **A** fast and low-power microelectromechanical system-based non-volatile memory device. *Nature communications,* 2:220, 2011.
- **[23]** Owen Loh, Xiaoding Wei, John Sullivan, Leonidas **E** Ocola, Ralu Divan, and Horacio **D** Espinosa. Carbon-carbon contacts for robust nanoelectromechanical switches. *Advanced Materials,* 24(18):2463-2468, 2012.
- [24] Changhong Ke and Horacio **D** Espinosa. In situ electron microscopy electromechanical characterization of a bistable nems device. *small,* 2(12):1484-1489, **2006.**
- **[25] S** Axelsson, Eleanor EB Campbell, LM Jonsson, **J** Kinaret, SangWook Lee, Yung-Woo Park, and Martin Sveningsson. Theoretical and experimental investigations of three-terminal carbon nanotube relays. *New Journal of Physics,* 7(1):245, **2005.**
- **[261** You Qian, Liang Lou, Minglin Julius Tsai, and Chengkuo Lee. **A** dual-siliconnanowires based u-shape nanoelectromechanical switch with low pull-in voltage. *Applied Physics Letters,* **100(11):113102,** 2012.
- **[271** Peng Li, Zheng You, and Tianhong Cui. Graphene cantilever beams for nano switches. *Applied Physics Letters,* **101(9):093111,** 2012.
- **[28]** Changhong Ke, Horacio **D** Espinosa, and Nicola Pugno. Numerical analysis of nanotube based nems devices a ATpart ii: Role of finite kinematics, stretching and charge concentrations. *Journal of Applied Mechanics,* **72(5):726-731, 2005.**
- **[29]** M Rasekh, **SE** Khadem, and M Tatari. Nonlinear behaviour of electrostatically actuated carbon nanotube-based devices. *Journal of Physics D: Applied Physics,* **43(31):315301,** 2010.
- **[30]** Miao Lu, Xuekun Lu, Min-Woo Jang, Stephen **A** Campbell, and Tianhong Cui. Characterization of carbon nanotube nanoswitches with gigahertz resonance frequency and low pull-in voltages using electrostatic force microscopy. *Journal of Micromechanics and Microengineering,* **20(10):105016,** 2010.
- **[31]** Ngoc Huynh Van, Manoharan Muruganathan, Jothiramalingam Kulothungan, and Hiroshi Mizuta. Fabrication of a three-terminal graphene nanoelectromechanical switch using two-dimensional materials. *Nanoscale,* **2018.**
- **[32]** Rhesa Nathanael, Vincent Pott, Hei Kam, Jaeseok Jeon, and Tsu-Jae King Liu. 4-terminal relay technology for complementary logic. In *Electron Devices Meeting (IEDM), 2009 IEEE International,* pages 1-4. **IEEE, 2009.**
- **[33]** Benjamin Osoba, Bivas Saha, Liam Dougherty, Jane Edgington, Chuang Qian, Farnaz Niroui, Jeffrey H Lang, Vladimir Bulovic, Junqiao Wu, and Tsu-Jae King Liu. Sub-50 my nem relay operation enabled **by** self-assembled molecular coating. In *Electron Devices Meeting (IEDM), 2016 IEEE International,* pages **26-8. IEEE, 2016.**
- [34] Jeong Oen Lee, Yong-Ha Song, Min-Wu Kim, Min-Ho Kang, Jae-Sub Oh, Hyun-Ho Yang, and Jun-Bo Yoon. **A** sub-1-volt nanoelectromechanical switching device. *Nature nanotechnology,* **8(1):36, 2013.**
- **[35]** Ji-Hun Kim, Zack CY Chen, Soonshin Kwon, and Jie Xiang. Three-terminal nanoelectromechanical field effect transistor with abrupt subthreshold slope. *Nano letters,* **14(3):1687-1691,** 2014.
- **[361 D** Acquaviva, **A** Arun, **S** Esconjauregui, **D** Bouvet, **J** Robertson, R Sma**jda, A** Magrez, L Forro, and AM Ionescu. Capacitive nanoelectromechanical switch based on suspended carbon nanotube array. *Applied Physics Letters,* **97(23):233508,** 2010.
- **137]** Abdulilah M Mayet, Aftab M Hussain, and Muhammad M Hussain. Threeterminal nanoelectromechanical switch based on tungsten nitride $\hat{A}$ Tan amorphous metallic material. *Nanotechnology,* **27(3):035202, 2015.**
- **[38]** K Yoo, **D** Lee, R Tiberio, **J** Conway, **H-S** P Wong, and Y Nishi. Design and materials selection for low power laterally actuating nanoelectromechanical relays. In *SOI Conference (SOI), 2012 IEEE International,* pages 1-2. **IEEE,** 2012.
- **[391** Jin-Woo Han, Jae-Hyuk Ahn, Min-Wu Kim, Jeong Oen Lee, Jun-Bo Yoon, and Yang-Kyu Choi. Nanowire mechanical switch with a built-in diode. *Small,* **6(11):1197-1200,** 2010.
- [40] Kerem Akarvardar and **H-S** Philip Wong. Ultralow voltage crossbar nonvolatile memory based on energy-reversible nem switches. *IEEE Electron Device Letters,* **30(6):626-628, 2009.**
- [41] WS Lee, **S** Chong, R Parsa, **J** Provine, **D** Lee, **S** Mitra, **H-SP** Wong, and RT Howe. Dual sidewall lateral nanoelectromechanical relays with beam isolation. In *Solid-State Sensors, Actuators and Microsystems Conference (TRANS-DUCERS), 2011 16th International,* pages **2606-2609. IEEE,** 2011.
- [42] R Parsa, M Shavezipur, WS Lee, **S** Chong, **D** Lee, **H-SP** Wong, R Maboudian, and RT Howe. Nanoelectromechanical relays with decoupled electrode and suspension. In *Micro electro mechanical systems (MEMS), 2011 IEEE 24th international conference on,* pages **1361-1364. IEEE,** 2011.
- [43] Mohammad Shavezipur, Kimberly Harrison, William Scott Lee, Subhasish Mitra, **H-S** Philip Wong, and Roger T Howe. Partitioning electrostatic and mechanical domains in nanoelectromechanical relays. *J. Microelectromech. Syst,* **24:592-598, 2015.**
- 144] Roozbeh Parsa, W Scott Lee, Mohammad Shavezipur, **J** Provine, Roya Maboudian, Subhasish Mitra, **H-S** Philip Wong, and Roger T Howe. Laterally actuated platinum-coated polysilicon nem relays. *Journal of Microelectromechanical Systems,* **22(3):768-778, 2013.**
- [451 **D** Lee, WS Lee, **J** Provine, **J-0** Lee, **J-B** Yoon, RT Howe, **S** Mitra, and **H-SP** Wong. Titanium nitride sidewall stringer process for lateral nanoelectromechanical relays. In *Micro Electro Mechanical Systems (MEMS), 2010 IEEE 23rd International Conference on,* pages *456-459.* **IEEE,** 2010.
- [46] Ji Cao, Ling Li, Kimihiko Kato, Tsu-Jae King Liu, and **H-S** Philip Wong. Sub-5 nm gap formation for low power nem switches. In *Energy Efficient Electronic Systems (E3S), 2015 Fourth Berkeley Symposium on,* pages **1-3. IEEE, 2015.**
- 1471 XL Feng, MH Matheny, Christian **A** Zorman, Mehran Mehregany, and ML Roukes. Low voltage nanoelectromechanical switches based on silicon carbide nanowires. *Nano letters,* **10(8):2891-2896,** 2010.
- [48] **SN** Cha, **JE** Jang, Y Choi, **GAJ** Amaratunga, **D-J** Kang, **DG** Hasko, **JE** Jung, and **JM** Kim. Fabrication of a nanoelectromechanical switch using a suspended carbon nanotube. *Applied Physics Letters,* **86(8):083105, 2005.**
- [49] Yuhei Hayamizu, Takeo Yamada, Kohei Mizuno, Robert **C** Davis, Don **N** Futaba, Motoo Yumura, and Kenji Hata. Integrated three-dimensional microelectromechanical devices from processable carbon nanotube wafers. *Nature nanotechnology,* **3(5):289, 2008.**
- **[501** Jungwook Choi, Jae-Ik Lee, Youngkee Eun, Min-Ook Kim, and Jongbaeg Kim. Aligned carbon nanotube arrays for degradation-resistant, intimate contact in micromechanical devices. *Advanced Materials,* **23(19):2231-2236,** 2011.
- **[511 JE** Jang, **SN** Cha, Y Choi, TP Butler, **DJ** Kang, **DG** Hasko, **JE** Jung, YW Jin, **JM** Kim, and **GAJ** Amaratunga. Nanoelectromechanical switch with low voltage drive. *Applied Physics Letters,* **93(11):113105, 2008.**
- **[52] JE** Jang, **SN** Cha, Y Choi, Gehan **AJ** Amaratunga, **DJ** Kang, **DG** Hasko, **JE** Jung, and **JM** Kim. Nanoelectromechanical switches with vertically aligned carbon nanotubes. *Applied Physics Letters,* **87(16):163114, 2005.**
- **[531** Jae Eun Jang, Seung Nam Cha, Young Jin Choi, Dae Joon Kang, Tim P Butler, David **G** Hasko, Jae Eun Jung, Jong Min Kim, and Gehan **AJ** Amaratunga. Nanoscale memory cell based on a nanoelectromechanical switched capacitor. *Nature Nanotechnology,* **3(1):26, 2008.**
- [54] **A** Kis, K Jensen, **S** Aloni, W Mickelson, and **A** Zettl. Interlayer forces and ultralow sliding friction in multiwalled carbon nanotubes. *Physical Review Letters,* **97(2):025501, 2006.**
- **<sup>1551</sup>**VV Deshpande, H-Y Chiu, HW **Ch** Postma, **C** Miko, L Forro, and M Bockrath. Carbon nanotube linear bearing nanoswitches. *Nano Letters,* **6(6):1092-1095, 2006.**
- **1561** Jeong Won Kang and Qing Jiang. Electrostatically telescoping nanotube nonvolatile memory device. *Nanotechnology,* **18(9):095705, 2007.**
- **[571** Arunkumar Subramanian, LX Dong, Bradley **J** Nelson, and Antoine Ferreira. Supermolecular switches based on multiwalled carbon nanotubes. *Applied Physics Letters,* **96(7):073116,** 2010.
- **[581** Usama Zaghloul and Gianluca Piazza. Sub-1-volt piezoelectric nanoelectromechanical relays with millivolt switching capability. *IEEE Electron Device Letters,* **35(6):669-671,** 2014.
- **[591** BD Davidson, **D** Seghete, **SM** George, and VM Bright. **Ald** tungsten nems switches and tunneling devices. *Sensors and Actuators A: Physical,* **166(2):269- 276,** 2011.
- **[601** Anupama B Kaul, Eric W Wong, Larry **Epp,** and Brian **D** Hunt. Electromechanical carbon nanotube switches for high-frequency applications. *Nano letters,* 6(5):942-947, **2006.**
- **[611** Andrey V Danilov, Per Hedega'rd, Dmitrii **S** Golubev, Thomas Bjornholm, and Sergey **E** Kubatkin. Nanoelectromechanical switch operating **by** tunneling of an entire c60 molecule. *Nano letters,* **8(8):2393-2398, 2008.**
- **[621** Farnaz Niroui, Annie I Wang, Ellen M Sletten, Yi Song, Jing Kong, Eli Yablonovitch, Timothy M Swager, Jeffrey H Lang, and Vladimir Bulovic. Tunneling nanoelectromechanical switches based on compressible molecular thin films. *ACS nano,* **9(8):7886-7894, 2015.**
- **[63]** Farnaz Niroui, Parag B Deotare, Ellen M Sletten, Annie **I** Wang, Eli Yablonovitch, Timothy M Swager, Jeffrey H Lang, and Vladimir Bulovic. Nanoelectromechanical tunneling switches based on self-assembled molecular layers. In *Micro Electro Mechanical Systems (MEMS), 2014 IEEE 27th International Conference on,* pages **1103-1106.** IEEE, 2014.
- [64] **S** Paydavosi, FM Yaul, **Al** Wang, F Niroui, TL Andrew, V Bulovi6, and **JH** Lang. Mems switches employing active metal-polymer nanocomposites. In *Micro Electro Mechanical Systems (MEMS), 2012 IEEE 25th International Conference on,* pages **180-183.** IEEE, 2012.
- **<sup>1651</sup>**Jin-Woo Han, Jae-Hyuk Ahn, Min-Wu Kim, Jun-Bo Yoon, and Yang-Kyu Choi. Monolithic integration of nems-cmos with a fin flip-flop actuated channel transistor (finfact). In *Electron Devices Meeting (IEDM), 2009 IEEE International,* pages 1-4. **IEEE, 2009.**
- **[66]** Hamed Dadgour, Alan M Cassell, and Kaustav Banerjee. Scaling and variability analysis of cnt-based nems devices and circuits with implications for process design. In *Electron Devices Meeting, 2008. IEDM 2008. IEEE International,* pages 1-4. IEEE, **2008.**
- **[671** Jack Yaung, Louis Hutin, Jaeseok Jeon, and **T-J** King Liu. Adhesive force characterization for mem logic relays with sub-micron contacting regions. *J. Microelectromech. Syst,* **23(1):198-203,** 2014.
- **[68]** Jeong-Oen Lee, Min-Wu Kim, Seung-Deok Ko, Hee-Oh Kang, Woo-Ho Bae, Min-Ho Kang, Ki-Nam Kim, Dong-Eun Yoo, and Jun-Bo Yoon. 3-terminal nanoelectromechanical switching device in insulating liquid media for low voltage operation and reliability improvement. In *Electron Devices Meeting (IEDM), 2009 IEEE International,* pages 1-4. **IEEE, 2009.**
- **[69]** MYA Yousif, P Lundgren, F Ghavanini, Peter Enoksson, and Stefan Bengtsson. Cmos considerations in nanoelectromechanical carbon nanotube-based switches. *Nanotechnology,* **19(28):285204, 2008.**
- **[70] E** Dujardin, V Derycke, MF Goffman, R Lefevre, and **JP** Bourgoin. Selfassembled switches based on electroactuated multiwalled nanotubes. *Applied Physics Letters,* **87(19):193107, 2005.**
- **[71]** Jingqi Li, Qing Zhang, Ning Peng, and Qi Zhu. Manipulation of carbon nanotubes using ac dielectrophoresis. *Applied Physics Letters,* **86(15):153116, 2005.**
- **[72]** Sarbajit Banerjee, Brian **E** White, Limin Huang, Blake **J** Rego, Stephen OAA2Brien, and Irving P Herman. Precise positioning of single-walled carbon nanotubes **by** ac dielectrophoresis. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena,* **24(6):3173-3178, 2006.**
- **[73]** Sang Wook Lee, Dong Su Lee, Raluca **E** Morjan, Sung Ho Jhang, Martin Sveningsson, **OA** Nerushev, Yung Woo Park, and Eleanor EB Campbell. **A** threeterminal carbon nanorelay. *Nano letters,* 4(10):2027-2030, 2004.
- [74] Fred Chen, Hei Kam, Dejan Markovic, Tsu-Jae King Liu, Vladimir Stojanovic, and Elad Alon. Integrated circuit design with nem relays. In *Proceedings of the 2008 IEEE/ACM International Conference on Computer-Aided Design,* pages **750-757. IEEE** Press, **2008.**
- **[75]** Nicolas Abel6, R Fritschi, K Boucart, F Casset, P Ancey, and Adrian Mihai Ionescu. Suspended-gate mosfet: bringing new mems functionality into solidstate mos transistor. In *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International,* pages 479-481. **IEEE, 2005.**
- **[761** Soogine Chong, Byoungil Lee, Kokab B Parizi, **J** Provine, Subhasish Mitra, Roger T Howe, and **H-S** Philip Wong. Integration of nanoelectromechanical (nem) relays with silicon cmos with functional cmos-nem circuit. In *Electron Devices Meeting (IEDM), 2011 IEEE International,* pages **30-5. IEEE,** 2011.
- **[771** Soogine Chong, Byoungil Lee, Subhasish Mitra, Roger T Howe, and **H-S** Philip Wong. Integration of nanoelectromechanical relays with silicon nmos. *IEEE Transactions on Electron Devices,* **59(1):255-258,** 2012.
- **[781** Sumit Saha, **U** Sajesh Kumar, Maryam Shojaei Baghini, Mayank Goel, and V Ramgopal Rao. **A** nano-electro-mechanical switch based power gating for

effective stand-by power reduction in finfet technologies. *IEEE Electron Device Letters,* **38(5):681-684, 2017.**

- **[79]** Soogine Chong, Kerem Akarvardar, Roozbeh Parsa, Jun-Bo Yoon, Roger T Howe, Subhasish Mitra, and **H-S** Philip Wong. Nanoelectromechanical (nem) relays integrated with cmos sram for improved stability and low leakage. In *Proceedings of the 2009 International Conference on Computer-Aided Design,* pages 478-484. **ACM, 2009.**
- **[801** Chen Chen, W Scott Lee, Roozbeh Parsa, Soogine Chong, **J** Provine, Jeff Watt, Roger T Howe, **H-S** Philip Wong, and Subhasish Mitra. Nano-electro-mechanical relays for fpga routing: Experimental demonstration and a design technique. In *Design, Automation* **&** *Test in Europe Conference & Exhibition (DATE), 2012,* pages **1361-1366. IEEE,** 2012.
- **[81]** John **G** Simmons. Electric tunnel effect between dissimilar electrodes separated **by** a thin insulating film. *Journal of applied physics,* **34(9):2581-2590, 1963.**
- **[82] G** Palasantzas, **PJ** Van Zwol, and **J** Th M De Hosson. Transition from casimir to van der waals force between macroscopic bodies. *Applied Physics Letters,* **93(12):121912, 2008.**
- **[83]** Cameron **J** Shearer, Ashley **D** Slattery, Andrew **J** Stapleton, Joseph **G** Shapter, and Christopher T Gibson. Accurate thickness measurement of graphene. *Nanotechnology,* **27(12):125704, 2016.**