GaN Nanowire n-MOSFET with 5 nm Channel Length for Applications in Digital Electronics

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***Abstract*— We study the performance of GaN nanowire n-MOSFETs (GaN-NW-nFETs) with channel length, Lg=5 nm based on fully ballistic quantum transport simulations. Our simulation results show high I_{ON}=1137 µA/µm and excellent ON-OFF characteristics with Q=g_m/SS=188 µS-dec/µm-mV calculated for I_{OFF}=1 nA/µm and V_{GS}=V_{DS}=V_{CC}=0.5 V. These results represent (i) ~15% higher I_{ON} than Si-NW-nFET, and (ii) ~17% better Q than Si-NW-nFET, all with Lg=5 nm, thus suggesting the GaN n-channel an intriguing option for application in logic at sub-10 nm channel length. The superior performance of GaN channel compared to Si and other semiconductors at this scaled dimension can be attributed to its relatively higher effective mass of electron and lower permittivity.**

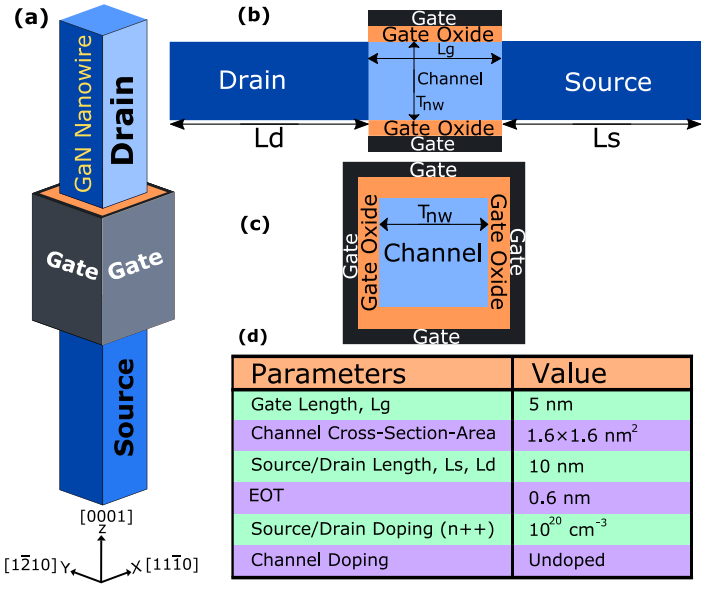
***Index Terms*— Nanowire, GaN, Si, Ge and InAs**

I. Introduction

Gallium Nitride (GaN), a wide bandgap (~3.4 eV) semiconductor, has some remarkable attributes that may prove to be useful in sub-10 nm transistor technology. Its wide band-gap significantly reduces band-to-band tunneling and gate induced drain leakage (GIDL) and allows for high temperature operation [1]. Because of the high optical phonon energy (~ 93 meV) [2], wide valley separation (nearest valley to Γ is M and it is >1 eV apart) and high mobility, fully ballistic transport is expected in the sub-30 nm regime [3]-[4]. Room temperature ballistic transport in GaN has already been experimentally demonstrated in [4], and GaN-based transistors with a current gain cut-off frequency approaching 500 GHz have already been reported [5]. In addition, being a direct bandgap material, GaN-based on chip optical communication is possible thanks to the maturity of GaN based photonic devices [6]. In addition, its spontaneous and piezoelectric polarization offers a new degree of freedom to dope the source and drain region without the impact of Random Dopant Fluctuation (RDF) effects and thermal diffusion of dopants [7]-[8]. Finally, it has been demonstrated that the modulation of polarization charge in the III-Nitride system could yield sub-40 mV/dec switching operation [9]. The piezoelectricity in GaN has also been proposed to attain steep subthreshold behavior [10]. All these benefits make a GaN channel an intriguing option for future n-MOSFET devices for digital applications, which could complement the well-known markets of GaN for RF [11] and power applications [12].

II. Simulation Approach And Results

The simulations of Nanowire Transistors (NW-nFETs) performed in this work are based on the self-consistent solution of Poisson and Schrodinger equations within the Non-equilibrium Green Functions framework, on a generic three dimensional domain using the NanoTCAD ViDES simulation environment [13]-[14], which has been extended in order to simulate GaN nanowires.



Parameters	Value
Gate Length, Lg	5 nm
Channel Cross-Section-Area	1.6×1.6 nm^2
Source/Drain Length, Ls, Ld	10 nm
EOT	0.6 nm
Source/Drain Doping (n++)	10^{20} cm^{-3}
Channel Doping	Undoped

Fig. 1: Schematic of the GaN Nanowire n-MOSFET (GaN-NW-nFET) simulated in this work showing: (a) Device Structure (3-D), (b) 2-D lateral cross-section view, (c) 2-D vertical cross section view, and (d) important device parameters.

The structure of the simulated devices and key device parameters are shown in Fig. 1. The cross-section area of the NW has been carefully chosen, so that the channel length, L_g<6λ (here $\lambda = \sqrt{\frac{\epsilon_{channel}}{4\epsilon_{OX}} \times EOT \times T_{NW}}$ is the natural length

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of the device [15]), which allows for the proper mitigation of short channel effects (SCEs). Fig. 2(a) shows variation of λ with the thickness of nanowire for different channel materials. As can be seen, for a given channel thickness GaN has the lowest λ thanks to its relatively low permittivity. Transistor benchmarking for digital applications is traditionally performed with threshold voltage (V_T) tuned to obtain a fixed target I_{OFF}. In this work, the tuning of threshold voltage was performed by tuning the metal work function, *i.e.*, flat-band voltage (V_{FB}) keeping all other device parameters fixed. The same device structure (channel length, Lg=5 nm, channel thickness, T_{NW}=1.6 nm and EOT=0.6 nm) has been used to benchmark the performance of GaN-NW-nFET with NW-nFETs of other common semiconductors such as Si, Ge and InAs. Table. 1 lists permittivity, transport effective mass of electron (without including non-parabolicity) and channel orientation of all the semiconductor nanowires used in this study. For Si nanowire transport direction ⟨100⟩ is chosen as it yields the highest ON current compared to other directions at this scaled dimensions.

TABLE I: MATERIAL PARAMETERS AND CHANNEL ORIENTATION

Material	Permittivity ϵ_r	Electron effective mass (m_{eff})	Transport direction
GaN	8.9	0.370m_0 [16]	⟨0001⟩
Si	11.8	0.340m_0 [17]	⟨100⟩
Ge	16	0.180m_0 [18]	⟨100⟩
InAs	15.15	0.153m_0 [19]	⟨111⟩

Fig. 2(b) shows the variation of ON current with OFF current for different semiconductor NW-nFETs having the same device structure and a fixed power supply voltage, V_{CC}=0.5 V, neglecting any resistances (both series and contact resistance) at the source and drain ends. At low OFF current of 1 nA/µm the ON current for GaN is ~15 % higher than that of Si, whereas at high OFF current of 100 nA/µm the ON current of GaN is only 2.5 % higher. This is due to the fact that at low off current the drive current is dominated by subthreshold characteristics whereas at high OFF current this is dominated by both sub and super threshold characteristics. GaN has slightly better subthreshold characteristics compared to Si because of its relatively higher electron effective mass (see Table I), which reduces the source drain direct tunneling leakage. In super threshold zone the performance is mainly dictated by electron velocity which actually reduces as effective mass of electron is increased. To observe both the ON and OFF-state device performance, we plot SS *vs* intrinsic-g_m in Fig. 2(c) for devices of both Low Standby Power (LP- I_{OFF}=1 nA/µm and V_{CC}=0.5 V) applications and High Performance (HP- I_{OFF}=100 nA/ µm and V_{CC}=0.5 V) applications. As, can be seen from this plot, the ON-OFF performance metric Q=g_m/SS [20] (Q_{GaN}=187.79 µS-dec/µm-mV (LP), 252 µS-dec/µm-mV (HP) and Q_{Si}=161 µS-dec/µm-mV (LP), 187 µS-dec/µm-mV (HP)), is about 17 % higher for LP and 35 % higher for HP in GaN compared to Si channel. In Fig. 2(d) we plot V_{CC}-I_{ON} (calculated at I_{OFF}=10nA/µm V_{GS}=V_{DS}=V_{CC}) for different semiconductor NW-nFETs. These results show that GaN gives higher I_{ON} at lower V_{CC} where I_{ON} is more sensitive to the subthreshold behavior. At V_{CC}=0.3V, I_{ON} of GaN is 1.25x higher than that of Si channel. Fig. 2(e) shows the I_{DS}-V_{GS} characteristics of all the considered NW transistors at I_{OFF}=1 nA/ µm. Electron density cross section profiles of both GaN and Si channel are presented in Fig. 2(f).

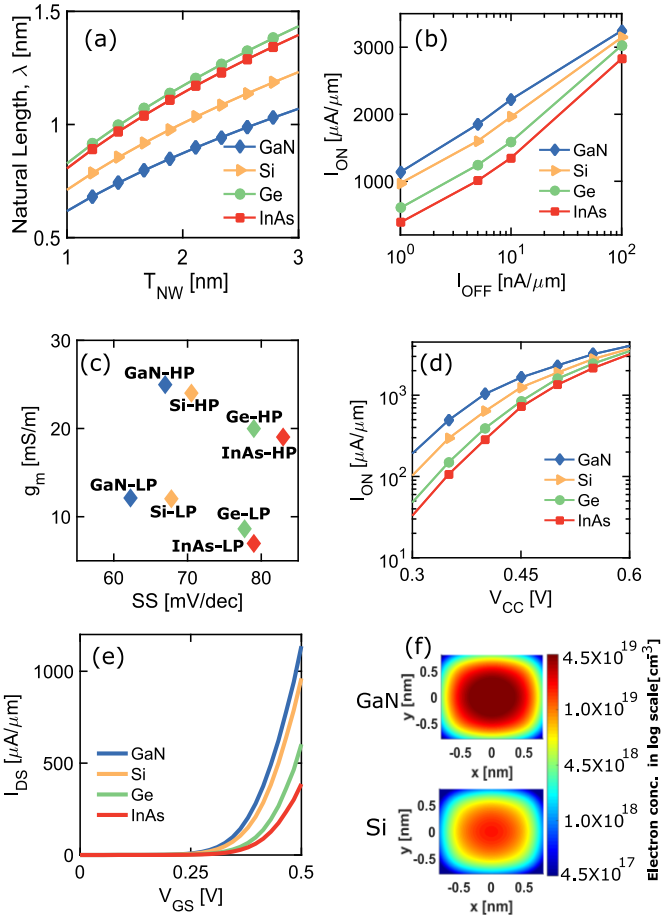

Fig. 2: (a) Dependence of λ on channel thickness,T_{NW} of square cross-section nanowire, for different semiconductors. GaN has lower λ compared to other semiconductors making it more immune to short channel effects. (b) Comparison of I_{ON} *vs* I_{OFF} (calculated at V_{CC}=0.5 V) of GaN-NW-nFET (Lg=5 nm) with other semiconductor (Si, Ge, InAs) NW-nFETs having the same device structure and doping level. The GaN-NW-nFET shows ~15% better I_{ON} at I_{OFF}=1 nA/µm than Si. (c) Comparison of intrinsic–g_m (calculated at V_{GS}=V_{DS}=0.5 V) *vs* SS of GaN-NW-nFET with NW-nFETs of other semiconductors (Si, Ge, InAs). These results translate to Q=g_m/SS (Ref. [20]) of 188 µS-dec/µm-mV for Low Standby Power (LP- I_{OFF}=1 nA/µm, V_{CC}=0.5 V), and 252 µS-dec/µm-mV for High Performance (HP- I_{OFF}=100 nA/ µm, V_{CC}=0.5 V) applications for GaN which are ~17% and ~35% better than Si data for LP and HP respectively. (d) Comparison of I_{ON} *vs* V_{CC} (calculated at LP condition) of GaN-NW-nFET with other semiconductor (Si, Ge, InAs) NW-nFET showing that GaN gives better I_{ON} at lower V_{CC}. At V_{CC}=0.3 V I_{ON} of GaN is ~1.25x higher than Si. Current and g_m are normalized by the width of the nanowire. (e) I_{DS} *vs* V_{GS} curves of Si, GaN, Ge and InAs nanowire transistors (f) Electron density (in cm^{-3}) cross section profile in the middle of the channel for both GaN and Si

To further investigate the reason behind the superior performance of GaN over other semiconductors in terms of drive current and subthreshold-swing, we study the impact of the two most important channel material parameters: (1) electron effective mass, and (2) relative permittivity on the drive current for the same supply voltage. As shown in Fig. 3(b) there exists an optimum electron effective mass in the channel

material which yields the highest ON current. For low effective mass, the tunneling probability ($T\alpha e^{-\sqrt{m_{eff}}}$) increases significantly and degrades the subthreshold behavior (see Fig. 3(a)). Whereas, for very high effective mass, the electron velocity ($v_e \alpha \frac{1}{\sqrt{m_{eff}}}$) is reduced yielding a lower drive current ($I = Q \times v_e$) . These two factors determine an optimum region for the electron effective mass around $0.3m_0$-$0.4m_0$ (see Fig. 3(b)) for LP devices.

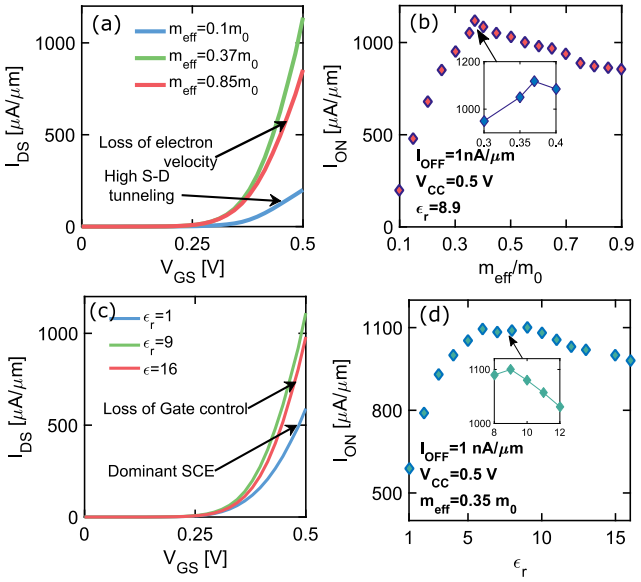

Fig. 3: (a) Impact of electron effective mass on the I_{DS}-V_{GS} characteristics for different channel materials. (b) I_{ON} (calculated at V_{GS}=V_{DS}=0.5V I_{OFF}=1nA/μm) *vs* effective mass of channel material (c) Impact of permittivity of the channel material on I_{DS}-V_{GS} characteristics. (d) I_{ON} (calculated at V_{GS}=V_{DS}=0.5V I_{OFF}=1nA/μm) *vs* permittivity(ϵ_r) of the channel material. Here, current is normalized by the width of the nanowire

The effect of the relative permittivity (ϵ_r) of the channel material upon the ON current is shown in Fig. 3(d). As we can see here, when ϵ_r is very low (1~5) the drive current is significantly decreased. This is due to the fact that when ϵ_r is low, the gate control over the channel diminishes because of reduced effective gate capacitance, resulting in low intrinsic transconductance (g_m) and drive current (I_{ON}). On the other hand, when ϵ_r is very high (>15), short channel effects come into the picture (*i.e.* λ increases) and degrade the subthreshold –swing which in turn degrades the ON current (see Fig. 3(c)). As shown in Fig. 3(d), the optimal relative permittivity values of the channel material lie within 7-13. For the small channel diameters studied in this work, the GaN NW has an electron effective mass of $0.37m_0$ [16] and relative permittivity of 8.9 [21]. Both of these parameters values fall into optimal zones thus yielding superior ON-OFF performance compared to other commonly used semiconductors. Fig. 4 shows a comparison of the threshold voltage (V_T) for different NW-nFETs at I_{OFF}=100 nA/μm. Here the threshold voltage has been extracted by extrapolation of the linear region I_{DS}-V_{GS} characteristics. As demonstrated in this graph, the GaN channel offers the lowest V_T (i.e. 250mV) whereas InAs channel gives the highest, V_T= 320 mV.

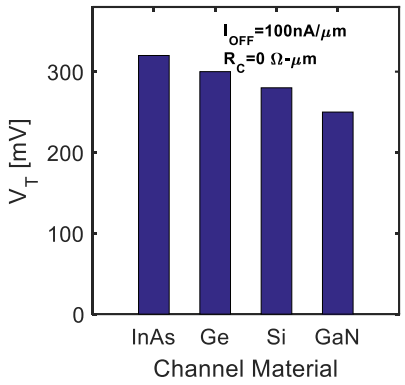

Fig. 4: Comparison of threshold voltage (V_T) of GaN-NW-nFET with other semiconductor NW-nFET having same device structure. For the same OFF current of 100 nA/μm, the GaN channel requires lower V_T because of its better subthreshold behavior due to its higher effective mass. Here it is worth mentioning that in this work a basic gate metal work function of 4.2 eV has been used and then it is varied in the range of hundreds of mili-eVs (10^{-3}eV) to match the targeted OFF current.

Since, the OFF current is given by $V_T \sim -SS \times log(I_{OFF})$, the channel material that has the lowest SS yields the lowest V_T when tuned at the same OFF current. As the GaN channel has the best sub-threshold behavior (*i.e.* lowest SS) because of its higher m_{eff}, it yields the lowest V_T thereby obtaining the highest ON current for the same supply voltage, V_{CC}.

III. Conclusion

In this paper, we presented performance projection of GaN-NW n-FET with 5 nm channel length and benchmark that with NW-nFETs of other semiconductors like Si, Ge and InAs. In terms of performance parameters such as I_{ON}, SS, and g_m, GaN outperforms other semiconductors mainly because of its relatively higher electron effective mass-which reduces source to drain direct tunneling and lower permittivity-which yields better short channel characteristics. From the detailed comparison presented here, it can be concluded that GaN NW n-FET can provide best drive current and ON-OFF characteristics for both Low Standby Power and High Performance applications compared to other semiconductors in transistors with an Lg= 5 nm.

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