

## MIT Open Access Articles

*GaN Nanowire n-MOSFET with 5 nm Channel Length for Applications in Digital Electronics*

The MIT Faculty has made this article openly available. **Please share** how this access benefits you. Your story matters.

**Citation:** Chowdhury, Nadim, Giuseppe Iannaccone, Gianluca Fiori, Dimitri A. Antoniadis and Tomás Palacios. "GaN Nanowire n-MOSFET with 5 nm Channel Length for Applications in Digital Electronics." *Electron Device Letters* 38, issue 7 (July 2017): pp. 859 - 862.

**As Published:** 10.1109/LED.2017.2703953

**Publisher:** Institute of Electrical and Electronics Engineers (IEEE)

**Persistent URL:** <https://hdl.handle.net/1721.1/121568>

**Version:** Author's final manuscript: final author's manuscript post peer review, without publisher's formatting or copy editing

**Terms of use:** Creative Commons Attribution-Noncommercial-Share Alike



# GaN Nanowire n-MOSFET with 5 nm Channel Length for Applications in Digital Electronics

Nadim Chowdhury, *Student Member*, Giuseppe Iannaccone, *Fellow, IEEE*, Gianluca Fiori, *Senior Member, IEEE* Dimitri A. Antoniadis *Life Fellow, IEEE*, and Tomás Palacios, *Fellow, IEEE*

**Abstract**— We study the performance of GaN nanowire n-MOSFETs (GaN-NW-nFETs) with channel length,  $L_g=5$  nm based on fully ballistic quantum transport simulations. Our simulation results show high  $I_{ON}=1137 \mu A/\mu m$  and excellent ON-OFF characteristics with  $Q=g_m/SS=188 \mu S\text{-dec}/\mu m\text{-mV}$  calculated for  $I_{OFF}=1$  nA/ $\mu m$  and  $V_{GS}=V_{DS}=V_{CC}=0.5$  V. These results represent (i)  $\sim 15\%$  higher  $I_{ON}$  than Si-NW-nFET, and (ii)  $\sim 17\%$  better  $Q$  than Si-NW-nFET, all with  $L_g=5$  nm, thus suggesting the GaN n-channel an intriguing option for application in logic at sub-10 nm channel length. The superior performance of GaN channel compared to Si and other semiconductors at this scaled dimension can be attributed to its relatively higher effective mass of electron and lower permittivity.

**Index Terms**— Nanowire, GaN, Si, Ge and InAs

## I. INTRODUCTION

Gallium Nitride (GaN), a wide bandgap ( $\sim 3.4$  eV) semiconductor, has some remarkable attributes that may prove to be useful in sub-10 nm transistor technology. Its wide band-gap significantly reduces band-to-band tunneling and gate induced drain leakage (GIDL) and allows for high temperature operation [1]. Because of the high optical phonon energy ( $\sim 93$  meV) [2], wide valley separation (nearest valley to  $\Gamma$  is M and it is  $>1$  eV apart) and high mobility, fully ballistic transport is expected in the sub-30 nm regime [3]-[4]. Room temperature ballistic transport in GaN has already been experimentally demonstrated in [4], and GaN-based transistors with a current gain cut-off frequency approaching 500 GHz have already been reported [5]. In addition, being a direct bandgap material, GaN-based on chip optical communication is possible thanks to the maturity of GaN based photonic devices [6]. In addition, its spontaneous and piezoelectric polarization offers a new degree of freedom to dope the source and drain region without the impact of Random Dopant Fluctuation (RDF) effects and thermal diffusion of dopants [7]-[8]. Finally, it has been demonstrated that the modulation of polarization charge in the III-Nitride system could yield sub-40 mV/dec switching operation [9]. The piezoelectricity in GaN has also been proposed to attain steep subthreshold behavior [10]. All these benefits make a GaN channel an intriguing option for future n-MOSFET devices for digital applications, which could

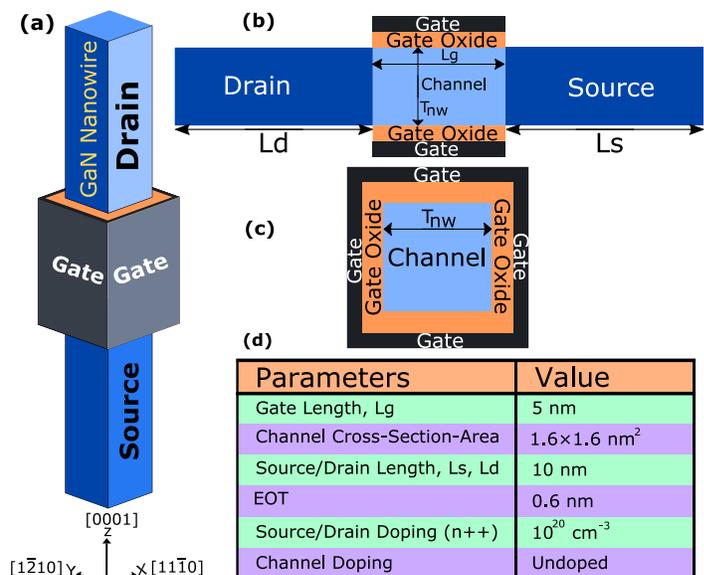
This paragraph of the first footnote will contain the date on which you submitted your paper for review. This work was partly supported by MIT-PISA MISTI program and ONR-PECASE program.

Nadim Chowdhury, Dimitri A. Antoniadis and Tomás Palacios are with Microsystems Technology Laboratories, Massachusetts Institute of

Technology, Cambridge, MA 02139, USA (email : [nadim@mit.edu](mailto:nadim@mit.edu); [daa@mit.edu](mailto:daa@mit.edu); [tomas@mit.edu](mailto:tomas@mit.edu))

## II. SIMULATION APPROACH AND RESULTS

The simulations of Nanowire Transistors (NW-nFETs) performed in this work are based on the self-consistent solution of Poisson and Schrodinger equations within the Non-equilibrium Green Functions framework, on a generic three dimensional domain using the NanoTCAD ViDES simulation environment [13]-[14], which has been extended in order to simulate GaN nanowires.



**Fig. 1:** Schematic of the GaN Nanowire n-MOSFET (GaN-NW-nFET) simulated in this work showing: (a) Device Structure (3-D), (b) 2-D lateral cross-section view, (c) 2-D vertical cross section view, and (d) important device parameters.

The structure of the simulated devices and key device parameters are shown in Fig. 1. The cross-section area of the NW has been carefully chosen, so that the channel length,  $L_g < 6\lambda$  (here  $\lambda = \sqrt{\frac{\epsilon_{channel}}{4\epsilon_{OX}} \times EOT \times T_{NW}}$  is the natural length

Technology, Cambridge, MA 02139, USA (email : [nadim@mit.edu](mailto:nadim@mit.edu); [daa@mit.edu](mailto:daa@mit.edu); [tomas@mit.edu](mailto:tomas@mit.edu))

Giuseppe Iannaccone and Gianluca Fiori are with Dipartimento di Ingegneria dell'Informazione, Università di Pisa, Via G. Caruso 16, 56126 Pisa, Italy (email: [g.fiori@iet.unipi.it](mailto:g.fiori@iet.unipi.it); [giuseppe.iannaccone@unipi.it](mailto:giuseppe.iannaccone@unipi.it))

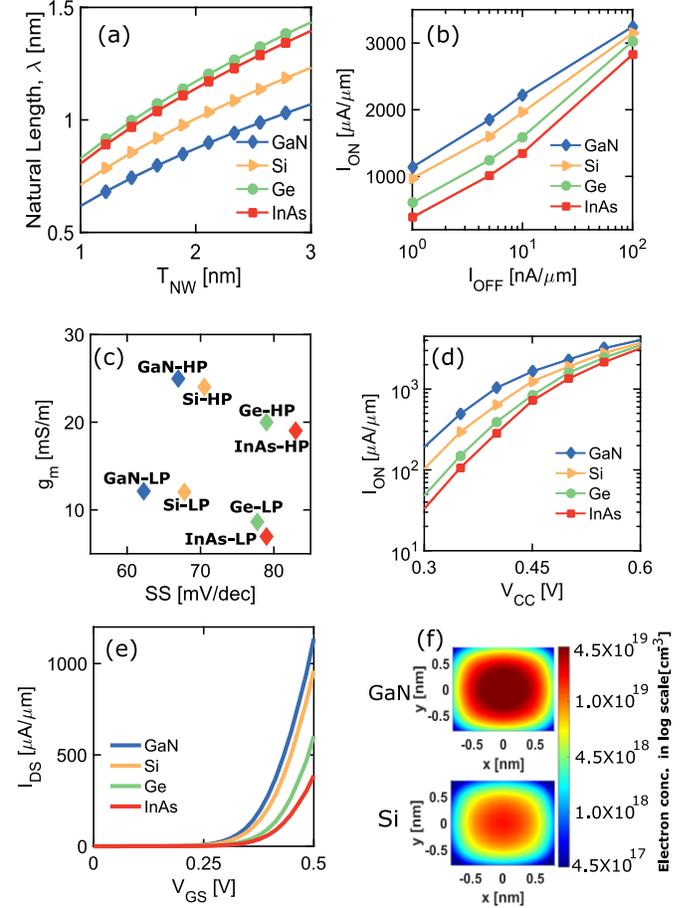
of the device [15]), which allows for the proper mitigation of short channel effects (SCEs). Fig. 2(a) shows variation of  $\lambda$  with the thickness of nanowire for different channel materials. As can be seen, for a given channel thickness GaN has the lowest  $\lambda$  thanks to its relatively low permittivity. Transistor benchmarking for digital applications is traditionally performed with threshold voltage ( $V_T$ ) tuned to obtain a fixed target  $I_{OFF}$ . In this work, the tuning of threshold voltage was performed by tuning the metal work function, *i.e.*, flat-band voltage ( $V_{FB}$ ) keeping all other device parameters fixed. The same device structure (channel length,  $L_g=5$  nm, channel thickness,  $T_{NW}=1.6$  nm and  $EOT=0.6$  nm) has been used to benchmark the performance of GaN-NW-nFET with NW-nFETs of other common semiconductors such as Si, Ge and InAs. Table. 1 lists permittivity, transport effective mass of electron (without including non-parabolicity) and channel orientation of all the semiconductor nanowires used in this study. For Si nanowire transport direction  $\langle 100 \rangle$  is chosen as it yields the highest ON current compared to other directions at this scaled dimensions.

TABLE I: MATERIAL PARAMETERS AND CHANNEL ORIENTATION

Material	Permittivity $\epsilon_r$	Electron effective mass ( $m_{eff}$ )	Transport direction
GaN	8.9	$0.370m_0$ [16]	$\langle 0001 \rangle$
Si	11.8	$0.340m_0$ [17]	$\langle 100 \rangle$
Ge	16	$0.180m_0$ [18]	$\langle 100 \rangle$
InAs	15.15	$0.153m_0$ [19]	$\langle 111 \rangle$

Fig. 2(b) shows the variation of ON current with OFF current for different semiconductor NW-nFETs having the same device structure and a fixed power supply voltage,  $V_{CC}=0.5$  V, neglecting any resistances (both series and contact resistance) at the source and drain ends. At low OFF current of  $1$  nA/ $\mu$ m the ON current for GaN is  $\sim 15\%$  higher than that of Si, whereas at high OFF current of  $100$  nA/ $\mu$ m the ON current of GaN is only  $2.5\%$  higher. This is due to the fact that at low off current the drive current is dominated by subthreshold characteristics whereas at high OFF current this is dominated by both sub and super threshold characteristics. GaN has slightly better subthreshold characteristics compared to Si because of its relatively higher electron effective mass (see Table I), which reduces the source drain direct tunneling leakage. In super threshold zone the performance is mainly dictated by electron velocity which actually reduces as effective mass of electron is increased. To observe both the ON and OFF-state device performance, we plot SS vs intrinsic- $g_m$  in Fig. 2(c) for devices of both Low Standby Power (LP-  $I_{OFF}=1$  nA/ $\mu$ m and  $V_{CC}=0.5$  V) applications and High Performance (HP-  $I_{OFF}=100$  nA/ $\mu$ m and  $V_{CC}=0.5$  V) applications. As, can be seen from this plot, the ON-OFF performance metric  $Q=g_m/SS$  [20] ( $Q_{GaN}=187.79$   $\mu$ S-dec/ $\mu$ m-mV (LP),  $252$   $\mu$ S-dec/ $\mu$ m-mV (HP) and  $Q_{Si}=161$   $\mu$ S-dec/ $\mu$ m-mV (LP),  $187$   $\mu$ S-dec/ $\mu$ m-mV (HP)), is about  $17\%$  higher for LP and  $35\%$  higher for HP in GaN compared to Si channel. In Fig. 2(d) we plot  $V_{CC}-I_{ON}$  (calculated at  $I_{OFF}=10$  nA/ $\mu$ m  $V_{GS}=V_{DS}=V_{CC}$ ) for different semiconductor NW-nFETs. These results show that GaN gives higher  $I_{ON}$  at

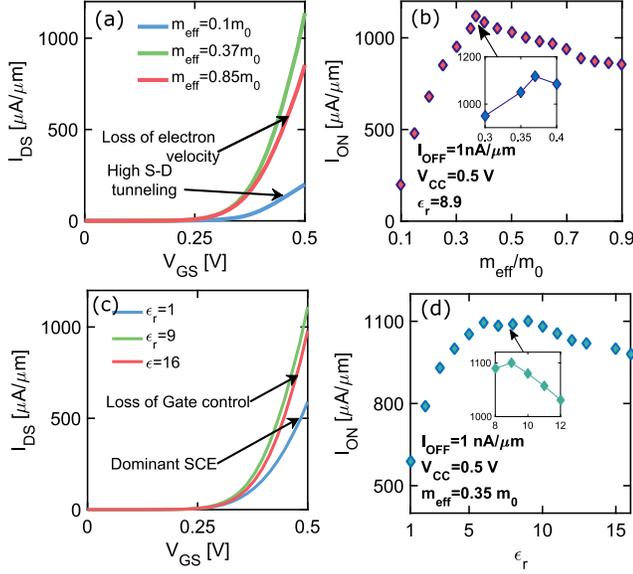
lower  $V_{CC}$  where  $I_{ON}$  is more sensitive to the subthreshold behavior. At  $V_{CC}=0.3$  V,  $I_{ON}$  of GaN is  $1.25\times$  higher than that of Si channel. Fig. 2(e) shows the  $I_{DS}-V_{GS}$  characteristics of all the considered NW transistors at  $I_{OFF}=1$  nA/ $\mu$ m. Electron density cross section profiles of both GaN and Si channel are presented in Fig. 2(f).



**Fig. 2:** (a) Dependence of  $\lambda$  on channel thickness,  $T_{NW}$  of square cross-section nanowire, for different semiconductors. GaN has lower  $\lambda$  compared to other semiconductors making it more immune to short channel effects. (b) Comparison of  $I_{ON}$  vs  $I_{OFF}$  (calculated at  $V_{CC}=0.5$  V) of GaN-NW-nFET ( $L_g=5$  nm) with other semiconductor (Si, Ge, InAs) NW-nFETs having the same device structure and doping level. The GaN-NW-nFET shows  $\sim 15\%$  better  $I_{ON}$  at  $I_{OFF}=1$  nA/ $\mu$ m than Si. (c) Comparison of intrinsic- $g_m$  (calculated at  $V_{GS}=V_{DS}=0.5$  V) vs SS of GaN-NW-nFET with NW-nFETs of other semiconductors (Si, Ge, InAs). These results translate to  $Q=g_m/SS$  (Ref. [20]) of  $188$   $\mu$ S-dec/ $\mu$ m-mV for Low Standby Power (LP-  $I_{OFF}=1$  nA/ $\mu$ m,  $V_{CC}=0.5$  V), and  $252$   $\mu$ S-dec/ $\mu$ m-mV for High Performance (HP-  $I_{OFF}=100$  nA/ $\mu$ m,  $V_{CC}=0.5$  V) applications for GaN which are  $\sim 17\%$  and  $\sim 35\%$  better than Si data for LP and HP respectively. (d) Comparison of  $I_{ON}$  vs  $V_{CC}$  (calculated at  $I_{OFF}=10$  nA/ $\mu$ m  $V_{GS}=V_{DS}=V_{CC}$ ) of GaN-NW-nFET with other semiconductor (Si, Ge, InAs) NW-nFET showing that GaN gives better  $I_{ON}$  at lower  $V_{CC}$ . At  $V_{CC}=0.3$  V  $I_{ON}$  of GaN is  $\sim 1.25\times$  higher than Si. Current and  $g_m$  are normalized by the width of the nanowire. (e)  $I_{DS}$  vs  $V_{GS}$  curves of Si, GaN, Ge and InAs nanowire transistors (f) Electron density (in  $\text{cm}^{-3}$ ) cross section profile in the middle of the channel for both GaN and Si

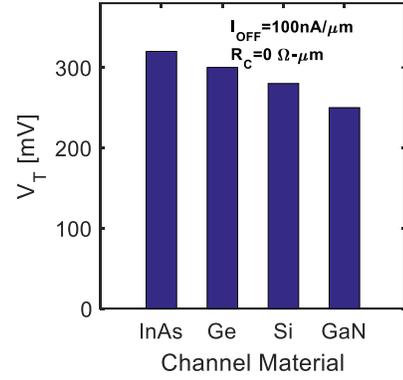
To further investigate the reason behind the superior performance of GaN over other semiconductors in terms of drive current and subthreshold-swing, we study the impact of the two most important channel material parameters: (1) electron effective mass, and (2) relative permittivity on the drive current for the same supply voltage. As shown in Fig. 3(b) there exists an optimum electron effective mass in the channel

material which yields the highest ON current. For low effective mass, the tunneling probability ( $T \propto e^{-\sqrt{m_{eff}}}$ ) increases significantly and degrades the subthreshold behavior (see Fig. 3(a)). Whereas, for very high effective mass, the electron velocity ( $v_e \propto \frac{1}{\sqrt{m_{eff}}}$ ) is reduced yielding a lower drive current ( $I = Q \times v_e$ ). These two factors determine an optimum region for the electron effective mass around  $0.3m_0$ - $0.4m_0$  (see Fig. 3(b)) for LP devices.



**Fig. 3:** (a) Impact of electron effective mass on the  $I_{DS}$ - $V_{GS}$  characteristics for different channel materials. (b)  $I_{ON}$  (calculated at  $V_{GS}=V_{DS}=0.5V$   $I_{OFF}=1nA/\mu m$ ) vs effective mass of channel material (c) Impact of permittivity of the channel material on  $I_{DS}$ - $V_{GS}$  characteristics. (d)  $I_{ON}$  (calculated at  $V_{GS}=V_{DS}=0.5V$   $I_{OFF}=1nA/\mu m$ ) vs permittivity( $\epsilon_r$ ) of the channel material. Here, current is normalized by the width of the nanowire

The effect of the relative permittivity ( $\epsilon_r$ ) of the channel material upon the ON current is shown in Fig. 3(d). As we can see here, when  $\epsilon_r$  is very low (1~5) the drive current is significantly decreased. This is due to the fact that when  $\epsilon_r$  is low, the gate control over the channel diminishes because of reduced effective gate capacitance, resulting in low intrinsic transconductance ( $g_m$ ) and drive current ( $I_{ON}$ ). On the other hand, when  $\epsilon_r$  is very high ( $>15$ ), short channel effects come into the picture (*i.e.*  $\lambda$  increases) and degrade the subthreshold  $-swing$  which in turn degrades the ON current (see Fig. 3(c)). As shown in Fig. 3(d), the optimal relative permittivity values of the channel material lie within 7-13. For the small channel diameters studied in this work, the GaN NW has an electron effective mass of  $0.37m_0$  [16] and relative permittivity of 8.9 [21]. Both of these parameters values fall into optimal zones thus yielding superior ON-OFF performance compared to other commonly used semiconductors. Fig. 4 shows a comparison of the threshold voltage ( $V_T$ ) for different NW-nFETs at  $I_{OFF}=100nA/\mu m$ . Here the threshold voltage has been extracted by extrapolation of the linear region  $I_{DS}$ - $V_{GS}$  characteristics. As demonstrated in this graph, the GaN channel offers the lowest  $V_T$  (*i.e.* 250mV) whereas InAs channel gives the highest,  $V_T=320mV$ .



**Fig. 4:** Comparison of threshold voltage ( $V_T$ ) of GaN-NW-nFET with other semiconductor NW-nFET having same device structure. For the same OFF current of  $100nA/\mu m$ , the GaN channel requires lower  $V_T$  because of its better subthreshold behavior due to its higher effective mass. Here it is worth mentioning that in this work a basic gate metal work function of 4.2 eV has been used and then it is varied in the range of hundreds of milli-eVs ( $10^{-3}eV$ ) to match the targeted OFF current.

Since, the OFF current is given by  $V_T \sim -SS \times \log(I_{OFF})$ , the channel material that has the lowest SS yields the lowest  $V_T$  when tuned at the same OFF current. As the GaN channel has the best sub-threshold behavior (*i.e.* lowest SS) because of its higher  $m_{eff}$ , it yields the lowest  $V_T$  thereby obtaining the highest ON current for the same supply voltage,  $V_{CC}$ .

### III. CONCLUSION

In this paper, we presented performance projection of GaN-NW n-FET with 5 nm channel length and benchmark that with NW-nFETs of other semiconductors like Si, Ge and InAs. In terms of performance parameters such as  $I_{ON}$ , SS, and  $g_m$ , GaN outperforms other semiconductors mainly because of its relatively higher electron effective mass-which reduces source to drain direct tunneling and lower permittivity-which yields better short channel characteristics. From the detailed comparison presented here, it can be concluded that GaN NW n-FET can provide best drive current and ON-OFF characteristics for both Low Standby Power and High Performance applications compared to other semiconductors in transistors with an  $L_g=5nm$ .

### REFERENCES

- [1] Y. Cai, Z. Cheng, Z. Yang, W. C.-W. Tang, K. M. Lau, and K. J. Chen, "High temperature operation of AlGaIn/GaN HEMTs direct-coupled FET logic (DCFL) integrated circuits," *IEEE Electron Device Lett.*, vol. 28, no. 5, pp. 328-331, May 2007. DOI: 10.1109/LED.2007.895391
- [2] C. Bulutay, B. K. Ridley, and N. A. Zakhleniuk, "Full-band polar optical phonon scattering analysis and negative differential conductivity in wurtzite GaN," *Physical Review B*, 62.23, 15754-15763, Nov, 2000. DOI: 10.1103/PhysRevB.62.15754
- [3] M. Lundstrom, *Fundamentals of carrier transport*. Cambridge University Press, July 2009. DOI: 10.1088/0957-0233/13/2/703
- [4] E. Mاتيoli, and T. Palacios, "Room-Temperature Ballistic Transport in III-Nitride Heterostructures," *Nano letters* 15.2, 1070-1075, Jan. 2015. DOI: 10.1021/nl504029r
- [5] K. Shinohara, D.C. Regan, Y.Tang, A.L. Corrión, D.F. Brown, J.C. Wong, J.F. Robinson, H.H. Fung, A. Schmitz, T.C. Oh and S.J. Kim, "Scaling of GaN HEMTs and Schottky diodes for submillimeter-wave MMIC applications," *IEEE Transactions on Electron Devices*, 60(10), pp.2982-2996, Oct. 2013. DOI: 10.1109/TED.2013.2268160

- [6] N. Tansu, H. Zhao, G. Liu, X.H. Li, J. Zhang, H. Tong and Y.K. Ee, "III-nitride photonics," *IEEE Photonics Journal*, 2(2), pp.241-248, Oct. 2010. DOI: 10.1109/JPHOT.2010.2045887
- [7] D. Jena, S. Heikman, D. Green, D. Buttari, R. Coffie, H. Xing, S. Keller, S. DenBaars, J.S. Speck, U.K. Mishra and I. Smorchkova, "Realization of wide electron slabs by polarization bulk doping in graded III-V nitride semiconductor alloys," *Applied physics letters*, 81(23), pp.4395-4397, Nov. 2002. DOI: 10.1063/1.1526161
- [8] Y. Li, C. H. Hwang and T. Y. Li, "Random-dopant-induced variability in nano-CMOS devices and digital circuits," *IEEE Transactions on Electron Devices*, 56(8), pp.1588-1597, Oct. 2009. DOI: TED.2009.2022692
- [9] H.W. Then, S. Dasgupta, M. Radosavljevic, L. Chow, B. Chu-Kung, G. Dewey, S. Gardner, X. Gao, J. Kavalieros, N. Mukherjee and M Metz., "Experimental observation and physics of "negative" capacitance and steeper than 40mV/decade subthreshold swing in Al<sub>0.83</sub>In<sub>0.17</sub>N/AlN/GaN MOS-HEMT on SiC substrate," *IEEE International Electron Devices Meeting*, pp. 28-3, December, 2013. DOI: 10.1109/IEDM.2013.6724709
- [10] R.K. Jana, A. Ajoy, G. Snider and D. Jena, "Sub-60 mV/decade steep transistors with compliant piezoelectric gate barriers," *IEEE International Electron Devices Meeting*, pp. 13-6, Dec. 2014. DOI: 10.1109/IEDM.2014.7047047
- [11] K. Shinohara, D. Regan, A. Corrión, D. Brown, S. Burnham, P.J. Willadsen, I. A.-Rodríguez, M. Cunningham, C. Butler, A. Schmitz and S. Kim. December. "Deeply-scaled self-aligned-gate GaN DH-HEMTs with ultrahigh cutoff frequency," *International Electron Devices Meeting*, pp. 19-1, Dec. 2011. DOI: 10.1109/IEDM.2011.6131582
- [12] M.S. Shur, "GaN based transistors for high power applications," *Solid-State Electronics*, 42(12), pp.2131-2138, Dec. 1998. DOI: 10.1016/S0038-1101(98)00208-1
- [13] <http://vides.nanotcad.com/vides>
- [14] G. Fiori, G. Iannaccone "Multiscale Modeling for Graphene-Based Nanoscale Transistors," *Proceedings Of IEEE*, Vol. 101, p. 1653-1669, July 2013. DOI: 10.1109/JPROC.2013.2259451
- [15] I. Ferain, C.A. Colinge and J.P. Colinge, "Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors," *Nature*, 479(7373), pp.310-316, Nov. 2011. DOI: 10.1038/nature10676
- [16] D.J. Carter, J.D. Gale, B. Delley and C. Stampfl, "Geometry and diameter dependence of the electronic and physical properties of GaN nanowires from first principles," *Physical Review B*, 77(11), p.115349, March 2008. DOI: 10.1103/PhysRevB.77.115349
- [17] Y. Zheng, C. Rivas, R. Lake, K. Alam, T.B. Boykin and G. Klimeck, "Electronic properties of silicon nanowires," *IEEE transactions on electron devices*, 52(6), pp.1097-1103, May 2005. DOI: 10.1109/TED.2005.848077
- [18] M. Bescond, N. Cavassilas, K. Nehari and M. Lannoo, "Tight-binding calculations of Ge-nanowire bandstructures," *Journal of Computational Electronics*, 6(1-3), pp.341-344, 2007.
- [19] C.L.D. Santos and P. Piquini, "Diameter dependence of mechanical, electronic, and structural properties of InAs and InP nanowires: A first-principles study," *Physical Review B*, 81(7), p.075408, July 2010. DOI: 10.1103/PhysRevB.81.075408
- [20] G. Doornbos, and M. Passlack, "Benchmarking of III-V n-MOSFET maturity and feasibility for future CMOS," *IEEE Electron Device Letters*, 31(10), pp.1110-1112, Oct. 2010. DOI: 10.1109/LED.2010.2063012
- [21] M.E. Levinshtein, S.L. Rumyantsev and M.S. Shur, *Properties of Advanced Semiconductor Materials: GaN, AlN, InN, BN, SiC, SiGe*. John Wiley & Sons. Feb. 2001.