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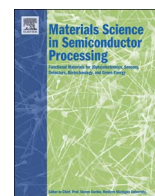
Materials and processing issues in vertical GaN power electronics

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ABSTRACT

Silicon-based power devices are reaching their fundamental performance limit. The use of wide-bandgap semiconductors with superior material properties over silicon offers the potential for power electronic systems with much higher power densities and higher conversion efficiency. GaN, with a high critical electric field and carrier mobility, is considered one of the most promising candidates for future high-power, high frequency and high temperature applications. High voltage transistors and diodes based on both lateral and vertical structures are of great interest for future power electronics. Particularly, vertical GaN power devices have recently attracted increasing attention due to their many unique properties. This paper reviews recent progress and key remaining challenges towards the development of high-performance vertical GaN transistors and diodes with emphasis on the materials and processing issues related to each device architecture.

1. Introduction

Power electronics is the application of electronic switching devices for efficient conversion and the control of electrical power [1]. For the past 60 years, silicon-based power devices have been the dominant player used in power circuits to accomplish these tasks. The design of new device structures such as thyristors and insulated gate bipolar transistors (IGBT) and the optimization of the fabrication processes have enabled a significant improvement in device performance. However, Si-based power devices are now reaching their theoretical limit. Innovation in power devices is needed to further improve the performance of power electronics and bring us closer to realize a sustainable society.

Wide-bandgap (WBG) semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) are promising material candidates for the next generation power devices. Due to their high critical electric field, WBG semiconductors can enable the fabrication of power devices with lower capacitance and resistance for a given breakdown voltage than their Si counterparts. Table 1 shows the comparison of material parameters for GaN with Si and SiC. The Baliga's figure of merit (BFOM) ($\varepsilon_S \mu_n E_C^3$) [2,3], which describes the fundamental relationship between on-resistance and breakdown voltage (BV), shows that GaN promises the best performance among the current candidates for power electronics. GaN-based devices can meet the increasing performance demands of the evolving power systems, operating at higher power densities and temperatures than existing Si power devices.

Lateral power transistors and diodes based on AlGaN/GaN heterostructures have already demonstrated excellent electrical characteristics [4–9], and enhancement-mode GaN products are commercially available since June 2009 [10]. However, the power handling of GaN transistors with a lateral configuration is typically limited to a few kW. For higher power ratings, the chip size of lateral GaN transistors increases significantly, resulting in inefficient utilization of the material, difficult current extraction, and poor reliability. The vertical buffer breakdown also limits the operating voltage of the device below 1 kV due to the difficulty of growing thicker (Al)GaN layers on a silicon substrate [11]. Additionally, lateral GaN transistors and diodes suffer from electron trapping at the surface due to the presence of high surface electric field under off-state operation [12,13]. This current collapse phenomenon can severely degrade the device performance and affect its long-term stability and reliability, especially for very high-voltage operations [14,15].

Power devices based on vertical GaN are promising candidates to overcome the challenges described above for the lateral GaN transistors. The breakdown voltage in vertical GaN devices can be increased by increasing the thickness of the drift region, while keeping the device footprint constant. The maximum electric field in vertical GaN devices is far away from the surface, which minimizes trapping effects and reduces dynamic on-resistance. Moreover, the vertical current extraction in vertical GaN transistors allows for the delivery of much higher power density than in lateral GaN devices. In vertical GaN devices, the electric field is more uniform and current distribution is much more

Table 1
Comparison of material parameter and BFOM for Si, SiC and GaN.

	Si	SiC	GaN
ϵ_r(-)	11.7	9.7	8.9
μ_n(cm^2 V^{-1} s^{-1})	1350	1100	1100
E_C(MV/cm)	0.2	2	3.75
BFOM	1	675	3713

spread, giving rise to a superior thermal performance than lateral GaN devices [16]. Recently, various transistor and diode architectures based on vertical GaN have been reported. Vertical GaN p-n diodes with breakdown voltage over 4 kV [73] and vertical GaN trench metal-oxide-semiconductor field effect transistor (MOSFET) with blocking voltage of 1.6 kV [18] have been demonstrated on free-standing GaN substrate. To reduce the substrate cost, quasi- and fully vertical GaN-on-Si power diodes with excellent performance have also been recently demonstrated with a BV over 500 V [19].

This paper summarizes the recent progress of vertical GaN power electronics and highlights the issues related to the material growth and device fabrication. The paper is organized as follows. Section 2 deals with the material growth and doping control. Section 3 introduces various vertical GaN transistors and discuss the issues of device processing. Section 4 reviews the progress on vertical GaN diodes/rectifiers on both free-standing GaN substrate and Si substrate, and benchmarks the performance.

2. Materials growth and doping

2.1. GaN substrate

The demands for high-quality bulk GaN in solid-state lighting and power electronics have driven the development and commercialization of bulk GaN substrate. The classical Czochralski crystal growth process commonly used for the growth of silicon and GaAs cannot be used for GaN, due to its extreme conditions of melting. Therefore, the most common and cost-effective approach for manufacturing GaN substrates today is the hydride vapor phase epitaxy (HVPE) [17,18], which is able to produce high-quality material at high growth rate [22]. The HVPE growth of GaN substrate is described in Fig. 1(a). Freestanding GaN crystals are typically grown on foreign substrates followed by substrate lift-off process. Fig. 1(b) shows the thermal expansion coefficient of typical substrates and their lattice mismatch with GaN [20]. The first HVPE-GaN was reported by Maruska et al. in 1969, using sapphire as the substrate [23]. However, the large mismatch in the thermal expansion coefficients between GaN and the sapphire substrate typically creates cracking in the GaN layer. The lower mismatch in the thermal

expansion coefficient makes GaAs a better substrate candidate to avoid cracks and reduce wafer bending [20]. Furthermore, GaAs can be etched away easily by aqua regia [24] or by mechanical grinding and lapping [20]. In 2000, Motoki et al. successfully prepared 2-inch free-standing GaN substrates using GaAs as a starting substrate for the first time. However, a large number of dislocations (in the order of 10^9 cm^{-2}) form at the interface between GaN and the foreign substrates, due to the large mismatch in crystal lattice. The threading dislocation density (TDD) of the GaN layers on GaAs can be reduced to 10^6–10^7 cm^{-2} by utilizing the void associated separation (VAS) method [25]. By using additional dislocation-reduction techniques [26], the TDD can be even reduced to 10^4 cm^{-2} over an area of ~ mm^2. To illustrate the importance of foreign substrate selection on the TDD, Fig. 2 compares the dislocation density of GaN crystal grown on sapphire and GaAs by using HVPE. Bulk GaN substrate with low TDD is of particular importance for vertical GaN power devices. In [25], a p-n diode with breakdown voltage over 3000 V has been fabricated by using VAS GaN substrate with reduced dislocation density. Currently, "native" GaN substrates are available in wafer diameters up to 6-in. However, the substrate cost is high and becomes a significant component of the total cost of the device due to limited production volume.

To reduce the cost of the substrate, there is an important effort worldwide to grow GaN on large silicon wafers. This growth is, however, challenging due to the large mismatch in thermal expansion coefficient and lattice constant between GaN and silicon [Fig. 1(b)], which results in difficulties to grow high-quality and thick n$^+$-GaN/n$^-$-GaN layers by using silicon as a carrier. The TDD of GaN epilayers grown on silicon is ~ 10^9 cm^{-2}, and the thickness of the entire GaN stack is limited to a few microns, making the fabrication of high voltage vertical devices very difficult.

2.2. n-type GaN by metal-organic chemical vapor deposition

For high-voltage vertical GaN devices, the thickness and doping of the n$^-$-GaN drift region that blocks most of the voltage needs to be well-designed and controlled. This layer is typically grown by using metal-organic chemical vapor deposition (MOCVD) for both GaN-on-GaN and GaN-on-Si technologies. Fig. 3 shows the cross-section of the basic device epitaxial-structure, highlighting the lightly doped GaN drift region and the electric field profile in the drift layer when the critical electric field (E_C) is reached. From electrostatics, the breakdown voltage (BV) can be described as [27]

$$BV = E_C W - \frac{qN_D W^2}{2\epsilon_S} \tag{1}$$

where W is the thickness of the n$^-$-GaN drift layer, q is the electron charge, ϵ_S is the permittivity of GaN, and N_D is the net carrier density of
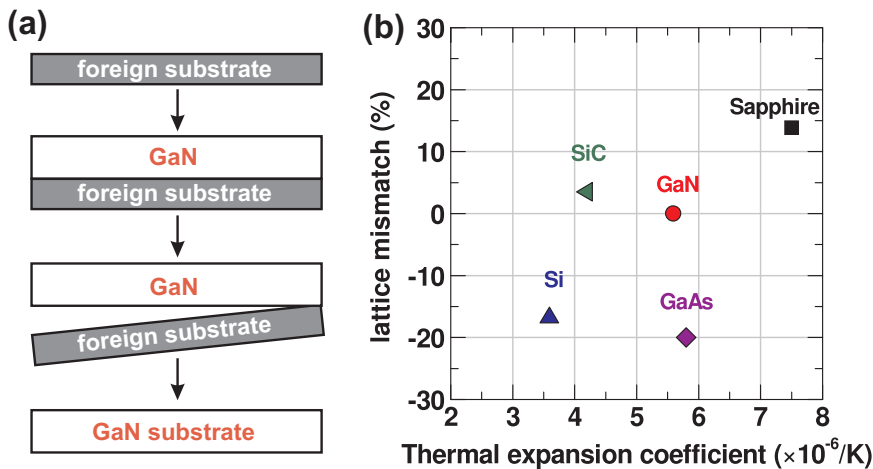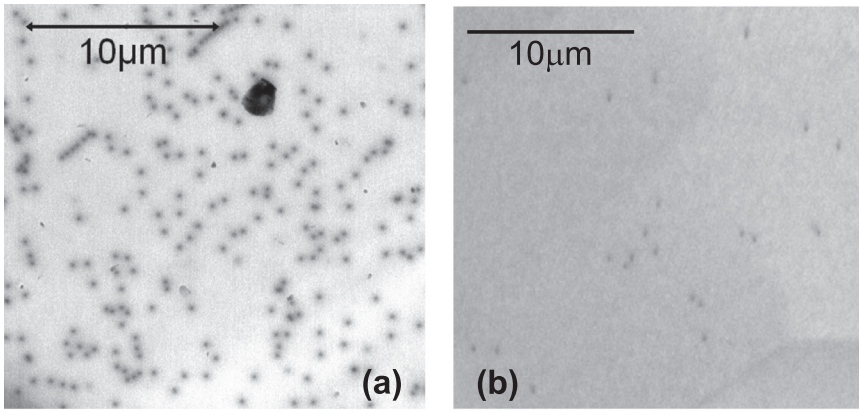
Fig. 2. Plan-view cathodoluminescence (CL) images showing threading dislocation as dark spots for GaN grown on sapphire substrate (a) and on GaAs substrate (b) [21].

the n⁻ GaN layer. Fig. 4 benchmarks the breakdown voltage vs drift layer thickness in vertical GaN power devices on GaN and silicon substrates from literature. The solid lines represent the theoretical limit of the BV as a function of the drift layer thickness for 3 different doping concentration levels in the drift layer. As shown in the figure, the thickness of the GaN drift layer in GaN-on-silicon technology is currently limited to about 5 μm.

From the equation above and the results in Fig. 4, it is clear that the net carrier concentration in the drift layer plays a crucial role and that it should be kept below 10^{16} cm⁻³ to achieve high breakdown voltage. It is however difficult to achieve reproducible doping densities in the 10^{15}–10^{16} cm⁻³ range by MOCVD [28]. It was reported that the MOCVD-(Al)GaN epitaxial layers can be incoporated with impurities including Oxygen, Carbon, etc. Oxygen as a shallow donor in Wurtzite GaN with a transition to a DX-like state under hydrostatic pressure has been studied by first-principle calculation and experiments [29,30]. It was also found out that Oxygen incorporation was less susceptible to growth conditions than that of carbon [31]. The carbon incorporation is introduced by the gallium source in MOCVD (i.e. trimethyl gallium (TMG) or triethyl gallium) [32]. By growing the GaN under an optimized MOCVD conditions at high temperature, high growth pressure and a high V:III ratio, the carbon background doping can be reduced to 10^{15}–10^{16} cm⁻³ range [28]. Thus the net doping (N_D–N_A) in the GaN drift region can be controlled through the silicon concentration (donor N_D), which is determined by the flow rate of diluted silane [28,32]. It should be noted that the control of the net doping in GaN should take into account of all impurities (O, H, C, etc.). It is generally assumed that carbon creates deep acceptor states in GaN by sitting at the nitrogen site, compensating the intentional donors. However, Tanaka et al. recently reported that donor-like C_{Ga} (gallium-site carbon) can appear when the carbon concentration is low. Ref. [32] proposes a two-level C_{Ga}–C_N model which highlights that the control of the residual carbon
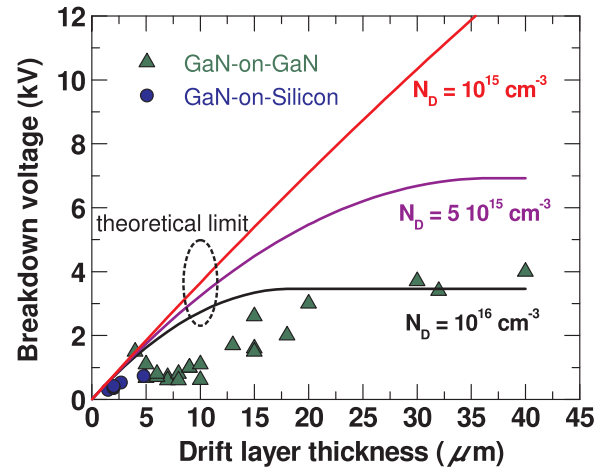

Fig. 4. The breakdown voltage versus drift layer thickness for various vertical GaN transistors and diodes. The solid lines represent the theoretical limit of the BV as a function of the drift layer thickness for different doping concentration of the drift layer.

concentration in the n-GaN drift layer is essential to maintain high-voltage operation of GaN power devices without degrading the on-resistance.

2.3. Activation of implanted p-type GaN

The success of many vertical Si and SiC power devices relies on the p-type regions to form junction termination extension (JTE) structures [35] and avoid electric field crowding at the edge of the junction, thus achieving high breakdown voltage [36]. Vertical GaN power devices can benefit from selective p-type doping in implanted guard rings for
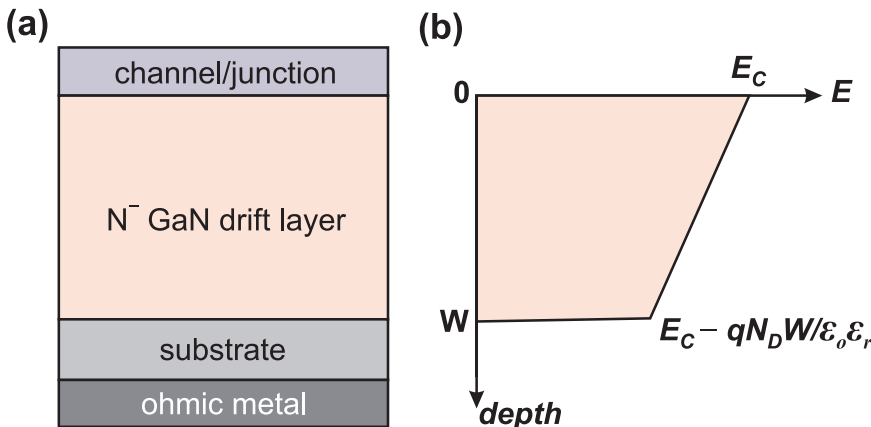

Fig. 3. (a) Cross-section schematic of the device epi-structure highlighting the lightly doped GaN drift layer. (b) The electric field profile in the drift layer when breakdown phenomenon is occurring.

electric field spreading, merged pn/Schottky (MPS) structures to protect surge currents, and current blocking layers (CBL) for the current aperture vertical electron transistors (CAVET) [37,38]. However, the activation of implanted p-type dopant (i.e. Mg) requires an annealing temperature over 1300 °C [39], which causes the decomposition of GaN at atmospheric pressure. The decomposition brings about a loss of nitrogen, surface damage and the creation of nitrogen vacancies [33,40]. In order to prevent the loss of nitrogen loss at the GaN surface, it is desirable to deposit a high-quality capping layer before the annealing step, followed by a reliable removal process after annealing [41]. Moreover, permanent clusters can be formed during the Mg implantation, and N vacancy complexes can prevent Mg diffusion into the Ga vacancy sites during the activation annealing [41]. Due to these issues, the energy and dose of the implanted Mg species are currently limited [41].

To overcome the issues above, Feigelson et al. combined a multi-cycle rapid thermal annealing (MRTA) process in a controlled N_2 overpressure with an AlN cap deposited by chemical vapor deposition (CVD) [39]. The MRTA process enabled the activation of implanted Mg with activation efficiency of over 8% and the demonstration of p-type conductivity [42]. Although the implantation-induced lattice damage can be restored by the proposed MRTA process, additional structural changes in the GaN sample were created because of the process with rapid heating and cooling cycles [33]. To overcome this issue, a modified MRTA process has been developed by introducing an conventional annealing step after the multi rapid heating and cooling cycles as shown in Fig. 5. It was also demonstrated that this symmetric MRTA (SMRTA) process can improve the p-type conductivity in the samples compared with those annealed with the MRTA process [33].

High performance vertical GaN junction barrier Schottky (JBS) rectifiers have been recently demonstrated by using implanted Mg in n-GaN followed by activation using the SMRTA process [34]. The annealing procedure consists of a 1000 °C anneal for 30 min, followed by 40 pulses of 20 s up to 1350 °C for each cycle, and another 1000 °C anneal for 30 min. Fig. 6 (a) shows the rectifying behavior of the implanted Mg pn diode with a turn-on voltage of ~ 3.5 V. Fig. 6(b) presents the $I-V$ curves for the "ohmic" contacts formed on implanted Mg regions. Due to a low acceptor concentration (~ 5×10^{16} cm^{-3}) in the p-GaN, the TLM I-V curves are not perfectly linear. These device results demonstrate the successful p-type implant activation, which will be a key enabling step for next-generation vertical GaN power electronics [34].

3. Vertical GaN power devices

Thanks to the recent progress in GaN material growth and device processing, several device architectures based on vertical GaN have been proposed. In this section, we will introduce each device structure and discuss their specific processing challenges.
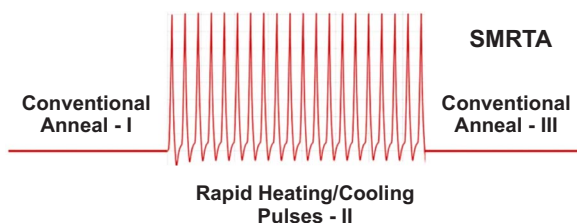

Fig. 5. Schematic of the temperature profiles for the Symmetric Multicycle Rapid Thermal Annealing (SMRTA) process. The SMRTA process includes three stages: a preliminary conventional anneal, rapid heating/cooling cycles, and a final conventional anneal [33].

3.1. Vertical GaN transistor

Fig. 7 shows four different architectures for vertical GaN transistors fabricated on free-standing GaN substrate. In 2004, Ben Yaacov et al. [37] proposed a current aperture vertical electron transistor (CAVET) structure [Fig. 7(a)], similar to a double diffused metal-oxide-semiconductor (DMOS) structure. One of the key challenges in the CAVET is to design a robust current blocking layer (CBL) to suppress the leakage current in the vertical direction. In the first demonstration of CAVET, the CBL was formed with Mg-doped GaN grown by MOCVD to create an energy barrier below the source. In this case, the aperture region requires dry-etching of the Mg-doped GaN and a regrowth of the n-GaN channel. It was reported that etching of the aperture region exposes non-c planes and regrowth on such facets can result in a non-planar surface. This leads to severe gate leakage current [37]. Other studies showed that high concentration of n-type impurities tend to incorporate in the aperture region. This causes an increase of the peak electric field in the channel and a reduction of the device breakdown voltage. To circumvent these issues, a selective Mg-ion-implanted GaN layer was used as the CBL without the regrowth of the GaN in the aperture region [38]. However, the AlGaN/GaN layers were grown by MOCVD on top of the Mg-doped CBL. Memory effects related to Mg induced Mg out-diffusion into the AlGaN/GaN layers [43], giving rise to reliability issues. To suppress the diffusion of Mg and improve the yield and reproducibility, Chowdhury et al. used Plasma-MBE technique to grow AlGaN/GaN layers at low temperature (720 °C) [44]. AlGaN/GaN CAVET with a combination of MOCVD and MBE-growth techniques has demonstrated excellent performance with good repeatability, making it very promising for power electronics.

Another critical issue related to the original CAVET structure is its intrinsic normally-on operation and poor pinch-off capability [38,46]. Shibata et al. proposed a new vertical GaN transistor by using a trench CAVET structure [45]. The device features a regrowth of p-type gate/AlGaN/GaN epitaxial layers over the V-groove [Fig. 7(b)]. It was shown that the polarization charges at the AlGaN/GaN heterojunction reduce with the increase of the titled angle from the c-plane. Fig. 8 shows that the lateral p-type gate transistor with a slanted channel leads to 1.5 V higher V_{TH} compared to the transistor fabricated on the c-plane. By implementing the trench CAVET structure, a high V_{TH} of 2.5 V was achieved. In both CAVET and trench CAVET structures, the leakage path through the CBL causing the punch-through current can limit its high-voltage operation. It is mainly attributed to the activation inefficiency of the Mg-doped p-type layer. In [45], a thin carbon-doped GaN layer was inserted to reduce the leakage current in the p-GaN region. A hybrid blocking layers (HBLs) with a carbon-doped GaN and p-type GaN well layer successfully reduces the punch-through effect and improves the BV from 580 V to 1.7 kV.

A second type of vertical GaN transistor is the vertical trench MOSFET [Fig. 7(c)] which has the advantage of high packing density and the absence of the JFET region [48,49]. One of the main challenges of trench MOSFET is to obtain a reliable positive V_{TH} for real normally-off operation. In [50], the channel of the GaN MOSFET is fabricated on (0001) plane, where spontaneous and piezo-electric polarization effects are present. This channel formation results in poor pinch-off capability of the MOSFET due to the charges induced at the GaN/dielectric interface. Therefore, it is attractive to use a non-polar surface by trench etching on (0001) plane GaN [51]. The dry etching for the trench formation is performed by using Cl_2/BCl_3 gases. However, the increased surface roughness and the damage by the ion bombardment make the dry-etched surface unsuitable for the gate channel region. Therefore, post-treatment of the etched surface is necessary for smoothing the surface and removing the damage [52]. Itoh et al. reported a smooth (1$\bar{1}$00) plane by using KOH wet etching [53]. To avoid the contamination from alkaline metal, TMAH-based wet clean was used to achieve smooth non-polar (1$\bar{1}$00) plane [51]. Recently, a damage-free corner rounding technology was developed by using
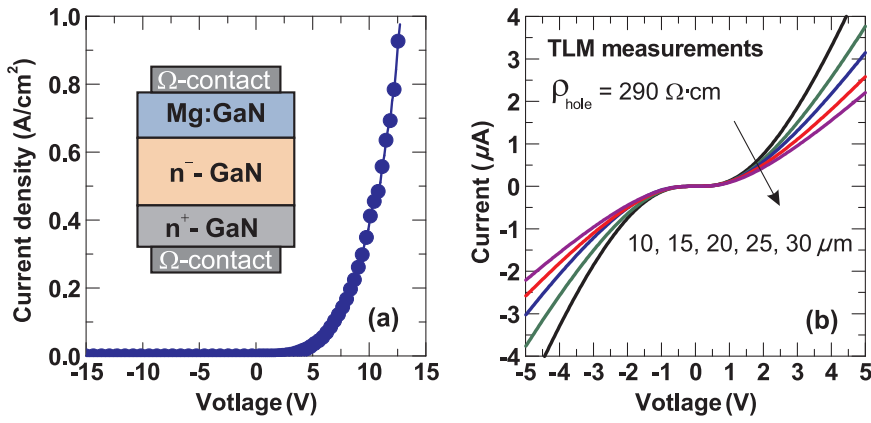
Fig. 6. (a) Forward I-V characteristic for the Mg-implanted p-n diode. (b) TLM I-V curves for the ohmic contacts formed on Mg-implanted regions [34].
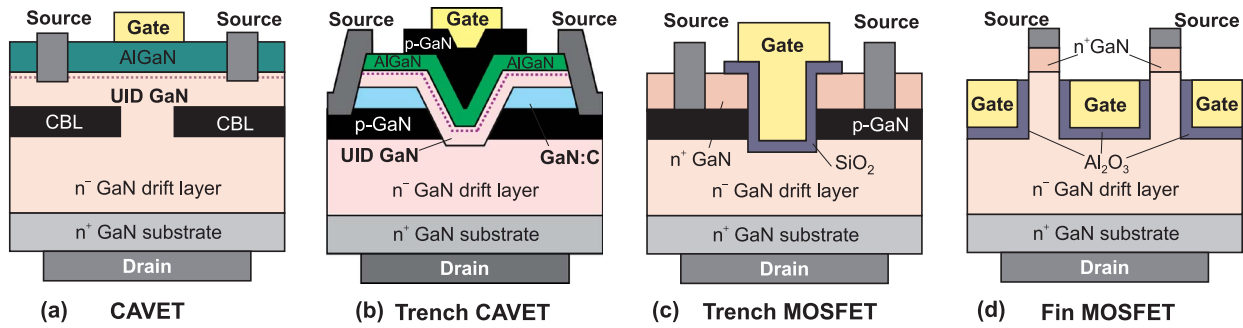

Fig. 7. Schematic of representative vertical GaN transistors: (a) current aperture vertical electron transistor (CAVET), (b) trench CAVET with V-shaped regrowth channel, (c) trench metal-oxide-semiconductor field effect transistor (MOSFET), (d) vertical fin MOSFET.
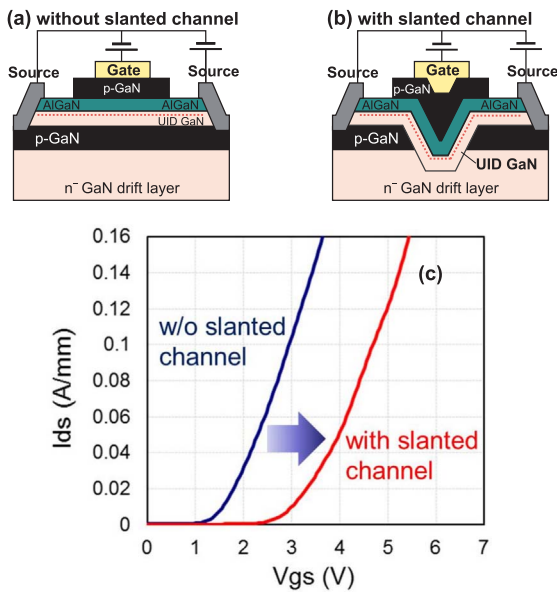

Fig. 8. (a) Lateral transistor with a p-type gate without using a slanted channel. (b) The lateral transistor with a p-type gate structure in a slanted channel. (c) The comparison of the transfer characteristics of the two transistors. By using a slanted channel, 1.5 V higher V_{TH} can be obtained compared to the transistor without slanted channel [45].

Tetramethylammonium hydroxide wet etching and piranha clean [52]. By optimizing the ICP dry etching conditions and applying the rounding technology, different trench shapes such as flat-bottom rounded trench and tapered-bottom rounded trench have been demonstrated. The U-shape trench with rounded corners and smooth sidewalls is optimal to achieve high-voltage vertical GaN power devices, due to the suppression of the electric field crowding at the corners [52].

Due to the lack of suitable native oxide, the gate stability is always a concern for GaN-based MOSFET. In [49], an AlN/SiN dielectric stack grown by MOCVD was used. However, a hysteresis of $\sim$ 0.6 V was observed from gate bias double-sweeps. This hysteresis indicates the existence of interface states at the gate dielectric and the p-GaN sidewall or border traps in the gate dielectric. To ensure an improved step coverage, atomic layer deposited (ALD) SiO_2 was deposited as gate dielectric in [54]. A hysteresis of $\sim$ 0.5 V was also seen in the GaN MOSFET with ALD SiO_2 as the gate dielectric.

In the GaN CAVET and Trench MOSFET structures, epitaxial regrowth or p-GaN layer for the CBL or channel layer is required. This increases the process complexity and introduces additional epitaxial cost. Additionally, the poor transport properties of the inverted p-GaN channel results in high on-resistance [54–56,48]. Recently, a normally-off GaN vertical fin MOSFET [Fig. 7(d)] with excellent performance has been demonstrated [47]. One key feature of this novel fin MOSFET is that only n-GaN epitaxial layers are used, while no regrowth or p-GaN layer is needed to achieve high-voltage blocking capability at V_{GS} of 0 V. The enhancement-mode operation of this fin vertical MOSFET relies on the submicron fin technology and the control of the doping in the n-GaN channel. Fig. 9(a)-(c) show the simulated electron density in the fin structure for different fin width, where the Si doping concentration in the n-GaN drift layer is $\sim 2 \times 10^{16}$ cm^{-3}. As the fin width scales down to 200 nm or below, the channel in the fin is fully depleted. This allows for normally-off operation and the suppression of punch-through leakage currents. Moreover, the subthreshold slope of the transfer curves is also improved by scaling down the fin width without sacrificing the on-state current [Fig. 9(d)-(e)]. With a channel fin width of 180 nm, the GaN fin MOSFET with a threshold voltage of 1.0 V and an excellent subthreshold swing of 75 mV/dec was demonstrated. The normalized on-resistance (to the total active fin area) of this device is 0.36 mΩ cm^2. A further reduction of the on-resistance can be achieved by optimizing the ohmic annealing temperature, although a careful optimization is needed to not increase the gate leakage current [47].
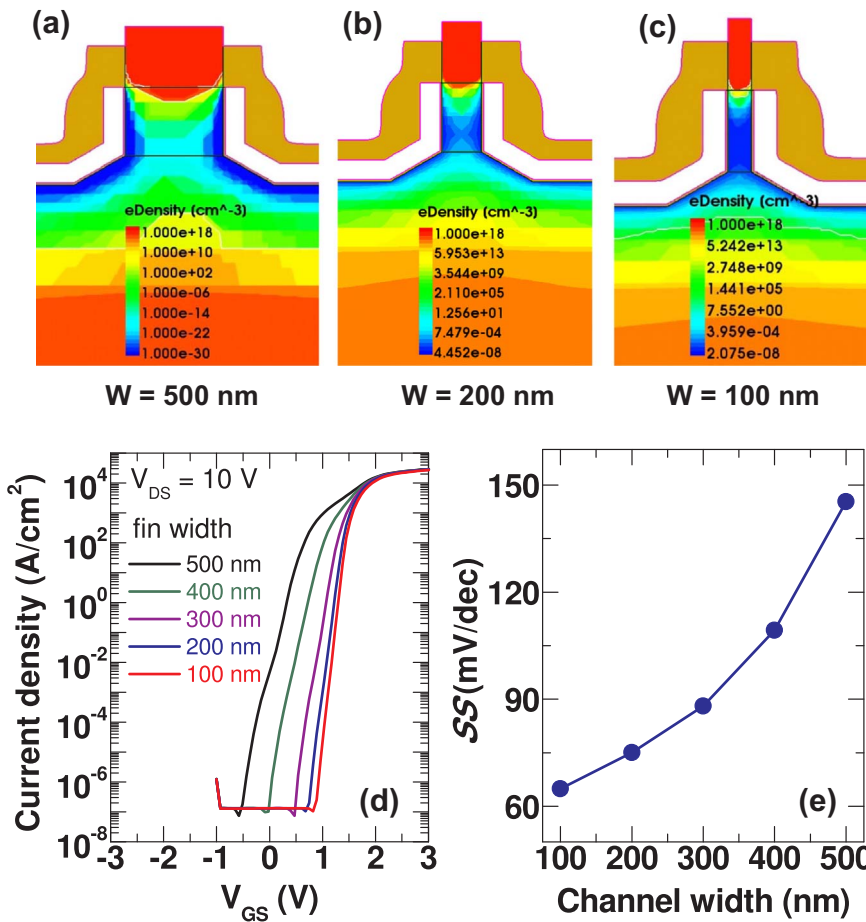
Fig. 9. (a)-(c) Simulated electron density distribution in the fin at equilibrium for fin width of 500 nm, 200 nm, and 100 nm, respectively. (d) Simulated transfer characteristics for different fin width at VDS of 10 V. (e) Simulated subthreshold slope (SS) as a function of the fin width.

In order to obtain smooth sidewalls in the fin, a Cl_2/BCl_3-based dry etch is performed followed by a wet etch based on hot TMAH [47,57]. It was found out that the sidewalls are very rough showing many triangular shapes, when the fins were aligned to m-plane ($<1\bar{1}00>$), since wet etching of GaN is dependent on the crystal orientation [53]. By aligning the fin to the a-plane instead of m-plane, a much smoother sidewalls of the fin were obtained. In the gate fabrication, a 15-nm Al_2O_3 is used as the gate dielectric by atomic layer deposition (ALD). A sputtered molybdenum is deposited as the gate metal. The conformal process enabled by ALD and sputtering is essential to avoid electrical short between gate and source. Additionally, a SiO_2 spacer was used to allow the isolation between the gate and source electrodes.

In the vertical fin transistors under off-state operation, a high peak electric field is present at the edge of the gate and at the bottom of the fins in the GaN. Without a design of edge termination structure [Fig. 10(a)], the breakdown voltage (BV) is limited to 100 V. With the implementation of a gate field plate [Fig. 10(b)], the BV is increased to 400 V. The breakdown mechanism in these structures is attributed to the failure of the gate dielectric due to a concentrated electric field at the edge. To avoid this pre-mature degradation, a 100-nm thick oxide layer was deposited in the etched trench to reduce the electric field in the ALD Al_2O_3 gate dielectric. This has increased the BV up to 800 V. From gate bias double-sweeps, no hysteresis was observed indicating a very good interface between the ALD Al_2O_3 and the GaN sidewalls. Extensive reliability studies on this device are still on-going to investigate its degradation mechanisms [58].
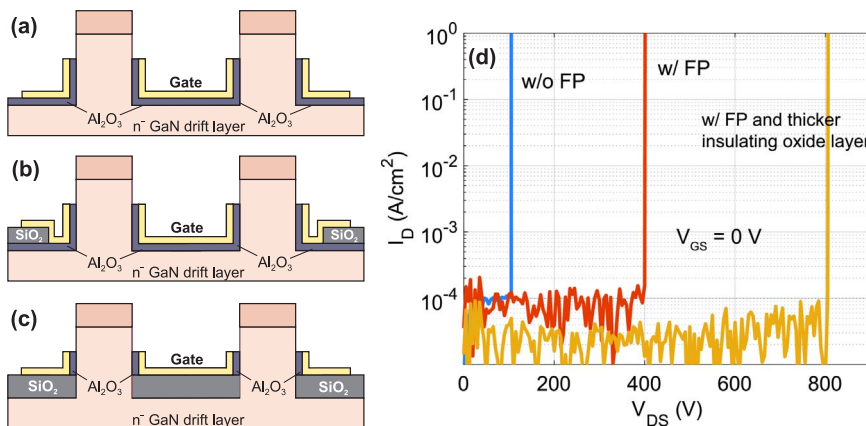

Fig. 10. Cross-section schematic of transistor without field plate (a), with a gate field plate at the device edge (b), with an oxide in the trench (c). (d) Breakdown measurements on three transistor designs [47].

3.2. Vertical GaN diodes

3.2.1. Vertical GaN-on-GaN diodes

The first demonstration of vertical GaN power diodes dates back to over 16 years ago [59]. There are two basic types of vertical power diodes, i.e. pn diodes and Schottky barrier diodes (SBDs). Vertical GaN pn diodes with a specific on-resistance (R_{ON}) of $2\ m\Omega\ cm^2$ for a breakdown voltage (BV) of 2.6 kV and $2.9\ m\Omega\ cm^2$ for a BV of 3.7 kV [26] have been demonstrated. A more recent paper reported a specific R_{ON} of $0.95\ m\Omega\ cm^2$ for a BV of 3.48 kV [60]. These performances showed near-theoretical power figure of merit. Avalanche breakdown capability with excellent device robustness were also been demonstrated in GaN vertical pn diodes [61].

Despite the high BV and low leakage of GaN pn diodes, their large turn-on voltage ($V_{ON} > 3\ V$), due to the large bandgap of GaN, can result in high conduction loss in a power switching circuit. Vertical GaN SBDs have a much lower V_{ON} ($< 1\ V$), but suffer from high OFF-state leakage current. State-of-the-art vertical GaN SBDs have been reported with a BV of 1.1 kV and R_{ON} of $2\ m\Omega\ cm^2$ [62].

Several advanced structures have been developed in Si and SiC devices to combine the good forward characteristics of SBDs (e.g. low turn-on voltage) and reverse characteristics of pn diodes (e.g. low leakage current and high BV). The key concept for these advanced diodes is to move the peak electric field from the top Schottky contact into the bulk semiconductor device at high reverse biases, while maintaining good Schottky-like forward characteristics. For example, the trench metal-insulator-semiconductor (MIS) barrier Schottky (TMBS) diode [Fig. 11(a)] consists of multiple trenches and utilizes the MIS structures at the trench bottoms and sidewalls to reduce the electric field at the top Schottky barrier contact. The junction barrier Schottky (JBS) diodes [Fig. 11(b)] benefit from the pn junctions in the lateral direction to reduce the electric field at the Schottky contact. The merged pn-Schottky (MPS) diodes [Fig. 11(c)] have similar structures with JBS diodes, but the top anode forms Ohmic contacts to p-type grids, which could sustain a large inductive surge current.

Vertical GaN TMBS diodes were demonstrated in 2016 by combining the TMBS structure and field rings [63]. These devices showed 10^4-fold lower leakage current and a significantly improved BV compared to conventional vertical GaN SBDs. Vertical JBS diodes were also demonstrated by selective p-type ion implantation and activation [34,64]. Due to the difficulties in p-type ion activation in GaN, the lateral pn junctions in vertical JBS diodes were also made by n-type ion implantation into epitaxial p-GaN layers [34]. Vertical GaN MPS diodes were demonstrated by making trenches through the epitaxially-grown p-GaN layers [Fig. 11(d)] [65,66], a BV close to 2 kV was reported [66]. Second turn-on in forward characteristics was demonstrated in these MPS diodes, indicating the capability to sustain large inductive currents. However, compared to MPS diode structure incorporating lateral pn junctions in semiconductor devices [Fig. 11(c)], these trench-MPS diodes could not take the advantage of the lateral depletion of pn junctions at high reverse biases.

In spite of the great progress of these advanced vertical diodes, the full potential of vertical GaN SBDs and advanced SBDs has not been exploited yet. The BV demonstrated in these devices, with no avalanche capability reported, is still much lower than the avalanche BV in vertical GaN pn diodes. The lack of avalanche capability greatly compromises the device robustness when operating in inductive switching environments. Although the nature of avalanche breakdown is still not fully understood in GaN devices, a key factor is believed to be good edge termination technologies and a way to remove holes from the structure, which is still lacking in vertical GaN unipolar diodes.

The development of advanced vertical GaN SBDs is also at an early stage. From the discussion on JBS and MPS diodes, it can be seen that a key issue is to make high-quality and defect-free patterned lateral pn junctions. In particular, p-type ion implantation and activation in GaN are far from mature. The activation ratio for acceptors is typically below 5%, resulting in very low concentration and mobility for the activated free holes. This makes it difficult to form Ohmic contact onto implanted p-GaN regions, greatly limiting the performance of MPS diodes with pn junctions incorporated into the drift region.

3.2.2. Vertical GaN-on-Si diodes

While most vertical devices utilize expensive GaN substrates, the commercialization of vertical GaN power devices has been hindered by the high cost of bulk GaN substrates. The mainstream GaN substrates are 2-in., while 4- and 6-in. GaN substrates are available very recently in small volumes. The wafer cost (per area) for 2-in. GaN-on-GaN is $60–$100/cm^2, still much higher than the cost for 4-in. SiC ($\sim$ \$ 8/cm^2) and 8-in. GaN-on-Si ($\sim$ \$1/cm^2) [57,8]. The demonstration of vertical GaN devices on Si substrates could allow for almost 100-fold lower wafer and epitaxial cost as well as access to 8-in. fabrication facilities [8].

There are, however, two main challenges for the demonstration of high performance vertical GaN-on-Si devices: (a) high dislocation (typically $\sim$ $10^9\ cm^{-2}$) in GaN layers grown on Si substrates, and (b) limited thickness for the GaN layer that can be grown on Si substrates and buffer layers, due to the lattice and thermal stress.

First vertical GaN-on-Si power diodes were demonstrated in 2014, by utilizing a quasi-vertical structure [67], where a mesa structure was created and the anode and cathode located on the same side of the wafer. With only 1–1.5-μm-thick drift region, these diodes exhibited a BV of 200–300 V with a R_{ON} of 6–10 $m\Omega\ cm^2$. Three advanced processes, including the plasma treatment, Tetramethylammonium hydroxide wet etching and field ring implantation, greatly reduced the parasitic leakage current along the etching sidewalls in the quasi-vertical devices [57]. By increasing the drift region thickness, lowering the carrier concentration in the drift region and optimizing the current spreading layer to reduce device R_{ON} [19], a BV over 500 V with a R_{ON} below 1 $m\Omega\ cm^2$ as well as the capability to operate up to 300 °C have been demonstrated in quasi-vertical GaN-on-Si pn diodes [19] (Fig. 12).

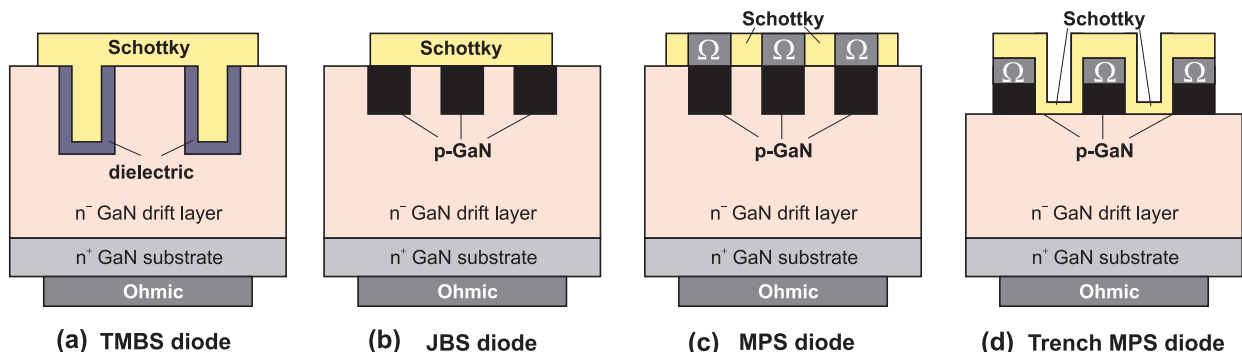**Fig. 11.** Schematics of (a) TMBS diodes, (b) JBS diodes, (c) MPS diodes and (d) trench-MPS diodes.
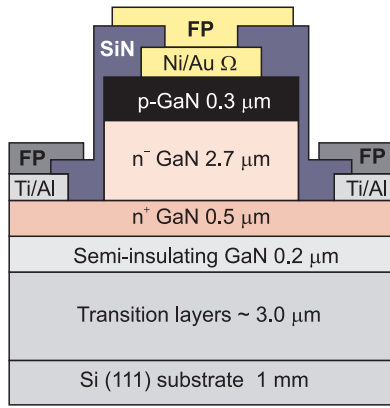
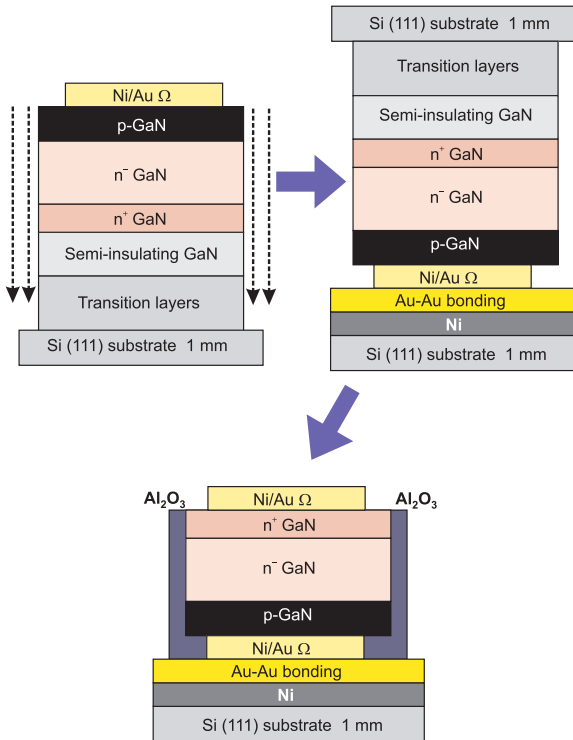**Fig. 12.** Device cross-section of a quasi-vertical GaN-on-Si pn diode.

Fig. 13. The main steps to fabricate fully-vertical GaN-on-Si pn diodes by layer transfer technologies.

Fig. 14. Design space of the off-state leakage current of vertical GaN diodes as a function of the total dislocation density level in the structure, and the average electric field in the drift layer (E_{AV} = 13 MV/cm).The different dislocation density represents vertical GaN diodes fabricated on different substrates. The leakage currents of state-of-the-art GaN lateral diodes with similar Eav and dislocation density are also shown [68].

Fully-vertical GaN-on-Si power diodes have also been recently developed. The fully-vertical structure, where the electrodes are located at different sides of the wafer, could allow for a more uniform current distribution and a smaller device area, but is difficult to implement in GaN-on-Si structures due to the highly resistive and defective buffer layers. This challenge has been addressed by two methods: (a) layer transfer technologies (Fig. 13) [19,69], where the original wafer was flipped over and bonded to another Si substrate, followed by the removal of the original Si substrate and buffer layers; (b) conductive buffer layers [70], where the whole buffer layers were highly doped (Si: over 10^{19} cm^{-3}) to make them conductive. The state-of-the-art fully-vertical GaN-on-Si power diodes shows a BV over 500 V with a R_{ON} below 1 mΩ cm^2 [19,71].

To understand the full potential of vertical GaN-on Si devices, it is important to study the origin and design space of the off-state leakage current [68]. This leakage is dominated by the variable-range hopping through threading dislocations and the device breakdown is typically given by trap-assisted space-charge limited current [68]. In
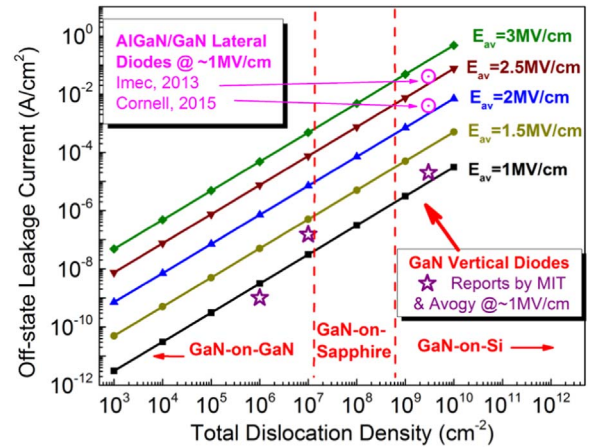
comparison, vertical GaN-on-GaN pn diodes have similar leakage mechanisms but show avalanche breakdown. In Ref. [68], the MIT group and Synopsys demonstrated a simulation model for the leakage current in vertical GaN power devices, with the simulation model well calibrated by the experimental data of vertical GaN power diodes on Si, sapphire and GaN substrates. From the simulation, they derived the design space of leakage current of vertical GaN power devices (Fig. 14). It can be seen that although the leakage current of GaN-on-Si vertical devices is $10^2 - 10^3$-fold higher than that in GaN-on-GaN device, it is much lower than that in lateral AlGaN/GaN diodes, for a similar reverse electric field level. In addition, it was recently reported that vertical GaN-on-Si pn diodes could survive repetitive avalanche tests with surge current and voltages, indicating similar breakdown ruggedness to the avalanche breakdown [72]. These results support the great potential of the cost-effective vertical GaN-on-Si devices for high-voltage applications.

4. Conclusion

In this review, we summarized several key aspects of vertical GaN power electronics including material growth, device architectures, device physics, and processing issues. High-performance vertical GaN transistors and diodes have been demonstrated on free-standing GaN substrate and low-cost silicon wafer. With the advances in substrate technology and the optimization of the field engineering, vertical GaN power devices with breakdown voltage beyond 5 kV can be realized. There are however, very limited reliability studies on vertical devices so far. A careful study of the origin of the breakdown mechanism in these devices is also needed. The maturity of the substrate technology together with the optimization of the device processing will soon enable the commercialization of vertical GaN power devices.

Acknowledgements

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