Magnetic Domain Wall Devices: from Physics to System Level Application

by

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Submitted to the Department of Electrical Engineering and Computer Science on November 30, 2018, in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering and Computer Science

Abstract

Spintronics promises intriguing device paradigms where electron spin is used as the information token instead of its charge counterpart. Spin transfer torque-magnetic random access memory (STT-MRAM) is considered one of the most mature nonvolatile memory technologies for next generation computers. Spin based devices show promises also for beyond-CMOS, in memory computing and neuromorphic accelerators. In the future cognitive era, nonvolatile memories hold the key to solve the bottleneck in the computational performance due to data shuttling between the processing and the memory units. The application of spintronic devices for these purposes requires versatile, scalable device design that is adaptable to emerging material physics. We design, model and experimentally demonstrate spin orbit torque induced magnetic domain wall devices as the building blocks (i.e. linear synaptic weight generator and the nonlinear activation function generator) for in-memory computing, in particular for artificial neural networks. Spin orbit torque driven magnetic tunnel junctions show great promise as energy efficient emerging nonvolatile logic and memory devices. In addition to its energy efficiency, we take advantage of the spin orbit torque induced domain wall motion in magnetic nanowires to demonstrate the linear change in resistances of the synaptic devices. Modifying the spin-orbit torque from a heavy metal or utilizing the size dependent magnetoresistance of tunnel junctions, we also demonstrate a nonlinear activation function for thresholding signals (analog or digitized) between layers for deep learning. The analog modulation of resistances in these devices requires characterizing the resolution of the resistance. Since domain wall in magnetic wires is the nonvolatile data token for these devices, we study the spatial resolution of discrete magnetic domain wall positions in nanowires. The studies on domain wall is further extended to identify energy-efficient and dynamically robust superior magnetic material for ultra-fast and efficient devices for neuromorphic accelerators.

Thesis Supervisor: Marc A. Baldo
Title: Professor of Electrical Engineering and Computer Science
Acknowledgments

I had an amazing journey pursuing PhD at MIT. This journey would not be possible without support from groups of people in my professional network, my family and friends.

I am fortunate to have a hands-on advisor like Marc. He is always there for any kind of support. Every discussion with him is an opportunity to learn about cutting-edge research or to develop professional perspective. It is easy to get distracted by all the exciting opportunities available at MIT. Thanks to Marc for teaching me the opportunity cost in research and how to prioritize my goals.

Caroline is not only my research advisor but also a counselor for difficult times. By training, I’m an Electrical Engineer and without Caroline’s guidance it would not been possible to explore the materials science part of my thesis. I always feel inspired after any scientific discussion with her.

Thanks to Luqiao for the guidance and suggestions in the past couple years. We spent a lot of time together in the lab running experiments and I feel lucky to work with him.

I like to extend my appreciation to Dr. Ching-tzu Chen from IBM T. J. Watson Research Center, who was an inspiring mentor during my internship. Apart from Marc, Caroline and Luqiao’s labs, I was privileged to use the facilities and equipment in many other PI’s lab at MIT. Thanks to all of them specially, Dr. Jagadeesh Moodera, Profs. Geoffrey Beach, Pablo Jarillo-Herrero and Tomás Palacios.

I will always cherish the discussions with Prof. Millie Dresselhaus about my interests, research and future carrier in her office. I’m really grateful that she managed time for meetings during her busy schedule although I was not her student. Profs. Jing Kong and Vivienne Sze are two very inspiring mentors for me. Although their research fields have very little overlap with mine, I had their advice and support in developing my career. It was my pleasure to work with Prof. Leslie Kolodziejski on few occasions while working with EECS Graduate Student Association (GSA) and Path of Professorship. I was fortunate enough to be a part of the student focus group.
to introduce “Professional Perspective for graduate students” and learn about her vision on future of graduate education.

As a graduate student, I feel privileged to be part of three groups during my PhD. I had chances to interact with colleagues from these groups, discuss research, and learn from them. I specially appreciate working with Jean Anne, Joe, Jiahao, Sumit, Sungmin, Jinshuo, Astera, Enno, Ho-Pin, Peng, Lara and Frank. Apart from pursuing research in spintronics, I have developed interests and skills in other fields, for example, nanopatterning using self-assembly and electrical and optical applications of 2D materials. Thanks to Li-chen, Kun-Hua and Sangho for numerous discussions on self-assembly techniques. I must thank Ahmad, Dr. Amirhasan Nourbakhsh, Yafang, Brian, Dr. Hugh Churchill, Tony, Xu, Dong-Gwang and Farnaz for their help in developing my understanding on 2D materials and helping me with exploratory experiments.

Thanks to colleagues and lab mates – Nick, Phil, Dan, Matthias, Paul, Mengfei, Markus, Cole, Michelle, Ting-An, Jan, Eduardo, Saman, Andy, Shuchi, Mehmet, Dong Hun, Nicolas, Taichi, Ethan, Jackson, Shuai, Takian, Bingqian, Hexin, Yabin, Taqiyyah, Justin, Hailong and Yanfei for many friendly discussions inside and outside labs. I would like to thank Vicky for her mentorship during my service as a member of the Process Technology Committee of Microsystems Technology Laboratories.

During my PhD, I heavily used the fabrication facilities in Nanostructures Laboratory (NSL) and Microsystems Technology Laboratories (MTL). Thanks to all the staffs who play pivotal roles in running these laboratories. Special thanks to Mark and Jim from NSL, Kurt, Gary, Dave, Dennis, Bob, Donal, Ryan, Paudely, Eric and Scott from MTL. This thesis would not been possible without the materials characterization facilities in MIT’s Materials Research laboratory (MRL) and Harvard’s Center for Nanoscale Systems (CNS). Special thanks to Libby and Scott from MRL and Jason from CNS.

I would like to thank everyone in the Research Communication Laboratory led by Carol Lynn, Karine and Megan from Museum of Science, Boston.

Life at MIT was not limited to classrooms and labs. I developed my leadership skill
while organizing Path of Professorship (PofP), serving as an officer (treasurer) of EECS GSA and coordinator for Orientation of Graduate Student Council (GSC). Thanks to Senior Associate Dean Blanche Staton, friends from PofP, GSA and GSC. Special thanks to Ehsan, Nafisa, Sumaiya, Sujoy, Tapoti and all Bangladeshi friends in Boston for making me feel at home.

I started my research during undergrad and had an invaluable experiences working with Profs. Feroz Alam Khan (Physics, BUET), Shah Alam (EEE, BUET), Anisul Haque (EEE, EWU) and Q.D.M. Khosru (EEE, BUET). The experience I gathered during that time helped me in the next steps of my career.

I like to thank my parents, in-laws, grandmother, aunts and uncles for their unconditional love and support. You are the inspirations for all the journeys.

Finally, I want to thank my husband, who is my best friend, partner in all adventures, listener of my all random research ideas, personal chef, cleanroom buddy and support system for my life!
Contents

1 Introduction .............................................................................................................................. 13
  1.1 Domain walls in magnetic wires ................................................................................... 13
  1.2 Technological applications .......................................................................................... 15
    1.2.1 Memory ................................................................................................................... 16
    1.2.2 Logic ....................................................................................................................... 18
    1.2.3 Logic-in-memory device .................................................................................... 22
  1.3 Organization of the thesis ........................................................................................... 25
2 Spatial resolution of magnetic domain wall motion .......................................................... 32
  2.1 Micromagnetic Simulation .......................................................................................... 33
  2.2 Analytical modeling of pinning sites .......................................................................... 40
  2.3 Experiments and Results ............................................................................................ 44
    2.3.1 Patterning of closely-packed nanowires ................................................................ 44
    2.3.2 DWs motion in nanowires ................................................................................... 51
3 Domain wall motion in ferrimagnetic materials ............................................................... 67
  3.1 Current-induced domain wall motion: Spin-orbit torque ........................................... 68
  3.2 Sample fabrication ....................................................................................................... 70
  3.3 Magnetization & angular momentum compensation point ......................................... 71
  3.4 DW motion in Co$_{1-x}$Tb$_x$.................................................................................... 75
  3.5 Modeling of current induced domain wall motion in ferrimagnet ............................... 83
  3.6 Domain wall chirality in ferrimagnetic materials ....................................................... 86
4 Magnetic Domain Wall Logic Devices ............................................................................. 93
  4.1 Current induced domain wall motion: Spin transfer torque ....................................... 98
  4.2 Magnetic tunnel junctions ........................................................................................... 99
  4.3 Proposal of logic device using magnetic tunnel junction and magnetic domain wall . 100
  4.4 Fabrication of prototype magnetic logic devices ...................................................... 105
  4.5 Characterization of prototype device .......................................................................... 110
    4.5.1 Characterization with magnetic fields .................................................................. 110
    4.5.2 Electrical characterization of individual gates ...................................................... 112
    4.5.3 Fan-out ................................................................................................................. 115
    4.5.4 Shift oscillators .................................................................................................... 117
4.6 Device-to-device variation ................................................................. 119
4.7 Switching Energy ........................................................................... 120

5 Synaptic and activation function generation with magnetic domains .......... 124

5.1 Domain wall motion in a magnetic wire with constant width and synaptic model for a single domain wall motion in a magnetic wire: ................................................................. 129
5.2 Model for activation/threshold function with single domain wall .............. 131
5.3 Activation function generation with a single domain wall ......................... 132
5.4 Development of perpendicular magnetic anisotropy tunnel junction .......... 135
5.5 Fabrication of PMA MTJs.................................................................... 144
5.6 Characterization of MTJs..................................................................... 148
5.6.1 Switching with magnetic field ............................................................ 148
5.6.2 Switching with electrical current ......................................................... 151
5.7 Synaptic Function generator with multiple domain walls and MTJs .......... 155
5.7.1 Model for synaptic function generation ............................................... 155
5.7.2 Fabrication and characterization of the synaptic device ....................... 156
5.8 Activation function generation............................................................... 160
5.8.1 Activation function generation with multiple domains and MTJs: .......... 160
5.8.2 Fabrication and characterization of thresholding devices ..................... 161
5.9 Discussions......................................................................................... 165

6 Summary and Outlook............................................................................... 170
6.1 Summary ............................................................................................ 170
6.2 Outlook............................................................................................... 172
Table of Figures

Figure 1.1 (a) Vortex and (b) transverse domain walls in in-plane magnetic anisotropy material [2].................................................................................................................................................. 14

Figure 1.2 (a) Schematics of a 90° domain wall. Micromagnetic simulation of a (b) 180° [11] and (c) 360° [11] domain walls in nanowires.................................................................................. 15

Figure 1.3 (A) A vertical racetrack memory. The U-shaped nanowire is normal to the plane of the substrate. The two U-shaped nanowires show the magnetic patterns in the racetrack before and after the DWs have moved. (B) A horizontal racetrack memory. (C) Read and (D) Write operations. (E) Arrays of vertical U-shaped racetracks built on a chip [12]......................... 17

Figure 1.4 Proposed cell structure for solid state memory. The cell has two transistors and one magnetic tunnel junction (MTJ) (2T1MTJ). The area of the cell is 12F², where F is the technology node. [13]..................................................................................................................................... 18

Figure 1.5 (a) Schematic of an all-metallic ferromagnetic NOT gate. (b to e) Operations of NOT-gate magnetization reversal by successive magnetization directions (arrows) and domain wall (thick line) positions within a NOT gate. (f) Magnetic ring, including one NOT junction. The bright white shade corresponds to the magnetic material. (g) Focused ion beam image of a NOT gate [16]................................................................................................................................................ 19

Figure 1.6 A magnetic nanowire network containing one NOT gate, one AND gate, two fan-out junctions, and one cross-over junction (Focused ion beam image) [17]. ................................. 20

Figure 1.7 Schematic of the proposed logic device at (a) ON and (b) OFF states [18]............ 21

Figure 1.8 mCell cross section [19]. .......................................................................................... 21

Figure 1.9 Estimated device parameters and system-level metrics of analog synaptic devices from the NeuroSim Platform for online training of a million MNIST images with a two-layer fully connected neural network (image is generated from the data in [21]).................................. 23

Figure 2.1(a) Scanning electron microscope image of a 30-nm-wide wire (nanowire 1), (b) initial position of the DW in discretized nanowire 1, (c) traveling distances of DWs in five different discretized nanowires after applying magnetic field along their length. Insets show the DW at pinning sites A, C and D in nanowire 1. The DW was not pinned at B [14]........................................ 33

Figure 2.2 Power spectral density of the line edge roughness of the discretized wire, the average of 104 synthesized self-affine wires, and the average of 104 synthesized random-edge wires. The correlation length, ξ, is extracted from the discretized wire and is applied to synthesize the self-affine wires [22]. ........................................................................................................... 36

Figure 2.3 A single domain wall as shown in micromagnetic models of (a) an IMA wire (mx) and (b) a PMA wire (mz) [22]. ........................................................................................................... 37
Figure 2.4 (a) Final positions into which domain walls relax from their initial positions of domain wall nucleation, for one wire in micromagnetic simulations. The bin width is chosen to be the size of one simulation cell, 3 nm. Inset: Zoom of initial positions. (b) Line width roughness profile of the wire shows that the traps often correspond to local minima in width [22].

Figure 2.5 (a) Schematics of major DW traps in a nanowire defined by the correlation length \( \xi \). (b) Distribution of spacing \( \Delta x \) between domain wall discrete positions for IMA wires, including wires with self-affine edge profiles with correlation length \( \xi \) and wires with random-edge profiles. The distributions are normalized by area.

Figure 2.6 Distribution of spacing \( \Delta x \) between domain wall discrete positions for PMA wires, including wires with self-affine edge profiles with correlation length \( \xi \) and wires with random-edge profiles. The distributions are normalized by area [22].

Figure 2.7 Distributions of distances traveled by domain walls in simulated nanowires. The sample size is 1500 wires. The fractal analytical model is the overlaid line with parameters listed for each applied field [22].

Figure 2.8 (a-f) Schematic illustration of the step-by-step fabrication process. (g) Cross-sectional SEM image after step 4 showing the bilayer resist on top of the CoFeB thin film. Top down SEM images (h) after ion beam etching to transfer the feature into the metal (step 5) and (i) resulting 50 nm wide CoFeB wire (step 6).

Figure 2.9 Cross-sectional SEM images of bilayer resist stack after 1 min O\(_2\) RIE (step 4), for HSQ widths (a) 468 nm, (b) 261 nm, (c) 95 nm, and (d) 61 nm. This RIE time was not long enough for the wider two HSQ masks and did not produce an undercut. (e) SEM image of metal wire showing only partial mask removal due to nonoptimized RIE time [34].

Figure 2.10 Scanning electron microscope images of 20, 30 and 50 nm wires with 2w, 3w and 4w pitches, where w is the width of the wires [35].

Figure 2.11 Average LER vs wire width. The standard deviation is measured across five separate wires on the same substrate. Wires are patterned with electron beam acceleration voltage of (a) 125 keV and (b) 30 keV [34].

Figure 2.12 (a) The magnetization distribution inside a 60 nm wide nanowire and the in-plane stray field distribution outside the wire. Navy solid lines show the two edges of the wire and blue dotted lines show edges of neighboring nanowires. The red and the blue background outside the wire shows the stray field strength. (b) Stray field distribution from a DW in a smooth-edged nanowire of width 60 nm and 80 nm as a function of distance from the wire. Red and blue markers show the stray field along the red and blue arrows in (a), respectively, perpendicular to the core of the DW.

Figure 2.13 (a) SEM image of Co wires of 80 in the shape of concentric wires. (b) MFM images of initial positions of tail-to-tail and head-to-head domain walls. Insets show the Neel domain walls configuration in IMA Co wires. (c) Zoomed-in MFM image of the 15 individual tail-to-tail domain walls in 15 Co nanowires. The white dotted lines show the edges of the wires.
Figure 2.14 (a) SEM images of L-shaped wires. (b) Initial positions of the tail-to-tail domain walls in the cured regions of the L-shaped wires. .......................... 53

Figure 2.15 (a) Magnetic force microscopy images of domain walls in concentric rings with applied magnetic fields of 20 kA/m, 24 kA/m, 28 kA/m, and 32 kA/m along the y-axis. The black and the white arrows indicate the positions of two separate domain walls in two different nanowires at different magnetic fields. (b) Fractal analytical model and (c) exponential analytical model overlaid on distributions of distances traveled by domain walls in experiment. The sample size is 94, 94, 83, and 134 wires in increasing order of applied fields [22]. ................................. 55

Figure 2.16 Magnetic force micrographs of L-shaped nanowires. The black and the white arrows indicate the positions of two separate domain walls in two different nanowires at different magnetic fields [22]. ..................................................................................................................... 56

Figure 2.17 (a) weakly interacting and (b) strongly interacting Co concentric rings after applying a magnetic field of 20 kA m⁻¹ and 32 kA m⁻¹ along the y direction. Black and white (blue and yellow) arrows indicate the positions of two separate domain walls in two weakly (strongly) interacting nanowires at different magnetic fields. .................................................................................. 59

Figure 2.18 Experimental measurement of the stochastic nature of domain wall motion. Histograms of the traveling distance of DWs in (a) weakly interacting wires and (b) strongly interacting wires at different fields. The blue dashed lines in (a) show the distributions of DW displacement according to the proposed model. The pink dotted line in the bottom left panel shows the distribution with b = 0 in the proposed model [14]. ........................................... 60

Figure 3.1 Schematic of spin Hall effect in non-magnetic materials [6]......................... 68

Figure 3.2 Schematic of the patterned wire (blue rectangle), connecting regions (green) and the contact pads (purple squares)................................................ 70

Figure 3.3 Hysteresis loop measured for Co₁₋ₓTbx thin film series. ................................. 72

Figure 3.4 Saturation magnetizations and coercive fields for Co₁₋ₓTbx thin film series. ....... 72

Figure 3.5 Schematics of the anomalous Hall measurement set-up. .................................................. 73

Figure 3.6 Anomalous Hall resistance of 4-μm wide Pt/Co₁₋ₓTbx Hall bars. ..................... 74

Figure 3.7 (a) Electrical set-up for the domain wall motion measurement. The yellow and the green regions represent ↓ and ↑ domains in the MOKE microscope image of 4-μm wide Co₀.₆₉Tb₀.₃₁ wire. (b) Domain wall motion in Co₀.₆₉Tb₀.₃₁ wire with consecutive current pulses. Blue and red dotted lines show the initial positions of ↓↑ and ↑↓ domain walls in the top MOKE image, respectively. ....................................................................................................................................................... 75

Figure 3.8 Estimated Kerr rotation of Co₁₋ₓTbx thin films (Kerr rotation is calculated from Eq. 5 in [14])................................................................. 76
Figure 3.9 Wire width dependence of domain wall velocity of Pt/Co$_{1-x}$Tbx. Domain wall velocity as a function of current density for Pt/Co$_{0.79}$Tb$_{0.21}$ wires. ........................................ 77

Figure 3.10 Domain wall velocity as a function of current density for (from bottom to top panel) Pt/Co$_{0.74}$Tb$_{0.26}$, Pt/Co$_{0.67}$Tb$_{0.33}$ and Pt/Co$_{0.59}$Tb$_{0.41}$. ........................................................................................................ 78

Figure 3.11 Domain wall velocity as a function of current density for Pt/Co$_{1-x}$Tbx at x = 0.17, 0.21, 0.26, 0.31, 0.33, 0.38 and 0.41 (from bottom to top panel). The error bars reflect standard deviations from multiple measurements. .................................................. 79

Figure 3.12 Domain wall mobility extracted from the dotted lines in Figure 3.10 for Pt/Co$_{1-x}$Tbx. ................................................................................................................................. 80

Figure 3.13 Temperature dependent magnetic properties of Pt/Co$_{0.79}$Tb$_{0.21}$. (a) Out-of-plane hysteresis loops of Pt/Co$_{0.79}$Tb$_{0.21}$ films measured at different temperatures. (b) Summary of coercive fields and the remanence magnetization in Pt/Co$_{0.79}$Tb$_{0.21}$ film with temperature. ............. 82

Figure 3.14 Threshold and maximum applicable current densities of Pt/Co$_{1-x}$Tbx with different compositions. ........................................................................................................... 82

Figure 3.15 Calculated current-induced domain wall velocity for a series of ferrimagnetic samples with different net angular momentum, S$_{eff}$. ................................................................. 85

Figure 3.16 Domain wall velocity as a function of current density at different longitudinal fields along the length of the Pt/Co$_{0.79}$Tb$_{0.21}$ sample for (a) $\uparrow\uparrow$ and (b) $\uparrow\downarrow$ domain walls. ......................... 86

Figure 3.17 Schematic illustration of the domain wall texture for $\uparrow\uparrow$ and $\uparrow\downarrow$ Néel domain walls in magnetically Co-dominant samples. ......................................................... 87

Figure 3.18 Domain wall velocity as a function of in-plane field for samples of (a) Pt/Co$_{0.79}$Tb$_{0.21}$, (b) Pt/Co$_{0.67}$Tb$_{0.33}$ and, (c) Pt/Co$_{0.59}$Tb$_{0.41}$ wires, respectively. Red squares (negative current) & red circles (positive current) represent $\uparrow\uparrow$ domain walls and blue triangles (negative current) & blue stars (positive current) represent $\uparrow\downarrow$ domain walls, respectively. Red solid lines and blue dashed lines are the linear fit of the experimental data for $\uparrow\uparrow$ and $\uparrow\downarrow$ domain walls. ......................... 88

Figure 3.19 Schematic illustration of the domain wall texture for $\uparrow\uparrow$ and $\uparrow\downarrow$ Néel domain walls in magnetically Tb-dominant samples. ........................................................................... 89

Figure 3.20 Effective Dzyaloshinskii-Moriya interaction fields in different Pt/Co$_{1-x}$Tbx samples. ............................................................................................................................. 90

Figure 4.1 Schematics of a field-effect transistor at (a) OFF and (b) ON states. ......................... 93

Figure 4.2 Single spin flip is NOT allowed in a ferromagnetic material................................. 94

Figure 4.3 Micromagnetic simulation of a magnetic domain wall in a ferromagnetic wire. If the energy landscape of the wire is set up with two energy minimums (1) and (2), then the magnetic moments can collectively switch over the energy barrier $\Delta E$ [2]. ......................................................... 95
Figure 4.4 Current induced domain wall motion. Conduction electrons are labeled by the red arrow, local magnetic moments by the black arrows. The domain wall region is shown in yellow [2]...

Figure 4.5 Two configurations of magnetic tunnel junctions. (a) Parallel or low resistance state and (b) Antiparallel or high resistance state [2]............................................................................................................ 99

Figure 4.6 (a) ON and (b) OFF states of the proposed magnetic logic devices [6].............. 101

Figure 4.7 Initial configuration of (a) NAND, (b) NOR and, (c) AND gates [2].................... 103

Figure 4.8 (a) IMA and (b) PMA logic devices. (c) Power-delay product versus delay, shown for IMA materials (blue), PMA materials (red), and 40 nm CMOS (green). Dotted lines are constant EDP. The desired corner is the bottom left. (d) Gate scaling behavior, showing the power-delay product scales vs. wire width, for IMA at 0.1 V (blue) and PMA at both 0.01 V and 0.004 V (red) [5].......................................................................................................................... 104

Figure 4.9(a) Thin film stack. Numbers are in units of nm. (i) Free layer. (ii) Synthetic antiferromagnet fixed layer. (b) In-plane hysteresis loop of the stack. (c) Zoom in view of the hysteresis loop [2]....................................................................................................................... 105

Figure 4.10 Prototype device fabrication steps [2].................................................................... 106

Figure 4.11 (a) Top-down SEM after step (ii) in Figure 4.10. (b) End-point detector signal for different elements in the film stack [2]........................................................................................................................................ 107

Figure 4.12 (a) SEM image of a device after Step 8, with PMMA removed. (b) Augers signal showing Ru on the MTJs (blue curve) [2]................................................................................................................. 108

Figure 4.13 Prototype IMA device [6]........................................................................................ 110

Figure 4.14 (a) Resistance of a MTJ vs. magnetic field. The spin orientations of the domains at different resistance states are shown in the insets. (b) Resistance of MTJs with areas. ............ 111

Figure 4.15 Inverter operation. (a), Transient showing the MTJ resistance and applied voltage pulses between IN and CLK versus time. At 3.80 V, the device switches from low resistance ('1') to high resistance ('0'). (b), Transfer characteristic of I_{OUT} through the MTJ versus I_{IN} across the wire. The SEM images show the configuration below $I_{TH}$, with the DW position approximated by the red dot and $I_{IN}$ electron flow direction shown by the yellow arrow, and the approximate DW position after $I_{TH}$. Inset shows simple circuit diagram to represent the device, including the wire resistance and the variable tunnel junction resistance [6]................................................................................................. 112

Figure 4.16 Buffer operation. (a) Transient behaviour showing a buffer operation, plotting $R_{MTJ}$ and $V_{IN}$ versus measurement step as we increase the 1-μs voltage pulse amplitude in 0.01 V steps. This device has similar $R_W$ to the previous device, but slightly higher $R_{MTJ}$ and TMR. At 3.97 V, the device switches from a high-resistance output to a low-resistance output. (b), Transfer characteristic for the buffer. inset, Comparison of this transfer characteristic (right black curve) to that of another device (left blue curve) with less well matched $R_W$ and $R_{MTJ}$............................... 114

7
Figure 4.17(a) SEM image of a circuit where, one device output is connected to the inputs of two devices. Voltage pulses are applied to CLK₁ with CLK₂ and CLK₃ grounded. Scale bar, 100 μm. Inset shoes the schematics of the initial configurations of the three devices, with the DWs initialized on the left. Red signifies magnetized right and grey signifies magnetized left. (b) Plot of MTJ resistance versus pulsed voltage applied at CLK₁, showing one device can power a switch in two subsequent devices. The error bars represent the average noise fluctuation in R_MTJ monitored for each device at each voltage step [6].

Figure 4.18 (a) Shift oscillator with three devices connected in series, with the output of device 3 feeding back into the input of device 1. The devices are initialized with their domain walls (DWs) on the left and the tunnel junctions parallel. In the experiment, at Step 1 we apply a voltage pulse at CLK₁ to read the state of device 1 while writing the state of device 2. The voltage pulse is applied between CLKₙ and CLKₙ₊₁. Yellow arrows represent electron flow direction. In this case the DW in device 2 switches. (b) Cartoon of Step 2, where we now apply a voltage pulse at CLK₂ to read the state of device 2 while writing the state of device 3. In this case the DW in device 3 does not switch. In Step 3 and Step 4 this is repeated at CLK₃ and CLK₁, respectively. (c) SEM of three devices in series. Rₚ₁=23.8 Ω, Rₚ₂=19.0 Ω, and Rₚ₃=18.4 Ω. Scale bar, 50 μm. (d) MTJ resistance at each step in the three inverters circuit, showing the oscillation of the DW position at each step between the parallel (low MTJ resistance, bit 1) and antiparallel (high MTJ resistance, bit 0) device states [6].

Figure 4.19 Threshold voltage versus bias field for three different devices, where the error bars represent the depinning voltage standard deviation repeated at least 3 ×, with the DW reinitialized between each. Grey=device 1, red=device 2 and blue=device 3. The lines are a linear fit. Devices 2 and 3 were fabricated together, while device 1 was fabricated at a later time on a different wafer piece [6].

Figure 5.1 Neuromorphic computation scheme for deep learning in a single layer.

Figure 5.2(a) Domain wall based magnetic tunnel junction for synaptic weights [23]. (b) Domain wall position and the MTJ resistance as a function of input current between V⁺ and V⁻.

Figure 5.3 Domain wall velocity in perpendicular magnetic anisotropy CoFeB as a function of current density.

Figure 5.4 Current-induced linear domain wall motion in wires with constant width. (a) Electrical set-up for the domain wall motion measurement. The brown and the green regions represent down (↓) and up (↑) domains in the MOKE microscope image of 4 μm wide CoTb wire. (b) Domain wall motion in CoTb wire with consecutive current pulses. Blue and red symbols show the initial positions of ↓↑ and ↑↓ domain walls in (a), respectively. The error bars reflect standard deviations from multiple measurements.

Figure 5.5 Domain wall position in a perpendicular magnetic anisotropy wire as shown in the schematic (inset) with 4 ns current pulse. The analytical model is obtained from a shifted sigmoid function.

Figure 5.6 (a) Schematic of an activation function generator with a single domain wall in a CoTb wire. The bottom Pt layer is patterned so that its width varies along the length of the wire.
to the analytical model obtained from a shifted sigmoid function [24]. The width of the CoTb wire is constant. (b) Magnetic domain wall travelling distances in a CoTb wire as shown in the inset with 300 ns current pulses. Inset shows the magnetoptic Kerr microscopy image of a CoTb wire with two domain walls. The black dotted line marked by A in the inset shows the initial position of the domain wall for all currents.

Figure 5.7 CoFeB based magnetic tunnel junction

Figure 5.8 Steps for optimizing MTJs for neuromorphic devices

Figure 5.9 Hysteresis loops of as deposited and annealed free layers

Figure 5.10 Interface anisotropy energy of as deposited and annealed CoFeB free layer of MTJs

Figure 5.11 Hysteresis loops of as deposited and annealed Ta/CoFeB(0.4 nm)/MgO/CoFeB(tCoFeBtop)/Ta/Ru stack with 0.7 nm < tCoFeBtop < 1.7 nm

Figure 5.12 Saturation magnetization and the coercive fields of Co/Pt multilayers as a function of (a) Co thickness and (b) Pt thickness

Figure 5.13 Out-of-plane hysteresis loop of (a) as deposited and (b) annealed reference layers in Figure 5.8(d) with different thickness of CoFeB (tCoFeBtop)

Figure 5.14 Antiferromagnetic coupled exchange field and estimated exchange coupling energy density (Jex) vs. Ru thickness (tRu) in as-deposited SAF structures [28]

Figure 5.15 (a) As deposited and (b) annealed Co/Pt synthetic antiferromagnets with different Ru thickness

Figure 5.16 (a) Final structure of the MTJ for synaptic and activation devices. (b) Hysteresis loop of the thin films in (a) after annealing at 250 °C. The magnetic configuration of the different magnetic layers are shown as the field is swept

Figure 5.17 (a) Zoomed in TEM image of the CoFeB/MgO/CoFeB layers. (b) TEM image of the full MTJ film stack after annealed at 250 °C on hot plate in inert environment

Figure 5.18 Fabrication steps for PMA MTJs for synaptic and activation function generator. Step (xiii) shows the schematic of a complete device

Figure 5.19 Scanning electron microscope images of a 1 μm × 3 μm magnetic tunnel junction without (a) and with (b) electrical contacts (false colored), including the electrical schematic for measuring the magnetoresistance of the fabricated tunnel junctions. (c) Schematic side view of the MTJ with the measurement set-up. (d) Magnetoresistance of the device in (a). Magnetic fields are applied out of the plane of the junctions

Figure 5.20 RA product and TMR of MTJs of different areas. RA product is 1200(±200) kΩ-μm² with junction area
Figure 5.21 (a) Magnetic switching of regions the CoFeB wire with and without tunnel junctions. The switching of the CoFeB wires under the tunnel junction is completely dominated by the stray field from the tunnel junction. (b) Schematic of the fabricated tunnel junction after applying a small magnetic field along –z direction. The region of the wire under the tunnel junction with initial parallel state of spins, remain parallel. The rest of the wire behave as a magnetically free ferromagnetic layer and switches with small magnetic field. Therefore, two domain walls are nucleated at the two sides of the tunnel junctions.

Figure 5.22 Field induced magnetic switching of the CoFeB wire under 200 nm × 400 nm magnetic tunnel junction.

Figure 5.23 Schematic of the magneto-electrical set-up for measuring the magnetoresistance of the magnetic tunnel junctions with magnetic domain walls. A small bias field lower than the switching field of the free layer is applied out-of-plane of the junction to reduce the pinning of the domain walls.

Figure 5.24 Magnetoresistance of a 200 nm × 400 nm magnetic tunnel junction with different bias fields and 20 ns current pulses. The inset of the top panel in (a) shows the SEM image of the MTJ.

Figure 5.25 (a) Maximum and minimum current required to switch MTJs by using domain wall motion. (b) Switching current density calculated from the current in (a) and the cross-sectional area of wires with constant width.

Figure 5.26 (a) Schematic of a series of tunnel junctions device for discretized synaptic weight generation. The boundaries between the blue (up domain) and the red (down domain) regions in the free layer show the magnetic domain walls at the edges of the tunnel junctions. (b) & (c) Scanning electron microscope images of nine 200 nm × 400 nm magnetic tunnel junctions without (b) and with (c) electrical contacts. The tunnel junctions are connected in parallel to each other.

Figure 5.27 Resistance of nine parallel MTJs shown in Figure 5.26c. (b) Switching of MTJs from parallel to antiparallel states with out-of-plane magnetic field.

Figure 5.28 Switching of the parallelly connected magnetic tunnel junctions in (e) with a bias field of -480 Oe. The eight steps correspond to the switching of seven MTJs with 8 ns current pulses. The linear fits of the magnetoresistance confirm the linear weight generation using MTJs.

Figure 5.29 (a) Scanning electron microscope images of seven 400 nm × 1200 nm magnetic tunnel junctions after the process step of reference layer milling. The tunnel junctions are connected in parallel to each other after the final process step. (b) The switching of the parallelly connected magnetic tunnel junctions in (a) with a bias field of -85 Oe.

Figure 5.30 The change in magnetoresistance of the designed MTJ device with nine MTJs connected in parallel. The large MTJs in the center of the wire, corresponding to the steepest portion of the activation characteristic.
Figure 5.31 (a) Schematic of a series of tunnel junctions device for discretized synaptic weight generation. The boundaries between the blue (up domain) and the red (down domain) regions in the free layer show the magnetic domain walls at the edges of the tunnel junctions. (b) Scanning electron microscope images of nine magnetic tunnel junctions. The width of the free layer is varying linearly along its length. ................................................................. 161

Figure 5.32 Tunnel magnetoresistance of nine parallel MTJs shown in Figure 5.31b. .............. 163

Figure 5.33 Switching of the parallelly connected magnetic tunnel junctions in Figure 5.31b with a bias field of 200 Oe. The magnetoresistances are averaged from 75 measurements with 8 ns current pulses and the error bars show the standard deviation of magnetoresistance. .............. 164

Figure 5.34 Switching of the parallelly connected magnetic tunnel junctions in Figure 5.31(b) with a bias field of -400 Oe. The magnetoresistances are averaged from 40 measurements with 8 ns current pulses and the error bars show the standard deviation of magnetoresistance. Magnetoresistances are normalized with respect to the resistances of the MTJs in regions of parallel to antiparallel switching ................................................................. 164

Figure 6.1 (a) Circuit symbols and models for the synaptic MTJ and thresholding MTJ. (b) Crosspoint array using synaptic MTJs and thresholding MTJs as analog logic and memory elements [6] ................................................................. 173

Figure 6.2 Integrated neural accelerators with magnetic domain wall based synaptic and activation function generators ........................................................................................................... 173
1 Introduction

A magnetic domain wall is a boundary between two oppositely oriented domains, where all spins are aligned along the same direction. In magnetic thin films, domain walls exist to reduce the magnetostatic energy, $H_d M$, where $H_d$ is demagnetization field and $M$ is the magnetization. Domain walls may span a few lattice constant of the material depending on the anisotropy energy and the exchange interaction between the spins. In this thesis, we characterize magnetic domain walls in micro and nanowires fabricated from magnetic thin films and demonstrate their implementations for logic and logic-in-memory applications.

1.1 Domain walls in magnetic wires

Domain walls inside magnetic wires can be of many different types. Depending on the spin orientation inside a domain wall, it can be of vortex or transverse type. Figure 1.1 shows the micromagnetic simulation of a vortex and a transverse domain wall inside in-plane magnetic anisotropy wires. The phase boundary between these two types of domain walls is approximated by $w \times t \sim 60L_{ex}^2$, where $w$ and $t$ are the width and the thickness of the wire and $L_{ex}$ is the ferromagnetic exchange length. $L_{ex} \sim 3-5$ nm in Fe or Co [1]. Thinner and narrower wires favor transverse domain walls.
Domain walls in nanowires with in-plane magnetic anisotropy (IMA) (magnetization oriented in the plane of the wire) experience pinning and depinning while moving under an applied magnetic field or electrical current and demonstrate complex dynamic behavior. Thus, the domain wall motion in IMA nanowire demonstrate stochastic behavior. The chirality (sense of rotation of spins) of domain walls plays important role in the stochastic nature of their motion [3-6].

Transverse domain walls in magnetic nanowires with IMA and perpendicular magnetic anisotropy (PMA) magnetization can be further categorized into Bloch and Néel type. If spins inside the domain wall rotate in the plane of the wall, it is a Bloch domain wall. In contrast, if spins rotate in the plane perpendicular to the plane of the wall, the domain wall is of Néel type. In PMA materials, the domain wall type depends on the out-of-plane magnetic anisotropy strength, exchange constant and the wire dimensions. In PMA thin films, heavy metal materials (i.e. Pt, Ta, and W) are often used as an under layer or top layer to stabilize Néel domain walls [7-10].
However, domain walls can also be of different types depending on the spin orientations of the separated domains:

(i) 90 degree  
(ii) 180 degree  
(iii) 360 degree  
(iv) 720 degree etc.

Figure 1.2 shows different types of domain walls based on the domain structures. Depending on the crystalline anisotropy of the materials, other types of domain walls are also possible i.e. Ni has 72 degree, 109 degree domain walls from crystalline anisotropy giving <111> easy axes.

![Figure 1.2](image)

*Figure 1.2 (a) Schematics of a 90° domain wall. Micromagnetic simulation of a (b) 180° [11] and (c) 360° [11] domain walls in nanowires.*

In this thesis, we are interested in the transverse 180° domain walls in IMA and PMA wires.

1.2 Technological applications

The domain walls can be manipulated by magnetic fields or electrical current. From technological perspective, domain walls inside magnetic nanowires are most important due to the confinement of electrical current inside the wires. In this thesis, we are interested in nanodevices for memory, logic and logic-in-memory applications.
1.2.1 Memory

Magnetic domain wall inside a nanowire can be an information token for storing data in computer memories. In 2008, Parkin et al. proposed [12] racetrack memories with a vision of single type of solid state memory device instead of a separate hard disk drive (HDD) devices and random access memories (RAMs). Racetrack memory promises to combine the low cost of the HDD, the high performance of RAM and reliability of solid-state memory. A series of domain domains separated by the $180^\circ$ domain walls are proposed to encode the ‘0’ s and the ‘1’ s. This proposal initiate studies on the static and the dynamic properties of magnetic domain walls in nanowires [7-10].
Reading data from the stored pattern is done by measuring the tunnel magnetoresistance of a magnetic tunnel junction (MTJ) element consisting of the free layer, tunnel barrier and the reference layer, connected to the racetrack (Figure 1.3C). The detail of the MTJ is discussed in Chapter 4. Writing data is accomplished by the fringing fields of a domain wall moved in a second ferromagnetic nanowire oriented at right angles to the storage nanowire (Figure 1.2D).

In 2009, Fukami et al. experimentally demonstrated another type of solid state memory device based on magnetic domain walls [13] where a single cell consists of a three terminal MTJ and two transistors (T). Figure 1.4 shows the proposed cell structure. The MTJ, reads the spin orientation of the magnetic domain under the tunnel barrier electrically. Pinning layer with opposite spins on the two bottom terminals would confirm a single magnetic domain wall in the free layer. Based on the position of the domain wall the magnetic tunnel junction resistance can be high (low) representing ‘0’ (‘1’).
The current through the free layer would move the domain wall between the two edges of the tunnel barrier (write operation) based on the signal in the WL.

1.2.2 Logic

The motivation for using magnetic non-volatile devices for logic application was to utilize the collective phenomenon of the electron spins, which can lower the operating voltage for the logic devices and consequently the power of the logic circuitry. A large number of spintronic devices have been explored as beyond-CMOS initiative in the past decades [14, 15]. Here, we discuss only the domain wall based spintronic logic devices.
In 2002, magnetic domain wall devices was proposed for logic applications [16]. Allwood et al. demonstrated that a domain wall in a magnetic wire with a turn could be modulated with the rotating magnetic field to mimic the logical NOT operation. Two stable magnetization directions within magnetic wires represent the two Boolean logic states, ‘1’ and ‘0’. Figure 1.5 shows the schematic and focus ion beam (FIB) image of the NOT gate and its operations with rotating magnetic field.

Four logic architecture elements (i.e. NOT, AND, fan-out and crossing) have been proposed using this approach [17]. Figure 1.6 shows a magnetic domain wall logic circuit with these four elements.
Figure 1.6 A magnetic nanowire network containing one NOT gate, one AND gate, two fan-out junctions, and one cross-over junction (Focused ion beam image) [17].

Later, after the proposal of Fukami et al. [13], Currivan et al. [18] and Bromberg et al. [19] proposed similar device structures with IMA and PMA materials, respectively, for logic applications. These devices are more suitable for solid-state applications compared to devices proposed by Allwood et al. as they are designed to operate with electrical current instead of the magnetic field. We discuss the advantages, challenges and promises of such devices for logic operations in Chapter 4. Figure 1.7 shows the schematics of the proposed logic device based on IMA materials. These logic devices are identified as spin transfer torque (STT) – domain wall devices [14, 15].
The read path is through the ‘Output’ and the ‘Clock’ terminals and the write path is through the ‘Input’s and the ‘Clock’ terminals. In contrast, the proposed device by Bromberg et al. has separate read and write terminals [19]. Figure 1.8 shows the proposed mCell logic devices based on PMA materials. The read and write paths are through RR’ and WW’ terminals.

Later both of these domain wall logic devices are demonstrated experimentally [2, 20]. We discuss the details of the experimental demonstration of IMA STT-domain wall devices in Chapter 4.
1.2.3 Logic-in-memory device

Recently, there have been great interests of utilizing novel non-volatile devices for non-von Neumann architecture [21]. This approach is motivated by the data-oriented computations *i.e.* pattern recognition [22-24]. In von Neumann architecture, the memory unit and the processing unit are separated from each other. Pulling data from memory takes most of the computation energy, as there remains a huge performance gap between the memory and the computation units (memory wall) [25]. Modern technologies are tackling these roadblocks from many angles, from the component level to the systems architecture design. Solutions include extensive use of parallelism, *i.e.* graphics processing unit (GPU), which enhances parallelism by using many cores. Besides, application-specific processors known as accelerators are designed to match the computing algorithms and data flow [26]. Tensor processing unit has been recently developed for accelerating the multiply-accumulate operation, which constitutes the major workload in the inference phase of neural networks in data centers [27]. Also, solutions for high data-transfer rate and high memory density *i.e.* hybrid memory cube [28], and high bandwidth memory [29] are also considered.

New and emerging non-volatile memories (NVMs) have also been introduced into the traditional memory hierarchy to reduce the physical distance between computing and the data [30]. Besides, recently, non-von Neumann architecture *i.e.* artificial neural network inspired by human brains shows significant promises for energy-efficient and low-latency computation using analog signals. NVMs are prime candidates for designing such neuromorphic accelerators [21]. NVMs are usually implemented as the synaptic devices, the purpose of which is to generate programmable resistances varying linearly with a signal. Phase-change memory (PCM) [31, 32], resistive random access memories (RRAMs) [33] and ferroelectric (FE) memories [34] are examples of NVMs which have been demonstrated from device to system levels for implementing neural networks. However,
these devices are limited by their large energy consumption, nonlinear transfer characteristics and slow response time (require $> 100$ ns voltage pulses) [21].

The performance of any neural network for classifications is usually determined by implementing it to identify the Modified National Institute of Standards and Technology (MNIST) database [35], a large database of handwritten digits. Figure 1.9 shows the estimated device parameters and the system-level metrics of different RRAM devices for classifying a million MNIST images. For all RRAM devices, the parameters are significantly far from the targeted values and the accuracy of classification is very poor.

Alternate NVM, i.e. ferromagnetic tunnel junctions have been designed [36] and demonstrated [37] for in-memory computing with $\leq 50$ ns. Besides, domain wall device similar to STT-domain wall device has been proposed [38] and demonstrated [39] to some extent for synaptic applications. However, these devices do not possess the required characteristics (i.e. linearity, programmable thresholding, latency etc.) for implementing for in-memory or neuromorphic computation. Using
the domain/domain walls in a magnetic wire and MTJ, we have developed prototype magnetic devices, which operates with < 10 ns current pulses, shows energy consumption comparable to PCM and RRAM devices and demonstrates the required linear characteristics. Most importantly, these devices can be designed to operate as the programmable thresholding devices, unlike any other non-volatile technologies. We explore such devices in this thesis.
1.3 Organization of the thesis

In this thesis, we have studied nanoscale magnetic materials, domain wall physics inside micro/nano wires made of these materials and their application for more energy-efficient logic devices and accelerators for neuromorphic computation.

In chapter 2, we discuss the domain wall motion inside sub-100-nm width wire. Such narrow wires are important for technological applications of domain wall based devices. We have developed low-edge-roughness lithography technique using bilayer resists for closely spaced 25-nm-wide magnetic wires to explore the technological challenges for driving domain walls in these wires. Edge-roughness is inevitable for any natural or artificial wires specially for those patterned lithographically – it results from the nature of chemical reactions in the patterning resists during exposure which then transfers to the actual wires. Using high-resolution (HR) electron-beam (e-beam) resist, high-energy e-beam and high-contrast resist-developer, we ensure the low-edge-roughness of the wires. And we solve the challenge of removal of the HR e-beam resist by adding a sacrificial e-beam resist underneath. We characterize the line-edge-roughness (LER) of these wires and determine if there is any correlation of domain wall motion with LER. This correlation lead to identify discrete stable domain wall positions inside the nanowires. If the nanowire is designed as an electrode of magnetic tunnel junctions, the discrete positions for domain walls gives the resolution of magnetoresistance, which is a key parameter for analog synaptic devices suitable for neural network.

In chapter 3, we study domain wall motion in a ferrimagnetic material to explore its fast dynamic behavior. Atiferromagnetic materials (with antiparallelly aligned spins of equal magnetization and zero magnetic and angular moments) are the fastest magnetic materials in terms of spin dynamics. Because of the high exchange energy between spins, antiferromagnetic materials show the fastest
switching speed among all the magnetic materials. However, the spins in antiferromagnetic materials are difficult to manipulate or detect electrically which is essential for their applications in emerging logic or memory devices. Ferrimagnetic materials also have antiparallelly aligned spins but from two different lattices. As a result, their total moments can be tuned by changing the composition or the temperature of the materials. Depending on the two sublattices, two different compensation point can be achieved – magnetic moment compensation point and the angular momentum compensation point. Rare earth – transition metal (RE-TM) alloys are examples of ferrimagnetic materials where RE and TM forms the two sublattices. Since electrical responses depend on the fermi-surface and only d-electrons of TM are near the fermi surface, these materials are easy to manipulate electrically like the ferromagnets. However, due to the high exchange energy like the antiferromagnet they should switch fast like the antiferromagnet. These properties make the ferrimagnet an interesting platform for spintronic dynamics research. We explore the fast dynamics of a ferrimagnet material studying the domain wall motion in the RE-TM alloy *i.e.* CoTb. By varying the composition of Co and Tb, we measure the domain wall velocity in microwires fabricated with different compositions. The magnetization and the angular momentum compensation of CoTb do not occur at the same composition. Therefore, we identify which compensation point is essential for the faster domain wall velocity. Moreover, we use analytical model to explain our observations. Domain walls’ internal structure is very crucial for their efficient motion with an applied current. Therefore, we also characterize the types & the chirality of domain walls in CoTb samples across those compensation points.

In chapter 4, we demonstrate logic functionality of magnetic domain wall based devices, a potential candidate for beyond-CMOS computation. We utilize an in-plane magnetic tunnel junction to define the ‘1’ and ‘0’ of binary logic devices based on the resistances. This all-metallic
three-terminal device act as NOT or Buffer gate if a single input is applied. The same device would operate as a NAND or AND, NOR or OR gate if multiple inputs could be combined in the input terminal. We have developed a complete process for designing the binary magnetic tunnel junction devices with a single magnetic domain wall. We address the challenges of device fabrication, demonstrate the operations of the devices with current pulses, discuss device-to-device variability and estimate the energy consumption.

Chapter 5 covers our research on the development of magnetic domain wall based devices for synaptic and activation function evaluation. Using optical read-out, we first show that the domain wall not only show linear motion in a magnetic wire, it can be designed to move nonlinearly with an applied current. However, optical read-out is not suitable for technological applications. Therefore, we develop thin films for perpendicular tunnel junctions as they are more energy-efficient compared to IMA materials. We demonstrate step-by-step development of PMA tunnel junctions. We use slightly different fabrication technique to build these devices compared to those in Chapter 4 and reduce an e-beam lithography step in the processing as it saves time, cost and complexity of fabrication. Magnetic tunnel junctions cannot support domain walls inside them and therefore, we design a synaptic device with multiple tunnel junctions to demonstrate a discretized version of the analog counterpart. In three-terminal synaptic device, tunnel junctions are built on top of wires with linearly varying width along their length. For discretized thresholding, we vary the size of the tunnel junctions to implement arbitrary monotonic nonlinear functions. Our synaptic devices overcome the two critical issues - linearity and asymmetry, and our thresholding devices will improve the latency of multilayer neural network by eliminating the requirement of analog-to-digital conversion between layers.
Finally, in chapter 6, we summarize our findings and provide an outlook of the magnetic domain wall based devices.
References


2 Spatial resolution of magnetic domain wall motion

Magnetic domain walls (DWs) translated by an electric current or a magnetic field, can serve as an information token in logic and memory devices [1-7]. These devices rely on unimpeded motion of the DWs along magnetic wires, and/or the pinning of DWs at specific engineered pinning sites such as notches. However, DW motion and pinning can be affected by local variations in magnetic anisotropy resulting from the microstructure or by fabrication defects that are exacerbated at small device length scales. As the wire widths decrease below ~100 nm, the line edge roughness (LER) of the wires becomes increasingly significant in providing trapping sites leading to stochastic DW behavior, and thus presenting a major challenge for device reliability [6, 8].

Experimental studies of the statistical behavior of DW motion have been reported for wires with widths on the order of a few hundred nanometers [9, 10]. Pinning sites were found to be randomly located in these wires, having little correlation with edge roughness [11]. Device scaling considerations have motivated the fabrication of narrower wires with linewidths of < 100 nm [6, 12, 13]. Indeed, edge roughness becomes more important for narrow widths, and furthermore, as the pitch of the lines decreases, interwire magnetostatic interactions start influencing DW dynamics. Thus, an understanding of the statistics of DW depinning and propagation in nanowires with small width and pitch is essential to the technological development of domain wall nanoelectronic devices.
In this chapter, we will develop an analytical model for predicting the stochastic behavior of DW motion in sub-100-nm-wide wires due to the LER arising from lithographic resolution of the fabrication process.

2.1 Micromagnetic Simulation

![Figure 2.1(a) Scanning electron microscope image of a 30-nm-wide wire (nanowire 1), (b) initial position of the DW in discretized nanowire 1, (c) traveling distances of DWs in five different discretized nanowires after applying magnetic field along their length. Insets show the DW at pinning sites A, C and D in nanowire 1. The DW was not pinned at B [14].](image)

We first describe the statistical behavior of a field-driven DW in an IMA rough-edged nanowire simulated using the Object Oriented MicroMagnetic Framework (OOMMF) software [OOMMF: Object Oriented MicroMagnetic Framework 2002] [15]. The edge profile of the nanowire is discretized from a scanning electron microscope (SEM) image of a 30-nm-wide nanowire (Figure 2.1(a)) using a cell size of $3 \times 3 \times 2.5 \text{ nm}^3$. The wire is 5 nm thick with saturation magnetization
$M_s = 1.44 \times 10^3$ kA m$^{-1}$, exchange stiffness of $A = 1 \times 10^{-11}$ J m$^{-1}$ and randomly oriented uniaxial magnetocrystalline anisotropy of 100 Jm$^3$ (Figure 2.1b). The simulation is repeated for five different images of nanowires of similar width and thickness. Figure 2.1c shows the simulated results of DWs’ propagation in the wires. We observe DW trapping at notches created by the line width roughness (LWR). For example, in the nanowire highlighted in Figure 2.1b, the DW is pinned at a 6-nm-deep notch (C) positioned 244 nm from the left end of the wire, with a depinning field of 16.7 kA m$^{-1}$. The stepwise movement of the DWs between pinning sites at fields up to few tens of kA m$^{-1}$ agrees with the experiment described in the next section and supports the assumption that edge roughness is primarily responsible for DW pinning in these wires and the observed LWR distribution gives rise to a distribution of pinning sites.

LER of nanowires is statistically self-affine [16-18]. Broadly, any edges are self-affine if they look smooth over large length scales, but close-up, appear like the coastlines familiar from fractals [18, 19]. The transition between smooth and rough length scales is defined by the correlation length, $\xi$, a property of the particular fabrication process used to make the wires. The central result of this work is that the correlation length determines the spatial quantization in the wire because it is the shortest length scale before the amplitude of the edge roughness begins to decrease at finer resolution [19-21]. Thus, the coastline of the wire can be understood as a series of harbors of width $\sim \xi$. Each harbor contains finer edge roughness, but if the domain wall width is smaller than $\xi$, then each harbor roughly corresponds to a single dominant trap site for a domain wall.

To analyze the impact of edge roughness, we fabricate magnetic nanowires, characterize their edge profiles, and compare to self-affine fractal models. Previously, the Weierstrass-Mandelbrot (WM) model has been used to describe the edges of wires, such as those of antennas [18]. The edge
deviation $\Delta y$ as a function of the position $x$ along the wire length is given by the WM model in one dimension:

$$\Delta y(x) = B_{LER} \sum_{p=1}^{\infty} C_p \nu^{-pH_Q} \sin \left[ \frac{2\pi}{\xi} \nu^p \left( x \cos \Psi_p \right) + \Phi_p \right]$$

2.1

The WM model is appropriate to model a self-affine wire because it starts with a sinusoid with an amplitude $B_{LER}$, defined by the line edge roughness of our fabricated wires, and a period $\xi$, defined by the correlation length. Then, additional higher-frequency modes are added, with decreasing amplitude and increasing spatial frequency. The Hurst exponent, $H_Q = 0.3$, and the seed of the geometric progression that accounts for spectral separation, $\nu = 1.5$, are empirical parameters taken from the antenna model in reference [18]. $H_Q$ represents how weak the higher frequency modes become. Since $\nu$ is not unity, the spatial frequency of higher modes increases nonlinearly rather than as integer multiples like harmonics. Furthermore, the amplitudes $C_p$ of each mode are randomized with a Gaussian distribution with zero mean and a standard deviation of 1, and the phases $\Psi_p$ and $\Phi_p$ of each mode are randomized with a uniform distribution on $[-\pi, \pi]$. 

![Power Spectral Density](image-url)
Figure 2.2 Power spectral density of the line edge roughness of the discretized wire, the average of 104 synthesized self-affine wires, and the average of 104 synthesized random-edge wires. The correlation length, $\xi$, is extracted from the discretized wire and is applied to synthesize the self-affine wires [22].

The power spectral density (PSD) of line edge roughness in the measured wires is shown in Figure 2.2. Straight lines such as Figure 2.1a are characterized to extract the parameters: $B_{LER} = 2$ nm and $\xi = 255$ nm, as determined from the knee of the PSD at $1/\xi$ [19]. The concentric ring nanowires exhibit similar edge roughness, but longer correlation lengths of $\xi = 0.99 \mu$m.

For comparison with the experimentally determined edge roughness distribution of the Co wires, we numerically synthesize wires with self-affine statistics using Equation 2.1. In addition, we synthesize wires with a random-edge profile, where the edge deviation of each edge cell is randomly assigned a value between -6 nm and 6 nm with a uniform distribution. Good agreement is found between the PSD of the self-affine wires and the experimental wires, but the random-edge wires clearly diverge from the characteristics of real wires. This contrast highlights the key role of self-affine statistics suppressing roughness at short length scales in real wires.

The edge roughness of the wires leads to a variation in the total energy of a domain wall as a function of distance along the wire, with the consequence that a domain wall will be trapped at certain locations as it moves along the wire in response to a magnetic field. In order to determine the distribution of domain wall trap sites and relate domain wall traveling distances to the applied field, we use micromagnetic models of 60-nm-wide, 5-nm-thick Co wires with self-affine or random-edge roughness, discretized by the cell size of $3 \times 3 \times 2.5$ nm$^3$. The Co has random magnetocrystalline anisotropy and its magnetic easy axis is dominated by shape, leading to IMA. For this wire geometry, the domain walls are transverse walls with core magnetization lying in
plane, transverse to the length of the wire, and the domain wall width is similar to the wire width.

Typical domain wall configurations are shown in Figure 2.3.

![Figure 2.3 A single domain wall as shown in micromagnetic models of (a) an IMA wire (mx) and (b) a PMA wire (mz) [22].](image)

A single domain wall is placed at a specific location along a wire, and then allowed to relax at zero field with its final position recorded; this is repeated for all possible starting locations along the wire. Figure 2.4a shows the initial and final domain wall positions for one wire, indicating that there are specific pinning sites or traps along the wire (Figure 2.4b) to which the domain wall is attracted. These are typically locations of local minima in the wire width at which the energy of the domain wall is minimized.

We define $\Delta x$ to be the distance from one discrete domain wall trap to the next one along the wire. In other words, the $\Delta x$ values are the distances between the discrete domain wall traps in Figure 2.4a. Figure 2.5a shows schematics of a nanowire with fractal edges. The major DW traps are defined by the correlation lengths as shown by the red arrows. Figure 2.5b shows the distribution of spacing between domain wall traps in simulations of 41 synthetically generated self-affine wires.
with $\xi = 255$ nm. There is a peak, $\Delta x_0$, for self-affine wires at 85 nm $\approx \xi/3$. Note that the distribution is non-uniform. The mean $\Delta x_\mu = 125$ nm and the standard deviation $\Delta x_\sigma = 77$ nm.

Figure 2.4 (a) Final positions into which domain walls relax from their initial positions of domain wall nucleation, for one wire in micromagnetic simulations. The bin width is chosen to be the size of one simulation cell, 3 nm. Inset: Zoom of initial positions. (b) Line width roughness profile of the wire shows that the traps often correspond to local minima in width [22].
Figure 2.5 (a) Schematics of major DW traps in a nanowire defined by the correlation length $\xi$. (b) Distribution of spacing $\Delta x$ between domain wall discrete positions for IMA wires, including wires with self-affine edge profiles with correlation length $\xi$ and wires with random-edge profiles. The distributions are normalized by area.

In simulations of 30 self-affine wires with a shorter correlation length $\xi = 127$ nm, we find $\Delta x_0 = 33$ nm, showing that $\Delta x_0$ decreases with decreasing $\xi$. In 30 wires with a random-edge profile, the $\Delta x$ distribution shows that domain wall traps are more likely to be spaced closely together. This is consistent with the higher amplitude of roughness at short length scales in a random-edge wire.

![Distribution of spacing $\Delta x$ between domain wall discrete positions for PMA wires, including wires with self-affine edge profiles with correlation length $\xi$ and wires with random-edge profiles. The distributions are normalized by area.](image)

Figure 2.6 Distribution of spacing $\Delta x$ between domain wall discrete positions for PMA wires, including wires with self-affine edge profiles with correlation length $\xi$ and wires with random-edge profiles. The distributions are normalized by area [22].

In contrast, domain walls are narrower in wires with perpendicular magnetic anisotropy (PMA) [23, 24]. In Figure 2.6, we simulate 30 CoFeB wires with PMA. As in the IMA simulations, we find that domain walls relax to positions distributed in discrete locations along the wire. The standard deviation of the trap locations is less than that found in the IMA Co wire simulations since the narrow PMA domain walls interact with mostly high-frequency roughness. We further observe strong anticorrelations between the pinning sites, suggesting that the self-affine edge roughness statistics manifest similarly in PMA and IMA.

After identifying the zero-field pinning sites in self-affine nanowires, we apply steady-state magnetic fields to move the domain walls along 1500 micromagnetic models of synthetic IMA
wires. A domain wall is initialized in a trap on one end of each wire, and the traveling distance of the domain wall to its final position is then calculated after applying the field. Figure 2.7 shows the histograms of the distances traveled by domain walls from an initial trap to a final trap, under four different steady-state magnetic field values. We do not perform this simulation in PMA because domain walls are completely detrapped by the high critical field for motion, i.e., once they start moving they continue until the end of the wire.

![Histograms of domain wall distances](image)

*Figure 2.7 Distributions of distances traveled by domain walls in simulated nanowires. The sample size is 1500 wires. The fractal analytical model is the overlaid line with parameters listed for each applied field [22].*

### 2.2 Analytical modeling of pinning sites

We propose an analytical model for the distribution of the propagation distances of domain walls when applying a steady-state magnetic field $H$:
\[
\frac{df}{dx} = \left( -\frac{1}{l_0} + k\Delta y(x - x_{\text{min}}) \right) f
\]

Here, \(\Delta y(x)\) is the edge profile and \(f\) is the fraction of domain walls that are still propagating at distance \(x\). We define \(x = 0\) to be the initial position of each domain wall, and \(x_{\text{min}}\) is the value of \(x\) at the minimum of \(\Delta y(x)\) within \(0 < x < 1 \mu m\). The fit parameters, \(k\) and \(l_0\), account for the effects on trapping probability that are dependent and independent of edge roughness, respectively. We assume that \(l_0\) characterizes all spatially independent sources of pinning, such as the effect of fluctuations in the magnetic anisotropy within the microstructure. While it is likely that there are spatial correlations in the magnetic anisotropy, we presume that these are on the order of the grain size of \(\sim 10\) nm, and much smaller than \(\xi\). The fit parameter, \(k\), weights the significance of trapping due to edge roughness.

The analytical model \((-df/dx)_{\text{mean}}\) is found by solving Equation (2) with Equation (1) by separating variables:

\[
f(x) = \exp \left( -\frac{x}{l_0} \prod_{p=1}^{\infty} \exp \left( \frac{kB_{\text{LEK}}C_p \xi}{2\pi} \nu^{-p\mu_0+1} \cos \Phi_p - \cos \left( \frac{2\pi}{\xi} \nu^p \left( (x - x_{\text{min}}) \cos \Psi_p \right) + \Phi_p \right) \right) \right)
\]

\[
-\frac{df}{dx} = \left( -\frac{1}{l_0} + kB_{\text{LEK}} \sum_{p=1}^{\infty} C_p \nu^{-p\mu_0+1} \sin \left( \frac{2\pi}{\xi} \nu^p \left( (x - x_{\text{min}}) \cos \Psi_p \right) + \Phi_p \right) \right)
\times \exp \left( -\frac{x}{l_0} \prod_{p=1}^{\infty} \exp \left( \frac{kB_{\text{LEK}}C_p \xi}{2\pi} \nu^{-p\mu_0+1} \cos \Phi_p - \cos \left( \frac{2\pi}{\xi} \nu^p \left( (x - x_{\text{min}}) \cos \Psi_p \right) + \Phi_p \right) \right) \right)
\]

\[
\left( -\frac{df}{dx} \right)_{\text{mean}} = \frac{1}{N} \sum_{w=1}^{N} \left( -\frac{df}{dx} \right)_w
\]
We use $-\frac{df}{dx}$ because it is the derivative of $1 - f$ that gives how many DWs are trapped at a certain distance $x$. We expect $\frac{df}{dx} < 0$ because $f(x = 0) = 1$ and $f$ decreases with $x$ until all domain walls have been trapped. We determine the analytical model $(-\frac{df}{dx})_{\text{mean}}$ in Equation (5) by calculating Equation (4) for $N = 1500$ wires. The coefficient $k$, which weights the edge profile $\Delta y(x)$ in the substitution of Equation (1) in Equation (2), represents the magnitude of width effects and is chosen such that $(-\frac{df}{dx})_{\text{mean}}$ is still positive and the total area under the curve converges to unity.

The solution is a function of random variables, thus for fitting purposes we determine $(-\frac{df}{dx})_{\text{mean}}$, the average of $(-\frac{df}{dx})$ for $N = 1500$ wires. In Figure 2.7, $(-\frac{df}{dx})_{\text{mean}}$ is fitted to the distributions of distances traveled by domain walls in IMA Co wires found in the simulation.

The analytical model parameters, $l_0$ and $k$, obtained from fits to the simulation data, are listed in Figure 2.7. As expected, $l_0$ increases with increasing $H$ since domain walls move farther at higher fields before encountering a trap that can prevent further motion.

As shown in Figure 2.7, the simulations and analytic model for domain wall propagation in nanowires with self-affine edge profiles show oscillations in trapping probability over distances equivalent to multiple correlation lengths. The strongest impact of edge roughness, however, occurs within the first correlation length. Under this approximation, we can then simplify the analytic model to the width-independent term, $-1/l_0$, and a width-dependent exponentially decaying auto-correlation term:

$$\frac{df}{dx} = \left(-\frac{1}{l_0} + b \exp(-x/\lambda)\right)f$$

2.6

The simplified analytical model with Equation 2.6 is solved as follows:
\[
- \frac{df}{dx} = \left( -\frac{1}{l_0} + b \exp(-x/\lambda) \right) \exp\left( -\frac{x}{l_0} + b\lambda(1 - \exp(-x/\lambda)) \right)
\] 2.7
2.3 Experiments and Results

To verify the analytical modeling, we conducted experiments using the lithographically patterned Co wires to identify the density of statistical pinning sites for domain walls.

2.3.1 Patterning of closely-packed nanowires

Patterning of thin films into sub-100 nm features is essential so that the magnetic logic and memory devices [25] can have switching energies competitive with those of CMOS-based devices [26, 27]. Here, we describe a method for patterning metallic wires down to 25 nm width. In particular, low edge-roughness is prioritized for reproducibility of the magnetic switching characteristics. Besides, edge-roughness in the nanostructures can act as a domain wall trap, increasing the energy required to translate a domain wall through a wire, or can promote the formation of reverse domains [28-30]. We use a removable bilayer polymethyl methacrylate (PMMA) and hydrogen silsesquioxane (HSQ) resist mask combined with ion beam etching. A PMMA/HSQ bilayer has been investigated previously for liftoff processes [31, 32], but has not been explored as a mask for subtractive patterning. The bilayer process described here was developed to facilitate patterning of transition metal alloy films, with Co$_{60}$Fe$_{20}$B$_{20}$ (CoFeB) chosen as a primary example. However, reactive ion etching of transition metals and their alloys is difficult since they form involatile halides when treated with many common reactive etching gases [33]. Thus, high-resolution subtractive patterning is usually done using ion beam etching (ion milling), focused ion beam patterning, or damascene processes to selectively remove the metal.

HSQ is an excellent negative-tone resist for high-resolution electron beam lithography down to 4.5 nm half-pitch. However, after exposure and development, the etch resistance of crosslinked HSQ increases [32], and its subsequent removal requires hydrofluoric acid or a CF$_4$ reactive ion etch; both can damage an underlying metallic thin film. This motivated our development of a
bilayer resist process which combines the high etch resistance of HSQ with a PMMA layer that allows removal of the HSQ features using a solvent such as n-methyl-2-pyrrolidone (NMP) or acetone, after etching the metal film.

Figure 2.8 (a-f) Schematic illustration of the step-by-step fabrication process. (g) Cross-sectional SEM image after step 4 showing the bilayer resist on top of the CoFeB thin film. Top down SEM images (h) after ion beam etching to transfer the feature into the metal (step 5) and (i) resulting 50 nm wide CoFeB wire (step 6).

Figure 2.8(a-f) shows the process flow for patterning the magnetic structures. All patterning was done on silicon substrates with a native oxide. In step 1, amorphous Ta (3 nm)/CoFeB (10 nm)/Au (3 nm) films were deposited using UHV DC magnetron sputter deposition at $2 \times 10^{-8}$ Torr. In step 2, 2% PMMA in anisole was spun at 4 krpm for 60 s and baked at 180 °C for 90 s to produce a film thickness of 30 nm. Then 2% HSQ in methyl isobutyl ketone was spun at 4 krpm for 60 s and baked at 110 °C for 60 s to produce a film thickness of 30 nm. In step 3, the HSQ was exposed. For line widths >50 nm, a Raith 150 electron beam lithography tool was used at 30 keV electron energy and 400–800 μC/cm² dose. The samples were developed using 2.4%
tetramethylammonium hydroxide in water (CD-26) developer for 2–4 min. For <50 nm line width, an Elionix F-125 e-beam lithography tool was used at 125 keV with dose 32 mC/cm² and developed using 4% NaCl/1% NaOH in water for 20 s. The electron beam exposure of the HSQ caused scission in the PMMA beneath the HSQ, which increased its solubility, so HSQ development had to be carried out using nonsolvents for PMMA.

In step 4, an O₂ RIE was performed at base pressure $1 \times 10^{-4}$ Torr, using 10 sccm oxygen and 90 W, for 60–180 s. The etch time was chosen to produce an undercut in PMMA under the HSQ. In step 5, ion beam etching was used to transfer the pattern into the CoFeB using Ar⁺ ions at base pressure $1 \times 10^{-7}$ Torr, with Ar flow of 1.5 sccm, 10 mA beam current, and a 2 cm beam diameter.

In step 6, the PMMA/HSQ mask was removed by placing the sample in NMP at 135 °C for 90 min, sonicating for 30 min, leaving the sample in NMP for 15 h unheated, then sonicating again for 30 min. This dissolved the PMMA and removed the HSQ. The extended removal time is required due to redeposition of the HSQ on the sidewalls of the structures during ion milling, which reduced the surface area of PMMA exposed to the solvent.

Figure 2.8(g-i) shows scanning electron microscope (SEM) images during different steps of the process. Figure 2.8g shows a cross section of the double-resist stack after step 4, on top of CoFeB film. There is undercut in PMMA. The HSQ line was nominally 50 nm wide, with an actual average width of $w_{\text{HSQ}} = 49$ nm (to within ±5%, from the SEM images); the PMMA had $w_{\text{PMMA}} = 23$ nm. The HSQ was 30 nm thick, with 40 nm thick PMMA underneath. We ensured the HSQ thickness was thicker than the 14 nm thick film, since the ion beam etch rate was found to be similar for HSQ and the metallic film. The O₂ RIE process time of 120 s was chosen to produce an undercut in the PMMA so that the high-resolution HSQ mask defined the eventual feature size in the metal.
Figure 2.8h shows the sample after step 5 with \( w = 59 \) nm at the base of the feature. The mask shows a tapered cross section after ion beam etching. Figure 2.8i shows a top-down view of the CoFeB wire after step 6 with \( w = 55 \) nm, close to the width of the HSQ mask.

![Image](image_url)

Figure 2.9 Cross-sectional SEM images of bilayer resist stack after 1 min O\(_2\) RIE (step 4), for HSQ widths (a) 468 nm, (b) 261 nm, (c) 95 nm, and (d) 61 nm. This RIE time was not long enough for the wider two HSQ masks and did not produce an undercut. (e) SEM image of metal wire showing only partial mask removal due to nonoptimized RIE time [34].

Figure 2.9 demonstrates the effects of the linewidth on the undercut of the PMMA. The bilayer resist in this example was made from higher concentration solutions of 4\% PMMA in anisole and 4\% HSQ in methyl isobutyl ketone keeping all other parameters the same as above to improve visibility of the stack during SEM. The HSQ was exposed at 10 keV and developed to form lines with \( w_{HSQ} = \) (a) 468 nm, (b) 261 nm, (c) 95 nm, and (d) 61 nm (±5\%) followed by step 4 O\(_2\) RIE for 60 s. The HSQ is slightly tapered in (a) and (b), which could be due to backscattered electron exposure. The SEM images show that while this RIE time produced an undercut of PMMA for
\( w_{HSQ} < 100 \, \text{nm} \) in (c) and (d), it was insufficient to produce an undercut in the wider lines of (a) and (b), \textit{i.e.}, the \( O_2 \) RIE time must be matched to the desired wire width. The linewidth dependence of the PMMA undercut may originate from differences in the electron beam exposure of the PMMA affecting its response to the oxygen RIE. Figure 2.9e shows a top–down SEM image of a metal wire after ion beam etching for a case where the RIE time was optimized for wires narrower than 100 nm. A remaining part of the mask can be seen on the metal wire in the upper part of the image.

Figure 2.10 shows closely spaced arrays of patterned lines of 20 nm – 50 nm width at different pitches. The lines were exposed with a 125 keV electron beam and area dose of 6.4 mC/cm\(^2\). This dose is lower than that used for isolated lines (32 mC/cm\(^2\)) due to proximity effects of the nearby lines. The proximity effect was similar to that of a single layer of HSQ, since only the HSQ is developed and not the PMMA. Below 2\( w \) pitch, 20 nm and 30 nm lines were not resolved for these exposure and development conditions.
<table>
<thead>
<tr>
<th>Pitch</th>
<th>4w</th>
<th>3w</th>
<th>2w</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wire Width (nm)</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>After O2 RIE</td>
<td><img src="image1.png" alt="Image" /></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>After O2 RIE</td>
<td><img src="image2.png" alt="Image" /></td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>After O2 RIE</td>
<td><img src="image3.png" alt="Image" /></td>
<td></td>
</tr>
</tbody>
</table>

Figure 2.10 Scanning electron microscope images of 20, 30 and 50 nm wires with 2w, 3w and 4w pitches, where w is the width of the wires [35].
The root-mean square (RMS) line edge roughness (LER) of these lines, calculated as described below, was $r_{\text{RMS}} = \sim 2$ nm, which is similar to those of isolated lines of same width. We conclude that the proximity of multiple lines does not affect the LER of small-pitched CoFeB lines patterned using this method.

![Figure 2.11 Average LER vs wire width. The standard deviation is measured across five separate wires on the same substrate. Wires are patterned with electron beam acceleration voltage of (a) 125 keV and (b) 30 keV [34].](image)

Figure 2.11 describes the $3\sigma$ and RMS LER vs. wire width $w$. For each nominal $w$, five SEM images (pixel size 0.89 nm) were taken of different wires patterned on the same substrate. Both the average and standard deviation of RMS LER were then calculated by measuring the edge deviation in nanometer along the wire using summit Litho Analysis Software [36]. We find RMS roughness is $\sim 2$ nm independent of wire width. These wires were up to 1 mm long, and the RMS roughness is the same at several different locations measured along the length. The LER of the patterned HSQ layer is 0.6–0.7 nm, so there was an increase of 1.3–1.4 nm in LER when the pattern was transferred from the HSQ to the metal by ion beam etching. The electron beam voltage was increased from 30 to 125 keV for wires $<50$ nm to reduce the electron beam diameter.

This roughness is small compared to domain wall widths (i.e., $\sim 45$ nm in 25 nm wide wires with in-plane magnetic anisotropy). Narrow magnetic wires will be useful for magnetic logic and
memory applications, where magnetic domain walls have to propagate long distances driven by low magnetic fields or current densities.

2.3.2 DWs motion in nanowires

Experiments were conducted on nanowires made from Ta/Co/Au films, patterned using electron beam lithography with two-layer resist and ion beam etching as described in Section 2.3.1. The magnetic moment of the film indicates a Co thickness of 5 nm. Two sets of wires are patterned. First set consists of 80 nm wide, 40 nm spaced wires formed as concentric rings and as L shapes with curved corners of similar radii as the rings (5–5.5 μm). A second set consists of 60 nm wide, 30 nm spaced wires formed as concentric rings only.

In thin, narrow wires, DWs have a transverse Néel configuration with wall length similar in size to the wire width, and in-plane magnetization transverse to the wire at the core. The stray field around a DW in a 60 nm wide and 5 nm thick nanowire is shown in Figure 2.12a. Black arrows inside the nanowire indicate the magnetization direction and outside the nanowire show the stray field in the plane of the wire, with the locations of the neighboring wires shown by the dotted lines. The stray field magnitude along a trajectory through the center of the DW perpendicular to the nanowire in the plane of the film is shown in Figure 2.12b. The stray field has a strong dependence on distance from the wire, and it is different on each side of the wire because of the contribution from the transverse DW core. The stray field on the high-field side of an 80 nm wide nanowire at a distance of 40 nm (corresponding to the nearest edge of the next wire) and 80 nm from the edge (corresponding to the center of the next wire) is 23 kA m\(^{-1}\) and 7.1 kA m\(^{-1}\), respectively. For a 60 nm wide nanowire, the stray field at a distance of 30 nm (edge of the next wire) and 60 nm (center of the next wire) is 31 kA m\(^{-1}\) and 12.5 kA m\(^{-1}\), respectively. Both 60 nm wide and
80 nm wide wires produce quite similar stray field distributions and the main difference in interaction field is caused by the larger spacing of the 80 nm wide wires. Thus, DWs in the 80 nm wide, 40 nm spaced wires are more weakly coupled to one another than in the 60 nm wide, 30 nm spaced wires or assumed to be individual wires. For DWs with the same core magnetization direction, as produced by the field saturation process used here, the magnetostatic interaction between the DWs in adjacent wires is attractive.

**Figure 2.12** (a) The magnetization distribution inside a 60 nm wide nanowire and the in-plane stray field distribution outside the wire. Navy solid lines show the two edges of the wire and blue dotted lines show edges of neighboring nanowires. The red and the blue background outside the wire shows the stray field strength. (b) Stray field distribution from a DW in a smooth-edged nanowire of width 60 nm and 80 nm as a function of distance from the wire. Red and blue markers show the stray field along the red and blue arrows in (a), respectively, perpendicular to the core of the DW.

DW translation under an in-plane applied field is measured in both sets of nanowires using magnetic force microscopy (MFM). Before each measurement, we apply a magnetic field of 239 kA m⁻¹ along the x-direction in the rings to yield remanent onion states with two opposite 180° DWs along the diameter in each ring [37, 38]. An MFM image of the tail-to-tail DWs (dark dots) and the head-to-head DWs (bright dots) in the onion states of the 80 nm wide rings is shown in
Figure 2.13b. Figure 2.13(c) shows a zoomed in view of the MFM image of the tail-to-tail DWs in the 60 nm wide rings. In this experiment, only the tail-to-tail DWs are measured.

![Images of Co wires, MFM images, and zoomed-in MFM images of tail-to-tail domain walls.](image)

**Figure 2.13** (a) SEM image of Co wires of 80nm in the shape of concentric wires. (b) MFM images of initial positions of tail-to-tail and head-to-head domain walls. Insets show the Neel domain walls configuration in IMA Co wires. (c) Zoomed-in MFM image of the 15 individual tail-to-tail domain walls in 15Co nanowires. The white dotted lines show the edges of the wires.

![Images of L-shaped wires.](image)

**Figure 2.14** (a) SEM images of L-shaped wires. (b) Initial positions of the tail-to-tail domain walls in the cured regions of the L-shaped wires.
For the L-shaped nanowires the field was applied at 45° bisecting the L, producing DWs at the center of the curved region. These applied fields are much lower than the Walker breakdown field of the DWs in the nanowires. When the applied field is high enough to depin the DWs from their initial remanent position, they move until they encounter a pinning site that impedes further motion. The initial and final positions of the DWs are measured for each in-plane field, with the DWs reset by 239 kA m⁻¹ saturation after each field value.

The domain walls in the nanowires experienced the magnetic stray field from the magnetic force microscope probes during scanning which can perturb their positions. To exclude this possibility, we note there was no dragging of domain walls evident in low-resolution (large scan area) magnetic force micrographs. The dragging effect is more prominent in samples imaged after applying small fields and it decreases with higher applied fields. Domain wall displacements showing any evidence of domain wall dragging by the probe were removed from the statistical analysis. Otherwise, magnetic force microscopy is considered as a noninvasive process, and domain wall positions can be determined to within 50 nm.

2.3.2.1 DWs in individual nanowires

The translation of domain walls in the nanowire rings required fields > 16 kA/m, much higher than the coercive field of the continuous Co film, which is 2 kA/m. Figure 2.15a and Figure 2.16 show the MFM images of nanowire rings and L-shaped nanowires after applying different magnetic fields along the wire.
Figure 2.15 (a) Magnetic force microscopy images of domain walls in concentric rings with applied magnetic fields of 20 kA/m, 24 kA/m, 28 kA/m, and 32 kA/m along the y-axis. The black and the white arrows indicate the positions of two separate domain walls in two different nanowires at different magnetic fields. (b) Fractal analytical model and (c) exponential analytical model overlaid on distributions of distances traveled by domain walls in experiment. The sample size is 94, 94, 83, and 134 wires in increasing order of applied fields [22].
The average traveling distances of the domain walls increased with field, but some of the domain walls remained at the same position even after applying a higher magnetic field. For example, the domain wall marked by a black arrow in Figure 2.15a remained at the same position at 20 kA/m and 24 kA/m, was translated after applying 28 kA/m, then remained pinned at 32 kA/m. Similarly, the domain wall marked by the white arrow changed its position when the field increased from 20 kA/m to 24 kA/m and remained at that site at 28 kA/m and 32 kA/m. In this case, the depinning field of the first site was between 20 kA/m and 24 kA/m, and the second was more than 32 kA/m.

Figure 2.15b shows our experimental results of the nanowire rings after applying different magnetic fields along the wires. The data include the DWs from both concentric rings (for DW movement of $< 2.5 \, \mu m$) and the straight part of the L-shaped nanowires (for DW movement of $> 2.5 \, \mu m$). For the lower fields, the distributions show that travelling probability of the DWs decreases with distances. However, for the two large fields, the DWs travelling probabilities show distinct maxima.
In Figure 2.15b, \((-df/dx)_{\text{mean}}\) is fitted to the distributions of distances traveled by domain walls in IMA Co wires found in experiments. The fit between \((-df/dx)_{\text{mean}}\) and the experimental data in Figure 2.15b also shows an increase in \(l_0\). The constant \(k\) decreases with increasing \(H\) in fits to both simulation and experimental data. We find that \(\zeta = 0.99\ \mu\text{m}\) in the analytical model fits the experimental data well, and this value of \(\zeta\) matches the correlation length extracted from the PSD of the specific concentric ring wires (Figure 2.13a) fabricated for the experiment.

We fit the simplified model in Equation 2.7 to the experimental data in Figure 2.15c. We choose \(\lambda = 0.4\zeta\) because the distance to the first trap can be approximated by \(\Delta x_0\), which is roughly \(\zeta/3\) and \(0.45\zeta\) in Figure 2.5b, for \(\zeta = 255\ \text{nm}\) and \(127\ \text{nm}\), respectively. In the fit in Figure 2.15c, \(\zeta\) remains the same as in Figure 2.15b, \(l_0\) has values similar to those in Figure 2.15b and also increases with \(H\). The fit constant \(b\) represents the weight of the exponentially decaying term corresponding to line edge roughness. We have sufficient experimental data and resolution in the magnetic force micrographs to group the propagation distances into 0.5-\(\mu\text{m}\)-wide bins. Given this constraint, we require higher fields such that \(l_0 >> 0.5\ \mu\text{m}\) to image any effects of roughness. Indeed, clear deviation from an exponential decay with \(b > 0\) is observed in the highest field case of \(H = 32\ \text{kA/m}\), confirming the effect of edge roughness in these wires.

Here, fabrication of narrow self-affine magnetic nanowires is found to generate a discrete distribution of domain wall traps. The maximum density of locations at which a domain wall can be found at remanence is observed in the peak of \(\Delta x\) distributions, found to be below \(\zeta\). For a representative correlation length of \(\zeta = 255\ \text{nm}\), the PMA wires have an information density of \(1/\Delta x_\mu \sim 14\ \text{positions}/\mu\text{m}\), higher than that of the IMA wires, \(1/\Delta x_\mu \sim 10\ \text{positions}/\mu\text{m}\). When domain walls are moved by a magnetic field or current, the distribution of their distance traveled can be modeled analytically by Equation (2), whose width-independent component creates the
shape of an exponential decay with increasing distance and whose width-dependent component is based on the edge deviation fractal model. Notches with a higher pinning potential than that derived from line edge roughness may be introduced for predictable control, but at the cost of decreasing the information density. These results are relevant to the scaling performance of domain wall devices into regimes where line edge roughness dominates the energy landscape in which the walls move.

2.3.2.2 Effect of magnetostatic interactions on stochastic domain wall motion

In the previous section, the distance travelled by a DW in 80 nm wide and 40 nm spaced Co nanowire under an applied magnetic field are fitted to a function that included a roughness-dependent and a roughness-independent term. However, this approach did not consider the magnetostatic interactions between DWs in closely-spaced nanowires which can affect the propagation of DWs. In this section, we report on the distribution of pinning sites for DWs moving in parallel nanowires with strong magnetostatic interactions, and show that these interactions qualitatively change the DW propagation distances.

Figure 2.17(a) show the MFM images of 80 nm wide nanowire rings after applying different magnetic fields in the range of 20 kA m⁻¹ to 32 kA m⁻¹, respectively (Same as Figure 2.15(a)). The white and the black arrows indicate the DWs in two weakly interacting nanowires. The average translation distances of the DWs increased with field, although some of the DWs are trapped at the same position even after re-initializing the DWs then applying a higher magnetic field. Figure 2.17(b) show the MFM images of the 60 nm wide wires at the same fields and the blue and the yellow arrows indicate the final positions of two DWs in two strongly interacting nanowires.
Figure 2.17 (a) weakly interacting and (b) strongly interacting Co concentric rings after applying a magnetic field of 20 kA m$^{-1}$ and 32 kA m$^{-1}$ along the y direction. Black and white (blue and yellow) arrows indicate the positions of two separate domain walls in two weakly (strongly) interacting nanowires at different magnetic fields.
We have done the statistical experiment with magnetic fields on 300 wires of 60 nm wide, and 30 nm spacing concentric rings.

Figure 2.18 Experimental measurement of the stochastic nature of domain wall motion. Histograms of the traveling distance of DWs in (a) weakly interacting wires and (b) strongly interacting wires at different fields. The blue dashed lines in (a) show the distributions of DW displacement according to the proposed model. The pink dotted line in the bottom left panel shows the distribution with \( b = 0 \) in the proposed model [14].
For side-by-side comparison, we showed the pinning histograms of individual or weakly interacting magnetic nanowires again in Figure 2.18. Figure 2.18 show the histograms of the DW displacement at different fields for both types of nanowires. We will focus here on a comparison of the field-driven displacements below 3 µm in the two types of nanowires. A striking result is that at higher fields (28 kA m\(^{-1}\) and 32 kA m\(^{-1}\)) the 80 nm wide nanowires show a pinning probability that initially increases with distance, whereas the 60 nm wide nanowires show a monotonic decrease.

The blue dotted lines in Figure 2.18(a) (Same as the black solid lines in Figure 2.15c) show fits of Equation 2.7 to the data from the 80 nm wide wires. In contrast, for the 60 nm wide wires which are strongly interacting, the data are well fitted by setting \(b = 0\) yielding a simple exponential function (Figure 2.18(b)). In comparison \(b = 0\) yields a poor fit for the 80 nm wires as shown by the dotted pink line in the last panel of Figure 2.18(a). The fitting parameters in Equation 2.7 for the two sets of wires are given in Table 2.1.

Table 2.1 Fitted parameters describing the pinning probability per unit length. For weakly coupled nanowires \(l_0\) and \(b\) are extracted by fitting Eq. (2.7) with \(\lambda = 0.4\) µm. For strongly coupled nanowires \(l_0\) is extracted from Eq. (2.7) with \(b = 0\).

<table>
<thead>
<tr>
<th>Applied Field (kA m(^{-1}))</th>
<th>(l_0) (µm)</th>
<th>(b) (µm(^{-1}))</th>
<th>(l_0) (µm)</th>
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</thead>
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<tr>
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<td>2.25</td>
<td>0.01</td>
<td>0.79</td>
</tr>
<tr>
<td>24</td>
<td>3.18</td>
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<td>1.33</td>
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<tr>
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<td>32</td>
<td>6.07</td>
<td>0.07</td>
<td>2.69</td>
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</tbody>
</table>

61
To understand the implications of these results, we first note that $l_0$ represents the effects of the spatially invariant (uncorrelated) pinning sites. $l_0$ increases with field as the probability of pinning decreases and DWs move further before encountering an effective pinning site. It is smaller for the strongly interacting wires because the magnetostatic interactions provide additional pinning that impedes the motion of DWs.

The differences in DW propagation in the wires are most evident in the value of $b$. The non-zero $b$ is the parameter that leads to the peak in the distributions for the weakly interacting 80 nm wide wires evident particularly at the higher fields (i.e. the peak is at $\sim 1.5$ μm at 32 kA m$^{-1}$). This peak is not present in the data from the 60 nm wide wires. The peak originates from the self-affine fractal edge roughness which has a characteristic spacing between the larger edge roughness fluctuations that contribute to pinning. Pinning sites are therefore spaced apart, and a DW depinned from one site where it relaxed at remanence statistically does not encounter another deep pinning site until it has moved a certain distance. The increasing importance of the anticorrelation of pinning sites at high applied fields is illustrated by the increase in the weighting parameter $b$ with field.

Both sets of nanowires are patterned on the same thin film sample at the same time and their edge profiles are expected to be the same. We attribute the qualitatively different behavior of the 60 nm wires instead to the magnetostatic interaction between the DWs. The attractive interaction between DWs in neighboring wires favors shorter translation distances, overcoming the effect of the anticorrelated pinning sites originating from the fractal edge roughness, and giving an exponential decay in the distribution of DW propagation distances and $b = 0$. This implies that the magnetostatic interaction between the neighboring DWs suppresses the effect of edge roughness for the range of applied fields in the strongly interacting nanowires.
In short, for weakly interacting wires, counter to the possible expectations of a uniform density of pinning sites along a wire, there is a transition in the statistics at a characteristic length scale, representing the anticorrelations between roughness fluctuations predicted by the self-affine fractal roughness model [39]. However, when wires are closely spaced, interactions between DWs limit the propagation distance, reducing the effect of autocorrelations and leading to a corresponding reduction in the DW propagation lengths.

To summarize this chapter, we have developed a fabrication process for patterning short pitched wires with widths ranging from 25 nm to 100 nm. The edge roughness of the wires are characterized. From statistical analysis of the magnetic domain wall motion in these wires, we have identified there is close relationship between the pinning sites for domain walls and the edge-roughness of the wires. There exists a dominating pinning site within one correlation length of the wire’s edge-roughness – a fundamental limit of information density if domain walls in nanowires are used as the information token. However, if magnetostatic interaction between domain walls in neighboring wires is higher than the threshold fields, the information propagation probability will not be very different compared to domain wall in an individual nanowire. Care should be taken in designing magnetic domain wall based memory and logic devices so that there is little interactions between the domain walls in neighboring devices.
References


3 Domain wall motion in ferrimagnetic materials

Antiferromagnetic materials show the fastest spin dynamics in the THz frequencies. Therefore, the natural choice for ultrafast magnetic devices is utilizing antiferromagnetic materials as the active magnetic layer in the magnetic memories and logic devices. Moreover, immunity to external magnetic field, absence of stray magnetic field make them attractive for ultra-dense integrated spintronic devices. However, detecting and manipulating the magnetic moment of antiferromagnetic materials are not trivial. This motivates to examine the spin dynamics in ferrimagnetic materials, where the spins are aligned antiparallel to each other like the antiferromagnet. Ferrimagnetic materials offers a unique way of modulating the magnetic moment and the angular moments. Ferromagnetic materials are usually alloys of two magnetic materials where the spins of two different materials are aligned antiparallel to each other and based on their magnetic moments, the total moment of the alloyed material can have a finite or zero net moment. The particular combination, for which the magnetic moment of the alloy becomes zero, is called magnetic compensation point and the material can behave as an antiferromagnet. However, based on the g-factor of the individual materials, the angular momentum compensation may or may not occur at magnetic compensation point.

Previous theoretical studies predict that high DW speed could be realized in conventional antiferromagnets such as NiO or CoO and CuMnAs [1, 2]. However, it is unclear if the same argument holds for ferrimagnetic systems with unequal sublattices. Particularly, it remains an open question whether the speed advantage associated with the antiferromagnetic ordering would show
up at the angular momentum compensation or the magnetization compensation point. Since our films cover the whole composition range of interest, the current induced domain wall dynamics revealed in our experiments can help to clarify this issue.

Transition metals- rare earth (TM-RE) metal alloys form ferrimagnetic materials where the spins from TM and RE align antiparallel to each other. We choose Co_{1-x}Tb_{x} as the example material to examine the spin dynamics in the ferrimagnetic materials.

3.1 Current-induced domain wall motion: Spin-orbit torque

Recently, a new source of spin transfer torque, spin-orbit interaction, has been identified and provided a more efficient and versatile platform for developing more powerful spintronic devices [3-5]. In this section, we will discuss the current driven domain wall motion induced by spin-orbit torque (SOT) in magnetic nanostructures.

![Figure 3.1 Schematic of spin Hall effect in non-magnetic materials [6].](image)

There are a few sources to generate the SOT. The most well-known is spin Hall effect. Here, we focus on the extrinsic spin Hall effect only. When unpolarized electrons are injected into a non-magnetic material along +x-direction so that the current flows along -x-direction. Then the relativistic effect generates an Oersted field in count-clockwise direction (Figure 3.1). Consequently Zeeman-like effect sets up a preference of scattering of specific spins whose directions are parallel to Oersted field direction, thus generating spin currents along y and z
directions with spin polarizations along $z$ and $y$ directions, respectively. This occurs due to the spin–orbit coupling, an interaction between the electron’s spin with its motion inside a potential. Note that the charge current, spin current and spin polarization directions are perpendicular to each other. No charge current or accumulation is induced along $y$ and $z$-direction because the injected spins are not polarized in non-magnetic material and magnetic scattering is not needed to induce the spin Hall effect [3]. When a spin current source is interfaced with a ferromagnetic layer, the accumulated spins and spin current are injected into the ferromagnetic layer and thus applying a spin-transfer torque on the moment, which is the SOT.

The damping-like spin Hall torque rotates the moment of DW ($M$) magnetization towards the spin polarization of the non-magnetic/ferromagnetic interface, thus DW cannot be moved by spin Hall torque alone. Hence an additional torque is needed to move the DWs.

Since the ferromagnet/heavy metal system is subject to a substantial spin-orbit interaction and broken inversion symmetry with respect to the interface, the Dzyaloshinskii-Moriya interaction (DMI) is inherently involved [7, 8]. DMI exchange energy can be written as, $\varepsilon_{D12} = D \cdot (M_1 \times M_2)$, where $D$ is the DMI antisymmetric exchange coupling and $M_1$ & $M_2$ are the moments of the two domains. DMI exchange energy not only favors Neel type wall against Bloch type wall but set up a chirality of DWs depending on the spin-orbit coupling. DMI in DWs produces a local field ($H_D$), which essentially generates a torque along the out-of-plane direction.

The spin Hall torque and DMI field torque, the combination of these two torques move the DWs along the current direction depending on the spin-orbit interaction.
3.2 Sample fabrication

Pt(3 nm)/Co_{1-x}Tb_{x}(2-3nm)/SiN_{x}(3 nm) thin films are deposited on Si/SiO_{2} (500 nm) substrate at room temperature. The metallic films are deposited by DC magnetron sputtering with base pressure of 3×10^{-9} Torr. The Co_{1-x}Tb_{x} layer is grown by co-sputtering from Co and Tb targets in a confocal geometry. To prepare films with different compositions, the power of Tb source is varied from 20 W – 80 W while that of the Co source is kept fixed at 100 W. A 3-nm SiN_{x} film is deposited as a capping layer with RF sputtering at 150 W power. All the films were deposited at 2 mTorr of Ar atmosphere. The wires and the Hall bar structures were fabricated by single e-beam lithography and ion milling. The devices for magneto-optical Kerr effect (MOKE) measurement are patterned into the shape of micron size wire (width 2-5 μm) connected with large contact pads of 100 μm × 100 μm. All the process temperatures are kept ≤ 110 °C to prevent the diffusion of the Tb into the adjacent layers and to keep the Co_{1-x}Tb_{x} composition unaltered after all the fabrication steps.

PMMA/HSQ bilayer resists are used for the e-beam lithography as described in Section 2.3.1, except the baking temperature of PMMA is 110 °C. Here, we use two different currents and three different doses for patterning the devices. The schematic of the designed wire is shown in Figure 3.2 and the parameters for e-beam exposure are shown in Table 3.1.

Figure 3.2 Schematic of the patterned wire (blue rectangle), connecting regions (green) and the contact pads (purple squares).
Table 3.1 E-beam exposure parameters for different regions of the pattern shown in Figure 3.2.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Wires (blue)</th>
<th>Contact regions (green)</th>
<th>Pads (purple)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Field size</td>
<td>500 μm</td>
<td>500 μm</td>
<td>500 μm</td>
</tr>
<tr>
<td>Number of dots in a field</td>
<td>50000</td>
<td>50000</td>
<td>50000</td>
</tr>
<tr>
<td>Resolution</td>
<td>10 nm</td>
<td>10 nm</td>
<td>10 nm</td>
</tr>
<tr>
<td>Beam current</td>
<td>10 nA</td>
<td>10 nA</td>
<td>30 nA</td>
</tr>
<tr>
<td>Dose time</td>
<td>0.4 μs/dot</td>
<td>0.25 μs/dot</td>
<td>0.1 μs/dot</td>
</tr>
</tbody>
</table>

After exposure, HSQ is developed with salty developer for 20 s, cleaned with DI water for 1 min and dried with N₂. The sample is then transferred to a RIE chamber for O₂ plasma etching of PMMA to create an undercut. Later, we leave the samples in acetone for 30 min to remove the resists. Since the patterns are micron size, acetone works very well for the resists removal.

3.3 Magnetization & angular momentum compensation point

We vary x from 0.17 to 0.45 in a series of samples of Pt/Co₁₋ₓTbx/SiNy. By measuring the samples with vibrating sample magnetometer (VSM), we find that the saturation magnetization of the samples reaches almost to zero while x ≈ 0.33 and the coercive field also increases to > 4000 Oe. Afterwards, with the increase in Tb concentration, the magnetization starts to increase and the coercive field decreases simultaneously. The hysteresis measurement of the samples with different composition of Co₁₋ₓTbx are shown in Figure 3.3.
Figure 3.3 Hysteresis loop measured for Co$_{1-x}$Tb$_x$ thin film series.

Figure 3.4 summarizes the saturation magnetizations and the coercive fields for the thin films.

Figure 3.4 Saturation magnetizations and coercive fields for Co$_{1-x}$Tb$_x$ thin film series
We identified Co$_{1-x}$Tb$_x$ reaches its magnetization compensation point at $x = 0.34$, where $M_s$ is minimum and $H_c$ diverges. Note that the magnetization compensation composition is different from that observed in Ta/Co$_{1-x}$Tb$_x$ samples [9]. The high concentration of Tb may be necessary due to the proximity induced magnetization in the Pt layer. Taking the g-factor of Co (~2.2) [10] and Tb (~1.5) [11, 12], we calculate the angular momentum compensation point occurs at $x = 0.25$.

![Figure 3.5 Schematics of the anomalous Hall measurement set-up.](image)

The deposited films were patterned into micron size wires and Hall bar structures for DW motion measurement and anomalous Hall resistance ($R_{AH}$) characterization, respectively. $R_{AH}$ is measured using Hall bar devices with the width of 4 $\mu$m. A Keithley 2400 source meter is utilized for the quasi-DC measurements. Figure 3.5 shows the schematics of the anomalous Hall measurement set-up.
Figure 3.6 shows the measured anomalous Hall resistance. $R_{AH}$ changes sign between $\text{Co}_{0.67}\text{Tb}_{0.33}$ and $\text{Co}_{0.64}\text{Tb}_{0.36}$ (Fig. 1c), which is consistent with a transition from being Co-dominated to being Tb-dominated in magnetic moment [9, 13]. The coercive fields of the patterned structures differ from that of the continuous films due to domain nucleation and pinning processes at wire edges.
Note that the sample is named Co-dominated or Tb-dominated based on the parallel alignment of the materials' spins with the applied magnetic field. However, irrespective of the spin alignment, electrons of Co always responsible for transport since only Co has density of states at the Fermi level.

3.4 DW motion in $\text{Co}_{1-x}\text{Tb}_x$

Figure 3.7 (a) Electrical set-up for the domain wall motion measurement. The yellow and the green regions represent $\downarrow$ and $\uparrow$ domains in the MOKE microscope image of 4-μm wide $\text{Co}_{0.65}\text{Tb}_{0.35}$ wire. (b) Domain wall motion in $\text{Co}_{0.65}\text{Tb}_{0.35}$ wire with consecutive current pulses. Blue and red dotted lines show the initial positions of $\uparrow\uparrow$ and $\downarrow\downarrow$ domain walls in the top MOKE image, respectively.

Figure 3.7a shows the schematic of the set-up for studying DW motion in 2-5 μm wide $\text{Co}_{1-x}\text{Tb}_x$ magnetic wires. All the velocity measurements are done at room temperature. For DW velocity measurement, the fabricated devices are bonded onto a radio frequency chip carrier with the cut-off frequency of $\sim$5 GHz. An Agilent 8114A pulse generator is employed to provide the 20-ns current pulses. The MOKE images are captured with a custom-built set-up equipped with in-plane and out-of-plane magnets.

First, a large external magnetic field along the out-of-plane $z$ direction ($H_z$) was applied to saturate the magnetization. Next, a 1−100 ms duration magnetic field pulse in the opposite direction was
applied to nucleate and initiate DW propagation from the large contact pad region. MOKE microscopy was utilized to track the position of the DWs. By sweeping \( H_z \) on a series of samples, we verified that the yellow and green regions in our MOKE image represent domains where the Co sublattice points along the \(-z\) and \(+z\) direction, respectively, for all chemical compositions studied. This is consistent with the observations that the TM sublattice dominates the Kerr signal for TM-RE alloys in the visible light regime [14, 15]. Figure 3.8 shows that the Kerr rotation angle decreases with the increase in Tb concentrations but does not change sign within the concentrations of interest.

For convenience, we will label the two different domains as \( \downarrow \) and \( \uparrow \) domains in the following discussion, where \( \downarrow \) and \( \uparrow \) denote the orientations of the Co sublattice. After the initial nucleation of DWs, electrical current pulses of 20-ns duration were then applied to the wires to move the DW. The initial and the final positions of the DWs were measured with MOKE microscopy and the velocity was calculated from the DW displacement and the total pulse length. Figure 3.7b gives an
example of the positions of DWs after multiple current pulses of the same width. Samples with different channel widths (2 μm - 5 μm) were tested, but no dependence of velocity on sample width was observed as shown in Figure 3.9. In our experiment, both ↑↓ and ↓↑ DWs move along the direction of the charge current (Figure 3.10), similar to the direction of DW motion observed previously in Pt/ferromagnet systems [16, 17], which supports the essential role of SOT.

Figure 3.9 Wire width dependence of domain wall velocity of Pt/Co$_{1.4}$Tb$_{0.6}$. Domain wall velocity as a function of current density for Pt/Co$_{0.79}$Tb$_{0.21}$ wires with different widths.
Figure 3.10 Domain wall velocity as a function of current density for (from bottom to top panel) $\text{Pt/Co}_{0.59}\text{Tb}_{0.41}$, $\text{Pt/Co}_{0.67}\text{Tb}_{0.33}$ and $\text{Pt/Co}_{0.74}\text{Tb}_{0.26}$. 
The DW velocity as a function of the applied current density in a series of Pt/Co$_{1-x}$Tb$_x$ wires ($x = 0.17 - 0.41$) is summarized in Figure 3.11. To exclude the contributions from differences in threshold current densities between samples, we focus on the regions where the velocity and the current density roughly satisfy a linear relationship. The DW mobility of all the samples, defined as the ratio between the velocity and the current density, is determined by fitting the slopes of the linear regions in Figure 3.11. The results are summarized in Figure 3.12 and show that the DW mobility varies by more than an order of magnitude depending on the chemical composition.
Starting from the Tb-dominant samples, the mobility increases with Co concentration and reaches a maximum around $x \approx 0.26$, which is very close to the estimated angular momentum compensation point. We note that the fact that DW attains its maximum speed when the net angular momentum rather than the magnetization reaches zero is also consistent with recent study on field-induced DW motion [18], despite the different driving mechanisms.

The DW mobility [$\sim 5 \times 10^{-10} \text{m}^3/(\text{A}\cdot\text{s})$] obtained in our compensated CoTb sample is much higher than what was observed previously with ferromagnetic layers (e.g., CoFeB [19, 20] and Co/Ni/Co[16]) where the mobility is $0.2 \times 10^{-10} \text{m}^3/(\text{A}\cdot\text{s}) - 1 \times 10^{-10} \text{m}^3/(\text{A}\cdot\text{s})$, and is comparable to the values found in synthetic antiferromagnet multilayers [21]. Compared with these previous experiments, the current densities used in our experiment are relatively low ($< 5 \times 10^{11} \text{A/m}^2$ vs $1-5 \times 10^{12} \text{A/m}^2$). To achieve even higher absolute values of DW velocity, larger current densities
are required. We found that above a certain current density (defined as the maximum current density), nucleation of new domains starts to occur, which puts an upper limit on the applicable current. This is similar to a previous observation in the Ta/CoFeB/MgO system, where the breakdown of DW motion was attributed to current-induced weakening of the perpendicular anisotropy[19]. The decrease in anisotropy was observed in the temperature-dependent vibrating sample magnetometry as shown in Figure 3.13. Note that the heating effect always accompanies applied current. Temperature change can influence the compensation points of magnetization and angular momentum. In Figure 3.13, we observe that with the increase of temperature, the coercive field of the film significantly decreases while the net saturation magnetization remains about same. No significant magnetization change was observed when the coercive field reduces to almost zero. Since our films always maintain PMA during the measurement, we can expect similar or smaller variation in magnetic moment in our current induced domain wall motion measurement. In contrast, the neighboring composition film with lower coercive field (i.e. Co$_{0.76}$Tb$_{0.24}$) has much larger difference in magnetization (~64%). Therefore, we can confirm that while current pulse induced heating will cause drift of the angular momentum compensation, it is not large enough to completely shift the angular momentum compensation point to neighboring compositions.

The maximum applicable current density and the threshold current density (defined as the smallest current density that moves the DW) are summarized for Co$_{1-x}$Tb$_x$ wires with different compositions in Figure 3.14. We noticed that in addition to having a high DW mobility, the samples with compositions close to the angular momentum compensation have the further advantage of a larger dynamic range of applicable current densities.
Figure 3.13 Temperature dependent magnetic properties of Pt/Co$_{0.79}$Tb$_{0.21}$. (a) Out-of-plane hysteresis loops of Pt/Co$_{0.79}$Tb$_{0.21}$ films measured at different temperatures. (b) Summary of coercive fields and the remanence magnetization in Pt/Co$_{0.79}$Tb$_{0.21}$ film with temperature.

Figure 3.14 Threshold and maximum applicable current densities of PtCo$_{1.4}$Tb$_{x}$ with different compositions.
3.5 Modeling of current induced domain wall motion in ferrimagnet

To answer the question how the DW velocity changes as a function of the net angular momentum in a ferrimagnetic system, we model the domain wall motion for magnetic thin films with perpendicular anisotropy and interfacial DMI. As is discussed in the main text, since the magnetic dynamics of ferrimagnet can be described by the modified Landau–Lifshitz–Gilbert equation with the effective damping and effective gyromagnetic ratio, the micromagnetic energy term of DW can be written out correspondingly by replacing the regular $\alpha$ and $\gamma$. This further leads to the domain wall equations under $q$-$\Phi$ model [22, 23]:

$$\dot{\Phi} + \alpha_{\text{eff}} \frac{\dot{q}}{\Delta} = \gamma_{\text{eff}} H_a,$$

$$\frac{\dot{q}}{\Delta} - \alpha_{\text{eff}} \Phi = \gamma_{\text{eff}} \left(-H_K \sin \Phi \cos \Phi + H_D \sin \Phi \right).$$

Here, $H_a$ is the applied field in the perpendicular direction which drives the domain wall motion. $q$ and $\Phi$ represent the domain wall position and the domain wall magnetic moment angle. $\Delta$ is the domain wall width. $H_D$ is the DMI effective field within the domain wall, with $H_D = \frac{nD}{2\mu_0 M_{\text{eff}} \Delta}$, where $D$ is the DMI coefficient. $H_K$ is the in-plane magneto-static anisotropy field of the domain wall, which favors the Bloch wall configuration in the absence of other interactions. $\mu_0$ and $M_{\text{eff}}$ are the vacuum permeability and net magnetization. In ferrimagnet, $\alpha_{\text{eff}}$, $\gamma_{\text{eff}}$ and $M_{\text{eff}}$ result from competitions between the two sublattices that are antiferromagnetically coupled. Specifically, $M_{\text{eff}} = M_1 - M_2$, $\gamma_{\text{eff}} = (M_1 - M_2)/(S_1 - S_2)$, and $\alpha_{\text{eff}} = (\alpha_1 S_1 + \alpha_2 S_2)/(S_1 - S_2)$, where $M_{1,2}$, $S_{1,2}$ and $\alpha_{1,2}$ are the magnetization, angular moment per unit volume and damping coefficient of the two sublattices [24, 25]. $M_{1,2}$ and $S_{1,2}$ are connected through the relationship of $M_{1,2} = g_{1,2} S_{1,2} \frac{\mu_B}{h}$, where $g_{1,2}$ denotes the $g$ factors.
For current induced domain wall motion, the spin orbit torque plays the role as an effective perpendicular field within the domain wall: $H_a = H_{ST} \cos \Phi$, where $H_{ST} = \frac{\pi \hbar \theta_H j}{4e \mu_0 M_{eff} t}$ is due to the damping-like spin orbit torque with $\theta_H$, $t$ and $j$ representing the spin Hall angle, magnetic film thickness and applied current density [22]. The factor of $\cos \Phi$ in $H_a$ comes from the expression of spin orbit torque of $\tau_{ST} \propto m \times (\sigma \times m)$. This self-limiting factor decreases the effective field experienced by the domain wall when $\Phi$ is rotated towards $\pi/2$, alleviating the Walker breakdown under large driving current. Following the derivation of ref. [22], one can reach the current induced domain wall velocity from equation (1) and (2):

$$v = \frac{v_S}{\sqrt{1 + (j_S/j)^2}},$$

with $v_S$ and $j_S$ representing the saturation velocity and saturation current density: $j_S = 2 \alpha_{eff} t e D / (\hbar \theta_H \Delta)$ and $v_S = \gamma_{eff} \Delta H_D$.

Two extreme cases can be considered using the expressions above: in the small current limit ($j \ll j_S$), $v \approx (v_S/j_S) \cdot j = j \cdot \frac{\pi \hbar \theta_H \Delta}{2 \mu_0 t \alpha (a_1 S_1 + a_2 S_2)}$, which is independent of the net angular momentum. Therefore, the ratio of $v/j$ remains constant, no matter whether the magnet is in the ferromagnetic or antiferromagnetic state. In the large current regime ($j \gg j_S$), $v \approx v_S \propto \frac{\gamma_{eff}}{M_{eff}} = \frac{1}{S_1 - S_2}$. The maximum velocity that a domain wall can reach is thus dominated by the net angular momentum.

In compensated ferrimagnet, $v_S$ diverges when $S_1 - S_2 \rightarrow 0$, and the current induced domain wall velocity does not exhibit breakdown or saturation under large driving current. For intermediate current densities, we can calculate $v$ by substituting the expressions of $\alpha_{eff}$ and $\gamma_{eff}$ into the formulas above. Utilizing material parameters measured in our experiment and reported in literature [$\Delta = 10$ nm, $t = 2$ nm, $\theta_H (Pt) = 0.02$, $D = 0.5$ mJ/m$^2$, $\alpha_{1,2} = 0.1$, $g_{Co} = 2.2$, $g_{Tb} = 1.5$, $M_{Co} = 1.4 \times 10^6 A/m$, $\frac{S_{Co}}{S_{Tb}} = 0.35$ (calculated from the measured magnetic moment compensation point)], we plot the relationship between $v$ and $j$ for ferrimagnets with different net momentum in
Figure 3.15. It can be seen that a ferrimagnet with compensated angular moment exhibits advantages in velocity (or mobility) at large and intermediate current densities due to the unsaturated maximum velocity. This is consistent with our experimental observations.

![Graph showing calculated current-induced domain wall velocity for a series of ferrimagnetic samples with different net angular momentum, $S_{\text{eff}}$.](image)

Figure 3.15 Calculated current-induced domain wall velocity for a series of ferrimagnetic samples with different net angular momentum, $S_{\text{eff}}$.

A recent study reported linear increase in DW velocity for a ferrimagnetic material at the compensation point [26].
3.6 Domain wall chirality in ferrimagnetic materials

DMI plays an important role in stabilizing the DW chirality and alleviating the velocity reduction caused by Walker breakdown. In a ferromagnet, the effective field from DMI directly determines the highest DW velocity that can be reached. For a compensated ferrimagnet, as discussed above, the DW velocity is no longer restrained by $H_D$. However, a non-zero DMI is still critical to ensure that a Néel type of DW is favorable, for which the spin orbit torque has the highest efficiency as shown in Section 3.5. So far, little is known about the DMI at the interface between heavy metals and ferrimagnetic alloys. In particular, it is not clear how the DW chirality varies when the net magnetization or net angular momentum goes through zero as the composition varies. To characterize DMI in ferrimagnetic $\text{Co}_{1-x}\text{Tb}_x$, we measured current-induced DW velocities as a function of in-plane field ($H_x$) along the wire direction. The results from a $\text{Co}_{0.79}\text{Tb}_{0.21}$ sample are illustrated in Figure 3.16.

![Figure 3.16: Domain wall velocity as a function of current density at different longitudinal fields along the length of the Pt/Co$_{0.79}$Tb$_{0.21}$ sample for (a) $\uparrow\uparrow$ and (b) $\uparrow\downarrow$ domain walls.](image)

Figure 3.16 Domain wall velocity as a function of current density at different longitudinal fields along the length of the Pt/Co$_{0.79}$Tb$_{0.21}$ sample for (a) $\uparrow\uparrow$ and (b) $\uparrow\downarrow$ domain walls.
Under positive (negative) $H_x$, the $\downarrow\uparrow$ DW in $\text{Co}_{0.79}\text{Tb}_{0.21}$ moves faster (slower) compared with the zero field case. The trend is opposite for $\uparrow\downarrow$ DWs, and the DW velocities even change direction at $H_x = \pm 1000$ Oe. The fact that the motion for one type of DW is enhanced while the other is suppressed is consistent with the Néel wall characteristics, where the applied $H_x$ strengthens (or weakens) the effective DMI field as shown in Figure 3.17. This is in contrast with other DW configurations (e.g., a Bloch wall), where a symmetric variation of the DW velocity under $H_x$ is expected. In Figure 3.17, Blue and green arrows represent the magnetizations from Co and Tb sublattices, respectively. The effective fields from Slonczewski-like torque ($H_{\text{SL}}$) on Co and Tb sublattices are shown by yellow and brown arrows, respectively. It can be seen that $H_{\text{SL}}$ on the two sublattices work constructively to move domain walls. The domain wall motion direction remains the same in both samples. The black $\downarrow$ and $\uparrow$ arrows show the domain orientation as detected in the MOKE measurement. The length of the blue and green arrows below the domain wall region reflects the influence of external field $H_x$ on domain wall chirality.
Figure 3.18 Domain wall velocity as a function of in-plane field for samples of (a) Pt/Co$_{0.75}$Tb$_{0.25}$, (b) Pt/Co$_{0.67}$Tb$_{0.33}$ and, (c) Pt/Co$_{0.59}$Tb$_{0.41}$ wires, respectively. Red squares (negative current) & red circles (positive current) represent $\uparrow\downarrow$ domain walls and blue triangles (negative current) & blue stars (positive current) represent $\uparrow\downarrow$ domain walls, respectively. Red solid lines and blue dashed lines are the linear fit of the experimental data for $\uparrow\downarrow$ and $\uparrow\downarrow$ domain walls.

To answer the question of whether the DW changes its chirality at the compensation points, we plot the dependence of DW velocity as a function of $H_x$ in Figure 3.18 for three different Co$_{1-x}$Tb$_x$ samples. Since the angular momentum and magnetization compensation points are at $x = 0.25$ and 0.34 respectively, the samples with $x = 0.21$, 0.33, and 0.41 in Figure 3.18 represent three different cases: Co-dominant in both angular momentum and magnetization, Co-dominant in magnetization and Tb-dominant in angular momentum, and Tb-dominant in both angular momentum and magnetization, respectively. First, we find that there is no qualitative change in the DW motion characteristics across the angular momentum compensation point (Figure 3.18a and b). Under an $H_x$ field, the Co$_{0.67}$Tb$_{0.33}$ sample exhibits similar behavior to the previously discussed Co$_{0.70}$Tb$_{0.21}$ sample, where the velocity of $\downarrow\uparrow$ ($\uparrow\downarrow$) DWs increases (decreases) under small positive $H_x$. However, across the magnetization compensation point, the opposite trend was seen (Figure 3.18c), where the velocity of the $\downarrow\uparrow$ ($\uparrow\downarrow$) DWs decreases (increases) under the same positive $H_x$ field. The sign reversal in the $v \text{ vs } H_x$ slopes across the magnetization compensation point can be explained by the schematic DW structures shown in Figure 3.17 and Figure 3.19.
A positive $H_x$ field will stabilize the $\uparrow \downarrow$ DW in magnetically Co-dominant samples, while it will destabilize the $\uparrow \downarrow$ DW in Tb-dominant samples. Therefore, the sign reversal reflects that the left-handedness is maintained throughout all our Pt/Co$_{1-x}$Tb$_x$ samples, suggesting that the DMI is correlated with the spin orientations of specific sub-lattices rather than the net magnetization. The in-plane magnetic fields which overcome DMI and result in zero domain wall velocity for the above three compositions are summarized in Figure 3.20. It is noted that $H_{DMI}$ does not simply scale following the expected relationship of $D/M_{eff}t\mu_0\Delta$, where $D$, $t$, $\mu_0$ and $\Delta$ representing the interfacial DMI energy density, film thickness, vacuum permeability and DW width [22]. Instead, samples with higher Tb concentration tend to have larger $H_{DMI}$, which is likely due to the strong spin orbit coupling associated with rare earth element. We note that besides allowing for fast DW movement, the strong DMI and robust chirality exhibited in our compensated ferrimagnet provide the possibility of engineering skyrmion structures with zero total angular momentum. Because of the cancelation of the side deflections from the skyrmion Hall effect of two sublattices, these compensated skyrmions are expected to have greatly enhanced mobility [27, 28].
To summarize this chapter, we experimentally investigated the fast domain wall dynamics in \( \text{Co}_{1-x}\text{Tb}_x \) ferrimagnetic samples. We found that the domain wall mobility reaches a maximum in samples with compensated angular momentum and it is higher than those in the ferromagnetic electrodes. The high domain wall velocity in a compensated ferrimagnet is consistent with our theoretical modelling, where it is shown that the absence of velocity saturation ensures a high mobility. By measuring the influence of in-plane field on the domain wall velocity, we further demonstrated that the domain walls have chiral internal structures which are stabilized by the Dzyaloshinskii-Moriya interaction and the same chirality is maintained across the compensation points. Our study on current-induced domain wall motion in ferrimagnets opens the opportunity to electrically probe the fast domain wall dynamics in angular-momentum compensated systems. The low magnetic moment, large electrical and optical response, as well as the possibility of reaching high speed dynamics makes it highly attractive to employ ferrimagnets for spintronic applications.
Reference


All transistors that operate in thermodynamic equilibrium must have a potential energy difference between their ON and OFF states. For CMOS transistors, this energy difference is controlled by the supply voltage $V$ at the gate. Figure 4.1 shows schematic of a field-effect transistor, comprising of three terminals: source, drain, and gate.

![Figure 4.1 Schematics of a field-effect transistor at (a) OFF and (b) ON states.](image)

As voltage $V_{GS}$ increases between the source and the gate, at a threshold voltage electrons start to flow in the channel between the source and the drain, and the transistor is switched on. The energy difference between the ON and OFF states is $\Delta E = \frac{1}{2} qV$, where $q$ is the electron charge and $V$ is the supply voltage. The current when the device is in the off state is limited by the probability of thermal excitation from OFF to ON:

$$\frac{I_{ON}}{I_{OFF}} = e^{\frac{\Delta E}{kT}} \quad 4.1$$

Even when the device is nominally OFF, there is still thermal leakage. To ensure minimum static power consumption, generally $I_{ON}/I_{OFF} = 10^6$, which limits $V_{GS}$ to about 0.35 V.
To stay above the thermal limit, the threshold energy to switch a transistor is limited to about $E_{th} = 60\ kT$. When the device is ON, if the number of electrons in the channel, $N_e = 200$, then the power delay product, $PDP_{CMOS} = N_e\ E_{th} \sim 1.2 \times 10^4\ kT$. But, if the electrons in the transistor behaved collectively, such that the device could only switch from OFF to ON when all of the electrons switched together into the channel, then $\Delta E = \frac{1}{2}QV$, where the total charge in the transistor $Q >> q$. The fundamental limit in the OFF state current is

$$I_{ON} = I_{OFF}\ e^{\frac{qV}{kT}}$$ \tag{4.2}$$

This has motivated researchers to investigate new types of logic that use collective phenomena to enable switching closer to the Shannon-von Neumann-Landauer limit. The focus of this chapter is one of such device, switches based on nanomagnetism. In a ferromagnetic material, exchange interaction and anisotropy couples the magnetic moments in a collective direction. For example, for a ferromagnetic material, it is not possible to modulate the spin of an individual electron (Figure 4.2).

![Single spin flip is NOT allowed in a ferromagnetic material.](image_url)
Figure 4.3 shows micromagnetic simulation images of magnetization vector in a 15 nm wide IMA Co wire. This wire has a magnetic domain wall, which is a transition region between two domains of different magnetic orientation. If the domain wall starts out sitting in the energy minimum (1), an energy $\Delta E$ can collectively move the magnetic moments of the domain wall to the next energy minimum (2). The energy to switch a nanomagnet [1]:

$$PDP_{\text{mag}} = \frac{1}{2} \mu_0 \mu_B N_S H_k,$$

where, $\mu_0$ is the permeability of free space, $\mu_B$ is the Bohr magneton, $N_S$ is the number of spins, and $H_k$ is the anisotropy field, i.e. the field required to saturate the magnetization in the hard axis ($y$ axis of Fig. 1.5). For cobalt, $H_k \approx 0.8-1.5$ T. If we assume $N_S \approx 1 \times 10^4$, we get $PDP_{\text{mag}} \approx 60$ kT $<< PDP_{\text{CMOS}}$. Thus, nanomagnetism is a promising materials class to explore for more energy-efficient computing. Qualitatively, there is no “thermal leakage” limiting the voltage.

Moreover, charge-based transistors suffer from further unwanted leakage due to quantum tunneling across the gate insulator depicted as “oxide” in Figure 4.1. While solutions such as high-$k$
dielectrics help alleviate this leakage, it is still present and becomes more pronounced as the
insulator dimensions are scaled down. Magnetic-based solutions can utilize this tunneling to detect
the magnetization states, thus utilizing the wasted energy.

Magnetic materials are also non-volatile: they maintain their state even when no energy is supplied.
This could allow memory and logic to be performed with the same transistors. One of the biggest
delays in modern CPUs is the time it takes to access memory, which is located on a different part
of the chip than logic. Thus, being able to perform memory and logic on the same part of the chip
will improve computing speed. We will discuss more on this in Chapter 5.

The various magnetic device concepts show many exciting opportunities for logic using magnetic
materials, and each has its advantages which could be implemented for specific applications. Our
motivation for designing DW-Logic was to try to build a magnetic-based logic gate that satisfies
as many required and desired characteristics for beyond-CMOS as possible.

The following are the main requirements for future logic devices:

1. Nonlinearity: requires distinct ON and OFF states.

2. Gain: one device needs to be able to drive more than one output devices.

3. Cascadability: we want a single element that can be concatenated to build up circuits.

4. Feedback prevention: unidirectional propagation for the information is necessary to prevent
feedback errors.


There are also a number of non-essential but desired characteristics for logic devices:

1. Scalability: decrease in device size should reduce the switching energy.
2. Room temperature operation.

3. Compatibility with CMOS circuits and processing.

4. Switching energy competitive or better than CMOS.

In this chapter, we will experimentally show that DW-Logic can satisfy all of the required characteristics. We will also experimentally show desired characteristics 1 and 2 in this chapter. As DW-Logic technology is similar to embedded magnetic random access memories (e-MRAM), it can easily be integrated in CMOS foundries. At the end of this chapter, we discuss potential direction for reducing the switching energies to make it comparable to CMOS devices.
4.1 Current induced domain wall motion: Spin transfer torque

Information is stored in the position of a magnetic DW in a short, narrow ferromagnetic wire for the DW-logic device present in this chapter. A DW is a transition region between two magnetic domains. There are different types of DWs depending on the competition between exchange energy and magnetostatic energy to minimize the total energy in the material.

![Diagram of domain wall motion](image)

*Figure 4.4 Current induced domain wall motion. Conduction electrons are labeled by the red arrow, local magnetic moments by the black arrows. The domain wall region is shown in yellow [2].*

In DW-Logic, information is written by moving the DW with electrical current, a phenomenon known as current-induced domain wall motion. Figure 4.4a shows a schematics of a ferromagnetic wire with aligned magnetic moments (black arrows). The DW is shown in yellow. If a voltage is applied across the magnetic wire, conduction electrons (red arrow) will start to flow. Due to interactions between the conduction band and the valence band of the atoms, the conduction electrons become partially spin polarized to match the local magnetic moments. When the conduction electrons encounter a DW, the electron spin orientation changes to match the local...
changes in the magnetic moment. This process produces a torque on the DW itself, which translates it along the wire, shown in Figure 4.4b.

4.2 Magnetic tunnel junctions

A magnetic tunnel junction (MTJ) provides a way to translate between magnetic information and electrical information. It consists of a thin ($d < 4$ nm) insulating tunnel barrier between two ferromagnetic electrodes, as shown in Figure 4.5. The tunnel barrier is shown in yellow, and the magnetization of the electrodes is designated by white arrows. The magnetization can be either in the plane of the ferromagnet or perpendicular. If a voltage $V$ is applied across the electrodes, electrons will tunnel across the insulator. Tunneling in general preserves spin. When both electrodes have the same magnetization direction $\mathbf{M}$, there is more density of states (DOS) available for the electrons on the other side of the barrier; when the electrodes have opposite $\mathbf{M}$, there are less states available to tunnel to. Therefore, a modulation in current is high / low when $\mathbf{M}$ is parallel / antiparallel.

Tunneling can be understood by plotting the energy levels $E$ vs. density of states (DOS) when a voltage is applied, shown in Figure 4.5. The voltage creates an energy difference $eV$ between

---

Figure 4.5 Two configurations of magnetic tunnel junctions. (a) Parallel or low resistance state and (b) Antiparallel or high resistance state [2].
ferromagnet 1 (FM1) and ferromagnet 2 (FM2), where $e$ is the electron charge. If we treat the ferromagnets using a rigid band model, we can separate DOS for each spin type, as shown by the blue and red bands. The amount of electrons of each spin type depends on DOS at and below the Fermi level $E_F$. In Figure 4.5a, there are more electrons with down spin on both sides, and thus the majority tunnel current $I_{maj}$ is greater than the minority current $I_{min}$ and the resistance $R_P$ is low. In Figure 4.5b, both $I_{maj}$ and $I_{min}$ are small and the resistance $R_{AP}$ is high.

MTJs are characterized by two parameters, the resistance-area (RA) product when in the parallel state and tunnel magnetoresistance (TMR). The RA product is defined as $RA = R_p \times A$, where $A$ is the area of the junction. TMR is defined as [3]

$$TMR = \frac{R_{AP} - R_P}{R_P} \times 100\%$$ \hfill (4.4)

So far, the highest TMR observed using an MgO tunnel barrier is 604\% [4]. However, this high TMR has rarely been achieved to date, and TMR $= 100\% - 300\%$ is more common.

4.3 Proposal of logic device using magnetic tunnel junction and magnetic domain wall

In 2012, logic gates have been proposed combining the magnetic tunnel junctions and the current-induced magnetic domain wall motion [5]. Binary logic gates requires well separated ON ('1') and OFF ('0') states.
Figure 4.6 (a) ON and (b) OFF states of the proposed magnetic logic devices [6].

Figure 4.6 shows the ON and the OFF states of the proposed three-terminal device depending on the position of the magnetic domain wall. The left and the right terminals are the “Input” and “GND”/“clock” terminals, respectively. The magnetic tunnel junction in the middle is the “Output” terminal which can electrically read the spin orientation of the wires underneath it. The MTJ is placed close to the “Input” terminal to ensure the RESET of the device while driving other devices.

The wire length $L$ is greater than the width $w$ and thickness $t$, which confirms a transverse Néel DW in the magnetic wire [7]. The magnetization direction $M$ of the wire is confined in the $(x, y)$ plane, allowing two possible magnetization states for the wire region under the magnetic tunnel junction, depending on the DW position. To ensure that only one DW is present, antiferromagnetic contacts (i.e., IrMn) can be placed on both ends of the wire, creating exchange bias that confirms opposite $M$ at the two ends [8].
The gate operation includes a write step and a read/reset step. During writing, current injected into wires at the “Input(s)” contact is spin-polarized and translates the DW along $x$, switching the gate from ON (Fig. 4.1a, Fig. 4.2) to OFF (Fig. 4.1b). The DW is translated by spin transfer torque given by the Landau–Lifshitz–Gilbert equation [9]. The magnetization of the DW cant in $z$ while it moves, but oscillations in velocity are avoided by operating well below Walker breakdown [10]. For current-driven motion, the Walker breakdown transition depends on $(\alpha - \beta)$, where $\alpha$ is the adiabatic damping parameter and $\beta$ is the nonadiabatic parameter.

The current-induced DW motion can exhibit a threshold behavior, where the DW will only move when the applied current exceeds a threshold value $I_{th}$ [11]. When $\beta = 0$, there is an intrinsic threshold, but for finite $\beta$ the threshold is determined by extrinsic pinning sites such as line edge roughness [12] or local magnetic fields. We discussed the effect of line edge roughness on DW motion in Chapter 2. The nonlinear threshold behavior of DWs allows the gate to have distinct OFF and ON currents.

The states of the gate are read using a magnetic tunnel junction (Figure 4.6). A synthetic antiferromagnetic (SAF) stack minimizes stray fields that could impede DW motion. To sense the magnetization of the soft layer directly beneath the MTJ, a voltage $V_{CLK}$ is applied to the “Clock” terminal. The output current $I_{OUT}$ through the MTJ can be either high ($I_{ON}$) or low ($I_{OFF}$) depending on the tunnel magnetoresistance as defined in Section 4.2. $R_P$ increases with increasing barrier thickness $d$. Tunnel junctions even smaller than 10 nm diameter is possible [13]. The higher the TMR, the more robust the system is against variations in $I_{th}$, since high TMR creates a larger difference between $I_{ON}$ and $I_{OFF}$.
If instead of a single input terminal, the device has two input terminals with currents $I_A$, $I_B$ and the Clock terminal is grounded, the device behaves as a logical two-input NAND gate. Provided that the input impedance is sufficiently low, only when $I_A + I_B \geq I_{Th}$ (where both $I_A, I_B < I_{Th}$), the device switch from ON to OFF state due to the domain wall motion. Thus, a single device can act as a universal NAND gate, replacing four CMOS transistors [5]. Other standard logic operations can also be done using a single gate, as shown in Figure 4.7. If $I_A, I_B \geq I_{Th}$, the device performs a NOR operation. One way to accomplish this is to design the width of the wire half compared to the NAND gate, requiring less energy to push the DW. By reversing the magnetization of the pinned ferromagnetic layer of the MTJ in the initial state, the gate can perform AND/OR operations.

![Figure 4.7 Initial configuration of (a) NAND, (b) NOR and, (c) AND gates [2].](image)

In Figure 4.8c, the comparison of power-delay products (PDP) and energy-delay products (EDP) between 15 nm linewidth DW-Logic ($R_P = 10$ kΩ) and 40 nm CMOS is shown using transient model. The PDP is the energy required to switch a single gate and is expressed in $kT$ at 300 K. The detail of the simulation will be found in [2].

The CMOS simulation does not include energy dissipation in the clock, like the magnetic logic simulations, and ignores interconnect resistance [2]. The IMA magnetic logic PDP is competitive...
with CMOS but with longer delays, calculated for a voltage range of 0.3–0.1 V. PMA magnetic logic is about 100x more energy efficient but with even longer delays, for the range 10–4 mV. The EDP (dotted lines) of CMOS, however, is far superior to the simulated IMA magnetic logic and superior to PMA magnetic logic. While a reduction in gate length will reduce the delay of CMOS further, leakage currents are expected to affect the PDP. Thus, it has been concluded that PMA magnetic logic will perform better than IMA, and is especially attractive for energy-efficient applications where the merit parameter is PDP not EDP [2].

Figure 4.8 (a) IMA and (b) PMA logic devices. (c) Power-delay product versus delay, shown for IMA materials (blue), PMA materials (red), and 40 nm CMOS (green). Dotted lines are constant EDP. The desired corner is the bottom left. (d) Gate scaling behavior, showing the power-delay product scales vs. wire width, for IMA at 0.1 V (blue) and PMA at both 0.01 V and 0.004 V (red) [5].

Figure 4.8(d) shows that with the decrease in wire width the PDP decreases for both IMA and PMA materials. This is because the DW size scales with the wire width and smaller the DW, the less energy it takes to move it across the device [2].
4.4 Fabrication of prototype magnetic logic devices

The fabrication of the prototype device start with the deposition of magnetic thin films with MTJ stack. The thin film stack used in this experiment are obtained from National Institute of Standards and Technology. The stack consists of Si (substrate)/ SiO₂ (500 nm) / Ta (3 nm) / Co₄₀Fe₄₀B₂₀ (4 nm) / MgO (1 nm) / Co₄₀Fe₄₀B₂₀ (2.5 nm) / Ru (0.8 nm) / Co₄₀Fe₄₀B₂₀ (2.5 nm) / IrMn (10 nm) / Ta (3 nm) / Ru (7 nm) as shown in Figure 4.9a.

The film was post-annealed in-situ at 280 °C for 30 minutes, and ex-situ at 300 °C for 1 hour in a 1 T field. The free layer (i) in Figure 4.9a is for DW motion, and the top two CoFeB layers (ii) form a SAF to reduce the stray field from the tunnel junction to minimize its effect on the DW. The IrMn antiferromagnetic layer pins the SAF through exchange bias to keep the SAF harder than the free layer [14]. The easy axis hysteresis loop is shown in Figure 4.9b and Figure 4.9c. The free layer switches at \( H_{C+} = 7 \) Oe and \( H_{C-} = -20 \) Oe. At high magnetic fields, we observe a gradual increase to the saturation magnetization as the SAF unravels to align with the field [2].

Figure 4.9(a) Thin film stack. Numbers are in units of nm. (i) Free layer. (ii) Synthetic antiferromagnet fixed layer. (b) In-plane hysteresis loop of the stack. (c) Zoom in view of the hysteresis loop [2].
The fabrication steps are shown in Figure 4.10. In Step (i), we spin 4% HSQ at 3.5 k rpm (~ 75 nm thick). The HSQ is soft baked at 110 °C for 60 s. In Step (ii), we pattern the HSQ using the Raith 150 (Elionix F-125 kV) e-beam lithography tool and develop in aqueous CD-26 (Salty developer [15]) for 2 minutes (20 sec). Figure 10.4a shows a topdown scanning electron microscope (SEM) image of MTJ pattern after step (ii). In order to contact the ends of the bottom magnetic wire using the same etching times as the center MTJ, we pattern large 5 μm × 5 μm MTJs on either end that will act as contacts. These MTJs are large enough so that their TMR are insignificant due to the presence of pinholes in MgO.
In Step (iii), we use ion milling to transfer the pattern into the thin film. Since ion milling is not selective, the thickness of HSQ mask is kept thicker than the desired etch depth. Figure 4.11b plots the counts/s vs. time seen on the end-point detector during milling. The end-point detector is essential for stopping the etch within the 1 nm MgO. We can clearly see the Ru, Ta, Mn, and Co peaks in the end-point detector plot.

After patterning the MTJ, we pattern the bottom magnetic wire. The remaining HSQ mask from Step (iii) is left on top of the MTJs. In Step (iv), we again spin 4% HSQ at 5 krpm (~60 nm thick), baked at 110 °C for 60 s, and pattern the magnetic wires using e-beam lithography. In Step (v), we do another ion mill to etch down to the Si substrate.

Next, we need to open vias on top of the junctions to electrically contact the device. In Step (vi), we spin 4% HSQ at 5 krpm and cross-link the HSQ surface to transform it into insulating barriers. We cross-link the HSQ surface by reactive ion etching the sample in O₂ plasma for 3 minutes,
using 150 W power, and 6 mTorr Argon pressure. The base pressure of the chamber is $1 \times 10^{-4}$ Torr.

![Image](image_url)

Figure 4.12 (a) SEM image of a device after Step 8, with PMMA removed. (b) Augers signal showing Ru on the MTJs (blue curve) [2].

In Step (vii), we spin 3% PMMA at 2.5 krpm (~200 nm thick) and soft bake it at 150 °C for 90 s. While PMMA is usually baked at 180 °C, we decrease the baking temperature since the IrMn Néel temperature is about 185 °C. Too high temperatures during patterning may reset the IrMn antiferromagnetic pinning. We use electron-beam lithography to pattern holes in the PMMA. The alignment tolerance < 50 nm in this e-beam step. The PMMA is developed in 1:3 MIBK:IPA solution for 2 minutes. In Step (viii), we conduct a CF$_4$ reactive ion etch at 125 W power and 6 mTorr Argon pressure. This etches the HSQ in the holes to open up the junction tops for electrical connections.
contact. We carefully time the etch so we are at the Ru surface of the MTJs. We then remove the leftover PMMA using an O₂ reactive ion etch for 5 minutes, which also helps cross-link the sidewalls of the exposed HSQ.

Figure 4.12a shows the SEM image of a device after Step (viii), with the PMMA removed. During the CF₄ etch, we monitor the surface of the MTJs using Auger spectroscopy, which detects elements those are present within the first 1-3 nm of the surface. Auger spectroscopy is particularly useful because we can analyze the surface elements at different spots along a feature with the same resolution as a SEM. Figure 4.12b shows the differential Augers signal, electron counts/s vs. electron kinetic energy. The blue curve corresponds to the blue dot location in Figure 4.12a, on top of the MTJs, while the pink curve corresponds to the pink dot, which is on top of the HSQ/PMMA resist. We clearly see a Ruthenium signal on top of the MTJs and no silicon signal, which means we have etched far enough through the HSQ. The signal at the red dot only shows carbon, showing there is still PMMA on the surface. Both curves show a small oxygen signal around 500 eV.

In Step (ix), we spin 3% PMMA at 2.5 krpm, baked at 150 °C, and use electron-beam lithography to pattern electrodes. We develop the PMMA in 1:3 MIBK:IPA solution for 90 seconds. We then e-beam evaporate Ta (5 nm) / Au (125 nm) and later lift-off the metals in NMP at 85 °C for 1 hour. The SEM of a complete prototype device is shown in Figure 4.13.
4.5 Characterization of prototype device

4.5.1 Characterization with magnetic fields

We first characterize the field-driven behavior of a device. We apply magnetic field along $H_i$ directions as shown in Figure 4.13 to saturate the sample and remove it eventually. This nucleates a DW on the left of the magnetic wire, shown by the white arrows in Figure 4.13. The field $H$ is set at a $50^\circ$ angle from the horizontal line to be parallel with the DW. The tunnel junction resistance vs. $H$ and the device configurations at different magnetic fields are shown in Figure 4.14a. The initial device configuration is depicted in schematics (1), with the DW on the left and the MTJ in a parallel, low-resistance state. We start by sweeping the field in $+H$ to 200 Oe. The DW switches past the MTJ at $H_{DW} = 36$ Oe to configuration (2), and eventually the MTJ top also aligns with the field at $H_{MTJ} = 64$ Oe, shown by configuration (3). Then we sweep the field in $-H$. At $H= -36$ Oe we reach configuration (4) with a high resistance, and at $H = -64$ Oe both sides of the MTJ saturate in the negative direction. To operate the device without switching the MTJ top, we need to keep the field below 64 Oe for this particular device. We can see the switching field behavior is not
exactly repeatable in the +H direction between two runs. This is most likely because of the initialization field, which does not always nucleate the DW in the exact same position inside the wire. However, after driving the DW and MTJ in +H, the depinning behavior is repeatable in -H. After the DW depins from its center pinning site, it goes to the same pinning site when +200 Oe is applied.

![Figure 4.14 (a) Resistance of a MTJ vs. magnetic field. The spin orientations of the domains at different resistance states are shown in the insets. (b) Resistance of MTJs with areas.](image)

A useful metric to characterize MTJs after fabrication is to characterize $R_{MTJ}$ (parallel state) scaling with the tunnel junction area $A$. $R_{MTJ}$ is shown for three different junction areas in Figure 4.14b. The blue line is a linear fit: $R_{MTJ} = \frac{27}{A_{MTJ}} - 5.2$. The linear trend shows there is little perimeter-dependent edge degradation during fabrication. The resistance-area product $RA = 27 \Omega \cdot \mu m^2$, and the series resistance $R_S = 5.2 \Omega$. $R_S$ is a measure of the contact resistance. The contact resistance is improved when using wire bonding instead of probes for resistance measurements. It is also important to make sure that the MTJ top surface has direct contact with the Ti/Au electrodes using Auger spectroscopy.
4.5.2 Electrical characterization of individual gates

A single device can be used as a logic gate with multiple inputs if \( I_{IN} \) were a sum of multiple input currents. Figure 4.15 shows an example of a device acting as an inverter, which can be used to perform two-input NAND operations, with parallel MTJ resistance \( R_P = 23.7 \, \Omega \), antiparallel MTJ resistance \( R_{AP} = 25.7 \, \Omega \), wire resistance \( R_w = 1.18 \, k\Omega \) and tunnel magneto-resistance 8.4%.

Initialization with \( H_t \) sets the MTJ initially in a parallel state (‘1’), with the DW on the left. A bias field \( H_B = 30 \, \text{Oe} \) is then applied parallel to the DW. We apply a series of 1-\( \mu \text{s} \) voltage pulses, \( V_{IN} \), increasing in 0.05 V steps, to the IN terminal. Each input pulse is followed by a 100 mV DC voltage applied to the CLK terminal to measure the resistance through the MTJ, \( R_{MTJ} \). Between \( V_{IN} = 3.75 \, V \) and 3.80 V, corresponding to an input current, \( I_I = 3.099 \, mA \pm 0.041 \, mA \) (with range determined by the voltage step) and current density \( J_I = 1.9 \times 10^{12} \, A \, m^{-2} \), the DW is translated across the MTJ, switching the output from \( R_P \) (‘1’) to \( R_{AP} \) (‘0’).

![Figure 4.15 Inverter operation. (a), Transient showing the MTJ resistance and applied voltage pulses between IN and CLK versus time. At 3.80 V, the device switches from low resistance (‘1’) to high resistance (‘0’). (b), Transfer characteristic of \( I_{OUT} \) through the MTJ versus \( I_{IN} \) across the wire. The SEM images show the configuration below \( I_{Th} \) with the DW position approximated by the red dot and \( I_{IN} \) electron flow direction shown by the yellow arrow, and the approximate DW position after \( I_{Th} \). Inset shows simple circuit diagram to represent the device, including the wire resistance and the variable tunnel junction resistance [6].](image-url)
The current is calculated using the circuit in Figure 4.15b, with the wire resistance represented by \( R_W = R_{\text{LEFT}} + R_{\text{RIGHT}} \) and the MTJ represented by a variable resistor \( R_{\text{MTJ}} \). For an isolated device, we define the input current as

\[
I_{\text{IN}} = \frac{V_{\text{IN}}}{R_S + R_{\text{LEFT}} + R_{\text{RIGHT}}}, \tag{4.5}
\]

where, \( R_S \) is the load resistor from the voltage supply. If we read each device using \( V_{\text{OUT}} \), then we define the output current for an isolated device as

\[
I_{\text{OUT}} = \frac{V_{\text{OUT}}}{R_S + R_{\text{RIGHT}} + R_{\text{MTJ}}}. \tag{4.6}
\]

Device stages are pulsed in a sequence, where in each stage a device can also have an input resistor that is tuned to put the input current in the correct range to read the data from the previous stage. Thus, if the input current originates from two logic gates, with output resistances such that the input currents sum in the subsequent gate, then that device switches from 1 to 0 only when the input current exceeds \( I_T \). The resulting transfer characteristic is shown in Figure 4.15b. The change in the MTJ resistance modulates the output current by \( \Delta I_{\text{OUT}} = 8.96 \mu A \), assuming a CLK voltage pulse of 3.80 V and no external load attached to the OUT terminal.
Figure 4.16 Buffer operation. (a), Transient behaviour showing a buffer operation, plotting $R_{MTJ}$ and $V_{IN}$ versus measurement step as we increase the 1-μs voltage pulse amplitude in 0.01 V steps. This device has similar $R_w$ to the previous device, but slightly higher $R_{MTJ}$ and TMR. At 3.97 V, the device switches from a high-resistance output to a low-resistance output. (b), Transfer characteristic for the buffer. inset, Comparison of this transfer characteristic (right black curve) to that of another device (left blue curve) with less well matched $R_w$ and $R_{MTJ}$.

Figure 4.16a shows the same device structure acting as a buffer gate instead. The buffer is shown for a different device with $R_F=46.5$ Ω, $R_{AP}=52.1$ Ω, $R_w=1.10$ kΩ, and $TMR=12\%$. The device is initialized with the same approach as mentioned previously. We program it to act as a buffer rather than an inverter by applying a higher bias field $H_B=48$ Oe, above the field switch of the reference layer of the MTJ but below that of the DW, initializing the MTJ in the antiparallel state ('0'). The DW switches across the MTJ between 3.96 and 3.97 V, or $I_r=3.441$ mA±0.009 mA, $J_r=2.0 \times 10^{12}$ A m$^{-2}$. The output switches from high resistance ('0') to low resistance ('1'). Across multiple devices, the transfer characteristic shows very sharp switching between resistance states, $\Delta V_{IN}<0.01$ V (the limit of the voltage supply). This enables stable '0' and '1' outputs even with $TMR=8$–$20\%$ seen in our devices. $\Delta I_{OUT}/\Delta I_{IN}=3.1$ for this particular device. Figure 4.16b shows $I_{OUT}$ versus $I_{IN}$ for the isolated buffer device with $V_{OUT}=3.97$ V. The change in current between the '0' and '1' output bits is $\Delta I_{OUT}=28.8$ μA assuming no output load.
While $\Delta I_{OUT}=28.8 \mu A$ is an appreciable difference in current for stable 0 and 1 bits, the fractional output current change is $\Delta I/I=(I_P-I_{AP})/I_{AP}=0.3\%$ of ‘0’ output current $I_{AP,OUT}=4.5 \text{ mA}$. In an ideal device, $\Delta I/I$ should be maximized for the best noise margin and potential fanout. Using Equation 4.5 with fixed $V_{OUT}$, and assuming that the gate drives a single subsequent ferromagnetic wire,

$$\frac{I_P}{I_{AP}} = \frac{R_S+2R_{RIGHT}+R_{LEFT}+R_{AP}}{R_S+2R_{RIGHT}+R_{LEFT}+R_P} \quad 4.7$$

If we define the output resistance in the parallel state $R_{OUT}=R_P+R_{RIGHT}$ and the load resistance $R_{LOAD}=R_{LEFT}+R_{RIGHT}+R_S$, then we can define a figure of merit:

$$\frac{\Delta I}{I} = \left( \frac{TMR}{(R_{OUT}+R_{LOAD})/R_P} \right) \quad 4.8$$

Equation 4.8 shows that the highest noise margin and fanout is obtained by maximizing the $TMR$ and matching the MTJ parallel resistance and the resistance of the wire.

Inset of Figure 4.16b compares $I_{OUT}$ versus $I_{IN}$ of the original buffer device (black curve) to another tested device with higher $R_w=2.54 \text{ k}\Omega$, $R_P=12.4 \Omega$, and $TMR=21\%$ (blue curve). Even though the $TMR$ is higher, since $(R_{OUT} + R_{LOAD})/R_P$ is also higher we find lower $\Delta I/I=0.1\%$. For a given wire resistivity and MTJ resistance-area product, we can reduce the ratio between the wire and MTJ resistances by properly choosing the size of the wire and the size of the MTJ. Implementing PMA and spin Hall-induced switching could reduce power consumption and $J_T$ by 100 times [16-19].

4.5.3 Fan-out

Figure 4.17a shows SEM image showing three devices concatenated together, with device 1’s output feeding the input of device 2 and device 3. The dotted boxes identify individual devices. The initial state is shown in the inset of Figure 4.17a. After initialization and $H_B=20 \text{ Oe}$, devices
1 and 2 are in an inverter configuration, and device 3 is a buffer. We then apply 1 µs voltage pulses to the CLK₁ terminal with the CLK₂/CLK₃ terminals maintained at ground and all other terminals floating. Figure 4.17b shows $R_{MTJ}$ after applications of each pulse. The output current from device 1 switches both device 2 and device 3, at 4.5 V±0.3 V and 4.7 V±0.2 V, respectively (range is from three experiment repeats). The resistance of device 1 remains unchanged because its DW is initialized on the left side of its wire, and thus we are able to read device 1 without disturbing its logic state. This demonstrates that one gate can drive two gates, and that we can read the state of device 1 and then use that output current as the input to write devices 2 and 3. We can power more than two gates by further increasing the voltage pulse amplitude or tuning the resistance-area product of the MTJ to output higher current.

Figure 4.17(a) SEM image of a circuit where, one device output is connected to the inputs of two devices. Voltage pulses are applied to CLK₁ with CLK₂ and CLK₃ grounded. Scale bar, 100 µm. Inset shoes the schematics of the initial configurations of the three devices, with the DWs initialized on the left. Red signifies magnetized right and grey signifies magnetized left. (b), Plot of MTJ resistance versus pulsed voltage applied at CLK₁, showing one device can power a switch in two subsequent devices. The error bars represent the average noise fluctuation in $R_{MTJ}$ monitored for each device at each voltage step [6].
4.5.4 Shift oscillators

Figure 4.18 shows a circuit of shift oscillators with three inverters where three devices are concatenated in series. The output of device 3 is fed back into the input of device 1. We initialize all devices in the inverter configuration, as shown in Figure 4.18a. To drive the logic flow, we apply sequential voltage pulses to CLK1, CLK2 and then CLK3. For example, in Step 1, the voltage pulse applied to CLK1 with CLK2 grounded allows us to read device 1 while writing device 2. Since the output of device 1 is high (‘1’), the current is high enough to switch the DW in device 2, changing it from ‘1’ to ‘0’. In Step 2 (Figure 4.18b), we apply a voltage pulse to CLK2 with CLK3 grounded to read device 2 while writing device 3. Since device 2’s output current is now low (‘0’), the DW in device 3 does not switch and it stays as ‘1’.

Figure 4.18c shows an SEM image of a fabricated three inverters circuit, initialized in the inverter configuration with $H_B=30$ Oe. In Figure 4.19d, we measure $R_{MTJ}$ as the information propagates around the circuit. The devices are clocked in sequence by 4.5-V pulses such that at each stage the data token is inverted. The voltage amplitude of 4.5 V is optimized for device 3, such that when device 2 is in the antiparallel state the DW of device 3 does not switch. To see the inverting operation, each resistance is normalized to its own $R_P$. The output resistance at each pulse step oscillates between $R_P$ and $R_{AP}$ as we move around the circuit, showing oscillation between 1 and 0 bits. Operation is stopped after four steps because additional propagation requires a reset step to return all DWs to the left side. We expect that scaled down devices or materials with lower threshold currents should operate without the need of a bias field, allowing the reset to occur during reading.
Figure 4.18 (a) Shift oscillator with three devices connected in series, with the output of device 3 feeding back into the input of device 1. The devices are initialized with their domain walls (DWs) on the left and the tunnel junctions parallel. In the experiment, at Step 1 we apply a voltage pulse at CLK₁ to read the state of device 1 while writing the state of device 2. The voltage pulse is applied between CLKₙ and CLKₙ₊₁. Yellow arrows represent electron flow direction. In this case the DW in device 2 switches. (b) Cartoon of Step 2, where we now apply a voltage pulse at CLK₂ to read the state of device 2 while writing the state of device 3. In this case the DW in device 3 does not switch. In Step 3 and Step 4 this is repeated at CLK₃ and CLK₁, respectively. (c) SEM of three devices in series. $R_{p₁}=23.8 \, \Omega$, $R_{p₂}=19.0 \, \Omega$, and $R_{p₃}=18.4 \, \Omega$. Scale bar, 50 µm. (d) MTJ resistance at each step in the three inverters circuit, showing the oscillation of the DW position at each step between the parallel (low MTJ resistance, bit 1) and antiparallel (high MTJ resistance, bit 0) device states [6].
In the experimental demonstration, \( I_{\text{OUT}} \) does not show the oscillation behavior, as the individual devices do not reset while driving the next devices due to the bias field applied. However, a transient micromagnetic/circuit simulation shows that in the absence of the bias field in the scaled simulation, the logic resets itself during the read operation [5, 6].

4.6 Device-to-device variation

Figure 4.19 shows the threshold voltage, \( V_T \), vs. \( H_B \) for three different devices to assess the variability in \( V_T = I_T(R_W) \) and between devices. The DW depinning voltage is repeatable within \( \pm 0.15 \) V at each bias field. There is a linear trend within a device, but variation between different devices. Devices 2 and 3 were fabricated at the same time from the same 10 mm \( \times \) 10 mm thin-film wafer piece, while device 1 was fabricated at a different time from a separate wafer piece and shows higher device-to-device variation in the \( V_T \) versus \( H_B \) slope. Thus, we can conclude that the device-to-device variation seen in the prototypes arises from variations in fabrication, i.e., electron-beam resist age and etching rates, and variation in the MgO thickness across the initial 3-inch diameter thin film wafer, which causes variation in TMR across the wafer.

![Figure 4.19 Threshold voltage versus bias field for three different devices, where the error bars represent the depinning voltage standard deviation repeated at least 3 \( \times \), with the DW reinitialized between each. Grey=device 1, red=device 2 and blue=device 3. The lines are a linear fit. Devices 2 and 3 were fabricated together, while device 1 was fabricated at a later time on a different wafer piece [6].](image-url)
We can estimate the zero-field current density from the linear trends: for device 1, $V_T(H_B=0) = 6.27 \text{ V}$. Converting to $I$ with $R_w = 4.4 \text{ k}\Omega$, we find $I_T(H_B=0) = 1.4 \text{ mA}$ and $J_T(H_B=0) = 8.75 \times 10^{11} \text{ A/m}^2$. This is in agreement with the current density needed to translate a DW in in-plane magnetic anisotropy wires [20].

### 4.7 Switching Energy

The velocity of spin torque transfer can be defined as [9]:

$$v_{\text{STT}} = \frac{I_{\text{app}} P g B M_s}{2 w t e M_s}$$

(4.9)

where, $w$ and $t$ are the width and thickness of the magnetic wire, ($w = F$, $F$ = DRAM’s half-pitch), $P$ is the polarization of the magnetic materials, $e$ is the charge of electron, $M_s$ is the saturation magnetization, $g$ is the Lande factor, $\mu_B$ is Bohr magnetron and $I_{\text{app}}$ is operating current for DW-Logic switching. Assuming, $w = 15 \text{ nm}$, $t = 3 \text{ nm}$, $P = 0.8$, $M_s = 6 \times 10^5 \text{ A/m}$ and $I_{\text{app}} = 6 \mu\text{A}$, $v_{\text{STT}} = 7.88 \text{ m/s}$. A reasonable assumption could be that the DW velocity is about $3 \times v_{\text{STT}}$, $v_{\text{DW}} \approx 24 \text{ m/s}$.

If the DW has to travel at least $2F$ distance to switch the device, the minimum switching time would be $\tau = 2F / v_{\text{DW}} = 1.26 \text{ ns}$. The device switching energy:

$$E = I_{\text{app}} V \tau$$

(4.10)

The switching energy then becomes 17.5 aJ. If the magnetic wire thickness is reduced to $t = 1 \text{ nm}$, then $\tau$ would be 0.4 ns and switching energy would be $\sim 6 \text{ aJ}$.

The above calculations only include spin torque transfer as the mechanism for DW motion. If the DW motion occurs due SOT, introduced in Chapter 3, the current density necessary to depin a DW can be on the order of $10^{10} \text{ A/m}^2$ [16]. We can calculate $I_{\text{app}} = 450 \text{ nA}$ without even considering
the increase in DW velocity, the switching energy would be one to two orders of magnitude lower for SOT driven DW-Logic devices.

In summary, we have demonstrated the capability of DW-based devices as logic gates, including inverter, buffer, and circuit operation. The DW depinning is non-linear with a sharp switching threshold \( \delta V < 0.01 \) V, allowing stable ‘0’ and ‘1’ bits below and above the DW depinning voltage. The gates exhibit gain, one gate can drive two subsequent gates, and the three-device circuits shows that they can be cascaded into circuits. The micromagnetic/circuit simulation shows analogous switching behavior to the experiment in further scaled devices. While the information is encoded in the DW position, the inputs and outputs are current, maintaining compatibility with conventional field-effect transistors. These results show that magnetic-based logic has a realistic path to implementation, and may provide the basis for digital systems at the end of the semiconductor roadmap.
References


There has been great interest in artificial intelligence both in research and in industrial applications [1, 2]. Recently, artificial neural networks have shown significantly improved accuracy in large-scale visual and auditory recognition and classification tasks, even comparable to human level accuracy [3]. Particularly, convolutional neural network, recurrent neural network algorithms and their variants have proved efficacy in a wide range of video [4], image [5] & voice [6] recognition and in biological applications. This performance has been realized by increasing the depth and the size of the neural network [7]. Thus, state-of-the-art systems present significant challenges to hardware implementations in terms of computation, memory and communication resources. The reliable classifications of data requires thousands of processor core, hundreds of kWatts of power [8], and days to train the network.

Figure 5.1 Neuromorphic computation scheme for deep learning in a single layer.
Figure 5.1 shows the operation scheme of an artificial convolutional neural network in a single layer. An image or speech signal is divided into multiple channels of input signals. Then the signals are convoluted with the predefined weights (synaptic weight) and eventually summed and passed through an activation/thresholding block, entering the next layer for next level of classifications. Learning of the synaptic weights and the activation functions are done using a procedure named back propagation [9]. The learning procedure is based on minimizing the difference between the actual output vector and the desired output vector. The synaptic devices are required to have a linear and symmetric relationship between the conductance and the number of identical programming pulses for a direct mapping of the weights in the algorithms to the conductance in the devices. Complete parallelism in each layer requires small footprint threshold devices after the convolution operation.

Today’s deep neural network is typically trained with GPU accelerators in a data center. This is not viable for the embedded systems and Internet of Things (IoT) devices (i.e. autonomous vehicle, health monitoring devices, etc.) because of the constraints in power, efficiency and performance. There have been a few on-chip solutions in complementary metal oxide semiconductor (CMOS) technology, i.e. IBM’s TrueNorth [2], MIT’s Eyeriss [10] etc. However, limitations still exist in on-chip memory capacity, off-chip memory access, on-line learning and most importantly energy efficiency.

Most of the CMOS accelerators are built with static random access memory (SRAM) as the synaptic memory on-chip. These accelerators typically suffer from insufficient SRAM density (100-200 F$^2$ per bit, where, F is the technology node) and limiting the capacity to store the large number of parameters necessary for deep learning algorithm. The parallelism is also limited in
SRAM accelerators due to row-by-row operations. The leakage power of SRAM is also very high for accelerators.

Table 5.1 Comparison of key features of existing and emerging memories (adapted from [11]).

<table>
<thead>
<tr>
<th></th>
<th>SRAM</th>
<th>eDRAM</th>
<th>DRAM</th>
<th>eFlash (NOR)</th>
<th>Flash (NAND)</th>
<th>FeRAM</th>
<th>PCM</th>
<th>STT-MRAM</th>
<th>BRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Endurance (cycles)</td>
<td>Unlimited</td>
<td>Unlimited</td>
<td>Unlimited</td>
<td>$10^4$</td>
<td>$10^8$</td>
<td>$10^{10}$</td>
<td>10^8</td>
<td>Unlimited</td>
<td>$10^9$</td>
</tr>
<tr>
<td>Read/write access time (ns)</td>
<td>&lt;1</td>
<td>1-2</td>
<td>30</td>
<td>$10/10^3$</td>
<td>$100/10^6$</td>
<td>30</td>
<td>10/100</td>
<td>2-30</td>
<td>1-100</td>
</tr>
<tr>
<td>Density</td>
<td>Low (six transistors)</td>
<td>Medium</td>
<td>Medium</td>
<td>Medium</td>
<td>High (multiple bits per cell)</td>
<td>Low (limited scalability)</td>
<td>High (multiple bits per cell)</td>
<td>Medium</td>
<td>High (multiple bits per cell)</td>
</tr>
<tr>
<td>Write power</td>
<td>Medium</td>
<td>Medium</td>
<td>Medium</td>
<td>High</td>
<td>High</td>
<td>Medium</td>
<td>Medium</td>
<td>Medium</td>
<td>Medium</td>
</tr>
<tr>
<td>Standby power</td>
<td>High</td>
<td>Medium</td>
<td>Medium</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Other</td>
<td>Volatile, Refresh power and time needed</td>
<td>Volatile, Refresh power and time needed</td>
<td>Volatile, Refresh power and time needed</td>
<td>High voltage required</td>
<td>High voltage required</td>
<td>Destructive readout</td>
<td>Operating $7&lt;125^\circ C$</td>
<td>Low read signal</td>
<td>Complex mechanism</td>
</tr>
</tbody>
</table>

Significant disadvantages are marked in bold. Estimates for emerging memories are based on expectations for functioning chips, not demonstrations of individual bits. See text for abbreviations.

An alternative hardware platform for these accelerators is the emerging non-volatile memory (eNVM) device for storing the synaptic weights. These devices promise the benefits of high density and fast parallel analog computing with low leakage power. eNVM devices with multilevel resistance/conductance states can emulate the synaptic behavior in neural networks. Examples of eNVM devices can be divided into two main categories (i.e. electronic and magnetic) based on the computational state (i.e. charge or spin of electron) of the devices. Electronic eNVMs include phase change memory (PCM) [12, 13], resistive random access memory (RRAM), three terminal ferroelectric [14, 15] and floating gate memory [16] have been widely studied in recent years. In contrast, magnetic NVMs (i.e. magnetic tunnel junctions (MTJ) [17], spin-torque memristor [18]) have not been explored extensively for neuromorphic accelerators. Compared to electronic eNVMs, magnetic NVMs show lower energy consumption and higher cell density, which is
essential for implementing neuromorphic computation. Table 5.1 shows the important performance metrics for conventional memory devices and eNVM [11].

In this chapter, we will show the experimental implementation of MTJs as discretized synaptic and activation function generators for neuromorphic accelerators. In particular, we will develop a linear synaptic resistor by utilizing the domain wall motion in the free layer of the magnetic tunnel junction. Besides, taking advantage of the size dependent magnetoresistance of the tunnel junctions, we will also demonstrate the nonlinear activation function (i.e. sigmoid function).

MTJs are used as magnetic random access memory (MRAM) [19], read head [20] for storage class magnetic memory and magnetic field sensors [21]. For the first two cases, the two-resistance states are enough to store 1's and 0's on the computers. However, for the synaptic device, a multistate linear resistor is required to achieve higher classification accuracy [22]. We propose to introduce a magnetic domain wall (DW) inside the free layer and drive the DW with electrical current. This will change the relative alignment of the spins in the reference layer and free layer and therefore, will create a gradual change of the resistance of the MTJ. The resistance modulation of the MTJ will be:

\[ R_{\text{MTJ}} = R_p \left( \frac{x}{L} \right) + R_{\text{AP}} \left( 1 - \frac{x}{L} \right). \]

where, \( R_p \) (\( R_{\text{AP}} \)) is the resistance of the MTJ while the spins in the two FMs are parallel (antiparallel). \( x \) is the position of the DW inside the free layer and \( L \) is the length of the MTJ.

Figure 5.2a and Figure 5.2b show the device structure and the position of the DW & the resistance modulation of MTJ with the DW driving current, respectively.
The DW in the FM layer is typically moved by pulsed current where the pulse duration is usually in the order of nsec. If the amplitude of the current pulse is high enough (above a certain threshold value), DWs move at a constant velocity. Figure 5.3 shows the experimental measurement of DW velocity as a function of the current density. We propose to drive the DWs in the linear regime where the DW velocity increases linearly with the current density for the synaptic weight MTJs.

![Figure 5.2(a) Domain wall based magnetic tunnel junction for synaptic weights [23]. (b) Domain wall position and the MTJ resistance as a function of input current between V+ and V-.

![Figure 5.3 Domain wall velocity in perpendicular magnetic anisotropy CoFeB as a function of current density.](image)
The complete convolution layer also requires a thresholding operation on the convoluted signals. Usually, in PMA wires, the motion of DWs rely on the electrical current in the high spin-orbit interaction (SOI) layer adjacent to the FM, thanks to spin orbit torque (Chapter 3). Therefore, by varying the current density in the SOI layer, we can move the DW at different speeds depending on its position along the MTJ and thus obtain nonlinearity in resistance vs. current relationship. We can create a variable current density by patterning the SOI layer. The detail model for the threshold function is derived in the later sections.

5.1 Domain wall motion in a magnetic wire with constant width and synaptic model for a single domain wall motion in a magnetic wire:

We use magnetic CoTb to observe domain wall (DW) motion experimentally in micro-wires of constant width with MOKE microscopy (Chapter 3 Section 3.4 for the detail of MOKE measurement). The electrical set-up is shown in Figure 5.4a. Both up (↑) and down (↓) domains move along the current direction with the applied pulses. We apply current pulses of increasing amplitude with constant pulse width. With the increase in the pulse amplitude, travelling distance of both the ↓↑ and ↑↓ DWs increases with constant slope of 2.155 μm/mA.

If the magnetic wire forms the free layer of a magnetic tunnel junction, the linear DW motion in the wire due to spin orbit torque will change the ratio of the parallel to antiparallel magnetic orientations with respect to the reference layer and can provide a linear change in magnetoresistance (Figure 5.4b).
Figure 5.4 Current-induced linear domain wall motion in wires with constant width. (a) Electrical set-up for the domain wall motion measurement. The brown and the green regions represent down (↓) and up (↑) domains in the MOKE microscope image of 4 μm wide CoTb wire. (b) Domain wall motion in CoTb wire with consecutive current pulses. Blue and red symbols show the initial positions of ↓ and ↑ domain walls in (a), respectively. The error bars reflect standard deviations from multiple measurements.
5.2 Model for activation/threshold function with single domain wall

We develop an analytical model for the SOT driven DW based MTJ to identify the width variation of the SOI layer under the free layer [24]. Let $x_0(I_{IN})$ be a function to generate output domain wall position $x_0$ with input current $I_{IN}$. The output of the MTJ function evaluator is an analog resistance value. The output resistance of the DW based MTJ can be expressed using Equation 5.1.

We derive the width $w(x)$ as a function of distance $x$ along the wire from the initial DW position, necessary to satisfy $x_0(I_{IN})$, starting from equations with the final position of the DW. We start with the DW velocity function $v(x)$:

$$v(x) = \begin{cases} 
0, & J < J_c \text{ (i.e. } x = 0) \\
(\eta f(x) - J_c), & J \geq J_c \text{ (i.e. } x > 0) 
\end{cases}$$

where, $J_c$ is the critical current density for DW motion, and $\eta$ is the proportionality constant between the current density and domain wall velocity. Now, input current ($I$) is related to the current density by the width and thickness of the wire:

$$\frac{dx}{dt} = \eta \frac{(x_0) - I_c}{w(x)d}.$$  \hspace{1cm} 5.3$$

where, $d$ is the thickness of the nanowire and $I_c$ is the critical current. If we assume the current is applied as a pulse of width $t_0$ and $x > 0$, the width variation along the length of the MTJ becomes:

$$w(x_0) = \frac{\eta t_0}{d} \frac{dx_0}{dx_0}.$$  \hspace{1cm} 5.4$$

Here, $I(x_0)$ is the inverse function of $x_0(I_{IN})$. Note that although $I(x_0)$ is a function with an offset, we do not need to know the offset in order to calculate its derivative to obtain $w(x_0)$. However, there is a constraint on the desired transfer function that the $x_0$ must increase monotonically with $I_{IN}$ [24].
5.3 Activation function generation with a single domain wall

We use micromagnetic simulation first to simulate the activation function generation using a single domain wall in a ferromagnetic wire. We use Mumax3 [25] to simulate the micromagnetic dynamics in the device including spin-orbit torque with $\alpha = 0.01$, unit cell size of $1.5 \text{ nm} \times 1.5 \text{ nm} \times 2 \text{ nm}$, and standard materials parameters for CoFeB (saturation magnetization $7960 \text{ kA/m}$, exchange stiffness $10^{-12} \text{ J/m}$, and magnetocrystalline anisotropy $7.82 \times 10^5 \text{ J/m}^3$) [24]. We use a spin Hall angle of 0.15 and an interfacial Dzyaloshinskii-Moriya strength of $-0.5 \text{ mJ/m}^2$ [24].

![Micromagnetic simulation and Analytical model](image)

Figure 5.5 Domain wall position in a perpendicular magnetic anisotropy wire as shown in the schematic (inset) with 4 ns current pulse. The analytical model is obtained from a shifted sigmoid function.

We used Object-Oriented Micromagnetic Framework (OOMMF) [26] to analyze the results from Mumax3. The micromagnetic simulation shows that DW travelling distances can be a nonlinear function of the input current (Figure 5.5). The width of the bottom heavy metal is shown in the inset of Figure 5.5. The nonlinear function in this particular case is the sigmoid function, which is one of the widely used activation function for neuromorphic or deep learning accelerators [27].
The fit from the analytical model in Figure 5.5 shows that the simulated DW motion agrees well with the sigmoid function.

To experimentally demonstrate thresholding function using a single magnetic domain wall, we use a Pt (3 nm)/CoTb (2 nm)/SiNx (3 nm) structure and magneto-optic Kerr effect measurements to examine nonlinear domain wall motion in a wire with non-uniform width. We pattern the Pt wire in a shape determined from the analytical function in Section 5.2 and keep the CoTb wire width constant as shown in the schematics in Figure 5.6a.

The CoTb samples are deposited using DC magnetron co-sputtering of Co and Tb. The films are capped with 3 nm of SiNx insulating layer using RF sputtering. The samples for magneto optic Kerr effect measurement are patterned using a bilayer resist stack of HSQ and PMMA (similar to the process described in Chapter 2) in two e-beam lithography steps. In the first e-beam lithography step, we pattern the bottom Pt wire. The films are then ion-milled with Ar⁺ ions. We remove the resists stack and spin the same resists stack again for the second e-beam lithography step. In this step, the CoTb/SiNx wires with constant widths are patterned and ion-milled afterwards. Finally, we remove the resists stack in hot NMP. We ensure that the processing temperature of the CoTb samples remains < 100 °C to eliminate the possibility of change in the magnetic properties of thin films.

Using the magneto-optic Kerr effect and electrical setup shown in Figure 5.4a, we measure the domain wall motion after applying current pulses of width 300 ns (Figure 5.6b). For each measurement, the domain walls are initialized at A as shown in the inset of Figure 5.6. We observe that the domain wall travelling distances successfully follow the sigmoid function design for the activation function generator.
Figure 5.6 (a) Schematic of an activation function generator with a single domain wall in a CoTb wire. The bottom Pt layer is patterned so that its width varies along the length of the wire according to the analytical model obtained from a shifted sigmoid function [24]. The width of the CoTb wire is constant. (b) Magnetic domain wall travelling distances in a CoTb wire as shown in the inset with 300 ns current pulses. Inset shows the magnetoptic Kerr microscopy image of a CoTb wire with two domain walls. The black dotted line marked by A in the inset shows the initial position of the domain wall for all currents.
5.4 Development of perpendicular magnetic anisotropy tunnel junction

A successful demonstration of the linear synaptic weight and the nonlinear threshold function using an MTJ requires the development of a carefully engineered film stack with precise requirements over the deposition of nanometer scale thin films. A typical film stack is shown in Figure 5.7. Usually, the free layer is designed as the top ferromagnetic electrode because it makes the choice of the seed layers convenient for depositing the reference layer first. However, we need a PMA MTJ with the free layer as the bottom FM of our stack since we introduce the DW in this layer and the driving mechanism is SOT from the SOI layer. This makes the development of MTJ films even challenging due to the inability to deposit proper thin films for seeding the reference layer.

The thin metal films for the magnetic tunnel junction structures are deposited by DC magnetron sputtering while the tunnel barrier, MgO is deposited by radio frequency sputtering at 2 mTorr on a thermally oxidized Si substrate. The base pressure of the chamber is $8 \times 10^{-9}$ Torr.

Different thin films for MTJs are optimized in multiple steps. The detailed steps of the development of the MTJ films is shown in Figure 5.8.

![Figure 5.7 CoFeB based magnetic tunnel junction.](image)
In our first step, we develop a CoFeB free layer with PMA. The seed layer is Ta and we deposit a series of Ta/CoFeB/MgO structures by varying the thickness of CoFeB layer from 0.6 nm – 1.1 nm at 0.1 nm step. MgO will work as the insulating layer for the MTJ. Figure 5.9 shows the hysteresis loop of the as deposited and annealed thin films measured using vibration sample magnetometry (VSM). The thin films were annealed at 300 °C for improving the PMA of the samples. Figure 5.10 shows that the annealed sample has better uniaxial anisotropy compared to the as deposited sample.

Figure 5.8 Steps for optimizing MTJs for neuromorphic devices.
Figure 5.9 Hysteresis loops of as deposited and annealed free layers.

Figure 5.10 Interface anisotropy energy of as deposited and annealed CoFeB free layer of MTJs.
In the second step, we develop the PMA CoFeB films for the reference layer. We deposit CoFeB on top of MgO and vary its thickness to identify the exact thickness required for the PMA. We deposit a very thin layer of CoFeB (0.4 nm) underneath the MgO to ensure the right crystal structure and the growth of the insulator. We confirm that 0.4 nm thick CoFeB layer acts as a magnetically dead layer. Figure 5.11 shows the hysteresis loop for the as deposited and the annealed samples. Unlike the bottom CoFeB layer, none of these samples shows 100% remanence in the as-deposited state. However, after annealing at 300 °C on the hotplate the structures with top CoFeB thickness between 1.4 nm to 1.7 nm shows PMA. The anisotropy energies of the top CoFeB layers are smaller than the anisotropy energies of the bottom PMA layers. Therefore, in the patterned MTJ, the top CoFeB will act as the free layer, which is opposite to what we need.
To ensure that the top CoFeB layer is the reference layer for MTJs, the coercive field of the CoFeB layer need be increased. Since the PMA in CoFeB comes from the interfacial anisotropy, increasing the thickness of the CoFeB layer is not an option. Rather this will require ferromagnetic coupling of this layer with another hard magnet. We choose a Co/Pt multilayer (ML) as the hard ferromagnet which shows strong PMA and also good tunability of saturation magnetization with the number of repeated layers. We developed a series of Co/Pt ML, to identify the thicknesses of Co and Pt layers and the number of repetitions in the ML stack. Figure 5.12(a) and Figure 5.12(b) show the coercive fields and the saturation magnetization of the films with the thickness of the Co and Pt layers, respectively. We use constant thickness of Pt (1.0 nm) and Co (0.5 nm) while varying the thickness of the other material. We choose Co thickness of 0.5 nm and the Pt thickness of 1.0 nm as this combination gives the most square out-of-plane hysteresis loop.

The next step is to couple the Co/Pt ML with the top CoFeB layer. We use a thin layer of Ta between the CoFeB and the Co/Pt ML since it improves both the coupling between the CoFeB and the Co/Pt ML and the tunnel magnetoresistance of the MTJ. The hysteresis loop of the reference
layer is shown in Figure 5.13. However, after patterning the MTJ, the coercivity of the free layer may increase due to the pinning from the edges. Therefore, the coercivity of \(-500\) Oe for the reference layer may not be enough to switch the free layer in the MTJ without switching the reference layer using magnetic field or electric current. We observe that the coercivity of the reference layer do not increase with the repetitions of Co/Pt layers (Figure 5.12), which eliminates the options of increasing the repetitions of the MLs.

![Figure 5.13 Out-of-plane hysteresis loop of (a) as deposited and (b) annealed reference layers in Figure 5.8(d) with different thickness of CoFeB (t_{CoFeB}).](image)

To improve the coercive field of the reference layer, we propose to ferromagnetically couple a synthetic antiferromagnet (SAF) of Co/Pt ML with the top CoFeB. Before developing the combined reference layer, we develop the sputtering recipe for the Co/Pt SAF. SAF is a sandwich structure of FM/normal metal/FM where the two FM layers are indirectly exchange coupled with each other antiferromagnetically. Previous studies show that there exists a long-range indirect magnetic exchange coupling between two FM layers separated by thin layers of nonmagnetic
(NM) transition metals [28-31]. The exchange coupling shows oscillatory behavior with the thickness of the nonmagnetic metal (Figure 5.14). Among all the 3d, 4d and 5d transition metals, Ru shows the highest exchange coupling between the FM [30]. We vary the thickness of the Ru layers between the two [Co(0.5 nm)/Pt(1 nm)]₃ layers from 0.4 nm – 1.3 nm. We do not observe the antiferromagnetic coupling at the first peak of the oscillation because the Ru films may not be continuous at those thicknesses (0.4 nm – 0.6 nm). However, antiferromagnetic coupling at the second peak of oscillation starts from 0.8 nm thickness of Ru in these samples. We calculate the exchange coupling energy of the antiferromagnetic coupling with the Ru thickness from \( J_{Ru} = H_{Ru} t M_s \), where \( J_{Ru} \) is the exchange energy, \( t_{Ru} \) is the thickness of the Ru layer, \( H_{Ru} \) and the \( M_s \) are coercive field and the saturation magnetization of the complete FM/NM/FM stack.

![Graph](image)

**Figure 5.14** Antiferromagnetic coupled exchange field and estimated exchange coupling energy density \( (J_{ex}) \) vs. Ru thickness \( (t_{Ru}) \) in as-deposited SAF structures [28].

For improved TMR of the MTJ, the film stack needs to be annealed at high temperature. To confirm that the SAF behaves properly after annealing in the final stack, we annealed these stacks at 300 °C for an hour on a hot plate in N₂ environment. Figure 5.15(a) and 5-11(b) show the
hysteresis loops of as-deposited and annealed SAFs, respectively. SAFs with Ru thickness between 0.8 nm – 1.0 nm preserve their antiferromagnetic properties even after annealing. The other stacks starts to lose their antiferromagnetic coupling which may cause due to the inter-diffusion of Co and Pt layers and/or Co diffusion in Ru layer [32].

![Hysteresis Loops](image)

Figure 5.15 (a) As deposited and (b) annealed Co/Pt synthetic antiferromagnets with different Ru thickness.

From the characterization of all the above thin films stack, we design the optimized structure as shown in Figure 5.16(a). Figure 5.16(b) shows the hysteresis loop of the deposited stack after annealing at 250 °C for 15 min on hot plate in N₂ environment.
Figure 5.16 (a) Final structure of the MTJ for synaptic and activation devices. (b) Hysteresis loop of the thin films in (a) after annealing at 250 °C. The magnetic configuration of the different magnetic layers are shown as the field is swept.

We characterize the annealed thin films also using transmission electron microscopy (TEM). The cross-sectional TEM sample was prepared via focused ion beam (FIB) on the FEI Helios Nanolab 600 Dual Beam System. Prior to FIB, 20 nm of Au was sputter coated onto the devices using a MS Q150T ES coater to reduce charging effects from insulating layers during the TEM sample preparation process. Afterwards, high-resolution TEM images were collected with a JEOL 2010 FEG Analytical Electron Microscope. The TEM image in Figure 5.17 shows the crystalline MgO, CoFeB and Co/Pt MLs.
5.5 Fabrication of PMA MTJs

The fabrication of the PMA MTJs could be same as the fabrication of the IMA MTJs. However, to reduce an e-beam lithography step in the process and save processing time and improve the yield of fabrications, we patterned the devices following steps in [33].

Fabrication of the devices is completed using three electron-beam lithography steps and two Ar$^+$ ion-milling steps. The step-by-step details of the fabrication steps are shown in Figure 5.18.
Figure 5.18 Fabrication steps for PMA MTJs for synaptic and activation function generator. Step (xiii) shows the schematic of a complete device.
In the first lithography step, we pattern the free layer (bottom wires) using HSQ/PMMA bilayer stack as described in Chapter 2 (Steps (i), (ii) and (iii)). The e-beam exposure of HSQ is completed using Elionix F-125 Tool. The exposure parameters are given in Table 5.2.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
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</thead>
<tbody>
<tr>
<td>Field size</td>
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</tr>
<tr>
<td>Number of dots in a field</td>
<td>50000</td>
</tr>
<tr>
<td>Resolution</td>
<td>10 nm</td>
</tr>
<tr>
<td>Beam current</td>
<td>10 nA</td>
</tr>
<tr>
<td>Dose time</td>
<td>0.25 μs/dot</td>
</tr>
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</table>

Later thin films are ion-milled using Ar⁺ ions at 1×10⁻⁴ Torr pressure with 3 sccm gas flow. The base pressure of the ion-milling chamber is 1×10⁻⁷ Torr. In this step, the complete film stack is milled (step (iv)). We design the many large (100 μm × 100 μm) pads around the sample so that in the next step there are enough materials on the substrate to be detected easily with the end-point-detector. After the ion-milling step, we remove the resists stack in NMP on hot plate at 130 °C. Occasional sonication is used to help the resists removal (step (v)).

For the next lithography step, we spin OMNICOAT in two steps on the sample at 1000 rpm (thickness ~30 nm) and bake the samples at 150 °C on hot plate after each spin. The use of OMNICOAT is essential for successful lift-off of the insulating SiO₂ in the later steps. Afterwards, we spin and bake the HSQ/PMMA resists stack similar to step (i) (step (vi)). We pattern the MTJs with the e-beam exposure with 1 nA current at 1.25 nm resolution using Elionix F-125. After developing HSQ and creating undercut in PMMA with O₂ plasma (step (vii)), the stack is ion-milled up to the MgO barrier using the milling conditions in step (iv) (step (viii)). The use of an end-point detector is essential for the precision of the etch-stop.
After the second ion-milling step, we evaporate SiO$_2$ at base pressure $2 \times 10^{-6}$ Torr to ensure the electrical separation of the top and the bottom contacts of the tunnel junctions without removing the OMNICOAT/HSQ/PMMA stack (step (ix)). SiO$_2$ is then lifted off using combination of hot NMP (1 hour) and sonication (30 min) in turns (step (x)). This step requires 3-6 hours (i.e. 2-4 runs of hot NMP/sonication).

For the last lithography step, we spin 4% PMMA in Anisole at 2000 rpm (thickness ~300 nm) (step (xi)). The e-beam exposure parameters for this step are given in Table 5.3.

<table>
<thead>
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<th>Parameters</th>
<th>Values</th>
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<tbody>
<tr>
<td>Field size</td>
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</tr>
<tr>
<td>Number of dots in a field</td>
<td>50000</td>
</tr>
<tr>
<td>Resolution</td>
<td>30 nm</td>
</tr>
<tr>
<td>Beam current</td>
<td>10 nA</td>
</tr>
<tr>
<td>Dose time</td>
<td>0.32 µs/dot</td>
</tr>
</tbody>
</table>

After developing the samples in 1:3 MIBK:IPA solution, we evaporate Ti (10 nm)/Au (100 nm) for the contacts of the wires and tunnel junctions at $2 \times 10^{-6}$ Torr pressure (step (xii)) and lift-off the metals afterwards with Acetone (step (xiii)).

A schematic of the complete sample is shown in the bottom panel of Figure 5.18.
5.6 Characterization of MTJs
5.6.1 Switching with magnetic field

After fabrication of the MTJs, we first characterize the tunnel resistance as a function of magnetic field at room temperature. Prior to electrical measurements, we apply a large magnetic field of 10 kOe to align the reference layer to a single domain state (†). Figure 5.19a and Figure 5.19b show the scanning electron microscope (SEM) images of a 1 μm × 3 μm MTJ and a complete device along with the two terminal resistance measurement setup, respectively. The magnetic tunnel junctions are measured on a custom built probe station equipped with an out-of-plane electromagnet. The anomalous Hall resistance of the wires is measured using four contacts and the magnetoresistance of the tunnel junctions is measured using two contacts. A Keithley 2400 source meter is utilized for these quasi DC measurements. The current applied to measure the tunnel
junction was 100 nA. Figure 5.19c shows that the TMR of a 1 \( \mu m \times 3 \mu m \) MTJ is \(-44\%\) as calculated from a two terminal measurement.

![Graph showing RA product and TMR of MTJs of different areas.](image)

Figure 5.20 RA product and TMR of MTJs of different areas. RA product is 1200(\pm200) k\( \Omega \)-\( \mu m^2 \) with junction area.

Magnetic tunnel junctions (MTJs) of different cross-sectional areas were fabricated for use in synaptic and activation function generators and characterize the resistance-area (RA) product and TMR as a function of MTJ area. Figure 5.20 shows RA product for the MTJs are 1300\(\pm100\) k\( \Omega \)-\( \mu m^2 \), as expected for \(\sim\) 2 nm thick MgO. For small area MTJs, TMR increases with the junction area. MTJs with area larger than 2 \(\mu m^2\), do not show any correlation with their junction area.
Figure 5.21 (a) Magnetic switching of regions the CoFeB wire with and without tunnel junctions. The switching of the CoFeB wires under the tunnel junction is completely dominated by the stray field from the tunnel junction. (b) Schematic of the fabricated tunnel junction after applying a small magnetic field along -z direction. The region of the wire under the tunnel junction with initial parallel state of spins, remain parallel. The rest of the wire behave as a magnetically free ferromagnetic layer and switches with small magnetic field. Therefore, two domain walls are nucleated at the two sides of the tunnel junctions.

To understand the effect of the reference layer on the free layer switching, we measure the anomalous Hall resistance of the bottom CoFeB wire with and without the top CoFeB layer. Figure 5.21a demonstrates the impact of the stray field of the reference layer. Bottom CoFeB wire switches with < 50 Oe in the absence of the reference layer. In contrast, the switching of the bottom CoFeB wire with a reference layer on its top depends completely on its stray fields. Therefore, the switching fields are much higher than the standalone CoFeB wire. Figure 5.21b shows the schematics of the MTJ and the domain orientations in a CoFeB wire with a small magnetic field. The applied field is large enough to switch the bottom CoFeB wire in regions without the reference
layer but is not large enough to switch the regions under it. We utilize this approach for generating discrete magnetic domains underneath the MTJs later.

5.6.2 Switching with electrical current

In this section, we characterize a 200 nm × 600 nm MTJ which we will use to demonstrate the synaptic functionality. The field induced magnetic switching of this MTJ is shown in Figure 5.22.

![Figure 5.22 Field induced magnetic switching of the CoFeB wire under 200 nm × 400 nm magnetic tunnel junction.](image)

We design a test setup with out-of-plane magnetic field to characterize the current-induced switching of the MTJs. The current to switch the MTJs is applied in the CoFeB wire to drive the nucleated domain walls using SOT from the Ta layer, which eventually will switch the MTJs. The schematics of the set-up is shown in Figure 5.23.
Figure 5.23 Schematic of the magneto-electrical set-up for measuring the magnetoresistance of the magnetic tunnel junctions with magnetic domain walls. A small bias field lower than the switching field of the free layer is applied out-of-plane of the junction to reduce the pinning of the domain walls.

To measure the current induced domain wall motion, we use radiofrequency probe for applying the nano-second current pulses in CoFeB wires using either an Agilent 8130A or an Agilent 8114A pulse generator and utilize DC probes to measure the tunnel magnetoresistance using a Keithley 2400. The current applied to measure the tunnel junction is 100 nA. We apply a series of current pulses with increasing amplitude and measure the resistance of the tunnel junction after each current pulse.
We nucleate domain walls on the edges of the MTJ by following the approach shown in Figure 5.21. Figure 5.24 shows the complete switching of 200 nm × 400 nm MTJ from parallel to antiparallel state at different bias field. With the increase in the bias fields, the current required to switch the free layer of the magnetic tunnel junction reduces. Irrespective of the bias fields, the tunnel junction switches completely due to the domain wall motion in the free layer from one edge of the reference layer to its other edge. For the same bias magnetic field, the tunnel junction switches at similar electrical current irrespective of the current directions, which is consistent with the fact that the device is symmetric. The switching current densities extracted from similar
experiments on different width MTJ agree well with the threshold current of the DW motion in a CoFeB wire (Figure 5.3).

![Figure 5.25](image)

**Figure 5.25** (a) Maximum and minimum current required to switch MTJs by using domain wall motion. (b) Switching current density calculated from the current in (a) and the cross-sectional area of wires with constant width.

We induce the current-induced MTJ switching with wires of different width and plot the switching current as a function of wire width. The threshold current density for MTJ switching is obtained from measurements summarized in Figure 5.25. We obtain $J_{th} = (1.0 \pm 0.25) \times 10^{11} \text{ A/m}^2$. 
5.7 Synaptic Function generator with multiple domain walls and MTJs

We next design and characterize a synaptic function generator with a linear relationship between input current and output resistance.

5.7.1 Model for synaptic function generation

Since the patterned reference layer of the magnetic tunnel junction causes pinning of two domain walls inside the magnetic wire of free layer, there are $2N$ domain walls in the wire. Here, $N$ is the number of total MTJs. For the model of synaptic function generator, we assume all the MTJ’s are identical and spaced evenly. MTJs switch when the current density in the free-layer is higher than the threshold current density, $J_{T_{th}}$.

$$I(x) = J_{T_{th}}w(x)d,$$ \hspace{1cm} (5.5)

where, $I(x)$, $w(x)$ and $d$ are the current at position $x$ along the length, width of the heavy metal, and thickness of the bottom heavy metal, respectively. The total resistance of the parallel-connected MTJs can be expressed as,

$$R = R_{AP} \frac{n}{N} + R_p \left( 1 - \frac{n}{N} \right).$$ \hspace{1cm} (5.6)

where, $n$ and $N$ are the number of MTJ already switched and the total number of MTJs. $R_p$ and $R_{AP}$ are the total resistance when all the MTJ’s are oriented parallel and antiparallel, respectively. Here, $n = N \frac{x_n}{L}$, where, $x_n = x$ for which $\frac{I(x)}{w(x)d} \geq J_{T_{th}}$ and $L =$ length of the wire (over which the MTJ’s are patterned).

A linear input-output characteristic is obtained for a linear relation between width and the length along the wire, $w(x) = mx$, where $m$ is a constant. Thus, $I(x) = J_{T_{th}}mxd$ and $x_n = \frac{l}{J_{T_{th}}md}$.

The total resistance then becomes,

$$R = R_{AP} \frac{l}{J_{T_{th}}mdL} + R_p \left( 1 - \frac{l}{J_{T_{th}}mdL} \right).$$ \hspace{1cm} (5.7)
5.7.2 Fabrication and characterization of the synaptic device

Following the analytical model, we pattern a series of discrete MTJs each with dimensions 200 nm × 400 nm on a CoFeB free layer. The linear function is implemented by patterning the free layer (bottom CoFeB) and the underlying heavy metal (Ta) with linearly varying width. Figure 5.26a and Figure 5.26b-c show the schematic and SEM images of the patterned structure, respectively. All MTJs are connected in parallel. At a suitable bias field, each of the MTJs supports a discrete magnetic domain.

![Figure 5.26](image)

Figure 5.26 (a) Schematic of a series of tunnel junctions device for discretized synaptic weight generation. The boundaries between the blue (up domain) and the red (down domain) regions in the free layer show the magnetic domain walls at the edges of the tunnel junctions. (b) & (c) Scanning electron microscope images of nine 200 nm × 400 nm magnetic tunnel junctions without (b) and with (c) electrical contacts. The tunnel junctions are connected in parallel to each other.

TMR measurements under a magnetic field yield steps in resistance vs. magnetic field characteristics, which correspond to the switching of nine MTJs from parallel to antiparallel states (Figure 5.27). Steps marked by B & D correspond to the switching of two single MTJs; C & E
correspond to switching of two MTJs simultaneously and A corresponds to switching of three MTJs. The regions of the CoFeB wire under the MTJs switch at slightly different magnetic fields due to fabrication-induced inhomogeneities in the local pinning fields.

Figure 5.27 Resistance of nine parallel MTJs shown in Figure 5.26c. (b) Switching of MTJs from parallel to antiparallel states with out-of-plane magnetic field.

To measure the electrical characteristics, we apply a series of 8-ns current pulses along the CoFeB/Ta wire with increasing amplitudes and observe the increase in magnetoresistance across the MTJs. Figure 5.28 shows the resistance of the parallel MTJs as a function of both positive and negative current in the CoFeB/Ta wire. The eight different resistance values correspond to consecutive switching of seven MTJs. Note that we did not observe the switching of the remaining two MTJs on the narrowest part of the wire. The current required to switch them is higher than the breakdown current of the narrowest part of the wire. The dotted lines show that the resistance of the synaptic device change linearly with the applied current.
Figure 5.28 Switching of the parallelly connected magnetic tunnel junctions in (e) with a bias field of -480 Oe. The eight steps correspond to the switching of seven MTJs with 8 ns current pulses. The linear fits of the magnetoresistance confirm the linear weight generation using MTJs.
Figure 5.29 (a) Scanning electron microscope images of seven 400 nm × 1200 nm magnetic tunnel junctions after the process step of reference layer milling. The tunnel junctions are connected in parallel to each other after the final process step. (b) The switching of the parallelly connected magnetic tunnel junctions in (a) with a bias field of -85 Oe.

We also characterize another device with seven magnetic tunnel junctions of size 400 nm × 1200 nm. The device characterization is shown in Figure 5.29. Four out of seven MTJs switch, yielding the expected linear response.
5.8 Activation function generation

We utilize the magnetic tunnel junctions to demonstrate the activation function generation. Prior to fabrication of the devices, we design the device structure using analytical modeling.

5.8.1 Activation function generation with multiple domains and MTJs:

To create domain walls at the edges of MTJs, we pattern a series of tunnel junctions on top of a single wire. For a shifted sigmoid thresholding function, the desired resistance as a function of input current is

\[ R = (R_{AP} - R_p) \cdot \frac{x_A}{L} \cdot \tanh \left( \frac{l_1 - l_2}{l_2} \right) + (R_{AP} - R_p)x_B + R_p \]  

where \( I_1, I_2, x_A, \) and \( x_B \) are scaling constants. Assuming identical, evenly-spaced MTJs, the corresponding width of the wire is:

\[ w(x) = \frac{1}{j_{\text{sat}}} \left( I_1 + I_2 \cdot \tanh^{-1} \left( \frac{x-x_B}{x_A} \right) \right) \]

Unfortunately, given this steep change in width profile, the current required to switch MTJs on the narrowest region (with maximum pinning) of the wire can be higher than its breakdown current density, which is \( 1.5 \times 10^{11} \text{ A/m}^2 \) in this particular case. To avoid this, we maintain a linear variation in the wire width, and a regular spacing between the MTJs, but we vary the size of each MTJ. The designed input-output characteristic shown in Figure 5.30 is based on the measured resistance-area and TMR products of our MTJs, and a switching current density of \( 0.7 \times 10^{11} \text{ A/m}^2 \).
Figure 5.30 The change in magnetoresistance of the designed MTJ device with nine MTJs connected in parallel. The large MTJs in the center of the wire, corresponding to the steepest portion of the activation characteristic.

5.8.2 Fabrication and characterization of thresholding devices

To implement a nonlinear function, we again pattern a series of MTJs on a CoFeB/Ta wire as shown in Figure 5.31.

Figure 5.31 (a) Schematic of a series of tunnel junctions device for discretized synaptic weight generation. The boundaries between the blue (up domain) and the red (down domain) regions in the free layer show the magnetic
domain walls at the edges of the tunnel junctions. (b) Scanning electron microscope images of nine magnetic tunnel junctions. The width of the free layer is varying linearly along its length.

In addition to varying the width of the CoFeB/Ta wire, we vary the MTJ areas, with large devices in the center of the wire, corresponding to the steepest portion of the activation characteristic, which is chosen to approximate a sigmoid function. The size of the MTJs are given in Table 5.4 (The MTJs are labeled from the left).

Table 5.4 Nominal area of the MTJs in the sigmoid thresholding function

<table>
<thead>
<tr>
<th>MTJ's label</th>
<th>Area</th>
</tr>
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<tbody>
<tr>
<td>1</td>
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<tr>
<td>2</td>
<td>200 nm x 400 nm</td>
</tr>
<tr>
<td>3</td>
<td>400 nm x 400 nm</td>
</tr>
<tr>
<td>4</td>
<td>600 nm x 600 nm</td>
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<tr>
<td>5</td>
<td>600 nm x 600 nm</td>
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<tr>
<td>6</td>
<td>600 nm x 600 nm</td>
</tr>
<tr>
<td>7</td>
<td>400 nm x 400 nm</td>
</tr>
<tr>
<td>8</td>
<td>200 nm x 400 nm</td>
</tr>
<tr>
<td>9</td>
<td>200 nm x 400 nm</td>
</tr>
</tbody>
</table>

The CoFeB/Ta wire is patterned with a linear increase in width along its length to initiate the switching of each MTJ at regularly-spaced input currents. Like the synaptic weight generator, all the MTJs are connected in parallel. Figure 5.31a and Figure 5.31b show a schematic and SEM images of the fabricated activation function generator, respectively.
We first characterize the nonlinear MTJ device by applying an out-of-plane magnetic field and observing the field induced switching of the nine MTJ's in the resistance vs. field plot (Figure 5.32). The MTJs switch non-uniformly as a function of magnetic field in both directions (from parallel to antiparallel and from antiparallel to parallel). The variation in switching fields is caused by variation in the pinning fields for the domain walls created at the edges of the MTJs. We also observe stochasticity due to thermal noise while sweeping the magnetic field in repeated multiple tunnel magnetoresistance measurements. Next, we use the experimental setup of Figure 5.23 to measure the electrical characteristics, with input current pulses ramped from zero to 620 μA. The bias field is chosen to be 200 Oe allowing us to observe switching of the maximum number (seven) of MTJs while also minimizing the potential barrier opposing domain switching within the free layer. The remaining two devices switch at lower fields due to inhomogeneity in the pinning field caused by fabrication imperfections. Averaged over 75 cycles to reduce thermal noise, the resistance of the parallel MTJs when switching with increasing current is shown in Figure 5.33.
Figure 5.33 Switching of the parallelly connected magnetic tunnel junctions in Figure 5.31(b) with a bias field of 200 Oe. The magnetoresistances are averaged from 75 measurements with 8 ns current pulses and the error bars show the standard deviation of magnetoresistance.

Figure 5.34 Switching of the parallelly connected magnetic tunnel junctions in Figure 5.31(b) with a bias field of -400 Oe. The magnetoresistances are averaged from 40 measurements with 8 ns current pulses and the error bars show the standard deviation of magnetoresistance. Magnetoresistances are normalized with respect to the resistances of the MTJs in regions of parallel to antiparallel switching.
The experimental data compares well to the design using seven MTJs, and even to the target shifted sigmoid activation function.

The low-high magnetoresistance switching characteristic is shown in Figure 5.34.

5.9 Discussions

The linear and nonlinear behavior exhibited by the devices in Figs 2 and 3 demonstrates that these three terminal MTJs can be customized for multiple functionalities within a neuromorphic accelerator. Optimization of the functional behavior could also occur post fabrication. In the same way that information is stored in MRAM, it is possible to drive current through individual MTJ to selectively program particular steps in the desired magnetoresistance curve by initializing each magnetic domain prior to applying the input current [34, 35].

A key consideration for application to neuromorphic systems is power consumption. Considering the resistive loss in the bottom CoFeB/Ta wire, the power required to switch the individual MTJs in prototype linear and nonlinear devices varies from 0.15 mW to 2.0 mW. With an 8 ns current pulse, the energy consumption ranges from 1 pJ to 16 pJ, which is better than most of the phase-change memory devices and comparable to resistive-random access memories [36]. For a scaled 10-nm-wide MTJ, the bottom CoFeB wire can be as narrow as 15 nm in width and the expected power to switch the scaled MTJs is as small as 420 nW considering the similar current density required to depin the domain walls in scaled devices. Given the same 8 ns current pulses employed here, the expected energy consumption per synaptic event is ~3 fJ. Thus, the energy consumption in a 10 nm wide MTJ is lower than other nonvolatile devices and even comparable to biological synapses [37].
MTJ-based devices are the basis of MRAMs and are compatible with traditional silicon processing. For application into cross-point array architectures, the resistances of the synaptic weight generators are required to be in the range of mega ohms [38]. This can be achieved in the proposed design by increasing the thickness of the MgO tunnel barrier if the size of the MTJs are chosen same as shown in Figure 5.26b. However, the thickness of MgO barrier should be 1.6 nm – 1.8 nm for scaled MTJ of 20 nm × 10 nm, considering the resistance-area product [39].

To summarize, in this chapter, we have demonstrated a linear synaptic weight generator and a programmable activation function generator using domain wall motion and a series of magnetic tunnel junctions. Our prototype devices operate with 8 ns current pulses with energy consumption on the order of 1 pJ. The energy required by scaled devices can be even comparable to that of biological synapses. Furthermore, the proposed devices are compatible with state-of-the-art CMOS processe flow. The versatility of magnetic DW technology for both computation and memory suggests that it is an excellent candidate for use in neuromorphic accelerators.
References


http://mumax.github.io/.

https://math.nist.gov/oommf/.


6 Summary and Outlook

6.1 Summary

CMOS electronics is approaching its limit. This is an exciting time to combine the rich physics and engineering to explore the creative applications of novel nano materials and devices. The DW-Logic devices explored in this thesis is one possible emerging technologies. We have developed device prototype with an in-plane anisotropy material, showing both individual logic functionality and integration in circuits. We experimentally verified that DW-Logic satisfies a number of required and desired characteristics for beyond-CMOS, including nonlinearity, gain, cascadability, feedback prevention, universal gate capability, scalability, and room temperature operation [1]. DW-Logic devices similar to STT-MRAM are compatible with CMOS circuits and processing. Besides, we theoretically predict it should operate with switching energies competitive or better than CMOS. This makes it a promising candidate for future computing applications.

Moreover, to enable the future computing using neural network, we have designed and modeled linear synaptic and programmable thresholding function evaluators. We have experimentally demonstrated the operations of both evaluators using a single domain wall and also using multiple domains. The synaptic function evaluators show linear behavior with the applied current, a desired characteristics for improved accuracy for pattern recognition. Moreover, our prototype activation function evaluator can generate sigmoid function for thresholding the accumulated signal at the end of any multiply and accumulation operations, unique to DW non-volatile devices. These devices are also comparable with the CMOS technologies. Besides, they show energy consumption
on the pico joule and operate faster than any other proposed non-volatile devices for synaptic operations.

In exploring magnetic materials for logic and logic-in-memory applications, we have developed a new method for fabricating magnetic nanostructures with sub-25 nm linewidth and low edge roughness [2]. We applied this method to model the pinning density for DWs in a nanowire in the presence of edge roughness. The pinning density identifies the stable DW position inside a nanowire, which effectively defines the resolution of DW motion with an applied field or current [3]. For a synaptic MTJ device with a single domain wall in the free layer this resolution directly translates to the resolution of the weights generated from such device. In designing such devices, magnetostatic interaction from neighboring domain walls need to be considered to achieve such resolution [4].

For fast and energy-efficient DW devices, we have studied the domain wall motion in a ferrimagnetic material using spin-hall effect. By varying the composition of the material, we identified the DW mobility is highest for the composition with zero angular momentum [5]. We also identified the internal structure *i.e.* type of domain wall and the chirality. For all the compositions, the domain wall is of Néel type with left-handed chirality. The presence of same chiral DW in all samples with different compositions ensures that DMI effectively work between the heavy metal and the spins of constituent materials instead of the total magnetization of the ferrimagnetic material. Our study opens up an avenue for angular momentum compensated ferrimagnetic materials in designing fast and energy-efficient domain wall devices [5].

Before we can predict the real promise of DW-devices, much more work needs to be done to investigate the system-level energy consumption and use that information to build new device and
circuit designs catered to the unique problems [1]. We theoretically predicted in Chapters 4 and 5 that the switching energy of DW-Logic device and scaled synaptic/activation function evaluators are competitive with CMOS and switching energy and even comparable to biological neurons, respectively. However, we still need to figure out how to reduce the energy-consumption in the peripheral circuit for driving these devices. Device-circuit co-designs will be necessary to address problems at the system level. Overall, this thesis shows the promise of magnetic-based computing, in particular DW-Logic and domain wall based neural network.

6.2 Outlook

Future work can address the issues we encounter in designing an electrically readable analog synaptic/activation function evaluator. This will require modifying the pinning field at the edges of the tunnel junctions. One possible approach could be shaping the corners of the reference layer as soft edges instead of abrupt termination. Micromagnetic modeling will be helpful in predicting the stray magnetic field from such reference layers.

In the system level, it is still an open question which type of devices (i.e. analog devices with single domain wall or discretized devices with multiple domains) will be technologically beneficial in terms of latency, energy consumption and complexity of peripheral circuit design. However, whether analog or discretized, domain wall devices can be integrated in the back-end-of-the-line (BEOL) of CMOS technologies between the interconnect levels as cross point architecture. Figure 6.1 shows the circuit implementations for cross point architecture suitable for neural network.
Figure 6.1 (a) Circuit symbols and models for the synaptic MTJ and thresholding MTJ. (b) Crosspoint array using synaptic MTJs and thresholding MTJs as analog logic and memory elements [6].

Figure 6.2 Integrated neural accelerators with magnetic domain wall based synaptic and activation function generators.
Figure 6.2 shows schematics of an approach for integration the devices with CMOS technologies. The $5 \times 5$ crossbars with a synaptic weight generator in each crosspoint and an activation function generator at the end of each column. The connections with the selector transistors are designed according to the architecture demonstrated in Figure 6.1. The synaptic and the activation function generators are between the interconnect levels in BEOL of CMOS system. The transistors in BEOL work as the selectors for the synaptic and activation function generators.

In summary, it is an exciting time for magnetic domain wall devices to shift gear from memory applications to logic and more importantly to logic-in-memory implementations. Novel magnetic materials, deep understanding of physics of these materials in conjunction with device-system co-design are the pre-requisites for enabling the fast and energy-efficient computational systems.
References


