Three-dimensional Device and Circuit Architectures:

New Systems with New Nanotechnologies

by

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Bachelor of Applied Science, University of Waterloo (2017)

Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2019

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Chair, Department Committee on Graduate Students
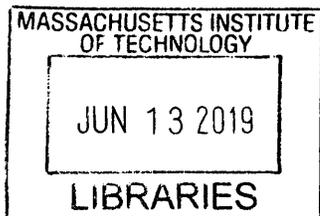
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Abstract

Physical scaling of silicon-based field-effect transistors (FETs) has been a major driving force to improve computing energy efficiency (quantified by the energy-delay product, EDP, the product of energy consumption and circuit delay) for decades. However, continued silicon scaling is becoming increasingly challenging. This is motivating the search for beyond-silicon nanotechnologies, such as one-dimensional carbon nanotubes (CNTs) or two-dimensional nanomaterials such as transition metal dichalcogenides (TMDs). Yet simply relying on new materials alone is insufficient for realizing the next generation of energy-efficient computing. Rather, *coordinated advances* across the entire computing system stack are required, as their combined benefits are greater than the sum of their individual benefits. In this work, I illustrate how by combining multiple advances - from new nanomaterials to new device geometries to new circuit architectures – there is a feasible and exciting path towards realizing the next generation of energy efficiency for digital very-large-scale integrated (VLSI) systems.

As a case study, this thesis focuses on CNT-based electronics. I experimentally demonstrate that by leveraging this new nanomaterial, we can naturally realize CNT field-effect transistors (CNFETs) that take advantage of new device geometries (specifically, new three-dimensional (3D) stacked-channel transistor geometries), as well as new 3D integration schemes (specifically, 3D circuit architectures based on stacked-channel transistors and new schemes for monolithic 3D *heterogenous* integration of a wide range of technologies spanning silicon, III-V, and CNTs).
The key contributions of this thesis are the following:

1. We experimentally demonstrate, *DISC-FETs* (Dual Independent Stacked Channel Field-Effect Transistors), a new 3D transistor architecture naturally enabled by CNFETs low temperature processing requirements.

2. We use this new 3D transistor architecture to enable new 3D circuit layouts, providing a promising path for energy-and area-efficient very-large scaled integrated (VLSI) circuits.

3. We develop and experimentally realize *X3D*, a new paradigm for monolithic 3D heterogenous integration of a wide range of nanowire-based semiconductors (e.g. silicon, III-V, and CNTs), enabling new system design that leverages a range of technologies for a range of different functionality - *all within the same chip* (wide-bandgap III-Vs for power management, CNTs for energy efficiency, tailored bandgaps for specialized sensors or imagers, *etc.*).

4. We leverage X3D to experimentally realize digital logic spanning multiple vertical circuit layers and heterogeneous nanowire-based semiconductors.

Thesis Supervisor: Max Shulaker

Title: Emmanuel E. Landsman (1958) Career Development Assistant Professor of Electrical Engineering and Computer Science

Acknowledgements

I would also like to thank my thesis advisor Professor Max Shulaker for all of his mentorship and patience with me for the last two years at MIT. I am incredibly appreciative of the opportunity to work alongside him and the rest of the NOVELs group and I am very excited to see what is on the horizon for the entire team.

I am sincerely grateful to Dr. Samuel Fuller, Yosi Stein, Denis Murphy, and Susan Feindt of Analog Devices Inc. for their support and encouraging words.

I would like to acknowledge all students and staff members of Microsystems Technology Laboratories (MTL), where I performed the majority of my research.

Last, but not certainly not least, I would like to thank my everyone back home in Brampton, Ontario, Canada. Thank you to Ajitpal Singh Chattha, Jagtar Singh, and Varun Sharma for always picking up my calls on my way home. In particular, a big and heartfelt thank you to my parents Jaswinder Singh Kanhaiya and Amrit Kaur Kanhaiya as well as my late brother Manpreet Singh Kanhaiya for the truly unconditional love, support, and unadulterated guidance throughout my entire life. I dedicate this thesis to you.

Table of Contents

List of Illustrations

Permission

Part of this thesis has been reproduced with permission from P.S. Kanhaiya et al.:

1. Kanhaiya, S. Pritpal, Gage Hills, Dimitri A. Antoniadis, Max M. Shulaker, *"DISC-FETs: Dual Independent Stacked Channel Field-Effect Transistors"*. *IEEE Electron Device Letters* 39, no. 8 (2018): 1250-1253.

2. Kanhaiya, S. Pritpal, Yosi Stein, Wenjie Lu, Jesús A del Alamo, Max M. Shulaker *"X3D: Heterogeneous Monolithic 3D Integration of "X"(Arbitrary) Nanowires: Silicon, III-V, and Carbon Nanotubes"*. *IEEE Transactions on Nanotechnology* 18, (2019): 270-273.

Chapter 1: Introduction

1.1 Background

While progress with silicon-based FETs continues, alternative technologies are currently being explored. For example, emerging one-dimensional (1D) and two-dimensional (2D) semiconductors are exciting emerging nanomaterials, promising improved carrier transport and electrostatic control versus bulk semiconductor materials (such as silicon). Single-walled carbon nanotubes (SWCNTs, or CNTs), are one such promising 1D nanomaterial with excellent electrical, thermal and physical properties [Riichiro 1998, Wei 2009]. CNTs are essentially rolled up sheets of graphene forming nanocylinders made with a diameter of ~1 nm. Carbon nanotube field-effect transistors, CNFETs, are formed by multiple CNTs defining the channel whose conductance is modulated by a metal gate. Figure 1.1 shows the schematic of a CNFET. Gate and source/drain contacts are defined by traditional lithography techniques. Owing to their ultra-thin body thickness (~1 nm diameter of the CNT), CNFETs exhibit excellent electrostatic control and simultaneously high carrier transport [Hills 2015]. Due to these benefits, CNFETs are projected to achieve an order of magnitude benefit in energy-delay product (EDP) compared to silicon CMOS for digital VLSI circuits [Hills 2019]. Importantly, CNFETs can be fabricated at low processing temperatures (<400°)[a] [Shulaker 2013; Shulaker 2017; Patil 2009], and therefore naturally enable monolithic three-dimensional (3D) integration (whereby layers of circuits are fabricated sequentially and directly vertically overlapping one-another, all over the same starting substrate [Shulaker 2017]. Such monolithic 3D integration enables new paradigms in designing heterogeneous nanosystems [Shulaker 2017], allowing fine-grained integration of sensing, logic and memory at the nanoscale.

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[a] While CNTs are synthesized at high temperature (>800 °C), they can be transferred to arbitrary substrates through either layer transfers or by solution-based processing at room temperature. This decouples the high-temperature processing of the CNTs from the monolithic 3D IC.
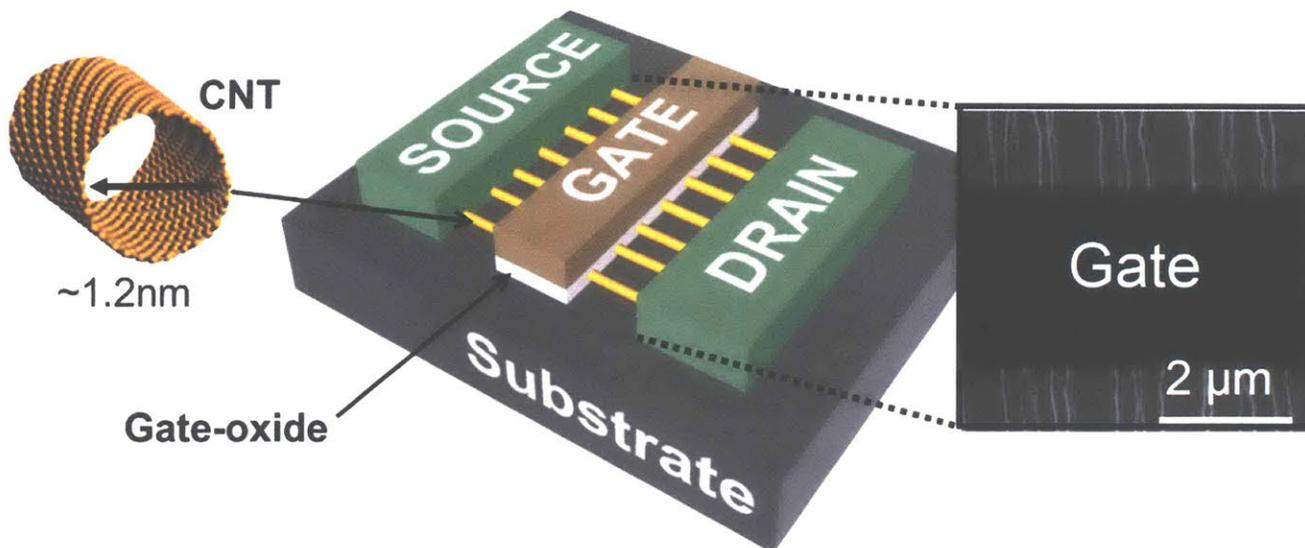
Figure 1.1 Schematic of carbon nanotube field-effect transistor (CNFET) with multiple parallel CNTs (nanocylinders made with atomically thin sheet of carbon atoms with diameter ~ 1 nm) bridging the source to drain contact.

Moreover, CNFETs are a rapidly maturing nanotechnology that has progressed substantially over the past decade. CNFETs are unique among emerging nanotechnologies as complete CNFET digital systems [Shulaker 2013, Shulaker 2014a], highly-scaled CNFETs with sub-10 nm channel lengths [Franklin 12], and complementary p- and n-type CNFETs operating at scaled supply voltages of <400 mV [Wei 2013] have all been experimentally shown.

1.2 Contributions

In this thesis, we focus on leveraging CNFETs low temperature processing requirements to (1) enable new 3D device architectures to, in turn, realize new 3D circuit layouts, and to (2) experimentally demonstrate a new paradigm in monolithic 3D heterogeneous integration. To do so, this work spans a range of disciplines, from to material synthesis, to device engineering, to 3D circuit design. We demonstrate de-coupling the high temperature synthesis of nanowire-based semiconductors (e.g., Si, III-V, and/or CNTs) from the low temperature FET (< 250 °C) fabrication steps enables monolithic 3D integration whereby additional circuit and device layers can be fabricated on top of one another on the same starting substrate.

This work shows the following:

1) A new three-dimensional (3D) field-effect transistor (FET) architecture leveraging emerging nanomaterials: Dual Independent Stacked Channel FET (DISC-FET). DISC-FET is comprised of two FET channels vertically integrated on separate circuit layers separated by a shared gate. This gate modulates the conductance of both FET channels simultaneously, although the stacked channels are independent, i.e., n-type or p-type with separate source and drain terminals separately accessed via routing. This 3D FET architecture enables new opportunities for area-efficient 3D circuit layouts. The key to enabling DISC-FET is low temperature processing to avoid damaging lower-layer circuits during upper-layer circuit fabrication. As a case study, we use carbon nanotube (CNT) FETs (CNFETs) since they can be fabricated at low temperature (e.g., <250 °C). We demonstrate wafer-scale CMOS CNFET-based digital logic circuits: 2-input "not-or" (NOR2) logic gates designed using DISC-FETs with independent NMOS CNT channels below and PMOS CNT channels above a shared gate. This work highlights the potential of 3D integration not only for enabling new 3D system architectures, but also new 3D FET architectures and 3D circuit layouts.

2) We extend this idea of de-coupling the high temperature synthesis from the low temperature FET fabrication to other nanowire-based semiconductors. In particular, we demonstrate a new paradigm for monolithic three-dimensional (3D) integration: X3D, which enables a wide range of semiconductors – including silicon (Si), III-V, and nanotechnologies such as carbon nanotubes (CNTs) – to be heterogeneously integrated together in monolithic 3D integrated systems. Such flexible heterogeneous integration has potential for a wide range of applications, as each layer of monolithic X3D integrated circuits (ICs) can be customized for specific functionality (e.g., wide-bandgap III-V-based circuits for power management, CNT field-effect transistors (CNFETs) for energy-efficient computing, and tailored materials for custom sensors or imagers). As a case study, we experimentally demonstrate monolithic X3D ICs with 5 vertical circuit layers heterogeneously integrating 3 different semiconductors: Si junctionless nanowire field-effect transistors (JNFETs), III-V JNFETs, and CNFETs (also junctionless). The layers of monolithic X3D IC are, from bottom-to-top: Si p-JNFETs, n-CNFETs, Si n-JNFETs, p-CNFETs, and III-V n-JNFETs. Each layer is fabricated using an identical process flow for ease of integration. Importantly, we show that circuits fabricated

on each vertical layer are agnostic to subsequent monolithic X3D processing, experimentally demonstrating ability to interleave these "X" (arbitrary) semiconductors in arbitrary vertical ordering. As a final demonstration, we fabricate complementary digital logic circuits comprising different technologies that span multiple vertical circuit layers. This work demonstrates a new paradigm for ICs, allowing for flexible and customizable electronic systems.

1.3 Outline

Chapter 2 presents DISC-FETs as a new 3D FET architecture, whereby we leverage CNFETs as a case-study to experimentally realize wafer-scale CMOS DISC-FET-based digital logic. Chapter 3 extends the decoupling of high temperature synthesis and low temperature FET fabrication to experimentally realize a new paradigm for monolithic three-dimensional (3D) integration: X3D, which enables a wide range of semiconductors – including silicon (Si), III-V, and nanotechnologies such as carbon nanotubes (CNTs) – to be heterogeneously integrated together in monolithic 3D integrated systems. As a case study, we experimentally demonstrate monolithic X3D ICs with 5 vertical circuit layers heterogeneously integrating 3 different semiconductors: Si junctionless nanowire field-effect transistors (JNFETs), III-V JNFETs, and CNFETs (also junctionless).

Chapter 2: Dual Independent Stacked Channel Field-Effect Transistors (DISC-FETs)

2.1 Background

As physical and equivalent scaling of silicon CMOS grows increasingly challenging [Liebmann 2016, ITRS 2015, Gielen 2008, Kim 2010], alternative paths to improve energy efficiency of digital systems, e.g., by leveraging new materials, FETs, circuits, and architectures, are actively being pursued [Meindl 2003, Del Alamo 2011, Kang 2007, Chau 2007, Guisinger 2010]. Here, we present and experimentally demonstrate a 3D FET architecture: Dual Independent Stacked Channel Field-Effect Transistor (DISC-FET). As illustrated in Fig. 2.1, DISC-FET is a 3D FET architecture with a shared gate that controls two vertically overlapping FET channels physically located above and below the gate. DISC-FET has five terminals: source and drain for the lower-layer FET, source and drain for the upper-layer FET, and the shared gate. Due to the reduced footprint of two vertically overlapping channels, the 3D geometry of DISC-FETs enables new opportunities for area-efficient 3D circuit layouts [Antoniadis 1983, Mallik 2017].
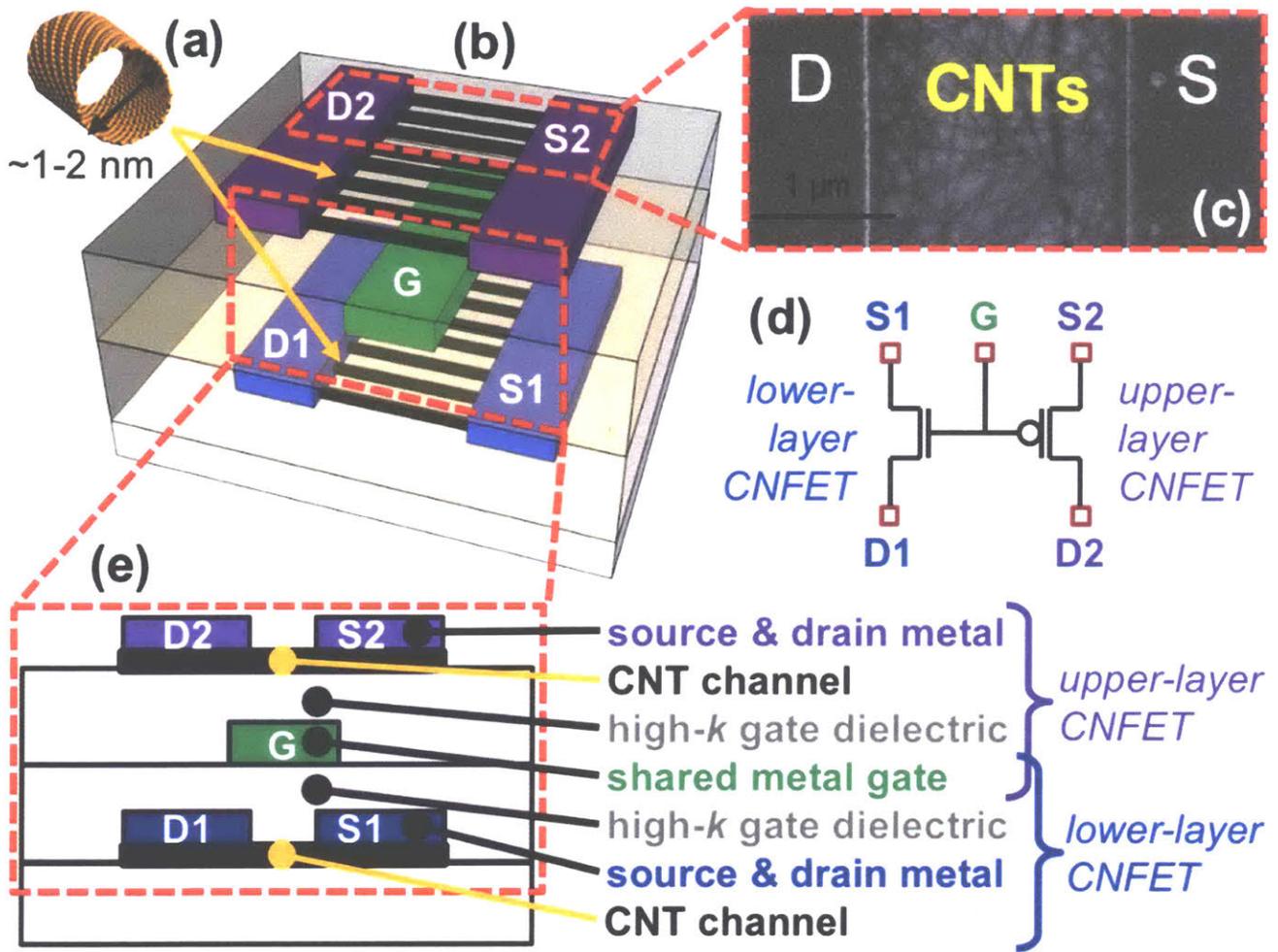
Fig. 2.1. CNFET-based DISC-FET. (a) Carbon nanotube (CNT). (b) DISC-FET 3D illustration, including source and drain for the lower-layer CNFET ("S1" and "D1"), source and drain for the upper-layer CNFET ("S2" and "D2"), and shared gate ("G"). (c) Scanning electron microscope (SEM) image of the upper-layer CNFET. (d) 5-terminal circuit schematic of DISC-FET, including 1 PMOS FET and 1 NMOS FET, although each CNFET can be either NMOS or PMOS. (e) Cross-section showing vertically integrated layers.

However, physically realizing DISC-FETs poses inherent challenges for conventional silicon-based FETs: the fabrication of the upper FET channel must be low temperature (e.g., <400 °C) to avoid damaging the FETs and metal interconnects on the lower circuit layers [Shulaker 2017, Batude 2011]. To overcome this challenge, we leverage carbon nanotubes (CNTs) as the channel material for both the upper- and lower-layer FETs, since carbon nanotube FETs (CNFETs) can be fabricated at low processing temperatures (e.g., <250 °C, process flow in Sec. II [Shulaker 2013]), and so multiple layers of CNFETs can be built directly on top

of each other over the same starting substrate, with conventional back-end-of-line (BEOL) inter-layer vias (ILVs) to connect the vertical circuit layers [Shulaker 2017]. Moreover, CNFETs promise an order of magnitude improvement in energy delay product (EDP, a metric of energy efficiency) vs. silicon FETs for digital VLSI circuits [Wei 2009, Shulaker 2014]. Thus, this approach offers EDP benefits simultaneously with area-efficient 3D circuit layouts.

2.2 Stacked Channel Benefits

DISC-FET offers potential area benefits for technology node scaling by reducing the height of standard library cells with vertically overlapping NMOS and PMOS FETs as relative standard cell area is typically quantified by the product of the contact gate pitch (CGP), metal 1 pitch (MP), and number of metal routing tracks (T) [Yakimets 2017]. Despite reduced standard cell area = CGP*MP*T, however, overall area benefits may be limited by back-end-of-line interconnect routing, which should be the focus of future analysis. Additionally, since DISC-FET circuits involve new layouts, parasitics should be extracted for these circuits depending on their precise 3D circuit structure. Importantly, these parasitics will also include coupling capacitance between the upper and lower FET layers, which will be an important aspect of analyzing DISC-FET circuit performance for future analysis.

2.3 Experimental Demonstration: DISC-FET-based Inverters & NOR2 Logic Gates

To experimentally demonstrate 3D circuit layouts enabled by DISC-FETs, we fabricate CNFET-based static CMOS DISC-FET inverters (INV) and 2-input "not-or" (NOR2) digital logic gates. Schematics and scanning electron microscopy (SEM) images of fabricated circuits are in Fig. 2.2. As a demonstration, lower-layer CNFETs are NMOS, and upper-layer CNFETs are PMOS, although CNFETs on each layer can be independently designed to be either NMOS or PMOS. As shown in Fig. 2.2, upper- and lower-layer CNFETs are vertically overlapping and are controlled by a shared gate.
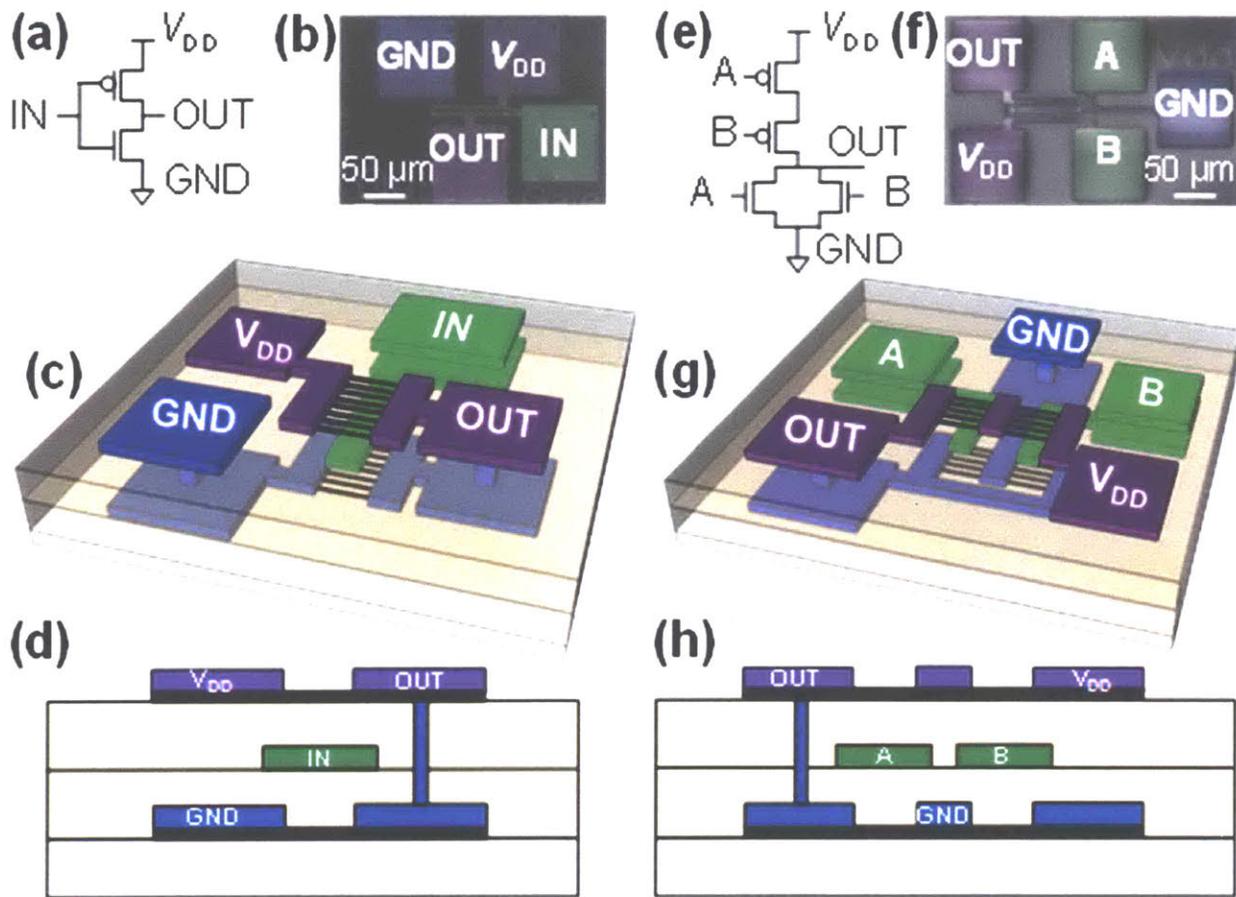
Fig. 2.2. Fabricated CNFET-based static CMOS DISC-FET digital logic gates. (a) Inverter schematic, (b) SEM, (c) 3D illustration, and (d) cross-section. (e) 2-input NOR schematic, (f) SEM, (g) 3D illustration, and (h) cross-section.

CNFET-level characterization results are shown in Fig. 4: drain current vs gate-to-source voltage (I_D vs. V_{GS}) and drain current vs. drain-to-source-voltage (I_D vs. V_{DS}) for both the upper-layer PMOS CNFET and lower-layer NMOS CNFET in a typical 5-terminal DISC-FET. The shared metal gate modulates the conductance for both CNFETs simultaneously.
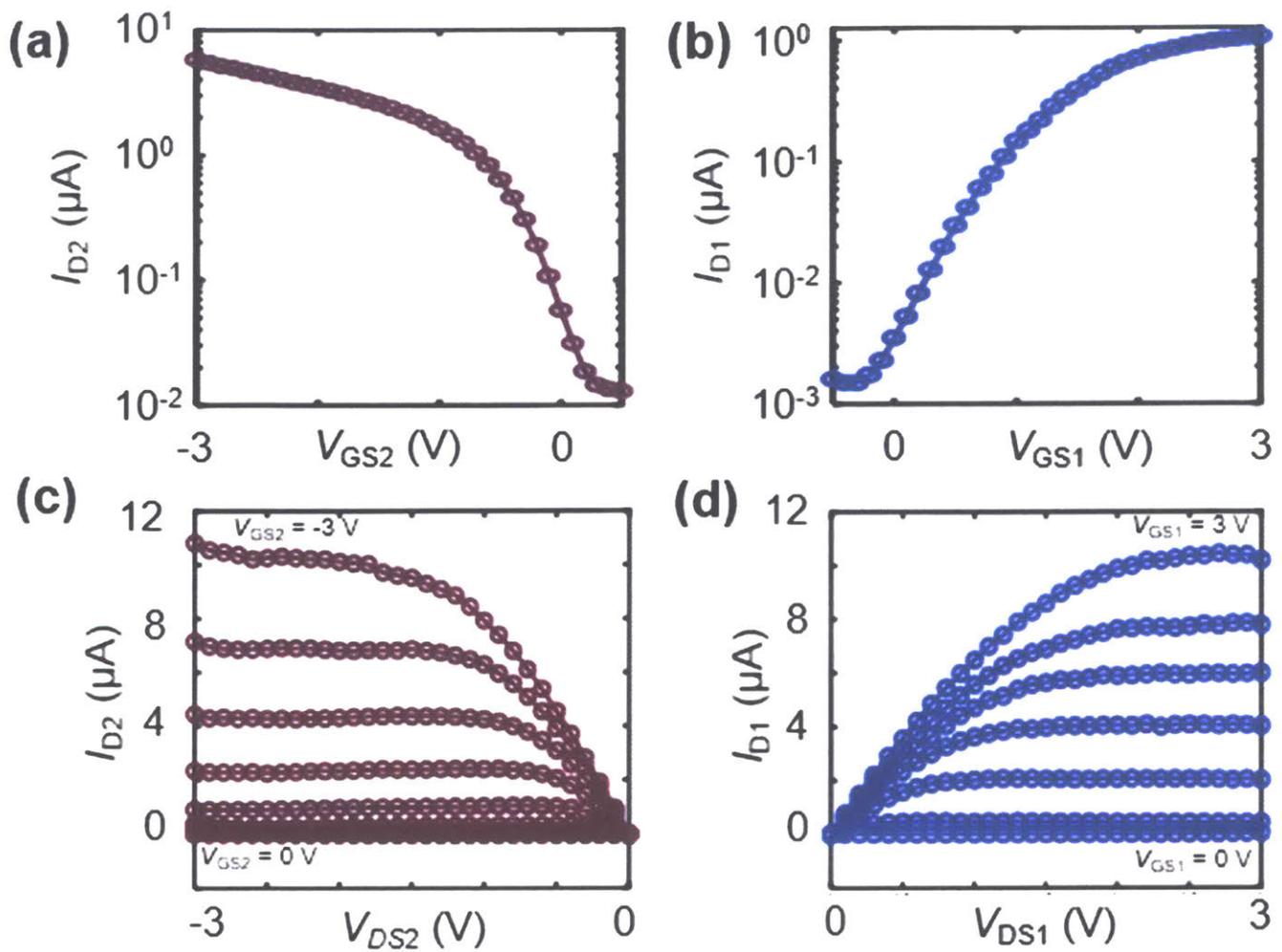
Fig. 2.3. I_D vs. V_{GS} characteristics of a typical DISC-FET (schematic in Fig. 2.1). The CNT density is ~10 CNTs/μm. (a,c) Upper-layer PMOS CNFET, with source and drain terminals S2 and D2. V_{GS2} is the gate-to-S2 voltage, V_{DS2} (-3 V in (a)) is the D2-to-S2 voltage, and I_{D2} is measured at D2. (b,d) Lower-layer NMOS CNFET, with source and drain terminals S1 and D1. V_{GS1} is the gate-to-S1 voltage, V_{DS1} (3 V in (b)) is the D1-to-S1, and I_{D1} is the current measured at D1. The channel length and width are ~2 μm and 36 μm respectively for all devices. The dimensions of the DISC-FET are set by the limitations of an academic fabrication facility; prior work has demonstrated the scalability of CNFETs to sub-10 nm channel lengths [Franklin 2012]. Measurements are performed at 25 ℃ in ambient. Importantly, the DISC-FET characteristics (such as drive current) can be improved by leveraging techniques that have been previously developed for optimizing CNFET device performance [Shulaker 2014, Shulaker 2015]. Future work should continue to explore new methods for further improving CNFET performance and minimizing variations. For instance, improving the interface between the CNTs and high-k gate dielectrics would minimize interface traps that have been implicated as a dominant source of CNFET hysteresis and threshold voltage variation [Park 2016].

To characterize each digital logic gate (INV and NOR2), we experimentally measure the output voltage, V_{OUT}, as a function of the input voltage for each input of that logic gate: INV has a single input (voltage: V_{IN}), while NOR2 has two inputs, A and B (voltages: $V_{IN,A}$ and $V_{IN,B}$). For INV, we refer to the relationship between V_{OUT} and V_{IN} as the voltage transfer curve (VTC), and we measure it two separate cases: 1) *forward sweep*: sweeping V_{IN} from 0 V to the supply voltage (V_{DD}), and 2) *reverse sweep*: sweeping V_{IN} from V_{DD} to 0 V. Ideally, the two cases would result in the exact same V_{OUT} vs. V_{IN} relationship; however, due to hysteresis, this is not necessarily the case (details below). Fig. 5a shows example INV forward and reverse sweep VTCs. For each NOR2 input (A and B), we measure the forward and reverse sweep VTCs while applying 0 V (digital logic "0") to the other input, so that the logic level of V_{OUT} is a function of the logic level of the input voltage. Fig. 5c shows example NOR2 forward and reverse sweep VTCs for input A (with $V_{IN,B} = 0$ V). Fig. 5c also shows that for $V_{IN,B} = V_{DD}$, V_{OUT} correctly corresponds to logical "0" for 0 V $\leq V_{IN,A} \leq V_{DD}$. For each VTC, we quantify the following performance metrics (illustrated in Fig. 2.4):

1)   *Output voltage "swing"* (V_{SWING}) – the difference between the maximum V_{OUT} and minimum V_{OUT} over all input voltages within the range 0 to V_{DD} (Fig. 2.4a).

2)   *Gain* – the maximum value of $-\Delta V_{OUT}/\Delta V_{IN}$ (Fig. 2.4b).

3)   *Hysteresis* ($V_{HYSTERESIS}$) – the difference in V_{IN} to achieve $V_{OUT} = V_{DD}/2$ for the forward and reverse VTCs (Fig. 2.4a).
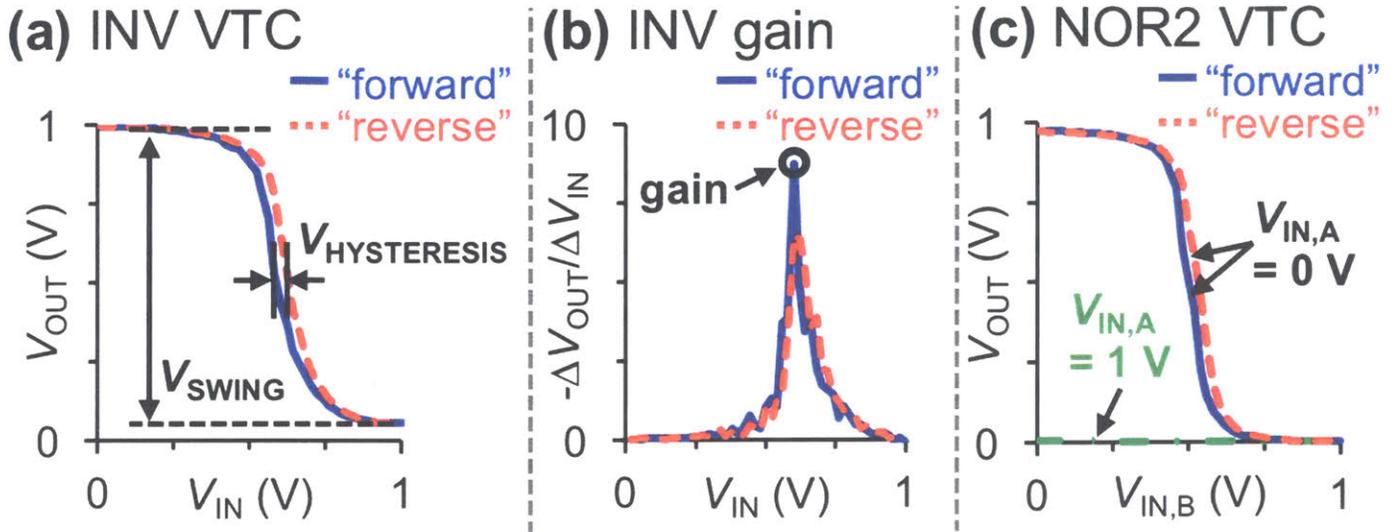
Fig. 2.4. VTCs (forward and reverse sweeps) of CNFET-based DISC-FET logic gates, illustrating performance metrics for characterization (V_{DD} = 1 V). (a) INV: V_{SWING} = 94% V_{DD}, $V_{HYSTERISIS}$ = 4% V_{DD}. (b) INV $-\Delta V_{OUT}/\Delta V_{IN}$ (for fixed increments: ΔV_{IN} = 20 mV): gain – 8.7. (c) NOR2 VTCs for input A.

To experimentally demonstrate wafer-scale design and fabrication of CNFET-based DISC-FETs, we quantify V_{SWING}, gain, and $V_{HYSTERESIS}$ across 500 CNFET-based static CMOS DISC-FET NOR2 gates, measured with V_{DD} = 1 V. The VTCs corresponding to inputs A and B are shown in Fig. 2.5a and Fig. 2.5b, respectively, with corresponding statistical distributions in Fig. 2.6 (reported V_{SWING} and gain correspond to the forward sweep VTCs). Averaged over 500 NOR2 gates, and including both inputs A and B, our experimentally measure results are as follows. Average V_{SWING}: μ_{SWING} = 94% V_{DD}, average gain: μ_{GAIN} = 6.3, and average $V_{HYSTERESIS}$, $\mu_{HYSTERESIS}$ = 2.3% V_{DD}.
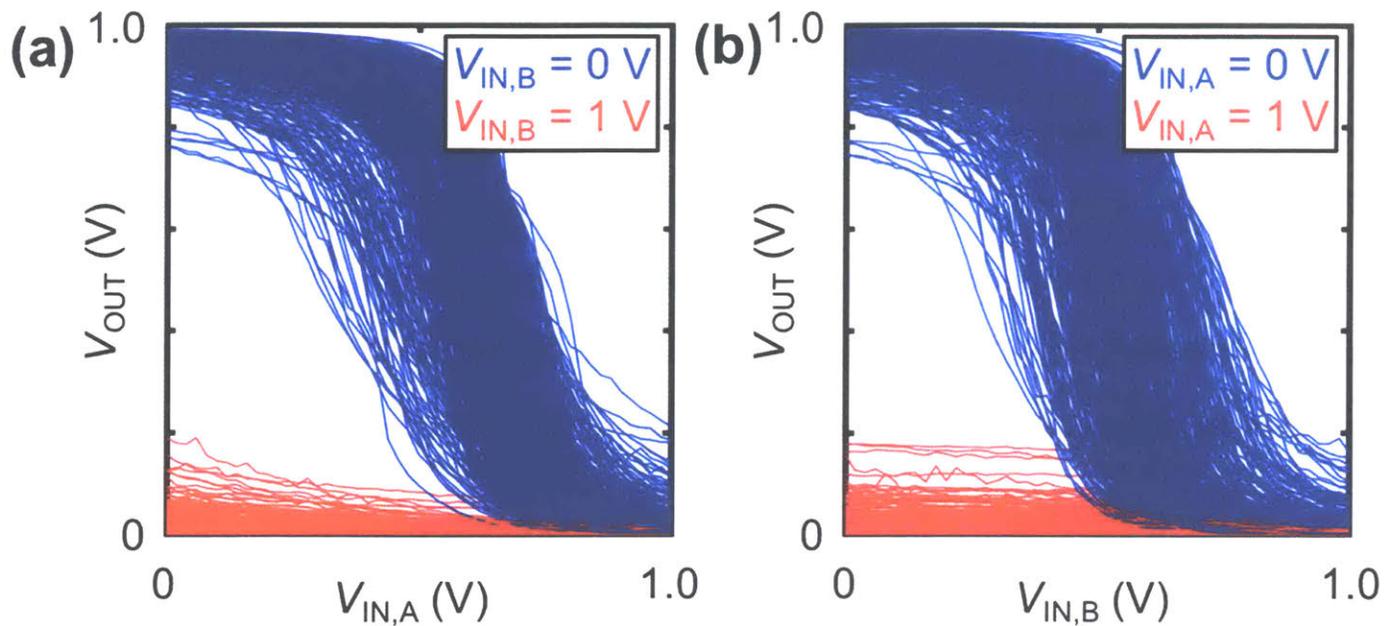
Fig. 2.5. Forward sweep VTCs of 500 CNFET-based DISC-FET NOR2 gates (NOR2 design shown in Fig. 2.2e-f). (a) V_{OUT} vs. $V_{IN,A}$. (b) V_{OUT} vs. $V_{IN,B}$.
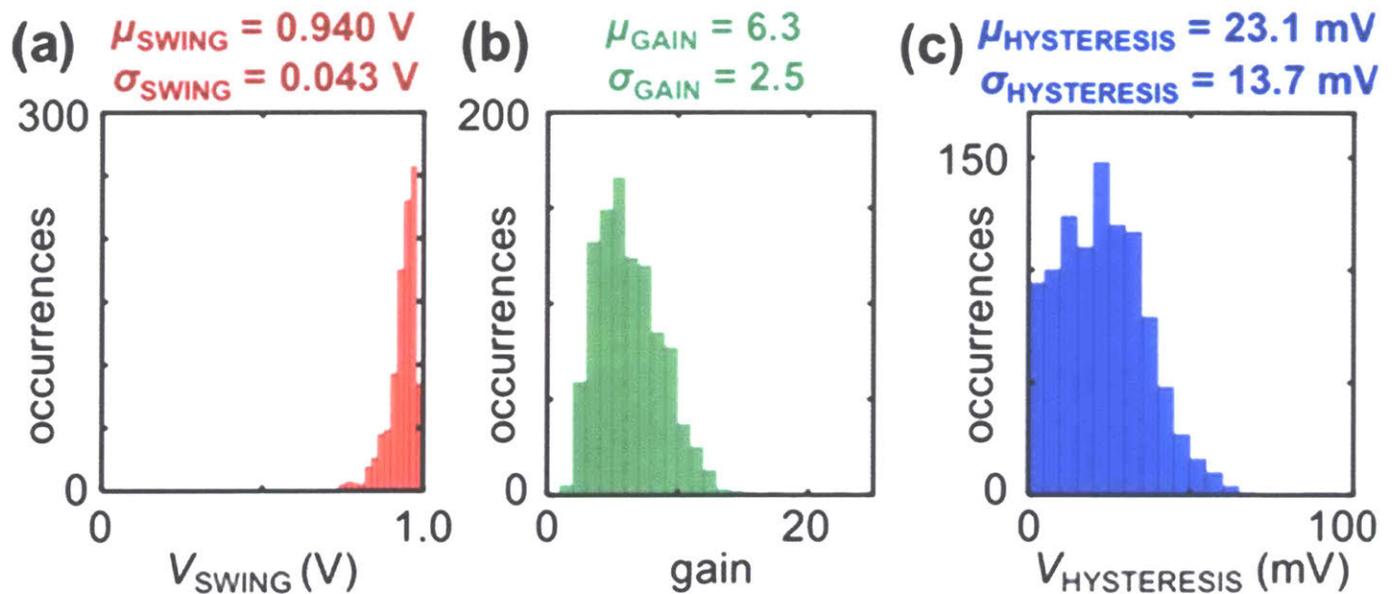
Fig. 2.6. Statistical distributions of V_{SWING}, gain, and $V_{HYSTERESIS}$, measured from 500 CNFET-based static CMOS DISC-FET NOR2 digital logic gates, extracted from the VTCs in Fig. 6. (a) V_{SWING} mean (μ_{SWING}) and standard deviation (σ_{SWING}). (b) gain mean (μ_{GAIN}) and standard deviation (σ_{GAIN}). (c) $V_{HYSTEREIS}$ mean ($\mu_{HYSTERESIS}$) and standard deviation ($\sigma_{HYSTERESIS}$). Variability is primarily attributed to interface traps at the CNT/ high-k dielectric interface, as well as the fact that the upper-layer PMOS CNFETs are not passivated and exposed to ambient.

19

2.4 Conclusion

We experimentally demonstrate DISC-FET, a 3D FET architecture, using CNFETs. Importantly, DISC-FETs are naturally enabled by CNFETs due to low temperature requirements to fabricate multiple layers of CNFETs directly on top of one another over the same starting substrate. CNFET-based DISC-FETs can be used leveraged to realize new 3D circuit layouts, e.g. for digital logic circuits, and are thus a promising path for creating future generations of energy- and area-efficient very-large-scale integrated circuits.

Chapter 3: X3D: Heterogeneous Monolithic 3D Integration

of "X" (Arbitrary) Nanowires

3.1 Background

As mentioned previously, as continued physical and equivalent scaling of silicon FETs yields diminishing returns, multiple alternative paths for improving the energy efficiency of digital VLSI circuits and systems are being pursued. On one hand, improved FETs fabricated with beyond-silicon technologies ranging from III-V compound semiconductors to emerging nanotechnologies such as CNFETs promise improved scalability and energy efficiency. On the other hand, new integration techniques, such as three-dimensional (3D) integrated circuits (ICs), promise new computing architectures and further energy efficiency benefits. Monolithic 3D integration, whereby multiple layers of circuits are fabricated directly over one-another on the same starting substrate (i.e., no wafer bonding required), enables nano-scale inter-layer vias (ILVs) to connect vertical layers of a 3D IC providing fine-grained and dense vertical connectivity between circuit layers [Vinet 2011, Shulaker 2014]. Such massive physical connectivity can translate to large increases in data bandwidth between vertical layers, which can improve energy efficiency by >100× for abundant-data applications [Aly 2015, Shulaker 2017].

Despite these promising directions, there are substantial challenges for realizing these future electronic systems. For instance, monolithic 3D integration requires that all processing on the upper layers must be low temperature (e.g., <400 °C), as higher temperatures damage lower-level FETs and destroy low-temperature back-end-of-line (BEOL) metal interconnects [Shulaker 2017]. As a result, many technologies, including silicon and beyond-silicon semiconductors (such as III-V compound semiconductors), are challenging to integrate in monolithic 3D systems, since they require high-temperature processing for both high-quality single-crystalline synthesis and high-temperature anneals (>1000 °C) for doping and junction formation in traditional FETs.

3.2 X3D Concept

Here, we present a new paradigm for electronic systems: X3D. X3D enables a wide-range of semiconductors, including conventional silicon, next-generation III-V compounds (as an example, in this work we use GaAs), and nanotechnologies such as CNTs to be heterogeneously integrated over the same starting substrate in a monolithic 3D IC. Thus, X3D combines the energy efficiency benefits of beyond-silicon devices, the benefits of monolithic 3D integration, and the flexibility of customizing different vertical 3D layers enabled by a wide-range of semiconductors. Importantly, this work is in stark contrast to previous demonstrations of monolithic 3D integration of heterogeneous technologies (silicon and CNTs [Shulaker 2014, Shulaker 2017]), as upper-layers of circuits were all constrained to CNTs; X3D enables arbitrary vertical interleaving of Si, III-Vs, CNTs, etc.

The key to X3D is using junctionless nanowire FETs (JNFETs) [Colinge 2010a] in which: (1) the high temperature synthesis and uniform doping of each "X" semiconducting channel is performed on a donor substrate (i.e., which is separate from the substrate used for circuit fabrication), (2) the "X" nanowires (NWs, including CNTs and Si-/III-V-based NWs) are released in different solutions, and (3) for any circuit layer in the monolithic X3D IC, "X" NWs are deposited on the substrate using a low-temperature process (e.g., solution-based processing), followed by transistor fabrication (all <200 °C). Importantly, there are no additional high-temperature processing steps (e.g., doping) on the target substrate (X3D IC).

3.3 Experimental Results

As an experimental demonstration of X3D, we fabricate a monolithic X3D IC with 5 vertical circuit layers comprising 3 different semiconductors (Si, III-V, and CNTs). As shown in Fig. 3.1, it comprises (from bottom to top): Si p-JNFETs, n-CNFETs, Si n-JNFETs, p-CNFETs, and III-V n-JNFETs. The ordering of the layers is chosen to explicitly demonstrate the ability to arbitrarily stack these technologies within the monolithic X3D IC: silicon (layer 3) is integrated over silicon (layer 1), CNT (layer 4) is integrated over CNT (layer 2), CNT (layer 2) is integrated over silicon (layer 1), silicon (layer 3) is integrated over CNT (layer 2), and III-

V is integrated over both silicon (layers 1 and 3) and CNT (layers 2 and 4). The FETs shown in Fig. 3.1a are staggered for visibility; FETs can be vertically overlapping as well. To characterize the monolithic X3D process, we fabricate and measure the JNFETs across every layer of the monolithic X3D IC. To validate that the JNFETs can be vertically interleaved on arbitrary circuit layers, we measure the JNFETs on each layer immediately after fabrication of that layer, as well as after the entire subsequent monolithic X3D processing (Fig. 3.2). As shown in Fig. 2c, the JNFETs on all layers exhibit negligible performance change due to subsequent monolithic X3D processing; the on-state drive current (I_{ON}, i.e., measured drain current when $|V_{GS}| = |V_{DS}| = V_{DD}$) of each vertical layer immediately after fabrication and post subsequent monolithic X3D processing exhibit insignificant change (we fail to reject the null hypothesis that the average I_{ON} are the same before and after monolithic X3D fabrication, using the two samples t-test for difference in mean with 95% confidence [Norušis 2006]).
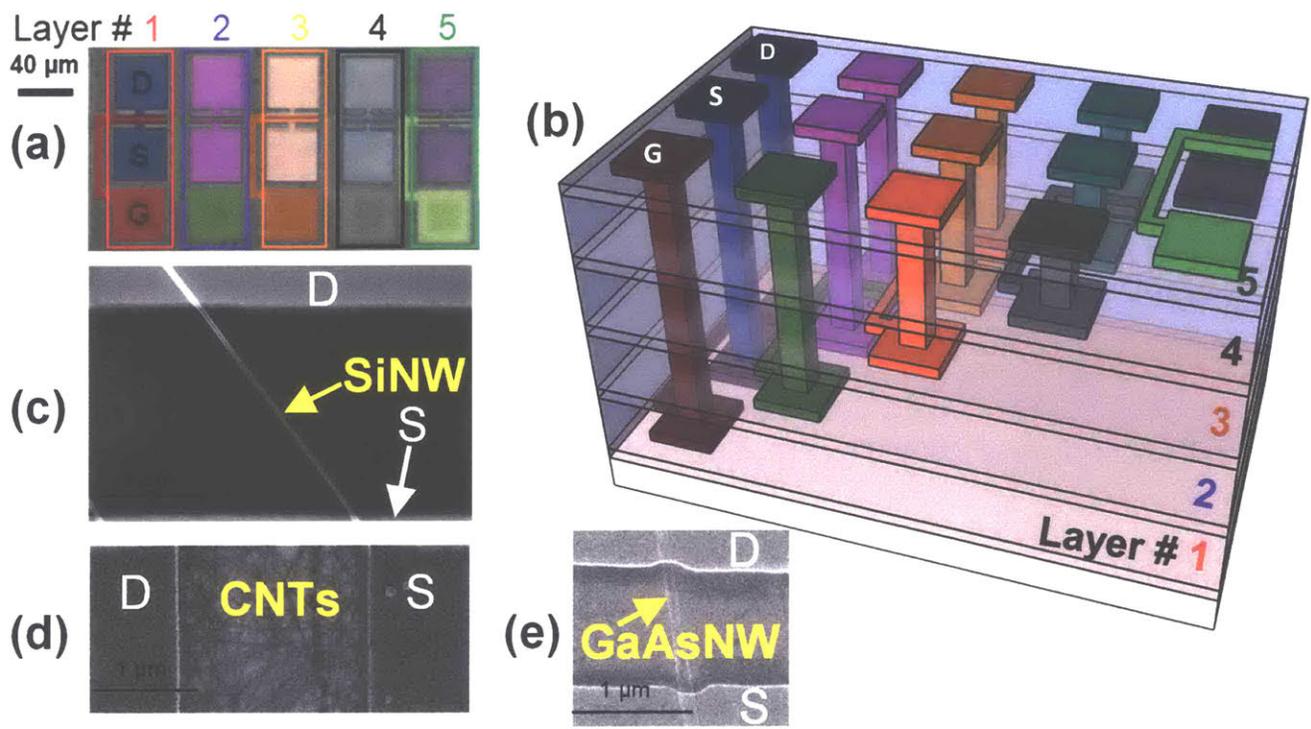
Fig. 3.1. (a) Optical microscopy image of devices fabricated on each layer of the 5-layer X3D chip, with their respective source, drain, and gate metals highlighted. (b) 3D schematic of fabricated 5-layer X3D stack. SEMs of (c) SiNWs ($d \sim$ 20 nm), (d) CNTs ($d \sim 1$ nm), and (e) GaAsNWs ($d \sim 100$ nm) bridging the source and drain contacts. All FETs are fabricated with a top-gate geometry, except for the p-CNFETs (layer 4) which use a local bottom-gate geometry. All FETs have 40 nm source and drain contacts (Pt), leverage a high-k metal gate stack (25 nm high-k HfO_x gate dielectric, 20 nm Pt gate). The inter-layer dielectrics (ILDs) are all 100 nm SiO_2.
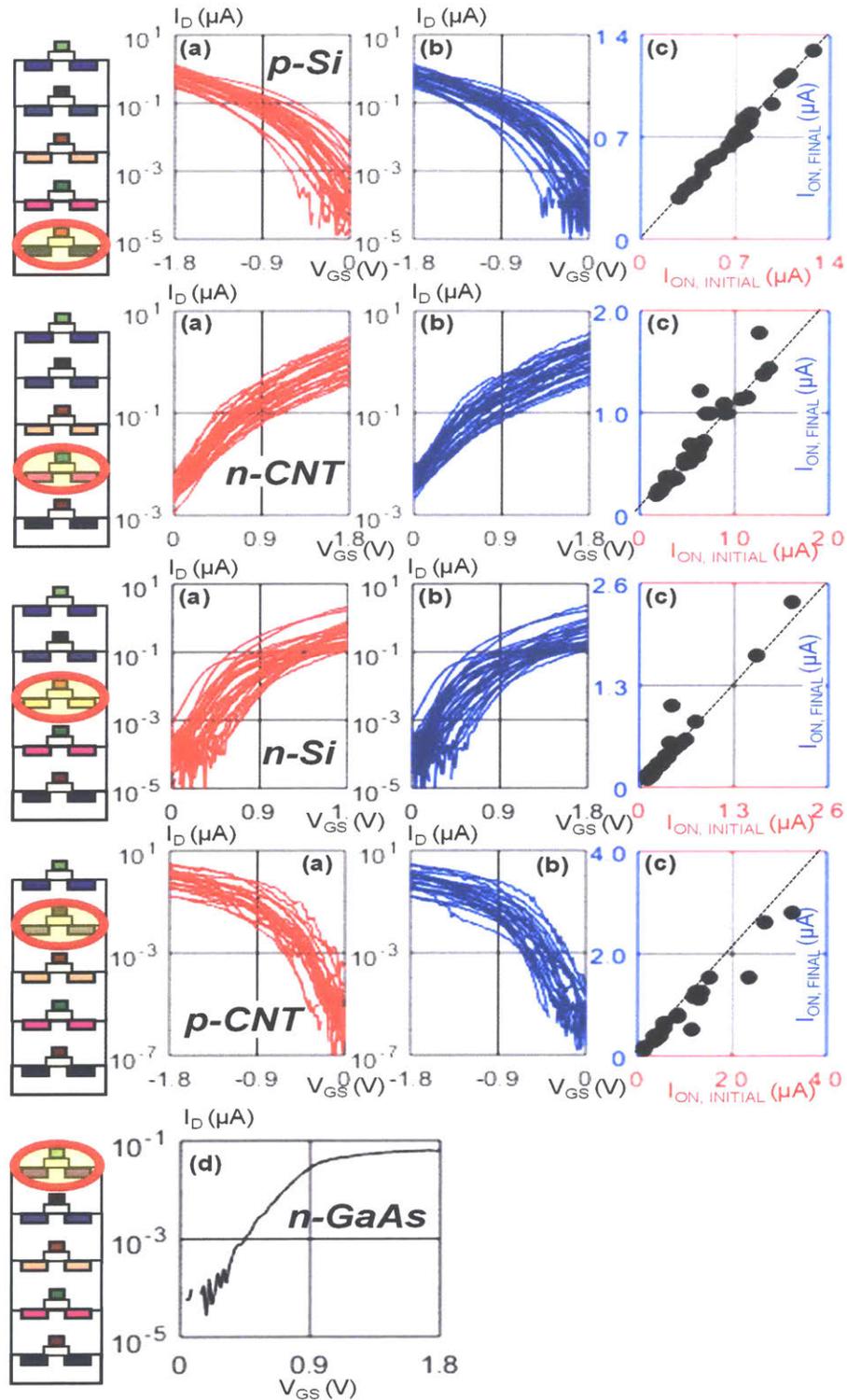
Fig. 3.2: $I_D - V_{GS}$ characteristics of first four layers of devices (30 FETs per layer). (a) measured immediately after fabrication, and (b) measured again after monolithic X3D processing. (c) I_{ON} pre- and post- monolithic X3D processing shows negligible change resulting from X3D processing. The line with slope of 1 is the ideal case. Sub-threshold slopes ~100-200 mV/decade. (d) $I_D - V_{GS}$ characteristic of a typical GaAs n-JNFET on the fifth layer of the monolithic X3D IC.

Post- monolithic X3D processing I_D-V_{GS} are not shown as this is the final layer of the monolithic X3D stack. Si- and GaAs-based JNFETs have ~1-2 NWs per JNFET, while CNT-based JNFETs have ~30 CNTs/μm.

As a demonstration, we experimentally show functional complementary digital logic circuits spanning multiple vertical circuit layers and semiconductor technologies: between Si p-JNFETs (layer 1) and n-CNFETs (layer 2), and between p-CNFETs (layer 4) and Si n-JNFETs (layer 3) (Fig. 3.3). As shown in Fig. 3.3a, the source terminals of layers 1 and 2 are connected using ILVs to define the output terminal for inverter 1, and the gate terminals of layers 1 and 2 are likewise connected through ILVs to define the input terminal. The same case holds for inverter 2 spanning layers 3 and 4. Correct inverter logic functionality is illustrated in Fig. 3c when operating at a supply voltage of 1.8 V_{DD}, where logical low input signals return a logical high output and logical high input signals return a logical low output.
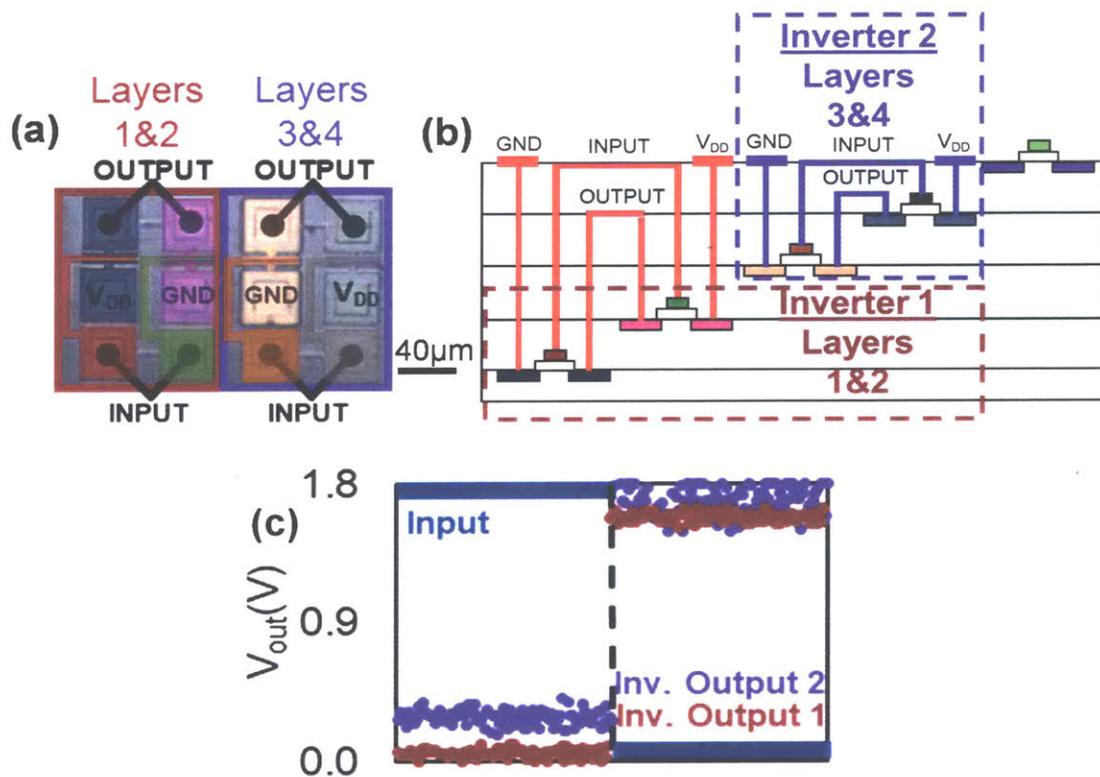
Figure 3.3: (a) Optical microscopy image of two fabricated monolithic X3D CMOS inverters, with inverter 1 spanning layer 1 (Si p-JNFET) and layer 2 (n-CNFET), and inverter 2 spanning layer 3 (Si n-JNFET) and layer 4 (p-CNFET). (b) Cross-sectional schematic of monolithic X3D inverters. (c) Output voltages given inputs toggled between 0 V and V_{DD} (1.8 V).

3.4 Conclusion

This work demonstrates X3D, a new paradigm for monolithic 3D integration, which enables heterogeneous integration of a wide range of nanowire-based semiconductors. With our first demonstration of X3D, we integrate three different technologies (silicon, CNTs, and III-Vs) spanning 5 vertically-interleaved layers, forming complementary digital logic. Importantly, X3D provides a framework that allows all layers to be fabricated with identical processing steps for ease-of-integration and allows arbitrary ordering of layers. While an example case-study, such flexible and customizable heterogeneous integration has potential for a wide range of applications. Each layer of monolithic X3D ICs can be customized for specific functionality; e.g., wide-bandgap III-Vs for power management, CNTs for energy efficient computing, and tailored bandgaps for specialized sensors or imagers. Thus, this work provides a new direction for future generations of electronic systems to grow in diversity and customization, integrating an increasingly wide range of new technologies within ICs.

Chapter 4: Concluding Remarks

Emerging nanotechnologies, such as CNTs, promise significant EDP benefits for digital VLSI design [Hills 2018]. Moreover, new integration techniques, such as three-dimensional (3D) integrated circuits (ICs), promise new computing architectures and further energy efficiency benefits. In this thesis, we demonstrate DISC-FET, a new 3D device architecture, to realize new 3D circuit layouts naturally enabled by CNFETs low temperature processing requirements. We extend the idea of decoupling the high temperature synthesis of nanowire-based semiconductors with their low temperature FET fabrication to experimentally realize X3D: monolithic 3D integration of heterogeneous nanotechnologies.

Thus, this work illustrates how coordinated advances across the stack – from nanofabrication to device geometries to digital VLSI circuit analysis – can be combined to realize benefits far greater than the sum of their individual benefits. While this work represents an important step forwards for CNT-based electronics, CNTs are solely a case study. The same approaches (and even same techniques and processes discussed in this thesis) are applicable to a wide range of emerging 1D and 2D nanomaterials. Therefore, while this work represents a major departure from conventional silicon CMOS, it represents an exciting path for realizing the next generation of energy-efficient computing systems. With continued progress, such technologies promise to enable future applications that will continue to benefit our lives for decades to come.

Appendix:

A.1: DISC-FET Process Flow

The process flow for a CNFET-based complementary (CMOS) DISC-FET, i.e., with an upper-layer PMOS CNFET, and lower-layer NMOS CNFET, is shown in Fig. A1.1. A solution of purified CNTs, sorted to achieve >99.9% semiconducting CNT (s-CNT) purity [Isosol, Seo 2013], is deposited over a starting SiO_2 substrate by submerging the substrate in the CNT solution at low temperature (25 °C). Importantly, this solution-based process is key for decoupling the high temperature CNT synthesis (>1,000 °C) from the final substrate used for DISC-FET fabrication [Shulaker 2017]. Source and drain metal contacts for the bottom channel are defined by lithographic patterning and depositing Ti/Pt (1 nm/ 40 nm) using physical vapor deposition (PVD). CNTs outside the channel region of the lower-layer CNFET are then etched using oxygen plasma [Patil 2007]. To fabricate the gate stack for DISC-FET – which comprises the high-k gate oxide for the lower-layer CNFET, the shared metal gate, and the high-k gate oxide for the upper-layer CNFET (as shown in Fig. 1e) – a 20 nm HfO_X film is first deposited through atomic layer deposition (ALD, at 200 °C) directly over the CNTs, followed by lithographic patterning and PVD of Ti/Pt (1 nm/ 20 nm) to form the metal gate. This HfO_X electrostatically dopes the lower-layer CNFET channel, forming an NMOS CNFET [Ha 2014]. The lithographic patterning and metal deposition for the metal gate is also used to form fine-grained ILVs to connect the lower-layer CNFET source and drain terminals to the upper-layer CNFETs [Shulaker 2017]. 20 nm of HfO_X is then deposited directly on top of the existing metal gate, using ALD, forming the gate oxide for the upper-layer CNFET. This is followed by a second CNT deposition, using the same low temperature solution-based processing described above. The source and drain for the upper-layer PMOS CNFET are then formed using the same process as the lower-layer CNFET source and drain (1 nm Ti/ 40 nm Pt). CNTs outside of the upper-layer channel region are etched using oxygen plasma, and subsequent BEOL routing can continue.
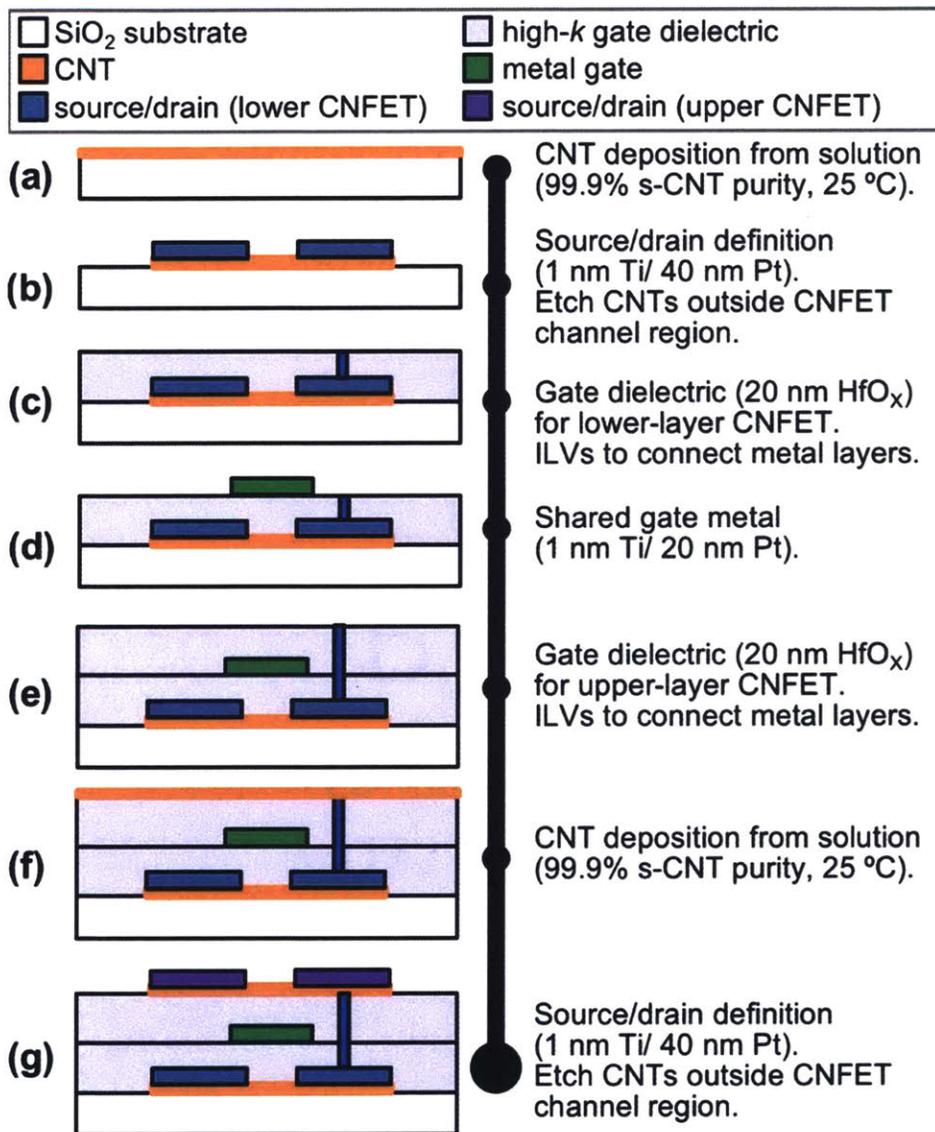
Figure A1.1: Process flow used to realize CNFET-based CMOS DISC-FETs.

A.2: X3D Process Flow

The process flow for X3D decouples the nanowires' high-temperature synthesis, doping, and annealing fabrication steps from the low-temperature FET fabrication steps (Fig. A.2.1). First, NW synthesis of "X" technology is performed on a donor substrate. NWs are then uniformly-doped either by introducing the dopants during NW synthesis (in-situ doping) or post-synthesis (through gas-phase doping or implantation). Following these high-temperature processing steps – which are all performed on the donor substrate (i.e., not on the monolithic X3D IC) – the NWs are released into solution using ultrasonication. To fabricate an "X" layer within a monolithic X3D IC, the desired NW solution is deposited on the target substrate. This solution processing is performed at room-temperature. For FET fabrication, the source, drain, and gate are lithographically patterned, and all NW segments outside FET channel regions are etched away and thus are removed from the circuit. Due to the decoupled NW synthesis and lack of junction formation once on the monolithic X3D IC, all processing on the monolithic X3D IC is <200 °C, rendering the process monolithic 3D compatible as well as silicon CMOS compatible. Following fabrication of each monolithic X3D layer, inter-layer dielectrics (ILDs) are deposited, and ILVs used for metal routing are defined. Importantly, these ILVs can be >1,000× denser versus through-silicon vias (TSVs) owing to monolithic 3D integration, providing dense connectivity between vertical layers of the monolithic X3D IC [Vinet 2011, Shulaker 2014].

(a)

(b)
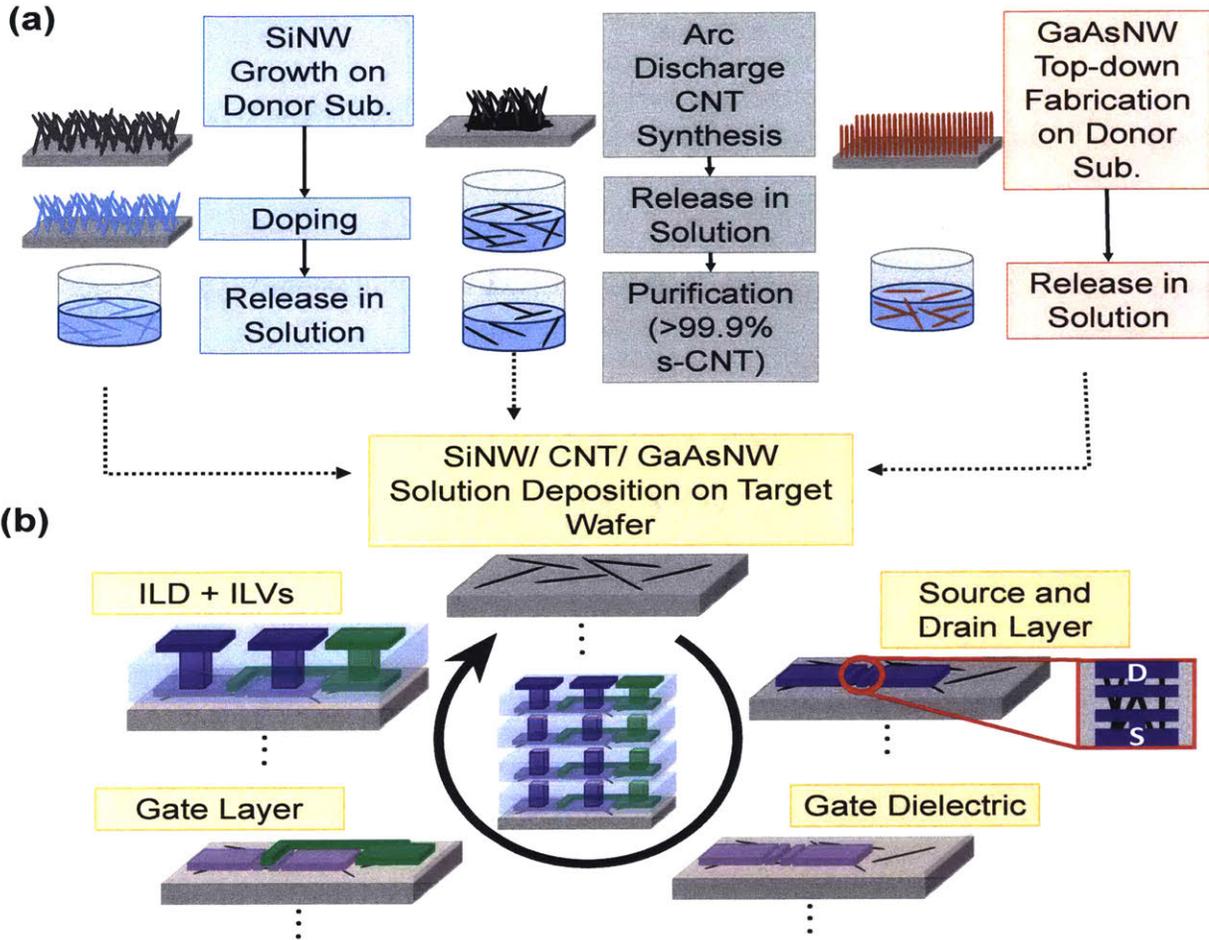
Figure A2.1: Process flow of X3D. (a) Schematic of NW and CNT synthesis and doping. (Left) SiNWs are synthesized and gas-phased doped post-synthesis on a donor substrate. Ultrasonication releases the SiNWs in IPA. (Middle) CNTs are grown via arc discharge, released in solution and sorted via density gradient centrifugation. (Right) GaAsNWs are synthesized through a top-down fabrication of a pre-doped GaAs substrate. Ultrasonication releases the GaAsNWs in IPA. (b) VLSI–scalable and CMOS compatible device fabrication flow of each X3D vertical layer. The "X" semiconductor solution is deposited, followed by PVD of source, drain, and gate (Ti/Pt) with ALD-deposited HfO_X as the high-k gate dielectric. Between each vertical layer, an inter-layer dielectric (PVD SiO_2) is deposited and ILVs (metal vias) are defined. These same steps are repeated for every layer in the X3D chip.

The use of NWs is essential, as it allows each of the "X" semiconductors to be released in solution for subsequent use in identical processing steps. JNFETs are essential as the entire NW can be uniformly doped; this enables the NWs to be placed in arbitrary locations across the substrate without requiring specific doping regions or precise alignment with the subsequent transistor formation (e.g., NPN aligning with source, gate, and drain). Moreover, the NWs and JNFETs are ideal pairings as the ultra-thin body thickness of the NWs are essential for JNFET electrostatic control [Colinge 2010a, Colinge 2010b].

The detailed NW synthesis flow is shown in Fig. A2.2. SiNWs are grown in a low-pressure chemical vapor deposition (LPCVD) system via a vapor-liquid-solid (VLS) method [Albuschies 2006]. CNTs are synthesized through arc discharge [Arnold 2005], and >99.9% semiconducting CNTs are sorted and released in solution via density gradient centrifugation [Sarker 2011, Iijima 1993]. GaAsNWs are defined through top-down fabrication using precision reactive ion etching [Lu 2017, Lin 2014]. To form either p-type or n-type JNFETs, the NWs are doped either before or during synthesis (e.g., GaAsNWs are defined in pre-doped GaAs substrate), through gas-phase doping post-synthesis (for SiNWs) [Ingole 2008, Cui, 2000], or through field-effect doping (for CNTs) [Ha 2014, Chen 2005, Lau 2018]. Post-doping, the NWs are deposited on the target layer of the monolithic X3D through solvent deposition. To do so, the NWs are dispersed in solvent (SiNWs and GaAsNWs in IPA, CNTs in toluene) through ultrasonication. The solution with suspended NWs is then drop-casted and dried on the monolithic X3D IC, depositing the NWs. While we leverage a simple drop-casting technique to deposit the NWs over the monolithic X3D IC for ease of integration, a range of techniques have demonstrated aligned and dense NW deposition from solution [Assad 2012, Yu 2007, Yao 2013, Li 2015, Cao 2013]. Once the doped NWs are deposited on the substrate, the JNFETs to form the circuit on that layer of the monolithic X3D IC are defined. The source, gate, and drain (~1 nm titanium / ~30 nm platinum) are lithographically patterned, while the high-k gate dielectric (~25 nm HfOx) is ALD-deposited (all processing <200 °C).
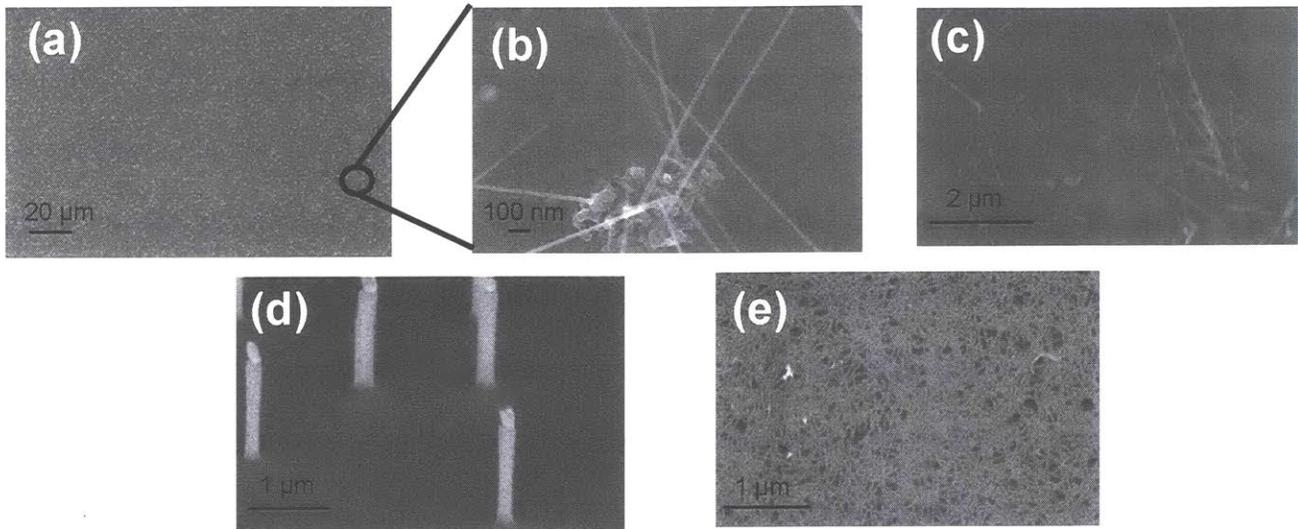
Figure A2.2: SEMs of donor and target substrates. (a-b) single-crystalline SiNWs on donor. (c) SiNWs deposited over the target X3D substrate. (d) GaAsNWs on donor. GaAsNWs are etched by ICP-RIE into an n-doped GaAs substrate. (e) CNTs deposited over the target X3D substrate.

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