SHARC: Self-Healing Analog with RRAM and CNFETs

by

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Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

Next-generation applications require processing on massive amount of data in real-time, exceeding the capabilities of electronic systems today. This has spurred research in a wide-range of areas: from new devices to replace silicon-based field-effect transistors (FETs) to new circuit and system architectures with fine-grained and dense integration of logic and memory. However, isolated improvements in just one area is insufficient. Rather, enabling these next-generation applications will require combining benefits across all levels of the computing stack: leveraging new devices to realize new circuits and architectures. For instance, carbon nanotube (CNT) field-effect transistors (CNFETs) for logic and Resistive Random-Access Memory (RRAM) for memory are two promising emerging nanotechnologies for energy-efficient electronics. However, CNFETs suffer from inherent imperfections (such as of metallic CNTs, m-CNTs), which have prohibited realizing large-scale CNFET circuits in the past. This work proposes a circuit design technique that integrates and combines the benefits of both CNFETs with RRAM to realize three-dimensional (3D) circuits that are immune to m-CNTs. Leveraging this technique, we show the first experimental demonstration of CNFET-based analog mixed-signal circuits.

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1. Chapter 1 Introduction

1.1 Background and Motivation

Physical and equivalent scaling of silicon complementary metal-oxide semiconductor (CMOS) technology has been a major driving force for improving computing energy efficiency for decades. This progress has had dramatic impact in all of our lives: from enabling self-driving cars to genome sequencing to the "internet of-everything" (IOE). Yet as these applications demand increasingly energy-efficient computing, progress in computing is coming to an abrupt halt. Continued scaling of silicon-based FETs is growing increasingly challenging, and the benefits afforded by scaling (*e.g.*, Dennard Scaling [1],[2]) no longer follow their historical trends. Therefore, continuing with "business as usual" is insufficient – new innovation is required. As evolving today's technology is insufficient for meeting the computing demands of future applications [3], alternative approaches and technologies are being explored. For example, emerging one-dimensional (1D) and two-dimensional (2D) semiconductors are exciting emerging nanomaterials, promising improved carrier transport and electrostatic control versus bulk semiconductor materials (such as silicon). Single-walled carbon nanotubes (SWCNTs, or CNTs), are one such promising 1D nanomaterial with excellent electrical, thermal and physical properties [4]. CNTs are nanocylinders made of a single atomically-thin sheet of carbon atoms with a diameter of ~1 nm. Fig. 1.1 shows the schematic of a single CNT and a CNT FET (CNFET). To form a CNFET, multiple CNTs in parallel act as the channel, whose conductance is modulated by the gate. The gate stack uses a high-*k* gate dielectric with metal gate, and the gate, source, and drain contacts are defined by traditional lithography.

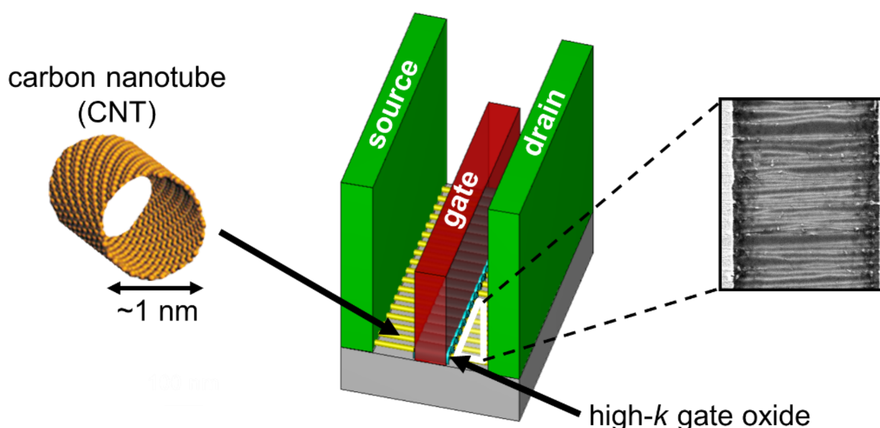


Fig. 1.1 Schematic of carbon nanotube field-effect transistor (CNFET) with multiple parallel CNTs (nanocylinders made with atomically thin sheet of carbon atoms with diameter ~ 1 nm) bridging the source to drain contact. Conductance of the CNTs are modulated by the gate to turn the transistor on or off

Owing to their ultra-thin body thickness (~1 nm diameter of the CNT), CNFETs exhibit excellent electrostatic control with simultaneously high carrier transport [5]. Due to these benefits, CNFETs are projected to achieve an order of magnitude benefit in energy-delay product (EDP, a metric of energy efficiency) compared to silicon CMOS FETs for digital VLSI circuits [6]. Moreover, CNFETs promise performance benefits for analog circuits as well, as an aggressively scaled CNFET at the 10-nm technology node can still achieve high intrinsic gain; as illustrated in Fig. 1.2, while silicon FET intrinsic gain degrades substantially with technology node scaling, a 10-nm technology node CNFET is projected to achieve instrinic gain equivalent to a >1 µm technology node silicon FET. This enables analog and digital circuits to be implemented in the same aggressive node without scarifying circuit performance. Thus, CNFET technology is ideal for energy-efficient analog mixed-signal systems. Additionally, CNFETs can be fabricated at low processing temperatures (<400°C) [7], [8], and therefore naturally enable monolithic three-dimensional (3D) integration (whereby layers of circuits are fabricated sequentially and directly vertically overlapping one another, all over the same starting substrate) [7]. Such monolithic 3D integration enables new paradigms in designing heterogeneous nano-systems [7], allowing fine-grained integration of sensing, logic and memory at the nanoscale.

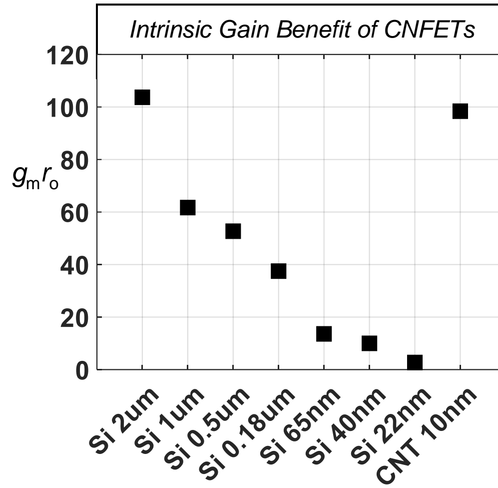


Fig. 1.2 . Intrinsic gain ($gm\ r_o$) of silicon versus CNFET. (The intrinsic gain is extracted from circuit simulations (Cadence Spectre®) using commercial process design kits (PDKs) for silicon CMOS, and using an experimentally calibrated compact model for CNFETs (calibrated using CNFETs with sub-10 nm channel length) [9])

Despite these benefits, the reported system level demonstrations using CNFET technology have been primarily limited to PMOS-only digital logic implementations such as 3D Nano System (which demonstrated sensing, computing, and memory integrated all on the same chip) [7], and a hyper-dimensional computing case study exploiting CNFETs and RRAM [10]. In addition, all reported CNFET CMOS demonstrations have been limited to only individual devices, small-scale circuits, or digital logic. However, no CNFET CMOS analog circuitry – a critical component of electronic systems for applications ranging from sensor interfaces to communication systems front-end to peripheral memory circuitry – has ever been reported. Major technical challenges have prohibited realizing CNFET CMOS analog circuits, which is the focus of this work.

1.2 Contributions

In this thesis, we focus on realizing the first CNFET analog mixed-signal circuits. To do so, this work analyses and overcomes one of the major obstacles facing CNFET analog circuits: metallic CNTs (m-CNTs). Specifically, we propose and experimentally validate a new circuit design technique that leverages the unique 3D heterogeneous integration capability of CNFETs with resistive RAM (RRAM) to overcome this challenge. This work shows the following:

(1) A new circuit design technique that enables CNFET circuits to "self-heal" in the presence of m-CNTs. This technique, name SHARC (Self-Healing Analog with RRAM and CNFETs) is non-volatile and can scale to any arbitrary circuit (*e.g.*, is wafer-scalable and VLSI compatible).

(2) Leveraging SHARC, we show the first functional experimental demonstration of CNFET mixed-signal circuits such as 4-bit capacitive DAC, and 4-bit SAR ADC. These circuits are the most advanced and largest CNFET CMOS circuits reported to date.

1.3 Thesis Organization

Chapter 2 provides an overview and thorough analysis of how metallic CNTs (m-CNTs) pose a major obstacle to CNFET analog and mixed-signal circuits. Chapter 3 presents SHARC, the design technique developed to overcome m-CNTs, and illustrates how to apply SHARC on multiple different circuits. Chapter 4 shows the fabrication process flow and the first experimental demonstration of CNFET CMOS circuits leveraging SHARC. Chapter 5 concludes the key contributions of this thesis and presents future research directions.

2. Chapter 2 Metallic CNTs: Impact on analog mixed-signal circuits

In this chapter, we discuss the major inherent CNT imperfection of metallic CNTs and provide an in-depth study on their impact on analog and digital circuits and systems.

2.1 Metallic CNTs

Despite the energy efficiency and intrinsic gain benefits afforded by CNFETs, CNTs suffer from substantial inherent imperfections. CNTs can be either semiconducting or metallic, dictated by the diameter and chirality of the CNT. While semiconducting CNTs form an ideal FET channel, metallic CNTs have zero or near-zero bandgap and hence their conductivity cannot be controlled by the CNFET gate, leading to increased leakage current and potential incorrect logic functionality (details below, Fig. 2.1).

Unfortunately, every synthesis and ensemble of CNTs includes some percentage of m-CNTs. For instance, Fig. 2.2 shows CNFET I-V characteristics for 1000 PMOS devices and 1000 NMOS devices, where each CNFET contains ~10-100 individual CNTs in parallel as the FET channel. While the majority of CNFETs have on-current (I_{ON})/ off-current (I_{OFF}) ratios of >1,000, due to the random presence of metallic CNTs, a percentage of CNFETs have high leakage off-state current resulting in I_{ON}/I_{OFF} ratio of <10. Unfortunately, small I_{ON}/I_{OFF} ratio degrades circuit performance and can result in incorrect circuit functionality. Thus, m-CNTs reduces both the performance and yield of CNFET circuits and pose a major barrier towards realizing a future CNFET technology.

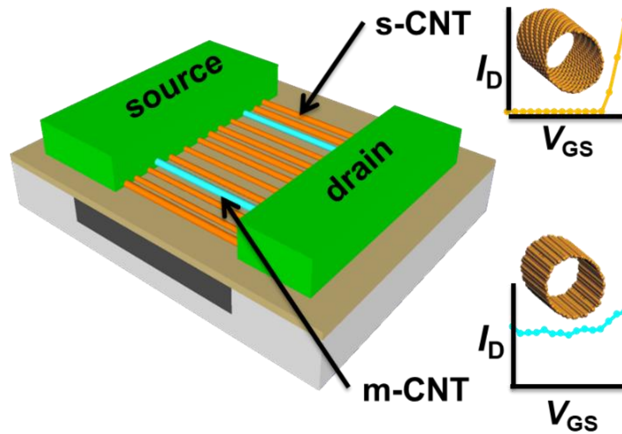


Fig. 2.1 CNFET with m-CNT in the channel resulting in excessive leakage current when $V_{GS} < V_{TH}$

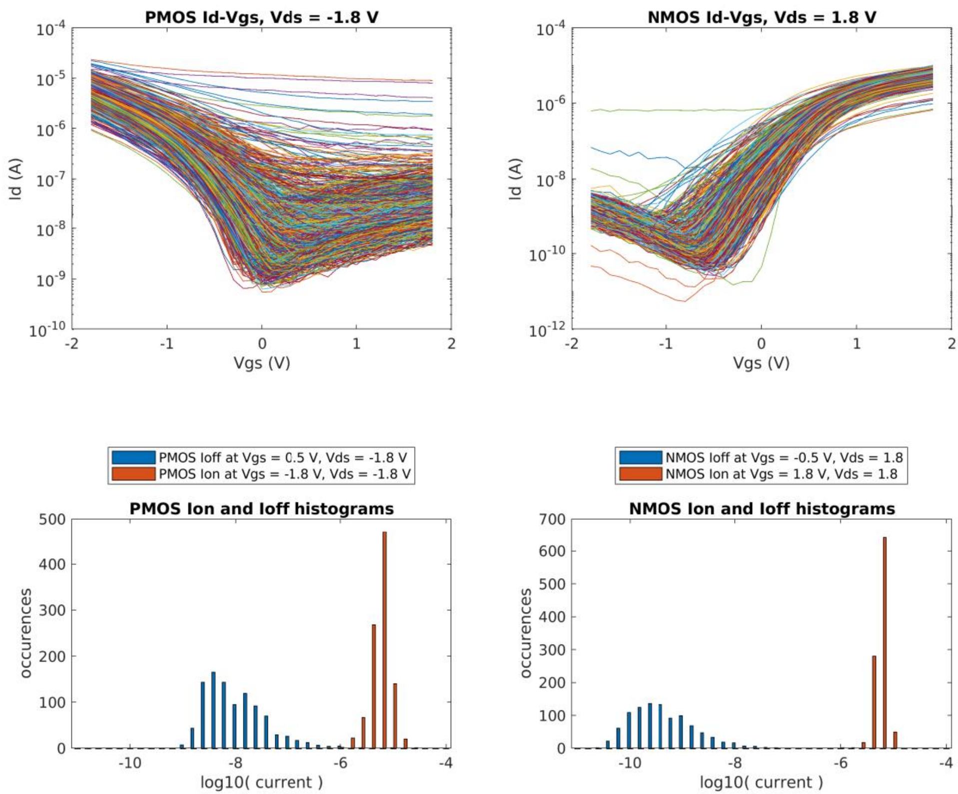


Fig. 2.2 Fabricated and measured CNFET I-V Characteristics for 1000 PMOS CNFETs, and 1000 NMOS CNFETs. While the majority of

CNFETs has $I_{ON}/I_{OFF} > 1,000$, due to the random presence of m-CNTs, a small percentage of CNFETs has increased leakage current and therefore severely degraded $I_{ON}/I_{OFF} < 10$.

While significant research has attempted to reduce or remove the percentage of m-CNTs, prior attempts have been inadequate. While digital VLSI systems require >99.99% s-CNTs, no technique today can realize this purity without sacrificing CNFET performance. For instance, techniques to optimize the CNT growth to preferentially grow s-CNTs [11], [12] typically yield 90%–96% s-CNTs, while recent work has demonstrates >99% s-CNTs on a small scale (<1 cm × 1 cm samples) [13]. Thus, while synthesizing 100% s-CNTs remains an open challenge, several techniques have been developed to remove m-CNTs post-synthesis. On one hand, solution-based CNT sorting (whereby CNTs are preferentially sorted after being dispersed in solution [14]) can preferentially remove m-CNTs, resulting in < 0.1% m-CNTs. Alternatively, electrical breakdown (whereby the gates of the CNFETs are biased to turn the s-CNTs off and a large source-drain bias is applied to "burn" the m-CNTs away, much like a fuse) can realize 99.99% s-CNTs [15]. However, the use of a high breakdown voltage requires the CNFETs to be fabricated with a thick gate dielectric to withstand the electrical breakdown process. This thicker gate dielectric impacts the threshold voltage (V_{TH}) and degrades key device metrics (such as inverse sub-threshold slope and drive current, I_{ON}). Therefore, no technique today can realize pure s-CNTs.

2.2 M-CNTs impact on circuit functionality and performance

As it is currently infeasible to realize 100% s-CNTs, it is critical to understand and analyse the impact any remain m-CNTs have on different circuits. In this section, we discuss the impact of m-CNTs on both digital and analog circuits in detail.

2.1.1 M-CNTs impact on digital logic

We start by analyzing the simplest digital logic gate, an inverter (illustrated in Fig. 2.3). To model an m-CNT, we use a resistor in parallel to the FET, where the resistor value decreases with number of m-CNTs in the device (we experimentally calibrate the value of the resistor for a single m-CNT to 25 kΩ). We use a resistor to model m-CNTs as their conductance is negligibly modified by the gate. Fig. 2.4b shows the impact m-CNTs can have on a single CNFET inverter: the presence of even a single m-CNTs degrades the logic levels of the inverter, in turn degrading the static noise margin. Moreover, as illustrated in Fig. 2.5, the static noise margin degradation increases as the number of m-CNTs within the CNFET increases. Due to the degraded static noise margin, if two cascaded CNFET logic gates containing m-CNTs are cascaded, it can result in incorrect logic functionality. For instance, Fig. 2.5 illustrates when a NAND logic gate with m-CNTs in the pull-up network (PUN) is cascaded to a NOR logic gate with m-CNTs in the pull-down network (PDN), the resulting logic is incorrect (i.e., there is zero static noise margin).

In addition to incorrect logic functionality, m-CNTs can provide a static current path between the supply rails which results in substantially increased static power consumption which increases the overall energy (total power= dynamic power + static power). Fig. 2.4a shows that the energy of a 32-bit commercial processor implemented at the 7-nm node can increase by 5× in the presence of m-CNTs (assuming 0.1% → 1% m-CNTs, see [16] for analysis details). We perform a full physical design of the processor and use experimentally calibrated models for 7-nm node CNFETs.

However, it is important to note that while m-CNTs always result in increased static power dissipation, it is possible to realize functional digital logic even in the presence of m-CNTs. As illustrated in Fig. 2.5, while three m-CNTs in both the NAND and NOR are required to result in incorrect logic functionality, if the NAND and NOR each had <3 m-CNTs,

the static noise margin would be >0 and thus would still realize correct logic functionality.

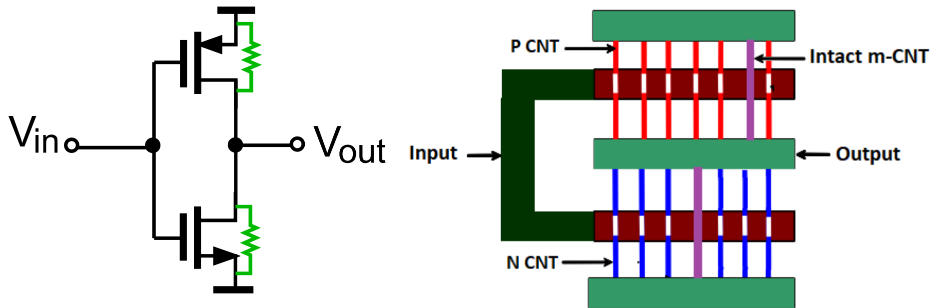


Fig. 2.3 Inverter with m-CNTs in both NMOS and PMOS

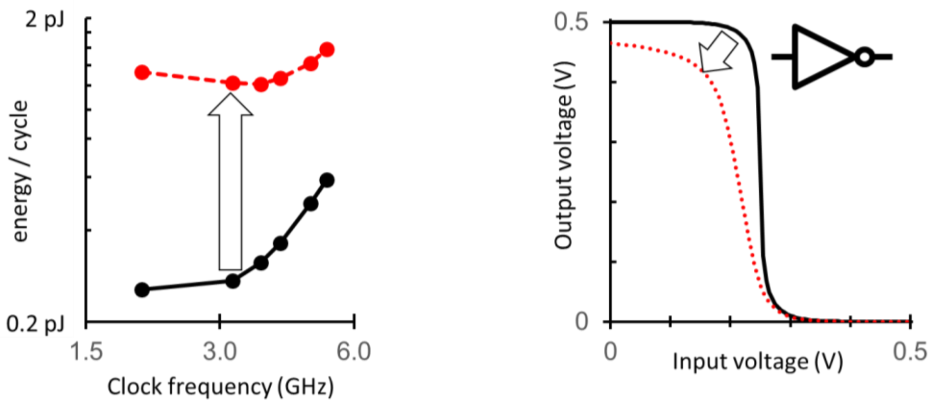


Fig. 2.4 Impact of m-CNT on digital circuits (a) CORTEX M0 processor in 7-nm node with m-CNTs (b) inverter transfer characteristics with m-CNTs in pull-down network

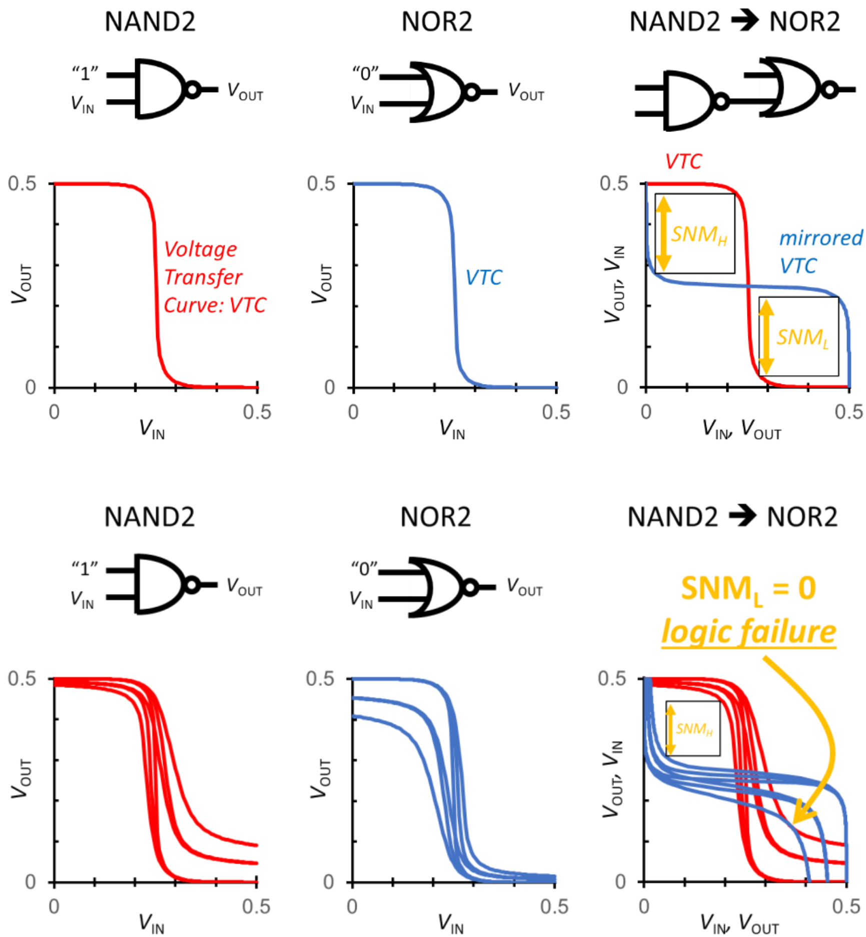


Fig. 2.5 Cascading logic gates with m-CNTs and impact on voltage transfer characteristics

2.1.2 M-CNT impact on analog circuits

While digital logic can still realize functional operation in the presence of m-CNTs, the impact of m-CNTs on analog circuitry can be much more severe. In contrast to digital logic where m-CNTs result in static noise margin degradation and static power dissipation, even a single m-CNT in an analog circuit can cause a wide variety of potentially fatal consequences, such as shifting the DC operating point or reducing the output impedance of a FET impacting an amplifiers performance. To analyse the impact of m-

CNTs in analog circuits, we initially analyze a differential amplifier, shown in Fig. 2.6. If all the CNFETs contain semiconducting CNTs, the amplifier achieves a gain of 34 dB and a bandwidth of 20MHz. When only a single m-CNT is introduced in the NMOS CNFET acting as the current source, there is a 2dB gain degradation (a gain degradation of 6%) while the bandwidth increases by 6% (GBW= (gm_n/C_L) ≈ constant). However, introducing a single m-CNT in the PMOS CNFET acting as the active load has a significantly more severe impact on the circuit. By changing the DC operating point of the circuit (the m-CNT causes the PMOS CNFET to operate in the triode region which reduces the PMOS CNFET Rout while simultaneously decreasing the circuit output impedance, $R_{out}=R_{outn}//R_{outp}//R_{m\text{-}CNT}$, which increases the amplifier bandwidth to 1GHz), the amplifier actually *attenuates* the signal by 3.6 dB, rather than provides gain. As an even starker example – with a single m-CNT in the NMOS CNFET input transistors, again the amplifier *attenuates* the signal by 130 dB (due to degradation in transconductance and output impedance by driving the NMOS in triode region). Thus, the presence of only a single m-CNT can result in catastrophic circuit failure in analog circuits (in addition, m-CNTs can also impact other amplifier metrics such as power consumption, common mode rejection ratio, and noise).

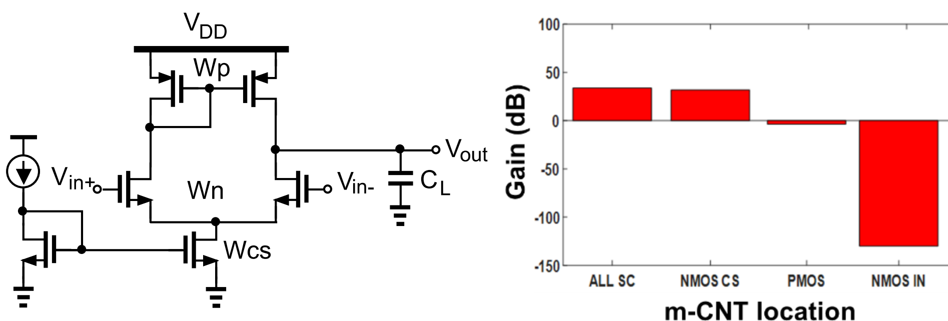


Fig. 2.6 M-CNTs Impact on Differential Amplifier Circuit

Importantly, the differential amplifier in Fig. 2.6 is not unique; Table 2-1 shows a wide variety of different analog building block circuits and their sensitivity to a single m-CNT placed in different FETs within the circuit. In all cases, a single-CNT can cause catastrophic failure when placed in a sensitive FET within the circuit. For example, a single m-CNT results in a worst-case gain reduction of 106 dB for a folded cascade amplifier. All simulations are performed using CNFET compact models calibrated for a 10nm technolody node assuming an m-CNT has resistance of 25 KΩ.

Table 2-1 M-CNTs impact on different amplifier configurations with different locations

M-CNT location	Common Source	Source Follower	Common Gate	Diff. Pair	Folded Cascode
None (All S.C)	43 dB	-50 mdB	40.5 dB	33.8 dB	67.7 dB
Input (1)	-3.4 dB	-108 dB	2.13 dB	-130 dB	40.5 dB
Active Load (2)	2.8 dB	-1.2 dB	2.76 dB	-3.6 dB	1.2 dB
Current Source (3)	-			31.9 dB	-38.8 dB 45.8 dB
Cascode (4)					22.7

Since a single m-CNT can cause a complete circuit failure within amplifiers (which are the main blocks for analog circuits), then a single m-CNT can also result in catastrophic functional failure for larger analog mixed-signal systems. Fig. 2.7 shows 8-bit DAC schematics and transfer characteristics, analysing m-CNTs placed within different locations within the circuit. With only a single m-CNT within the entire circuit, the output can latch to one of the supply rails – again catastrophic circuit failure. Therefore, even realizing 99.99% s-CNT purity (the requirement for digital VLSI circuits) is insufficient for analog mixed-signal circuits. Since 100% s-CNT purity is not feasible, analog and mixed-signal circuits *must be designed* to be robust to any remaining m-CNTs.

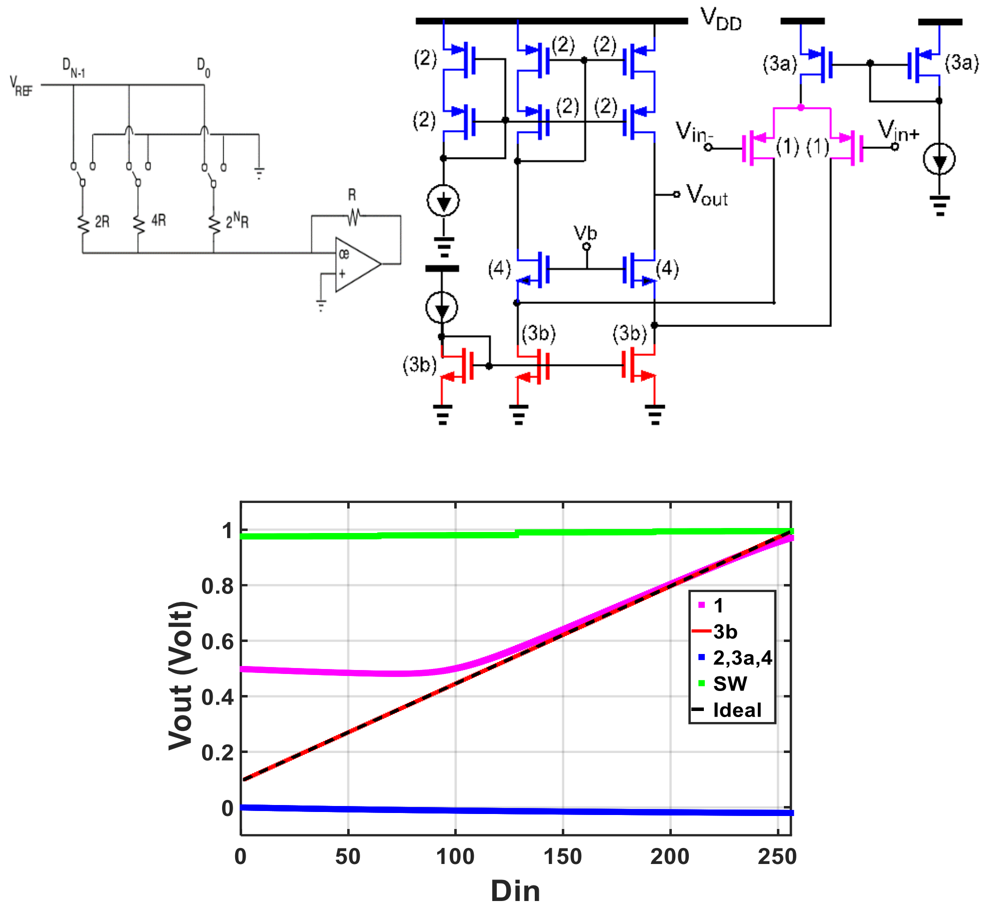


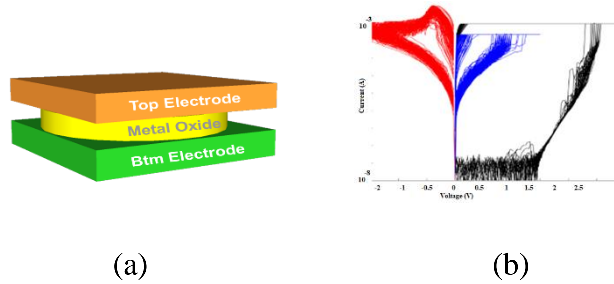
Fig. 2.7 8-Bit DAC Transfer Characteristics with different M-CNTs Locations

3. Chapter 3 SHARC: Self-Healing Technique with RRAM and CNFETs

In this chapter, a new circuit design technique is proposed to overcome the presence of m-CNTs by heterogeneously integrating CNFETs with RRAM.

3.1 Basic Principle

The main benefits of our self-healing technique are that it is (1) non-volatile, (2) wafer-scalable and VLSI compatible, and (3) is compatible and be used with any of the techniques discussed previously for improving starting CNT purity. The key to our approach is leveraging monolithic 3D integration of CNFETs with RRAM. RRAM is a non-volatile memory, that traditionally has a high-*k* dielectric (such as HfO_2) between two dissimilar metal electrodes, as shown in Fig. 3.1(a). Initially the dielectric does not conduct current, making the RRAM cell in its high resistance state (HRS). When a sufficiently high positive voltage is applied between the two electrodes, oxygen vacancy diffusion within the high-k dielectric forms a low-resistance oxygen filament through the RRAM dielectric, converting the RRAM to its low resistance state (LRS, SET operation). The first time the RRAM is programmed into its LRS is called the FORM operation (black line in Fig. 3.1(b)), which requires higher voltage that the SET as it forms the initial filament in the RRAM cell. This low resistance filament can be reversed by applying a negative voltage across the RRAM. With sufficient current flow, the RRAM will be reprogrammed back into its HRS (RESET operation, individuated in the red curve in Fig. 3.1(b)). The RRAM can repeatedly be programmed into its LRS and HRS by performing repeated SET and RESET operations.



(a) (b)

Fig. 3.1 (a) RRAM (b) I-V characteristics (black: Form, blue: SET, red: Reset)

To perform SHARC and leverage the RRAM within the CNFET analog circuitry, we perform the following main steps:

(0): Starting FET: Fig. 3.2 shows an initial CNFET containing an m-CNT. Thus, the initial I_{ON}/I_{OFF} ratio is severely degraded, and can cause catastrophic circuit failure in an amplifier, for instance.

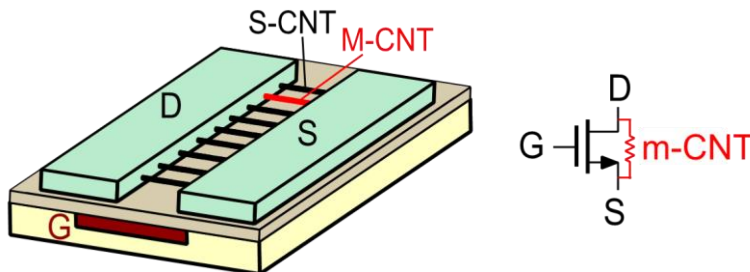


Fig. 3.2 CNFET with m-CNT resulting in high leakage current

(1) Sub-CNFETs: To perform SHARC, each CNFET in the design is split into multiple minimum width FETs (i.e., “sub-CNFETs”) as shown in Fig. 3.3.

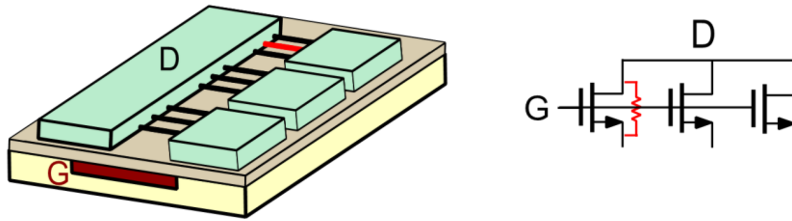


Fig. 3.3 CNFET is split into sub-CNFETs

(2) RRAM integration: Then we integrate a RRAM cell in series to each sub-CNFET by fabricating the RRAM directly under (or over) the source or drain contact of each sub-CNFET. Critically, this is enabled by the low-temperature fabrication of both the CNFET and RRAM (<400 °C). In stark contrast, silicon FETs which require >1000 °C to fabricate would damage and destroy and devices fabricated directly beneath them.

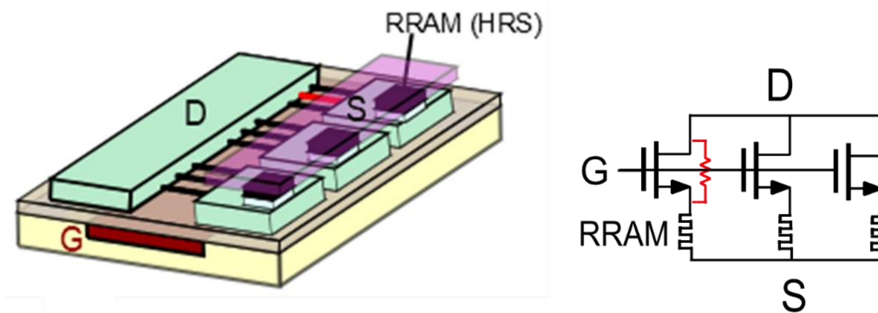


Fig. 3.4 3D integration of RRAM with sub-CNFET Fig

(3) Initialization: a positive voltage is applied across the RRAM electrodes (top-to-bottom) to program the RRAM into a low resistance state (LRS); this is the RRAM “FORM” operation.

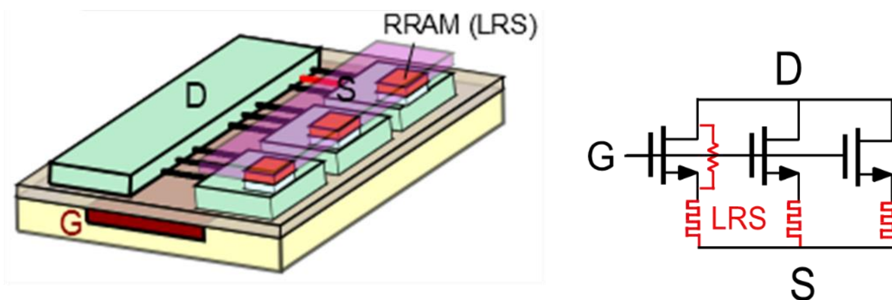


Fig. 3.5 CNFET after Forming RRAM

(3) Self-Healing: the gate terminals of the CNFETs are biased to turn the CNFETs "OFF" and a negative voltage (*i.e.*, opposite polarity used during the previous FORM operation) is applied across the CNFET and RRAM. CNFETs with only semiconducting CNTs (s-CNTs) in the channel do not conduct significant current, and thus the RRAMs in series with those CNFETs remain in a low resistance state. However, CNFETs containing m-CNTs in the channel conduct current (m-CNTs are not controlled by the gate and conduct current regardless of gate bias), and with sufficient current under negative bias the RRAM is re-programmed into a high-resistance state (HRS) (the RRAM "RESET" operation).

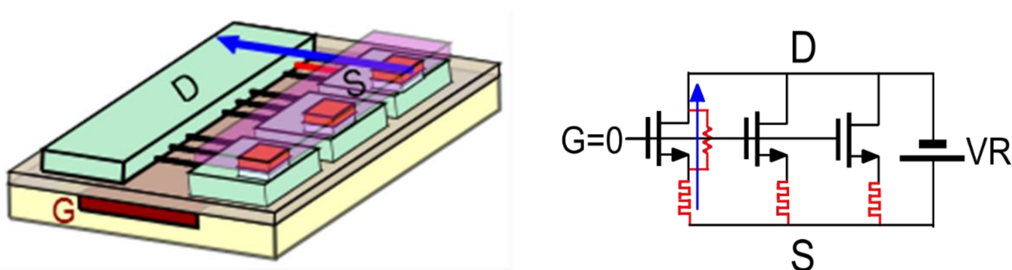


Fig. 3.6 Self-Healing: Reset RRAM in series with m-CNTs

(4) Final circuit fabrication: Perform final chip fabrication (*e.g.*, additional metal layers). After performing SHARC, sub-CNFETs containing mCNTs are in series with the RESET high-resistance RRAM (effectively removing those sub-CNFETs from the circuit), while CNFETs containing only s-CNTs are in series with SET low-resistance RRAM as shown in Fig. 3.7.

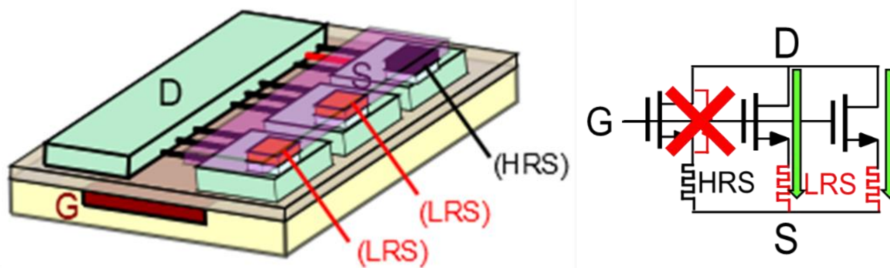


Fig. 3.7 Circuit "self-trims" sub-CNFETs containing m-CNTs

Fig. 3.8 shows measured current-voltage (IV) transfer curves for typical CNFET prior- and post- performing the SHARC self-healing. Prior to the self-healing, the CNFET exhibits substantial off-state leakage current due to the presence of m-CNTs (typical measured I_{ON}/I_{OFF} is <10 for a CNFET containing m-CNTs). Post self-healing, the CNFETs exhibit I_{ON}/I_{OFF} >1000 and I_{OFF} reduces by >800× due to the series RRAM resetting to a high resistance state during the self-healing.

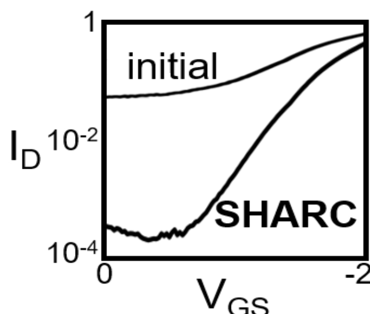


Fig. 3.8 CNFET measured I-V Characteristics prior and post SHARC

3.2 Circuit Implementation

SHARC is a broad technique that can be applied to a wide range of analog circuit blocks such as amplifiers, and comparators. shows the schematic of a 2-stage OPAMP with SHARC where each CNFET is split into 2 sub-CNFETs and a RRAM cell is integrated in series with each of the sub-CNFETs. Simulation results show that after implementing SHARC, the

OPAMP gain suffers negligible degradation due to the presence of m-CNTs within the circuit. For comparison, Fig. 3.9 also shows the gain for the same circuit before (or without) applying SHARC: a single m-CNT can result in the OPAMP becoming an attenuator similar to the differential amplifier discussed previously. To validate SHARC and demonstrate the ability to realize a functional analog circuit integrating CNFET CMOS with RRAM, Fig. 3.10 shows the same 2-stage OPAMP fabricated in a relaxed 1 μm technology node. The transfer characteristics (also shown in Fig. 3.10) indicates a gain of >800, matching simulation results.

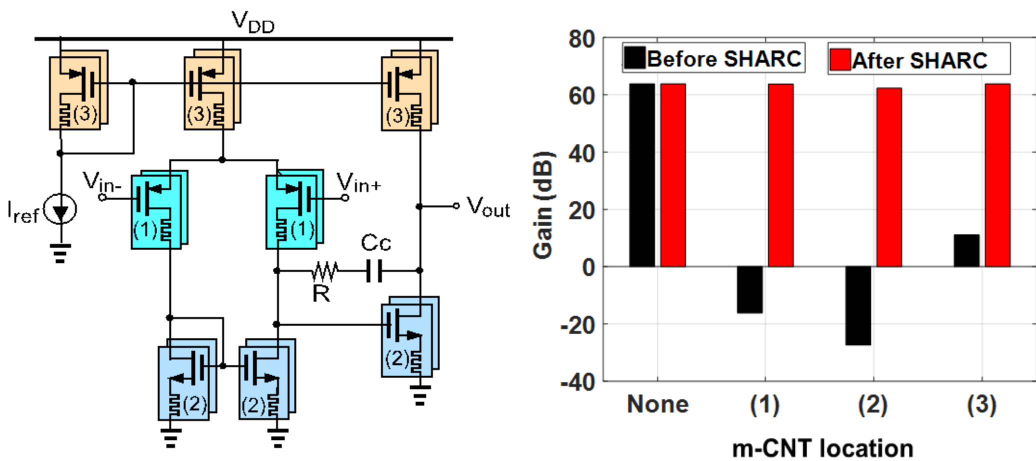


Fig. 3.9 2-stage OPAMP with SHARC (left) and gain with different m-CNT location (right)

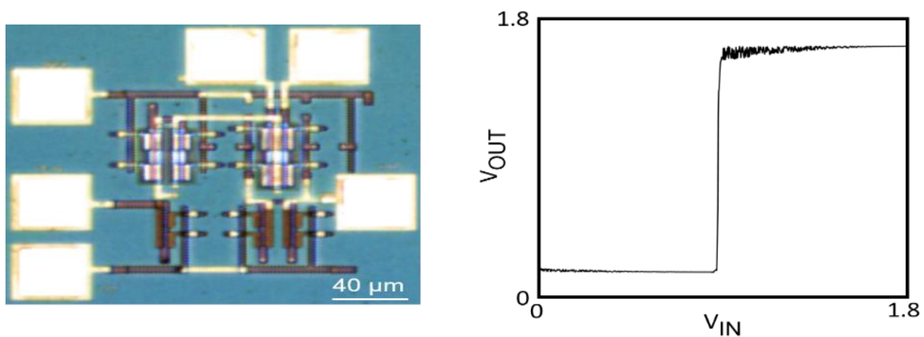


Fig. 3.10 Die Photo of 2-stage op-amp (left), and its measured transfer characteristics (right)

SHARC can also be applied to various amplifiers configurations. Fig. 3.11 shows the schematics of five different amplifiers, highlighting the RRAM locations (colors represent matching sub-CNFET transistors). Table 3-1 illustrates the benefit of SHARC on these amplifiers. Simulations, based on experimentally calibrated CNFET and RRAM compact models for 10-nm technology nodes [9], confirm that all of these circuits retain correct functionality despite inserting a m-CNT within any CNFET in the circuit. As an example, without SHARC, a single m-CNT in the current source for a cascode amplifier results in a worst-case reduction of gain by 106dB, while with SHARC, a single m-CNT results in a worst-case reduction of gain of only 3dB. For the common source and common gate when input transistors have m-CNTs, the gain after SHARC decreases; this is caused by one of the input transistors sub-CNFETs being effectively removed by the RRAM during the SHARC process, which slightly changes the DC operating point. However, this would have minimal impact in a realistic system (due to using the amplifier in negative feedback, or by implementing common mode feedback circuits to adjust the output DC voltage of the different circuit).

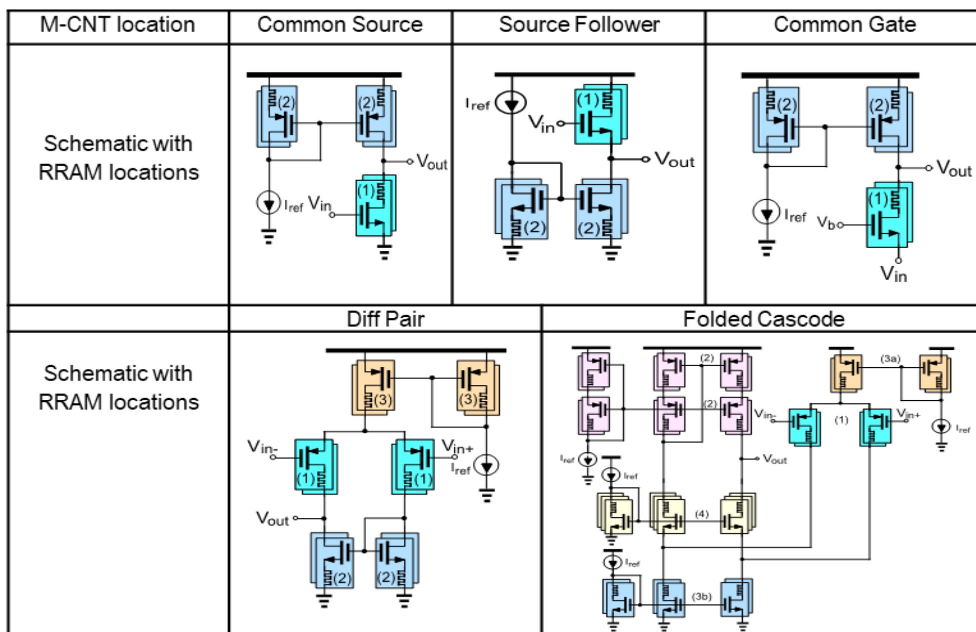


Fig. 3.11 Different Amplifiers Schematics with SHARC

Table 3-1 Benefits of SHARC on different amplifiers configurations. (Models experimentally calibrated to 10-nm CNFETs are used for simulation)

m-CNT location	Common Source		Source Follower		Common Gate		Diff. Pair		Folded Cascode	
	Baseline	**SHARC**	Baseline	**SHARC**	Baseline	**SHARC**	Baseline	**SHARC**	Baseline	**SHARC**
None (All S.C)	**43 dB**	**42.89 dB**	**-50 mdB**	**-48 mdB**	**40.5 dB**	**40.7 dB**	**33.8 dB**	**35.4 dB**	**67.7 dB**	**67.7 dB**
Input	**-3.4 dB**	**9.3 dB***	**-108 dB**	**-75 mdB**	**2.13 dB**	**7.8 dB***	**-130 dB**	**32 dB**	**40.5 dB**	**66 dB**
Active Load	**2.8 dB**	**40.8 dB**	**-1.2 dB**	**-57 mdB**	**2.76 dB**	**38.6 dB**	**-3.6 dB**	**34.4 dB**	**1.2 dB**	**65 dB**
Current Source	-		-		-		**31.9 dB**	**35.4 dB**	**-38.8 dB**	**65 dB**
									45.8 dB	**67.5 dB**
Cascode	-		-		-		-		**22.7 dB**	**65.5 dB**

*Gain reduction due to high impedance node: can be solved in –ve FB systems

SHARC is not limited to isolated amplifiers. Here we illustrate how SHARC can also be applied to larger analog mixed-signal systems such as an 8-bit SAR ADC as shown in Fig. 3.12 (whereas Vin is the sampled input). The self-healing technique is applied on the strong-arm latch (comparator) and switches since they are the most sensitive components to m-CNTs. A single m-CNT in the SA latch results in latching the comparator output to either VDD or GND, and a single m-CNT in the switches will introduce linear errors (offset and gain error) as well as non-linear errors in the ADC transfer curve as shown in Fig. 3.13 in addition to drastically increasing the power consumption. While the SAR logic (digital circuits) could be implemented with SHARC, we choose not to in order to: (1) demonstrate that SHARC can be selectively implemented within a circuit to achieve a designer's goals for robustness, and (2) the digital circuits can still function in the presence of a limited number of m-CNTs, albiet with higher power consumption. Fig. 3.13 shows the 8-bit SAR ADC transfer curve with m-CNTs prior and post SHARC indicating that post SHARC the circuit maintains correct functionality despite the presence of m-CNTs. Simulations were performed using compact models calibrated for 10 nm technology nodes (for CNFETs and RRAM including parasitics). The ADC consumes 10 nWatt from 1.1 V supply with 20 kHz clock frequency.

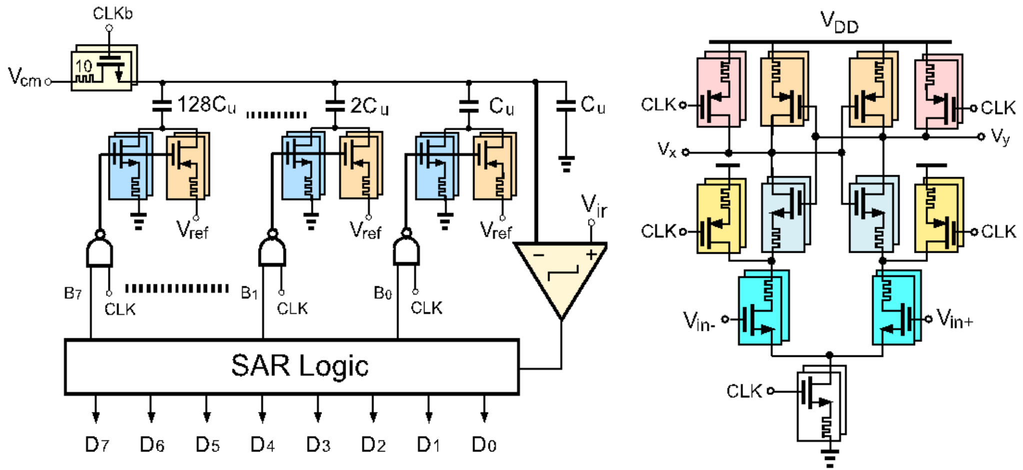


Fig. 3.12 8-bit SAR ADC with SHARC (a) ADC Schematics, (b) SA Latch with SHARC

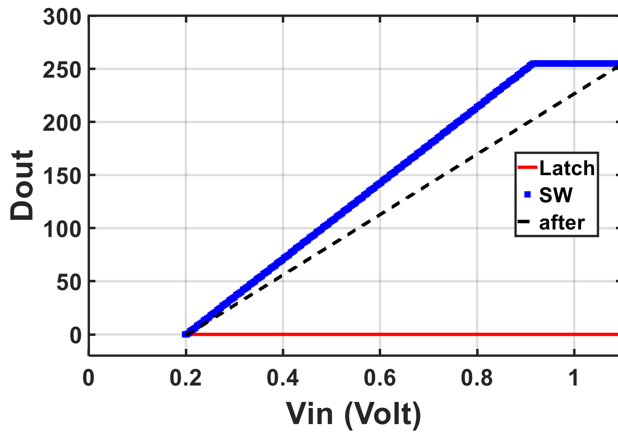


Fig. 3.13 8-bit SAR ADC transfer characteristics prior and post SHARC with different m-CNTs locations (Simulations based on 10-nm CNFET models)

3.3 Design Considerations

It is very critical to avoid programming RRAM during normal circuit. Thus, the RRAM stack is engineered so that the subsequent SET voltages ($V_{SET} \geq$ 2.5 V) are above the operating voltage of the circuit (VDD=1.8V). Therefore, the RRAM is not inadvertently programmed during normal circuit operations (importantly, the 2.5 V required for the SET operation is still dramatically lower than the >10 V required for electrical breakdown, discussed previously).

Additional factors should also be taken into consideration to minimize impacting circuit performance. For example, the absolute values and ratios between the RRAM high and low resistance states is a key metric. The RRAM high-resistance value impacts the circuit leakage power (*e.g.*, increased RRAM high-resistance decreases leakage current through sub-CNFETs containing m-CNTs). On the other hand, the RRAM low-resistance value impacts the output signal swing (*e.g.*, increased RRAM low-resistance decreases available voltage headroom by ($I_{dc} * R_{LRS}$)).

Moreover, the location of the RRAMs in the circuit can impact amplifier gain and input referred noise. For the case of input transistors to amplifiers where the input is fed to the gate of the transistor: the RRAM should be placed in series with the drain terminal of the sub-CNFETs rather than the source terminal in order not to impact the V_{GS}, and hence g_m, and r_o of the CNFET. The output impedance of the 1st stage in can be expressed by

$$R_{out} = (ro_1 + R_{LRS})//(ro_2 + R_{LRS})$$

Which is approximately equal to the ideal case with no RRAM ($ro_1 \,//\, ro_2$) resulting in almost the same bandwidth as the ideal case. For CNFETs within current mirrors, the RRAM can be placed either in the source or drain of transistor as their V_{GS} will be adjusted to support the current in the branch.

Matching in analog circuits is another important design aspect. The colors in the previous schematics represent which transistors should be well-matched for the circuits to work properly. For example, in the amplifiers the self-

healing technique should maintain the matching between input transistors and current mirrors. Specifically, if one of the sub-CNFETs in one of the input transistors has a m-CNT and is removed from circuit after applying SHARC, then this should also happen for the other input transistor to maintain symmetry. One can enforce matching CNFETs through physical layout. By fabricating CNFETs in the same row (e.g., alone the direction of the CNTs on the wafer), these CNFETs will share essentially identical CNTs, and thus will be match (e.g., a m-CNT running through one CNFET will preferentially run through all matched CNFETs laid out along the direction of the CNTs, Fig. 3.14 [16]).

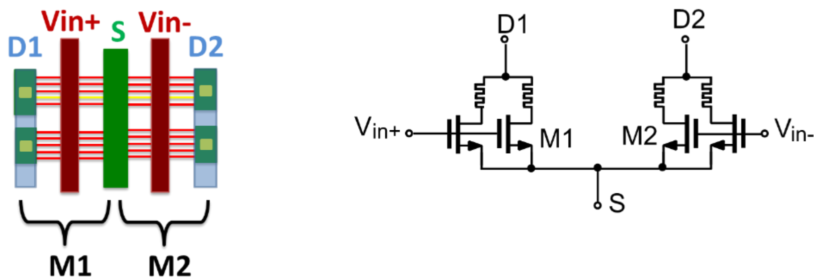


Fig. 3.14 Matched Transistors Layout

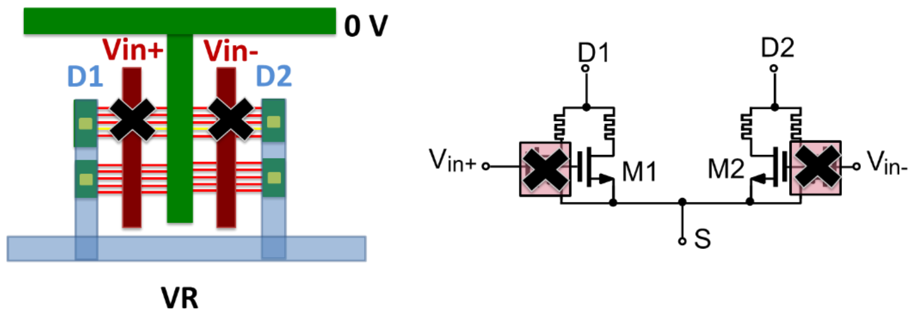


Fig. 3.15 Matched Transistors after Self-Healing Process are highly correlated

3.4 Costs and Benefits

While SHARC provides substantial benefits, there are important costs that must also be considered. SHARC can impact the circuit performance by decreasing the available voltage headroom, decreasing amplifiers gain bandwidth (g_m decreases if one of the sub-CNFETs of input transistors has m-CNTs while the bandwidth remains almost the same), and increasing input referred noise due to the RRAM. However, designing the circuits carefully (based on the design consideration illustrated previously) can mitigate many of these drawbacks. Since the transistor width in analog circuits are typically larger than the minimum allowed width in the technology, a CNFET can be split into a larger number of sub-CNFETs, ensuring all sub-CNFETs are removed during SHARC. Splitting CNFETs into sub-CNFETs does have an area overhead: splitting an initial CNFET into N sub-CNFETs results in an area overhead of (~(N-1)*S/W), where S is the minimum lithographic pitch and W is the original CNFET width.

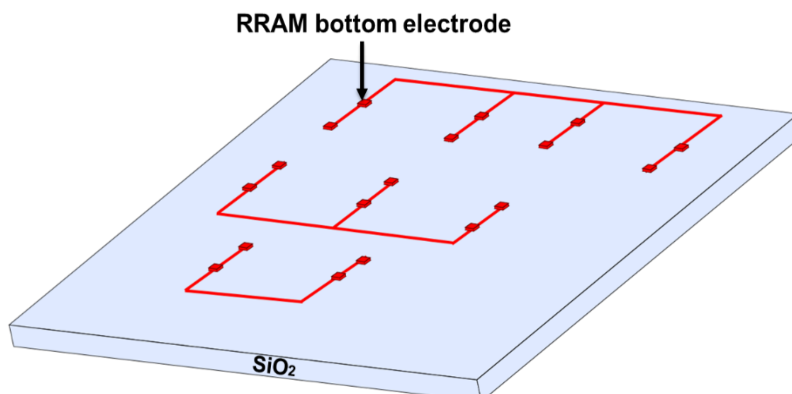
The key benefits of SHARC are: (1) the self-healing process (e.g., RRAM programming) is automatically performed by the m-CNTs themselves (as the mCNTs provide the current path for resetting the RRAM during the self-healing process). (2) CNFETs and RRAMs are fabricated at low temperatures (<300°C), and therefore can be fabricated directly vertically overlapping one-another in a monolithic three-dimensional fashion; this allows each RRAM cell to be fabricated either above or below the source or drain contact of the CNFET, minimizing area penalty associated with SHARC. (3) SHARC is non-volatile due to the non-volatility of RRAM with retention times >10 years. Even though the circuit retains its healed configuration due to the non-volatility of the RRAM, future implementations of SHARC can investigate the ability to repeatedly reprogram the RRAM during runtime, enabling real-time and continuous circuit self-healing.

4. Chapter 4 Fabrication Process and Measurement Results

In this chapter, we illustrate the key SHARC fabrication process steps. We use this process to experimentally realize the first functional CNFET analog mixed-signal systems (such as 4-bit SAR ADC, and 4-bit DAC), and show their measured results.

4.1 Fabrication Process Flow

While Chapter 3 illustrates how to perform SHARC for isolated CNFETs, here we show how SHARC can scale to large-scale circuits as the self-healing process can be performed once for all CNFETs in the circuit in parallel. The process flow (illustrated for a 2-stage OPAMP) is shown in Fig. 4.1- Fig. 4.5. Bipolar RRAMs are initially fabricated on the first layer of the chip by depositing the RRAM bottom metal electrode on the starting SiO_2 substrate, then the RRAM dielectric (HfO_2), then RRAM top metal electrode. The metal layer used to implement the RRAM top electrode can also be used as the CNFET bottom gate metal. While not required, this can decrease the number of required metal layers and make physical design more compact.



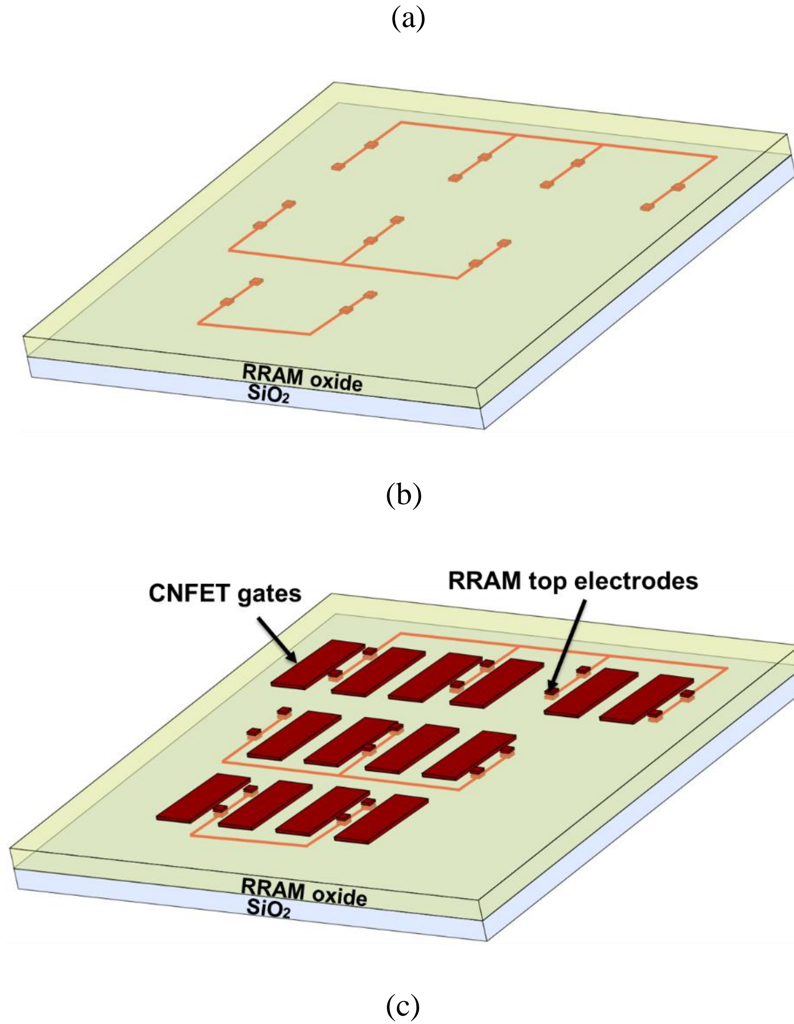


Fig. 4.1 RRAM Fabrication Steps

To FORM the RRAMs, a sacrificial layer of metal is defined and connects all the RRAMs cells in parallel as shown in Fig. 4.2. Then a positive voltage (V_{FORM}) is applied between the RRAMs electrodes. The sacrificial layer of metal is then removed, followed by the CNFET fabrication (CNFET source and drain contacts are patterned directly vertically overlapping the RRAM cells). The CNFETs are fabricated by depositing solution-based purified (~99.99% s-CNTs) CNTs on the wafer, followed by lithographically defining the source and drain regions as shown in Fig. 4.3.

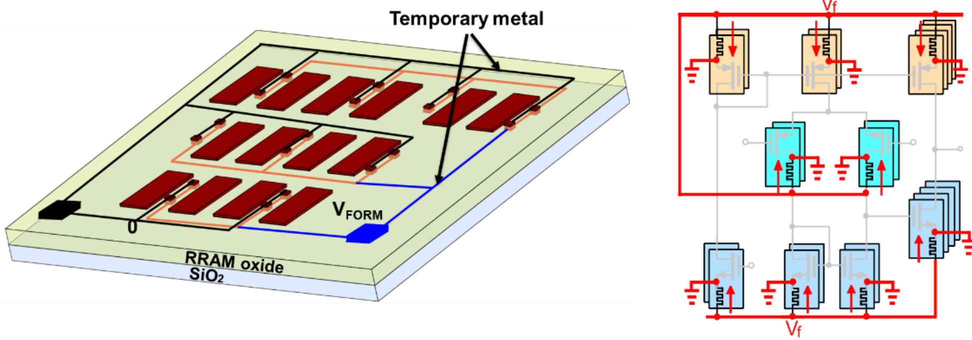
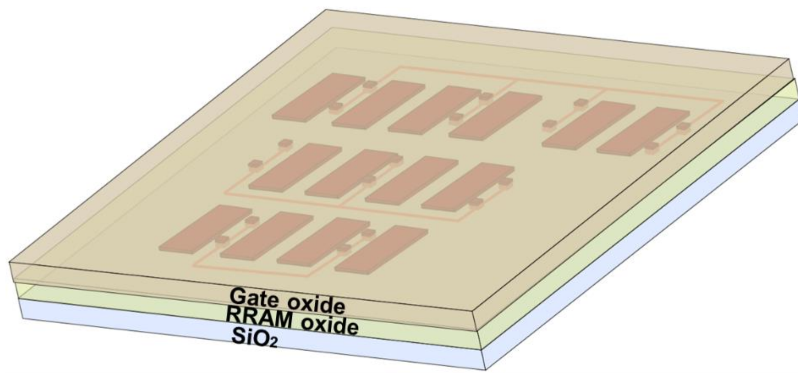
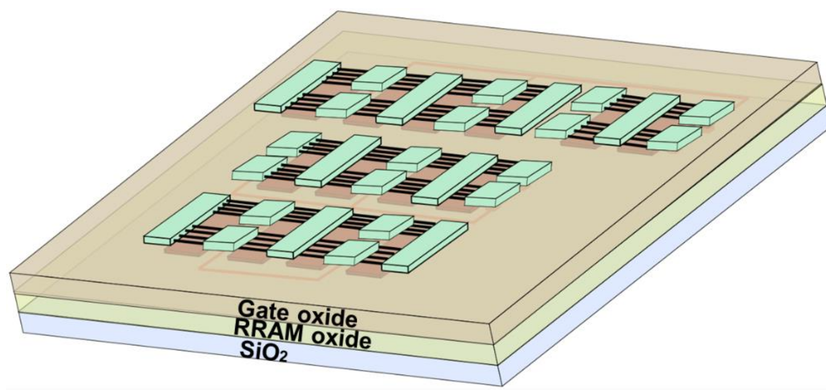


Fig. 4.2 RRAM Form



(a)



(b)

Fig. 4.3 CNFET Fabrication

Another sacrificial layer of metal can be used to configure the circuit so all sub-CNFET gates are connected, and all CNFET-RRAM pairs are connected in parallel. This enables all sub-CNFETs gates to be biased (e.g., $|V_{GS}| = 0V$) simultaneously, as well as for all the RRAMs to undergo the self-healing RESET operation in parallel (importantly, all the CNFETs are PMOS as-fabricated, allowing a single gate bias to turn off all the CNFETs simultaneously). To ensure RRAM RESET, the RRAM stack should be designed to require less reset current than the off-state leakage current through an m-CNT (<100μA for a scaled technology node).

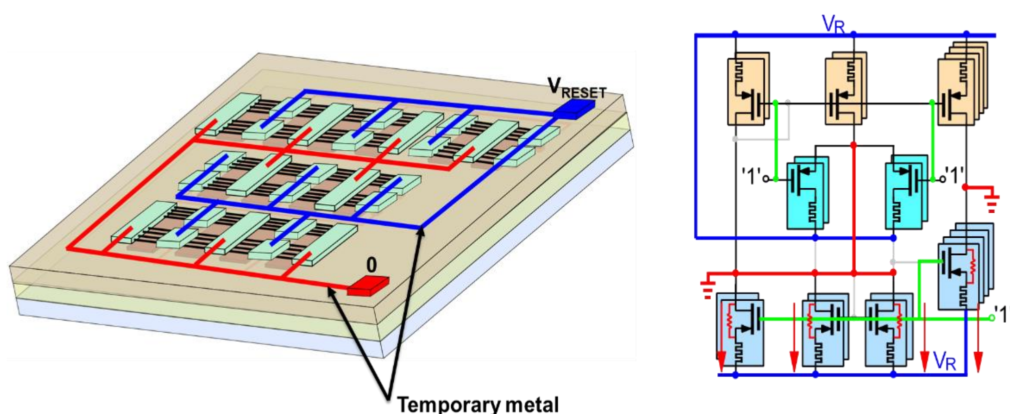


Fig. 4.4 Reset RRAM: Self-Healing step

After performing the self-heating RESET operation, the sacrificial layer of metal is removed, and the CNFETs are doped to form the PMOS CNFETs and NMOS CNFETs followed by the final metal routing to complete the circuit (the NMOS CNFETs are formed through electrostatic doping, whereby a non-stoichiometric HfO_X dielectric is deposited over exposed CNTs in the channel of the FETs, converting PMOS CNFETS to NMOS CNFETs [17]). This process can be applied to any arbitrary circuit. Fig. 4.6 shows the schematics of the strong-arm latch during RRAM form and reset operations. Importantly, all the experimental circuits fabricated and reported in this work are complementary (using both PMOS and NMOS CNFETs). The additional sacrificial metal layers used to form and reset the RRAM cells negligibly impacts chip area as they are removed prior to final chip fabrication.

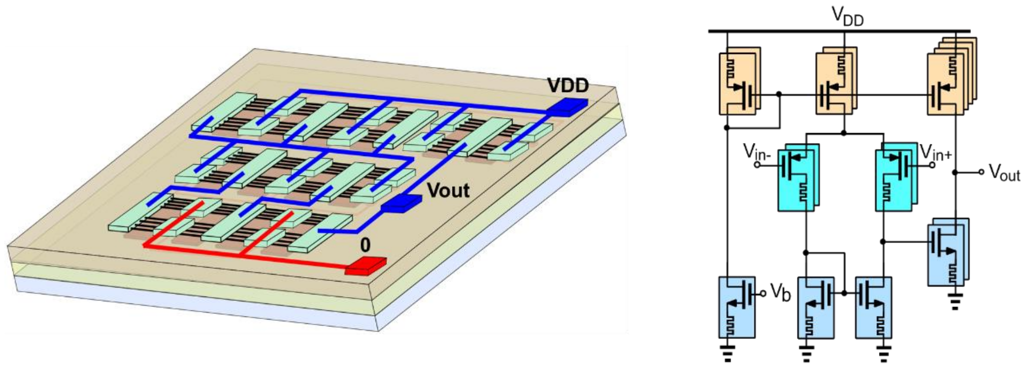


Fig. 4.5 Final Circuit fabrication 2-stage OPAMP

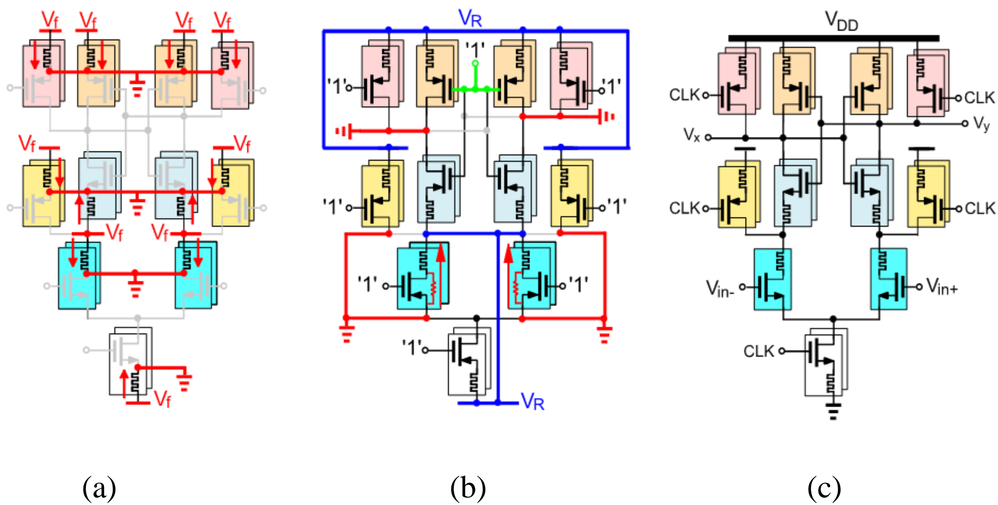


Fig. 4.6 Strong-Arm Latch (SAR ADC comparator) Schematics (a) RRAM Form, (b) Self-Healing Step, (c) Final Circuit

4.2 Measurement Results

As an experimental demonstration, we use SHARC to fabricate the following analog and mixed-signal circuits: common source amplifier, 2-stage OPAMP, strong-arm latch, 4-bit capacitive DAC, and 4-bit SAR ADC. The chip die photo is shown in Fig. 4.7. Due to the limitations of an academic cleanroom, all circuits are implemented at a relaxed ~1 μm technology node (however, there is not fundamental limitations to applying SHARC to scaled technology nodes). The 4-bit capacitive DAC schematic with the die photo

are shown in Fig. 4.8. In the 4-bit capacitive DAC, we implemented SHARC in the 2-stage op-amp and in the switches. Measured transfer characteristics with INL and DNL with digital codes are shown in Fig. 4.9. The DAC response is monotonic, with a maximum DNL of 0.8 LSB. INL is <0.87 LSB for the majority of the codes except the last 2 codes (<2 LSB due to op-amp saturation which can be modified by increasing V_{DD} of the op-amp to be greater than V_{ref} by 0.2V).

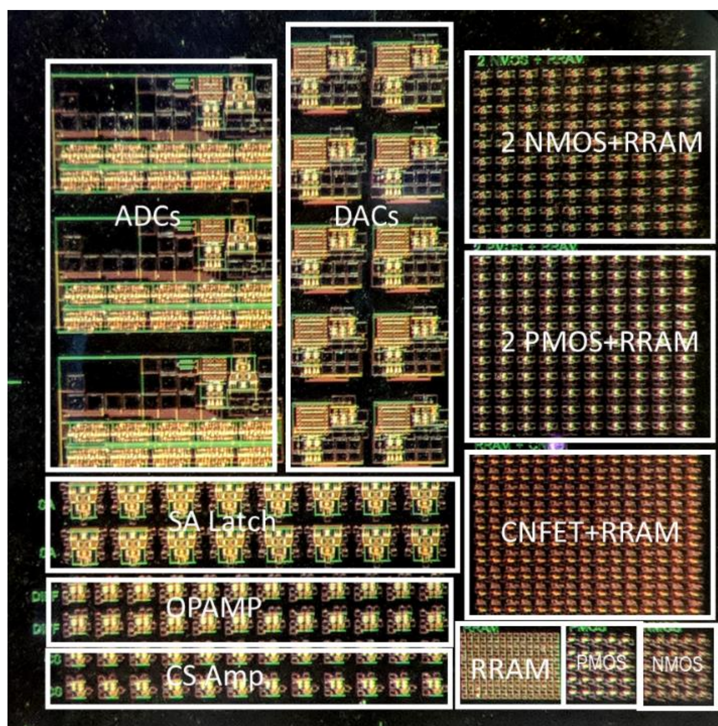
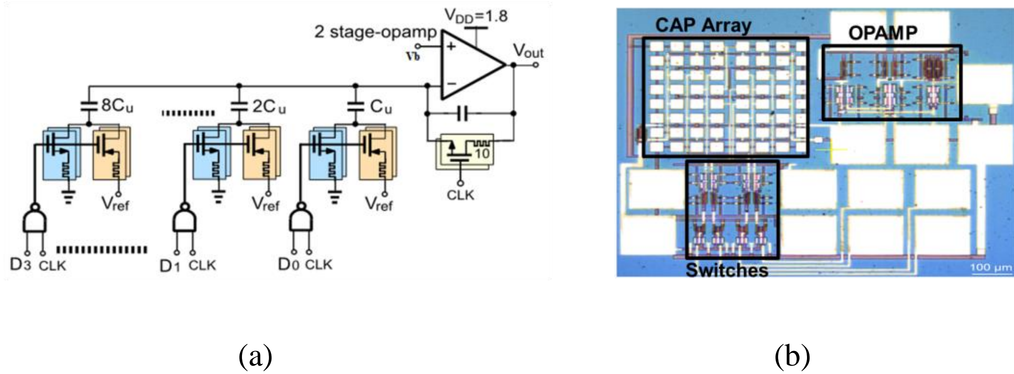
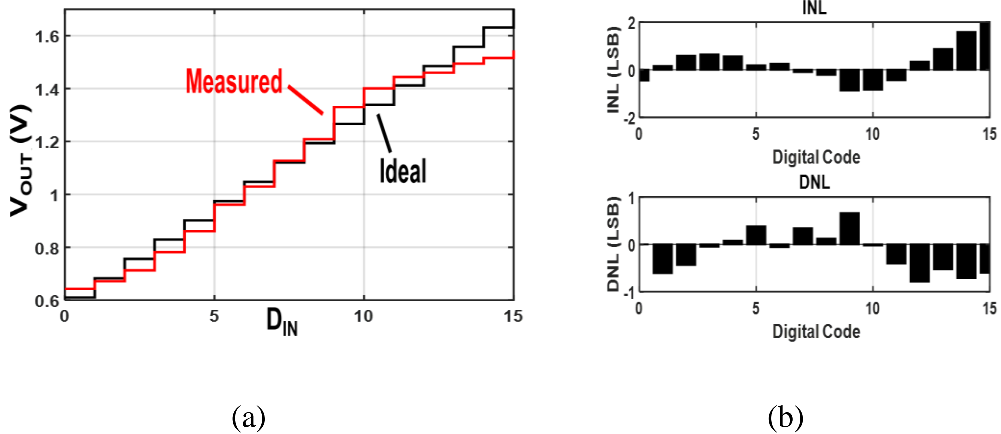


Fig. 4.7 Die photo of the chip showing different circuits



(a) (b)

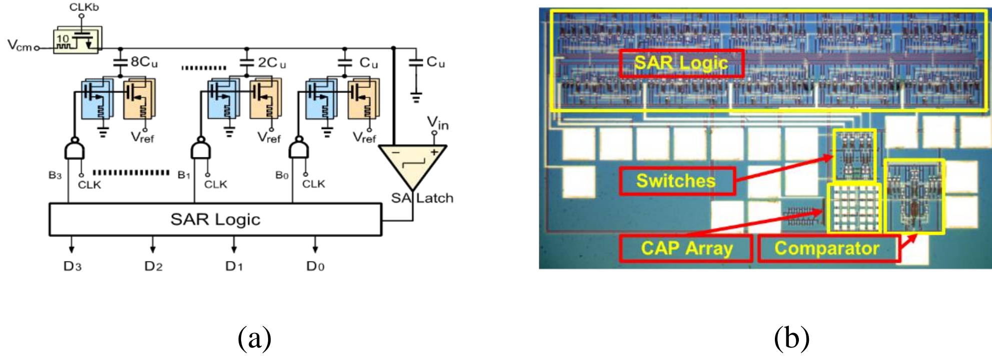
Fig. 4.8 4-Bit capacitive DAC with SHARC, (a) Schematic and (b) die photo



(a) (b)

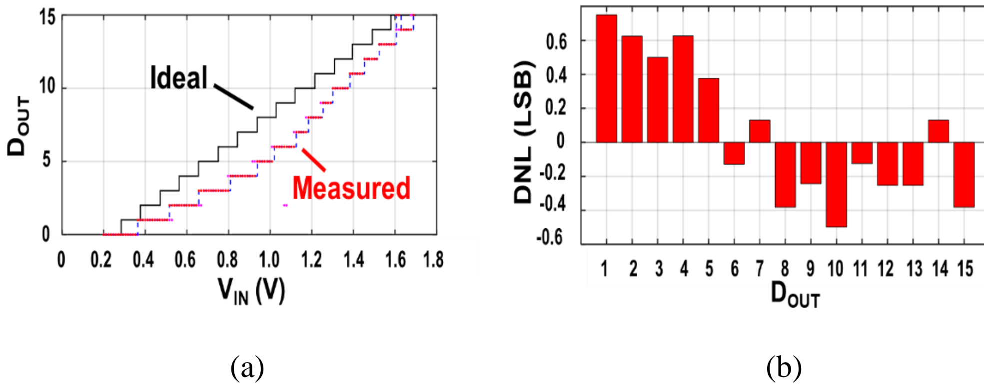
Fig. 4.9 4-Bit capacitive DAC (a) measured characteristics show the monotonic behavior with offset (50mV) and (b) non-linearity (INL, DNL curves)

In the 4-bit SAR ADC, SHARC was implemented in the SAR comparator (strong-arm latch) and in the switches as shown in Fig. 4.10 (Vin is the sampled input). The measured transfer characteristics in Fig. 4.11 show monotonic behaviour with non-linearity (-0.5 LSB < DNL < 0.75 LSB) and gain error (due to large parasitic caps and routing resistance). These circuits are the first functional mixed-signal CNFET circuits demonstrated, and the largest reported CMOS CNFET circuits to-date (see the comparison Table 4-1[18],[19],[20]).



(a) (b)

Fig. 4.10 4-Bit SAR ADC (a) schematic, and (b) its die micrograph



(a) (b)

Fig. 4.11 4-Bit SAR DAC (a) Measured characteristics show the ADC monotonic behavior with offset (35mV), non-linearity and gain error whereas the DNL (b) is (-0.5 LSB→ 0.75 LSB)

Table 4-1 Comparison to state-of-the-art CNFET CMOS demonstrations

Circuit	CNFETs per Circuit	Reference
4b-ADC	**306**	**This Work**
4-bit full adder	132	[18]
Inverter	2	
SRAM Cell	6	[19]
Ring Oscillator	12	[20]
Inverter	2	

5. Chapter 5 Conclusions and Future Work

5.1 Summary

CNFETs are a promising emerging technology for energy-efficient electronics. Despite this promise, CNTs are subject to substantial inherent imperfections; every ensemble of CNTs includes some percentage of m-CNTs, which results in conductive shorts between CNFET source and drain, resulting in excessive leakage and degraded (potentially incorrect) circuit functionality (degrades the noise margin of logic gates). While several techniques have been developed to remove the majority of m-CNTs, no technique today removes 100% of m-CNTs. While these techniques enabled the first digital CNFET circuits, even a single m-CNT can cause catastrophic failure for analog or mixed-signal CNFET circuits (a single m-CNT degrades the intrinsic gain of the CNFET and changes the DC operating point of the whole circuit).

This work presents a new circuit design technique, Self-Healing Analog with RRAM and CNFETs (SHARC), that is based on 3D integrating the CNFETs with non-volatile resistive RAM (RRAM). Each CNFET is split into multiple minimum width FETs (i.e., “sub-CNFETs”), with a RRAM cell in series fabricated directly under (or over) the source or drain contact of each sub-CNFET. SHARC leverages the programmability of RRAMs to automatically “self-heal” analog circuits in the presence of m-CNTs. The sub-FETs including m-CNTs become series to RESET high-resistance RRAM that effectively removes those sub-CNFETs from the circuit, while CNFETs containing only semiconducting CNTs are in series with SET low-resistance RRAM. Post SHARC, a single m-CNT results in a worst-case reduction of amplifier gain of only 3 dB instead of 106 dB before using SHARC.

SHARC is a VLSI-compatible and non-volatile technique that can be applied to any arbitrary circuit. RRAM programming step can be performed once for all CNFETs in parallel for larger-scale circuits during fabrication process.

Using SHARC, we experimentally demonstrate analog CNFET circuits robust to m-CNTs as well as the first mixed-signals CNFET subsystem (4-bit DAC and SAR ADC; these are the largest reported complementary (CMOS) CNFET circuit demonstrations to-date).

5.2 Future Work

By combining continued progress in CNFET processing, SHARC lays the foundation for future work to realize high-performance CNFET-based electronics. Building on this work, some directions might be explored:

Improving Circuit Performance:

Since SHARC is implemented at the CNFET-level, it can be combined with additional existing circuit techniques to further improve performance, such as technology node scaling to improve energy efficiency and improved circuit topologies to improve linearity.

Scaling to Larger Systems:

Leveraging the low temperature fabrication of CNFET technology, we can implement compact nano-systems by 3D integrating sensors, ADCs, and digital logic using CNFETs. However, the design of high-resolution ADCs and DACs using CNFET technology is very challenging. In this work, we proposed a technique to overcome the m-CNTs problem; which is one of the major obstacles facing CNFET circuits. Moreover, CNFET device noise and hysteresis can also degrade the system performance as they degrade SNR and linearity for analog circuits and degrade the noise margin and increase delay variations for digital logic. Modelling these non-idealities and introducing new techniques to overcome them can be explored. In addition, quantitative study of CNFET VLSI circuits yield with m-CNTs, noise, and hysteresis can be performed.

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