Carbon Nanotube CMOS Analog Circuitry

by

Rebecca Ho

B.S., The University of Texas at Austin (2017)

Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Engineering and Computer Science

at the

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Abstract

Carbon nanotube (CNT) field-effect transistors (CNFETs) promise significant energy efficiency benefits versus today's silicon-based FETs. Yet despite this promise, complementary (CMOS) CNFET analog circuitry has never been experimentally demonstrated. This work presents the first reported demonstration of CNFET CMOS analog circuits. For characterization, we fabricate analog building-block circuits such as multiple instances of two-stage op-amps. These CNFET CMOS op-amps achieve gain >700, operate at a scaled sub-500 mV supply voltage, achieve high linearity, and are robust over time. Additionally, we demonstrate a front-end analog sub-system that integrates a CNFET-based breath sensor with an analog sensor interface circuit (transimpedance amplifier followed by a voltage follower to convert resistance change of the chemoresistive CNFET sensor into a buffered output voltage).

However, further progress in large-scale CNFET analog circuits is difficult to realize due to the inherent presence of metallic-CNTs (m-CNTs), which create an electrical short between the source and drain of a transistor and can result in excessive leakage current and severe degradation to analog circuit performance. Self-Healing Analog with RRAM and CNFETs (SHARC) is a novel circuit technique that leverages the programmability of resistive random-access memory (RRAM) to overcome the presence of m-CNTs for analog circuits. Here, we experimentally validate SHARC for multiple analog and mixed-signal circuit topologies. Using SHARC, we experimentally demonstrate the first mixed-signal and complex analog circuits fabricated with CNFETs.

Thesis Supervisor: Max Shulaker

Title: Emmanuel E. Landsman (1958) Career Development Assistant Professor of Electrical Engineering and Computer Science

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1. Ho, Rebecca, Christian Lau, Gage Hills, and Max Shulaker. 2019. "Carbon Nanotube CMOS Analog Circuitry." *IEEE Transactions on Nanotechnology*, 1–1. https://doi.org/10.1109/TNANO.2019.2902739.
2. Amer, Aya G., Rebecca Ho, Gage Hills, Anantha P. Chandrakasan, and Max M. Shulaker. 2019. "29.8 SHARC: Self-Healing Analog with RRAM and CNFETs." In *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*, 470–72. IEEE.

Chapter 1: Introduction

1.1 Background

While physical and equivalent scaling of silicon complementary metal-oxide semiconductor (CMOS) technology has been a major driving force for improving computing energy efficiency for decades, continued scaling is yielding diminishing returns. Unfortunately, progress in computing is halting at the *exact moment* next-generation applications are demanding the largest gains in energy-efficiency. To enable these next-generation applications, isolated advances (whether it be continued scaling, materials improvements, circuit and system design, or software optimizations) alone are insufficient. Thus, coordinated advances across the entire system stack – from materials to circuits to systems – are required. In this thesis, I explore both new nanomaterials, new circuit topologies designed around these new nanomaterials, and new system integrations leveraging the unique properties of new nanodevices, in order to demonstrate future next-generation electronic systems.

To begin realizing such new electronic systems, we initially focus on an emerging nanotechnology which are the backbone of beyond-silicon electronic systems. Emerging one-dimensional (1D) and two-dimensional (2D) semiconductors are exciting emerging nanomaterials, promising improved carrier transport and electrostatic control versus bulk semiconductor materials (such as silicon). Single-walled carbon nanotubes (SWCNTs, or CNTs), are one such promising 1D nanomaterial with excellent electrical, thermal and physical properties [Riichiro 1998; Wei 2009]. CNTs are nanocylinders made of a single atomically-thin sheet of carbon atoms with a diameter of ~1 nm. Carbon nanotube field-effect transistors, CNFETs, are formed by multiple CNTs in parallel forming the channel whose conductance is modulated by a metal gate. Figure 1.1 shows the schematic of a single CNT and a CNFET. Gate and source/ drain contacts are defined by traditional lithography. Owing to their ultra-thin body thickness (~1 nm diameter of the CNT), CNFETs exhibit excellent electrostatic control and simultaneously high carrier transport [Hills 2015]. Due to these benefits, CNFETs are projected to achieve an order of magnitude benefit in energy-delay product (EDP) compared to silicon

CMOS for digital VLSI circuits [Chang 2012; Wei 2009; Tulevski 2014]. Importantly, CNFETs can be fabricated at low processing temperatures (<400°)[a] [Shulaker 2013a; Shulaker 2017; Patil 2009], and therefore naturally enable monolithic three-dimensional (3D) integration (whereby layers of circuits are fabricated sequentially and directly vertically overlapping one-another, all over the same starting substrate. Such monolithic 3D integration enables new paradigms in designing heterogeneous nanosystems [Shulaker 2017], allowing fine-grained integration of sensing, logic and memory at the nanoscale.

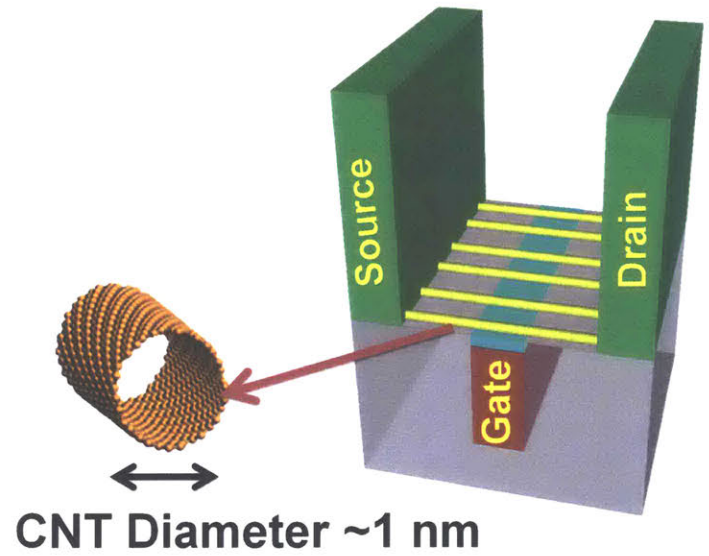

Figure 1.1: Schematic of carbon nanotube field-effect transistor (CNFET) with multiple parallel CNTs (nanocylinders made with atomically thin sheet of carbon atoms with diameter ~ 1 nm) bridging the source to drain contact. Conductance of the CNTs are modulated by the gate to turn the transistor on or off.

Moreover, CNFETs are a rapidly maturing nanotechnology which has progressed substantially over the past decade. CNFETs are unique among emerging nanotechnologies, as complete CNFET *digital* systems [Shulaker 2013a; Shulaker 2014], highly-scaled CNFETs with sub-10 nm channel lengths [Franklin 2012], and complementary p- and n-type CNFETs operating at scaled supply voltages of <400 mV [Wei 2013] have all been experimentally shown. However, prior to the work presented in this thesis, there has been no reported demonstration of CNFET CMOS-based analog or mixed-signal circuits.

1.2 Contributions

In this thesis, I focus on utilizing the unique properties of CNTs to realize the first analog and mixed-signal

[a] While CNTs are synthesized at high temperature (>800 °C), they can be transferred to arbitrary substrates through either layer transfers or by solution-based processing at room temperature. This decouples the high-temperature processing of the CNTs from the monolithic 3D IC.

circuits fabricated with a CNFET CMOS technology. Specifically, this work shows the following:

1) By leveraging our CNFET CMOS process (which results in robust and well-matched NMOS and PMOS CNFETs), we realize the first CNFET CMOS-based analog circuits. We demonstrate multiple instances of a 2-stage op-amp and a front-end analog sub-system that integrates a CNFET-based breath sensor with an analog sensor interface circuit (transimpedance amplifier followed by a voltage follower to convert resistance change of the chemoresistive CNFET sensor into a buffered output voltage). These experimental demonstrations are the first reports of CNFET CMOS analog functionality that is essential for a future CNFET CMOS technology.

2) We combine the programmability of non-volatile resistive-RAM (RRAM) with CNFET-based analog circuits to experimentally demonstrate a "self-healing" circuit technique (SHARC: self-healing analog with RRAM and CNFETs) that is robust to the major inherent imperfection of m-CNTs. This is the first demonstration of CNFET-based mixed-signal circuits (4b-DAC and SAR ADC) and is the largest and most complex CNFET CMOS yet demonstrated.

1.3 Outline

Chapter 2 presents the first reported experimental demonstration of CNT CMOS analog circuits, culminating in a complete front-end analog sub-system. Chapter 3 demonstrates SHARC, a new circuit technique which overcomes the presence of m-CNTs to enable large-scale CNFET-based analog and mixed-signal circuits. Chapter 4 concludes this thesis.

Chapter 2: The First CNFET CMOS Analog Circuitry

2.1 Background

Carbon nanotubes (CNTs) are an emerging nanotechnology for next-generation electronics [Hills 2018; Shulaker 2013a]. CNTs can be used to form CNT field-effect transistors (CNFETs), which owing to their nanometer thin body (~1 nm CNT diameter) exhibit excellent electrostatic control and simultaneously high carrier transport [Appenzeller 2008; Franklin 2012; Tulevski 2014]. Due to these properties, digital circuits fabricated with CNFETs promise a 10× improvement in energy-delay product (EDP: a metric of energy efficiency), versus silicon FETs [Hills 2018].

Despite these advantages, there remain major challenges towards realizing a future CNFET technology. While a full complementary (CMOS) CNFET technology is required to realize the above energy-efficiency benefits [Weste 2010], all complete digital CNFET systems have been fabricated from PMOS-only CNFETs [Shulaker 2013a; Shulaker 2013b; Shulaker 2014; Shulaker 2017], and all reported CNFET CMOS demonstrations have been limited to only individual devices, small-scale circuits, or digital logic [Lau 2018; Shahrjerdi 2013; Yang 2017; Suriyasena Liyanage 2014; Zhang 2011; Ha 2015]. Importantly, due to the lack of a robust CNFET CMOS process, there has been no reported demonstration of CNFET CMOS analog circuitry (while the vast majority of circuitry in a system today is digital logic, analog circuits are still essential for applications ranging from sense amplifiers for memory arrays to high speed input/output links [Hodges 2004]). Moreover, similar to benefits for digital logic, CNFET CMOS promise analog circuit performance benefits, providing additional motivation to realize CNFET CMOS for analog circuitry (Fig. 2.1).

First, I summarize our CNFET CMOS process flow (Chapter 2.2), followed by illustrating how we leverage this process to realize the first CNFET CMOS analog circuits (Chapter 2.3).

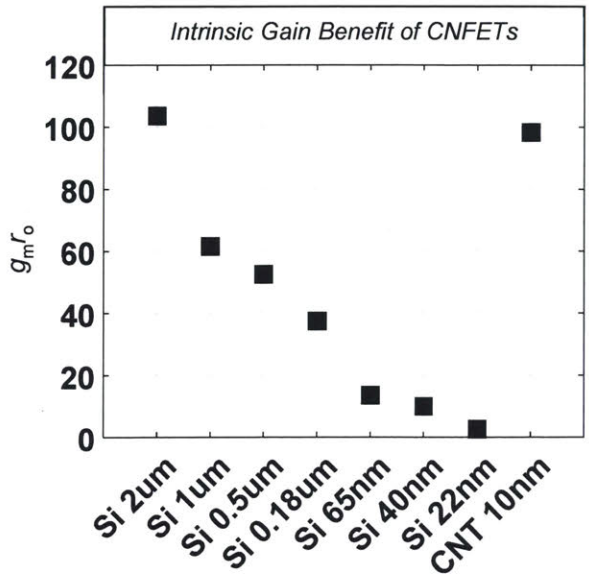

Figure 2.1: Intrinsic gain ($g_m r_o$) [Razavi 2017] benefits of CNFETs. The intrinsic gain is extracted from circuit simulations (Cadence Spectre®) using commercial process design kits (PDKs) for silicon CMOS and using an experimentally calibrated compact model for CNFETs (calibrated using CNFETs with sub-10 nm channel length) [Lee 2015].

2.2 CNFET CMOS Process Flow

Fig. 2.2 shows our CNFET CMOS fabrication flow [Lau 2018]. The CNFETs are fabricated with a back-gate device structure with a metal gate (Pt) and high-*k* gate dielectric (20 nm HfO_2 deposited through atomic layer

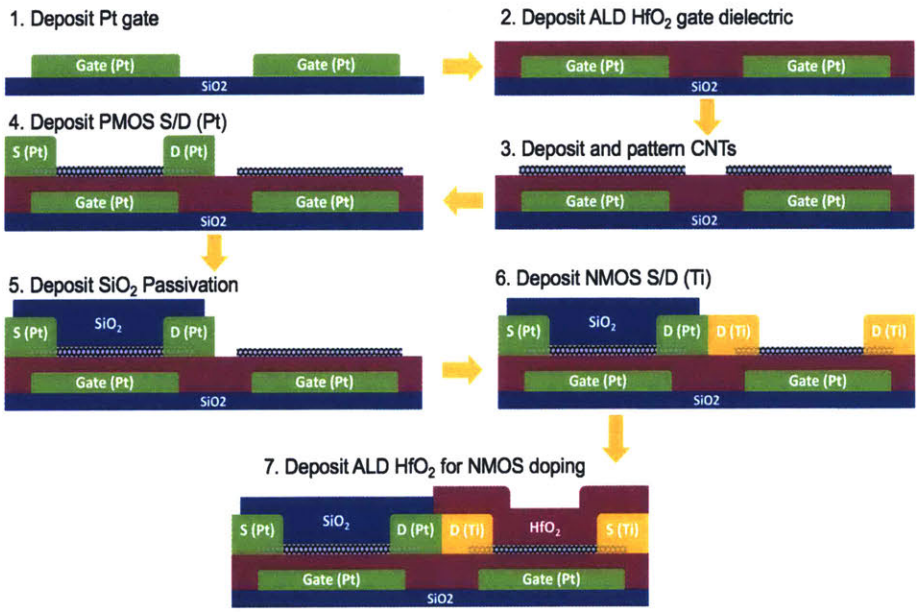

Figure 2.2: CNFET CMOS process flow. A back-gate geometry is used for both the PMOS and NMOS CNFETs. All low-temperature (<250 °C) processing is performed with solid-state and silicon CMOS compatible materials.

deposition, ALD). Post gate-stack fabrication, the CNTs are deposited through a solution-based incubation process [NanoIntegris]. This solution-based CNT deposition enables the entire CNFET fabrication process to be low temperature (<250 °C)[b]. To fabricate the PMOS and NMOS CNFETs, we leverage a dual doping strategy which uses both source and drain metal contact work function engineering as well as oxide-based electrostatic doping. The source and drain are lithographically patterned (0.5 nm Ti / 45 nm Pt for PMOS, 75 nm Ti for NMOS), and the PMOS CNFETs are encapsulated with SiO_X while the NMOS devices are encapsulated with ALD-deposited HfO_X (the stoichiometry of the SiO_X and HfO_X sets the threshold voltage of the PMOS and NMOS, respectively). This CNFET CMOS process leverages only solid-state and silicon CMOS compatible materials, and results in well-matched PMOS and NMOS CNFETs (Fig. 2.3).

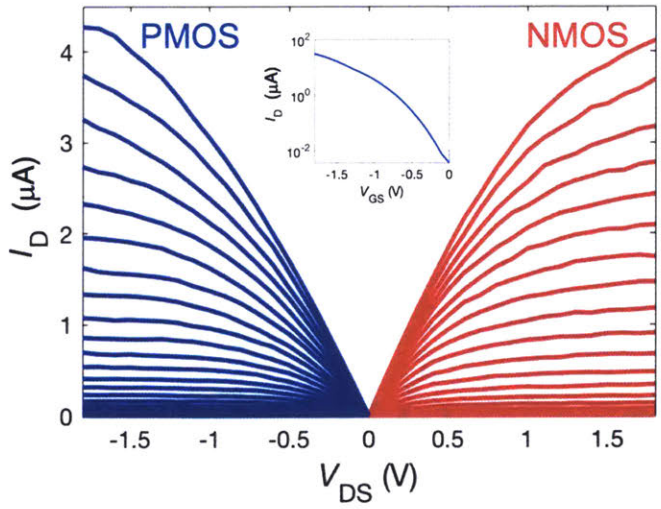

Figure 2.3: Characteristics of PMOS and NMOS CNFETs with a channel length of ~2.5 μm and width of ~4 μm. I_D-V_{DS} curves show well-matched CNFET CMOS (i.e., with similar on-current for both NMOS and PMOS). V_{GS} range from 0 V to V_{DD} (1.8 V) with an increment of 0.1 V (for NMOS, V_{GS} from 0 to -V_{DD} for PMOS). Inset shows an I_D-V_{GS} curve of a PMOS CNFET with I_{ON}/I_{OFF} > 8000.

2.3 Experimental Demonstration of CNFET CMOS Analog Circuitry

As an initial demonstration of CNFET-based analog circuits, we fabricate a fundamental analog building-block: a two-stage op-amp [Razavi 2017]. Fig. 2.4a displays the circuit schematic of our two-stage op-amp, while Fig 2.4b shows a scanning electron microscopy (SEM) image of a fabricated CNFET CMOS op-amp. Fig. 2.4c displays a voltage transfer curve for a differential amplifier (the first stage of the op-amp shown in

[b] The high-temperature growth process of CNTs is decoupled from the wafer substrate by using a solution-based incubation process to deposit CNTs. Such low-temperature fabrication enables greater CNFET integration, as the CNFETs can be fabricated in the back-end-of-line (BEOL) directly over silicon CMOS substrates.

Fig. 2.4a). Measurements of multiple instances of a two-stage op-amp are overlaid in Fig. 2.4d, where the differential input voltage ($\Delta V_{in} = V_{in}^{+} - V_{in}^{-}$) is swept from -1 to 1 V (with a supply voltage of 2 V). The op-amp achieves a maximum gain >700 (Fig. 2.4e). Device mismatch is minimal, with the average offset voltage (V_{OFFSET}, defined as the differential input voltage that achieves maximum gain) being $V_{OFFSET} < 12$ mV.

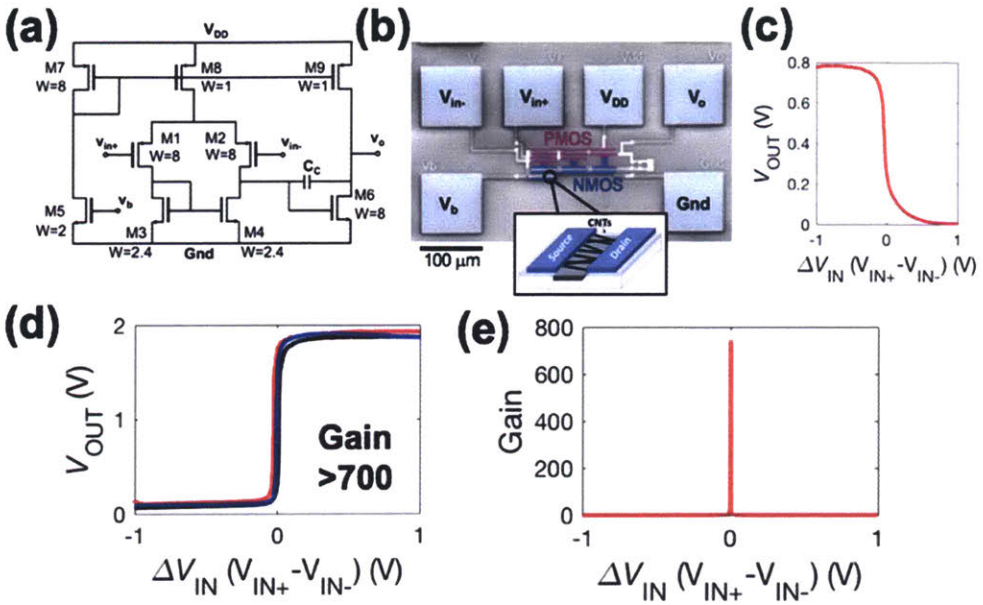

Figure 2.4: Experimental demonstration of a single-ended two-stage op-amp using CNFETs. a) The topology of the op-amp is a differential amplifier followed by a common-source 2nd stage. b) SEM of the fabricated op-amp. c) Measured waveforms of a CNFET-based differential amplifier (first stage of the two-stage topology) and d) multiple (three) instances of a two-stage op-amp, where the output voltage is a function of ΔV_{in} ($V_{in}^{+} - V_{in}^{-}$). The output swing is >90% of V_{DD} and average $V_{OFFSET} < 12$ mV, indicating well-matched devices. e) Derivative of the transfer-curve for the two-stage op-amp, showing gain >700.

Leveraging this building block, we demonstrate a CNFET-based analog sub-system: a front-end integrated sensor and sensor interface circuit that converts the resistance change of a chemoresistive CNFET sensor into a buffered output voltage. The sub-system consists of a transimpedance amplifier (TIA) to convert the input current (a function of the chemoresistive CNFET sensor) to a voltage, cascaded to a voltage buffer. To characterize the sub-system, we initially fabricate the circuit shown in Fig. 2.5a. The CNFET chemoresistive gas sensor is replaced with an externally controlled current source (I_{IN}) to remove any variability introduced by the sensor itself. An SEM (false-colored for clarity) of the fabricated circuit is shown in Fig. 2.5b. To characterize the circuit, we sweep a DC current at the input of the system and measure the corresponding voltage output from the voltage buffer. Fig. 2.5c shows the measured output (with a 2 V supply voltage); as

expected, the output voltage changes linearly with the input current over the entire input range (10 μA to 50 μA, designed the match the chemoresistive sensor). To quantify the linearity of the response, we calculate the coefficient of determination, R^2, for the measured response to a best-fit linear line [Rao 2001]. The average R^2 across the entire input range is 0.999, illustrating high linearity (*e.g.*, the measured response closely follows a linear relationship to input current). Moreover, Fig. 2.5d shows 100 repeated measured waveforms overlaid on top of one-another, illustrating robust operation with minimal drift.

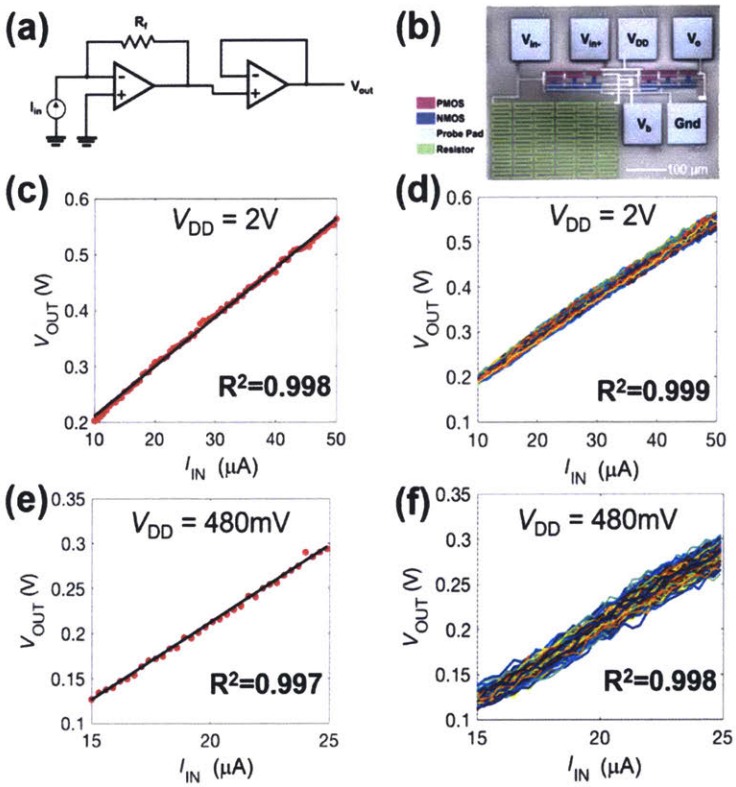

Figure 2.5: Characterization of analog sub-system, with the CNFET sensor replaced with an external current source. (a-b) Schematic and SEM. (c) Measured linear response of the sub-system, converting input current to output voltage. (d) 100 repeated measurement cycles, illustrating minimum drift. (e-f) Repeated measurements of (c-d), with supply voltage reduced from 2 V to 480 mV. Functionality and linearity are not sacrificed even at scaled <500 mV supply voltages.

Additionally, we show the CNFET CMOS circuitry can operate at scaled supply voltages without degrading key circuit performance metrics. Fig. 2.5(e-f) shows the response of the system with a scaled 480 mV supply voltage. The measured response still exhibits high linearity (R^2 value of 0.998 to a best-fit linear line), as well as similarly minimal drift over 100 repeated measurements.

Fig. 2.6 shows the complete integrated sensor and sensor interface sub-system. As shown in the schematic in Fig. 2.6a, an on-chip integrated CNFET chemoresistive gas sensor replaces the external DC current supply

at the input of the TIA. The CNFET chemoresistive gas sensor is fabricated using the same process flow shown in Fig. 2.2[c], but all of the oxide covering the CNFET chemoresistive gas sensor is removed with a dilute HF wet etch[d]. Thus, the CNFET chemoresistive gas sensor is exposed to the environment, while all other CNFETs (e.g., the CNFETs comprising the amplifiers) are encapsulated with a dielectric and are thus protected from the ambient. An SEM of the fabricated sub-system is shown in Fig. 2.6b. To characterize the response of the sub-system, the sensor is kept in a controlled constant ambient (*e.g.*, dry air), and the input voltage (V_{IN}, Fig. 2.6c-d) applied across the sensor is swept. Similar to the sub-system in Fig. 2.5 with a constant current source as the input, the measured output voltage (V_{OUT}) of the sub-system exhibits high

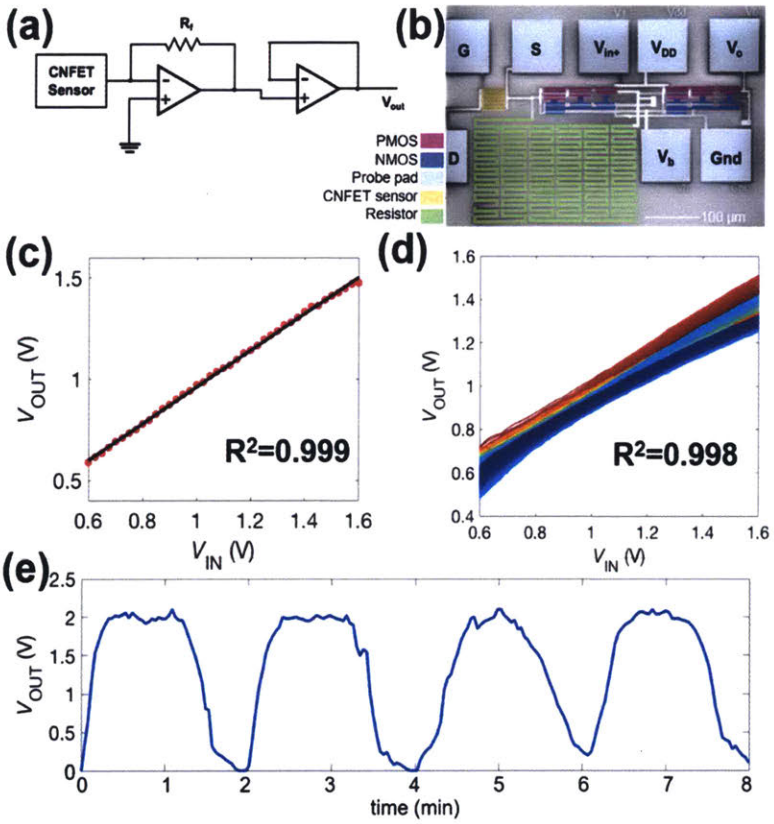

Figure 2.6: Characterization of analog sub-system, with an on-chip integrated CNFET chemoresistive breath sensor. (a-b) schematic and SEM. (c) Measured linear response of the sub-system, measured by keeping the sensor in N_2 ambient air and sweeping the input voltage, V_{IN+}, applied across the sensor. The response is highly linear with a R^2 value of 0.999. (d) 10,000 repeated measurement cycles, illustrating minimum drift. The first 2500 cycles are red, the next 2500 cycles are yellow, the next 2500 cycles and light blue, and the last 2500 cycles are dark blue. The spread in the measured outputs is not random noise, but rather minor slow drift of the circuit after constant measuring for 12 hours. Future work can improve upon stability by optimizing the gate stack to minimize interface traps at the CNT-gate dielectric interface. (e) Measured response of the sub-system in response to alternative exposures to warm breath and N_2. The oscillating response in the circuit illustrates correct functionality of the integrated sensor/ sensor interface circuit.

[c] The CNFET chemoresistive gas sensor is also functionalized with a polymer to increase its sensitivity to ambient conditions. There is rich literature describing the design and fabrication of CNFET gas sensors (Kong 2000; Liu 2015; Zhang 2006).

[d] The dilute HF wet etch has a high etch selectivity of SiO_X over HfO_X and does not etch or degrade the CNTs.

linearity (R^2 value of 0.999 to a best-fit linear line). Moreover, Fig. 2.6d shows the circuit is robust and air-stable: 10,000 repeated DC measurements performed over 12 hours illustrate minimal drift.

To test the full integrated sensor and sensor interface circuity, we alternate between one-minute intervals of breathing and blowing N_2 gas directly over the sensor. The CNFET gas sensor reversibly responds to warm breath, resulting in the front-end sub-system voltage output toggling between ~0 V and ~2 V, illustrating correct functionality of the circuit with successful detection and response to breath.

2.4 Conclusion

We present the first demonstration of CNFET CMOS analog circuits by fabricating foundational building block op-amps up to an analog-based sensor interface circuit. As an experimental demonstration, we integrate the sensor interface circuit with an on-chip chemoresistive CNFET gas sensor, illustrating response and detection of breath. The CNFET CMOS analog circuits achieve high gain (>700) and linearity and operate at scaled sub-500 mV supply voltages (without sacrificing linearity). Thus, this experimental work is a key step towards demonstrating analog functionality that is essential for a future CNFET CMOS technology.

Chapter 3: SHARC – Self Healing Analog with RRAM and CNFETs

3.1 Background

While CNFETs promise performance benefits for analog circuitry, CNTs suffer from a major inherent imperfection: every ensemble of CNTs contains some metallic-CNTs (m-CNTs), which cause an electrical short between the CNFET source and drain. This results in substantial leakage current and degradation in circuit performance (or even catastrophic circuit failure). Although techniques have been developed to further purify CNT solutions and enable the demonstration of digital CNFET circuits (digital circuits can still maintain correct functional operation even in the presence of a limited number of m-CNTs) [Zhang 2009],

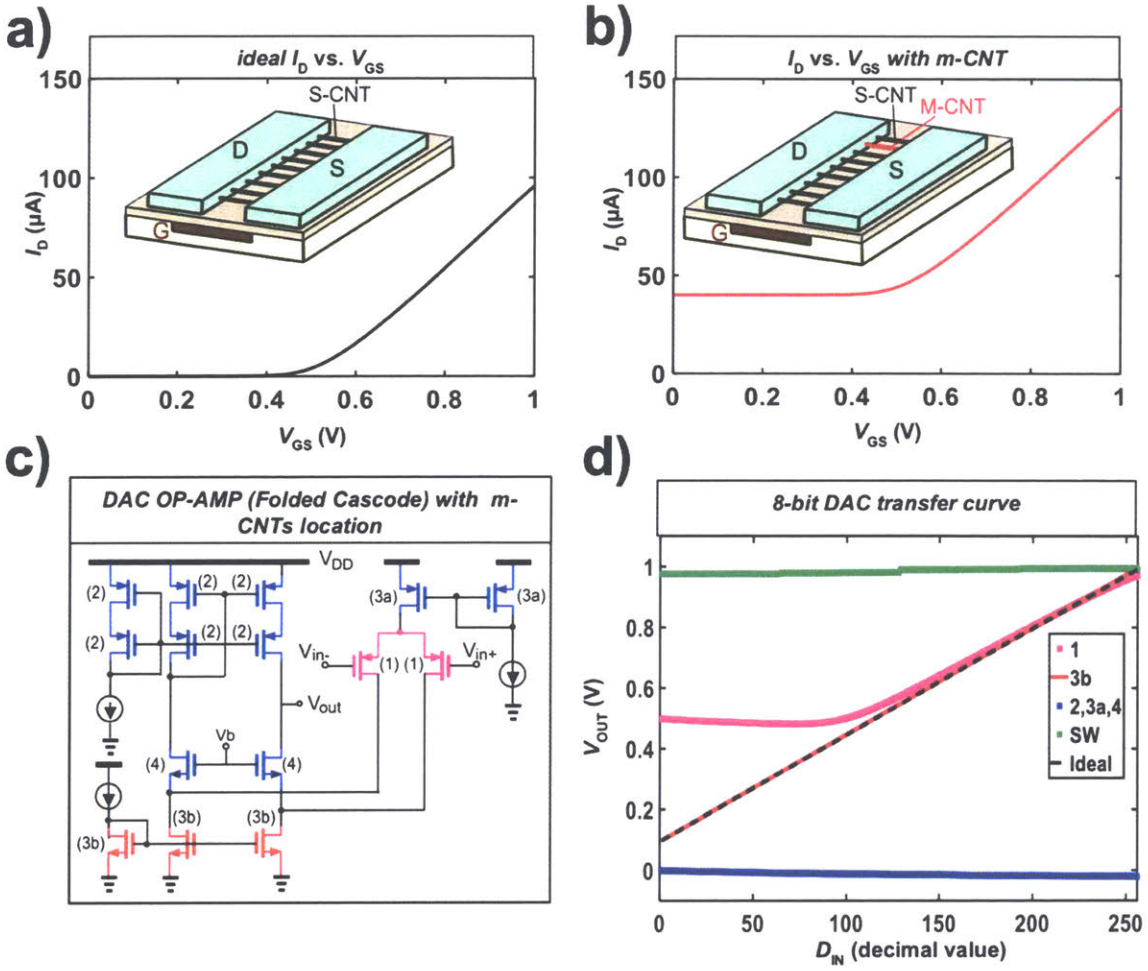

Figure 3.1: CNFET schematics and I_D-V_{GS} curves for a) a CNFET with all semiconducting-CNTs (s-CNTs) and b) a CNFET with a single m-CNT. Leakage current (defined as the current through the transistor when it is off) is higher in the presence of an m-CNT. c) Schematic of an 8-bit DAC designed with an op-amp. Transistors in the DAC are color-coded to match d) graph of the output voltage of the DAC with different placements of a single m-CNT in the CNFET channel. The compact model used for circuit simulations is calibrated to experimental data for the 10 nm technology node (m-CNT off-state resistance is 25 KΩ).

m-CNTs present a major obstacle to realizing large-scale analog and mixed-signal circuits. The effects of a single m-CNT on the performance of an 8-bit DAC are displayed in Fig. 3.1 for different locations of the m-CNT within the circuit, illustrating that even a *single* m-CNT can cause catastrophic circuit failure for analog circuits (*e.g.*, the output of the DAC latches to either V_{DD} of ground due to a single m-CNT placed within a single CNFET in the circuit).

3.2 Principles of SHARC

Here, we present a new circuit design technique that overcomes the presence of m-CNTs in analog circuits. By combining the programmability of non-volatile resistive-RAM (RRAM) with the ability to fabricate monolithic 3D circuits with CNFETs, we demonstrate a circuit design technique whereby a circuit can "self-heal" in the presence of m-CNTs.

The process of SHARC is displayed in Fig. 3.2. First, CNFETs are fabricated, with each CNFET in the circuit topology split into multiple minimum-width FETs (which we refer to as "sub-CNFETs"). An RRAM cell is fabricated directly over (or under) the source or drain contact of each CNFET so that each CNFET is in series with an RRAM cell. Critically, the RRAM fabrication directly over or under the sub-CNFET contact minimizes the area penalty of SHARC and is directly enabled by the low-temperature fabrication of the CNFETs and RRAM (*e.g.*, the high-temperature >1000 °C fabrication of silicon FETs would damage or destroy any devices previously fabricated underneath the silicon FET on a wafer). Both RRAM and CNFETs require <400 °C processing, and thus naturally enable such heterogeneous monolithic 3D integration.

After fabricating the RRAM and CNFETs, the RRAM cells are then "formed" by applying a positive voltage across the RRAM electrodes, which sets the RRAM into a low-resistance state (LRS). The RRAM stack is designed so that its form voltage is higher than the operating voltage of the circuit, preventing any unwanted programming of the RRAM during circuit operation. Next, a voltage is applied across the source and drain of each CNFET, with the gates of the CNFETs biased so that each transistor is in its off-state (*e.g.*, $|V_{GS}| < |V_{TH}|$). Thus, if a CNFET contains only semiconducting CNTs (s-CNTs), it will not conduct current. However, if a CNFET contains an m-CNT, the m-CNT is ungated and thus still conducts current. With

sufficient biasing and current, the RRAM in series with CNFETs containing m-CNTs are reset to their high-resistance state (HRS). This effectively "self-heals" the circuit, by automatically programming the RRAM in series with CNFETs containing m-CNTs in a high-resistance, effectively removing that CNFET from the circuit. To ensure proper resetting of the RRAM, the reset current of the RRAM should be designed to be less than the off-state leakage current through an m-CNT (<100 μA for a scaled technology node). The last step in the SHARC process is to fabricate the final metal layers of the circuit. The final result is a CNFET circuit where sub-CNFETs containing only s-CNTs are in series with RRAM in a LRS, while sub-CNFETs containing any m-CNTs are in series with RRAM in a HRS. Post self-healing, CNFETs containing m-CNTs experimentally exhibit $I_{ON}/I_{OFF} > 1000$ and I_{OFF} reduces >800×.

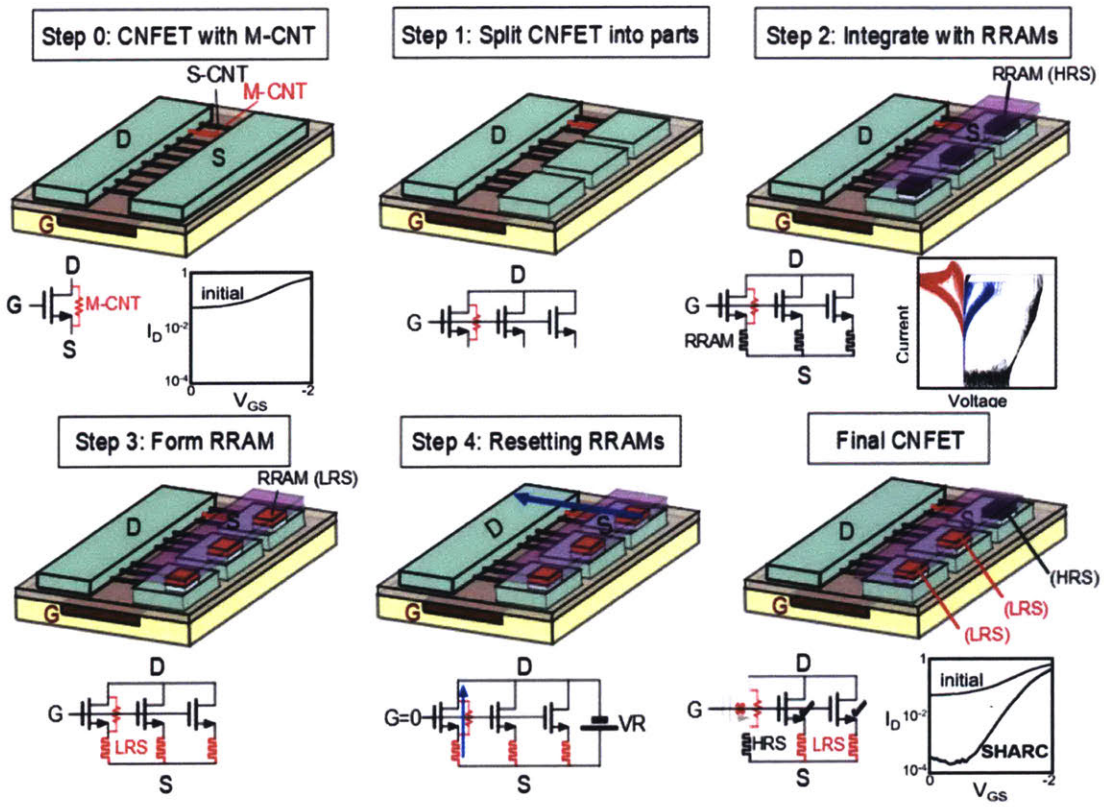

Figure 3.2: Principles of SHARC. The initial and final I_D-V_{GS} curves when using SHARC are shown in step 0 and the final step. I_{ON}/I_{OFF} of all sub-CNFETs combined is improved from ~10 before SHARC to >1000 in the final step. Steps 1 through 4 illustrate how the RRAM is first formed to a low-resistance state (LRS) and then reset to a high-resistance state (HRS) in the presence of an m-CNT. In the final step, an RRAM in a high-resistance state is shown in series with a sub-CNFET containing an m-CNT.

SHARC is a broad technique that can be applied to a wide range of analog circuit blocks and scales to larger-scale circuits, since SHARC only has to be performed once for all CNFETs in parallel. Additional parameters

in the circuit design of SHARC, such as the minimum ratio between RRAM high- and low-resistance states (in order to prevent drawing excessive current from the power supply) or RRAM cell placement (*e.g.*, on the drain of input CNFETs instead of the source), must also be taken into consideration, and are analyzed in detail in [Amer 2019].

The key benefits of SHARC are: (1) since the m-CNTs provide the current path for resetting the RRAM during the self-healing process (*e.g.*, RRAM programming), the self-healing process occurs automatically (2) because of the low-temperature fabrication of both CNFETs and RRAM (<300 °C), they can be fabricated directly vertically overlapping one-another in a monolithic three-dimensional fashion, minimizing area penalty associated with SHARC, and (3) RRAM is non-volatile, allowing the circuit to retains its healed configuration (though due to their programmability, the RRAM can potentially be reprogrammed repeatedly in the future).

3.3 SHARC Process Flow

The fabrication process flow for SHARC is displayed in Fig. 3.3. First, the bottom electrodes of the RRAM are lithographically patterned and deposited (3 nm Ti/ 30 nm Pt), followed by deposition of the RRAM oxide (5 nm HfO_2). Prior to the deposition of the RRAM top electrodes, a 2-minute oxygen plasma descum is performed to remove any residue on the circuit's surface and prevent delamination of later metal layers. A back-gate geometry is used for the CNFETs, allowing the top RRAM electrodes and gates of the CNFETs (25 nm TiN/ 25 nm Pt) to be deposited simultaneously (this is not a requirement, but highlights how process complexity can be reduced through careful processing-circuit co-optimization). The RRAM are then formed to their low-resistance state. The CNFETs are fabricated up to the source/drain layer by the same process described in Section 2.2, with slight modifications to the source/drain metal layer (1 nm Ti/ 70 nm Pt for PMOS, 72 nm Ti/ 3 nm Pt for NMOS). A sacrificial metal layer (0.5 nm Ti/ 15 nm Al) is deposited to perform the circuit self-healing step. The sacrificial metal layer is removed, and the CNFETs are passivated and doped as described in Section 2.2. In the final step of the process, the final metal routing

layer is lithographically defined and deposited.

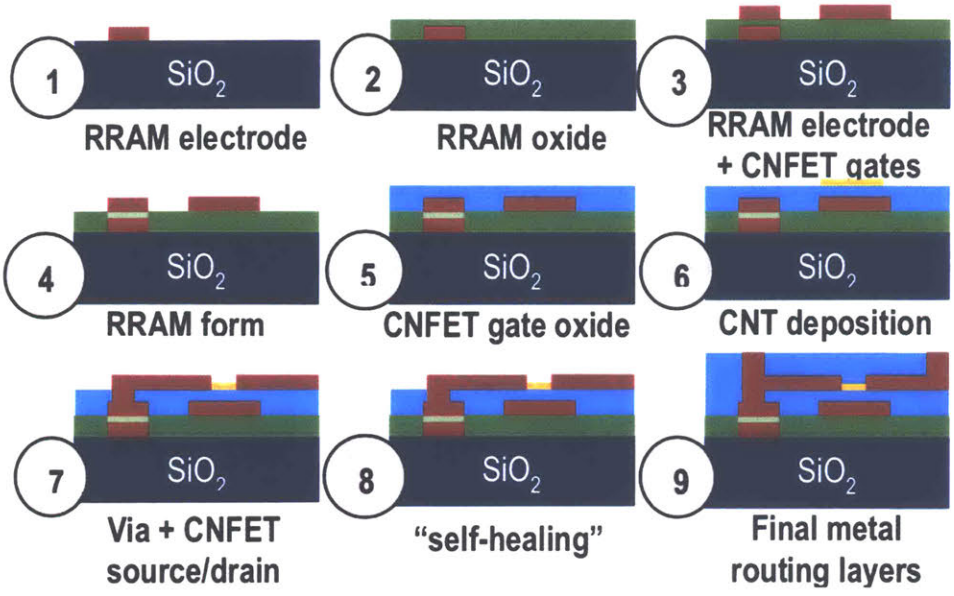

Figure 3.3: Fabrication process flow of SHARC.

3.4 Experimental Demonstration of SHARC

As an experimental demonstration of SHARC with analog and mixed-signal circuits, we use SHARC to fabricate a two-stage op-amp, 4-bit digital-to-analog converter (DAC, SHARC implemented in the two-stage op-amp and switches), and a 4-bit successive approximation register analog-to-digital converter (SAR ADC, SHARC implemented in the strong-arm latch and switches). All demonstrations are implemented at a relaxed 2 μm technology node due to the limitations of an academic fabrication facility (importantly, SHARC, the CNFET CMOS process, and all other aspects of this work can be scaled to arbitrary technology nodes). As an example of the impact of SHARC, Fig. 3.4 shows the effects of an m-CNT on a two-stage op-amp. Without SHARC, a single m-CNT within the circuit can reduce gain by >100 dB (making the amplifier an attenuator). However, with SHARC, the worst-case gain reduction is <3 dB. To illustrate a functional circuit implementing SHARC (e.g., that the circuit still functions with the full monolithic 3D process flow integrating RRAM and CNFETs), we fabricate this two-stage op-amp using SHARC. The results are shown in Figure 3.4; gain is >800 and matches simulations performed with experimentally calibrated CNFET and RRAM compact models. Fig. 3.5 displays the schematic and die image of a 4b DAC. The measured transfer characteristics show monotonic behavior with non-linearity and

gain error (due to large parasitic caps and routing resistance). Fig. 3.6 shows the SAR ADC schematic, its die image and its transfer characteristics.

These circuits are the first demonstration of mixed-signal and complex analog CNFET circuits, and the largest and most complex reported CNFET CMOS circuits to-date (see Table 3.1 for comparison to previous works [Geier 2015; Han 2017; Tang 2018; Yang 2017; Zhang 2018]).

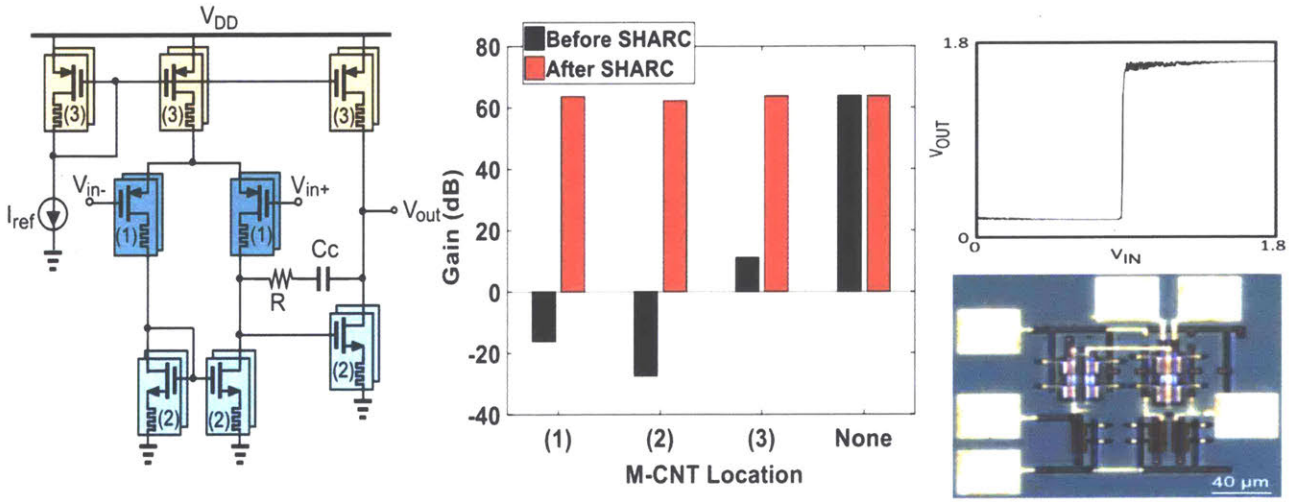

Figure 3.4: Two-stage op-amp with SHARC. (left) Schematic. (middle) Gain (dB) of op-amp when an m-CNT is located in different locations of the op-amp (labeled in schematic) before and after SHARC. Before SHARC, gain can reduce by >100 dB, while after SHARC gain is reduced by a maximum of 3 dB. (right) Die photo and experimental measurement of op-amp using SHARC, achieving gain >800.

Circuit	CNFETs per Circuit	Reference
4b-ADC	**306**	**This Work**
4-bit full adder	132	Yang et al.
Inverter	2	
SRAM Cell	6	Geier et al.
Inverter	2	Han et al.
Ring Oscillator	12	
Inverter	2	Tang et al.
Inverter	2	Zhang et al.

Table 3.1: Comparison of this work to state-of-the-art CNFET CMOS demonstrations.

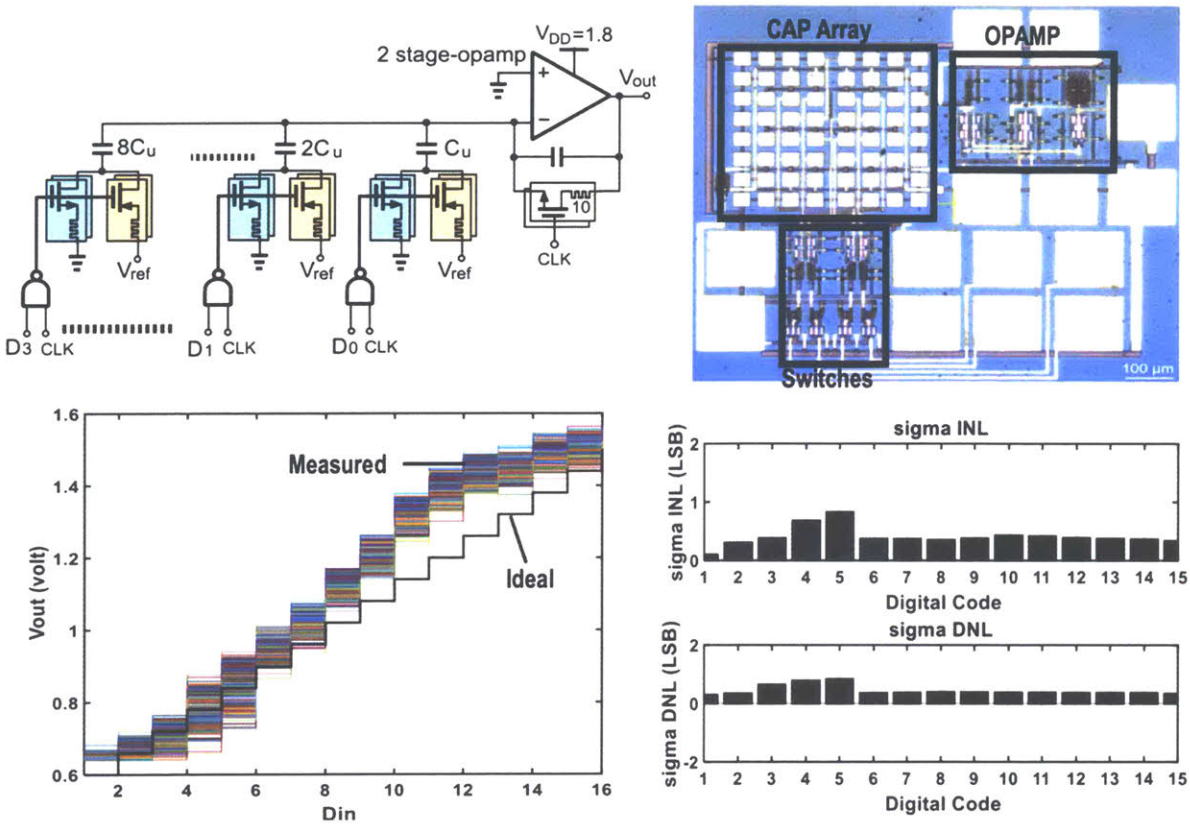

Figure 3.5: 4-bit capacitive DAC with SHARC. (top) Schematic and die photo. (bottom) Measured characteristics show the monotonic behavior with offset (50mV) and non-linearity where the maximum σ_{INL} and σ_{DNL} is 0.8 LSB.

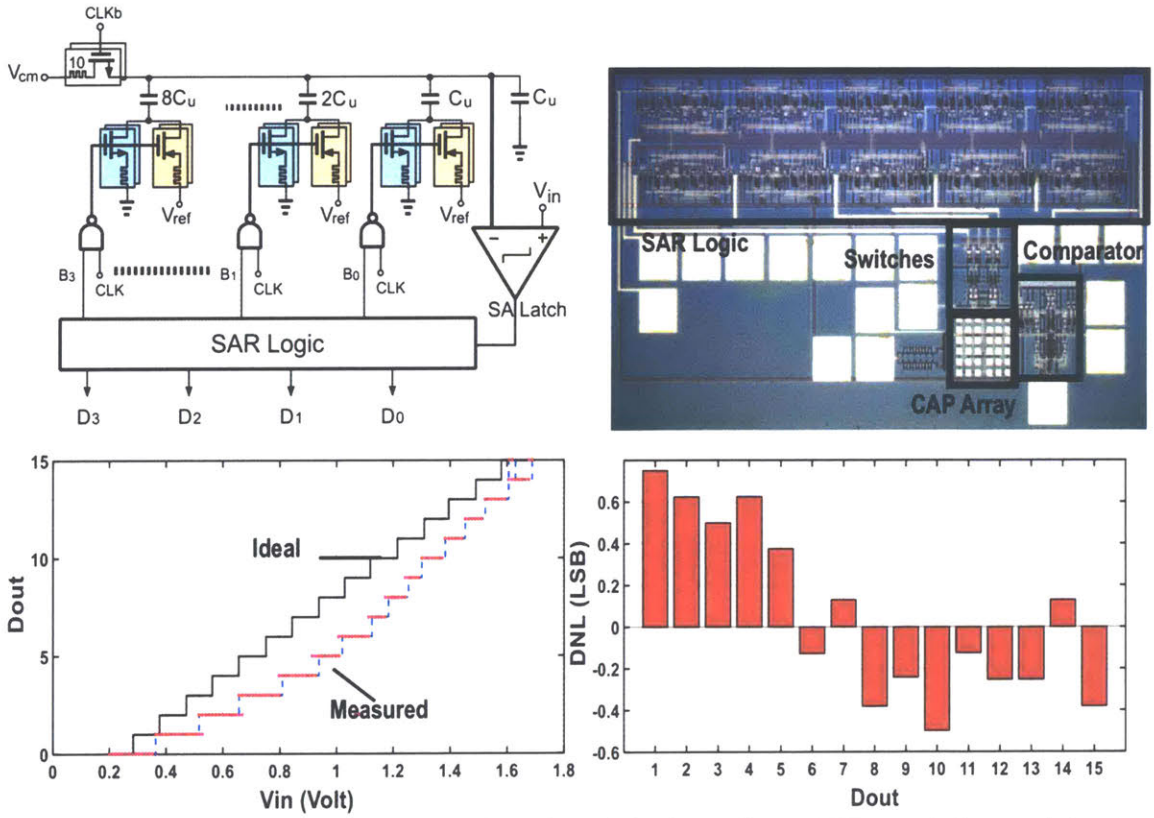

Figure 3.6: 4-Bit SAR ADC with SHARC. (top) Schematic and die photo. (bottom) Measured characteristics show the ADC behavior with offset (35mV), non-linearity and gain error whereas the DNL (-0.5 LSB→0.75 LSB).

3.5 Conclusion

We experimentally validate a new circuit design technique, SHARC, that overcomes the presence of m-CNTs on analog circuits. This technique is enabled by the programmability of non-volatile RRAM, and it utilizes the ability to fabricate monolithic 3D circuits with CNFETs. By placing RRAM in series with the CNFETs, the circuit is able to automatically "self-heal" by resetting any RRAM in series with an m-CNT to its high-resistance state. Using SHARC, we experimentally demonstrate the first mixed-signal and complex analog circuits with CNFETs. The implementation of SHARC at the CNFET-level gives it versatility; it can be combined with additional existing circuit techniques to further improve performance, such as technology node scaling to improve energy efficiency and existing circuit topologies to improve linearity. Thus, SHARC can be leveraged to realize large-scale, energy-efficient analog and mixed-signal circuits with CNFETs.

Chapter 4: Concluding Remarks

CNTs are an emerging nanotechnology that promise significant EDP benefits for digital VLSI design [Tulevski 2014; Wei 2009]. Yet despite this promise, no analog circuits have ever been demonstrated with CNFET CMOS. By leveraging our CMOS CNFET fabrication process, we experimentally demonstrate the first CNFET CMOS-based analog circuitry up to a complete analog-based sensor interface circuit.

Despite this progress, the unavoidable presence of metallic-CNTs (m-CNTs) prohibited the realization of large-scale and increasingly complex CNFET-based analog circuits. While new techniques have been developed to enable the fabrication of CNFET digital logic even in the presence of m-CNTs, a single m-CNT can cause catastrophic functional failure to analog circuits. Self-healing Analog with RRAM and CNFETs (SHARC) is a new circuit design technique to overcome the presence of m-CNTs for analog circuits. SHARC leverages heterogeneous monolithic 3D integration of CNFETs and RRAM to enable circuits to automatically "self-heal" in the presence of m-CNTs, while still maintaining transistor matching and proper operation within the circuit. With this technique, we experimentally demonstrate the first mixed-signal and complex analog circuits with CNFETs.

This work illustrates the potential – and promise – of CNFETs for analog circuitry. By demonstrating the ability to realize these analog circuit building blocks, this work is the foundation for future efforts to realize increasingly complex CNFET-based systems. For instance, by leveraging the low-temperature fabrication process of CNFETs, novel systems and architectures – such as vertical layers of sensing, sensor interface circuitry, and computing logic – can be fabricated directly over one another in a monolithic 3D fashion. Such systems will be able to capture raw data from the outside world and compute on it – all within the same chip. As progress continues to be made in these underlying nanotechnologies, we aim to realize the promise and benefits of these beyond-silicon technologies.

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