Design of a Power-Scaling, Precision Instrumentation Amplifier Using Correlated Double Sampling

by Henry W. Love

B.S., Electrical Engineering, Massachusetts Institute of Technology, 2018

Submitted to the Department of Electrical Engineering and Computer Science in Partial Fulfillment of the Requirements for the Degree of

Master of Engineering in Electrical Engineering and Computer Science

at the

Massachusetts Institute of Technology

May 2019

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Abstract

With the ever increasing prevalence of battery powered electronics and the rise of the Internet of Things (IoT), power consumption has become a critical metric for electronic devices. In a sampling system, energy can be saved by power-cycling the electronics between the samples, only consuming significant power when a measurement needs to be taken. This strategy has limitations. With today's modern electronics, when the throughput of a signal chain drops below a certain threshold, the shutdown current starts to dominate the energy consumption of the system. This is not an efficient use of energy, and creates a "power-floor," where the signal chain can not operate below a minimum power. In other words, power consumption ceases to scale linearly with the throughput of the system.

This thesis describes the design and operation of an amplifier that is intended to have low shutdown current and fast turn-on and turn-off times to minimize power consumed when not making a measurement. The proposed design is a switched capacitor circuit that uses an operational transconductance amplifier (OTA) to amplify a small differential signal produced by a sensor. The amplifier is intended to be used with the AD7686 successive approximation register (SAR) analog to digital converter (ADC) and a state-of-the-art voltage reference that has been created by Analog Devices Inc. (ADI) to efficiently power-cycle. Together, the amplifier, ADC, and voltage reference offer a complete signal chain that is capable of true power-cycling, and present a linear relationship between power consumption and sampling rate, particularly in low throughput domains, where prior technology has had difficulty doing so.

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Acknowledgements

Contents

List of Figures

List of Tables

Chapter 1

Introduction

The natural world operates in an inherently analog fashion[1] while most modern signal processing is performed in the digital domain. Bridging these two vastly different worlds are analog to digital (ADC) and digital to analog converters (DAC) that channel information between the two realms; a translator, if you will, that translates the analog language to the digital dialect and vice-versa. Without these converters, it would be difficult for computers and embedded systems to communicate with the external world. This thesis project concerns itself with the conversion of an analog signal to the digital domain, more specifically, a successive approximation (SAR) based data acquisition signal chain, focusing on the design of an energy efficient amplifier with power consumption that scales linearly with throughput/sampling rate.

1.1 Motivation for a True Power-Scaling Signal Chain

With the rise of the Internet of Things (IoT), the integration of computers into the physical world is becoming more and more desirable, and the advent of mass storage is making this transition relatively easy to accomplish. However, connecting the analog world to the digital world presents some difficulties that have still not been addressed. Difficulty arises when the throughput of a data acquisition signal chain drops to a low rate. In this situation, the signal chain is found sitting idle for a majority of time. Power-cycling can prove to be an extremely useful technique to save power while the circuit is idle. Power-cycling saves power by making the circuit active only when a sample needs to be taken, and puts the circuit in an inactive state between samples. While this certainly helps improve the efficiency of the systems, there is still shutdown, or inactive power that is consumed by the circuit while in the dormant state. Figure 1.1 below illustrates this concept [1].

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[1]At least on a macroscopic scale.
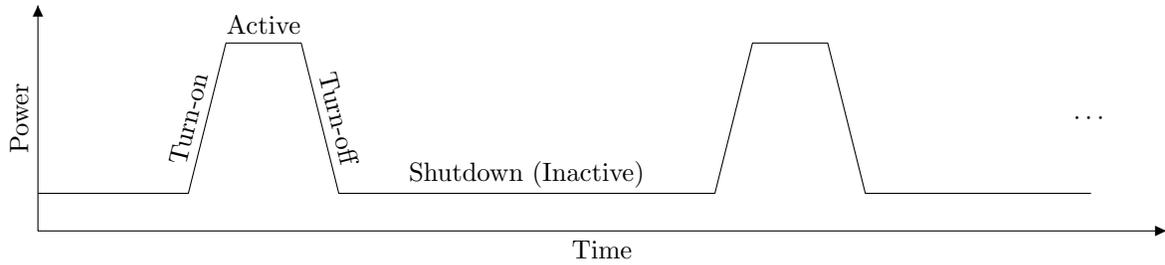
Figure 1.1: Power vs time in a typical power-cycling system

Assume a data acquisition chain is measuring at a 100Hz rate with an active power consumption of 1mW and a inactive power consumption of 1uW. When considering most low-power applications, it is the average integrated power (energy per measurement) that matters to customers. With a turn-on time of 1us (linear ramp up), an active period of 2us, a turn-off time of 2us (linear ramp down), and a corresponding inactive period of ~10ms, each operation consumes 0.5nJ, 2nJ, 1nJ, and 10nJ respectively. One can easily see that approximately 75% of energy is consumed *between* the measurements, when the system is inactive. As the example has shown, at low sampling rates, energy per measurement no longer scales with throughput, as inactive power draw dominates the energy consumption of the circuit. High power draw is acceptable as long as it is not prolonged, maintaining a low energy per measurement. Currently, SAR ADCs consume relatively fixed energy per conversion with energy consumption on the order of 10nJ/conversion for ~16-bit ADCs. Thus, the power consumption of a SAR ADCs should scale proportionally with measurement throughput. Voltage references rarely support power-cycling, however, there have been made advancements in this area recently at Analog Devices (ADI). The remaining area waiting for improvement are the amplifiers. Traditional amplifiers have incomplete power-down performance, and are typically not designed for the capacitive loads of an ADC. Furthermore, some amplifier designs have slow power-up characteristics, making it difficult to power-cycle them efficiently. Thus, it is the goal of this thesis to present an amplifier that has optimal turn-on and turn-off characteristics with minimum shutdown power, offering the widest scaling span with a truly linear relationship between power and throughput.

1.2   Canonical Data Acquisition Signal Chain

A standard data acquisition signal chain is comprised of three main elements: an amplifier, an ADC, and a voltage reference. Figure 1.2 below depicts a canonical data acquisition signal chain which utilizes a SAR ADC as the converter. A SAR ADC is of interest as this style of converter fits the larger goal of the signal chain; that is, SAR ADCs typically have fixed energy consumption per measurement; thus, to a first order, their power scales linearly with their throughput.
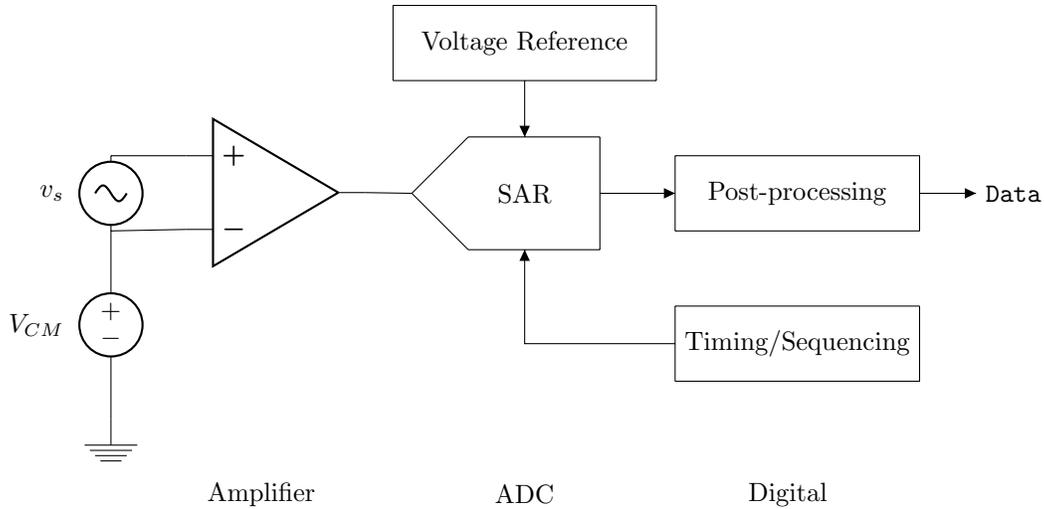
Figure 1.2: Canonical data acquisition signal chain

The purpose of the amplifier is to condition the signal of interest such that the input range of the ADC is fully utilized. The ADC converts the analog output of the amplifier to a digital code or sometimes directly interfaces with a micro controller via a digital serial protocol such as I2C or SPI. Lastly, a voltage reference is connected to the ADC to provide a sense of scale, that is, how an analog input maps to a digital output code. Ultimately, the output of the converter can be (rather abstractly) expressed as:

$$\texttt{Data} = \frac{\text{Signal}}{V_{REF}} \tag{1.1}$$

We now turn our attention to the signal source, i.e. sensor, and voltage reference. Sensors can provide absolute measurements or relative measurements. Examples of such absolute sensors include pH sensors, photo detectors, or thermocouples. The output signal these sensors provide are "absolute", depending only on the physical quantity/characteristic of what they are measuring. Thus, for the output data to be accurate, we wish to provide a voltage reference that itself is absolute and does not depend on external factors. The reference must be very stable.

In contrast, there are also ratiometric sensors; sensors that provide an output signal that depends on a factor other than just the physical property of what they are measuring. An example of such a sensor would be a Wheatstone bridge, commonly used to measure pressure. Taking this as an example, the output signal of the Wheatstone bridge depends not only on the pressure applied to the bridge, but also on the excitation voltage used to power it. Now the signal becomes some output that is a result of both the excitation voltage (V_{DD}) and the parameter being measured (pressure). In other words:

$$\texttt{Data} = \frac{\text{Signal}}{V_{REF}} = \frac{\text{Parameter} * V_{DD}}{V_{REF}} \tag{1.2}$$

If the reference voltage, V_{REF}, of the ADC is connected to the same excitation voltage (V_{DD}) of the Wheatstone bridge, this expression becomes:

$$\texttt{Data} = \frac{\text{Parameter} * V_{DD}}{V_{DD}} = \text{Parameter} \tag{1.3}$$

Thus, by using a sensor with excitation voltage that is the same as that provided to the ADC as a reference, the output data from the ADC becomes independent of the reference or excitation voltage of the sensor and solely depends on the parameter being measured. It appears to be an absolute measurement, and variations in the reference are canceled.

When either using an absolute sensor or a ratiometric sensor, we desire the output data to be solely dependent on the input signal. This can either be done by providing a extremely stable reference (in the absolute case), or by using the same sensor excitation for the voltage reference such that variations are naturally canceled (ratiometric case). This mindset is the basis behind the signal chain that is better suited for power-cycling, as proposed in the following section.

1.3   Proposed Data Acquisition Signal Chain

The section above provided insight as to how the different components of a signal chain, specifically the voltage reference and sensor voltage, impact the digital output data. The amplifier proposed in this thesis is intended to be used in a slightly different signal chain; one that is designed to be power-cycled. To accommodate power-cycling, the voltage reference is moved to the input of the ADC and a thermometer (to calibrate the voltage reference) is also added. Furthermore, architectural changes to both the voltage reference and the amplifier are made. These architectural changes are described in detail in §6.1 and §6.2. A multiplexer ensures that the outputs of the amplifier, voltage reference, and thermometer can each be independently converted by the ADC. Figure 1.3 depicts the proposed signal chain [1].
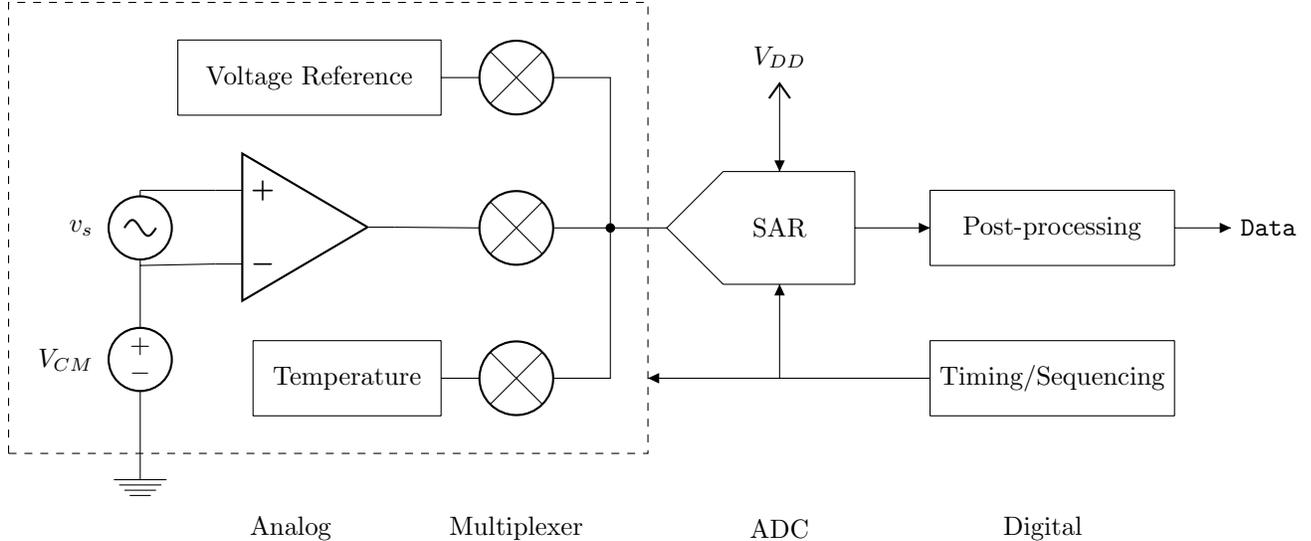
Figure 1.3: Proposed data acquisition signal chain

Ignoring the thermometer for now, the SAR ADC will first sample the voltage reference, and then the signal source. Noting that the SAR reference is connected to V_{DD}, the output data from measuring the voltage reference is:

$$\texttt{Data} = \frac{V_{REF}}{V_{DD}} \tag{1.4}$$

and the output data from the signal is:

$$\texttt{Data} = \frac{\text{Signal}}{V_{DD}} \tag{1.5}$$

If, in post-processing, Equation 1.5 is divided by Equation 1.4, the result is:

$$\texttt{Data} = \frac{\text{Signal}}{V_{REF}} \tag{1.6}$$

This result is the same obtain in Equation 1.1. In this scenario, however, the voltage reference can be turned off while not being sampled by the ADC, and the ADC reference, V_{DD}, need not be very stable.

1.4 Key Metrics

There are some notable key metrics that we must keep in mind while designing the circuitry. Of particular interest to us is energy consumed per measurement, the driving metric of this project. Energy consumed per measurement depends on two things: power consumption, and the length of time the electronics are consuming the power. We achieve optimal efficiency when the integrated power, with respect to time, is minimized. As mentioned in §1.1, there are a few varieties of power consumption: active power consumption,

inactive power consumption, and the power consumed during the transitions between the active and inactive states. Active power consumption is loosely defined as the power consumed by the electronics while they are doing useful things: amplifying a signal, converting a sample, or simply waiting for a response to settle. Inactive power consumption is defined as the power consumed while the electronics are dormant and not being used. Ideally, inactive power consumption is zero; however, in reality, leakage currents, standby currents for faster start up, and long inactive periods can cause this inactive energy consumption to become non-negligible. The turn-on/turn-off energy is typically attributed to parasitic capacitances in the circuit that need to be charged/discharged for the circuit to arrive at the proper operating point. All three types of power consumption (active, inactive, and transitional) can have a major impact on the total energy consumption of the system; the impact of each on energy consumed per measurement depends on the application and how the electronics are being used. For the low throughput application, the target of this project, inactive power consumption dominates the power consumption of the overall system; however, the power consumption due to the other states cannot be neglected. The thesis will discuss the various factors that impact the energy consumed during each state and design decisions made to minimize energy consumed per measurement. Ultimately, we strive to have fast turn-on and turn-off times, low power, and short sampling windows to drive this consumed energy per measurement as low as possible.

1.5   State of the Art, Low-Power, Precision Components

The power-scaling nature of this unique signal chain is inspired by the power-scaling behavior inherent to SAR converters. Is is difficult to compare a switched capacitor architecture to a traditional, continuous time implementation, as it is a bit like comparing apples to oranges. Nonetheless, there are still important big picture goals that are shared and should be met by both types of circuitry including low power consumption and fast settling times. The AD8236 is one of the lowest power instrumentation amplifiers in the industry, with $40\mu A$ maximum supply current [2]. This is appealing for battery-powered applications. However, the AD8236 has settling times much larger than the settling time of the amplifier proposed in this thesis, ultimately resulting in a larger consumed energy per measurement than one may initially suspect. In addition, the AD8236 is intended to be used in a continuous-time signal chain; this has the downside of making it difficult to cancel its offset voltage, as will be done with the topology described in this thesis. Finally, the AD8236 is not optimized for power-cycling, and, as we have seen in §1.1, most of the power consumption in a low throughput signal chain is attributed to the shutdown state. The LTC2063 is another state-of-the-art low-power precision component that boasts $2\mu A$ supply current; however, its leakage current (170nA per amplifier) and start-up time (2ms) are not ideal for a power-cycled application. Figure 1.4 below provides a

visual of power consumption versus throughput for components currently offered in Analog Devices' (ADI) portfolio [1]. While not all amplifiers, the graph below depicts the lack of efficient amplifiers in the precision low-power domain. The precision low-power domain is loosely defined as power $< 1\mu$W and throughput $<$ 1000SPS. The leakage current of some come common batteries, such as the CR2032, CR927, and LR44 are also plotted in the plot below. This provides insight and a frame of reference to the currents and power in question. Standby/shutdown currents lower than the leakage currents of the batteries imply the weak link is not the amplifier/active components, but rather the battery itself. Of course, if the leakage of the battery is higher than the power consumption of the electronics, then the solution is a smaller battery, which then puts the pressure back on the electronics to minimize current consumption.
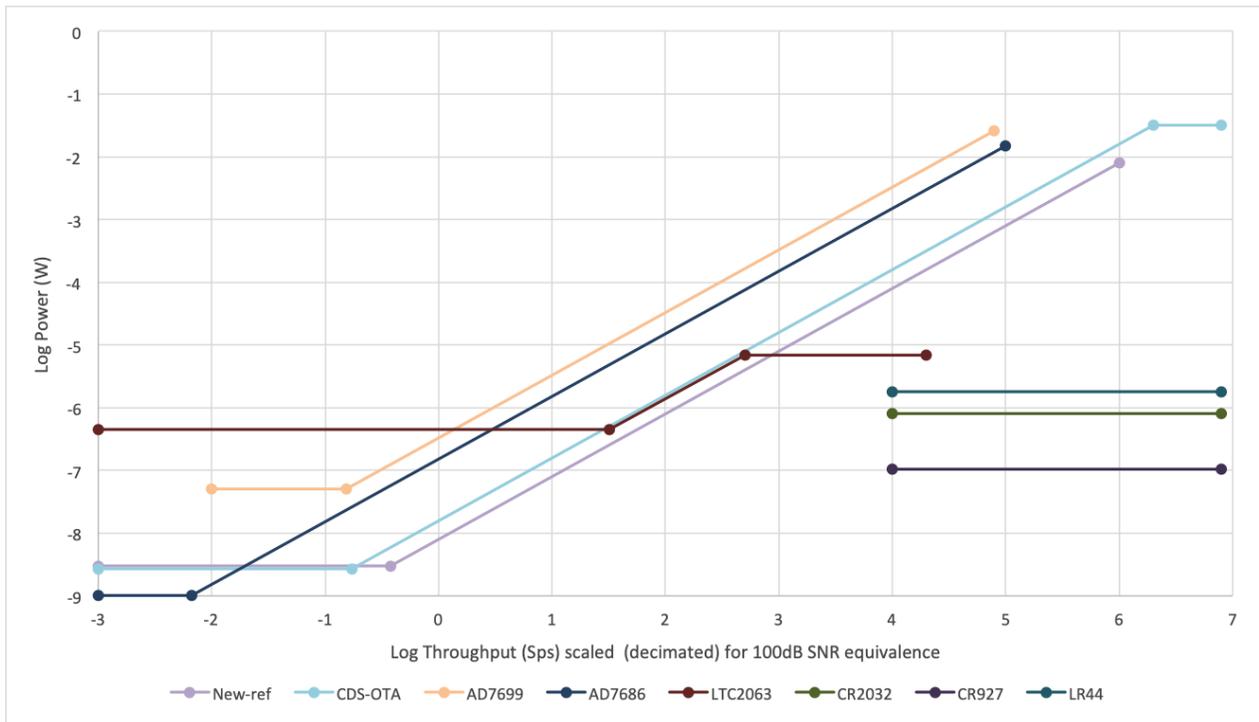
Figure 1.4: Chart of power versus measurement throughput for best-in-class low-power precision components

1.6 Target Application

It is not expected that the signal chain proposed in §1.3 will be a suitable for all applications. The signal chain is designed to optimize energy consumed per measurement when the amplifier and voltage reference are being power-cycled. This is *not* the same thing as optimizing for power consumption. If this signal chain is run in a continuous fashion, and not power-cycled, it will likely exhibit poor performance, and a more traditional signal chain will probably perform more efficiently. Therefore, the proposed signal chain

is targeted towards power-cycled systems, where the sampling and throughput of this signal chain is rather low, hence why you want to power-cycle in the first place. Thus, it is assumed that a typical signal this analog front end (AFE) will monitor will be slow in nature and will have relatively little (important) high frequency content. This lends itself to the measurement of physical systems that innately have large time constants associated with them, such as temperature, humidity, pressure, pH, etc.

1.7 Thesis Organization

This thesis is organized in a top-down fashion: high level circuity is presented in the initial chapters of the thesis, and transistor level circuit design ensues in Chapter 3. Chapter 1 describes the circuitry at the level of the signal chain, discussing trade-offs and considerations of different high-level topologies. Chapter 2 zooms in a level to the correllated double sampling (CDS) operational transconductance amplifier (OTA) and discusses the novel CDS and switched capacitor scheme. Chapter 3 goes in depth into the design of the OTA and discusses low level trade-offs and topological considerations. Simulation results (Chapter 4) follow the circuit design, along with Chapter 5, dedicated to the layout and physical creation of the circuitry. Finally, an evaluation setup is presented with some discussion regarding supporting circuitry, such as voltage and thermometer. The thesis is concluded in the last chapter, a summary of work is presented along with a plan of future steps.

Chapter 2

Approach and Concept

The motivation for a low throughput power-scaling signal chain has been addressed; thus, we turn to the high level implementation of the amplifier circuitry in this chapter. We begin by presenting a switched capacitor circuit that performs the amplification and conditioning of the signal for the ADC. After the circuit is introduced, theoretical calculations are performed and the CDS scheme is discussed. Concluding the chapter is a short discussion on high level trade-offs and ways to improve the amplifier in certain applications.

2.1   High Level Circuitry

There are some important benefits of placing an amplifier in front of an ADC: to sequester the ADC from the sensor/signal source, to scale the input signal such that the noise floor of the different elements in the signal chain is balanced, and lastly, to attenuate the common mode signals. These benefits are well acknowledged by academia and industry.

When acquiring a signal from a sensor, it is important to interfere with the signal source as little as possible. The sequestering the amplifier performs can be broken up into two areas: providing unidirectionality and impedance transformation. The unidirectionally of the amplifier ensures that what happens at the ADC input (e.g. switching noise associated with sampling and conversion) does not propagate back to the sensor and pollute the original signal. Secondly, the amplifier hopefully appears as some high impedance load[2] such that the original signal remains true to its natural value and the sensor remains unloaded by the signal acquisition chain. An amplifier may pose significantly higher input impedance to the sensor than that of the downstream circuitry. In this way, amplifiers drastically improve the accuracy of an acquisition chain.

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[2]At least when measuring voltage.

Scaling the input is important to balance the noise floor of the elements in the signal chain. This is discussed in a bit more depth in §3.1.3; however, the end goal is to scale the output of the amplifier such that it is able to cover the entire input span of the ADC while ensuring that the referred-to-input (RTI) noise of the amplifier is comparable to that of the sensor[3]. In the proposed design, the noise will be dominated by thermal noise, and the RTI thermal noise will be that of the ADC, reduced by the closed loop gain of the amplifier.

Finally, the amplifier is used to attenuate the common mode, whether it be in a relative fashion (as it is in this case) or an active attenuation. Relative attenuation refers to the amplification of the differential signal without amplification of the common mode signal. Active attenuation refers to using a resistor divider, or other means, to make the output common mode signal smaller than that at the input. While the proposed amplifier does not actively attenuate the common mode, it does not amplify it, thus making it appear smaller when compared with the amplified differential signal at the output.

As discussed in Chapter 1, inactive power becomes a critical metric for the precision low-power domain. Considering the power-cycling scheme that will be used, the amplifier must have low inactive power, fast turn-on time, low offset, low RTI noise (including $1/f$), high gain, and good common mode rejection. To address these challenges, a correlated double sampling scheme will be used. Capacitive feedback is used to minimize inactive power draw and to avoid thermal noise associated with resistors. In addition, due to the high impedance elements the low-power domain warrants, capacitive feedback is likely to consume less area than that of resistive feedback. It also becomes relatively easy to select different capacitors to program the closed loop gain of the amplifier while using capacitive feedback. An OTA structure for the amplifier is appealing due to its fast turn-on and turn-off times and its ability to drive capacitive loads. Finally pre-charge buffers will also be used to reduce input loading. Figure 2.1 below depicts the high level topology just described. Figure 2.2 is the proposed timing diagram for driving the switches and sampling the ADC shown in Figure 2.1. Please note that Figure 2.2 is not drawn to scale.

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[3]If power consumption is not a concern, the RTI noise of the amplifier should be made smaller than the noise of the sensor.
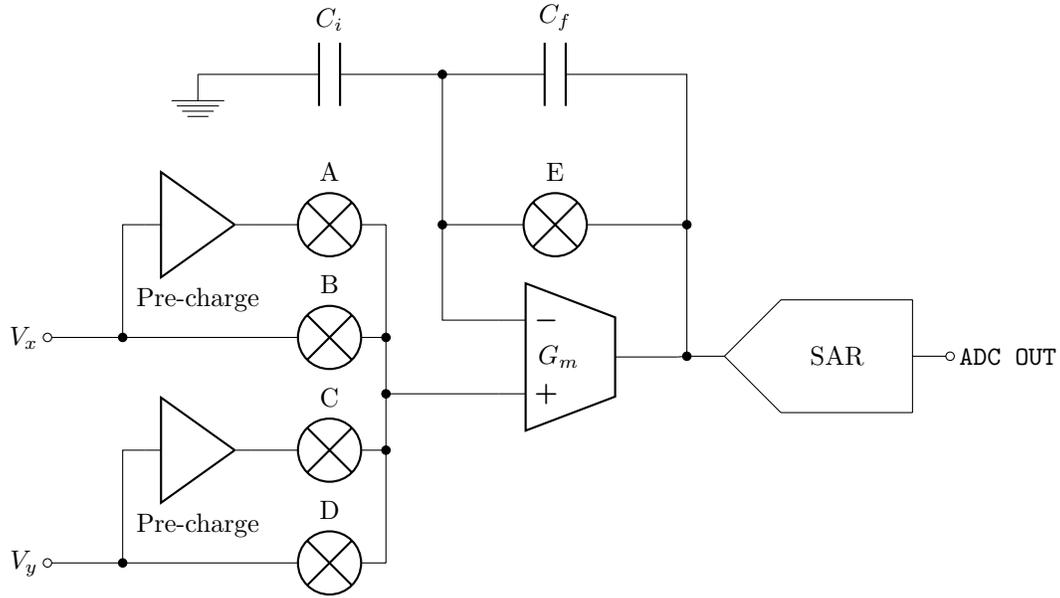
Figure 2.1: High level circuitry as proposed by Mike Coln
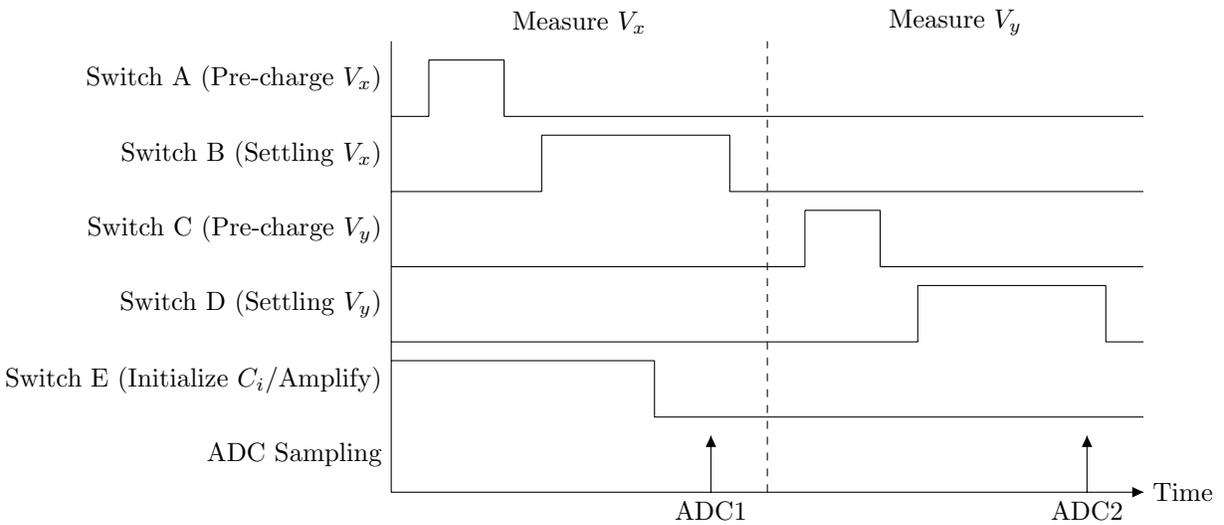
Figure 2.2: Timing diagram for one CDS event

2.1.1 Theoretical Operation

The purpose of the CDS OTA circuit shown above in Figure 2.1 is to obtain an amplified differential signal that is unaffected by errors introduced by the OTA after some processing has been performed. Errors intrinsic to the OTA and common mode voltages are eliminated by subtracting two correlated samples. One CDS cycle comprises of a combination of consecutive events, roughly depicted in Figure 2.2. First, the OTA is configured in a unity gain fashion, with the output tracking the input. Switch E clears any charge

stored on C_f, and switch A pre-charges the input of the OTA to V_x. We refer to this phase of operation as "pre-charging V_x." Next, once pre-charging V_x has completed, switch A opens, and switch B closes. Note that switch E remains closed at this point. We refer to this phase of operation as "settling V_x." After some time, switch E opens, and soon after, the ADC samples the output of the OTA. After sampling, the SAR ADC carries out its successive approximation algorithm and appears disconnected from the output. This is the first sampling event of the correlated double sampling. After the ADC completes it successive approximation algorithm, pre-charging of the input of the OTA to V_y begins, and switch C is thrown to connect the V_y buffer to the input of the OTA. After sufficient time, switch C is opened, and switch D is closed, directly amplifying V_y onto the output[4]. After time is allocated for V_y to settle, the ADC samples once more. Finally, the ADC runs its second successive approximation algorithm with the newly acquired sample. The two ADC samples, depicted in Figure 2.2 as "ADC1" and "ADC2" and sampled close together in time, are the aforementioned "correlated double samples."

The closed loop gain of the amplifier is dictated by the feedback capacitors C_i and C_f, where C_i is the capacitor from the negative input of the OTA to ground, and C_f is the capacitor bridging the output and the negative input of the OTA. We are particularly interested in the output of the amplifier when the ADC samples are taken. By means of conservation of charge, one can show:

$$V_{out,ADC1} = V_x \tag{2.1}$$

$$V_{out,ADC2} = V_y + \frac{C_i}{C_f}V_y - \frac{C_i}{C_f}V_x \tag{2.2}$$

Subtracting $V_{out,ADC2}$ from $V_{out,ADC1}$, one obtains:

$$V_{out,ADC1} - V_{out,ADC2} = \left(1 + \frac{C_i}{C_f}\right)(V_x - V_y) \tag{2.3}$$

When the author refers to the closed loop gain, please note that this is referring to $\left(1 + \frac{C_i}{C_f}\right)$ of Equation 2.3. Any offset or common mode input that is present when the ADC samples is canceled when the double samples are subtracted from each other in the processor. In addition, by nature of the architecture, an OTA driving a capacitive load presents very low noise, appearing primarily as $\frac{kT}{C}$ sampled noise. The presented scheme is promising, as it addresses and presents a solution to most of the concerns that arise with power-cycling.

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[4]In addition to the amplification of V_y to the output, there is also an offset that is proportional to V_x and the ratio of C_i/C_f.

2.2 Correlated Double Sampling

The circuit topology presented above utilizes correlated double sampling to reject errors associated with charge injection, offsets, common mode, and $1/f$ noise. As briefly mentioned already, the amplifier is configured to take two samples. Relative to the frequency content of the signal, the double sampling occurs very quickly, at a frequency much higher than that of the signal. In this way, the common mode, offsets, and differential signal can be approximated to be constant over the double sampling window - the two measurements are correlated.

If we re-visit the calculations performed in §2.1.1, and assume $V_x = \frac{1}{2}v_{diff} + V_{CM}$, $V_y = -\frac{1}{2}v_{diff} + V_{CM}$ and the amplifier has some offset, V_{os}, we find:

$$V_{out,ADC1} = \frac{1}{2}v_{diff} + V_{CM} + V_{os} \tag{2.4}$$

$$V_{out,ADC2} = \left(-\frac{1}{2}v_{diff} + V_{CM}\right) + \frac{C_i}{C_f}\left(-\frac{1}{2}v_{diff} + V_{CM}\right) - \frac{C_i}{C_f}\left(\frac{1}{2}v_{diff} + V_{CM}\right) + V_{os} \tag{2.5}$$

Subtracting $V_{out,ADC2}$ from $V_{out,ADC1}$, one obtains:

$$V_{out,ADC1} - V_{out,ADC2} = \left(1 + \frac{C_i}{C_f}\right)v_{diff} \tag{2.6}$$

The small signal, v_{diff}, is amplified, and V_{CM} and V_{os} are canceled. We will now discuss how the correlated double sampling filters some of the noise present in the signal.

There are two main noise components attributed with MOSFETs: $1/f$ noise[5] and thermal noise. $1/f$ noise is typically associated with discontinuities and traps in the silicon crystal of a MOSFET and, hence the name, has power spectral density that is inversely proportional to the frequency of the signal. That is, there is much more $1/f$ noise at lower frequencies than higher frequencies. The power spectral density of $1/f$ noise can be expressed as:

$$\overline{V_{n,1/f}^2} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \cdot \Delta f \tag{2.7}$$

Conversely, thermal noise can be largely considered as white nose, with a nearly constant power spectral density throughout the frequency spectrum. Thermal noise is due to thermal fluctuations of the unevenly

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[5]$1/f$ noise is sometimes also referred to as pink noise or flicker noise.

distributed channel resistance of the transistor and can be expressed as:

$$\overline{V_{n,th}^2} = \frac{4kT\gamma\Delta f}{g_m} \tag{2.8}$$

Where $\gamma = 1$ when the transistor is in triode, and $\gamma = 2/3$ when the transistor is in the saturation region. Depending on the spectral density of the signal of interest, $1/f$ noise may be more problematic than thermal noise, or vice-versa. The corner frequency, f_c, of the $1/f$ noise serves as a measure of what part of the frequency band is mostly corrupted by flicker noise; below this corner frequency $1/f$ noise dominates; however, above it, thermal noise dominates. The corner frequency can be determined by equating Equation 2.7 to Equation 2.8:

$$\frac{K}{C_{ox}WL} \cdot \frac{1}{f_c} \cdot \Delta f = \frac{4kT\gamma\Delta f}{g_m} \tag{2.9}$$

$$f_c = \frac{Kg_m}{4kT\gamma C_{ox}WL} \tag{2.10}$$

Because this amplifier is intended to be power-cycled, it is assumed that the signal of interest will not be varying much over time; its frequency content will largely overlap with that of the $1/f$ noise. The low frequency noise changes very little over a CDS sampling interval, assuming a short sampling interval between the double sampling; thus, it is in this way that the $1/f$ noise is rejected. Alternatively, one may consider CDS as a form of high-pass filtering for signals other than the signal being measured [4].

2.3 Advantages of an OTA Structure

An OTA is characterized by having high output resistance and a transconductance that is constant at frequencies up to the unity-gain frequency. Two stage and other multi-stage op amps are not OTAs, as it can be shown that the transconductance of the amplifier is a function of frequency. A benefit of using an OTA in this application is its fast turn-on time. Because there is no second amplifying stage, there is no internal compensation capacitor that adds an additional time constant to the turn-on time. Thus, the turn-on time is dictated by C_L, the only significant capacitor in the circuit. The correlated double sampling rejects the $1/f$ noise, and the closed-loop gain of the amplifier attenuates the RTI noise of the ADC. Because of this, the collective RTI noise is made low. Using a single stage, however, comes at the cost of gain, and therefore the design of the OTA will have to be a creative design that provides enough gain to ensure an accurate output that has approximately 16-bits of resolution. To minimize the effects of thermal noise that may not be filtered by the CDS, g_m of the input differential pair should be made large.

2.4 Pre-charge Buffers

When measuring the output voltage of a sensor, we (obviously) wish to measure the true output voltage. It turns out that this can become quite difficult to do, especially when the sensor has high output impedance and the measurement device has low input impedance. Take, for example, the Thevenin equivalent circuit of a sensor loaded by the input resistance of an amplifier.
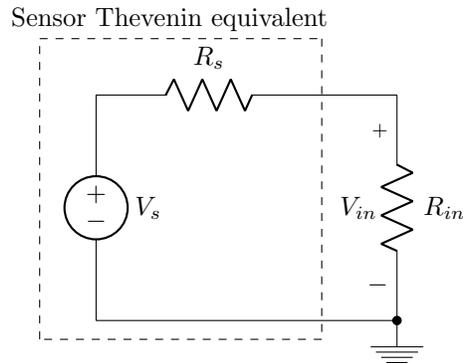
Figure 2.3: Thevenin equivalent of a sensor loaded by amplifier

If we are trying to measure the output sensor voltage, V_s, and we model our measurement device (our amplifier in this case) as some input resistance, R_{in}, we find that the voltage across the input of the amplifier can be expressed as:

$$V_{in} = \frac{R_{in}}{R_s + R_{in}} V_s \tag{2.11}$$

In the case that $R_s >> R_{in}$, very little of the sensor voltage is applied to the input of the amplifier; V_s is attenuated by the resistor divider comprised of R_{in} and R_s, exactly what we do *not* want. On the other extreme, when $R_s << R_{in}$, all of V_s is applied to the input of the amplifier. Thus, we wish to make $R_{in} >> R_s$ to efficiently couple the source voltage to the input of the amplifier without any attenuation of V_s.

For the intended region of operation, the input impedance the OTA appears capacitive; the input voltage is applied to the gate of transistors which naturally have relatively[6] large parasitic gate capacitance. Thus, we can model the input of the OTA as some capacitance that switches between V_x and V_y at some frequency f_s.

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[6]Relative to the series resistance and inductance of the gate.
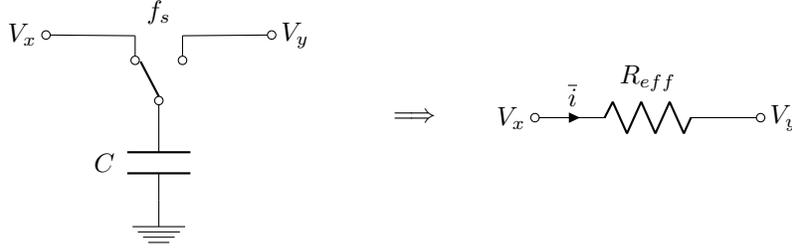
Figure 2.4: Switched capacitor approximated as a resistor

As shown in Figure 2.4, when a capacitor is switched at frequency f_s, the average current can be approximated by Ohm's law [3][7]:

$$\Delta Q = C(V_x - V_y) \tag{2.12}$$

$$\bar{i} = \Delta Q f_s = f_s(V_x - V_y) \tag{2.13}$$

$$R_{eff} = \frac{1}{f_s C} \tag{2.14}$$

Thus, returning to Figure 2.3, $R_{in} = R_{eff} = \frac{1}{f_s C}$, where C is the input capacitance of the OTA, and f_s is the frequency at which the input of the amplifier is switched between V_x and V_y. Even though there is no DC path from the input of the amplifier to ground, the amplifier still draws non-zero average current from the sensor during one CDS cycle, resulting in attenuation of V_s, as described by Equation 2.11.

To prevent loading the sensor with the virtual input impedance of the OTA described above, pre-charge buffers are employed and connected in the circuit as shown in Figure 2.1. With the pre-charge buffers, the charge required to commutate the input capacitance of the OTA between V_x and V_y no longer comes from the sensor, but rather now from the power supply. By using two pre-charge buffers for each input (V_x and V_y), the input capacitance of each pre-charge buffer remains charged at either V_x or V_y, and thus no average current flows into the buffers. By first connecting the input of the OTA to the output of the pre-charge buffer and then directly to V_x (or V_y) after the input of the OTA has charged, the input impedance of the OTA is increased.

A few considerations must be noted. First, as with anything, the pre-charge will be non-ideal. Specifically, the pre-charge buffers will have some inherent offset voltage that will cause non-zero average current to flow into the OTA when the input is switched from the output of a pre-charge buffer to V_x or V_y. Thus,

---

[7]One may recognize Figure 2.4 as an extremely powerful parity, as this concept is fundamental for switched-capacitor filters. Berkeley and UCLA often argue for credit of this idea, however, this equivalence was ultimately first realized by James C. Maxwell and presented in *A Treatise on Electricity and Magnetism* in 1873 [5] [3].

pre-charge buffers will only be useful in the event that their offsets are smaller than the differential signal, $V_x - V_y$. One may argue that as long as the offset voltages of the pre-charge buffers are the same, their offsets will not impact the measurement of $V_x - V_y$; this is indeed true, however, a dangerous assumption to make. Because it is possible for the offsets of the pre-charge buffers to differ in reality, V_x (or V_y) can be directly connected to the input of the OTA via switch B (or D) after the pre-charge buffers have done their job and charged the input capacitance of the OTA sufficiently close to V_x or V_y. Second, the pre-charge buffers add complexity, area, and power consumption to the design of the amplifier. These are trade-offs we recognize and have accepted. Each pre-charge buffer has a dedicated shutdown pin; thus, if the they prove not useful in certain applications, the amplifier can be operated without them.

2.4.1 Sensor Modeling

There are a plethora of sensors, each capable of measuring different physical phenomena, and sometimes not always providing an electrical output as simple as a voltage waveform. However, for a large portion of the cases, a sensor output can be considered as, or converted to, a small differential voltage that rides on top of a common mode component. Therefore, for simulation purposes, we assume the sensor provides a small signal voltage to the input of the amplifier accompanied by a characteristic source resistance, R_s. As we observed above, the source resistance of the sensor can have significant impact on the voltage applied to the input of the amplifier. Table 2.1 below provides a brief overview of typical source resistances of sensors that can output a low frequency differential voltage and have the potential to interface with this amplifier. Note that these are order of magnitude approximations, not exact values.

Phenomena	**Sensor**	**Typical R_s**
Chemical	pH	10MΩ - 1GΩ [11]
	CO	1kΩ - 10kΩ [12]
Force, Weight, Torque, Pressure	Piezoelectric	100MΩ [13]
	Wheatstone Bridge	100Ω - 10kΩ
Magnetic	Hall Effect	0.1Ω - 1Ω [14] [15]
Temperature	Thermocouple	< 1Ω
Motion and Vibration	Accelerometer	0.1Ω - 10kΩ [16] [17]
Flow	Magnetic Flowmeter	10Ω - 10MΩ [18]

Table 2.1: Source resistances for a variety of sensors

The source impedance of the sensor is not the only concern; bandwidth is also a limiting factor. Continuously biased sensors, or sensors that have difficulty turning on/off contradict the power-cycling nature of this project; therefore, sensors such as these, often found as gas sensors, will probably not fit well with the overall goal of the signal chain. In addition, the sensor should not consume significantly more power than the

other components of the signal chain. A thermocouple may be a nice fit for this scheme as it does not need to be biased by a power supply and the resultant signals are typically low frequency. In addition, its low series resistance minimizes the thermal noise voltage at the input of the amplifier. Unsurprisingly, we find ourselves looking for the same key metrics in the sensor as we did in the amplifier; the ability to start-up (and shutdown) quickly, low inactive power consumption, and, less importantly, low active power consumption. Together, these minimize the energy consumed per measurement, and allow for the power-scaling attribute.

For simulation purposes, $R_s = 2\text{M}\Omega$ was used to capture the behavior of the signal chain when non-negligible source impedance is included. The switching frequency of the CDS scheme and the input capacitance of the OTA roughly determines how large of a source impedance is acceptable; therefore, this should not be considered the absolute maximum R_s the amplifier can support. A 2MΩ source impedance sufficiently captures the range of output impedances depicted in Table 2.1, minus a few outliers.

Chapter 3

Circuit Design

This chapter describes the process of deciding on a circuit topology for the amplifier in the correlated double sampling scheme. Topological trade-offs are addressed, and device sizes are included. A discussion on the circuit design for the supporting structures such as biasing networks, switches, and digital logic follows the main amplifier design.

3.1 Design Decisions

Unlike an amplifier that is designed to a specific customer's needs and/or specifications, this amplifier was devised using approximate back of the envelope calculations that provide enough guidance to lead to a final design. The process of arriving at these specifications is described below. Once design decisions have been made, physical circuit design ensues.

3.1.1 ADC Decision

The design of the amplifier hinges on the SAR ADC it will precede. The purpose of this thesis is not to squeeze every last drop of performance out of the amplifier, but rather to propose a proof-of-concept solution to the presented power-cycling issue, hopefully improving the performance of the signal chain by at least an order of magnitude in some areas such as power consumption and turn-on/turn-off speed. Because of this, the selected ADC is the AD7686, a modest 16-bit 500kSPS PulSAR ADC. The AD7686's power dissipation scales linearly with throughput and has a standby current of 1nA. It has a single-ended input with a single supply voltage of 5V. All of these characteristics were important considerations when selecting this ADC to design the amplifier around. According to the AD7686 datasheet, the input structure of the ADC can be modeled as shown in Figure 3.1 below.

29
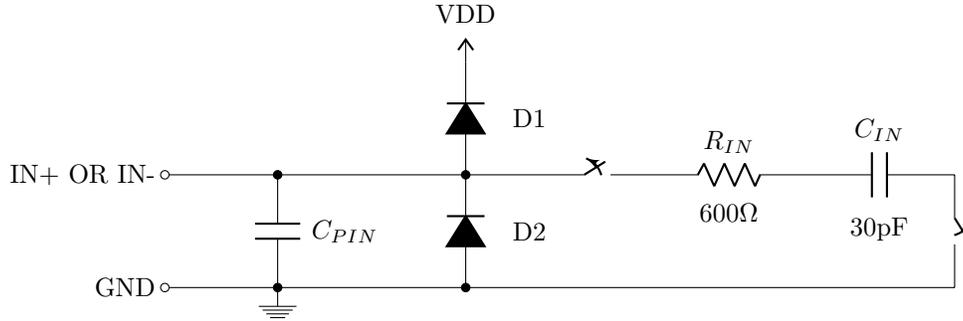
Figure 3.1: Equivalent analog input circuit of AD7686

During the acquisition phase, the switches are closed, and during the conversion phase, the switches open. D1 and D2 are electrostatic discharge (ESD) protection for the analog inputs IN+ and IN-.

3.1.2 Process Decision

Since the common mode (CM) is passed through the amplifier at unity gain, the output common mode voltage will be similar to that of the input. In other words, the CM is not removed from the signal until processing has been performed on the correlated double samples; the amplifier is not the mechanism that removes the common mode. The fact that the output assumes the same common mode of the input means that the common mode input range is dictated by the ADC that will be converting the amplified signal. Since the AD7686 runs on 5V, 5V is the logical power supply for this amplifier. Due to these constraints, the l50_mixsig_1p5m_1p8bv_5v[8] process will be used for the initial design of this amplifier. Using this process will also increase the likelihood of a piggy-back tapeout for this proof-of-concept, as the 0.18μm CMOS process is commonplace and widely used by many others.

3.1.3 Closed Loop Gain

For this design, the closed loop gain will be small powers of two, somewhere between unity and 16. The purpose of the amplifier is to condition a differential signal to be sampled by an ADC, passing through the common mode at unity gain. If the amplifier has too little gain, the output of the ADC may be too quantized, with not enough resolution to reconstruct the original signal. If the amplifier presents too much gain, the output of the ADC will be dominated by front end noise, and the lower bits of the ADC will be random, wasting the ADCs resolution. Depending on the amplitude of the input signal, a configurable gain may be advantageous to capture a larger range of input swings. Therefore, as proof-of-concept, two closed loop gain configurations will be supported: a gain of 4 and a gain of 16.

---

[8]TSMC 0.18 MixSig Single-Poly Five-Metal 1.8V/5V Process

3.1.4   Open Loop Gain

The open loop gain of an amplifier determines how precise a feedback system is. Take, for example, an amplifier with open loop gain $= A$, configured in a unity gain fashion as shown in Figure 3.2.
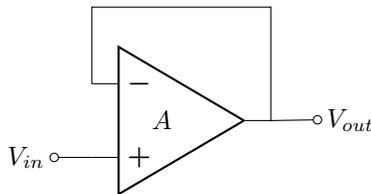
Figure 3.2: Amplifier configured in unity gain

In physical systems, amplifiers are non-ideal and A is some (hopefully large) finite number. In the circuit shown in Figure 3.2 above, the true closed loop gain of the feedback system is not 1, but rather:

$$\frac{V_{out}}{V_{in}} = \frac{A}{A+1} = \frac{1}{\frac{1}{A}+1} \tag{3.1}$$

For a system with 16-bits of resolution, we would want Equation 3.1 to be within the range 1 ± 2^{-16}. Since Equation 3.1 can never be greater than unity, we can explicitly solve for A as:

$$\frac{A}{A+1} > 1 - 2^{-16} \tag{3.2}$$

$$A > 65535 \tag{3.3}$$

to add a margin of safety, we impose:

$$A > 100000 = 100\text{dB} \tag{3.4}$$

It must be noted that the statement made in Equation 3.1 only remains valid for unity gain configurations. In the case that the closed loop gain is greater than one, for example, 16, it can be shown that:

$$\frac{V_{out}}{V_{in}} = 16\frac{1}{\frac{16}{A}+1} \tag{3.5}$$

in which case A must be increased by a factor of 16, or in other words, increased by 24dB, to preserve the same 16-bit resolution. Achieving an open loop gain of 124dB is very difficult to do, let alone with a single stage amplifier. Thus, the circuit will be designed with a target open loop gain of 100dB, a compromise that will still show proof-of-concept.

Gain error is not actually that detrimental to the system as it can be calibrated out in post-processing. What is more important is that the output is linear. The open loop gain, A, discussed above is a strong function of common mode voltage. This non-linearity is much more difficult to fix post-measurement. While a larger open loop gain will help to some degree, this non-linearity is an issue that is almost impossible to avoid.

3.1.5   Load/Feedback Capacitance

The capacitance the amplifier drives is important to consider in order to ensure the amplifier is stable during normal operation. The AD7686 has an input capacitance of 30pF (mainly attributed to the ADC sampling capacitor). For best performance, C_i and C_f are sized to similar values to C_{ADC} (on the order of pF's) so the ADC input does not dominate the load capacitance or vice-versa. It is also important to make these feedback capacitors sufficiently larger than parasitics (typically on the order of 100fF) in order to have reasonable control over the closed loop gain. At this time, it is important to recognize that the effective load capacitance, C_L, changes depending on the phase of operation and the closed loop gain of the system. As stated before, the amplifier will be designed with two programmable options for the gain; one option with a gain of 4, and another with a gain of 16. Therefore, there are a total of three different gain configurations for which the amplifier must be simulated to ensure stability: unity gain, gain of 4, and gain of 16. For the unity gain configuration (phase 1 operation), one can calculate the effective load capacitance as:

$$C_L = C_{ADC} + C_i \tag{3.6}$$

For the gain of 4 configuration (phase 2 and 4 operation for gain of 4), noting that $C_i = 3C_f$, the effective load capacitance can be written as:

$$C_L = \frac{C_i}{4} + C_{ADC} \tag{3.7}$$

and for the gain of 16 configuration (phase 2 and 4 operation for gain of 16), noting that $C_i = 15C_2$, the effective load capacitance can be written as:

$$C_L = \frac{C_i}{16} + C_{ADC} \tag{3.8}$$

For the purpose of simulation, a value of $C_{ADC} = 30\text{pF}$ will be used for all cases/modes of operation. The values for C_i and C_f are shown in Table 3.1 below, and the resulting C_L is calculated based on the equations above.

Gain Configuration	Capacitor	Value[9]
Gain of 4	C_i	30pF
	C_f	10pF
	C_L (switch E closed)	60pF
	C_L (switch E open)	37.5pF
Gain of 16	C_i	30pF
	C_f	2pF
	C_L (switch E closed)	60pF
	C_L (switch E open)	31.875pF

Table 3.1: Effective load capacitances

Note that while the ADC performs its SAR algorithm, the input capacitance of the ADC, C_{ADC}, appears disconnected from the output of the OTA. To compensate for this, a dummy capacitor may be added to the output of the OTA to ensure that the output of the OTA does not ring uncontrollably when the ADC carries out its SAR algorithm.

3.1.6 Settling Time

It is important that the amplifier settles within each sampling period; thus, given the 500kSPS of the AD7686, the amplifier will be desinged to settle in 1μs to 16-bits of resolution, or, in other words, approximately 0.0015% of the final value, both in settling up *and* down. From here, one can calculate a corresponding τ:

$$e^{-1\mu s/\tau} = 0.000015 \tag{3.9}$$

solving for $1/\tau$ we find:

$$1/\tau = \omega \approx 11 \times 10^6 \text{rad/sec} \rightarrow f \approx 2\text{MHz} \tag{3.10}$$

Again, at this point, one must realize the different gain configurations for which the OTA must be stable: gain of 1, gain of 4, and gain of 16. With these different feedback factors, one can calculate the corresponding unity (open loop) gain bandwidth of the amplifier. Please note that ω_u (and f_u) represents the corresponding unity gain crossover frequency.

Closed Loop gain of 1 ($C_L = 60\text{pF}$): This presents a feedback factor of 1; therefore:

$$\omega_u \approx 11 \times 10^6 \text{rad/sec} \rightarrow f_u \approx 2\text{MHz} \tag{3.11}$$

---

[9]Assuming the ADC (30pF) is connected to the output of the OTA.

Closed Loop gain of 4 ($C_L = 37.5$pF): This presents a feedback factor of 1/4; therefore:

$$\omega_u \approx 4 * 11 \times 10^6 \text{rad/sec} \rightarrow f_u \approx 8\text{MHz} \tag{3.12}$$

Closed Loop gain of 16 ($C_L = 31.875$pF): This presents a feedback factor of 1/16; therefore:

$$\omega_u \approx 16 * 11 \times 10^6 \text{rad/sec} \rightarrow f_u \approx 32\text{MHz} \tag{3.13}$$

The design of the OTA is limited by the OTA configured with a gain of 16 as this requires the largest open loop unity gain frequency to ensure the output settles within 1μs. The OTAs presented below will be designed with this in mind.

3.1.7   Input Differential Pair Transistors

The input transistors impact the common mode input range of the amplifier. Typically, an amplifier with p-channel MOSFET (PMOS) input transistors is capable of operating at low common mode input voltages, whereas an amplifier with n-channel MOSFET (NMOS) input transistors offers the opposite and has good behavior for signals with high common mode voltage. In addition to this trade-off, NMOS devices typically have higher mobility than their PMOS counterparts; thus, one may achieve greater g_m/I_D using NMOS inputs, ultimately leading to lower active power consumption.

In a signal chain, it is important that parts are compatible and work together symbiotically. The input span of the AD7686 is dictated by its reference voltage, which itself is with respect to ground. Thus, the AD7686 will have no problems converting input signals with low common mode voltage. Because of this, it is logical that the amplifier be designed such that signals with low common mode voltage can be easily amplified. This leads to the choice of PMOS gender inputs. With this decision, the amplifier may consume more power than if NMOS input devices were used; however, the swing of the signal chain is maximized, and the overall goal of zero *inactive* power, with fast turn-on and turn-off times, is still met.

3.2   Standard OTA

All schematic reference designators in this section are in reference to Figure 3.3 below unless otherwise noted.

Figure 3.3: Standard OTA

The design of this circuit starts with the most basic OTA topology, referred to as the "standard OTA" in this thesis. The circuit consists of an input differential pair that converts a small signal input voltage into a small signal current, by virtue of the input pair's transconductance. The small signal current is mirrored through devices such that it is ultimately routed to the (single) output of the amplifier, producing an output signal that is proportional to both the small signal current and output resistance of the amplifier.

3.2.1 Device Sizing

The calculations for a standard single-ended OTA are presented below. These calculations are not repeated for each OTA topology presented in this thesis, as the majority of the design/main requirements (i.e. settling time, load capacitance, etc.) remain constant for all topologies. The design methodology is listed below [5]:

- Determine required g_m from circuit bandwidth, $\frac{g_m}{C_L}$.

- Starting with minimum L, choose current density, I_D/W, for optimal performance.

- Confirm the transition frequency, f_T, of the devices is sufficiently large.

- Iterate on the design/topology until gain requirement is met.

The two most important design specifications for this amplifier are power consumption and settling time, as these dictate the energy consumed per measurement. Given the settling time specification discussed in the section above, the design will start here. As mentioned, the design of the OTA is limited by closed loop

gain of 16 configuration, as this requires the largest open loop unity gain frequency to ensure the output settles within 1μs. This corresponds to $f_u = 32$MHz and $C_L \approx 31.875$pF. It can be shown that the unity gain frequency, ω_u, of an OTA driving a load capacitance, C_L, is $\frac{g_m}{C_L}$ where g_m is the transconductance of the input differential pair transistors. We now calculate the necessary g_m that corresponds to $f_u = 32$MHz:

$$2\pi * 32\text{MHz} = \frac{g_m}{31.875\text{pF}} \tag{3.14}$$

$$g_m = 6.4\text{mS} \tag{3.15}$$

Using PMOS transistors as the input differential pair, preliminary sizing of transistors can be calculated by graphing the transconductance efficiency (g_m/I_D) of a unit-size $(1\mu$m$)$ PMOS transistor. With the required g_m in hand, we now turn to Figure 3.4 below. The transconductance efficiency of a unit sized PMOS transistor was plotted over a current density range of 10^{-8}A$/\mu$m to 10^{-4}A$/\mu$m for lengths $= 0.6\mu$m, 0.78μm, 0.96μm, 1.14μm, 1.32μm, and 1.5μm.
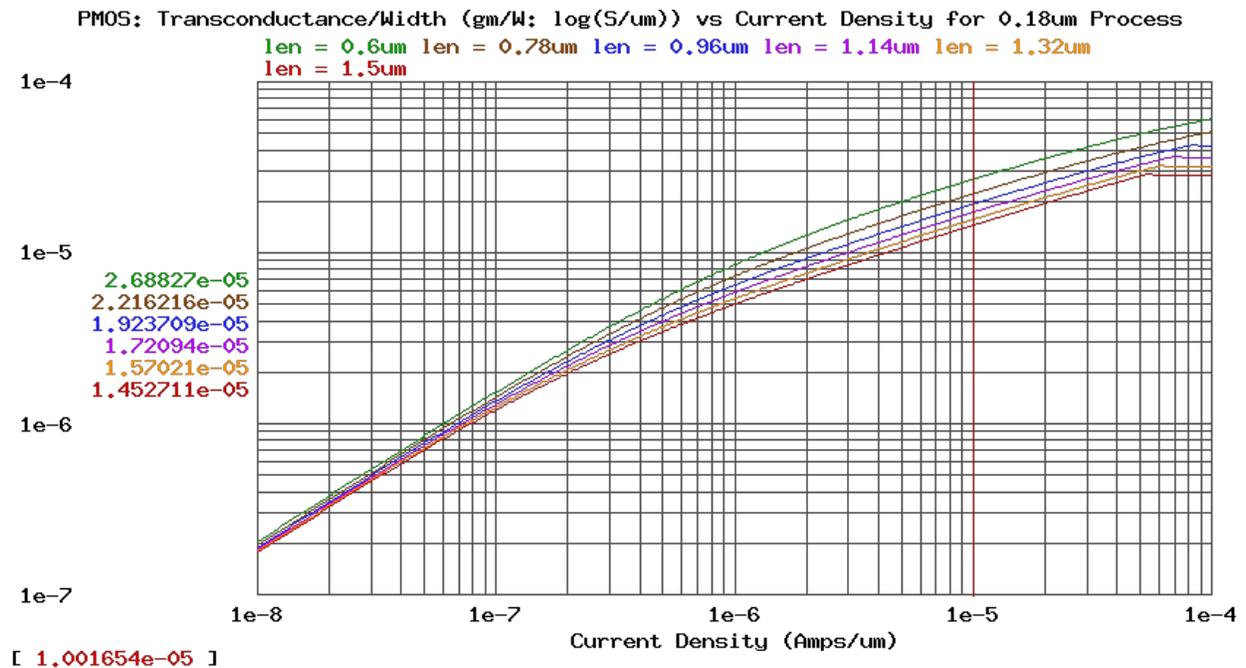
Figure 3.4: Transconductance/width vs current density of a PMOS device for 0.18μm process

For optimum performance (power, speed, and area) the bias current density, W/I_D, is set at the edge of weak inversion, where the slope of the graph in Figure 3.4 transitions from a slope of approximately 1 (weak inversion) to a slope of approximately 1/2 (strong inversion). For this process, this transition roughly corresponds to a bias current density of 10μA$/\mu$m, as marked by the vertical red line in Figure 3.4 above. The minimum

length transistor offers the best transconductance efficiency; thus, length $\boxed{L_{MP1} = L_{MP2} = 0.6\mu\text{m}}$ is used for the input differential pair transistors.

As a general rule of thumb, the maximum device frequency, f_T, should be five to ten times the maximum operating frequency of the circuit, otherwise the devices may introduce significant phase shift. Plotting f_T vs current density (please see Figure 3.5), a bias current density of $10\mu\text{A}/\mu\text{m}$ with a length of L $= 0.6\mu\text{m}$ corresponds to $f_T \approx 3\text{GHz}$, which is well above $10 * 32\text{MHz} = 320\text{MHz}$.
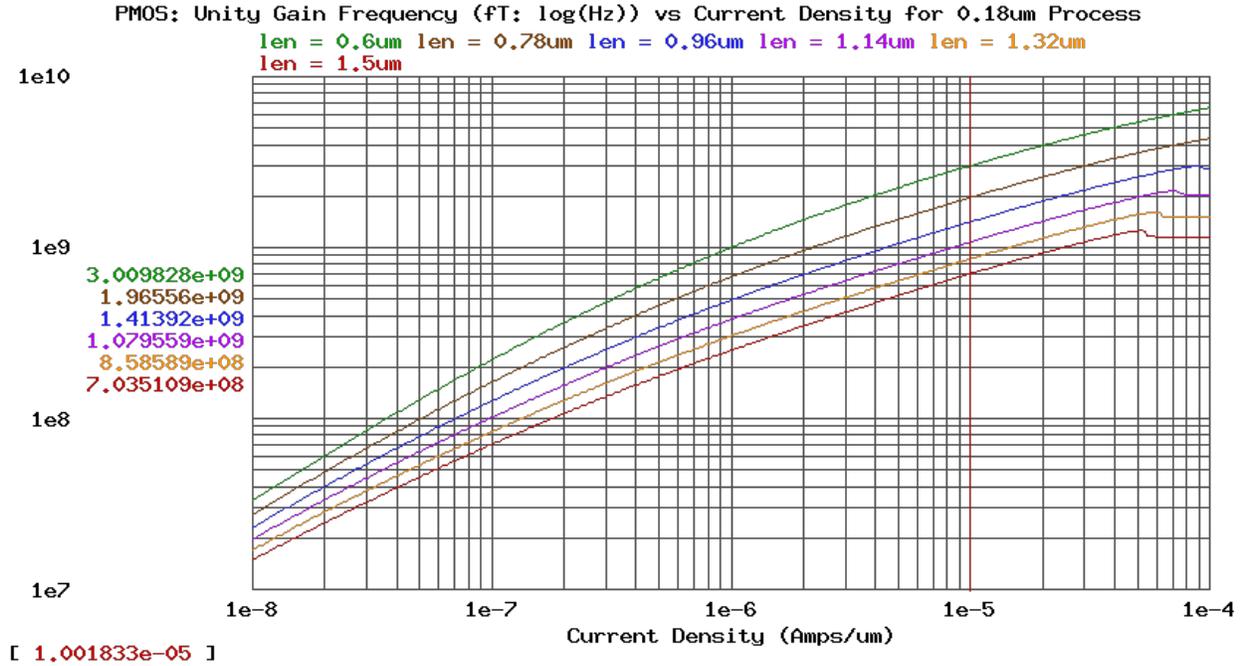
Figure 3.5: Unity gain frequency (f_T) vs current density of a PMOS device for $0.18\mu\text{m}$ process

With transition frequency confirmed, device sizing of the input differential pair can begin. At $10\mu\text{A}/\mu\text{m}$ with length of L $= 0.6\mu\text{m}$, $g_m/W = 27\mu\text{S}/\mu\text{m}$. Using the result from Equation 3.15 above:

$$W_{MP1} = W_{MP2} = \frac{6.4\text{mS}}{27\mu\text{S}/\mu\text{m}} = 237\mu\text{m} \approx \boxed{240\mu\text{m} = W_{MP1} = W_{MP2}} \tag{3.16}$$

With the widths of MP1 and MP2 known, the bias current, I_{TAIL}, can now be calculated, recalling a bias current density of $10\mu\text{A}/\mu\text{m}$ and noting that half the tail current flows though MP1 and the remaining current through MP2:

$$\frac{I_{TAIL}}{2} = W_{MP1} * I_D/W = 240\mu\text{m} * 10\mu\text{A}/\mu\text{m} = 2.4\text{mA} \tag{3.17}$$

$$I_{TAIL} = 4.8\text{mA} \qquad\qquad (3.18)$$

The NMOS and PMOS mirrors, consisting of MN1-4 and MP3-4, are sized to $\boxed{W_{MN1-4} = W_{MP3-4} = 240\mu\text{m}}$ such that all devices are operating at the same bias current density, and thus exhibit similar characteristics. The lengths of these mirror transistors are increased to $\boxed{L_{MN1-4} = L_{MP3-4} = 1.5\mu\text{m}}$ to make the mirrors more robust against process variations that may cause slight mismatches in lengths of these transistors. Mismatched lengths lead to mismatched mirrors ratios which cause offsets. This CDS scheme should be able to reject offsets intrinsic to the OTA; however, significant offsets should be avoided if possible.

Component	Value	
I_{TAIL}	4.8mA	
Transistor	**Width**	**Length**
MP1-2	$240\mu\text{m}$	$0.6\mu\text{m}$
MP3-4	$240\mu\text{m}$	$1.5\mu\text{m}$
MN1-4	$240\mu\text{m}$	$1.5\mu\text{m}$

Table 3.2: Standard OTA design summary

OTA Topology	DC Gain	Open loop f_u[10]	Active Power[11]
Standard OTA	43dB	32MHz	48mW

Table 3.3: Standard OTA preliminary simulation results

After preliminary simulation of the OTA presented above, the results shown in Table 3.3 were obtained. It is clear that the standard OTA does not meet the gain requirement of at least 100dB; thus, an output cascode is added in an effort the increase the output resistance of the amplifier. This is discussed in the following section.

3.3 Standard OTA with Output Cascode

All schematic reference designators in this section are in reference to Figure 3.6 below unless otherwise noted.

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[10]Simulated with $C_L = 31.875\text{pF}$
[11]Measured with a 2.5V DC input signal.
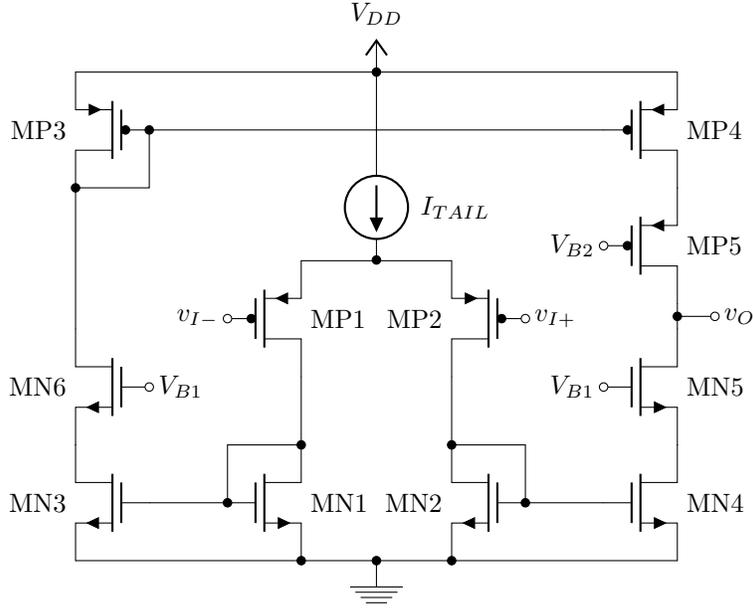
Figure 3.6: Standard OTA with output cascode

The standard OTA presented in the section above failed to meet the gain specification of at least 100dB imposed on this project. Because of this, in hopes to increase the gain, an output cascode is added to the OTA. A cascode stage is commonly utilized when more gain is needed, but not at the expense of bandwidth or power consumption. The drawback, however, is that the output cascode devices decrease the output swing of the amplifier.

A cascode stage is a cascade of a common source stage and a common gate stage. To analyze the behavior of the cascode, the structure will be considered piece by piece. For the time being, we will abstract the PMOS devices to their incremental output resistance, $R_{o,p}$, and assume $\lambda = \gamma = 0$ for MN4 and MN5, as shown below [10].
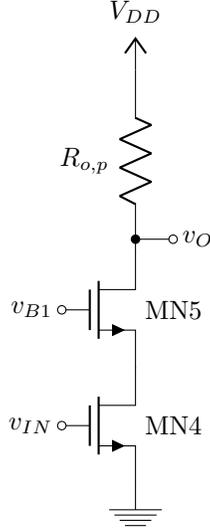
Figure 3.7: Output cascode stage

Figure 3.7 above shows a simplification of the output leg for a standard OTA with an output cascode. First we will examine the behavior of the cascode when an incremental voltage, $v_{IN} = V_{IN} + v_{in}$, is applied to the gate of MN4 with $v_{B1} = V_{B1}$ held constant, and then the cascode will be analyzed when $v_{IN} = V_{IN}$ is held constant and an incremental voltage, $v_{B1} = V_{B1} + v_{b1}$, is applied to the gate of MN5. The complete behavior of the cascode structure can then be classified as the superposition of these two studies, assuming the circuit behaves linearly about its operating point, providing insight into the operation of the circuit. Thus, we begin with an incremental voltage applied to the gate of MN4 while holding v_{B1} constant. A voltage of $v_{IN} = V_{IN} + v_{in}$ applied to MN4 will result in a small signal current $i_{d,MN4} = g_{m,MN4} \cdot v_{in}$ flowing through the output leg. This small signal current flows through the source of MN5, which has an impedance of $1/g_{m,MN5}$; thus, resulting in $v_{s,MN5} = -(g_{m,MN4}/g_{m,MN5}) \cdot v_{in}$. Similarly, this small signal current flows through $R_{o,p}$, causing an output signal $v_o = -R_{o,p} \cdot g_{m,MN4} \cdot v_{in}$, akin to a solo common source stage. Now let us consider the case when v_{in} is fixed at V_{IN} and a small signal is applied to the gate of MN5, such that $v_{B1} = V_{B1} + v_{b1}$. Since $V_{GS,MN4}$ is constant and $r_{o,MN4} \to \infty$, we can consider MN4 as a constant current source with MN5 operating as a source follower, i.e., $v_{s,MN5} = v_{b1}$, regardless of the value of $R_{o,p}$. In contrast, the output, v_o, does not change since the drain current through the output leg remains constant. In other words, $\frac{v_o}{v_{b1}} = 0$. This property will be leveraged when designing the bias circuitry for the cascode devices, as discussed in §3.6.4. While this rather qualitative analysis was performed on the NMOS devices, similar arguments can be made for the PMOS device, MP4 and MP5.

An important characteristic of cascode stages are their high output impedance [10]. Using the lemma

$A_v = G_m R_o$, one can directly see how an increase of the output resistance of the amplifier leads to an increase in the gain.
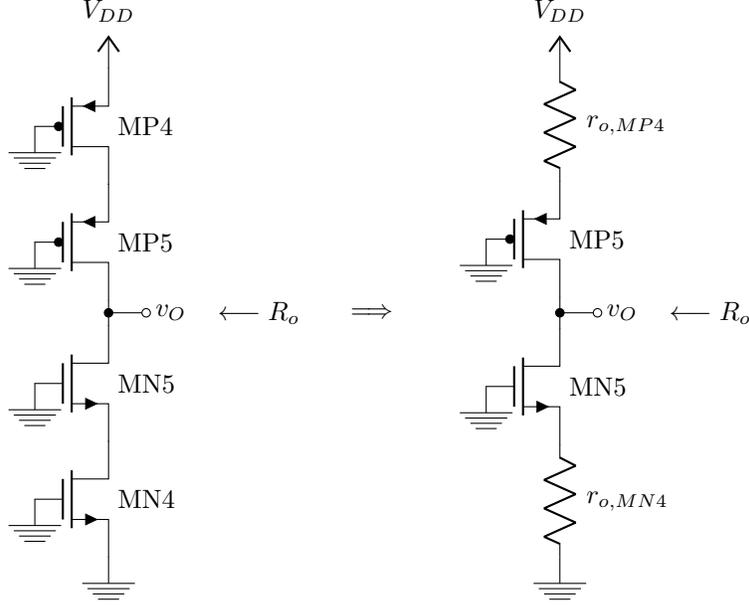
Figure 3.8: Output resistance of cascode stage

For purposes of calculating the output resistance, R_o, of the cascode stage, the structure can be approximated by MP5 and MN5 operating as common source stages with degeneration resistors $r_{o,MP4}$ and $r_{o,MN4}$, respectively, as shown in Figure 3.8. The output resistance of a common source stage with source degeneration, R_S, can be expressed as:

$$R_o = [1 + (g_m + g_{mb})r_o]R_S + r_o \tag{3.19}$$

Thus, it follows that:

$$R_{o,up} = [1 + (g_{m,MP5} + g_{mb,MP5})r_{o,MP5}]r_{o,MP4} + r_{o,MP5} \tag{3.20}$$

$$R_{o,up} \approx (g_{m,MP5} + g_{mb,MP5})r_{o,MP5}r_{o,MP4} \tag{3.21}$$

and similarly:

$$R_{o,down} = [1 + (g_{m,MN5} + g_{mb,MN5})r_{o,MN5}]r_{o,MN4} + r_{o,MN5} \tag{3.22}$$

$$R_{o,down} \approx (g_{m,MN5} + g_{mb,MN5})r_{o,MN5}r_{o,MN4} \tag{3.23}$$

Where $R_{o,up}$ is the output resistance looking up into the PMOS devices, and $R_{o,down}$ is the output resistance

looking down into the NMOS devices. Noting that the output resistance is the amalgamation of $R_{o,up}$ and $R_{o,down}$, we have:

$$R_o = R_{o,up} || R_{o,down} \approx \frac{1}{2}(g_{m,MN5} + g_{mb,MN5})r_{o,MN5}r_{o,MN4} \tag{3.24}$$

assuming similar characteristics between NMOS and PMOS devices.

In the case of the standard OTA without the output cascode stage, the output resistance of the amplifier is simply:

$$R_o = r_{o,MP4} || r_{o,MN4} \approx \frac{1}{2}r_{o,MN4} \tag{3.25}$$

again, assuming similar characteristics between NMOS and PMOS devices. By comparing Equations 3.24 and 3.25, one can see that by adding the cascode output stage, the output resistance of the amplifier is increased by a factor of approximately $g_m r_o$.

The benefits of the cascode structure have been shown; however, it comes with its costs. We will now examine how the output cascode limits the output swing of the amplifier. Output swing is quantified by the range of output voltages for which the transistors in the output leg of the amplifier are all saturated.

For the standard OTA without an output cascode stage (Figure 3.3), for MN4 and MP4 to be saturated, V_O must be in the range:

$$V_{DD} - (|V_{GS,MP4}| - |V_{T,p}|) \geq V_O \geq (V_{GS,MN4} - V_{T,n}) \tag{3.26}$$

Where we sometimes call $(V_{GS} - V_{T,n}) \approx (|V_{GS}| - |V_{T,p}|)$ one overdrive, or $V_{D,sat}$. In other words, the standard OTA without the output cascode can swing within one $V_{D,sat}$ of either rail.

Now let us consider the case when the output cascode is added. In this scenario, in order for MN4 to be saturated, $V_{B1} - V_{GS,MN5} \geq (V_{GS,MN4} - V_{T,n})$[12], and hence, $V_{B1} \geq (V_{GS,MN4} - V_{T,n}) + V_{GS,MN5}$. In order for MN5 to be saturated, $V_O - (V_{B1} - V_{GS,MN5}) \geq V_{B1} - (V_{B1} - V_{GS,MN5}) - V_{T,n}$, or put more simply: $V_O \geq V_{B1} - V_{T,n}$. It follows:

$$V_O \geq (V_{GS,MN4} - V_{T,n}) + (V_{GS,MN5} - V_{T,n}) \tag{3.27}$$

Similar calculations can be made for the PMOS devices MP4 and MP5, bounding V_O from above such that

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[12]When both MN4 and MN5 are in saturation, $V_{DS,MN4}$ is determined primarily by V_{B1}, as MN5 behaves as a source follower.

the output swing of the amplifier can be fully described by:

$$V_{DD} - (|V_{GS,MP4}| - |V_{T,p}|) - (|V_{GS,MP5}| - |V_{T,p}|) \geq V_O \geq (V_{GS,MN4} - V_{T,n}) + (V_{GS,MN5} - V_{T,n}) \quad (3.28)$$

$$V_{DD} - 2V_{D,sat} \geq V_O \geq 2V_{D,sat} \quad (3.29)$$

By adding the cascode stage on the output of the amplifier, the output swing is reduced symmetrically by $2V_{D,sat}$ when compared to that of the standard cascode.

3.3.1 Device Sizing

The circuit remains similar to what was presented in §3.2.1. Compared to §3.2.1, three extra transistors are added to the design, and two bias voltages are created. MN5 and MP5 are the output cascode devices, and MN6 serves to improve the symmetry of the OTA such that offset voltages are reduced. To preserve a current density of $10\mu A/\mu m$, $\boxed{W_{MP5} = W_{MN5} = W_{MN6} = 240\mu m}$. As we discovered above with Equation 3.29, $V_{D,sat}$ of the cascode devices limit the swing of the amplifier. For a given transistor, we have:

$$V_{D,sat} = \sqrt{\frac{2I_D L}{\mu C_{ox} W}} \quad (3.30)$$

Thus, by assigning minimum length to the cascode devices, such that $\boxed{L_{MP5} = L_{MN5} = L_{MN6} = 0.6\mu m}$, the effect the cascode devices have on the output swing is minimized. However, this comes with a trade-off (as always), as shorter devices have lower output resistance than longer devices.

The cascode bias voltages, V_{B1} and V_{B2}, are determined such that V_{DS} mismatches are minimized. For now, ideal voltage sources are used to bias the cascode devices. To determine values for V_{B1} and V_{B2}, the OTA was configured in a unity gain (closed loop) fashion with $v_{IN} = V_{IN} = 2.5V$. Performing a DC operating point simulation allowed voltages at certain nodes to be measured, in particular, $V_{G,MP3}$, $V_{G,MN2}$, and the gate-to-source voltages of the cascode devices. With these voltages in hand, V_{B1} and V_{B2} were set such that $V_{DS,MP4} = V_{DS,MP3}$ and $V_{DS,MN4} = V_{DS,MN2}$. The values for V_{B1} and V_{B2} are shown in Table 3.4 below.

Component	Value	
I_{TAIL}	4.8mA	
V_{B1}	2.8V	
V_{B2}	1.1V	
Transistor	**Width**	**Length**
MP1-2,5	240μm	0.6μm
MP3-4	240μm	1.5μm
MN1-4	240μm	1.5μm
MN5-6	240μm	0.6μm

Table 3.4: Standard OTA with output cascode design summary

OTA Topology	DC Gain	Open loop f_u[13]	Active Power[14]
Standard OTA with output cascode	70dB	32MHz	48mW

Table 3.5: Standard OTA with output cascode preliminary simulation results

Again, the amplifier fails to meet the requirements set forth for the gain. We turn to the nested current mirror topology in hopes of achieving more gain.

3.4   Nested Current Mirror OTA

All schematic reference designators in this section are in reference to Figure 3.9 below unless otherwise noted.
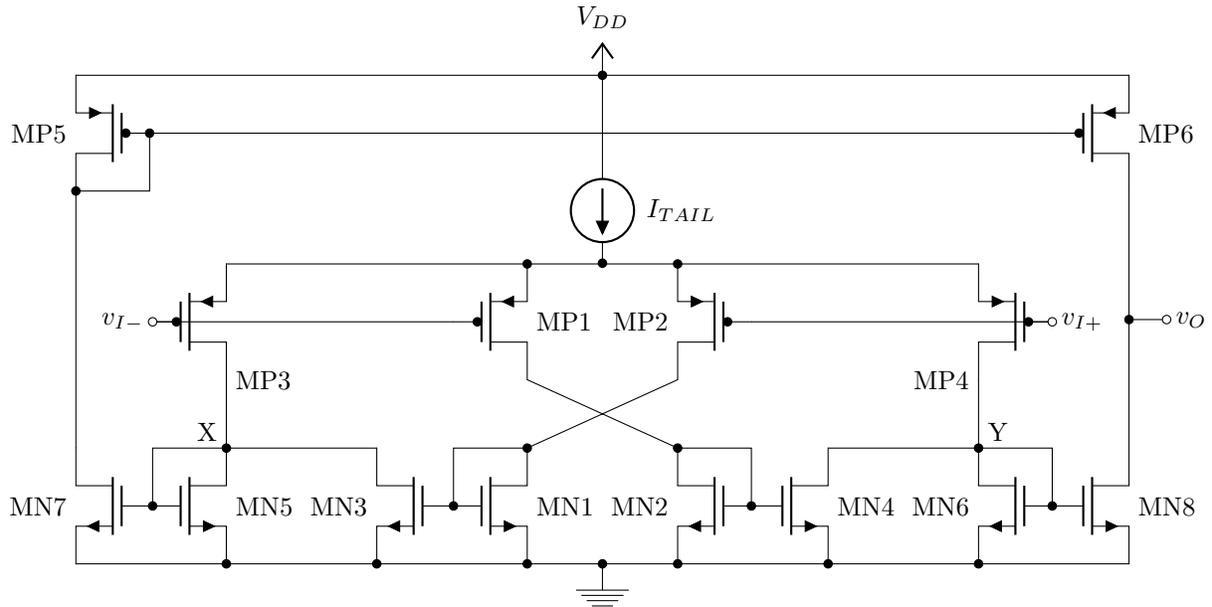
Figure 3.9: Nested current mirror OTA

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[13]Simulated with $C_L = 31.875$pF
[14]Measured with a 2.5V DC input signal.

Increasing the output resistance of the standard OTA by means of a cascode stage proved inadequate in meeting the gain requirements. To achieve acceptable open loop gain without sacrificing other important specifications, such as area and power consumption, topological changes must be made. A nested current mirror (NCM) OTA is proposed for the amplifier in this correlated double sampling scheme [6]. A good designer must understand how topological changes actually improve the circuit's performance; thus, this is discussed below.

The standard OTA design presented in §3.2 had a few drawbacks that were not mentioned above but will now be addressed. For a transconductance amplifier, an important metric is G_m/I_{BIAS}, or in other words, how efficiently the amplifier uses the current it is supplied to produce a transconductance. Ideally G_m/I_{BIAS} is a large number. The standard OTA above was biased using a tail current source, and, during steady state operation, this tail current was split between the two input legs, with $\frac{1}{2}I_{TAIL}$ flowing through MP1 and $\frac{1}{2}I_{TAIL}$ flowing through MP2 in Figure 3.3. The mirrors MN1:MN3 and MN2:MN4 in Figure 3.3 replicate $I_{TAIL}/2$ to the external legs. Thus, to a first order, the standard OTA consumes $\sim 2I_{TAIL}$ of bias current. Now let us investigate how the nested current mirror OTA improves this.

The NCM OTA shown in Figure 3.9 employs a set of nested current mirrors (hence the name) to prevent the bias currents through the core of the amplifier from being mirrored to outer legs, while still allowing the small signal current to propagate through the circuit. For a cursory, qualitative analysis, let us assume $\lambda = 0$ for all devices in the NCM OTA and that $\frac{(W/L)_{MN3}}{(W/L)_{MN1}} = \frac{(W/L)_{MN4}}{(W/L)_{MN1}} = 1$. Please note that with these ideal assumptions and the proposed current mirror ratios, MN5 and MN6 would be starved of current. However, for reasons discussed below that take into account the finite output resistance of the devices, this configuration operates, albeit may not be a sound design in practice[15]. We will first examine the behavior of the circuit during steady state, when $v_{I-} = v_{I+} = V_{CM}$. Following that we will study the behavior of the circuit when a small differential signal is applied to the input of the NCM OTA; that is $v_{I-} = -\frac{1}{2}v_{diff}$ and $v_{I+} = \frac{1}{2}v_{diff}$. These experiments will give us insight as to how the NCM OTA differs from the standard OTA and provide reasoning for using this topology.

In the case of steady state operation, $v_{I-} = v_{I+}$, and I_{TAIL} is divided such that $I_{D,MP1} = I_{D,MP2} = I_{D,MP3} = I_{D,MP4} = \frac{1}{4}I_{TAIL}$. Performing KCL on nodes X and Y, one can see that $I_{D,MN5} = I_{D,MN6} = 0$ as the bias currents are stolen from MN5 and MN6 by MN3 and MN4, respectively. Thus, with the ideal approximations, no standing current flows through the outer legs of the OTA.

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[15]for more detail, please see §3.6.7.

Now let us investigate what happens when a small, differential signal is applied to the amplifier. Assuming $v_{I-} = -\frac{1}{2}v_{diff}$ and $v_{I+} = \frac{1}{2}v_{diff}$, $i_{d,MP1} = i_{d,MP3} = -\frac{1}{2}g_m v_{diff}$ and $i_{d,MP2} = i_{d,MP4} = \frac{1}{2}g_m v_{diff}$, where g_m is the transconductance of the PMOS input devices. Performing KCL on node X, $i_{d,MN5} = -g_m v_{diff}$, and similarly, by performing KCL on node Y, $i_{d,MN6} = g_m v_{diff}$. The small signal current is delivered to the output of the OTA by the current mirrors formed by MN6:MN8, MN5:MN7, and MP5:MP6.

To a first order, the NCM OTA consumes $\sim I_{TAIL}$ of bias current. To compare like to like, let us assume the input transistors in the NCM OTA are sized to be $1/2$ of the size of the input transistors in the standard OTA, such that G_m is the same for both topologies. When this is the case, one can see that the transconductance efficiency, G_m/I_{BIAS}, of the NCM OTA is twice as good as that of the standard OTA. More specifically, for the NCM OTA, $G_m/I_{BIAS} = G_m/I_{TAIL}$, whereas for the standard OTA, $G_m/I_{BIAS} = G_m/2I_{TAIL}$. Realistically, the NCM OTA will require some non-zero amount of bias current through the outer most legs to operate.

A careful reader might realize that the NCM OTA outperforms the standard OTA in another area as well: output resistance. The output resistance of a device can be expressed as $r_o = \frac{1}{\lambda I_D}$. Thus, as the drain current of the device decreases, output resistance increases. This is especially useful for achieving high gain, when considering $A_v = G_m R_o$. High output resistance is exactly our goal since the design has been falling short of providing an acceptable open loop gain. For the reasons of good transconductance efficiency and high output resistance (thus high gain), the NCM OTA is a strong candidate for this project.

While transconductance efficiency and output resistance of the amplifier has improved with this NCM OTA topology, slew rate has been degraded. Assuming 1:1 current mirrors in both the standard and NCM OTA, in the event of slew, the NCM OTA will only be able to provide a maximum of $I_{TAIL}/2$ output current, whereas the standard OTA will be able to provide full I_{TAIL} output current. Slew rate in the NCM OTA can be improved by increasing the ratio between MN5:MN7 and similarly between MN6:MN8, such that $\frac{(W/L)_{MN7}}{(W/L)_{MN5}} = \frac{(W/L)_{MN8}}{(W/L)_{MN6}} > 1$. This idea is incorporated into the design and discussed further in §3.4.1.

The analysis presented above may have left the reader a bit unsatisfied as it assumed *all* the bias current was stolen from MN5 and MN6, a circuit that would surely have troubles in the real world. We will now take a closer look at this, no longer assuming $\lambda = 0$, but still, however, assuming V_T matches across all NMOS and PMOS devices. With these assumptions, the drain current of a NMOS transistor in strong inversion

$(V_{GS} > V_T)$, operating in saturation $(V_{DS} > V_{GS} - V_T$) can be described by the equation:

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \tag{3.31}$$

Similarly, for a PMOS and still assuming $\lambda \neq 0$, the drain current of a PMOS transistor in strong inversion $(|V_{GS}| > |V_T|)$, operating in saturation $(|V_{DS}| > |V_{GS}| - |V_T|$) can be described by the equation:

$$|I_D| = \frac{\mu_p C_{ox}}{2} \frac{W}{L} (|V_{GS}| - |V_T|)^2 (1 + \lambda |V_{DS}|) \tag{3.32}$$

With this in mind, and noting that the total tail current is I_{TAIL}, the drain current through an input PMOS device, MPi, can be described by:

$$|I_{D,MPi}| = \frac{(1 + \lambda |V_{DS,MPi}|)}{\sum_{j=1}^{4} (1 + \lambda |V_{DS,MPj}|)} \cdot I_{TAIL} \tag{3.33}$$

At this point, it is important to note the drain-to-source voltages of the transistors in the input stage of this amplifier, particularly those of MP1-4 and MN1-6. In steady state operation, $v_{I+} = v_{I-}$; therefore, V_{GS} of MP1-4 are all equal. Now, taking a look at V_{DS} of the input transistors, one can observe that the drain-to-source voltages of MP3 and MP4 are greater than those of MP1 and MP2. This is due to the fact that very little current flows through MN5 and MN6 because MN3 and MN4 steal the bias current away from each of the respective transistors. The low currents through MN5 and MN6 pull-down nodes X and Y, as these node voltages are directly set by $V_{GS,MN5}$ and $V_{GS,NMN6}$, respectively. Since $V_{DS,MP3} > V_{DS,MP1}$ and $V_{DS,MP4} > V_{DS,MP2}$, it follows that $|I_{D,MP3}| > |I_{D,MP1}|$ and $|I_{D,MP4}| > |I_{D,MP2}|$ as Equation 3.33 highlights. Please note that this is in steady state operation. Because of this fact, the outer legs (MP3 and MP4) of the differential pair possess a surplus of current, which ultimately leads to non-zero current flowing through MN5 and MN6 when the widths of MN1-MN6 are all equal. In addition, finite output resistance causes errors in the mirrors, most notably the mirrors MN1:MN3 and MN2:MN4. Let us take, for example, the mirror consisting of MN1 and MN3. The drain current through MN3, $I_{D,MN3}$, can be expressed as:

$$I_{D,MN3} = \frac{\left(\frac{W}{L}\right)_{MN3} (1 + \lambda V_{DS,MN3})}{\left(\frac{W}{L}\right)_{MN1} (1 + \lambda V_{DS,MN1})} I_{D,MN1} \tag{3.34}$$

It is simple to see that $V_{DS,MN3} = V_{GS,MN5}$ and $V_{DS,MN1} = V_{GS,MN1}$. Furthermore, $V_{GS,MN5} < V_{GS,MN1}$, since less bias current flows through MN5 than MN1. Thus, $V_{DS,MN3} < V_{DS,MN1}$ and hence $\frac{I_{D,MN3}}{I_{D,MN1}} < 1$. Similar arguments can be made for the mirror consisting of MN2 and MN4.

In summary, it has been shown that the finite output resistance of the devices work to our advantage in two ways: 1) by driving more of the tail current through MP3 and MP4 than MP1 and MP2 when $v_{I+} = v_{I-}$, and 2) by making the current mirror gains of MN1:MN3 and MN2:MN4 less than one when the widths of MN1-6 are all equal. These facts explain why the amplifier is able to operate with 1:1 current stealing mirror ratios. However, V_T mismatches and other process variations could cause $\frac{I_{D,MN3}}{I_{D,MN1}} > 1$. Therefore, the ability to control the current stealing mirror ratios is supported in the design and is discussed in §3.6.7.

3.4.1 Device Sizing

With the input now split among four transistors, to preserve the required transconductance to achieve acceptable bandwidth, the width of the input devices are reduced by a factor of two, such that $\boxed{W_{MP1-4} = 120\mu\text{m}}$. At this time, the width of the mirror devices are reduced to save area: $\boxed{W_{MN1-6} = 30\mu\text{m}}$. The widths, $\boxed{W_{MP5-6} = W_{MN5-8} = 50\mu\text{m}}$ are adjusted to increase the slew rate of the circuit, making up for the reduced slew rate of the NCM OTA. Since the standard OTA is capable of delivering an output current equal to I_{TAIL}, the proposed widths for MN5-8 allow the NCM OTA to deliver $\frac{5}{6}I_{TAIL}$ output current in the event of slew, making it comparable to the slew current achieved with the standard OTA. This change also increases the bandwidth of the amplifier while reducing the gain. The reasoning behind the lengths of the transistors and the tail current of the amplifier has already been discussed above.

Component	Value	
I_{TAIL}	4.8mA	
Transistor	**Width**	**Length**
MP1-4	$120\mu\text{m}$	$0.6\mu\text{m}$
MP5-6	$50\mu\text{m}$	$1.5\mu\text{m}$
MN1-6	$30\mu\text{m}$	$1.5\mu\text{m}$
MN7-8	$50\mu\text{m}$	$1.5\mu\text{m}$

Table 3.6: NCM OTA design summary

OTA Topology	DC Gain	Open loop f_u[16]	Active Power[17]
NCM OTA	71dB	43MHz	25mW

Table 3.7: NCM OTA preliminary simulation results

The active power has been reduce by approximately one-half, and there are all-around improvements in the gain and bandwidth. As done with the standard OTA, we will now investigate an output cascode stage on the NCM OTA.

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[16]Simulated with $C_L = 31.875$pF
[17]Measured with a 2.5V DC input signal.

3.5   Nested Current Mirror OTA with Output Cascode

All schematic reference designators in this section are in reference to Figure 3.10 below unless otherwise noted.
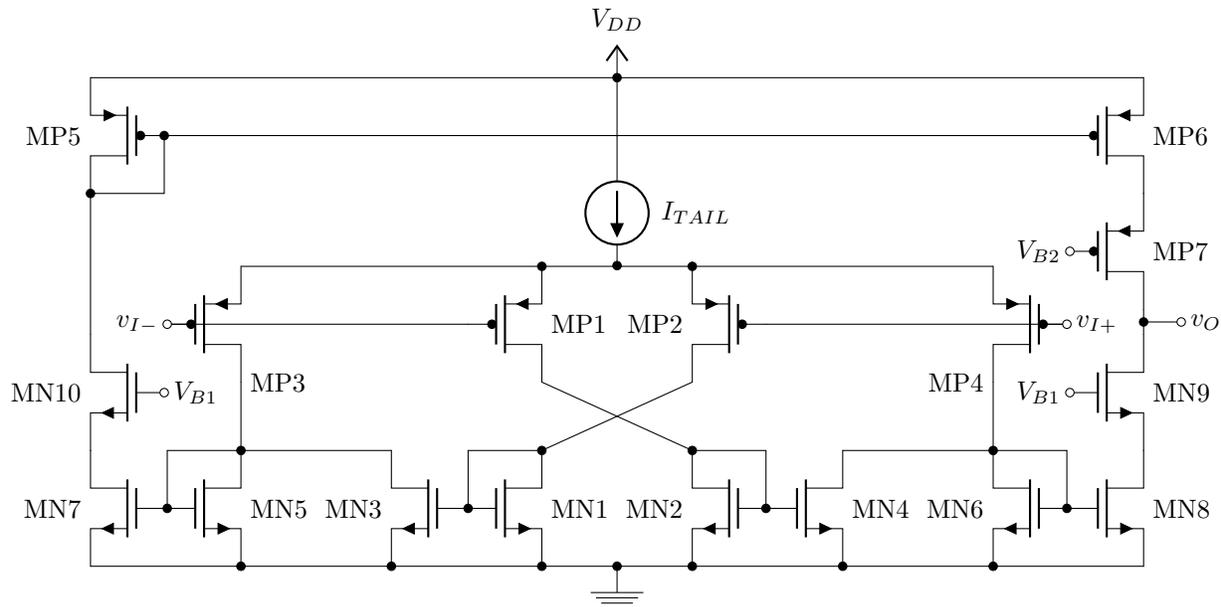
Figure 3.10: Nested current mirror OTA with output cascode

We have observed the advantages (and disadvantages) of both the output cascode stage and the NCM OTA topology. Since we are willing to sacrifice some performance specification for the advancement of others, such as the trade-off between less output swing for improved gain, it is time to combine the output cascode stage with the NCM OTA in hopes of achieving adequate gain.

3.5.1   Device Sizing

The device sizes of the NCM OTA remain the same as presented above. Cascode voltages, V_{B1} and V_{B2} were determined the same way described in §3.3.1, i.e., set to minimize V_{DS} differences in the mirrors. The output cascode devices, MP7, MN9, and MN10, are designed such that $\boxed{L_{MP7} = L_{MN9} = L_{MN10} = 0.6\mu\text{m}}$, to improve output swing, and $\boxed{W_{MP7} = W_{MN9} = W_{MN10} = 50\mu\text{m}}$ such that all the devices in the output leg share the same current density.

Component	Value	
I_{TAIL}	4.8mA	
V_{B1}	2.3V	
V_{B2}	2.3V	
Transistor	**Width**	**Length**
MP1-4	120μm	0.6μm
MP5-6	50μm	1.5μm
MP7	50μm	0.6μm
MN1-6	30μm	1.5μm
MN7-8	50μm	1.5μm
MP9-10	50μm	0.6μm

Table 3.8: NCM OTA with output cascode design summary

OTA Topology	DC Gain	Open loop f_u[18]	Active Power[19]
NCM OTA with output cascode	104dB	42MHz	25mW

Table 3.9: NCM OTA with output cascode preliminary simulation results

As shown above in Table 3.9, with appropriate topological changes, and with the help of an output cascode, we now have an OTA that meets, and surpasses, the design goals set forth above. The following sections now pertain to the supporting circuitry that surrounds the amplifier in the switched capacitor circuit.

3.6 Scaffolds

The design up to this point has been concerned with the amplifier, and ideal sources were used for preliminary simulation. Now that we have a topology that meets our base requirements, we set out to replace these ideal sources with realistic circuits. There are many supporting structures that are necessary to have a functional amplifier. These include biasing networks, pre-charge buffers, digital circuitry, switches, and other circuitry that is required to perform the correlated double sampling. Such elements are referred to as "scaffolds" to the main amplifier.

3.6.1 Current Reference

Since the current reference is used to produce the tail current through the input differential pair, the current reference can have a significant impact on the performance of the amplifier. It may be desired that the current reference be designed to keep a key specification of the amplifier, such as bandwidth, constant over a wide temperature range. The tail current directly affects the transconductance, g_m, of the input differential pair

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[18]Simulated with $C_L = 31.875$pF
[19]Measured with a 2.5V DC input signal.

transistors, and thus the bandwidth of the amplifier as a whole. Prior research has proposed methods of constant G_m amplifiers that are immune to a plethora of variations; however, this is unnecessary for this project [7]. One must always keep returning to the big picture of the scheme and question how design decisions fit into the overarching goal set forth in the beginning. The most important metric of the amplifier proposed in this thesis is arguably consumed energy per measurement, which is dictated by both the power consumption and settling time of the amplifier. A constant G_m, thus constant bandwidth, amplifier would allow the timing diagram presented in Figure 2.2 to have fixed timing intervals for any operating temperature. However, to sustain a constant bandwidth, the current consumption at higher temperatures would be larger than that at lower temperatures. Therefore, consumed energy per measurement would be dependent on temperature, which is contradictory to the overall big picture. This brings to light an important insight: a design with constant settling time over a wide temperature range will have temperature dependent power consumption, and a design with temperature independent power consumption will have temperature dependent settling time. In either case, the energy consumed per measurement will be dependent on temperature, assuming the duty cycle of the switches are chosen such that energy consumed per measurement is minimized, i.e. dictated by the settling time of the pre-charge buffers and OTA. Constant energy consumption per measurement over a large temperature range can be achieved by sub-optimally assigning duty cycles, where at low temperatures, the circuit settles well within the duty cycle of the switches and at high temperatures, the circuit settles just in time. In the scenario just described, the current reference has a temperature coefficient of zero (i.e. band-gap reference) and the timing diagram is fixed based on worst-case settling times (i.e. high temperature settling times).

As a test chip, it is desirable to make the bias currents through the amplifier adjustable, providing maximum flexibility when testing the circuit. Because of this, the current reference will be created off-chip, either by an external current source or resistor. Three separate references are made, one for the core OTA, and two for each pre-charge buffer. This allows the references to be independently power-cycled when not in use, minimizing the total energy consumed per measurement.

3.6.2 Tail Current Feedback

The tail current source is responsible for delivering the (scaled) reference current to the input differential pair and is usually realized as a current mirror. Up to this point, the tail current source of the amplifier was assumed ideal. In this section we discuss how the tail current is physically implemented. Figure 3.11 below abstracts the input transistors of the OTA as two PMOS devices and depicts a simple current mirror

to produce the tail current. We will first discuss the behavior of this simple tail current source and then present circuitry that makes improvements.
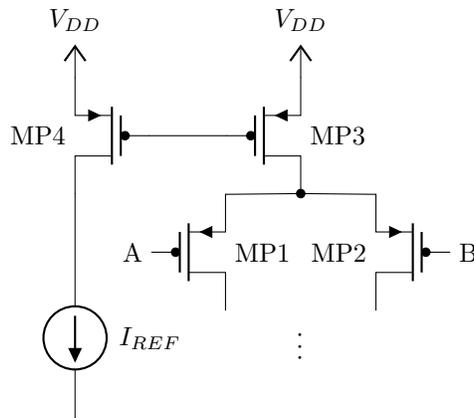
Figure 3.11: Simple differential pair bias network

An important metric for a current source is output resistance; regardless of the voltage across the current source, the output current should always remain the same. In other words, we desire a current source to have infinite output resistance. Cascode and regulated cascode configurations can increase the output resistance of the tail current source, improving this issue and the accuracy of the current mirror; however, these configurations require more voltage headroom to operate, decreasing the input swing of the amplifier. In Figure 3.11 above, as the common mode voltage of inputs A and B increase, the voltage at the drain of MP3 increases correspondingly. There will be a point at which MP3 is crushed and pushed into the triode region ($|V_{DS}| < |V_{GS}| - |V_T|$), and MP3 will cease to accurately mirror I_{REF}. Even before MP3 is pushed into the triode region, the finite output resistance, $\frac{1}{\lambda I_D}$, of MP3 will cause the tail current to modulate slightly with changes in common mode voltage. To summarize, in building the tail current source, there are two traits of interest: 1) the output resistance of the current source, and 2) the voltage, ΔV, required across the current source to ensure I_{REF} is accurately mirrored to the input differential pair. If the output resistance of the tail current source is increased, the common mode gain of the amplifier is decreased, and if less voltage is required to keep MP3 mirroring I_{REF} of current, the input swing of the amplifier is improved. To address both of these issues, tail current feedback, shown in Figure 3.12 below, is employed [8].
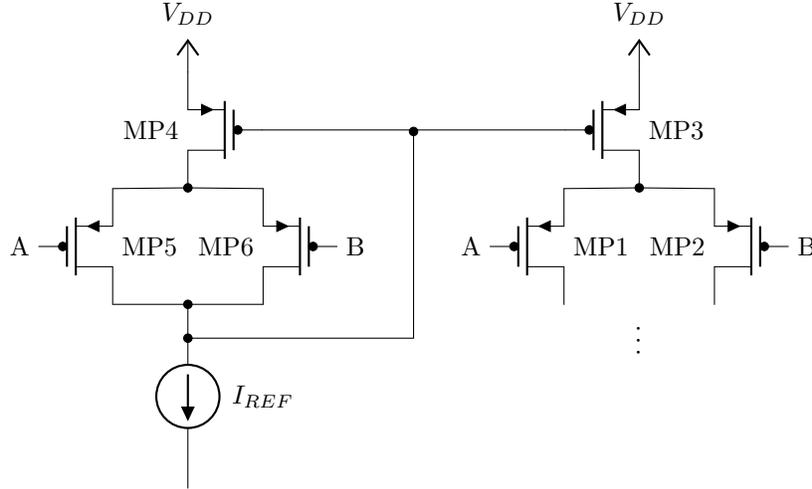
Figure 3.12: Tail current feedback bias

The circuit shown Figure 3.12 forces the drain-to-source voltages of MP4 and MP3 to track. Since the replica circuit, consisting of MP4-6, drives a much smaller capacitive load than the main amplifier, MP5 and MP6 can be scaled. To ensure that voltages in the replica circuit track those in the main amplifier, the widths of MP5 and MP6 are adjusted, while the lengths are set to match those of MP1 and MP2. In the same vein, the current through the transistors is also scaled accordingly. In this particular design, the replica circuitry is scaled to 1/4 the size of the main amplifier, presenting minimal impact to the active power consumption of the amplifier while also ensuring stability. Transistors MP3-4 are made minimum length to minimize their $V_{D,sat}$, as expressed in Equation 3.30, further extending the input common mode range. Table 3.10 below summarizes the design of the feedback circuity shown in Figure 3.12 above. The widths of MP3 and MP4 were sized such that both operate at a current density of $12\mu A/\mu m$. Please note that MP1-2 have already been sized based on discussion in §3.4.1

Component	Value	
I_{REF}	1.2mA	
Transistor	Width	Length
MP3	$400\mu m$	$0.6\mu m$
MP4	$100\mu m$	$0.6\mu m$
MP5-6	$60\mu m$	$0.6\mu m$

Table 3.10: Tail current design summary
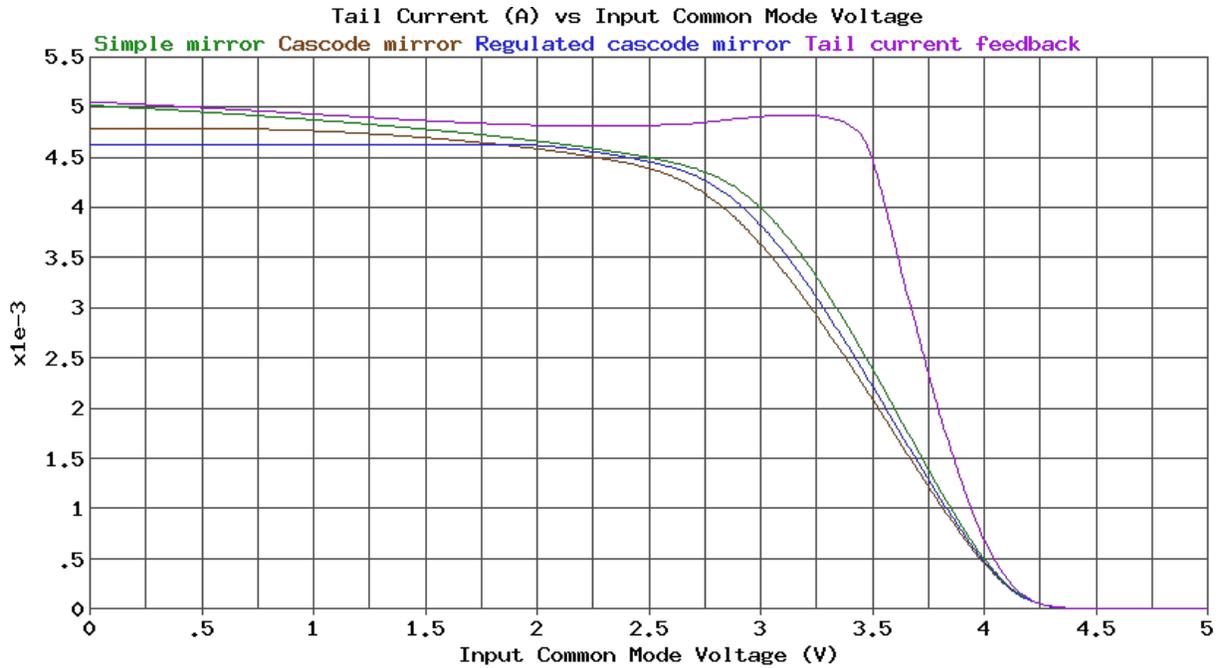
Figure 3.13: Tail current (A) vs input common mode voltage (V)

Figure 3.13 above shows simulation results from a variety of different tail current source configurations: a simple mirror, as depicted in Figure 3.11, a cascode mirror, a regulated cascode mirror, and the replica tail feedback method described above, as shown in Figure 3.12. One can see how the tail current feedback improves the input swing of the amplifier; the tail current persists for a larger span in input common mode voltages. The flat characteristic of the cascode and regulated cascode mirrors, especially at low input common mode voltages, corroborates that these topologies do indeed have very high output resistance. For the tail current feedback, in the event that the input common mode voltage of A and B are low, one can approximate MP5 and MP6 (referring to Figure 3.12) as good conductors (wires), and the replica feedback circuitry reduces to the circuit shown in Figure 3.11. This explains why the tail current for the feedback topology tracks that of the simple mirror for low input common mode voltages. As the common mode input rises, MP5 and MP6 start to conduct less, causing the gate voltage of MP4 to fall, in turn, causing MP4 to drive more current into the differential pair (MP1 and MP2). This negative feedback increases the output resistance of MP4 (and MP3) and extends the range of input voltages for which I_{REF} is accurately mirrored to MP3. This topology allows MP3 to go into the triode region while still accurately mirroring I_{REF}. Though the tail current feedback may not offer as high output resistance as the regulated cascode topology, the improved input swing the tail current feedback provides is deemed worth the trade-off.

3.6.3 Pre-charge Buffers

All schematic reference designators in this section are in reference to Figure 3.14 below unless otherwise noted.
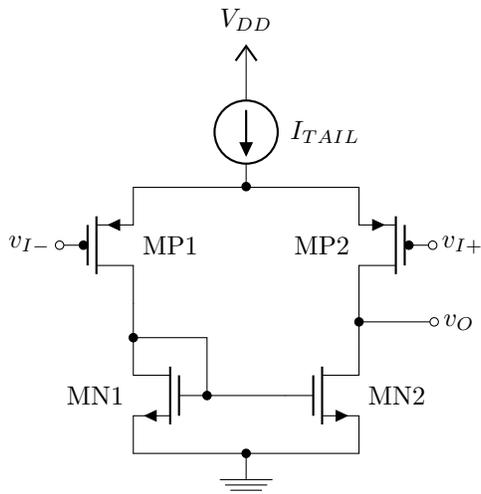
Figure 3.14: Pre-charge buffer

The purpose of the pre-charge buffers are to reduce the load seen by the sensor. As the name implies, the pre-charge buffers pre-charge the input capacitance of the OTA to a voltage similar to that of the output voltage of the sensor[20]. By using the buffers, the input capacitance of the OTA is charged via charge from the power supply rather than charge from the sensor. In the case of a sensor with high source impedance and a pre-charge buffer with low offset voltage, this technique makes the measurements more accurate.

The design of the pre-charge buffers was kept simple by using a single stage op-amp, an OTA itself. Since these buffers are not critical to the operation of the CDS OTA, minimal power and area were allocated to the buffers.

To conserve power, the transistors in the pre-charge buffers are biased at a bias current density of approximately $0.5\mu A/\mu m$. Since the main OTA uses PMOS inputs for the differential pair, PMOS gender inputs for the pre-charge buffers is logical. As with the main amplifier, to maximize g_m/I_D, minimum length transistors were used for MP1 and MP2; thus $\boxed{L_{MP1} = L_{MP2} = 0.6\mu m}$. The load capacitance the pre-charge buffers drive is primarily the input capacitance of the OTA, which was estimated through simulation to be approximately 200fF. Due to the low load capacitance, the input transistors of the buffers need not be

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[20]The pre-charge buffers will have some offset voltage themselves, so the output of the buffers may be different than the input by a few millivolts.

very wide to achieve acceptable bandwidth. To save area, the widths of MP1 and MP2 were made to be $\boxed{W_{MP1} = W_{MP2} = 1\mu\text{m}}$. With the widths determined and the bias current density chosen, the tail current of the pre-charge buffers can now be calculated:

$$\frac{I_{TAIL}}{2} = W_{MP1} * I_D/W = 1\mu\text{m} * 0.5\mu\text{A}/\mu\text{m} = 0.5\mu\text{A} \tag{3.35}$$

$$\boxed{I_{TAIL} = 1\mu\text{A}} \tag{3.36}$$

The NMOS mirror consisting of MN1 and MN2 is sized to $\boxed{W_{MN1} = W_{MN2} = 1\mu\text{m}}$ such that all devices are operating at the same bias current density. The lengths of the mirror transistors are increased to $\boxed{L_{MN1} = L_{MN2} = 1.5\mu\text{m}}$ for the same reasons described in §3.2.1. The tail current source is realized by the circuit shown in Figure 3.11, with I_{REF} being created off-chip using a resistor, or by other means as described in §3.6.1. Each pre-charge buffer has a separate reference current source to facilitate independent power-cycling.

Component	Value	
I_{TAIL}	$1\mu\text{A}$	
Transistor	Width	Length
MP1	$1\mu\text{m}$	$0.6\mu\text{m}$
MP2	$1\mu\text{m}$	$0.6\mu\text{m}$
MN1	$1\mu\text{m}$	$1.5\mu\text{m}$
MN2	$1\mu\text{m}$	$1.5\mu\text{m}$

Table 3.11: Pre-charge buffer design summary

Topology	DC Gain	Open loop f_u[21]	V_{os}[22]	Active Power[23]	$R_{\text{BIAS\_ADJ\_x\_BUF}}$
Differential pair	39dB	4MHz	16mV	$9.9\mu\text{W}$	$4\text{M}\Omega$

Table 3.12: Pre-charge buffer preliminary simulation results

Offset voltage is an important consideration for the pre-charge buffers as it ultimately dictates the minimum small signal voltage for which the pre-charge buffer will actually improve sensor loading. In other words, if the differential signal produced by the sensor is smaller than the offset voltage of the pre-charge buffer, the pre-charge circuitry will actually induce more loading on the sensor and negatively affect the performance of the signal chain. By allowing external control of all the switches in the circuit, the user is provided maximum flexibility and may choose when and when not to use the pre-charge circuitry. Finite gain of the pre-charge buffers will introduce some error and contribute to the offset, as explored in §3.1.4. Finally the pre-charge buffer must be able to settle quickly. With a unity gain frequency of 4MHz, the buffers should be able to

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[21]Simulated with $C_L = 200\text{fF}$
[22]Measured with a 2.5V DC input signal.
[23]Measured with a 2.5V DC input signal.

charge the input capacitances of the OTA in a timely fashion; the settling time of the system is still dictated by the main amplifier (as discussed in §3.1.6).

3.6.4 Output Cascode Biasing

All schematic reference designators in this section are in reference to Figure 3.15 below unless otherwise noted.
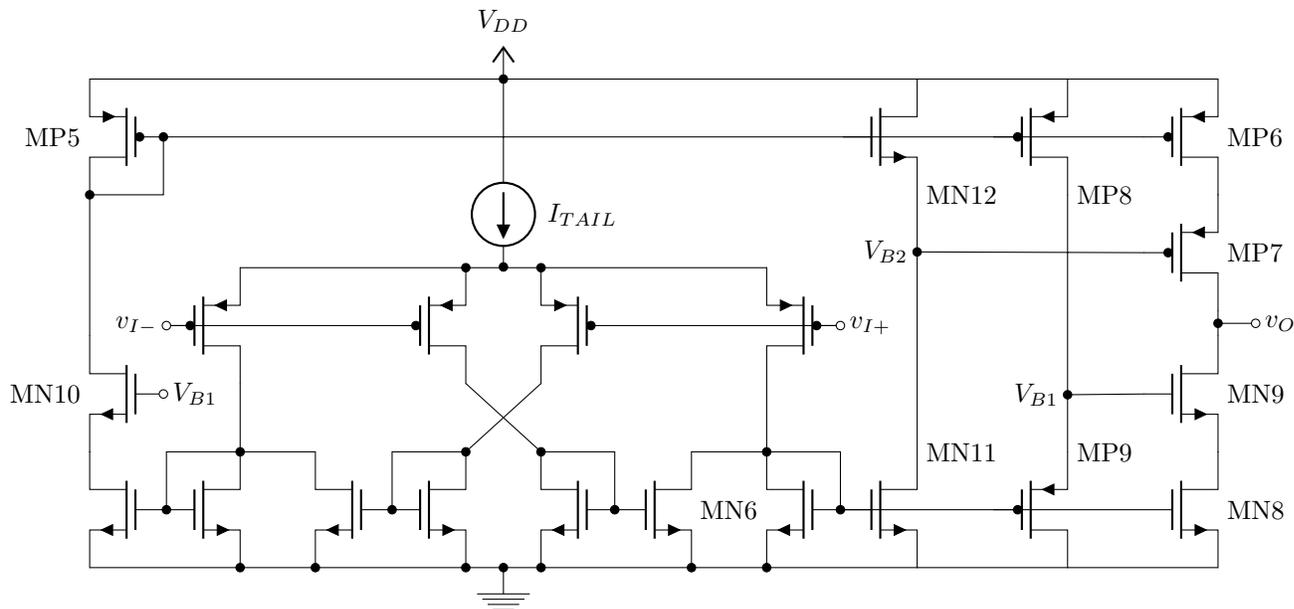
Figure 3.15: NCM OTA with output cascode and bias

For initial simulation, the output cascode devices were biased using ideal voltage sources. Ultimately, these voltages must be realized with physical devices. In order to keep the energy per measurement low, it is preferable that the bias circuitry does not consume substantial power. This section describes the decisions made while designing such circuitry.

Bias voltages can be created quite simply by running a current through a diode connected transistor. Assuming $\lambda = 0$, the gate to source voltage, V_{GS}, of said transistor can be expressed as:

$$V_{GS} = V_T + \sqrt{\frac{2I_D}{\mu C_{ox} \frac{W}{L}}} \tag{3.37}$$

A constant bias voltage, V_{GS}, results from a constant bias current, I_D. Sometimes, in order to keep power consumption low, these biasing transistors can assume narrow dimensions, that is, $W << L$. While this technique certainly works to create bias voltages for cascode devices, a slightly different methodology was

employed in this design.

It was discovered in simulation that using voltage sources to bias the cascode devices led to an offset voltage that was dependent on the common mode input voltage. Offsets are typically caused by asymmetries in the signal path of the amplifier, most notably, the current mirrors. Replacing these mirrors with ideal mirrors made the offset voltage independent of common mode input voltage, indicating that these were indeed the source of the problem. To address this issue, the scheme presented in Figure 3.15 was implemented.

In Figure 3.15, MP8-9 and MN11-12 form the biasing network for the cascode devices. In essence, MP9 and MN12 are source followers that are biased with current set by MP8 and MN11, respectively. The source followers reduce mirror errors by ensuring the drain-to-source voltages of select current mirrors track. Let us take for example the PMOS mirror consisting of MP5 and MP6. To minimize errors, we wish to have $|V_{DS,MP5}| = |V_{DS,MP6}|$ across all common mode input voltages. Noting that $|V_{DS,MP5}| = |V_{GS,MP5}|$, we desire $|V_{DS,MP6}| = |V_{GS,MP5}|$. MN12 acts as a source follower such that V_{B2} follows the gate voltage of MP5, shifted down by one V_{GS}. By biasing the cascode device, MP7, with V_{B2}, it follows that the source voltage of MP7 sits one V_{GS} above its gate. Thus, $|V_{DS,MP6}| = |V_{DS,MP5}| - V_{GS,MN12} + |V_{GS,MP7}|$. Assuming $V_{GS,MN12} = |V_{GS,MP7}|$, we have $|V_{DS,MP6}| = |V_{DS,MN5}|$. Similar calculations hold for the mirror consisting of MN6 and MN8 and the corresponding bias circuitry (MP8, MP9). Since low currents flow through the outer legs of the amplifier, sizing MN11 and MP8 the same as MN8 and MP6 does not add significant current draw and increases the power consumption by approximately 10%. Transistors MN12 and MP9 were sized to minimize the offset dependence on input common mode. Table 3.13 below summarizes the design results, and the following graph depicts the offset voltage variation on common mode input for the two biasing techniques.

Transistor	Width	Length
MP8-9	50μm	1.5μm
MN11-12	50μm	1.5μm

Table 3.13: Output cascode bias circuitry
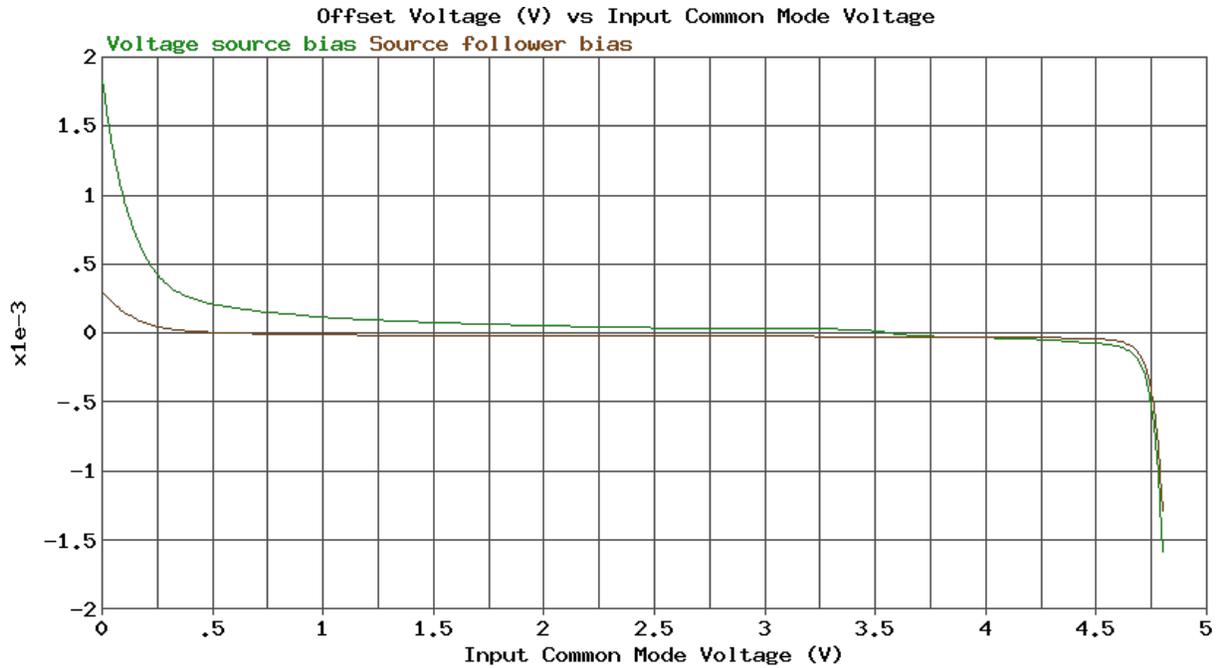
Figure 3.16: Offset voltage (V) vs input common mode voltage (V)

Larger measures may be taken to minimize offsets; however, the CDS scheme deems such heroics fruitless. The presented biasing technique produces offset variations that are on the order of 1 LSB over a large range of common mode input voltages. This variation is sufficient for this test chip.

3.6.5 Inverters

All schematic reference designators in this section are in reference to Figure 3.17 below unless otherwise noted.
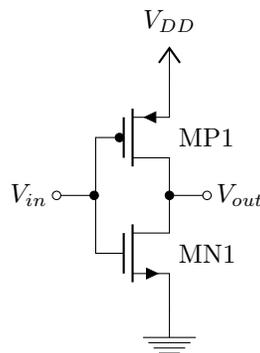
Figure 3.17: Inverter

It is necessary to produce the complement of many digital signals to ensure proper operation of this circuit. For example, the transmission gates described below in §3.6.8 need both a digital high (for the NMOS

devices) and a digital low (for the PMOS devices) to turn-on. Inverters are used to create complements of all the digital signals entering the chip. The structure of the inverters used in this design is shown in Figure 3.17. MP1 and MP2 are created using minimum length and width devices to save area and minimize propagation delay. Table 3.14 below summarizes the design.

Transistor	Width	Length
MP1	0.22μm	0.6μm
MN1	0.22μm	0.6μm

Table 3.14: Inverter design summary

3.6.6 Digital Buffers

All schematic reference designators in this section are in reference to Figure 3.18 below unless otherwise noted.

Figure 3.18: Schmitt trigger

CMOS Schmitt triggers are used to buffer the digital signals that enter the chip [9]. The digital signals that are buffered include the switch control lines for switches A-E, the shutdown pins, the gain select switch, and the optional switch to switch in a dummy load capacitor when the SAR ADC is performing its successive approximation algorithm.

A Schmitt trigger is a comparator that provides hysteresis such that erratic switching behavior does not occur. In some circuits, this hysteresis must be well defined; however, for purposes of buffering the digital signals mentioned above, the amount of hysteresis does not need to be exact[24]. One should recognize MP1-2 and MN1-2 as two cascaded inverters, which, in concert, buffer the digital input signal. MN3 is an extra device that adds positive feedback, which therefore introduces hysteresis. When the input of the Schmitt trigger is low, the output is correspondingly low, and in turn, MN3 is off. As the input rises, MN1 begins

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[24]One can make an argument that hysteresis is not even needed!

to turn-on and MP1 begins to turn-off. At some $V_{in} = V_{01}$, the output goes high. This transition voltage, V_{01}, is dictated by the ratio of widths between MP1 and MN1. Now that the output is high, MN3 turns on, presenting additional conductance to GND at node X. Thus, as the input falls from high to low, MP1 must work against both MN1 and MN3 to pull node X high. Hysteresis is introduced by virtue that MN3 is inactive for the low-high transition, while active during the high-low transition. In summary, to adjust V_{01}, one can change the ratio of widths between MP1 and MN1, and to modify V_{10}, one can alter the width of MN3. Lengths may also be used as a knob in the design; however, in this Schmitt trigger, all transistors were designed with minimum length.

Transistor	Width	Length
MP1	4μm	0.6μm
MP2	1μm	0.6μm
MN1	1μm	0.6μm
MN2	1μm	0.6μm
MN3	0.3μm	0.6μm

Table 3.15: Schmitt trigger design summary

V_{01}	V_{10}	V_{Hys}
2.57V	2.20V	0.37V

Table 3.16: Schmitt trigger preliminary simulation results

3.6.7 Current Stealing Mirror Adjustment

All schematic reference designators in this section are in reference to Figure 3.19 below unless otherwise noted.
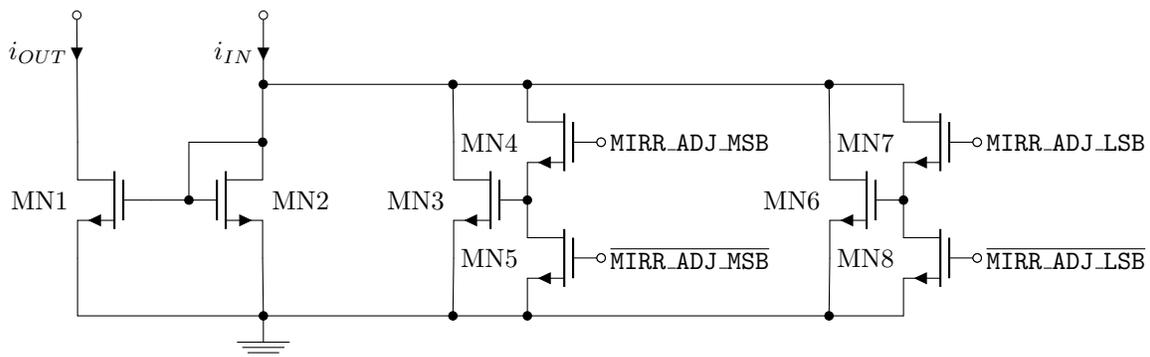
Figure 3.19: Adjustable current mirror

As mentioned in §3.4, there is a concern that the current stealing mirrors in Figure 3.9 become too good and start to steal more current than what is flowing through MP3 and MP4, resulting in a dead band, where some small differential signal is needed to wake up the NCM OTA. §3.4 proposed reasons why 1:1 current

stealing mirrors may work; however, a 1:1 mirror may still be cutting the current stealing too close due to variations that can occur from device to device. Thus, to address this risk, the current stealing mirrors that consist of MN1:MN3 and MN2:MN4, shown in Figure 3.9, are designed to have configurable current gain and are replaced by the circuity shown in Figure 3.19. The user is able to control the values of `MIRR_ADJ_MSB` and `MIRR_ADJ_LSB` to modulate the width of MN2.

Transistor	Width	Length
MN1-2	30μm	1.5μm
MN3	3μm	1.5μm
MN6	2μm	1.5μm
MN4-5,7-8	0.22μm	0.6μm

Table 3.17: Adjustable current mirror design summary

`MIRR_ADJ`	i_{OUT}/i_{IN}	% Stealing	$R_{\text{BIAS\_ADJ\_OTA}}$	DC gain	Open Loop f_u[25]
00	30/30	100%	20kΩ	105dB	40MHz
01	30/32	94%	40kΩ	103dB	35MHz
10	30/33	91%	50kΩ	102dB	33MHz
11	30/35	86%	60kΩ	100dB	31MHz

Table 3.18: Adjustable current mirror preliminary simulation results

For the same biasing conditions, a lower current stealing ratio results in lower gain as more bias current flows through the output leg of the amplifier. The tail current of the amplifier, set by $R_{\text{BIAS\_ADJ\_OTA}}$, can be adjusted based on the value of `MIRR_ADJ` to ensure the amplifier has gain of approximately 100dB. Decreasing the tail current by increasing $R_{\text{BIAS\_ADJ\_OTA}}$ helps the gain; however, bandwidth and slew rate are degraded.

3.6.8 Switches

Naturally, in a switched capacitor circuit, there are switches. For simplicity, the switches are realized as complimentary switches, or in other words, transmission gates. This removes the need for any bootstrap circuitry that may complicate the design.
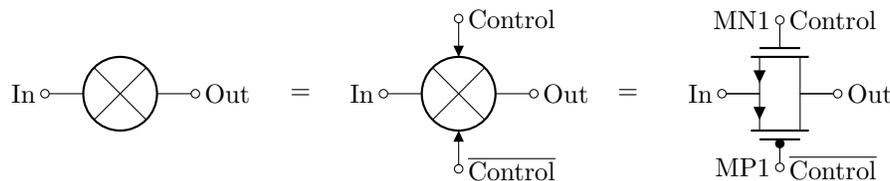
Figure 3.20: Circuit implementation of a switch

The switches in the CDS OTA are broken up into five categories: front end switches (switch A, B, C, and

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[25]Simulated with $C_L = 31.875$pF

D), the feedback switch (switch E), the gain select switch, the stability capacitor switch, and the shutdown switches. For all MOS devices, it is helpful to note that on-resistance can be expressed as:

$$R_{ON} = \frac{1}{\mu C_{ox} W/L (V_{GS} - V_T)} \tag{3.38}$$

where μ is the mobility of the type of device, e.g. μ_p or μ_n. The switches were simulated using the testbench shown in Figure 3.6.8.
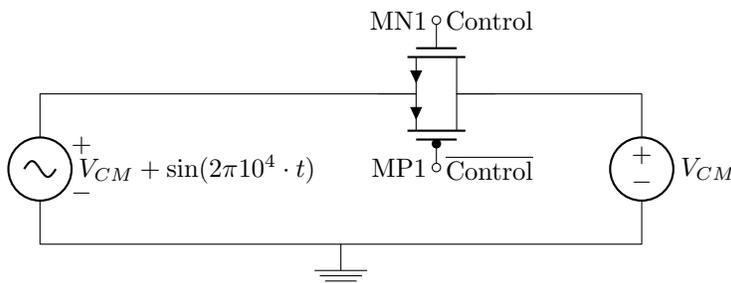
Figure 3.21: Switch testbench to determine incremental switch on-resistance

Front End Switches

Switches A, B, C and D are referred to as "front end switches." If we think of these switches as resistors with value $R = R_{ON}$ when on, it becomes obvious that these switches appear as additional source resistance to the amplifier. In addition, as with any physical resistance, these switches contribute noise, specifically thermal noise. The front end switches also cause errors due to charge injection when they transition states. To minimize charge injection, relatively small devices are used for these front end switches. Referring to Figure 3.20, the widths for MN1 and MP1 were chosen to be $\boxed{W_{MN1} = 1\mu m}$ and $\boxed{W_{MP1} = 5\mu m}$. The lengths of both MN1 and MP1 were set to $\boxed{L_{MN1} = L_{MP1} = 0.6\mu m}$ to minimize R_{ON}. The left-most peak in the graph shown in Figure 3.22 primarily corresponds to the on-resistance of the NMOS device, and similarly, the right-most peak primarily corresponds to that of the PMOS device. Due to lower mobility in PMOS devices, the width of the MP1 was increased past that of MN1 until both peaks roughly matched.

Transistor	Width	Length
MP1	5μm	0.6μm
MN1	1μm	0.6μm

Table 3.19: Front end switch design summary

On-Resistance of Transmission Gate (Ron: Ohms) vs Common Mode Voltage

[1.977099]
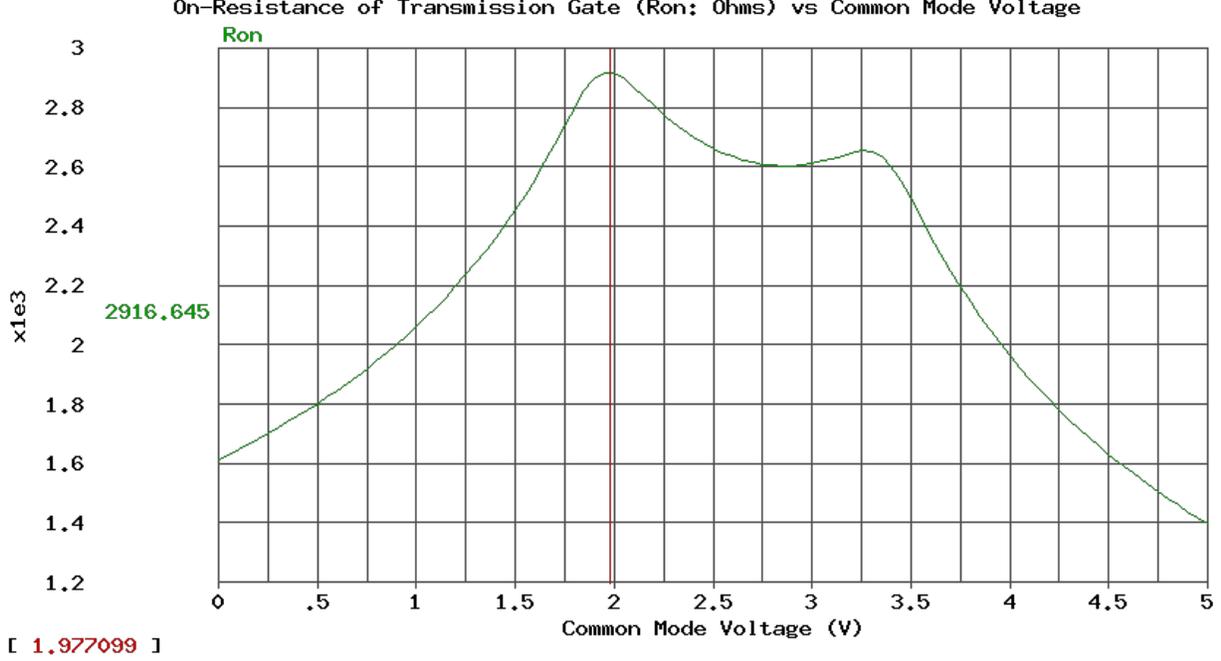
Figure 3.22: On-resistance of front end transmission gate (Ω) vs common mode voltage (V)

Figure 3.22 shows that the maximum on-resistance of switches A, B, C and D is approximately $R_{ON,max} \approx 3k\Omega$. The thermal noise due to the random motion of electrons in a resistor with resistance R can be expressed as $\overline{V_n^2} = 4kTR\Delta f$. Ultimately, since this noise is present at the input of the OTA, the noise from the front end switches will be multiplied by the closed loop gain of the amplifier. Considering this and the bandwidths of the different gain configurations, the gain of 16 presents the largest RMS noise voltage to the input of the ADC. Assuming worst-case $R_{ON} = 3k\Omega$, $\Delta f = 3$MHz (corresponding to gain of 16 configuration) the input referred RMS noise voltage attributed to the front end switches can be calculated at T=300K:

$$V_{n,RMS} = \sqrt{\overline{V_n^2}} = \sqrt{4kTR_{ON}\Delta f} \approx 12\mu V_{RMS} \tag{3.39}$$

Multiplying by 16, we arrive at the output referred RMS noise voltage, which we can also express as peak noise voltage:

$$V_{n,RMS} \approx 192\mu V_{RMS} \tag{3.40}$$

$$V_{n,peak} = \sqrt{2} * V_{n,RMS} \approx 272\mu V \tag{3.41}$$

Assuming the ADC input range is 0V to 5V, 1 LSB corresponds to approximately $\frac{5V}{2^{16}} = 76\mu V$. The noise contributed by the front end switches is roughly on the order of a few LSB of the ADC. This will suffice for proof-of-concept.

Gain Select Switch

The gain select switch is responsible for selecting the closed loop gain of the amplifier. As mentioned before, the amplifier may be operated in a closed loop gain of 4 or 16. The gain select circuitry is shown in Figure 3.23 below.
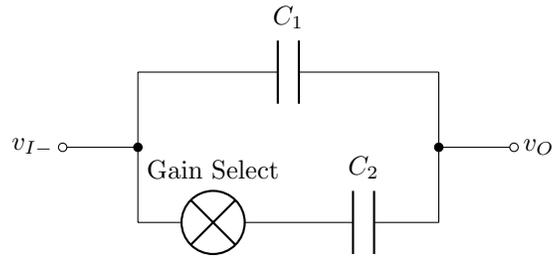
Figure 3.23: Gain select block

In the case of the gain of 4 configuration, C_f should equal 10pF, whereas in the gain of 16 configuration, C_f should equal 2pF. To achieve this, in Figure 3.23 above, $C_1 = 2$pF and $C_2 = 8$pF. When the gain select switch is open, the feedback capacitor is solely $C_1 = 2$pF. However, when the gain select switch is closed, the OTA now "sees" a combined feedback capacitance of $C_1 || C_2 = 10$pF.

The placement of the gain select switch is not arbitrary. Physically, C_2 is realized by two parallel metal plates with a dielectric in between the plates. Each of these plates forms a parasitic capacitance to ground as explicitly shown in Figures 3.24 and 3.25.
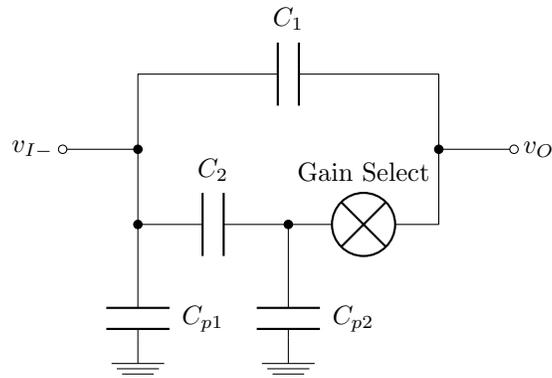
Figure 3.24: Gain select block with parasitic capacitances; switch between C_2 and v_O
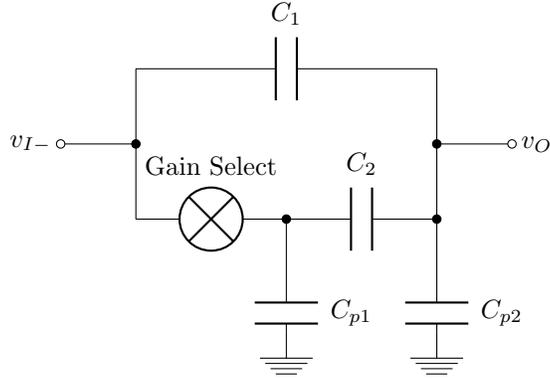
Figure 3.25: Gain select block with parasitic capacitances; switch between v_{I-} and C_2

In the case shown in Figure 3.24, the switch is placed between C_2, and the output of the OTA and parasitic capacitance is introduced to the negative input of the OTA. Since the capacitance at the negative input of the OTA directly impacts the closed loop gain of the amplifier, this configuration will introduce error and lead to a slightly larger closed loop gain, $(1 + \frac{C_i}{C_f})$.

In the case shown in Figure 3.25, with the switch located between the negative input of the OTA and C_2, the switch isolates the parasitic capacitance C_{p1} from the negative input of the OTA. However, now the output of the OTA sees C_{p2}. Since the output of the OTA can easily drive capacitive loads, this should not pose a problem to the overall scheme. The feedback will force the output to the correct value, regardless of the small parasitics present on v_O. Rather than introducing closed loop gain error, as in the case before, this configuration slightly reduces the bandwidth of the amplifier, as C_L is now $C_L = (C_{ADC} + C_{p2}) + (C_f C_i)/(C_f + C_i)$.

By placing the switch such that it is between the negative input of the OTA and C_1, parasitic capacitance at the negative input of the OTA is minimized, and closed loop gain errors are thus reduced. The placement of the gain select switch comes at the cost of bandwidth; however, with some extra bandwidth built into the design of the OTA, this is not a problem.

The incremental circuit of the gain select block can be modeled as shown in Figure 3.26.
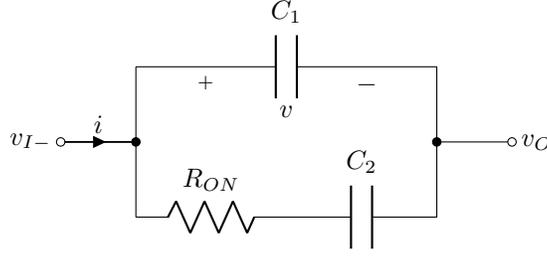
Figure 3.26: Equivalent incremental circuit of gain select block

It is important that the gain select block behaves as a capacitor over the frequency range of interest. There will be some frequency at which the impedance of R_{ON} dominates the impedance of the lower branch of the circuit shown in Figure 3.26, that is when $R_{ON} = |1/(sC_2)|$. In other words, R_{ON} introduces a zero in the transfer function of the gain select block:

$$H(s) = \frac{V(s)}{I(s)} = \frac{sC_2 R_{ON} + 1}{s^2 C_1 C_2 R_{ON} + s(C_1 + C_2)} \tag{3.42}$$

Noting that $C_2 = 8\text{pF}$, the location of the zero, ω_z can be calculated:

$$\omega_z = \frac{1}{R_{ON} C_2} = \frac{1}{R_{ON} \cdot 8\text{pF}} \tag{3.43}$$

Correspondingly:

$$f_z = \frac{1}{2\pi \cdot R_{ON} \cdot 8\text{pF}} \tag{3.44}$$

The frequency range of interest mentioned above for which this gain select block must appear as a capacitor is dictated by the unity gain frequency of the OTA when connected in a gain of 4 configuration, as this is when the gain select switch is on. The unity gain frequency of an amplifier describes the frequency range for which the circuit behaves as an amplifier. Above this frequency, input signals are attenuated by the circuit. Thus, we desire the location of the zero described above to fall (well) above the unity gain frequency of the amplifier when configured with a gain of 4. When configured as such, the unity gain frequency of the amplifier must be at least 8MHz (as discussed in §3.1.6). With this in mind, the maximum value of R_{ON} can be determined using Equation 3.44:

$$8\text{MHz} = \frac{1}{2\pi \cdot R_{ON} \cdot 8\text{pF}} \tag{3.45}$$

$$R_{ON} \approx 2.5k\Omega \tag{3.46}$$

With the maximum R_{ON} in hand, device sizing can begin. Using the testbench shown in Figure 3.6.8,

R_{ON} of the transmission gate was simulated with various device widths. Minimum length transistors were used, and the widths were modified to achieve adequate R_{ON}. For the gain select switch, a starting point of $W_{MN1} = 1\mu m$ was chosen, where MN1 (and MP1) refers to Figure 3.20. The widths of both MN1 and MP1 were adjusted until acceptable (much less than 2.5kΩ) R_{ON} was achieved, as shown in Figure 3.27 below.
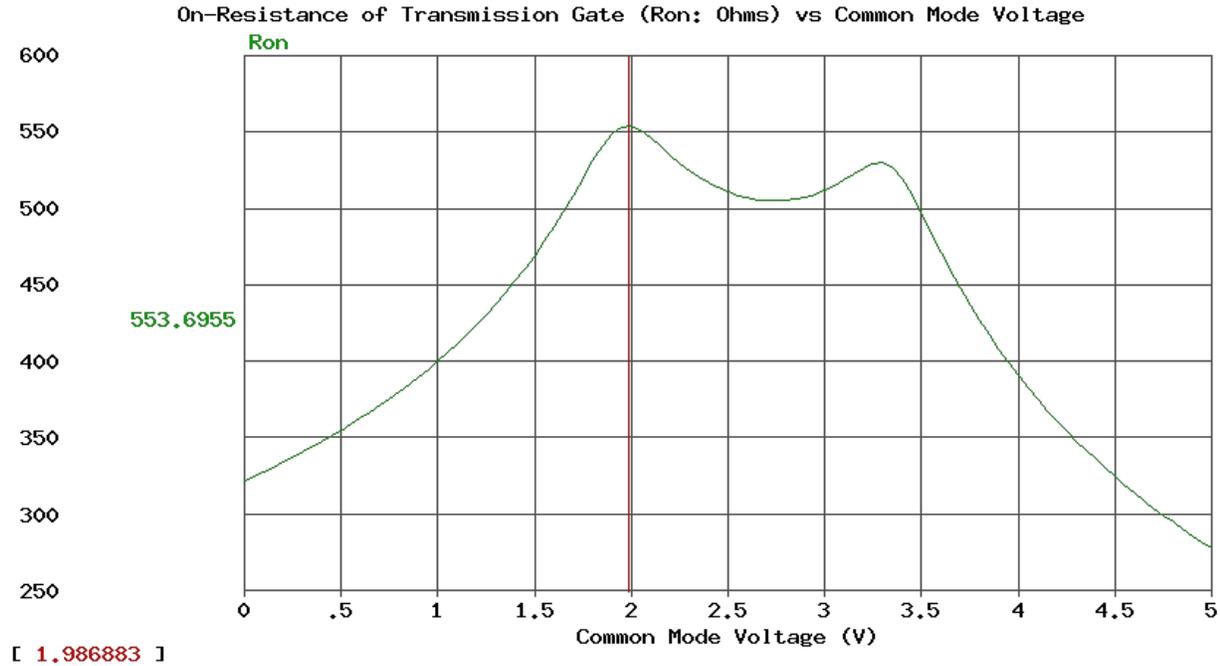
Figure 3.27: On-resistance of gain select transmission gate (Ω) vs common mode voltage (V)

Table 3.20 below summarizes the sizing results for the gain select switch.

Transistor	Width	Length
MP1	25μm	0.6μm
MN1	5μm	0.6μm

Table 3.20: Gain select switch design summary

Using maximum $R_{ON} \approx 554\Omega$ obtained from Figure 3.27, the corresponding zero the switch introduces into the transfer function presented in Equation 3.42 resides at $f_z \approx 36$MHz, well above the 8MHz unity gain frequency of the amplifier!

Feedback Switch

The feedback switch (switch E), which is responsible for clearing the charge on C_f at the beginning of the CDS cycle, is not an especially critical switch. Since switch E opens before the first ADC sample is taken, any errors that may be introduced by charge injection are captured in this initial measurement. Since the

charge on the negative input of OTA is frozen once switch E opens, these same errors are also captured in the second ADC sample. Thus, the correlated double sampling will cancel the resulting error switch E introduces. For simplicity, the same device sizes used for the gain select switch are used for switch E.

Stability Capacitor Switch

The stability capacitor switch connects an optional, dummy capacitor to the output of the OTA. The dummy capacitor is intended to be connected to the output when the SAR ADC is carrying out its successive approximation algorithm. When the ADC is in conversion mode, the switches shown in Figure 3.1 are open, and the effective C_L of the OTA consists of C_{PIN} in parallel with the series combination of C_f and C_i. This state may render the OTA unstable and cause unwanted ringing that may interfere with the ADC algorithm. Thus, the stability capacitor offers a solution to this problem by increasing the load capacitance on the output of the OTA when the stability capacitor switch is on. It is desirable to make the stability capacitor switch and the dummy capacitor have similar impedance to that of the SAR ADC input, as the OTA is designed to be stable when loaded by the AD7686. As mentioned above, the switch for the gain select block has a maximum on-resistance of approximately 554Ω. Since 554Ω is reasonably close to R_{IN} of the ADC shown in Figure 3.1, the switch used for the gain select block is re-used for this application.

Shutdown Switches

The shutdown switches are responsible for putting the OTA and pre-charge buffers in shutdown mode. This includes disconnecting the bias resistors and pulling down/up select nodes in the OTA and pre-charge buffer circuitry. Like the switches mentioned above, the switches responsible for disconnecting the bias resistors are implemented as transmission gates. The same transmission gate used for the gain select switch is used for this application, i.e. MN1 and MP1 are sized according to Table 3.20. One may argue that a smaller transmission gate may have less leakage when off, however, the leakage of the larger transmission gates presented in Table 3.20 is still significantly less than the 1nA standby current associated with the AD7686 ADC. Thus, the larger transmission gates allow for the use of a wider range of bias adjust resistors while still ensuring adequately low leakage current. Each pre-charge buffer and the OTA have separate bias adjust shutdown switches to independently disconnect the corresponding bias resistor in the event of shutdown.

As mentioned, there are also pull-up/pull-down switches that ensure certain nodes of the amplifier are fixed to either V_{DD} or GND in the event of shutdown. Any high impedance node that is left floating in shutdown could cause the amplifier to turn back on and draw non-negligible shutdown current. Since these shutdown switches are directly connected to either V_{DD} (PMOS pull-ups) or GND (NMOS pull-downs), only

a single device, NMOS or PMOS, is needed, i.e. no transmission gates. These devices are realized using minimum sized transistors with $\boxed{W = 0.22\mu m}$ and $\boxed{L = 0.6\mu m}$ for both PMOS and NMOS, minimizing leakage currents and area. The circuitry is configured such that the user may independently shutdown each pre-charge buffer and OTA, allowing all, some, or none to be shutdown at a given time.

Chapter 4

Simulation Results

A design has been proposed in the prior chapter. This section of the thesis concerns itself with the simulation results of the proposed amplifier and the accompanying drive scheme to confirm the theoretical calculations and predictions. First, the simulation results of just the amplifier are discussed, and following that, the simulation results of the entire correlated double sampling scheme are presented. These simulation results are predicted behaviors of the electronics; in reality, actual lab results will vary due to device mismatches, physical layout, and other non-ideal effects that are not captured in simulation. Please note that when the simulation results for a particular `MIRR_ADJ` value are presented, you can assume the appropriate $R_{\text{BIAS\_ADJ\_OTA}}$ resistor is used, as given in Table 3.18.

4.1   OTA Performance

The simulation results of this section pertain solely to the OTA itself. Such studies include in depth investigations of open loop gain, bandwidth, common mode rejection ratio (CMRR), positive power supply rejection ratio (PSRR+), noise, and input and output swing of the OTA. Higher-level simulations regarding the entire CDS scheme can be found in §4.2.

4.1.1   Open Loop Gain, Bandwidth, and Phase Margin

When simulating the amplifier, we are most concerned with worst-case scenarios. For the given OTA, we are particularly interested in the behavior of the amplifier when loaded by 31.875pF. This corresponds to load the amplifier sees when connected in a closed loop gain of 16 and is the lowest load capacitance the OTA needs to drive during the operation of the CDS scheme. If the amplifier is stable for this configuration, it should also be stable when loaded by 37.5pF and 60pF. Additionally, the closed loop gain of 16 configuration

necessitates the largest bandwidth. We strive for a unity gain bandwidth of approximately 32MHz or greater when the OTA is driving a load of 31.875pF. The following plots show the AC behavior of the amplifier with a load capacitance of 31.875pF for all possible values of MIRR_ADJ. Please note that the design goal was to create an amplifier with unity gain frequency of approximately 32MHz and open loop gain of at least 100dB. Figures 4.1 through 4.4 show that this design specification was met and exceeded for all configurations except for MIRR_ADJ = 11. Since the constraint on open loop gain and bandwidth are loose requirements, the performance of the OTA when MIRR_ADJ = 11 is sufficient for the proof-of-concept application in mind. Table 4.4 summarizes the differential open loop gain of the amplifier in all configurations. These values are later used to calculate CMRR and PSRR+ of the amplifier.
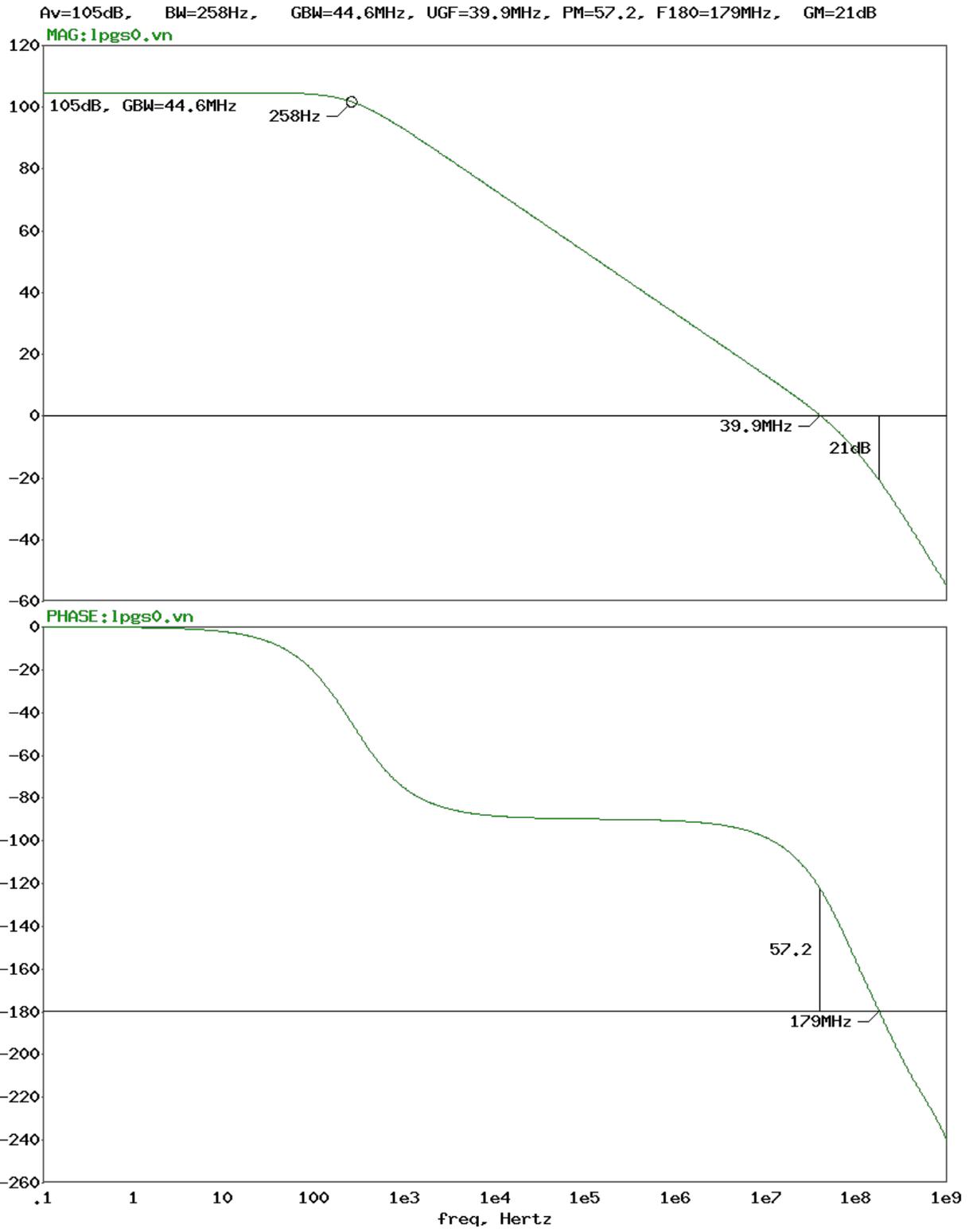
Figure 4.1: Gain and phase characteristics vs frequency (Hz) with `MIRR_ADJ = 00` and $C_L = 31.875$pF

Av=103dB,   BW=270Hz,   GBW=38MHz,   UGF=34.8MHz, PM=60.1, F180=167MHz,   GM=21.5dB

MAG:lpgs0.vn

103dB, GBW=38MHz

270Hz

34.8MHz

21.5dB

PHASE:lpgs0.vn

60.1

167MHz

freq, Hertz
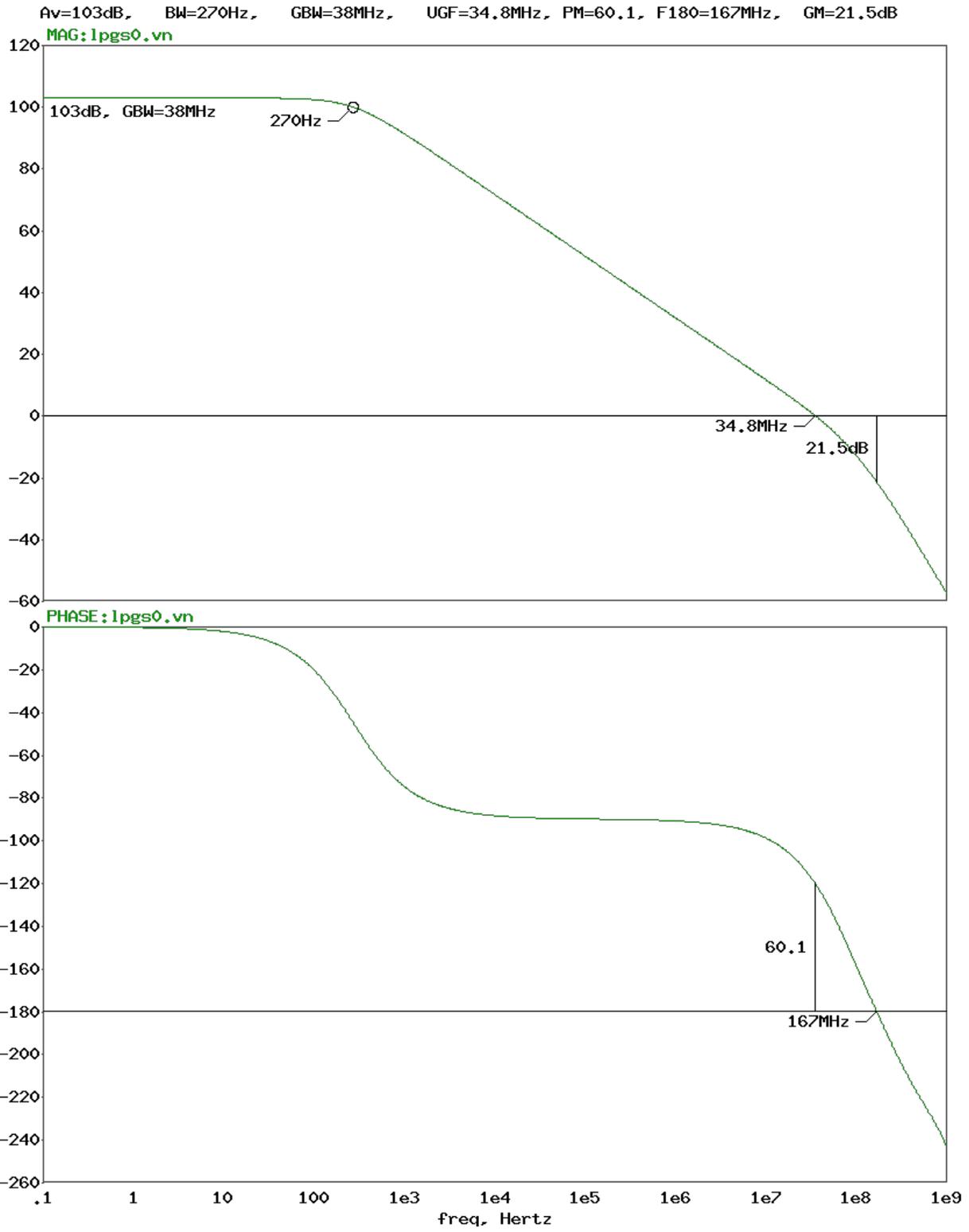
Figure 4.2: Gain and phase characteristics vs frequency (Hz) with MIRR_ADJ = 01 and $C_L = 31.875$pF
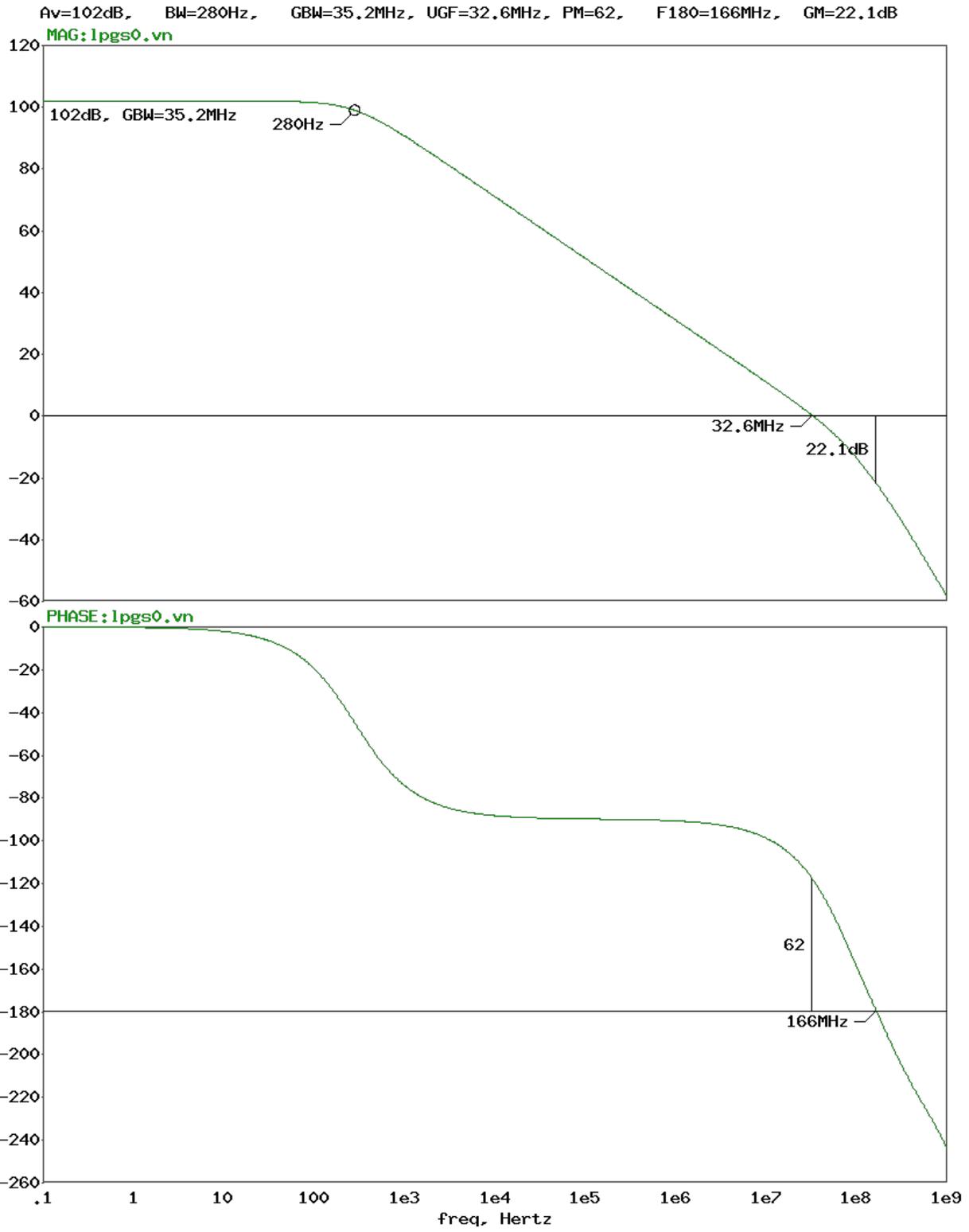
Figure 4.3: Gain and phase characteristics vs frequency (Hz) with MIRR_ADJ = 10 and $C_L = 31.875$pF
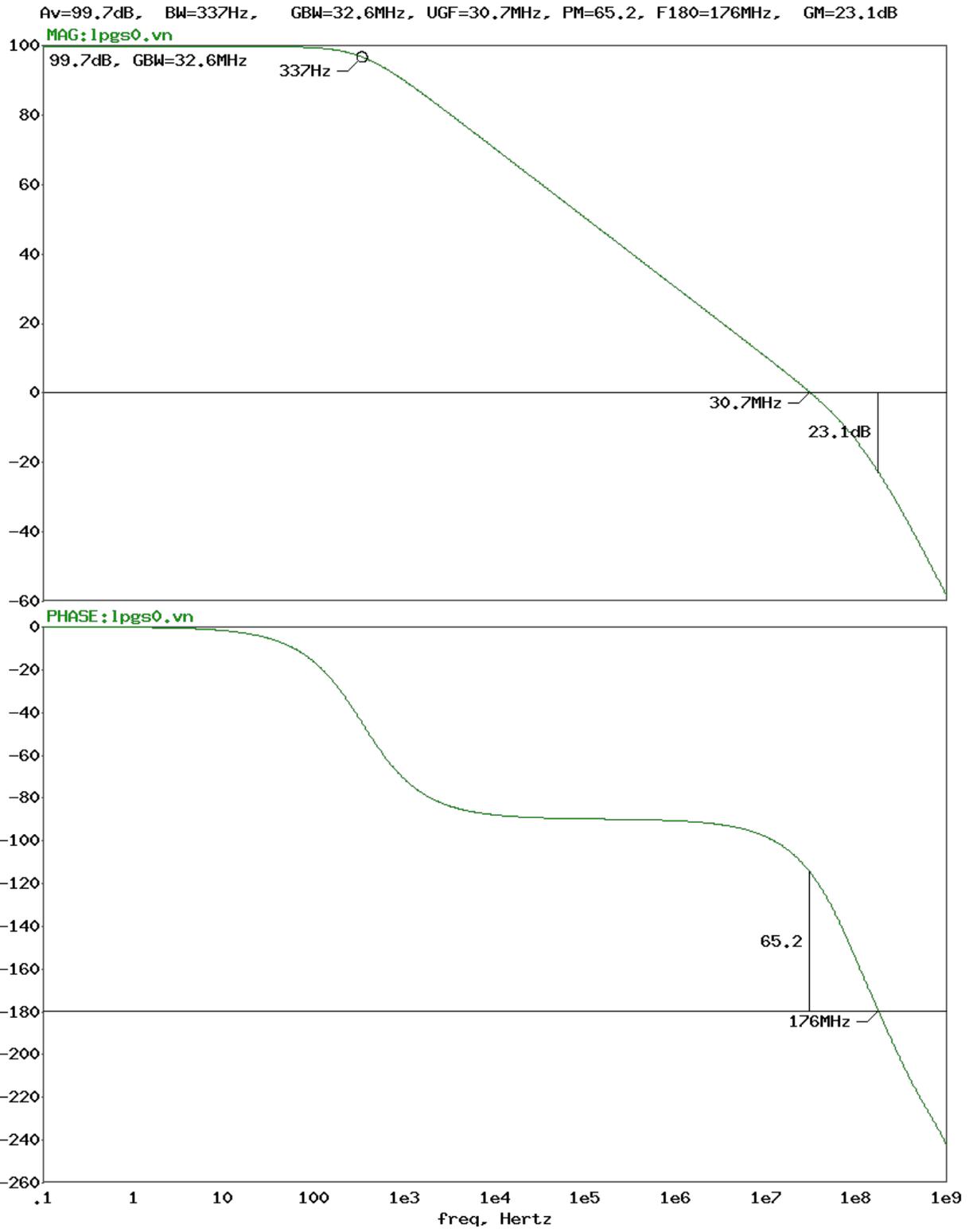
Figure 4.4: Gain and phase characteristics vs frequency (Hz) with MIRR_ADJ = 11 and $C_L = 31.875$pF

4.1.2 CMRR

CMRR is defined as the ratio of open loop differential gain (a_{vd}) to common mode gain (a_{cm}) of the amplifier:

$$\text{CMRR} = \frac{a_{vd}}{a_{cm}} \tag{4.1}$$

Figures 4.5 through 4.8 depict the common mode gain (not CMRR!) of the amplifier for all values of `MIRR_ADJ`. For simulating the common mode gain, a signal $V_{in} = V_{CM} + v_{cm}$ was applied to both inputs of the amplifier. For the applied signal, $V_{CM} = 2.5$V, and v_{cm} was a small signal AC waveform with AC magnitude of 1. The common mode gain was compared to the open loop differential gains, and the results are summarized in Table 4.4 at the end of this chapter.
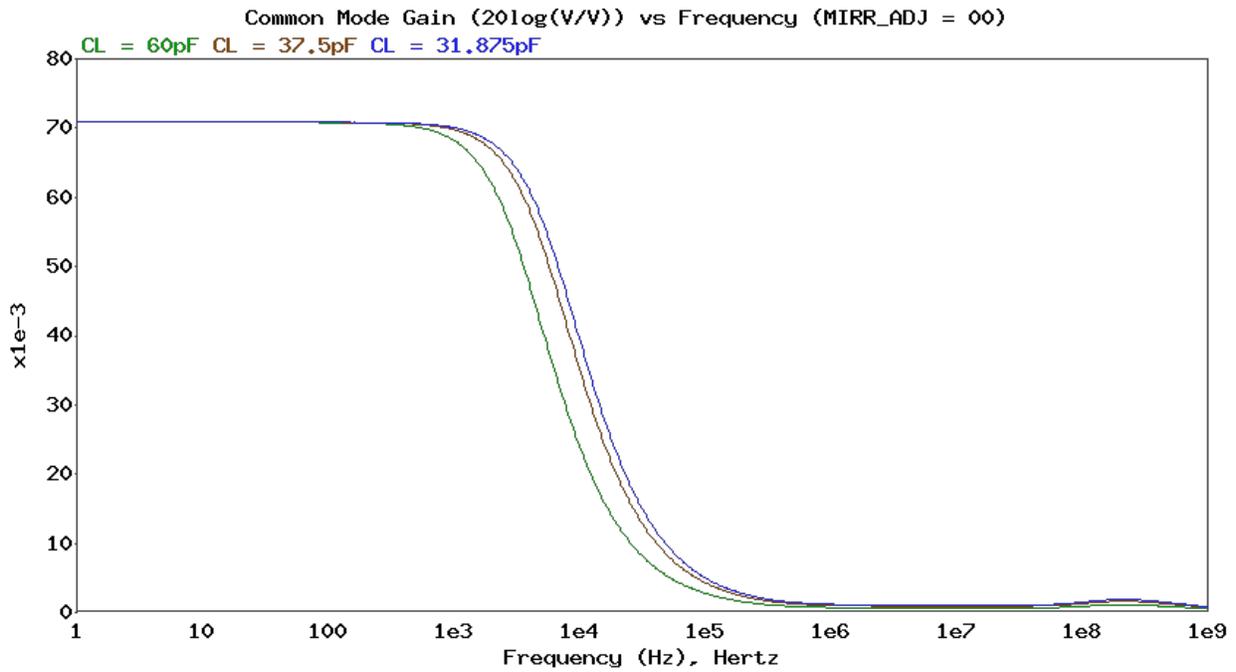
Figure 4.5: Common mode gain (dB) vs frequency (Hz) with `MIRR_ADJ = 00`
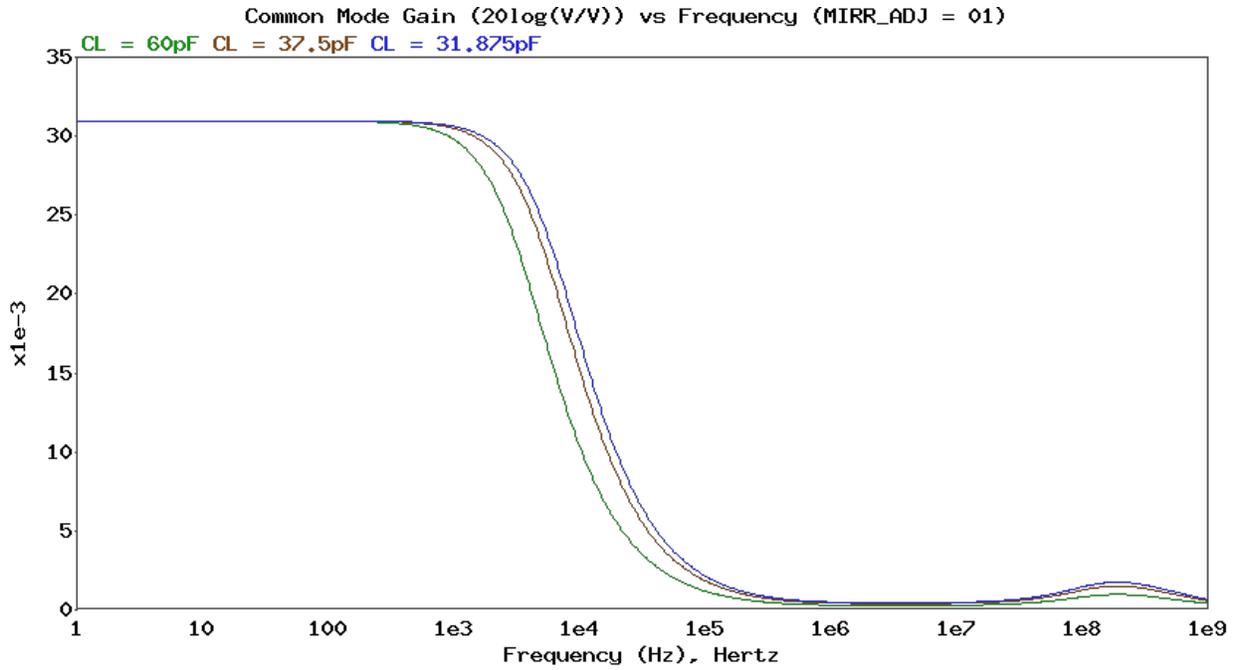
Figure 4.6: Common mode gain (dB) vs frequency (Hz) with MIRR_ADJ = 01
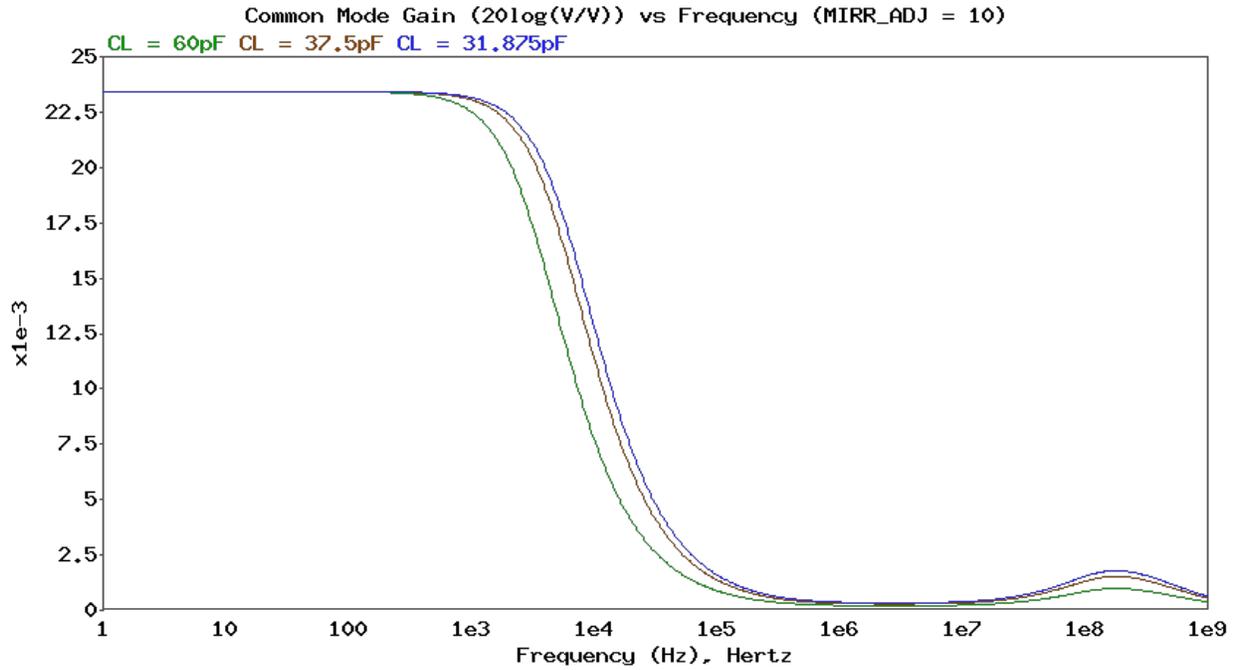
Figure 4.7: Common mode gain (dB) vs frequency (Hz) with MIRR_ADJ = 10
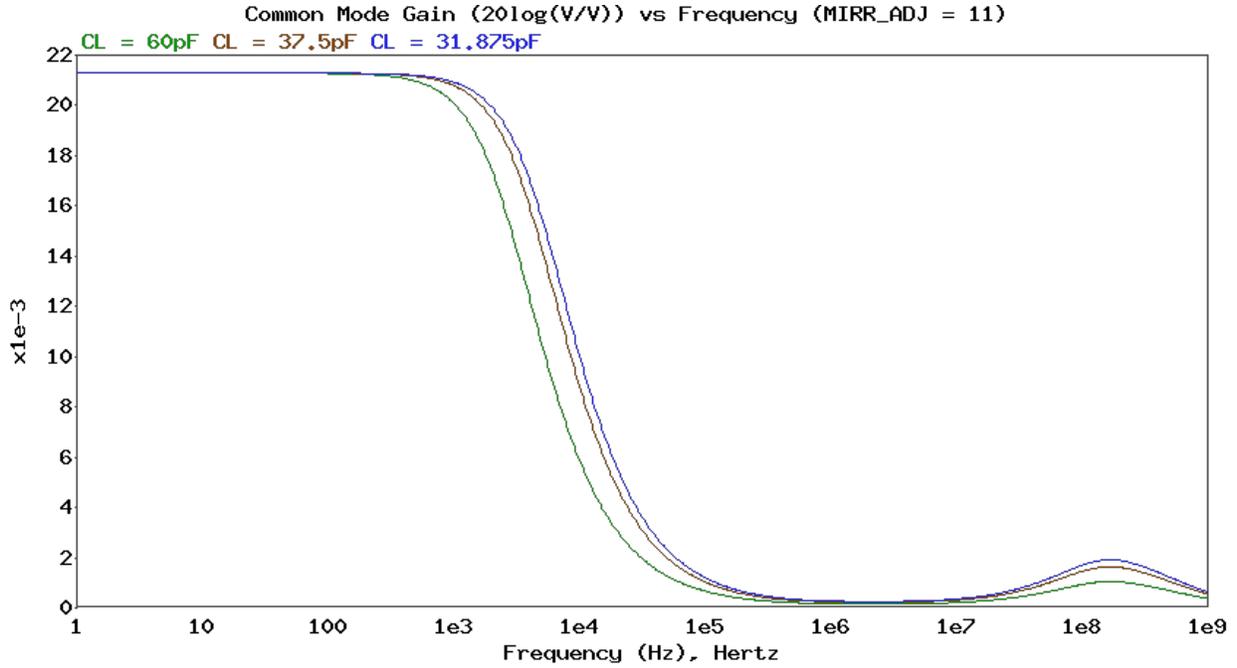
Figure 4.8: Common mode gain (dB) vs frequency (Hz) with `MIRR_ADJ = 11`

4.1.3 PSRR+

PSRR+ is defined as the ratio of open loop differential gain (a_{vd}) to power supply gain (a_{ps+}) of the amplifier:

$$\text{PSRR+} = \frac{a_{vd}}{a_{ps+}} \tag{4.2}$$

Figures 4.9 through 4.12 depict the power supply gain (not PSRR!) of the amplifier for all values of `MIRR_ADJ`. For simulating the power supply gain, a signal $V_{in} = V_{PS} + v_{ps}$ was applied to the VDD rail of the amplifier while the inputs of the amplfier were held at $V_{CM} = 2.5$V. For the applied signal, $V_{PS} = 5$V, and v_{ps} was a small signal AC waveform with AC magnitude of 1. The power supply gain was compared to the open loop differential gains, and the results are summarized in Table 4.4 at the end of this chapter.
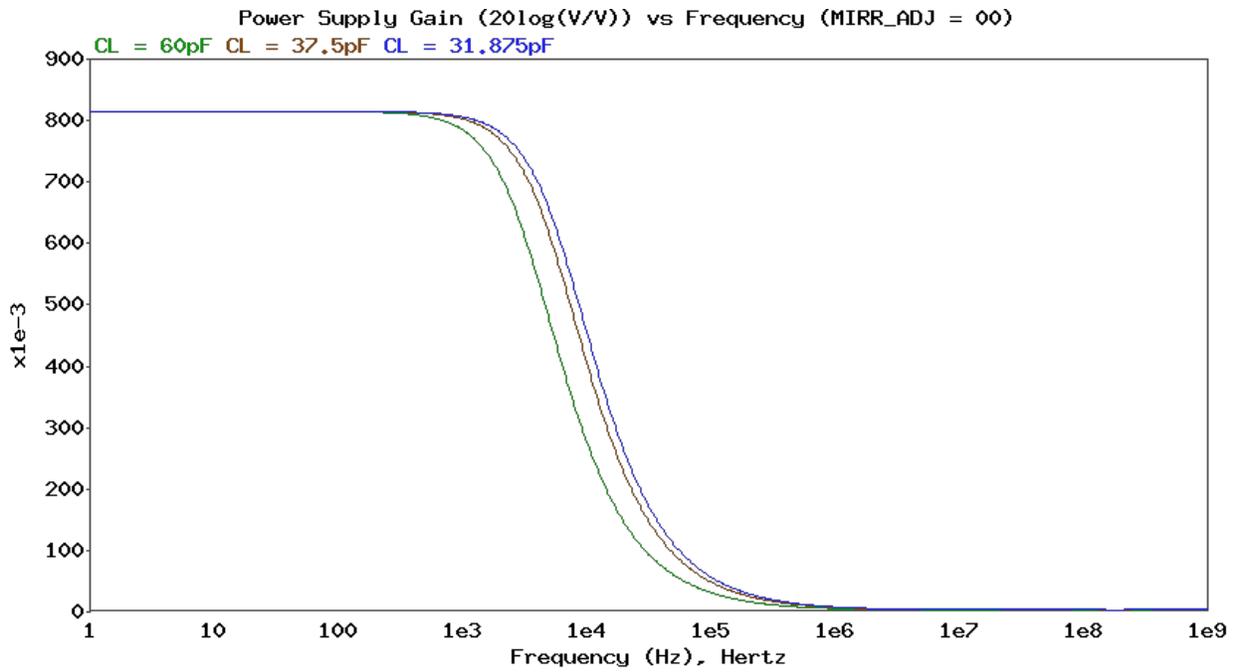
Figure 4.9: Power supply gain (dB) vs frequency (Hz) with MIRR_ADJ = 00
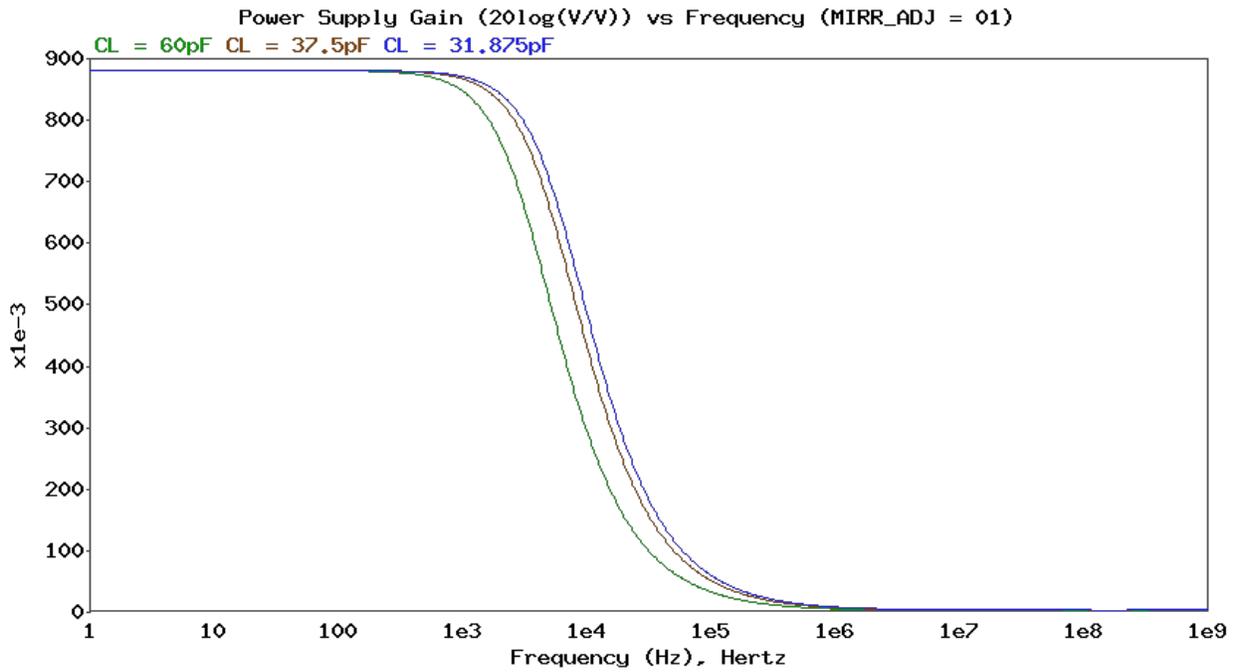
Figure 4.10: Power supply gain (dB) vs frequency (Hz) with MIRR_ADJ = 01
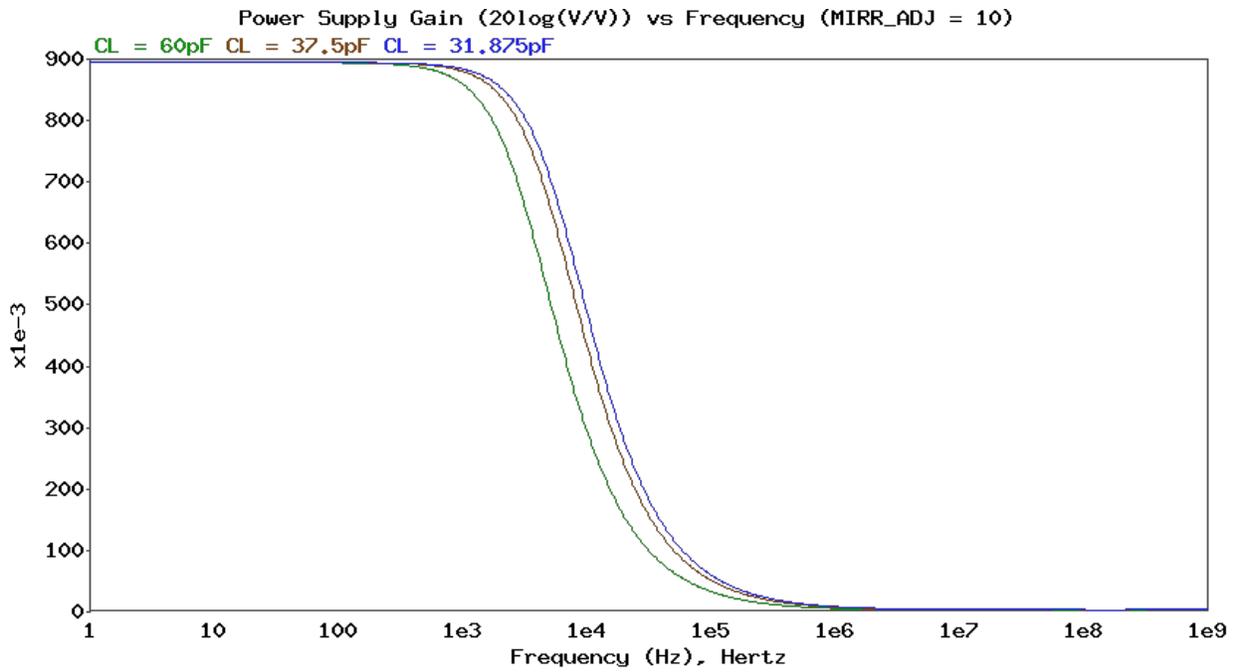
Figure 4.11: Power supply gain (dB) vs frequency (Hz) with MIRR_ADJ = 10
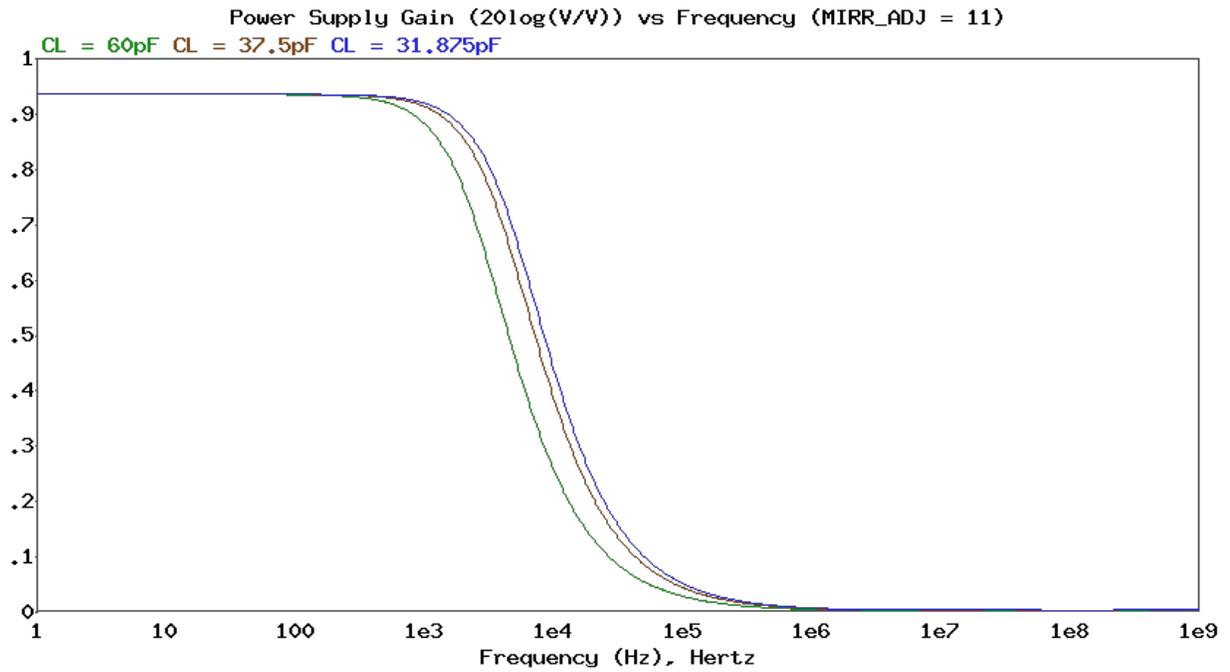
Figure 4.12: Power supply gain (dB) vs frequency (Hz) with MIRR_ADJ = 11

4.1.4 Loop Gain

Loop gain is defined as the total gain around a feedback loop. Loop gain can be calculated by breaking a feedback loop in one location and calculating the gain of the broken loop from beginning to end. For our purposes, loop gain is simulated using a built-in ADICE[26] method that utilizes the Middlebrook method [19]. Figures 4.17 through 4.20 show the loop gain of the amplifier for each closed loop configuration of the CDS scheme: unity gain, gain of 4, and gain of 16. These simulations were performed for every possible value of `MIRR_ADJ`, resulting in the four plots shown below. Numerical results, including loop gain and unity gain bandwidth of each configuration, are summarized in Table 4.5 at the end of this chapter. By observing the numerical unity gain bandwidth values, we indeed see that the settling time of the amplifier is limited by the closed loop gain of 16, as this configuration has unity gain bandwidth 2.0MHz when the feedback path is connected. This implies that in the worst-case, the amplifier will still settle within 1μs, as designed. The results are further corroborated by the fact that the loop gain decreases by approximately 12dB every time the closed loop gain increases by a factor of 4; this is expected. For all simulated results, the input common mode voltage was $V_{CM} = 2.5$V.
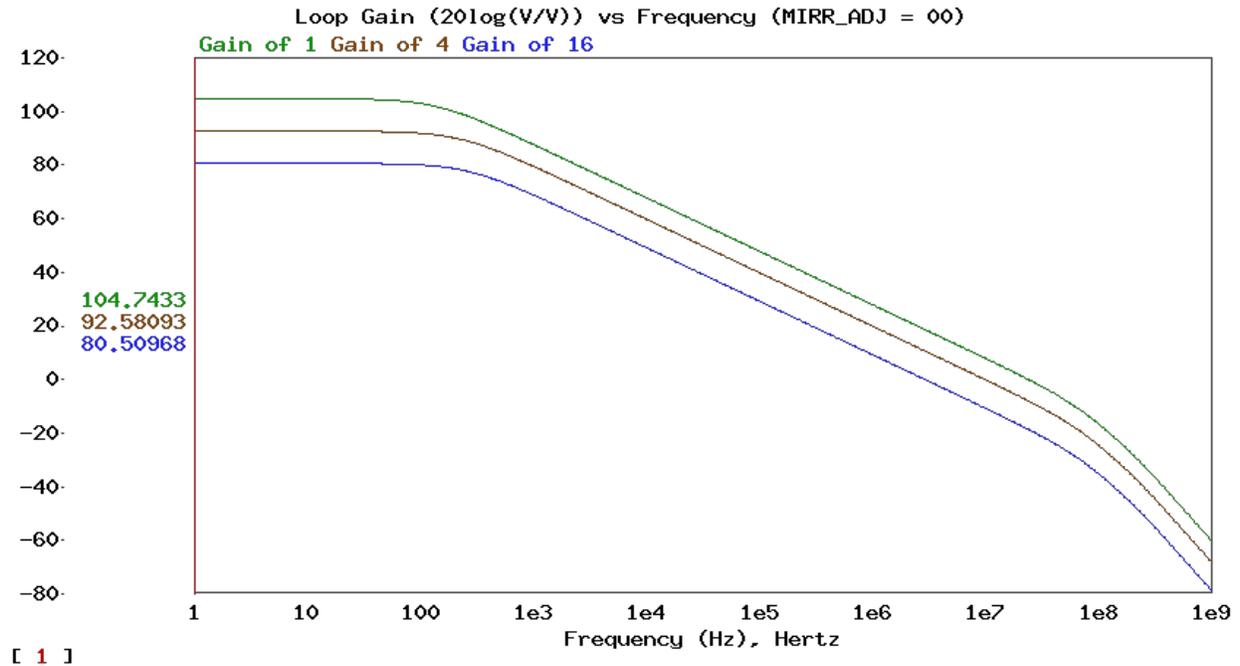
Figure 4.13: Loop gain (dB) vs frequency (Hz) with `MIRR_ADJ = 00`

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[26]ADI's proprietary version of SPICE.
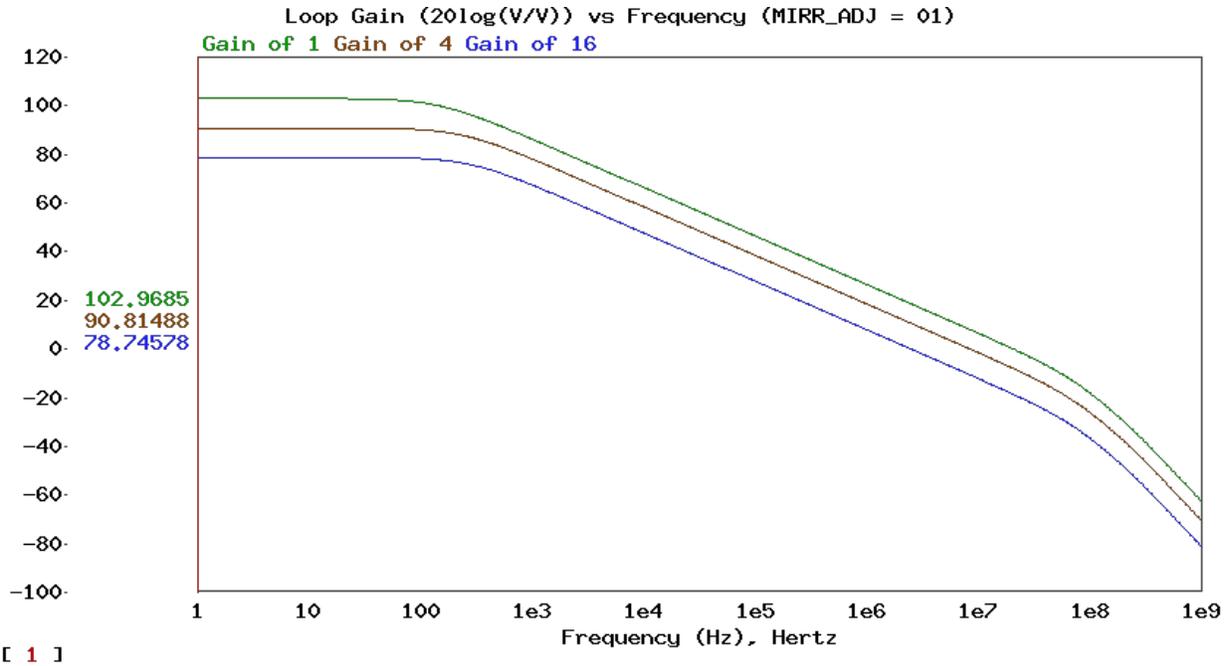
Figure 4.14: Loop gain (dB) vs frequency (Hz) with `MIRR_ADJ = 01`
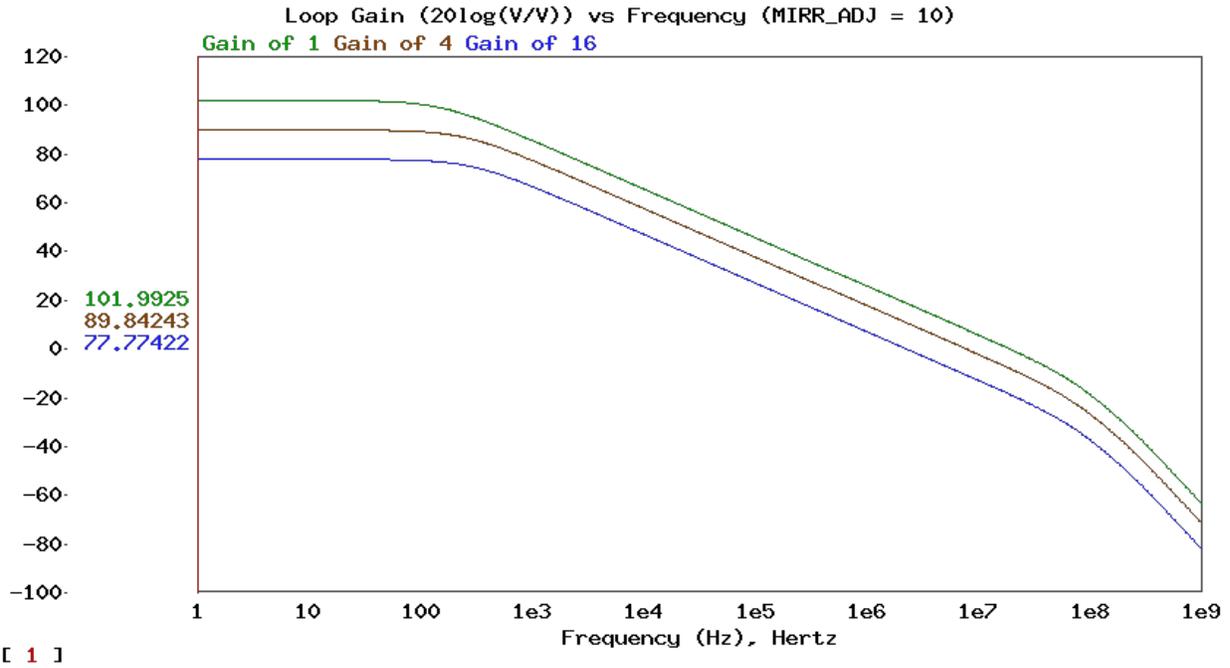
Figure 4.15: Loop gain (dB) vs frequency (Hz) with `MIRR_ADJ = 10`
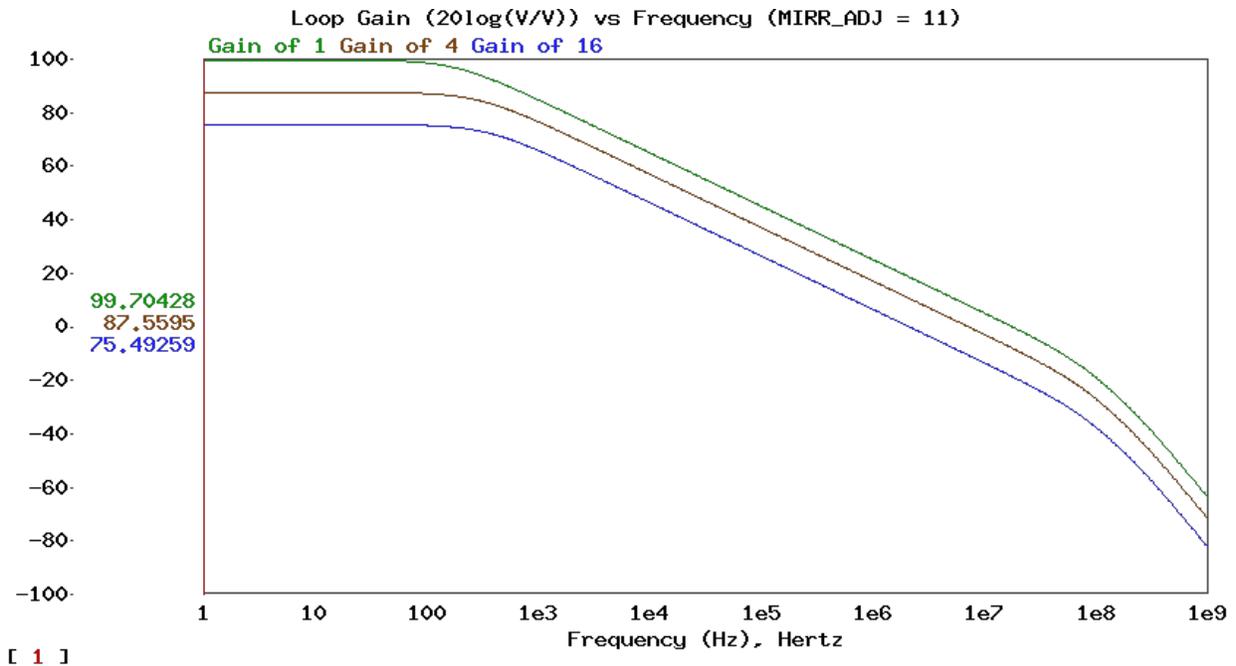
Figure 4.16: Loop gain (dB) vs frequency (Hz) with `MIRR_ADJ = 11`

4.1.5 Power Consumption

A quick sanity check is performed to confirm the power consumption of the amplifier matches the expected value. For this analysis, the bias adjust resistor of the OTA was adjusted until the tail current was approximately 4.8mA. The tail current feedback circuit draws an additional $I_{TAIL}/4$ current. The current consumption of the output legs and cascode biasing legs can be neglected in this analysis, as they consume much less current than the input stage. With 4.8mA attributed to the OTA, and an additional 1.2mA for the replica circuit, the total current consumption is approximately 6mA, corresponding to an active power of roughly 30mA. This agrees well with the simulated 31.5mW power consumption of the OTA when `MIRR_ADJ` = `00`, i.e. $I_{TAIL} \approx 4.8$mA.

4.1.6 Noise

A noise analysis was performed over a frequency range of 1Hz to 1GHz. Output and input referred voltage noises are shown in the plots shown in Figures 4.17 through 4.20 for all gain configurations and `MIRR_ADJ` values. Specific noise values were measured at 100kHz, where thermal noise is the main contributor to total noise power. These numerical results are summarized in Table 4.6 at the end of this chapter. In the figures below, we can observe the $1/f$ nature of the noise spectral density; the noise power is much greater at lower frequencies than higher frequencies. This low-frequency $1/f$ noise will be rejected by the CDS, as described

in §2.2. At 100kHz, it makes intuitive sense that the higher values of MIRR_ADJ have poorer voltage noise performance than the lower MIRR_ADJ values, as thermal noise voltage of a MOSFET increases as its bias current decreases (please see Equation 2.8). Since higher MIRR_ADJ values imply a decrease in the tail current, thermal noise voltage increases.
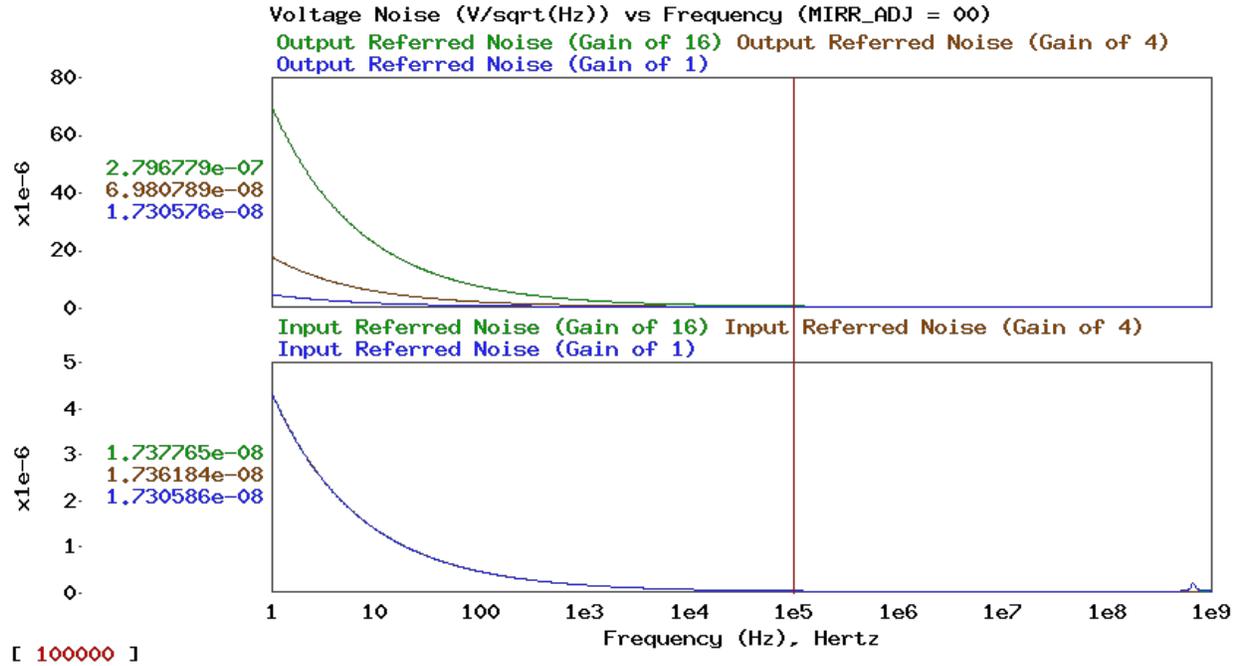
Figure 4.17: Voltage noise $(V/\sqrt{Hz})$ vs frequency (Hz) with MIRR_ADJ = 00
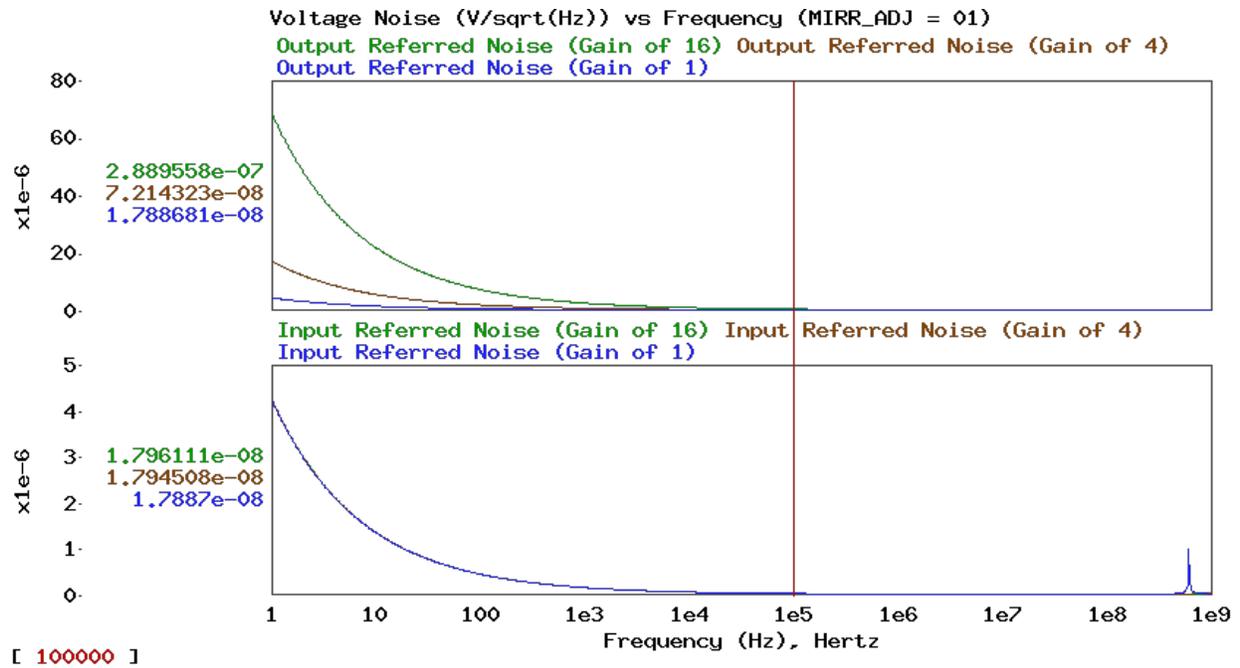
Figure 4.18: Voltage noise $(V/\sqrt{Hz})$ vs frequency (Hz) with `MIRR_ADJ = 01`
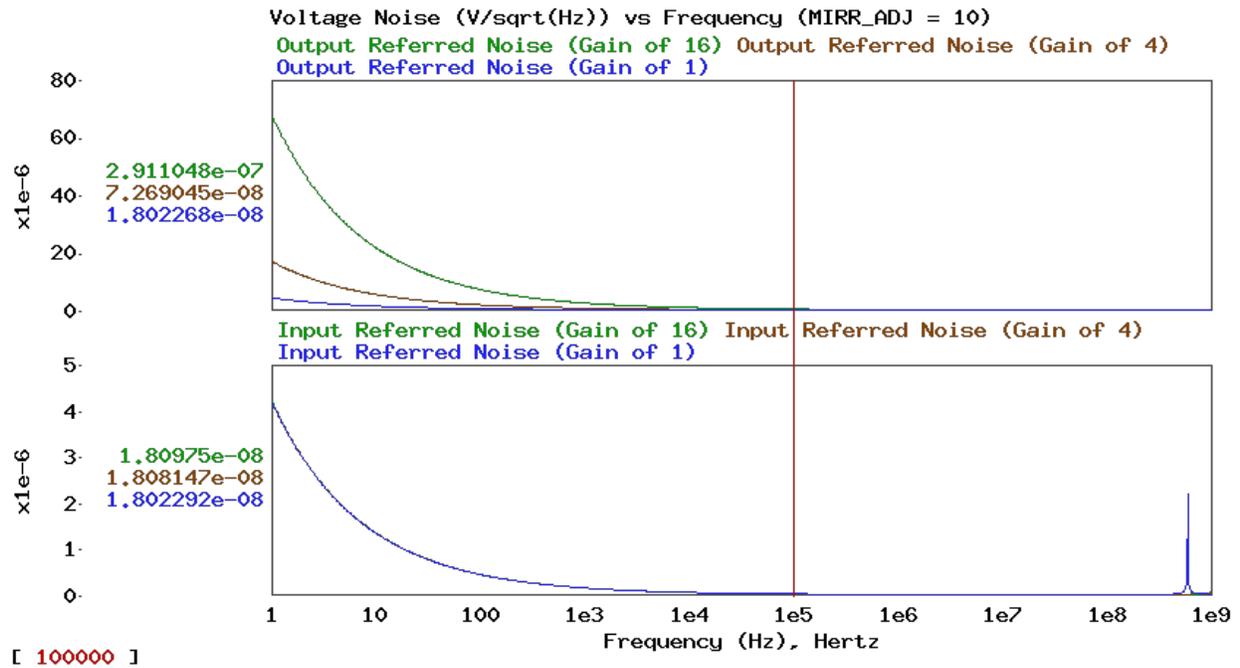
Figure 4.19: Voltage noise $(V/\sqrt{Hz})$ vs frequency (Hz) with `MIRR_ADJ = 10`
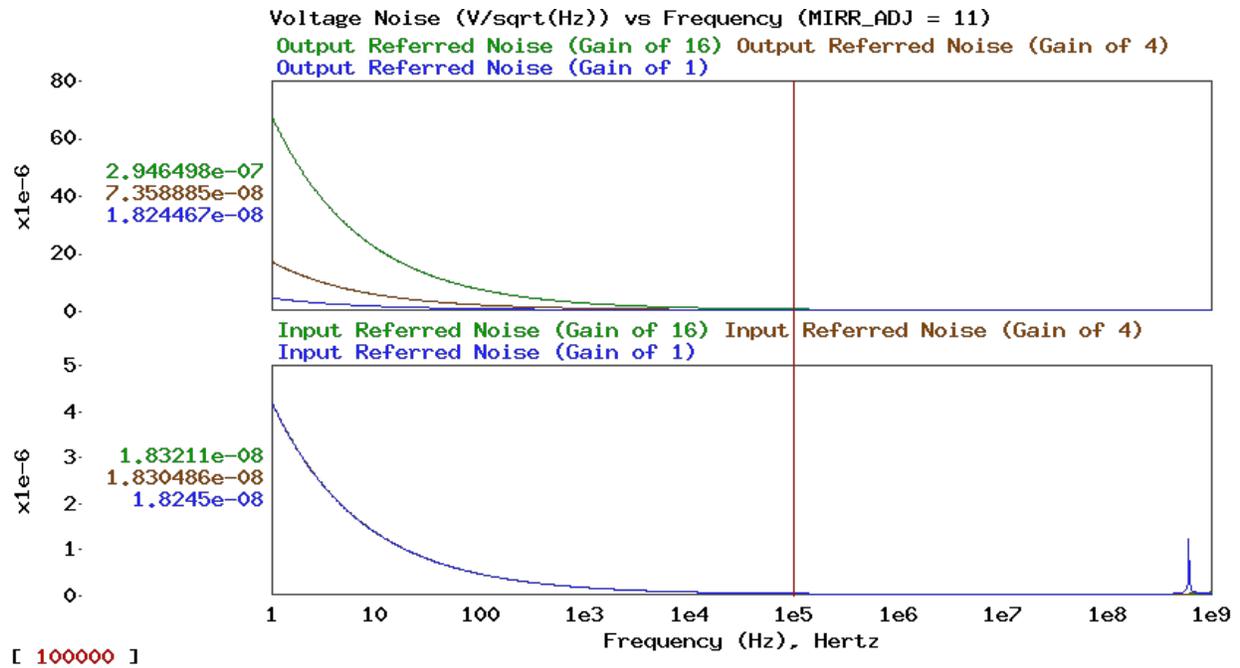
Figure 4.20: Voltage noise $(V/\sqrt{Hz})$ vs frequency (Hz) with `MIRR_ADJ = 11`

4.1.7 Input Swing

The input common mode range of the amplifier is limited by the tail current source. In this section, we roughly define the input swing as the range of common mode input voltages for which the tail current source still conducts non-zero current. We find that for this amplifier, the input common mode range spans from 0V to approximately 4.3V for all values of `MIRR_ADJ`. This is shown in Figure 4.21.
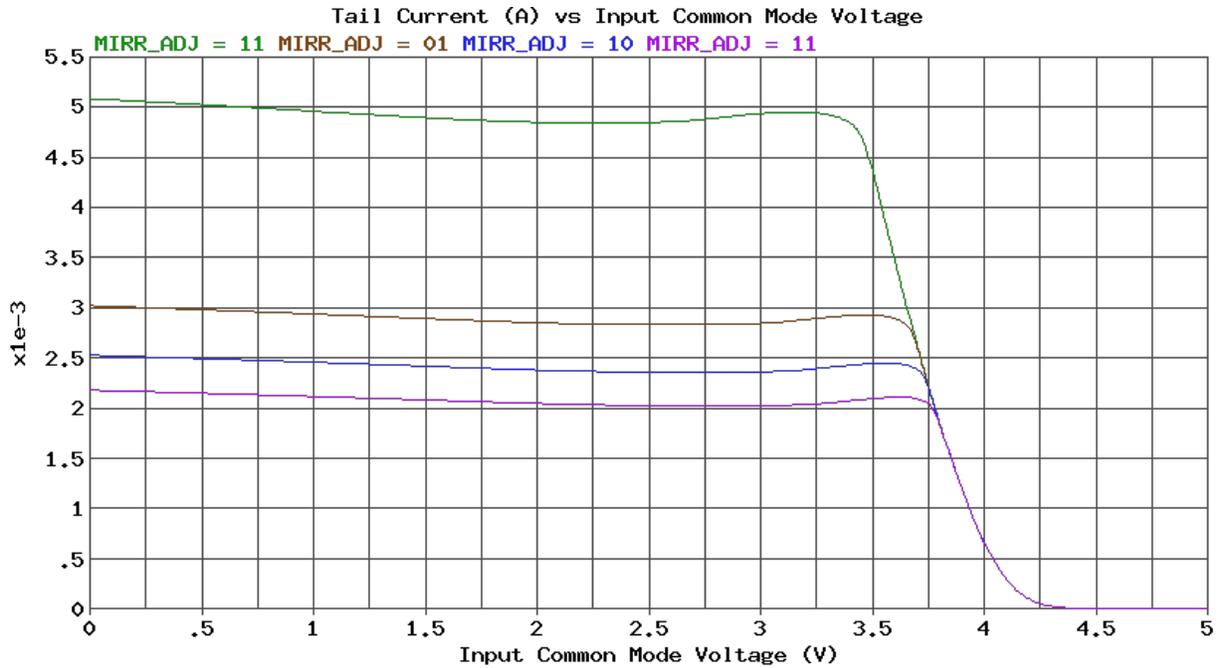
Figure 4.21: Tail current (A) vs input common mode voltage (V) for all values of MIRR_ADJ

4.1.8 Output Swing

The output swing of the amplifier was measured by configuring the amplifier in unity gain and driving it with a $6V_{pp}$, 10kHz input signal with an offset of 2.5V. The results are shown in Figure 4.22. Because of the PMOS input transistors, the amplifier can easily drive the output close to ground. That said, we can observe some distortion as the output nears ground due to the output cascode transistors loosing headroom, ultimately reducing the open loop gain of the OTA. On the high side of the output swing, the waveform shows much more clipping. This is due to the tail current source collapsing as the input rises, which in turn significantly reduces the open loop gain of the amplifier. Reduced high side output swing is an element of the design that was expected, and reasoning for this is provided in §3.1.7.
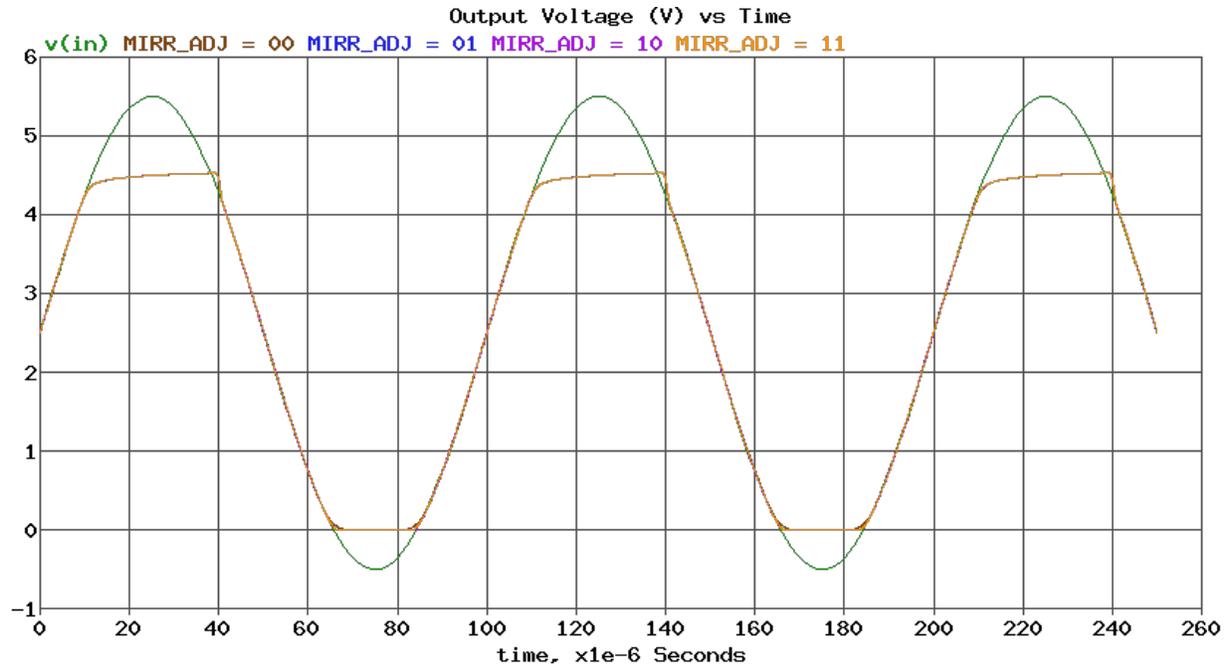
Figure 4.22: Output voltage (V) vs time (ms)

For the purpose of quantifying output swing, we find the boundaries where the output voltage is no longer within 5% of the input voltage. This is a rather loose definition; tolerable output voltages will ultimately come down to the application in hand and the feedback factor (β) used. With this definition, we find that the output can swing within 700mV of V_{DD}, and within 35mV of GND. It is no surprise that the high side output swing has the same 4.3V maximum as the input common mode range we discovered in §4.1.7 above, as the amplifier is configured in unity gain. The high side output swing can be improved by using a smaller feedback factor (i.e. $\beta = 1/4$ or $\beta = 1/16$); however, we are concerned with the worst-case scenario, which is unity gain for our CDS scheme.

4.2   CDS OTA Performance

The simulation results presented in this section pertain to the overall CDS OTA system, such as leakage currents, total active power consumption, transient response, etc. A timing diagram is also proposed for the CDS scheme. These simulations include the effects from not just the OTA, but also from the pre-charge buffers, switches, and ESD structures.

4.2.1 Active Power

The active power consumption of the CDS OTA is dominated by the power consumption of the OTA itself. Since the OTA is the workhorse of the circuit, this is expected. The bias adjust resistor for the OTA sets the bias/tail current of the OTA, and thus has a large impact on the power consumption of the CDS OTA as a whole. DC operating point simulations were performed for each value of `MIRR_ADJ`, and the current draw from each part of the amplifier was measured: OTA current, buffer current, and digital current. OTA current includes the current flowing through the OTA bias adjust resistor and the current through the OTA. Buffer current is the total current flowing through *both* pre-charge buffers and includes the current through the respective bias adjust resistors. Finally, digital current refers to the current draw from the digital electronics, including the inverters, digital buffers, switches, ESD, etc. Table 4.1 summarizes the current draw of the CDS OTA with a 2.5V DC input. While higher values of `MIRR_ADJ` offer lower power consumption, it will take the amplifier longer to settle with these values of `MIRR_ADJ`; thus, total integrated energy may not actually be improved.

MIRR_ADJ	00	01	10	11
OTA current	6.295mA	3.9mA	3.312mA	2.906mA
Buffer current	3.962uA	3.962uA	3.962uA	3.962uA
Digital current	1.833nA	1.82nA	1.82nA	1.806nA
Total current	6.299mA	3.904mA	3.316mA	2.91mA

Table 4.1: Active current draw of CDS OTA at 27°C

4.2.2 Inactive Power

Inactive power consumption is one of the most important aspects of this project. We desire inactive power consumption to be as low as possible, as it is expected that this circuit will be off for the majority of time. As we saw in §1.1, the inactive power consumption is the culprit for the "power-floor" of typical signal chains. ESD structures can contribute significantly to the leakage/inactive power as they are typically realized as large devices. Assuming the use of a large clamping ESD structure, as used on the digital V_{DD} rail (please see §5.2.3), the drain of this clamping MOSFET is connected to the +5V supply rail and forms a reverse-biased diode with the P-substrate. This reverse-biased diode has leakage current that increases with temperature. It is therefore necessary to examine the leakage current over a wide range of temperatures. Figure 4.23 depicts the leakage current attributed to different parts of the circuit over a temperature range of 0°C to 150°C. Please note the numbers to the left of the graph are the simulated leakage currents at the cursor position of 27°C. Total CDS OTA leakage refers to the total leakage current of the integrated circuit. Total OTA leakage comprises of the leakage current through the VDD_OTA pin plus the leakage current

through the OTA bias adjust resistor. Finally, the total buffer leakage current refers to the leakage current through the VDD_BUF pin, which is comprised of the leakage current through both pre-charge buffers and the leakage current through their respective bias adjust resistors. The leakage current of the CDS OTA is maximized when MIRR_ADJ = 00 ($R_{\text{BIAS\_ADJ\_OTA}} = 20k\Omega$). During this simulation, $V_{CM} = 2.5V$ was applied to V_x and V_y of the CDS OTA. The results from this setup are shown in Figure 4.23 below. Table 4.2 summarizes how each part of the circuit contributes to the leakage current for all values of MIRR_ADJ at 27°C. The total leakage current of the CDS OTA at 27°C is of the same order of magnitude as the leakage current of the AD7686, which has standby current of approximately 1nA at 27°C. This is favorable, as the inactive power consumption of the signal chain will be (relatively) evenly distributed among all parts of the analog/mixed signal devices. Please note the the leakage currents presented here include the leakages from the ESD structures, which are discussed in Chapter 5.
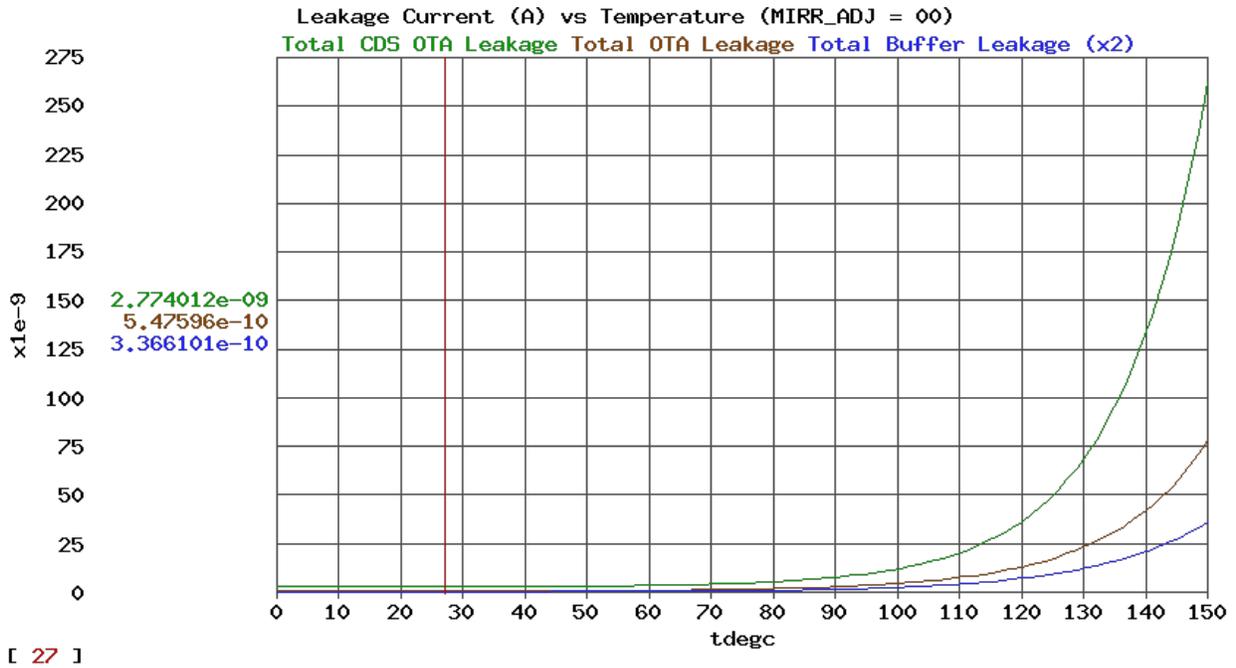
Figure 4.23: Leakage current (A) vs temperature (°C) with MIRR_ADJ = 00

MIRR_ADJ	00	01	10	11
OTA current	0.5476nA	0.5476nA	0.5476nA	0.5476nA
Buffer current	0.3366nA	0.3366nA	0.3366nA	0.3366nA
Digital current	1.89nA	1.875nA	1.875nA	1.861nA
Total current	2.774nA	2.76nA	2.76nA	2.745nA

Table 4.2: Inactive current draw of CDS OTA at 27°C

4.2.3 Transient Simulation

We now bring the pieces together and present a transient simulation of the entire CDS OTA system. We will begin by proposing a timing diagram, like the one shown in 2.2, and follow with the resulting output waveform of the CDS OTA when driven with the proposed timings.

Proposed Timing Diagram

A timing diagram has been proposed in an earlier chapter, however, it omitted specific duty cycles for the waveforms. In this section, we will propose these timings and present reasoning behind the choice of each. Ultimately, the pulse widths of each waveform are dictated by the settling time of the circuit and the acquisition/conversion times of the AD7686. These timings reflect low R_s scenarios. R_s forms a low pass filter with the input capacitance of the OTA ($\sim$200fF); therefore, if R_s is too large, this low pass filter could take significant time to settle and may necessitate longer duty cycles. There are 6 states or events that need to happen in the CDS scheme. In between each state, we allocate 100ns of deadtime which will make it easier to see the effects the switching events have on the operation of the circuit. In practice, the deadtime can be modified to suit the application.

1. **Pre-charge V_x (switch A):** The time allocated to this state is a bit arbitrary. Recalling that the pre-charge buffers have a unity gain bandwidth of approximately 4MHz, and assuming a small voltage step at the input of the pre-charge buffer, the output of the pre-charge buffer will settle to 4% of its final value in 800ns. We allocate 800ns for pre-charging[27].

2. **Settling V_x (switch B):** The amount of time switch B is closed not only depends on the settling time of the OTA, but also on the acquisition time of the ADC. We give switch B a pulse width of $3\mu s$. After the first 100ns switch B is closed, switch E opens, freezing the charge at the negative input of the OTA. After switch E opens, the OTA is given $1\mu s$ to settle[28] until the ADC acquisition and sampling begins. The AD7686 has a worst-case acquisition time of 400ns and worst-case conversion time of $1.6\mu s$ [20][29]. Therefore, after the OTA settles, switch B is kept closed for at least 400ns longer. Once the ADC acquires the settled OTA output, switch B remains closed while the ADC performs its conversion. Depending on the behavior of the amplifier when the ADC appears disconnected, this may be a good time to connect the dummy capacitor to the output of the OTA. Switch B opens 100ns

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[27]800ns makes the timing diagram neat, such that one sampling period is an interger value of μs. There is nothing special about 4%, other than that is good enough for our purposes.

[28]The amplifier has the lowest bandwidth when `MIRR_ADJ = 11` and $1\mu s$ of settling time reflects this performance. If a different value of `MIRR_ADJ` is used, the time allocated for the OTA to settle can be reduced, based on the specifications shown in Table 4.5.

[29]Whenever we refer to ADC acquisition/conversion time, we are referring to these worst-case values.

before the SAR ADC completes its conversion, which allows us to change states as soon as the ADC conversion is complete, while preserving 100ns of deadtime between switching events.

3. **Pre-charge V_y (switch C):** As with the pre-charge of V_x, we allocate 800ns to pre-charge V_y.

4. **Settling V_y (switch D):** As with the settling of V_x, the total time switch D is closed is $3\mu s$. In reality, 100ns can be shaved from this pulse width, since we are not waiting for switch E to open, as we were when V_x was settling; however, $3\mu s$ keeps things symmetric.

5. **Initialize C_i/amplify (switch E):** Switch E closes at the beginning of the CDS cycle to initialize C_i and clear the charge stored on C_f. Switch E remins closed while the OTA input is pre-charged to V_x, but then opens 100ns after switch B closes. Switch E remains open for the rest of the CDS cycle. Thus, given 800ns for precharging V_x, 100ns of deadtime between switch A opening and switch B closing, and an additional time of 100ns for the transients effects of switch B closing to clear, the total pulse width of switch E is $1\mu s$.

6. **ADC sampling:** An ADC sampling event happens twice during the CDS cycle. The first ADC sample (of V_x) happens $2.4\mu s$ after the beginning of the CDS cycle, and the second ADC sample (this time of V_y) occurs $6.4\mu s$ after the beginning of the CDS cycle. Please note that we define an ADC sampling event as after the ADC has acquired the sample, but before conversion has taken place.

We can now determine the time it takes for one sample to be made (T_S), and from that, determine the period of one CDS cycle (T_{CDS}):

$$T_S = T_{\text{ON, switch A}} + T_{\text{deadtime}} + T_{\text{ON, switch B}} + T_{\text{deadtime}} = 4\mu s \tag{4.3}$$

Given the time required to measure one sample, and due to symmetry, we can determine the time needed for each CDS cycle:

$$T_{\text{CDS}} = 2 * T_S = 8\mu s \tag{4.4}$$

In summary, if the power-cycling is periodic with period T_{PC}, where $T_{\text{PC}} \geq T_{\text{CDS}}$, then for $0 \leq t < T_{PC}$, we have:

$$V_{\text{switch A}}(t) = 5u(t) - 5u(t - 0.8\mu s) \tag{4.5}$$

$$V_{\text{switch B}}(t) = 5u(t - 0.9\mu s) - 5u(t - 3.9\mu s) \tag{4.6}$$

$$V_{\text{switch C}}(t) = 5u(t - 4\mu s) - 5u(t - 4.8\mu s) \tag{4.7}$$

$$V_{\text{switch D}}(t) = 5u(t - 4.9\mu s) - 5u(t - 7.9\mu s) \tag{4.8}$$

$$V_{\text{switch E}}(t) = 5u(t) - 5(t - 1\mu s) \tag{4.9}$$

$$V_{\text{ADC}}(t) = \delta(t - 2.4\mu s) + \delta(t - 6.4\mu s) \tag{4.10}$$

where Equations 4.5 through 4.10 are also periodic with period T_{PC}. The annotated control waveforms are shown below in Figure 4.24 for $0 \leq t \leq T_{\text{CDS}}$.
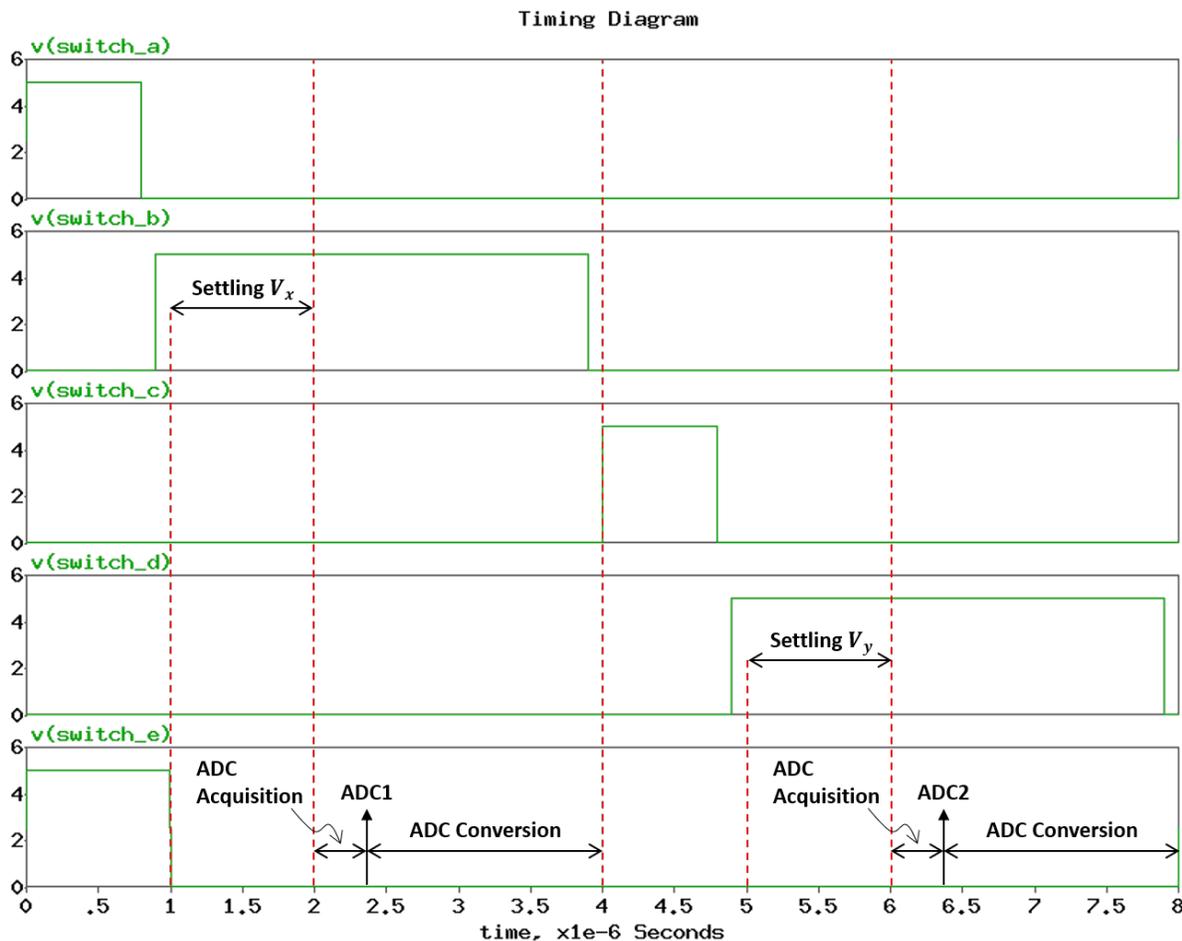
Figure 4.24: Annotated timing diagram

The diagram above provides a visual of relative timings of each event in the CDS cycle. One can see that the acquisition and conversion times of the AD7686 consume the majority of the cycle. To reduce the period of a CDS cycle, it may be advantageous to begin pre-charging V_y as the ADC converts its first sample of V_x. Alternatively, an ADC with faster acquisition and conversion times could be used. That said, the purpose of this project is not to go to extraordinary lengths to optimize the performance of this scheme, but rather to show its promise as a novel concept. Additionally, please note that the control sequence shown above is

94

not exhaustive; signals that control peripheral circuitry (pre-charge shutdown, dummy stability capacitor, etc.) are not shown. The flexibility of this chip provides a lot of options; for example, it may be desirable to shut down each pre-charge buffer after they have perform their duties. The fact that they are OTAs themselves with a resistive bias should allow them to start up quickly when needed. Power-cycling these buffers will allow the consumed energy of the CDS OTA to be further reduced. That said, the main OTA consumes significantly more power than both pre-charge buffers combined, so the impact this will have may be negligible on the total performance of the system. For now, we strive for simplicity over optimization of the fine details.

Output Waveform

The transient response of the amplifier for both closed loop gain settings is shown in Figure 4.25 using the timing diagram presented in Figure 4.24. This output is a result of a small signal differential input signal of 100mV with $V_{CM} = 2.5$V, $R_s = 50\Omega$, and `MIRR_ADJ = 00`. The waveforms shown in Figure 4.25 represent the output of the OTA (OUT pin of the integrated circuit) with a load of 600Ω in series with 30pF. Please note that there is no power-cycling performed; thus, the two CDS cycles shown below occur over a period of 16μs (8μs per CDS cycle). In this example, the pre-charge buffers are employed; however, one can observe how their offsets limit the precision of the pre-charging. The overshoot/undershoot during pre-charging (between 0 and 0.8μs and between 4μs and 4.8μs) is a result of the pre-charge buffer and main OTA behaving as a multistage amplifier with two (dominant) poles. An observant reader may notice that the actual closed loop gain settings of 4 and 16 have some error; this is due to parasitic capacitance at the negative input of the OTA that increases the apparent value of C_i. This can be calibrated out in post-processing. The time at which the ADC begins its conversion is depicted by the impulses on the x-axis.
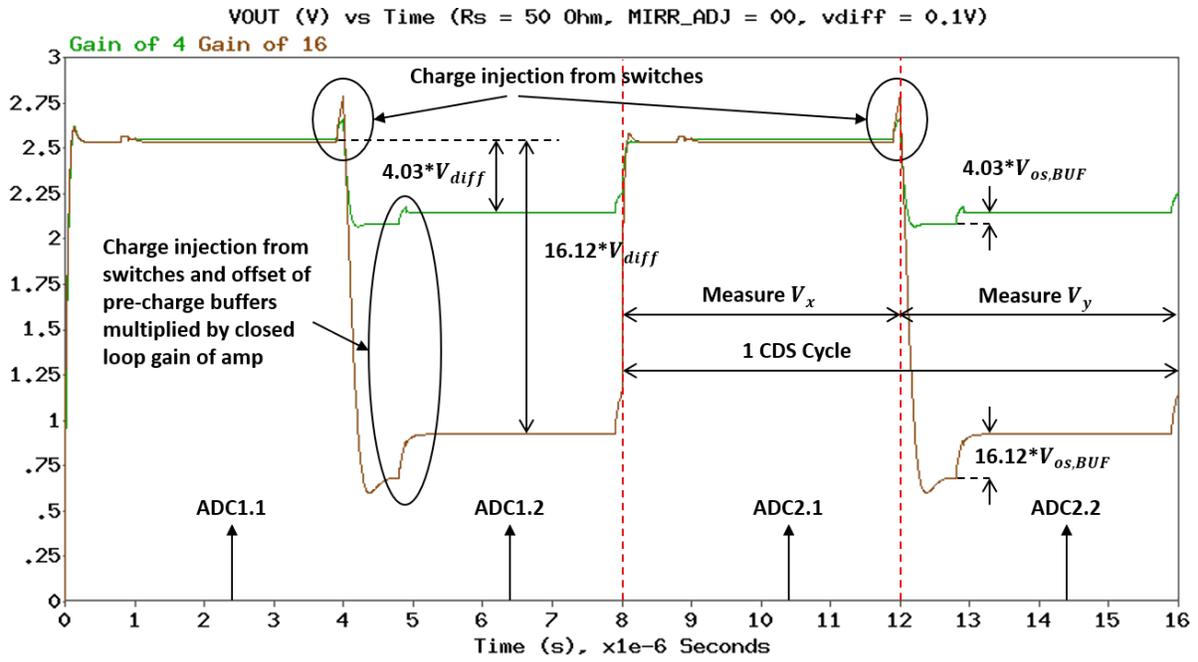
Figure 4.25: Annotated transient response of CDS OTA using timing diagram as shown in Figure 4.25

4.3 CDS OTA Performance Summary

A summary of the simulation results discussed in this chapter are compiled and presented in Table 4.3 below. All of these values were obtained at a temperature of 27°C. In addition, all active/inactive power measurements were measured with a 2.5V input signal (as mentioned in prior sections).

CDS OTA				
Process	180nm			
Die Size[30]	1.63mm^2			
Area[31]	0.14mm^2			
V_{DD}	5V			
Active Power[32]	31.5mW			
Inactive Power[33]	13.9nW			
OTA				
Area[34]	0.035mm^2			
Input Capacitance	$\sim$203.2fF			
Inactive Power[35]	2.7nW			
MIRR_ADJ	00	01	10	11
Active Power	31.5mW	19.5mW	16.6mW	14.5mW
DC Gain	105dB	103dB	102dB	100dB
Open Loop f_u[36]	40MHz	35MHz	33MHz	31MHz
Phase Margin[37]	57°	60°	62°	65°
RTI Noise[38]	$17.4nV/\sqrt{Hz}$	$18.0nV/\sqrt{Hz}$	$18.1nV/\sqrt{Hz}$	$18.3nV/\sqrt{Hz}$
CMRR at 1Hz	128dB	133dB	135dB	133dB
CMRR at 10MHz	74dB	80dB	81dB	81dB
PSRR+ at 1Hz	107dB	104dB	103dB	100dB
PSRR+ at 10MHz	67dB	64dB	63dB	67dB
Single Pre-Charge Buffer[39]				
Area	83μm^2			
Active Power	9.9μW			
Inactive Power	0.84nW			
DC Gain	39dB			
Open Loop f_u[40]	4MHz			
Offset Voltage[41]	16mV			

Table 4.3: Summary of CDS OTA performances

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[30]Die area includes the pads
[31]Corresponds to area of "CDS OTA" block in Figure 5.5
[32]MIRR_ADJ = 00, $R_{\text{BIAS\_ADJ\_OTA}} = 20\text{k}\Omega$
[33]MIRR_ADJ = 00, $R_{\text{BIAS\_ADJ\_OTA}} = 20\text{k}\Omega$
[34]Corresponds to area of "Amplifier" block in Figure 5.6
[35]MIRR_ADJ = 00, $R_{\text{BIAS\_ADJ\_OTA}} = 20\text{k}\Omega$
[36]Simulated with $C_L = 31.875\text{pF}$
[37]At unity gain crossover with $C_L = 31.875\text{pF}$
[38]At 100kHz
[39]Simulated with $R_{\text{BIAS\_ADJ\_X\_BUF}} = 4\text{M}\Omega$
[40]Simulated with $C_L = 200\text{fF}$
[41]Measured with 2.5V DC input signal

4.4 Energy Per Measurement

With the timing diagram determined and the simulation results collected, we can now determine a rough estimate for the energy per measurement we may expect with this amplifier. We recall that this metric is an important figure of merit of this design; therefore, we wish for the energy per measurement of the amplifier to be comparable to (optimally less than) that of the ADC. Please note that for the ADC, energy per measurement is not the same as energy per conversion, though the two are proportional. A measurement refers to all the events that must occur when an analog voltage is measured by the signal chain, i.e., there are multiple ADC conversions per measurement. To re-iterate, in this proposed scheme, there are 3 (or even more) conversions as the ADC is converting both signal and power-cycling reference with respect to its power supply. An ADC architecture designed to use the power-cycling reference directly could avoid one of these conversions.

Up to this point, we have been designing the amplifier with the AD7686 in mind. In evaluation, however, a similar ADC with comparable performance will be used: the AD7699. The AD7699 is an 8-channel ADC that contains an internal multiplexer. This multiplexer will be useful for switching the input of the ADC between the amplifier output, the voltage reference, and the thermometer. An informed reader may be aware that the AD7699 also has a built in band-gap and thermometer; however, these will not be utilized in evaluation as they are not optimized for power-cycling.

The energy per conversion of the AD7699 is approximately 52nJ[42] [21]. At least 3 conversions are needed from the ADC per measurement; two conversions for the amplifier and one conversion for the voltage reference; therefore, the energy per measurement of the ADC7699 is at least 156nJ[43]. As we have seen above, the worst-case active power consumption of the CDS OTA is 31.5mW. For a CDS cycle with a period of $8\mu s$, the total time the CDS OTA needs to be on is $6.4\mu s$ (see Figure 4.24); thus, the (maximum) energy per measure of the CDS OTA will be approximately 202nJ. Please note that this is a worst-case figure! The timing diagram presented in Figure 4.24 is fairly conservative and is designed to still work with `MIRR_ADJ = 11`, where the active power consumption of the CDS OTA drops to 14.5mW (see Table 4.3). When `MIRR_ADJ = 11`, the energy per measurement of the CDS OTA drops to approximately 93nJ. When `MIRR_ADJ = 00`, the bandwidth of the amplifier is larger; thus, the CDS cycle can be shortened, offering some extra energy savings. The worst-case timing diagram presented in Figure 4.24 assumes a settling time of $\sim 1\mu s$ for the

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[42]This may vary depending on what on-chip peripherals are used, e.g. band-gap reference, temperature sensor, etc.

[43]If we add another conversion for the thermometer (using V_{be}), then that is 208nJ per measurement for the AD7699. For a PTAT measurement, two conversions of the thermometer are needed; which attributes 260nJ to the ADC per measurement. See §6.2 for more details.

OTA, which is only the case for `MIRR_ADJ = 11`; all the other `MIRR_ADJ` settings have faster settling times (higher bandwidth), as revealed in Table 4.5, and the timing diagram can be adjusted accordingly. With 93nJ per measurement for the CDS OTA with `MIRR_ADJ = 11`, we see that the amplifier will not be a particularly dominant energy consumer in the signal chain.
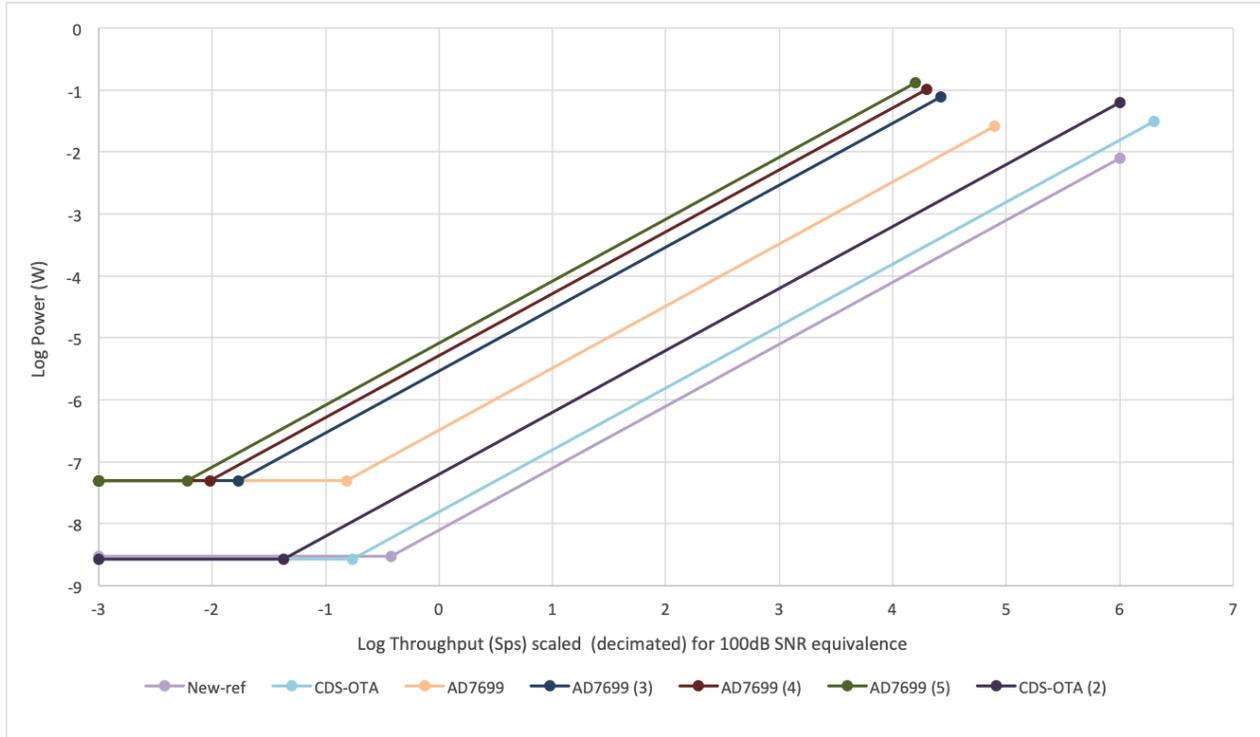
Figure 4.26: Chart of power versus measurement throughput for proposed signal chain components

Figure 4.26 depicts power versus throughput of the different components of the proposed signal chain: the AD7699, the CDS OTA, and the new voltage reference. Please note that for this plot, the inactive power used for the CDS OTA is 2.7nW, which omits the leakage currents from the digital blocks and ESD structures[44]. In the legend, CDS-OTA (2), AD7699 (3), AD7699 (4), AD7699 (5) take into account the multiple conversions/samples that each respective components needs to make per one measurement. For example, AD7699 (3) refers to the corresponding power versus throughput of the AD7699 with 3 conversions per measurement. We see that the components have a formidable window in the precision low-power domain where power scales with the throughput of the system. The graph above assumes 50nA shutdown current for the AD7699, and is the culprit for the rather high "power-floor" the AD7699 exhibits; however, this 50nA figure may be improved if the internal voltage reference and temperature sensor of the AD7699 are not utilized.

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[44]Total inactive power of the chip is 13.9nW. See Table 4.3.

MIRR_ADJ	00			01			10			11		
C_L	**60pF**	**37.5pF**	**31.875pF**	**60pF**	**37.5pF**	**31.875pF**	**60pF**	**37.5pF**	**31.875pF**	**60pF**	**37.5pF**	**31.875pF**
a_{vd} **(1Hz)**	172600	172700	172700	140700	140700	140700	125800	125800	125800	96650	96650	96650
a_{vd} **(10MHz)**	2.378	3.78	4.434	2.028	3.224	3.782	1.877	2.985	3.502	1.737	2.763	3.242
a_{cm} **(1Hz)**	0.07081	0.07081	0.07081	0.03095	0.03095	0.03095	0.02343	0.02343	0.02343	0.02129	0.02129	0.02129
a_{cm} **(10MHz)**	0.00045	0.00072	0.00084	0.00021	0.00033	0.00039	0.00017	0.00027	0.00032	0.00016	0.00025	0.00030
CMRR (1Hz)	128dB	128dB	128dB	133dB	133dB	133dB	135dB	135dB	135dB	133dB	133dB	133dB
CMRR (10MHz)	74dB	74dB	74dB	80dB	80dB	80dB	81dB	81dB	81dB	81dB	81dB	81dB
a_{ps+} **(1Hz)**	0.8147	0.8147	0.8147	0.8808	0.8808	0.8808	0.8945	0.8945	0.8945	0.9356	0.9356	0.9356
a_{ps+} **(10MHz)**	0.0011	0.0018	0.0021	0.0013	0.0021	0.0025	0.0013	0.0020	0.0024	0.00080	0.0013	0.0015
PSRR+ (1Hz)	107dB	107dB	107dB	104dB	104dB	104dB	103dB	103dB	103dB	100dB	100dB	100dB
PSRR+ (10MHz)	67dB	67dB	67dB	64dB	64dB	64dB	63dB	63dB	63dB	67dB	67dB	67dB

Table 4.4: Simulation results for open loop gain, CMRR, and PSRR+

MIRR_ADJ	00			01			10			11		
Closed loop gain	**1**	**4**	**16**	**1**	**4**	**16**	**1**	**4**	**16**	**1**	**4**	**16**
Loop gain	105dB	93dB	81dB	103dB	91dB	79dB	102dB	90dB	78dB	100dB	88dB	76dB
Unity gain bandwidth	23MHz	9.5MHz	2.8MHz	20MHz	8.1MHz	2.4MHz	18MHz	7.5MHz	2.2MHz	17MHz	6.9MHz	2.0MHz

Table 4.5: Simulation results for loop gain

MIRR_ADJ		00			01			10			11		
Closed loop gain		**1**	**4**	**16**	**1**	**4**	**16**	**1**	**4**	**16**	**1**	**4**	**16**
Input referred voltage noise at 100kHz $(nV/\sqrt{Hz})$		17.3	17.4	17.4	17.9	17.9	18.0	18.0	18.1	18.1	18.2	18.3	18.3
Output referred voltage noise at 100kHz $(nV/\sqrt{Hz})$		17.3	69.8	279.7	17.9	72.1	288.9	18.0	72.7	291.1	18.2	73.6	294.6

Table 4.6: Simulation results from noise analysis

Chapter 5

Physical Realization

A design for the amplifier has been presented and simulation results have been shown. In this chapter, we discuss the physical implementation of the circuit in silicon and discuss real-life design practices that are sometimes pushed aside during theoretical discussion. We begin by proposing a padring and then discuss electrostatic discharge (ESD) protection. Finally, we present an overview of the floor plan of the integrated circuit and discuss performance trade-offs related to the layout. I want to thank Paul Fenders and Kam Mistry for their help on the layout of this chip - due to their expertise, the chip was completed early enough to be taped out.

5.1   Padring

A padring is exactly what the name implies: a collection of bond pads that encompass the integrated circuit. The bond pads are used to connect the integrated circuit with its package, so wires/traces connected to the package pins ultimately have a low impedance path to the silicon die. Since it is not desirable that bond wires cross, in most cases, the padring ultimately determines the pin-out of the package. For this chip, digital pins were grouped together, and, similarly, analog pins were placed adjacent to each other. The proposed test chip has a total of 22 pins; therefore, rounding up to the nearest standard package size, the test chip is packaged in a 24 pin package with two pins not connected. The padring/pin-out is shown in Figure 5.5.

This particular test chip is pad-limited, or in other words, the area the padring circumscribes is larger than that of the actual circuitry. In a product, a pad-limited chip is undesirable and avoided because silicon goes unused and money is wasted; however, in a test chip, this can be quite common as production numbers are small, and it is advantageous to have access to as many signals (pins) as possible. More pins correspond to

a larger padring perimeter and, therefore, larger enclosed area. The area of this integrated circuit is 1275μm x 1275μm. Table 5.1 below provides a description of each pin's function and groups the pins into categories somewhat representative of how they are grouped in the padring.

Pad	Function	Description
SW_A	Digital input	Controls the state of switch A. If this pin is high, switch A is closed, if this pin is low, switch A is open.
SW_B	Digital input	Controls the state of switch B. If this pin is high, switch B is closed, if this pin is low, switch B is open.
SW_C	Digital input	Controls the state of switch C. If this pin is high, switch C is closed, if this pin is low, switch C is open.
SW_D	Digital input	Controls the state of switch D. If this pin is high, switch D is closed, if this pin is low, switch D is open.
SW_E	Digital input	Controls the state of switch E. If this pin is high, switch E is closed, if this pin is low, switch E is open.
C_STBL	Digital input	Connects an optional load capacitance to the output of the OTA to be used when the SAR ADC appears disconnected. If this pin is high, an additional $30\text{pF} + 554\Omega$ is attached to the output of the OTA.
GAIN_SEL	Digital input	Selects the closed loop gain configuration of the amplifier. If this pin is high, the amplifier operates in a gain of 4 configuration, and if low, the amplifier operates in a gain of 16 configuration.
MIRR_ADJ_MSB	Digital input	This pin sets the MSB of the current stealing mirror adjustment scheme described in §3.6.7.
MIRR_ADJ_LSB	Digital input	This pin sets the LSB of the current stealing mirror adjustment scheme described in §3.6.7.
$\overline{\text{OTA\_SHDN}}$	Digital input	Sets the shutdown state of the OTA. If this pin is high, the OTA is on, if it is low, the OTA is in shutdown mode.
$\overline{\text{A\_BUF\_SHDN}}$	Digital input	Sets the shutdown state of the A buffer. If this pin is high, the buffer is on, if it is low, the buffer is in shutdown mode. The A buffer is the pre-charge buffer connected to switch A.
$\overline{\text{C\_BUFF\_SHDN}}$	Digital input	Sets the shutdown state of the C buffer. If this pin is high, the buffer is on, if it is low, the buffer is in shutdown mode. The C buffer is the pre-charge buffer connected to switch C.
BIAS_ADJ_OTA	Analog input	Provides the current reference for the OTA and ultimately sets the tail current of the main amplifier.
BIAS_ADJ_A_BUF	Analog input	Provides the current reference for the A buffer and ultimately sets the tail current of this pre-charge buffer.
BIAS_ADJ_C_BUF	Analog input	Provides the current reference for the C buffer and ultimately sets the tail current of this pre-charge buffer.
V_X	Analog input	Input voltage corresponding to V_x in Figure 2.1.
V_Y	Analog input	Input voltage corresponding to V_y in Figure 2.1.
OUT	Analog output	Output of the amplifier, which gets connected to the ADC.
VDD	Power	This pin powers all digital blocks and ESD cells.
VDD_OTA	Power	This pin powers the OTA.
VDD_BUF	Power	This pin powers both pre-charge buffers.
GND	Power	This pin is universal ground (also connected to the substrate).

Table 5.1: Pin functions and descriptions

5.2 ESD Protection

ESD protection may not be considered so important in an academic environment, but is fully recognized as a critical attribute of a commercial product. ESD protection ensures the integrated circuit is sheltered from harsh operating environments; a layer of armor. Having the protection will not only save time during debugging; it will likely prove necessary to deliver a robust product. As the name implies, ESD cells are specifically designed to protect the IC from electrostatic discharge, which has the potential to damage the thin oxide and metal layers in the chip. The gate oxide of the MOSFETs used in this design can also be damaged by a high voltage event; therefore, it is important that any large potential difference between two nodes is quickly and safely discharged.

The ESD cells used in this CDS OTA are standard to the `l50_mixsig_1p5m_1p8bv_5v` process. In general, the pins of the CDS OTA were grouped into three categories: analog/digital input pins, analog output pin, and power. Each category received their own type of ESD cell best suited to the problem in hand.

5.2.1 Analog/Digital Input Pins

Analog/digital input pins were given a typical ESD cell as shown in Figure 5.1.
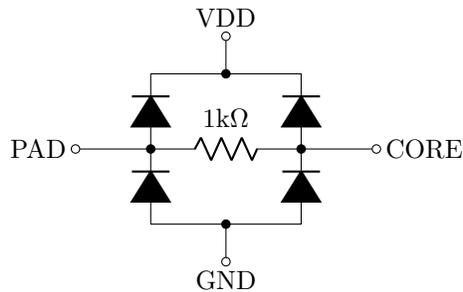
Figure 5.1: Analog/digital input ESD cell

The four diodes in Figure 5.1 above act as clamping diodes to prevent the pin in question from going above VDD or below GND. 1kΩ series resistance limits the in-rush current in the case of an ESD event. For the digital inputs, this series resistance is rather arbitrary, as the digital pins typically interface with the gate of a device, which is already high impedance. However, for the analog input pins, 1kΩ series resistance was chosen, as it is approximately on the order of the on-resistance of the front end switches (switches A - D). Larger series resistance offers better protection at the cost of degraded noise performance. Using the same ESD cell for both digital and analog input pins keeps things simple.

5.2.2 Analog Output Pin

Figure 5.2 shows the ESD cell used for the analog output pin.
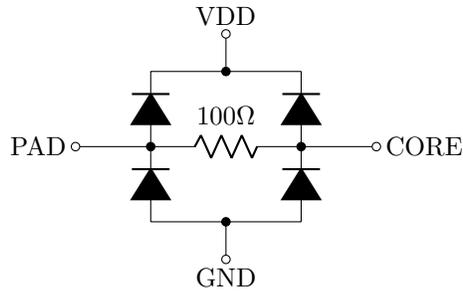
Figure 5.2: Analog output ESD cell

One can see that this ESD cell is very similar to the ESD cell presented in the section above; however the series resistance is lower. In the event of slew, the output of the amplifier can conduct significant current, on the order of mA's; thus, we wish to minimize the series resistance associated with the ESD cell to avoid a voltage drop across the cell, which would limit how fast the load capacitance can settle. Clamping diodes are still used to protect the output in the presence of an over voltage event.

5.2.3 Power

For the power pins, it is undesirable to have series resistance, as this will cause the power supply voltage to droop when current is drawn from the supply. Therefore, ESD structures with zero series resistance were used for the power supply pins. The GND pad is directly connected to GND on the core of the IC, leaving three other power pins in need of protection: VDD, VDD_OTA, and VDD_BUF. As mentioned in Table 5.1, VDD is responsible for supplying power to all the digital blocks and other ESD cells in the circuit. A large clamping MOSFET is used to provide a low resistance path from VDD to GND in the case of an ESD event on the VDD bus. While very effective, the large ESD clamp used for the VDD pin has high leakage; it is still our goal to keep the inactive power consumption of the amplifier as low as possible, and ESD cells with large leakage currents will hinder this objective. We accept our losses for the digital supply, VDD; however, since it is the analog electronics we are trying to prove, low leakage ESD structures are implemented on the analog supply pins, VDD_OTA and VDD_BUF, resulting in slightly less robust protection. Figures 5.3 and 5.4 show the protection used for these power supplies.
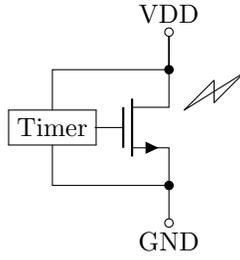
Figure 5.3: Digital power supply ESD cell
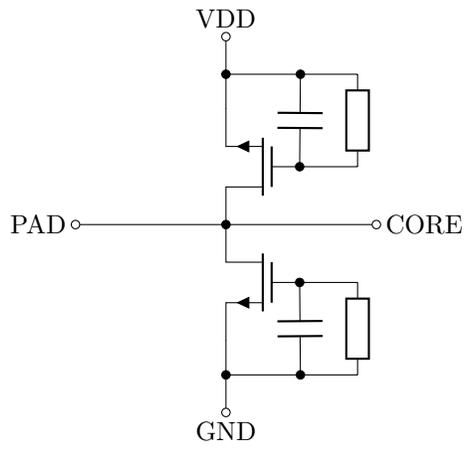
Figure 5.4: Analog power supply ESD cell

5.3 Layout

5.3.1 Complete Integrated Circuit
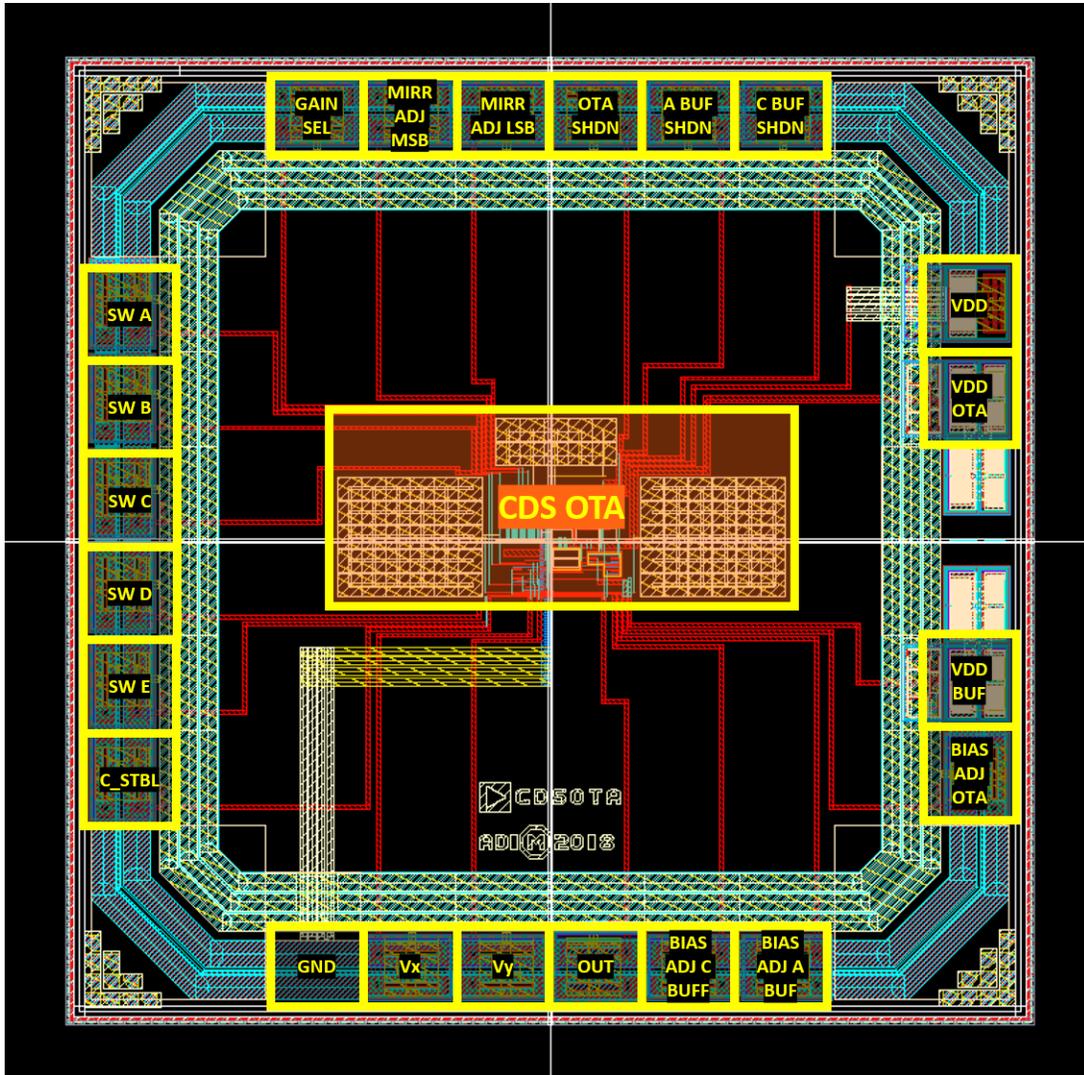
Figure 5.5: Layout of complete integrated circuit

The layout of the entire circuit is shown in Figure 5.5 above. The padring encompasses the circuitry and the CDS OTA sits at the core of the chip. It is now easy to understand why the padring has "ring" in its name. One can also see how the integrated circuit is pad limited, as there is a lot of empty space of unused silicon. Metal traces connect nodes in the CDS OTA to their respective pads. Please note that metal fill, used to improve the planarity of the wafer and die as they are manufactured, is not shown. Metal fill surrounds the CDS OTA block, but does not overlap with it.

5.3.2 CDS OTA
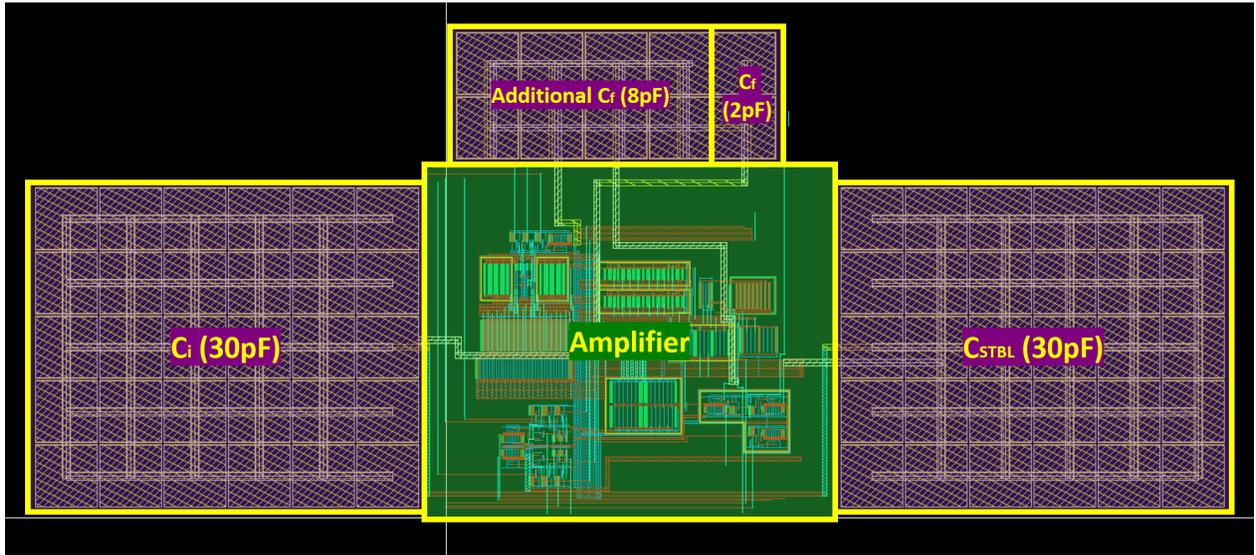
Figure 5.6: Layout of CDS OTA

We now zoom in to the orange CDS OTA block shown in Figure 5.5 to get a closer look at the CDS OTA layout, as shown in Figure 5.6 above. It is interesting to note the relative scale of the physical circuitry; the capacitors consume more than twice the area as the amplifier itself! The capacitors are created using unit size capacitors, each having capacitance of approximately 1pF. To the left of the amplifier is C_i, which is always 30pF, regardless of the closed loop gain setting. Above the amplifier resides the feedback capacitor, C_f, which sets the closed loop gain and can be either 2pF, or 10pF, depending on the state of the GAIN_SEL pin. Finally, C_{STBL} sits to the right of the amplifier and can be connected to the output of the OTA to improve stability. The capacitors used in this layout are Metal-Insulator-Metal (MIM) capacitors; the two plates that form the capacitor occupy two different metal layers with a thin oxide layer between them. Since the lower plate of the MIM capacitor is closer to the grounded substrate of the integrated circuit, it presents significantly more parasitic capacitance to ground than the plate of the capacitor on the higher metal layer. For this reason (and as described in §3.6.8), the bottom plate (lower metal layer) of C_f is connected to the output of the OTA and the top layer is connected to the inverting input of the OTA (or gain select switch). When the opportunity arises, as with C_i and C_{STBL}, the bottom plate of the MIM capacitor is directly connected to ground to eliminate this parasitic capacitance. The majority of the circuitry resides in the green amplifier block and is discussed in the following section.

5.3.3 Amplifier
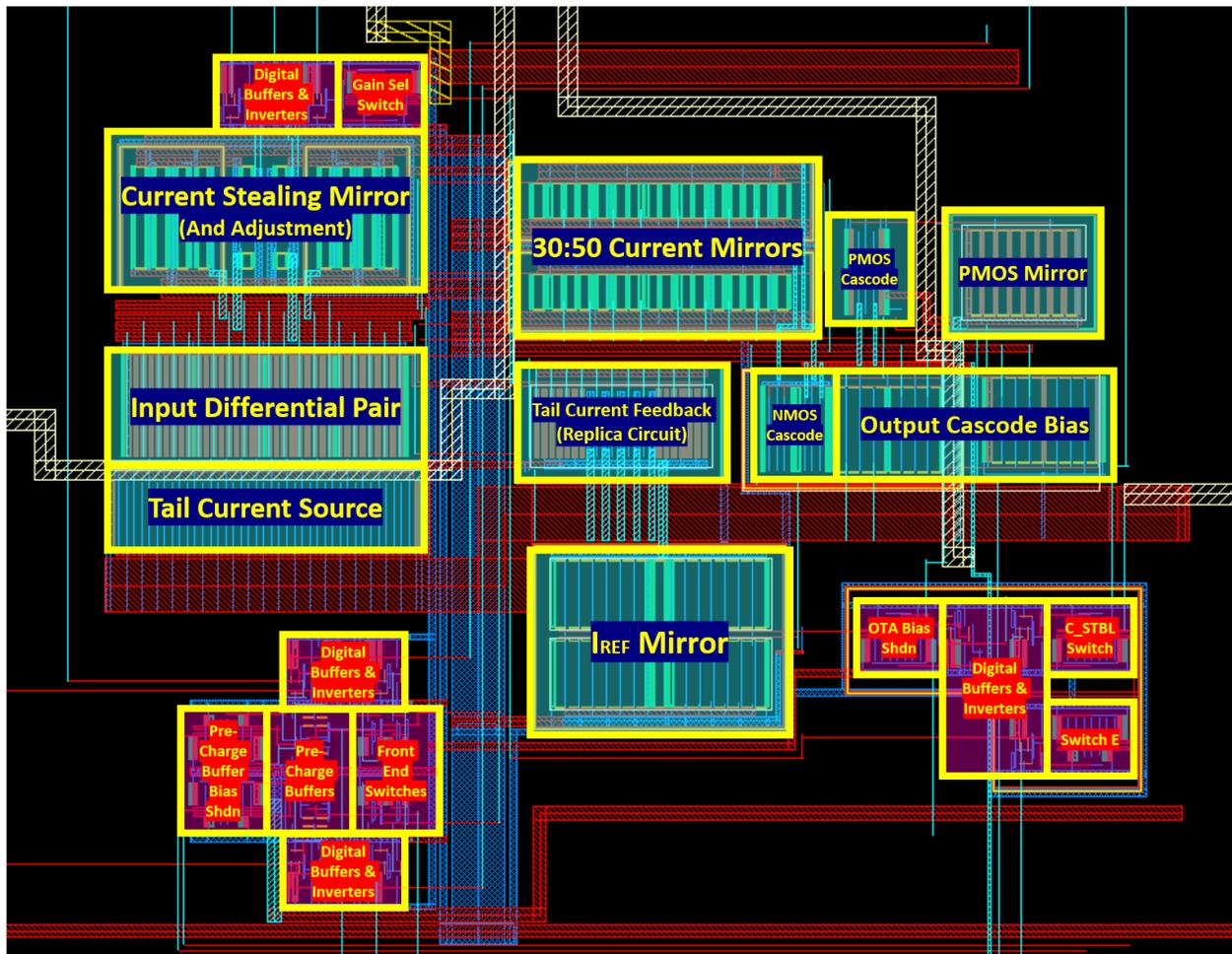
Figure 5.7: Layout of Amplifier

We now take a look at the layout of the amplifier itself, as shown in Figure 5.7 above. The blue blocks in Figure 5.7 contain the circuitry pertaining to the OTA, and the pink/red blocks denote the digital and pre-charge circuitry. The pull-up and pull-down transistors mentioned in §3.6.8, responsible for shutting down the amplifier, are not highlighted, as they are too small at this scale, but are dispersed throughout the circuit accordingly. To improve matching, minimize offsets, and increase mirror accuracy, the input differential pair transistors and mirror devices are interdigitated. This mitigates mismatches that arise from process variations that manifest spatially as linear gradients. Take, for example, the input differential pair transistors (for reference, one may also refer to MP1-4 in Figure 3.10). Figure 5.8 shows these input transistors divided into smaller devices to allow for interleaving. The widths of MPxA/B are half that of MPx shown in Figure 3.10, i.e. $W = 60\mu$m for these interdigitated devices.
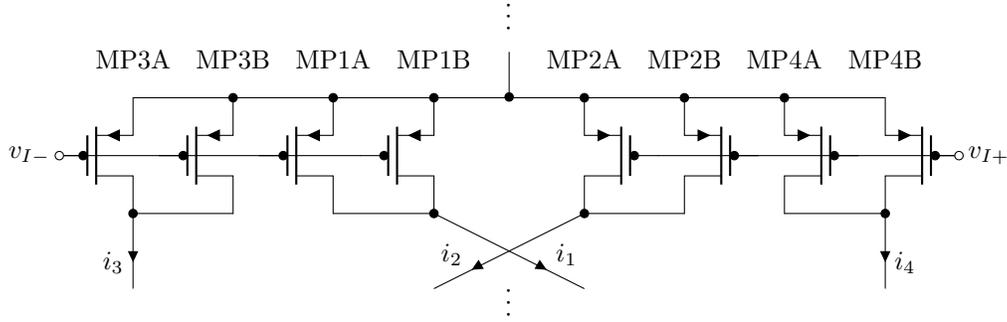
Figure 5.8: Divided input transistors for improved matching

We want the interleaving pattern to cancel first order process variations. In other words, if we assume a linear gradient in doping concentration from MP3A to MP4B in Figure 5.8 above, physically interleaving the transistors in the pattern: MP1A - MP2A - MP3A - MP4A - MP4B - MP3B - MP2B - MP1B will ensure that the non-inverting and inverting paths through the amplifier *and* the current stealing mirrors have equal weight. That is, for some small signal input, the suggested[45] layout pattern will ensure that $i_1 = i_2 = i_3 = i_4$, regardless of a gradient in the process as described. In a similar fashion, the devices in the current stealing mirrors (shown in Figure 3.19), the 50:30 mirrors (MN5-8 in Figure 3.10), and the PMOS mirror (MP5-6 in Figure 3.10) are all interdigitated to improve mirror accuracy. For the current stealing mirrors, the $W = 30\mu$m transistors were broken up into two $W = 15\mu$m devices; for the 50:30 current mirrors, the devices were divided into $W = 5\mu$m transistors, and for the PMOS mirror, the $W = 50\mu$m transistors were split into $W = 25\mu$m devices.

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[45]There are other layout patterns that will work.

Chapter 6

Evaluation Approach

This chapter details the evaluation setup for testing this power-cycling amplifier in the entire signal chain proposed in §1.3. I would like to thank Sean Kowalik for the design of most of the evaluation setup, PCB layout, and assembly logistics. Some minor practical changes are made for evaluation, such as the use of an ADC with a built in multiplexer - the AD7699. The design approach of the voltage reference and the thermometer are also discussed.

6.1   Modification of Traditional Voltage References

We now dedicate some time to explain why voltage references can be difficult to power-cycle and how the voltage reference in the proposed signal chain circumvents these difficulties. When discussing the voltage reference, we are referring to the "Voltage Reference" block in Figure 1.3, not the V_{DD} reference directly connected to the SAR ADC.

Voltage references are designed to produce a very constant output voltage regardless of their operating environment. Temperature coefficients of 1.5 to 20 ppm/°C are typical for voltage references in ADI's portfolio. Classic voltage references use the silicon band-gap to create such stable references by adding a V_{be} (CTAT) to a scaled V_{th} (PTAT), resulting in a zero temperature coefficient output voltage. These references typically impress this combination of voltages across a resistor. Resistors inherently possess thermal noise; thus, it is typical to filter the output voltage using a low pass filter, lowering the bandwidth of the circuit, and thus reducing the contribution of white noise associated with the resistor. This has detriments to power-cycling, most notably because of the filtering. Since a low pass filter is typically used, it can take classical band-gap voltage references significant time to settle.
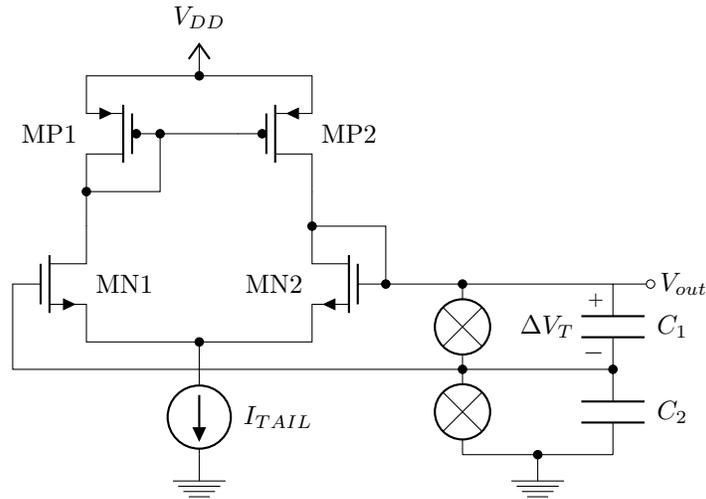
Figure 6.1: Voltage reference designed for power-cycling

The proposed voltage reference, recently successfully tested at ADI, uses a ΔV_T as the reference, as shown in Figure 6.1 above. The ΔV_T arises from making MN1 and MN2 have different threshold voltages through different implants. The ΔV_T is impressed upon a capacitive voltage divider, which presents less noise than a resistor. While not as accurate as a band-gap reference, the ΔV_T circuit eliminates the need for low pass filtering, and therefore the circuit can start up and settle quickly. As always, there are some trade-offs. First, the capacitive voltage divider must be initialized properly to clear stray charge. This increases complexity of the timing and sequencing block. Second, a ΔV_T reference is not as stable over temperature as a band-gap reference. To remedy this, a thermometer is also included in the signal chain for the calibration and correction of the voltage reference. This thermometer is depicted in Figure 1.3 as the "Temperature" block. Because the thermometer is just refining the value of the ΔV_T reference, the thermometer need not be exact: a simple PTAT, or even a single V_{be} may be good enough.

6.2   Thermometer

As mentioned in the section above, a simple thermometer can be used to calibrate the voltage reference. Figure 6.2 depicts the PTAT reference used for this project.
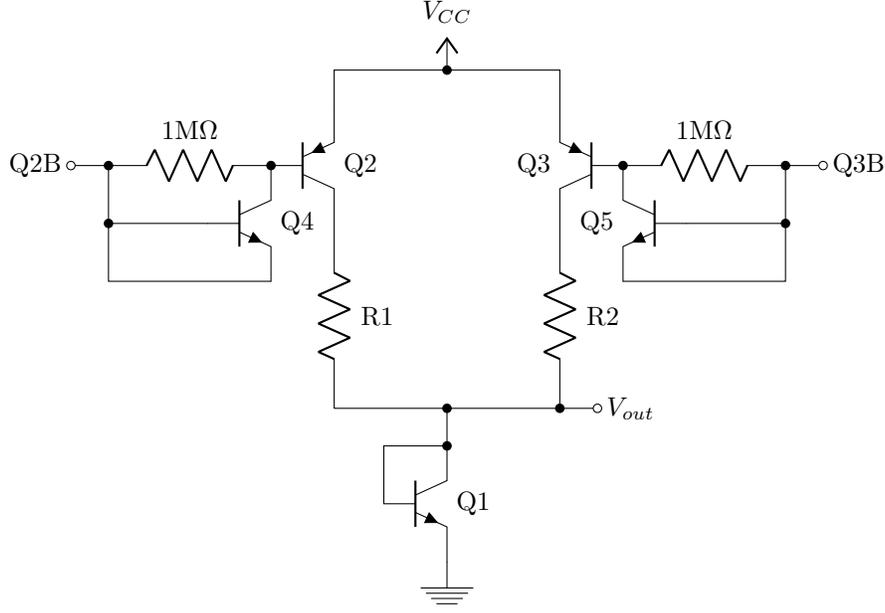
Figure 6.2: CDS PTAT reference

For this evaluation setup, the thermometer is constructed from discrete devices, unlike the voltage reference and the amplifier. This leads to different constraints (devices and device modeling) than one has in the monolithic environment. This reference makes use of the CDS scheme to produce a PTAT measurement after post-processing. PNP transistors Q2 and Q3 are used to either entirely shutdown the reference (Q2B and Q3B both high), or to allow current to flow through Q1, producing $V_{out} = V_{be,Q1}$. To obtain a PTAT measurement, two samples are taken; first, a sample, $V_{out,ADC1}$, is taken with Q2B low and Q3B high. We have:

$$V_{out,ADC1} = V_{be,Q1} \approx V_{th} \ln \left(\frac{I_{C1}}{I_S} \right) \tag{6.1}$$

where I_{C1} is the collector current of Q1, set by R1, I_S is the saturation current of the transistor, and $V_{th} = \frac{kT}{q}$. Next, a sample, $V_{out,ADC2}$, is taken with Q2B high and Q3B low:

$$V_{out,ADC2} = V_{be,Q1} \approx V_{th} \ln \left(\frac{I_{C2}}{I_S} \right) \tag{6.2}$$

where I_{C2} represents the collector current of Q1; however, this time set by R2. If, in post-processing, the result of Equation 6.2 is subtracted from Equation 6.1, we have:

$$V_{PTAT} = V_{th} \ln \left(\frac{I_{C1}}{I_{C2}} \right) \tag{6.3}$$

For this project, R1 = 100kΩ and R2 = 1MΩ; thus, we can approximately say $I_{C1} \approx 10 I_{C2}$. With this

consideration, and after post-processing, our PTAT voltage can be expressed as:

$$V_{PTAT} = \ln(10)V_{th} = \frac{\ln(10)kT}{q} \tag{6.4}$$

The 1MΩ base resistors on Q2 and Q3 ensure that the base currents of the transistors do not contribute much energy consumption to the overall circuit. MOS transistors were not used for the switches due to limited options and poor device models. High value base resistor might slow down the turn-off; thus, diodes (realized as NPN transistors, Q4 and Q5) are added in parallel with the resistor to improve the turn-off time. The thermometer is made from discrete components and is not integrated at this time. NPN transistors are 2N3904 transistors, and PNP transistors are 2N3906 transistors. This thermometer is appealing due to its flexible design; if needed, the CTAT property of a V_{be} may be used as the thermometer, necessitating only one sample, rather than requiring two samples, as for a PTAT measurement.

6.3   Complete Evaluation Setup

The AD7699, the amplifier, and the voltage and thermometer described above were complied into one conglomerate system on a single PCB. A field programmable gate array (FPGA) is used to create the timing diagrams presented earlier in this thesis to control the operation of each section of the signal chain. If this proof-of-concept is successful, a dedicated logic circuit may be created to assume the job of the FPGA in a physical product. A schematic for the evaluation setup is provided at the end of this thesis.

Chapter 7

Conclusion

7.1   Discussion and Summary of Contributions

The scope of this thesis project was to design an amplifier to fit into a larger signal chain scheme currently being pursued by ADI. Based on current state-of-the-art components in ADI's portfolio, this amplifier fills a void that no other existing part could fill. The minimized capacitance of the circuit and the novel switched capacitor scheme provides a solution tailored to power-cycled applications and the low throughput domain. With 2.7nW[46] of inactive power, a unity gain frequency of 2MHz, and an active power of 31.5mW (maximum), this amplifier is able to quickly respond to an input signal and effectively turn-off after a measurement has been acquired. When off/in standby, the amplifier has lower inactive power than the nominal leakage current of a standard coin cell battery.

In the Introduction, this thesis provided context for this project and defined the problem being addressed. Specifics of the novel signal chain were described in Chapter 2, and later, a design for an amplifier was presented. After review of the circuit, simulation results were shown, and a sample control waveform was introduced. Using this data, the key metrics of the amplifier were compared to those of the ADC and voltage reference, and the results demonstrated that the amplifier shows promise when used together with these components. Finally, physical realization was discussed, and an evaluation approach for testing the amplifier and the complete signal chain was presented.

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[46]This is the inactive power attributed to just the CDS OTA and does not include power dissipated by the ESD cells.

7.2 Future Work

There is still work to be done on two levels: the level of the amplifier, and the level of the signal chain as a whole. We will first discuss the remaining work to be done for the amplifier, and then move to the larger picture.

While simulation results are promising, real lab results are much more indisputable. Thorough evaluation will need to be performed to ensure the amplifier behaves as expected and to fully characterize the performance of the circuit. That said, the progress made on this amplifier over the course of the year was quite impressive - this was possible due to the tremendous amount of help received from ADI engineers, MIT faculty, and other administrative assistants.

On a larger scale, there is still work to be done before this concept can be marketed as a solution for a customer. First, it will be advantageous to create a monolithic thermometer. Due to the tight timeline of this thesis, a monolithic thermometer was not pursued, but rather one was made of discrete components. Once the operation of each part of the signal chain is confirmed and evaluated, a larger, holistic package may be assembled to offer the complete signal chain as an easy, "plug-and-play" solution.

7.3 Final Thoughts

There will always be a drive for more efficient electronic components, especially today, when IoT devices are becoming widespread and commonplace. The Fourth Industrial Revolution describes the current trend we see around us, with large technological advancements being made in communication, connectivity, automation, and cyber-physical systems. While certainly just a small piece of the puzzle, this thesis project fits seamlessly into this revolution. More than ever, people are connecting sensors, appliances, tools, cars, lights, and other pieces of hardware to the internet, where they can be remotely controlled and monitored. With some of these devices battery powered, using the minimum amount of energy is essential to their longevity. The amplifier designed in this thesis, working together with the proposed signal chain, will allow for efficient electronics, filling in the void and providing a solution for the precision low-power domain.

Appendix

Appendix A

AC - Alternating Current

ADC - Analog to Digital Converter

ADI - Analog Devices Incorporated

AFE - Analog Front End

BJT - Bipolar Junction Transistor

CDS - Correlated Double Sampling

CM - Common Mode

CMOS - Complementary MOSFET

CMRR - Common Mode Rejection Ratio

CTAT - Complementary to Absolute Temperature

DAC - Digital to Analog Converter

DC - Direct Current

ESD - Electrostatic Discharge

FPGA - Field Programmable Gate Array

GND - Ground

IC - Integrated Circuit

IoT - Internet of Things

KCL - Kirchhoff's Current Law

KVL - Kirchhoff's Voltage Law

LSB - Least-Significant-Bit

MIM - Metal-Insulator-Metal

MIT - Massachusetts Institute of Technology

MOSFET - Metal-Oxide-Semiconductor Field-Effect Transistor

MSB - Most-Significant-Bit

NCM - Nested Current Mirror

NMOS - N-Channel MOSFET

NPN - N-type, P-type, N-type BJT

OTA - Operational Transconductance Amplifier

PCB - Printed Circuit Board

PMOS - P-Channel MOSFET

PNP - P-type, N-type, P-type BJT

PSRR - Power Supply Rejection Ratio

PTAT - Proportional to Absolute Temperature

RTI - Referred to Input

SAR - Successive Approximation Register

SPS - Samples Per Second

Appendix B

a_{cm} - Small Signal Amplifier Common Mode Voltage Gain

a_{ps+} - Small Signal Amplifier Power Supply (+) Voltage Gain

$A_v = A$ - Amplifier Open Loop Voltage Gain

a_{vd} - Small Signal Amplifier Differential Voltage Gain

C_L - Load Capacitance

C_{ox} - Oxide Capacitance Per Unit Area

f_c - Flicker Noise Corner Frequency

f_s - Switching Frequency

f_T - Transit Frequency

f_u - Unity Gain Frequency (Hz)

f_z - Frequency Corresponding to a Zero in the Transfer Function (Hz)

G_m - Amplifier Transconductance

g_m - Device Transconductance

g_{mb} - Device Backgate Transconductance

I_C - BJT Collector Current

I_D - MOSFET Drain Current

I_S - BJT Saturation Current

k - Boltzmann Constant

L - MOSFET Length

Q - Charge of Capacitor

q - Electronic Charge

R_o - Amplifier Output Resistance

r_o - Device Output Resistance

R_{ON} - On-Resistance

T - Temperature (Kelvin)

T_S - Sampling Period

$V_A = 1/\lambda$ - Early Voltage

V_{be} - BJT Base-to-Emitter Voltage

V_{CM} - Common Mode Voltage

V_{DD} - Supply Voltage

V_{DS} - MOSFET Drain-to-Source Voltage

V_{GS} - MOSFET Gate-to-Source Voltage

V_n - Voltage Noise

V_{os} - Offset Voltage

V_{REF} - Reference Voltage

V_T - MOSFET Threshold Voltage

$V_{th} = \frac{kT}{q}$ - Thermal Voltage

W - MOSFET Width

β - Feedback Factor

μ - Mobility

ω_u Unity Gain Frequency (rad/sec)

ω_z Frequency Corresponding to a Zero in the Transfer Function (rad/sec)

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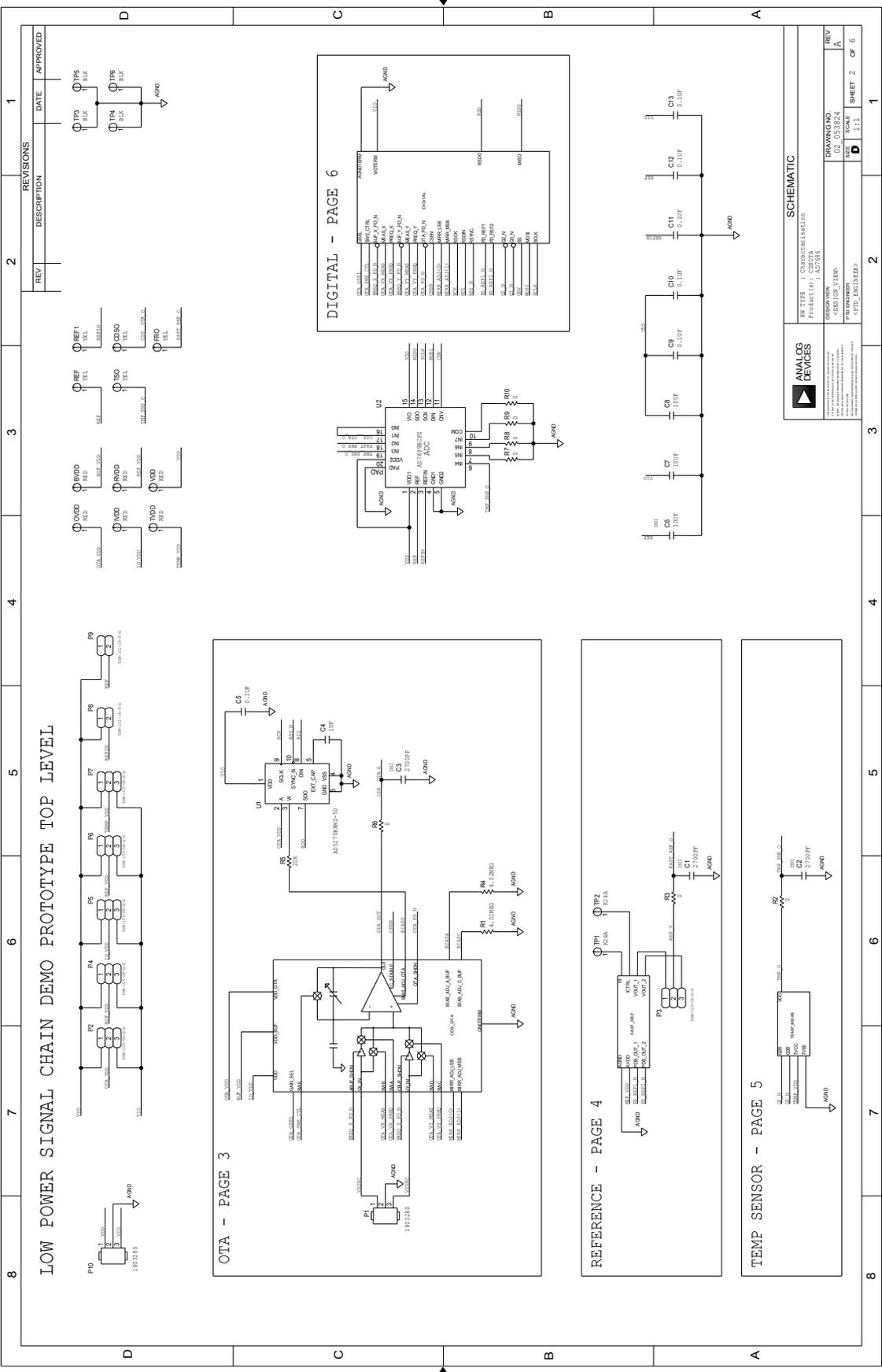
LOW POWER SIGNAL CHAIN DEMO PROTOTYPE TOP LEVEL

OTA – PAGE 3

REFERENCE – PAGE 4

TEMP SENSOR – PAGE 5

DIGITAL – PAGE 6

SCHEMATIC

ANALOG
DEVICES

HW TYPE : Characterization
Product(s) : CDSOTA
              AD7686

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SIZE D
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REV A
SHEET 2 OF 6

AGND

SCHEMATIC

DRAWING NO.
02_053824

REV
A

SIZE
D

SCALE
1:1

SHEET 3 OF 6

HW TYPE : Characterization
Product(s) : CD07A
AD786

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ANALOG DEVICES

U3
LBS_CD807A

FAST REFERENCE

SCHEMATIC

ANALOG DEVICES

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

DRAWING NO.
02_053824

SIZE D
SCALE 1:1
SHEET 4 OF 6
REV A

U4

NC	1	14	ICTRL
AGND	2	13	B
AVDD	3	12	PDB_OUT_2
NC	4	11	PDB_OUT_1
VOUT_2	5	10	
VOUT_1	6	9	NC
NC	7	8	NC

CTRL
B
PDB_OUT_2
PDB_OUT_1

FASTREF

TP9 TP10 TP11
TP12 TP13 TP14

C17
0.1UF

NOTE:
TEST POINTS ADDED TO NC PINS FOR FUTURE DEBUG.
PLACE TP IN PHYSICAL PROXIMITY TO FAST REFERENCE
-BKONKLER 11-JAN-19
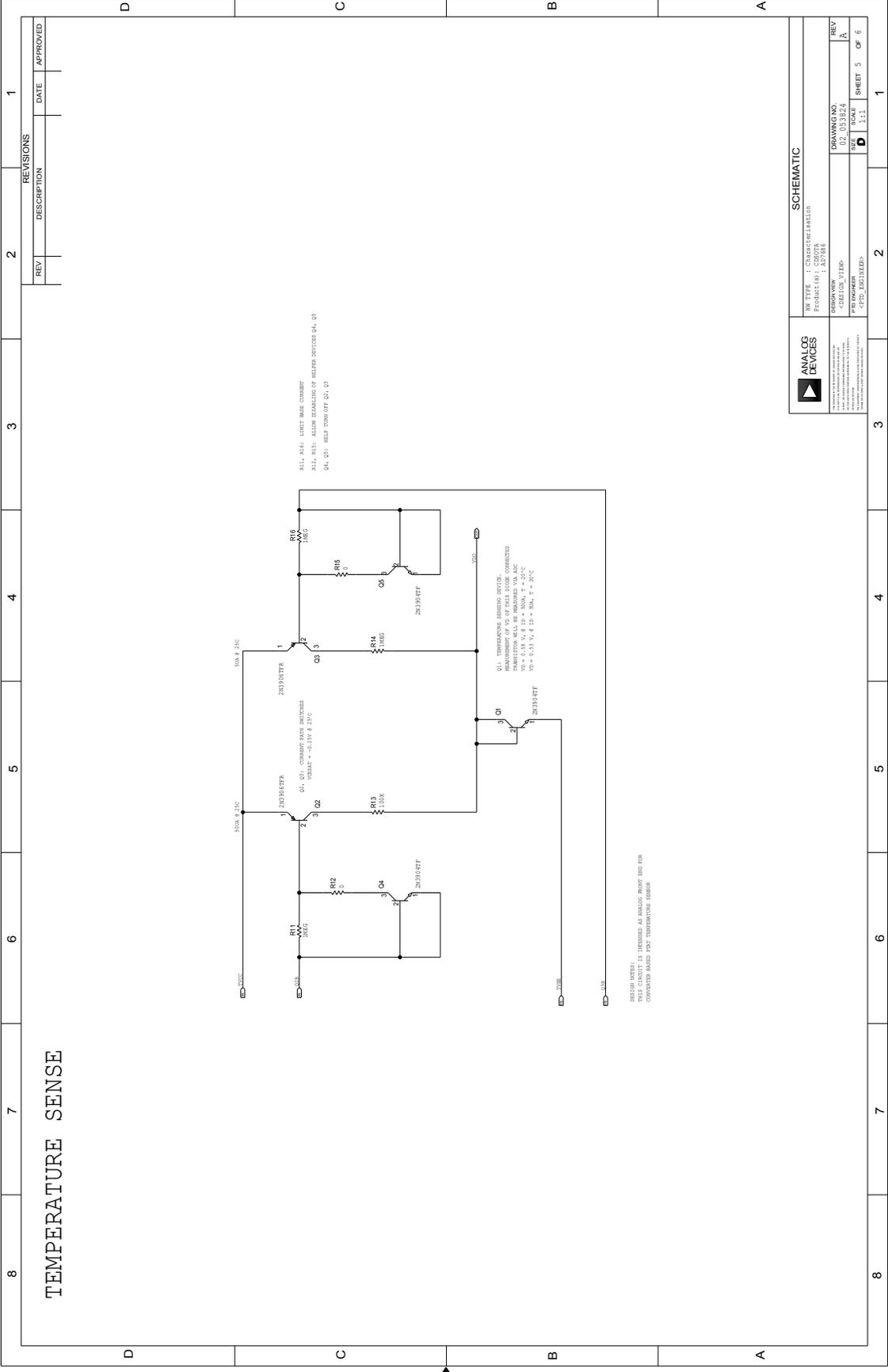
TEMPERATURE SENSE

R11, R16: LIMIT BASE CURRENT

R12, R15: ALLOW DISABLING OF HELPER DEVICES Q4, Q5

Q4, Q5: HELP TURN-OFF Q2, Q3

R16
100KΩ

R15
0

Q5
2N3904TF

R14
1MEG

Q3
2N3906TFR

50A @ 25C

Q3A

Q11: TEMPERATURE SENSING DEVICE;
MEASUREMENT OF VD OF THIS DIODE CORRECTED
TRANSISTOR WILL BE MEASURED VIA ADC.
VD = 0.58 V, @ ID = 50A, T = 20°C
VD = 0.53 V, @ ID = 50A, T = 20°C

Q1
2N3904TF

VDD

R13
100K

Q2
2N3906TFR

500A @ 25C

Q2, Q3: CURRENT PATH SWITCHES
VDSAT = -0.25V @ 25°C

R12
0

Q4
2N3904TF

R11
100KΩ

VDDC

Q1B

Q1A

TDIE

Q1B

DESIGN NOTES:
THIS CIRCUIT IS INTENDED AS ANALOG FRONT END FOR
CONVERTER BASED PN1 TEMPERATURE SENSOR

ANALOG
DEVICES

SCHEMATIC

HW TYPE   : Characterization
Product(s) : CDOTA
             AD766

DESIGN VIEW
<DESIGN_VIEW>

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<PTD_ENGINEER>

DRAWING NO.
02_053824

SIZE D   SCALE
          1:1

REV
A

SHEET 5   OF 6