An optimization approach for high-efficiency high-power-density boost converters

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Abstract – **Boost converters running in valley switching mode have the advantages of low switching loss and small inductor size. However, the switching frequency is not fixed as operating conditions vary, which can make inductor design for this converter challenging. In this paper, a systematic optimization approach is presented that is suitable for wide-input-voltage range designs such as power factor correction (PFC) converters. The loss of each component is modeled as a function of the operating point, and the efficiency is estimated over the entire input voltage range. Given a set of selected cores and Litz wire, an optimal inductor design can be found on a plot of efficiencies and air-gap lengths. Genetic algorithms can be used to find the optimal design with customizable cores. Experiments are conducted to verify the model and the approach. One of the prototypes, designed as the first stage for an ac-dc converter system, achieves around 98% efficiency over the input range of 70V to 170V, boosting to 363V at 45W. The prototype converter has a total volume of 2.8cm^3 and reaches a power density of 263W/in^3.**

Keywords – Boost converter, valley switching mode, optimization, genetic algorithm

I. Introduction

Single-phase ac-dc power supplies are manufactured in extraordinarily large quantities. Single stage topologies such as fly-back converters have been very popular for low-to-moderate power applications [1, 2], while 2-stage ac-dc converters are widely used for achieving miniaturization at higher power levels, and are becoming of interest even at low powers (e.g., [3-7, 17-19, 27]). In a typical two-stage ac-dc converter, the front-end ac-dc stage is often called the power factor correction (PFC) stage; in addition to controlling line current harmonic content, it can be used to reduce bulk capacitor size. It transforms a wide range of input voltages derived from the ac line into an approximately fixed dc voltage for the back-end isolated dc-dc stage while controlling instantaneous current and power from the ac source. This front-end stage is often implemented with a boost converter owing to its simplicity and wide input-voltage operating range.

A key feature of the boost converter is that it is both very simple and can achieve high efficiency and power density. When a diode is used for the top switch in the half-bridge, only a single low-side gate driver is needed. If the boost converter is run in valley switching mode (or quasi-boundary conduction mode), the switching loss can be greatly mitigated, and zero voltage switching (ZVS) can be achieved for some operating conditions [8, 9]. Likewise, a smaller numerical value for the inductor can be employed (often corresponding to a smaller physical inductor) compared to that of a converter operating in continuous conduction mode (CCM).

An important characteristic of the valley switching mode operation is that the switching frequency varies with circuit parameters — input voltage, output voltage, and power level. This varying switching frequency affects the total power loss of the circuit and increases the complexity of design optimization. To achieve good performance, then, a valley-switched boost converter for PFC systems should be optimized for its operating across a wide range of conditions.

In this paper, a systematical design workflow for both power density and efficiency optimization of a low power-rated boost converter is presented. We focus on a valley-switched design suitable for use in a low-power 2-stage ac-dc converter system. First, state-of-the-art components are selected including GaN switches, SiC diodes, high-performance MLCC capacitors [10] and ferrite materials. Next, the inductor is modeled and parameterized. The construction of the inductor substantially affects the achievable size and energy loss of the converter. Third, the operational parameters are estimated such as the switching frequency and inductor current. Then the losses in each component are analyzed and further derived into evaluation functions that estimate both the overall energy efficiency and the total volume of the converter. Several optimized builds of inductors are tested and compared to validate the proposed design approach. As an example, one optimized prototype of a 45 W boost converter has a total volume of approximately 2.8cm^3 and around 98% efficiency over a wide input voltage range from 70V to 170V, boosting to 363V at a maximum power of 45W. The power density is about 16 W/cm^3 or 263 W/in^3.

II. Circuit Description

In this paper, we focus on a boost converter design that operates to boost input voltage in a low-power 2-stage ac-dc converter system when operating from rectified voltages from 110 Vac input, and simply providing a "pass through" when operating from higher ac voltages; this operating function is valuable for narrowing the operating voltage range of a second-stage converter and for reducing the physical size of the twice-line-frequency energy storage capacitor in an ac-dc adapter.

Despite the numerous variations employed in converter topology to achieve wider operating ranges (e.g., [11]) these

techniques usually increase complexity, making them difficult to use in low-power systems owing to component count and size. Here we explore the topologically simple case of the valley-switched boost converter operating within its zero-voltage switching range ($V_{in} < ½V_{out}$). A diode is selected for the top switch in the half-bridge so that no high side gate driver or level shifter required. In this case, it is the boost inductor which dominates the overall volume of the converter (neglecting consideration of line-frequency energy buffering required in an ac-dc converter system), and which – together with the boost diode – incurs the largest portion of converter loss.

The peripheral circuit elements include voltage dividers to scale down the high voltage signals in the circuit, and a logic circuit to drive the bottom switch gate, as shown in Fig.1. The entire logic circuit runs on very low voltage and is only using basic components such as comparators, current mirrors and logic gates, which can be integrated into a single ASIC. Therefore, in optimizing the design of this miniaturized boost converter, the volume of the logic circuit is neglected. The two comparators in the logic circuit determine when to turn-on and -off the switch (similar to designs in [11, 23, 24]). When the bottom switch is in on, the voltage on the ramp-generator increases and eventually hit a reference voltage "I_{ref}", and then the switch is turned off. This reference voltage "I_{ref}" controls the on time of the bottom switch and therefore determines the peak current in the inductor. When the bottom switch is off for some time and the inductor current decreases and eventually the switching-node voltage drops lower than another reference voltage "V_{ref}", and the other comparator turns the bottom switch on. This reference voltage "V_{ref}" determines the turn-on voltage which is related to part of the switching loss.

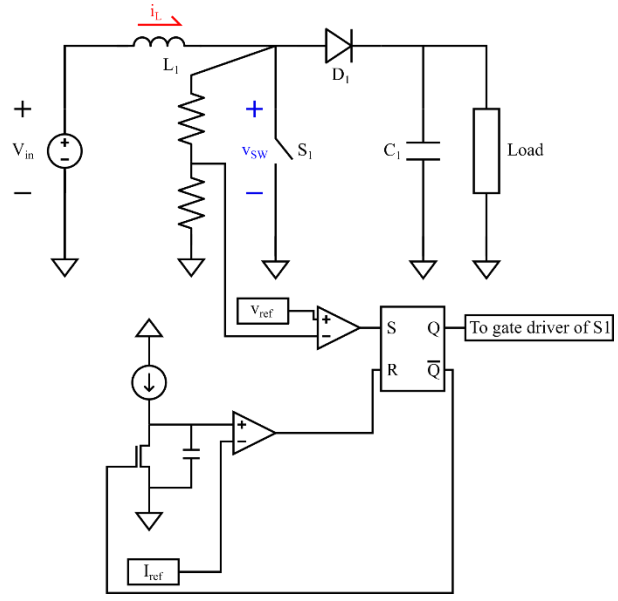

Fig. 1. Schematic of the boost converter and its controller.

The circuit operation can be illustrated by the inductor current and switching node voltage waveforms shown in Fig. 2.

Consider the initial current in the inductor is zero and switch S1 is on. The current increases at a rate of $\frac{V_{in}}{L}$, and when the ramp voltage hits the current reference at inductor current I_{peak}. The bottom switch is turned off. The duration of this interval is denoted as t_{rise}. The switching node voltage then rings up over an interval t_{hold} until it reaches output voltage V_{out}. The diode turns on and the current in the inductor decreases at the rate of $\frac{V_{out}-V_{in}}{L}$. As soon as the inductor current hits zero, the diode turns off. This interval is denoted as t_{fall}. Then the switching node voltage starts to ring down. When the input voltage is smaller than half of the output voltage, the valley of this voltage ring down can hit zero, providing ZVS turn-on for the switch. If the input voltage is higher than half of the output voltage, the voltage will not ring down to zero, and the reference V_{ref} needs to be set at an appropriate level to ensure that turn-on happens for the next switching cycle. This resonance operation interval is noted as t_{ring}, and the negative peak value of the inductor current (minimum current) is noted as I_{npeak}. In the last interval, the inductor current starts to rise again and reaches zero in a time denoted t_{rise}, finishing a complete cycle.

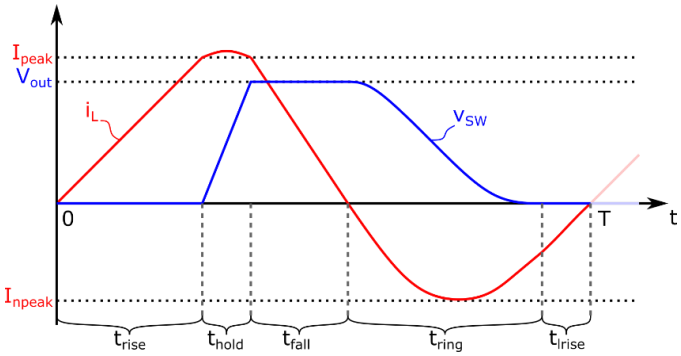

Fig. 2. Waveforms of inductor current and switching node voltage.

To evaluate the energy efficiency of the circuit, the details of the inductor current are needed — the positive and negative peak current, the duration of each interval, and the frequency. These values are related to the instantaneous input voltage, output voltage and the power being converted. These relationships can be derived from the equation of energy conservation. On the left side of this equation is the total energy flows into the converter in a cycle and on the right side is the total energy flows out from the converter.

$$\frac{1}{2}V_{in}I_{peak}(t_{rise}+t_{fall})+W_{C_{tot},in}=P_{out}T+W_{C_{tot},out}+\frac{1}{2}V_{in}I_{npeak}t_{lrise} \quad (1)$$

where $W_{C_{tot},in}$ and $W_{C_{tot},out}$ are the energy entering and exiting the total parasitic capacitance at the switching node during the two resonant ringing times. They should be equal to each other in normal operations. This total capacitance value normally consists of the drain-to-source capacitance of the bottom switch, the junction capacitance of the diode, the parasitic capacitance on the PCB traces and the capacitors in parallel with the sensing resistors. Practically these capacitances are non-linear over the variable dc bias, which is difficult to model and predict, as illustrated in Fig. 3.

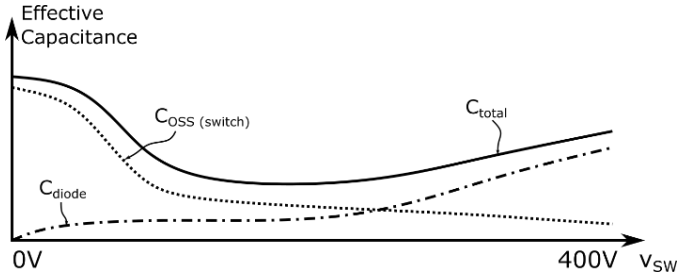

Fig. 3. Total switching node capacitance versus switching node voltage

An easier way is to estimate the equivalent total capacitance value for a certain circuit design in the experiment at the desired output voltage. The switching frequency is measured in the experiment and it should match the frequency calculated from the equation using the estimated capacitance. Then this equivalent total capacitance can be used in further design workflow for this specific circuit.

III. Loss Analysis

The power loss of each component is closely examined according to the estimated current and voltage waveforms.

A. Switch Loss

The significant losses taking place in the bottom switch comprise conduction loss and switching loss. The conduction loss can be calculated by the integral over the switch on time.

$$P_{S_{conduction}} = \frac{1}{t_{rise}} \int_0^{I_{peak}} i^2 R_{dson} \mathrm{d}i + \frac{1}{t_{lrise}} \int_0^{I_{npeak}} i^2 R_{dson} \mathrm{d}i \quad (2)$$

It has been found [13, 14, 24] that for many commercial GaN switches operating at hundreds of volts and MHz frequencies, the dc conduction resistance should be scaled by a factor, yielding an appropriate value for dynamic R_{dson} that may be 3-6 times the dc room temperature on-state resistance value. It is also known that at sufficiently high frequencies, output capacitance loss of GaN switches may be important even under ZVS operating conditions [25, 26], but for our operating conditions (up to few MHz operation) it is believed that dynamic R_{dson} is the dominant loss concern [24].

The switching loss of the switch can be neglected because of ZVS takes place at both turn-on and turn-off transitions. When turning off the switch, the parasitic capacitance at the switching node clamps the voltage across the switch near zero during turn-off. The turn-on transition is triggered when the switching node voltage reaches zero.

B. Diode Loss

The diode forward conduction loss can be approximated as the product of averaged output current and forward voltage drop on the diode V_f.

$$P_{diode} \approx I_{out} V_f \approx P_{out} \frac{V_f}{V_{out}} \quad (3)$$

C. Inductor Loss

The major losses in the inductor are the losses in the core material and losses in the winding copper.

For the core loss estimation, there are a lot of existing methods, among which the Steinmetz equation and its improved versions are the most commonly used, e.g., [15, 16]. Steinmetz model data are sometimes provided in the datasheet of the material or available from other sources (e.g., [20, 21]). In this work, as the inductor current has a large ac component and a moderate dc component and with positive and negative peaks are part of LC resonance, we simply employ traditional Steinmetz loss estimates approximating the inductor current as sinusoidal. It is noted that for some materials (e.g., Ferroxcube 3F46), the classic Steinmetz equation form may not fit well over a wide flux density range; as described in Appendix A, for such cases we utilize a modified equation that fits over a wider range.

The copper conduction loss owes to skin effect and proximity effect. Using Litz wire with strands of certain fineness can greatly mitigate skin effect. The copper loss due to proximity effect is evaluated using the following equations from [12].

$$P_{copper} = F_r I_{ac}^2 R_{dc} \quad (4)$$

$$F_r = 1 + \frac{\pi^2 \omega^2 \mu_0^2 N^2 n^2 d_c^2 k}{768 \rho_c^2 b_c^2} \quad (5)$$

where n is the number of strands in Litz wire, d_c is diameter of copper of one strand, k is a factor that normally equals to 1, ρ_c is the copper resistance at the operating temperature, b_c is the breadth of the window in core, and I_{ac} is the ac rms current in the inductor. In [12], the author showed that to minimize the copper loss, the optimal solution is always with a full bobbin provided the correct wire can be obtained. Practically, to build an inductor for our application and frequency range, served Litz wire with extra inter-turn insulation is preferred, and we limit the number of strands and the strand diameter to that available from manufacturers' catalogs. With each of the specific type of Litz wire, the number of turns to make a full bobbin can be estimated using the equations provided in [12]. When the core and Litz wire are selected, there is only air-gap length left as the sole variable to determine the inductance of the inductor, and once the inductance is known, the power loss in the inductor can be calculated.

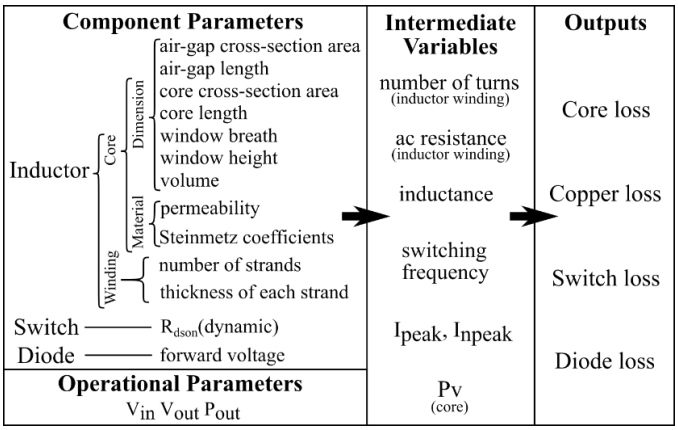

Fig. 4. Map of parameters and variables for loss analysis.

In summary, the component waveform and power loss modeling map the component and circuit parameters to the total power loss of the system for a given operating condition, as shown in Fig. 4. Therefore, it can be wrapped into a single evaluation function for optimization, as elaborated in the next section.

IV. Optimization

A. With Commercial Cores

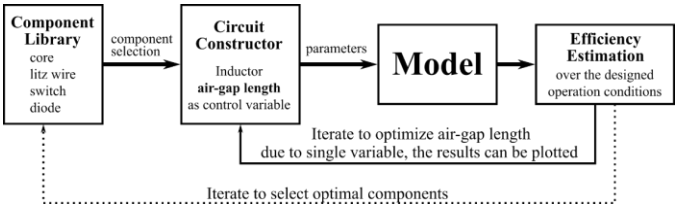

Fig. 5, Flowchart for circuit optimization with ready-made cores.

Fig. 5 illustrates the optimization workflow for a boost converter using standard commercial cores. The outer optimization loop iterates to sweep through the selection of inductor core and material, Litz wire, switch and diode that used in this design in an outer loop (dotted path at the bottom in Fig. 5). The considerations are not only high efficiency but also reasonable sizes of the components, leading to a Pareto front optimizing the combination of size and loss. An inner iteration loop operates to determine the optimal air-gap length for the inductor; this loop structure - and its use of modeling in the inner loop — is a bit different than that taken on in other optimization approaches (e.g., [28]). Notice that the outer loop relies on the inner loop's optimal air-gap length to compare the different selections of components.

Here we focus on the optimization of the boost inductor, as it contributes the vast majority of the volume of the boost converter itself and is a major contributor, with the diode, to overall boost converter loss. There is only one control variable which is the air-gap length of the inductor, as in a given loop the core's window area is fixed and the number of turns of the winding using the selected Litz wire is also fixed to provide a full bobbin.

We consider optimizing the boost converter for delivering a fixed (maximum) output power over a specified input voltage range during the line cycle; this yields input current waveforms that are acceptable with good efficiency and tends to reduce the required energy twice-line-frequency energy buffering and reduce switching-frequency variation over the line cycle (e.g., [22, 23]). For optimization purposes, we consider the maximum average operating power of the converter and operate the converter over the line cycle at a fixed power level. Considering that the boost converter is converting a variable input voltage to a much higher fixed output voltage with fixed maximum output power, the relationship between the energy efficiency and air-gap length can be plotted. For example, Fig. 6 shows the estimated converter efficiency vs. air-gap length for different input voltages from 70V to 170V for a converter boosting to 370V at a fixed power of 45 W. The core is Ferroxcube EFD15 3F46 and the winding is made of 26 turns of 450/48AWG Litz wire. It can be seen from the plot that when the air-gap length is small, a higher efficiency happens at a higher input voltage and vice versa. Depending on the actual operation region and distribution, the best air-gap length can be easily found on the plot. In this example, an air-gap length of 0.58mm would result in an inductor of 16.8μH. The efficiency curves for different input voltages are crossing at this air-gap length approximately, indicating that the efficiency of the converter remains relatively high over the entire operating range, which is desirable for the operating conditions considered in this work.

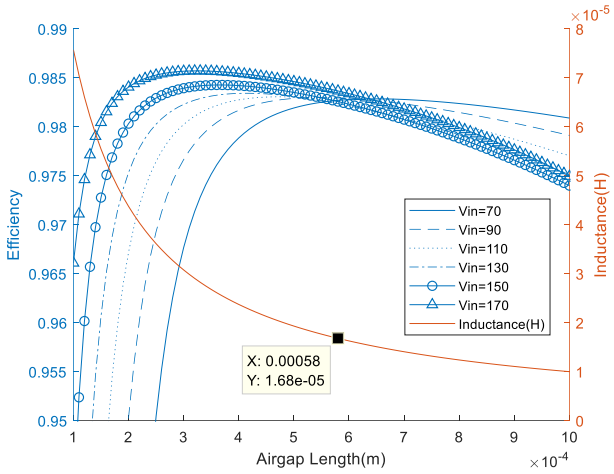

Fig. 6. Efficiency—Air-gap-length—Input-voltage plot for EFD15 core inductor with 26 Turns of 450/48AWG Litz wire.

B. With Customizable Cores

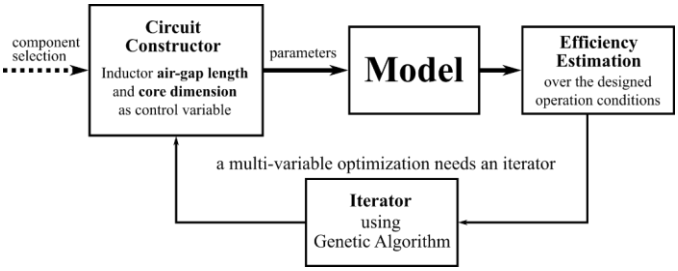

Fig. 7. Workflow for optimization with customizable cores.

With commercial core geometries as in the previous subsection, the dimension of the core is fixed and only the air-gap length is optimizable. With customized cores, one can obtain improvements in combinations of efficiency and inductor volume. The workflow is illustrated in Fig. 7. Assume that the component selection part is similar, the dimension parameters of the core together with the air-gap length are iterated by an automated process to find the best parameters. A genetic algorithm is very suitable for this process.

To use the genetic algorithm, the candidate solution needs to be identified first. While a core can be designed in arbitrary shapes, it is easier to start with a commonly seen and regular geometry. It would help to reduce the number of unknown variables to define the dimension, and also is more likely to be

feasible for fabrication. The shape of the core affects the efficiency considerably, even with the same inductor volume. Intuitively, a core with cylindrical center-post has the minimal average turn length for the winding covering the same cross-sectional area.

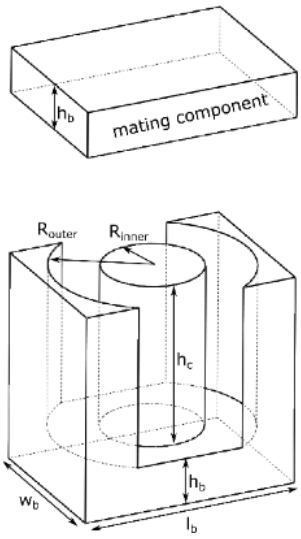

Fig. 8. The dimension of EQ cores

We consider the case of a core having a cylindrical center-post and a cuboid outer shape, which is preferred for a maximum packing factor of the final assembly. An EQ type core model with free and continuous scaling of its dimension (Fig. 8) is used here. There are four control variables to define a core, which are the radius of the center-post R_{inner}, the outer radius of the window R_{outer}, the height of the center post h_c and the width of the base rectangle w_b. The rest of the dimension parameters can be calculated from the constraint of constant core cross-sectional area along the flux loop approximately. The mating core is a single piece of a cuboid that has a height equal to the base thickness h_b.

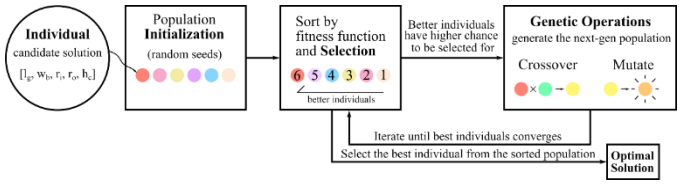

Fig. 9. Workflow for the genetic algorithm.

Illustrated in Fig. 9, so now a candidate solution (individual) for genetic algorithm has five scalar variables. A pool of multiple individuals (population) is firstly initialized with random individuals. Then the population is sorted by the fitness function. The fitness function is defined as the inverse of the product of total power loss of the circuit and the volume of the inductor ($\frac{1}{P_{loss} \times Vol_L}$) so that smaller and more efficient cores are preferred. The better fitness value an individual is got, the more likely it is chosen for generating the next generation population. The selected individuals are crossovered with each and mutated randomly to produce new individuals. The crossover rates and mutation rates are random numbers with approximate normal distribution and unity standard deviation. After a certain number of iterations, the best individual in the population converges and the loop stops. In an example shown below, the core geometries are optimized considering using both 180-strand 48AWG Litz wire and 450-strand 48AWG Litz wire for the winding. The population size is 1000, and the number of iterations is 2000. It normally converges after around 500 iterations, but sometimes there are still better individuals popping out afterwards. An extra limit is applied that the volume of the inductor can be specified in GA to generate the Pareto front for optimized results of power loss vs. volume, as shown in Fig. 10. Also shown are predicted power losses for the three inductors used in experimental verification.

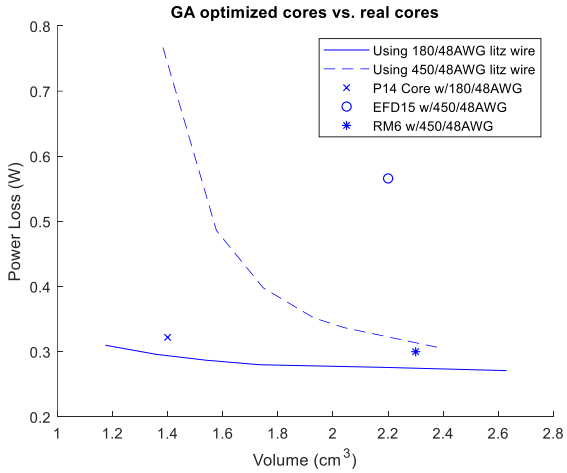

Fig. 10. Power loss and volume of GA optimized cores with 180 and 450 strands Litz wire and three real core inductors.

There are several findings with this GA optimized results. Firstly, using Litz wire with a smaller number of strands helps reduce the power loss. However, the decrement in the power loss slows down when increasing the volume budget. On the other hand, with larger sizes of the inductor and larger number of turns in the winding, the inductance value is getting larger and operating frequency is lower than the valid estimation ranges for the specific material. The error between the experimental measurement and prediction is much larger under such circumstances. Secondly, an EFD15 core with a rectangular cross-sectional area has a much worse performance than the optimized cores. The finished EFD15 inductor is almost cuboid so that is a direct comparison to show the significance to optimizing the core shape. Thirdly, an RM6 core inductor has a better performance compared to the GA optimized one, but its volume is the net volume (2.3cm^3) instead of box volume (2.7cm^3). The optimized core has a loss number only a little bit larger than the RM6 inductor considering net volume. Fourthly, an RM6 core with 450/48AWG Litz wire inductor is still better than a P14 core with a 180/48AWG inductor. For the P14 core inductor, the net volume is considered. Lastly, the core eventually evolves into a tall structure with four symmetrical legs by GA, although the model was firstly started with two legs, as shown in Fig. 11.

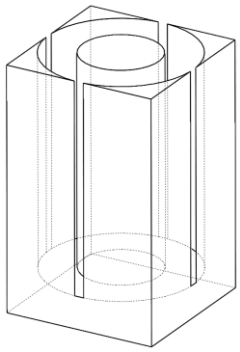

Fig. 11. Optimized core shape (base) by genetic algorithm.

V. Experiment Verification

A prototype circuit is made to verify the model. The components used and the testing conditions are listed in Table I.

TABLE I. EXPERIMENT SETUPS

Components	**Model Number**
Bottom switch	GS66504B
Diode	C3D1P7060Q
Input and output capacitors	C5750X6S2W225K250KA
Test conditions	
Input Voltage	From 70V to 170V
Output Voltage	363V
Load Resistance	2950Ω
Output Power	45W

In Fig. 6 it predicts that there is a splitting air-gap length that to the left, the efficiency is higher when the input voltage is higher, and vice versa. Therefore, six RM6 inductors with different air-gap lengths around this splitting gap are made and tested in the experiment. They are all made of 21 turns of 450/48AWG Litz wire. The splitting point estimated is with around 30μH of inductance, as shown in Fig. 12.

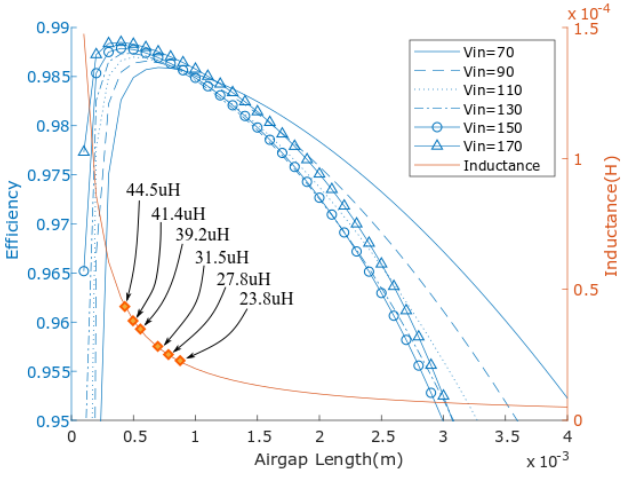

Fig. 12. Efficiency—Air-gap-length—Input-voltage plot for RM6 core inductor with 21 Turns of 450/48AWG Litz wire.

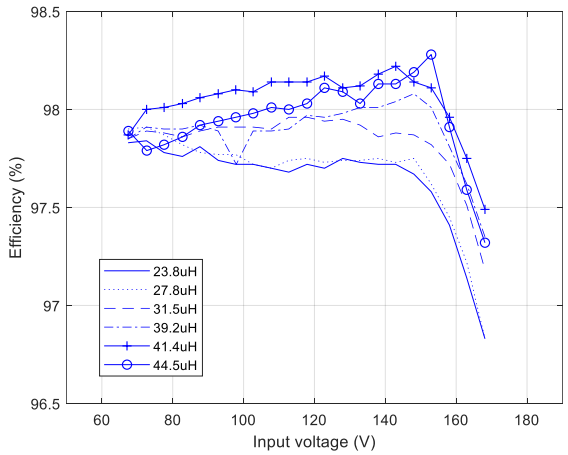

Fig. 13. Efficiencies of six RM6 inductors with different air-gap lengths and inductance values.

In Fig. 13, the efficiencies of the six inductors are all starting from approximately the same value. This matches the phenomenon that the 70V trace in Fig. 12 is almost flat for the tested inductance range. The efficiencies started to decrease significantly for input voltages from 150V to 170V because the switching node voltage fails to reach zero during t_{ring} as expected and the turn-on transition is losing ZVS. This is due to the non-linear total capacitance at the switching node. For the input voltages from 70V to 150V, inductors larger than 31.5μH have increased efficiencies when the input voltage is increasing. When the inductance is getting too big (44.5μH), the efficiency at lower voltages are getting worse. On the other hand, the efficiencies for smaller inductors have decreased trend on input voltage increment. The measured efficiencies are slightly smaller than the predictions in terms of absolute numbers. It will not be able to accurately predict the power losses but this method can compare the relative goodness among different designs.

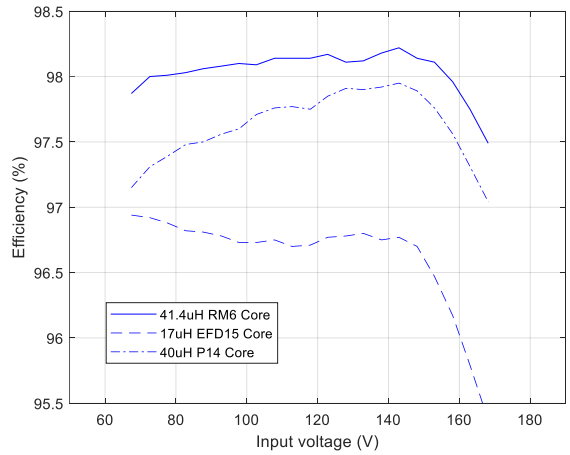

Fig. 14. Efficiencies of three different inductors with different cores.

The three different cores compared in the previous section are built with their optimized (around the splitting point) air-

gaps in the experiment. The efficiencies are measured and plotted in Fig. 14. The EFD15 core and RM6 core are with approximately the same size (EFD15:2.2cm^3, RM6:2.3cm^3), but the efficiency of the EFD15 core is much lower than RM6. The P14 core inductor, however, only has a net volume of 1.4 cm^3 while only losing extra 0.2% to 0.6% efficiency over the operating range.

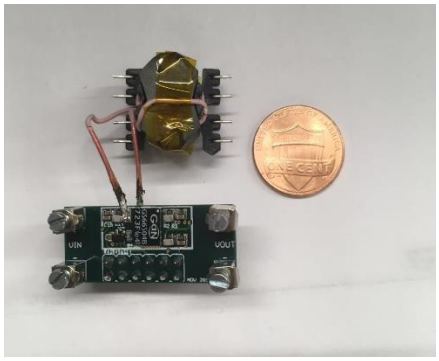

Fig. 15. Photo of a prototype boost converter with an RM6 core inductor.

Fig. 15 shows the photo of an RM6 core inductor and the boost circuit. It has a total volume of approximately 2.8cm^3 (considering only the boost converter and net volume of the inductor) processing 45W, boosting a wide input variation from 70V to 170V to a fixed 363V, at the efficiency of around 98%. The power density is 16W/cm^3 or 263W/in^3.

VI. Conclusion

In this paper, a systematical approach of designing a high-efficiency high-energy-density boost converter that operates on a wide input voltage range to a fixed output voltage is presented. The boost converter operates in valley switching mode to mitigate switching loss, and therefore the switching frequency and other operational parameters are not fixed through the variation of the input voltage. The loss for each component is modeled and calculated and used to evaluate the designs and selections of the components. With commercial cores, the only control variable is the air-gap length of the inductor if the construction of Litz wire is selected. The relationships among the variable input voltage, the air-gap length, and estimated efficiencies can be plotted through the loss estimation models, and the optimal solution can be easily found on the plot. If customizable cores are allowed, the optimal solutions can be found by a genetic algorithm. Experiments are conducted to verify the estimation model. The boost converter designed in this work is suitable for boosting input voltage in a low-power 2-stage ac-dc converter system and reducing the physical size of the twice-line-frequency energy storage capacitor.

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APPENDIX A

An issue regarding the core loss of magnetic materials is that when trying to use curve fitting to find the coefficients in the original Steinmetz equation, the replotted curve deviates from the measurements a lot. An original Steinmetz equation lays straight lines on a logarithmic plot while the real measurements are bent curves, as seen in Fig. A.1.a, there are three sets of curve fitting results but none of them can well describe the loss characteristics covering operation range of interest. The material is Ferroxcube 3F46 in this example, which is one of the best materials in the 1MHz to 3MHz operation range.

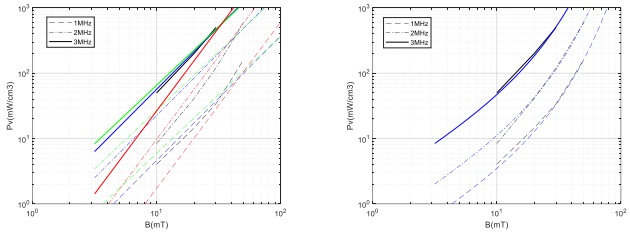

Fig. A.1. Extraction of Steinmetz coefficients for Ferroxcube 3F46 material. (a) Original Steinmetz equation, color traces are different curve fitting results, the black traces are from the datasheet (b) Altered equation.

$$P_v = C_m f^x B^y a^{f/2e6} b^{B/50e-3} f^{kB} \tag{6}$$

Therefore, an altered form of Steinmetz equation is proposed. Several additional terms are added to enhance the detail description capability. The new curve fitting results are shown in Fig. A.1.b. In the suggested operation range and with a single equation, the predictions are close to the measurements.