A High Frequency Inverter for Variable Load Operation

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***Abstract*—Inverters operating at high frequency (HF, 3-30MHz) are important to numerous industrial and commercial applications such as induction heating, plasma generation, and wireless power transfer. A major challenge in these applications is that the load impedance can vary dynamically in both real and complex components over a wide range, making it difficult to maintain high-efficiency soft-switched operation. The constraints that a variable load impedance place on high frequency inverter design results in systems that are often bulky, expensive, and inefficient. This paper presents the design, physical prototype, controller, and experimental results of a high-frequency variable load inverter that is able to directly drive widely variable loads with high efficiency. The prototype can deliver 1kW into a 22 ohm load at 95.4% efficiency as well as deliver significant power to a wide range of both capacitive and inductive loads.**

I. Introduction

There are many applications that require high-frequency, high-power inverters such as induction heating, plasma generation, and wireless power transfer. These applications are often narrow band e.g., utilizing one of the ISM band frequencies (6.78 MHz, 13.56 MHz, 27.12 MHz,...), and present a load impedance with time-varying real and imaginary components. The high power level and varying impedance present a significant design challenge as switch-mode inverters typically require some minimum inductive load current to achieve the zero voltage switching needed for high efficiency operation at high frequency. While an inverter can be inductively preloaded to provide the needed inductive load current for zero voltage switching across all expected operating points, this decreases efficiency due to the additional circulating current.

In practice, an inverter designed to drive a fixed load impedance is often used in conjunction with a tunable matching network (TMN). The TMN is used to dynamically match the time-varying load impedance to the load impedance desired for the inverter, allowing for high efficiency zero voltage switching operation under varying loads. While the TMN simplifies inverter design, it requires variable impedances that are subjected to high power levels. Possible implementations of the variable impedances include mechanically variable components, switched arrays of discrete components, or switched mode circuits capable of emulating a variable impedance [1]–[3]. However, these choices are typically some combination of expensive, lossy, and physically large. Additionally, in the most common case of TMNs that use mechanically-variable components to form the matching network, adjustment is extremely slow, limiting overall system dynamic performance and efficiency under rapidly-varying loads. Eliminating the TMN represents a possible improvement in system cost, volume, and performance.

Previous approaches to eliminating the TMN have included the impedance compression network, which is able to reduce the variation in load impedance for a pair of identical loads through a passive matching network [4]–[6]. However, the requirement for two identical loads is difficult to achieve in many applications. There is thus an unmet need for a high-performance drop-in replacement for the TMN and inverter combination widely used today.

This paper presents a high-frequency inverter system that can directly drive widely-varying load impedances with high efficiency and fast dynamic response. Based on the architecture proposed in [7], the proposed inverter system uses interactions among multiple inverters to maintain desirable loading for the constituent inverters as the load varies. Unlike the related approach in [8], the design here utilizes two individual inverters connected together via an immittance converter, with the voltage and phase of each inverter controlled to deliver the desired load power while maintaining desirable effective driving-point load impedances for each inverter despite wide changes in the system load impedance. Section II of the paper discusses the variable-load inverter architecture, section III presents the prototype system, section IV covers the system control scheme, section V presents experimental results, and section VI concludes the paper.

II. System Architecture

The HF variable-load inverter architecture, illustrated in Figure 1, comprises two HF inverters with independently-controllable amplitude and phase connected together via an immittance converter [7]. The immittance converter acts as a specialized lossless power combining network through which the two inverters each supply the load while also modulating the effective impedance seen by the other. The system is controlled such that the individual inverters see desirable individual loadings for a wide range of system load impedances.

To simplify the analysis in this section, we treat the two inverters as identical ideal sinusoidal voltage sources capable of driving any resistive / inductive load, subject only to maximum output voltage and current constraints. One inverter (inverter A) is connected directly to the load while the other (inverter B) is connected through the immittance converter. The immittance converter symmetrically transforms a voltage

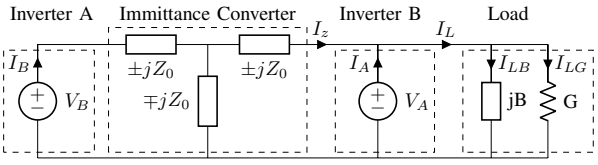

Fig. 1: Structure of the variable-load inverter architecture.

applied to one port into a phase shifted current on the other port and converts capacitive (inductive) susceptances seen at one port into inductive (capacitive) impedances at the other port. Through the interaction of the two inverters via the immittance converter, the effective impedances they each see can be controlled through their voltages and relative phase to each appear as a resistive/inductive, while the system load impedance varies across a large load range including both inductive and capacitive variations. This "load modulation" effect is beneficial as there exist classes of high efficiency zero-voltage switching inverters, such as variants of D, E, and Φ_2, which can efficiently drive a wide range of resistive / inductive loads but not capacitive loads [9]–[11]. The action of the immittance converter allows a system utilizing these zero-voltage switching inverters to drive capacitive loads that they could not otherwise individually drive.

The proposed architecture utilizes inverter A to support inductive components of the load susceptance, inverter B to support capacitive components of load susceptance via the action of the immittance converter, and both inverters to supply the real power to the conductive component of the load. If desired, the immittance converter can also be utilized to synthesize inductive loading currents for each inverter to support ZVS soft switching.

The equations below denote the relationships of voltage and current among inverter A, inverter B, and the load, where V_A and V_B are phasors representing the RMS inverter output voltages, I_A and I_B are phasors representing the RMS inverter output currents, I_Z is the phasor representing RMS immittance converter output current, and I_L is the phasor representing the RMS load current. Φ_B is the phase of inverter B voltage V_B with respect to a desired reference; Φ_A, the phase of inverter A, is taken here to be zero.

$$I_L = V_A/Z_L \tag{1}$$
$$I_L = I_A + I_Z \tag{2}$$
$$I_Z = -j \cdot V_B/Z_0 \tag{3}$$
$$I_B = j \cdot V_A/Z_0 \tag{4}$$
$$P_{out} = \mathrm{Re}(V_A \cdot I_L^*) \tag{5}$$

As inverter A is connected directly to the load, the value of V_A determines I_L, P_{out}, and, through the action of the immittance converter, I_B. $|V_B|$ and Φ_B can then be set to determine I_A, and thus the effective impedance seen by inverter A, and the phase angle of the effective impedance seen by inverter B. The allowable load impedance range for a given power level is determined by V_{max} and I_{max} ratings of the inverters, the impedance of the immittance converter, Z_0, and the range of impedances each inverter can operate into while maintaining constraints such as zero voltage switching. When the two inverters are identical, Z_0 is chosen as the "maximum output power impedance" of the inverters, $Z_m = V_{max}/I_{max}$, allowing for full utilization of each inverter.

Figure 2 shows the maximum power that can be delivered into a given load impedance by the proposed architecture, assuming identical inverters that can drive any resistive / inductive load within a voltage V_{max} and current I_{max}; these curves are derived in [7][1]. Power is normalized to $P_{ri} = V_{max} \cdot I_{max}$, the maximum output power rating of a single inverter, and impedance is normalized to Z_m. As desired output power is reduced there is available inverter output current or voltage capability which can drive resistive loads that deviate increasingly from V_{max}/I_{max} as well as reactive load components, leading to an expanded load range. As each inverter can deliver maximum power into an impedance of Z_m, the maximum power load impedance of the system, Z_{out}, is $Z_m/2$.

For points in Figure 2 at which the desired power level is on the boundary of that achievable for a given impedance, there is only one set of values for V_A, V_B, and Φ_B for which the system can satisfy all constraints. At points where the desired power level is less than the maximum power level at that impedance the system of equations is under-constrained and there are many values of V_B and Φ_B which satisfy the constraints. In that case some additional criteria (e.g., maximizing efficiency) can be used to constrain the system and determine the system operating parameters. Methods for determining system operating conditions for under-constrained operating points as well as for inverters that have limitations beyond a maximum current and voltage are covered in section IV.

III. Prototype

A prototype inverter system has been constructed to validate the proposed HF variable load inverter concept. The system consists of the two constituent inverters, immittance converter, and control circuity, all on a single PCB. A simplified system schematic is show in Figure 3 with component values in Table I; details may be found in [12]. The zero voltage switching class D half bridge was chosen as the topology of the two constituent inverters due to the high switch utilization and flexible constraints on loading to maintain zero voltage switching [10]. A series resonant filter on the output of each inverter reduces harmonic content in the output voltage and inverter load current. For inverter B the capacitors of the immittance converter and output filter are combined into one element. A STM32F334 microcontroller is used to control the system and generate gate drive signals with adjustable phase and duty cycle. Isolated gate drive is provided by a combination of a RP-1206S isolated DC/DC converter, UCC27611 gate drive

[1]In [7] derivations are given using peak voltages and currents. Here we use RMS values.

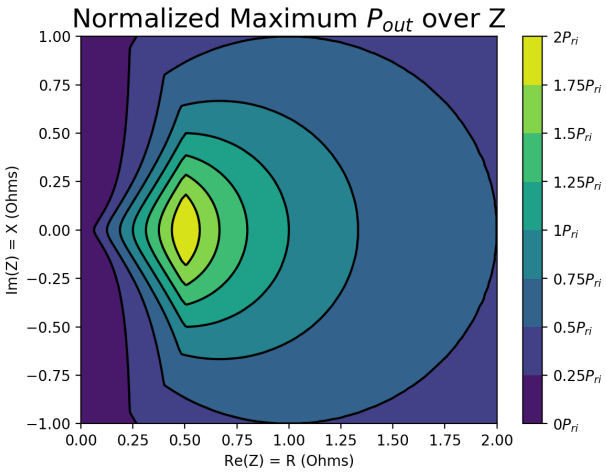

Fig. 2: Normalized maximum P_{out} over load impedance for idealized variable-load inverter system, with $V_{max} = 1$, $I_{max} = 1$ and $Z_o = 1$

IC, and ISO7720 digital isolator. System power comes from two independent controllable lab power supplies (KLP 600-4-1200 and XLN60026), operated over voltage ranges of 5 - 375 volts. The whole system is controlled by a computer over USB.

The class D half bridge requires some minimum inductive load current to achieve zero voltage switching, dependent on the supply voltage and the capacitance on the switching node. Nominally, some of this inductive load current is provided by the load while the rest is synthesized via the immittance converter, circulating power between the two inverters. However, solely synthesizing inductive load current in this way reduces the inverter current available to drive the load and increases losses in the output filters and immittance converter due to the additional circulating power. Thus, limited inductive preloading is used on each inverter to reduce the need for synthesized load current. This inductive preloading consists of an inductor (L4 and L5 respectively) and a DC blocking capacitor from the switching node of each inverter to ground. As the preload circuit is not resonant it provides a triangular commutating current that can achieve the same commutating effect with lower RMS current as compared to the the sinusoidal current synthesized through the immittance converter.

The maximum inverter supply voltage and output current (375V DC, 4A RMS) were chosen to maximize the system output power and load range given the thermal limitations of the GaN devices used. GaN devices often exhibit higher C_{oss} losses and a higher Rds_{on} value than indicated in the manufacturer provided datasheet when operating at high frequencies [13], [14]. Additionally, the C_{oss} losses are highly influenced by dv/dt, so even with zero voltage switching the supply voltage has a significant impact on transistor loss. To determine optimized values of the maximum inverter supply

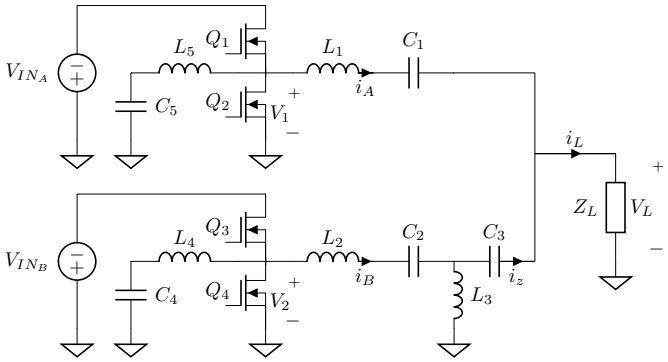

Fig. 3: Simplified System Schematic of the prototype HF Variable-Load Inverter

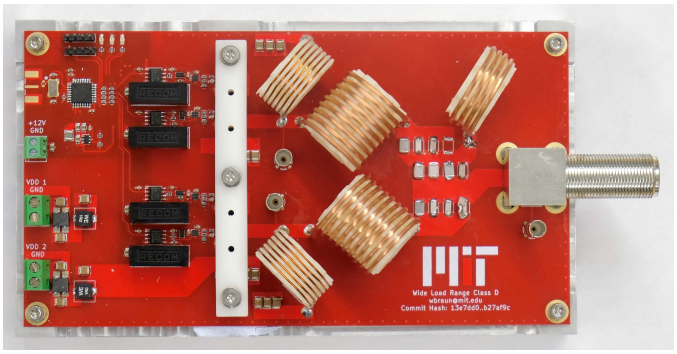

Fig. 4: Prototype System

voltage and output current, analytical data from [13] was used to model device loss across possible operating points.

Excluding connectors, the bounding box dimensions of the system including the heatsink are 190mm x 110mm x 60mm. Figure 4 shows a picture of the inverter electronics and Table II provides final details of the system.

TABLE I: Prototype Component Values

Component	Value	Implementation
Q1, Q2, Q3, Q4	$C_{oss} \approx 37pF$ $R_{on} \approx 140m\Omega$	PGA26E19BA
L1, L2	$1.14\mu H$	9 turns 1.6mm wire 22mm diameter, 2.75mm pitch
L3	$430nH$	4 turns 1.6mm wire 26mm diameter, 2.4mm pitch
L4, L5	$950nH$	6 turns 0.7mm wire 25mm diameter, 1.8mm pitch
C1	$121pF$	Parallel 3KV C0G Capacitors
C2	$84pF$	Parallel 3KV C0G Capacitors
C3	$327pF$	Parallel 3KV C0G Capacitors
C4, C5	$0.3\mu F$	3x $0.1\mu F$ 500V X7RC1210C104KCRACTU

TABLE II: Prototype Parameters

Frequency	$13.56MHz$
Z_{out}	21.3Ω
P_{max}	$1kW$
$V_{IN_{max}}$	$375V$

IV. Control Scheme

A. Control Challenges

In Section II the high frequency variable load inverter was modeled with each constituent inverter as an ideal voltage source that could drive any resistive / inductive load, only subject to maximum output voltage and current limits. However, real inverters have additional limitations and loss mechanisms which impact system performance.

In the Class D half bridge topology chosen for the prototype system there is a dv/dt limit at the switching node imposed by the common-mode transient immunity (CMTI) limit of the digital isolator used for level shifting in the gate drive circuity ($85V/ns$), a supply voltage dependent device capacitance which impacts the required inductive current for zero voltage switching, and a dv/dt related C_{oss} loss. These may be considered together with an additional control parameter, the switch duty cycle. Additionally, we control the supply voltage to each constituent inverter, but the magnitude of the output voltage and the exact phase in relation to the gate drive waveforms in a class D half bridge depends on loading [11]. A control system is desired that can determine if a given load point and power level combination is achievable, and if so, generate optimal system operating parameters. However, the previously mentioned limitations, non-idealities, and loss mechanisms are difficult to model analytically or only with numerical approximations. This makes it impractical to derive system operating conditions through analytically solving a system of equations as may be done for simpler systems.

B. Quasi-Static Model Prediction Control

The control requirements for the high frequency variable load inverter differs from many other power electrics applications in two key ways. The first difference is that transient dynamics happen on a time scale that is quite short compared to typically required control speeds. Due to the high switching frequency and modest associated energy storage elements, the system reaches steady state operating conditions on a time scale that is significantly smaller than the time scale at which the load impedance typically varies (e.g., in rf plasma drive or wireless power transfer systems). The second difference is that one of the most important parameters of the system, the presence of zero voltage switching, is effectively a hidden parameter. Due to the high switching frequency it is often impractical to have the controller directly measure ZVS conditions or maintain them under closed-loop control.

Taking these differences into account we have created what we term a quasi-static model prediction controller. Quasi-static signifies that our controller does not store or track the detailed system state or dynamics (e.g., as in [15], [16]). Rather, each inner-loop query to the controller provides an open-loop estimate of behavior based on the periodic steady state. It is effectively a feed forward model. The predictive part of the controller is due to the fact that we predict the presence of the zero voltage switching that we can not directly observe with the models of the two constituent inverters.

Our implementation of the controller consists of the aforementioned inverter model and a search function. Given a load impedance and desired power level, the search function searches over the space of possible distributions of load current between the two inverters. At each point the search function queries the model of the constituent inverters to determine if zero voltage switching and other constraints are met for both inverters such that the point represents valid operating conditions and obtain all operating parameters for that point. The search function then uses additional performance data provided by the inverter model to select the most optimal point according to some cost function.

This approach has several advantages when compared to analytically solving the system of equations 1 - 5 with additional constraints directly applied. We can use a numerical model of the inverter that is simpler to derive and more accurately captures non-linear phenomena such as some of the loss mechanisms and optimize the control for arbitrary cost functions, only limited by the parameters available through the inverter model.

C. Inverter Model

The constituent inverter model can be considered a black box that takes a load point consisting of a desired output voltage and output current as input, determines if zero voltage switching is achievable for the load point, and if so, returns the operating parameters (V_{in}, duty cycle) along with any parameters needed for system optimization. Currently, the search function only optimizes power dissipation so this is the only additional parameter that is calculated.

The ability to achieve zero voltage switching and the duty cycle for which this occurs is determined by the desired output voltage and output current. In the class D half bridge, the switch duty cycle determines the deadtime in which both switches are off and the inductive portion of the load current and/or additional preload current delivers charge to the switching node, commutating it from one supply rail to the other and enabling zero voltage switching. The charge required is dependent on the supply voltage and the capacitance on the switching node while the charge delivered is the integral of the current into the switching node during the deadime period. Too little charge delivered leads to a failure to achieve zero voltage switching while too much charge leads to the reverse conduction of the switching device, both conditions which lead to increased losses and should be avoided.

The required deadtime, and thus the duty cycle, can be calculated by solving for when the integral of the current flowing into the switching node is equal to the required charge. For some load points there is no solution to this integral as there is not enough inductive load current and/or additional preload current to meet the charge requirement, representing a point for which zero voltage can not be achieved.

Solving this integral symbolically would be difficult as there are voltage dependent non-linearities in the switching device capacitance, the output voltage varies in phase with the gate drive signals as a function of loading, and the

commutating current consists of the sinusoidal load current and the triangular current provided by the preload inductor. However, this integral can be solved numerically with some simplifications while still retaining the accuracy needed for the controller.

To obtain a numerical solution for the deadtime, the inverter output voltage was assumed to have a fixed relation with the phase of the gate drive signals and the amplitude of the supply voltage. A polynomial curve fit from the datasheet provided graph of time-related charge and drain-source voltage was used to approximate the non-linear voltage dependent device capacitance. As the charge integral is monotonically increasing with increasing deadtime over the range of interest this integral is solved with binary search over the possible range of deadtime values.

The full system of equations that are used to solve this dead time integral are shown below. V_o and I_o are the phasors representing the RMS output voltage and current, both of which are assumed to be sinusoidal. The phase of V_o is taken to be zero with I_o having a phase relative to V_o, and the switching deadtime occurs symmetrically around $t = 0$. $C_{sw}(V_{in})$ is a function providing the voltage dependent time related equivalent capacitance for the switching device used and is derived from the device datasheet. $i_{AG}(t, V_{in})$ represents the switching augmentation current provided by the preload inductance. This current is assumed to be triangular and periodic, with amplitude dependent on V_{in}, and as an inductive current, lagging V_o by a quarter cycle. Q_{sw} is the charge delivered to the switching node while Q_{zvs} is the charge required to achieve zero voltage switching. $i_{SW}(t)$ is the current flowing into the switching node, used for subsequent equations.

$$V_{in} = \frac{|V_o|\pi\sqrt{2}}{2} \tag{6}$$

$$Q_{zvs} = 2V_{dss}(C_{sw}(V_{in}) + C_{static}) \tag{7}$$

$$i_{SW}(t) = -\sqrt{2}\,\mathrm{Re}(I_o e^{jt2\pi f_{sw}}) - i_{AG}(t, V_{in}) \tag{8}$$

$$Q_{sw} = \int_{-D/(2f_{sw})}^{D/(2f_{sw})} i_{SW}(t)dt \tag{9}$$

$$Q_{sw} = Q_{zvs} \tag{10}$$

Finding a valid duty cycle for which zero voltage switching can be achieved does not mean that the operating point is valid; there is still a need to check additional constraints. There is a maximum supply voltage for the inverter, $V_{in_{max}}$, and a maximum output current $I_{o_{max}}$, both chosen to protect the semiconductor devices. The maximum power dissipation, P_{max} was chosen based on the maximum semiconductor junction temperature and the thermal resistance of the heatsink. A maximum dv/dt limit is imposed by the CMTI of the digital isolator used in the gate drive circuity. P_{oss} is the power dissipated in the switching device capacitance, which can be significant for GaN devices. $E_{oss\_diss}(\cdot,\cdot)$ is a function that returns the expected energy dissipated in the switching device capacitance per cycle based on the analytical data presented in [13]. P_{rds} is the I^2R loss due to the on resistance, R_{on}, of the switching device, a loss that only occurs during condition. The equations for these checks are shown below.

$$V_{in} \leq V_{in_{max}} \tag{11}$$

$$|I_o| \leq I_{o_{max}} \tag{12}$$

$$\frac{dv}{dt} = \max_{|t| \leq D/(2f_{sw})} \frac{i_{SW}(t)}{C_{sw}(V_{in})} \tag{13}$$

$$\frac{dv}{dt} \leq \frac{dv}{dt}|_{\max} \tag{14}$$

$$P_{coss} = 2f_{sw}E_{oss\_diss}(\frac{dv}{dt}, V_{in}) \tag{15}$$

$$P_{rds} = 2\int_{(D/2)/f_{sw}}^{(1-D/2)/f_{sw}} R_{on} i_{SW}(t)^2 dt \tag{16}$$

$$P_{max} \geq P_{coss} + P_{rds} \tag{17}$$

If a valid duty cycle is calculated and all additional checks pass the inverter model returns that the operating point is valid along with all associated operating parameters.

D. Search Function

The search function takes an load impedance and output power and, utilizing the inverter model, finds the most optimal set of operating parameters according to some cost function. As from equations 1 - 5, given an output power and load impedance the load current, I_L, is fixed, but the distribution of the load current between the two inverters is not. Provided the output current of inverter A, I_A, the contribution of inverter B, I_Z is fixed and the system is fully constrained. This represents a two dimensional search space, the real and complex components of I_A. Given the low dimensionality of this space it is not computationally intensive to search over, either by brute force as currently implemented or by some form of gradient decent or peak finding.

At each tested point the search function uses the present value of I_A to calculate the phasor V_B from the fixed I_L. Once the the pairs (V_A, I_A) and (V_B, I_B) are calculated they are used to query the inverter model. As previously specified, the inverter model returns if each load point is valid and returns some performance data to be used for optimization. The search function then selects the distribution of current between the two inverters amongst all valid distributions that has the highest performance according to some cost function. The cost function that the controller current uses is minimization of the sum of the power dissipated in the two inverters, as calculated in equation 17. This cost function only takes into account losses in the switching devices, ignoring losses in passive components. However, it is computationally simple and closely approximates maximizing system efficiency.

As mentioned in Section III, the inverters rely on some amount of inductive current that is synthesized via the immittance converter to achieve zero voltage switching. Without synthesized inductive current, zero voltage switching conditions could not be found for many combinations of load impedance and output power. Synthesized inductive currents do not affect the load current and equations 1 - 5 still hold.

To include synthesized inductive currents in the search our controller extends the range of the complex components it searches over. Instead of searching over the reactive current range of $[0, \mathrm{Im}(I_L)]$ the search is over $[0, I_{max}]$. Any point for which $\mathrm{Im}(I_A) > \mathrm{Im}(I_L)$ represents a point with some amount of synthesized load current.

E. Implementation

The entire system controller is currently written in Python2.7 and can generate system operating conditions for arbitrary impedances and power levels in approximately 180ms on a consumer laptop (dual core x86-64 processor). The system controller does not currently run in real time so little effort has been placed in optimizing the speed of the controller. However, there is nothing structurally preventing the controller for achieving high update rates. Optimization in how the search for the optimal operating point is found and a rewrite in a compiled programing language would likely allow for a real-time implementation on an embedded processor.

Additionally, as the system is quasi-static and the input space is only three dimensional (real and imaginary components of load impedance, output power), this controller maps well to a lookup table implementation. A precomputed lookup table would allow for almost instantaneous generation of system operating conditions. At 8 bit precision for all inputs and outputs, a lookup table implementation would take approximately 84MB of memory, and interpolation would enable significantly higher resolution without additional storage. External flash memory of this capacity costs only a few dollars, allowing the controller to be ported to even very low performance embedded devices if this approach is taken.

To illustrate how the additional limitations placed on the inverters impacts the load range when compared to the idealized system in Figure 2 we used the system controller to generate a plot of maximum output power over load impedance for our prototype system, shown in Figure 5. In this plot, the most significant deviation from the curves presented for the idealized system is the reduced load range at impedances with magnitude below that of the system's optimal output impedance. Most of the reduction in load range is primarily due to the dv/dt limit imposed by the gate drive circuity, which effectively places a limit on the maximum inductive current during the deadime period. This reduces the load range for very reactive impedances.

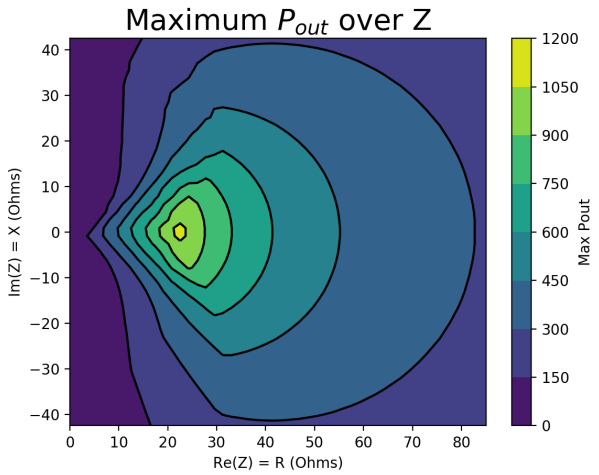

Fig. 5: Maximum P_{out} over load impedance for prototype variable-load inverter system, considering practical limits such as dv/dt

V. Experimental Results

To evaluate the system as a whole the system controller was used to generate operating points for the hardware prototype across a wide range of load impedances and delivered power levels. A TMN (MKS model MWH-100) coupled to a 50 ohm load (BIRD model 8201) was used to provide a variable load impedance. A V/I probe (MKS Model 000-1106-117) was used to monitor the output of the inverter system, allowing accurate measurements of delivered power and load impedance at the inverter system output. The system controller was run in an open loop mode, generating operating parameters for the system based on a single measurement of the load impedance provided by the TMN and the desired output power level. However, due to some phenomena not fully modeled in the system controller and mis-tuning of the output filters and immittance converter, the output power did not always match the value provided to the controller. The reference output power was proportionally adjusted to achieve a more exact output power, allowing for a more accurate evaluation of the system at fixed power levels at the expense of a slightly reduced allowable impedance range. To realize closed loop power control, one might utilize the proposed model and controller for feedforward, feeding back measured output power and load impedance, where the output power is compared to the target value, and a compensator is used to generate an input to the model.

Due to the ease of generating arbitrary load points through the TMN and the computerized control of the system and associated test equipment, we were able to characterize the system across a wide range of power levels and impedances. In Figure 6 we present plots of the system efficiency at $250W \pm 10\%$ and $500W \pm 20\%$ delivered power for numerous load points spanning a wide range of resistances and both inductive and capacitive loading. At a $250W$ power level the load range is primarily limited by the range of impedances that can be provided via the test setup. At a $500W$ power level the boundaries of the plot are determined by the allowable impedance range of the inverter prototype. With a minimum efficiency of 90.6% across the entire load range at a $500W$ and 79.6% at $250W$ and a high average efficiency it is evident that the system is successful in driving a wide load range. In both cases, the highest efficiency is close to the optimal load impedance for the system. At this load point equal power is delivered by the two inverters, minimizing I^2R losses, and the inverters source only the minimum reactive load current

required for zero voltage switching. In these test cases the power of the control and gate drive circuity is not included in the input power. However, the control and gate drive circuity draws $1.7W$, representing less than a 1% decrease in efficiency at $250W$ and 0.5% at $500W$.

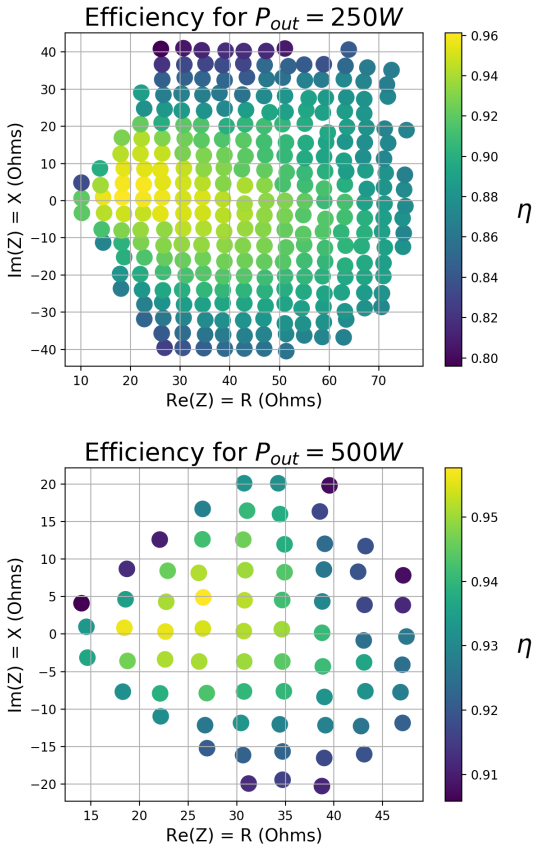

Fig. 6: Measured efficiency over load range for $250W \pm 10\%$ and $500W \pm 20\%$

In Table III and Figure 7 we present exact efficiencies and operating parameters as well as waveforms for the system at three load points representing (a) a purely resistive load, (b) a resistive/inductive load, and (c) a resistive/capacitive load, all with magnitude close to the optimal load impedance of the system. As can be seen, power delivery efficiency is high at all three load points. The converter waveforms show that zero voltage switching is achieved at all three operating points. The distortion evident in the output voltage (particularly for case c) is partially due to the relatively low Q of the output filters on each constituent inverter, the high pass characteristic of the immittance converter topology chosen, and the frequency dependent load impedance presented by the load. Although the distortion has little impact on efficiency or performance in this application, it could be improved by increasing the Q of the output filter, adding a parallel resonant filter to shunt harmonics to ground, or by using an immittance converter with low-pass characteristics. Several such variations of the immittance converter are presented in [17].

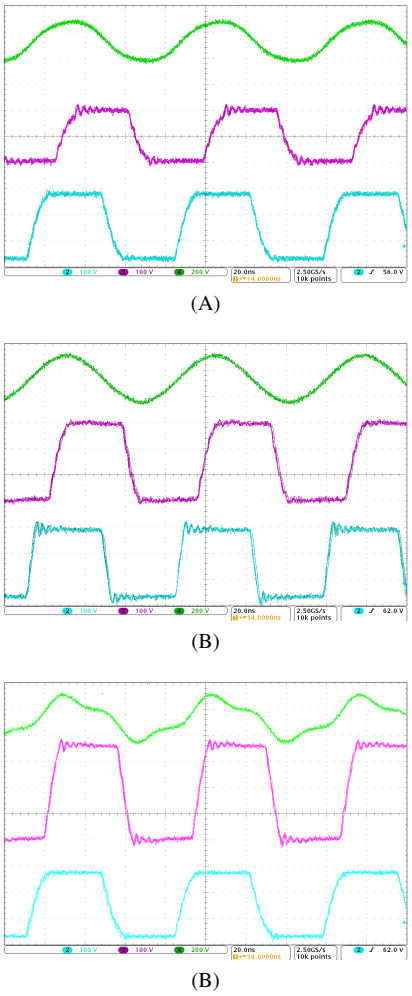

Fig. 7: Experimental converter waveforms for loads A-C (Table III) showing zero voltage switching. Output voltage in Green (200V/div), Inverter A switching node in Turquoise (100V/div), Inverter B switching node in Purple (100V/div)

TABLE III: System parameters for loads a-c

	A	B	C
Z_L	$21.6 + 0.7j$	$18.6 + 10.6j$	$18.6 - 10.4j$
P_{out}	$497W$	$497W$	$498W$
η	95.8%	90.7%	92.1%
V_{IN_A}	$246V$	$258V$	$242V$
V_{IN_B}	$194V$	$288V$	$351V$
Duty A	0.35	0.39	0.34
Duty B	0.35	0.33	0.39
ϕ_B	$69°$	$74°$	$26°$

VI. Conclusion

This paper presents a physical prototype and an efficiency optimizing controller for a high-frequency variable-load inverter system. The prototype delivers RF power at 13.56MHz with a maximum power output of $1kW$ and can drive a wide range of resistive, capacitive, and inductive loads while maintaining high efficiency and zero voltage switching.

Common zero voltage switching inverter topologies are subject to load limitations imposed by the requirements for

zero voltage switching, typically limiting the allowable load to some range of resistive and inductive loads. The presented system overcomes this limitation by distributing the load between two zero voltage switching inverters, the first connected directly to the load and the second connected via an immittance converter. The immittance converter transforms capacitive load currents into inductive load currents, allowing the second inverter to drive capacitive load components that could otherwise not be driven while maintaining zero voltage switching. The first inverter drives inductive load components while both inverters can contribute to the real component of the load. Current can also be circulated through the immittance converter to synthesize arbitrary inductive load currents for each inverter independent of the external load. Through these this topology and control scheme the allowable load range of the constituent inverters can be relatively decoupled from the load range of the entire system. Due to the extended load range the variable-load inverter holds great promise for applications like wireless power transfer, induction heating, and plasma generation, leading to a possible decrease in size and cost and increase in efficiency.

REFERENCES

[1] Y. Lim, H. Tang, S. Lim, and J. Park, "An adaptive impedance-matching network based on a novel capacitor matrix for wireless power transfer," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4403–4413, Aug 2014.

[2] A. S. Jurkov, A. Radomski, and D. J. Perreault, "Tunable impedance matching networks based on phase-switched impedance modulation," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct 2017, pp. 947–954.

[3] F. C. W. Po, E. de Foucauld, D. Morche, P. Vincent, and E. Kerherve, "A novel method for synthesizing an automatic matching network and its control unit," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 9, pp. 2225–2236, Sept 2011.

[4] J. Lu, D. J. Perreault, D. M. Otten, and K. K. Afridi, "Impedance control network resonant dc-dc converter for wide-range high-efficiency operation," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 5040–5056, July 2016.

[5] A. A. Bastami, A. Jurkov, P. Gould, M. Hsing, M. Schmidt, J. I. Ha, and D. J. Perreault, "Dynamic matching system for radio-frequency plasma generation," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 1940–1951, March 2018.

[6] Y. Han, O. Leitermann, D. A. Jackson, J. M. Rivas, and D. J. Perreault, "Resistance compression networks for radio-frequency power conversion," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 41–53, Jan 2007.

[7] D. J. Perreault, "A new architecture for high-frequency variable-load inverters," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2016, pp. 1–8.

[8] A. Kumar, S. Sinha, and K. K. Afridi, "A high-frequency inverter architecture for providing variable compensation in wireless power transfer systems," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018, pp. 3154–3159.

[9] L. Roslaniec, A. S. Jurkov, A. A. Bastami, and D. J. Perreault, "Design of single-switch inverters for variable resistance / load modulation operation," *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3200–3214, June 2015.

[10] D. J. Perreault, J. M. Rivas, and C. R. Sullivan, "Gan in switched-mode power amplifiers," in *Gallium Nitride Enabled High Frequency and High Efficiency Power Conversion*. Springer-Verlag, 2018.

[11] D. C. Hamill, "Class DE inverters and rectifiers for dc-dc conversion," in *PESC Record. 27th Annual IEEE Power Electronics Specialists Conference*, vol. 1, Jun 1996, pp. 854–860 vol.1.

[12] W. D. Braun, "A high frequency variable load inverter architecture," Master's thesis, Massachusetts Institute of Technology, Cambridge, MA, To be submitted.

[13] G. Zulauf, S. Park, W. Liang, K. Surakitbovorn, and J. M. R. Davila, "C_{OSS} losses in 600V GaN power semiconductors in soft-switched, high- and very-high-frequency power converters," *IEEE Transactions on Power Electronics*, 2018.

[14] B. J. Galapon, A. J. Hanson, and D. J. Perreault, "Measuring dynamic on resistance in GaN transistors at MHz frequencies," *IEEE Workshop on Modeling and Control in Power Electronics*, June 2018.

[15] S. R. Sanders, J. M. Noworolski, X. Z. Liu, and G. C. Verghese, "Generalized averaging method for power conversion circuits," *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp. 251–259, Apr 1991.

[16] A. M. Stankovic, D. J. Perreault, and K. Sato, "Synthesis of dissipative nonlinear controllers for series resonant dc/dc converters," *IEEE Transactions on Power Electronics*, vol. 14, no. 4, pp. 673–682, Jul 1999.

[17] M. Borage, K. V. Nagesh, M. S. Bhatia, and S. Tiwari, "Resonant immittance converter topologies," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 3, pp. 971–978, March 2011.