

# Improving Piezoelectric Energy Harvesting Power Bandwidth with the Bias-flip Method

by

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S.B., Massachusetts Institute of Technology (2018)

Submitted to the  
Department of Electrical Engineering and Computer Science  
in Partial Fulfillment of the Requirements of the Degree of  
Master of Engineering in Electrical Engineering and Computer Science  
at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

September 2019

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## Abstract

Vibration energy harvesters may be used as robust and reliable sources of energy for low-power devices such as wireless sensors. Of the many type of vibration energy harvesters, the piezoelectric energy harvesting device (PEHD) is favored for its high energy density and ability to self-start. As a high-Q resonant system, however, a PEHD delivers substantial power only when the ambient vibration frequency matches the PEHD's resonant frequency. Unfortunately, manufacturing uncertainties, and variations in ambient vibration frequency make this frequency match an unrealistic pursuit. The bias-flip style of power electronics is examined as a means to extend the frequency range over which considerable power can be harvested. Comprised of a switch and small inductor, bias-flip power electronics act as a much larger tunable inductor that can come very close to cancelling out the PEHD net capacitive impedance, thereby implementing a nearly complex-conjugated matched load. The bias-flip electronics showed a power improvement of  $\sim 2.5x$  at resonance and  $\sim 5.6x$  at 5 Hz away from resonance, when compared to the optimal resistive load at the end of a full-bridge rectifier. This thesis examines the Bias-flip method in detail and experimentally evaluates its effectiveness in extending power bandwidth. In the final section we test the bias-flip power electronics' resiliency in an environment with multiple vibration frequencies.

Thesis Supervisor: Jeffrey H. Lang

Title: Professor of Electrical Engineering and Computer Science



# Acknowledgements

First and foremost, I would like to thank Professor Jeffrey Lang for his guidance in my research and thesis writing, and for exposing me to the world of energy harvesting. Our weekly meetings and almost endless email exchanges were conducive to the success of this project, and I am much grateful for that. None of this would have been possible if it weren't for my parents, who never fall short on support and encouragement. My father, for inspiring excellence and always setting high standards, and my mother for her unconditional care. Lastly, I would like to thank Tara for always believing in me and embarking on this 5-year adventure with me.



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# Chapter 1

## Introduction

With advancements in wireless sensor networks, microelectromechanical systems, and the internet of things comes a growing need for a self-sufficient energy source. Currently, the above technologies rely greatly on batteries or wired connections as sources of power. With batteries, issues concerning lifetime, disposal, and installment must be dealt with frequently. Vibration energy harvesters provide a viable alternative to conventional sources of energy by converting normally wasted vibration energy in the environment into usable electrical power for low-power and low-voltage devices. For instance, Kinergizer<sup>1</sup>, a company specialized in motion harvesting applications, places vibration energy harvesters on industrial equipment to power sensors in remote places. Replacing batteries, vibration energy harvesters reduce maintenance costs associated with battery replacement and disposal, allowing businesses to operate more efficiently. The three main types of vibration energy harvesters are electromagnetic, piezoelectric, and electrostatic, all of which are bidirectional transducers between mechanical and electrical energy. Piezoelectric energy harvesters have emerged as popular harvesters because of their high efficiency in converting energy, reliability, ease of miniaturization, and ability to self-start. However, as a high-Q resonant system, power is severely degraded as the ambient vibration frequency drifts away from resonance. There are different ways to improve this power bandwidth shortcoming. Of the many ways, this thesis examines the use of the bias-flip method, which was proposed in reference [2], because of its ease of implementation, and ability to integrate in self-powering applications.

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<sup>1</sup>[www.kinergizer.com](http://www.kinergizer.com)

## 1.1 Thesis Objective

The main objective in this research is to experimentally verify that the bias-flip electronics can significantly extend power bandwidth, and even increase the power harvested at resonance. This thesis will build off of the work in reference [4] by experimentally examining the power harvested using a piezoelectric energy harvester with a slightly different physical parameter. Finally, a real-world complication is addressed, the ability of the bias-flip electronics to operate soundly in an environment with multiple frequencies.

## 1.2 Thesis Organization

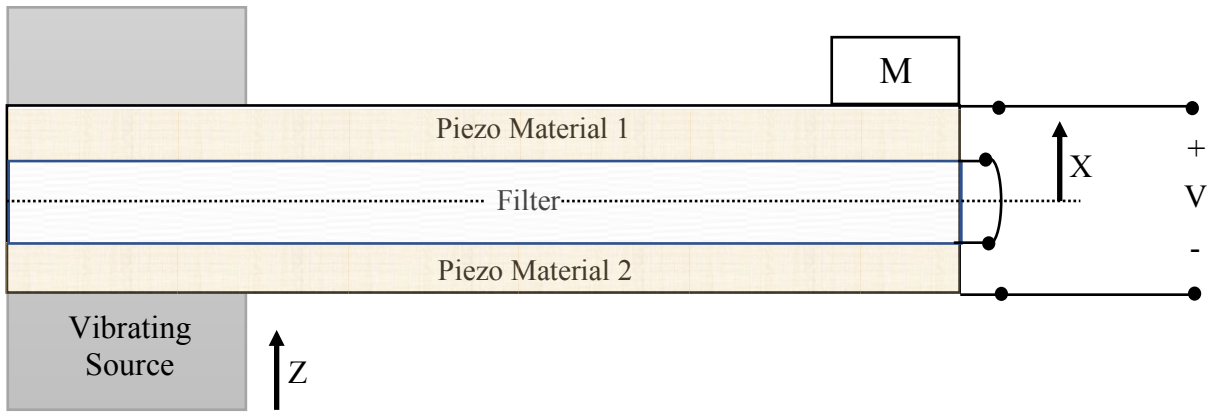
The purpose of this chapter is to emphasize the importance of vibration energy harvesters in achieving the self-powering initiative. However, vibration harvesters have a drawback in that they can only harvest power at the resonant frequency. The challenge in this thesis is to increase the frequency range for which ample power is harvested [8]. In Chapter 2, the piezoelectric energy harvester is modelled, and an equivalent circuit, defined by a set of parameters, is derived. The parameters are then experimentally determined using a thoroughly explained procedure. With a fully characterized harvester, we then move on to Chapter 3, where the power harvested with passive loads is discussed. Chapter 3 makes it apparent that using a passive load to harvest power is either impractical, or wasteful. Chapter 4 introduced the bias-flip electronics, and analytically derives the optimal power that could be harvested. The bias-flip efficiency is then calculated and measured, and the non-ideal bias-flip case is discussed. Chapter 5 gives an overview of the complete harvesting system used in the lab, discussing the design choices made for the circuit and controller. The experimental results are also presented in this chapter and compared to those predicted by LT Spice and MATLAB. Finally, Chapter 6 summarizes the work done in the thesis, reflects on the finds, and proposed future work.



# Chapter 2

## Piezoelectric Harvester Modelling

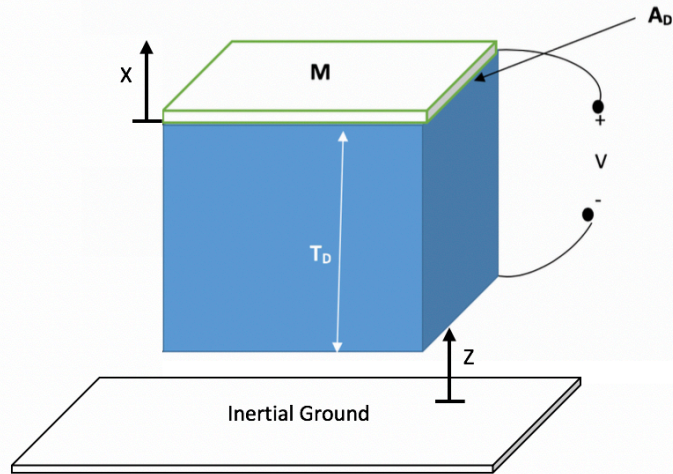
Piezoelectric vibration energy harvesters are bidirectional transducers between electrical and mechanical energy. When the harvester is subjected to mechanical stress, charge is generated in response at its electrical terminals [1]. At the same time, a voltage applied its electrical terminals will create a mechanical stress in the material. As a consequence, the piezoelectric energy harvesting (PEHD) can be characterized in two interdependent domains: the mechanical domain, and electrical domain. In order to understand the behavior of each domain, and establish a relationship between the domains, the spring-mass-damper model is employed. The spring-mass-damper model describes the behavior of a system in 1-D, however the cantilever piezoelectric harvester, shown in Figure 2-1, exhibits piezoelectric behavior in all 3 dimensions. Nonetheless, analyzing the cantilever piezoelectric harvester's behavior in 1-D is sufficient, because we will be using a 1-D source of vibration in the experiments. In this chapter, we will derive an equivalent electromechanical circuit model that describes the behavior of the PEHD. We will then introduce the experimental set-up and discuss the methods used to find the lumped-parameters of the electromechanical circuit. The analysis in the coming chapters will depend on our PEHD model, and therefore, it is imperative that a logical and consistent characterization is established before moving on to the next chapter.



**Figure 2-1.** Cantilever piezoelectric harvesting device with additional mass ( $M$ ) on the surface, with top and bottom electrodes connected in series.

## 2.1 Equivalent PEHD Circuit Model

In order to simplify the following analysis, the 1-D PEHD structure shown in Figure 2-2 will be evaluated. The results obtained in the analysis of the simplified 1-D PEHD can be generalized to the cantilever PEHD by adding geometric constants [7].



**Figure 2-2.** Schematic of the simplified 1-D PEHD device with a surface mass ( $M$ ).

In Figure 2-2,  $A_D$  is the area of the energy harvesting device,  $T_D$  is the height,  $X$  represents the mechanical displacement of the mass relative to the original surface of the PEHD, and  $Z$  is the amplitude of the displacement of the harvester relative to inertial ground.

The piezoelectric material equations can now be applied to the structure in Figure 2-2 [7].

$$\text{Piezoelectric Hooke's Law:} \quad \delta = \frac{1}{Y} \sigma + d_{33} E \quad (2.1)$$

$$\text{Piezoelectric Gauss's Law:} \quad D_3 = \epsilon E + d_{33} \sigma \quad (2.2)$$

where the above parameters, used in (2.1) and (2.2), are defined as:

- $\delta$  = mechanical strain (displacement/length),
- $\sigma$  = mechanical stress(force/area),
- $Y$  = Young's Modulus (force/area),
- $\epsilon$  = dielectric constant,
- $d_{33}$  = piezo-electric coefficient (m/volt),
- $D_3$  = electrical displacement (coulombs/m<sup>2</sup>),
- $B$  = mechanical damping factor,
- $D$  = transduction coefficient
- $K_m$  = mechanical spring constant given as  $\frac{A_D Y}{T_d}$ .

We also make the following approximations:  $\delta \approx \frac{X}{T_D}$  and  $E \approx \frac{V}{T_D}$ , where V is the voltage

drop shown in Figure 2-2. Using the PE material equations and the approximations shown above,

we can now derive lumped-parameter mechanical and electrical equations that define the

behavior of the PEHD. Let  $a_{environmental}$  be the acceleration of the harvester with respect to

inertial ground that results from the changes in the displacement Z such that  $a_{environmental} = \frac{d^2 Z}{dt^2}$ .

Furthermore, let  $f_{electrical}$  reflect the force exerted by the electrical domain back onto the

mechanical domain as a result of electrical loading across the terminals of the harvester.

Therefore, using piezoelectric Hooke's Law in Equation 2.1, the total force exerted on the

harvester is

$$f_{total} = -\sigma A_D = Y d_{33} A_D E - A_D Y \delta = f_{electrical} - f_{mechanical},$$

where  $f_{electrical} = Y d_{33} A_D E$ , and  $f_{mechanical} = A_D Y \delta = K_m X$ .

Mechanical equation:

The equation that describes the spring-mass-damper model [6] can be written as

$$f_{electrical} - f_{mechanical} = f_{environmental} + M \frac{d^2X}{dt^2} + B \frac{dX}{dt} \quad (2.3)$$

where  $f_{environmental} = M a_{environmental} = M \frac{d^2Z}{dt^2}$ .

Replacing  $f_{electrical}$  and  $f_{mechanical}$  in Equation 2.3, we get the following result

$$f_{environmental} - (d_{33}K_m)V = M \frac{d^2X}{dt^2} + B \frac{dX}{dt} + K_m X \quad (2.4)$$

Electrical equation:

The accumulated charge (Q) is proportional to the electrical displacement ( $D_3$ ) and cross-section area ( $A_D$ ) and can be written as

$$\begin{aligned} Q &= A_D \times D_3 = A_D (\epsilon E + d_{33} \sigma) \\ &= (d_{33}K_m)X - \left( \frac{\epsilon A_D}{T_D} - K_m d_{33}^2 \right) V, \end{aligned} \quad (2.5)$$

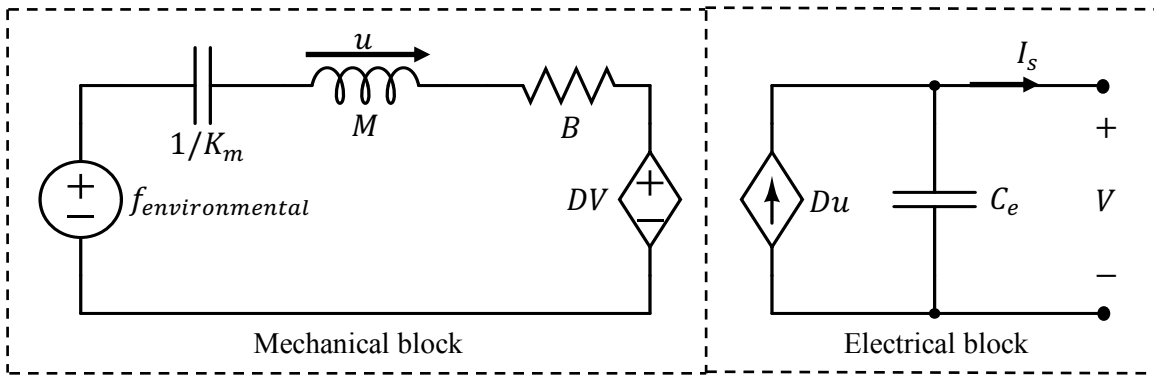
where Gauss's law in Equation 2.2 was replaced. The current ( $I_s$ ) flowing across the harvester is equal to the rate of change of charge (Q). Therefore,

$$I_s = (d_{33}K_m) \frac{dX}{dt} - \left( \frac{\epsilon A_D}{T_D} - K_m d_{33}^2 \right) \frac{dV}{dt}.$$

We now define the parasitic capacitance as  $C_e = \left( \frac{\epsilon A_D}{T_D} - K_m d_{33}^2 \right)$  and the piezoelectric conversion factor as

$D = (d_{33}K_m)$ . We now get the electrical relation

$$I_s = D \frac{dX}{dt} - C_e \frac{dV}{dt}. \quad (2.6)$$

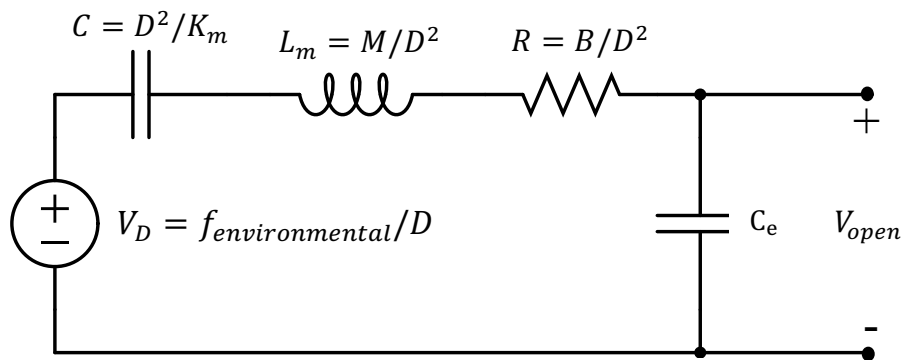


**Figure 2-3.** Equivalent electromechanical model of the piezoelectric harvester [5].



The electromechanical model shown in Figure 2-3 is constructed from Equations 2.4 and 2.6. The mechanical block of Figure 2-3 is derived from the mechanical equation (2.4) where the voltage sources,  $f_{environmental}$  and  $DV$ , represent the forces  $f_{environmental}$  and  $DV$ , and the current represents the velocity  $u = \frac{dx}{dt}$ . With current representing velocity, it's apparent from the mechanical equation that the inductor represents mass (M), the capacitor represents the spring (1/K), and the resistor represents the damping factor (B). Moreover, the transduction between electrical and mechanical energy is modelled by the interdependent voltage and current source with conversion factor D. That said, we have a voltage-dependent voltage source on the mechanical side (DV). The electrical block is described by the electrical equation (2.6). Again, with current representing velocity, it is apparent that the parasitic capacitor is connected in parallel to the current-dependent current source (Du).

We can now pass the mechanics through the two dependent-sources, and obtain the equivalent electrical circuit model shown in Figure 2-4. Also, the circuit components of Figure 2-3 are renamed in Figure 2-4 for a more intuitive circuit representation. In Figure 2-4,  $M/D^2$  is replaced with  $L_m$ ,  $B/D^2$  is replaced with  $R$ ,  $D^2/K_m$  is replaced with  $C$ , and  $f_{environmental}/D$  is replaced with  $V_D$ .



**Figure 2-4.** Equivalent PEHD electric circuit model without dependent sources.

In Figure 2-4, the voltage source ( $V_D$ ) is equal  $(M * a_{environmental})/D$ .

We may assume that vibrations are sinusoidal in nature, which means that the displacement  $Z$  in Figure 2-2 can be written as  $Z = Z_o \sin(\omega t)$ , where  $Z_o$  is the amplitude of the displacement  $Z$ . Therefore, the acceleration of the PEHD caused by the vibrating source is  $a_{environmental} = -\omega^2 Z_o \sin(\omega t)$ . Replacing the amplitude of the acceleration ( $\omega^2 Z_o$ ) with  $A$ ,  $V_d$  can now be expressed as

$$V_D = \frac{MA}{D} \sin \omega t. \quad (2.7)$$

In sinusoidal steady-state, the input voltage source takes the form  $V_D = \Re(\widetilde{V}_D e^{j\omega t})$ , hence the output voltage in Figure 2-4 is calculated as

$$\widetilde{V}_{open} = \frac{\widetilde{V}_D / C_e}{j\omega R + 1/C - \omega^2 L_m + 1/C_e} \quad (2.8)$$

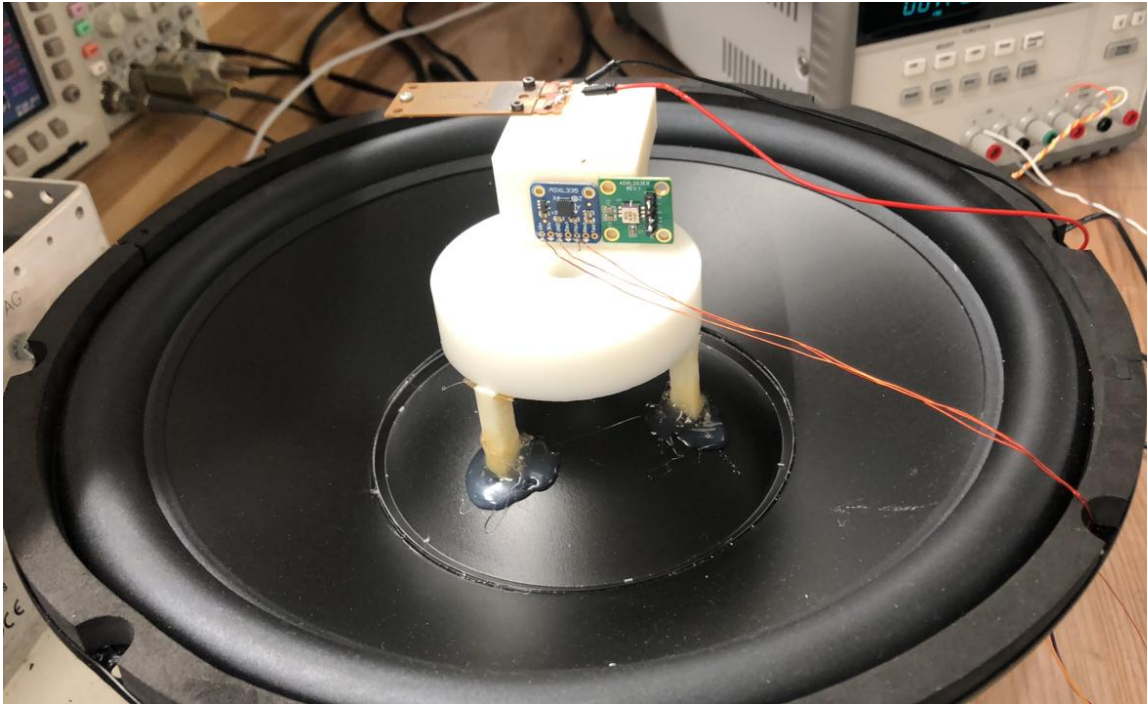
Now that we have derived an electrical circuit that characterizes the behavior of the piezoelectric energy harvester, it's time to find the parameters in Figure 2-4. The next section introduces the experimental setup, as well as the methods used to find the parameters in the electrical circuit model.

## 2.2 Experimental Setup and Data Acquisition

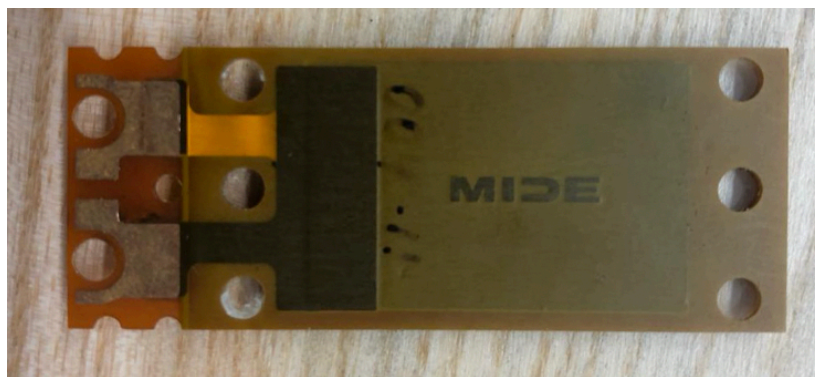
In this chapter, the experimental setup is introduced. The four fundamental components in the setup are the custom shaker table, the piezoelectric energy harvester, microcontroller, and the mounted accelerometer. In order to mimic a vibrating source from which the harvester can generate power from, a calibrated shaker table was used. The source of vibration in the shaker table is a speaker sub-woofer, whose vibration frequency and amplitude can be easily controlled, as shown in Figure 2-5. The sub-woofer can be used as a vibrating source, because the harvester is relatively light, and is subjected to accelerations below 1g [4].

An accelerometer (ADXL335) is mounted onto the vibrating surface in order to measure the vertical acceleration applied by the shaker table onto the harvester. One of the main purposes

for attaching an accelerometer is to ensure that the acceleration amplitude is held constant, which is essential for collecting consistent results. Lastly, a MIDE (PPA-2014) was used as the piezoelectric energy harvester with a screw placed on the tip as an additional mass. I choose to use the Pyboard V1.1 as the microcontroller.



**Figure 2-5.** Piezoelectric energy harvester setup. The speaker woofer acts as a shaker table, and the harvester and accelerometer are attached to a custom mount. A screw is placed at the tip of the harvester to act as an additional mass.

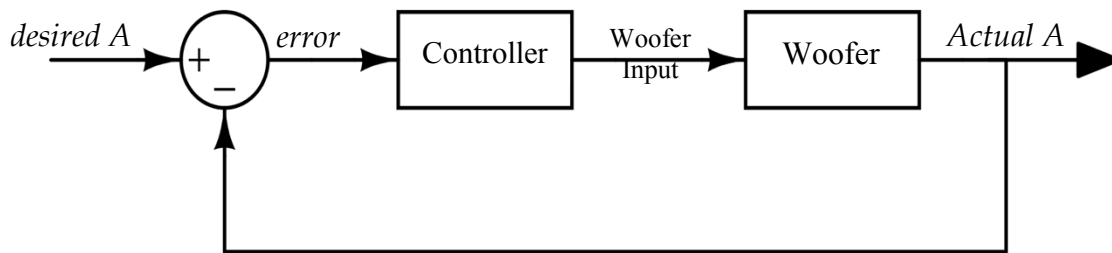


**Figure 2-6.** MIDE (PPA-2014) cantilever piezoelectric harvester.

## 2.3 Piezoelectric harvester characterization

The microcontroller was programmed (shown in A3.1 of the appendix) to be able to characterize the PEHD quickly and repeatedly [5]. This involves measuring the open-circuit voltage (V) and short-circuit current, while sweeping through frequency at a constant acceleration. The microcontroller outputs a voltage sine-wave  $V_{vibration} = V_g \sin(\omega t)$  using its built-in DAC, which powers the shaker table through a power amplifier. In order to maintain a fixed acceleration the feedback controller shown in Figure 2-7 is implemented, where

$$error = |desired\ acceleration - actual\ acceleration|. \quad (2.9)$$



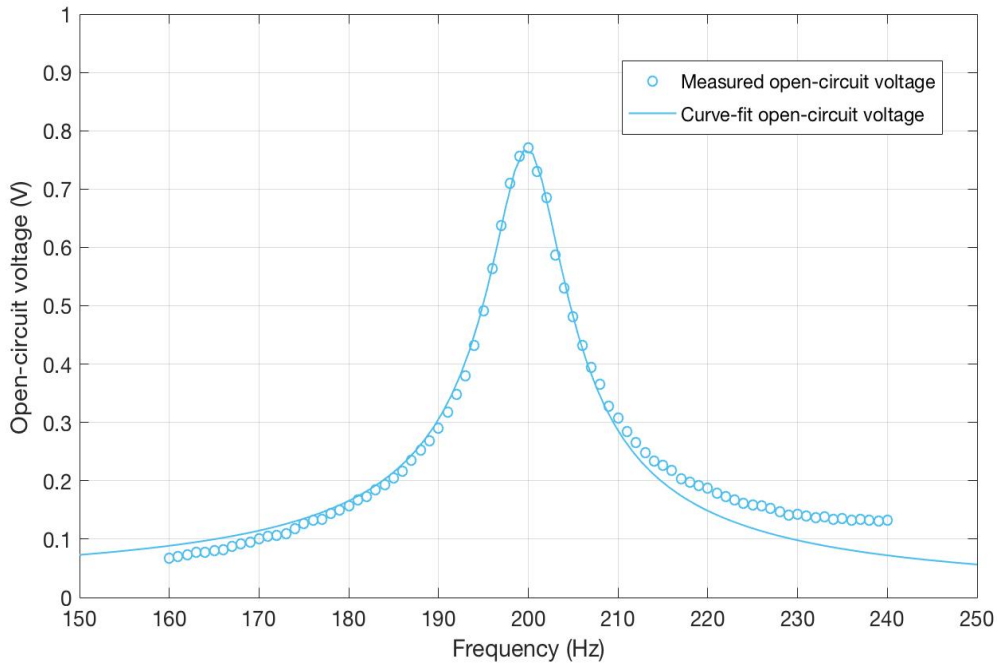
**Figure 2-7.** Simplified diagram of the feedback circuit used to maintain constant acceleration.

The accelerometer outputs an analog voltage, proportional to the acceleration it senses. This voltage is read by the microcontroller using the built-in ADC and is compared to the desired acceleration. If the error term is larger than a certain threshold, the amplitude of  $V_{vibration}$  is adjusted. The adjustments continue to happen until the error term is less than a specified threshold, which was chosen as  $0.005g$ , where  $g = 9.81 \text{ m/s}^2$ . The code that enables the maintenance of a fixed acceleration during the frequency sweep is given in the appendix A3.1. The open-circuit voltage measured, while sweeping frequency at a constant acceleration of  $0.193g$  is shown in Figure 2-8. Using the MATLAB curve-fitting feature, we can fit the

open-circuit voltage in (2.8) to the measured open-circuit voltage. Substituting the macro variables  $X_1 = DA/C_e$ ,  $X_2 = R/L_m$ , and  $X_3 = \frac{1}{cL_m} + \frac{1}{c_eL_m}$  in (2.8), we get the equivalent equation.

$$\widetilde{V}_{open} = \frac{X_1}{j\omega X_2 + X_3 - \omega^2} \quad (2.10)$$

Fitting equation 2.10 to the open-circuit voltage measurements, the macro variables are found as  $X_1 = 1280 \times (2\pi)^2 \text{ Vrad}^2/\text{s}^2$ ,  $X_2 = 8.32 \times 2\pi \text{ rad/s}$ , and  $X_3 = 39980 \times (2\pi)^2 \text{ rad}^2/\text{s}^2$ .

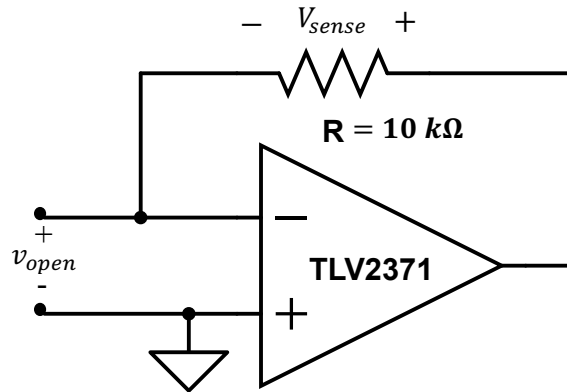


**Figure 2-8.** Measured and calculated open-circuit voltage across PEHD at an acceleration of 0.193g.

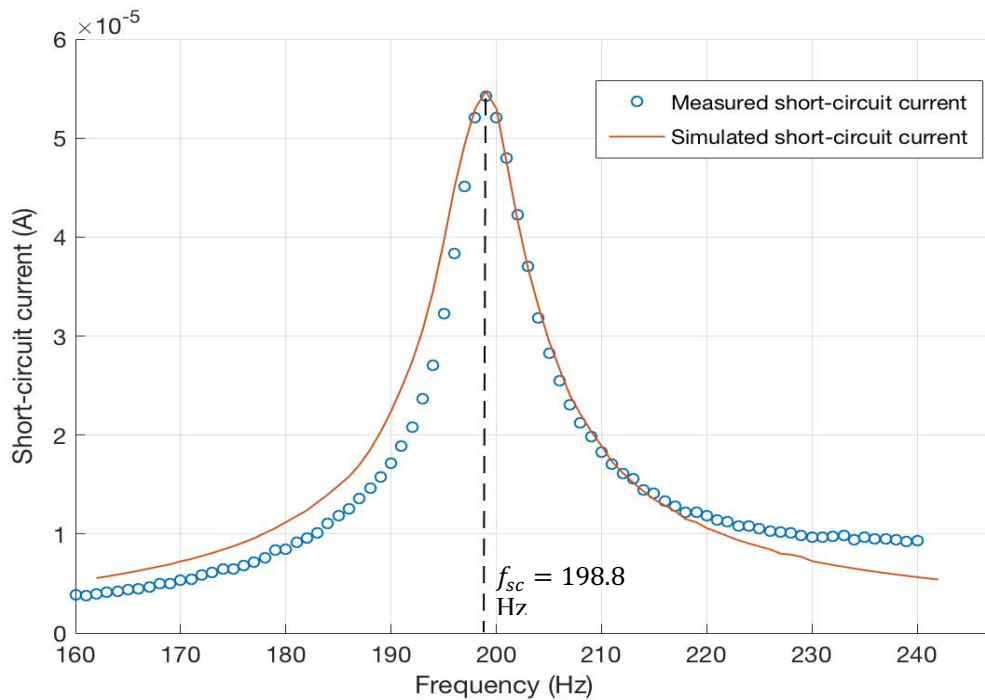
In Figure 2-8, the curve-fit plot aligns well with the measured voltage points close to resonance, but we notice a misalignment at frequencies far from resonance. This misalignment occurs because of the softening of the piezoelectric spring constant ( $K_m$ ) away from resonance.

Nonetheless, since the harvester is subjected to relatively low accelerations, this effect can be ignored [4]. With  $X_1$ ,  $X_2$ , and  $X_3$  found, we have three equations with 5 unknowns. The parasitic capacitance ( $C_e$ ) is measured with the impedance analyzer as  $57.2 \text{ nF}$ . Finally, we can use the short-circuit resonant frequency  $\omega_{sc} = \frac{1}{\sqrt{L_m C}}$  as the final equation. In order to find  $\omega_{sc}$ , we

measure the short-circuit current ( $i_{sc}$ ), while sweeping frequency, using the circuit shown in Figure 2-9. The frequency at which the short-circuit current is maximum is the short circuit resonant frequency. The short-circuit current indicated by  $V_{sense}$  in Figure 2-9 is plotted in Figure 2-10, and the short-circuit resonant frequency is  $f_{sc} = 198.8 \text{ Hz}$ .



**Figure 2-9.** Circuit used to measure short-circuit current ( $i_{sc}$ ). In this circuit  $V_{sense} = i_{sc}R$ .



**Figure 2-10.** Measured and simulated short-circuit current with respect to frequency at  $A = 0.193g$ .

With the parasitic capacitance measured at 57.2 nF, we now have 4-equations with 4-unknowns and can therefore solve for the unknown circuit parameters. The electrical and electromechanical circuit parameters are shown in Table 2-1. To be consistent in my analysis all measurements will be made at a fixed acceleration  $0.193g = 1.893 \text{ m/s}^2$ , unless otherwise specified.

<b>Circuit Parameters</b>	<b>Value</b>	<b>Units</b>
Damping factor <b>B</b>	0.1177	<i>Ns/m</i>
Effective Mass <b>M</b>	$2.252 \times 10^{-3}$	<i>kg</i>
Spring constant <b>K<sub>m</sub></b>	$3513 \text{ Kg/s}^2$	<i>N/m</i>
<b>R</b>	50.48	<i>kΩ</i>
<b>L<sub>m</sub></b>	961.7	<i>H</i>
<b>C</b>	0.6637	<i>nF</i>
Parasitic Capacitance <b>C<sub>e</sub></b>	57.2	<i>nF</i>
Conversion Ratio <b>D</b>	$1.526 \times 10^{-3}$	<i>N/V</i>
Voltage Source <b>V<sub>D</sub></b>	2.794	<i>V</i>
Acceleration <b>A</b>	1.893	<i>m/s<sup>2</sup></i>

**Table 2-1.** Electrical and electromechanical circuit model parameters of for MIDE (PPA-2014).

## 2.4 Chapter Summary

In this chapter, the piezoelectric energy harvester was modelled through a set electrical and mechanical equations from which the electromechanical model was derived. We then introduced the experimental setup, and detailed the process used to experimentally determine the parameters of the PEHD electrical circuit model. These parameters are shown in Table 2-1, and the electrical model is shown in Figure 2-4. With the PEHD electrical circuit model derived, we move on with our analysis to loading the harvester and studying the effects.





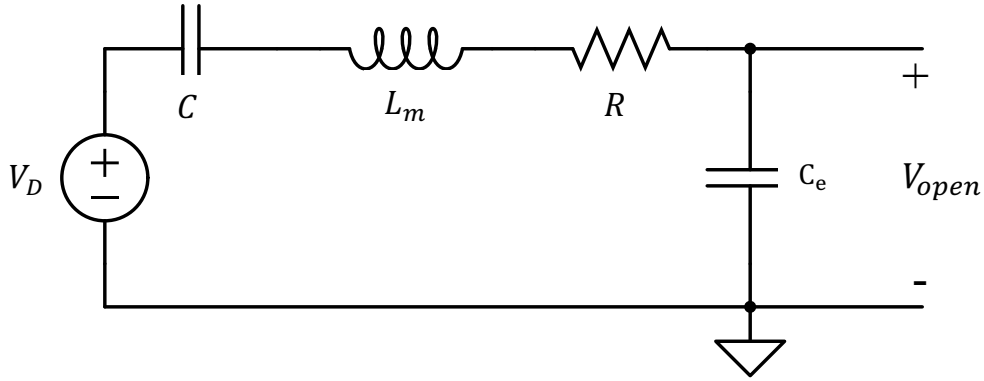
# Chapter 3

## Load Matching

One of the many ways to harvest electrical power is by connecting a passive load at the terminals of the PEHD. In this chapter, the amount of power delivered to different types of passive loads is explored with both actual measurements and calculations. Next, the concept of conjugate matching is introduced, and the maximum theoretical output power is calculated. The maximum theoretical output power will be used throughout the thesis as standard for comparison to other energy harvesting techniques. In order to analyze the power capabilities of the harvester, this chapter first simplifies the PEHD electrical circuit model into a Thevenin equivalent model.

### 3.1 Equivalent PEHD Circuit Characteristics

In Chapter 2, we derived an electrical circuit model for the PEHD, which is repeated here in Figure 3-1. The circuit parameters, derived in Chapter 2, are given in Table 3-1.



**Figure 3-1.** Equivalent electrical circuit model of PEHD harvester.

Electrical Circuit Parameters	Value
$R$	50.48 $K\Omega$
$L_m$	961.7 $H$
$C$	0.6637 $nF$
Parasitic Capacitance $C_e$	$57.2 \times 10^{-9} F$
Conversion Ratio $D$	$1.526 \times 10^{-3} N/V$
Voltage Source $V_D$	2.794 $V$

**Table 3-1.** Electrical model parameters of for MIDE (PPA-2014).

The complex amplitude of the open-circuit voltage ( $V_{open}$ ) can now be found. We assume the system is in sinusoidal steady state, and the voltage source ( $V_D$ ) can be represented as

$$V_D = \Re(\widetilde{V}_D e^{j\omega t}) = \Re(M\tilde{A}/D e^{j\omega t}).$$

$$\widetilde{V}_{\text{open}} = \frac{\widetilde{V}_D / C_e}{j\omega R + 1/C - \omega^2 L_m + 1/C_e} \quad (3.1)$$

The circuit in Figure 4 is characterized by two resonant frequencies: the short-circuit resonant frequency ( $\omega_{sc}$ ), and the open-circuit resonant frequency ( $\omega_o$ ). As implied by their names, the open-circuit and short-circuit resonant frequencies are the frequencies at which the net reactance is zero when the output is opened, and shorted, respectively.

Open-circuit resonant frequency:

$$\frac{1}{j\omega_o C_e} + \frac{1}{j\omega_o C} + j\omega_o L_m = 0$$

$$\omega_o = \sqrt{\frac{1}{L_m C} + \frac{1}{L_m C_e}} = 1256.3 \text{ rad/s}$$

$$f_o = 199.9 \text{ Hz} \quad (3.2)$$

Short-circuit resonant frequency:

$$\frac{1}{j\omega_{sc} L_m} + j\omega_{sc} C_m = 0$$

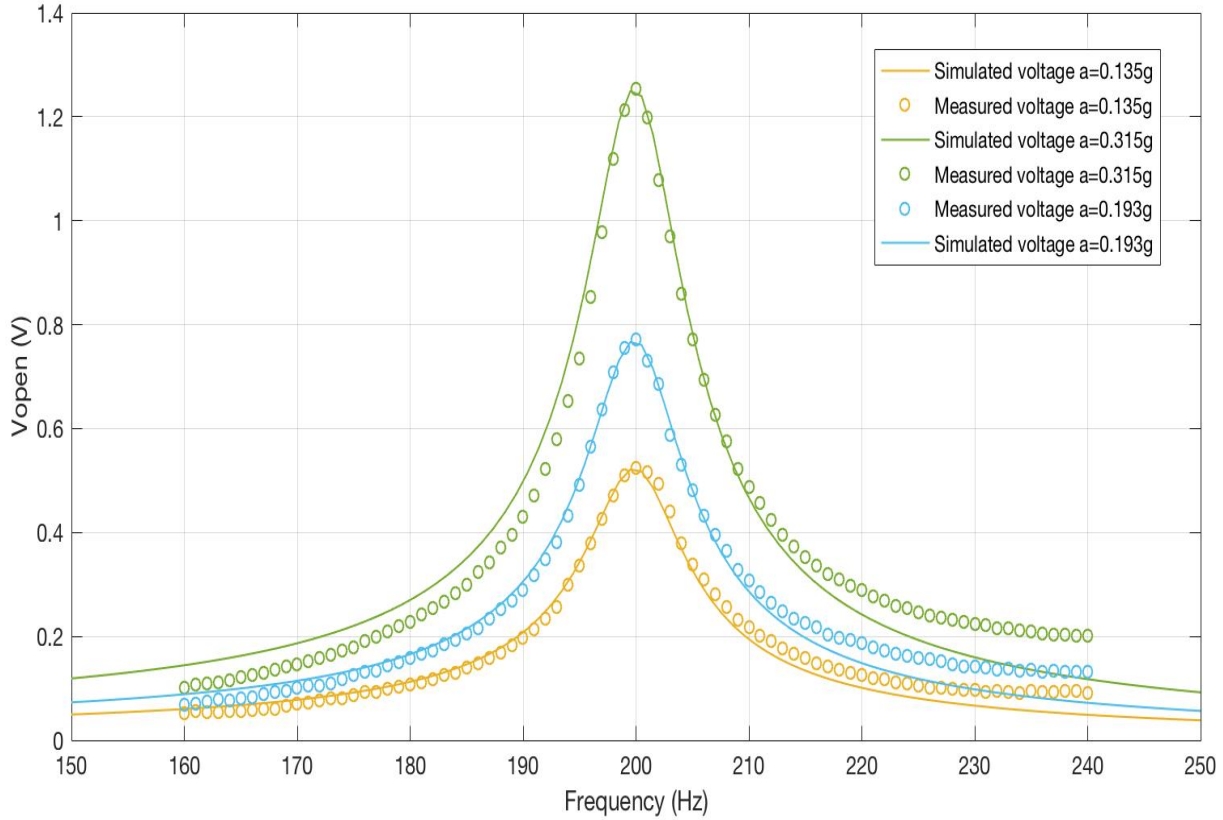
$$\omega_{sc} = \frac{1}{\sqrt{L_m C}} = 1249.1 \text{ rad/s}$$

$$f_{sc} = 198.8 \text{ Hz} \quad (3.3)$$

We expect  $\omega_o$  to always be slightly below  $\omega_{sc}$ . The difference between the two these two frequencies is explained by the coupling constant ( $\rho$ ) such that  $\omega_{oc} = \omega_{sc}(1 + \rho)$  [7]. The coupling constant ( $\rho$ ) depends on the physical parameters of the harvester

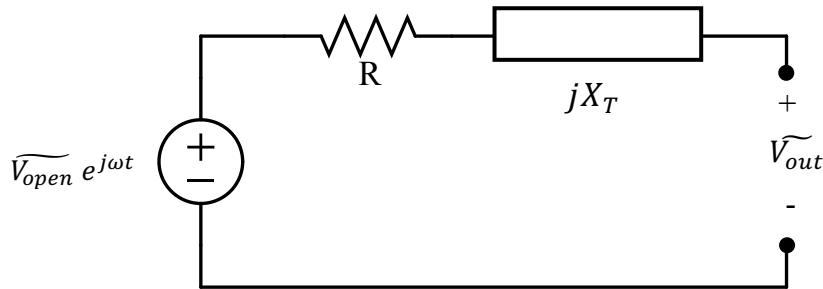
$$\rho = \frac{Y d_{33}^2 / \varepsilon}{1 + Y d_{33}^2 / \varepsilon}, \text{ where the } Y, d_{33}^2, \text{ and } \varepsilon \text{ are given in Section 2.1.}$$

In Figure 3-2, the amplitude of measured open-circuit voltage is proportional to acceleration (A), as predicted by  $\widetilde{V}_{\text{open}}$  in Equation 3.1. For the sake of consistency and in order to make fair comparisons, all future measurements, simulations, and calculations will be made at a constant acceleration of **0.193g**. Also, all simulations are done with LT Spice, and the Spice circuit used in this chapter is shown in A2.2 of the appendix.



**Figure 3-2.** Measured, and simulated open-circuit voltage ( $V_{oc}$ ) as a function of vibration frequency for accelerations: 0.315g, 0.193g, and 0.1g.

Now consider the Thevenin equivalent model of the circuit in Figure 3-1, with the total impedance equal to the sum of the reactance term ( $X_T$ ) and resistance term ( $R_T$ ).

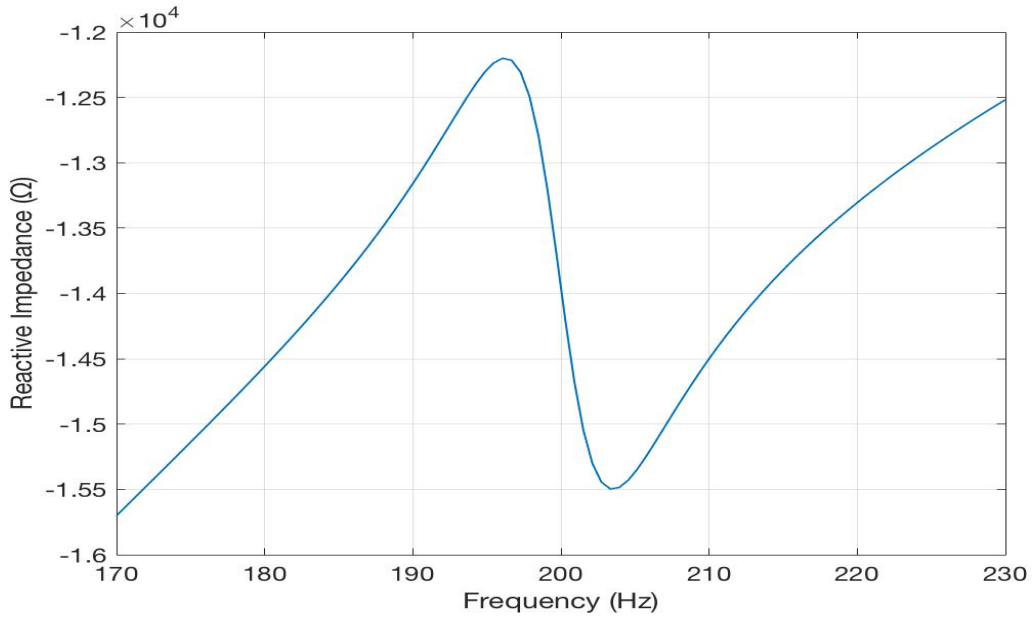


**Figure 3-3.** Thevenin-equivalent circuit model of PEHD.

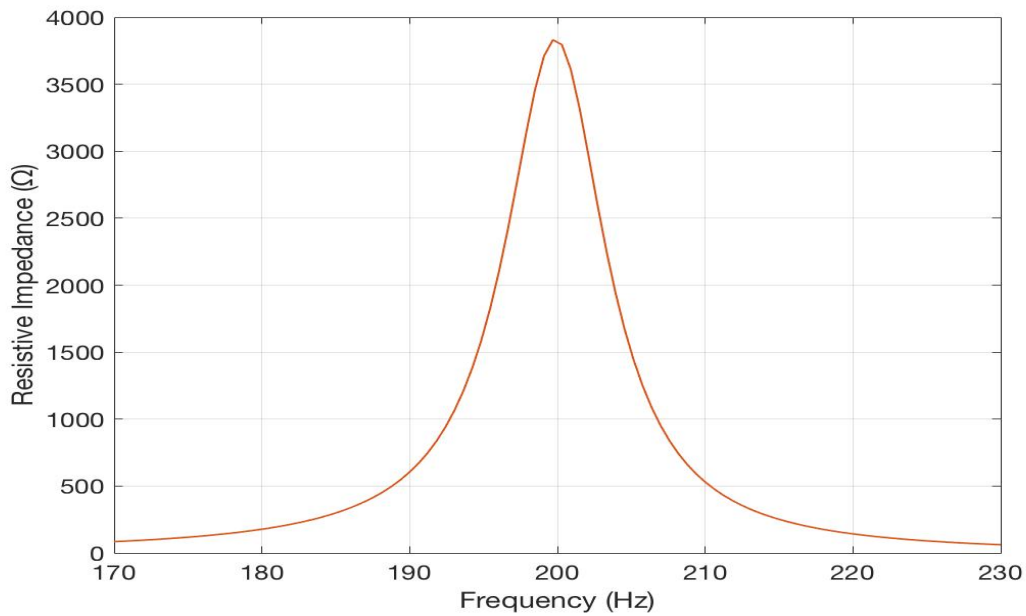
$$R_T = \frac{R/Ce^2}{\left(\frac{1}{C_e} + \frac{1}{C} - \omega^2 L_m\right)^2 + (\omega R)^2} \quad (3.4)$$

$$X_T = \frac{\left(\frac{\omega}{C} - \frac{L_m}{\omega}\right)\left(\frac{1}{C_e} + \frac{1}{C} - \omega^2 L_m\right) + \frac{\omega R^2}{C_e}}{\left(\frac{1}{C_e} + \frac{1}{C} - \omega^2 L_m\right)^2 + (\omega R)^2} \quad (3.5)$$

The imaginary ( $X_T$ ) and real parts ( $R_T$ ) of the Thevenin impedance and are plotted in Figures 3-4 and 3-5, respectively.



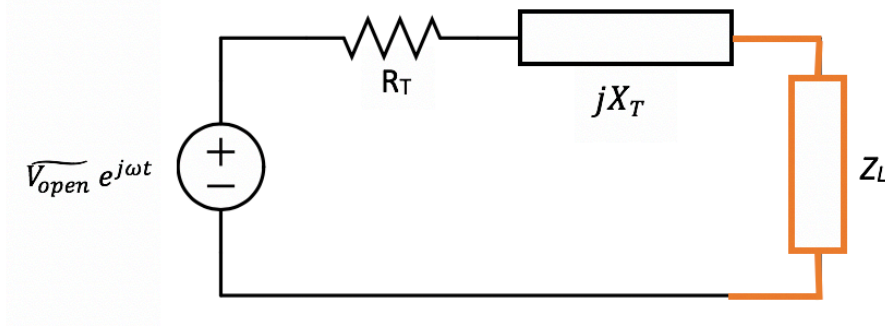
**Figure 3-4.** Reactive part of Thevenin equivalent impedance ( $X_T$ ) with respect to frequency.



**Figure 3-5.** Resistive part of Thevenin equivalent impedance ( $R_T$ ) with respect to frequency.

### 3.2 AC Power Delivered to Load

We start the analysis by examining the power delivered to the load ( $Z_L = R_L + jX_L$ ) shown in Figure 3-6. The real and imaginary parts of  $Z_L$  are  $R_L$  and  $X_L$ .



**Figure 3-6.** Thevenin-equivalent circuit model of PE EHD with load impedance ( $Z_L$ ).

The average power delivered to the load is

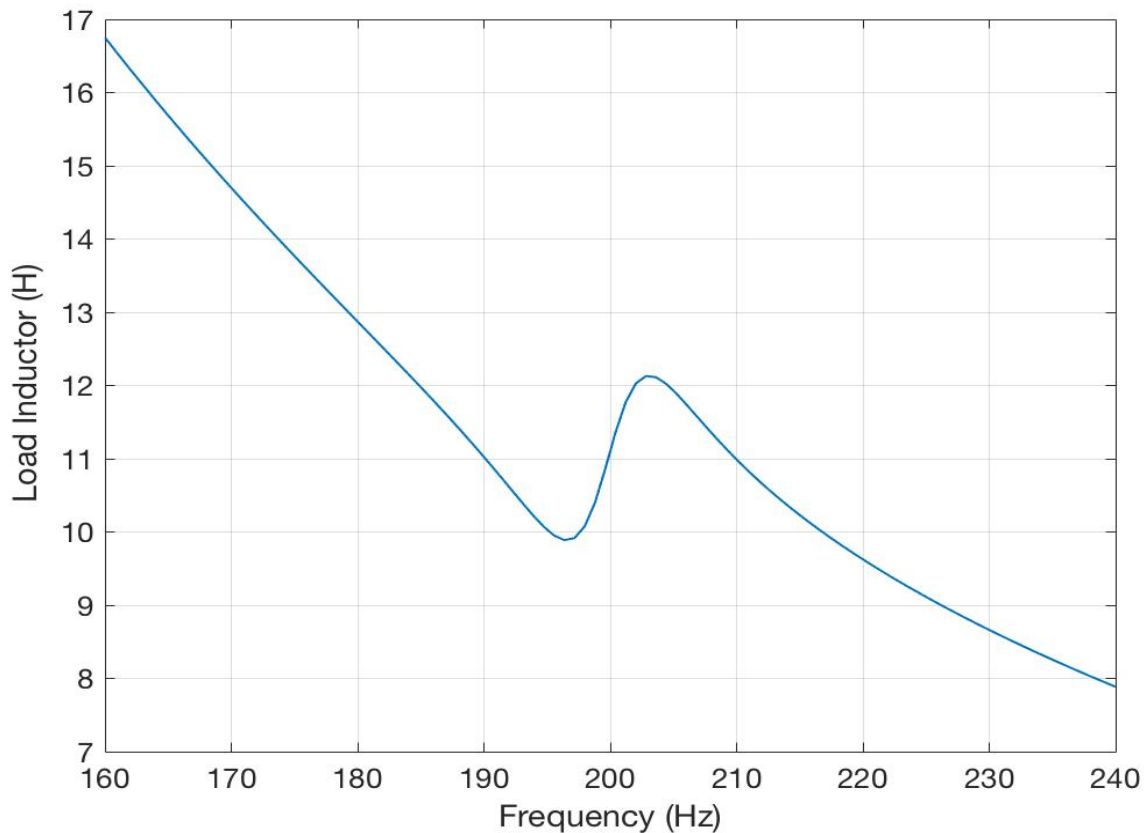
$$\begin{aligned}
 P_{out} &= I_{rms}^2 \times R_L = \left( \frac{|V_{open}|_{rms}}{|R_L + jX_L + R_T + jX_T|} \right)^2 (R_L) \\
 &= \frac{|V_{open}|^2}{(R_L + R_T)^2 + (X_T + X_L)^2} \left( \frac{R_L}{2} \right), \tag{3.6}
 \end{aligned}$$

where  $|V_{open}|_{rms}$  is the root-mean square voltage of  $|V_{open}|$ .

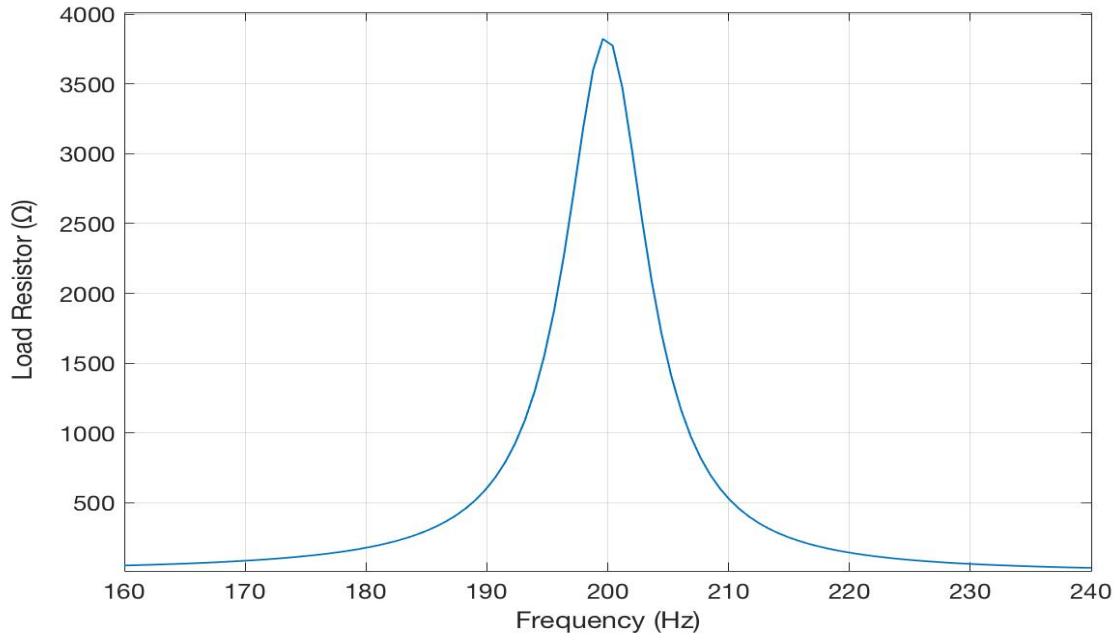
Maximum power is extracted when the load reactance and Thevenin reactance cancel out, and the resistances are equal. In other words,  $R = R_L$  and  $X_L = -X_T$  and conjugate load matching is achieved. Therefore, when the overall reactance is zero, the source vibration frequency is equal to the circuit's resonant frequency, and maximum power is delivered to the load. That said, we would always want to achieve conjugate load matching, or be as close as possible to conjugate load matching. The maximum average power delivered to the load ( $P_{optimal}$ ) is given by

$$P_{optimal} = \frac{1}{8} \left( \frac{|V_{open}|^2}{R_T} \right) = \frac{1}{8} \left( \frac{V_D^2}{R} \right) = 19.29 \mu W. \tag{3.7}$$

$P_{optimal}$  is the maximum theoretical average power that could be delivered to the load when conjugate load matching is implemented. The reactive term of the Thevenin equivalent model in Figure 3-6 is negative (net capacitive), which means the load impedance must comprise of a positive reactance (inductor), so that net reactance is zero. The circuit in Figure 3-9 shows the PEHD's Thevenin equivalent model loaded with an inductor and resistor.  $P_{optimal}$  can be delivered to the load resistor in Figure 3-9 when conjugate load matching is achieved. Figures 3-7 and 3-8 show the required values for the load inductor (L) and resistor ( $R_L$ ) at each frequency in order to attain conjugate load matching.



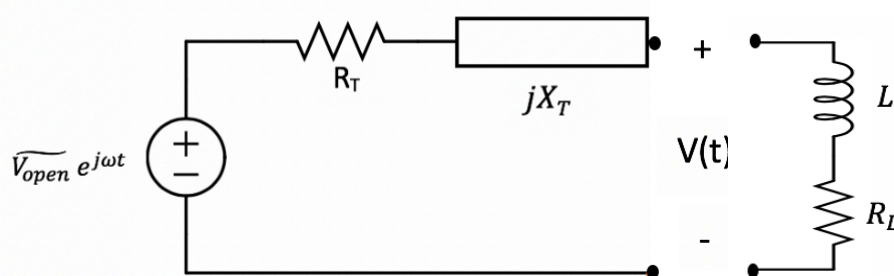
**Figure 3-7.** Load inductor required for conjugate matching.



**Figure 3-8.** Load resistor required for conjugate matching.

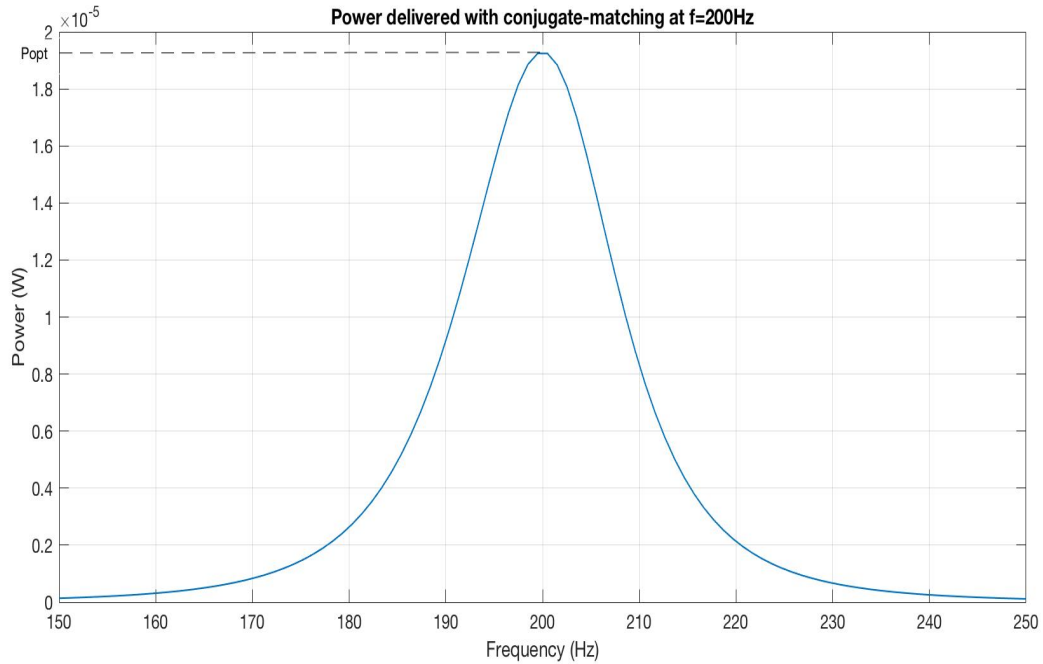
As we can see in the Figure 3-7, the inductor required for conjugate matching across all frequencies is extremely large. This is because of the small (on the order of nano-farads) parasitic capacitor ( $C_e$ ) that must be matched by an inductor at a relatively low frequency. Not only is it impractical to use such a large inductor, but the load inductor and resistor must be tuned at each frequency, to ensure that the conjugate matching condition remains satisfied.

With static load components, the average output power quickly dips as the source vibration frequency deviates away from the frequency at which conjugate matching was achieved. Figure 3-10 shows the power delivered to the load as a function of frequency with conjugate matching established for 200 Hz and 176 Hz, respectively.

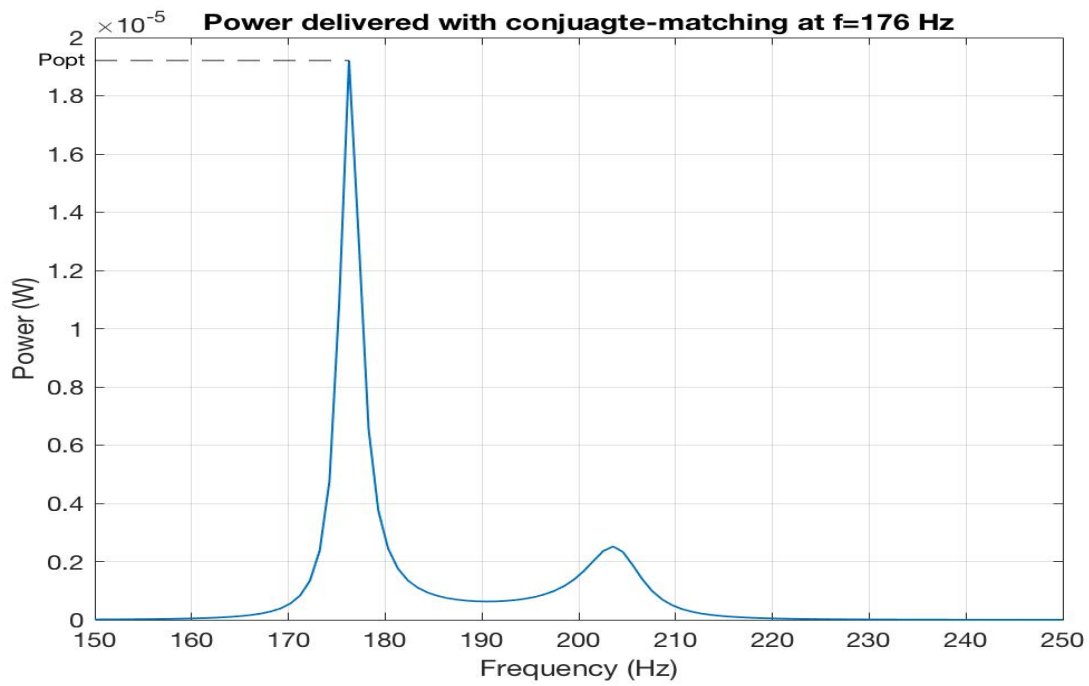


**Figure 3-9.** PEHD equivalent Thevenin model loaded with a series inductor and resistor.





(a)

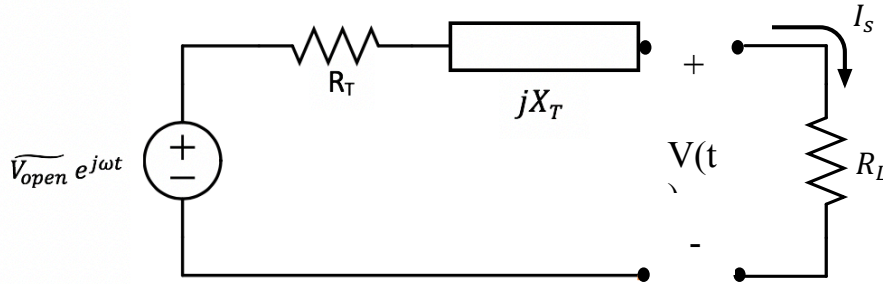


(b)

**Figure 3-10.** Power delivered to the load as function of vibration frequency with conjugate matching achieved at (a)  $f = 200$  Hz with  $Z_L = j(11.1\omega) + 3778$ , and (b)  $f = 176$  Hz with  $Z_L = j(13.52\omega) + 127.7$ .

**Resistive load:**

In the previous Section, we saw that the inductor needed to optimize power is impractically large and therefore cannot be used. In this Section, we will examine the power that can be extracted with a purely resistive load and derive an equation for the optimal resistive load at each frequency, as shown in Figure 3-11.



**Figure 3-11.** Schematic of PEHD circuit model Thevenin equivalent loaded with a resistor.

The power delivered to the resistive load ( $P_{res}$ ) is

$$P_{res} = \frac{V_{open}^2}{2} \frac{R_L}{(R_L + R_T)^2 + (X_T)^2}, \quad (3.8)$$

where the expressions for  $R_T$ ,  $X_T$ , and  $V_{open}$  are shown in (3.4), (3.5), and (3.1), respectively.

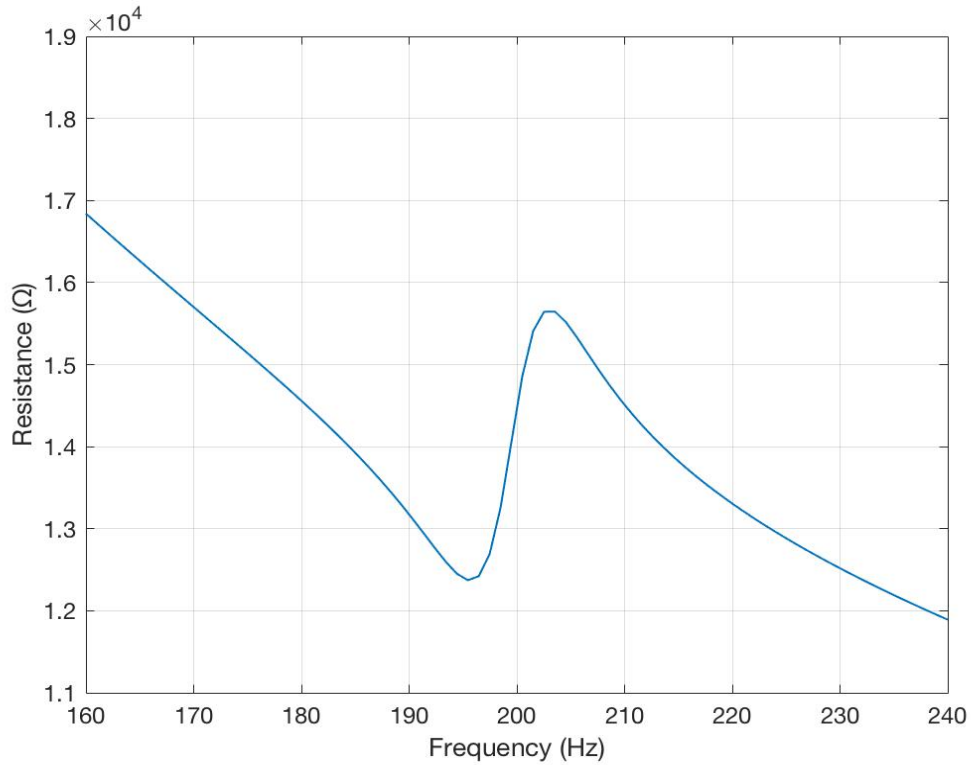
As expected, the maximum power harvested depends on the resistor size. Moreover, the power quickly decreases as we move away from the resonant frequency. In order to find the optimal resistor (with a purely resistive load) at each frequency, I set the first order derivative of  $P_{res}$  (shown in (3.8)) with respect to  $R_L$  to zero to obtain

$$\frac{d}{dR_L} P_{res} = \frac{V_{open}^2}{2} \frac{(R_L + R_T)^2 + X_T^2 - 2R_L(R_L + R_T)}{((R_L + R_T)^2 + X_T^2)^2} = 0.$$

Setting  $\frac{d}{dR_L} P_{res}$  to zero, we obtain the following expression for the optimal load resistance

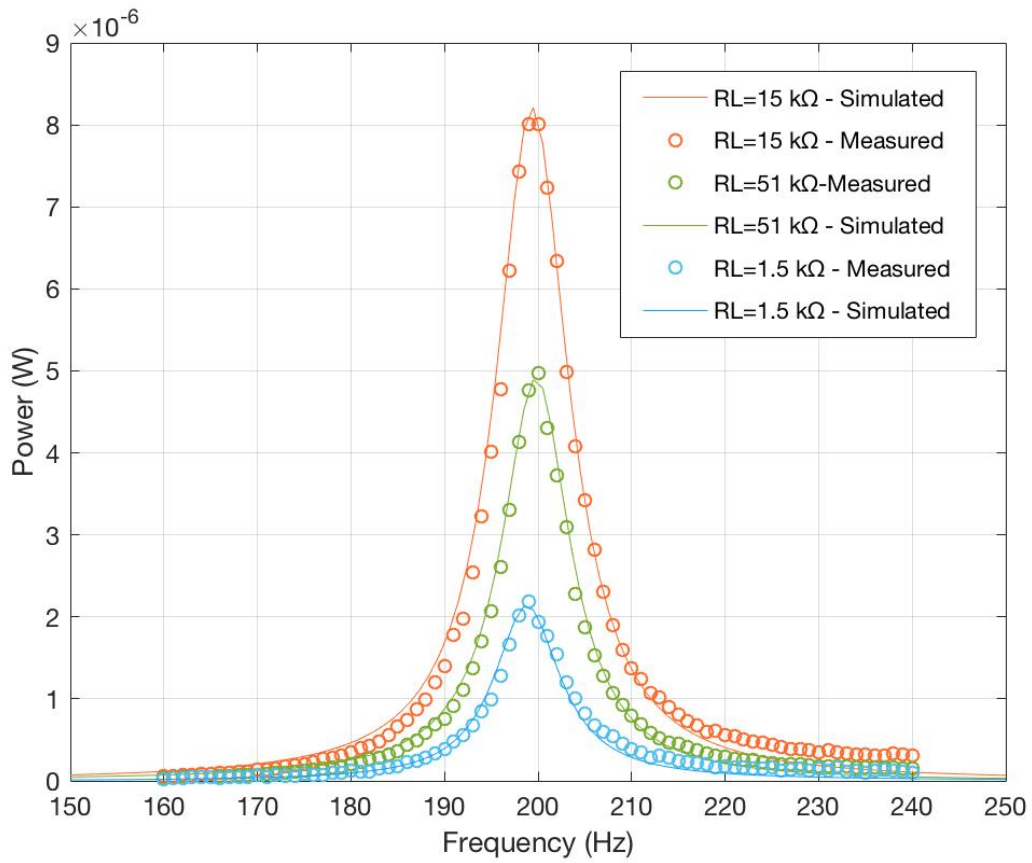
$$R_{L,opt} = \sqrt{R_T^2 + X_T^2}, \quad (3.9)$$

which is plotted in Figure 3-12 with respect to frequency.

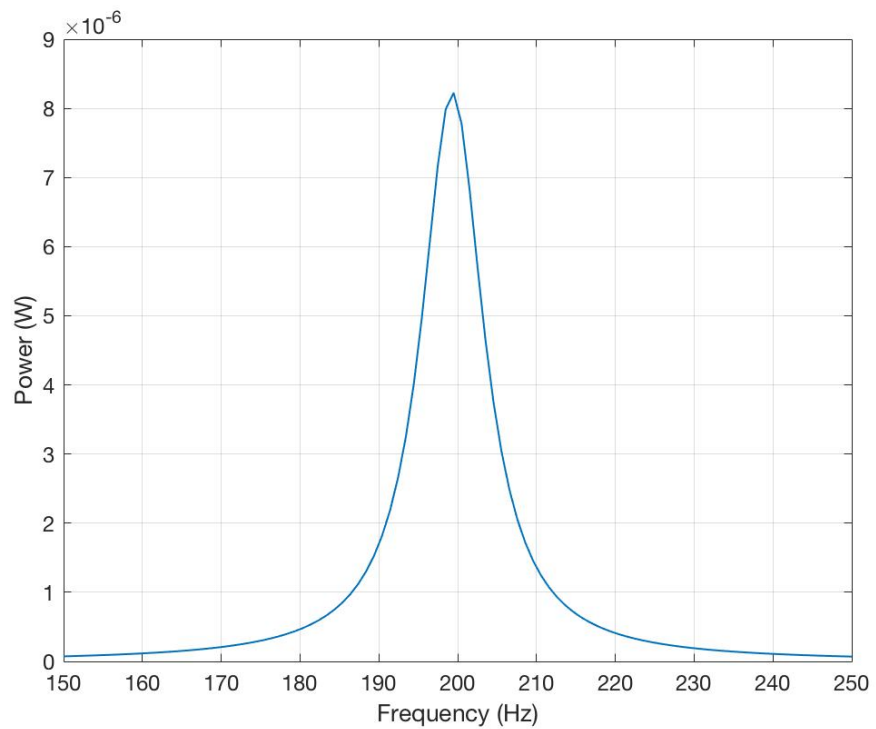


**Figure 3-12.** Optimal resistive load ( $R_{L,opt}$ ) as a function of frequency.

In Figure 3-13, we see that the power into the  $15\text{ k}\Omega$  load resistor is maximum at resonance at around  $8.2\ \mu\text{W}$ . However, this  $15\text{ k}\Omega$  resistor is the optimal for power delivery at only three specific frequencies as shown in Figure 3-12. In order to maximize power delivery at all frequencies with a resistive load  $R_{L,opt}$  must be used. Replacing  $R_{L,opt}$  in the equation 3.8 for resistive power ( $P_{res}$ ), we get the optimal resistive power, which is plotted in Figure 3-14. Of course, this can only be done with a tunable load resistor (power electronics designed to act as a resistor) equal to  $R_{L,opt}$ .



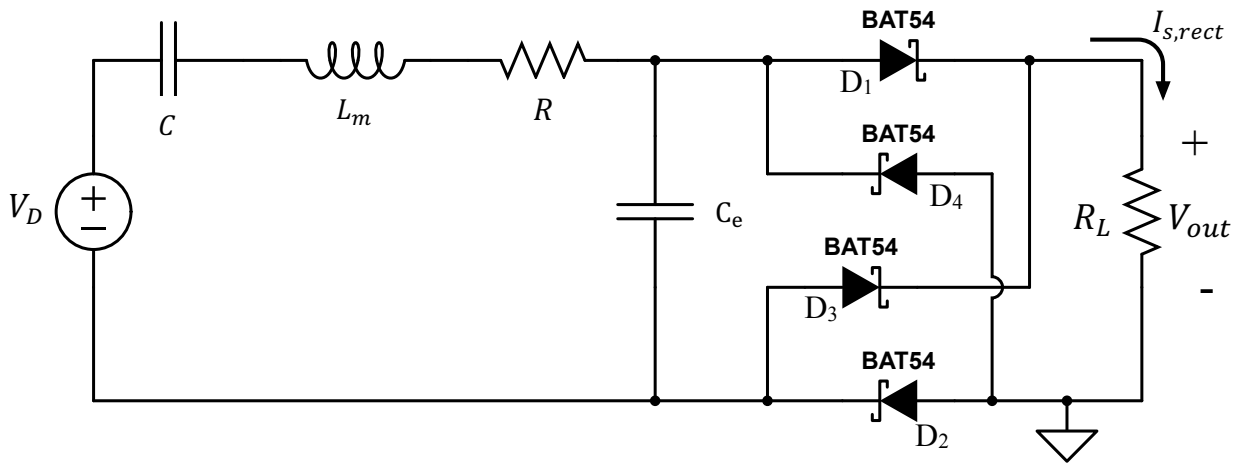
**Figure 3-13.** Measured and simulated output power for different resistors as a function of source vibration frequency.



**Figure 3-14.** Calculated optimal resistive power with respect to frequency.

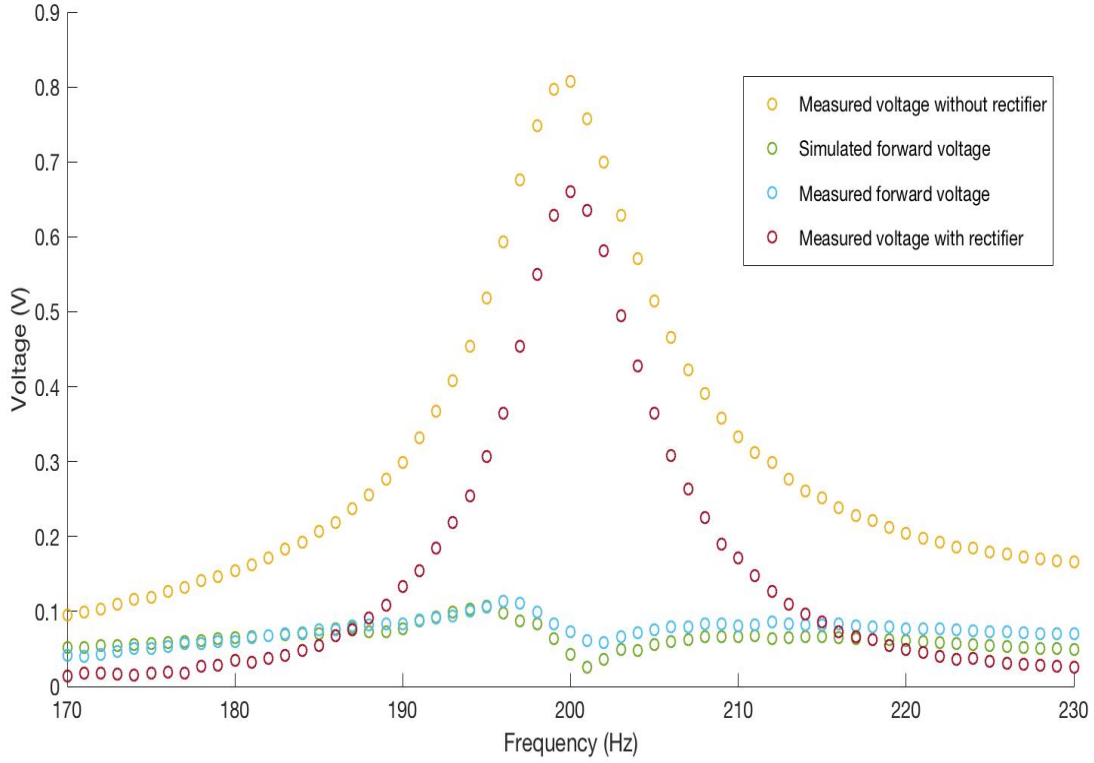
### 3.3 DC Power Delivered to Load

So far, we have discussed AC power being delivered to a resistive load. However, in most energy harvesting applications, we are interested in DC power harvesting. Therefore, the AC voltage must be rectified, so that it could be in DC form at the output stage. Subsequently, the DC voltage can be stored in a battery or super-capacitor. We propose to use a full-bridge rectifier with Schottky diodes (BAT54), as shown in Figure 3-15.



**Figure 3-15.** Schematic of equivalent PEHD model with a full-bridge rectifier and resistive load.

We recall that the voltage source ( $V_D$ ) has a sinusoidal form. During the positive cycle of the sine-wave, diodes  $D_1$  and  $D_2$  are on, while during the negative cycle, diodes  $D_3$  and  $D_4$  are on. Therefore, at any moment in time, two diodes will be on. If the above diodes were ideal (zero forward voltage), then the rectification process would be lossless, and we would expect to get the same power across  $R_L$  as in the previous section. However, the BAT54 diodes have a small forward voltage drop ( $V_f$ ) of around 0.2 V (at 0.1 mA current), so we expect power loss during conduction. In order to determine  $V_f$ , we take the difference between the peak voltage into the load resistor with and without the full-bridge rectifier as shown in Figure 3-16.



**Figure 3-16.** Peak voltage amplitude across  $15\text{ k}\Omega$  load resistor with and without the full-bridge rectifier at a  $0.315g$  acceleration.

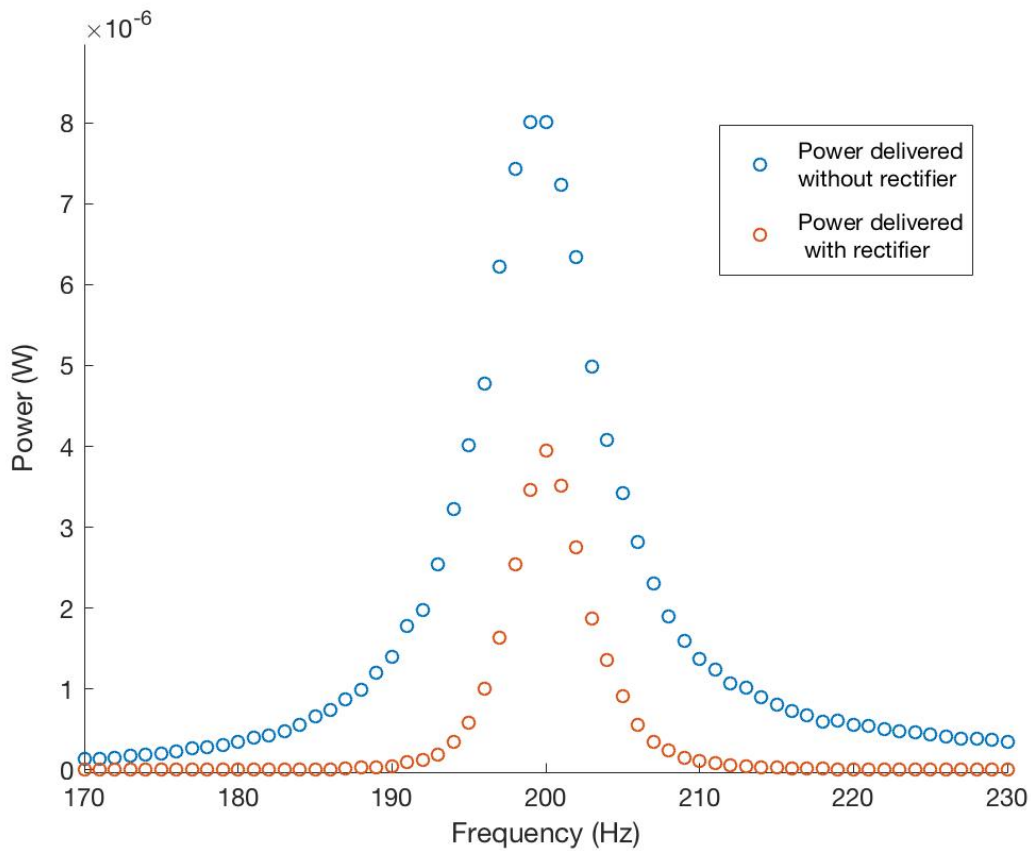
In Figure 3-16, it is clear that the forward voltage drop across the diodes slightly varies with frequency because of changes in the current ( $I_{rect}$ ). Around resonance, the average value for the forward voltage drop ( $V_f$ ) is  $85.1\text{ mV}$ . Assuming  $V_f$  remains constant at  $85.1\text{ mV}$ , we can now approximate the power lost in the rectifier. Each diode goes on for half a cycle, therefore the power dissipated in a single diode per cycle is

$$\begin{aligned}
 P_{loss,diode} &= \frac{1}{2T} \int_0^{T/2} (V_f \times I_{s,rect}) dt \\
 &= \frac{1}{\pi} V_f \int_0^{\pi} \frac{V_{out}}{R_L} \sin(\omega t) d(\omega t) = \frac{2V_f V_{out}}{\pi R_L}
 \end{aligned} \tag{3.10}$$

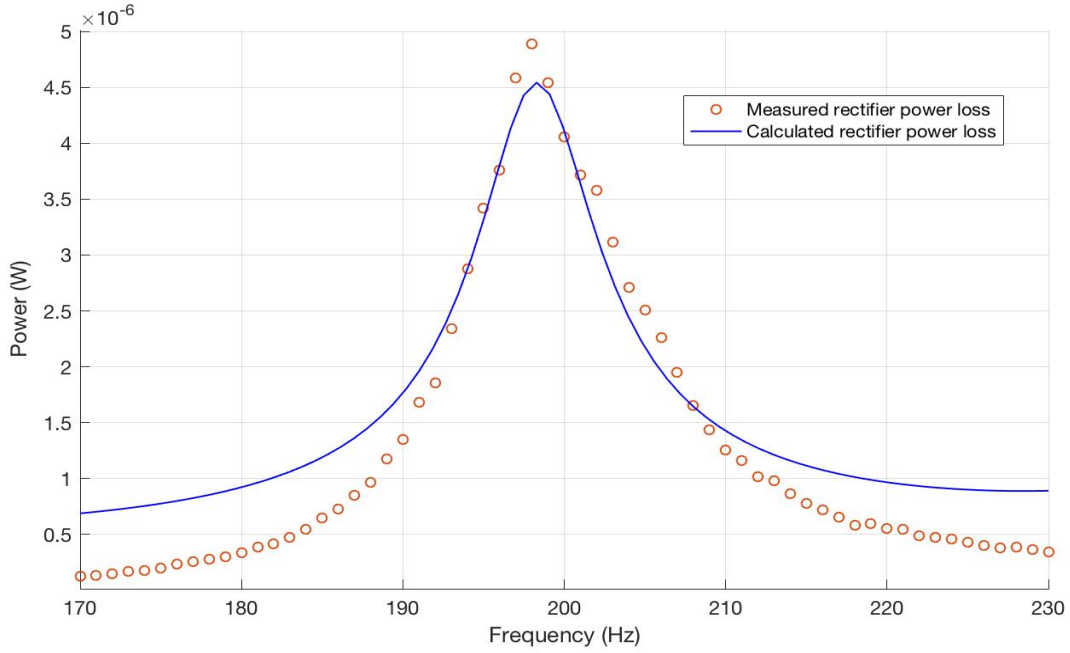
and, the total power loss in the rectifier is 2 times  $P_{loss,diode}$

$$P_{loss,rectifier} = \frac{4V_f V_{out}}{\pi R_L}. \tag{3.11}$$

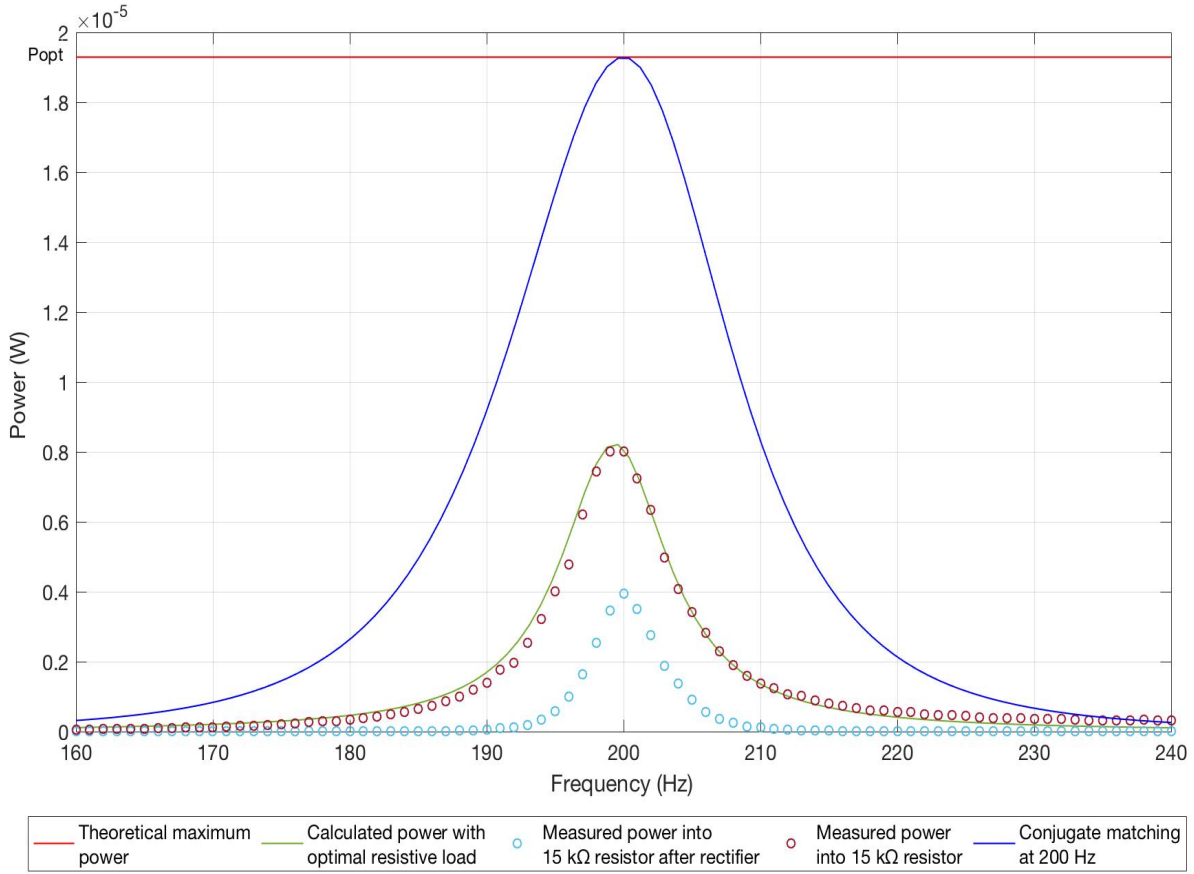
Of course,  $P_{loss,rectifier}$  in (3.11) is only an approximation of the power lost in the bridge rectifier, because  $V_f$  in reality is not constant. Figure 3-17 shows the measured power delivered to the  $15\text{ k}\Omega$  resistor with and without the bridge rectifier, and by subtracting these two terms, we can measure the power lost in the bridge rectifier. In Figure 3-18, the calculated power lost in the bridge rectifier as predicted by (3.11) is plotted alongside the measured rectifier loss. As expected, the power lost in the bridge rectifier is highest at resonance, since the current through the load is at its maximum. Figure 3-19 puts everything so far into perspective. We can see that the bridge rectifier severely degrades the power dissipated in the load. In the next chapter, the Bias-flip method is introduced as a means to improve the amount power harvested at resonance and extend the power bandwidth.



**Figure 3-17.** Measured power delivered to the  $15\text{ k}\Omega$  resistive load with and without the full-bridge rectifier at various frequencies.



**Figure 3-18.** Calculated and measured power loss in rectifier as a function of frequency.



**Figure 3-19.** Measured and calculated power harvested under various conditions as a function of frequency.



### 3.4 Chapter Summary

This chapter explored the power delivery capabilities of the piezoelectric energy harvester electrically loaded with passive components. In order to deliver the maximum theoretical power at a certain frequency, conjugate matching must be implemented. However, with conjugate matching come issues of practicality since the load inductor required is much too large. More importantly, the power bandwidth is extremely narrow, and we see a dramatic dip in power with slight changes in ambient vibration frequency. Unlike conjugate load matching, loading the harvester with a purely resistive load does not have any practicality issues; however, power delivery at all frequencies is much worse, and power bandwidth still suffers. In the last section, the full-bridge rectifier, used to harvest DC power, was introduced. We then moved on to measure forward voltage drop across the rectifier diodes, as well as the power lost in the rectifier. In real world applications, the vibration frequency rarely remains constant; thus, having a broad power bandwidth is extremely favorable, and one of the main motivations behind the bias-flip method, discussed in the next chapter.



# Chapter 4

## Bias-flip Method

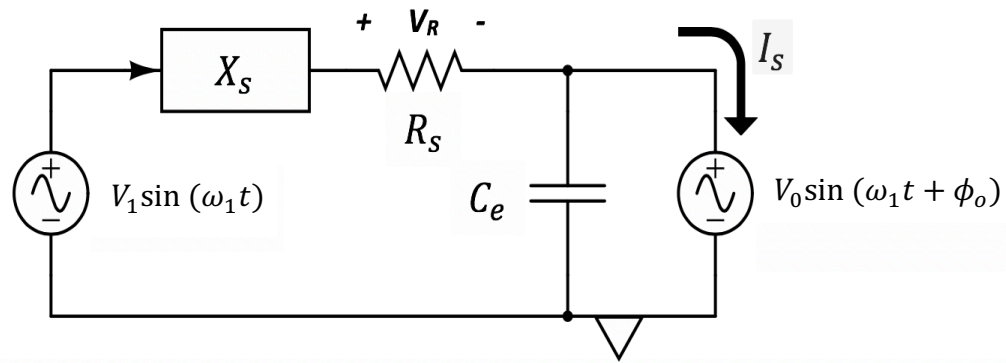
In the previous chapter, it was concluded that a passively loaded piezoelectric energy harvester has an extremely narrow bandwidth, which makes it unfit for harvesting power when the ambient vibration frequency varies or is unknown. Also, manufacturing variations create a challenge even when the source vibration frequency is known. In order to deliver the theoretical maximum power at all frequencies, we would need a tunable inductor and resistor for conjugate load matching, which is highly impractical. With the bias-flip technique, however, we can synthesize a reactive and resistive load impedance and come very close to conjugate matching [3]. The bias-flip circuit comprises of a small inductor in series with a switch, which when controlled correctly, can mimic the behavior of a much larger tunable inductor in series with a resistor [10]. In fact, it will be proven in this chapter that with a lossless or ideal bias-flip circuit approximately the theoretical maximum power can be harvested at all frequencies. Even with a lossy (non-ideal) bias-flip circuit, simulations show that output power before rectification can be improved by  $\sim 1.6x$  at resonance, and  $\sim 4.8x$  at 10 Hz away from resonance, when compared to the power harvested with a purely resistive load. Lastly, from a practicality standpoint, the bias-flip method is fit for ultra-low power applications and occupies a very small footprint [8].

## 4.1 Explaining the Bias-flip Method

The goal of this section is analytically explain how the bias-flip method works, and the extent to which power delivery and bandwidth can be improved.

### 4.1.1 Maximizing Power Delivery with Sine-wave

In order to explain how the bias-flip method works, it's worth taking a step back and examining the circuit in Figure 4-1.



**Figure 4-1.** Equivalent PEHD circuit model with sine-wave voltage generator connected at the output.

In the above circuit, we rename the components of Figure 4 to simplify the analysis.

$$X_S = \omega_1 L_m - \frac{1}{\omega_1 C} \quad ; \quad R_S = R \quad ; \quad V_1 = V_D$$

As we can see, a sinusoidal voltage generator with amplitude  $V_o$ , frequency  $\omega_1$ , and phase shift ( $\phi_o$ ) relative to the input voltage source is connected at the output of the circuit.

We would like to find the optimal  $\phi_o$ , and  $V_o$ , such that the average power ( $\langle P_o \rangle$ ) delivered to the output voltage source is maximized. In order for  $\langle P_o \rangle$  to be non-negative the frequencies of the two voltage sine-wave sources must be equal. At different frequencies, the terms  $\sin(\omega_1 t + \phi_x)$  and  $\sin(\omega_o t + \phi_o)$  are orthogonal. We also know that the current into the parasitic capacitor  $C_e$  is  $90^\circ$  out of phase with the output voltage  $V_o \sin(\omega_1 t + \phi_o)$ , and can therefore be ignored in the calculation of the average power.

Therefore, the average power ( $\langle P_o \rangle$ ) delivered to the output voltage source is calculated as

$$\langle P_o \rangle = \frac{1}{2} \Re\{\tilde{V}_o e^{j\phi_o} * \tilde{I}_s^*\}. \quad (4.0)$$

The complex current  $\tilde{I}_s$  is calculated as

$$\tilde{I}_s = \frac{\tilde{V}_1 - \tilde{V}_o e^{j\phi_o}}{jX_s + R_s} - \tilde{V}_o e^{j\phi_o} (j\omega_1 C_e).$$

Replacing  $\tilde{I}_s$  in (4.0), we get the following expression for average power delivered to the output source

$$\langle P_o \rangle = \frac{V_o}{2\sqrt{X_s^2 + R_s^2}} [V_1 \cos(\phi_X - \phi_o) - V_o \cos(\phi_X)],$$

$$\text{where } \phi_X = \arctan\left(\frac{X_s}{R_s}\right) = \arctan\left(\frac{\omega_1 L_m - \frac{1}{\omega_1 C}}{R}\right) \quad (4.1)$$

By simple observation, we notice  $\langle P_o \rangle$  is maximized when  $\phi_o = \phi_X$ . Replacing the optimal phase shift  $\phi_o$ , we get the following equation for average power

$$\langle P_o \rangle = \frac{V_o}{2\sqrt{X_s^2 + R_s^2}} [V_1 - V_o \cos(\phi_X)]. \quad (4.2)$$

Now to determine the optimal amplitude  $V_o$ , take the first order derivative of  $\langle P_o \rangle$  with respect to  $V_o$ .

$$\frac{d\langle P_o \rangle}{dV_o} = \frac{V_1}{2\sqrt{X_s^2 + R_s^2}} - \frac{V_o}{\sqrt{X_s^2 + R_s^2}} \cos(\phi_X) = 0$$

Therefore, the optimal amplitude is 
$$V_o = \frac{V_1}{2\cos(\phi_X)} = V_1 \frac{\sqrt{X_s^2 + R_s^2}}{2R_s}, \quad (4.3)$$

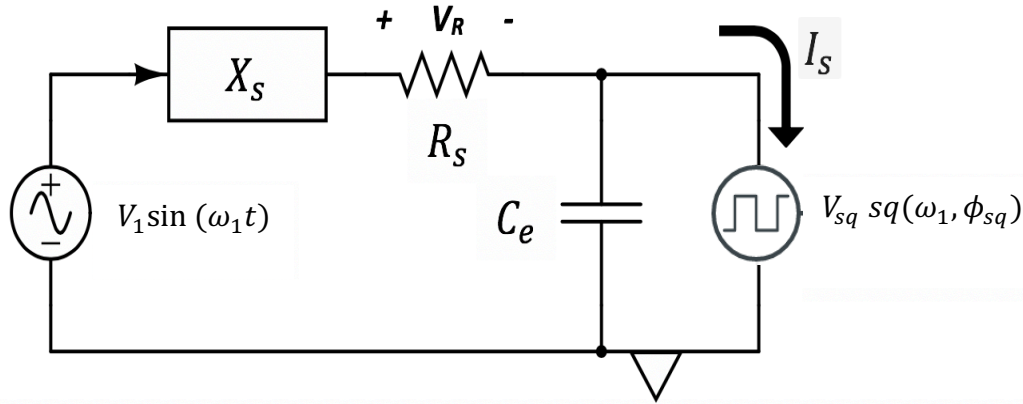
where  $\cos(\phi_X) = \frac{R_s}{\sqrt{X_s^2 + R_s^2}}$ . Replacing the optimal amplitude, frequency and phase shift into the Equation (4.2) for average power we get

$$\langle P_o \rangle_{\max} = \frac{V_1^2}{8\cos(\phi_X)\sqrt{X_s^2 + R_s^2}} = \frac{V_D^2}{8R}. \quad (4.4)$$

This is exactly the same as the theoretical maximum power result we got by replacing the optimal load impedance in Equation 3.7. In other words the voltage source behaves as a conjugate matched load [3].

#### 4.1.2 Maximizing Power Delivery with Square-wave

Now, we move one step further in the analysis and replace the output sine wave  $V_o$  in Figure 4-1 with a square wave  $V_{sq}$  as shown in Figure 4-2. The square-wave closely resembles the output waveform created by the bias-flip circuit, which will be introduced in Section 4.2.



**Figure 4-2.** Equivalent PEHD circuit model with square-wave voltage generator connected at the output.

In the above circuit, the square wave generator  $V_{sq} sq(\omega_1, \phi_{sq})$  has an amplitude of  $V_{sq}$ , frequency of  $\omega_1$  and phase shift with respect to input voltage source of  $\phi_{sq}$ . We will now find the values for  $V_{sq}$ , and  $\phi_{sq}$  that maximize the average power delivered to the output as done in the previous section. The average power as before is given by

$$\langle P_{sq} \rangle = \frac{1}{2} \Re \{ \widetilde{V}_{sq} e^{j\phi_{sq}} * \widetilde{I}_S^* \}. \quad (4.4)$$

We recall that a square wave can be decomposed into its Fourier series, which consists of an infinite combination of sine waves at various amplitudes and frequencies. Specifically, the

square wave is equal to a sine wave at the same frequency (the fundamental), plus an infinite number of odd-multiple sine wave harmonics, each decreasing in amplitude by a factor of  $1/n$ , where  $n$  is an odd integer [3].

Square wave Fourier series:

$$V_{sq}sq(\omega_{sq}, \phi_{sq}) = \frac{4V_{sq}}{\pi} \sin(\omega_{sq}t + \phi_{sq}) + \frac{4V_{sq}}{3\pi} \sin(3\omega_{sq}t + \phi_{sq}) + \frac{4V_{sq}}{5\pi} \sin(5\omega_{sq}t + \phi_{sq}) + \dots$$

$$V_{sq}sq(\omega_{sq}, \phi_{sq}) = \underbrace{\frac{4V_{sq}}{\pi} \sin(\omega_{sq}t + \phi_{sq})}_{\text{Fundamental Term}} + \underbrace{\frac{4V_{sq}}{\pi} \sum_{n=3}^{\infty} \text{odd}(1/n) \sin(n\omega_{sq}t + \phi_{sq})}_{\text{Odd-Harmonics}}$$

As we saw earlier, the average power ( $\langle P_o \rangle$ ) is positive only when frequency of the input and the output periodic signals are equal. This means only the fundamental term (at frequency  $\omega_1$ ) contributes to positive average power, while all the other harmonics are orthogonal to  $\sin(\omega_1t + \phi_x)$ . Consequently, the odd-harmonics will cause the average power to decrease. That said, we can now find the average power in two steps. In the first step, we find the average power contributed by the fundamental term. In the second step, we find the average power contributed by the odd-harmonics. We then take the sum of the two quantities to find the total power.

1. Average power contributed by the fundamental ( $\langle P_o \rangle_f$ ):

$$\langle P_{sq} \rangle_f = \frac{1}{2} \Re \left\{ \frac{4}{\pi} \tilde{V}_{sq} e^{j\phi_{sq}} * \tilde{I}_{s,f}^* \right\},$$

$$\text{where } \tilde{I}_{s,f} = \frac{\tilde{V}_1 - \frac{4}{\pi} \tilde{V}_{sq} e^{j\phi_{sq}}}{jX_s + R_s} - \frac{4}{\pi} \tilde{V}_{sq} e^{j\phi_{sq}} (j\omega_1 C_e).$$

Replacing  $\tilde{I}_{s,f}$  in  $\langle P_{sq} \rangle_f$  we get (4.6)

$$\langle P_{sq} \rangle_f = \frac{2}{\pi} \frac{V_{sq}}{\sqrt{X_s^2 + R_s^2}} \left( V_1 \cos(\phi_x - \phi_{sq}) - \frac{4}{\pi} V_{sq} \frac{R_s}{X_s^2 + R_s^2} \right),$$

where  $X_s = \omega_1 L_m - \frac{1}{\omega_1 C}$ . We notice that the current into the parasitic capacitor is  $\frac{\pi}{2}$  out of phase with fundamental, and therefore gets cancelled out.

2. Average power contributed by all the odd-harmonics ( $\langle P_o \rangle_{hamonics}$ ):

Since all the other odd-harmonics (3<sup>rd</sup> harmonic and above) are at frequencies greater than  $\omega_1$ , they are orthogonal to each other and to the input voltage source. Therefore, we can calculate the average harmonic power as

$$\begin{aligned} \langle P_{sq} \rangle_{hamonics} &= \frac{-V_{sq}^2}{2} \left[ \left( \frac{4}{3\pi} \right)^2 \frac{R_s}{X_{s,3}^2 + R_s^2} + \left( \frac{4}{5\pi} \right)^2 \frac{R_s}{X_{s,5}^2 + R_s^2} + \left( \frac{4}{7\pi} \right)^2 \frac{R_s}{X_{s,7}^2 + R_s^2} + \dots \right] \\ &= -\frac{8 V_{sq}^2}{\pi^2} \sum_{n=3 \text{ odd}}^{\infty} \frac{1}{n^2} \frac{R_s}{X_{s,n}^2 + R_s^2} \end{aligned} \quad (4.7)$$

where  $X_{s,n} = jn\omega_1 L_m + \frac{1}{jn\omega_1 C}$  and n is odd.

Now we can find the total average power:

$$\langle P_{sq} \rangle = \langle P_{sq} \rangle_f + \langle P_{sq} \rangle_{hamonics} \quad (4.8)$$

$$= \frac{2}{\pi} \frac{V_{sq} V_1}{\sqrt{X_s^2 + R_s^2}} \cos(\phi_X - \phi_{sq}) - \frac{8 V_{sq}^2}{\pi^2} \sum_{n=1 \text{ odd}}^{\infty} \frac{1}{n^2} \frac{R_s}{X_{s,n}^2 + R_s^2} \quad (4.9)$$

The first term in (4.9) is the power delivered by the fundamental sine-wave, while the second term sums the power lost in all infinite odd-harmonics. The power lost in the first two odd-harmonics (n=1 and n=3) are computed at three distinct frequencies: 170 Hz, 200 Hz, and 230 Hz. The results are shown in Table 4-1.

nth-Harmonic	Power lost ( $\mu\text{W}$ ) * $V_{sq}^2$		
	170 Hz	200 Hz	230 Hz
n = 1	0.273	2.39	0.332
n = 3	$6.66 \times 10^{-4}$	$4.37 \times 10^{-4}$	$3.11 \times 10^{-4}$
Relative magnitude	410	5470	1067

**Table 4-1.** Power lost in the first two odd-harmonics (n=1 and n=3) at three frequencies: 170 Hz, 200Hz, and 230 Hz. The last term is the relative magnitude of the 1<sup>st</sup> harmonic to 3<sup>rd</sup> harmonic.



As made evident in Table 4-1, the 1<sup>st</sup> harmonic is around three orders of magnitude larger than the 3<sup>rd</sup> harmonic thorough the frequency range of interest ( $\pm 30$  Hz from resonance).

This massive difference in magnitude can be explained by two simultaneous effects taking place. The first is the bandpass filtering effect of the resonator, which strongly attenuates the higher order harmonics. The second source of attenuation is the  $1/n^2$  factor that multiplies each odd-harmonic. Both of these effects cause higher-order harmonics to be attenuated more strongly. Hence, we can consider the power lost in the first harmonic, ignoring all the other higher-order harmonics. Rewriting (4.9) to reflect this approximation we get

$$\langle P_{sq} \rangle \approx \frac{2}{\pi} \frac{V_{sq} V_1}{\sqrt{X_s^2 + R_s^2}} \cos(\phi_X - \phi_{sq}) - \frac{8 V_{sq}^2}{\pi^2} \frac{R_s}{X_s^2 + R_s^2}. \quad (4.10)$$

Apart from the amplitude scaling factor and the  $\pi/2$  phase shift, Equations 4.10 and 4.2 are exactly identical. Taking the first order derivative of  $\langle P_{sq} \rangle$  with respect to  $V_{sq}$ , the optimal amplitude is calculated, and shown in (4.12).

The optimal phase difference ( $\phi_{sq,opt}$ ), and amplitude ( $V_{sq,opt}$ ) are

$$\phi_{sq,opt} = \phi_X = \arctan\left(\frac{\omega L_m - 1/\omega C}{R}\right) \quad (4.11)$$

$$V_{sq,opt} = V_1 \frac{\pi \sqrt{X_s^2 + R_s^2}}{8R_s} = \frac{\pi V_D}{8R} \sqrt{(\omega L_m - 1/\omega C)^2 + R^2}. \quad (4.12)$$

In (4.11) and (4.12)  $\omega$  is the ambient vibration frequency. We can now replace  $\phi_{sq,opt}$ , and  $V_{sq,opt}$  in (4.10) to find the maximum average power

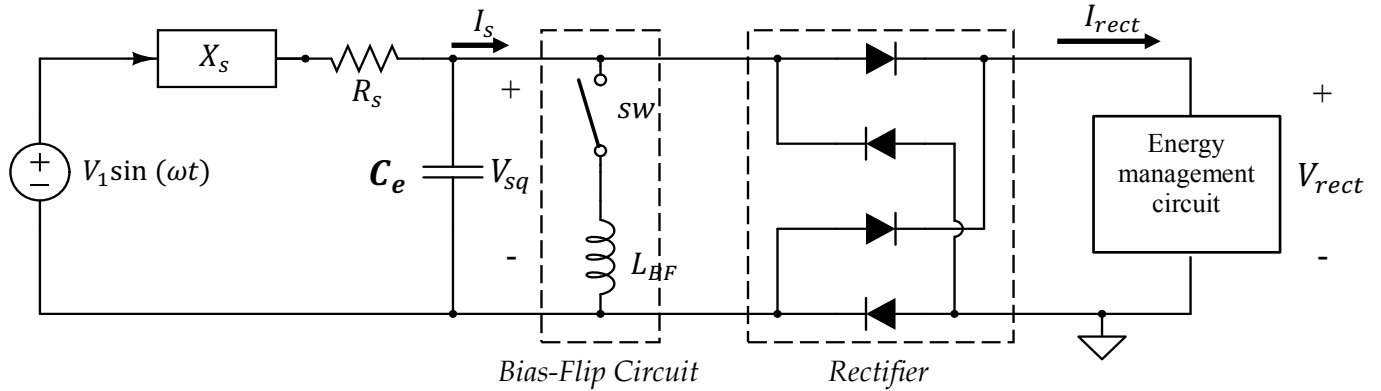
$$\langle P_{sq} \rangle_{max} = \frac{V_1^2}{8R_s} = \frac{V_D^2}{8R}. \quad (4.13)$$

Due to the filtering effect of the harvester, and the  $1/n^2$  attenuation factor of its higher harmonics, the square-wave is capable of achieving an almost perfect conjugate matched load.

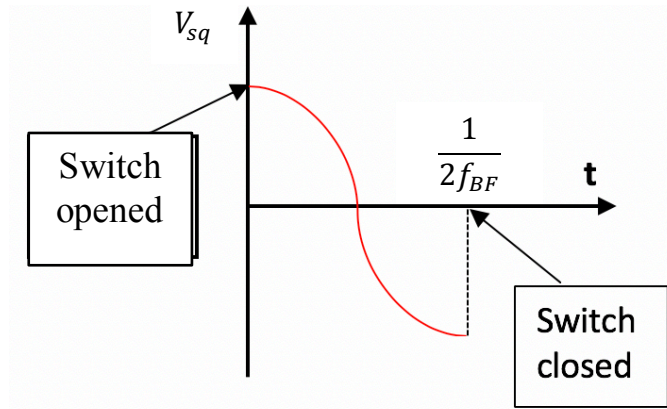
Therefore,  $\langle P_{sq} \rangle_{max}$  is approximately equal to the theoretical maximum power ( $P_{optimal} = \frac{V_D^2}{8R}$ ).

## 4.2 Implementing the Bias-flip Circuit

The circuit in Figure 4-3 shown below is the simplified bias-flip circuit.



(a)



(b)

**Figure 4-3.** (a) Equivalent PEHD model with Bias-flip circuit. (b) Voltage across  $C_e$  during switching.

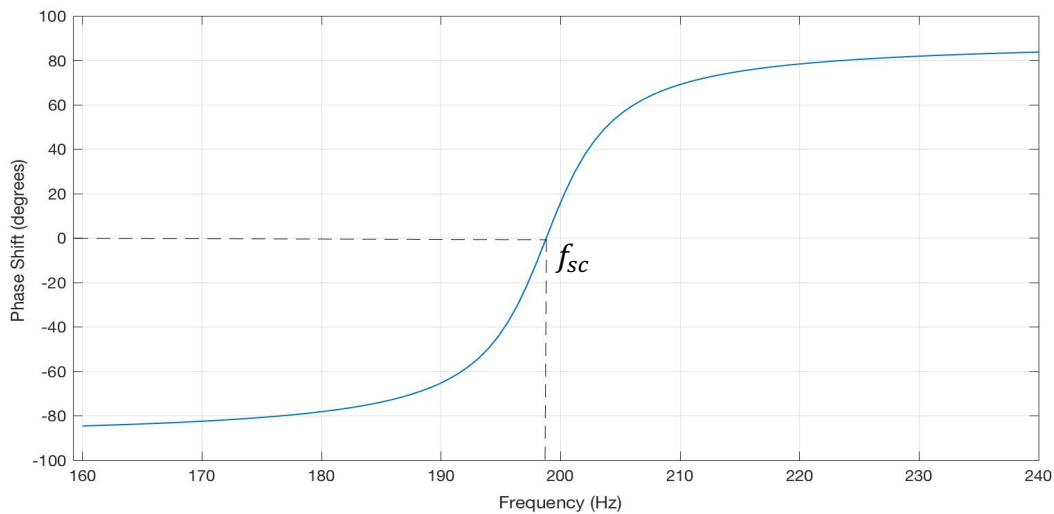
The Bias-flip circuit simply comprises of a switch and small inductor, which allows us to very quickly flip the voltage polarity across the capacitor ( $C_e$ ), in this way a near perfect square-wave can be created across the capacitor  $C_e$  [10]. In Section 2,  $C_e$  was measured as  $57.2 \text{ nF}$ ; therefore, we can achieve a bias-flip oscillation frequency ( $f_{BF}$ ) on the order of  $10 \text{ kHz}$  by choosing a reasonably sized inductor  $L_{BF}$ . This puts  $f_{BF}$  at around 100 times the source vibration frequency

( $\omega$ ). Because  $f_{BF}$  is much greater than the ambient vibration frequency, as soon as the switch closes,  $C_e$  oscillates with  $L_{BF}$  at a  $f_{BF} = \frac{1}{2\pi\sqrt{L_{BF}C_e}}$ , and we can switch the voltage polarity across the parasitic capacitor to approximate a square-wave. The Bias-flip method involves charging and discharging the parasitic capacitor at the right time in order to create an approximate voltage square-wave across  $C_e$  with the optimal phase, and amplitude for max power delivery.

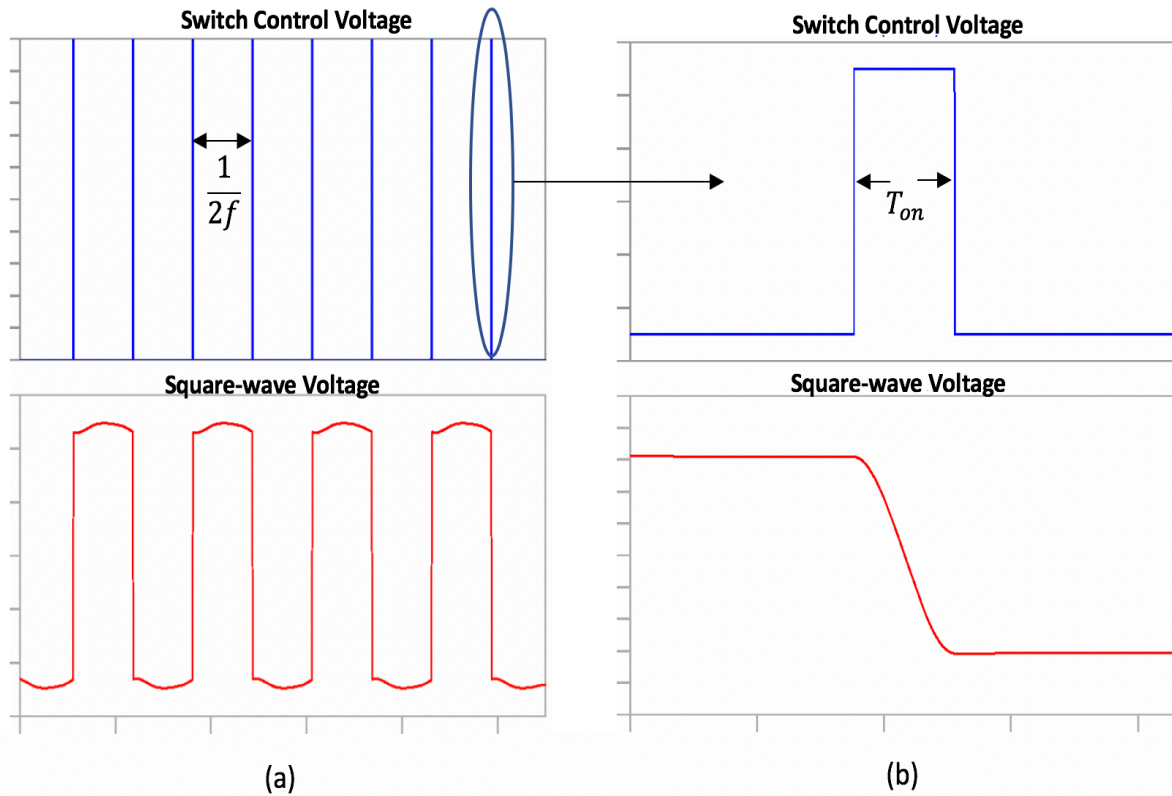
### 4.2.1 Optimal Phase Shift

In order to flip the voltage polarity (180-degrees phase shift) across the parasitic capacitor ( $C_e$ ), the bias-flip tank must oscillate for half a period. Therefore, the bias-flip switch in Figure 4-3 (a) must turn on for  $T_{on} = \pi\sqrt{L_{BF}C_e}$  seconds. Furthermore, in order for the frequency of the square wave to match that of the vibrating source, the bias-flip switch must turn on twice per period.

Figure 4-5 shows the operation of the bias-flip switch, as well as the square wave voltage generated. Now that we have figured out the switching duration and frequency, we move on to implement the optimal phase shift ( $\phi_{sq,opt}$ ) with respect to the input voltage source, found in the previous section. In in Figure 4-4, near short-circuit resonance ( $f_{sc}$ ), the optimal phase shift



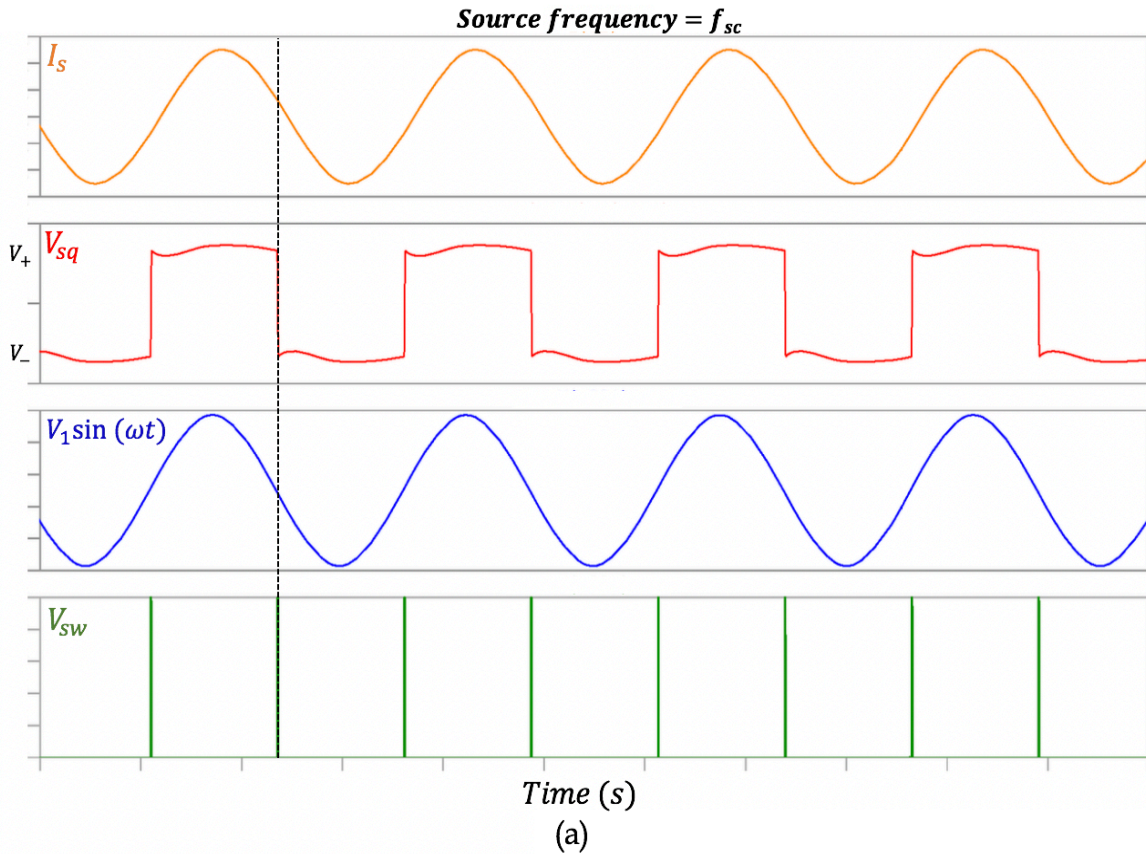
**Figure 4-4.** Optimal phase shift ( $\phi_{sq,opt}$ ) of square wave with respect to the input voltage source ( $V_1$ ).

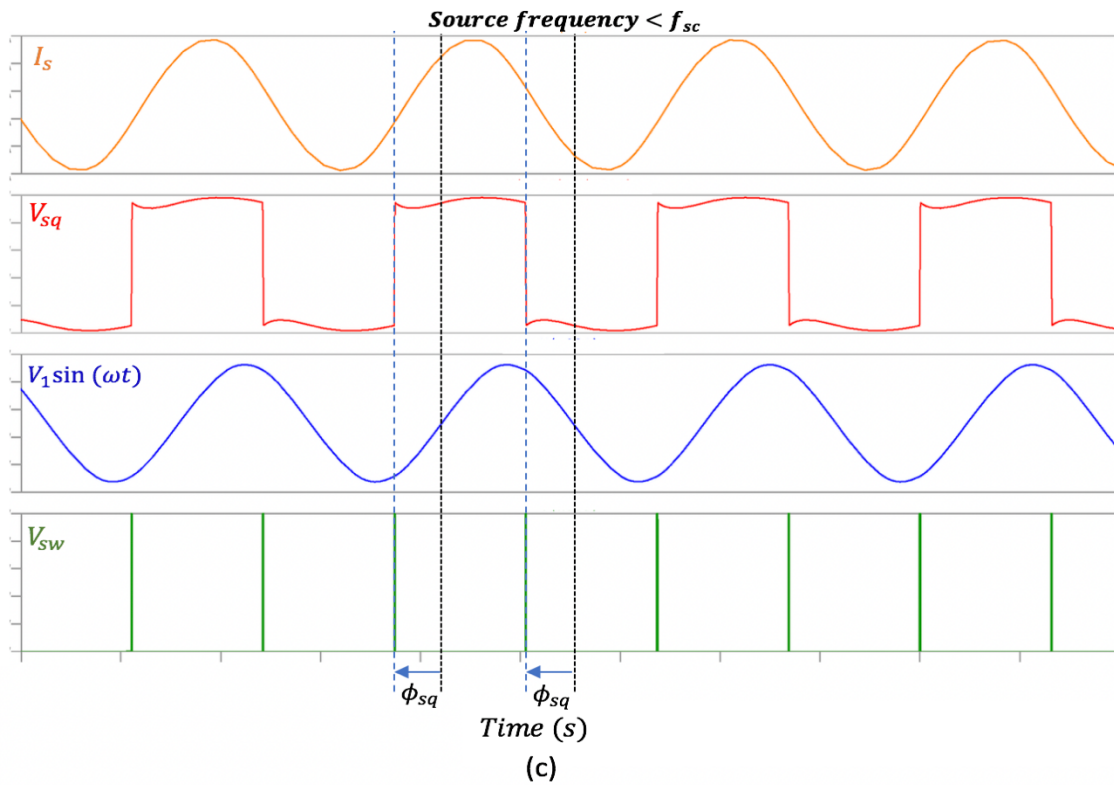
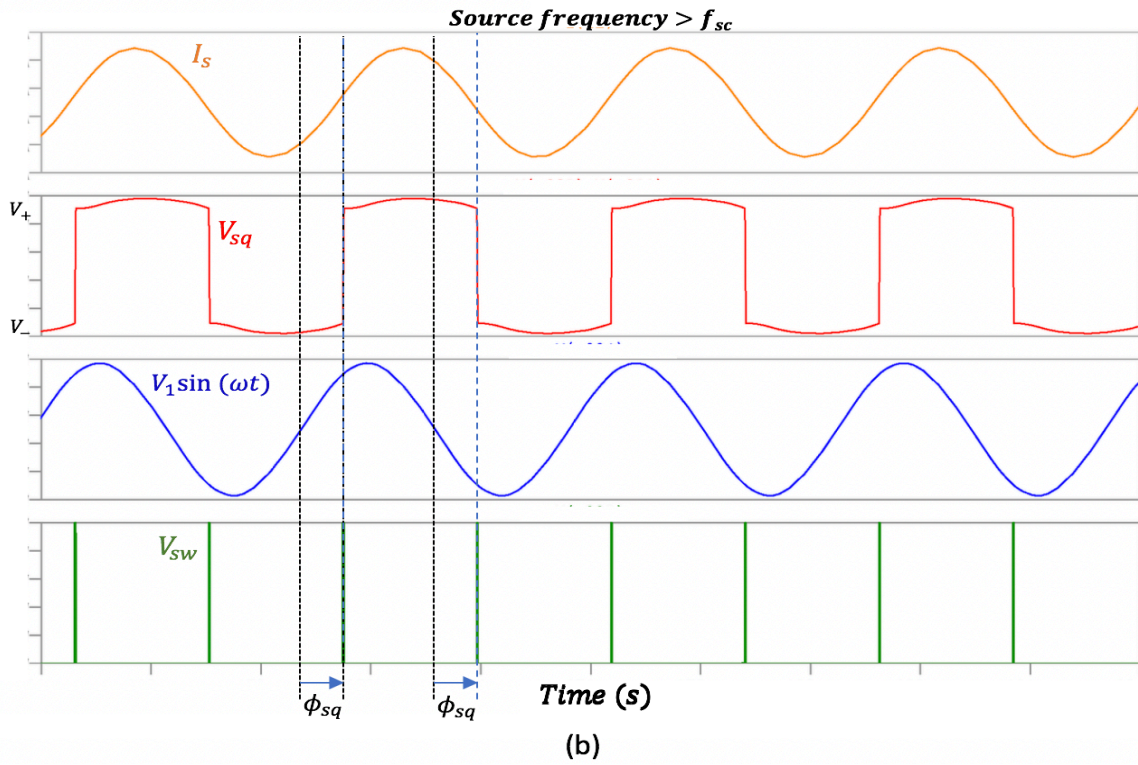


**Figure 4-5.** (a) Bias-flip switch control voltage and square-wave voltage with respect to time. (b) Zoomed-in version of plot on the left.

is close to zero. As we start increasing the frequency above resonance, the phase shift increases, and eventually reaches  $90^\circ$  at frequencies far from resonance. Below the resonant frequency, the phase shift decreases and eventually reaches  $-90^\circ$ . In Figure 4-5, the voltage  $V_{sq}$  across the parasitic capacitor switches sign whenever the bias-flip switch turns on. Therefore, we can fire the  $V_{sw}$  pulse train, shown in Figure 4-5, such that the optimal phase shift between the input voltage source, and square-wave is achieved. Figure 4-6 shows the bias-flip in action and all the details behind how the switching is done at various frequencies. The plots in Figure 4-6 were made with LT Spice simulations, and the circuit used in the simulations is given in the appendix (A2.3.1). When operating at the short-circuit resonant frequency, the optimal phase shift is zero, so we expect the voltage square-wave ( $V_{sq}$ ) to be in phase with the input voltage ( $V_1$ ) as shown

in Figure 4-6 (a). In this case, the bias-flip switch turns on at the zero crossing of the input voltage source. At frequencies above  $f_{sc}$ , the optimal phase difference between  $V_{sq}$  and  $V_1$  is positive. In Figure 4-6 (b), the bias-flip switch is closed  $T_{delay}$  seconds after  $V_1$  crosses zero, where  $T_{delay} = \frac{\phi_{sq,opt}}{2\pi f}$ . And lastly, at frequencies below resonance, the switch is triggered to close  $T_{delay}$  seconds before  $V_1$  crosses zero, as shown in Figure 4-6 (c). What all three plots in Figure 4-6 have in common is that  $V_{sq}$  and  $I_s$  are always in phase, a necessary condition for optimal power delivery. It is obvious in the simulation plots, that  $V_{sq}$  is not a perfect square-wave, but is extremely similar to one in shape. Approximating  $V_{sq}$  as a perfect square-wave, does not affect the derivations of the optimal phase, frequency, and amplitude.





**Figure 4-6.** Simulated voltage and current waveforms of the circuit shown in Figure 4-3 at (a) the short-circuit resonant frequency ( $f_{sc} = 198.8 \text{ Hz}$ ), (b) a frequency (205 Hz) greater than  $f_{sc}$ , and (c) a frequency (194 Hz) below  $f_{sc}$ .

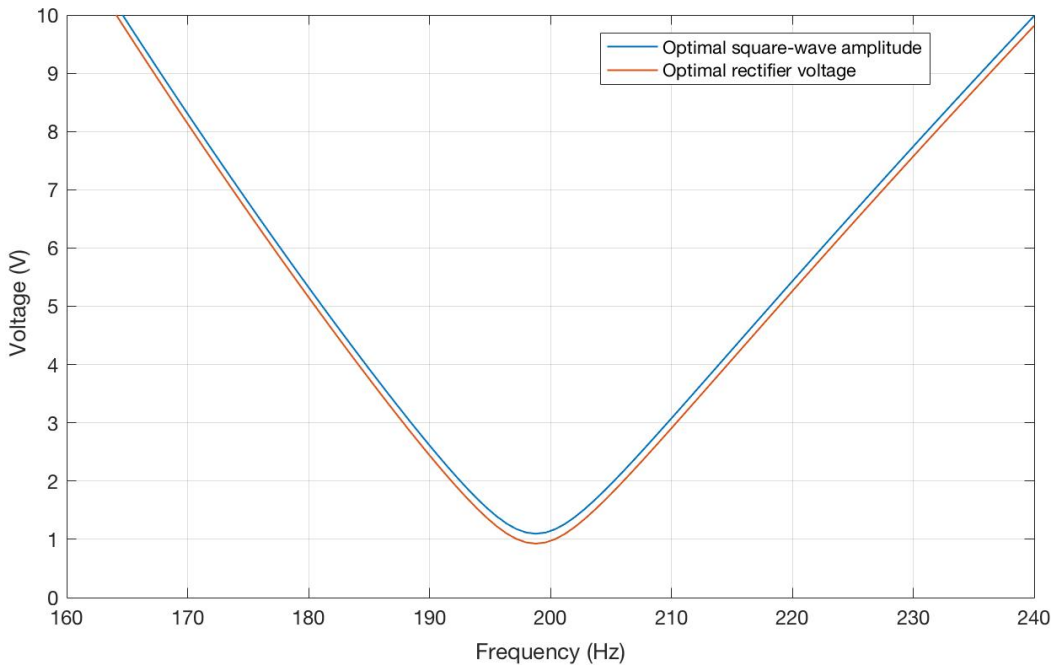
## 4.2.2 Optimal Amplitude

In Section 4.1.2, we derived the optimal square wave amplitude ( $V_{sq,opt}$ ) in 4.11, which is repeated here,  $V_{sq,opt} = \frac{\pi V_D}{8R} \sqrt{(\omega L_m - 1/\omega C)^2 + R^2}$ , where  $\omega$  is the source vibration frequency.

In Figure 4-7  $V_{sq,opt}$  is plotted with respect to vibration frequency.

Referring back to the circuit in Figure 4-3 (a), we see that at any time, the rectifier voltage  $V_{rect}$  is equal to the absolute value of  $V_{sq}$ . Assuming  $V_{sq}$  is a perfect square wave, then  $V_{rect}$  will be a constant voltage at  $|V_{sq}|$ . Therefore, we can set the amplitude of the square-wave to  $V_{sq,opt}$ , by setting  $V_{rect}$  to that voltage. It must be mentioned that the circuit Figure 4-3 (a) uses ideal diodes in the full-bridge rectifier, which have a zero forward voltage drop. In the actual circuit (shown in the next chapter) Schottky diodes (BAT54) are used. In the previous chapter, we calculated a forward voltage drop of approximately 85.1 mV. That said,  $V_{sq}$  will always be two forward voltage drops above  $V_{rect}$ .

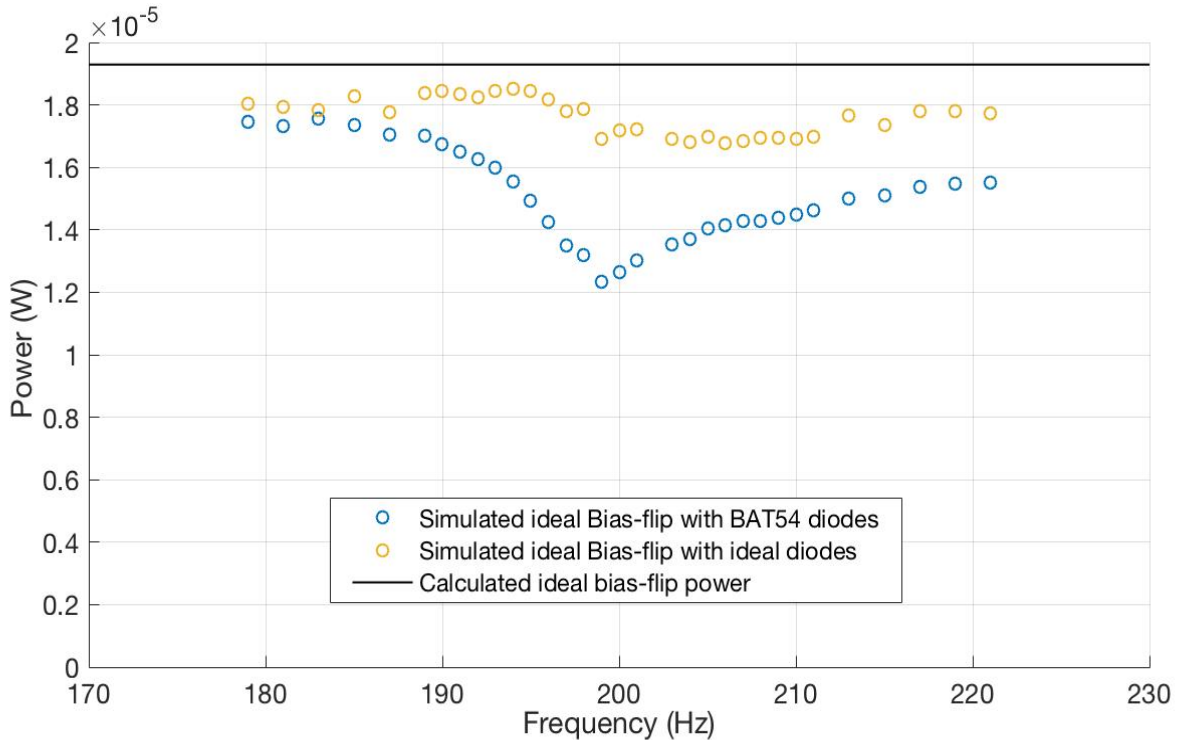
$$V_{rect} = V_{sq,opt} - 2 * V_f = V_{sq,opt} - 0.170 \quad (4.14)$$



**Figure 4-7.** Optimal square-wave amplitude ( $V_{sq,opt}$ ) and rectifier voltage with respect to frequency as predicted by equation 4.11.

### 4.2.3 Ideal Bias-flip Power Delivery

Now that we have outlined a method to create a square with the optimal phase-shift ( $\phi_{sq}$ ) and amplitude ( $V_{sq,opt}$ ), we can expect the power delivered to be close to the theoretical maximum power ( $19.3 \mu W$ ). It must be mentioned that this power can be delivered assuming ideal components are used. The ideal components include an ideal switch (zero ON-resistance), ideal inductor ( $L_{BF}$ ), zero PEHD parasitic resistance and ideal rectifier diodes. Figure 4-8 compares the average power delivered by the bias-flip circuit with and without ideal rectifier diodes to the theoretical maximum power. The simulated ideal bias-flip power is slightly below the theoretical maximum. This discrepancy can be explained by the square-wave approximation we made for the voltage across the parasitic capacitor ( $V_{sq}$ ). Since  $V_{sq}$  is not a perfect square-wave, some of the higher-order harmonics that were able to ignore, may now be non-negligible.

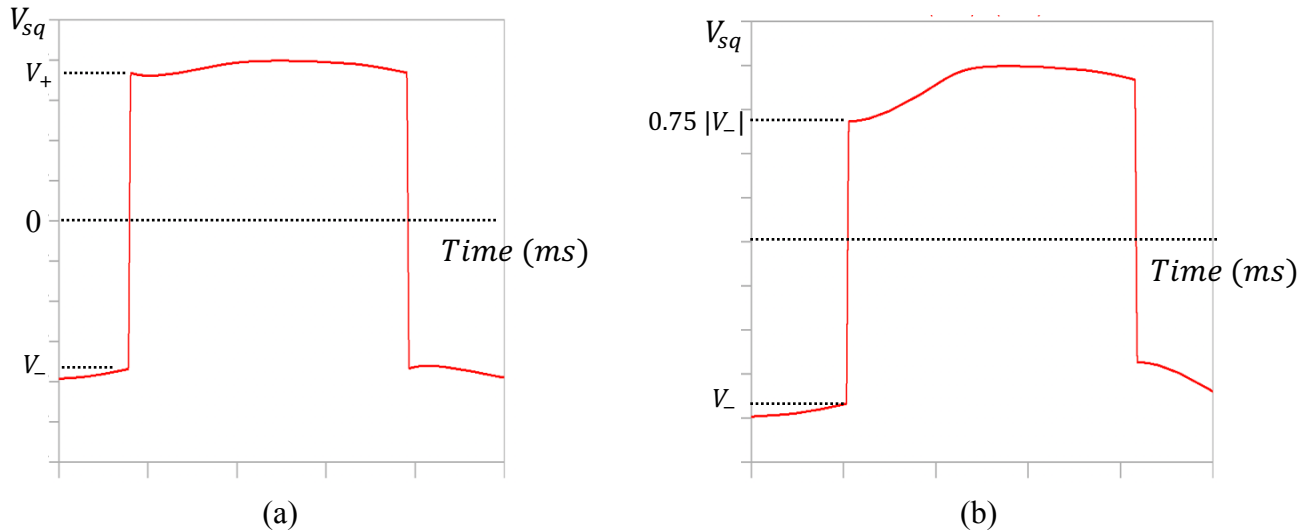


**Figure 4-8.** Calculated and simulated average power delivered with an ideal bias-flip circuit with ideal diodes and BAT54 diodes used in the rectifier.



### 4.3 Bias-Flip Efficiency and Power Loss

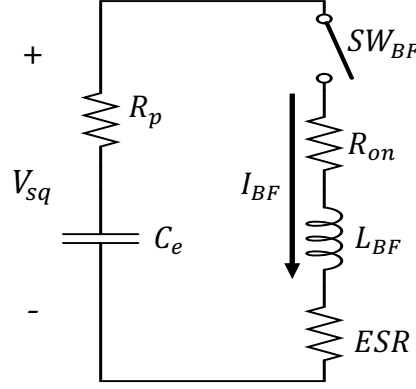
So far, we have assumed that the bias-flip is 100-percent efficient, which means that the voltage across the parasitic capacitor ( $C_e$ ) completely flips polarity. Hence, if the voltage across  $C_e$  is  $V_+$  right before the bias-flip switch closes, then the voltage across  $C_e$  is  $V_-$  after the bias-flip switch opens such that  $|V_+| = |V_-|$ , as shown in Figure 4-9 (a). In order for the bias-flip circuit to be 100-percent efficient, the components:  $L_{BF}$ ,  $SW$ , and the PEHD must be completely lossless. A 100-percent efficient bias-flip is referred to as an ideal bias-flip.



**Figure 4-9.** (a) Simulated voltage across parasitic capacitor ( $V_{sq}$ ) with ideal bias-flip.  
(b) Simulated voltage across parasitic capacitor with 75 % efficient bias-flip.

#### 4.3.1 Bias-flip Efficiency

In order to derive the bias-flip efficiency ( $\eta_{BF}$ ) we refer to the circuit in Figure 4-10. The bias-flip inductor has series resistance value (ESR), the switch has an on-state resistance ( $R_{on}$ ), and the harvester has a parasitic resistance ( $R_p$ ) in series with  $C_e$ .



**Figure 4-10.** Isolated bias-flip circuit.

In order to derive the bias-flip efficiency, I first write out the KCL equation of the above circuit,

with  $R_{total} = ESR + R_{on} + R_p$  and  $\omega_{BF} = 1/\sqrt{L_{BF}C_e}$ .

$$\frac{d^2 I_{BF}}{dt^2} + \frac{R_{total}}{L_{BF}} \frac{dI_{BF}}{dt} + \frac{I_{BF}}{L_{BF}C_e} = 0$$

$$I_{BF} = Ae^{kt}, \text{ where } A \text{ is a constant}$$

$$k^2 + \frac{R_{total}}{L_{BF}}k + \frac{1}{L_{BF}C_e} = 0 \rightarrow k = -\frac{R_{total}}{2L_{BF}} \pm \sqrt{\left(\frac{R_{total}}{2L_{BF}}\right)^2 - \frac{1}{L_{BF}C_e}}$$

In order for the bias-circuit to be under-damped,  $\frac{1}{L_{BF}C_e} > \left(\frac{R_{total}}{2L_{BF}}\right)^2$ , and therefore

$$L_{BF} > \frac{1}{4}C_e R_{total}^2. \quad (4.15)$$

Equation 4.15 puts a constraint on size of the bias-flip inductor we can use. Assuming the under-damping condition (4.15) is met, the current around the loop is

$$I_{BF} = e^{-\frac{R_{total}}{2L_{BF}}t} [A_1 \cos(\omega'_{BF}t) + A_2 \sin(\omega'_{BF}t)], \quad (4.16)$$

$$\text{where } \omega'_{BF} = \sqrt{\omega_{BF}^2 - \left(\frac{R_{total}}{2L_{BF}}\right)^2}.$$

We know that initially (at  $t = 0$ ) the bias-flip current is zero, which means  $A_1=0$ . Integrating  $I_{BF}$  with respect to time, the voltage across the parasitic capacitor ( $V_{sq}$ ) at  $t = 0$  is

$$V_{sq} = v_{initial} e^{-\frac{R_{total}}{2L_{BF}} t} \cos(\omega'_{BF} t), \quad (4.17)$$

where  $v_{initial} = V_{sq}$  before the switch turns on ( $t=0$ ). In my design,  $\omega_{BF} \gg \left(\frac{R_{total}}{2L_{BF}}\right)$  which means

$\omega'_{BF} \approx \omega_{BF}$ . The bias-flip switch closes at  $t = 0$  and opens after half an oscillatory period

( $t = T_{on} = \frac{\pi}{\omega_{BF}}$ ). At that time  $V_{sq}$  is

$$V_{sq} = -V_{initial} e^{-\frac{R_{total}}{2L_{BF}} \frac{\pi}{\omega_{BF}}} = -V_{initial} e^{-\frac{\pi R_{total}}{2} \sqrt{\frac{C_e}{L_{BF}}}}. \quad (4.18)$$

From Equation (4.18), we can tell that the bias-flip efficiency is

$$\eta_{BF} = e^{-\frac{\pi R_{total}}{2} \sqrt{\frac{C_e}{L_{BF}}}} = e^{-\frac{\pi(ESR+R_{on}+R_p)}{2} \sqrt{\frac{C_e}{L_{BF}}}}. \quad (4.19)$$

Table 4-1 provides the values of the bias-flip components I decided to use in my design along with the intrinsic resistances, measured at resonance.

Bias-flip circuit components	Part number	Specified value	Measured value
Parasitic capacitor ( $C_e$ )	–	–	57.2 nF
Bias-flip inductor ( $L_{BF}$ )	RFS1412-105KE	1 mH	1.02 mH
Bias-flip Switch ( $SW_{BF}$ )	MAX 4716	–	–

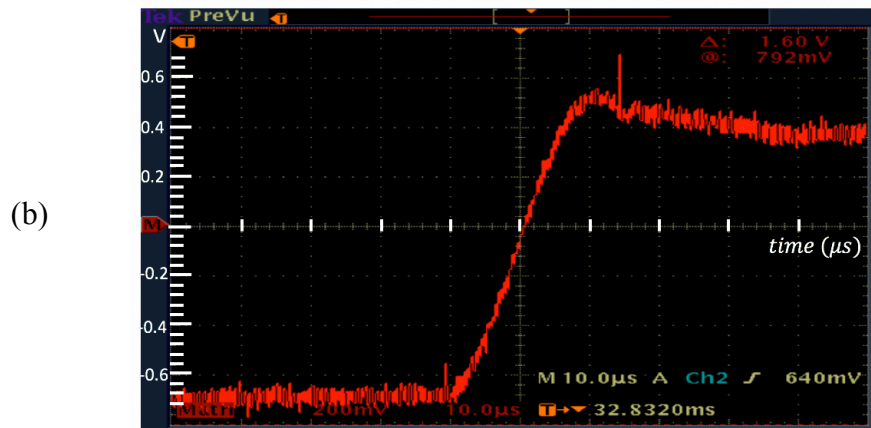
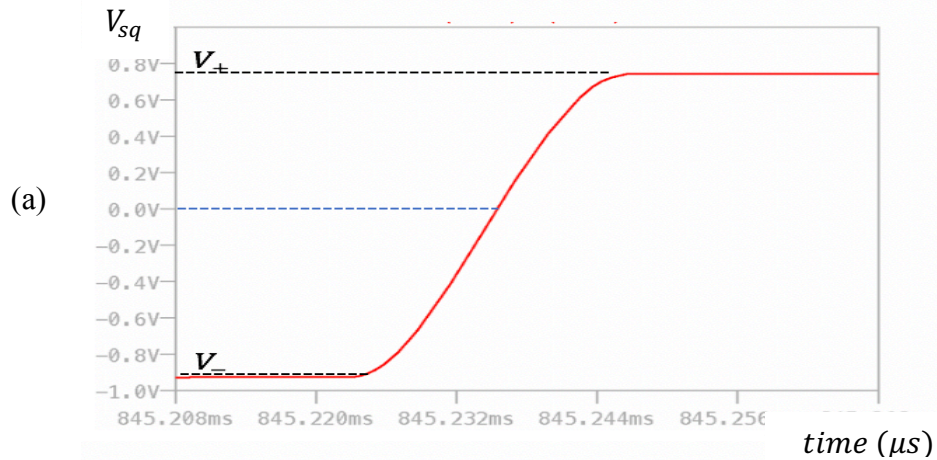
(a)

Bias-flip intrinsic resistances	Specified value	Measured value
Inductor <b>ESR</b>	1.01 $\Omega$	1.4 $\Omega$
Switch on-resistance ( $R_{on}$ )	0.4 $\Omega$	0.5 $\Omega$
PEHD parasitic resistance ( $R_p$ )	–	16.6 $\Omega$

(b)

**Table 4-2.** (a) Bias-flip circuit components with measured values made using an impedance analyzer. (b) Bias-flip circuit intrinsic resistances with ESR and  $R_p$  measured with an impedance analyzer at resonance. The specified values are taken from the manufacture's datasheet.

While choosing an inductor three considerations were taken into account. Firstly, the condition in (4.15) must be satisfied, which means  $L_{BF}$  must be larger than a certain threshold. Next, the bias-flip resonant frequency must be much greater than the source vibration frequency ( $\omega_{BF} \gg \omega_{source}$ ), which puts an upper limit on the size of  $L_{BF}$ . And lastly, the bias-flip efficiency in equation 4.18 improves as  $L_{BF}$  increases. Correspondingly, a 1 mH inductor (Coil Craft RFS1412-105KE) was used, which best balances the three conditions above. The calculated bias flip efficiency is around 80.2%, and  $\omega_{BF} = 132$  kHz, approximately 100 times the source vibration frequency. The bias-flip efficiency is calculated as the ratio of  $V_+$  to  $V_-$  of the voltage across the parasitic capacitor as measured in Figure 4-11. Table 4-2 shows the simulated and measured bias-flip efficiency at resonance. The spice simulation circuit is given in (A2.4).



**Figure 4-11.** (a) Simulated voltage across the parasitic capacitor ( $V_{sq}$ ). (b) Measured voltage across the parasitic capacitor ( $V_{sq}$ ).

Bias-flip circuit characteristics	Simulated value	Measured value
Resonant frequency ( $\omega_{BF}$ )	132 kHz	131.2 kHz
Bias-flip efficiency ( $\eta_{BF}$ )	79.8 %	79.6 %

**Table 4-3.** Simulated and measured bias-flip circuit characteristics.

### 4.3.2 Power Loss in Non-ideal Bias-flip Circuit

Power is lost in the bias-flip circuit of Figure 4-10 only when the bias-flip switch is on. We can calculate the power lost during bias-flip switching by comparing the energy stored in the parasitic capacitor before the switch closes ( $E_{C_e,initial}$ ) to the energy stored right after the switch opens ( $E_{C_e,final}$ ) [4]. The voltage across the parasitic capacitor before switching is  $V_{sq,initial}$ , and with an efficiency of  $\eta_{BF}$ , the voltage across  $C_e$  after switching is  $\eta_{BF} \times V_{sq,initial}$ .

Therefore, the energy dissipated during switching is calculated as

$$\begin{aligned}
 E_{BF,loss} &= E_{C_e,initial} - E_{C_e,final} \\
 &= \frac{1}{2} C_e V_{sq,initial}^2 - \frac{1}{2} C_e (\eta_{BF} V_{sq,initial})^2
 \end{aligned} \tag{4.20}$$

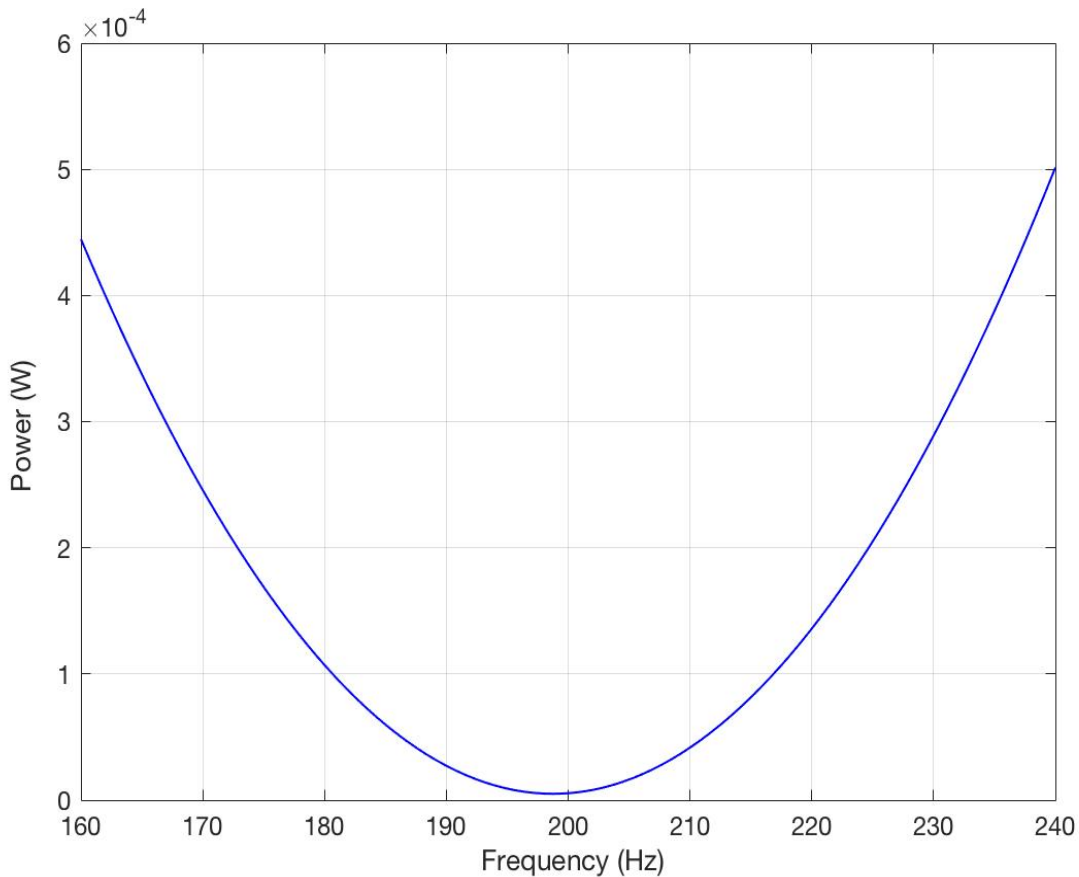
We know that the bias-flip switch turns on twice per period, which means the total energy dissipated per period is  $2 \times E_{BF,loss}$  and the average power is calculated as

$$P_{BF,loss} = (C_e)(f)(V_{sq,initial})^2(1 - \eta_{BF}^2), \tag{4.21}$$

where  $f$  is the ambient vibration frequency.

In Section 4.2.2, we saw that the amplitude of the voltage square wave ( $V_{sq}$ ) across the parasitic capacitor is set by the rectifier DC voltage, and the optimal square wave amplitude ( $V_{sq,opt}$ ) for power delivery at each frequency is shown in Figure 4-7. Setting  $V_{sq,initial}$  in Equation 4.12 as  $V_{sq,opt}$  and using the measured  $\eta_{BF} = 0.796$  found in the previous Section, the plot for  $P_{BF,loss}$  with respect to frequency is shown in Figure 4-12. At frequencies above and below short-circuit

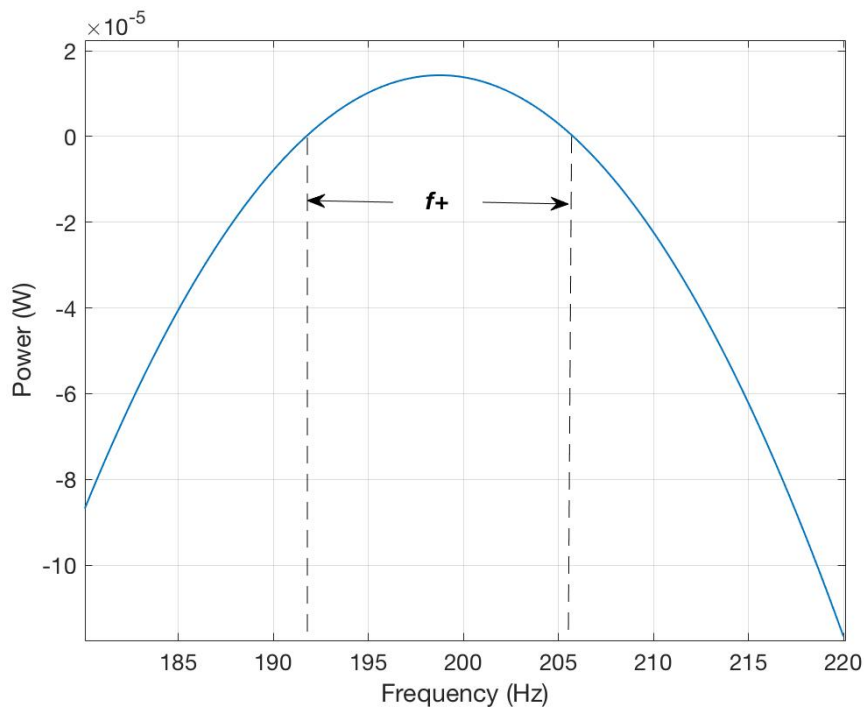
resonance,  $P_{BF,loss}$  increases drastically. In Section 4.2.2, we found the maximum power that could be harvested with an ideal bias-flip approximately equal to the theoretical maximum power  $P_{BF,opt} \approx 19.3 \mu W$ . From Figure 4-12, it is seen that the power dissipated in the bias-flip circuit exceeds  $P_{BF,opt}$  at frequencies only a few Hz from  $\omega_{sc}$ . This is, of course, impossible because current would have to flow through the rectifier diodes in the reverse direction. That said, the square-wave amplitude that was derived in Section 4.1 ( $V_{sq,opt}$ ) is optimal for the ideal bias-flip circuit, but not for the non-ideal case. In the next section, we will find the optimal square-wave amplitude for the non-ideal bias-flip circuit.



**Figure 4-12.** Average power lost in a 79.6% efficient bias-flip circuit, using the optimal square-wave amplitude  $V_{sq,opt}$ , shown in (4.11).

## 4.4 Non-ideal Bias-flip Model

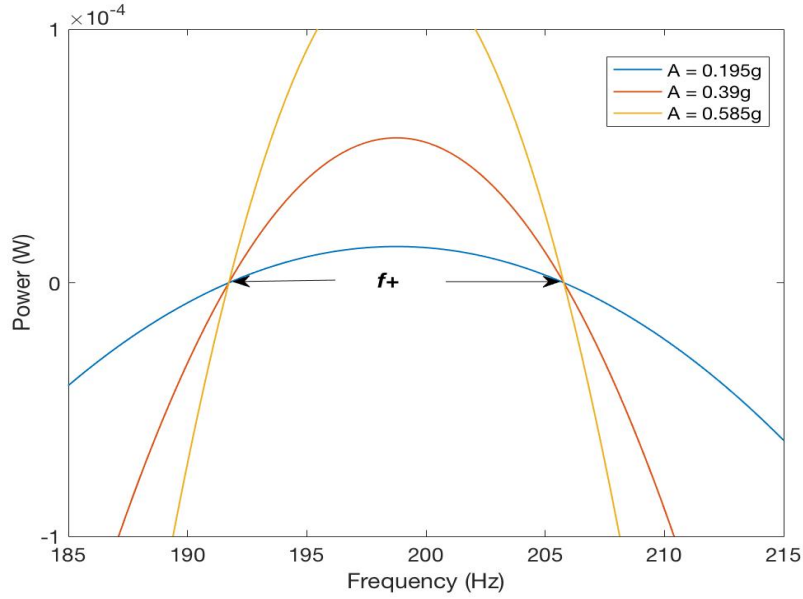
In Section 4.3.2, it was shown that the average power lost in the bias-flip circuit increases tremendously as we move away from the short-circuit resonant frequency, when using the optimal square-wave amplitude ( $V_{sq,opt}$ ). In Figure 4-13, the difference between the maximum bias-flip power that can be harvested ( $P_{BF,opt} \approx 19.3 \mu W$ ) and the power lost in the bias-flip circuit is plotted. This quantity will be referred to as the non-ideal bias-flip power ( $P_{BF,non-ideal}$ ).



**Figure 4-13.** Non-ideal bias-flip power ( $P_{BF,non-ideal}$ ) plotted with respect to frequency.

As Figure 4-13 makes clear, even before accounting for the power lost in the rectifier, the frequency range ( $f_+$ ) for which positive power can be harvested is extremely narrow (191.7 Hz to 205.8 Hz). For frequencies out of the  $f_+$  range,  $P_{BF,non-ideal}$  is negative, which means power must flow from the rectifier side of the circuit in Figure 4-3 to the harvester side, which is

impossible. It's worth mentioning that the frequency range  $f_+$  does not improve with changes in acceleration which is made evident in Figure 4-14.



**Figure 4-14.** Non-ideal bias-flip power ( $P_{BF,non-ideal}$ ) at different accelerations plotted with respect to frequency.

Optimal square-wave amplitude for non-ideal bias-flip circuit:

The previous optimal square-wave amplitude ( $V_{sq,opt}$ ) in Section 4.1 was derived for the ideal bias-flip circuit. However,  $V_{sq,opt}$  is not the optimal square-wave amplitude for the non-ideal bias-flip circuit. To calculate the optimal square-wave amplitude for the non-ideal case ( $V_{opt,non-ideal}$ ), we first write out the equation for average power delivered by the non-ideal bias-flip circuit.

$$P_{opt,non-ideal} = P_{sq} - P_{BF,loss},$$

where  $P_{sq}$  is the power harvested by the square-wave (derived in (4.9)), and  $P_{BF,loss}$  is the power lost in the bias-flip circuit shown in Equation 4.21.

$$P_{opt,non-ideal} = \frac{2}{\pi} \frac{V_{sq} V_1}{\sqrt{X_s^2 + R_s^2}} - \frac{8V_{sq}^2}{\pi^2} \frac{R_s}{X_s^2 + R_s^2} - (C_e)(f)(V_{sq})^2(1 - \eta_{BF}^2), \quad (4.22)$$

where  $X_s, R_s$  and  $V_1$  are defined in Figure 4.1. Taking the first order derivative of  $P_{opt,non-ideal}$



with respect to  $V_{sq}$ , we find the optimal square-wave amplitude as

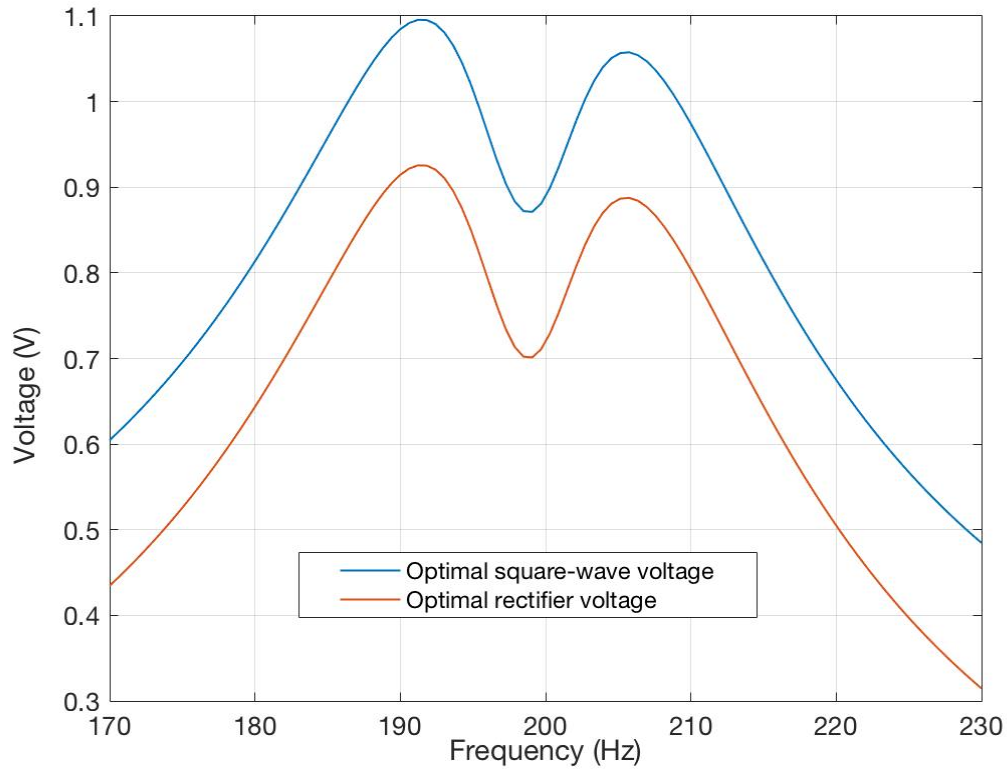
$$V_{opt,non-ideal} = \frac{V_D/\pi}{C_{ef}(1 - \eta_{BF}^2) Z_{eq} + \frac{8}{\pi^2} \frac{R}{Z_{eq}}}, \quad (4.23)$$

$$\text{where } Z_{eq} = \sqrt{\left(\omega L_m - \frac{1}{\omega C}\right)^2 + R^2}$$

We realize that  $V_{opt,non-ideal}$  increases with the efficiency of the bias-flip circuit. Thus, with a 100% efficient bias-flip,  $V_{opt,non-ideal}$  is reduced to  $V_{sq,opt}$ , which is exactly as expected. Recall in Section 4.2.2 that the rectifier voltage  $V_{rect}$  sets the square wave amplitude as given by

$$V_{rect,non-ideal} = V_{opt,non-ideal} - 0.170. \quad (4.24)$$

By setting the rectifier to the correct value, we can achieve a voltage of  $V_{opt,non-ideal}$  across the parasitic capacitor. In Figure 4-15,  $V_{opt,non-ideal}$  and  $V_{rect,non-ideal}$  are plotted.



**Figure 4-15.** Optimal square-wave voltage amplitude and rectifier voltage for non-ideal bias-flip circuit with respect to frequency.

## 4.5 Sources of Power Loss

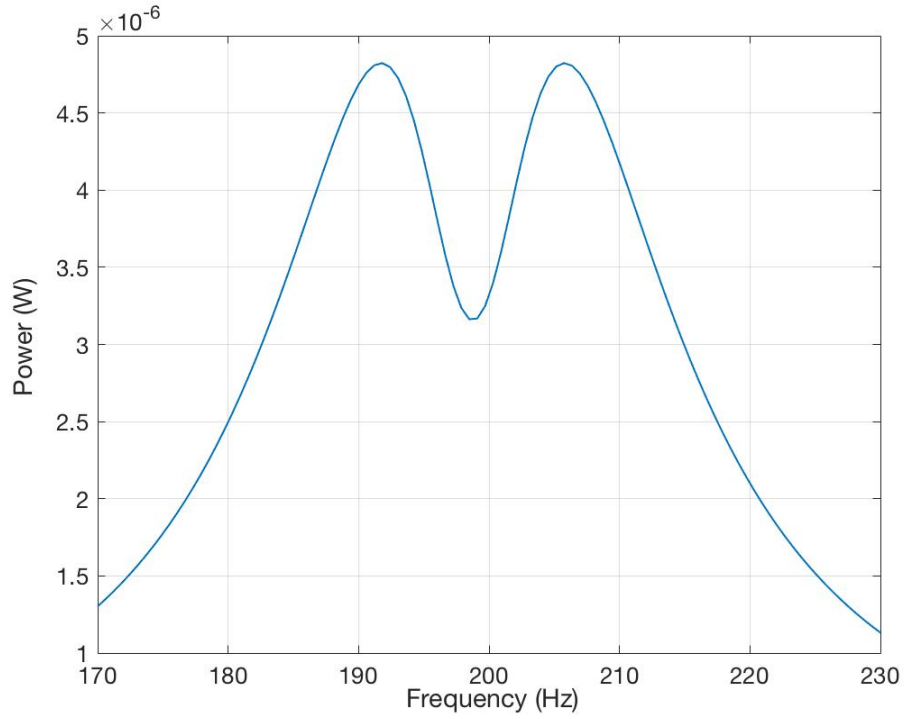
With an ideal bias-flip circuit and lossless diodes, it was concluded in the previous section that approximately  $P_{optimal}$  can be delivered. However, in Section 4.3 we discovered that the components in the bias-flip circuit are not lossless, and the diodes have a forward voltage drop. The total power lost in the circuit can be divided into two categories: bias-flip circuit loss and rectifier loss.

### 4.5.1 Bias-flip Circuit Power Loss

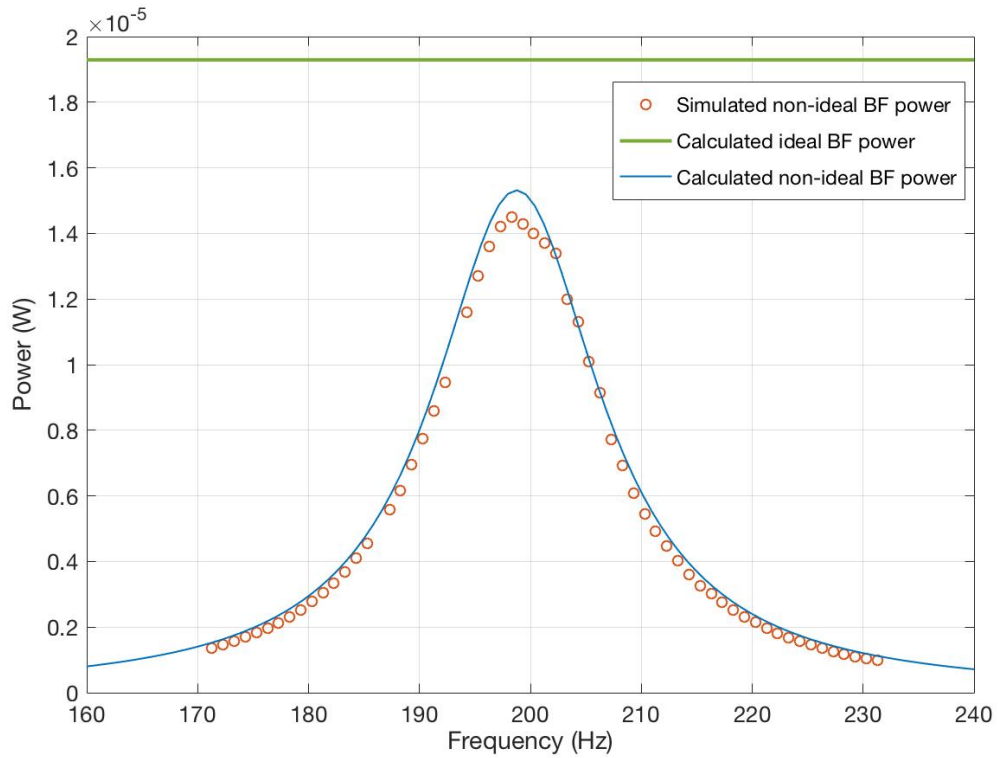
The power lost in the bias-flip circuit is given by Equation 4.21, and is repeated here for convenience

$$P_{BF,loss} = (C_e)(f)(V_{sq,initial})^2(1 - \eta_{BF}^2).$$

Replacing the optimal square-wave amplitude  $V_{opt,non-ideal}$  derived in (4.23) in  $P_{BF,loss}$ , we get the plot shown in Figure 4.16. Going further,  $V_{opt,non-ideal}$  is replaced into  $P_{opt,non-ideal}$  in Equation 4.22 to find the optimal power harvested by a non-ideal bias-flip circuit. In Figure 4-17 the calculated and simulated  $P_{opt,non-ideal}$  is plotted. The spice simulation circuit for this plot is given in the appendix (A2.3.2). We notice that the calculated  $P_{opt,non-ideal}$  is slightly higher than the simulated  $P_{opt,non-ideal}$ , which can be explained by the square-wave approximation we made in Section 4.1. The bias-flip voltage waveforms are not exactly identical to square-waves in shape, which means the power calculation we made in Section 4.1 and 4.21, which assumed perfect square-waves, is only an approximation. Furthermore, the optimization did not account for the rectifier diode drop, which gets worse at higher currents, instead  $V_f$  was assumed constant at all frequencies. The simulated plots more closely match the true behavior of the circuit.



**Figure 4.16.** Power lost in bias-flip circuit with optimized non-ideal bias-flip amplitude ( $V_{opt,non-ideal}$ ) used.



**Figure 4.17.** Optimal power harvested from non-ideal (79.6% efficiency) bias-flip circuit  $P_{opt,non-ideal}$  with respect to frequency.

## 4.5.2 Full-bridge Rectifier Power Loss

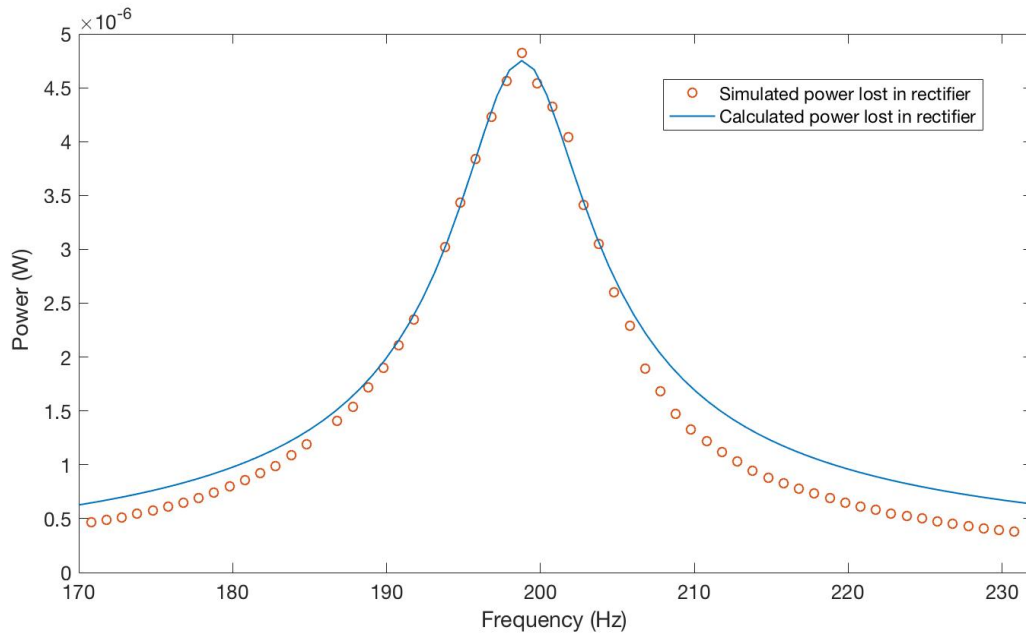
The power lost in the rectifier is pretty straight-forward to approximate if a constant  $V_f$  is assumed at all frequencies. We know that at any time two diodes are on. Therefore, the power dissipated in a diode is simply the rectifier current flowing through that diode times its forward voltage drop. Assuming the optimal square wave amplitude ( $V_{opt,non-ideal}$ ) is used the average rectifier current ( $I_{rect}$ ) in Figure 4-3 can be calculated as

$$I_{rect,avg} = \frac{P_{opt,non-ideal}}{V_{opt,non-ideal}}$$

With the choice of diodes (BAT54), a forward diode drop of  $85.1\text{ mV}$  was measured in Chapter 3. Hence, the average power dissipated in the rectifier is

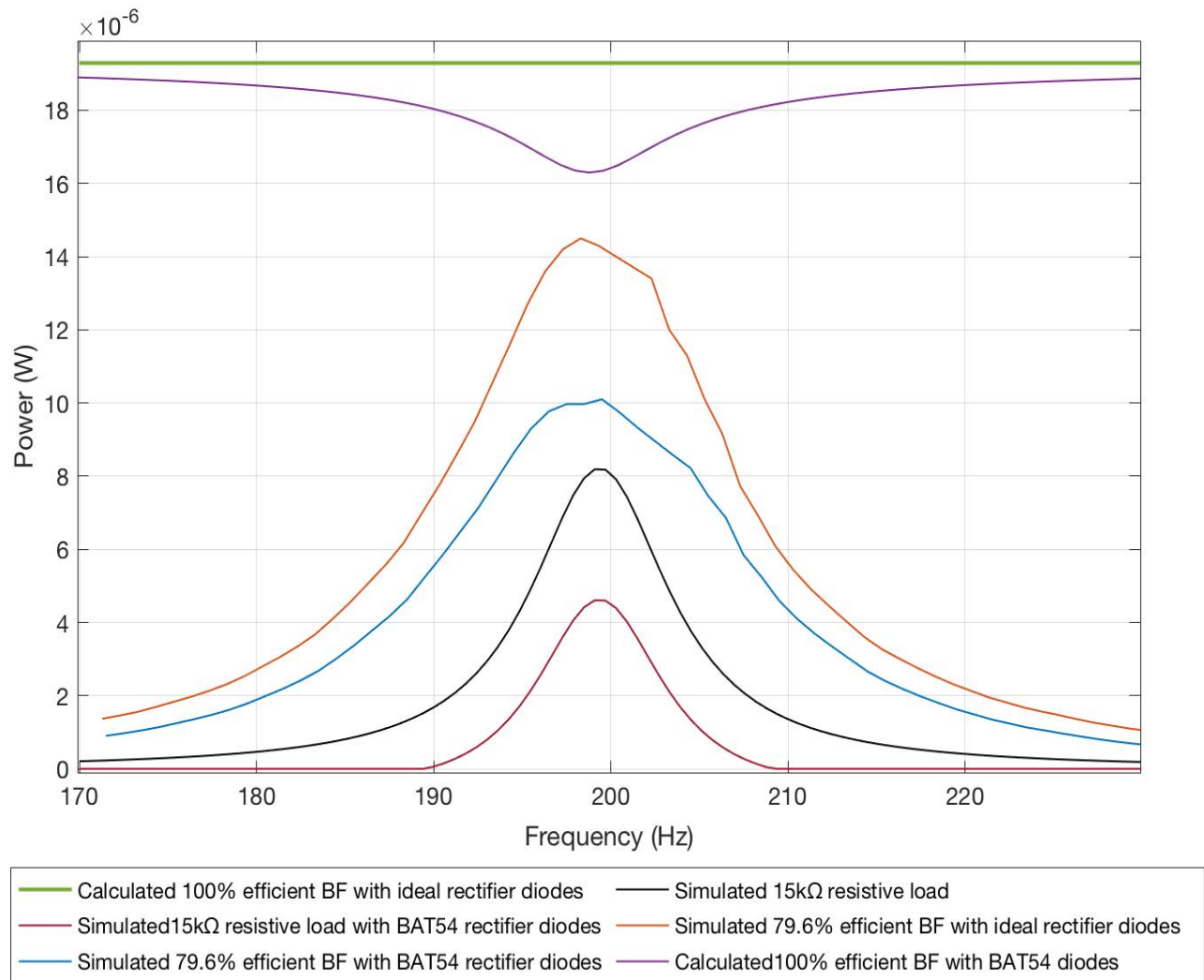
$$P_{loss,rect} = I_{rect,avg} \times 2V_f = 2V_f \frac{P_{opt,non-ideal}}{V_{opt,non-ideal}}. \quad (4.25)$$

The average power dissipated in the full-bridge rectifier is plotted Figure 4-18. As expected, the power lost is highest at resonance ( $\approx 3\mu\text{W}$ ), where average rectifier current is maximum.

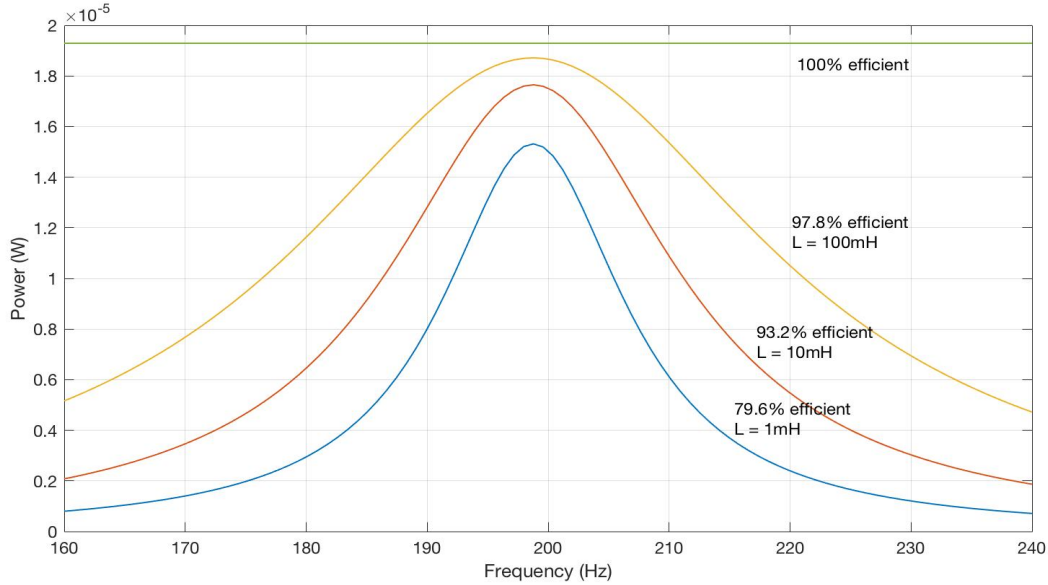


**Figure 4-18.** Average power dissipated in full-bridge rectifier using BAT54 diodes with respect to frequency.

The plot in Figure 4-19 summarizes everything we have seen so far in this section by comparing the power harvested by the non-ideal bias-flip circuit to the power harvested with different circuit techniques. As we can see, the 79.6%-efficient bias-flip circuit has a much lower power bandwidth than the 100% efficient circuit. However, when compared to the power delivered to the 15 kΩ resistor at the end of the rectifier, the 79.6%-efficient bias-flip circuit still performs extraordinarily well, improving power at resonance by around 2.1 times, and extending bandwidth by around 2.4 times.



**Figure 4-19.** Power harvested with respect to frequency under various conditions.



**Figure 4-20.** Calculated power harvested at different bias-flip efficiency levels.

## 4.6 Chapter Summary

This chapter introduced the ideal bias-flip circuit as well as the derivations for the optimal phase, amplitude and frequency. With an ideal bias-flip circuit, around the maximum theoretical power could be harvested at all frequencies. However, the bias-flip switch, inductor, and the PEHD have intrinsic resistances, which decrease the efficiency of the bias-flip circuit. The efficiency of the bias-flip circuit was then measured at resonance and closed-form equation for the power lost in the bias-flip circuit was provided. The optimal square-wave amplitude ( $V_{opt,non-ideal}$ ) for the non-ideal bias-flip circuit ( $\approx 80\%$  efficiency) was then derived, and consequently the maximum power harvested was calculated. What we realized is the power harvested with a  $\approx 80\%$  efficient bias-flip circuit is well below that of the ideal bias-flip circuit, especially away from resonance. Nonetheless, the non-ideal bias-flip circuit shows significant power improvement when compared to the purely resistive load. Finally, to end this chapter, the power harvested with the bias-flip circuit at different efficiencies is plotted in Figure 4-20. Next to each plot is the required bias-flip inductor ( $L_{BF}$ ) needed to achieve that efficiency level.



# Chapter 5

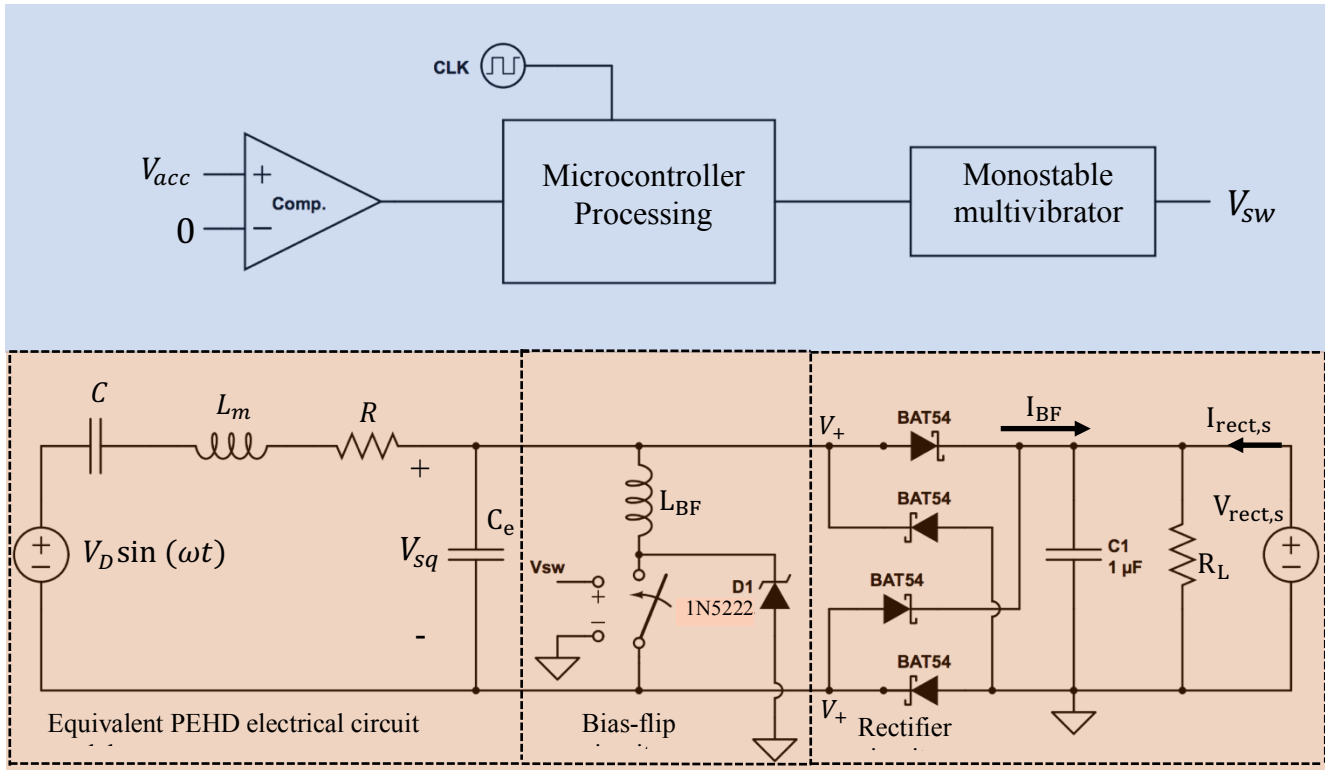
## Experimental Bias-flip

In Chapter 4, the general bias-flip circuit was introduced, and we established its optimal phase, amplitude and frequency for power delivery. This chapter describes the actual bias-flip circuit used, and explains how the bias-flip switch was controlled with the digital circuitry. In reality, there is no such thing as an ideal bias-flip circuit, that is 100% efficient, so the non-ideal bias-flip model is relevant. Once the bias-flip circuit is fully explained, the experimental waveforms will be compared to the simulated (LT Spice) waveforms, to demonstrate that the circuit performs as outlined.

After discussing the system architecture, the experimental results will be described, including how these measurements were made, as well as the reliability of each measuring technique. Finally, the measured power results will be compared to LT Spice simulations and MATLAB calculations. At the end of the chapter we will propose ways to optimize the circuit.



## 5.1 Experimental Bias-flip Circuit



**Figure 5-1.** Simplified diagram of the experimental Bias-flip circuit.

### Bias-flip circuit:

The complete circuit is shown in the orange shaded portion of Figure 5-1. The circuit can be divided into three sub-circuits: the equivalent PEHD circuit, the Bias-flip circuit, and the rectifier circuit. The equivalent PEHD electrical circuit model was characterized in Chapter 2, and the parameters are repeated in Table 5-1.

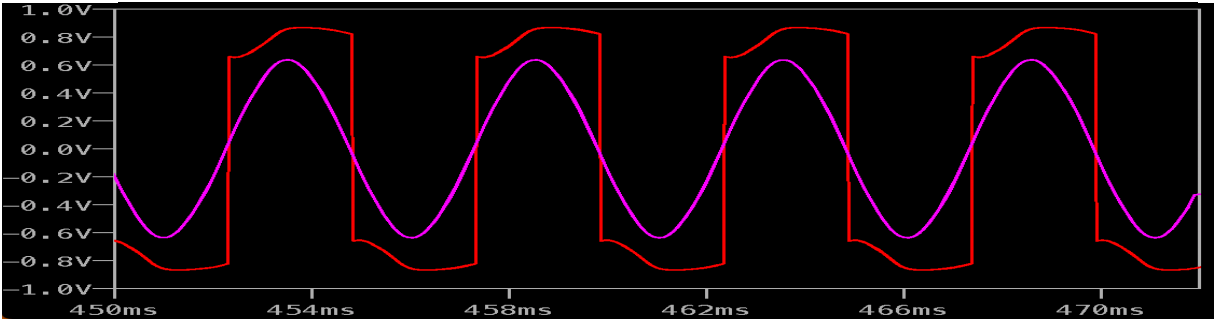
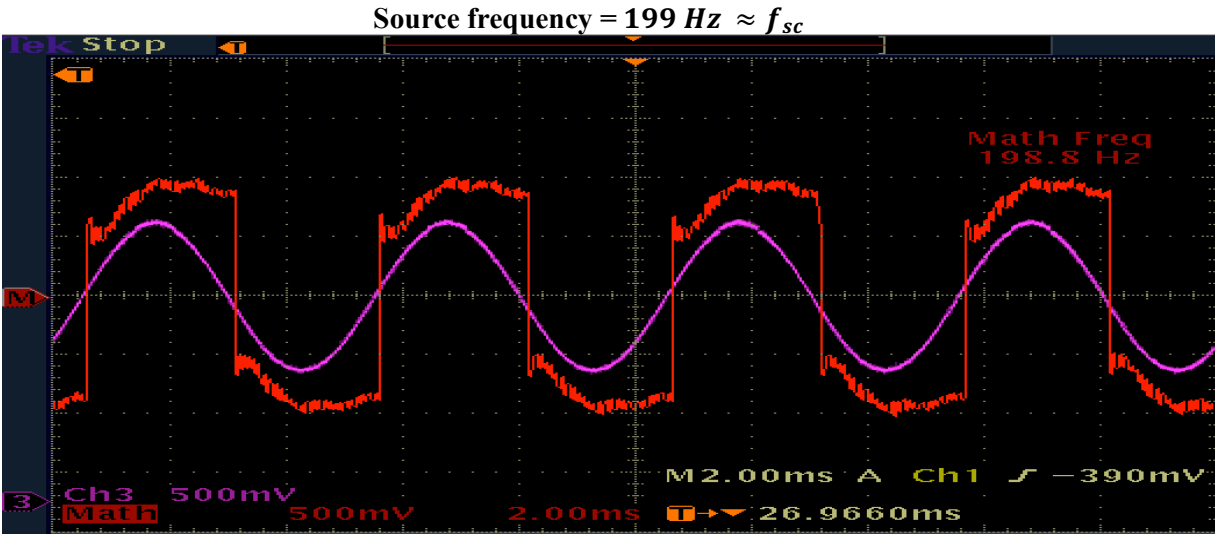
The bias-flip circuit is comprised of a bidirectional analog switch (MAX4716) and an inductor ( $L_{BF} = 1mH$ ). The analog switch has a maximum turn-on time of  $18 ns$  and turn-off time of  $12 ns$ , which is around 1000 times faster than the on-switch time  $T_{on} = \frac{1}{2f_{BF}} = 23.7 \mu s$ . The MAX4716 also has a maximum on-resistance of  $0.4 \Omega$ , which is almost negligible when

compared to the PEHD's parasitic resistance ( $R_p = 16.6 \Omega$ ). It is also worth mentioning that the top and bottom nodes  $V_+$  and  $V_-$  can never go below a forward diode drop below zero. This is important because the analog switch used in the bias-flip circuit can only tolerate voltages between  $-0.3V$  and  $3.3V$ . We measured the diode (BAT54) forward voltage drop in Chapter 3 at around  $85 mV$ , which means  $V_+$  and  $V_-$  are well within the switch's voltage specification.

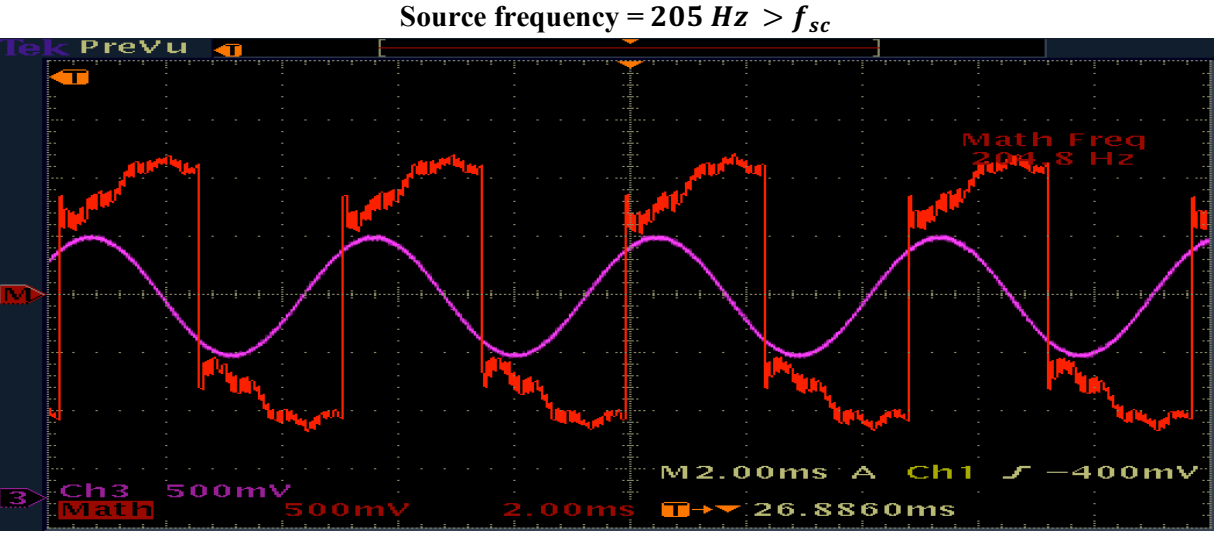
Chapter 4 detailed the factors that must be considered when sizing the bias-flip inductor, and after careful thought, a  $1 mH$  inductor was chosen. A Zener diode is also placed between the inductor's bottom node and ground in order to prevent any damages to the switch. When the switch closes,  $L_{BF}$  and  $C_e$  oscillate for half a period, so we expect the current in the inductor to be zero when the switch opens again. However, it's more than likely that some current will be left-over in the inductor, and that current is led to ground safely with the Zener diode.

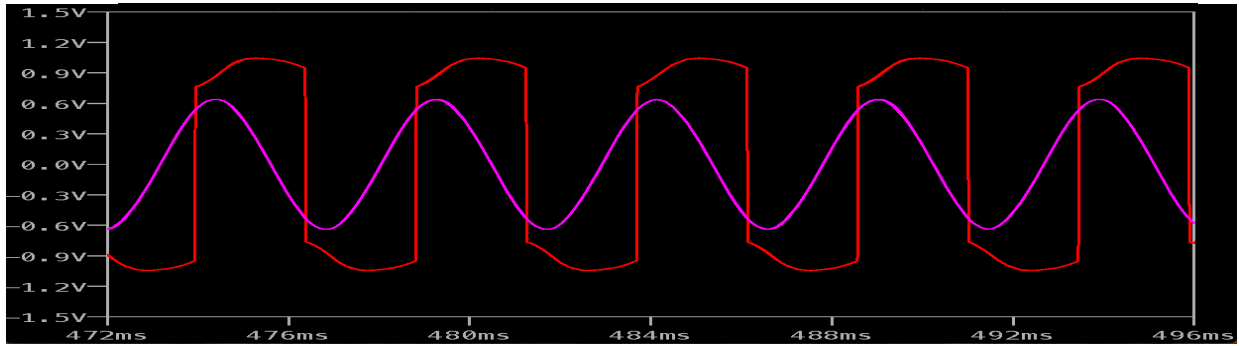
In the final stage, we have a full-bridge rectifier comprised of Schottky diodes (BAT54). The BAT54 diodes were chosen for two reasons. Firstly, the BAT54 has an extremely small forward voltage drop of  $0.2V$  as specified in the datasheet but was measured at  $0.085 mV$ . Secondly, the BAT54 allows little reverse current to flow through (around  $10 \mu A$ ). Also, on the rectifier side is a DC voltage source ( $V_{rect,s}$ ), which sets the square-wave amplitude to the optimal amplitude ( $V_{opt,non-ideal}$ ) at each frequency. This was done manually with a regular DC power supply, and later on with the microcontroller DAC, connected via a buffer (LM358). The output resistor ( $R_L$ ) was chosen to be  $100 \Omega$  so that the current supplied by the DC source  $V_{rect,s}$  would always be positive.  $I_{rect,s}$  is equal to  $\frac{V_{rect}}{R_L} - I_{BF}$ , where  $I_{BF}$  is the current supplied by the bias-flip circuit to the rectifier as shown in Figure 5-1. Lastly, a capacitor  $C_1 = 1 \mu F$  is placed in parallel with the load resistor. Figure 5-2 shows the oscilloscope and LT Spice readings for  $V_{sq}$  with the optimal phase, frequency, and amplitude at three different frequencies. Also plotted, is the input to the

shaker table, which is in phase with the input voltage source. We notice a perfect match between LT Spice simulations and the oscilloscope readings.



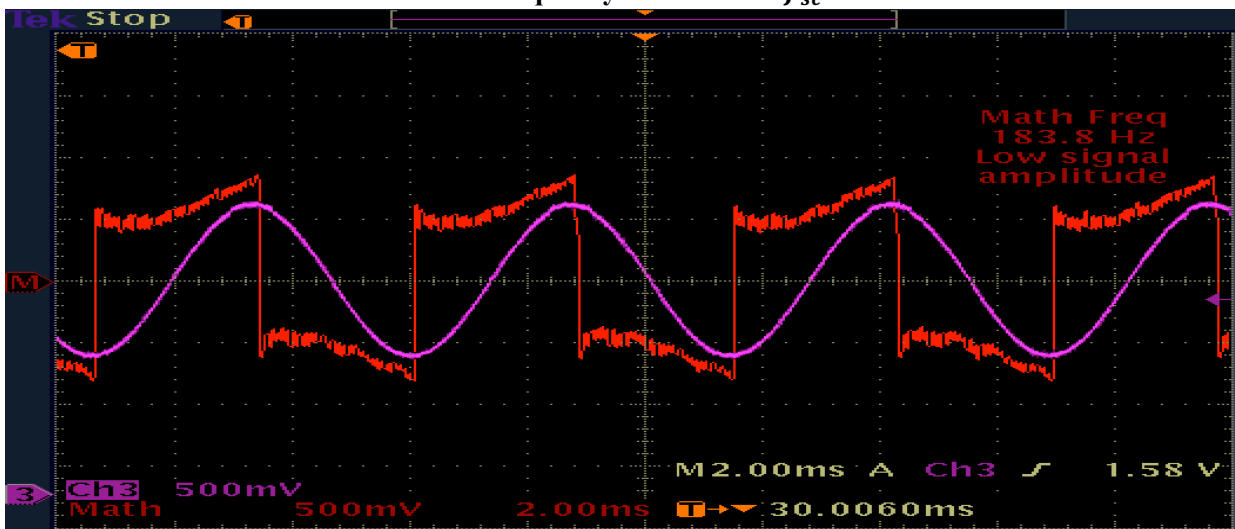
(a)





(b)

Source frequency =  $184 \text{ Hz} < f_{sc}$



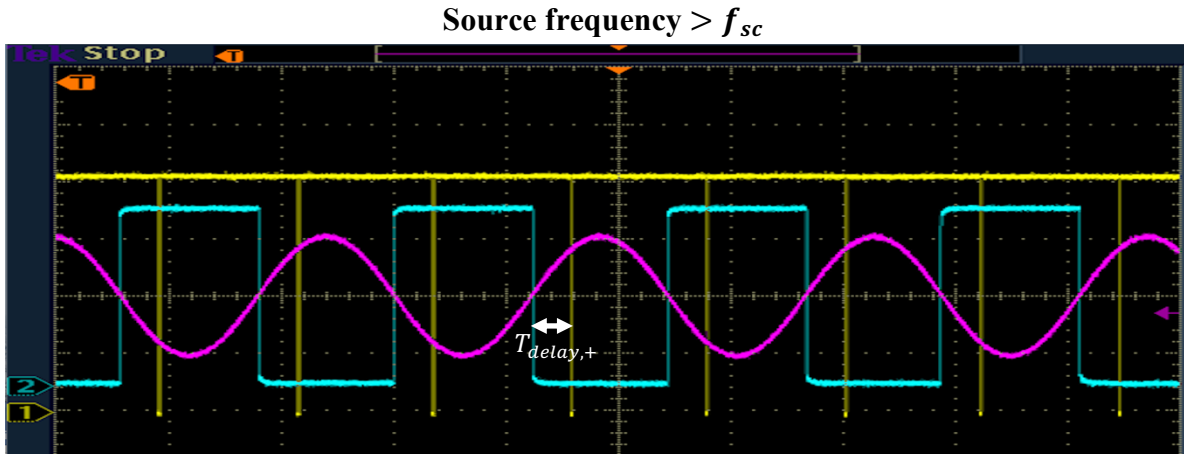
(c)

**Figure 5-2.** Oscilloscope and LT Spice plots of the square-wave ( $V_{sq}$ ) plotted in red, and the voltage sine-wave input plotted in purple at three frequencies (a)  $f = 188.8 \text{ Hz} \approx f_{sc}$ , (b)  $f = 205 \text{ Hz} > f_{sc}$ , and (c)  $f = 184 \text{ Hz} < f_{sc}$ .

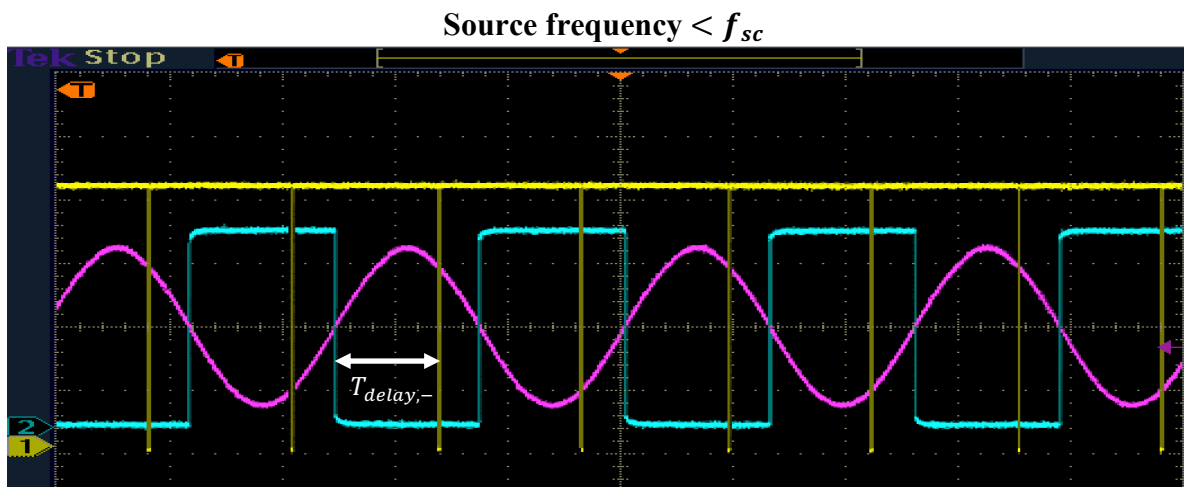
### Bias-flip switch input voltage:

In Chapter 4, we simulated the  $V_{sw}$  input voltage that controls the switch shown in Figure 4-5. While we know what the  $V_{sw}$  pulse train looks like, we have not yet established a practical method to create the pulse. The blue-shaded portion of Figure 5-1 shows the general procedure followed to create  $V_{sw}$ , such that the square-wave produced has the optimal phase shift ( $\phi_{sw,opt}$ ). As outlined in Figure. 5-1, the first step is to detect the zero-crossing of the input voltage source  $V_D \sin(\omega t)$ . However, the input voltage source is an abstract part of the electromechanical circuit model. Nonetheless, the accelerometer output voltage ( $V_{acc}$ ) is in phase with the input voltage source and therefore with a comparator we can detect zero-crossings. In Chapter 6, the controlling the bias-flip switch without an accelerometer is discussed. The microcontroller uses an external interrupt to detect changes in the comparator's output (rising edge or falling edge), then starts a timer, and waits  $T_{delay}$  seconds before signaling the monostable multivibrator to output a  $V_{sw}$  pulse. In Chapter 4, we derived  $T_{delay} = \frac{|\phi_{sq,opt}|}{2\pi f}$ . At source frequencies above  $f_{sc}$ ,  $\phi_{sq,opt}$  is positive and we therefore wait  $T_{delay+} = \frac{\phi_{sq,opt}}{2\pi f}$  seconds before sending a switch pulse. However, if the source frequency is below  $f_{sc}$ , then  $\phi_{sq,opt}$  is negative and we need to wait  $T_{delay-} = \frac{1}{2f} + \frac{\phi_{sq,opt}}{2\pi f}$  seconds before sending a switch pulse. The oscilloscope plots in Figure 5-3 shows how the  $V_{sw}$  pulse is formed.

$$T_{delay} \begin{cases} T_{delay+} = \frac{\phi_{sq,opt}}{2\pi f} & \text{for } f \geq f_{sc} & (5.1) \\ T_{delay-} = \frac{1}{2f} + \frac{\phi_{sq,opt}}{2\pi f} & \text{for } f < f_{sc} & (5.2) \end{cases}$$



(a)



(b)

**Figure 5-3.** Oscilloscope plot of accelerometer output, comparator output, and the input to the bias-flip produced by the monostable multivibrator at two distinct frequencies  
 (a) source frequency  $> f_{sc}$  and (b) source frequency  $< f_{sc}$ .

In Figure 5-3, the comparator's output (blue) toggles every time the accelerometer's output crosses zero (purple). The microcontroller senses the sudden change in comparator's output and waits the appropriate  $T_{delay}$  seconds before signaling the monostable multivibrator to form the input switch pulse (yellow). The bias-flip switch (MAX4716) switch turns on when the input is LOW, and off when the input is HIGH, which explains the shape of the monostable

multivibrator pulse. Table 5-1 summarizes the list of parts used in Figure 5-1 with the specified parameters and measured parameters shown. The microcontroller code used to form the  $V_{sw}$  pulse is given in the appendix (A3.2).

<b>PEHD Circuit Parameters</b>	<b>Value</b>	
Damping factor $R$	50.48 $K\Omega$	
Mass $L_m$	961.7 $H$	
Spring constant $C$	0.6637 $nF$	
Parasitic Capacitance $C_e$	$57.2 \times 10^{-9} F$	
Conversion Ratio $D$	$1.526 \times 10^{-3} N/V$	
Voltage Source $V_D$	2.794 $V$	

<b>Bias-flip Circuit Parts</b>	<b>Part Number</b>	<b>Value</b>
Bias-flip inductor ( $L_{BF}$ )	RFS1412-105KE	1 $mH$
Analog switch ( $SW_{BF}$ )	MAX 4716 (Maxim)	$R_{on} = 0.4 \Omega$
Zener diode	1N5222B (Vishay)	–
Measured Bias-flip resistance	–	18.5 $\Omega$

<b>Rectifier Circuit Parts</b>	<b>Part Number</b>	<b>Value</b>
Rectifier Schottky diodes	BAT54 (Vishay)	Measured $V_f = 85.1 mV$
Capacitor ( $C_1$ )	Film capacitor	1 $\mu F$
Load resistor ( $R_L$ )	–	100 $\Omega$

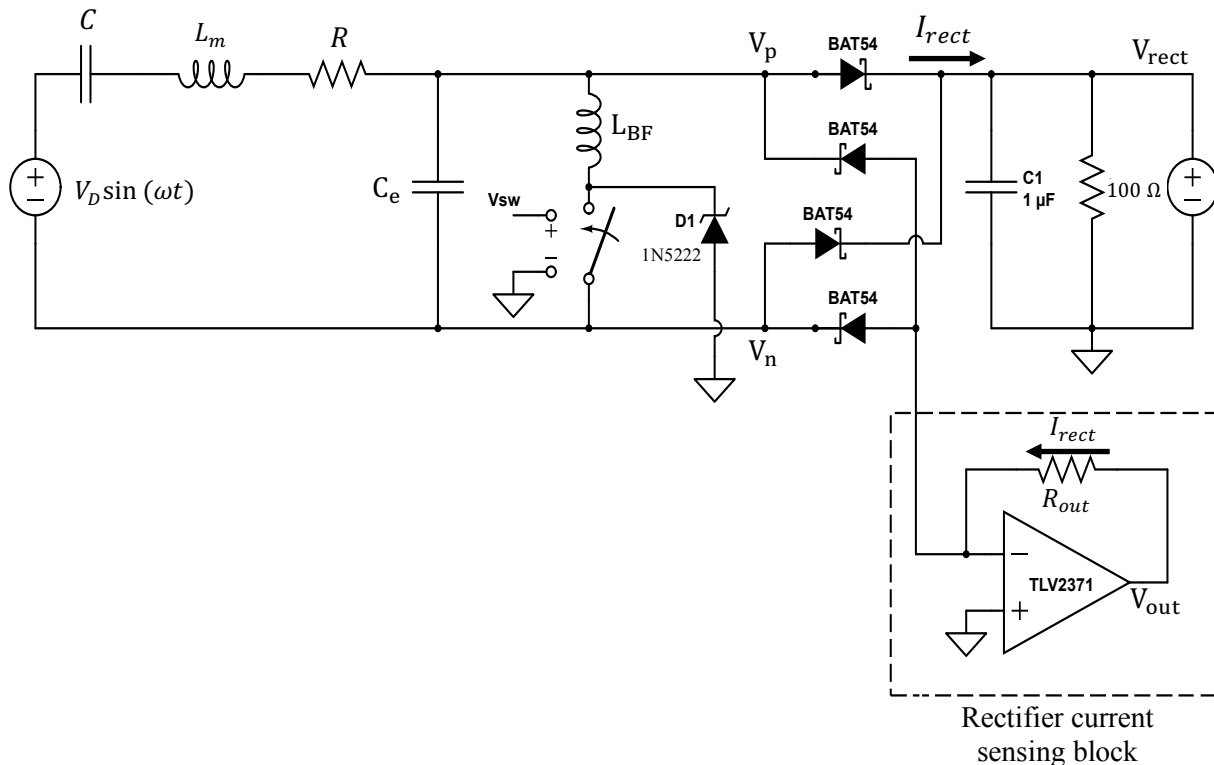
<b><math>V_{sw}</math> Control Hardware</b>	<b>Part Number</b>
Analog comparator	SN74LS08
Monostable multivibrator	CD4047BE
Op-amp	LM358
Microcontroller	Pyboard V1.1
Hex Inverter	SN74LS04

**Table 5-1.** List of parameters and parts used in the bias-flip circuit shown in Figure 5-1.

## 5.2 Power Measuring Techniques

The previous section presented the bias-flip circuit used in lab with all the details and control specifics. Now that a functional bias-flip circuit has been built, it's time to see how well it performs by measuring the improvements in power and bandwidth. The two power measurements of interest are: the power delivered by the harvester before rectification ( $P_{BR}$ ), and the power delivered after the rectifier ( $P_{AR}$ ). The difference between  $P_{BR}$  and  $P_{AR}$  is the power lost in the rectifier circuit.

In order to make the power measurements, the rectifier current sensing block has been added to the bias-flip circuit as shown in Figure 5-4. The rectifier current sensing block will be used to measure  $P_{AR}$  and  $P_{BR}$ .



**Figure 5-4.** Diagram of experimental bias-flip circuit with the current sensing block.



### Power delivered after rectification ( $P_{AR}$ ):

The instantaneous power delivered by the harvester in the rectifier is calculated as

$$P_{AR} = V_{rect} \times I_{rect}, \quad (5.3)$$

where  $V_{rect}$  and  $I_{rect}$  are given in Figure 5-1. Since  $V_{rect}$  is a DC voltage, we can write the

average power as 
$$\langle P_{AR} \rangle = \frac{V_{rect}}{T} \int_0^T I_{rect} dt = V_{rect} * \langle I_{rect} \rangle. \quad (5.4)$$

In order to find  $I_{rect}$  without affecting the operation of the circuit, the rectifier current sensing block was added as shown in Figure 5-4. The current through the feedback resistor ( $R_{out}$ ) is equal to  $I_{rect}$ , and therefore the output voltage  $V_{out} = I_{rect} R_{out}$ .

With  $I_{rect}$  on the order of  $10 \mu A$ , a relatively large feedback resistor ( $R_{out} = 20 k\Omega$ ) was chosen to measure  $V_{out}$  with reasonable accuracy. Finally, to find the average voltage

$\langle V_{out} \rangle$ , the microcontroller ADC was used to measure  $V_{out}$  at a sample-rate of  $200 * f_{ambient}$  for a duration 10 periods (for a total of 2000 samples). Since  $\langle I_{rect} \rangle = \frac{\langle V_{out} \rangle}{R_{out}}$ , we can write the average bias-flip power as

$$\langle P_{AR} \rangle = \frac{V_{rect}}{2000 R_{out}} \sum_{n=1}^{2000} V_{out} \quad (5.5)$$

In the next Section  $\langle P_{AR} \rangle$  is plotted with respect to frequency.

### Power delivered before rectification ( $P_{BR}$ ):

The average power delivered to the rectifier can be calculated as

$$\langle P_{BR} \rangle = \frac{1}{T} \int_0^T I_{rect} |V_p - V_n| dt, \quad (5.6)$$

where nodes  $V_p$  and  $V_n$  are labelled in Figure 5-4, and  $I_{rect}$  is the rectified current. Following the same calculation procedure as above, three ADCs were used to simultaneously measure

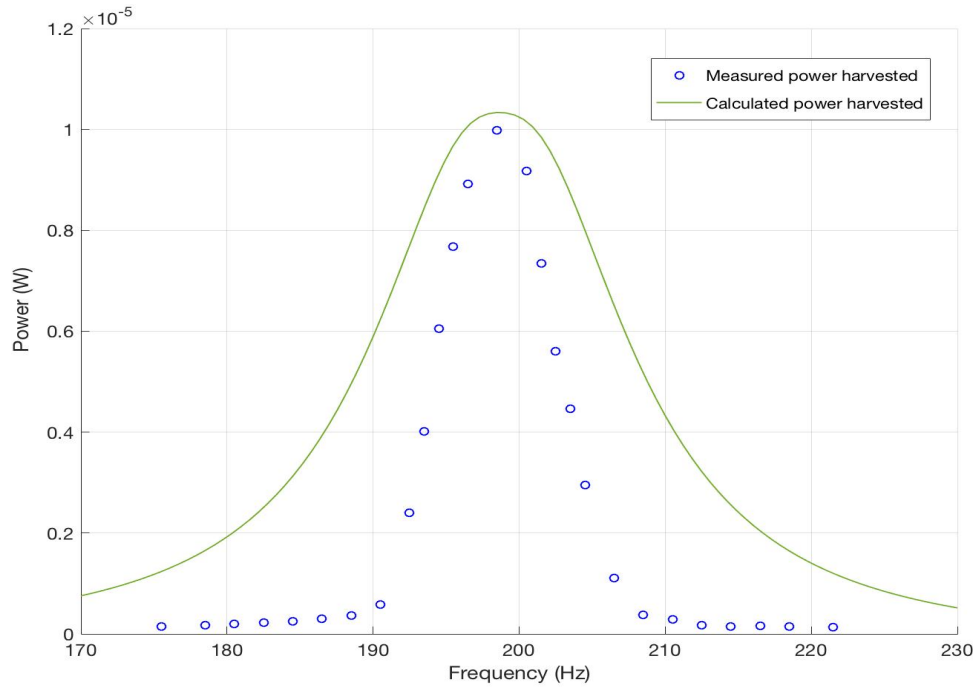
$I_{rect}$ ,  $V_p$ , and  $V_n$  at a sample rate of  $200 * f_{ambient}$  for a duration 10 periods. The sampled terms were then summed to find the average power, thus

$$\langle P_{BR} \rangle = \frac{1}{2000 R_{out}} \sum_{n=1}^{2000} V_{out} |V_p - V_n|$$

In the next section the average power harvested before rectification is plotted.

### 5.3 Experimental Results

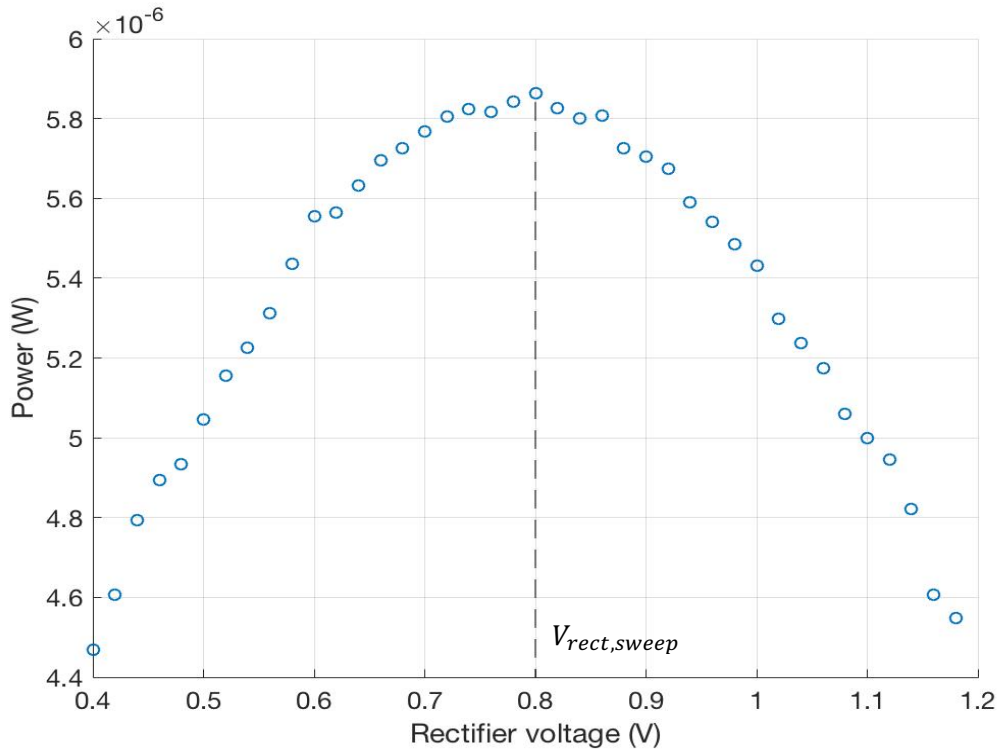
Using the experimental techniques outlined in Section 5.1, a square-wave was created with the optimal phase ( $\phi_{sq,opt}$ ), and amplitude ( $V_{opt,non-ideal}$ ). The power measuring techniques of Section 5.2 were used to calculate the power harvested after rectification. The results are plotted in Figure 5-5.



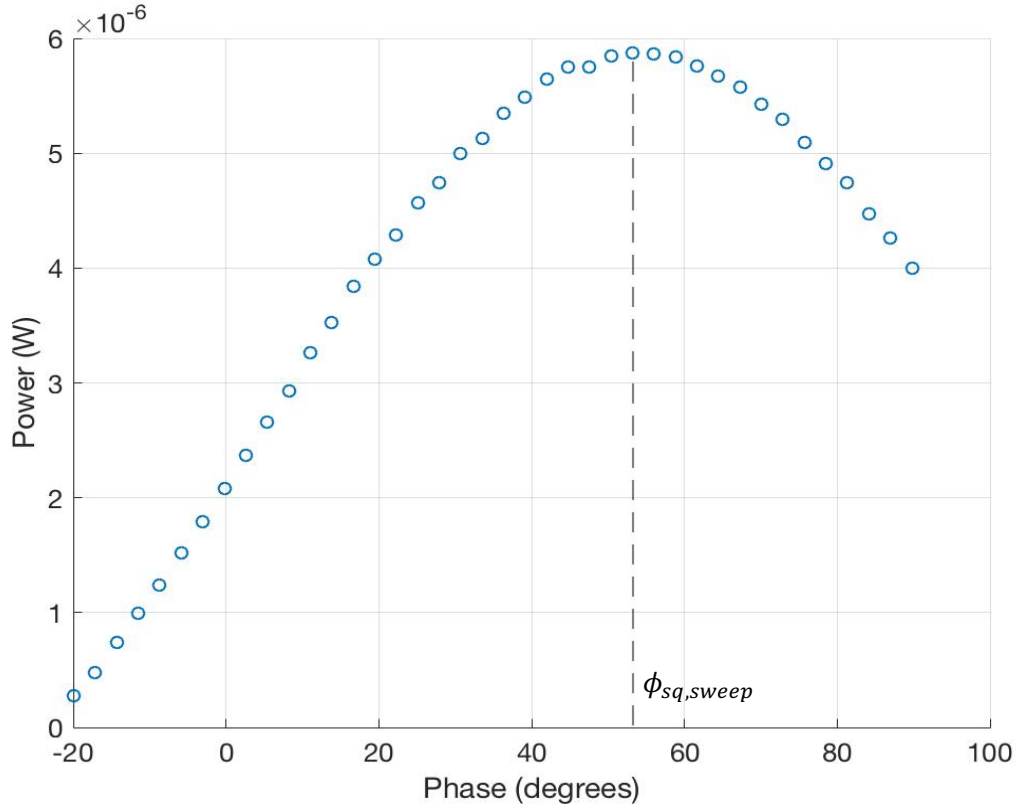
**Figure 5-5.** Measured and calculated power harvested after rectification using the optimal phase shift ( $\phi_{sq,opt}$ ) and amplitude ( $V_{opt,non-ideal}$ ) at 0.193g acceleration.

Phase and amplitude sweep for maximum power:

In order to assess how well the system was modelled, the phase  $\phi_{sq}$  and amplitude  $V_{rect}$  were swept at each frequency to find the value pairs  $(\phi_{sq,sweep}, V_{rect,sweep})$  that maximized harvested power. The phase and rectifier voltage sweeps were made with step increments of  $2.8^\circ$  and 0.2 V. At each new phase, the rectifier voltage does a sweep, recording the power harvested at each step. After the rectifier voltage completes its sweep, the phase increases by  $2.8^\circ$ , and the processes repeats itself. Figure 5-6 (a) plots the power harvested at 205 Hz at the optimal phase ( $53^\circ$ ) while sweeping the rectifier voltage. Figure 5.6 (b) plots the power harvested at 205 Hz while sweeping phase shift ( $\phi_{sq}$ ). In plot (b)  $V_{rect}$  is swept at each phase and the maximum power harvested is recorded. As expected, in Figure 5.6 (a) the rectifier voltage is swept at the optimal phase; hence, maximum power occurs when  $V_{rect} = V_{rect,sweep}$ . Likewise, in Figure 5.6 (b) maximum power occurs when the phase is equal to  $\phi_{sq,sweep} = 53^\circ$ .



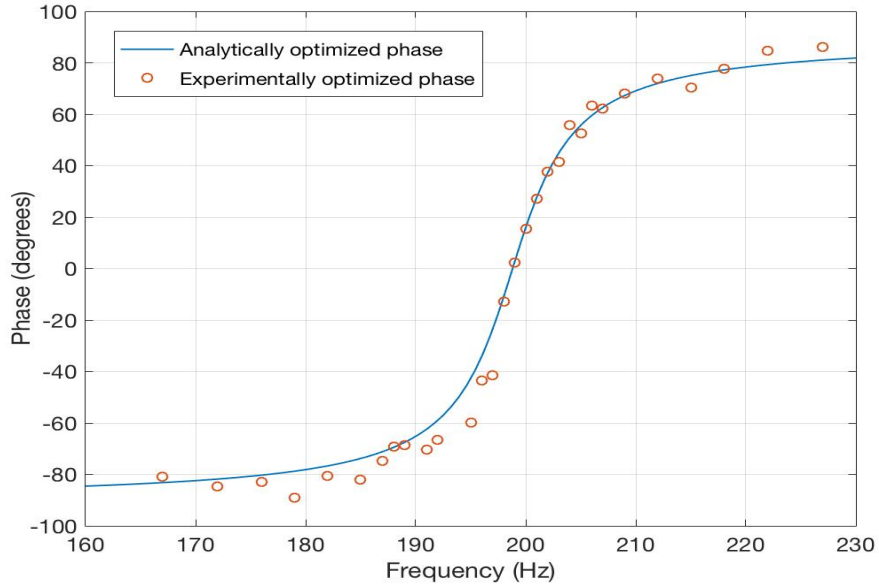
(a)



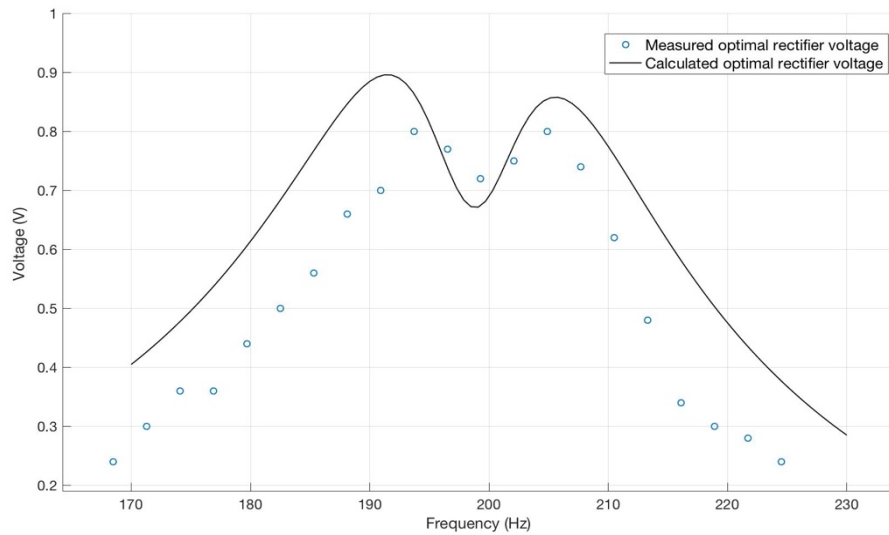
(b)

**Figure 5-6.** (a) Power harvested after the rectifier at  $f = 205 \text{ Hz}$  with respect to rectifier voltage. (b) Power harvested after the rectifier at  $f = 205 \text{ Hz}$  with respect to phase shift.

The pair values  $(\phi_{sq,sweep}, V_{rect,sweep})$  that maximized power at each frequency were recorded. If the PEHD were perfectly modelled, a smooth match at each frequency would be expected between  $\phi_{sq,sweep}$  and the optimal phase shift  $(\phi_{sq,opt})$ , and  $V_{rect,sweep}$  and the optimal rectifier voltage  $(V_{rect,non-ideal})$ .  $\phi_{sq,sweep}$ , and  $\phi_{sq,opt}$  are both plotted with respect to frequency in Figures 5.7, and  $V_{rect,sweep}$  and  $V_{rect,non-ideal}$  are plotted with respect to frequency in Figure 5.8. It is evident in the plots that the measured and calculated optimal amplitude do not align very well. A possible explanation for this is variations in the bias-flip efficiency at different frequencies, which will be discussed in detail in the next section.

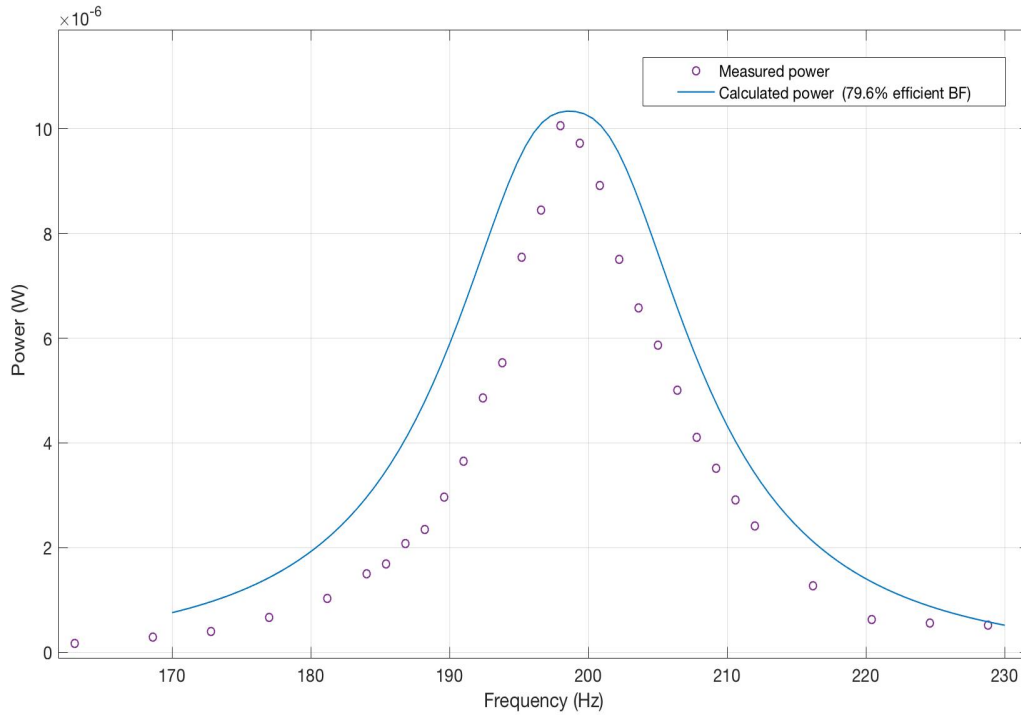


**Figure 5-7.** Measured optimal phase ( $\phi_{sq,sweep}$ ) and calculated optimal phase ( $\phi_{sq,opt}$ ) plotted with respect to frequency.

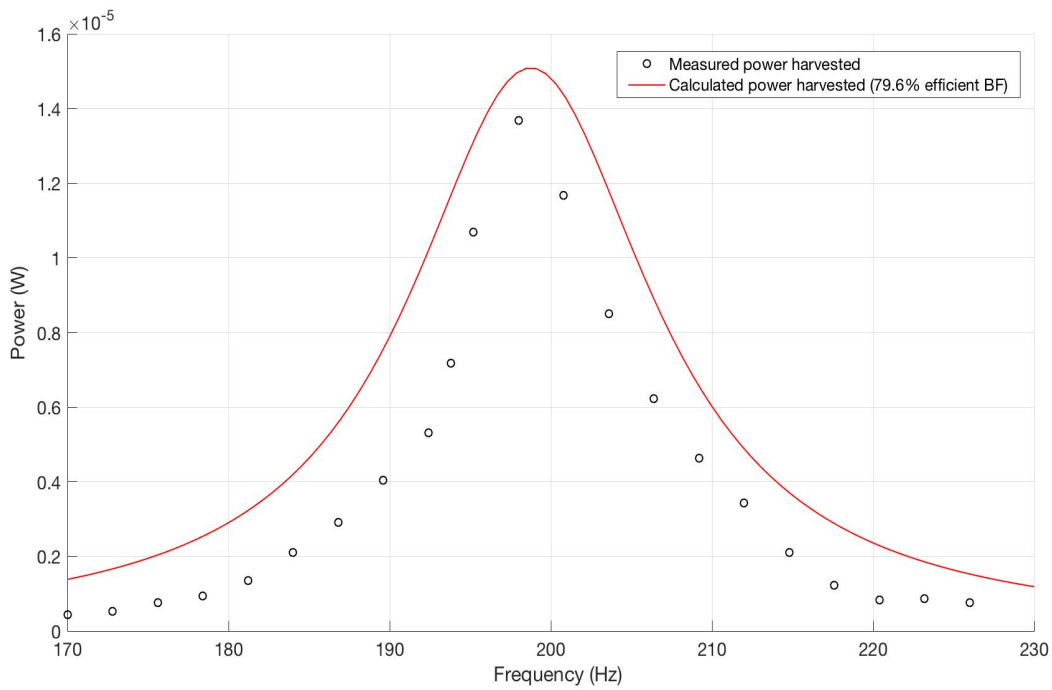


**Figure 5-8.** Measured optimal amplitude ( $V_{rect,exp}$ ) and calculated optimal amplitude ( $V_{rect,non-ideal}$ ) plotted with respect to frequency.

The maximum power harvested after the rectifier ( $P_{opt,exp}$ ) is measured by sweeping through phase and amplitude at every frequency and is plotted in Figure 5-9. We notice that the difference between the calculated and measured power harvested increases as we move away from resonance on both sides. This discrepancy will be explained in Section 5.4. Finally, to wrap up this section, a plot of the harvested power before loss in the rectifier is shown in Figure 5-10.



**Figure 5-9.** Measured and calculated maximum power harvested after the bridge rectifier ( $P_{opt,exp}$ ) with a 79.6% efficient bias-flip circuit with respect to frequency.



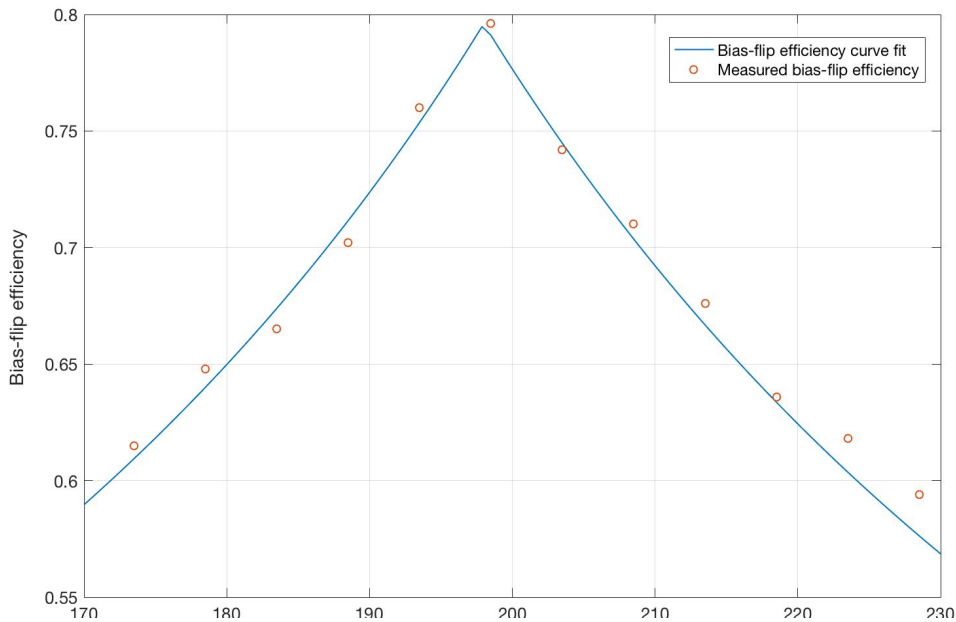
**Figure 5-10.** Measured and calculated maximum power harvested before rectification with a 79.6% efficient bias-flip circuit with respect to frequency.

## 5.4. Experimental Bias-flip Efficiency

In Chapter 4, the bias-flip efficiency ( $\eta_{BF}$ ) was calculated at resonance, and so far, has been assumed to be constant at all vibration frequencies. Nonetheless, after noticing a huge discrepancy between the measured bias-flip power and the calculated bias-flip power as shown in Figure 5-9, the BF efficiency was examined for an explanation. In order to measure the bias-flip efficiency, I took the ratio of  $\frac{V_+}{V_-}$  as done Figure 4-11 at each frequency. In Figure 5-11, the measured BF efficiency is plotted with respect to frequency. As we can see, the efficiency at resonance is highest, and begins to decrease as we move away from the resonant frequency. To simplify the analysis, the efficiency is fitted with a curve (plotted in Figure 5-11) whose equation is equal to

$$\eta_{BF}(fit) = \frac{0.796}{1 + \frac{1}{80} |f - 198|}, \quad (5.7)$$

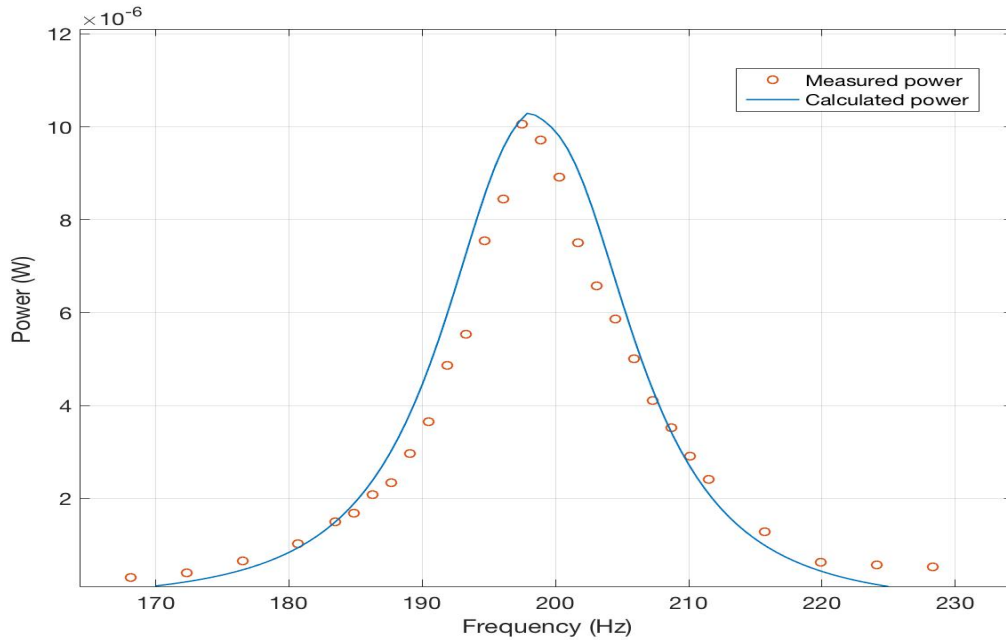
where  $f$  is the source vibration frequency.  $\eta_{BF}(fit)$  models the bias-flip efficiency's behavior with frequency and will be used in all future calculations.



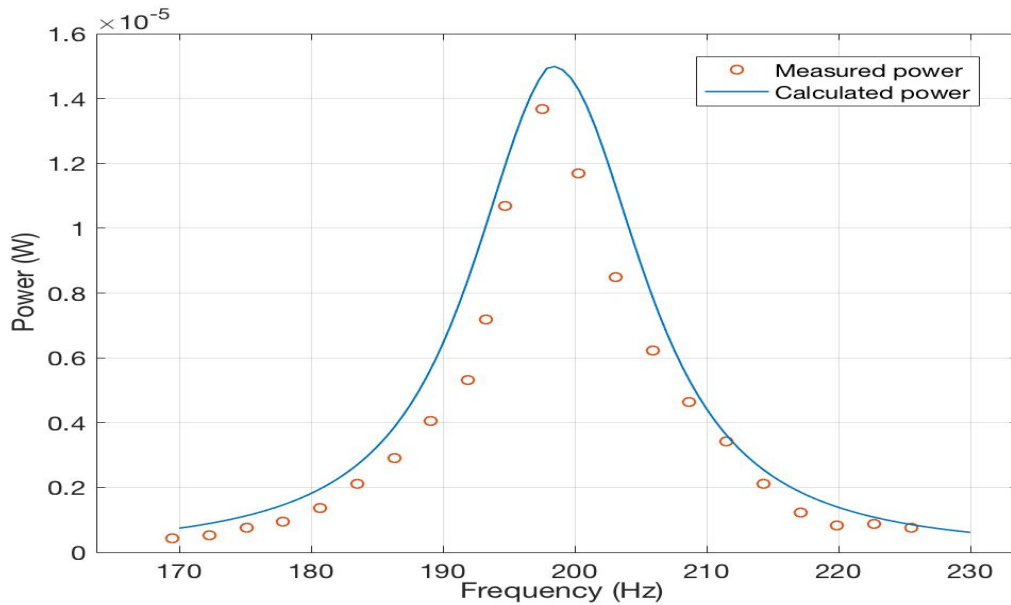
**Figure 5-11.** Measured bias-flip efficiency at different frequencies and BF-efficiency curve-fit.

The calculated power harvested is updated with the new equation for BF efficiency  $\eta_{BF}(fit)$ .

The measured and calculated power harvested after and before rectification are plotted in Figures 5-12, and 5-13, respectively.



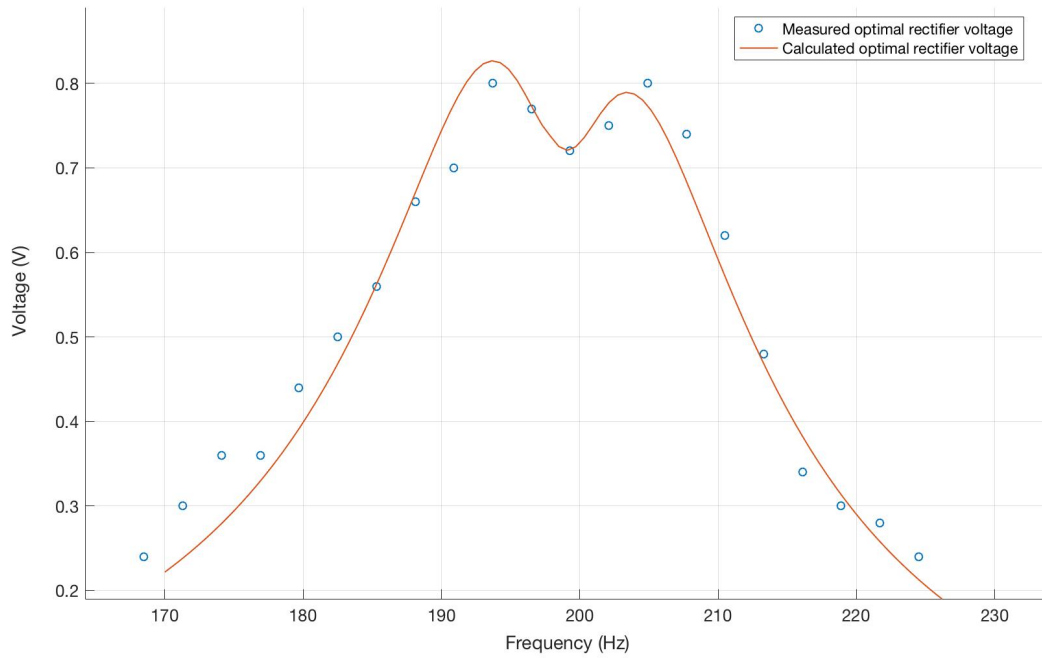
**Figure 5-12.** Measured and calculated power harvested after the bridge rectifier with updated bias-flip efficiency ( $\eta_{BF}(fit)$ ).



**Figure 5-13.** Measured and calculated power harvested before rectification with updated bias-flip efficiency ( $\eta_{BF}(fit)$ ).



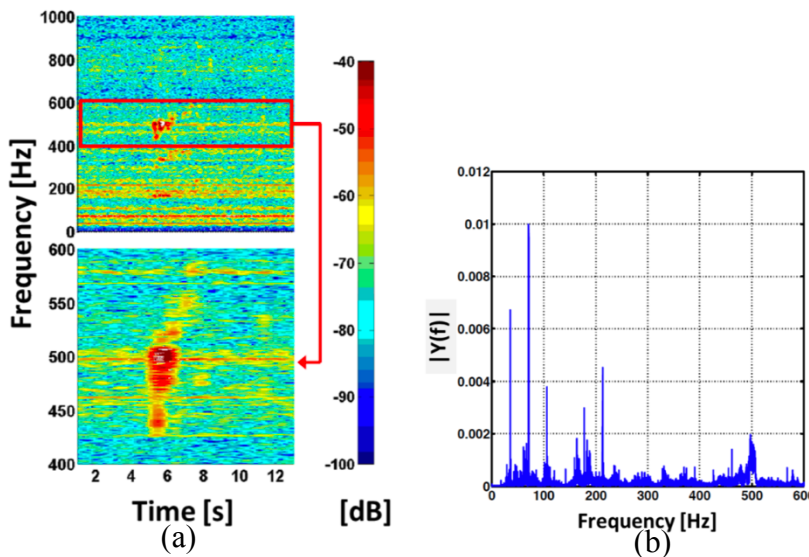
In Figure 5-8 in the previous section, we noticed a big mismatch between the calculated and measured optimal rectifier voltage ( $V_{rect,non-ideal}$ ) and ( $V_{rect,sweep}$ ).  $V_{rect,non-ideal}$  and  $V_{rect,sweep}$  are plotted again in Figure 5-14, with the bias-flip efficiency changed to the more appropriate  $\eta_{BF}(fit)$ .



**Figure 5-14.** Measured and calculated optimal rectifier voltage with bias-flip efficiency updated to  $\eta_{BF}(fit)$ .

## 5.5. Bias-flip Electronics in the Real World

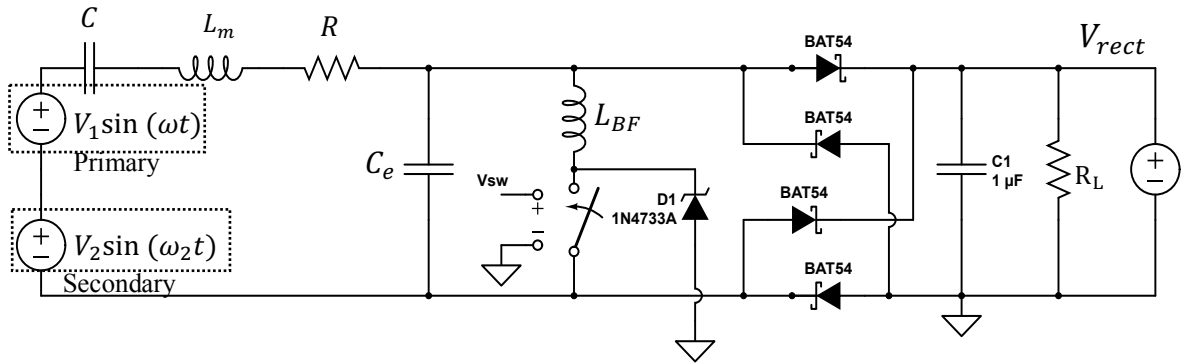
Throughout this thesis, there has been a strong emphasis on real-world applications, and in the real-world certain complications arise. The most pressing of these complications is changes and uncertainty in the ambient vibration frequency, and the bias-flip method was proposed as a solution. Another concern, however, is the presence of other vibration frequencies in the source. Vibration sources are spectrally rich, and it is not uncommon for multiple frequencies with equal prominence to be present [11]. As an example, an office window, vibrating due to high winds, is analyzed in Figure 5-15. The vibrations are measured of the window, and we notice at least 5 vibration frequencies of considerable strengths [11].



**Figure 5-15.** (a) Spectrogram and (b) spectrum of vibrations measured off an office window [11].

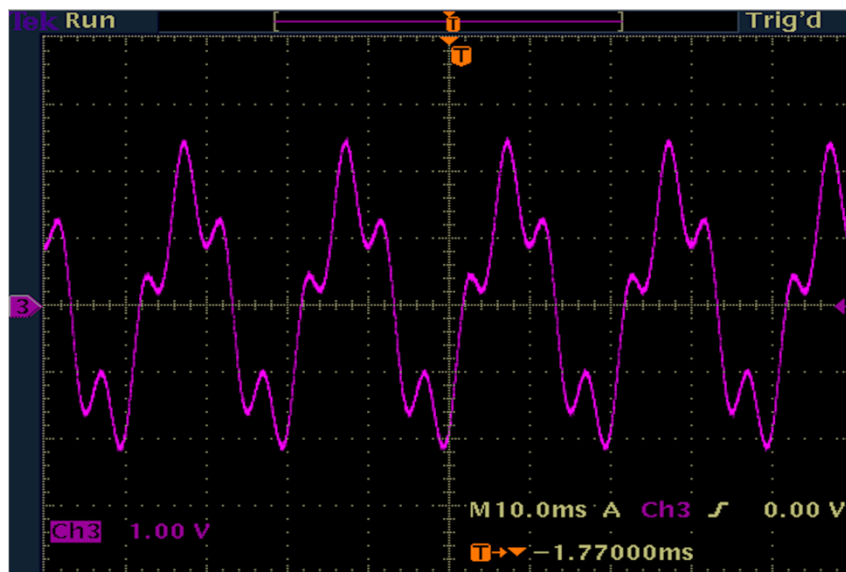
In order to assess the bias-flip's resiliency in an environment with multiple vibration frequencies, an experiment was conducted. In this experiment, a second vibration at a different frequency is superposed on top of the original frequency, from which the bias-flip circuit harvests energy. The primary purpose of this experiment is not to harvest energy from the secondary vibrating source, but rather to evaluate the extent to which the bias-flip power

harvested from the primary source is degraded. With the secondary vibrating source placed in series with the primary vibrating source, we get the circuit shown in Figure 5-16.



**Figure 5-16.** Equivalent PEHD bias-flip circuit with two input voltage sources that represent vibrations at two distinct frequencies.

To model the secondary vibrating frequency, I placed a secondary voltage sine-wave at frequency  $\omega_2$  in series with the primary voltage sine-wave at frequency  $\omega$ . The amplitudes were chosen such that  $V_2 = 1.5 * V_1$ . The resulting waveform, shown in Figure 5-17, is the input to the shaker table. According to my experimental findings, the secondary vibration frequency does not have a noticeable effect on the bias-flip power harvested from the primary source.



**Figure 5-17.** Input to shaker-table with primary and secondary sine-waves in series. The primary and secondary frequencies are 200 Hz and 100 Hz.

In Table 5-2, the power harvested with primary frequency at 200 Hz is measured with different secondary frequencies. The voltage amplitudes of primary and secondary signals are equal. The distorted waveform shape in Figure 5-17 makes it extremely difficult to use the comparator to track zero-crossings in the primary voltage source. Since the primary voltage source is generated by the microcontroller DAC, the zero-crossing could be detected internally without the use of any external hardware (i.e. no comparator). Apart from the zero-crossing detection method, everything else concerning the control the bias-flip circuit is left unchanged. In order to compare the results on fair grounds, the maximum power harvested in Table 5-2 was found by sweeping amplitude and phase.

Secondary Frequency (Hz)	Power harvested ( $\mu W$ )
50	9.198
100	9.057
150	9.042
250	9.073
350	9.068
500	9.146

**Table 5-2.** Bias-flip power harvested with primary voltage source at  $f = 200$  Hz at different secondary voltage source frequencies.

## 5.6 Chapter Summary

This chapter detailed the design considerations and hardware choices for the bias-flip circuit, rectifier, and switch control. A summary of all the parts used is given in Table 5-1. Furthermore, the procedure used to implement the optimal phase-shift and amplitude was discussed in detail. The experimental results for power harvested were then presented, as well as the methods used to extract these results. After realizing a discrepancy between the calculated and experimental plots, the bias-flip efficiency was inspected for an explanation. After updating the bias-flip efficiency, the calculated power harvested was replotted, and we noticed a much better match between the measured and calculated values. Finally, the bias-flip circuit's resiliency in an environment with multiple frequencies was put to test. This was done by superposing a second source of vibration, at a different frequency than the primary source. We learnt that the bias-flip's ability to harvest power was unaffected by the addition of the second vibration frequency.



# Chapter 6

## Summary and Conclusions

### 6.1 Summary

The main goal of this thesis is to extend the power-bandwidth of the piezoelectric energy harvester. Vibration energy harvesters are extremely effective at harvesting vibration energy when the ambient vibration frequency is matched to harvester's resonant frequency. As the ambient vibration frequency deviates from the resonant frequency, the harvested power drops tremendously. Nonetheless achieving this frequency match is unlikely because vibrating sources may exhibit frequency shifting and/or be at an unknown frequency. Even if the ambient vibration frequency is known before-hand, manufacturing tolerances make it hard to achieve a perfect frequency match. The motivation behind this research is, therefore, to experimentally verify that the bias-flip method is capable of mitigating the bandwidth problem. With a more flexible power bandwidth, the real-world applications of the harvester are vast.

Chapter 2 developed the PEHD electromechanical circuit model (Figure 2-3) by employing the spring-mass damper model. The equivalent electrical circuit model, shown in Figure 2-4, lumps the interdependent sources of electromechanical circuit model into a single circuit. The experimental set-up is then presented, which comprises of the piezoelectric

harvester, shaker table, accelerometer and processor. The next step is to characterize the harvester, and this is done using the data collection system to measure the open-circuit voltage and short-circuit current. With a fully characterized harvester, we move on to examine the power harvesting capabilities of the PEHD with and without the bias-flip electronics.

In Chapter 3, we explore the power delivery potential of the piezoelectric energy harvester electrically loaded with passive components. The theoretical maximum power is delivered with conjugate load matching. However, the large size of the of the load inductor required for conjugate load matching raises practicality concerns. Furthermore, power bandwidth remains a problem when conjugate load matching is implemented at a single frequency. A harvester electrically loaded with a resistor delivers less power at all frequencies, and still suffers from poor power bandwidth. Finally, the full-bridge rectifier, used to harvest DC power, is introduced. The forward rectifier diode drop is measured and presented in Figure 3-16, and correspondingly the total power lost in the bridge rectifier is approximated. The results of chapter are summarized in Figure 3-19, which underscores the severity of the power bandwidth problem.

In the ideal scenario, we would want conjugate load matching at every frequency. This would require a tunable load inductor and resistor. Using the bias-flip method, we can use a switch in series with a small inductor to mimic the behavior of a much larger tunable inductor, by creating an approximate square-wave at the output side. Chapter 4 explains both the ideal and non-ideal (lossless) bias-flip method in detail, deriving the optimal phase and amplitude for the square-wave. With an ideal bias-flip circuit close approximately the theoretical maximum power can be harvested. The bias-flip circuit efficiency is then measured, allowing the calculation of the approximate power harvested in the non-ideal bias-flip circuit. What we realized is the power harvested with an ~80% efficient bias-flip circuit is well below that of the

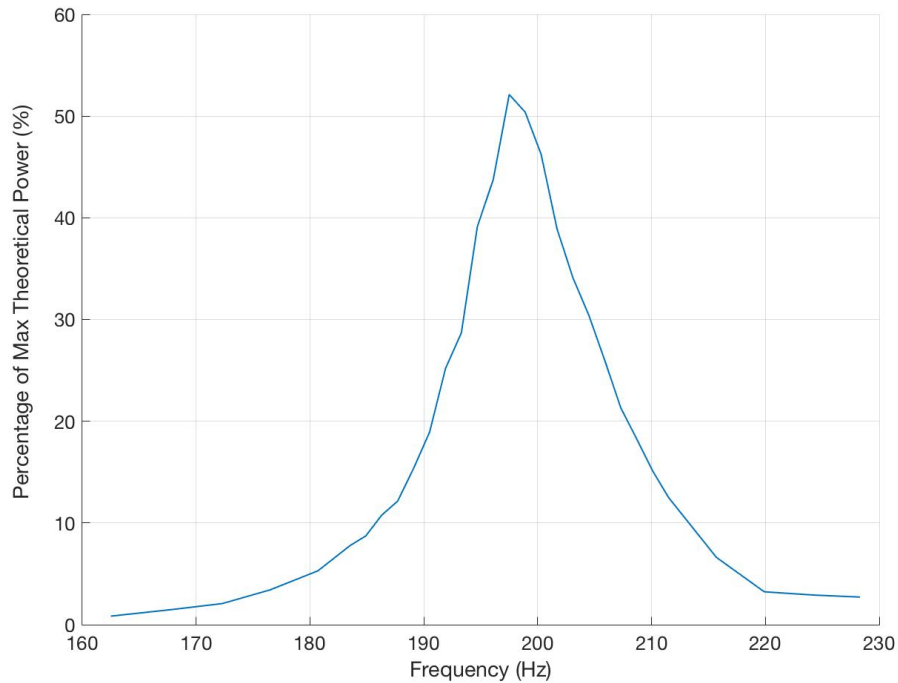


ideal bias-flip circuit. Even so, calculations show that the power harvested can be improved by  $\sim 1.6x$  at resonance, and  $\sim 4.8x$  at 10 Hz away from resonance, when compared to the power harvested in a purely resistive load. With promising calculations, we now move on see how well the bias-flip method actually does in experiments.

In Chapter 5, the design considerations as well as the hardware choices for the bias-flip circuit, rectifier circuit, and switch control are discussed in detail. The complete bias-flip circuit, used in experiments is presented in Figure 5-1, with all the relevant components listed in Table 5-1. We then move on to measure the power harvested after the bridge rectifier using the optimal phase shift and amplitude equations derived in the previous chapter. The results are plotted in Figure 5-5. In order to assess how well the PEHD was modelled, the maximum power harvested was measured at every frequency by sweeping through phase and amplitude. We realized that the optimal phase derived in Chapter 4 aligned really well with the sweep optimal phase as shown in Figure 5-7; however, the same couldn't be said about the amplitude (Figure 5-8). The maximum power measured with the sweeps before and after rectification is shown in Figures 5-9 and 5-10, respectively. The discrepancy between the measured and calculated optimal amplitude occurred because efficiency was assumed as constant, but in reality, efficiency decreased significantly away from resonance. The updated plots for the power harvested, and the square-wave amplitude are shown in Figures 5-12, 5-13, and 5-14. In the end, the bias-flip circuit's ability to harvest power with a second vibrating source superposed onto the first was examined. We found that the power harvested was unaffected by the addition of a second frequency.

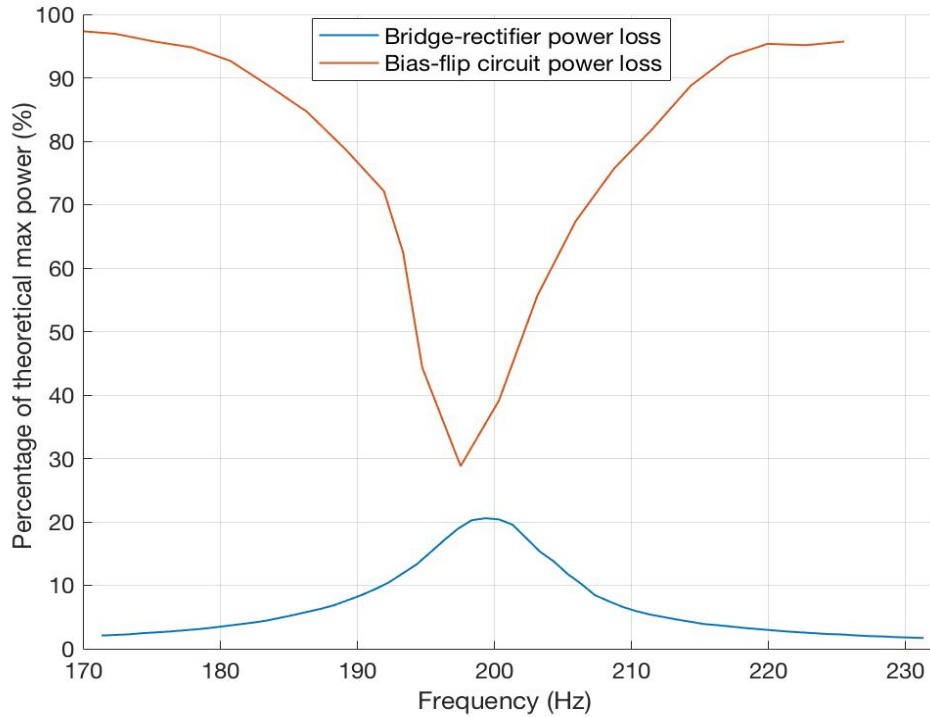
## 6.2 Conclusions

With an ideal bias-flip circuit and lossless diode bridge approximately the theoretical maximum power can be harvested ( $19.29 \mu W$ ). However, the bias-flip circuit efficiency was measured at 79.6%, and consequently there is some power lost in the bias-flip circuit. Moreover, power is lost in the diode-bridge rectifier. In Figure 6-1, the measured power harvested with the bias-flip circuit is plotted as a percentage of the theoretical maximum power.



**Figure 6-1.** Power harvested with bias-flip circuit after rectification as a percentage of the theoretical maximum power ( $19.29 \mu W$ ) with respect to frequency.

With the bias-flip circuit around 52% of the theoretical maximum power could be harvested at resonance. Also, moving only 10 Hz away from resonance, the power harvested as a percent of the theoretical maximum drops to around 20%. There are two sources of power loss as mentioned above: the bias-flip circuit and the full-bridge rectifier. In Figure 6-2, the power lost in the bias-flip circuit and the power lost in the bridge rectifier are plotted as a percentage of the theoretical maximum power with respect to frequency. It is evident in Figure 6-2 that the bias-flip circuit is the dominant source of power loss, especially at frequencies away from resonance.



**Figure 6-2.** Power lost in the bias-flip circuit and bridge rectifier as a percentage of the maximum theoretical power ( $19.29 \mu W$ ) with respect to frequency.

The power lost in the bias-flip circuit was derived in Chapter 4 and is caused by three intrinsic resistances: the BF inductor ESR, the BF switch on-resistance, and the PEHD's parasitic resistance. Calculations show that the PEHD's parasitic resistance ( $R_p$ ) is responsible for  $\sim 89\%$  of the power lost in the bias-flip circuit. That said, the harvested power can be significantly improved by manufacturing the PEHDs such that they have lower parasitic resistances. Lastly, calculations show that increasing the bias-flip inductor size improves the bias-flip efficiency. In fact, increasing the bias-flip inductor size by an order of magnitude improves the efficiency by around 7%. In conclusion the PEHD is such a high Q-resonant system, that the odd-harmonics (3<sup>rd</sup> and above) from the square-wave load are inconsequential from a power perspective, which means almost perfect conjugate load matching can be achieved. However, it is apparent that the non-ideal bias-flip circuit seriously degrades the amount of power harvested, and in the best case (at resonance) around 51% of the theoretical power could be harvested.



# Appendices

# Appendix A

## A.1 MATLAB Code Scrips

All the calculated plots shown in this thesis were made with the following MATLAB script.

```
% PEHD Parameters
C= 57.2e-9;
B=0.1177013659104880379848454801968;
M=0.002251532955928133813516882776921;
K=3512.940588607725892723517258485;
D=0.001526915913006145843208336379631;

% Acceleration
Acc = 1.893;

% Load Impedances
R_L=15000;
X_L= 11.1*2*pi*f;

% Frequency Range
f = linspace(170,230,100);

% Bias-flip efficiency
efficiency= 0.796./(1+abs(f-198)/80);

A = (K + (D^2)/C - M*(2*pi*f).*(2*pi*f))
Y = (-M*(2*pi*f).*(2*pi*f)+K);
Z = ((2*pi*f*B).*(2*pi*f*B));
J = (2*pi*f*C);

%%%%% reactance %%%%%%
X = -(A.*Y+Z)./(J.*(A.*A + Z));

%%%%% resistance %%%%%%
R = ((D^2)*(B/C^2))./(A.*A + Z);

%%%%% Open-circuit Voltage %%%%%%
V_open = ((D/C)*M*Acc)./sqrt(A.*A + Z);

%%%%% Theoretical Maximum Power %%%%%%
power_optimal = (V_open).*(V_open)./(8.*R);

%%%%% Optimal Resistive Load %%%%%%
```

```

h= D^2 - (2*pi*f).*(2*pi*f)*M*C + C*K;
n = B;
o = (2*pi*f*B*C);
p = (2*pi*f*M)- K./(2*pi*f);
R_optimal = sqrt((n.*n + p.*p)./(h.*h + o.*o));

%%%%%% Optimal Resistive Power %%%%%%%%%%
P_optimal_res =
(V_open.*V_open/2).*(R_optimal./(X.*X+(R_optimal+R).*(R_optimal+R)));

%%%%%% Load Voltage %%%%%%%%%%
V_load = (V_open).*abs(15000./(i*X+R+15000));

%%%%%% Load Resistor Power %%%%%%%%%%
p_res =(V_open.*V_open/2).*(R_L./((R_L+R).*(R_L+R)+(X).*(X)));

%%%%%% Load resistor and inductor Power %%%%%%%%%%
p_opt_ind =(V_open.*V_open/2).*(R_L./((R_L+R).*(R_L+R)+(X_L+X).*(X_L+X)));

%%%%%% Load Inductor for Conjugate Load Matching %%%%%%%%%%
L_load = (-X)./(2*pi*f);

%%%%%% Ideal BF optimal rectifier voltage %%%%%%%%%%
V_rect = ((M*Acc*pi)/(D*B*8))*sqrt(((2*pi*f*M)-(K./(2*pi*f)))*((2*pi*f*M)-
(K./(2*pi*f)))+B^2);

%%%%%% BF optimal phase shift %%%%%%%%%%
phase_delay = (180/pi)*atan((2*3.14159*f*M - K./(2*3.14159*f))/B);

%%%%%% Open-circuit voltage phase shift %%%%%%%%%%
v_open_phase= (-180/pi)*atan((D^2+K*C-M*C*(2*pi*f).*(2*pi*f))./(2*pi*f*C*B));

%%%%%% Power lost in BF circuit with ideal rectifier voltage used %%%%%%%%%%
P_BF_loss = (C*f).*(V_rect.*V_rect).*(1-efficiency.*efficiency);

%%%%%% Ideal BF Power %%%%%%%%%%
P_BF_opt = power_optimal;

%%%%%% X_s impedance term %%%%%%%%%%
impedance=sqrt(((2*pi*f*M)-(K./(2*pi*f)))*((2*pi*f*M)-(K./(2*pi*f)))+B^2);

%%%%%% Optimal Square-wave amplitude for non-ideal BF %%%%%%%%%%
v_opt_nonideal = (M*Acc/(D*pi))./((C/D^2)*(1-
efficiency.*efficiency).*f.*(impedance)+(8/pi^2)*(B./impedance));

%%%%%% non-ideal BF power harvested %%%%%%%%%%
P_non_ideal = (2/pi)*(D*M*Acc*v_opt_nonideal./impedance) -
(8/pi^2)*(B*(D^2)*v_opt_nonideal.*v_opt_nonideal)./(impedance.*impedance)-
C*(1-efficiency.*efficiency).*f.*v_opt_nonideal.*v_opt_nonideal;

%%%%%% power loss in non-ideal BF circuit %%%%%%%%%%
P_non_ideal_loss= C*(1-
efficiency.*efficiency).*f.*v_opt_nonideal.*v_opt_nonideal;

%%%%%% power lost in non-ideal BF rectifier %%%%%%%%%%

```

```

P_rect_loss=(2*0.135)*(P_non_ideal./(v_opt_nonideal));

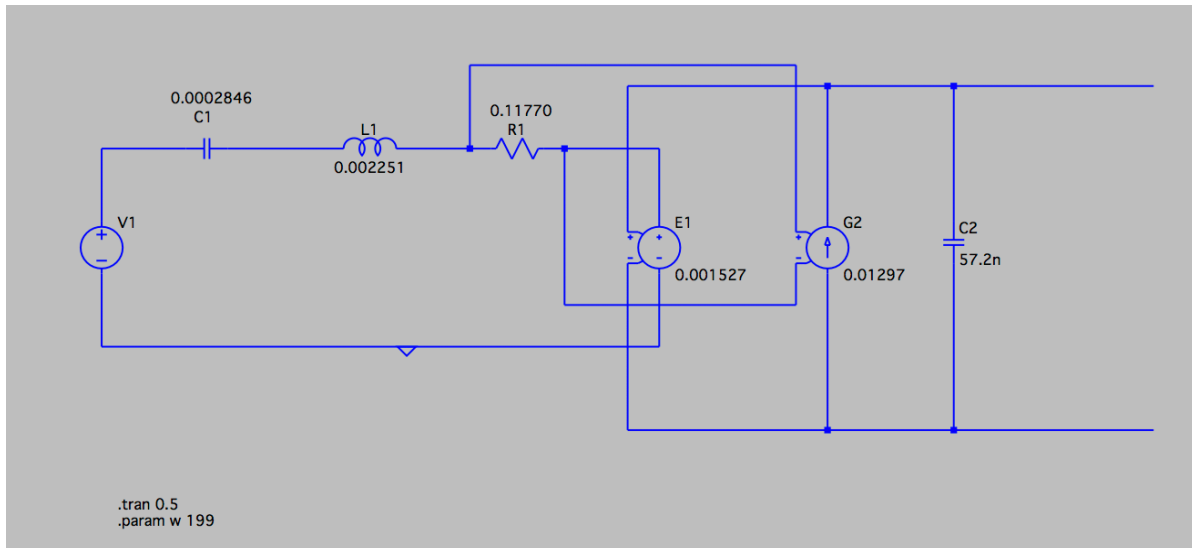
%plot(f,X)
%plot(f,R)
%plot(f,V_open)
%plot(f,power_optimal)
%plot(f,L_load)
%plot(f,R_optimal)
%plot(f,P_optimal_res)
%plot(f,V_load)
%plot(f_res,R_m)
%plot(f,V_rect-0.17)
%plot(f,phase_delay)
%plot(f,v_open_phase)
%plot(f,p_opt_ind)
%plot(f,P_non_ideal./p_res)
%plot(f,(max(p_res-(4*0.0851*V_load)/(pi*R_L),0)))
%plot(f,(P_non_ideal)./(p_res-(4*0.0851*V_load)/(pi*R_L)))
%plot(f,P_BF_loss)
%plot(f,P_BF_opt)
%plot(f,P_BF_opt-P_BF_loss)
%plot(f,P_BF_opt-P_BF_rectloss)
%plot(f,P_non_ideal)
%plot(f,P_non_ideal)
%plot(f,P_non_ideal_loss)
%plot(f,P_rect_loss)
%plot(f,efficiency)
%plot(f,v_opt_nonideal-0.17)
%plot(f,0.0000000572*f.*(v_opt_nonideal.*v_opt_nonideal).*(1-
efficiency.*efficiency))
%plot(f,v_opt_nonideal-0.17)

```



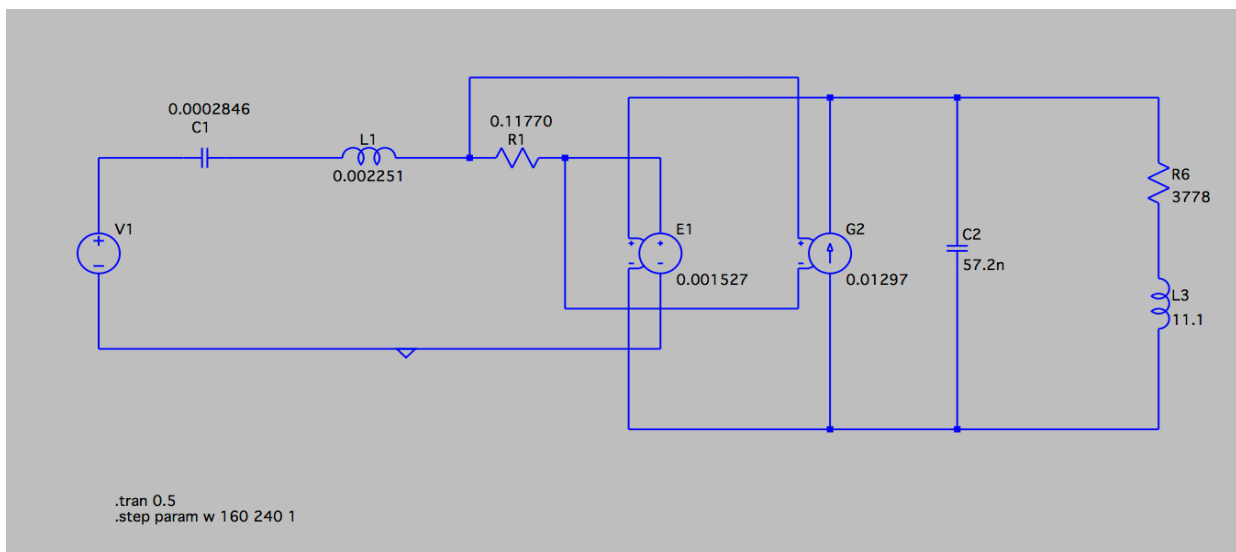
## A.2 LT Spice Simulations

### A.2.1 Chapter 2 PEHD Circuit

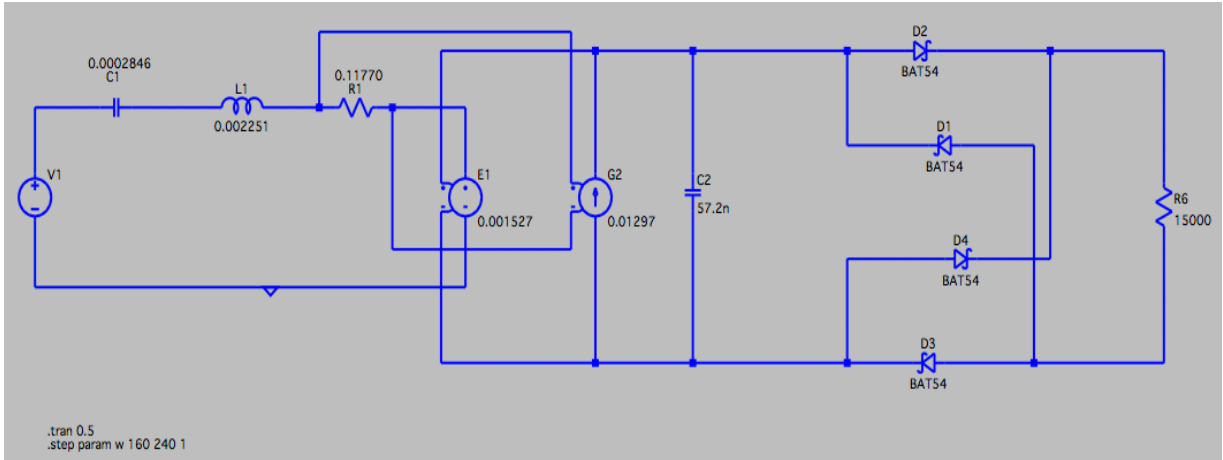


### A.2.2 Chapter 3 PEHD Circuit

#### A2.2.1 - AC Power Delivered to Load

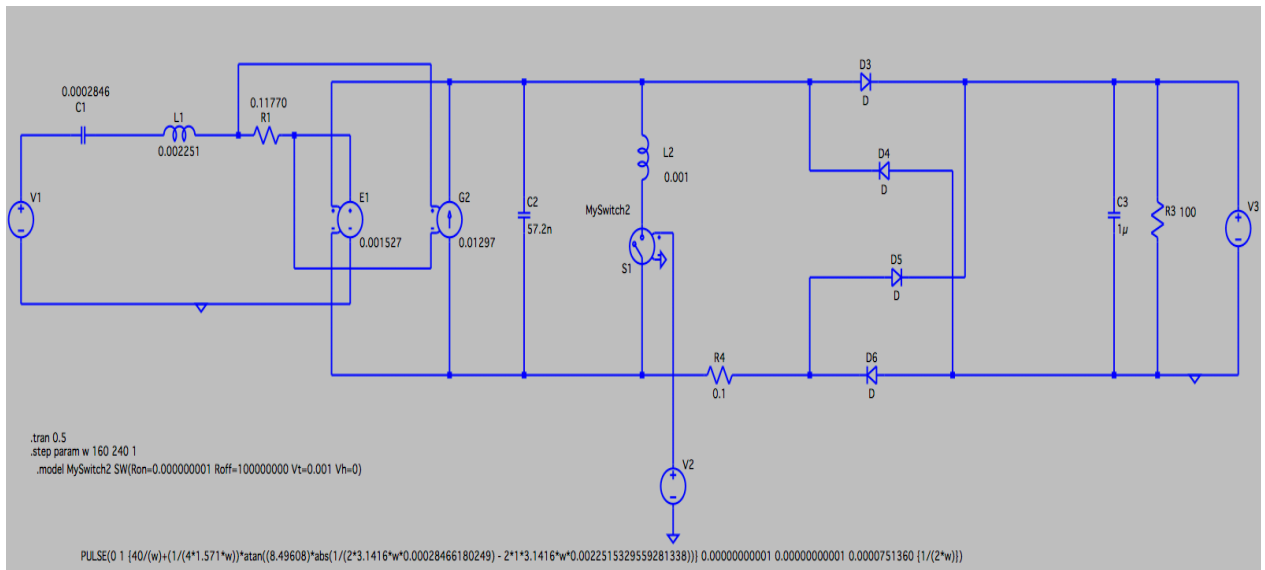


### A.2.2.2 - DC Power Delivered to Load

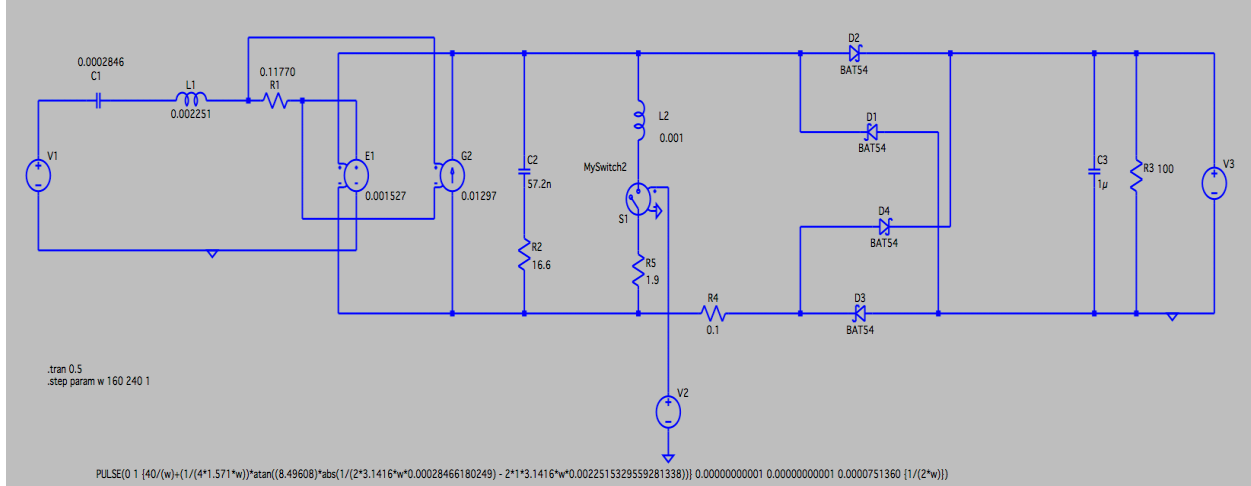


## A.2.3 Chapter 4 Bias-flip Circuit

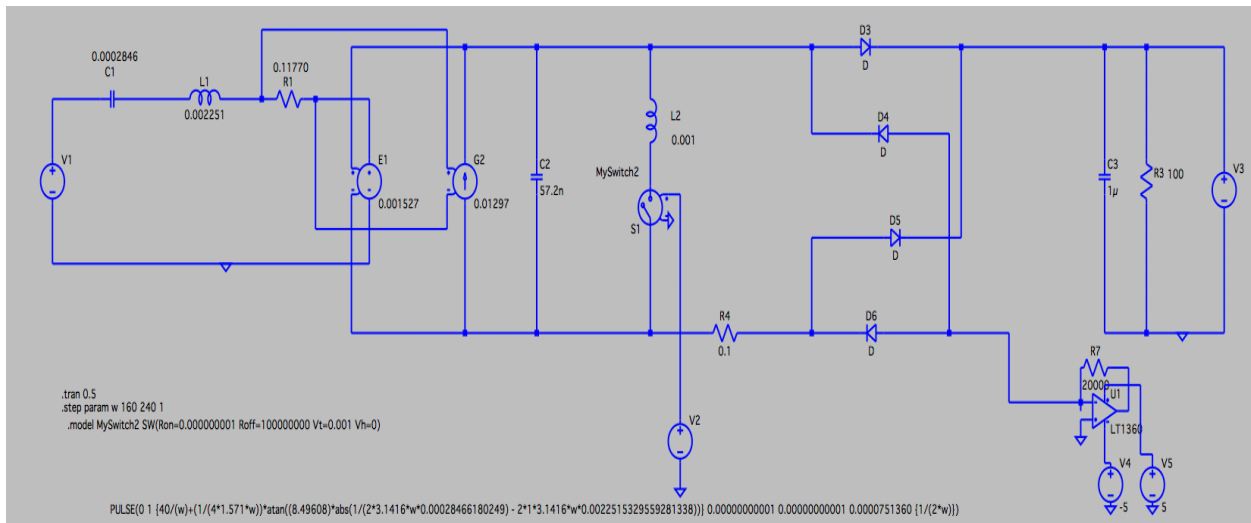
### A.2.3.1 - Ideal Bias-flip Circuit



### A2.3.2 - Non-ideal Bias-flip Circuit



### A.2.4 Chapter 5 Experimental Bias-flip Circuit



## A.3 Microcontroller Code (Pyboard V1.1)

### A.3.1 Data Acquisition Frequency Sweeper

This code is used in Chapters 2 and 3 to maintain constant acceleration, while sweeping frequency. The open-circuit voltage is measured, as well as the voltage into the loads.

```
import math
import pyb
from array import array
from pyb import DAC
from pyb import Timer
from pyb import ADC
from pyb import delay
from pyb import Pin

amplitude = 45          #controls the amplitude of the sine wave
                          #generated (initial value shown)
frequency = 160         #the start frequency of the sine wave
led=pyb.LED(1)
ledd=pyb.LED(2)
led_end = pyb.LED(3)
adc=ADC(Pin('X19'))
adc_2=ADC(Pin('X7'))
dacc = DAC(2, bits = 12)
count = 0
list_a = []
list_b=[]
list_adc = []
list_VOC = []          #this will be a list of lists

# create a buffer containing a sine-wave, using half-word samples
buf = array('H', int(2048 + int(2047 * math.sin(2 * math.pi * i /
128))/amplitude)-1500 for i in range(128))
dac = DAC(1, bits=12)
dac.write_timed(buf, frequency * len(buf), mode=DAC.CIRCULAR)
led.toggle()
ledd.toggle()

while frequency<241:
    adc_max = 0          #maximum value of ADC
    adc_min = 5000      #minimum value of ADC

    while (int(3.333*(adc_max-adc_min))>int(13.6*195) or
int(3.333*(adc_max-adc_min))<int(13.6*192)):          #this while loop
helps us find the right amplitude (standard vals: 998, 989)
        buf = array('H', int(2048 + int(2047 * math.sin(2 * math.pi *
i / 128))/amplitude)-1500 for i in range(128))
```

```

dac.write_timed(buf, frequency * len(buf), mode=DAC.CIRCULAR)
adc_max = 0 #maximum value of ADC
adc_min = 5000 #minimum value of ADC
pyb.delay(500)
list_a = []
count = 0
start = pyb.micros()

while count < 241: #This allows us to
find the list of values in the ADC
    if pyb.elapsed_micros(start) > 1000000/(frequency*201):
        val = adc.read()
        list_a.append(val)
        ledd.toggle()
        count+=1
        start = pyb.micros()

for adc_measure in list_a: #get the max and min ADC values
    if adc_measure >= adc_max:
        adc_max=adc_measure
    if adc_measure <= adc_min:
        adc_min=adc_measure
whisk = int(3.333*(adc_max-adc_min))

if (whisk) > int(13.6*195):
    amplitude += 0.1

if (whisk) < int(13.6*192):
    amplitude -= 0.1

ledd.toggle()
list_adc.append(whisk)
buf = array('H', int(2048 + int(2047 * math.sin(2 * math.pi * i /
128))/amplitude)-1500 for i in range(128))
dac.write_timed(buf, frequency * len(buf), mode=DAC.CIRCULAR)
frequency+=1
pyb.delay(1000)
ledd.toggle()

#setting all of the constants and timer to zero
start = pyb.micros()
count_2 = 0
list_b = []
Voc_max = 0
Voc_min = 5000
while count_2 < 201: #create a list with
all entries at a frequency
    if pyb.elapsed_micros(start) > 1000000/(frequency*201):
        v_oc = adc_2.read()
        list_b.append(v_oc)

```

```

        count_2+=1
        start = pyb.micros()

    for v_open in list_b:
        voltage
        #measure the maximum OC
        if v_open >= Voc_max:
            Voc_max = v_open
        if v_open <= Voc_min:
            Voc_min = v_open

        V_append = (Voc_max-Voc_min)/2
        list_VOC.append(V_append*(3.3/4095))
        #appending
        true value to the list

list_VOC = map(str, list_VOC)
list_VOC = ', '.join(list_VOC)

f = open('data.txt', 'w')
f.write(list_VOC)
f.close()

```

## A.3.2 Bias-flip Circuit Control

The code used here controls the bias-flip switch, creating the optimal phase and amplitude.

```
import math
import pyb
from array import array
from pyb import DAC
from pyb import Timer
from pyb import ADC
from pyb import delay
from pyb import Pin

amplitude = 40          #controls the amplitude of the sine wave
generated (initial value shown)
frequency = 205         #the start frequency of the sine wave
led=pyb.LED(1)
ledd=pyb.LED(2)
led_end = pyb.LED(3)
adc=ADC(Pin('X19'))
adc_2=ADC(Pin('X7'))
dac = DAC(1, bits=12)
comp_ref = DAC(2,bits=12)
res_freq = 0
switch_control = Pin('X2', Pin.OUT_PP)
switch_control.value(1)
phase_verify = Pin('X22', Pin.OUT_PP)
phase_verify.value(1)
time_micros = pyb.Timer(2, prescaler=83, period=0x3fffffff)
time_micros.counter(0)
count = 0
list_a = []
list_adc = []
sine_timer = pyb.Timer(4, prescaler=int(84000000/(128*frequency)) - 1,
period=127)
buff = bytearray(10000)

##### PZ EHD Parameters
#####
B_PZ = 0.1177013659104880379848454801968
D_PZ = 0.001526915913006145843208336379631
M_PZ = 0.002251532955928133813516882776921
K_PZ = 3512.940588607725892723517258485

##### Sine wave generator
#####
```

```

buf = array('H', int(2048 + int(2047 * math.sin(2 * math.pi * i /
128))/amplitude)-1850 for i in range(128))

dac.write_timed(buf, frequency * len(buf), mode=DAC.CIRCULAR)
led.toggle()

if frequency<250:
    adc_max = 0                #maximum value of ADC
    adc_min = 5000            #minimum value of ADC

    while (int(3.333*(adc_max-adc_min))>int(13.6*195) or
int(3.333*(adc_max-adc_min)<int(13.6*192))):        #this while loop
helps us find the right amplitude (standard vals: 998, 989)
        buf = array('H', int(2048 + int(2047 * math.sin(2 * math.pi *
i / 128))/amplitude)-1850 for i in range(128))
        dac.write_timed(buf, frequency * len(buf), mode=DAC.CIRCULAR)
        adc_max = 0                #maximum value of ADC
        adc_min = 5000            #minimum value of ADC
        pyb.delay(500)
        list_a = []
        count = 0
        start = pyb.micros()

        while count < 201:                #This allows us to
find the list of values in the ADC
            if pyb.elapsed_micros(start) > 1000000/(frequency*201):
                val = adc.read()
                list_a.append(val)
                ledd.toggle()
                count+=1
                start = pyb.micros()

        for adc_measure in list_a:        #get the max and min ADC values
            if adc_measure >= adc_max:
                adc_max=adc_measure
            if adc_measure <= adc_min:
                adc_min=adc_measure
        whisk = int(3.333*(adc_max-adc_min))

        if (whisk) > int(13.6*195):
            amplitude += 0.1

        if (whisk) < int(13.6*192):
            amplitude -= 0.1

led.toggle()
list_adc.append(whisk)
##### setting manual amplitude to control values ##### 35.1
for 199 ;41.7 for 205

```



```

    #amplitude=41.7
    buf = array('H', int(2048 + int(2047 * math.sin(2 * math.pi * i /
128))/amplitude)-1850 for i in range(128))
    dac.write_timed(buf, frequency * len(buf), mode=DAC.CIRCULAR)
    sine_timer.counter(0)

    frequency+=1
    pyb.delay(1000)
    led_end.toggle()

##### sine wave (V1) data
#####
offset = 1.725
amp = 10.851*3.3*(2047/(4095*amplitude))

##### Timing Calculations
#####

phase_delay = math.atan((2*3.14159*frequency*M_PZ -
K_PZ/(2*3.14159*frequency))/B_PZ)
time_delay = (1000000*phase_delay)/(2*3.14159*frequency)

if time_delay >=0:
    res_freq=1
    maximum=1
    trig_1= int((127/4)*(phase_delay)/(3.1416/2))
    trig_2= int(127/2 + (127/4)*(phase_delay)/(3.1416/2))
    comp_ref.write(4000)

else:
    maximum=1
    trig_1= int(127/2 + (127/4)*(phase_delay)/(3.1416/2))
    trig_2= int(127 + (127/4)*(phase_delay)/(3.1416/2))
    comp_ref.write(1)

##### Trigger Code
#####

while True:
    if res_freq==1:
        if maximum ==1:
            if sine_timer.counter()== trig_1:
                switch_control.value(0)
                start_micros = time_micros.counter()
                end_micros = time_micros.counter()
                while end_micros - start_micros
<(1000000/(4*frequency)):

```

```

        end_micros = time_micros.counter()
        switch_control.value(1)
        maximum =0
    else:
        if sine_timer.counter()== trig_2:
            switch_control.value(0)
            start_micros = time_micros.counter()
            end_micros = time_micros.counter()
            while end_micros - start_micros
<(1000000/(4*frequency)):
                end_micros = time_micros.counter()
                switch_control.value(1)
                maximum =1

    else:
        if maximum ==1:
            if sine_timer.counter()== trig_1:
                switch_control.value(0)
                start_micros = time_micros.counter()
                end_micros = time_micros.counter()
                while end_micros - start_micros
<(1000000/(4*frequency)):
                    end_micros = time_micros.counter()
                    switch_control.value(1)
                    maximum =0

            else:
                if sine_timer.counter()== trig_2:
                    switch_control.value(0)
                    start_micros = time_micros.counter()
                    end_micros = time_micros.counter()
                    while end_micros - start_micros
<(1000000/(4*frequency)):
                        end_micros = time_micros.counter()
                        switch_control.value(1)
                        maximum =1

```

## A.3.2 Bias-flip Amplitude and Phase Sweep

```
import math
import pyb
from array import array
from pyb import DAC
from pyb import Timer
from pyb import ADC
from pyb import delay
from pyb import Pin

amplitude = 32          #controls the amplitude of the sine wave
                          generated (initial value shown)
frequency = 200         #the start frequency of the sine wave
led=pyb.LED(1)
ledd=pyb.LED(2)
led_end = pyb.LED(3)
adc=ADC(Pin('X19'))
adc_2=ADC(Pin('X7'))
dac = DAC(1, bits=12)
comp_ref = DAC(2, bits=12)
res_freq = 0
switch_control = Pin('X2', Pin.OUT_PP)
switch_control.value(1)
phase_change = Pin('X22', Pin.OUT_PP)
phase_change.value(0)
start_control=Pin('X12', Pin.OUT_PP)
start_control.value(1)
time_micros = pyb.Timer(2, prescaler=83, period=0x3fffffff)
time_micros.counter(0)
count = 0
list_a = []
list_adc = []
phases=0
sine_timer = pyb.Timer(4, prescaler=int(84000000/(128*frequency)) - 1,
period=127)
buff = bytearray(10000)

##### PZ EHD Parameters
#####
B_PZ = 0.1177013659104880379848454801968
D_PZ = 0.001526915913006145843208336379631
M_PZ = 0.002251532955928133813516882776921
K_PZ = 3512.940588607725892723517258485

##### Sine wave generator
#####
```

```

buf = array('H', int(2048 + int(2047 * math.sin(2 * math.pi * i /
128))/amplitude)-1850 for i in range(128))

dac.write_timed(buf, frequency * len(buf), mode=DAC.CIRCULAR)
led.toggle()

if frequency<250:
    adc_max = 0                #maximum value of ADC
    adc_min = 5000            #minimum value of ADC

    while (int(3.333*(adc_max-adc_min))>int(13.6*195) or
int(3.333*(adc_max-adc_min)<int(13.6*192))):        #this while loop
helps us find the right amplitude (standard vals: 998, 989)
        buf = array('H', int(2048 + int(2047 * math.sin(2 * math.pi *
i / 128))/amplitude)-1850 for i in range(128))
        dac.write_timed(buf, frequency * len(buf), mode=DAC.CIRCULAR)
        adc_max = 0                #maximum value of ADC
        adc_min = 5000            #minimum value of ADC
        pyb.delay(500)
        list_a = []
        count = 0
        start = pyb.micros()

        while count < 201:                #This allows us to
find the list of values in the ADC
            if pyb.elapsed_micros(start) > 1000000/(frequency*201):
                val = adc.read()
                list_a.append(val)
                ledd.toggle()
                count+=1
                start = pyb.micros()

        for adc_measure in list_a:        #get the max and min ADC values
            if adc_measure >= adc_max:
                adc_max=adc_measure
            if adc_measure <= adc_min:
                adc_min=adc_measure
        whisk = int(3.333*(adc_max-adc_min))

        if (whisk) > int(13.6*195):
            amplitude += 0.1

        if (whisk) < int(13.6*192):
            amplitude -= 0.1

led.toggle()
list_adc.append(whisk)
##### setting manual amplitude to control values ##### 32 for
199 ;41.7 for 205

```

```

    #amplitude=32
    buf = array('H', int(2048 + int(2047 * math.sin(2 * math.pi * i /
128))/amplitude)-1850 for i in range(128))
    dac.write_timed(buf, frequency * len(buf), mode=DAC.CIRCULAR)
    sine_timer.counter(0)

    frequency+=1
    pyb.delay(1000)
    led_end.toggle()

##### sine wave (V1) data
#####
offset = 1.725
amp = 10.851*3.3*(2047/(4095*amplitude))

##### Timing Calculations
#####
phase_delay = math.atan((2*3.14159*frequency*M_PZ -
K_PZ/(2*3.14159*frequency))/B_PZ)
time_delay = (1000000*phase_delay)/(2*3.14159*frequency)

trig_1_list=[]
trig_2_list=[]

if time_delay >=0:
    res_freq=1
    maximum=1
    trig_1= int((127/4)*(phase_delay)/(3.1416/2))
    trig_2= int(127/2 + (127/4)*(phase_delay)/(3.1416/2))
    comp_ref.write(4000)

else:
    maximum=1
    trig_1= int(127/2 + (127/4)*(phase_delay)/(3.1416/2))
    trig_2= int(127 + (127/4)*(phase_delay)/(3.1416/2))
    comp_ref.write(1)

for i in range(-10,0):
    entry=trig_1+i
    if entry<0:
        entry=entry+128
    elif entry > 127:
        entry=entry-128
    trig_1_list.append(entry)

for i in range(-10,0):

```

```

    entry_2=trig_2+i
    if entry_2<0:
        entry_2=entry_2+128
    elif entry_2 > 127:
        entry_2=entry_2-128
    trig_2_list.append(entry_2)

trig_1=trig_1_list[0]
trig_2=trig_2_list[0]

##### Amplitude Size for testing only
'''
whisk=str(amplitude)

f = open('data.txt', 'w')
f.write(whisk)
f.close()
'''

##### External Interrupt
def callback(line):
    phase_change.value(1)

extint = pyb.ExtInt(Pin('X3'), pyb.ExtInt.IRQ_FALLING,
pyb.Pin.PULL_UP, callback)

##### Trigger Code

start_control.value(0)

while True:
    if phase_change.value()==1:
        if phases <len(trig_1_list)+1:
            phases+=1
            trig_1=trig_1_list[phases]
            trig_2=trig_2_list[phases]
            phase_change.value(0)

        if maximum ==1:
            if sine_timer.counter()== trig_1:
                switch_control.value(0)
                start_micros = time_micros.counter()
                end_micros = time_micros.counter()
                while end_micros - start_micros
<(1000000/(4*frequency)):
                    end_micros = time_micros.counter()
                    switch_control.value(1)
                    maximum =0
            else:
                if sine_timer.counter()== trig_2:
                    switch_control.value(0)

```

```

        start_micros = time_micros.counter()
        end_micros = time_micros.counter()
        while end_micros - start_micros
<(1000000/(4*frequency)):
            end_micros = time_micros.counter()
            switch_control.value(1)
            maximum =1

import math
import pyb
from array import array
from pyb import DAC
from pyb import Timer
from pyb import ADC
from pyb import delay
from pyb import Pin

count=0
led=pyb.LED(1)
ledd=pyb.LED(2)
led_end = pyb.LED(3)
adc=ADC(Pin('X19'))
tim = pyb.Timer(3, freq=40000)           # create a timer running at
10Hz
lista=[]
list_b=[]
list_c=[]
list_d=[]
list_length=0
start = pyb.micros()
v_rect = DAC(1, bits=12)
phase_change = Pin('X22', Pin.OUT_PP)
start_control = Pin('X2', Pin.OUT_PP)
start_control.value(0)
phase_change.value(1)
frequency=201
times=10
sw=pyb.Switch()
list_max=[]

##### PE Parameters #####
B_PZ = 0.1177013659104880379848454801968
D_PZ = 0.001526915913006145843208336379631
M_PZ = 0.002251532955928133813516882776921
K_PZ = 3512.940588607725892723517258485
ACC = 1.893

v_rectifier =
((M_PZ*ACC)/(D_PZ*B_PZ*3.1416))*(((2*3.1416*frequency*M_PZ)-
(K_PZ/(2*3.1416*frequency))**2+(B_PZ)**2)**0.5
v_list=[]

```

```

v_rectifier=0.8
for i in range(-10,10):
    v_list.append(v_rectifier+i*0.02)

##### Phase Infor
phase_delay = math.atan((2*3.14159*frequency*M_PZ -
K_PZ/(2*3.14159*frequency))/B_PZ)
time_delay = (1000000*phase_delay)/(2*3.14159*frequency)

trig_1_list=[]
trig_2_list=[]
phase_lista=[]

for i in range(-8,2):
    entry=180*phase_delay/(3.1416)+i*360/128
    if entry<-90:
        entry=180+entry
    elif entry >90:
        entry= entry-180
    phase_lista.append(entry)

##### interrupt to start (switch) #####

def f():
    start_control.value(1)

sw.callback(f)

while start_control.value()==0:
    car=1

pyb.delay(2000)

while times>0:
    list_c=[]
    for voltage in v_list:
        v_write=4095*voltage/3.3
        v_rect.write(int(v_write))
        pyb.delay(200)
        trials=1
        list_b=[]
        while trials>0:
            trials-=1
            list_length=0
            start = pyb.micros()
            lista=[]

```



```

        while list_length < 2001:                                #This
allows us to find the list of values in the ADC
        if pyb.elapsed_micros(start) >
1000000/(200*frequency):
            val = adc.read()
            lista.append(val)
            ledd.toggle()
            list_length+=1
            start = pyb.micros()

        for i in lista:
            count=count+i

            count= (3.3*count)/(4095*2000)
            list_b.append(voltage*count/20000)
whisk=0
        for element in list_b:
            whisk+=element
            list_c.append(whisk/1)

list_d.append(list_c)
times-=1
phase_change.value(0)
pyb.delay(500)
phase_change.value(1)

noodles=0
for item in list_d:

list_max.append([max(item),v_list[item.index(max(item))],phase_lista[n
noodles]])
            noodles+=1

'''
list_d.append(phase_lista)
list_d = map(str, list_d)
list_d = ', '.join(list_d)

f = open('data.txt', 'w')
f.write(list_d)
f.close()

'''

list_max.append(phase_lista)
list_max = map(str, list_max)
list_max = ', '.join(list_max)

f = open('data.txt', 'w')
f.write(list_max)
f.close()
led_end.toggle()

```

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