Sub-10-nm-Diameter InGaAs Vertical Nanowire MOSFETs: Ni Versus Mo Contacts

Sub-10 nm Diameter InGaAs Vertical Nanowire MOSFETs: Ni vs. Mo contacts

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***Abstract* — Sub-10 nm diameter InGaAs vertical nanowire MOSFETs have been recently demonstrated. The key to this achievement was the use of Ni for the top ohmic contact. In this work, we present a detailed study of the impact of Ni and Mo contacts on the electrical characteristics of highly scaled InGaAs VNW MOSFETs. Sequential annealing experiments are presented that reveal the optimum temperature for each type of contact. A negative temperature dependence of the ON-resistance of 7 nm diameter Ni-contacted devices suggests the existence of an energy barrier. We also observe an unexpected transconductance and DIBL dependence on transistor diameter in Ni-contacted devices as well as abnormal DIBL asymmetry to swapping source and drain. All these results can be explained by Ni diffusing down the nanowire during the contact annealing process, reducing the effective channel length and creating a Schottky barrier drain.**

***Index Terms*—digital etch, InGaAs, MOSFETs, nanowire, reactive ion etching, top-down, vertical channel.**

I. Introduction

Future deeply-scaled logic transistor technology can benefit from new channel materials including InGaAs [1], [2] as well as highly three-dimensional transistor structures, such as fin or nanowire (NW) geometries [3]. Recent circuit-level simulations have revealed that vertical nanowire (VNW) MOSFETs offer better performance, consume less power and occupy smaller area than horizontal NW MOSFETs [4]. This advantage is attributed to the relaxed gate length, spacer thickness and contact length that the vertical geometry affords, as opposed to the very tight contacted-gate pitch constraints of horizontal devices.

Combining a high mobility channel material, such as InGaAs, with a vertical nanowire transistor geometry is particularly interesting as the VNW geometry opens the door to heterojunction engineering in the transport direction. This new design freedom, not possible in all other lateral transistor configurations, potentially offers significant advantages, such as a reduction in gate-induced drain leakage [5]. In addition, the relaxed gate length scaling that the VNW architecture enables can alleviate the direct source to drain tunneling that is prominent in InGaAs MOSFETs with ultra-scaled dimensions [6].

InGaAs VNW MOSFETs with impressive performance have been demonstrated by bottom-up [7] - [9] as well as top-down techniques [10] - [13]. In both approaches, contact to the top of the nanowire is a very problematic issue as a result of the tiny contact area that is available [13]. This represents a major challenge for NW diameter scaling below 10 nm, as demanded by future ultra-scaled logic applications [4].

Only recently, through the use of Ni alloyed contacts, the first InGaAs VNW MOSFETs with sub-10 nm diameter were realized [14]. In this first demonstration, several unexpected observations were made. The peak transconductance ($g_{m,pk}$) was found to improve as the device diameter scales down to 7 nm, contrary to earlier observations [10]. Also, DIBL displayed an anomalous scaling behavior. A detailed study of these unique devices is valuable in our quest to identify directions for future device improvement.

In this work, we study the key electrical figures of merit (FOMs) of sub-10 nm InGaAs VNW MOSFETs first presented in [14] and examine the role of the top contact in detail. Section II summarizes the device structure and process flow in greater detail, as compared to [14]. Section III discusses the effect of rapid thermal annealing (RTA) on device characteristics. The impact of diameter scaling and device source/drain asymmetry are discussed in Section IV. Measurements at different temperatures and their analysis are presented in Section V. Section VI discusses the role of top contact in explaining the anomalous diameter scaling behavior of $g_{n,pk}$ and DIBL in Ni contacted devices.

II. Device Under Investigation

Fig. 1 shows the schematic cross-section of the top-down InGaAs VNW MOSFETs studied in this work [14]. This figure illustrates a device with a top Ni contact. Similar devices with top Mo contacts were also fabricated, as detailed below.

The starting heterostructure [14], also sketched in Fig. 1, consists of an 80 nm undoped $In_{0.53}Ga_{0.47}As$ channel sandwiched between two n^+ contact regions. The top contact region features a highly doped composite cap comprised of, from top, 11 nm $In_{0.53}Ga_{0.47}As$/ 2 nm InAs/ 6 nm $In_{0.7}Ga_{0.3}As$ (n^+-doped with Te at a level of 7×10^{19} cm^{-3}) on top of 55 nm $In_{0.53}Ga_{0.47}As$ (n^+-doped with Si at 2×10^{19} cm^{-3}). The bottom n^+

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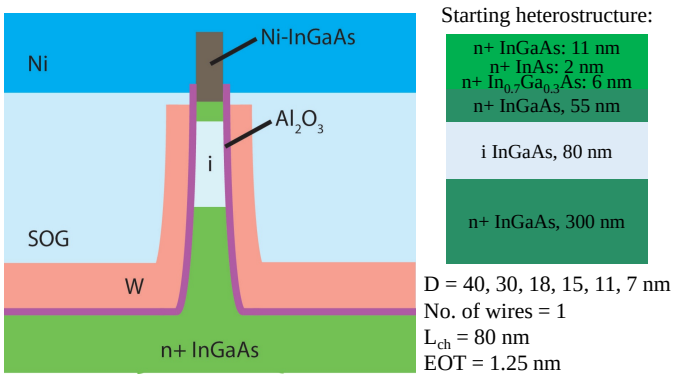

Fig. 1. Schematics of the device cross-section, starting heterostructure and device design parameters. In the heterostructure, the InGaAs composition is latticed matched to the InP substrate, unless indicated otherwise.

InGaAs is also doped with Si at 2×10^{19} cm^{-3}. This design was intended to reduce the contact resistance as InGaAs forms better ohmic contacts when the InAs composition is high [15], [16]. The top-most 11 nm $In_{0.53}Ga_{0.47}As$ layer was designed to be sacrificed during the process to reveal the underlying layers with a higher InAs composition. The 80 nm undoped InGaAs layer serves as the channel below which there is a 300 nm thick n^+-layer that serves at the bottom contact. The entire heterostructure is grown by MOCVD on a semi-insulating InP substrate.

Device fabrication followed our previous work [9], [14] and featured a precision InGaAs dry etch technology to create ultra-scaled, high aspect ratio nanopillars with a vertical and smooth sidewall [17].

To obtain sub-10 nm NWs with high yield, 7 cycles of a newly developed alcohol-based digital etch (DE) [18] were carried out in 10% (volume concentration) H_2SO_4:methanol. A SEM image of an exemplary nanowire before and after DE is shown in Fig. 2. Conventional water-based DE [19] results in nanowire destruction when attempting to cross below 10 nm in diameter (D) [18]. This is due to strong mechanical forces that arise from the high surface tension of the water-based acid used in the oxide removal step. Acids dissolved in alcohol feature a much lower surface tension and can enable remarkable scaling of NW diameter with high yield [18].

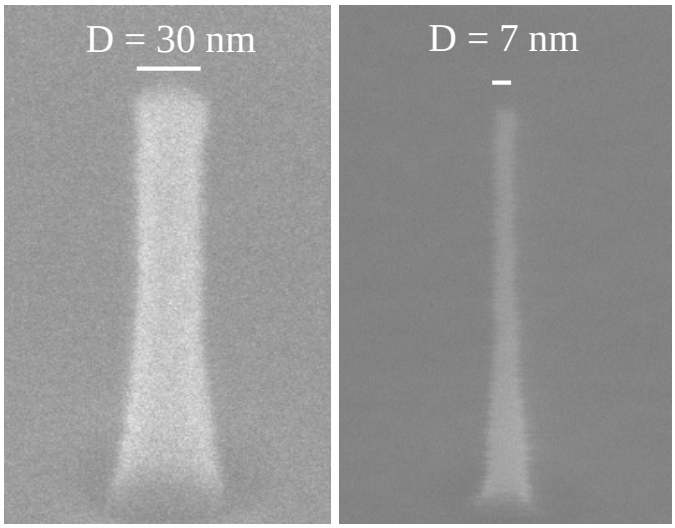

Fig. 2. D = 30 nm InGaAs nanowire right after RIE (left) reduced to D = 7 nm (right) after 10 cycles of digital etch with 10 % H_2SO_4 in methanol.

Immediately following the last cycle of DE, 2.5 nm Al_2O_3, as gate dielectric, is deposited on the sidewalls by ALD. A 40 nm thick W gate is then sputtered. This is immediately followed by a forming gas anneal (FGA) step at 350ºC for 30 min to alleviate RIE damage [20] and improve the oxide/semiconductor interface. Two steps of planarization and etch back process using spin-on glass (SOG) were then used to expose the NW tip for top contact formation while isolating the top contact metal from the gate metal [10]. The distance between the top edge of the gate and the bottom edge of the contact is 15 nm.

A critical challenge to obtain functional sub-10 nm VNW devices is contacting the tiny NW top. The use of Mo, which yields state-of-the-art contact resistance in planar transistors [21], becomes ineffective as top contact in narrow fins and NWs because of the existence of a “deadzone” under the metal [21]. Even in the case of a Mo contact to a heavily-doped InGaAs region, the outermost ~10 nm sub-surface layer beneath the sidewall ends up being non-conducting. The origin of this problem is not fully understood but it appears to be due to both electrostatic sidewall depletion and mobility degradation [22].

In contrast with this, Ni has been shown to react with InGaAs at a moderate temperature and form a highly conducting NiInGaAs metallic phase that yields a low resistance contact to n^+-InGaAs [23] - [26]. In our process, the sample is split at this point and both Mo and Ni are separately sputtered as contact metal with a thickness of 30 nm. The conformity of both metals was confirmed through SEM on fin structures with the same dimensions as the NWs. Following this, and with the goal of improving the contact resistance, a 1 min final rapid thermal annealing step was performed. As detailed below, temperatures between 200 and 350ºC were investigated.

The finished transistors feature a single NW with a channel length of 80 nm (the thickness of the intrinsic InGaAs layer, as seen in Fig. 1), D = 7, 11, 15, 18, 30 or 40 nm and 2.5 nm Al_2O_3 gate oxide (EOT of 1.25 nm).

Finished devices were electrically characterized by measuring output, transfer and subthreshold characteristics at different temperatures. In this work, we mostly focus on six key electrical figure of merits (FOMs): peak transconductance, $g_{m,pk}$ at V_{ds} = 0.5 V, ON resistance, R_{on}, extracted at V_{gs} = 1 V and small V_{ds} (0.05 V) , ON current, I_{on}, defined at I_{off} = 100 nA/μm and V_{dd} = 0.5 V, minimum subthreshold swing at V_{ds} = 0.05 V, S_{lin}, threshold voltage, $V_{t,lin}$, extracted at I_d = 1 μA/μm and V_{ds} = 0.05 V, and DIBL, defined as the ratio of the threshold voltage difference at V_{ds} = 0.05 V and V_{ds} = 0.5 V divided by the drain voltage difference (450 mV).

III. Impact of Rapid Thermal Annealing Temperature

To better understand the effect of thermal annealing and find the optimal annealing temperature (T), sequential RTA in N_2 ambient was carried out at 250, 300 and 350 ºC for both Ni and Mo contacts. The evolution of key device FOMs for D=30 nm devices as a function of annealing temperature is summarized

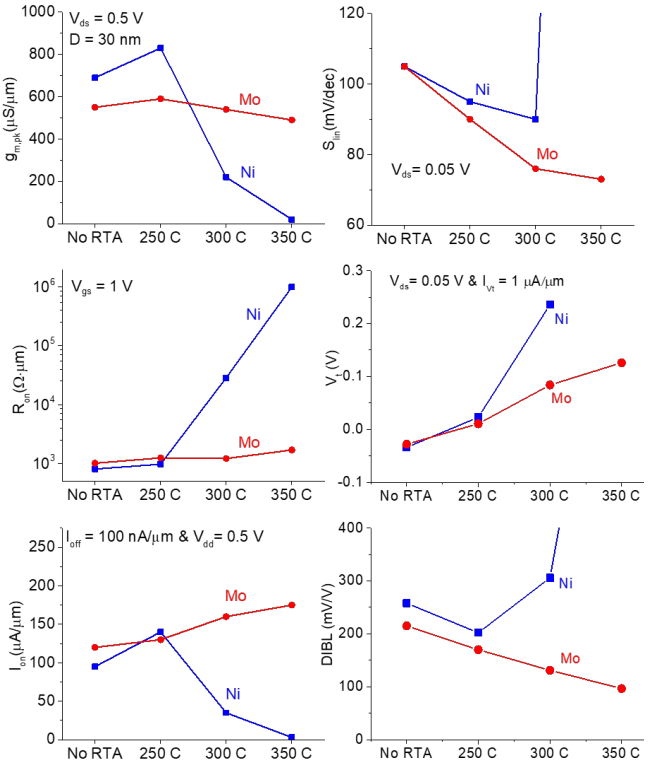

Fig. 3. Evolution of key figures of merit with RTA annealing temperature on Mo and Ni contacted transistors with D=30 nm diameter in sequential annealing experiments. The bottom contact serves as source.

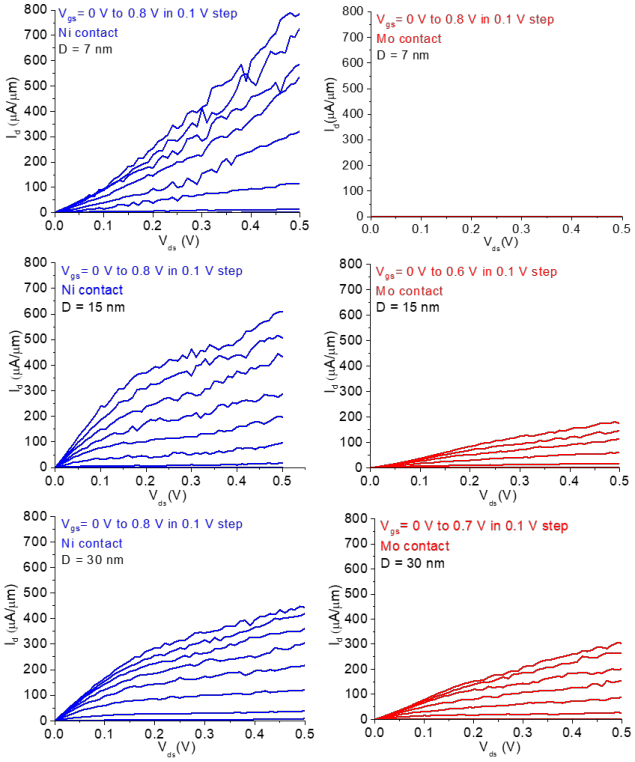

Fig. 4. Representative output characteristics of Ni- and Mo-contacted devices after annealing under optimal conditions. Devices with D = 7, 15 and 30 nm are shown. All measurements performed with the source at the bottom.

in Fig. 3. Each data point represents the mean value of 3 devices. In these results, the bottom electrode was used as the source.

Mo devices (red data) show relatively small changes with RTA, as expected from a refractory metal. While $g_{m,pk}$ and R_{on} remain rather flat until 350ºC, S_{lin} drops with increasing T as annealing improves the intrinsic oxide-semiconductor interface and reduces the interface trap density (D_{it}) inside the bandgap [27]. This also results in a continuous enhancement of I_{on} up to 350ºC. Positive V_t shift is observed after annealing, potentially due to the reduction of positive fixed charge in ALD Al_2O_3 [27]. Interestingly, DIBL also drops after RTA at higher T, suggesting the role of traps.

RTA is found to have a much more pronounced effect in Ni-contacted devices (blue data). Annealing at 250ºC enhances $g_{m,pk}$. We attribute this to an improvement in the top contact. However, the Ni contacts deteriorate rapidly after annealing at 300ºC. As a result, I_{on} first increases with annealing but eventually crashes at temperatures above 250ºC. Up to this temperature, S_{lin} and DIBL also improve. A more detailed explanation of all this changes is presented in Section VI.

These sequential annealing experiments were carried out on small pieces cut off from the main samples. Based on them plus other single-temperature studies not discussed here, an annealing temperature of 300ºC for 1 min in N_2 was selected for the main batch of Mo devices for all diameters. Regarding the Ni devices, since the starting temperature for the sequential annealing measurements shown in Fig. 3 was 250ºC and this was found to be the optimum annealing temperature, the device sample was first annealed at 200ºC under forming gas. The obtained results were better than at 250ºC in the test sample and no further annealing was performed.

IV. Diameter Scaling and Source/Drain Asymmetry

Representative output characteristics of Ni (blue) and Mo (red) contacted devices at D = 7, 15 and 30 nm are shown in Fig. 4 on identical scales. Generally, the Ni-contacted devices show significantly more current than the Mo transistors. The smallest diameter for functional devices with Mo contacts was found to be 15 nm, while many working D = 7 nm Ni-contacted transistors were obtained. Good output current saturation is obtained in Ni devices with D = 30 nm. The D=7 nm devices, however, show diode-like turn-on. This can be attributed to the top contact, as discussed in section VI.

Fig. 5 summarizes the key FOMs as a function of diameter for Ni and Mo devices after optimized final annealing (each data point represents the average of three transistors). This figure also shows the impact of swapping source and drain contacts [12]. In the normal configuration, the source is at the bottom (SB). This generally yields the best all-around performance. We denote the inverse configuration in which the source is at the top as ST.

Classical diameter scaling behavior is observed in the electrostatics metrics of Mo-contacted devices (red). The subthreshold swing and DIBL improve as D is reduced and V_t shifts positive. As expected, R_{on} increases as D is scaled down and consequently $g_{m,pk}$ drops. I_{on} reaches a peak at D = 30 nm

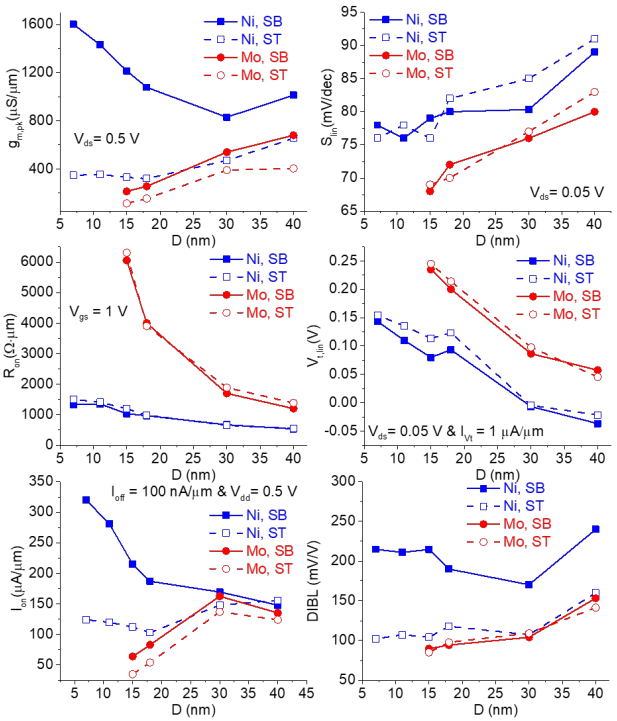

Fig. 5. Impact of diameter scaling and source/drain asymmetry in key FOMs for Ni- and Mo-contacted transistors annealed under optimum conditions.

due to the trade-off between electrostatics and contact resistance. Below D=15 nm, the transistors are non-functional due to an open top contact. This result supports the existence of a "deadzone" under the Mo contact [22].

When it comes to source/drain swapping, as in [12], Fig. 5 shows that the Mo-contacted devices are very symmetric in their electrostatic behavior. As in [12], we attribute this to our dry etch technology that produces a uniform nanowire cross-section towards the top where the intrinsic device is located. This can be seen in Fig. 2. The somehow lower $g_{m,pk}$ and I_{on} in the ST configuration reflects the higher contact resistance associated with the very small top contact.

For Ni devices (blue) in the SB configuration, V_t shifts positive and S_{lin} improves as D shrinks. This is expected from classic electrostatic scaling. In contrast, DIBL first drops and then, unexpectedly, increases. This matches the worsening current saturation in the output characteristics in devices with smaller diameter that is shown in Fig. 4. We come back to this below. DIBL and S_{lin} are worse for Ni-contacted devices as compared with Mo. This is because Mo allows a higher annealing temperature that further improves the intrinsic MOS interface.

The most interesting behavior of the Ni-contacted devices in the SB configuration is that they show a dramatic improvement in $g_{m,pk}$ despite a slightly rising R_{on} as D scales down. This abnormal $g_{m,pk}$ scaling is also attributed to the top contact and is discussed in detail in Section VI. R_{on} for Ni devices is much smaller and increases much more slowly as D shrinks, demonstrating the advantage of Ni-alloyed contacts for extremely scaled VNW transistors. As a consequence of the improving subthreshold swing and transconductance, I_{on} increases in a pronounced manner down to D = 7 nm.

Similar to Mo, $g_{m,pk}$ and I_{on} in Ni devices are much lower when the top electrode is used as source as a result of the high top contact resistance. As in Mo devices, R_{on}, S_{lin} and V_t do not exhibit much difference in the ST and SB configurations. This is again testament to the excellent diameter uniformity at the top of the NW. In contrast, DIBL shows considerable S/D asymmetry in Ni-contacted devices at all diameters. The ST configuration yields significantly better DIBL than when the source is at the bottom. The origin of this is not clear and discussed further in Sec. VI.

To gain further insight into the device electrostatics and D_{it} levels, Fig. 6 compiles S_{lin} of Ni- and Mo-contacted VNW MOSFETs as a function of L_g/λ_{eff}. L_g is the gate length, and λ_{eff} is the natural electrostatic length which is a measure of how far into the channel the drain impacts the channel potential [28]. To the first order, λ_{eff} is given by:

$$\lambda_{eff} = \sqrt{\frac{\pi \epsilon_s D^2}{4C_{ox}} + \frac{D^2}{16}} \quad (1)$$

ϵ_s is the dielectric constant of the channel material and C_{ox} is the gate oxide capacitance:

$$\frac{1}{C_{ox}} = \frac{\ln\left(1 + \frac{2t_{ox}}{D}\right)}{2\pi\epsilon_{ox}} \quad (2)$$

Here, t_{ox} and ϵ_{ox} are the thickness and dielectric constant of the oxide. The black line in Fig. 6 is the ideal relationship obtained from electrostatic simulations [28]. Multiple reports from the literature, including some of our own [21], show S_{lin} substantially worse than the ideal value. This is attributed to poor gate efficiency η due to oxide/semiconductor interface traps [27]. Including this, S_{lin} becomes:

$$S_{lin} = S_0 \times \eta \approx S_0 \times (1 + \frac{q\pi D D_{it}}{C_{ox}}) \quad (3)$$

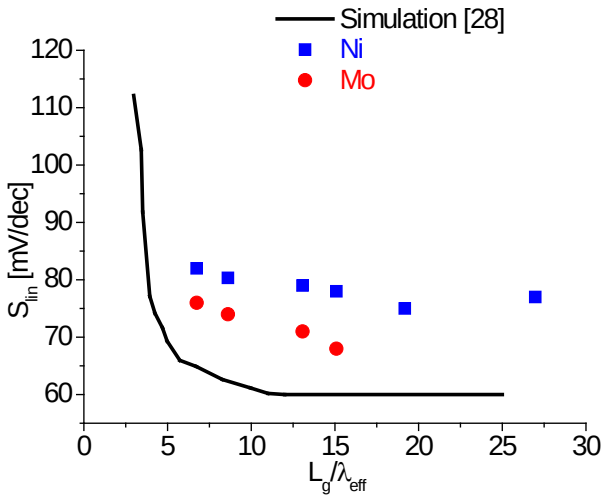

Fig. 6. S_{lin} versus L_g/λ_{eff} for both Ni- and Mo-contacted devices measured with source at bottom. The black line is the ideal electrostatic simulation [28]. Data points correspond to experimental results reported in this paper.

where S_0 is the ideal subthreshold swing shown by the black line in Fig. 6. Based on (3), we estimate D_{it} to be around 6 and $4 \times 10^{12}\ eV^{-1}cm^{-2}$, for Ni and Mo devices, respectively. The higher annealing temperature used for the Mo devices result in a lower D_{it} level.

V. Temperature Dependence

To gain further insight into the dominant physics, both Ni and Mo transistors were characterized at various temperatures from 230 – 330 K. Key FOMs for Ni devices with D = 7 and 40 nm and SB configuration are shown in Fig. 7. For the D=40 nm device, S_{lin} drops as T decreases, as expected. DIBL rapidly improves at lower T confirming again the role of traps. Slightly

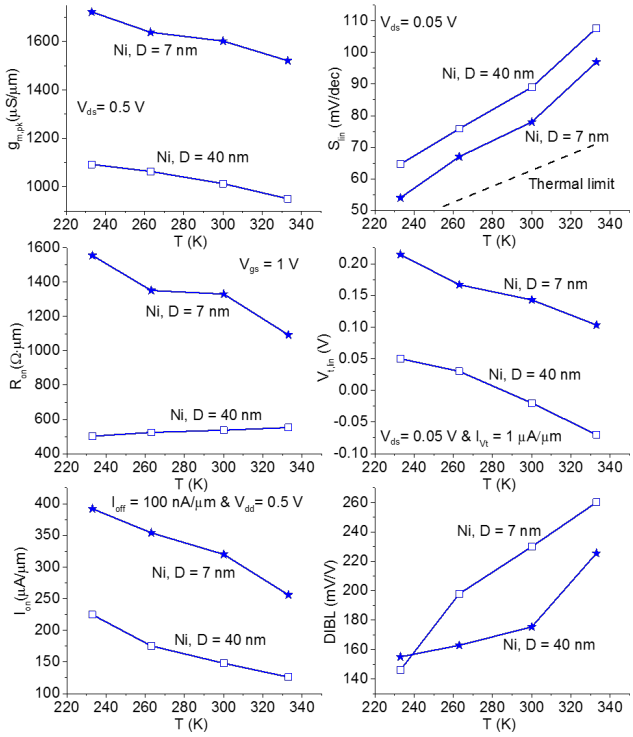

Fig. 7. Temperature dependence of key FOMs for Ni-contacted devices of two different diameters. In all cases, the source is at the bottom.

lower R_{on} is also obtained at lower temperatures, potentially due to a decreased series resistance of the n^+ contact region as a result of small increase in mobility. $g_{m,pk}$ improves as the temperature is reduced. A number of factors, including higher mobility and less charge trapping at lower T, are likely to contribute to this. As a result of higher transconductance and lower S_{lin} at lower T, I_{on} is also enhanced at low temperatures. Similar temperature dependencies have been observed in transistors with Mo contacts of all diameters (data not shown).

Ni-contacted devices with D=7 nm show a similar behavior as the wider devices with one important exception, i.e., R_{on} exhibits a strong negative temperature dependence. This is a key observation that we attribute to the top contact, as discussed in the next section.

VI. The Role of the Top Contact

This first realization of sub-10 nm diameter InGaAs VNW MOSFETs has yielded a number of surprises in the narrow D regime that Ni contacts have made possible. A rapidly improving $g_{m,pk}$ as D scales down, and a negative temperature dependence of R_{on} are unexpected. The details of the top Ni contact provide an explanation to these phenomena.

It is well known that when Ni reacts with InGaAs at a moderate temperature, a highly conducting NiInGaAs metallic phase is formed [23] – [26], [29], [30]. It has also been observed that during thermal annealing of Ni-contacted InGaAs FinFETs, Ni diffuses along the fins as it forms NiInGaAs [31]. A higher rate of diffusion is observed in narrower fins because the diffusion is surface-limited and narrower fins have a higher surface-to-volume ratio.

From these observations, it is reasonable to expect that in our devices, Ni diffuses further down the NW the narrower its diameter. For our annealing conditions, when D < 20 nm, Ni might diffuse through the entire n^+-doped layer stack and reach the undoped channel region. This would have two

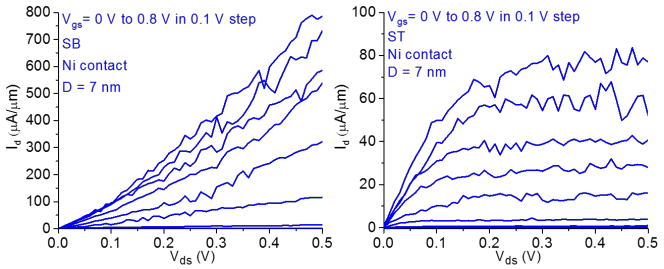

Fig. 8. Output characteristics measured with SB (left) vs. ST (right) of a representative D = 7 nm Ni-contacted transistor.

consequences. First, the effective electrical channel length becomes shorter, yielding an increasing transconductance, as seen in Fig. 5. In addition, the NiInGaAs comes now in direct contact with undoped InGaAs. Rather than an ohmic contact, this could result in a Schottky barrier [32]. In this instance, R_{on} should show a negative temperature dependence, as observed in Fig. 7.

Confirmation of this hypothesis comes from a comparison of the output characteristics of a D = 7 nm Ni device measured in the SB and ST configuration, as shown in Fig. 8 (the left characteristics are the same as those in the left corner of Fig. 4). As discussed above, when the source is at the bottom and the device is biased in the saturation regime, the Schottky diode at the drain is forward biased and the output characteristics show Schottky-like behavior (Fig. 8, left). With the source at the top, the transistor exhibits excellent current saturation but with much lower current (Fig. 8, right). In this configuration, the transistor behaves like a metal-source Schottky-barrier MOSFET with relatively high source resistance but good drain current saturation.

Fig. 5 shows that DIBL exhibits considerable S/D asymmetry in Ni devices of all diameters and is higher when the top electrode behaves as the drain. This asymmetry can potentially be caused by a diameter change in the semiconductor beneath the NiInGaAs region because of the strain introduced by

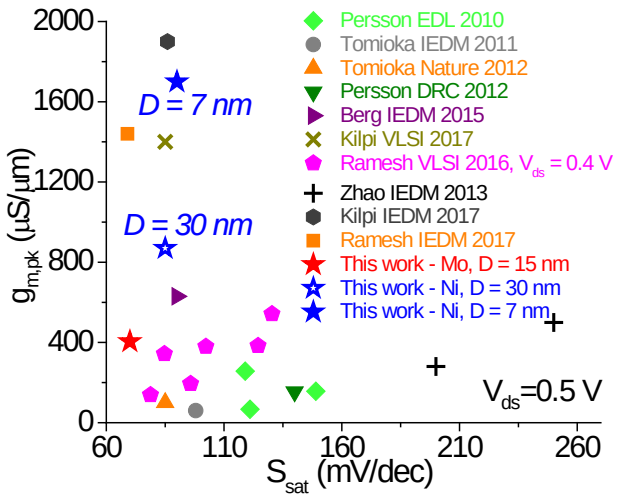

Fig. 9. Benchmark: $g_{m,pk}$ vs. minimum S_{sat} at V_{ds} = 0.5 V for InGaAs-based VNW MOSFETs.

NiInGaAs formation [31]. [12] shows that diameter nonuniformity results in DIBL asymmetry. The band structure of InGaAs can also change because of the strain and might lead to DIBL asymmetry. In addition, charge trapping can potentially play a role. Further detailed characterization of the NiInGaAs phase in the very small VNW via TEM, or other techniques is needed to verify our hypothesis.

Fig. 9 benchmarks transport and electrostatics metrics in recently published InGaAs VNW MOSFETs by plotting $g_{m,pk}$ vs. minimum S_{sat}, both at V_{ds} = 0.5 V. This graph captures the trade-off that often exists between transport and electrostatics in MOSFETs. Our D = 7 nm device with Ni contact shows a combination of high transconductance and good subthreshold swing, highlighting the potential of the top-down VNW approach.

It is of interest to compare our best D = 30 nm Ni-contacted device (plotted in Fig. 9) with the device that exhibits the highest $g_{m,pk}$ in Fig. 9 that has a D = 27 nm [9]. R_{on} in our device is around 650 Ω·µm while that of [9] reaches 450 Ω·µm. This excellent result might be due to the longer top contact region and leads to higher $g_{m,pk}$. Our device demonstrates comparable S_{sat} of 85 mV/dec (vs. 86 mV/dec in [9]). With D = 15 nm, our Mo-contacted MOSFET exhibits one of the lowest S_{sat} of 70 mV/dec (63 mV/dec reported for D = 30 nm in [13]).

Indeed, the top contact remains a key challenge for III-V VNW technology, especially at the scaled dimensions required for future nodes. Mo does not yield working contacts and Ni contacts are unlikely to survive the standard back-end-of-line (BEOL) process due to significant diffusion at even relatively low temperatures. Significant efforts are therefore required in order to develop a suitable contact technology that minimizes contact resistance while ensuring thermal stability. Refractory metals including Mo will likely require a mushroom contact [9], or InGaAs with high InAs composition [15], [16]. Alloyed contacts need careful optimization of the amount of metal to prevent excess diffusion.

VII. Conclusions

Extensive characterization was carried out of InGaAs vertical nanowire MOSFETs with both Ni and Mo contacts down to the sub-10 nm in diameter. The use of Ni as top contact has been key to achieve working transistors in this diameter regime. Temperature dependence of ON resistance, high transconductance and high DIBL in Ni contacted devices with narrow diameter suggests that Ni diffuses along the NW and reduces the effective channel length.

VIII. Acknowledgement

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References

[1] J. A. del Alamo, “Nanometer-scale electronics with III-V compound semiconductors,” *Nature*, vol. 479, no. 7373, pp. 317-323, Nov. 2011.

[2] H. Riel, L. -E. Wernersson, M. Hong and J. A. del Alamo, “III-V compound semiconductor transistors-from planar to nanowire structures,” *MRS Bulletin*, vol. 39, no. 08, pp. 668-677, Aug. 2014.

[3] K. J. Kuhn, "Considerations for ultimate CMOS scaling,"*IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1813-1828, Jul. 2012.

[4] D. Yakimets, G. Eneman, P. Schuddinck, T. H. Bao, , M. G. Bardon, P. Raghavan, A. Veloso, N. Collaert, A. Mercha, D. Verkest, A. V-Y. Thean, and K. De Meyer, “Vertical GAAFETs for the ultimate CMOS scaling,” *IEEE Trans. Electron Devices*, vol. 62, no. 5, pp. 1433-1439, May. 2015.

[5] J. Lin, D. A. Antoniadis and J. A. del Alamo, “Physics and mitigation of excess off-state current in InGaAs quantum-well MOSFETs,” *IEEE Trans. Electron Devices*, vol. 62, no. 5, pp. 1448-1455, May. 2015.

[6] V. Moroz, J. Huang, and R. Arghavani, “Transistor design for 5nm and beyond: slowing down electrons to speed up transistors”, in *ISQED Tech. Dig.*, 2016, pp. 278-283.

[7] C. Thelander, L. E. Fröberg, C. Rehnstedt, L. Samuelson, and L.-E. Wernersson, “Vertical enhancement-mode InAs nanowire field-effect transistor with 50-nm wrap gate,” *IEEE Electron Device Lett.*, vol. 29, no. 3, pp. 206-208, Mar. 2008.

[8] K. Tomioka, M. Yoshimura, and T. Fukui, "A III-V nanowire channel on silicon for high-performance vertical transistors." *Nature*, vol. 488, no. 7410, pp. 189-192, Aug. 2012.

[9] O.-P. Kilpi, J. Svensson, and L.-E. Wernersson, “Sub-100-nm gate-length scaling of vertical InAs/InGaAs nanowire MOSFETs on Si,” in *IEDM Tech. Dig.*, 2017, pp. 417-420.

[10] X. Zhao, J. Lin, C. Heidelberger, E. A. Fitzgerald, and J. A. del Alamo, "Vertical nanowire InGaAs MOSFETs fabricated by a top-down approach," in *IEDM Tech. Dig.*, 2013, pp. 695-698.

[11] S. Ramesh, T. Ivanov, E. Camerotto, N. Sun, J. Franco, A. Sibaja-Hernandez, R. Rooyackers, A. Alian, J. Loo, A. Veloso, A. Milenin, D. Lin, P. Favia, H. Bender, N. Collaert, A. V. Y. Thean, and K. D. Meyer, "Top-down InGaAs nanowire and fin vertical FETs with record performance," in *VLSI Tech. Dig.*, 2016, pp. 164-165.

[12] X. Zhao, J. Lin, C. Heidelberger, E. A. Fitzgerald, and J. A. del Alamo, "Source/drain asymmetry in InGaAs vertical nanowire MOSFETs,” *IEEE Trans. Electron Devices*, vol. 64, no. 5, pp. 2161-2165, Apr. 2017.

[13] S. Ramesh, T. Ivanov, V. Putcha, A. Alian, A. Sibaja-Hernandez, R. Rooyackers, E. Camerotto, A. Milenin, N. Pinna, S. El Kazzi, A. Veloso, D. Lin, P. Lagrain, P. Favia, N. Collaert, and K. D. Meyer, "Record performance top-down $In_{0.53}Ga_{0.47}As$ vertical nanowire FETs and vertical nanosheets," in *IEDM Tech. Dig.*, 2017, pp. 409-412.

[14] X. Zhao, C. Heidelberger, E. A. Fitzgerald, W. Lu, A. Vardi, and J. A. del Alamo, "Sub-10 nm diameter InGaAs vertical nanowire MOSFETs,” in *IEDM Tech. Dig.*, 2017, pp. 413-416.

[15] T. Nittono, H. Ito, O. Nakajima and T. Ishibashi, “Non-alloyed ohmic contacts to n-GaAs using compositionally graded $In_xGa_{1-x}As$ layers, ”*JPN J. Appl. Phys.*, vol. 27, no. 9, pp. 1718-1722, Jul., 1988.

[16] S. Kim, M. Yokoyama, R. Nakane, O. Ichikawa, T. Osada, M. Hata, M. Takenaka, and S. Takagi, Member, “High-performance InAs-on-insulator n-MOSFETs with Ni-InGaAs S/D realized by contact resistance reduction technology,” *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3342-3350, Oct. 2013.

[17] X. Zhao and J. A. del Alamo, "Nanometer-scale vertical-sidewall reactive ion etching of InGaAs for 3-D III-V MOSFETs," *IEEE Electron Device Lett*., vol. 35, no. 5, pp. 521-523, May. 2014.
[18] W. Lu, X. Zhao, D. Choi, S. El Kazzi, and J. A. del Alamo, "Alcohol-based digital etch for III-V vertical nanowires with sub-10 nm diameter," *IEEE Electron Device Lett*., vol. 38, no. 5, pp. 548-551, Apr. 2017.
[19] J. Lin, X. Zhao, D. A. Antoniadis, and J. A. del Alamo, "A novel digital etch technique for deeply scaled III-V MOSFETs", *IEEE Electron Device Lett*., vol. 35, no. 4, pp. 440-442, Apr. 2014.
[20] J. Lin, T.-W. Kim, D. A. Antoniadis, and J. A. del Alamo, "A self-aligned InGaAs quantum-well metal–oxide–semiconductor field-effect transistor fabricated through a lift-off-free front-end process," *Appl. Phys. Express*, vol. 5, no. 6, pp. 064002, May 2012.
[21] J. A. del Alamo, D. A. Antoniadis, J. Lin, W. Lu, A. Vardi and X. Zhao, " Nanometer-scale III-V MOSFETs," *IEEE J. Electron. Devices. Soc*., vol. 4, no. 5, pp. 205-214, Jul. 2016.
[22] A. Vardi and J. A. del Alamo, "Fin-width scaling of highly-doped InGaAs fins," *Compound Semicond. Week* 2018, Cambridge, MA, USA, May 29 – Jun. 1, 2018.
[23] S.-H. Kim, M. Yokoyama, N. Taoka, R. Iida, S. Lee, R. Nakane, Y. Urabe, N. Miyata, T. Yasuda, H. Yamada, N. Fukuhara, M. Hata, M. Takenaka, and S. Takagi, "Self-aligned metal source/drain $In_xGa_{1-x}As$ n-MOSFETs using Ni-InGaAs alloy," in *IEDM Tech. Dig*., 2010, pp. 596-599.
[24] X. Zhang, Ivana, H.-X Guo, X. Gong, Q. Zhou and Y.-C Yeo, "A self-aligned Ni-InGaAs contact technology for InGaAs channel n-MOSFETs," *J. Electrochem. Soc*., vol. 159, no. 5, pp. 512-515, Mar. 2012.
[25] M. L. Huang, S. W. Chang, M. K. Chen, Y. Oniki, H. C. Chen, C. H. Lin, W. C. Lee, C. H. Lin, M. A. Khaderbad, K. Y. Lee, Z. C. Chen, P. Y. Tsai, L. T. Lin, M. H. Tsai, C. L. Hung, T. C. Huang, Y. C. Lin, Y.-C. Yeo, S. M. Jang, H. Y. Hwang, H. C.-H. Wang, and C. H. Diaz, "High performance $In_{0.53}Ga_{0.47}As$ FinFETs fabricated on 300 mm Si substrate," in *VLSI Tech. Dig*., 2016, pp. 16-17.
[26] L. Czornomaz, M. El Kazzi, M. Hopstaken, D. Caimi, P. Mächler, C. Rossel, M. Bjoerk, C. Marchiori, H. Siegwart, J. Fompeyrine, "CMOS compatible self-aligned S/D regions for implant-free InGaAs MOSFETs," *Solid-State Electron.*, vol. 74, pp. 71-76, Aug. 2012.
[27] M. Si, J. Gu, X. Wang, J. Shao, X. Li, M. J. Manfra, R. G. Gordon, and P. D. Ye, "Effects of forming gas anneal on ultrathin InGaAs nanowire metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett*., vol. 102, no. 9, pp. 093505, Mar. 2013.
[28] C. P. Auth and J. D. Plummer, "Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's." *IEEE Electron Device Lett*., vol. 18, no. 2, pp. 74-76, Feb. 1997.
[29] R. Oxland, S. W. Chang, Xu Li, S. W. Wang, G. Radhakrishnan, W. Priyantha, M. J. H. van Dal, C. H. Hsieh, G. Vellianitis, G. Doornbos, K. Bhuwalka, B. Duriez, I. Thayne, R. Droopad, M. Passlack, C. H. Diaz, and Y. C. Sun, "An ultralow-resistance ultrashallow metallic source/drain contact scheme for III–V NMOS," *IEEE Electron Device Lett*., vol. 33, no. 4, pp. 501-503, Feb. 2012.
[30] R. J. W. Hill, C. Park, J. Barnett, J. Price, J. Huang, N. Goel, W.Y. Loh, J. Oh, C. E. Smith, P. Kirsch, P. Majhi, R. Jammy, "Self-aligned III-V MOSFETs heterointegrated on a 200 mm Si substrate using an industry standard process flow," in *IEDM Tech. Dig.*, 2010, pp. 130-133.
[31] R. Chen and S. A. Dayeh, "Size and orientation effects on the kinetics and structure of nickelide contacts to InGaAs fin structures," *Nano Lett*., vol. 15, no. 6, pp. 3770-3779, Apr. 2015.
[32] S. Mehari, A. Gavrilov, S. Cohen, P. Shekhter, M. Eizenberg, and D. Ritter, "Measurement of the Schottky barrier height between Ni-InGaAs alloy and $In_{0.53}Ga_{0.47}As$," *Appl. Phys. Lett*., vol. 101, no. 7, pp. 072103, Aug., 2012.