Silicon Pressure Sensor using Wafer Bonding Technology

by

Lalitha Parameswaran

B.Eng., Carleton University (1990)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Engineering

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Abstract

Capacitive pressure transducers offer higher sensitivity than conventional piezoresistive devices; however, due to the small capacitance variations, they often require on-chip signal conditioning circuitry. Silicon wafer bonding offers the possibility of fabricating a sensor with a process flow compatible with standard IC processes, thus facilitating sensor- circuit integration. The design and fabrication of a silicon capacitive pressure sensor utilizing such a process is described. The base structure for the sensor is a sealed cavity, in which silicon wafer bonding in a controlled ambient gas, and electrochemical etchback techniques are used to fabricate a structure that can withstand high temperature process steps. An electrode for capacitive detection is formed by means of a metal thermocompression bonding technique. The characteristics are simulated using MIT's MEMCAD system. Upon completion of the device, it was found that capacitance-pressure testing did not yield measurable capacitance changes, most probably due to contamination on the metallization as a result of the process used to open the pressure inlet ports. However, with suitable modifications to this step, it should be possible to successfully fabricate and integrate sensors using the sealed cavity process.

Thesis Supervisor: Martin A. Schmidt
Title: Associate Professor

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Chapter 1

Introduction

Research in the area of micromachined sensors and actuators has expanded dramatically in the past decade and a half, with a range of devices being developed to measure a wide variety of stimuli. Much of this work is based on existing silicon process technology, and the sensor industry has taken advantage of the fact that silicon, in addition to having well-characterized electrical properties, also has proven to be a high-strength, reliable mechanical material as well [1]. Among the many types of sensors currently available commercially, the pressure sensor was one of the first to be successfully manufactured and marketed in large scale. These sensors are widely used in many areas including industrial and automotive environments, biomedical applications, and instrumentation. There is a continuing need for low cost, high performance pressure sensors, and advances in microfabrication technology have made it possible to fabricate these devices economically by taking advantage of batch processing techniques.

1.1 Pressure sensors - A brief review

There are a variety of methods that can be used to sense an applied pressure load and convert it into an electrical signal, and conventional microfabricated pressure sensors can be divided into a number of categories, which will be briefly outlined.

One of the earliest microfabricated sensors was the piezojunction device [2], which

used stress-induced changes in the current characteristics of a p-n junction to transduce pressure changes. However, in order to obtain high sensitivity, it was necessary to operate them near the fracture stress of silicon, making them prone to mechanical failure.

Piezoelectric materials such as PZT (ceramic) and PVDF (polymer) have also been proposed for usage in sensor applications [3], mainly in the area of underwater devices, and acoustic sensors such as SAW devices. They tend to have high output impedances and are somewhat difficult to package, which limits their use to specialized applications.

Piezoresistive pressure sensors have been in use for many years, with one of the first applications being in the biomedical area [4], and are the most commonly available commercial sensor on the market today. They are relatively easy to fabricate and usually consist of a thin silicon diaphragm in which piezoresistors have been formed, by implantation and/or diffusion of boron (figure 1-1). The resistors are usually arranged in a Wheatstone bridge configuration so that the differential strains induced by deflections of the diaphragm can be sensed by the bridge elements, and are placed at the points where the stress reaches a maximum as the diaphragm is deformed due to the applied pressure. However, the resistors tend to be very sensitive to temperature changes, often necessitating the use of temperature compensation schemes [5, 6], and/or the use of resistor trimming [7, 8, 9].

Resonant sensors can be used to measure a wide variety of physical and chemical variables, including pressure, temperature, strain, etc. Their operation is based on a shift in the resonant frequency of the structure caused by a change in the external variable to be measured [10]. These sensors can offer high sensitivity but their stability depends on the mechanical properties of the structure as well as the type of detection circuitry used [11].

It is desirable to have a sensor that gives high sensitivity, as well as being insensitive to temperature and other ambient conditions. The capacitive pressure sensor is intrinsically capable of pressure sensitivities which are greater than those of the piezoresistive type by an order of magnitude or more [12, 13, 14, 15], and if packaged

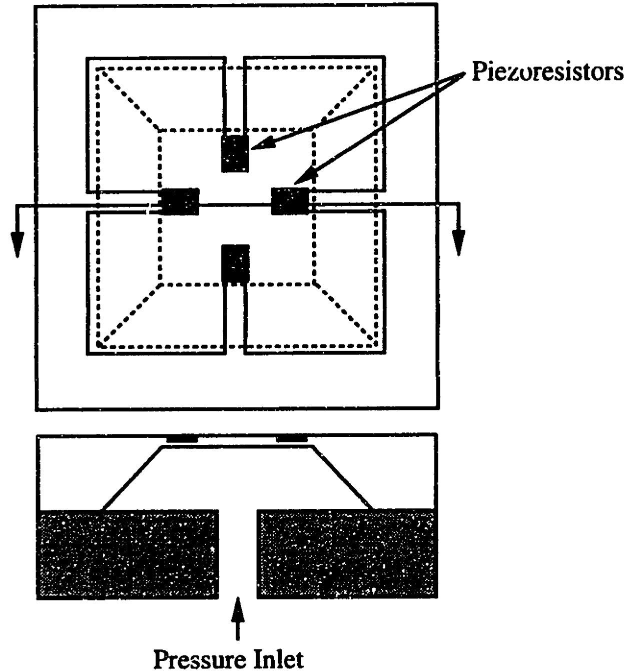


Figure 1-1: Basic bulk-micromachined piezoresistive pressure sensor

appropriately, suffers very little from temperature variations. However, as sensor size is scaled down, the main challenge in utilizing these devices is the ability to accurately detect small capacitance variations (<1pF) which can easily be overwhelmed by parasitic and stray capacitance contributions from leads and packaging. In order to take advantage of the higher intrinsic sensitivities, some form of on-chip signal amplification and conversion is usually required.

In its most basic form, the capacitive pressure sensor consists of two plates, one fixed and the other deformable under a pressure load. The plates are biased appropriately and the change in capacitance is sensed as the movable plate is deformed to vary the gap spacing. One of the first micromachined capacitive pressure sensors was developed in 1973, for use as a blood pressure monitor [14]. It involved the use of a pedestal-ring structure, which served as the input capacitance to a field-effect transistor on the silicon membrane. Most of the sensors currently being fabricated can be grouped into two categories: surface micromachined devices, usually employing thin membranes of polysilicon or silicon nitride, and bulk micromachined devices which

generally use single crystal silicon membranes.

Successful surface micromachining requires good control of the mechanical properties of the thin film being used. This includes the ability to deposit stress-free layers of the structural material to avoid buckling of membranes, as well as the use of appropriate annealing schemes to provide stress release for supended structures, and drying techniques to avoid stickdown of thin membranes[16]. There are numerous examples of pressure sensors fabricated using this technique, many of which employ polysilicon as the structural material [17, 18].

Bulk micromachining involves the removal of portions of the silicon substrate to create the necessary membrane. In its simplest form, the silicon wafer is etched anisotropically from the backside using an etchant such as KOH, TMAH, EDP or hydrazine, all of which have a high <100>:<111> etch-rate ratio. Generally, an etchstop layer has been formed in the silicon prior to etching. Figure 1-2a illustrates the resulting structure, in which the silicon sidewalls display the characteristic 54.7° angle of the <111> planes. This technique results in diaphragms that require a relatively large chip area, to accomodate the sidewalls. This requirement has been circumvented by using techniques such as the dissolved wafer process[19], in which a p++ layer is formed in a silicon wafer which is then anodically bonded to a glass substrate. The lightly doped silicon is then etched away, leaving the p++ diaphraghm bonded to the glass (figure 1-2c). Silicon wafer bonding can also be used to advantage in forming structures that do not take up a large area, and has been used to fabricate piezoresistive pressure sensors [20, 21].

The major stumbling block towards the widespread use of capacitive pressure sensors is the small value of ΔC, which can be swamped out by parasitic capacitances and noise. These effects become more prominent as the sensor is scaled down in size since the active capacitance is also reduced, and necessitates the use of some form of on-chip electronics to reduce the noise that can result from a hybrid scheme.

A number of capacitive sensors have been integrated with on-chip circuitry to varying degrees. For example, a digitally compensated CMOS circuit was integrated with a capacitive sensor[22], in which the sensor chip contained two CMOS capacitor-

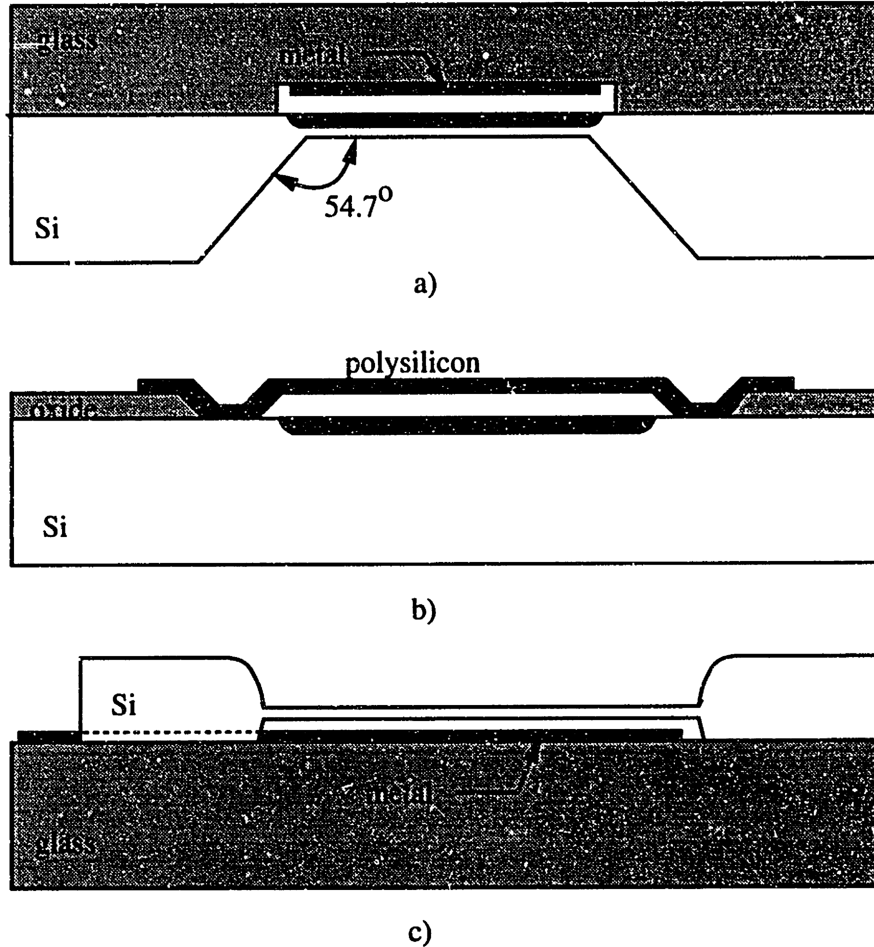


Figure 1-2: Capacitive pressure sensors fabricated using a) bulk micromachining, b) surface micromachining, c) dissolved wafer process

to-frequency converters, and operated with a hybrid digital chip to compensate for offsets. A digital readout technique was implemented by Kung[23] using a charge redistribution technique, with a polysilicon surface micromachined capacitor as the sensing structure. More recently, sigma-delta modulation is also coming into use for signal conversion and manipulation. As detection schemes advance and new processes are developed to facilitate merging of sensor and circuit, the capacitive pressure sensor may become the dominant type due to its inherently better characteristics.

1.2 Silicon wafer bonding

Silicon wafer bonding was introduced in the early 1980's as a promising new method of fabricating silicon-on-insulator substrates[24, 25]. It has subsequently found applications in power devices [26], as well as for providing new dielectric isolation schemes [27], and in recent years has become a valuable tool in the construction of a variety of micromechanical devices including accelerometers[28], valves[29], pressure sensors [20, 30, 31] and shear stress sensors[32], to name a few. Silicon wafer bonding offers the ability to make use of single crystal silicon layers as a structural material, where silicon's well-known mechanical and electrical properties can be used to advantage, both in sensor and circuit fabrication.

The basic wafer bonding process consists of the hydration and contacting of two polished silicon surfaces, one or both of which may be covered with a layer of silicon dioxide. Hydration involves the creation of hydroxyl groups on the wafer surface, by means of an immersion in H_2SO_4:H_2O_2 and/or the organic clean portion of an RCA clean (NH_4OH:H_2O_2:H_2O). When the hydrated surfaces are placed in contact, hydrogen bonding between the surfaces pulls them together. Subsequently, the wafers are subjected to a high temperature anneal in which a number of transitions occur as the temperature is raised. First, the hydroxyl groups are converted to water molecules which then dissociate, allowing the oxygen to bond to the silicon while the hydrogen diffuses through the wafer. At higher temperatures the oxygen will diffuse into the lattice also, and silicon atoms fill in any surface roughness through diffusion. After the anneal, the bond interface is virtually indistinguishable from the bulk of the silicon, and bond strength measurements have indicated that the strength approaches the fracture strength of single crystal silicon.

There are a number of other methods of joining wafers such as anodic or field-assisted bonding between silicon and glass[33], and low-temperature bonding utilizing interfacial glass layers[34]. Most of these methods are used in back-end processing and packaging, as they are for the most part low temperature steps. Silicon wafer bonding however, offers the ability to add on large thicknesses of single crystal silicon

to a substrate, with a process that is simpler and less expensive than epitaxy.

1.3 Sensor process partitioning

As mentioned previously, in using silicon wafer bonding a high temperature anneal is required to obtain a strong bond. This can pose problems when using substrates with heavily doped regions like p+ etchstop layers, or critical dopant profiles like MOSFET source/drain junctions, both of which can undergo considerable shifting under high temperature steps. This thesis describes a process sequence that avoids this problem by partitioning the sensor and circuit fabrication such that the high temperature processing necessary to create a base unit for the sensor is done first, followed by standard IC processing. The sensor is then completed using low temperature steps that will not affect on-chip circuitry. This process is illustrated in figure 1-3. The basic steps include the bonding of two silicon wafers, one containing cavities formed by dry or wet etching, followed by thinning using electrochemical etching to form a membrane over each cavity. Integrated circuitry is formed in the field regions around the cavity using a standard process, after which an appropriate etching step takes place to complete the mechanical structure. Finally, for a capacitive detection scheme, an appropriate overelectrode is formed, after which the whole structure is packaged. This process can be adapted to make a variety of sensors, two examples of which are illustrated in figure 1-3. A similar process was recently used to fabricate piezoresistive diaphragm pressure sensors with integrated temperature compensation circuitry[9]. By partitioning the fabrication in this manner, the process can take advantage of existing IC fabrication equipment and techniques without modification, thus facilitating integration and hopefully reducing manufacturing costs in the long run.

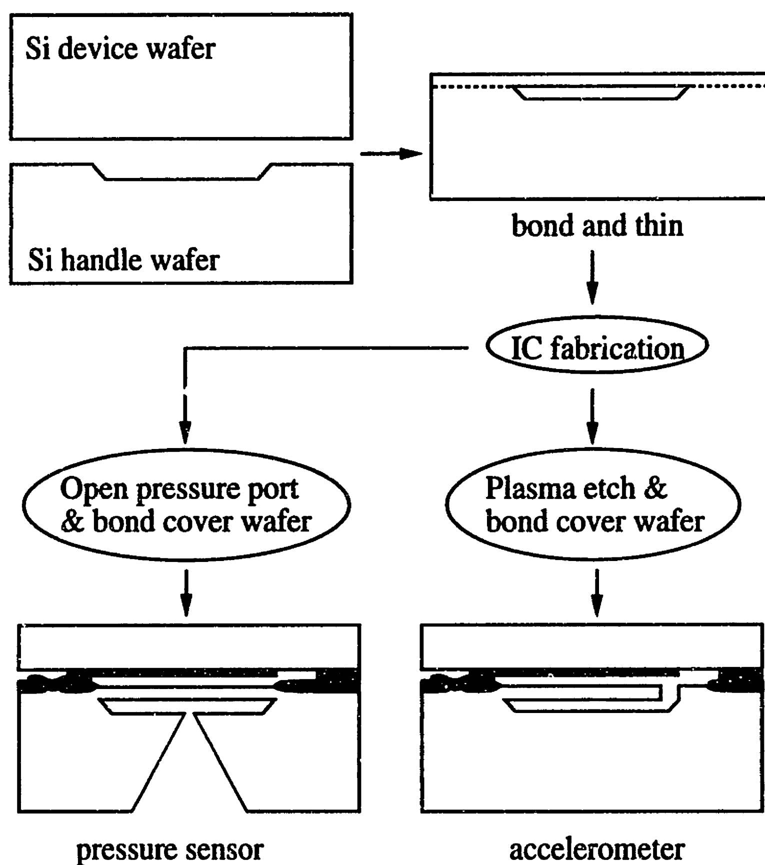


Figure 1-3: Basic process for sealed cavity structure

1.4 Scope of thesis

This thesis describes the design and fabrication of a capacitive pressure using a process that can be easily merged with a standard IC fabrication line. The work encompasses the mechanical design and process characterization necessary to fabricate the sensor.

Chapter Two discusses the design calculations used to determine the sensor dimensions and characteristics. It also contains results of finite element simulations of the capacitance-pressure characteristics of the device. Chapter Three describes in detail the steps necessary to fabricate the pressure sensor. Some experimental observations on electrochemical etching and silicon wafer bonding are explained in the context of the fabrication sequence. Chapter Four discusses the test setup and results, and conclusions are given in chapter Five.

Chapter 2

Pressure Sensor Design

The characteristics of the sensor were determined using a combination of exact analytical solutions and finite element analysis. Simulations were done using the MIT MEMCAD system[35], a suite of tools being developed to model microelectromechanical devices.

2.1 Analytical model

The basic sensor consists of two parallel circular plates separated by an air gap, with the bottom plate being stationary and the top plate being deformable under load but with clamped edges. A circular structure was selected to simplify the analysis of the membrane behaviour, as well as to avoid the problem of undesirable stress concentrations at the corners of rectangular membranes. A cross-sectional diagram is given in figure 2-1.

To obtain a linear relationship between the membrane deflection and the applied pressure, the membrane has been dimensioned to operate in the small deflection regime, where the maximum deflection is less than half of the membrane thickness. This constraint allows us to neglect the effect of in-plane stretching and simplifies the load-deflection relationship. From small deflection theory[36], the deflection of a

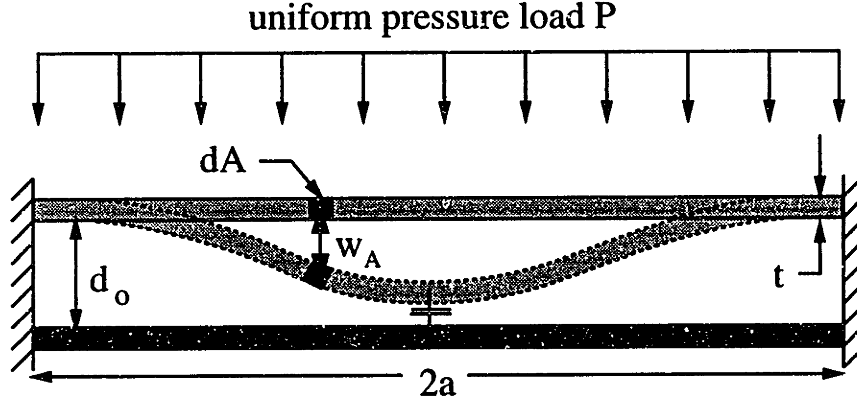


Figure 2-1: Cross-sectional diagram of basic capacitor

circular membrane with clamped edges is given by

$$w(r) = \frac{P}{64D}(a^2 - r^2)^2 \tag{2.1}$$

where D is the flexural rigidity of the plate, given by $D = \frac{Et^3}{12(1-\nu^2)}$, a and t are the radius and thickness of the membrane respectively, r is the radial distance from the center of the membrane, P is the applied pressure uniformly distributed across the membrane and the material constants of silicon (elastic modulus E and Poisson's ratio ν) are assumed in the thesis to be E =160GPa and $\nu = 0.25$.

The maximum allowable deflection is arbitrarily set to $w_{max} = d_o \leq 0.1t$, where d_o is the plate separation under no load. Combining this condition with equation 2.1 and inserting the appropriate physical constants, we get

$$\frac{a}{t} \leq \left(\frac{9.102 \times 10^{10}}{P_{max}}\right)^{\frac{1}{4}} \tag{2.2}$$

where P_{max} is defined as the pressure (in Pa) required to just contact the two plates

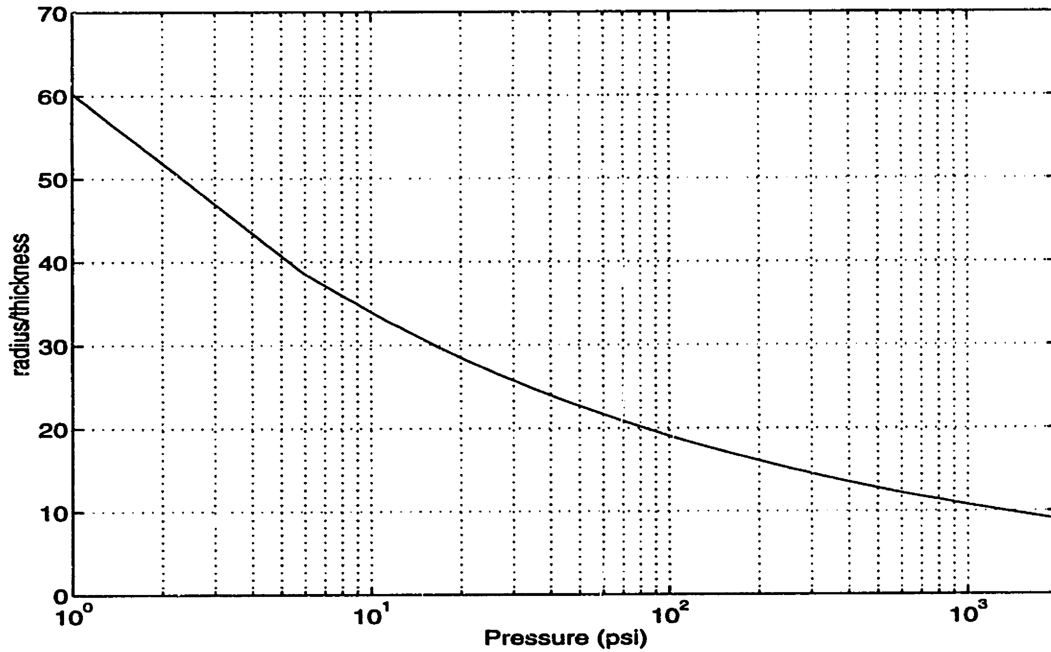


Figure 2-2: Radius/thickness ratio as a function of maximum applied pressure, for $d_o = 0.1t$

at the center, and is given by

$$P_{max} = d_o \frac{64D}{a^4} \tag{2.3}$$

The radius to thickness ratio can be plotted as a function of the desired pressure range for the sensor (for an assumed value of $d_o = 0.1t$) using the relationship given above, as shown in figure 2-2. This graph can be used to select a sensor radius for a desired maximum pressure.

Because the structure is circular, a simple analytical model can be used to determine the capacitance as a function of applied pressure, for a given sensor radius. Referring to figure 2-1, the total capacitance can be calculated by integrating the incremental contributions across the area of the membrane:

$$C = \int_A \frac{\epsilon_o dA}{d_o - w_A} \tag{2.4}$$

Substituting equation 2.1 for the deflection of a clamped circular membrane undergoing small deflections, an explicit expression for the capacitance of the pressurized

structure can be found by integrating across the entire membrane:

$$\begin{aligned} C &= \int_0^{2\pi} \int_0^a \frac{\epsilon_o r dr d\theta}{d_o - w(r)} \\ &= 4\pi\epsilon_o \sqrt{\frac{D}{P d_o}} \ln\left(\frac{8\sqrt{D d_o} + a^2\sqrt{P}}{8\sqrt{D d_o} - a^2\sqrt{P}}\right) \end{aligned} \tag{2.5}$$

for $P > 0$.

Representative capacitance versus pressure curves are given in figures 2-3 and 2-4. Also shown on these plots are results of finite element analysis of the structure, which is discussed in the next section.

As the pressure approaches the maximum (touching of plates) the capacitance becomes highly nonlinear, so that operation in the lower range of applied pressure is more desirable. The percent nonlinearity of the capacitance can be expressed as:

$$\%N = 100 \times \frac{C - C_{linear}}{C_o} \tag{2.6}$$

where C_{linear} is defined to be:

$$C_{linear} = C_o + \left[\frac{C_{fs} - C_o}{P_{fs}}\right] P \tag{2.7}$$

where P_{fs} is the desired full scale pressure, and $C_{fs} = C|_{P=P_{fs}}$ (see fig. 2-5).

By way of example, a plot of the nonlinearity is given in figure 2-6, for two sensors, one with a radius of 300 μm and the other with a radius of 100 μm, for an arbitrarily chosen full scale pressure of 10 psi. The plots show that the smaller sensor has a nonlinearity which is orders of magnitude lower than the larger one. This advantage is gained at the expense of sensitivity, as shown in figure 2-7, where the pressure sensitivity is:

$$\frac{1}{C}\frac{dC}{dP} = \frac{2\pi\epsilon_o}{CP}\left[\frac{16a^2 D}{64 D d_o - a^4 P} - \sqrt{\frac{D}{P d_o}} \ln\left(\frac{8\sqrt{D d_o} + a^2\sqrt{P}}{8\sqrt{D d_o} - a^2\sqrt{P}}\right)\right] \tag{2.8}$$

again for $P > 0$.

As the sensor radius is reduced, the pressure sensitivity for a given pressure range

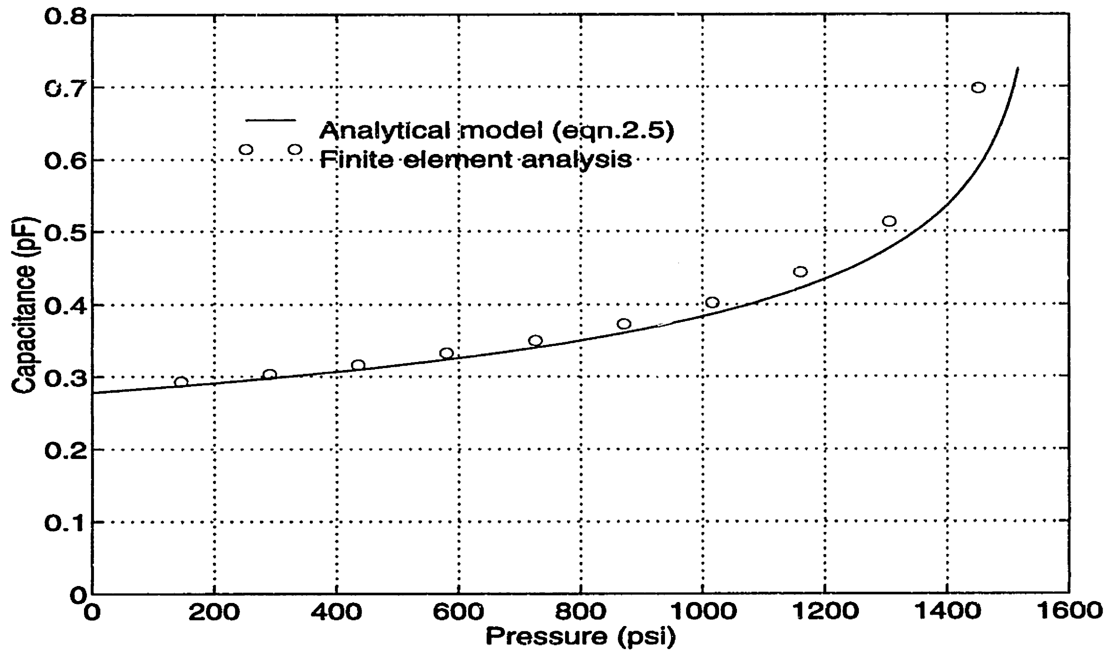


Figure 2-3: Capacitance vs. pressure for sensor radius=100 μm, membrane thickness=10 μm, air gap=1 μm

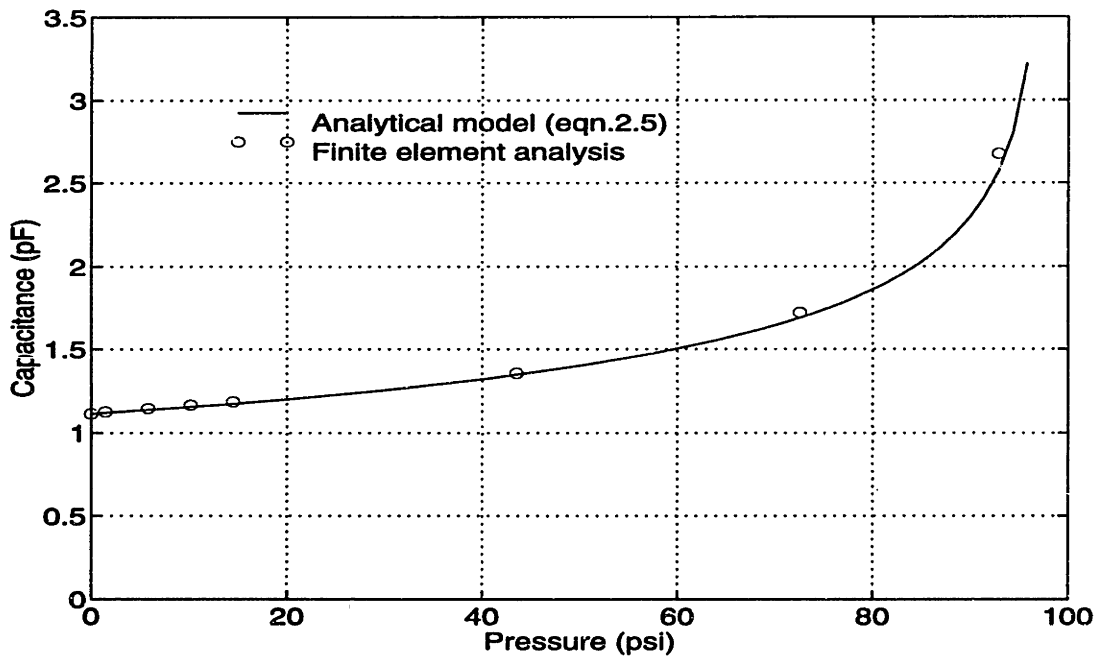


Figure 2-4: Capacitance vs. pressure for sensor radius=200 μm, membrane thickness=10 μm, air gap=1 μm

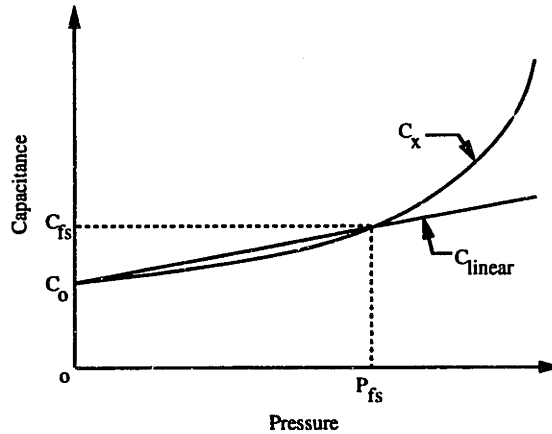


Figure 2-5: Definition of C_{linear} for nonlinearity calculation

decreases, due to the relative increase in stiffness of the membrane for a given pressure load. The tradeoff in nonlinearity vs. sensitivity can be exploited in developing schemes taking advantage of both aspects, by utilizing both large and small devices to contribute high sensitivity and low nonlinearity respectively. Specifically, for a given full-scale pressure a small diameter sensor can be used for linearity, while the large diameter sensor provides high resolution and sensitivity [37]. By suitably manipulating signals from the two sensors, it may be possible to continuously linearize the output.

It has also been shown that the linearity of a capacitive pressure sensor can be improved by operating the device in a touch-mode, where the membrane has flattened-out against the stationary electrode[38]. This type of device can be achieved either by operating the structure at pressures that cause it to flatten out (with a suitable insulating layer present on the membrane surface), or by stiffening the center portion with a boss that is thicker than the rest of the membrane. It is believed that this mode improves linearity of the response because the nonlinearity of the deflection is compensated for by the stiffening of the membrane as it is pressed against the stationary electrode, resulting in a more linear characteristic. However, the center boss can complicate fabrication.

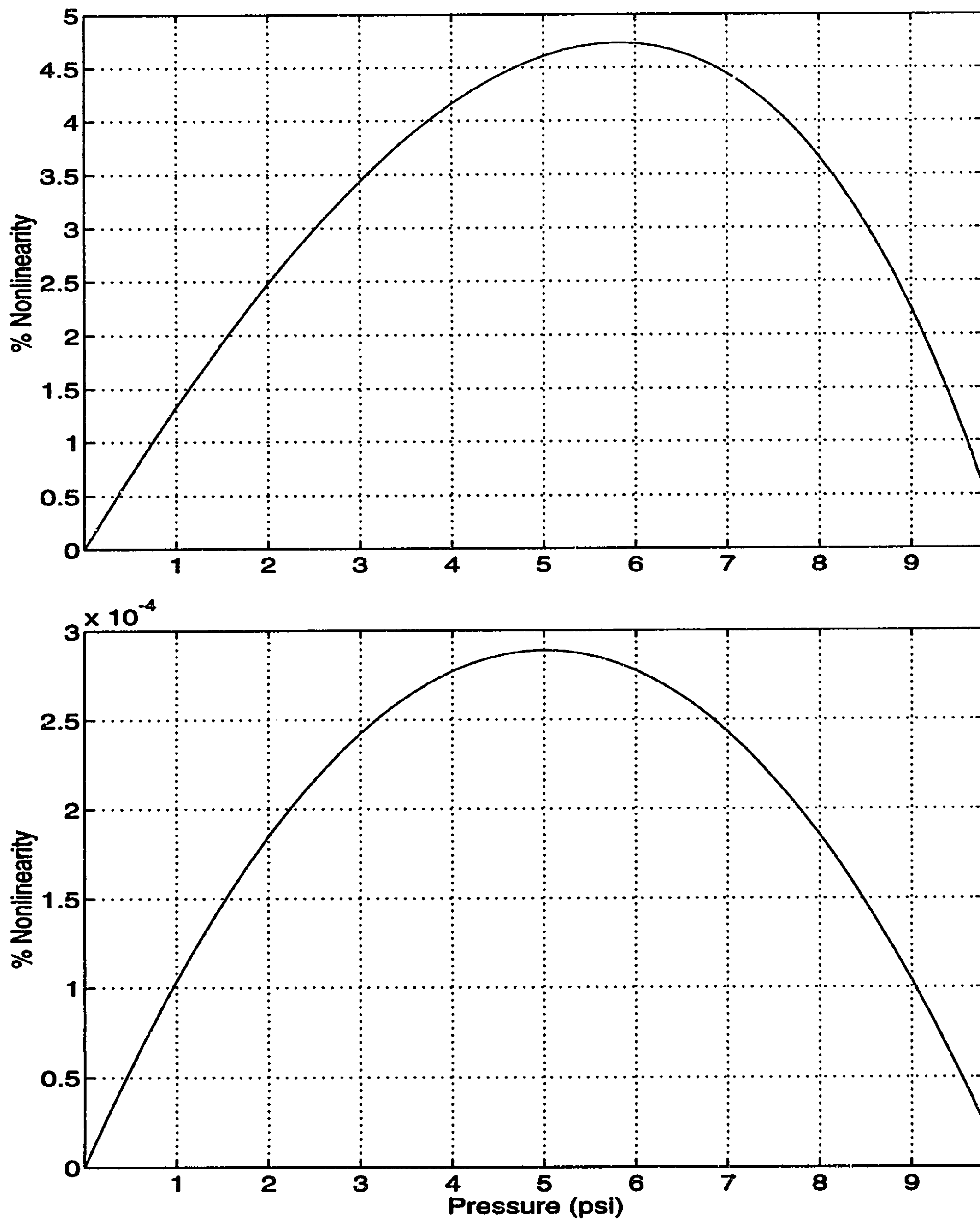
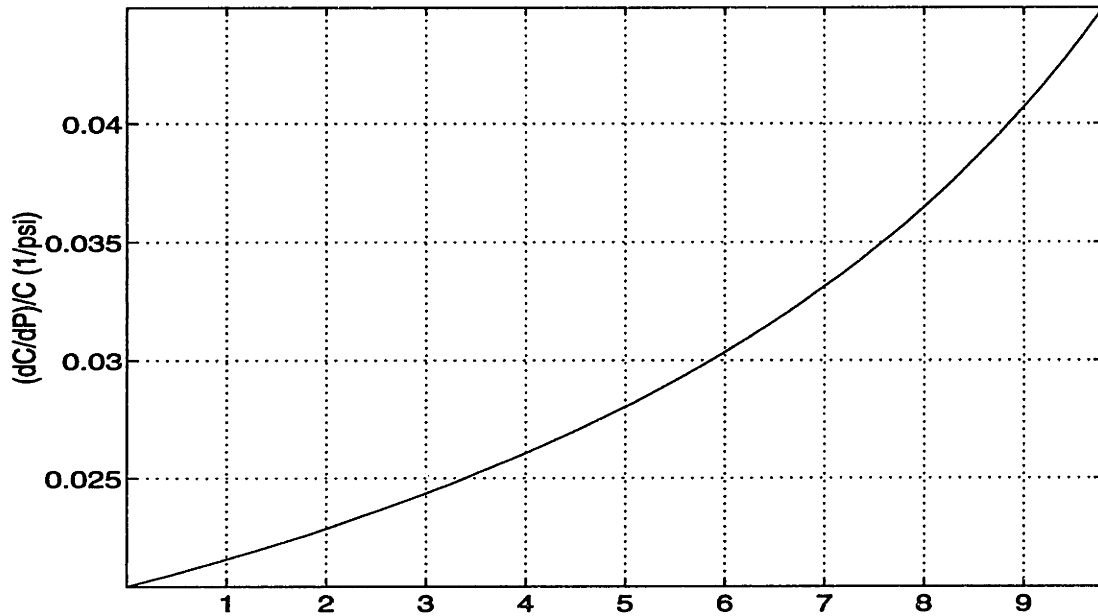


Figure 2-6: % Nonlinearity for sensors with a) radius=300 μm b) radius=100 μm



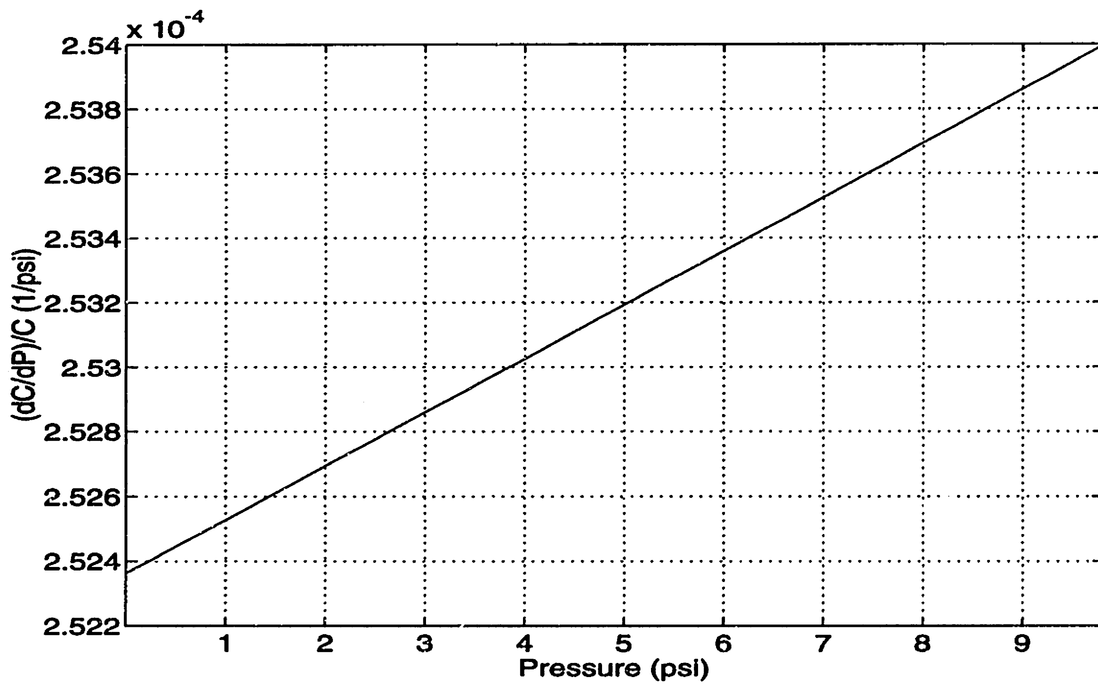


Figure 2-7: Pressure sensitivity for a) radius=300 μm b) radius=100 μm

2.2 Finite element simulation

In order to verify the validity of the analytical model, the capacitance-pressure characteristics were also obtained by simulating the structure using finite element analysis. The structure was simulated as a circular parallel plate capacitor, with one stationary plate and one movable plate. A uniform pressure was applied to the movable plate, which was constrained to have zero deflection and zero rotation at the edge (i.e. clamped edge). The stationary plate was discretized into 12 sections, each with 25 elements of equal area. The movable plate was discretized as shown in figure 2-8, with a finer mesh in the center and at the edges of the plate, since the stresses were expected to be larger in these regions. The solid modelling program PATRAN[39] was used to construct and mesh the model, and ABAQUS[40] was used to perform the finite-element analysis. The output of ABAQUS contains a matrix of deflection and stress values for each element of the membrane. In order to calculate the capacitance between the two plates, a program called FastCap[41], developed at MIT, was employed. FastCap takes as input an ABAQUS file containing the geometries and relative spacings of 2 or more conductors, and uses a multipole acceleration algorithm to calculate the net capacitance and conductance between the conductors.

The capacitance-pressure characteristic was obtained by applying a fixed pressure load to the movable membrane, simulating via FEA to obtain the deflected membrane shape, and then using the resulting matrix to calculate the capacitance using FastCap. This was repeated for a number of pressures. Simulations were done for two membrane radii: 100 μm and 200 μm. Figures 2-3 and 2-4 show the results, as compared to the analytical calculations. As expected, the simulations closely match the curves obtained using the analytical equation at the lower pressures. They deviate as the load approaches the touch-down pressure, giving higher values than the analytical solution indicates. This may be attributed to the fact that FastCap takes into account fringing fields associated with the edges of the plates, which result in larger charge densities in these regions and therefore higher capacitance.

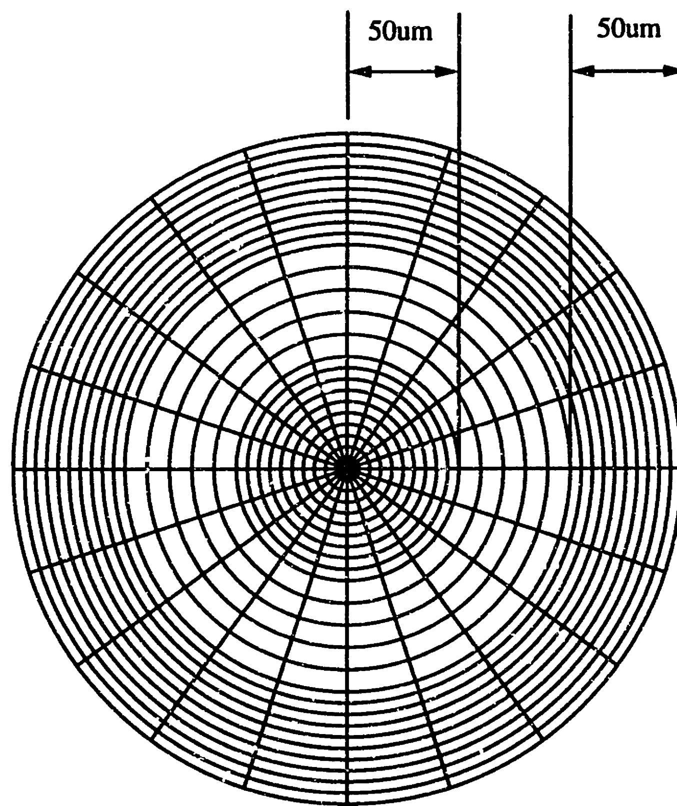


Figure 2-8: FEM mesh used for movable membrane

2.3 Self-testing

It is desirable to be able to test the sensor response before use, in order to verify its functionality. This can be done by means of electrostatically simulating an applied pressure on the movable plate. The pressure exerted on the membrane can be related to the applied electric field $\mathcal{E}$ by the following relationship:

$$P(r) = \frac{1}{2}\epsilon_o \mathcal{E}^2 = \frac{1}{2}\epsilon_o \left[\frac{V}{d_o - w(r)}\right]^2 \tag{2.9}$$

where V is the voltage applied across the plates of the capacitor and d_o is the zero-load gap spacing between the plates. The limiting factor in this test is the maximum breakdown voltage that can be sustained by the dielectric used to separate the two plates. For the sensor, the plates are separated by air; however in the field regions the metal lines run over a layer of low-temperature oxide. Assuming a dielectric strength of 1MV/cm for a deposited oxide with a thickness of 0.5 μm, the maximum pressure that can be tested is on the order of 25 psi, or about 170kPa. This may be adequate for a low pressure range sensor, but will not cover the full scale for a smaller sensor, with a higher pressure range.

In the equation given above, the membrane deflection $w(r)$ is a function of the pressure, and thus the electric field across the plates, so that an iterative solution is required to determine the pressure as a function of voltage. The pull-in voltage, that which will cause the two plates to touch, can be obtained through a coupled electromechanical simulation of the behavior of the membrane using the MEMCAD system. Doing such a simulation reveals that the membrane does not smoothly deform until the plates touch, but will continue to deform until a pull-in voltage is reached, at which time it will suddenly deflect in to touch the stationary electrode. The simulated pull-in voltage for a membrane of radius 350 μm with an air gap of 1 μm is approximately 55V [42].

Chapter 3

Fabrication

This chapter describes the detailed fabrication sequence for the pressure sensor. The complete process traveller is given in Appendix A. Following an overall description, various aspects of the fabrication are elaborated on, including some experimental observations on the three main areas of electrochemical etching, silicon wafer bonding in controlled ambients, and metal bonding.

3.1 Overall process sequence

The starting materials for the sensor consist of a device wafer and a handle wafer. The handle wafer is n-type <100> silicon, with a resistivity of 0.5-2 Ω-cm, and is polished on both sides. The wafer is subjected to a $POCl_3$ diffusion to heavily dope the front and back surfaces to ensure good electrical contact during the etchback step (section 3.3). The device wafer is a double-polished p-type <100> wafer, of resistivity 10-20 Ω-cm. It is prepared by implanting and diffusing phosphorus into the front side of the wafer to create a junction of depth 10 μm. This layer is the electrochemical etchstop, and will form the movable plate of the capacitor. The layer will also eventually be used as a substrate for any circuitry needed for signal conditioning. Thus the doping level of this layer will eventually be determined by the substrate requirements of the circuit fabrication process to be used.

The first step in the process is the formation of shallow circular cavities in the

handle wafer by plasma-etching (fig. 3-1a). The cavities are etched to a depth of 1 μm using an SF_6 plasma, and the radius determines the sensor dimension. Next, a narrow deep hole is formed at the center of each cavity, using a laser etching technique, in which an argon-ion laser beam is used to etch silicon in the presence of a chlorine ambient[43] (fig. 3-1b). This hole has a diameter of approximately 50 μm and is intended to have a depth of about 400 μm; however in reality the holes were formed to a depth of only 150 μm for the devices in this thesis. Figure 3-2 shows an SEM photograph of the surface of the laser-etched hole.

The next step is the joining of the two wafers using silicon wafer bonding (fig. 3-1c). This is done using a specially designed bonding chamber, to allow the wafers to be contacted in a controlled gas mixture. After contact, the wafers are annealed for one hour at 1000°C in an oxidizing ambient, to strengthen the bond and grow an oxide layer of about 5000Å. The oxide is removed from the device wafer side and patterned on the handle wafer side to leave a 1cm wide ring around the edge of the wafer. This oxide ring is used to protect the edges of the handle wafer from exposure during the electrochemical etching step.

The wafer pair is then thinned, using a combination of chemo-mechanical polishing and electrochemical etching, to leave a 10 μm thick layer of n-type silicon bonded to the handle wafer (fig. 3-1d). This results in the sealed cavity structure described in chapter 1, which can be used as the basis for a variety of sensors, as shown in figure 1-3 [44]. It is at this point in the process that the wafer would undergo a standard CMOS process sequence to fabricate the signal detection circuitry; however, CMOS fabrication was not investigated in this thesis in order to focus on the micromachining aspects of the process.

The next step in sensor fabrication is the formation of an electrical contact to the membrane, accomplished by means of a patterned boron implant into the membrane through a screening oxide layer, followed by an anneal to drive-in and activate the dopant (fig. 3-1e). After the screening oxide is removed, a layer of low temperature oxide (LTO) is then deposited and patterned to open contact holes and and clear the LTO from the membrane (fig. 3-1f).

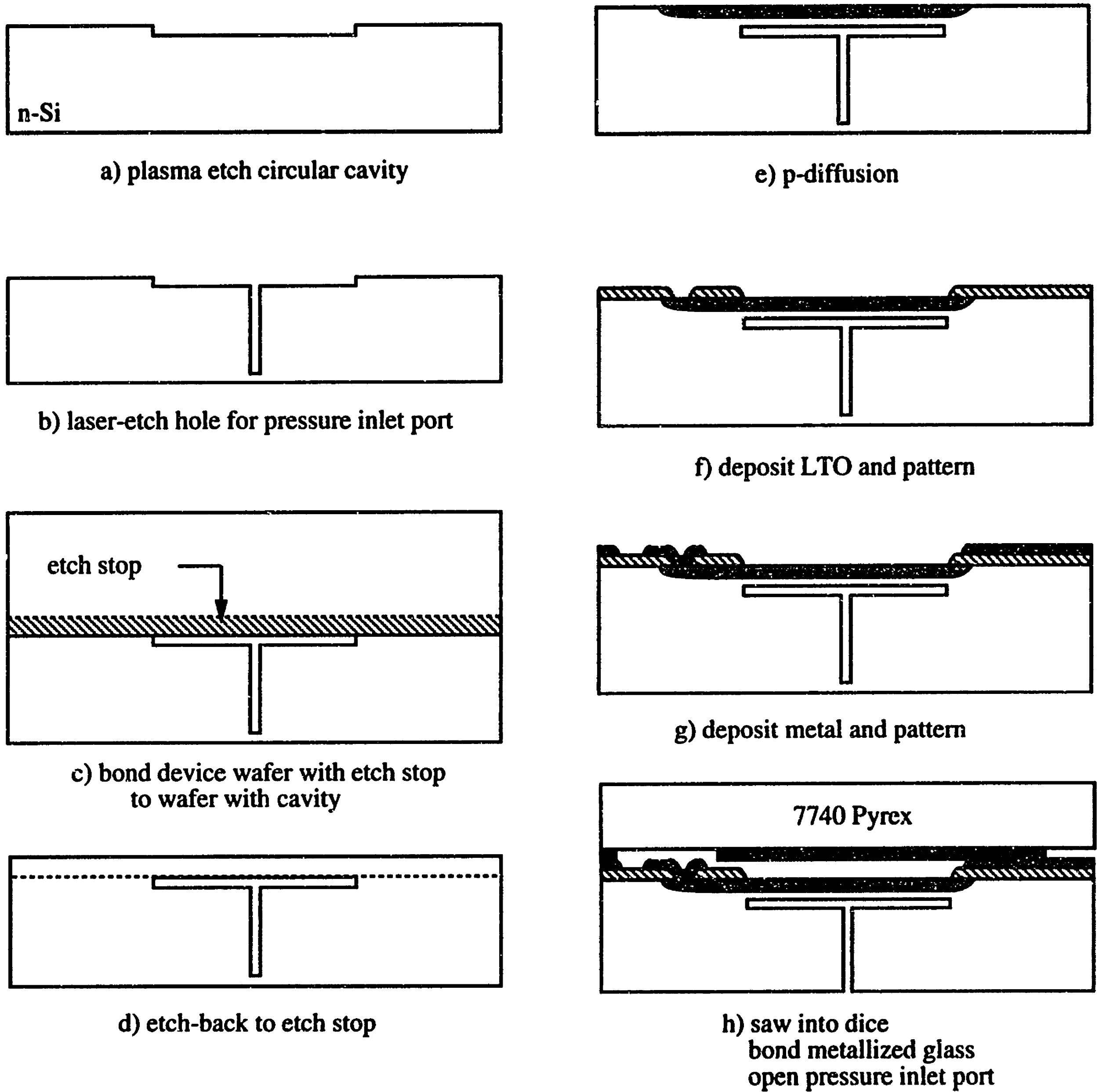


Figure 3-1: Complete fabrication sequence for capacitive pressure sensor

Figure 3-2: SEM of laser-etched via hole

Metallization is done using electron-beam evaporation of chromium and gold, and is patterned with a liftoff process. The wafers are subsequently sawed into $1cm^2$ dice. At this stage, the pressure inlet holes on the backside of each die are opened, again using laser etching (fig. 3-1g-h).

The top electrode of the capacitor is composed of patterned metal layers deposited on a glass wafer. The glass (Corning #7740 Pyrex) provides a rigid overpressure stop thus serving a packaging function, and is metallized using the same procedure as for the silicon wafers, and then sawed into dice. The glass and silicon are bonded together on a die-by-die basis using a gold-gold thermocompression bond, as discussed in section 3.5.2.

At this point the sensor is basically complete. Final packaging steps include mounting the die pair in a header and wire bonding to the bond pads along the outer edges of the silicon die.

The following sections elaborate on details involved in implementing the process, and focus on the areas of electrochemical etching, bonding in controlled ambients, and the metal bonding technique.

3.2 Mask set description

The mask set used for fabrication is given in Appendix C, in figures C-1 to C-5. The die size used is $1cm^2$ and each die has 4 rows of 6 sensors each, with each row containing sensors of radii 350, 240, 200, 130, 110 and 100 μm, corresponding to maximum pressure ranges of 10, 40, 80, 450, 900 and 1300 psi respectively. Metal contacts lead to pads along the edge of the die. The glass die has patterned metal to match the membranes on the silicon substrate, and is sized slightly smaller at $0.97cm^2$ to allow access to the bond pads, which are placed along two edges of the silicon die.

The metallized areas are sized to provide maximum bonding area to the silicon substrate, while also minimizing parasitic capacitance. To increase the bonded area, the unused field regions are covered with metal which is not electrically connected to any part of the devices. Similarly, to ensure a good mechanical bond around

each sensor while reducing parasitics, there is a partial ring of metal around each membrane, which is also not connected to the top plate metal. Contact to the top plate is made with one square of metal at the edge of the membrane.

Since the bond pads are restricted to 2 outer edges of the die, some of the metal lines leading to the pads are long, thus increasing the amount of parasitic capacitance to the substrate through the LTO. This problem can be reduced with a mask design in which the bond pads are closer to the sensor.

3.3 Electrochemical etching of silicon (ECE)

Presently there are a number of techniques available for the bulk removal of silicon, and a variety of etchants and etchstops. Chemomechanical polishing, which involves the removal of silicon by physical abrasion of the surface, uses special polishing pads and silica slurry to obtain a wide range of removal rates, but is generally used for bulk removal, and not for fine thickness control. Etchstops can be divided into two major categories: chemical and electrochemical etchstops. Among the etchants currently being used for silicon micromachining are potassium hydroxide (KOH), ethylenediamene pyrocatechol (EDP), hydrazine, and tetramethylammonium hydroxide (TMAH), all of which are anisotropic (preferentially etch <100> over <111> planes). Chemical etchstop layers usually consist of a heavily doped p++ layer which has a considerably lower etch rate than lightly doped silicon when using the previously mentioned etchants, as long as the boron levels in the etchstop layer are in excess of 10^{20}cm^{-3} [45]. The high dopant concentration necessary to achieve etchstopping can result in tensile stresses in the heavily doped layers, as well as imposing a limit on high temperature processing of the substrates to avoid spreading of the dopant into adjacent regions. In addition, the heavily doped silicon cannot be used as a substrate for circuitry.

An alternative method of selectively etching silicon is the technique of electrochemical etching (ECE). It has been found that when p or n-type silicon is immersed in an alkaline etchant such as potassium hydroxide and a variable bias is applied to

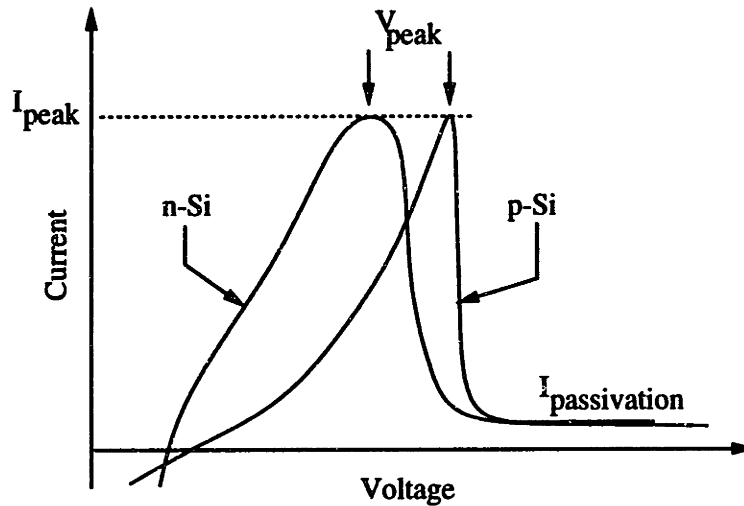


Figure 3-3: Current-voltage characteristics of p-Si and n-Si

the silicon with respect to the solution, that the current through the circuit follows the characteristic shown in figure 3-3 [46, 47]. The silicon will continue to etch until the potential applied reaches the passivation potential, at which time a layer of anodic oxide forms on the wafer and passivates the surface, thus terminating etching. The current required to form this anodic oxide is the peak passivation current and the current required to maintain the oxide layer is the steady-state passivation current.

The difference in passivation potentials between p-Si and n-Si can be utilized to selectively etch p-Si over n-Si in a diode structure, by biasing the n-layer at a level anodic to its passivation potential, as shown in figure 3-4. Assuming the reverse-biased p-n junction diode is ideal so that the leakage current is negligible, the p-type silicon is isolated from the circuit so that it floats to its open circuit potential and continues to be etched until it has been completely removed. At this time current flows through the remaining n-silicon causing it to be passivated by a layer of anodic oxide. The

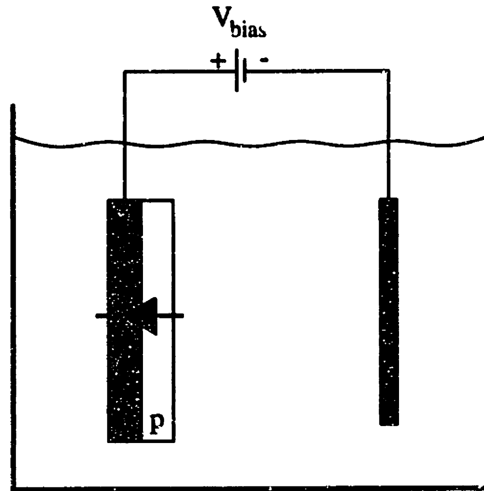


Figure 3-4: Basic two electrode junction electrochemical etchstop

technique is very useful in obtaining membranes with controlled thicknesses, without the requirement of a heavily doped etchstop layer.

Extensive work has been done by a number of groups to characterize the etch-rate and current-voltage characteristics of p and n-type silicon as well as pn junctions for various etchant concentrations and temperature conditions, the majority of the studies being done using KOH [47, 48, 49]. One of the conclusions of these investigations was that there are two factors that can affect the success of the electrochemical etching technique. The first involves the formation of ohmic drops along the n-type etchstop layer. It was found that if the sample is contacted at only one point, as is often the case when fabricating bond-and-etchback-SOI substrates, voltage drops along the n-layer due to resistive losses can result in the bias in portions of this layer falling below the passivation potential[48]. In these areas, the anodic oxide required to passivate the surface is not formed, and the silicon is overetched, thus destroying the membrane to be formed. The problem can be avoided by using a setup that allows contact over a large area of the n-type etchstop layer. This can be accomplished easily with a structure that contains a direct silicon-silicon bond without an insulating layer, since all parts of the etchstop layer are then electrically accessible from the back of

the wafer. With this type of structure, the ohmic losses along the etchstop layer are much reduced so that no portion of the layer falls below the passivation potential. If an SOI configuration must be used, then ohmic drops can be reduced by providing electrical contact through the insulating layer by means of conducting vias[50].

The second problem in using ECE concerns the occurrence of premature passivation of the etch in the p-type silicon, resulting in an etched-back layer that is thicker than the junction depth of the etchstop layer. This problem has been observed by a number of groups, and appears to be affected by a variety of factors including the etchant type and temperature, the applied bias voltage, and the quality of the diode formed by the etchstop layer. Section 3.3.2 discusses experiments to investigate the etchant temperature dependence of this phenomenon.

3.3.1 Etching apparatus and procedure

The setup used for electrochemical etching is given in figure 3-5. The wafer is held in a specially designed Teflon jig by means of a vacuum hold, and electrical contact to the back surface of the wafer is made with gold-plated spring-loaded pins attached to wires leading out of the chuck. A piece of platinum wire mesh is sandwiched between the wafer and the jig to increase the contact area to the wafer. An EG&G PARC potentiostat is used to maintain a constant bias applied to the n-type silicon, by adjusting current through a platinum foil counter electrode. A double-junction Ag-AgCl reference electrode is used to monitor the solution potential. The etchant is a 20% by weight solution of KOH in H_2O, used in quantities of 4L for each etch. For some of the etches, a fluorocarbon surfactant (FC-129, manufactured by 3M Corporation) was used to decrease surface roughness, and was added in the amount of 2g/L of KOH solution. The etchant was contained in a stainless steel tub immersed in a water bath with a temperature control of $\pm 0.1^{o}$C, and all etching was performed in the dark. Wafers which had unpolished surfaces were initially polished until mirror smooth before the etching was started. Final surface roughness of the wafers after etchback was 200-700Å, as measured on a Topo-3D optical surface profilometer[51].

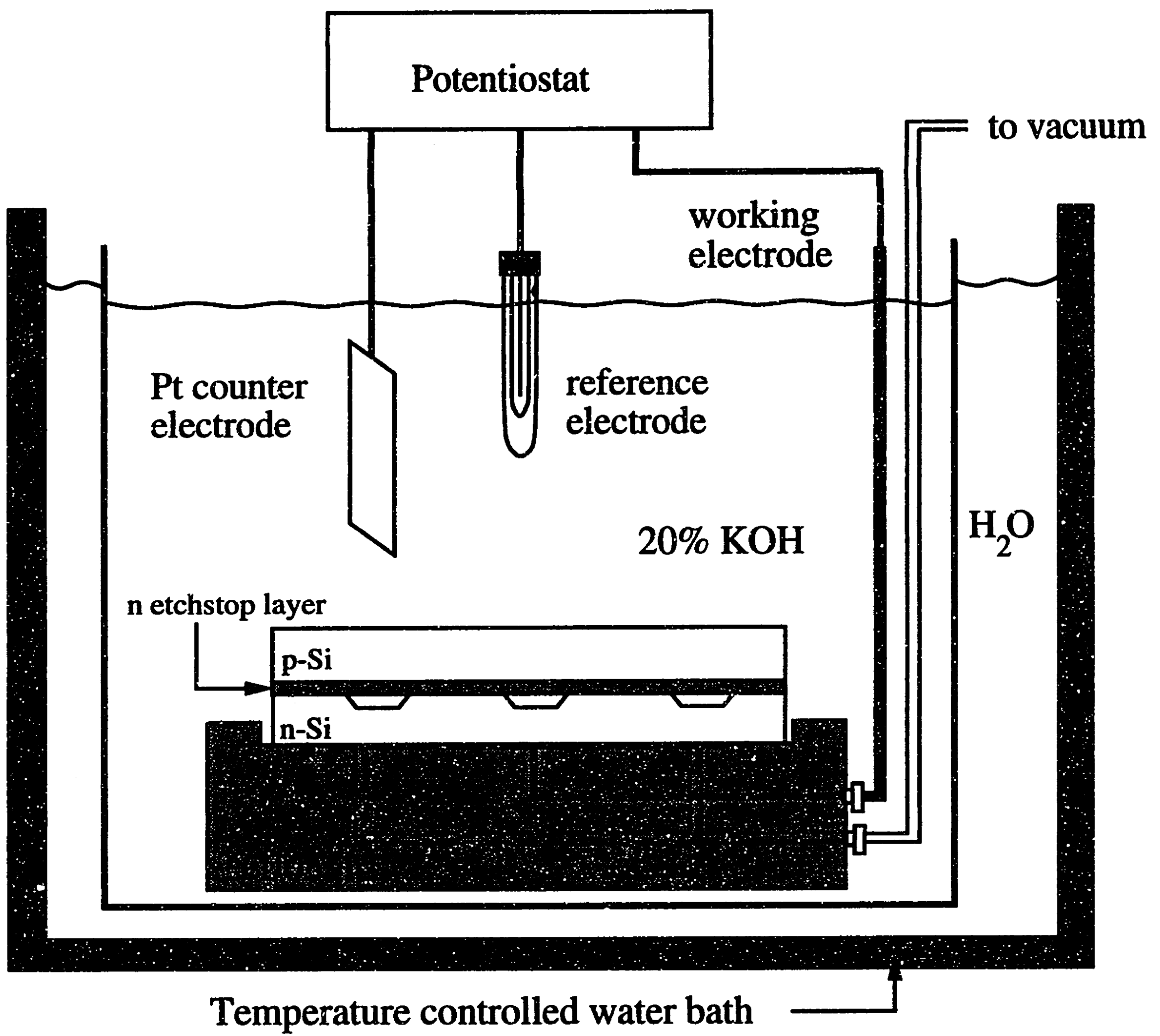


Figure 3-5: Electrochemical etchstop experimental setup

3.3.2 Experiment

As previously mentioned, the premature passivation phenomenon is affected by various factors, including etchant type and temperature, bias voltage, and junction quality. Experiments were done to investigate the effect of etchant temperature on this problem. Each pn junction sample consisted of 2 full 4-inch wafers bonded together, in which the n-type handle wafer was subjected to a phosphorus diffusion to heavily dope the surfaces ($> 10^{19}\text{cm}^{-3}$) for good electrical contact, and the p-type device wafer had a 10 μm thick etchstop layer formed by implanting and diffusing phosphorus. The handle wafer contained 12 cavities of depth 30-50 μm and diameter 3.6 mm.

Prior to the start of each etch, a current-voltage scan of the sample was done to ensure that electrical contact was being made to the n-layer, and to check for the presence of a diode structure. Figure 3-6 gives a representative I-V scan for a sample wafer pair, in which the current peak is due to the current required to passivate the n-type silicon extending beyond the O-ring on the jig, which is exposed to the etchant. If this area is covered by an oxide layer, grown during the bonding anneal, the I-V characteristic looks like figure 3-7, which more closely resembles a reverse-biased diode characteristic.

During the etch itself, the bias applied to the n-layer was held constant at 0V. As etching progressed, the current was monitored to determine the endpoint. Figure 3-8 gives the resulting I-t scan, in which the peak is quite sharp indicating a successful stop. Termination of the etch was also verified by observing that the evolution of hydrogen bubbles from the wafer surface had ceased.

3.3.3 Results

In order to determine the thickness of the etched back layer, the wafer was cleaved along the center of a cavity, and the thinned membrane was examined under an SEM. In using this technique, it appeared that all of the membranes were consistently 40 to 50% thicker than the expected value of 10 μm (fig. 3-9). However, measurements

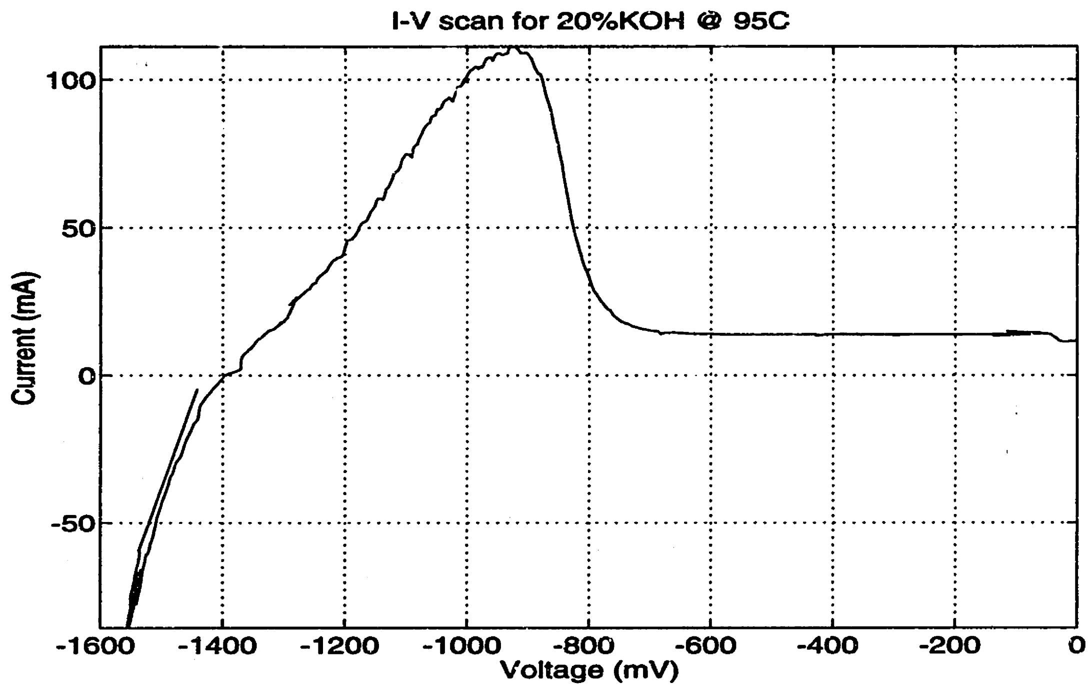


Figure 3-6: Current-voltage scan for ECE sample without oxide ring

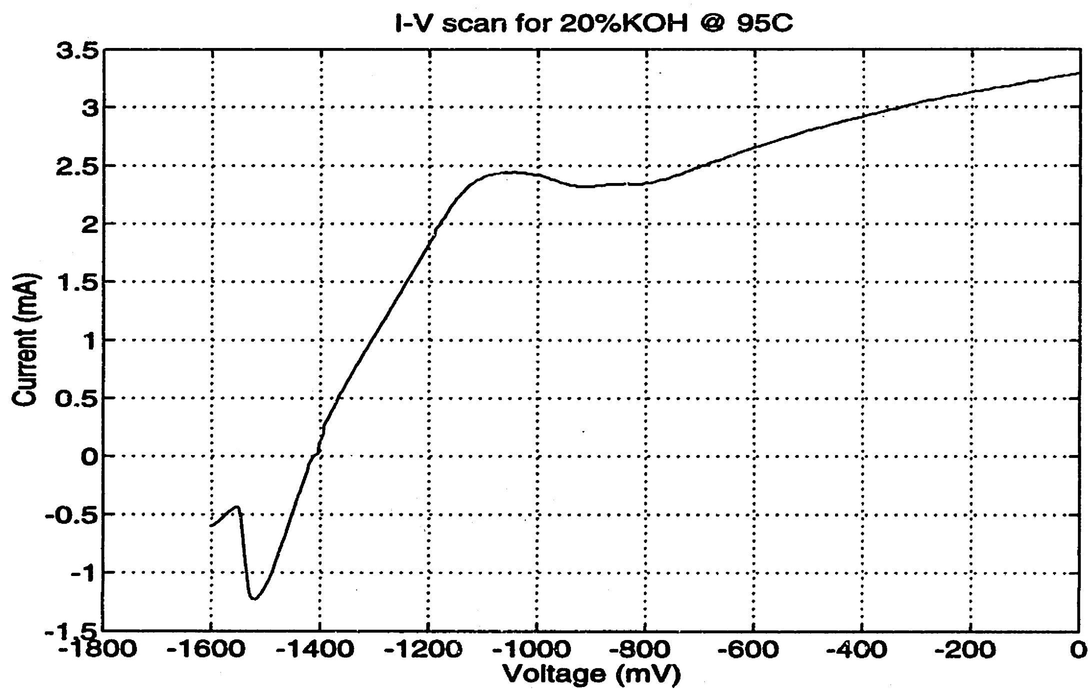


Figure 3-7: Current-voltage scan for ECE sample with oxide ring

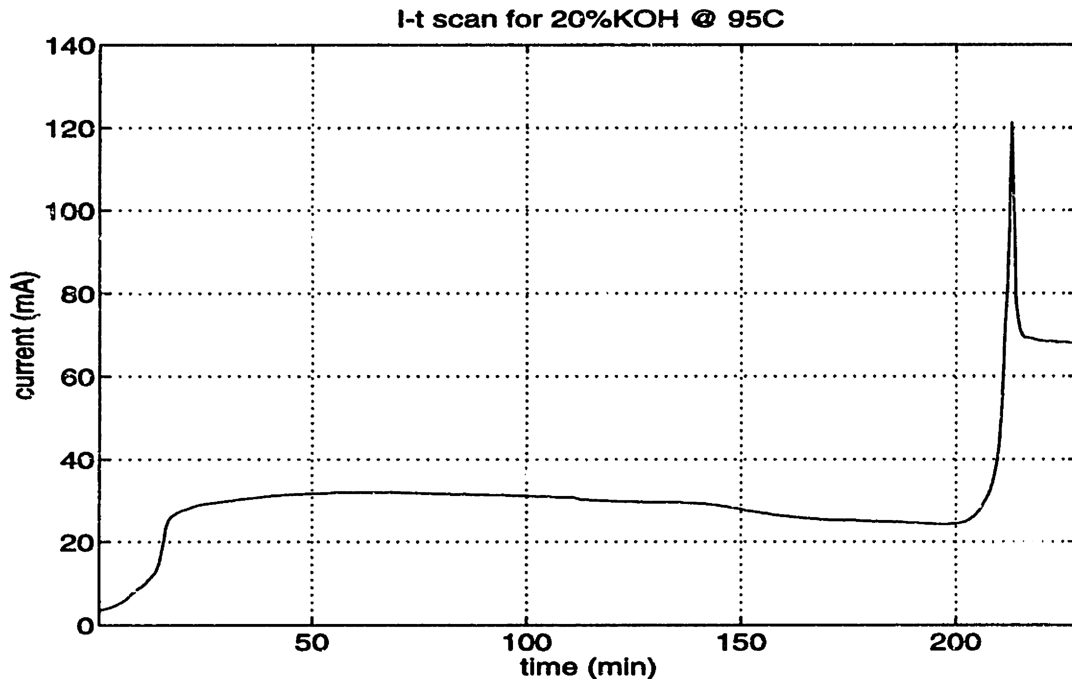


Figure 3-8: Current-time scan for ECE sample

made using a Dektak surface profilometer indicated that the discrepancy was smaller, and that the etched layer thickness was closer to 10% too high. This discrepancy was attributed to the fact that the SEM was not calibrated for measurements on a vertical scale, so that the SEM pictures could only be used to verify consistency between samples, and not for an absolute value of the thickness.

A cross-sectional schematic of the sample after etchback is given in figure 3-10. Of interest is the value of x_p, the amount of p-type silicon remaining unetched above the metallurgical junction, since if this value is zero, then the thickness of the membrane is determined by the junction depth of the etchstop layer. To determine x_p, spreading resistance profiling (SRP) of the surface dopant concentration was done on samples etched at various temperatures, the results of which are given in figures 3-11 and 3-12.

The SRP plots indicated a trend in the proximity of the etchstop point to the metallurgical junction, summarized in table 3.1. As etchant temperature was increased, the amount of unetched p-Si remaining decreased, and at an etchant temperature of 95°C, the etch stopping point appeared to reach the metallurgical junction.

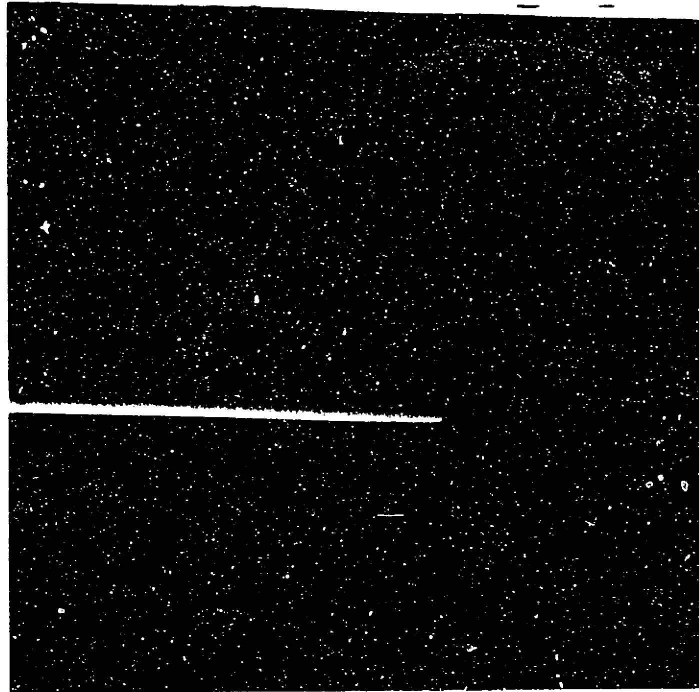


Figure 3-9: Cross-sectional SEM of membrane after ECE

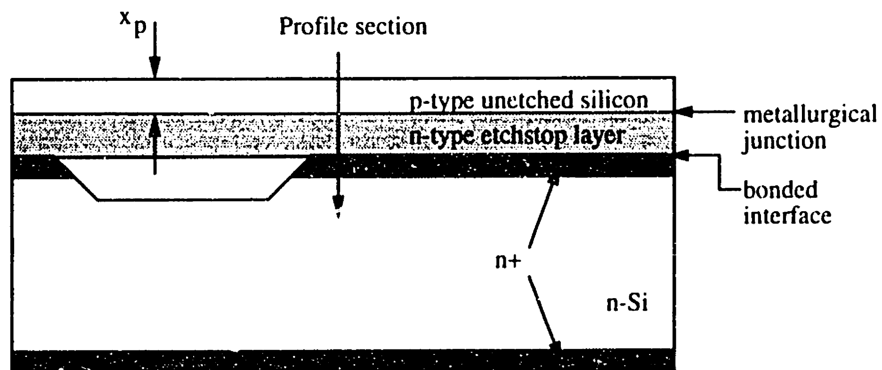
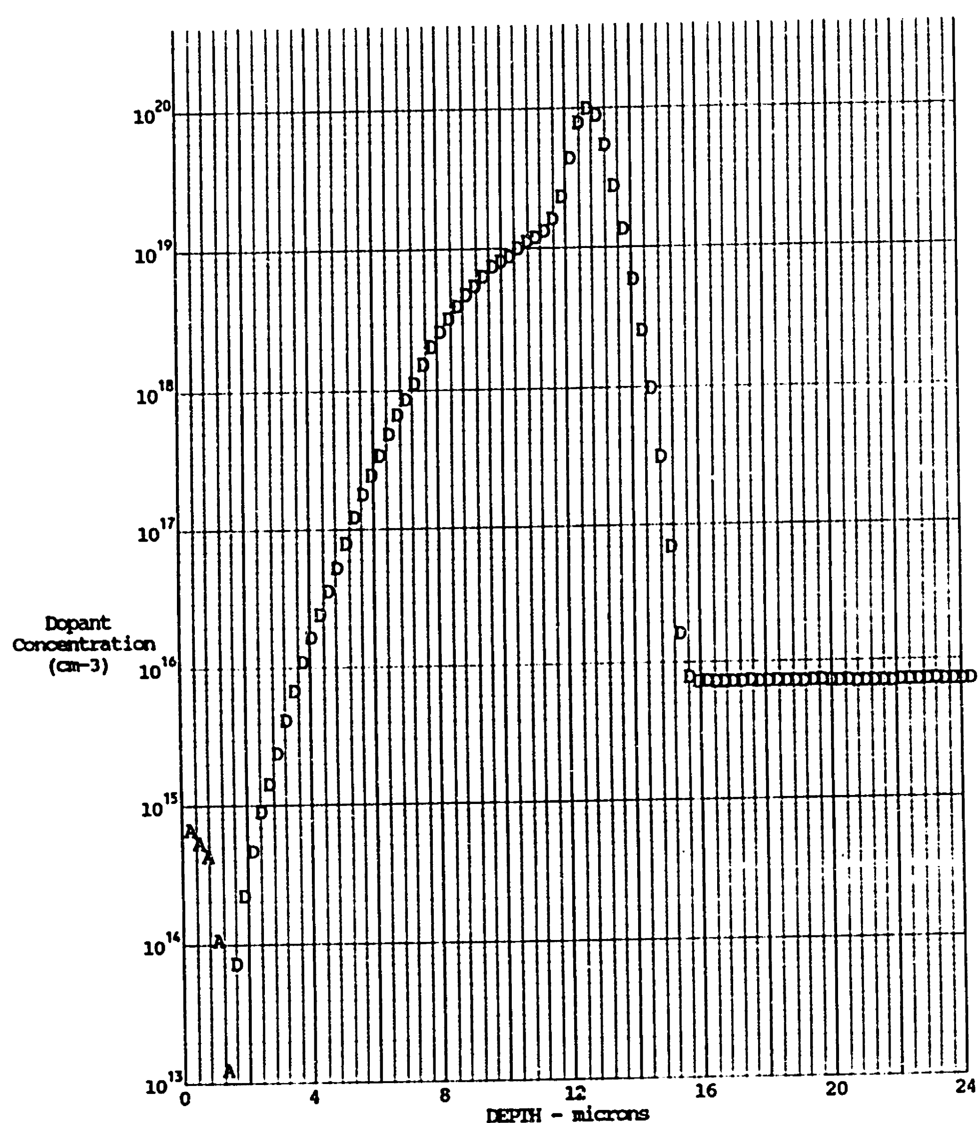


Figure 3-10: Schematic of sample used for spreading resistance profiles

Table 3.1: Electrochemical etch results

Etchant temp. (°C)	x_p from SRP (μm)
95	0.1±0.05
90	0.5±0.05
80	1.2±0.10
70	1.7±0.10

This trend can be explained as being caused by the relative temperature dependence of the peak passivation current and the junction leakage current. If the passivation current is a stronger function of temperature than the junction leakage current, then at a sufficiently high etchant temperature, the passivation current will exceed the leakage current until the p-layer has been completely removed. This appears to indicate that higher etchant temperatures can be used to decrease the effect of high junction leakage currents.



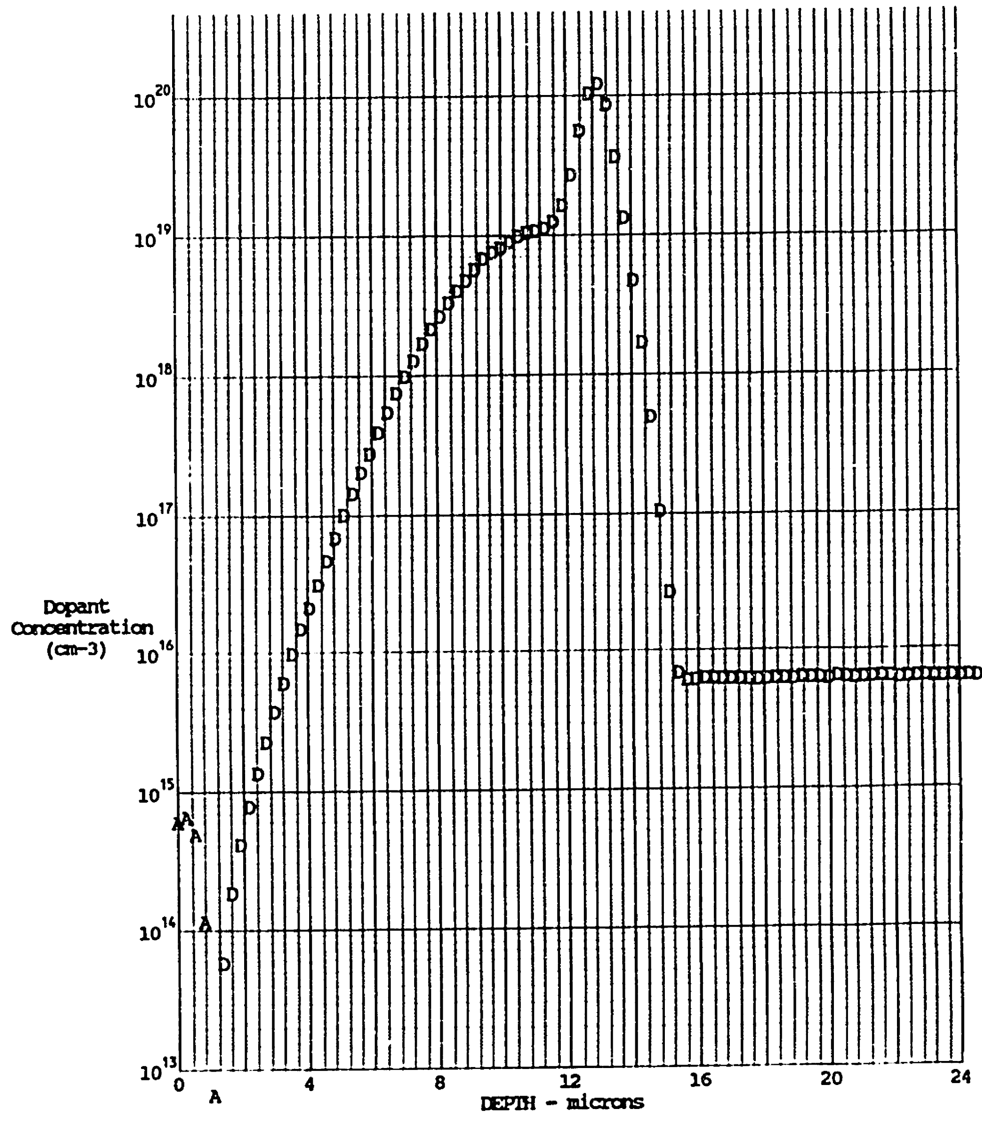
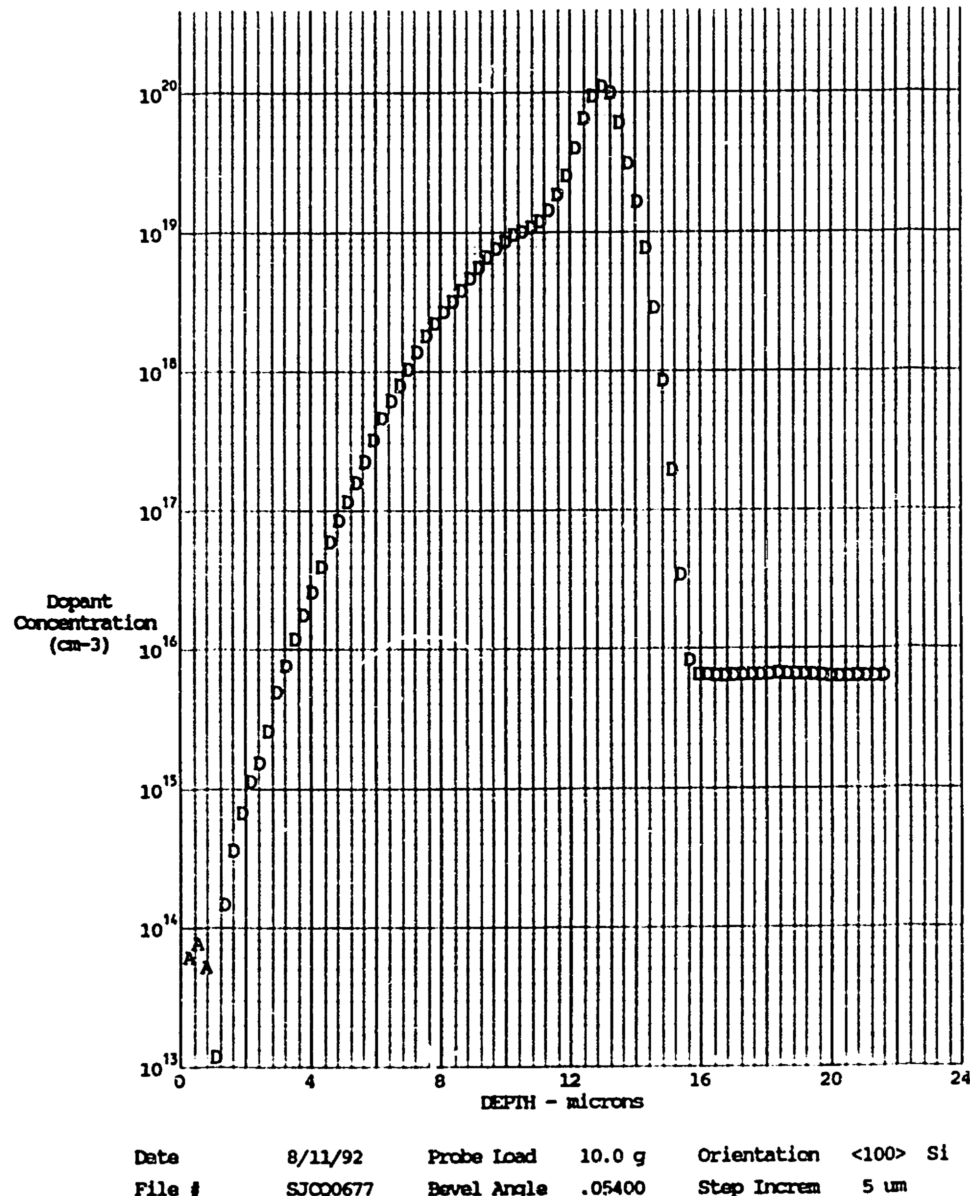


Figure 3-11: Spreading resistance profile for samples etched at a) 70°C, b) 80°C



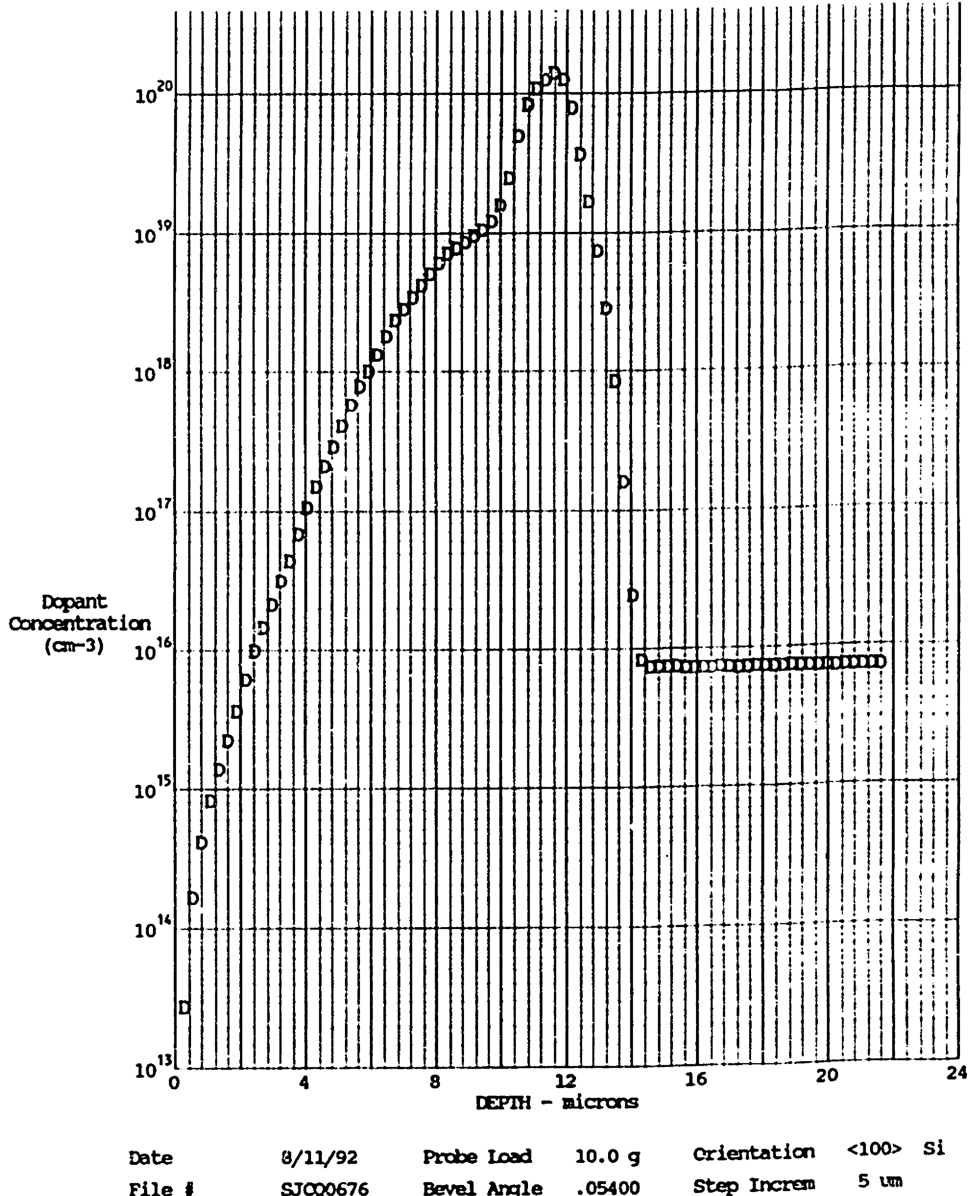


Figure 3-12: Spreading resistance profile for samples etched at a) 90°C b) 95°C

3.4 Bonding in controlled ambients

One of the key points to consider in the process is the ability to maintain the integrity of sealed cavities formed by bonding two wafers together. It has been shown that when silicon wafers with cavities are contacted in air and subsequently annealed, after annealing the residual pressure of the trapped gas in the cavities is approximately 0.8 atmospheres [29, 52]. This is a result of the reaction of the oxygen content of the trapped air with the sidewalls of the cavity, leaving the inert nitrogen remaining. It was also shown that if the bonded pair is thinned to form a membrane over the cavity and subsequently subjected to a high temperature step, the gas in the cavity will expand, loading the membrane. This can result in the occurence of plastic deformation of the silicon, leading to a permanent change in the shape of the membrane [53].

3.4.1 Model

A model has been developed by Huff [53, 54] to describe this deformation phenomenon. Figure 3-13 is a diagram of the structure under consideration, in which it is assumed that the gas trapped in the cavity obeys the ideal gas law, silicon behaves as a linearly elastic material with a zero temperature coefficient of modulus, and there is no residual stress initially present in the membrane. The third assumption is not justified if the membrane is heavily doped, particulary if boron-doped, since

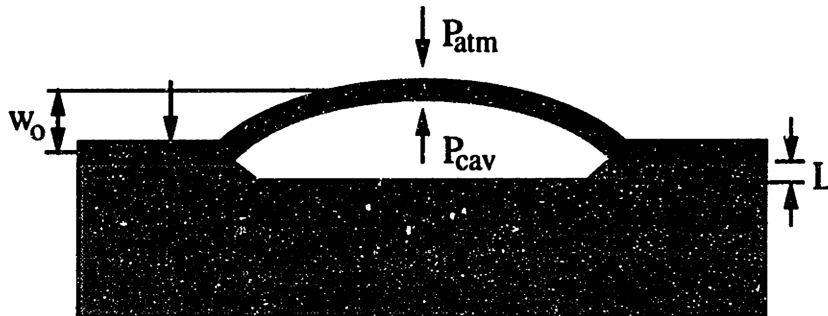


Figure 3-13: Model of sealed cavity under high temperature

it has been shown that such layers exhibit considerable tensile stress. However, for structures using the electrochemical etchstop technique for thinning, the membrane is moderately phosphorus doped, so that this assumption is justifiable. A more detailed study of the residual stress in wafer bonded layers can be found in [54], in which the buckling threshold technique was used to conclude that the stress in such layers does not exceed 4MPa in compression. Chapter 4 contains the results of load-deflection testing of membranes formed from the etchstop layer, which also indicate that the residual stress level is low ($\approx$ 25MPa in tension).

To avoid plastic deformation of the silicon membrane, the stress level in the membrane must not exceed a critical level referred to as the flow stress, which has been experimentally determined for single crystal silicon [55]. Therefore, of interest is the deformation of the membrane under high temperatures. The maximum deflection occurs at the center of the membrane and, assuming it undergoes small deflections only (deflection<half of membrane thickness), is given by [36]:

$$w_o = \frac{a^4}{64D}(P_{cav} - P_{atm}) \tag{3.1}$$

where P_{cav} is the residual pressure of the gas in the cavity, P_{atm} is atmospheric pressure, a is the cavity radius and D is the flexural modulus ($D = \frac{Et^3}{12(1-\nu^2)}$). P_{cav} is a function of the temperature of the wafers, and using the ideal gas law can be expressed as:

$$P_{cav} = \frac{T}{T_1}\frac{P_1 V_1}{V_1 + \Delta V} \tag{3.2}$$

where T_1=298K, P_1=cavity pressure at T_1, V_1=cavity volume at T_1, P_1 and the change in volume is approximated as a spherical cap so that $\Delta V \approx \frac{\pi}{2}a^2 w_o$.

Again from small deflection theory[36], the maximum stress in such a membrane occurs at its edge and is given by:

$$\sigma_{max} = \frac{3}{4}\left(\frac{a}{h}\right)^2 (P_{cav} - P_{atm}) \tag{3.3}$$

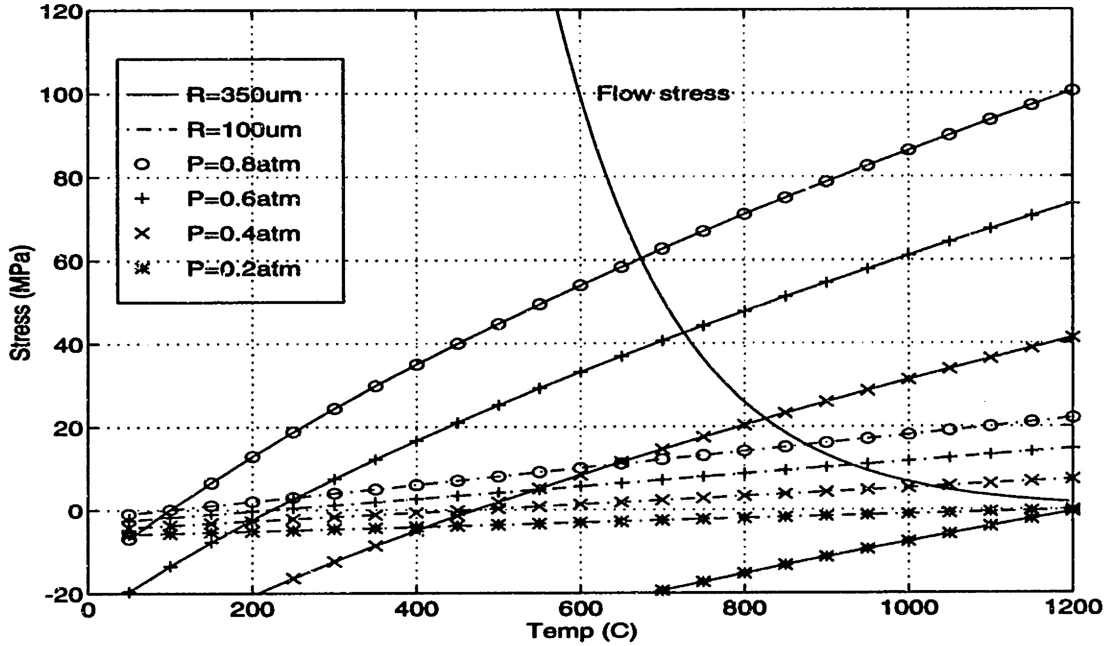


Figure 3-14: Stress vs. temperature for varying residual pressure, with membranes in small deflection. Cavity depth=1 μm, membrane thickness=10 μm

or, substituting equation 3.2,

$$\sigma_{max} = \frac{3}{4}\left(\frac{a}{h}\right)^2 P_{atm}\left[\frac{\frac{T}{T_1}\frac{P_1}{P_{atm}}}{1+\frac{w_o}{2L}} - 1\right] \tag{3.4}$$

Equations 3.1 and 3.2 can be solved for w_o, which is then used to obtain the membrane stress σ_{max}. To avoid plastic deformation of the membrane at a given temperature, the magnitude of the stress must remain below the flow stress of silicon at that temperature. Figure 3-14 is a plot of the stress as a function of temperature, for varying values of the initial trapped gas pressure in the cavity, calculated for two cavity radii (the membranes are all within the small deflection regime, as indicated by figure 3-15). Superimposed on this set of curves is the data for the flow stress of silicon as a function of temperature, taken from [55]. By way of example, if we select a cavity with a radius of 350 μm, with a residual gas pressure of 0.6atm, then the maximum safe temperature is approximately 720°C. However, if the residual pressure is lowered to 0.2 atmospheres, then the flow stress is not exceeded even at 1200°C.

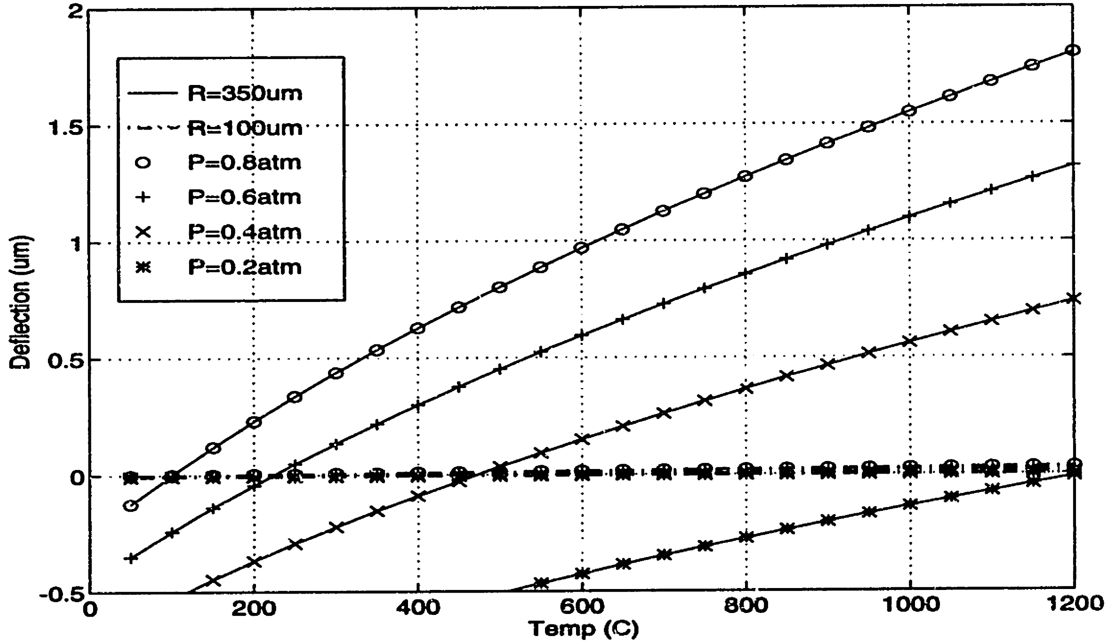


Figure 3-15: Deflection vs. temperature for varying residual pressure, with membranes in small deflection. Cavity depth=1 μm, membrane thickness=10 μm

A similar analysis can be carried out for membranes undergoing large deflections, in which case

$$w_o = 0.662\left(\frac{a^4}{Eh}\right)^{\frac{1}{3}}(P_{cav}(T) - P_{atm})^{\frac{1}{3}} \tag{3.5}$$

and

$$\sigma_{max} = 0.423\left[E\left(\frac{a}{h}\right)^2(P_{cav}(T) - P_{atm})^2\right]^{\frac{1}{3}} \tag{3.6}$$

Representative stress vs. temperature curves are given in figure 3-16.

These types of curves are useful in determining the process temperature limits for a given geometry. It is apparent that if bonding is done in pure oxygen, resulting in a vacuum in the cavity, then there is no danger of the membrane plastically deforming upwards at high temperatures. However, there may be deformation in the downward direction, especially if the cavity depth is large so that there is no surface available for the membrane to "bottom-out" and be constrained. Whether this will occur can be determined with similar stress-temperature plots, but this time comparing to the negative of the flow stress, as in figures 3-17 and 3-18. From figure 3-17, the

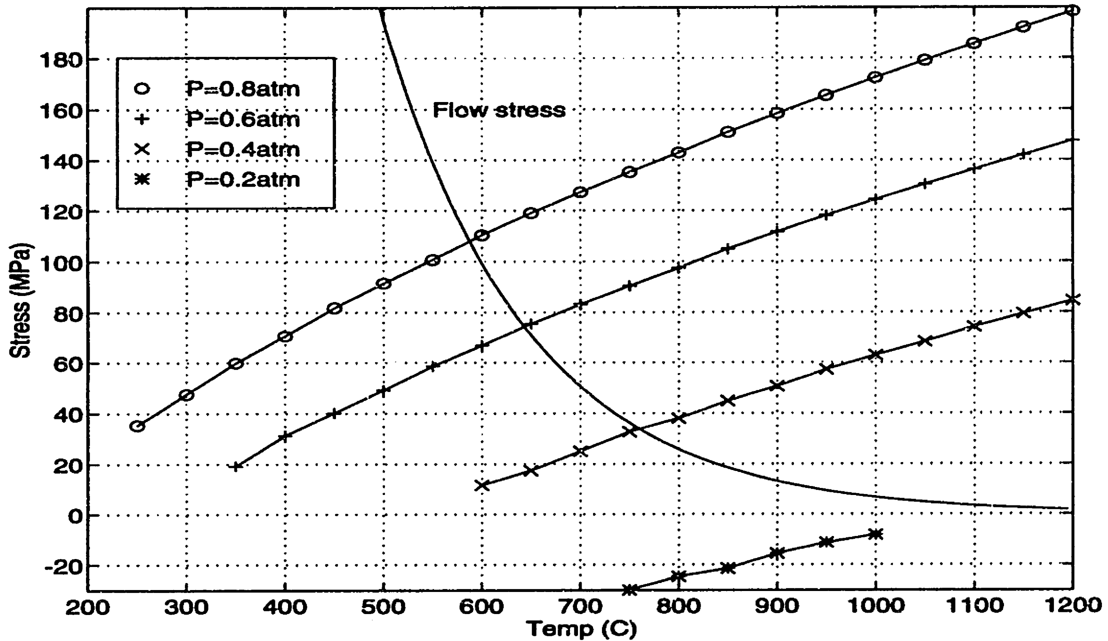


Figure 3-16: Stress vs. temperature for varying residual pressure, with membranes in large deflection. Cavity radius=1800 μm, depth=50 μm, membrane thickness=10 μm

temperature limit for a 350 μm cavity with a depth of 1 μm would be about 950°C, at a residual pressure of 0.2atm. However, if the cavity depth is increased to 10 μm, the safe temperature decreases to 800°C (fig.3-18). Thus for structures with large cavity depths, it may not be possible to avoid the occurrence of plastic deformation at high temperatures completely, even with a reduced trapped gas pressure in the cavity.

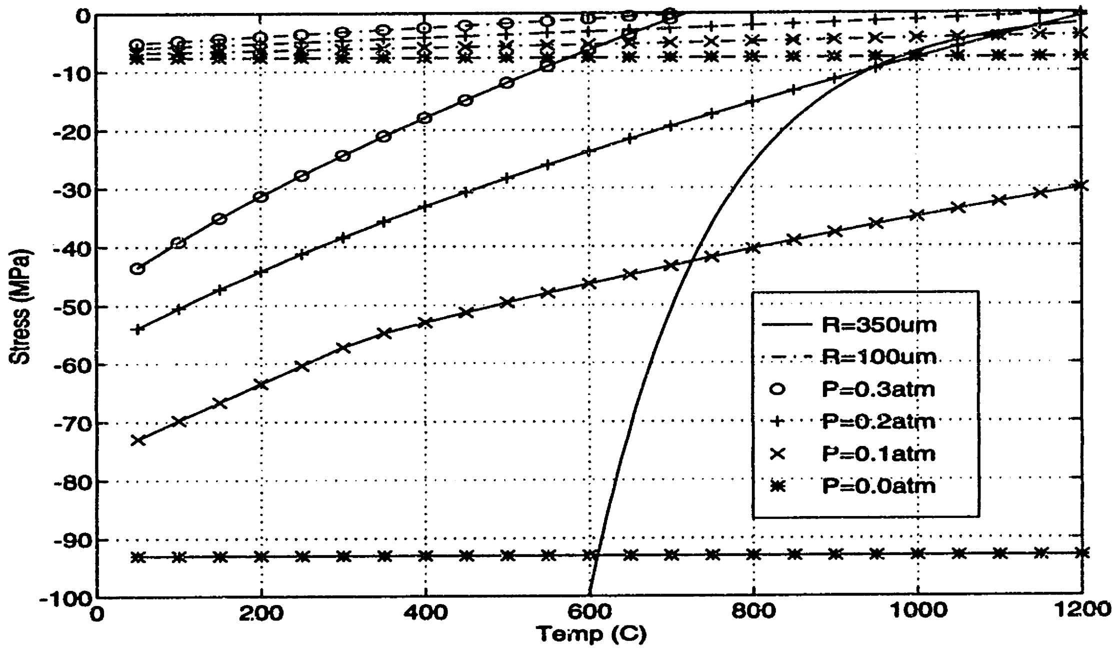


Figure 3-17: Stress vs. temperature for low residual cavity pressure. Cavity depth=1 μm, membrane thickness=10 μm

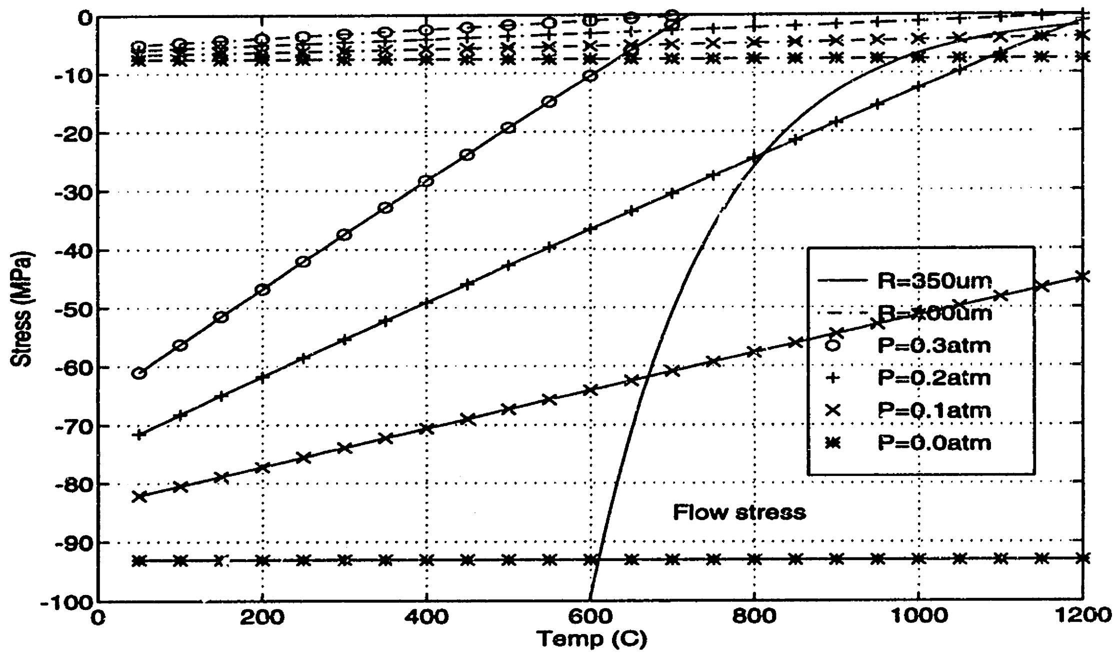


Figure 3-18: Stress vs. temperature for low residual cavity pressure. Cavity depth=10 μm, membrane thickness=10 μm

3.4.2 Bonding apparatus and procedure

In order to verify the theoretical calculations, a setup was developed in which wafers could be bonded in a variable mixture of oxygen and an inert gas, in this case nitrogen. This setup is shown in figure 3-19 and consists of a single-wafer spinner with a modified Teflon chuck which can hold two wafers face-to-face, separated by Teflon shims. This configuration is similar to one reported by Stengl et al. [56]; however, the function of this apparatus is solely to control the ambient during contacting. After being hydrated with a standard RCA clean, the dried wafers are placed in the spinner and the chamber is purged with the desired gas mixture for a period of 5 minutes, while the wafers are spun at 3000 r.p.m. They then sit stationary in the chamber for 5 minutes. Contact is achieved by spinning the chuck at 100 r.p.m. and knocking the Teflon shims away, allowing the top wafer to fall onto the bottom one. The wafers are pressed together to initiate contact, removed, and inspected for the presence of voids using an infrared lamp. They are then subjected to a high temperature anneal for one hour at 1000°C in a nitrogen ambient, to strengthen the bond. Thinning is accomplished using a combination of chemomechanical polishing and electrochemical etching, as previously described.

Experiments were done using a number of N_2:O_2 ratios, to achieve a range of trapped gas pressures, as shown in table 3.2. The residual pressures in this table were calculated by measuring the deflection of each membrane into the cavity after the wafers were bonded and thinned. The deflection value was then used to extract a value for the pressure using equation 3.1 or 3.5. Bonding in a pure oxygen ambient resulted in a cavity pressure of 0.05 atm (5 kPa), which was an upper limit based on the resolution of the deflection measurement. A lower limit for the vacuum of about 10 Pa can be inferred from the fact that the membranes deflected upwards when placed in a etching chamber at that pressure.

Various other pressures were achieved by varying the N_2:O_2 ratio, which was done by changing the relative flow rates of the gases into the chamber. An unusual result was observed when wafers were bonded in a pure nitrogen ambient. After thinning, it was found that the membranes were deflected up, instead of being flat as expected.

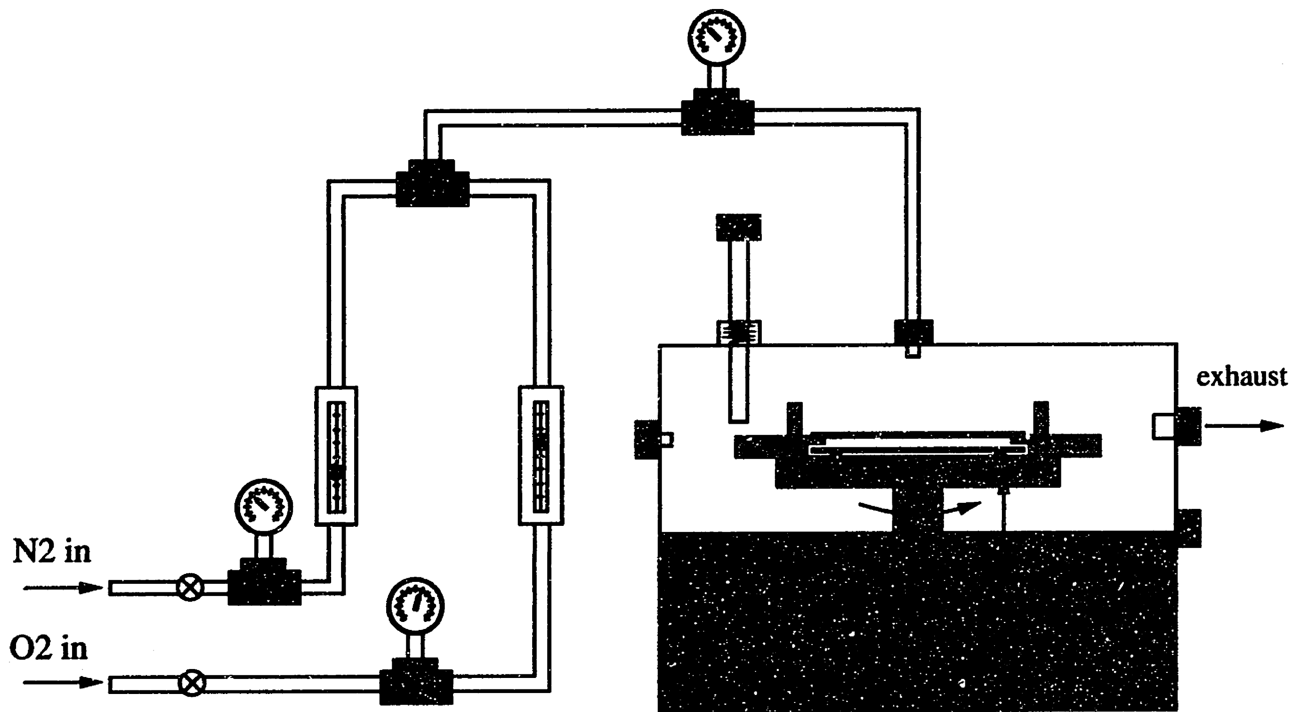


Figure 3-19: Setup for bonding in controlled ambient

Ambient	Residual cavity pressure
$50\%N_2/50\%O_2$ mix	0.56±0.05 atm
$30\%N_2/70\%O_2$ mix	0.38±0.05 atm
$20\%N_2/80\%O_2$ mix	0.17±0.05 atm
100% O_2	0.05±0.05 atm

Table 3.2: Residual cavity pressure for varying bonding ambients

Initially this was attributed to the occurence of some amount of plastic deformation of the silicon during the bonding anneal. In order to check this hypothesis, membranes were punctured by laser-etching a hole in the membrane, of radius approximately 50 μm. Upon forming the hole, the membrane immediately flattened, indicating that there was little or no deformation in the silicon. This appeared to indicate that the upward deflection was due to an overpressure in the cavity. This overpressure occurred both for wafers with both large (1.8 mm) and small (100-500 μm) radius cavities. Upon further examination of the gas pressure in the chamber during bonding, it was found that the chamber pressure was greater than atmospheric pressure, which may have resulted in pressurized gas being trapped in the cavity. To confirm that the result was not due to some problem with the gas lines supplying the bonding chamber, the experiment was repeated using argon as the inert gas, with similar results. We can calculate the overpressure required to cause the measured upward deflection using equations 3.1 or 3.5. For example, a cavity with r=1800 μm had a measured w=30 μm which would require $P_{cav} - P_{atm} \approx 2$ psi. This number is in line with the pressures indicated on the gauges placed in front of the bonding chamber, which showed a chamber pressure of 2-6 psi. The effect of an overpressure of the chamber gas would not show up as dramatically in the cavities with a partial oxygen content due to the fact that the oxygen will react and reduce the trapped gas pressure.

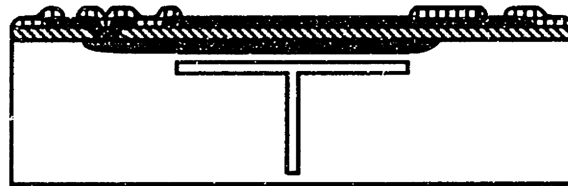
3.5 Formation of top electrode

The final stage of the fabrication is the formation of a top plate for the capacitor. A number of methods were considered, including the use of a polysilicon layer, metal layers deposited on a glass wafer, and plated metal. The first two of these were attempted and are discussed in the following sections. The third alternative, which can include electro- or electroless plating, is an interesting technique for forming relatively thick ($> 25\mu$m) layers of metal. Electroplating is currently being used to fabricate high aspect ratio structures such as micromotors [57]. Electroless plating has the advantage of not needing electrical contact to the base layer, and is can be used to deposit nickel and copper [58]. However, neither plating nor polysilicon can provide the packaging function that the metal-glass alternative can.

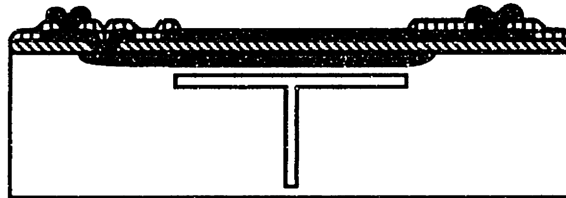
3.5.1 Polysilicon top plate

Initially, the fabrication sequence illustrated in figure 3-20 was to be used to construct a test version of the sensor. The process steps remain the same up to and including the boron doping of the membrane and the deposition of a layer of LTO. The LTO is then patterned to open holes where a subsequently deposited polysilicon layer of thickness 1 μm will be anchored to the silicon. The polysilicon is patterned as shown in figure 3-21, with perforations necessary for wet-etching of the sacrificial oxide to release the electrode. After deposition, annealing and patterning of the polysilicon, a layer of BPSG is deposited as a passivation layer, and patterned to open the membrane areas and contact holes to the polysilicon. During the wet etch to remove the BPSG from these areas, the HF also etches the LTO under the polysilicon through the perforations, thereby releasing the electrode.

A number of problems were encountered when attempting to implement this process, related to the compressive stresses present in thick polysilicon layers. It is known that polysilicon deposited at a temperature of 620-625°C exhibits compressive stresses on the order of 100-500 MPa [59]. These stresses can be relieved by depositing at a lower temperature and doping and annealing the layer. In order to be able to



deposit BPSG and pattern



metallization

backgrind wafer to open pressure inlet hole,
etch under polysilicon to release top electrode

Figure 3-20: Pressure sensor fabrication using polysilicon electrode

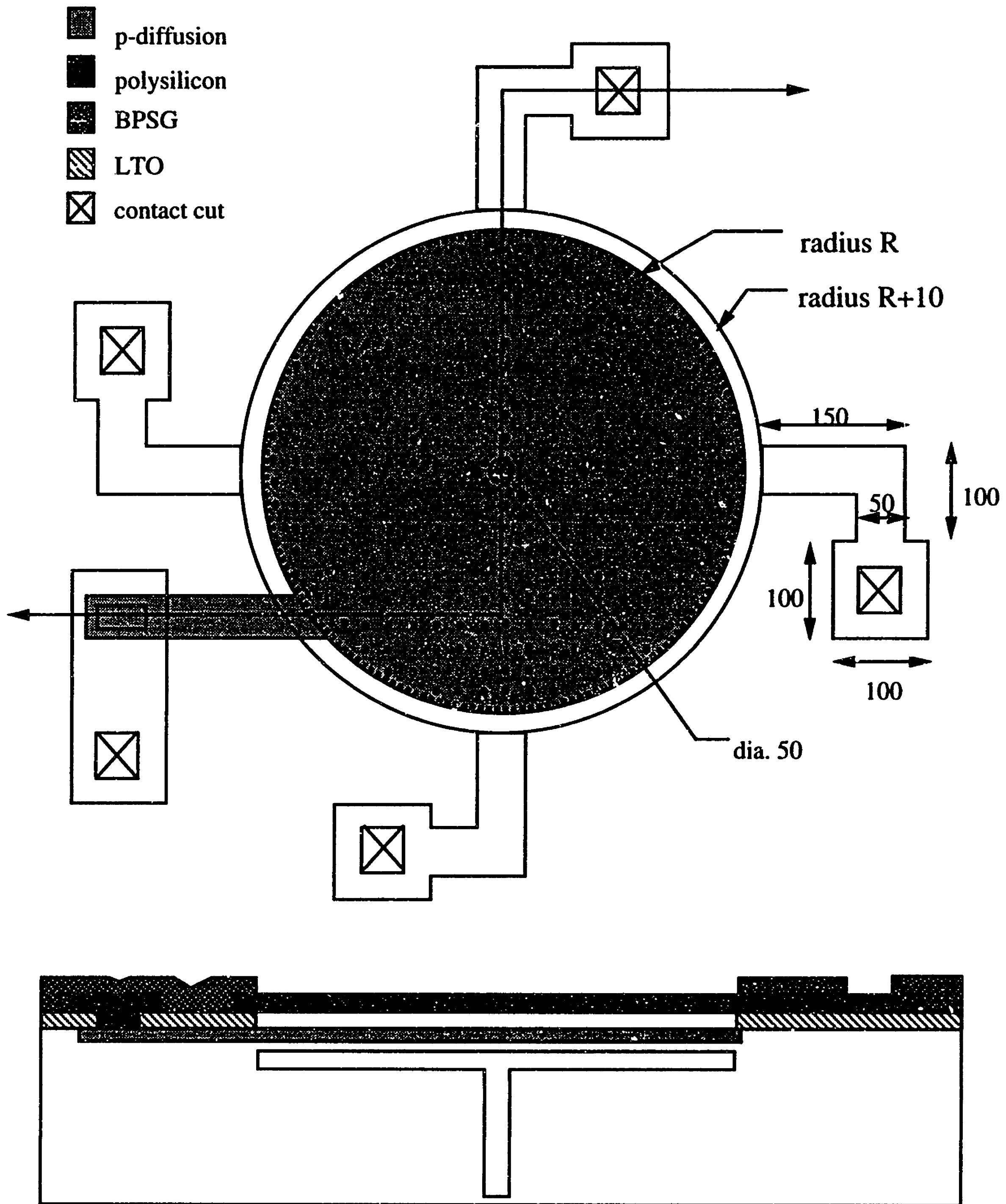


Figure 3-21: Polysilicon top electrode - mask pattern

use existing deposition recipes for polysilicon, an experiment was done to determine whether an anneal was sufficient to reduce stresses in a layer deposited at 625°C. The test structures included clamped bridges, of width 10 μm and lengths 20, 40, 60, 80 and 100 μm, as well as circular plates of radius 100-350 μm, with square perforations spaced at 25 μm intervals, and of size 3, 4 and 5 μm on a side. Structures were formed by depositing 1 μm of LTO, followed by 1 μm of undoped polysilicon. The poly was doped using a liquid $POCl_3$ source at 950°C and annealed at 1000°C for 1 hour. After patterning of the polysilicon, the wafer was immersed in 49%HF for 15 minutes to underetch the LTO. Upon observing the resulting structures under the SEM, two things were noticed. First, some of the bridges were buckled upwards, indicating that a compressive stress was present in the layer (figure 3-22). Second, the majority of the circular plates were stuck down to the substrate. This is attributed to the capillary action of the water present between the substrate and the poly layer as the wafer dries [60]. In order to alleviate this problem, an alternative rinsing scheme was used. After the HF etch was completed, the HF was diluted with DI water and rinsed. Without allowing the wafers to dry, the DI was diluted and replaced with methanol, after which the wafers were removed from the methanol and allowed to air dry for 24 hours. This resulted in some of the smaller plates being free of the substrate, but not the larger ones. The larger plates remained attached to the substrate, even when a probe tip was inserted underneath to try to release the structure.

Many of these problems can be avoided by depositing the polysilicon at a lower temperature. It has been found that polysilicon deposited at temperatures below 590°C is amorphous in nature, and in the range of 590-650°C is polycrystalline with varying stress levels [59]. It is possible to obtain stress-free or slightly tensile layers by depositing at temperatures below 600°C, however this requires careful characterization of the deposition conditions.

Due to these problems with polysilicon, as well as the fact that the high temperature anneal required to obtain suitably low-stress layers is not compatible with a standard CMOS process, an alternative approach of using a metal-glass electrode was considered and is described in the next section.

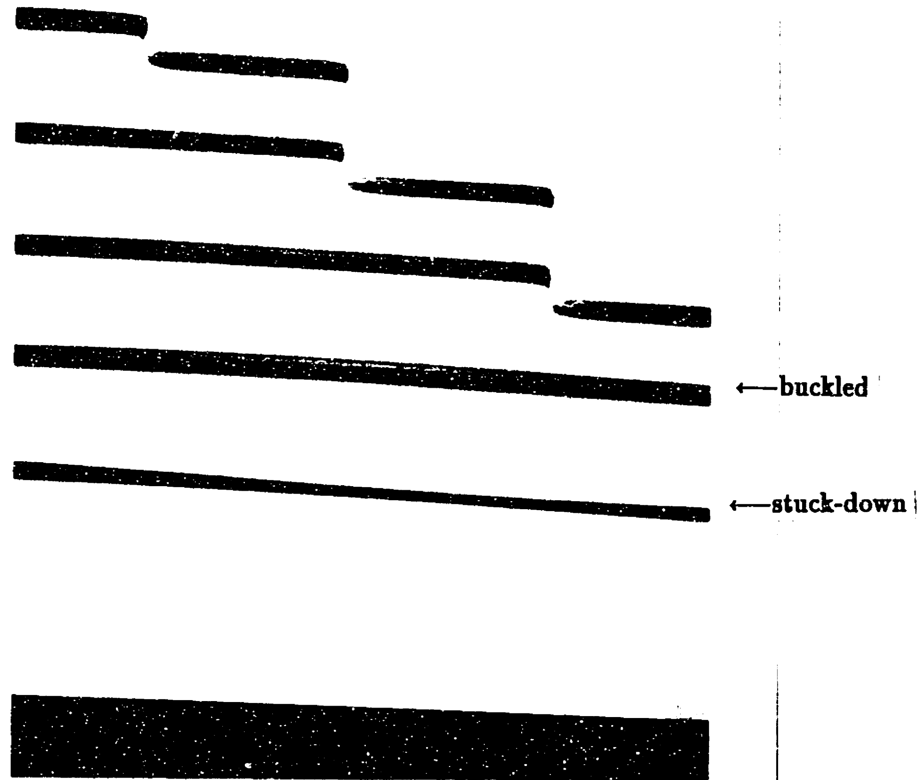


Figure 3-22: SEM of polysilicon bridges after stress-relief anneal

3.5.2 Metal bonding

In the final structure, the top electrode of the capacitor is composed of a metal layer deposited on a glass wafer, which is then bonded to a corresponding layer of metal on the silicon substrate. Electrical contact to the top plate is made through the metal which is bonded to lines connected to contact pads on the substrate.

It was decided that the metal-to-metal joint would be either a eutectic or a thermocompression bond. The main requirements for the process are that it can be accomplished at a bonding temperature no higher than 400°C, and that the metals be compatible with standard IC processes. Some possible metal combinations are the Al-Zn system and the Al-Ti system. Of the two, zinc poses a problem in that Zn deposition is not readily available in the facilities being used. The Al-Ti combination causes no problems in processing, as it is already being used in standard CMOS metallization, where titanium is often used as a barrier layer, as well as for silicides.

The aluminum and titanium layers were deposited using electron-beam evaporation. In attempting to implement a metal-to-metal bond, it was found that the presence of the native oxide on the surfaces of these metals inhibited bond formation when only heat and static loading were used. Since Al_2O_3 and Ti_2O_3 are both very stable oxides, neither will consume the other, so no contact was obtained while attempting to achieve a bond with any of the three combinations of Al and Ti coated wafers. Mechanical scrubbing action was also used to attempt to break through the native oxide layer, but due to the relatively large bonding area, was also not successful. Gold was therefore selected as an alternative metal, mainly because it does not form a native oxide.

For die bonding and packaging applications, gold is used in combination with either tin or indium, usually as a solder or preform. These systems are advantageous because they have relatively low eutectic temperatures and can be used to form die bonds that will withstand high temperatures. The alloys are usually formed through solid-liquid interdiffusion at the interface, followed by solidification upon cooling [61]. Therefore, for this application, initially, a gold-tin eutectic bond was attempted. The melting point of Sn is 230°C and the Au-Sn eutectic temperature is 280°C (at 20%

Sn), both well below the desired temperature limit of 400°C. However, because the bonding was done in air, a similar problem of oxide formation on the Sn layer inhibited bond formation. The lack of bond formation may also be related to the fact that the metal layers were much thinner than is normally used for die bonding. Thus there may have been insufficient material available to properly flow and start the interdiffusion process.

Next, a direct gold-gold bond was attempted. Au-Au bonding is most commonly used in wire-bonding, and often involves ultrasonic or scrubbing action to assist in the formation of an initial contact area between the two films[62]. Ball bonding usually consists of melting the tip of the wire to be bonded to form a ball, which is then pressed against a bond pad while ultrasonic vibration is applied to break through any surface films. Bonded areas are on the order of 0.5mm^2.

For our particular application, the bonded areas are larger, and the films are much thinner. Another difference is that since the two surfaces to be joined must be aligned, no scrubbing action can be used. The bond must be achieved solely by heat and static loading, using thermocompression. Additionally, since the capacitor gap spacing is determined in part by the metal thickness, for a small gap thin (<5000Å) layers must be used. The gold film was deposited over a layer of chromium, used to improve adhesion to the underlying substrate, as well as act as a barrier layer. The bilayer consisted of 200Å of chromium, followed by 3000Å of gold, deposited using electron-beam evaporation.

A number of studies have been done to assess bond strength of gold-gold thermocompression bonds, most involving the use of either a wirebond type of bond[63], or a large area thick film bond such as is used for die attachment to alumina substrates. Many of these tests involve somewhat elaborate test equipment generally applying a tensile load to the wire until failure.

Because such equipment was not immediately available, the bond strength was estimated using a simple shear test. Figure 3-23 gives a schematic of the sample used, which consists of a lap joint between the layers to be bonded. Initial testing involved the use of unpatterned metallized silicon wafers, cleaved into 1cm pieces and

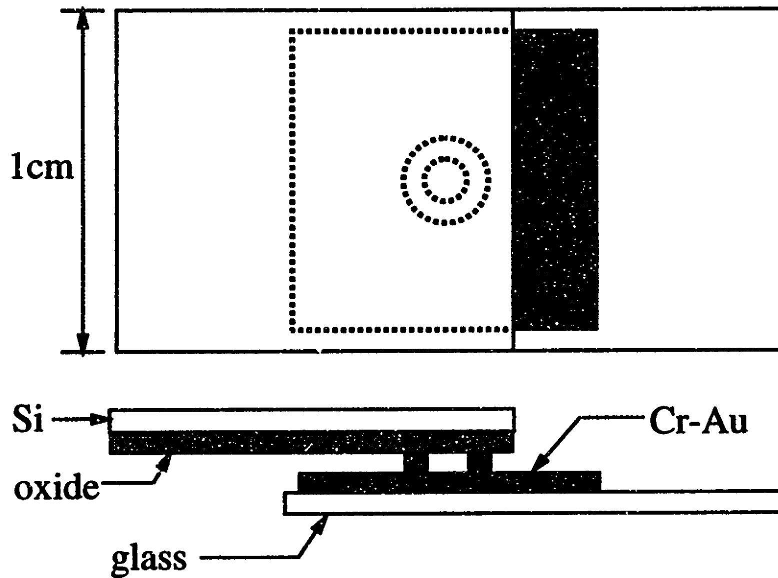


Figure 3-23: Metal bond strength test sample

bonded using a hot plate and metal weights.

Samples consisted of silicon wafers with 3000Å of LTO metallized with Cr-Au, which was patterned into the ring shape using liftoff. The glass wafer was also metallized with an identical Cr-Au layer. Both glass and silicon were cut into 1cm strips with a diesaw, after which bonding was done piece by piece.

The bonding procedure consists of cleaning the samples, placing them on a hot plate heated to 350°C, and applying a static load of about 20psi by pressing with tweezers for a period of 1-2 minutes. Cleaning is done by placing the samples in an ultraviolet ozone cleaner for 1 hour, to desorb any organic contaminants that may be present on the surface of the gold that could inhibit contact. It was found that successful bonding could only be achieved when this cleaning step was performed immediately prior to bonding.

Testing is done by mounting each sample in an Instron tensile test machine, as shown in figure 3-24. This loads the bond in shear. Testing conditions were as follows:

- load cell: 20lb
- pull rate: 0.02"/min
- temperature: 25°C

Bonded area (μm^2)	Load to fail (lb)	Load to fail (psi)	Comment
804248	11.13	8964	-
94641	1.13	7733	-
402124	2.92	4703	Si fractured
94248	5.89	40477	Si fractured
408408	9.32	14781	Si fractured

Table 3.3: Results of shear testing of Au-Au bond

Results of the tensile tests are given in table 3.3. These numbers are comparable to those obtained from standardized shear-tests of gold ball bonds (750-12000psi) [64].

The samples were examined under a microscope and SEM after testing to determine the failure interface. It was found that in most cases the failure occurred at the Au-Au interface, but in some regions it appeared that some of the silicon was actually removed from the substrate and attached to the glass. SEM pictures indicate a trench in the debonded area on the silicon piece and a corresponding hill of material on the matching glass piece (figure 3-25). This mode of fracture may be due to the diffusion of the gold through the relatively thin chromium barrier layer into the silicon. The diffusivity of gold in silicon is very high, so that if the Cr barrier is bypassed, then the gold can rapidly migrate through the silicon and possibly form a eutectic with the silicon (Au-Si eutectic temp.=363°C). Alloys of silicon and gold have been shown to be more brittle than plain gold, especially with a high silicon content, as would be present in this case. The increased brittleness may result in failure at the eutectic-silicon interface; however, to determine the exact cause of failure a much more detailed analysis of the material at the interface is necessary.

Additional tests were done using metallized dice with the pattern to be used for the sensor. Total bonded area for each sample was approximately 6.5mm^2. Since the samples consisted of 1cm^2 dice, the bonded pair was sandwiched between additional strips of silicon using epoxy, in order to be able to test the bond using the existing grips for the Instron. The bond strength of the epoxy was much larger than that

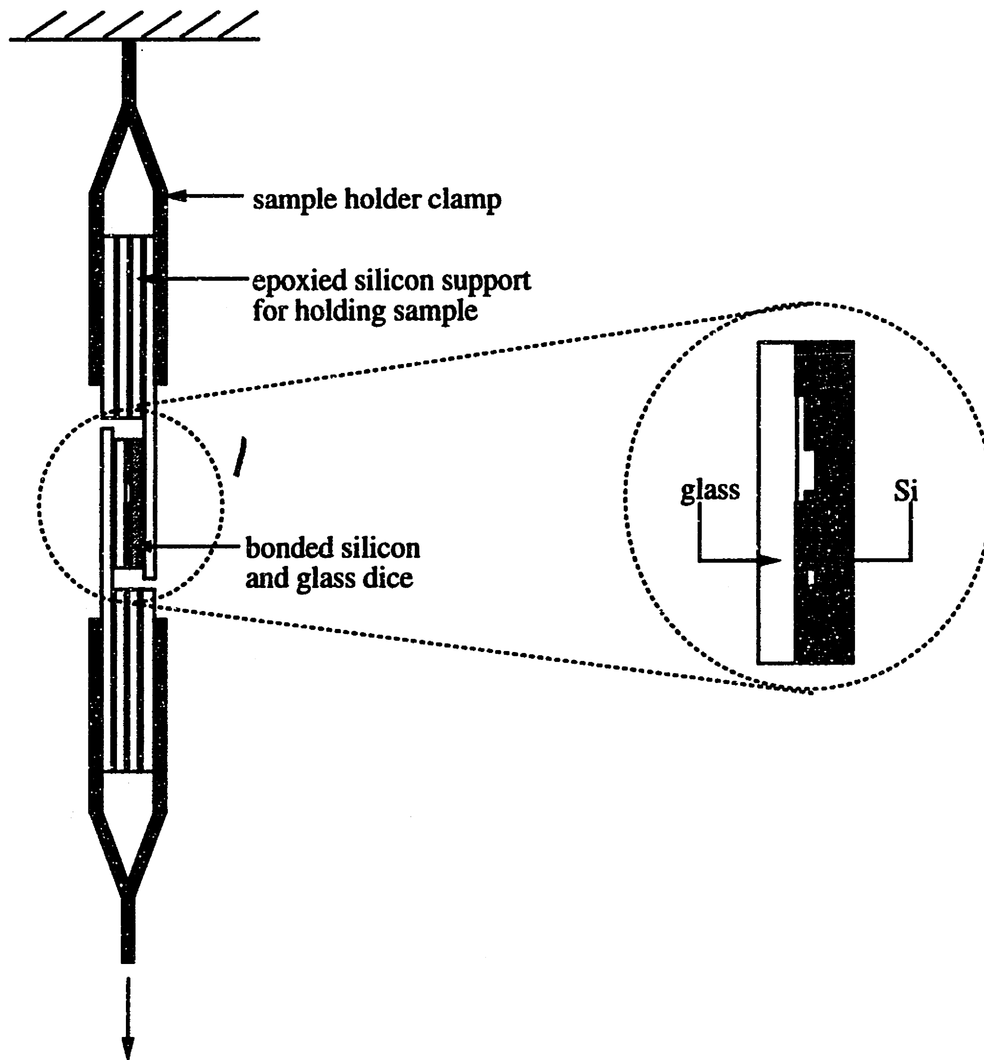
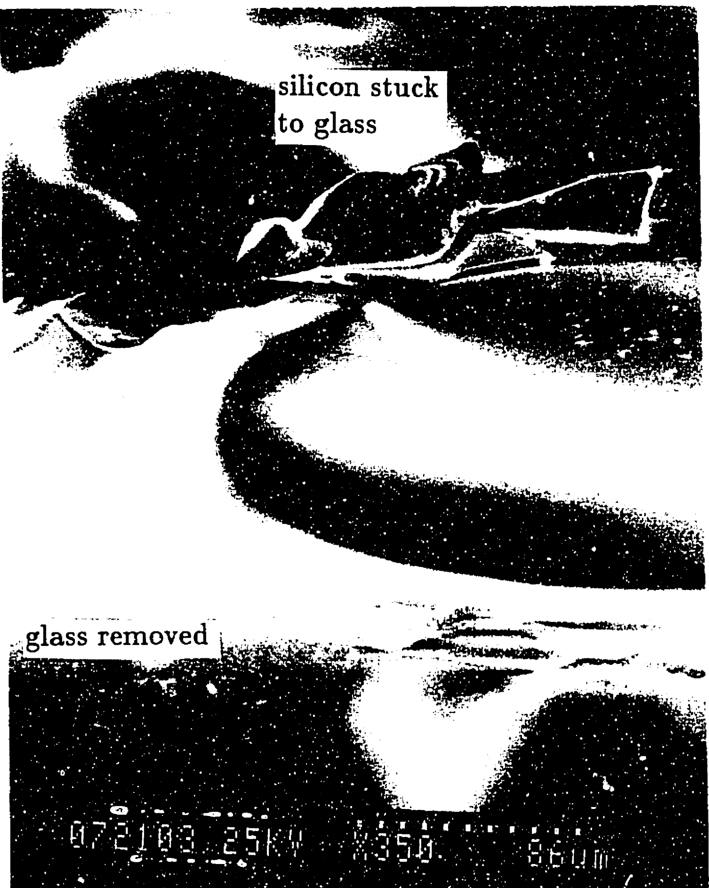


Figure 3-24: Metal bond shear testing setup



Glass surface

Silicon surface

Figure 3-25: SEM of metal bond interfaces after bond strength test

measured for the metal bond using the first set of samples, so that the epoxy joint was not expected to fail before the metal bond did.

Failure loads were comparable to those obtained in the first set of tests, and again, it appeared that some of the silicon was removed from the substrate and attached to the glass die.

3.5.3 Final device fabrication

The final steps in fabricating the pressure sensor consist of first metallizing both the silicon and glass substrates as described previously, sawing the substrates into dice, opening the backside pressure inlet port, and metal bonding. Since the laser etching to open the inlet port is done after the gold has been deposited on the wafers, the dice must be coated with photoresist to protect the gold surface from exposure to the chlorine during etching. At the elevated temperatures used for laser etching ($>150^{\circ}$C) the formation of gold chloride ($AuCl_3$) can occur and consume the gold, leaving a thin film coating on the surface. This can inhibit the metal bonding, as well as degrade the conductivity of the leads. In order to avoid this, a 5 μm thick layer of high viscosity photoresist (AZ4620) was spun onto the die before laser-etching. The thick resist layer was used because the initial hole from the topside of the wafer was not formed to a depth of 400 μm as desired, but was much shallower (see figure 3-26), so that the final release laser etching step took considerably longer than expected.

After the etching of the inlet ports, the resist was removed by ashing in an oxygen plasma for a period of about 30 minutes. The deflection of the membranes before and after the release was measured using a Topo-3D optical surface profilometer[51]. The surface profiles given in figures 3-27 and 3-28 indicate that the membrane is flat after the etch, thus confirming that it was indeed released.

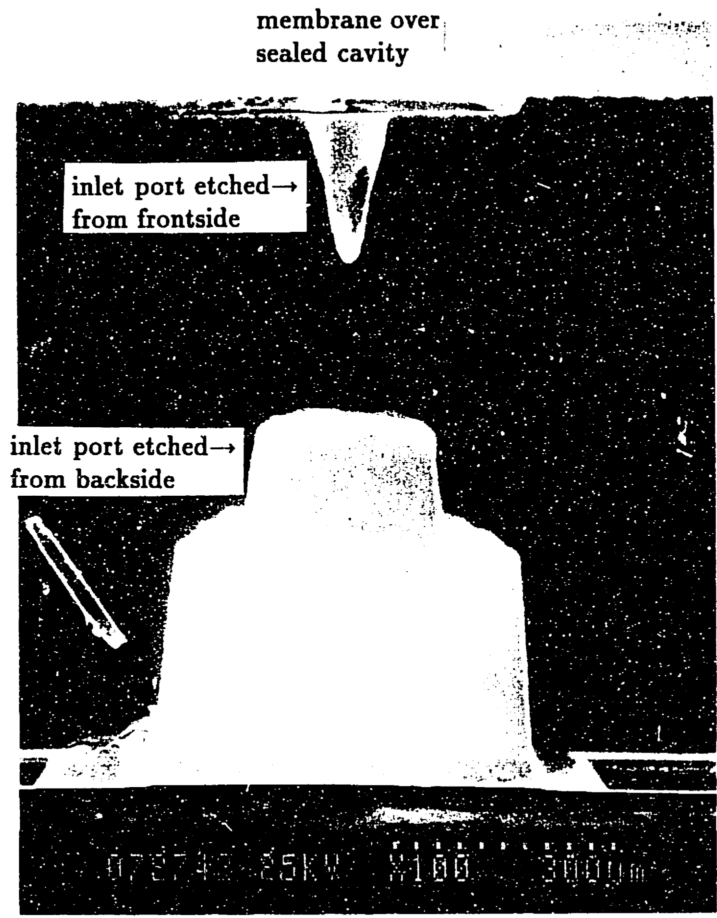


Figure 3-26: Cross-sectional SEM of partially etched presure inlet port

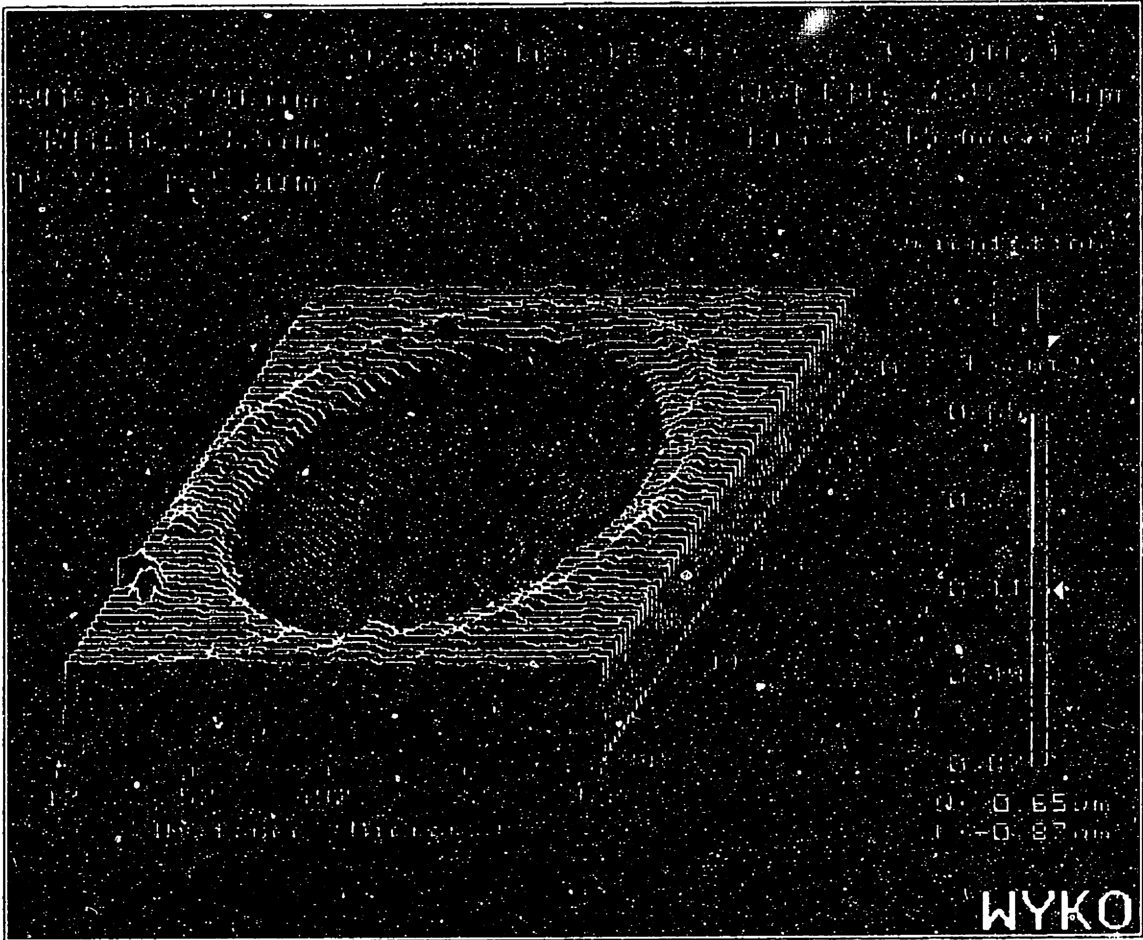


Figure 3-27: Surface profile of membrane before laser etching of pressure inlet port. Radius=350 μm

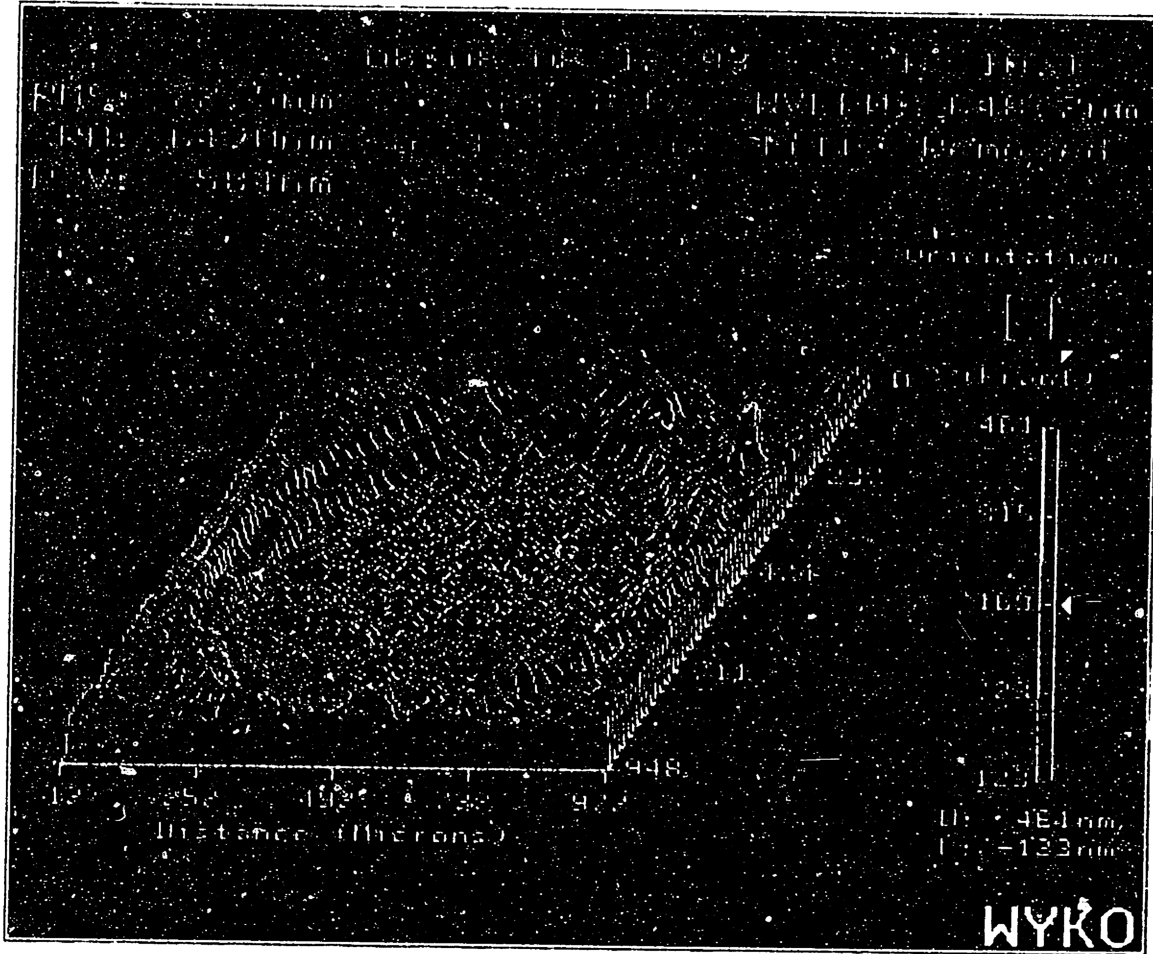


Figure 3-28: Surface profile of membrane after laser etching of pressure inlet port. Radius $\sim$350 μm

Chapter 4

Testing

The testing can be divided into two main areas. The first involved load-deflection measurements of relatively large silicon membranes, which were performed in order to obtain values for the biaxial modulus and residual stress in the bonded layer. The second set of tests was concerned with the behaviour of the capacitive sensors, the fabrication of which was previously described.

4.1 Load-deflection testing of silicon membranes

In order to obtain mechanical property information about the bonded and etched back silicon layer, load vs. deflection testing was done on membranes formed using the sealed cavity process described previously. The membranes had the following dimensions: radius=1800 μm, thickness=10 μm, cavity depth=50 μm. For modelling purposes, the membrane was considered to have a clamped edge, and its deflection behaviour was assumed to be in the large deflection regime. Under such assumptions, the pressure-deflection relationship has been experimentally found to be:

$$P = \frac{C_1 t \sigma_o}{a^2} d + \frac{C_2 t f(\nu)}{a^4} \frac{E}{1-\nu} d^3 \qquad (4.1)$$

where P is the applied uniform pressure, d is the deflection at the center of the membrane, a is the radius, t is the thickness, and C_1, C_2, and $f(\nu)$ are experimen-

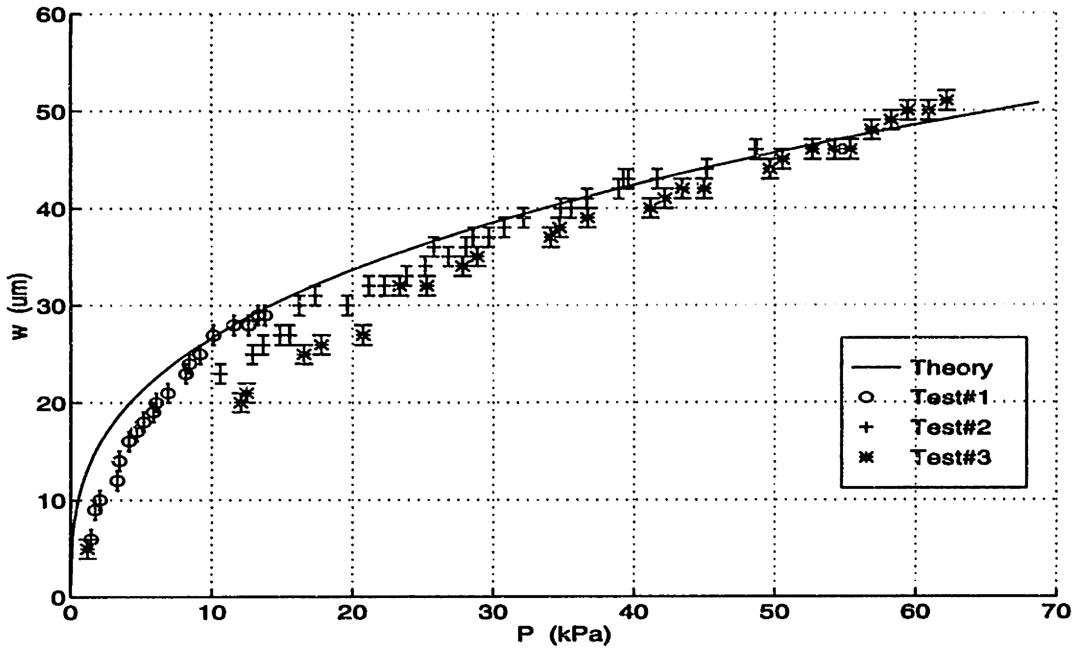


Figure 4-1: Measured load-deflection data. Radius=1800 μm, thickness=10 μm

Test	b_0 $\left[\frac{Pa}{\mu m}\right]$	b_1 $\left[\frac{Pa}{\mu m^3}\right]$	$\frac{E}{1-\nu}[GPa]$	$\sigma_o[MPa]$
1	182.8	0.3	129.44	14.80
2	288.4	0.4	173.33	23.36
3	507.9	0.3	130.33	41.13

Table 4.1: Fitted parameters and material properties from load-deflection tests

tally determined values specific to the membrane shape [65]. If a set of pressure vs. deflection data is fitted using least-squares to the following form:

$$P = b_0 d + b_1 d^3 \tag{4.2}$$

then, using the fitted values for b_0 and b_1, values for the biaxial modulus $\frac{E}{1-\nu}$ and the residual stress σ_o present in the membrane can be extracted[65].

Figure 4-1 shows the measured pressure vs. deflection data for three identical membranes with the dimensions given above. Least-squares analysis is done to fit the data to equation 4.2 and the resulting curves are given in figure 4-2. Table 4.1 contains the values of the fitting parameters, and the extracted material properties.

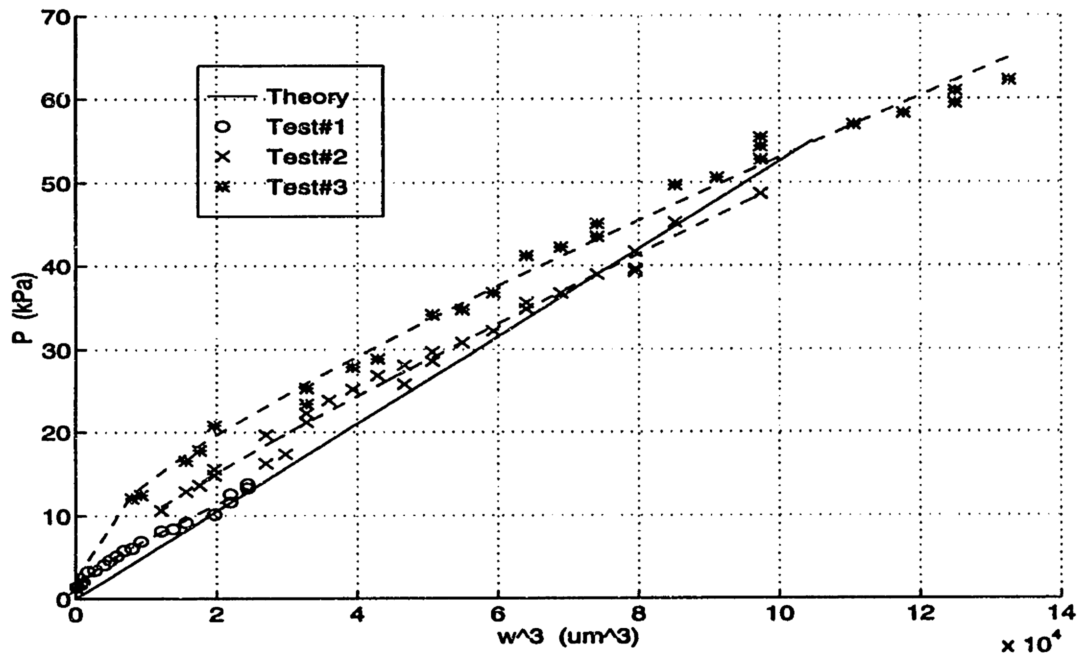


Figure 4-2: Fitted load-deflection curves. Radius=1800 μm, thickness=10 μm

A value of $\nu = 0.25$ was assumed to calculate the biaxial modulus, which resulted in an average Young's modulus value of $E = 108.3$ GPa. This is somewhat lower than the values found in the literature (120-190 GPa). The average residual stress was found to be 26 MPa in tension. The membrane was inferred to be in tension because the deflections were consistently lower than the calculated values assuming no residual stresses. The relatively low stress values justify the assumptions made in section 3.4, about neglecting the stress in the membrane when calculating its behaviour at elevated temperatures. Assuming uncertainties of $a \pm 5\mu$m, $t \pm 0.2\mu$m, $d \pm 1\mu$m and $P \pm 0.02$psi, the errors in the biaxial modulus and residual stress are approximately 11% and 5% respectively.

4.2 Capacitive pressure sensor testing

4.2.1 Test setup

The test setup used for capacitance-voltage measurements is illustrated in figure 4-3, along with the completed sensor in cross section. Capacitance measurements were

done using an HP4280 capacitance meter, in which a 30mV test signal at 1MHz is applied to the device under test, with a capacitance resolution of 1fF. The glass-silicon die was placed directly on the probe station, and electrical contact to the backside was made through the chuck, by means of the heavily doped backside surface of the silicon die.

For obtaining capacitance-pressure measurements, the load-deflection setup described in [65] was used. The glass-silicon die was mounted with epoxy onto a piece of plexiglass with a through-hole to provide a pressure port. Probes were used to contact to the bond pads on the die edges, and these were connected to the HP4280 with shielded coaxial cables, as for the C-V tests.

4.2.2 Diode characteristics

To verify that contact was being made to the backside of the die, the characteristics of the diode formed between the p+ portion of the membrane and the remaining n-type membrane + substrate were measured using an HP4145 semiconductor parameter analyser, both before and after the glass substrate was bonded on. Figure 4-4 is an example of the I-V characteristic, which was unchanged after the metal bonding step. The turn on voltage was approximately 0.5V and the breakdown voltage was about -40V. The diode curve was verified for each device prior to subsequent testing, as a check for the integrity of the connections to the die.

4.2.3 Static capacitance

Initial testing consisted of obtaining static capacitance measurements of each sensor before the final laser etching step to open the pressure inlet port. Measurements were done using the HP4280 in C-G mode, with zero bias applied across the plates.

First the capacitance was measured between the bond pads leading to the top and bottom plates, using a silicon die without the glass capping die. (fig. 4-5a). The substrate was connected to the heavily boron-doped bottom plate of the capacitor through the chuck contact to the backside of the die. Table 4.2 shows the measured

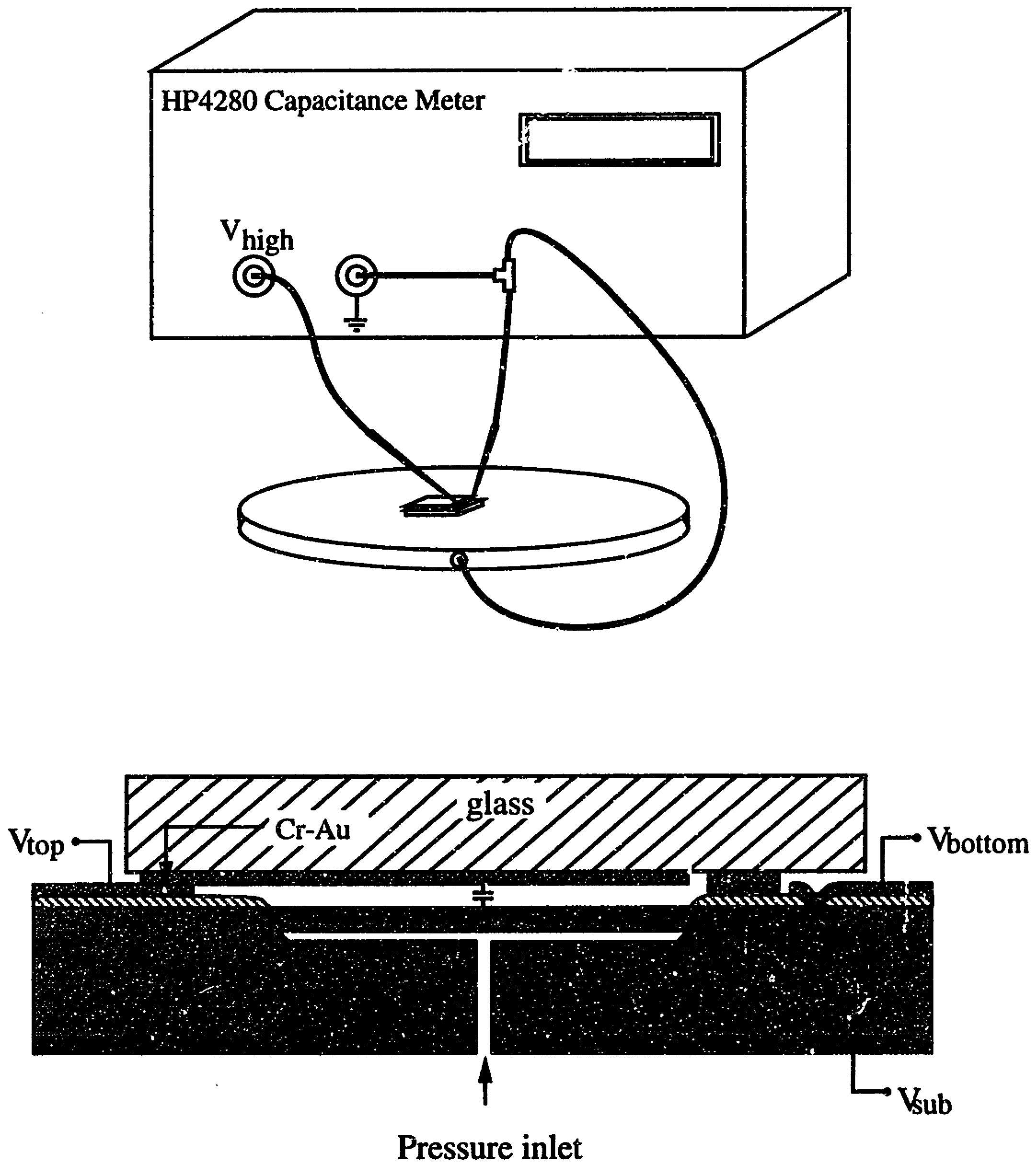


Figure 4-3: Test setup for capacitance measurements

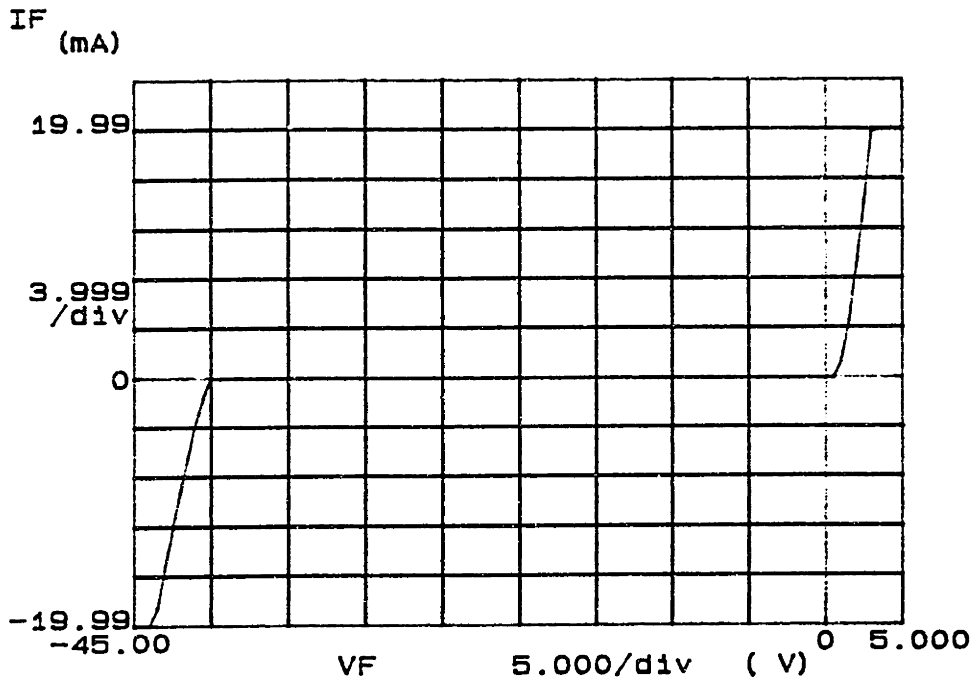


Figure 4-4: I-V characteristic for diode formed from p+membrane and n-substrate

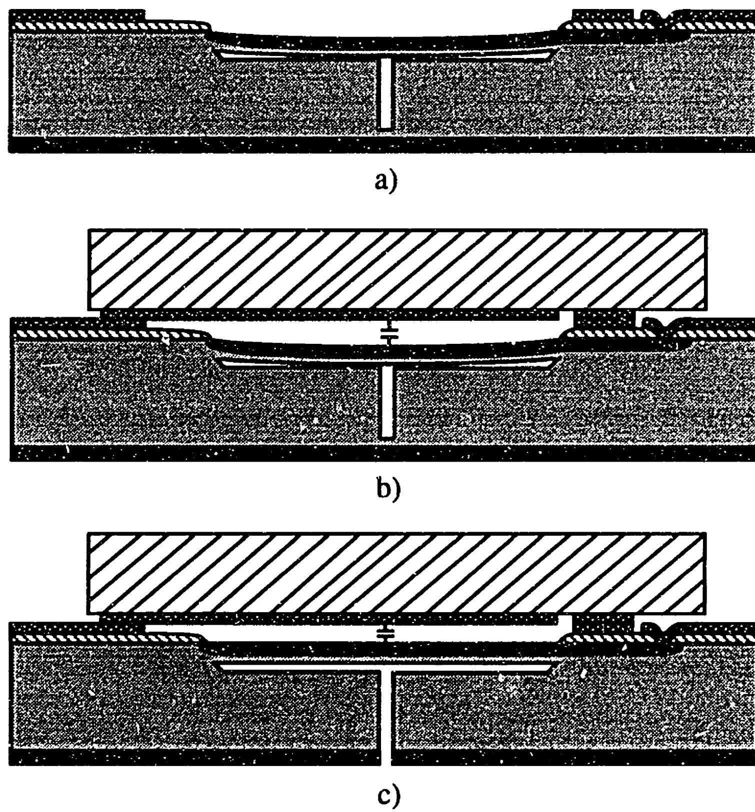


Figure 4-5: Devices tested: a) uncapped device, b) capped and unvented device, c) completed device (capped and vented)

Sensor	Radius (μm)	Capacitance (pF)
1	350	0.756
2	240	0.560
3	200	0.936
4	130	0.888
5	110	0.601
6	100	0.995
7	100	2.365
8	110	1.505
9	130	3.580
10	200	2.845
11	240	1.740
12	350	0.759
13	350	6.071
14	240	4.945
15	200	3.755
16	130	2.530
17	110	1.554
18	100	0.652
19	100	5.375
20	110	4.320
21	130	3.495
22	200	3.163
23	240	1.937
24	350	0.896

Table 4.2: Parasitic capacitance for each sensor on a die, measured at zero bias

parasitic capacitances. Refer to the mask set for the location of each sensor on the die. Basically, the values in this table give an indication of the magnitude of the parasitic capacitance from the field regions; thus the higher values correspond to those sensors that are located the farthest from the die edges where the bond pads are.

4.2.4 Capacitance-voltage testing

Recalling section 2.3, which relates the voltage applied across the plates to a simulated pressure, an attempt was made to electrostatically deflect the bottom plate and cause a capacitance change. This was done for the largest two sensors (radius=350 and 240

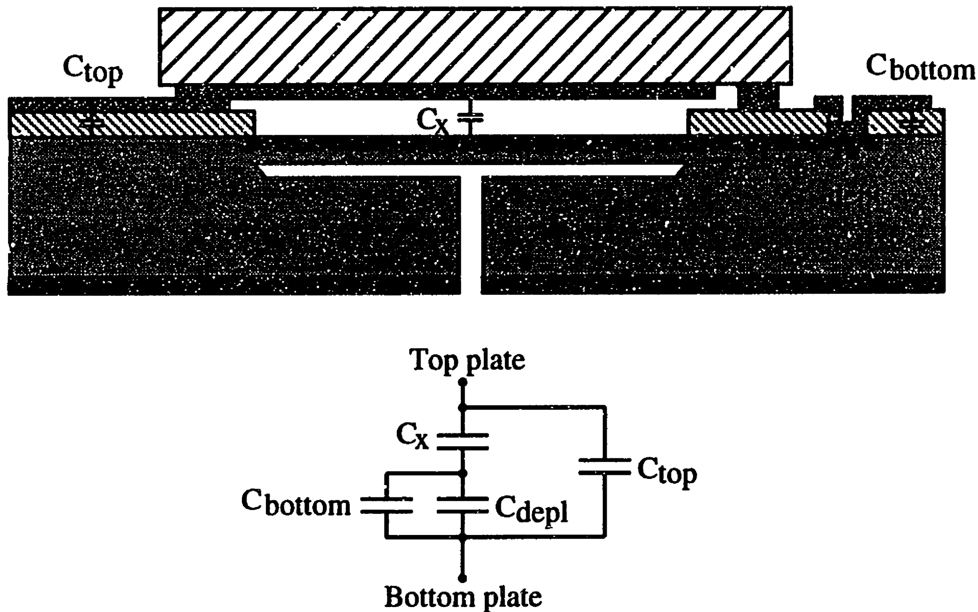


Figure 4-6: Model for equivalent capacitance across bondpads

μm), as they required the lowest voltages for a given change in capacitance.

Figure 4-6 illustrates the various capacitors that are present between the bond pads for the top and bottom plates. The variable of interest is C_x, the sensor. The capacitance contribution of the metal lines over the LTO can be treated as a MOS capacitor, using the appropriate area of each line over the oxide, taken from the mask set. C_{top} and C_{bottom} represent the metal-oxide capacitance from the tracks leading to the top and bottom plate bonding pads respectively. If the p+ membrane and the n-substrate are connected together, then the depletion capacitance of the pn junction, C_{depl}, and C_{bottom} are shorted out and can be neglected. If the parallel capacitance of C_x and C_{top} is calculated and plotted as a function of the applied voltage between the plates, the curve in figure 4-7 is obtained.

It is apparent from this graph that the capacitance of the field regions dominates the total for much of the lower voltage range. This is shown to be the case when measuring the capacitance as the voltage is slowly varied across a large range, as shown in figures 4-8 and 4-9, which were taken from unvented and vented devices

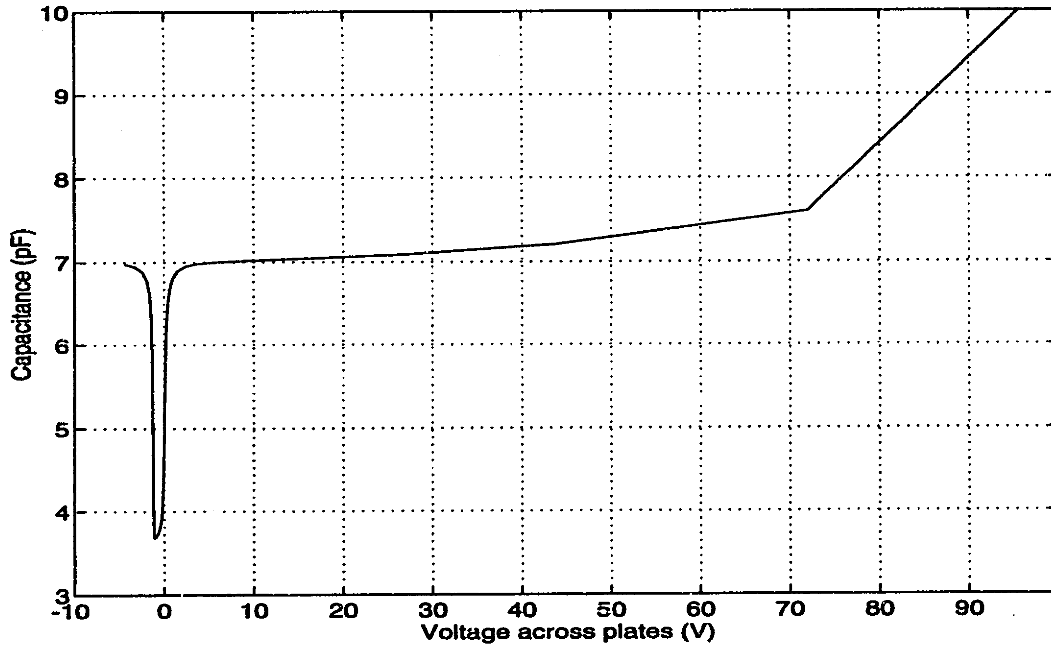
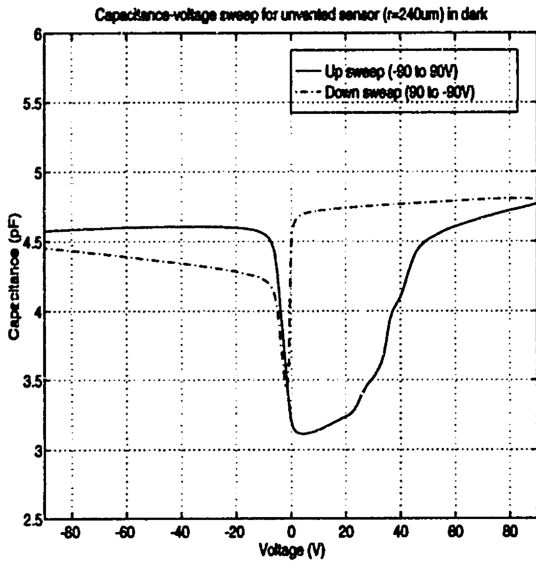
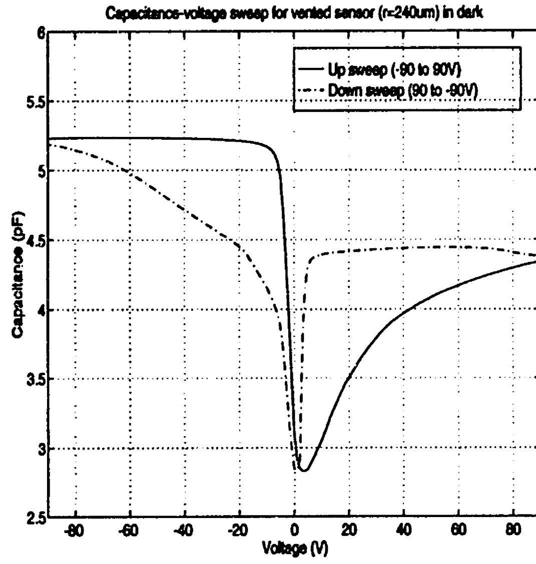


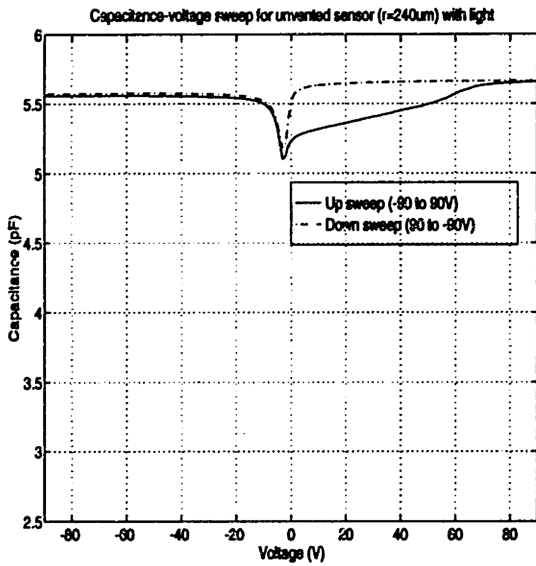
Figure 4-7: Calculated capacitance as a function of voltage across plates for device in figure 4-5b. r=350 μm, air gap=1 μm.

(fig. 4-5b and c). The measurements were obtained by stepping the voltage across the plates at 0.5V/s from -90 to +90V, holding at +90V for 10 seconds, and stepping back down to -90V at the same rate. The rate is slow to ensure a low frequency measurement.

A number of observations can be made from these measurements. First, there does not appear to be any significant increase in the capacitance at high voltages, especially for the largest device, and the expected sharp increase due to pull-in is not evident. Second, there is not much difference between measurements for the vented and unvented structures, whereas one would expect the vented structure capacitance to be at least 1pF higher due to the fact that the gap is smaller from the flattened out membrane. Third, the measurements done with the devices illuminated appear to have much sharper transitions from accumulation to inversion and vice-versa, which may be expected from the light-induced generation of more carriers.







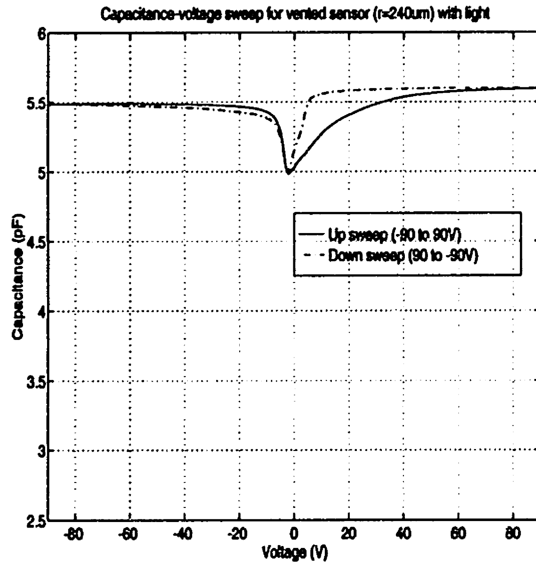
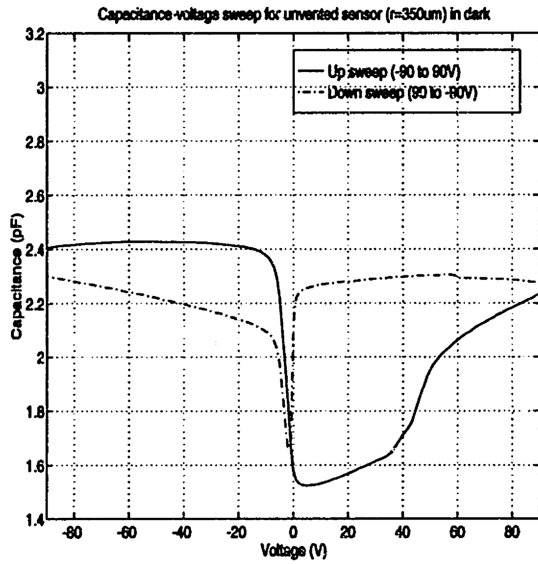
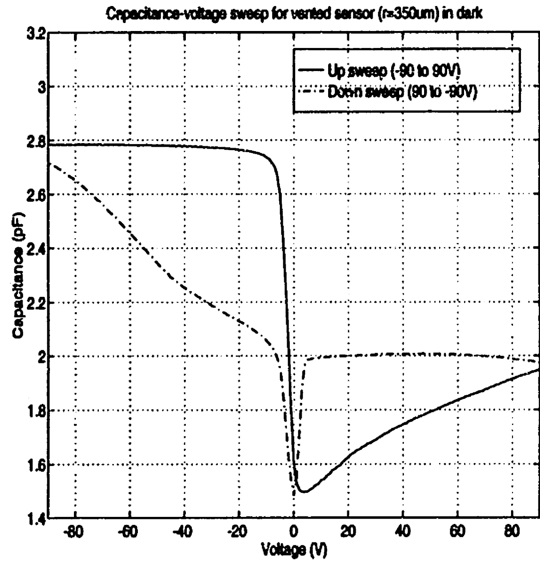
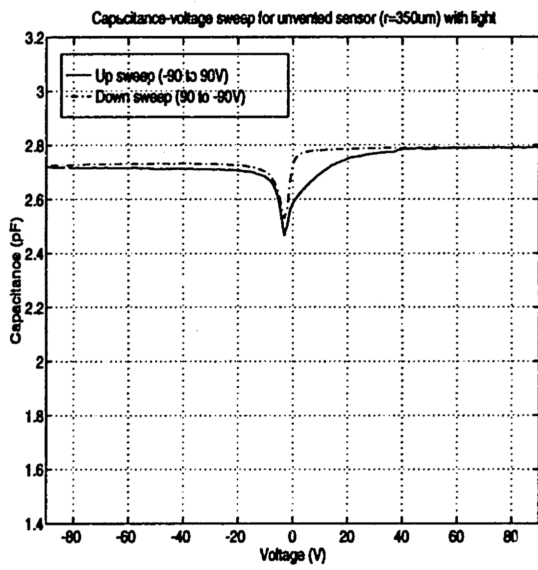


Figure 4-8: Capacitance-voltage measurements for devices with r=240 μm







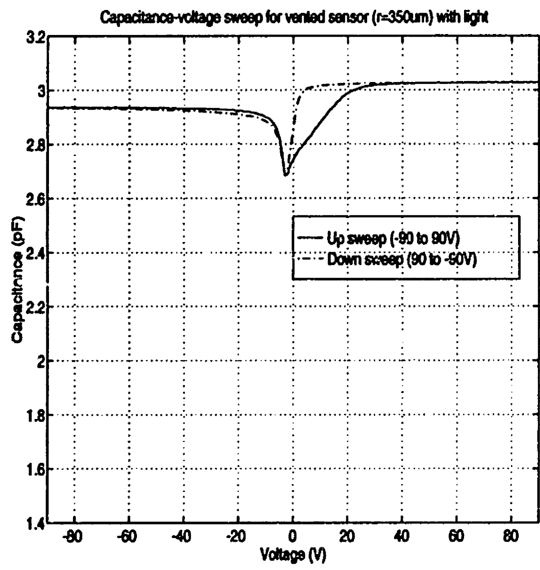


Figure 4-9: Capacitance-voltage measurements for devices with r=350 μm

Due to the distance of the bond pads from the sensor, C_x is swamped out by C_{top} so that the C-V curve resembles a MOS capacitor, with a threshold voltage of about -3V. Varying the light level on the sample shifted the whole curve up or down slightly, but did not appear to affect the threshold voltage. It did however cause the transitions to be faster, as previously mentioned.

The pull-in voltage required to touch the two plates together was simulated using the MEMCAD system [42]. For a sensor with radius=350 μm, membrane thickness=10 μm, and air gap=1 μm, the simulated pull-in voltage was about 55V, assuming the membrane was unloaded to begin with, as for a vented structure. This pull-in was not observed in the measured devices, and is presumed to be caused by poor electical contact at the Au-Au bond interface, as is discussed in the next section. For the unvented membranes, there was a built-in load of 0.8atm$\approx$10psi pushing them away from the top plate. If this is taken into account in the simulation, then the pull-in voltage increases to 125-130V. Since this is close to the breakdown voltage of the LTO dielectric being used, it does not appear to be feasible to use electrostatic pull-in to fully deflect the membranes, especially the smaller ones where the voltage requirement will only get higher. Also, the capacitance change will be much smaller than that already present due to parasitics, and will tend to be swamped out.

4.2.5 Capacitance-pressure measurements

As previously stated, for the capacitance-pressure tests, the bonded glass-silicon die was epoxied onto a plexiglass piece with an inlet hole, and the load-deflection setup was used to apply a pressure to the sensor. The HP4280 was again used for capacitance measurements.

Before the glass was bonded on, the membranes were pressurized and examined under the microscope to ensure that the inlet ports were not blocked. Upon testing the completed device, no significant variation in the capacitance was observed as the pressure was increased from 0 to 10psi, on the largest sensor (r=350 μm), when ideally, we would expect a change of at least a few picofarads. It is thought that the problem was in the contact between the metal on the glass and that leading to

the bond pad on the silicon, such that there was no electrical connection to the top electrode. This would cause the measured values to be just that of the parasitic lead-oxide-substrate capacitor. This also appears to explain the lack of change with a voltage sweep as shown by the similarity of the C-V curves for vented and unvented devices in figures 4-8 and 4-9, since simulations indicate that pull-in should occur at 55V for the vented structure, resulting in a sharp change in C at that point. This failure to obtain contact may be due to the presence of a thin residue on the gold surface of the photoresist used during the laser etching, or may be caused by nonuniformities in the surface which result in that area of the metallization being slightly lower than the surrounding areas. The problem may be eliminated by using an alternative method to release the pressure inlet ports, such as a wet chemical etch, or an alternative dry etching technique that will not affect the existing metallization present on the substrate.

Chapter 5

Conclusions

One of the main achievements shown in this work was the development of a sealed-cavity process, in which a sensor base structure was able to undergo standard IC process steps without damage. This provides a great advantage when moving towards a higher level of sensor-circuit integration.

Three key fabrication issues central to the success of this sealed-cavity process were investigated. First, it was shown that electrochemical etching of silicon can be used to form silicon layers of well-controlled thickness, and progress was made towards characterizing the conditions required to solve the particular problem of premature passivation in the p-type silicon. Second, by controlling the ambient gas in which the wafer bonding was done, it was possible to eliminate the plastic deformation of membranes over sealed cavities, which in turn allows the wafers to be subjected to high temperature IC process steps. The last area investigated was that of using metal thermocompression bonding to create a top electrode for capacitive sensing. The technique was relatively simple to implement, and bond strength tests showed promising results, however, it would be advantageous to find metals other than gold, that are more compatible with circuit processing.

A capacitive pressure sensor was the vehicle used to demonstrate the process. Full functionality of the sensors was not demonstrated due to difficulties with the final process steps, in particular the laser release and its effect on the metal surfaces. However, it is believed that these problems can be solved with non-critical process

modifications that eliminate the use of laser etching to open the pressure inlet port, for example by using a wet anisotropic etch to remove the bulk of the silicon and reach an etchstop layer formed in the cavity. Also, with a suitable mask design, much of the parasitic contributions from the field oxide can be eliminated.

It is also possible to adapt the process to make other capacitive sensors such as the touch-mode device that can offer better linearity, or to fabricate other sensors such as accelerometers, as previously described. It is hoped that the versatility of the sealed-cavity process will facilitate the development of more complex integrated sensors and actuators in the future.

Appendix A

Process Traveller

The following is the process description required for use in the Integrated Circuits Lab and the Technology Research Lab.

PROCESS TRAVELER

CAPACITIVE PRESSURE SENSOR

LOT cap-sensor1

LOT OWNER L.Parameswaran

STEP	STEP DESCRIPTION	STATUS

DEVICE WAFER
Starting material : p-type <100> Si, 10-20Ωcm

STEP	STEP DESCRIPTION	STATUS
1	Stress Relief Oxide dsro430.set (ICL)	Number wafers ________ Opset start ________ Opset finish ________
2	Implant phosphorus instop.set (ICL) energy=160keV, dose=5E15	Number wafers ________ Opset start ________ Opset finish ________
3	Phos drive-in dphosdrive.set (ICL) N2, 1150C, 15hrs	Number wafers ________ Opset start ________ Opset finish ________

4	SRO wet etch wsro430.set (ICL)	Number wafers ________ Opset start ________ Opset finish ________

HANDLE WAFER

Starting material: n-type <100> Si, 0.5-2Ωcm

1	Cavity pattern phcavity.set (TRL)	Number wafers ________ Opset start ________ Opset finish ________
2	Silicon plasma etch plsi10k.set (ICL) recipe 12	Number wafers ________ Opset start ________ Opset finish ________
3	Resist ash ash.set (ICL)	Number wafers ________ Opset start ________ Opset finish ________
4	Laser-drill holes (Lincoln Labs)	Number wafers ________ Opset start ________ Opset finish ________
5	Post-KOH clean postKOH.set (TRL)	Number wafers ________ Opset start ________ Opset finish ________

DEVICE AND HANDLE WAFERS - electrochemical etch stop

1	Bond wafers dbond.set (TRL) N2 1000°C 1hr.	Number wafers ________ Opset start ________ Opset finish ________
2	Electrochemical etch wetch_stop.set (RGL) KOH 20% 95°C 3.5hrs.	Number wafers ________ Opset start ________ Opset finish ________
3	Post-KOH clean postKOH.set (TRL)	Number wafers ________ Opset start ________ Opset finish ________
4	Stress Relief Oxide dsro430.set (ICL)	Number wafers ________ Opset start ________ Opset finish ________

5	Pattern p+ implant php+.set (TRL)	Number wafers ________ Opset start ________ Opset finish ________
6	Implant boron ipcontact.set (ICL) energy=40keV, dose=1E16	Number wafers ________ Opset start ________ Opset finish ________

** NOTE: Flag wafers before implant to indicate that they have been bonded

7	Resist ash ash.set (ICL)	Number wafers ________ Opset start ________ Opset finish ________
8	Boron drive-in dborondrive.set (ICL) 1000C, N2, 10hrs.	Number wafers ________ Opset start ________ Opset finish ________
9	SRO wet etch wsro430.set (ICL)	Number wafers ________ Opset start ________ Opset finish ________
10	Deposit LTO dLTO1u.set (ICL)	Number wafers ________ Opset start ________ Opset finish ________
11	Pattern LTO phLTO.set (TRL)	Number wafers ________ Opset start ________ Opset finish ________
12	Etch LTO wLTO1u.set (TRL)	Number wafers ________ Opset start ________ Opset finish ________
13	Resist strip wstrip.set (TRL)	Number wafers ________ Opset start ________ Opset finish ________
14	Resist pattern for metallization phsilicon.set (TRL)	Number wafers ________ Opset start ________ Opset finish ________
15	Metal deposition mCrAu.set (SSL)	Number wafers ________ Opset start ________

	200ÅCr + 3000ÅAu	Opset finish	________
16	Metal liftoff	Number wafers	________
	wliftoff.set (RGL)	Opset start	________
		Opset finish	________

GLASS WAFER

Starting material: 7740 Pyrex glass wafer, thickness=500 μm

1	Resist pattern	Number wafers	________
	phglass.set (TRL)	Opset start	________
		Opset finish	________
2	Metal evaporation	Number wafers	________
	mCrAu.set (SSL)	Opset start	________
	200ÅCr + 3000ÅAu	Opset finish	________
3	Metal liftoff	Number wafers	________
	wliftoff.set (RGL)	Opset start	________
		Opset finish	________

BOND GLASS AND SILICON

1	Dice wafers	Number wafers	________
	diesaw (ICL)	Opset start	________
		Opset finish	________
2	Open backside pressure inlet holes	Number wafers	________
	(Lincoln Labs)	Opset start	________
		Opset finish	________
3	Pre-bond clean	Number wafers	________
	ultraviolet ozone exposure (SSL)	Opset start	________
		Opset finish	________
4	Bond dice	Number wafers	________
	(RGL)	Opset start	________
	Heat on hotplate @ 350°C	Opset finish	________
5	Attach to header package	Number wafers	________
	diebonder (ICL)	Opset start	________
		Opset finish	________

Appendix B

SUPREM Simulations

The following files were used as input for SUPREM simulations of the formation of the device. The simulations were done using TMA Suprem-3, which has features that can be used to simulate wafer bonding. In particular, the EXTRACT command, which can be used to extract and save the dopant concentrations from a particular layer, and the INVERT command, used to invert the material layers and dopant profiles of the structure currently being simulated, were useful in approximating the process steps that occur during wafer bonding. Files for the device and handle wafer are run separately, after which the structures are merged together.

```
TITLE bonded wafers
$ Device (etchstop) wafer
INITIALIZE SILICON <100> THICKNES=30 X.LOCAT=0.0 Z.LOCAT=0.0 DX=0.01 +
 MIN.DX=0.001 XDX=0.0 SPACES=200 RESISTIV BORON=15
$ grow sro
DIFFUSION TEMPERAT=1000 TIME=30 INERT
DIFFUSION TEMPERAT=900 TIME=240 DRYO2
DIFFUSION TEMPERAT=1000 TIME=30 INERT
$ implant and drive-in etchstop layer
IMPLANT   PHOSPHOR PEARSON RP.EFF DOSE=5e15 ENERGY=160
DIFFUSION TEMPERAT=1150 TIME=900 INERT
ETCH      OXIDE ALL
$ extract dopant info for bonding
EXTRACT   THICKNES LAYER=1 NAME=Tsi
INVERT
EXTRACT   OUT.FILE=doping
LOOP      STEPS=300
ASSIGN    NAME=X N.VALUE=0 DELTA=@Tsi/300
EXTRACT   CHEMICAL PHOSPHOR Y.EXTRAC X=@X X.MIN=0.0 VARIABLE=@X
L.END
EXTRACT   CLOSE
PRINT     LAYERS
STOP
```

```
TITLE bonded wafers
$ Handle wafer
INITIALIZE SILICON <100> THICKNES=15 X.LOCAT=0.0 Z.LOCAT=0.0 DX=0.01 +
 MIN.DX=0.001 XDX=0.0 SPACES=200 CONCENTR PHOSPHOR=8.7e15
$ phos-dep to heavily dope surfaces
DIFFUSION TEMPERAT=925 TIME=90 SS.PHOSP INERT
DIFFUSION TEMPERAT=950 TIME=60 DRYO2
ETCH      OXIDE ALL
$ bond handle wafer - p-Si, 15ohm-cm
DEPOSITION SILICON <100> THICKNES=30 DX=0.01 MIN.DX=0.001 XDX=0.0 SPACES=100 +
 RESISTIV BORON=15
$ read in dopant info for ece stop
PROFILE   PHOSPHOR LAYER=1 CHEMICAL IN.FILE=doping X.OFFSET=0.0 X.SCALE=1.0 +
 X.COLUMN=1 C.COLUMN=2
PLOT      ACTIVE NET COLOR=1 LINE.TYP=1
$ bonding anneal
DIFFUSION TEMPERAT=1000 TIME=70 WETO2
PLOT      ACTIVE NET COLOR=1 LINE.TYP=1
ETCH      OXIDE ALL
$ etch silicon to junction (e-chem)
EXTRACT   ACTIVE NET X.EXTRAC Y=0 X.MIN=0.0 NAME=XJ
LOOP      STEPS=@XJ/0.05
ASSIGN    NAME=X N.VALUE=0 DELTA=0.05
ETCH      SILICON THICKNES=0.05
IF COND=(@X>@XJ)
L.MODIFY  STEPS=1
IF.END
L.END
PLOT      ACTIVE NET COLOR=1 LINE.TYP=1
$ implant boron for bottom capacitor plate contact & drive-in
IMPLANT   BORON PEARSON RP.EFF DOSE=5e16 ENERGY=50
DIFFUSION TEMPERAT=950 TIME=900 INERT
PRINT     LAYERS
PLOT      ACTIVE NET COLOR=1 LINE.TYP=1
SAVEFILE  OUT.FILE=bonded_pair ALL
STOP
```

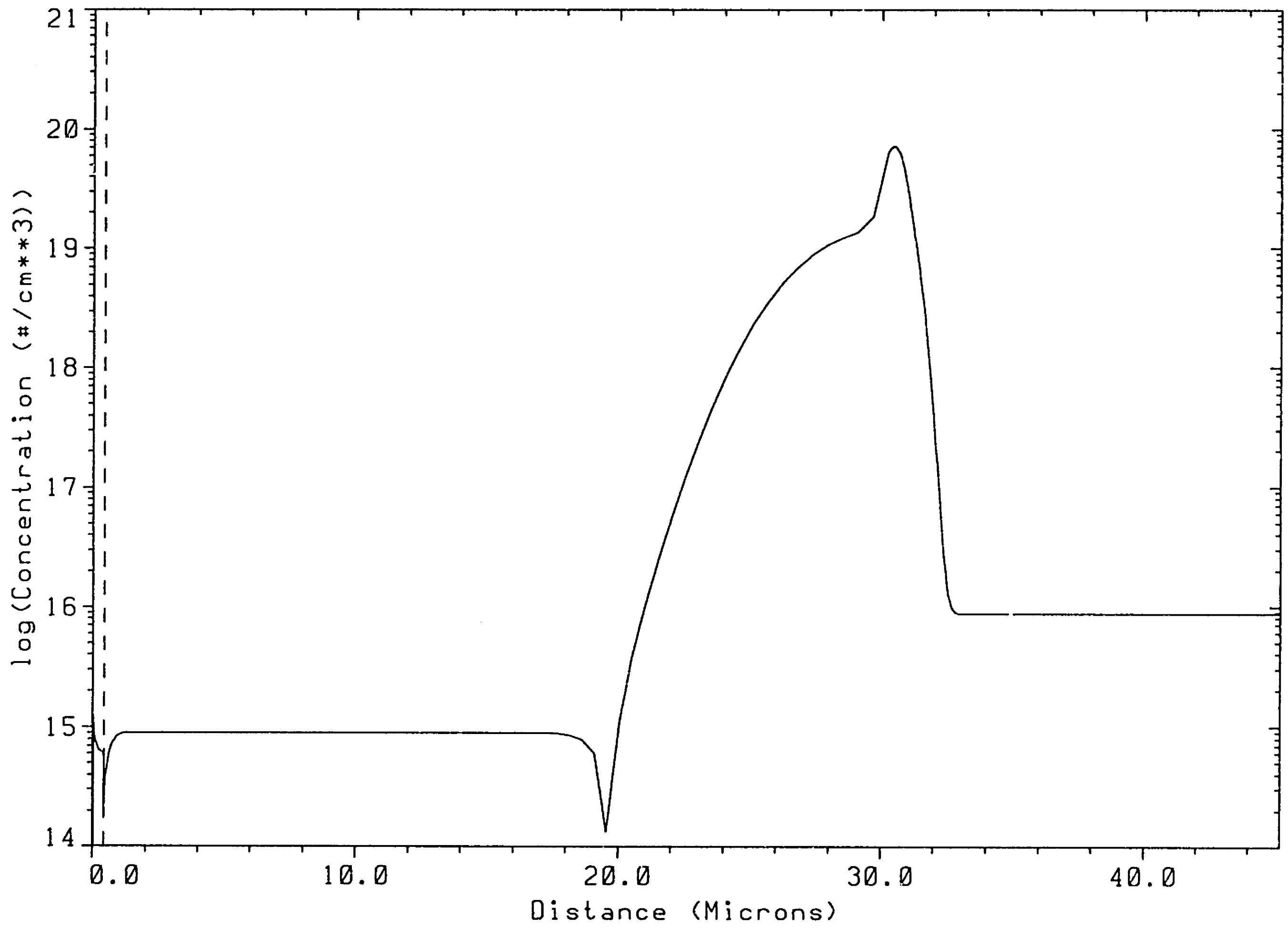


Figure B-1: Net dopant profile (n-type) after wafer bonding step and before etchback

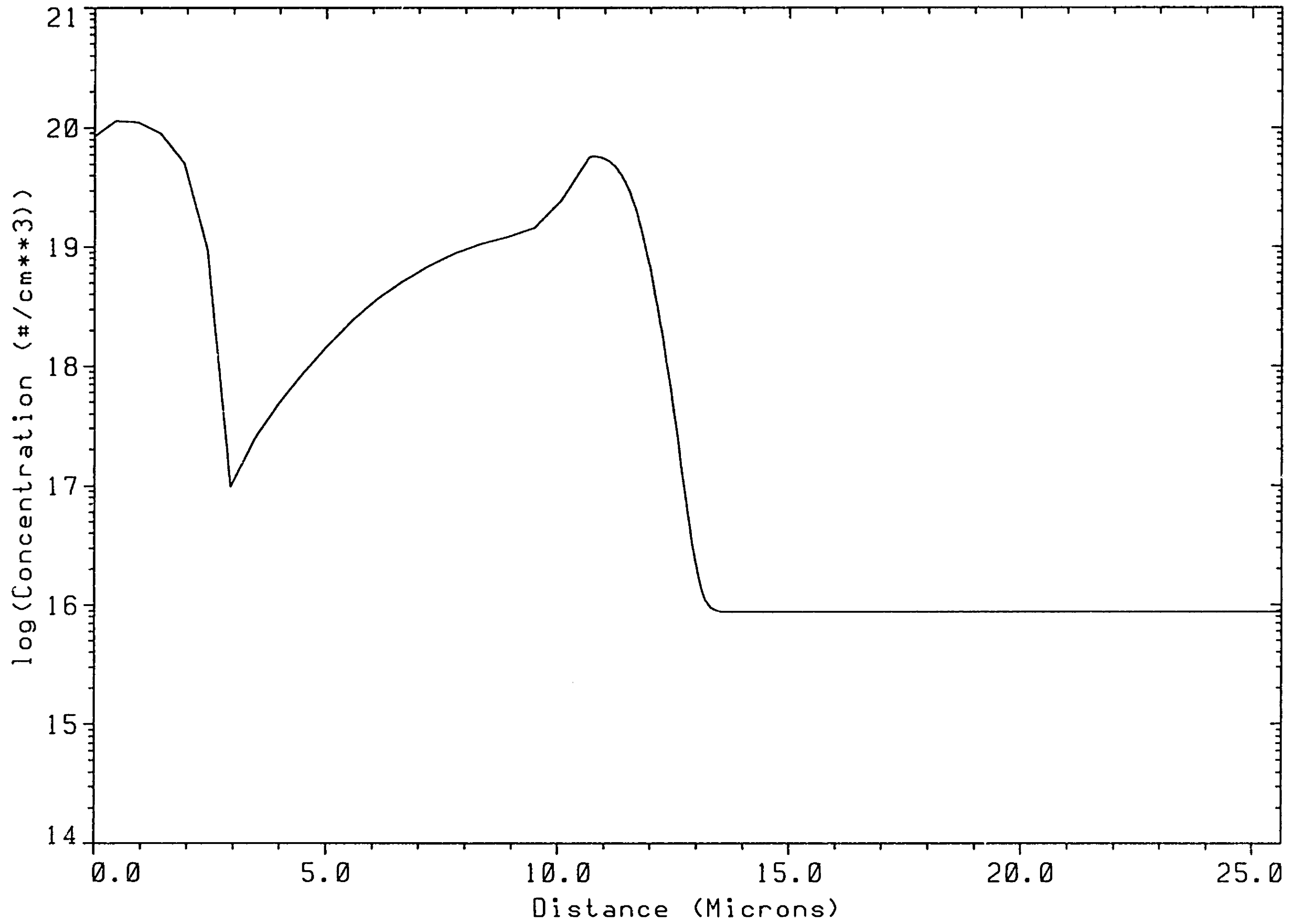


Figure B-2: Net dopant profile for final membrane (boron at surface, phosphorus for remainder of substrate)

Appendix C

Mask Set

This appendix contains layout diagrams for the mask set used to fabricate the sensors. The layout was done using KIC[66]. The masks are, in order, for:

- silicon trench etch
- boron implant in membrane areas
- membrane and contact cut through LTO
- metallization for silicon
- metallization for glass capping die

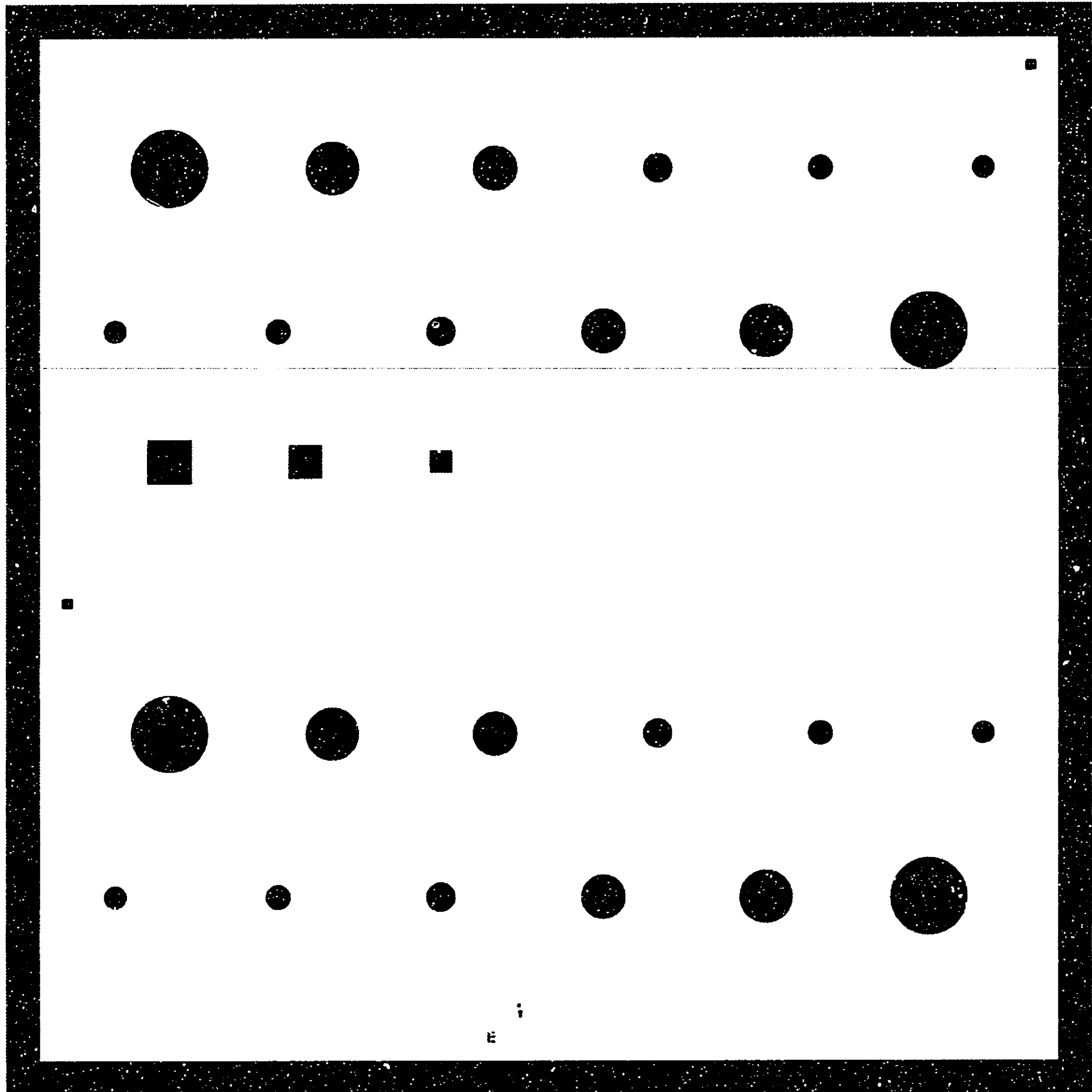


Figure C-1: Mask for silicon trench etch

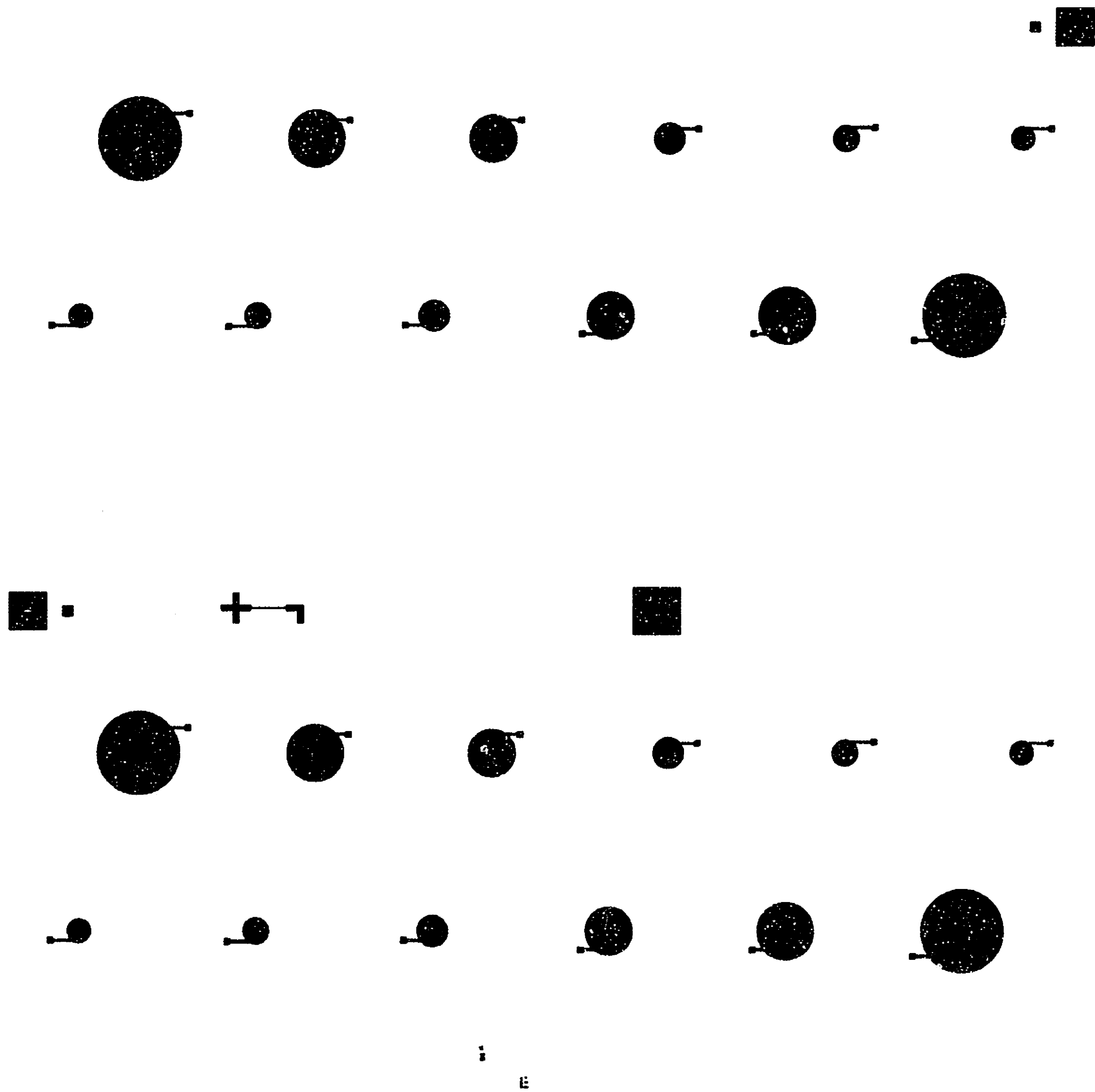


Figure C-2: Mask for boron implant to dope membrane

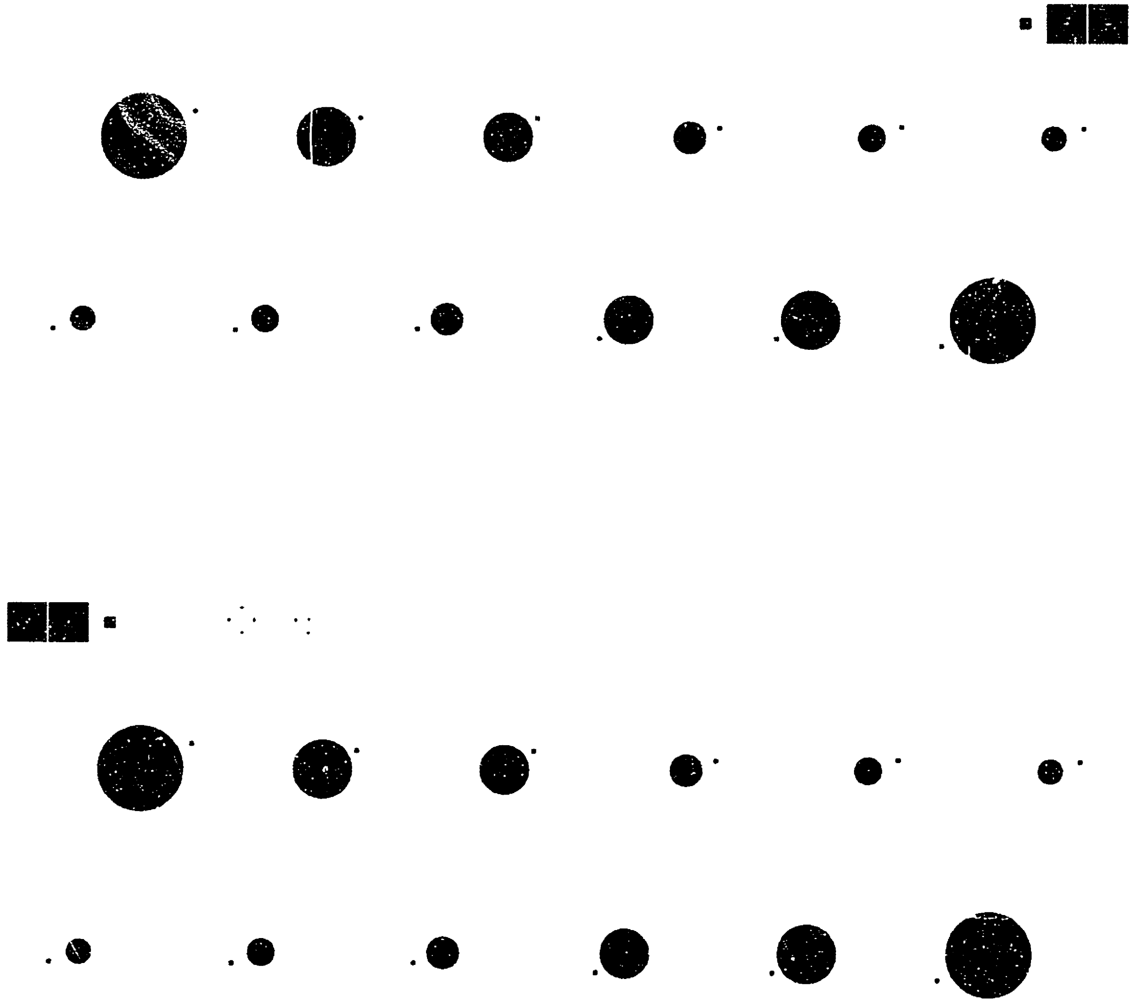


Figure C-3: Mask for LTO etch to clear membrane and contact areas

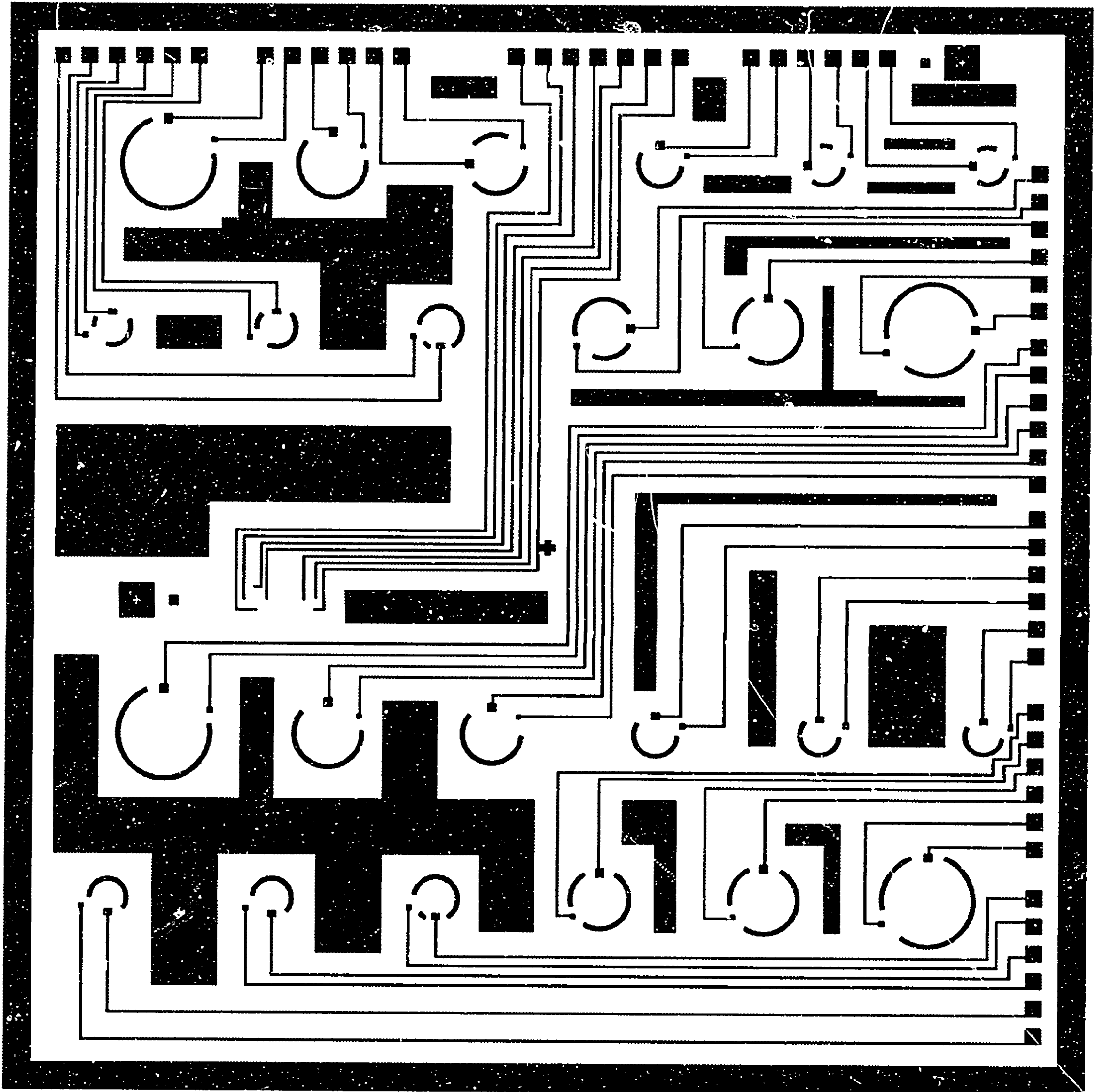


Figure C-4: Mask for silicon metallization

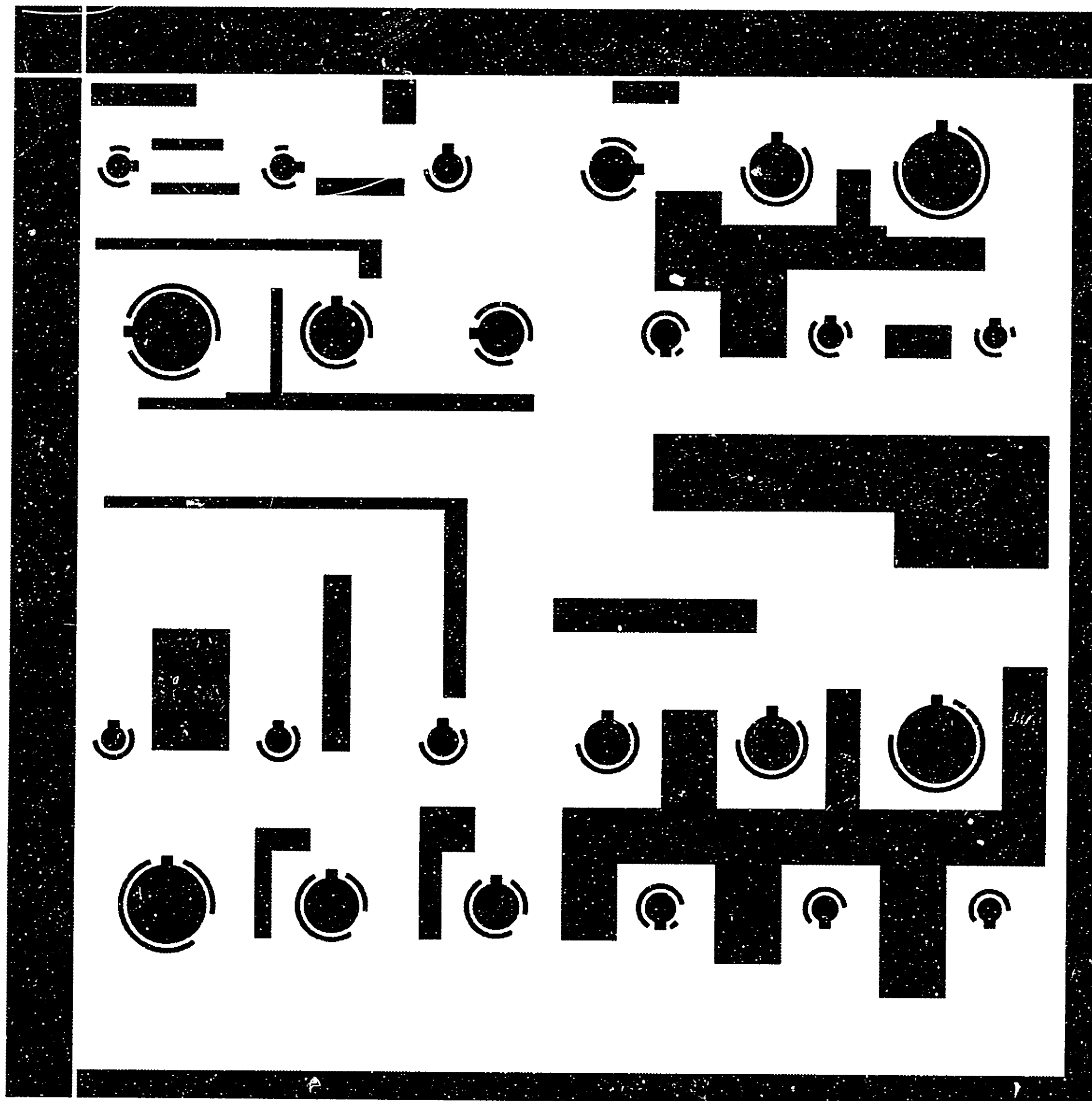


Figure C-5: Mask for glass metallization

Bibliography

[1] K.E. Petersen. Silicon as a mechanical material. *Proceeding of the IEEE*, 70, No.5:420–457, May 1982.

[2] J.J. Wortman and L.K. Monteith. Semiconductor mechanical sensor. *IEEE Transactions on Electron Devices*, ED-16, No.10:855–860, October 1969.

[3] P. Leaver and M.J. Cunningham. Piezoelectric polymer pressure sensors. *Sensors and Actuators*, A12:225–233, 1987.

[4] B. Samaun, K.D. Wise, and J.B. Angell. An IC piezoresistive pressure sensor for biomedical instrumentation. *IEEE Transactions on Biomedical Engineering*, BME-20, No.3:101–106, March 1973.

[5] T. Ishihara, M. Hirata, K. Suzuki, and H. Tanigawa. CMOS integrated pressure sensor. In *Custom Integrated Circuits Conference*, pages 34–37. IEEE, 1986.

[6] Y. Wang, X. Zheng, L. Liu, and Z. Li. A novel structure of pressure sensors. *IEEE Transactions on Electron Devices*, ED-38, No.8:1797–1801, August 1991.

[7] P. Kopystynski and E. Obermeier. An interchangeable silicon pressure sensor with on-chip compensation circuitry. *Sensors and Actuators*, A18:239–245, 1989.

[8] E. Obermeier. Polysilicon layers lead to a new generation of pressure sensors. In *Transducers '85 - 3rd International Conference on Solid-State Sensors and Actuators*, pages 430–433. IEEE, 1985.

[9] T. Fujii, Y. Gotoh, and S. Kuroyanagi. Fabrication of microdiaphragm pressure sensor utilizing micromachining. *Sensors and Actuators*, A34:217–224, 1992.

[10] M.A. Schmidt and R.T. Howe. Resonant structures for integrated sensors. In *IEEE Solid State Sensor and Actuator Workshop*. IEEE, 1986.

[11] T.E. Shirley. *Frequency-pulling effects in microfabricated resonant structures*. SM thesis, Massachusetts Institute of Technology, February 1993.

[12] S.K. Clark and K.D. Wise. Pressure sensitivity in anisotropically etched thin-diaphragm pressure sensors. *IEEE Transactions on Electron Devices*, ED-26, No.12:1887–1895, December 1979.

[13] H. Chau and K.D. Wise. Scaling limits in batch-fabricated silicon pressure sensors. *IEEE Transactions on Electron Devices*, ED-34, No.4:850–858, April 1987.

[14] W.D. Frobenius, A.C. Sanderson, and H.C. Nathanson. A microminiature solid state capacitive blood pressure transducer with improved sensitivity. *IEEE Transactions on Biomedical Engineering*, BME-20, No.7:312–314, August 1973.

[15] W.H. Ko, M. Bao, and Y. Hong. A high-sensitivity integrated-circuit capacitive pressure transducer. *IEEE Transactions on Electron Devices*, ED-29, No.1:48–56, January 1982.

[16] G.T. Mulhern, D.S. Sloan, and R.T. Howe. Supercritical carbon dioxide drying of microstructures. In *Transducers '93 - 7th International Conference on Solid-State Sensors and Actuators*, pages 296–299. IEEE, 1993.

[17] M. Farooqui and A.G.R. Evans. A polysilicon-diaphragm-based pressure sensor technology. *Journal of Physics E*, 20:1469–1471, 1987.

[18] H. Guckel and D.W. Burns. Planar processed polysilicon sealed cavities for pressure transducer arays. In *Technical Digest IEDM*, page 223. IEEE, 1984.

[19] S.T. Cho, K. Najafi, and K.D. Wise. Scaling and dielectric stress compensation of ultrasensitive boron-doped silicon microstructures. In *Proceedings of the IEEE Microelectromechanical Systems Workshop*, pages 50–55, 1990.

[20] L. Christel, K. Petersen, P. Barth, F. Pourahmadi, J. Mallon, and J. Bryzek. Single-crystal silicon pressure sensors with 500x overpressure protection. *Sensors and Actuators*, A21-23:84–88, 1990.

[21] Y. Wang, L. Liu, X. Zheng, and Z. Li. A novel pressure sensor structure for integrated sensors. *Sensors and Actuators*, A21-23:62–64, 1990.

[22] T. Nagata, H. Terabe, S. Kuwuhara, and S. Sakurai. Digital compensated capacitive pressure sensor using CMOS technology for low pressure measurements. In *Transducers '91 - 6th International Conference on Solid-State Sensors and Actuators*, pages 308–311. IEEE, 1991.

[23] J.T. Kung. *Integrated capacitive sensors using charge-redistribution sense techniques.* PhD thesis, Massachusetts Institute of Technology, June 1992.

[24] J.B. Lasky. Wafer bonding for silicon-on-insulator technologies. *Applied Physics Letters*, 48, No.1:78, 1986.

[25] W.P. Maszara, G. Goetz, A. Caviglia, and J.B. McKitterick. Bonding of silicon wafers for silicon-on-insulator. *Journal of Applied Physics*, 64, No.10:4943, 1988.

[26] A. Nakagawa, K. Watanabe, Y. Yamaguchi, H. Ohashi, and K. Furukawa. 1800v bipolar-mode mosfets: A first application of silicon wafer direct bonding (SDB) technique to power device. In *Technical Digest, IEDM*, pages 122–125. IEEE, 1986.

[27] H. Ohashi, J. Ohura, T. Tsukakoshi, and M. Shimbo. Improved dielectrically isolated device integration by silicon-wafer direct bonding (sdb) technique. In *Technical Digest, IEDM*, pages 678–681. IEEE, 1987.

[28] F. Rudolf, A. Jornod, and P. Bencze. Silicon microaccelerometer. In *Transducers '87 - 4th International Conference on Solid-State Sensors and Actuators*, pages 395–398. IEEE, 1987.

[29] M.A. Huff, M.S. Mettner, T.A. Lober, and M.A. Schmidt. A pressure-balanced electrostatically-actuated microvalve. In *Technical Digest, IEEE Solid-State Sensor and Actuator Workshop*, pages 123–127. IEEE, 1990.

[30] K. Petersen, J. Brown, T. Vermullen, P. Barth, J. Mallon, and J. Bryzek. Ultra-stable, high-temperature pressure sensors using silicon fusion bonding. *Sensors and Actuators*, A21-23:96–101, 1990.

[31] K. Petersen, P.W. Barth, J. Poydock, J. Brown, J. Mallon, and J. Bryzek. Silicon fusion bonding for pressure sensors. In *Proceedings of the IEEE Solid-State Sensor and Actuator Workshop*, page 144. IEEE, 1988.

[32] J. Shajii, K-Y Ng, and M.A. Schmidt. A microfabricated floating-element shear stress sensor using wafer-bonding technology. *IEEE Journal of Microelectromechanical Systems*, 1, No.2:89–94, 1992.

[33] R.C. Frye, J.E. Griffith, and Y.H. Young. A field-assisted bonding process for silicon dielectric isolation. *Journal of the Electrochemical Society*, 133:1673, 1986.

[34] A. Hanneborg, M. Nese, and P. Ohlckers. Silicon-to-silicon anodic bonding with a borosilicate glass layer. *J. Micromech. Microeng.*, 1:139–144, 1991.

[35] J.R. Gilbert, P.M. Osterberg, R.M. Harris, D.O. Ouma, X. Cai, A. Pfajfer, J. White, and S.D. Senturia. Implementation of a MEMCAD system for electrostatic and mechanical analysis of complex structures from mask descriptions. In *Proceedings of the IEEE Microelectromechanical Systems Workshop*, pages 207–212. IEEE, 1993.

[36] S.P. Timoshenko. *Theory of Plates and Shells.* McGraw-Hill, 1940.

[37] J.A. Lloyd. Personal communication.

[38] L. Rosengren, J. Söderkvist, and L. Smith. Micromachined sensor structures with linear capacitive response. *Sensors and Actuators*, A31:200–205, 1992.

[39] PDA Engineering, PATRAN Division, 2975 Redhill Avenue, Costa Mesa, CA 92626. *PATRAN.*

[40] Hibitt, Karlsson and Sorensen, Inc. *ABAQUS*, version 4.8 edition.

[41] K. Nabors and J. White. FastCap: A Multipole-Accelerated 3-D Capacitance Extraction Program. *IEEE Transactions on Computer-Aided Design*, 10, No.10:1447–1459, November 1991.

[42] Y. He and P. Osterberg. Personal communication.

[43] T. Bloomstein and D.J. Ehrlich. Laser deposition and etching of three-dimensional microstructures. In *Transducers '91 - 6th International Conference on Solid-State Sensors and Actuators*, page 507. IEEE, 1991.

[44] L. Parameswaran, V.M. McNeil, M.A. Huff, and M.A. Schmidt. Sealed cavity microstructure using wafer bonding technology. In *Transducers '93 - 7th International Conference on Solid-State Sensors and Actuators*, pages 274–277. IEEE, 1993.

[45] H. Seidel, L. Csepregi, A. Heuberger, and H. Baumgartel. Anisotropic etching of crystalline silicon in alkaline solutions. *Journal of the Electrochemical Society*, 137:3612, 1990.

[46] H. Seidel. The mechanism of anisotropic electrochemical silicon etching in alkaline solutions. In *Technical Digest, IEEE Solid-State Sensor and Actuator Workshop*, pages 86–91. IEEE, 1990.

[47] B. Kloeck, S. Collins, N. de Rooij, and R.L. Smith. Study of electrochemical etch-stop for high precision thickness control of silicon membranes. *IEEE Transactions on Electron Devices*, ED-36, No.4:663–669, 1989.

[48] V.M. McNeil, S.S. Wang, and M.A. Schmidt. Issues regarding the application of the electrochemical etch-stop technique to fabricate structures using wafer bonding. In *Proceedings of Symposium on Semiconductor Wafer Bonding Science, Technology and Applications.* Electrochemical Society, 1991.

[49] V.M. McNeil, S.S. Wang, K-Y Ng, and M.A. Schmidt. An investigation of the electrochemical etching of (100) Si in CsOH and KOH. In *IEEE Solid State Sensor and Actuator Workshop.* IEEE, 1990.

[50] V.M. McNeil, M.J. Novack, and M.A. Schmidt. Design and fabrication of thin-film microaccelerometers using wafer bonding. In *Transducers '93 - 7th International Conference on Solid-State Sensors and Actuators*, pages 822–825. IEEE, 1993.

[51] TOPO-3D Surface Profilometer, Wyko Corporation, Tucson, AZ.

[52] M.A. Huff, A.D. Nikolich, and M.A. Schmidt. A threshold pressure switch utilizing plastic deformation. In *Transducers '91 - 6th International Conference on Solid-State Sensors and Actuators*, pages 177–180. IEEE, 1991.

[53] M.A. Huff, A.D. Nikolich, and M.A. Schmidt. Design of sealed cavity microstructures formed by silicon wafer bonding. *IEEE Journal of Microelectromechanical Systems*, 2, June 1993.

[54] M.A. Huff. *Silicon Micromachined Wafer-Bonded Valves.* PhD thesis, Massachusetts Institute of Technology, February 1993.

[55] J.R. Patel and A.S. Choudhri. *Journal of Applied Physics*, 34:2788, 1963.

[56] R. Stengl, K-Y. Ahn, and U. Gösele. Bubble-free silicon wafer bonding in a non-cleanroom environment. *Japanese Journal of Applied Physics*, 27, No.12:L2364, 1988.

[57] B. Frazier, J.W. Babb, and M.G. Allen. Design and fabrication of electroplated micromotor structures. In *Winter Annual Meeting of the American Society of Mechanical Engineers.* ASME, December 1991.

[58] S. Furukawa, H. Miyajima, M. Mehregany, and C.C. Liu. Electroless plating of metals for micromechanical structures. In *Transducers '93 - 7th International Conference on Solid-State Sensors and Actuators*, pages 66–69. IEEE, 1993.

[59] P. Krulevitch, R.T. Howe, G.C. Johnson, and J. Huang. Stress in undoped LPCVD polycrystalline silicon. In *Transducers '91 - 6th International Conference on Solid-State Sensors and Actuators*, pages 949–952. IEEE, 1991.

[60] C.H. Mastrangelo and C.H. Hsu. Mechanical stability and adhesion of microstructures under capillary forces. *IEEE Journal of Microelectromechanical Systems*, Vol.2, No.1:33–62, March 1993.

[61] C.C. Lee, C.Y. Wang, and G.S. Matijasevic. Advances in bonding technology for electronic packaging. *Journal of Electronic Packaging*, 115:201–207, June 1993.

[62] G.C. Harman and J. Albers. The ultrasonic welding mechanism as applied to aluminum and gold-wire bonding in microelectronics. *IEEE Transactions on Parts, Hybrids and Packaging*, PHP-13, No.4:406–412, December 1977.

[63] N. Ahmed and J.J. Svitak. Characterization of gold-gold thermocompression bonding. *Solid State Technology*, pages 25–32, November 1975.

[64] American Society for Testing and Materials. *1992 Annual book of ASTM standards, Volume 10.04*.

[65] J.Y. Pan. *A study of suspended-membrane and acoustic techniques for the determination of the mechanical properties of thin polymer films.* PhD thesis, Massachusetts Institute of Technology, September 1991.

[66] G. Billingsley and K. Keller. *KIC: A graphics editor for Integrated Circuits.* University of California at Berkeley.