Entanglement scaling in quantum advantage benchmarks

Entanglement scaling in quantum advantage benchmarks

Jacob D. Biamonte,[1,*] Mauro E. S. Morales,[1,†] and Dax Enshan Koh[2,1,‡]
[1]*Deep Quantum Laboratory, Skolkovo Institute of Science and Technology, 3 Nobel Street, Moscow 121205, Russia*
[2]*Department of Mathematics, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA*

(Received 5 August 2019; published 31 January 2020)

A contemporary technological milestone is to build a quantum device performing a computational task beyond the capability of any classical computer, an achievement known as quantum adversarial advantage. In what ways can the entanglement realized in such a demonstration be quantified? Inspired by the area law of tensor networks, we derive an upper bound for the minimum random circuit depth needed to generate the maximal bipartite entanglement correlations between all problem variables (qubits). This bound is lattice geometry dependent and makes explicit a nuance implicit in other proposals with physical consequence. The hardware itself should be able to support superlogarithmic ebits of entanglement across some poly(n) number of qubit bipartitions; otherwise the quantum state itself will not possess volumetric entanglement scaling and full-lattice-range correlations. Hence, as we present a connection between quantum advantage protocols and quantum entanglement, the entanglement implicitly generated by such protocols can be tested separately to further ascertain the validity of any quantum advantage claim.

DOI: 10.1103/PhysRevA.101.012349

I. INTRODUCTION

Rapid experimental advancements have spawned an international race towards the first experimental quantum adversarial advantage demonstration, in which a quantum computer outperforms a classical one at some task [1–18]. There is likewise interest in understanding the effectiveness of low-depth quantum circuits for, e.g., machine learning [19] and quantum simulation [14]. Adding to this theory, we propose a quantification of the maximal entanglement (manifest in correlations between problem variables) that a given quantum computation can support [20]. Quantification of the minimal-size circuits needed to produce, even in principle, maximally correlated quantum states fills gaps missing in the theory of quantum adversarial advantage and low-depth circuits in general. Indeed, such minimal-depth circuits, as predicted by our theory, seem to be small quantum circuits that are difficult to simulate classically and hence might offer a quantum advantage for practical problems even beyond random adversarial advantage benchmarks.

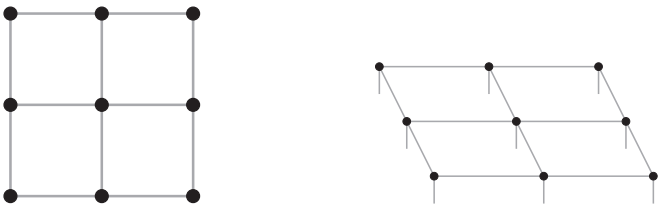
The goal of the quantum adversarial advantage is to perform any task that is beyond the capability of any known classical computer. A naive starting point would be to consider the evident memory limitations of classical computers and to create a quantum state exceeding that. If we consider an ideal quantum state, we must store at most $2^{n+1} \times 16$ bytes of information, assuming 32-bit precision. This upper bound reaches 80 terabytes (TB) at just less than 43 qubits and 2.2 petabytes (PB) at just under 47. Eighty TB and 2.2 PB are commonly referenced as the maximum memory storage capacity of a rapid supercomputing node and the supercomputer Trinity with the world's largest memory, respectively. Thus a quantum adversarial advantage might already be possible with 47 or more qubits (strong simulation). The problem is that the creation of states requiring 2^{n+1} independent degrees of freedom would require $O(\exp[n])$ gates, well beyond the coherence time of any device beyond the fault-tolerance threshold. Thus we must search for another adversarial advantage protocol, requiring lower-depth circuits.

II. BACKGROUND

Broadly speaking, the leading proposals for the quantum adversarial advantage can be divided into two categories: (i) those that provide strong complexity-theoretic evidence of classical intractability (based, for example, on the noncollapse of the polynomial hierarchy) and (ii) those that promise to be imminent candidates for experimental realization. Examples in category (i) include sampling from (a) boson sampling circuits [2], (b) instantaneous quantum polynomial circuits [1], and (c) deterministic quantum computation with one quantum bit circuits [21]. A leading example in category (ii) is the problem of sampling from random quantum circuits.

The existence of an efficient classical algorithm which can simulate random quantum circuits seems unlikely. In particular, it would imply the violation of the quantum threshold assumption [10]. However, this says nothing about the number of qubits and the depths of the circuits required to demonstrate this separation between quantum and classical computational devices. To address this, all arguments to date have extrapolated, based on numerics or counting resources, where the classical intractability crossover point will occur. Our theory does not avoid this *per se*; it simply provides upper bounds of the entanglement generated by a random circuit. The same amount of entanglement generated by a random adversarial

*j.biamonte@skoltech.ru
†mauricioenrique.moralessoler@skoltech.ru
‡daxkoh@mit.edu



(a) (b)

FIG. 1. Example of (a) a quantum processor grid and (b) the induced projected entangled pair state. (a) Grid for a quantum processor of 3×3 qubits. Each node represents a qubit and each edge a tunable coupling between the qubits. (b) PEPS induced by the grid in (a). Each node with an open wire is a tensor. The open wires represent physical degrees of freedom in the tensor network and the internal edges represent internal bonds of some fixed dimension.

advantage circuit can be tested external to the adversarial advantage demonstration. We bound the required gate depth to maximally entangle any bipartition on a quantum processor; prior numerical simulations of the benchmark proposed in [5] are below this bound. It is important to note that the gate depth required to maximally entangle all bipartitions is not a sufficient condition to achieve a quantum adversarial advantage. Our methods to perform an analysis of the entanglement are based on ideas from tensor networks. Alternative approaches have previously studied the role of entanglement in quantum algorithms such as Shor's algorithm [22,23].

An observation of central importance is that existing quantum processors rely on qubits where the restriction is that these qubits interact on the two-dimensional planar lattice. In the long term, the specific layout will be of less consequence. However, for low-depth circuits a subtle implication is that the lattice embodies a small-world property, in which long-range correlations must be induced as a sequence of nearest-neighbor operations. Indeed, the Hilbert space describing the quantum processor can be entirely induced by a tensor network [24] with the same underlying grid geometry of the Hamiltonian governing the quantum processor itself. Our bounds are formulated in this setting and are generally applicable across all current quantum adversarial advantage protocols.

III. RESULTS

We consider a quantum processor with a geometry represented as a graph $G = (V, E)$. Nodes $v \in V$ are qubits and edges $e \in E$ are couplings which can be adjusted to create interactions between qubits (two-body gates). At any point in the calculation, the state of the system is described by the wave function corresponding to the qubits of the quantum processor. This naturally gives rise to a projected entangled pair state (PEPS) tensor network [25].

We will consider quantum circuits that are formed by acting on the interaction graphs appearing in Fig. 1. A quantum process is hence a space-time diagram codified by a triple of natural numbers $l \times m \times g$ where we assume that $n = l \times m$ qubits enumerate the nodes of a rectangular lattice Q and g is the gate depth of circuits acting on Q. As will be seen, the variation over all circuits of depth at most g acting on an $l \times m$ qubit grid lifts to a state space. Here the edges of Q connect $2(\sqrt{n}-1)\sqrt{n}$ horizontal (otherwise vertical) nearest-neighbor pairs, where $\sqrt{n}$ will be deformed later so as to deviate from a perfect square and hence capture the rectangular structure of certain contemporary quantum information processors (see Appendix B). We will fix a canonical basis found from iterating all possible binary values of the qubits positioned on the nodes of Q, which is given by the complex linear extension of the domain $\{0,1\}^l \times \{0,1\}^m$.

This assignment lifts the internal legs of Q to linear operators between external (qubit) nodes and hence fully defines our state space. Indeed, the grid structure induces a dichotomy between tensors of (i) valence (3,1) and (ii) valence (4,1), where the first is of type $\mathbb{C}_\chi^{\otimes 3} \to \mathbb{C}_2$ and the second is $\mathbb{C}_\chi^{\otimes 4} \to \mathbb{C}_2$. The parameter χ will be defined later as the internal bond dimension. We note that the minimum edge cut bipartitioning n qubits into two halves is $\text{mincut}(Q) = \sqrt{n}$, which will become a quantity of significance. A graphical example of the induced PEPS from a grid is shown in Fig. 1.

The rank is the Schmidt number (the number of nonzero singular values) across any of the bipartitions into $\lceil n/2 \rceil$ qubits on a grid. The rank provides an upper bound on the bipartite entanglement that a quantum state can support; as will be seen, a rank-k state has at most $\log_2(k)$ ebits of entanglement. This provides an entanglement coarse graining which we use to quantify circuits.

An ebit is a unit of entanglement contained in a maximally entangled two-qubit (Bell) state. A quantum state with q ebits of entanglement (quantified by any entanglement measure) contains the same amount of entanglement (in that measure) as q Bell states. If a task requires r ebits, it can be done with r or more Bell states, but not with fewer. Maximally entangled states in $\mathbb{C}^d \otimes \mathbb{C}^d$ have $\log_2(d)$ ebits of entanglement. The question is then to upper bound the maximum amount of bipartite entanglement a given quantum computation can generate, turning to the aforementioned entanglement coarse graining to classify quantum algorithms in terms of both the circuit depth and the maximum number of ebits possible. For low-depth circuits, these arguments are surprisingly relevant.

To understand this, we note that the maximum number of ebits generated by a fully entangling two-qubit gate acting on a pair of qubits is never more than a single ebit. We then consider that the maximum qubit partition with respect to ebits is into two (ideally) equal halves, which is never more than $\lceil n/2 \rceil$. We then arrive at the general result that a g-depth quantum circuit on n qubits never applies more than $\min\{\lceil n/2 \rceil, g\}$ ebits of entanglement. This in turn (see Appendix A) puts a lower bound of $\log_2 \chi = \sqrt{n}/2$ on the two-qubit gate depth to potentially drive a system into a state supporting the maximum possible number of ebits of entanglement. However, the grid structure requires the two-qubit gates acting on each qubit to be stacked, immediately arriving at $\sim\sqrt{4n}$ as the lower bound for a circuit to even in principle generate $\lceil n/2 \rceil$ ebits of entanglement. This lower bound is just below the gate depths of interest which were successfully simulated in the literature (see Fig. 2 and Sec. IV). Under our definition of coarse graining, we do not increase entanglement by the addition of local gates. Following the benchmark of

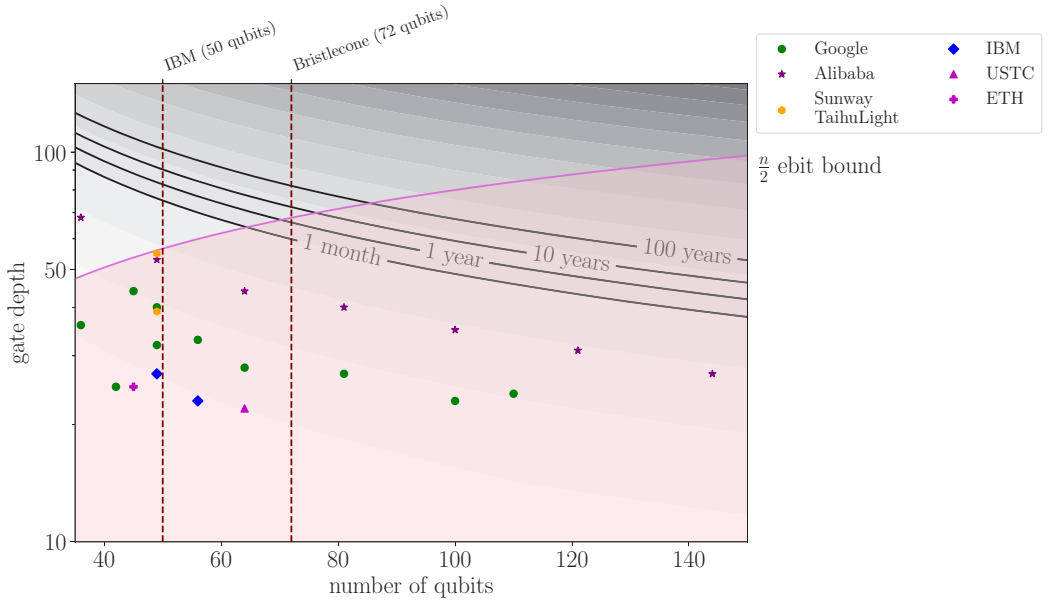


FIG. 2. Comparison of findings: qubits versus gate depths superimposed on runtimes. In pink is the area below the gate depth required to achieve maximally entangled states for every bipartition containing existing numerical data (depicted as the $n/2$ ebit bound). (Data points are from Google [5,8], Alibaba [12], Sunway TaihuLight [11], IBM [9], USTC [26], and ETH [27].)

[5], local gates are added before and after each two-qubit gate, multiplying the gate depth by a factor of 2, and the possible number of patterns of two-qubit gates is 8, which to take into consideration we multiply the gate depth by 2, yielding $\sim 8\sqrt{n}$. This number bounds the gate depth of the circuit following the protocol in [5] to maximally entangle any bipartition in the grid. This bound is shown in Fig. 2. For further generalizations see Appendix A.

IV. DISCUSSION

Figure 2 compares our bound to quantum adversarial advantage predictions. Data points included follow the prescription of a quantum circuit simulation by Google [5]. The gate set used in this prescription comprises H, $\sqrt{X}$, $\sqrt{Y}$, T, and controlled-Z gates. Gate definitions are given in Table I.

While some of these simulations, e.g., those done on the Sunway TaihuLight supercomputer [11] for a circuit depth of 39, involve the calculation of the amplitudes of all output bit strings (all 2^{46}-bit strings, in the case of Sunway TaihuLight), others such as Alibaba [9] or Sunway TaihuLight for a circuit depth of 55 involve only the calculation of a single amplitude. The data points were obtained from different simulations done recently [5,8,9,11,12,26,27].

It is interesting to note that the reported numerical simulations fall below the $n/2$ ebit bound (pink online) depicted in Fig. 2. Such circuits are considered to be low-depth circuits that are difficult to simulate classically.

We have also included a heat map with an estimation for the running time based on state-of-the-art algorithms from Alibaba [9]. To estimate the running time, we made use of the following upper bound by Markov and Shi [28]: Any α-local interacting quantum circuit of size M and depth g can be strongly simulated in time $t(M, g) = 10^{-17} M^{O(1)} \exp[O(\alpha g)]$, where a factor of 10^{-17} has been included so that the running time of the simulation is in units of seconds. For this factor, we assume that a classical computer is capable of doing 10^{17} flops. In the case of our tensor network G representing a $\sqrt{n} \times \sqrt{n}$ grid, $\alpha = \sqrt{n}$, since the quantum circuit that G represents is $\sqrt{n}$-local interacting. We also estimate the number of total gates naively as the number of couplers in the grid multiplied by the depth gate $M(n, g) = 2(\sqrt{n} - 1)\sqrt{n}g$. Hence, we consider the equation

$$t(n, g) = 10^{-17} M(n, g)^{a_1} 2^{a_2 g\sqrt{n}} \quad (1)$$

$$= 10^{-17} [2(\sqrt{n} - 1)\sqrt{n}g]^{a_1} 2^{a_2 g\sqrt{n}} \quad (2)$$

and fit it to the numerical results of Alibaba [9] (where it has been taken into consideration that only simulations for one amplitude were realized). For our fit, we obtain the parameters $a_1 = 4.360\,639\,01$ and $a_2 = 0.043\,154\,88$. With this fit we are able to give an estimation for the gate depth that can be simulated in 1 month, 1 year, 10 years, and 100 years. It is important to note here that Alibaba simulations calculate only one amplitude of an exponential number of possible strings. The algorithm is a modification from Boixo *et al.* [8] and

TABLE I. Gate set involved in the random circuit sampling benchmark recently proposed [5].

Gate	Definition
H	$\frac{1}{\sqrt{2}} \sum_{k,l=0}^{1} (-1)^{kl} \lvert k\rangle\langle l\rvert$
$\sqrt{X}$	$\frac{1}{2}[(1+i)\lvert 0\rangle\langle 0\rvert + (1-i)\lvert 0\rangle\langle 1\rvert + (1-i)\lvert 1\rangle\langle 0\rvert + (1+i)\lvert 1\rangle\langle 1\rvert]$
$\sqrt{Y}$	$\frac{1}{2}[(1+i)\lvert 0\rangle\langle 0\rvert + (-1-i)\lvert 0\rangle\langle 1\rvert + (1+i)\lvert 1\rangle\langle 0\rvert + (1+i)\lvert 1\rangle\langle 1\rvert]$
T	$\sum_{k=0}^{1} e^{i(\pi/4)k} \lvert k\rangle\langle k\rvert$
controlled-Z	$\sum_{k,l=0}^{1} (-1)^{kl} \lvert kl\rangle\langle kl\rvert$

TABLE II. Estimation based on the fit given by (1) for the gate depths achievable in the given runtime, assuming strong classical simulation of one amplitude. For our estimates, we assume that 1 year contains $365.2425 \times 24 \times 60^2$ seconds and that 1 month is $\frac{1}{12}$ of a year. The gate depths obtained are rounded up to the nearest integer.

Runtime	Gate depth for 50 qubits	Gate depth for 72 qubits
1 month	75	60
1 year	84	67
10 years	93	75
100 years	102	82

is based on treewidth to measure contraction complexity as shown by Markov and Shi. Thus, this estimation should be considered as an approximation. Finally, we include a pair of vertical lines corresponding to the quantum computers built by IBM and Google with 50 and 72 qubits, respectively. The estimations for achievable gate depths in classical computers for a given threshold are shown in Table II.

Work by Markov *et al.* [17] changes the prescription on how gates are applied. One of these changes is the inclusion of the ISWAP gate. They estimate that the gate depth to be simulated in a given runtime is about half that for the state-of-the art algorithms in this benchmark. We do not include simulations of their work in Fig. 2. Considering this, we show how the estimations are modified in Table III.

V. CONCLUSION

We have observed a nonlinear tradeoff between the number of qubits and gate depth, with the fleeting resource (with exponential dependence) being the gate depth. As is predicted, we remark that quantum adversarial advantage demonstrations (assuming completely random circuit families) should involve circuits of depth at least 50 (if not more) for 80–150 qubits. Circuits of such depth would be inside the area in pink in Fig. 2 that we derived in the study. We hence provide some handle to understand the physical entanglement that such adversarial advantage protocols aim to generate.

The data and source code used to make Fig. 2 are available online [29].

TABLE III. Estimation based on the fit given by (1) and estimation given by Google [17] considering the change of benchmark for the gate depths achievable in the given runtime, assuming strong classical simulation of one amplitude.

Runtime	Gate depth for 50 qubits	Gate depth for 72 qubits
1 month	38	30
1 year	42	33
10 years	46	38
100 years	51	41

ACKNOWLEDGMENTS

We thank Igor Markov and Mark Saffman for useful comments and Sergio Boixo for insightful discussion regarding this work.

APPENDIX A: LOWER BOUNDS FOR GENERAL TENSOR NETWORKS

In the main text we derived bounds for qubits positioned on a grid. In this Appendix we generalize the result to general graphs. Consider a tensor network G with n vertices and e edges. For convenience, we assume that n is even. Assume that the bond dimension associated with each edge is equal to χ. Let C be a cut of G that partitions the vertices of G into two disjoint subsets, each of equal size $n/2$. Let f be the number of edges that have exactly one end point in each of the two parts of C.

Proposition 1. If G supports the maximum number of ebits across C, then $\chi \geqslant 2^{n/2f}$. The total number of gates $\#_g$ needed to produce the state represented by G satisfies $\#_g \geqslant \frac{ne}{2f}$.

Proof. The maximum number of ebits across C is $n/2$. Hence, $2^{n/2} \leqslant \chi^f$, which implies that $\chi \geqslant 2^{n/2f}$. The total number of gates associated with each edge is $\log_2 \chi \geqslant \frac{n}{2f}$. Multiplying this quantity by the number of edges e, the total number of gates needed to produce the state represented by G satisfies

$$\#_g = e \log_2 \chi \geqslant \frac{ne}{2f}. \tag{A1}$$

■

In the case where G is a $\sqrt{n} \times \sqrt{n}$ grid, we have $e = 2\sqrt{n}(\sqrt{n} - 1)$. If C is a minimum cut of G, then $f = \sqrt{n}$. Substituting these values of e and f into Proposition 1 allows us to recover the equations obtained in the main text: $\chi \geqslant 2^{\sqrt{n}/2}$ and $\#_g \geqslant n(\sqrt{n} - 1)$.

Several other geometries can be analyzed as well. Consider a quantum processor with a line and a ring topology such as in Figs. 3(a) and 3(b). Following Eq. (A1), the total number of gates $\#_g$ to maximally entangle any bipartition in a quantum processor described by a graph G must be at least $\frac{ne}{2f}$, where n is the number of vertices, e is the total number of edges, and f is the number of edges that are cut by the bipartition cutting the most edges in the graph (but keeping the bipartition with an equal number of vertices). For the line we have that given n vertices, then $e = n - 1$ and $f = 1$; on the other hand, for the ring topology $e = n$ and $f = 2$. We thus conclude that

$$\#_g^{\text{line}} \geqslant \frac{n(n-1)}{2},$$

$$\#_g^{\text{ring}} \geqslant \frac{n^2}{4},$$

showing that achieving a maximally entangled bipartition requires more gates in the line topology than in the ring one for large n.

We consider as a last example a topology proposed by Rigetti [30] for a 128-qubit processor. The graph consists of octagons such as the one in Fig. 3(b), which form a grid as in Fig. 3(c). Call o the number of octagons in the graph; then

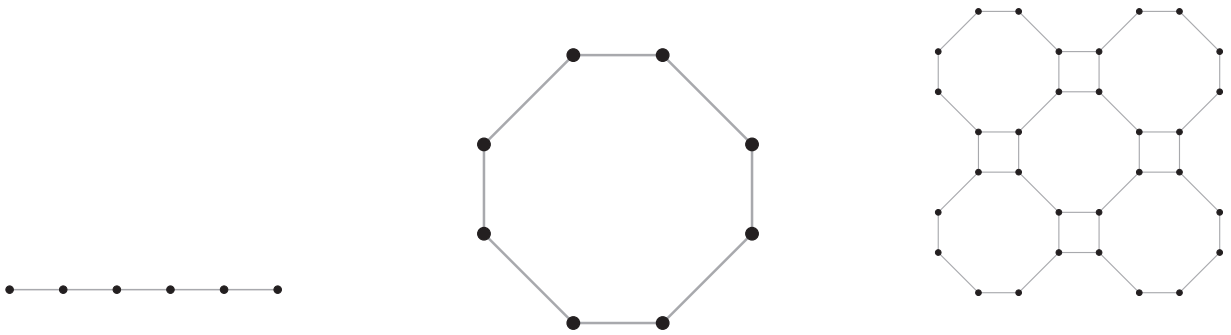


FIG. 3. Examples of graph topologies for a quantum processor: (a) Line topology, a line with $n = 6$ qubits, (b) Ring topology, a ring with $n = 8$ qubits, and (c) Rigetti topology, architecture announced by Rigetti [30]. We consider here a grid composed of octagonal rings connected as shown in the figure.

$e = 8o + 2 \times [2\sqrt{o}(\sqrt{o} - 1)]$. The first term comes from the fact that each octagon has eight edges and the second comes from the fact that there are $2\sqrt{o}(\sqrt{o} - 1)$ double edges between octagons in the grid of octagons. It is directly determined that the fewest number of edges that a bipartition can cross is $f = 2\sqrt{o}$. Since $o = \frac{n}{8}$, we have that

$$\#_g^{Rigetti} \geqslant \frac{ne}{2f} = \frac{3}{\sqrt{8}} n\sqrt{n} - n,$$

which implies that the required number of gates applied in the Rigetti topology is greater than in the grid case, as it would be expected.

APPENDIX B: LOWER BOUNDS FOR THE DEFORMED GRID

Let H be a $(\sqrt{n} - k) \times (\frac{n}{\sqrt{n}-k})$ grid. In other words, H is a deformation of the $\sqrt{n} \times \sqrt{n}$ grid G, wherein the number of qubits along one edge is reduced by k and the total number of qubits is kept constant at n. Assume that $\sqrt{n} > k \geqslant 0$, that n is a perfect square, and that $\sqrt{n} - k$ divides n, to ensure that the number of qubits in each row and column is an integer.

Note that the length of the longer edge can be written as

$$\frac{n}{\sqrt{n} - k} = \sqrt{n} + k + \frac{k^2}{\sqrt{n}} + O\left(\frac{k^3}{n}\right).$$

Hence, for H, the number of vertices is n and the number of edges is

$$e = 2\sqrt{n}(\sqrt{n} - 1) - \frac{k^2}{\sqrt{n}}\left(1 - \frac{k}{\sqrt{n}}\right)^{-1}.$$

If C is the minimum cut of G, then $f = \sqrt{n} - k$. Applying Proposition 1 to the graph H and the cut C then gives

$$\log \chi \geqslant \frac{\sqrt{n}}{2}\left(1 - \frac{k}{\sqrt{n}}\right)^{-1}$$

and

$$\#_g \geqslant n(\sqrt{n} - 1)\left(1 - \frac{k}{\sqrt{n}}\right)^{-1} - \frac{k^2}{2}\left(1 - \frac{k}{\sqrt{n}}\right)^{-2}.$$

Since $\frac{k}{\sqrt{n}} < 1$, we could expand $(1 - \frac{k}{\sqrt{n}})^{-2}$ and $(1 - \frac{k}{\sqrt{n}})^{-2}$ as Taylor series. This gives

$$\log \chi \geqslant \frac{\sqrt{n}}{2} \sum_{s=0}^{\infty} \left(\frac{k}{\sqrt{n}}\right)^s = \frac{\sqrt{n}}{2}\left[1 + \frac{k}{\sqrt{n}} + \frac{k^2}{n} + O\left(\left(\frac{k}{\sqrt{n}}\right)^3\right)\right]$$

and

$$\#_g \geqslant \sum_{s=0}^{\infty} \left[n(\sqrt{n} - 1) - \frac{k^2}{2}(s + 1)\right]\left(\frac{k}{\sqrt{n}}\right)^s.$$

[1] M. J. Bremner, R. Jozsa, and D. J. Shepherd, Classical simulation of commuting quantum computations implies collapse of the polynomial hierarchy, Proc. R. Soc. A **467**, 459 (2010).

[2] S. Aaronson and A. Arkhipov, in *Proceedings of the 43rd Annual ACM Symposium on Theory of Computing* (ACM, New York, 2011), pp. 333–342.

[3] J. Preskill, The theory of the quantum world, in *Proceedings of the 25th Solvay Conference on Physics, Brussels, 2011*, edited by D. Gross, M. Henneaux, and A. Sevrin (World Scientific, Singapore, 2013).

[4] E. Farhi and A. W. Harrow, Quantum supremacy through the quantum approximate optimization algorithm, arXiv:1602.07674.

[5] S. Boixo, S. V. Isakov, V. N. Smelyanskiy, R. Babbush, N. Ding, Z. Jiang, M. J. Bremner, J. M. Martinis, and H. Neven, Characterizing quantum supremacy in near-term devices, Nat. Phys. **14**, 595 (2018).

[6] A. W. Harrow and A. Montanaro, Quantum computational supremacy, Nature (London) **549**, 203 (2017).

[7] M. J. Bremner, A. Montanaro, and D. J. Shepherd, Achieving quantum supremacy with sparse and noisy commuting quantum computations, Quantum **1**, 8 (2017).

[8] S. Boixo, S. V. Isakov, V. N. Smelyanskiy, and H. Neven, Simulation of low-depth quantum circuits as complex undirected graphical models, arXiv:1712.05384.

[9] E. Pednault, J. A. Gunnels, G. Nannicini, L. Horesh, T. Magerlein, E. Solomonik, E. W. Draeger, E. T. Holland, and R. Wisnieff, Breaking the 49-qubit barrier in the simulation of quantum circuits, arXiv:1710.05867.

[10] S. Aaronson and L. Chen, in *Proceedings of the 32nd Computational Complexity Conference (CCC 2017)*, edited by R. O'Donnell (Schloss Dagstuhl–Leibniz-Zentrum fuer Informatik, Dagstuhl, 2017), pp. 22:1–22:67.

[11] R. Li, B. Wu, M. Ying, X. Sun, and G. Yang, Quantum supremacy circuit simulation on Sunway TaihuLight, arXiv:1804.04797.

[12] J. Chen, F. Zhang, C. Huang, M. Newman, and Y. Shi, Classical simulation of intermediate-size quantum circuits, arXiv:1805.01450.

[13] A. Bouland, J. F. Fitzsimons, and D. E. Koh, in *Proceedings of the 33rd Computational Complexity Conference (CCC 2018)*, edited by R. A. Servedio (Schloss Dagstuhl–Leibniz-Zentrum fuer Informatik, Dagstuhl, 2018), pp. 21:1–21:25, http://drops.dagstuhl.de/opus/volltexte/2018/8867.

[14] J. Bermejo-Vega, D. Hangleiter, M. Schwarz, R. Raussendorf, and J. Eisert, Architectures for Quantum Simulation Showing a Quantum Speedup, Phys. Rev. X **8**, 021010 (2018).

[15] A. Bouland, B. Fefferman, C. Nirkhe, and U. Vazirani, Quantum supremacy and the complexity of random circuit sampling, arXiv:1803.04402.

[16] A. M. Dalzell, A. W. Harrow, D. E. Koh, and R. L. La Placa, How many qubits are needed for quantum computational supremacy? arXiv:1805.05224.

[17] I. L. Markov, A. Fatima, S. Isakov, and S. Boixo, Quantum supremacy is both closer and farther than it appears, arXiv:1807.10749.

[18] R. Barends *et al.*, Digitized adiabatic quantum computing with a superconducting circuit, Nature (London) **534**, 222 (2016).

[19] J. Biamonte, P. Wittek, N. Pancotti, P. Rebentrost, N. Wiebe, and S. Lloyd, Quantum machine learning, Nature (London) **549**, 195 (2017).

[20] J. Biamonte, V. Bergholm, and M. Lanzagorta, Tensor network methods for invariant theory, J. Phys. A: Math. Gen. **46**, 475301 (2013).

[21] K. Fujii, H. Kobayashi, T. Morimae, H. Nishimura, S. Tamate, and S. Tani, Impossibility of Classically Simulating One-Clean-Qubit Model with Multiplicative Error, Phys. Rev. Lett. **120**, 200502 (2018).

[22] R. Orús and J. I. Latorre, Universality of entanglement and quantum-computation complexity, Phys. Rev. A **69**, 052308 (2004).

[23] V. M. Kendon and W. J. Munro, Entanglement and its role in Shor's algorithm, Quantum Inf. Comput. **6**, 630 (2006).

[24] J. D. Biamonte, J. Morton, and J. Turner, Tensor network contractions for #SAT, J. Stat. Phys. **160**, 1389 (2015).

[25] R. Orús, A practical introduction to tensor networks: Matrix product states and projected entangled pair states, Ann. Phys. (NY) **349**, 117 (2014).

[26] Z.-Y. Chen, Q. Zhou, C. Xue, X. Yang, G.-C. Guo, and G.-P. Guo, 64-qubit quantum circuit simulation, Sci. Bull. **63**, 964 (2018).

[27] T. Häner and D. S. Steiger, in *Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis* (ACM, New York, 2017), pp. 33:1–33:10.

[28] I. L. Markov and Y. Shi, Simulating quantum computation by contracting tensor networks, SIAM J. Comput. **38**, 963 (2008).

[29] https://github.com/Quantum-Machine-Learning-Initiative/Entanglement-QS, accessed 5 August 2019.

[30] S. S. Hong, A. T. Papageorge, P. Sivarajah, G. Crossman, N. Didier, A. M. Polloreno, E. A. Sete, S. W. Turkowski, M. P. da Silva, and B. R Johnson, Phys. Rev. A **101**, 012302 (2020).