10-nm Fin-width InGaSb p-channel self-aligned FinFETs using antimonide-compatible digital etch

10-nm Fin-Width InGaSb p-Channel Self-Aligned FinFETs Using Antimonide-Compatible Digital Etch

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***Abstract*—**We have fabricated self-aligned InGaSb p-channel FinFETs using a novel antimonide-compatible digital etch. This is the first demonstration of digital etch on InGaSb-based transistors of any kind. It has enabled the first fabricated InGaSb FinFETs featuring fin widths down to 10 nm and gate lengths of 20 nm. Single fin transistors with W_f = 10 nm and channel height of 23 nm (fin aspect ratio of 2.3) have achieved a record transconductance of 160 µS/µm at V_{DS} = 0.5 V. When normalized to device footprint, it reaches a record high g_m = 704 µS/µm. Digital etch has been shown to effectively improve the turn-off characteristics of the devices.

I. Introduction

Among III-V compound semiconductors, antimonide-based compounds such as InGaSb are promising material candidates for logic and high frequency devices, optoelectronics, and ultra-low-power transistors such as TFETs [1-4]. For electronics, antimonides feature a high hole mobility that improves with the application of compressive stress [5]. This makes this family of materials of interest for p-channel MOSFETs for future CMOS applications. A few demonstrations of p-type planar, fin, and nanowire MOSFETs have been published [6-12]. Nevertheless, progress in antimonide-based electronics has been slow. This can be partly explained by the challenging materials aspects of epitaxial growth and device fabrication due to the reactive nature of antimony-containing compounds.

In this work, we greatly advance the state-of-the-art of antimonide-based electronics by demonstrating deeply-scaled InGaSb p-channel FinFETs through a fully CMOS-compatible fabrication process. To achieve this, we have developed a new Sb-compatible digital etch which is controllable and benign, and we have perfected Ni ohmic contacts and fin RIE. We demonstrate the first InGaSb p-channel FinFETs with fin widths down to 10 nm and gate lengths down to 20 nm. These devices display record electrical characteristics.

II. Antimonide-compatible Digital Etch

One of the most critical challenges of InGaSb 3D device fabrication is the difficulty of performing digital etch (DE), a key process step in Si and InGaAs deeply scaled devices. DE is a process technique that separates the oxidation and oxide removal elements of conventional chemical etching enabling self-limiting nm-scale control. DE is essential to achieve devices with critical dimensions in the sub-10 nm range and also to remove RIE damage and passivate the fin/nanowire surface. Conventional DE using acids dissolved in water fails with antimonides due to their high reactivity. In a recent work [13], we demonstrated the first digital etch of InGaSb using oxygen plasma combined with HCl dissolved in alcohol. However, when attempting to make devices, we identified one important deficiency in this technique and that is material selectivity. Typical InGaSb-based devices include layers of arsenides and often contain aluminum compounds. It is very problematic if the DE etch rate shows a strong dependence on the different materials encountered in a device. This is unfortunately the case for the DE technique of antimonides. **Fig. 1** illustrates an InAs/InGaSb/AlGaSb nanowire. Alcohol-based DE produces an initial radial etch rate on the III-Sb of 1.0 nm/cycle, while the etch rate on the InAs portion of the nanowire is about 2.0 nm/cycle. To complicate matters, after 10 cycles, the average etch rate of the III-Sb portion of the structure is drastically reduced to about 0.21 nm/cycle, while all the InAs has already been etched away. Other authors have reported a similar much reduced etch rate of GaSb in water-based digital etch [3].

The issue lies in the oxidation properties of antimonides. For GaSb, strong oxidizing agents, like hydrogen peroxide, produce Sb_2O_5 in addition to Ga_2O_3, Sb_2O_3 and elemental Sb. Sb_2O_5 is insoluble in most acids or alkali [14]. Therefore, when enough Sb_2O_5 has been formed on the surface, digital etch stops. To address this issue, we have investigated digital etch by multiple combinations of oxidation and etch methods (**Fig. 2**). In the end, our study reveals that 3 min exposure in pure O_2 chamber at RT combined with 10% HCl:IPA etch for 30 s gives satisfactory results. **Fig. 3** shows the new DE process in action in the same heterostructure as in Fig. 1. A consistent radial etching rate of 2.0 nm/cycle for both InAs, InGaSb and AlGaSb is demonstrated. An issue worth noting is that AlGaSb is attacked and roughened after multiple cycles of DE, as shown in Fig. 3(d). Addressing this will require further studies.

III. InGaSb FinFET Fabrication

Fig. 4 shows the heterostructure utilized in this work. It is grown by MBE on (100) S.I. GaAs substrate. It features an $In_{0.25}Ga_{0.75}Sb$ channel with a thickness (H_c) of 23 nm. The buffer is $Al_{0.97}Ga_{0.03}Sb$ for high resistivity, with 50 nm liner-graded to $Al_{0.8}Ga_{0.2}Sb$ for reduced rate of oxidation when exposed, and also to yield a smooth channel interface. The p^+ cap features a composite InAs/InAsSb design [15] with a doping level of $3{\cdot}10^{19}$ cm^{-3}. There is a Be delta-doping layer with $5{\cdot}10^{11}$ cm^{-2} located 5 nm below the channel. **Fig. 5** shows the AFM and TEM cross-section measurements of the grown wafer. The surface mean roughness of the entire heterostructure and the $Al_{0.8}Ga_{0.2}Sb$ buffer surface is 1.29 nm and 0.65 nm, respectively. The interfaces are atomically smooth. **Fig. 6** summarizes key parameters of the grown wafer. The hole mobility is 1175 $cm^2/V{\cdot}s$. The buffer layer has high resistivity of $4.3{\cdot}10^6$ Ω·cm. From XRD, the InGaSb channel is found to be -1.09% compressively stressed.

Fig. 7 outlines the process flow for FinFET fabrication, and **Fig. 8** sketches final device cross-sections along and across the fin direction. First, the ohmic contact pattern is defined by e-beam lithography, and then Ni is e-beam evaporated and lifted off. The Ni contacts are then covered by a CVD SiO_2 spacer. The gate foot is next defined by EBL, followed by mesa photolithography and mesa SiO_2 RIE. The gate recess consists of two steps. The first 30 nm of the 35 nm p^+ cap are removed by timed Cl_2/N_2 dry etch. The rest is selectively etched in 10:1 citric acid:H_2O_2. This yields an undercut of the p^+ cap that is less than 20 nm, while maintaining a smooth top surface.

Fins are then patterned and RIE-etched using HSQ as the mask. Right after RIE, 1 cycle of the antimonide-compatible DE process described above is performed, followed by 3.5 nm ALD Al_2O_3 gate dielectric at 175°C. 60 nm of Al is sputtered as gate metal, and the gate head is defined by Ti/Au patterning and Al RIE. Finally, 30 nm of SiO_2 spacer is deposited and pads are formed following via photolithography and etching. The process results in a gate that is self-aligned to the p^+ cap. The HSQ fin mask remains till the end of the process, resulting in a double-gate FinFET structure. The Ni ohmic contact is unintentionally alloyed during the backend CVD step at 300°C.

Devices with L_g ranging between 20 nm and 1 μm and W_f between 10 nm and 100 nm were fabricated. The chip contained single-fin transistors as well as arrays with 25, 50, or 100 fins in parallel.

Fig. 9 illustrates the fin etch technology developed in this process which represents an improvement over what was demonstrated before [7]. The test structure comprises of 50 nm InAs on GaSb. RIE was performed by ICP $BCl_3/Ar/SiCl_4$ plasma at 250°C, 280 W RF platen power and 20 W ICP power. Smooth and vertical sidewalls are obtained with a fin width down to 15 nm, a marked improvement over [7] where the InAs layer was roughened during dry etch. Here, simultaneous etching of antimonides and arsenides is achieved without roughening any of the surfaces.

Fig. 10 shows ohmic contact resistance, measured by circular TLM test structures on the heterostructure in Fig. 4. The inset shows R_c obtained by Mo, W, and Ni contacts as a function of annealing temperature. Ni ohmic contacts annealed at 350°C for 3 min yield a record contact resistance of 22.3 Ω·μm, which corresponds to an ultra-low contact resistivity of $4.6 \cdot 10^{-9}$ Ω·cm^2. This R_c is a factor of 4X better than our earlier demonstration [15] and it arises from the use of a composite p+ cap design and a higher doping level ($3 \cdot 10^{19}$ vs. $1 \cdot 10^{19}$ cm^{-3} in [15]).

Fig. 11 shows an SEM image of a finished device. **Fig. 12** shows TEM cross sections of the fin structure of a completed device demonstrating a fin width of 10 nm, fin height of 115 nm and a channel aspect ratio (AR = H_c/W_f) of 2.3. The fin sidewall angle is 84° and the fin pitch is 100 nm.

IV. RESULTS

Fig. 13 shows the electrical characteristics of the most aggressively scaled InGaSb single-fin MOSFET with W_f = 10 nm and L_g = 20 nm. A peak g_m = 160 μS/μm and a lowest S_{lin} = 260 mV/dec are obtained. Characteristics of a 100 fin array device with W_f = 10 nm and L_g = 1 μm are displayed in **Fig. 14**, showing good saturation behavior. Unless indicated otherwise, all the FOMs are normalized by the total conducting periphery of the gate ($2H_c \cdot N_f$).

Scaling behavior of our devices is shown in **Fig. 15** and **16**. Maximum transconductance extracted at V_{DS} = -0.5 V shows well-behaved dependence on L_g and W_f. V_T extracted at V_{DS} = -50 mV shows mitigated V_T rolloff with fin-width scaling. **Figs. 17-18** shows the measurement of R_{on} (at V_{GS} = -1 V), and extraction of fin resistance R_f and access resistance R_{SD}. The expected scaling behavior of R_f and R_{SD} as $\sim 1/W_f$ is observed.

The demonstrated devices, even at long channel, show insufficient turn-off characteristics. Nevertheless, the results here represent a significant improvement over earlier InGaSb FinFETs [6] due to the new DE technique. To illustrate its role, **Fig. 19(a)** shows the impact of DE on the subthreshold characteristics of otherwise identical transistors. Without DE, turn-off is very poor. A single DE cycle yields a drastic improvement with the residual current dropping more than two decades. This illustrates the ability of DE to reduce sidewall RIE damage. Additional cycles of DE worsen the off-state behavior. This could be attributed to the fact that AlGaSb buffer is easily oxidized and damaged, especially during the oxidation process of DE, consistent with what we observed in **Fig. 3(d).**

The residual off-state current that is left after 1 DE cycle in Fig. 19(a) is due to buffer leakage. This is shown in **Fig. 19(b)** that shows the subthreshold characteristics of long-channel devices with fin width ranging from 100 nm to 14 nm. All devices were treated with 1 DE cycle. Below a fin width of 22 nm, the turn-off behavior remains unchanged. Test devices with no InGaSb channel but gated AlGaSb fins show that there is a residual leakage path underneath the channel which is responsible for the improper off-state behavior. This is likely due to the etched and exposed AlGaSb buffer which is easier to be oxidized than InGaSb forming a surface conduction leakage path. Alleviating this will require structural device innovations, such as lateral suspended or vertical device structures.

Fig. 20 benchmarks g_m vs. W_f among published InGaSb p-MOSFETs, normalized in two ways. When normalized by the conducting gate periphery, as in Fig. 20(a), a record g_m of 268 μS/μm is exhibited at W_f = 46 nm and V_{DS} = 0.5 V. The maximum g_m drops as W_f decreases, as in InGaAs FinFETs [16]. When g_m is normalized by the footprint of the fin, as is relevant for high-density FinFETs, the 10 nm fin width devices demonstrate a high g_m/W_f = 704 μS/μm (**Fig. 20(b)**).

V. CONCLUSIONS

Highly scaled InGaSb p-channel FinFETs with smallest fin width of 10 nm, fin AR > 2 and L_g=20 nm are demonstrated for the first time. These results are enabled by a new antimonide-compatible digital etch technique. Record results are demonstrated across a broad range of W_f and L_g. This work not only highlights the potential of InGaSb p-channel multigate MOSFETs, but also pushes significantly the state-of-the-art of antimonide fabrication technology for general applications in which the antimonide-based compounds can shine.

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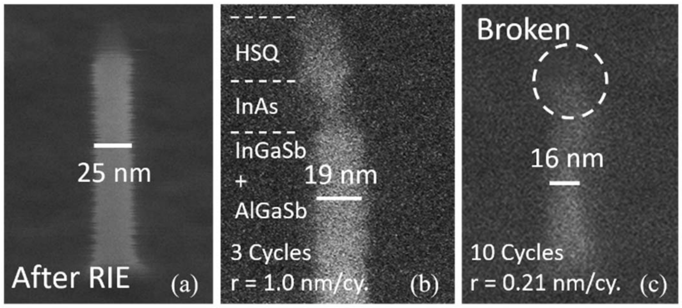

Fig. 1. (a) InAs/InGaSb/AlGaSb vertical nanowire after RIE with initial diameter of 25 nm, and after (b) 3 cycles and (c) 10 cycles of digital etch in O_2 plasma and HCl:IPA. Noted are the average radial etch rates of the InGaSb/AlGaSb portion of the nanowires.

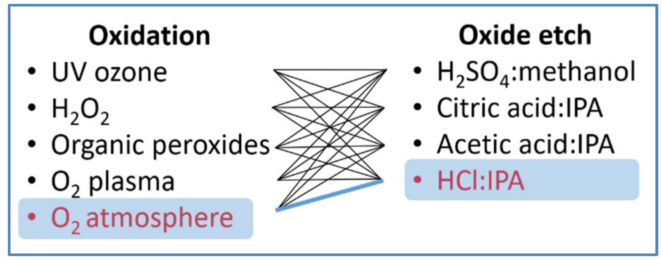

Fig. 2. A survey of digital etch techniques tested, by combining various oxidation methods and oxide etch solutions. Those marked in blue gave the best results.

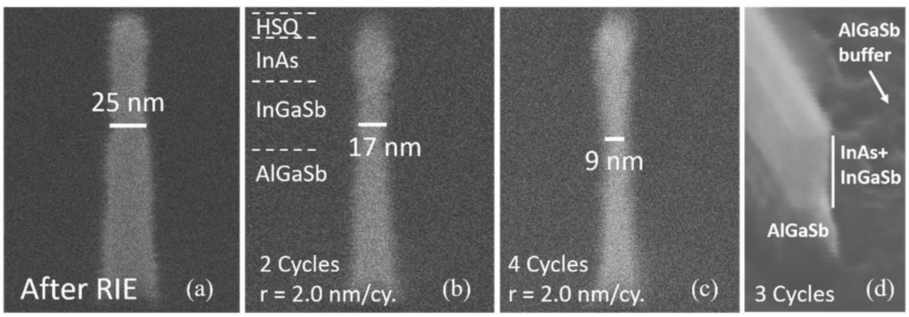

Fig. 3. (a) InAs/InGaSb/AlGaSb vertical nanowire after RIE with initial diameter of 25 nm, and after (b) 2 cycles, and (c) 4 cycles of digital etch in O_2 atmosphere and HCl:IPA showing stable and uniform etching rate. (d) Fin structure after 3 cycles of DE showing non-uniform sidewall and surface etching of the AlGaSb portion of the structure.

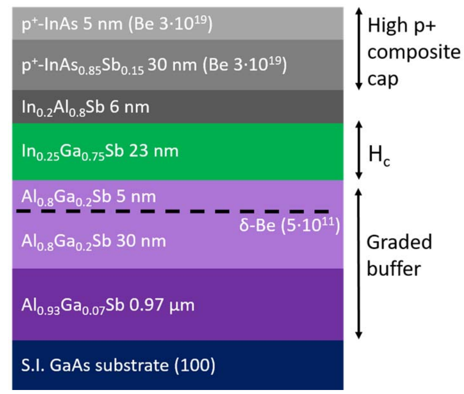

Fig. 4. Starting heterostructure for InGaSb p-channel FinFET fabrication.

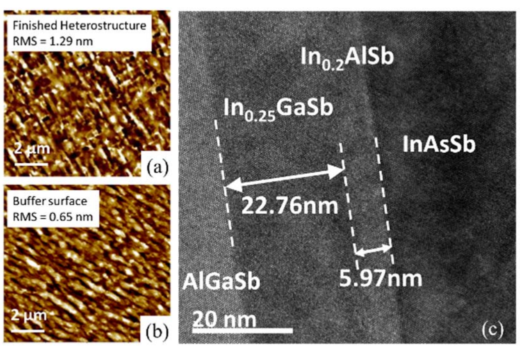

Fig. 5. AFM image of (a) as-grown MBE heterostructure and (b) of the surface of the graded buffer structure. (c) TEM lattice image of the channel and spacer region of the heterostructure.

N_s (cm^{-2})	$3.7 \cdot 10^{12}$
μ_h @ 300K (cm^2/V·s)	1175
μ_h @ 77K (cm^2/V·s)	2521
Channel resistivity (Ω·cm)	$3.6 \cdot 10^{-3}$
Buffer resistivity (Ω·cm)	$4.3 \cdot 10^{6}$

Fig. 6. Summary of electrical properties of the InGaSb heterostructure.

- HCl clean, Ni ohmic contact
- CVD SiO_2 contact spacer
- Gate EBL, SiO_2 dry etch
- Mesa photo, SiO_2 dry etch
- Gate recess I: p+ cap timed RIE
- Gate recess II: p+ cap selective wet etch
- Fin EBL, $BCl_3/Ar/SiCl_4$ dry etch
- Antimonide-compatible digital etch
- ALD Al_2O_3 gate dielectric, 175 °C
- Al gate sputtering
- Gate head photo and patterning
- CVD SiO_2, via photo and RIE
- Pad formation

Fig. 7. Process flow for InGaSb FinFETs.

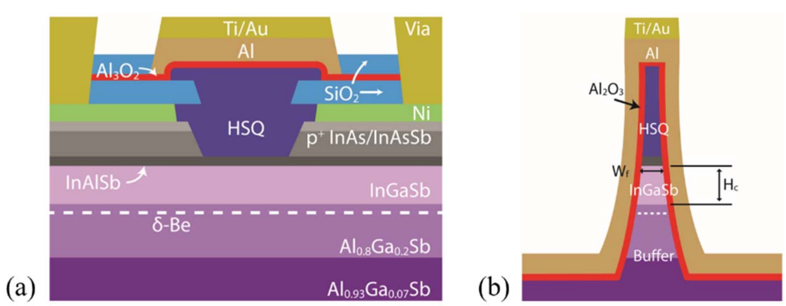

Fig. 8. Schematic of FinFET cross-sections (a) along the fin and (b) across the fin.

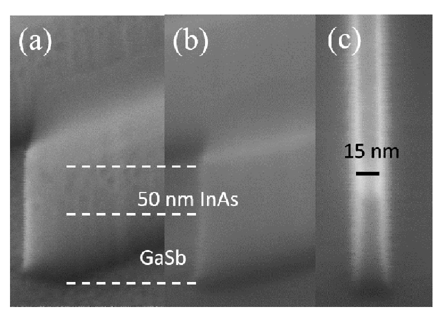

Fig. 9. SEM micrographs of RIE-etched InAs/GaSb fins following the recipe of (a) [7], and (b), (c) this work.

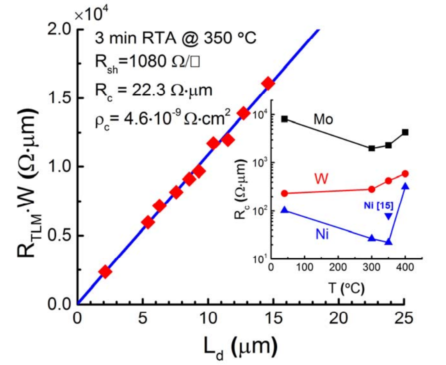

Fig. 10. Ni ohmic contact resistance on this heterostructure. Inset: R_c benchmark of Mo, W and Ni ohmic contacts and earlier results [15].

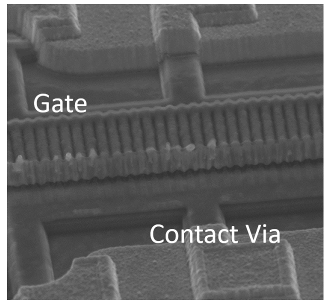

Fig. 11. SEM image of a finished InGaSb FinFET.

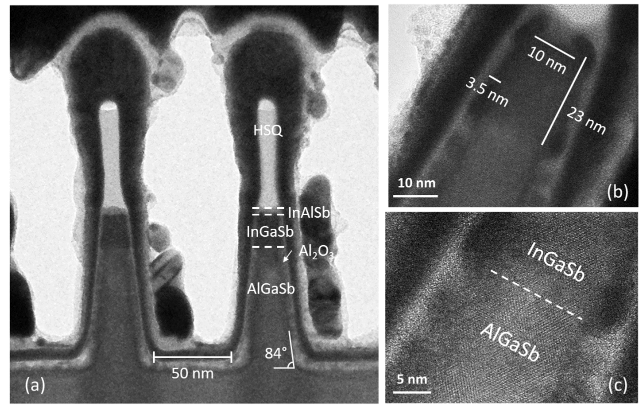

Fig. 12. HR-TEM images of finished InGaSb FinFET with fin width of 10 nm, fin aspect ratio of 2.3, and 3.5 nm Al_2O_3 gate dielectric.

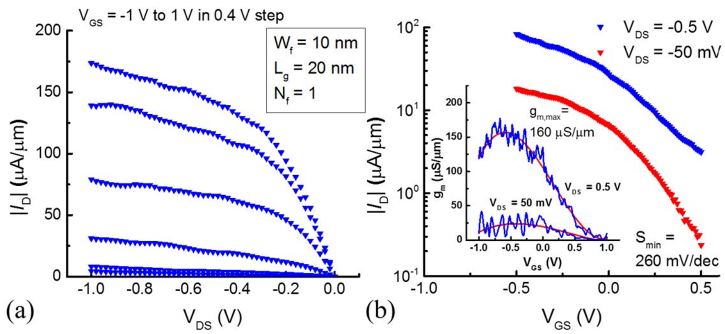

Fig. 13. (a) Output characteristics of InGaSb single-fin device with W_f = 10 nm, L_g = 20 nm; (b) subthreshold characteristics of the device. Inset: transconductance characteristics of the device, with peak g_m = 160 µS/µm.

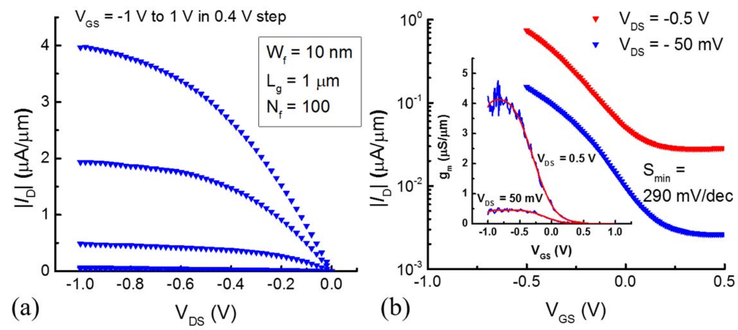

Fig. 14 (a) Output characteristics of InGaSb long channel array FinFET with W_f = 10 nm, L_g = 1 µm, N_f = 100; (b) subthreshold characteristics of the device. Inset: transconductance characteristics of the device.

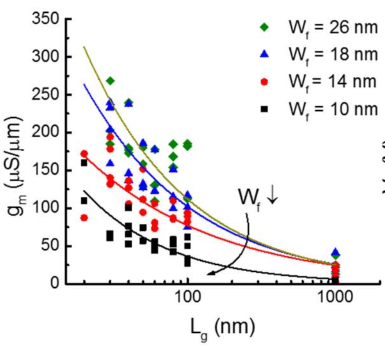

Fig. 15. Impact of W_f and L_g scaling on maximum g_m at V_{DS} = -0.5 V.

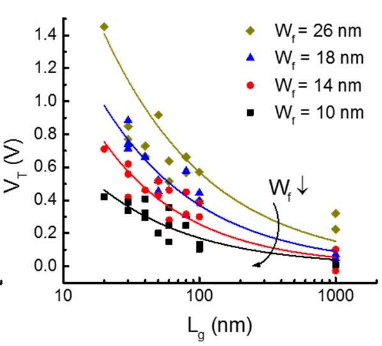

Fig. 16. Impact of W_f and L_g scaling on V_T at V_{DS} = -50 mV.

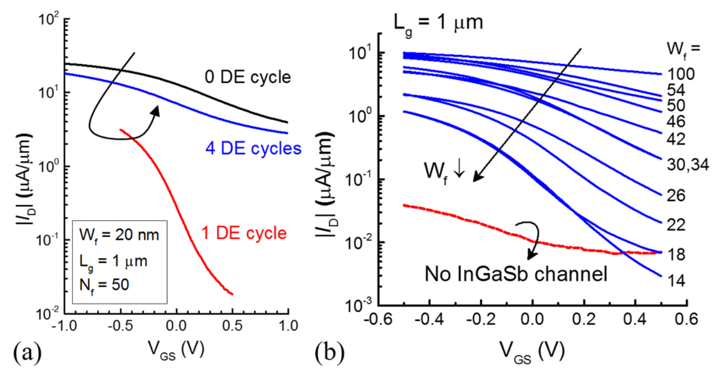

Fig. 19. (a) Subthreshold characteristics of FinFETs with the same final W_f = 20 nm, after 0, 1, and 4 digital etch cycles. (b) Subthreshold characteristics of FETs with various W_f and L_g = 1 µm, and test device with identical geometry but no InGaSb channel (1DE cycle in all).

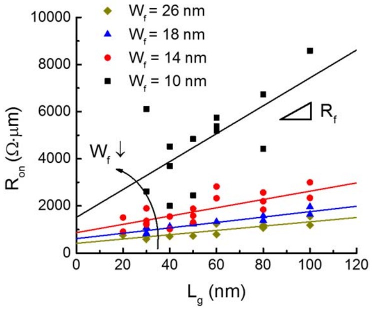

Fig. 17. ON resistance of devices with various W_f at V_{GS} = -1 V.

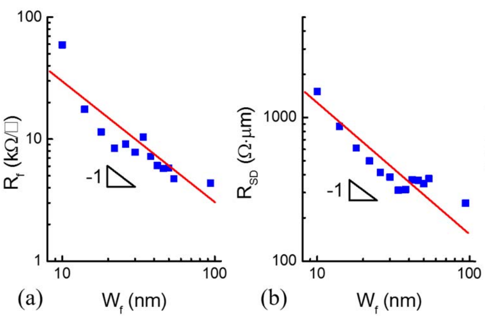

Fig. 18. Extracted (a) fin sheet resistance vs. fin width, and (b) access resistance vs. fin width.

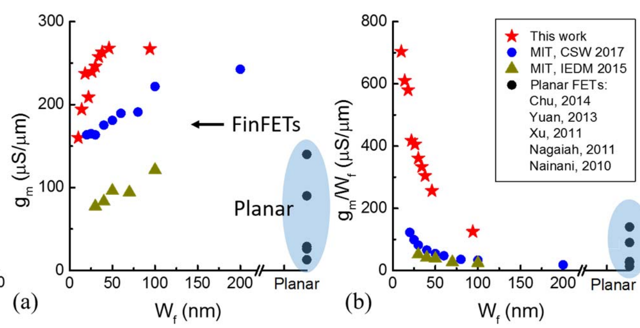

Fig. 20. Benchmark of maximum g_m vs. W_f for InGaSb FinFETs and planar MOSFETs. (a) g_m is normalized to the total conducting periphery. (b) g_m is normalized by fin footprint. The red stars represent the present work.