Material and Fabrication Developments in the Ion-Electrospray Propulsion System

by

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Submitted to the Department of Aeronautics and Astronautics in partial fulfillment of the requirements for the degree of

Master of Science in Aeronautics and Astronautics

at the

Massachusetts Institute of Technology

May 2020

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Abstract

In this thesis, new materials, microfluidic control devices, and fabrication techniques were developed in support of the ion electrospray propulsion system (iEPS) developed by MIT's Space Propulsion Lab. MEMS fabrication techniques are reworked to increase yield reliability of the thruster frames. The focus of this work is on propellant management, increasing thrust density, system robustness, and reducing cost of thruster production. Altered fabrication process steps have led to reliable 100 percent yields. A large focus of improving iEPS thrusters is tied to preventing premature wetting of the thruster emitter with propellant and adding the ability to modulate flow on command. The development of a flow-regulating solid-state valve using similar fabrication methods facilitates this. Initial designs and fabrication trials are explored alongside the underlying physics of operation.

Additionally, a new monodisperse, sintered porous silica ceramic was developed for use in emitter substrates. The highly-modifiable, photocurable ceramic resin used to cast the emitter substrates is a strong contender to replace the state-of-the-art borosilicate glass chips. An experimental new material emitter was tested to gain a voltage-current relation as well as time-of-flight spectroscopy. This new silica ceramic demonstrated promising tip geometry after laser ablation, good wetting characteristics, and excellent current emission in the purely ionic thruster operation mode.

Thesis supervisor: Paulo C. Lozano

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Acknowledgements

To begin, I would like to take the chance to thank Professor Paulo Lozano. He has been an indispensable graduate adviser throughout my time at MIT. His passion for the work we do and the students who work under his positive leadership have made it a pleasure to learn and work in the Space Propulsion Lab.

SPL is made great by the fantastic minds that inhabit its walls. To thank everyone who has had a positive impact on my life in the lab would make for a rather long read. Regina Apodaca was, without a doubt, the best desk-mate anyone could ask for. Our incessant search for late-night free food events throughout the semesters have forever changed my BMI. Elaine Petro provided a level of enthusiasm and optimism not commonly seen in post-docs. Every moment working with her, was a privilege not soon to be forgotten. Colin, Ximo, Andrew, Oliver, you guys are alright too I guess. Also to my UROPS, the work discussed in this work was directly enabled by your countless hours making experimental ceramic resins and thruster components.

To the best friend group anyone could ask for, FGC, I could not have enjoyed a second of my time at MIT without you all. In no favorite order: Allen, Katie, Lena, Mark, Regina, Faisal, Beldon, and Maya, you all are bedrock-level friends who's generosity knows no bounds. Thank you.

To even have the chance to be writing an acknowledgement section, I needed to have parents that pushed the importance of pursuing the challenging things in life. Your five dollar "good report card" bribes clearly had an effect.

I have also had the sincere pleasure to have had numerous mentors, both academic and in the field, who have taught me the importance of teamwork and the worth of simplicity in design. Cold gas propulsion will forever hold a place in my heart because of this.

Lastly, a thesis is only as good as its professional editor. Haley Biermann, your keen eye for my flaws in person and on paper keep me humble and happy!

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1 Introduction

With the proliferation of small satellite launches in recent years, specifically CubeSats as secondary payloads on rockets, components are becoming smaller, denser, and more modularized. Many of these satellites do not carry propulsion, but in the future adding this capability would allow them to extend their application domain to enable more ambitious missions.

1.1 The lack of efficient small satellite propulsion

When discussing rocket propulsion, it is best to start with Tsiolkovsky's rocket equation:

$$\frac{m_0}{m_f} = \exp\left(\frac{\Delta v}{c}\right) \tag{1}$$

This foundational equation exponentially relates the ratios of final spacecraft mass to its initial mass after a propulsive burn to gain some Δv and exhaust velocity c. Unless the maneuver needed must be done in a very short period of time, then it stands to reason that maximizing exhaust velocity would greatly improve total payload mass allowable for a spacecraft. For the aforementioned modular (10cmx10cmx10cm units) CubeSat, there is no small footprint, low power, and high-efficiency propulsion option outside of miniaturized conventional chemical propulsion systems. While these platforms are cheaper to build, their lack of attitude control poses a major restriction on mission capability. This lack of small satellite maneuverability is where the ion Electrospray Propulsion Systems really begins to shine.

1.2 Enter electrospray propulsion

In simple terms, ion electrospray propulsion operates via application of a high voltage between an "extractor" electrode and an ionic liquid propellant, from which, ions are accelerated to very high velocities for thrust. They are a class of electrostatic propulsion system not needing magnetic confinement. They are perhaps most unique in the sense that they do not produce a plasma in order to extract ions, but rather evaporate the ions

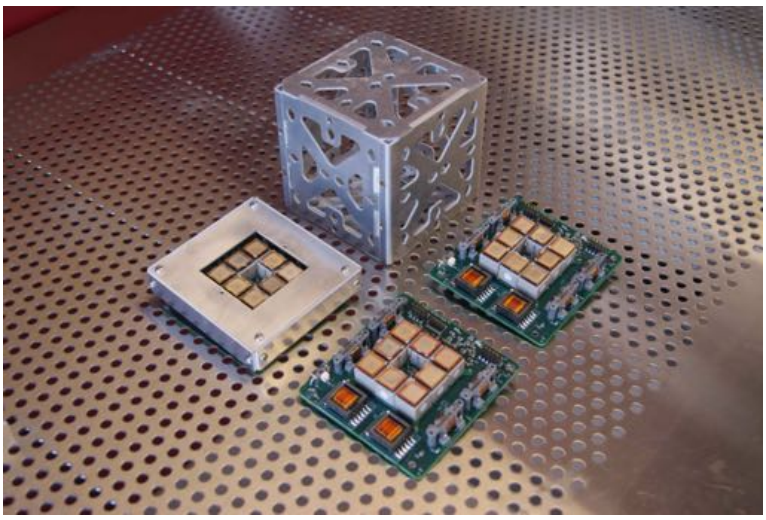

Figure 1: A 1U (1000cm^3) CubeSat with iEPS modules.

in the ionic liquid via very strong electric fields localized around small emitter tips where the ionic liquid is present. The iEPS thrusters discussed in this thesis are passively-fed (no conventional valves or pressurized systems) ionic liquid into tips formed out of a porous substrate. Due to the nature of ionic liquids, application of a electric field pulls the liquid into the conical emitter tips. At the very top of the emitter tips, the propellant forms a microscopic meniscus where the electrostatic forces are strong enough to overcome surface tension and pull the ions out where electrostatic forces take hold. The ions fall through the potential difference and follow the field lines, accelerating away from the emitter to provide thrust from each tip. The exhaust velocities currently attainable fall in the tens of thousands of meters per second, given specific impulse ranges from 1000-2000 seconds.

The development work discussed in this thesis builds off of work by Dakota Freeman and his final iEPS revisions, which in turn, are based on those who came before. The current design of the iEPS thruster package and its components is touched on in Section 2. Alterations to the thruster frame and valve design as well as a new flow regulating valve are discussed in Sections 3 and 4. MEMS fabrication is heavily utilized in the production of iEPS thruster components, therefore Section 5 serves to acquaint the reader with specific processes and terminology referenced in Section 6. Section 6 details the various fabrication steps to each of the thruster components and process changes

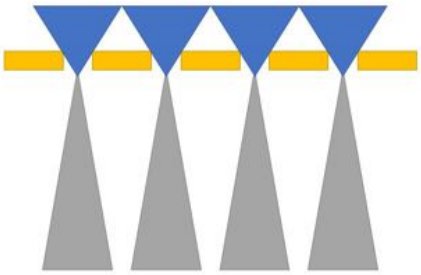

Figure 2: iEPS thruster operational diagram. The porous tips are shown in gray, the extractor in gold, and the ion beam in blue (although the actual ion beam is not visible to the naked eye.)

from previous component fabrication processes. Section 7 overviews a parallel material development effort to produce a new porous, monodisperse silica ceramic for use in emitter fabrication. The final section, Section 8, reviews the test firing of a thruster utilizing this new emitter material.

2 Current iEPS Thruster Package Design

Over the years of electrospray thruster research in SPL, the design of the final thruster package has evolved dramatically. The following section serves to outline the most current thruster package components and their general order of fabrication and assembly.

2.1 iEPS v3 thruster components

This section serves to summarize the current thruster components and their respective manufacturing approaches. Components discussed include the thruster frame, extractor, valve, and flow controller, which will be outlined in further detail in their respective sections and in the component manufacturing section. Full process flows for each of these can be found in the appendices.

2.1.1 Thruster frame

The frame is the structural component for the thruster that both serves to mount and align the extractor and emitter. It is also serves as an interface between the propellant tank and the emitter chip. The thruster is fabricated using MEMS fabrication techniques and is comprised of three wafer layers: a silicon base layer "L1"; a glass insulating layer "L2"; and a third silicon alignment layer "L3". The insulating glass L2 layer is crucial to the operation of the thruster, as it allows a high potential to be applied between the emitter chip and extractor without immediately shorting across the frame. It has several features that are important to thruster assembly as well.

There are several important regions of the frame to note. First, the outer frame border supports the corner posts. It is a thick border to bolster the strength of the components mounted to it and to counter the brittle nature of silicon. Testing this strength of this new frame showed great promise, as the frame broke consistently before the bond failed under 4.2 kg of load. This is shown in Figure 4.

Next, the inner frame region is dimensioned to support the emitter chip. A gap between this portion of the frame and outer border adds some deterrence for any ionic liquid that may leak out of the emitter chip from straying towards to extractor via the posts. The

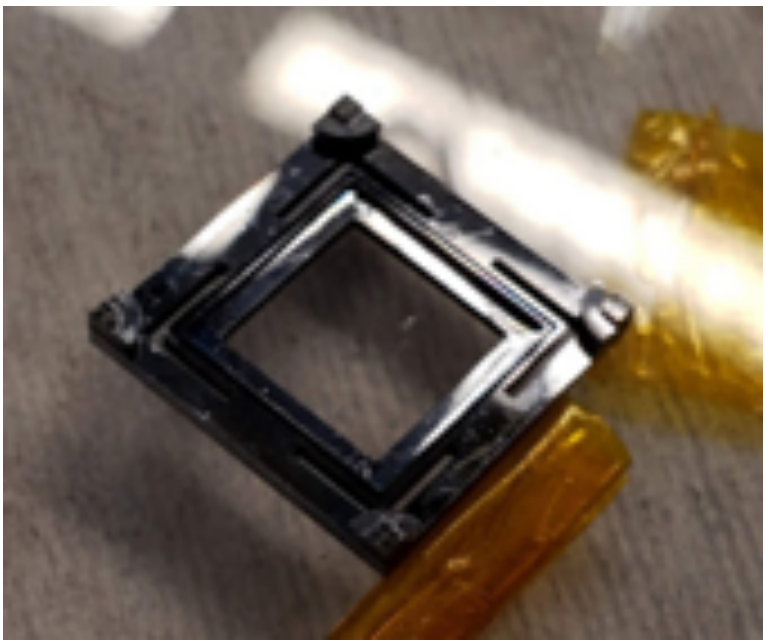

Figure 3: iEPS v3 frame

open area at the center of the frame is referred to as the port. It is sized to seat on the propellant tank and allow propellant to reach the emitter chip directly. The bridge of the frame is the connection between the inner and outer frame borders. It offers further protection against liquid making its way from the inner to outer frame regions. The final features are the posts and alignment marks. The posts serve as a physical interface between the frame and the extractor. They also have small alignment crosshairs for alignment when it comes time to laser ablate the tips into the emitter substrate. An additional feature of the posts is in the L2 glass layer. An isotropic wet etch forms a knife edge feature that restricts liquid travelling up the post to the extractor by keeping it pinned in the event a leak does occur. This edge shape is shown (although not as concave as in most physical frames) in Figure 5.

2.1.2 The emitter

The emitter is where the all the excitement of electrospray propulsion begins. It is typically comprised of a porous borosilicate glass used for filtration systems, although this work will further discuss newly developed materials to replace borosilicate glass.

Figure 4: iEPS v3 frame bond strength testing

Figure 5: Frame cross section. Green is the silicon base layer "L1," Gray is the glass insulating layer "L2" with a knife edge to retain liquid, and red is the silicon alignment layer "L3."

Using a lapping wheel, the chips are polished to be exactly in line with the frames alignment posts. This ensures that the highest point of the soon-to-be laser ablated tips are at the level of the extractor to be mounted on top of the posts. The chips are first bonded to the frame using a vacuum rated epoxy. Following this, the tips are then formed using a solid-state picosecond laser providing light at a wavelength of 248 nm. The glass, which absorbs UV light efficiently, is quickly ablated by the energy of the incoming light. Utilizing a square grid for laser passes, the tips are carved out of the monolithic emitter chip while the debris is vacuumed away to avoid fusing to the surface or interfering with the laser.

Following laser ablation, the tips often have small debris that may cause unintended

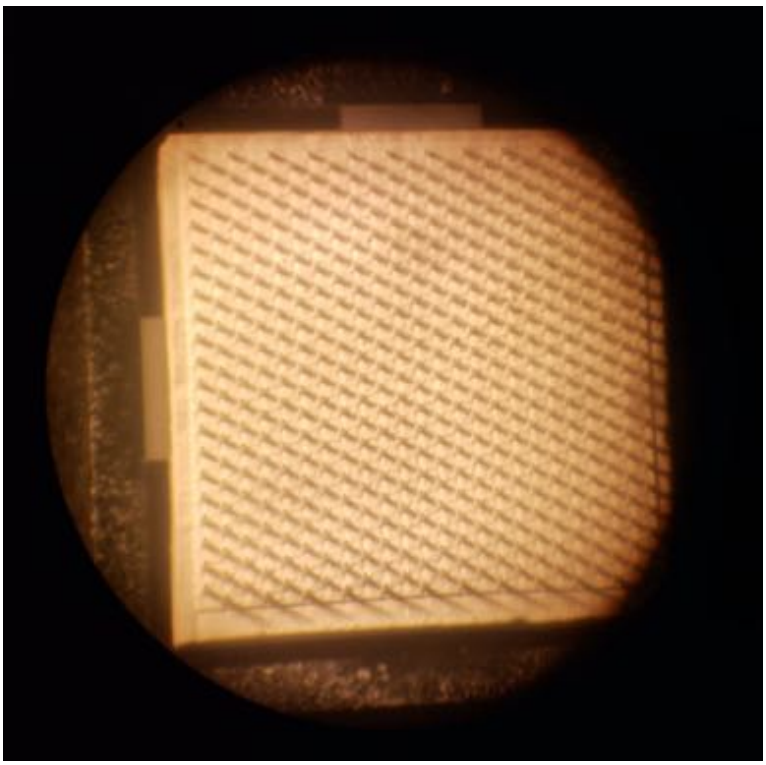

Figure 6: Thruster emitter after laser ablation.

droplet emission or possible liquid bridge formation site. These imperfections are removed by hand. Given the distance between tips is a mere 450 μm, this process is quite precarious. A small tungsten needle and single hair brush are used to dislodge material and and the brush is used to sweep the debris away without removing any formed tip. Lastly, the emitter is coated on all sides except the back a with a thin hydrophobic layer to reduce the risk of premature emitter flooding during storage and launch.

2.1.3 The extractor

In order to produce ion emission for thrust, a bias is needed across the emitter. Depending on which mode of operation desired, the extractor is the anode or cathode opposite the emitter. The extractor electrode is made from a silicon-oxide-insulator wafer (silicon wafer with buried oxide layer within) using MEMS fabrication techniques. This wafer type, paired with processing, to be discussed in later sections, enables very thin apertures a mere 350 μm or smaller in diameter. These apertures, via the frame posts, are aligned directly with the newly formed emitter tips. The apertures are sized to allow for

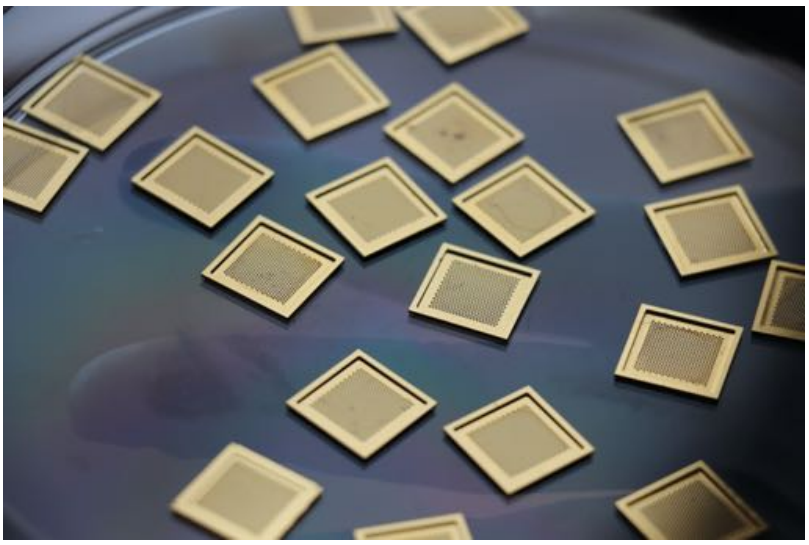

Figure 7: Several extractor electrodes.

minimal "intercepted current" from the emitters. This means that to an ion evaporating off of the emitter tip meniscus, it barely sees the extractor, and therefore, does not impact it on its trajectory out of the thruster. It was found that 40 μm thin extractor apertures were actually too thin from a structural standpoint, so an 80 μm extractor thickness is used with an added isotropic etch to reduce possible ion interception. A gold coated extractor atop an emitter and propellant tank cap is shown in Figure 7.

The extractor is first coated in titanium before an additional layer of gold is deposited. This titanium layer acts as a "glue" between the silicon wafer and gold coating. This gold layer serves the purpose of preventing oxide growing on the extractor while in atmosphere as well as providing a conductive surface to spread any intercepted current from the ion beams. By providing this dispersing ability via the gold coating, any excess current, Joule heating, or physical sputtering that may cause damage to bare silicon is mitigated more effectively. While gold has served its function well, it is not the only material capable of accomplishing the above requirements. It is simply a very easily accessible material for MEMS processing.

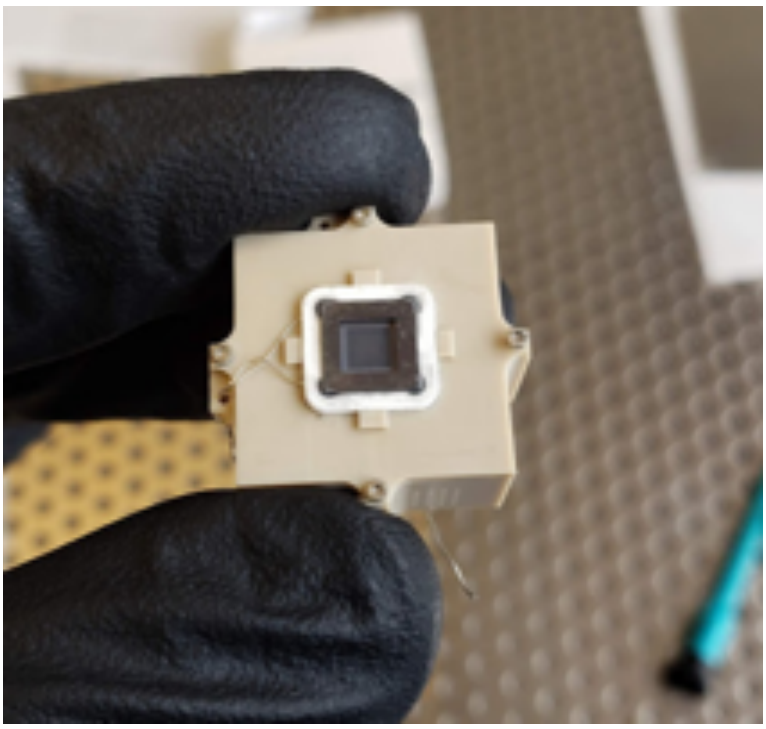

Figure 8: Assembled tank with electrowetting valve and beaker on top.

2.1.4 The valve

As may be shown and referenced lightly in this section, there is a solid state valve that sits beneath the emitter/frame component and atop the tank cap component. It acts as a barrier for propellant entry prior to thruster operation. It is discussed in much greater detail in the valve and flow regulator section of this thesis.

2.1.5 The tank cap

Mounting the finished thruster to a propellant tank required a simple interface. The tank cap was designed to accomplish this while adding structural strength to the overall thruster package. This cap is shown holding a teflon beaker and thruster valve in Figure 8.

The emitter/frame component is mounted above the valve which is in turn mounted to the tank cap on a raised ledge to further elevate the thruster frame and emitter above any potential leaked liquid. A second step is provided by a teflon beaker insert that holds a solid state valve and sits in the port of the emitter and frame assembly,

centering it with respect to the cap. A final small step in the teflon beaker insert allows for any excess epoxy used to bond the emitter to the cap to freely flow outward and not into the port where the wicking material lies. If epoxy were to make it into the port, the thruster may have serious liquid wicking problems during operation, if it even can fire. The cap is then fitted to the propellant tank.

2.1.6 The propellant tank

The propellant tank consists of PEEK (polyetheretherketone) shell for structural purposes and a machined teflon subtank that actually holds the ionic liquid. This is a useful material for a variety of reasons. The choice of teflon was simple due to its unreactive chemical nature, ionic liquids are safely stored in it for long durations. Additionally, its high temperature resistance as a fluoropolymer (roughly 250°C) makes it a strong performer in the space environment. Although the propellant reservoir is a lightly porous structure, it is quite malleable. This is why the outer PEEK shell component was added. PEEK is much more rigid than teflon, offers suitable UV resistance, and can withstand very high temperatures that a space operating environment may provide (low density plasmas for instance).

2.1.7 Distal electrode

Both anode and cathode are required to extract ions and establish an operational current. In earlier electrospray thruster research, using the emitter chip as the opposite electrode to the extractor seemed logical. However, it was demonstrated to be far less than ideal. Electrochemistry proved to be a serious concern during operation for the emitter-extractor pairing. By nature, ionic liquids can be effective electrolytic etchants to many materials. With the emitter acting as one of the electrodes, it is very likely that electrochemistry initiated during operation would erode the tips over time. A separate distal electrode made of carbon xerogel was placed away from both the extractor and emitter inside the propellant tank itself. This permits any electrochemical wear to occur far away from the much more delicate geometries in the thruster. One such electrode is shown in Figure 9. [3]

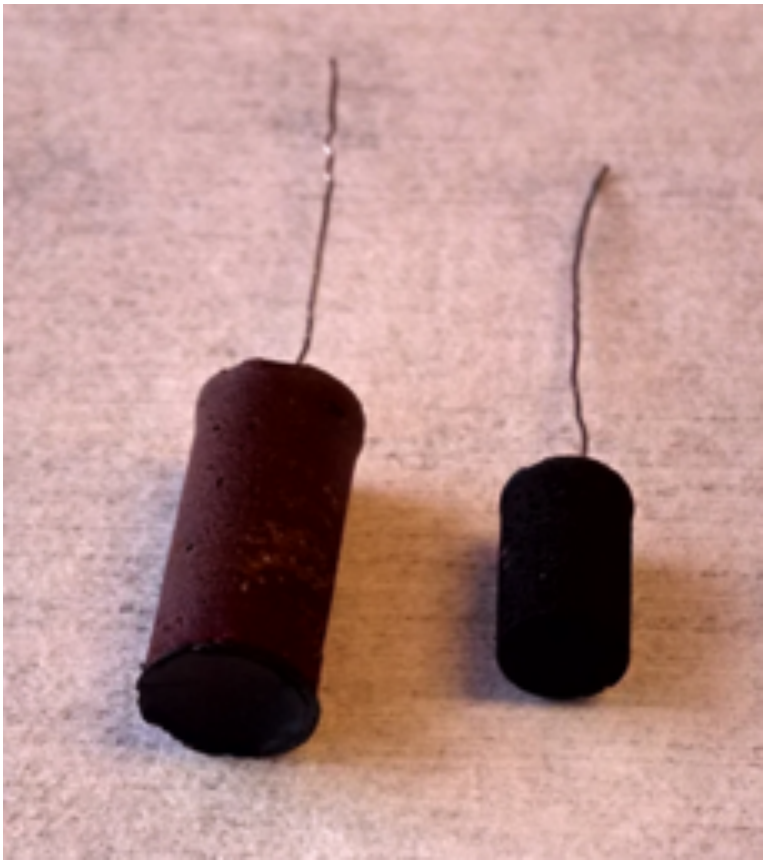

Figure 9: The three stages of the electrode assembly. The left-hand electrode has not yet been pyrolyzed, which causes the electrode to shrink and carbonize. [14]

The carbon xerogel is also used for wicking propellant to the emitter via its porous structure. The electrode wire is made of platinum because of its low reactivity and very high melting point and resistance to oxidation being during the pyrolizing step of making the electrode itself. All this to say that material selection is crucial when making passively fed electric propulsion systems.

While later sections further detail in depth, the component fabrication and final assembly of the thrusters, here is a brief overview of the birth of an electrospray thruster:

1. Fabricate the L1, L2 and L3 wafers and bond them together in the clean room to form a frame stack.
2. Fabricate the valve wafer in the clean room.
3. Fabricate the extractor electrode wafer (also a clean room process).
4. Dice the frame stack, valve, and extractor wafers into individual components.
5. Either make porous silica emitter substrates or procure porous borosilicate substrates to be polished and flattened.
6. Adhere the emitter substrate to the thruster frame and further polish any additional substrate material down to the frame alignment marks.
7. Laser ablate the emitter tips from the substrate.
8. Fabricate the distal electrodes.
9. Clean and remove any imperfections from the newly formed emitter tip arrays.
10. Coat the emitter arrays to provide hydrophobic protection layer.
11. Align and adhesively bond the extractor to the frame via the posts and alignment features. Precision alignment will be done under a microscope before adhesive cures.
12. Coat the valves in a hydrophobic fluoropolymer layer and sputter coat one edge to metallize.
13. Bond the valve to the tank cap.

14. Adhesively bond the finished thruster to the tank cap.
15. Thread the fill port to 4-40 to accept a post-filling plug.
16. Fit the tank into the PEEK tank shell with the distal electrode and its wire fitted.
17. Align and compress the tank assembly and thruster carefully.
18. Screw the the tank shell together with 000-120 screws.
19. Fill the subtank with ionic liquid via syringe.
20. Close the subtank with a 4-40 teflon plug in the recently threaded fill port.
21. Snap the baseplate of the tank shell into place routing the electrode wire through the center hole in the plate.
22. Wrap the electrode wire into a compressed coil in the recessed area in the back of the tank shell back cap.
23. Place the fully assembled thruster/tank package onto the PPU for final soldering and mounting.

Again, this a simple summary of the order of fabrication and assembly of an iEPS thruster. The individual component fabrication steps and detailed material production steps are outlined in later sections of this thesis.

3 iEPS Thruster Frames

3.1 Concerns over the previous design

3.1.1 IEPS v3 frames

The previous iteration of electrospray thruster frames created significant variation in the amount of current produced around the emitter. [12] The most likely issue was determined to be that the propellant reaches the emitter tips on the edges of the chips (at a greater distance) slower than the center. Darcy's law describing the flow through a porous medium states

$$Q = -\frac{\kappa A(p_b - p_a)}{\mu L}$$

where the flow rate Q is related to the permeabilty κ of the medium it is flowing through, the cross-sectional area A, the viscosity μ, the pressure drop, and the travel distance L. It is seen that the flow rate should be inversely proportional to the distance. In the case where ion current produced by the thruster is similar to the maximum flow rates possible, it will naturally be capped where the hydraulic impedance is greatest. This just so happens to be the edges of the emitter. To circumvent this limitation, a new frame structure was developed to allow the ionic liquid to come in contact with the full back side of the emitter area, thus ensuring that the flow rate will not be the limiting factor at the edges. This uniform propellant dispersion is achieved by etching a recessed well into the inner square area of the frame, which permits a spread of ionic liquid across the back emitter surface. This secondary volume of ionic liquid is analogous in function to that of a plenum in a conventional propellant system. The recessed area is then packed with filter paper that forces an even dispersion of ionic liquid to the emitter chip. [14]

3.1.2 Bond line alteration

Previous iterations of the thruster frames suffered from inconsistencies in the bond interface between the frame and emitter chip. The adhesives used would often flow over the edge of the frame and react with UV and become brittle, causing premature failure of the adhesive. To combat this issue, a small channel feature was added to the bond

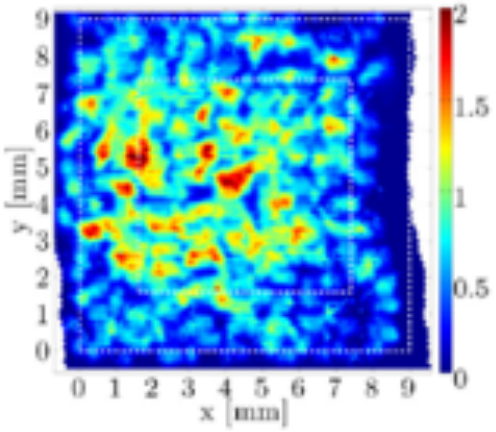

Figure 10: Inhomogeneous current emission from an emitter, reproduced from Guerra-Garcia *et al.*

region of the frame. This feature both increases the bonding area for the adhesive and prevents overflow of epoxy over the frame edge. The increase in area is necessary due to the propellant well feature that was just discussed.

3.1.3 Batch yield issues

Prior to this work, typical batch yield of V2 thruster frames containing all four corner alignment posts and pedestals was about 60 percent. The most recent v3 frame yield improved to approximately 85 percent with increased L1-L2-L3 bond area. Given that the final stage of the frame fabrication process requires dicing of the wafer with a die saw, significant stress is applied to the small corner post structures. The die saw is essentially a thin abrasive blade spinning at 30 kRPM requiring constand water flow to remain cool while cutting the wafer. If the corner post bonds are at all weak, this step will make that known, effectively ruining the frame for flight use. In addition to utilizing a slightly larger bond area in the v3 design, new cleaning and bonding techniques were employed to give a total frame yield of 100 percent, with only a single frame losing one post due to handling. A primary concern with this process is the fact that the silicon-glass-silicon frame stack is the opposite of the more common silicon sandwiched between glass wafers. [4] This has proven to be an issue when bonding the alignment L3 and insulating L2 layers, as delamination between these layers is typically where the corner post failure occurs most frequently. This concern was mostly alleviated through

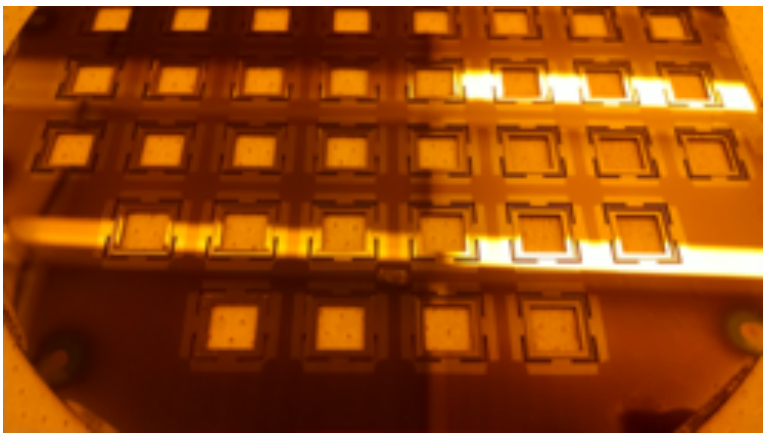

Figure 11: A revised L1 wafer. The well and moat features are clearly visible; the diffraction pattern at the edges of the wafer is produced by the clamps that hold the wafer to the chuck in the DRIE tool and have no effect on the functionality. [14]

careful changes to current limiting during anodic bonding and using chemical cleaning of the wafer followed by nitrogen drying within an hour of bonding. It is hypothesized that charge relaxation in a final polarity reveral of the L2-L3 bond also contributed to higher yield, ensuring that no spot welds were significant enough to allow the current to flow, and the whole contact area would anneal. The most recent bonds have proven to be resilient to most all clumsy handling cases, and the addition of the extractor to the posts via an epoxy bond, further increases the stability of the corner structure.

3.2 Fabrication process changes

Following work in [14], frame fabrication changes to improve ease of fabrication and overall yield were sought out. The most current frame base layer version is shown in Figure 11.

The primary focus was on improving the bond interface between the frame layers. Namely, the pedestal area. This was implemented through altering the photolithographic processes and cleaning steps. This process would ensure cleaner and slightly enlarged anodic bonding surfaces and better post-dicing yield of the full frames. All of these process changes will be discussed in the thruster component fabrication and photolithographic fabrication sections.

3.3 New frame materials

While MEMS fabricated thruster frames have proven to be very reliable and sturdy, they take a significant amount of time to fabricate. An initial trial run of 3D printed frames showed good promise. Utilizing the space-rated Cyanate Ester SLA printable resin, a few v3 iEPS frames modified for print stability were made for testing. The minimum feature size was 25 micron, allowing for all critical dimensions to be captured adequately. The result of these printing trials is shown in Figure 12.

Figure 12: iEPS v3 SLA printed frames made of Cyanate Ester (left) shown with emitter chip (center) and extractor (right).

4 The Electrowetting Flow Regulator

4.1 Motivation

The robustness of the iEPS thrusters was drastically increased with the inclusion of a solid-state electrowetting valve. This valve proved to be capable of holding back propellant until the thruster was ready for operation. One caveat with the design of this thruster was its single-use nature. Once the valve was actuated, it could not de-wet the emitter. Thus, the next logical progression for this technology was to develop a multi-use flow-controlling valve to eventually replace it. The design elements required were to keep the robustness of the prior valve while adding the ability to regulate propellant flow to the thruster.

4.2 The electrowetting valve

A valve based on the electrowetting principle was developed to fulfill the prescribed requirements. [14] The concept behind the electrowetting valve requires little modification to the existing thruster architecture. It utilizes the polar nature of ionic liquids and their forced wetting properties, which allows it to wet an otherwise hydrophobic surface given an applied electric field. [5] The design consists of an array of through-holes etched in a 200 μm silicon wafer to form capillaries. Once diced, each valve is then coated in a plasma-enhanced chemical vapor deposition (PECVD) machine with a fluoropolymer layer, with the approximate structure $C_2F_{3.5}$ not unlike Teflon. The thin hydrophobic film is capable of preventing EMI-BF_4 from entering the capillaries during launch conditions. Controlled liquid intrusion of the non-wetting layer and activation of the valve is achieved by applying an electric potential, polarizing the ionic liquid and forcing it to wet the coating [5]. The high contact angle of a liquid (water in this case) droplet deposited on top of a finalized valve can be seen at the left of Figure 13. The right figure shows a scanning electron microscope (SEM) image of a few of the through-holes.

The contact angle (θ) between a liquid of surface tension γ and a dielectric surface of thickness d can be modified with the application of an electric potential (V), according to the Young-Lippmann equation, where ϵ_0 is the permittivity of vacuum:

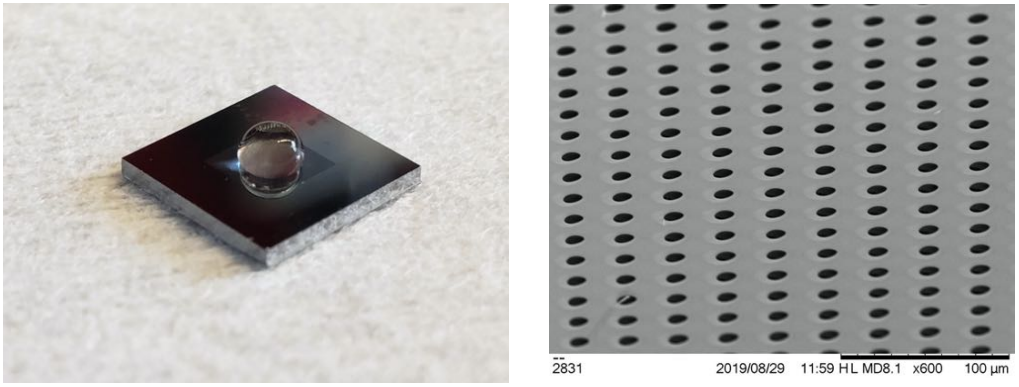

Figure 13: Left: Electrowetting valve displaying its hydrophobic nature with a water droplet. Right: An SEM image of an array of through-holes

$$\cos\theta_0 = \cos\theta - \frac{\epsilon_0\epsilon}{2\gamma d}V^2 \tag{2}$$

At sufficiently high voltage, the liquid can be forced to wet the dielectric surface. Notice the equation above predicts a voltage at which perfect wetting ($\theta = 0$) can be achieved. In practice, saturation occurs at some finite contact angle. The objective then is to design a system in which the contact angle changes from a non-wetting ($\theta > 90°$) to a wetting ($\theta < 90°$) condition. The final valve design consists of a matrix of through-holes etched in a silicon wafer. Each valve has a thermally grown silicon dioxide layer (dielectric constant ϵ_1, and thickness d_1) and is then coated via CVD with a non-wetting fluoropolymer film (ϵ_2, d_2). A thin polytetrafluoroethylene (PTFE) coat is capable of preventing the propellant to enter the through-holes under launch loads. It is worth noting, other hydrophobic materials are capable of accomplishing this too. The dielectric constant (ϵ) in Eq. 2 can be corrected as the two films are in series and have constant thickness via:

$$\frac{\epsilon}{d} = \left(\frac{\epsilon_1}{d_1} + \frac{\epsilon_2}{d_2}\right) \tag{3}$$

To confirm the dependence of contact angle on applied voltage, a bare silicon surface

coated in the non-wetting fluoropolymer film was utilized. A small droplet of water was placed on the center of the sample. One side of the piece with exposed silicon was used to ground a high-voltage power supply. The positive electrode from the supply was connected to a thin conductive wire placed in the water droplet without touching the silicon. The bias was increased between the droplet and the silicon in 5 volt increments up to 100 volts. This droplet experiment is shown in Figure 14. Contact angle begins at greater than 90 degrees, but decreases to 90 and surpasses the wetting threshold as voltage increases. The critical wetting voltage was measured to be approximately 40 volts. This is shown in the plot in Figure 15. [15]

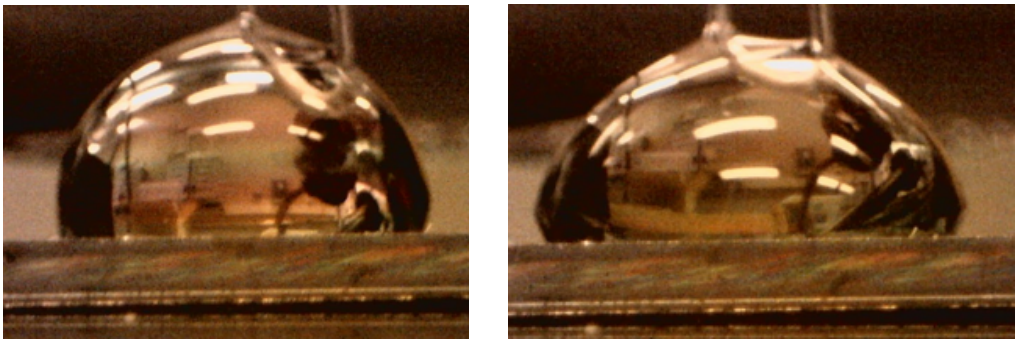

Figure 14: Electrowetting droplet test; left is droplet with 0 Volts applied and right is with 40 V applied.

This method of measuring contact angle is very similar to the method used to test the valve activation shown in Figure 16.

4.3 Design requirements

Work on the solid state flow controller, evolved from development of the electrowetting valve that adhered to the following criteria:

1. Be simple to actuate and allow the passage of ionic liquid in a known time in a reliable manner.

2. Be relatively simple to integrate into the existing architecture with a minimum of modification.

3. Resist the intrusion of ionic liquid for an arbitrary amount of time, sitting undis-

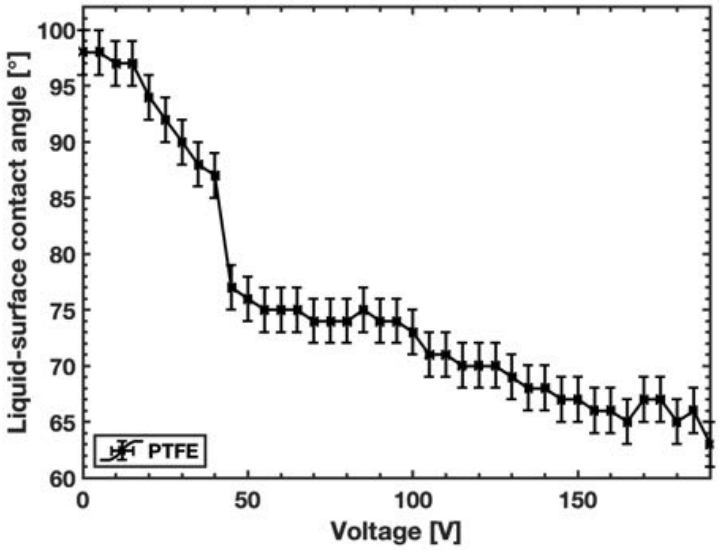

Figure 15: Plot of droplet contact angle measured along horizontal vs applied voltage between droplet and silicon.

turbed at room temperature and pressure.

4. Resist the intrusion of ionic liquid under harsh vibrational and pressure loading such that the system would experience at launch.

[14]

The flow controller must be able to meet these criteria while also adding the ability to wet and de-wet upon voltage application.

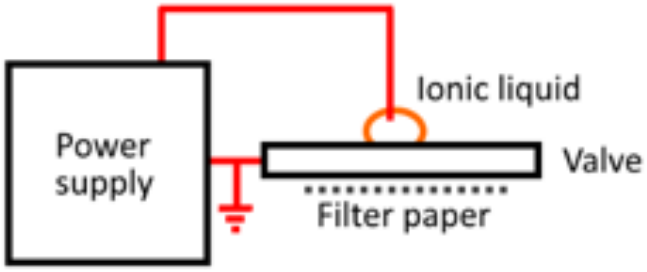

Figure 16: Setup for preliminary valve tests.

4.3.1 Simplicity of actuation

This requirement states that the flow controller usage must be straightforward. Flip a switch, the flow controller opens and allows ionic liquid through to the thruster. Flip off the switch, and the ionic liquid ceases to reach the emitter. It must be a reliable and quantifiable process to be usable for flight applications. Just like the previous valve, there must be a very rigid set of standards that enable a user to know the valve is functioning (perhaps, after a few minutes at 50 V, when the time-integrated current has reached a predetermined "wetting" value) or have a method of detecting the wetting (perhaps, an exposed bridge that, once wetted, would show a continuous circuit indicating presence of ionic liquid.)

4.3.2 Simplicity of integration

This requirement is strictly to mitigate unnecessary re-design of current thruster components and enable easy integration. This means that the dimensional footprint of the flow controller, or of the pieces used to accommodate it, cannot be altered from their original design. Additionally, whatever the final method of activating the valve and regulating flow, the alterations to the power processing unit (PPU) cannot require a re-design. The reason behind both of these points is simple: the PPU and thruster structural components are far more mature than that of the new flow controller. It would be unreasonably difficult to make design changes, enact them, qualify the new hardware, and maintain a launch-priority schedule. For simplicity, the same footprint as the previous generation of single-use electrowetting valve will be used. The layout of the new valve/flow controller (and old valve) in a thruster is shown in Figure 17.

4.3.3 Passive robustness

Prior to launch, the unit will be subject to an array of not-so-careful conditions. It is, therefore, crucial that the flow controllers be capable of withstanding long-term wetting of ionic liquid. This should include a verification via static test in ambient storage conditions, for at least a few weeks. This will prove that the lip feature still functions as a barrier to passive failure modes.

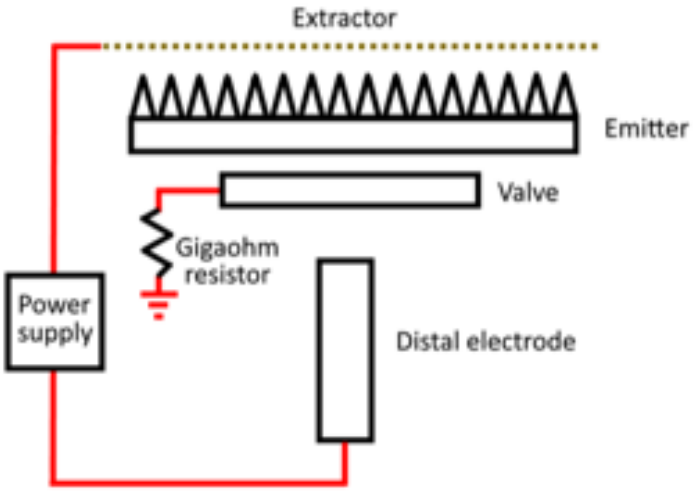

Figure 17: Diagram of valve integration into thruster. The valve is grounded via a resistor in case there is electrical contact between the ionic liquid.

4.3.4 Active robustness

Upon launch, the combination of the sudden pressure drop and the vibration is a recipe for inducing leaks. If there is any gas dissolved into the propellant (although care was taken to prevent this) it will come out of the solution as the pressure drops, maintaining the raised pressure inside the tank and causing liquid to be forced into any small gaps. This process occurs in the same way that the increased volume in the passive case could also cause failure. Therefore, the flow controller must be able to withstand this depressurizing/vibration regime in conditions similar to the launch. An oxide "lip" feature is carried over from the previous electrowetting valve design to pin the liquid upstream of the capillary. This feature ensures the capillaries will not wet prior to applying voltage. As will be discussed further in the fabrication portion of this thesis, this oxide lip can be quite difficult to get just right (see Figure 18.)

4.4 The electro-wetting flow controller

With minimal alterations to the already-proven electrowetting valve, development of the new flow controller began with focus on the capillary array architecture. The wetting capability of the oxide-lipped capillary array was already known to work, therefore the "wetting" function was no big hurdle. The "de-wetting" function is crucial for the

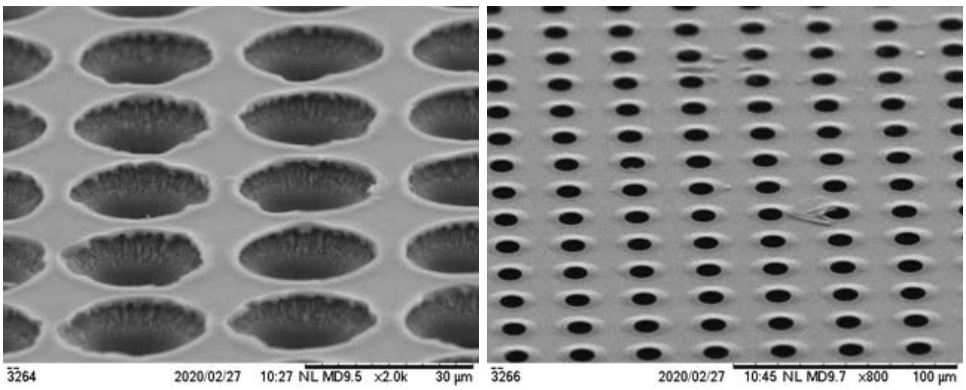

Figure 18: Valve lip used to pin liquid. Left: Oxide damaged by isotropic over-etch. Right: Undamaged lip; note the difference in scale.

following reasons:

1) When the liquid arrives at the porous emitter material, surface tension forces alone have the ability to force the liquid such that the meniscus contour between individual emitter tips can potentially become flooded, causing a short. This effect has been demonstrated in a laboratory setting and it will likely be more severe in the zero-g environment of space, with the loss of gravity as a controlling force in favor of preventing this. This flooding phenomenon is a slow moving process and relies on the contact angle of the ionic liquid with the substrate material. However, it is frequent enough during long thruster idle periods that a way to prevent it from occurring is needed. The single-use electrowetting valve is unable to address these idle period.

2) When the current version of the thruster is firing, flow is regulated by the suction force of the applied voltage and the device's hydraulic impedance alone. A useful operational capability would be added if that propellant flow rate could be controlled by means other than fixed hydraulic impedance and electric field effects. This would enable the current as well as the thruster exhaust composition to be optimized for a set performance. Having a variable flow controller during operation would allow for this tunability.

The concept of an electrowetting flow controller is effectively adding a liquid bridge feature to the existing electrowetting valve architecture. Once the valve is activated, the capillary array connects to a series of horizontal, open channels etched on the upper

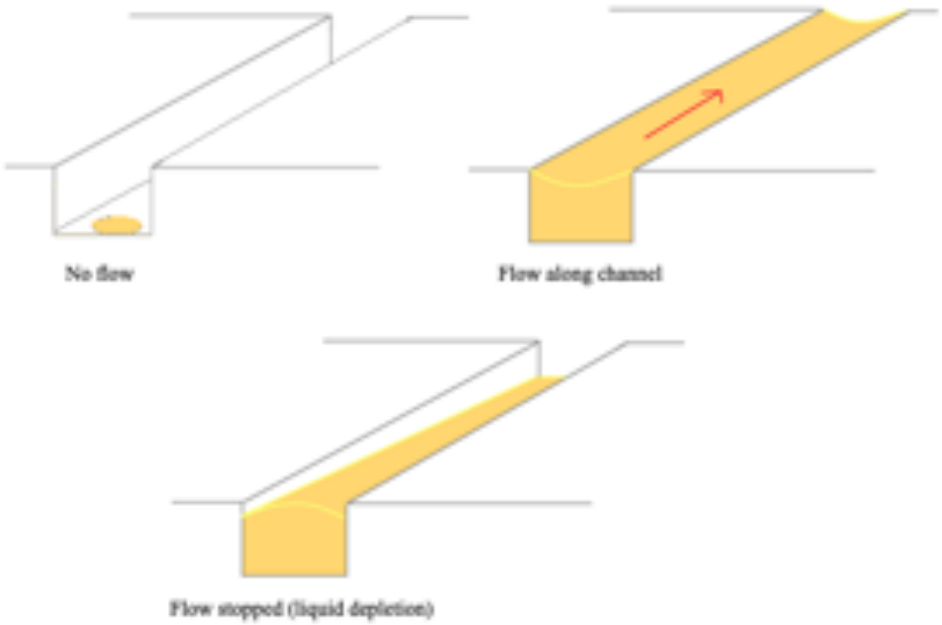

Figure 19: Conceptual operation of the electrowetting valve/flow controller. The liquid is shown in orange. Shown left to right and top to bottom: before actuation (liquid pinned in capillaries), after first actuation with channels filled up and with bias removed, the liquid in the channel is depleted.

surface of the device. These micro channels transport the liquid to the opposite end of the device surface, away from the side with the capillaries. A wicking material then transports the liquid from this side and brings it to the porous substrate emitter sitting on top of the valve for firing. Both the binary control and flow control is provided by these horizontal open channels. A cross section diagram of one such channel during these operational regimes is shown in Figure 19.

Figure 19 depicts the cross-section of one of many liquid transport channels during three stages of operation. Prior to voltage application (initial wetting), the liquid remains in the tank and the capillaries are dry. The pressure inside of the ionic liquid is altered via the electrowetting phenomena changing the contact angle. Once the capillaries are wetted in the same manner as in the electrowetting valve, the meniscus will be pinned at the edge of the capillary. The pressure inside of the filled capillary is constant. In the open microchannels, the pressure depends on the liquid curvature. For wetting, the pressure is negative and sucks liquid in. For non-wetting, a bias is applied causing the

pressure to become positive and push the liquid out of the channel. Once at this state, the liquid transport to the emitter ceases and the emitter tips can no longer be flooded by the aforementioned capillary forces, thus mitigating that potential failure mode. This reversible change from a wetting to a non-wetting condition, provides the desired on/off valve effect. This effect is imposed by a sub-micron thick hydrophobic fluoropolymer layer applied to the valve's exterior surfaces via plasma enhanced chemical vapor deposition (PECVD). The flow controlling feature is achieved by varying the amplitude of the applied voltage to manipulate the meniscus contact angle from 90 degrees down to the critical wetting angle value. Doing so effectively controls the channel's resistance which can be set to match a desired flow rate value, effectively making the device a flow regulator and valve in a single unit. While this all sounds quite complex in operational terms, the MEMS unit designs are quite simple, as will be discussed.

4.4.1 Initial flow controller design

The critical design factors for the electrowetting flow contoller include number of capillaries, size of capillaries, channel width, channel height, channel placement, and number of channels. The footprint of the previous electrowetting valve provided an initial constraint to build from. The same silicon wafer-based MEMS fabrication approach was used. The capillaries needed to be on side of the chip while the channels carried the capillary-supplied liquid to the other end of the chip where a wicking material would transport the liquid to the porous emitter. Two initial designs were created for fab development. One included one hundred thousand capillaries while a second one included a minimum of twenty-thousand capillaries (where no flow impedance would naturally hinder the thruster firing when "open".) These two designs are shown in Figures 20 and 21. The intended design would utilize MEMS (microelectromechanical systems) fabircation techniques similar to those required for the rest of the thruster components.

4.4.2 Revised design

Following initial fabrication trials, it was determined that a larger wick area would be required to ensure proper wetting of the emitter chip. This forced the wick retaining

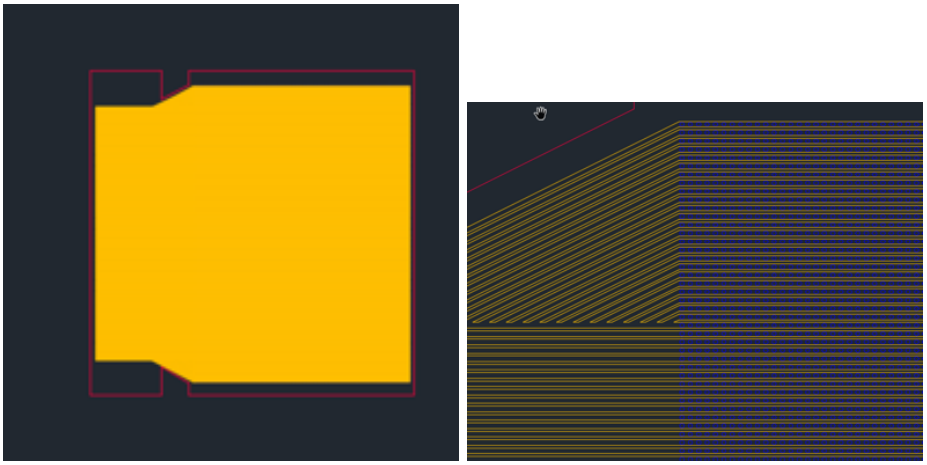

Figure 20: Initial design of photolithographic mask for the electrowetting flow controller with one hundred-thousand capillaries. Image on the right shows blue capillaries aligned with yellow channel walls.

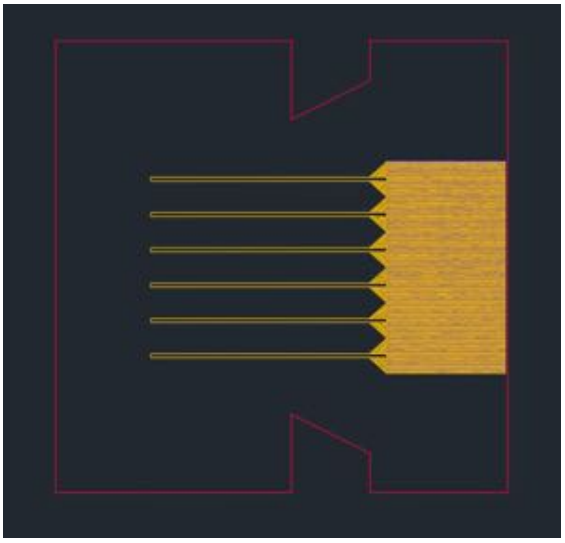

Figure 21: Initial design of photolithographic mask for the electrowetting flow controller with twenty thousand capillaries.

walls back towards the dicing line, further restricting the number of capillaries. Insights into channel alignment with the capillaries were taken into consideration as well. Therefore, two variants of the channel layouts included a half-channel-width offset relative to the capillaries to study this effect in testing. To minimize complexity of the first flow controllers, the combined channels were removed in lieu of straight channels for each row of capillaries. Additionally, the channel wall thickness was increased to be 10 microns marginally. This is due to the need for thermally grown oxide layer to prevent dielectric breakdown during operation. This oxide layer (2 microns thick) would have changed the electrowetting properties for the originally 5 micron wide channels by pseudo-blunting of the wall geometry. Lastly, the wick retaining walls were given sharp corner geometries in an attempt to further reduce the possibility of stray liquid from roaming to areas it should not. This is similar in nature to the oxide lip feature, in that the liquid meniscus becomes "pinned" at sharp corners. The revised mask design are shown in Figures 22 and 23.

The fabrication of all thruster components, including the electrowetting valves and these flow controller chips, is elaborated on in greater detail in the subsequent sections.

Following final dicing and fluoropolymer deposition, it is necessary to coat one edge in metal. This is a legacy feature of the electrowetting valve. An in-house sputter coater and valve holding jig is used to metallize valve edges. This enables soldering a lead to the valve that can then be connected to the control board for use.

Figure 22: Revised design of photolithographic mask for the electrowetting flow controller with eighty-thousand capillaries.

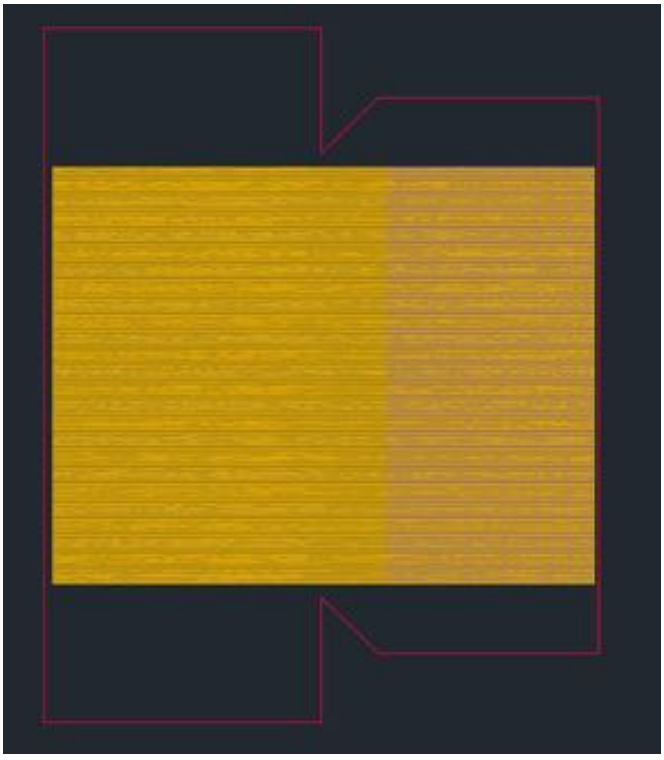

Figure 23: Revised design of photolithographic mask for the electrowetting flow controller with twenty-thousand capillaries.

5 Microfabrication

5.1 Techniques utilized in MEMS

5.1.1 Typical process steps

Most MEMS and semiconductor fabrication processes share many techniques. For electrospray thrusters, the end product is strictly mechanical in nature, therefore, material altering procedures are unnecessary. For every electrospray component, the general fabrication steps look similar to the following:

1. Examine blank wafers for damage or defects that would hinder further fab.
2. Clean wafers and deposit oxide via CVD or thermal growth.
3. Spin coat wafers with photoresist, a photocurable polymer, expose desired development patterns to UV source.
4. Pattern the oxide via wet or dry etch methods. This step (and patterning the bare silicon) can be repeated to "nest" patterns for complex designs.
5. Etch the developed pattern(s) into the silicon wafer.
6. Strip the photoresist and any unwanted oxide via chemical cleaning.
7. Dice the wafer into desired components.

While this is a simple overview of the steps, a more detailed discussion of each step follows.

5.1.2 Silicon Oxidation

In nearly all semiconductor fab processes, oxide is the first step. This is primarily due to the nature of silicon dioxide being quite opposite in a material aspect to bare silicon. It is a very effective insulator. Per micron deposited, it takes approximately 1 kilovolt to cause dielectric breakdown. This is very useful for selective doping processes. For the strictly mechanical fab processes relevant to iEPS thrusters, the oxide provides a very resilient "mask" for high aspect-ratio etch work, both wet and dry. As an example, during directed reactive ion (DRIE) etching, selectivity ratios of 200:1 or better can be

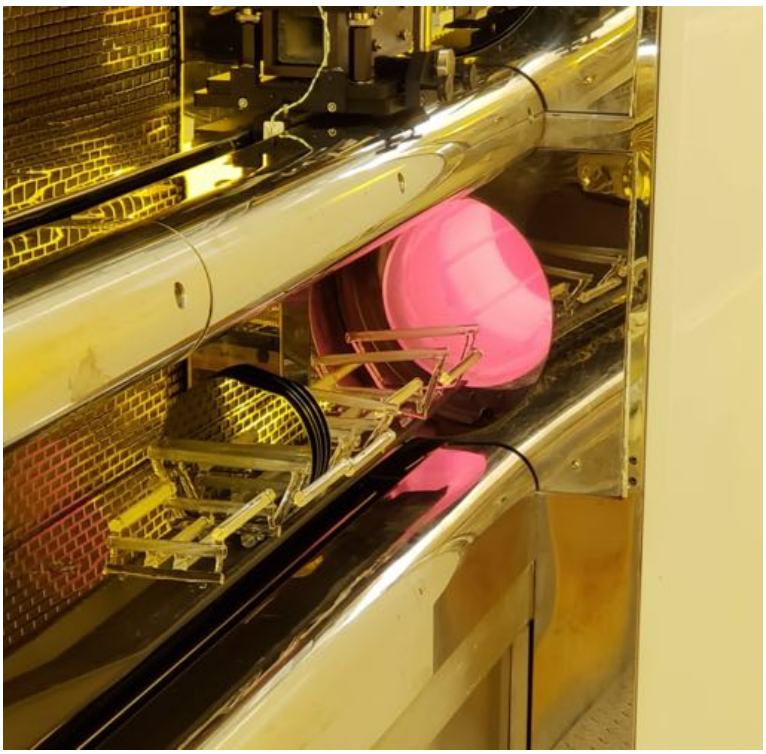

Figure 24: Wafers entering a furnace for thermal oxide growth. The quartz holder is needed to withstand the hot environment.

expected. This ratio means that for every 200 microns of silicon etched, only 1 micron of silicon oxide is etched. This is crucial for reasons outlined further in the component manufacturing section.

To produce this versatile oxide layer, two techniques are commonly used: thermal oxide growth and deposition. For thermal oxide growth, the first step is a thorough chemical cleaning of the wafers which removes organic materials, particles, and the imperfect outer oxide layer. The now bare silicon wafers are placed into a tube furnace, supplying a uniform oxidizing atmosphere at very high temperatures, on the order of 800 C. This high temperature speeds the rate of diffusion of the oxidizing agents into the silicon. At ambient condition, oxide develops, but very slowly otherwise (this is why the native oxide layer is often far from perfect). Two further options exist with this procedure: "wet" oxidation generally uses H_2O as the oxidizer, and "dry" oxidation employs O_2. Wet oxidation is a much faster growth option due to diffusion of water through silicon being higher than O_2. There are penalties to oxide density and uniformity with this

option, however. The iEPS thrusters do not require extremely high grade oxide layers, since it only serves as a mask for etch work later in the fabrication process.

The Deal-Grove model of silicon shows a decreasing rate of oxide growth as thickness increases. For a set oxide thickness X:

$$X(t) = \frac{A}{2}\left[\sqrt{1 + \frac{4B}{A^2}t} - 1\right]$$

where A and B correlate with the temperature and chemical kinetics. [10] Summarily, the thickness is directly proportional to the root of the growth time. Therefore, longer deposition times give little return after a while.

The oxide growth for iEPS thrusters features a long duration wet oxidation followed by short dry oxidation. This time-line gives both decent growth speed and oxide quality; the detailed steps are as follows: [14]

1. Load wafers and heat furnace to 1050°C, with constant nitrogen flow.
2. 20 minute N_2 purge.
3. 20 minute dry oxidation.
4. 200 minute wet oxidation (technically, owing to the controller input it is actually two successive 100 minute wet oxidations).
5. 20 minute dry oxidation.
6. 20 minute N_2 purge.
7. Cool to 300°C and unload wafers. The furnaces are generally left at higher temperature to prevent repeated thermal cycling potentially causing stress to the quartz tubes.

These steps result in a 1 micron thick oxide layer - verified via refractive index metrology - of acceptably dense oxide that enable the many nested patterns that the iEPS thruster

components have.

Unlike oxide growth into the silicon substrate, with oxide deposition, the oxide is developed on top of the substrate through chemical vapor deposition (CVD). A typical reaction may be between silane and oxygen:

$$SiH_4 + O_2 \rightarrow SiO_2 + H_2$$

When done in an ionized environment, this process is sped up dramatically. This deposition is known as plasma-enhanced chemical vapor deposition (PECVD). [14]

5.1.3 Maskless and optical projection photolithography

Photolithography is a very common MEMS fabrication process widely used at nearly every level of cleanroom microfabrication. Simply put, photolithography begins with coating a silicon wafer with a photo-curable polymer, often using a centrigugal spin coater, baking it in an oven to evaporate solvents, then exposing the photoresist to a UV source. As with oxides, there are a variety of photolithography processes available. Photoresist is generally classified as either positive or negative. For positive, the UV light degrades the cross-linking of the photocurable polymers. For negative, the UV exposure promote cross-linking. The extent of the cross-linking during exposure decides whether the photoresist is removed by the chemical developer - typically a mixture with tetramethylammonium hydroxide (TMAH) - for positive resist, or left intact in the case of negative resist. For the work in this thesis, two types of positive photoresist are commonly used: SPR-700 and AZ4620, often referred to as “thin” and “thick” resist respectively. Thin resist is typically used to produce one micron thick layers, while thick resist is used for coatings in the tens of microns. Thin resist is less viscous and easier to coat, while thick is much more viscous and more difficult to deposit correctly. Thick resists are usually only needed for when etching times may compromise the thinner 1 micron resist masks. This spin coating is shown in Figure 25.

Photolithography used in this work falls in the two categories of optical projection,

Figure 25: Spin coating a wafer with AZ4620 “thick” photoresist. Note the aluminum foil is used only to make resist cleanup easier.

"contact" photolithography, or maskless "contactless" photolithography. Contact photolithography has readily become the standard approach due to simplicity, speed, and high resolution. For this approach, a transparent mask usually backed with a chrome layer has the pattern to be transfered onto the photoresist layer. The solid mask is brought into contact with the wafer, then UV light is projected onto the mask for a set amount of time. The exact time depends on the feature size, resist thickness, and resist type. While this process is highly reliable, the chrome backed masks are custom made and add to the overall development time and cost.

Enter maskless photolithography. Instead of creating an entirely new physical mask for every feature/design change, a finely tuned UV laser can be precisely maniuplated across the surface of a resist-covered wafer to expose a unique pattern without a mask. This form of photolithography is not without its drawbacks, however. First, it is much slower than optical projection with a mask. It typically takes about an hour to produce a full six-inch wafer pattern at good quality. With larger features, lower resolution, and less area exposed, this can be trimmed down though. Another point: the laser spot size limits the critical feature size to about 1 micron. Anything below that will suffer a spot size exposure larger than the detail needed. While cheaper than designing and building a contact mask for development work, it does cost significantly more to run this process when compared directly to contact photolithography once the mask is on hand. If the design is constantly changing, this process obviously has a significant advantage. New designs can be drawn, converted for use in the maskless aligner tool and exposed in an afternoon. To that end, in the MEMS world, this tool is analogous to a 3D printer of sorts.

Both of these tools are generally able to exposure aligned patterns from either top or back-side alignment marks. The UV source is exposed only to the top surface, but it is common to pattern a complementary design on the back side of the wafer. To enable this, cameras are mounted to the top and bottom of the wafer chuck. The alignment of the pattern in the mask to the complementary pattern is achieved using alignment crosshairs. Using the cameras, the wafer chuck can be adjusted so the alignment marks pair with the mask. This ensures the patterns are aligned to each other on both sides

of the wafer. For back-side alignment, the mask alignment marks are on the opposite side of the patterned wafer. This requires alignment locations on the mask to be noted by the bottom cameras. The wafer is then loaded in to the chuck and aligned to these locations before exposure.

Another useful technique withing photolithographic fabrication is known as "nested mask" photolithography. This technique entails the patterning of an oxide layer beneath a photoresist layer to enable several etch steps with differing features. In the development work for the electrowetting flow controller, a technique for very shallow (approximately 10 micron) nested masks where both are made of cured photoresist. This is necessary to have a open-channel pattern as well as a wick retaining border on the same wafer side. This is permitted by first masking the channels, etching no more than 10 microns deep and then spin coating more photoresist on top of this side for further pattern exposure. This can be done using either contact or contactless approaches with thick resist, but may have vortices induced in thin resist interacting with the etched layer. This process will be further discussed in the component fabrication section.

5.1.4 Wet processing

"Wet processing" is a term used to describe nearly any chemical work requiring an acid bench or fume hood. The relevant "wet" processes used for iEPS thruster component manufacturing are outlined here.

RCA cleaning

Named for the Radio Corporation of America (RCA) that created this process, RCA cleaning is typically the first step to preparing wafer for the oxidation tube. Any contaminates present can make their way to other wafers and cause significant problems down the road. These contaminates and the native oxide layer must be removed. There are two steps and an optional third that encompass RCA cleaning. Step one, an organic material and particle clean consists of a 5:1:1 mixture of de-ionized (DI) water hydrogen peroxide, and ammonia are run at 80°C. Second, an optional step is a room-temperature

dip in a 50:1 dilution of hydrofluoric acid in DI water. The hydrofluoric acid, capable of etching glass, removes the native oxide layer that forms on silicon in ambient conditions to better prepare the surface for high quality oxide growth. Third, the final cleaning consists of 6:1:1 DI water, hydrochloric acid and hydrogen peroxide. This mixture scours any ionic contaminants present on the wafer. While this contamination is not an issue for the components made for iEPS thrusters, it is crucial not to contaminate the furnace for other users who require this level of cleanliness. [14]

Buffered Oxide Etch

Buffered oxide etch (BOE) is a pre-mixed solution of dilute HF and ammonium fluoride. This solution is typically used to etch the oxide layer once the pattern has been exposed and developed in the photoresist layer. The slow etch rate of BOE at roughly 2 nanometers per second is much more controllable than pure HF. Given HF eats glass rapidly, this process is always done in a plastic tank.

HNA stripping

HNA is an abbreviation for a 1:20:20 mixture of hydrofluoric acid, acedic acid and nitric acid, used to isotropically etch polycrystalline silicon. When preparing HNA, the nitric acid should be poured into the acetic acid as all strong acids should be added to weak acids. Although HF is a weak acid, its fluorine content is a strong oxidizer and therefore added last as not to cause excessive heat generation. Due to the presence of HF, although small, polypropylene containers should be used for reasons previously noted.

Piranha

Aptly named for its extremely aggressive ability to dissolve almost any organic matter it comes into contact with, piranha is typically a 3:1 mix of sulfuric acid and hydrogen peroxide. This ratio is not rigid, and has been used in ratios up to 7:1. It is enticing to add the sulfuric acid to the peroxide when preparing this solution due to its similarity to water. However, doing so can oxidize so rapidly that explosion may occur. For piranha, the peroxide must be added slowly to the acid. This preparation must be done in a quartz container due to the extremely exothermic reaction that ensues and the fact that nearly all plastic containers would be dissolved by the solution. Piranha is typically

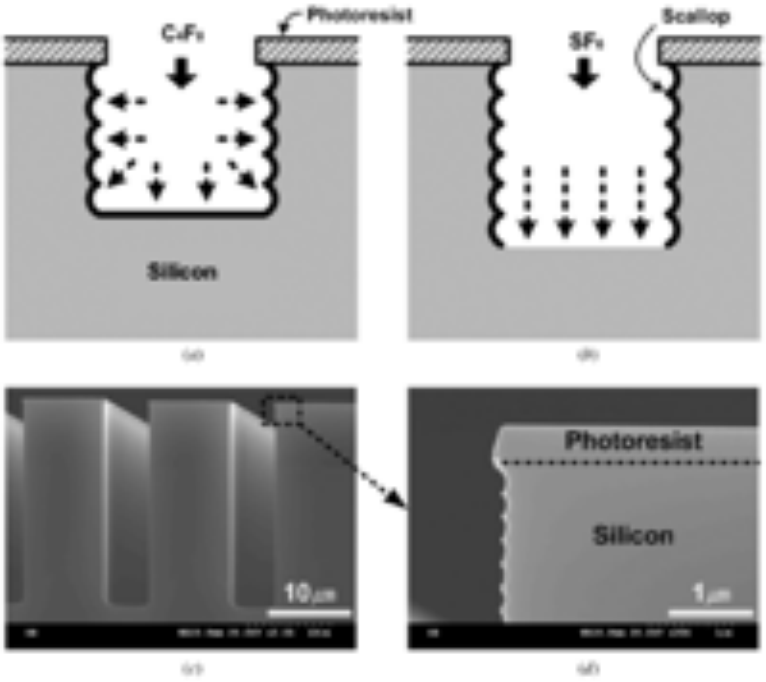

Figure 26: DRIE etch effect in silicon substrate. The etch and passivation steps (Bosch process) show the scalloping effect. [9]

used to strip photoresist after etching is complete. Additionally, it removes all organic impurities and ensures a pristine surface for further processing.

5.1.5 DRIE

DRIE (deep reactive ion etching) is a standard anisotropic silicon etching technique used in MEMS fabrication. This process is widely employed with very successful results. The contemporary recipe is called the Bosch process. It includes alternating steps of plasma etching and isotropic passivation. During the plasma etching phase, a sulfur hexafluoride (SF_6) plasma is directed at the silicon wafer to be etched by applying a voltage between the source and the wafer chuck. The SF_6 partially dissociates while the fluorine atoms react and etch the silicon away. During the passivation phase, a C_4F_8 fluorocarbon plasma is produced and adsorbed onto the wafer surface and polymerizes to form a thin non-reactive fluoropolymer film. The SF_6 plasma is unable to etch the fluoropolymer layer. However, with a bias applied, the ions can sputter away the coating normal to the biased wafer chuck, and etch the underlying silicon away. This repeated process

produces very small scallops that, together, provide a very directional anisotropic etch result. As mentioned, thermally grown oxide resists chemical etching very well. However, the oxide will eventually be sputtered away. Typical selectivity ratios of 200:1 can be expected for etch rates between silicon oxide and bare silicon, but 100:1 is more standard to avoid piercing through the oxide layer and etching the silicon underneath.

While highly tool and process dependent, etch aspect ratios of 20:1 can typically be achieved with DRIE, although claims of up to 200:1 for highly specialized tools and processes have been made. When the aspect ratio reaches its maximum, the etch slows substantially due to lack of plasma reaching the silicon surface. When this happens, formation of black silicon can occur which further slows etch rates and requires a ramp up in SF_6. These tools are also capable of providing isotropic etching for undercutting the oxide mask layer or to stop the production of black silicon. By turning of the applied bias as well as the passivation step, the etch is strictly SF_6 plasma driven and therefore isotropic. One should take note that without the passivation step, however, the etch rate of pure SF_6 plasma is considerably higher than the Bosch process. [14]

5.1.6 Material deposition techniques

While oxide deposition has been discussed, many other unique materials can be deposited on wafers for MEMS fabrication uses.

Chemical vapor deposition

Chemical vapor deposition (CVD) allows for deposition of many thin films via gaseous absorption onto a wafer's surface where it reacts and deposits a desired material. Polycrystalline silicon (typically refered to as polysilicone) is formed from a pure silane reaction at low pressure and high temperature. This process falls under the category of the aptly named low pressure chemical vapor deposition (LPCVD).

$$SiH_4 \rightarrow Si + H_2$$

Another process developed in [14] for deposition of thick lasers of fluoropolymer is also

commonly used for hydrophic microfluidic applications:

$$C_4F_8 \rightarrow CF_x^+ CF_x + F^-$$
$$CF_x \rightarrow [CF_2]_n$$

This is simply the passivation step of the aforementioned DRIE Bosch process. The experimental nature of this comes from the fact that the passivation step of the Bosch process typically lasts from 10-15 seconds and deposits a thin film. When passivation occurs in the Bosch process, however, it is only for a few seconds and a few nanometers of deposition. For hundreds of nanometers, tens of minutes are required to build up a layer useful for hydrophobic effects. Due to the much-longer-than-designed runtimes, this process requires constant measurement between runs to ensure deposition rates are near desired values. The use of a profilometer between runs can ensure reliable deposition with this technique.

5.1.7 Wafer bonding

Silicon contact bonding and anodic bonding are the two wafer bonding techniques utilized in iEPS component manufacturing. Both of these bonding techniques rely heavily on the cleanliness of the wafers to be bonded. A piranha dip followed by ashing is generally enough to ensure a pristine surface for a few hours, so speed in processing is key to getting good results.

The actual bonding of wafers is achieved when they are carefully aligned using an aligner very similar to that used for contact mask photolithography. The two aligned wafers are then temporarily clamped together before being placed into a bonding tool to be heated and compressed. Van der Waals forces drive the bonding of silicon/silicon wafers that are sufficiently clean. This bond is rather weak. However, to ensure a good bond, the wafers must be heated to anneal the interfacing surface and form stronger bonds that will withstand dicing.

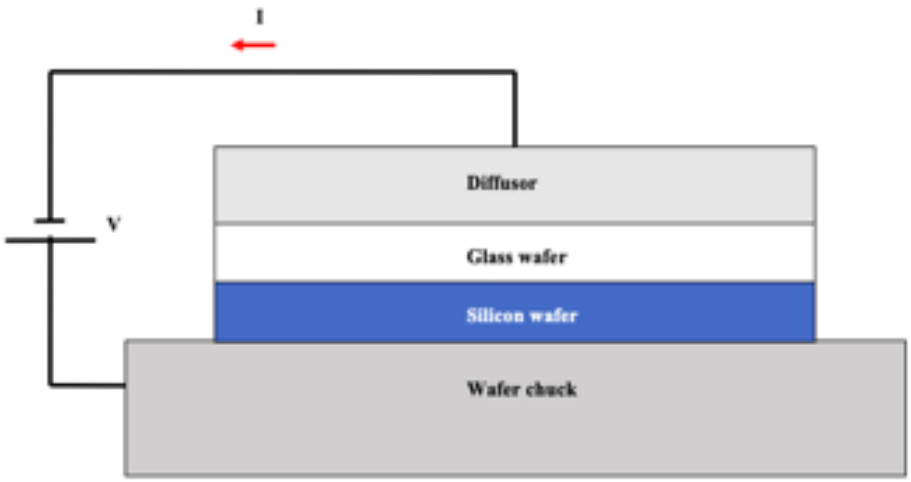

Figure 27: Anodic bonding depication of a glass wafer to a silicon wafer.

Anodic bonding is another beast entirely. Ionic impurities between two differing materials (typically a glass and silicon) are what drive the bond to form. Just like silicon contact bonding, the wafers must be thoroughly cleaned to form a good interface for uniform ion drift, since heat and pressure alone do not form a bond. A biasing voltage is applied across the the two wafers. This causes the sodium ions present in the glass to drift away from the silicon/glass interface (or depletion layer). This promotes a strong electrostatic attractive force due to the charge separation between the wafers. This force couples with strong elecetrochemically formed bonds to create a very robust bond.[4] This can be done with more than two wafers as well. Typical "stacks" are made of glass-silicon-glass or, for iEPS thruster frames, silicon-glass-silicon. This process is depicted in Figure 27.

5.1.8 Wafer dicing

Following wafer fabrication, cleaning, and any needed bonding steps, the wafer or wafer stack is diced into its respective components. This process inherently holds the highest risk due to extreme environmental conditions in the diesaw tool (moving water and a blade spinning at 30 kRPM while under suction clamping). This is amplified by the fact this step comes is the culmination of many work hours prior. The wafer is affixed to specialized thick tape and placed on a vacuum chuck where the saw blade will follow

Figure 28: Dicing a developmental extractor wafer. The wafer is mounted on dicing tape, which in turn is attached to the chuck via vacuum. The white tape around the edge is intended to prevent water getting underneath the tape and potentially lifting it.

a pre-programmed process to cut the individual dies (components) out of a wafer. The tape acts as both a malleable layer for the chuck to seal to and a sacrificial layer for the blade to cut into slightly. This tool is shown in Figure 28.

6 Thruster Component Manufacturing

As previously discussed, MEMS techniques differ greatly compared to contemporary manufacturing processes. This section serves to discuss in greater detail the fabrication steps for each of the thruster's MEMS-fabricated components and the changes to each process that have improved the overall thruster package.

6.1 Thruster frame fabrication

The fabrication of the current thrusters have changes only slightly in terms of processing. The base L1 layer consists of a 1 mm silicon wafer as a structural base for the additional layers and is thick enough to allow for the propellant well feature to be etched into it. The L2 layer is a 500 micron glass insulating wafer which serves the purpose of insulating the base layer from the extractor and mitigating propellant creep up the posts via a knife edge feature. Lastly, a 500 micron silicon wafer is used for the L3 alignment layer. The following subsections discuss fabrication of each layer, the anodic bonding step to form the wafer stack, and dicing the stack into individual frames.

6.1.1 L1 base layer

The L1 base layer is the bedrock for the emitter chip, frame posts, and extractor. Being the primary structure of the thruster, the base layer is crafted from a 1 mm thick prime grade double-side polished (DSP) silicon wafer. Throughout processing, no ion impurities or metal dopants are introduced. Simply put, in the clean room, this allows for the use of a wider variety of tools for processing than for those wafers which have metal dopants or ion impurities. In table 1, a simplified process for L1 fabrication is layed out. The wafer dimensions, crystal orientation, dopant type, and material are also included.

A thermally grown 0.5 μm oxide layer is required following proper RCA cleaning. As mentioned, no ionic impurities or doping is necessary for this layer, so a "rougher" oxide finish is suitable. Inspecting the oxide layer is good practice, but again, not strictly necessary given this oxide layer is only for mask purposes. To enable parallel processing in BOE with the L3 layers, only the top side of the wafer is coated with 1.3 μm of SPR-700 thin resist, leaving the wafer's back side uncoated.

L1 Base Layer Process		
Materials: 150mm x 1mm DSP <100>N-type Si wafer		
Step	Process	Comments
0.0	**RCA Clean**	
1.0	**Wet thermal oxidation**	500 nm
2.0	**Nested mask patterning**	Both sides, 1.3 μm resist. Top side: Pedestal mask
3.0	**Oxide patterning**	10 minutes BOE
3.1	Strip photoresist	10 minute piranha
		Top side, 10 μm resist. Mask: Well and moat
4.0	**Secondary patterning**	
		Back side, double coat10 μm resist. Mask: Halo and Ls
5.0	**Oxide patterning**	10 minutes BOE
6.0	**DRIE**	
6.1	Back side etch	Etch 750 μm deep
6.2	Top side etch	Expose back side etch
6.3	Strip photoresist	Ash 30 minutes pure O2, follow with 10 minutes piranha
6.4	Top side etch	Etch pedestals, 40 μm

Table 1: Process flow for revised L1 wafers.

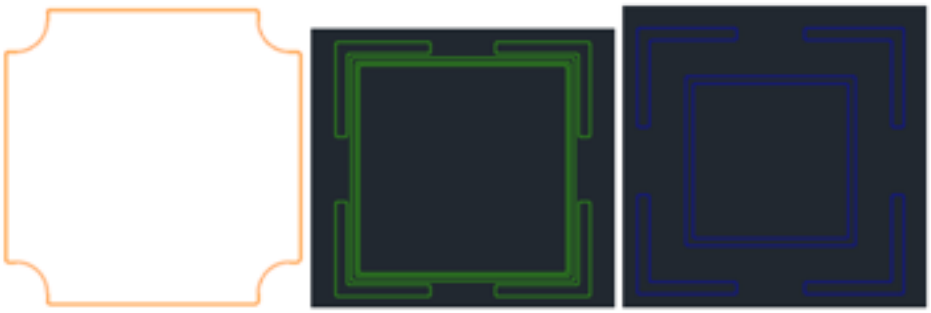

Figure 29: Mask files for the L1 base layer patterns. Left to right: pedestal mask, adhesive moat and propellant well, halo etch for material removal. [14]

Following a pre-bake of the resist to harden it to a handleable level, the L1 pedestal mask is exposed to the top side of the wafer. This step is necessary to keep the L2 posts as the only area that is bonded to the L1. The wafer is then developed to remove exposed resist. The pattern is then inspected under a microscope before moving to a final post-bake to further harden the resist layer. After the post-bake hardening, the oxide layer is patterned with a ten minute BOE dip. The photoresist for this pattern has now served its purpose and is stripped with a 10 minute bath in piranha.

Following oxide patterning, the masks for silicon etching must be exposed. These masks

will undergo deep etching via DRIE and thus require thick resist to withstand the etching plasma for the duration of the steps. The wafer top side is spin coated with 10 μm of AZ-4620 thick resist. The wafer is pre-baked for 10 minutes to become handleable and avoid damage from the spincoater vacuum chuck. This layer is thicker due to the bulk of etch work being done from this side of the wafer. The thick resist layers are then pre-baked for one hour before being exposed. The L1 well mask is then exposed using top-side alignment in the mask aligner tool. This is a prime example of the aforementioned "nested mask" technique. The pedestal mask is contained on the oxide layer and the well is contained in the bare silicon layer via the photoresist.

The final halo etch mask is then exposed using back-side alignment this time. Given the doubly thick layer of resist on this side of the wafer, the exposure flux needed to increase. A triple exposure at 15 seconds on 20 seconds off successfully transferred the pattern as compared to the single 22 second exposure for the single layer. Visual inspection of the development is difficult given the resist thickness on the back side, so a standard development followed by a microscope inspection and additional needed development is good practice. Once the exposed resist is fully developed and removed, the post-bake proceeds as usual. Thus completing the photolithographic portion of the L1 wafer.

Once the photoresist is cured, the wafer should be checked for any exposed oxide. If there is any, a second round of BOE is necessary (alignment L3 layer can be parallel dipped here.) Once all oxide is covered or removed, the deep DRIE work begins. It is standard practice to protect the alignment marks for bonding use with bits of kapton tape. Once the marks and any possible exposed silicon areas outside of the desired pattern is protected, the wafer back side is etched approximately 750 μm. Using the STS DRIE tool in the clean room take roughly 4.5 hours. Given the top side etch will expose this etch, the exact depth of the 4.5 hour etch is not absolutely critical. It need only be deep enough to be met from the top side etch without compromising the resist layer. Again, the process is checked using a microscope before proceeding, as more etch time may be required. The kapton tape coverings are then removed. To protect the newly etched trenches, the back side of the wafer is then taped with clean room tape

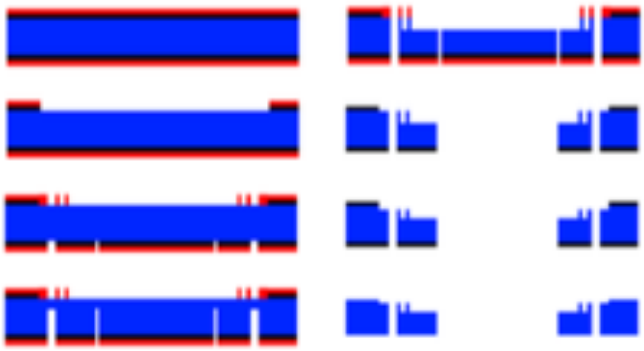

Figure 30: L1 base layer process flow. Red represents photoresist, black represents oxide, and blue represents silicon. [14]

and vented via slits cut into the tape. The L1 is now ready for the next round of etching.

The L1 wafer is flipped over for top side etching. Since the top side pattern has more silicon exposed, the top side etch rate is slower than the back by about 0.7 μm per minute. The top side pattern is etched until it meets the back etch. This typically takes about 2.5 hours to form the 300 μm well feature. The protective tape is once again removed from the wafer after the etch is complete. The wafer is ashed in an O2 plasma for 30 minutes to ash away any fluoropolymer left from the DRIE passivation steps. The wafer is then placed in a piranha solution for 10 minutes to strip the photoresist and leave the pedestal patterned oxide now exposed.

To complete the L1 wafer, the remaining oxide pattern is now etched for about 15 minutes to approximately 50 μm to create the ledge geometry. This final etch leaves the alignment marks uncovered by tape in order to transfer them into the bare silicon for bonding alignment later on. The oxide layer is now ready to be stripped via an hydrofluoric acid dip for about 5 minutes. Since this step is in preparation for bonding, parallel processing with the L3 alignment wafers is encouraged.

6.1.2 L2 insulating layer

The L2 insulating layer is the only frame component not formed in silicon, and it only requires a single mask pattern. The L2 insulating layer starts with a wafer of Pyrex

Figure 31: Insulating layer process flow. [14]

glass that requires isotropic wet etching. The Pyrex wafer is coated on both sides with 1 μm of thin resist and exposed. The wafer is then put through standard development and baking procedure before being subjected to a ten minute BOE dip to impress the alignment marks onto the glass. Next, the photoresist is stripped via piranha and thoroughly cleaned before depositing a 250nm layer of polysilicon front and back using a LPCVD method to form an HF-resistant mask layer. The polysilicon coated wafer is then spin coated with thin resist again, and the L2 pattern is aligned to the alignment marks using back side alignment and exposed. After development, the alignment marks are covered with thin resist to protect them and then baked before heading to the dry etching tool.

The STS1 dry etching tool is used to provide a short duration SF_6 plasma to etch the pattern into the polysilicon layer with no need for a passivation step given the Pyrex material is highly etch-resistant.

With the polysilicon mask formed, an undiluted hydrofluoric acid dip is used to etch the glass. The HF etches Pyrex roughly 5 μm per minute. To have a knife edge in the middle of the wafer, the 250 μm etch depth from both sides requires about 50 minutes of HF etching. A 10 minute piranha dip removes any leftover photoresist on the wafer exposing the unetched polysilicon underneath. This state of the wafer is shown in Figure 32. Lastly, the polysilicon layer is removed using a 10 minute HNA dip. Once complete, the L2 wafers are cleaned and ready for bonding.

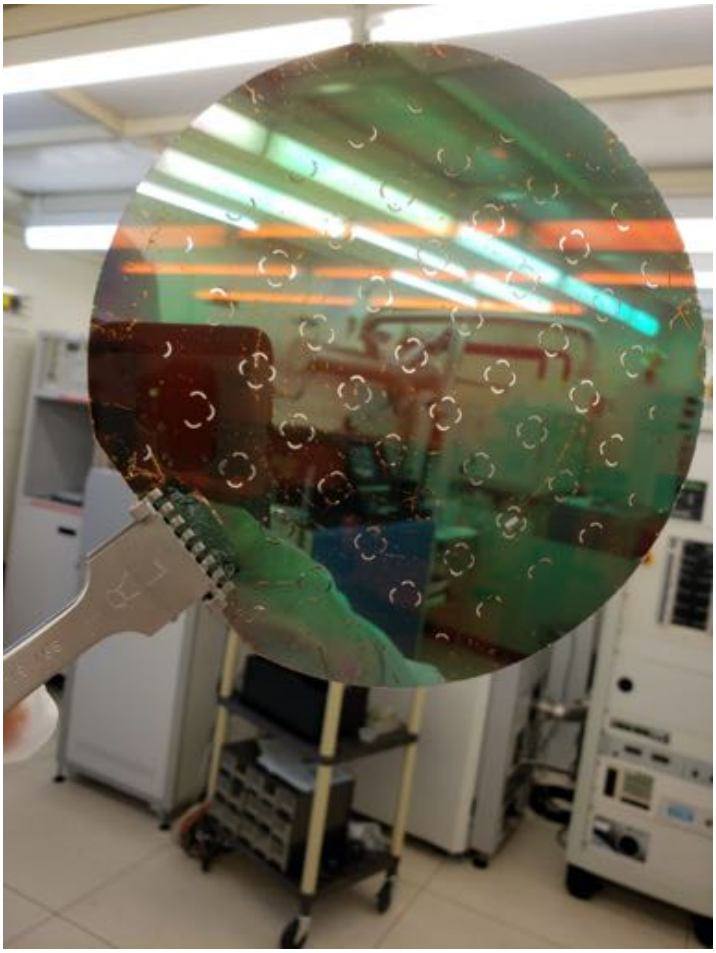

Figure 32: An L2 wafer prior to being stripped of its polysilicon layer. Once this layer is removed, the wafer is transparent.

6.1.3 L3 alignment layer

The L3 alignment layer is fabricated using a 500 μm thick prime DSP silicon wafer. This layer serves as an alignment tool for positioning the laser correctly when ablating the tips and doubles as an approximate mechanical alignment feature for the extractor to sit on.

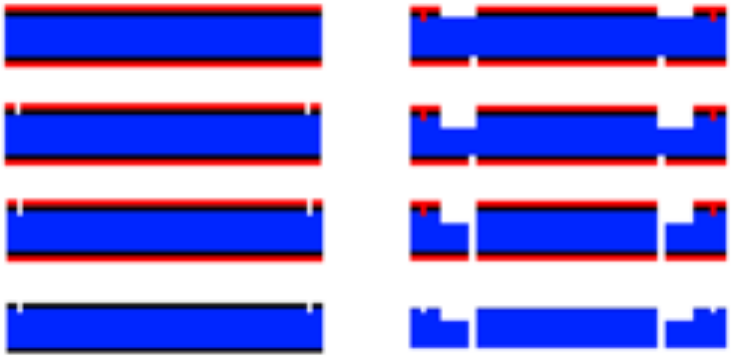

Figure 33: L3 alignment layer cross-section evolution. There are notched steps to both hold the shallow etched alignment crosses and support the extractor. [14]

Like the L1, the first step for L3 fab is growing 0.5 μm of oxide. The preceding cleaning steps for the L1 apply here too, so parallel processing is the wise move. The wafer is then coated on both sides with 1 μm of SPR-700 thin resist. The L3 Alignment Cross mask is used to expose the top side. The back is left alone for the moment, as it is merely there for protection of the oxide to be patterned later. Similar to the L1, following exposure, the pattern is checked for any glaring errors, baked, dipped in BOE, and then the photoresist is removed via piranha.

The 300 nanometer etch required to form the alignment crosses only takes about 20 seconds of SF_6 plasma exposure to complete (no passivation needed.) Following this step, the thin resist is now stripped with piranha. And the top and back of the wafer are coated with 10 μm of AZ-4620 thick resist. The L3 Post mask is exposed to the wafer's top side and the L3 Through Etch mask exposed to the back. Again, following a quick inspection and longer hard bake for the thick resist, a 10 minute BOE dip patterns

Figure 34: The L3 alignment layer masks. On the left is the through etch (same as L2 mask) and on the right is the pedestal mask. [14]

the oxide layers.

Following the BOE and removal of oxide, the pedestal features are etched to at least a depth of 150 μm to ensure the extractor sits flush with the emitter tips. The etch rate for this step is approximately 2.5 μm per minute, taking roughly one hour to reach the designed depth. A similar approach to checking the etch depth used for the L1 can be used here, checking half way through the etch, taping and continuing. The wafers back side is etched until it meets the top side etch. This should be a slight bit less than 350 μm. Given the smaller area of exposed silicon, this etch takes about 2 hours to complete at a faster 3 μm etch rate. Once the etching has completed, the thick photoresist is removed by ashing in O2 plasma for 30 minutes followed by a 10 minute piranha dip. Lastly, the L3 is ready to be bonded following a 5 minute undiluted HF dip to strip the oxide layer. The piranha dip step prior to bonding is shown in Figure 35.

6.1.4 Anodic bonding and dicing

Once the frame layer wafers are fabricated and cleaned, they are ready to be bonded into a full frame stack and then diced. This bonding step has been subject to many trials and tribulations, but for the previously discussed frame layer designs, a very reliable bonding approach has been devised.

Figure 35: Piranha solution stripping photoresist and organic materials from wafers prior to bonding.

Cleanliness is key to successful bonding. Since the wafers are very hard and very flat, any dust or debris will create gaps where bonding will fail. This thorough cleaning is done just prior to bonding and incorporates ashing in O2 plasma and then cleaning the wafers with piranha (the L1 and L3 oxide layers are then stripped with pure HF if they have not yet.) Ashing is always prior to piranha since the processing chamber of the tool is a possible contaminate source. The first bond is the L1-L2 silicon-glass bond. This is a typical anodic bond setup having the glass wafer atop the silicon base layer and a graphite diffuser atop the glass wafer. An aligning tool similar to that used for optical projection photolithography is utilized for backside alignment of the L2 to the L1. The L1-L2 stack is placed in the anodic bonder where it is then compressed, heated, and subject to a voltage bias to form the bond layer. Vacuum is applied following the waferbow pin being lowered to correct for wafer bow but before the compression piston is lowered in place. This helps mitigate trapped air in between layers. When the piston is in place, the chamber is vented again to avoid breakdown within the chamber at rough vacuum pressure. Shown in Figure 36 is the clear L2 wafer atop the silicon L1 wafer in the bonding tool. The graphite diffuser is seen in the reflection of the wafers.

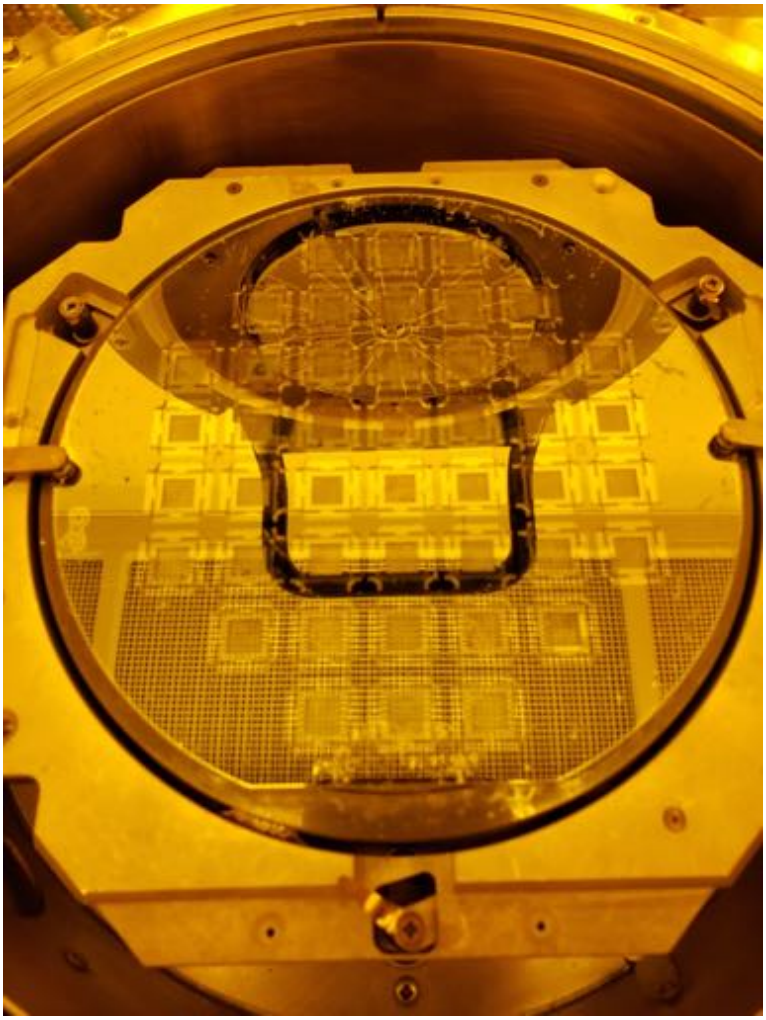

Figure 36: The L2 wafer bonded to the underlying L1 wafer. Lack of fringe patterns suggests successful bonding. The area near the left wafer clamp has a small fringe spot indicating poor bonding in the non-device area of the wafer.

The L3 bonding to the L1-L2 stack is the more difficult bond. Another piranha cleaning of the L1-L2 stack and L3 wafer is done to ensure cleanliness (this step is optional although it has shown improved final yield.) Back side alignment must be done for this bond as well. The bond setup follows as before, with the noted exception of polarity of the applied voltage being switched. Once heated and compressed, the voltage is then applied. The power supply is set for 800 V but current limited to 10 mA to enable current decay prior to voltage climbing. The current is slowly driven down to about 1 mA before the polarity is then switched *back* to the L1-L2 polarity. This is hypothesized to potentially smooth charge layers present in the bond layers. Since incorporating this step, final yield increased reliably to nearly 100 percent. Further study of this step and the underlying physics is still ongoing.

Following the successful bonding of the frame stack, dicing comes next. To keep the individual frame dies from moving around once diced, the entire stack is super glued to a sacrificial dummy wafer and then mounted to dicing tape. A second layer of dicing tape covers the top of the wafer to keep the posts as protected as possible. Once the first set of cuts are complete, kapton tape is used to cover these cuts before proceeding to the orthogonal cuts. This keeps the dicing tape on top of the stack from coming loose and interfering with the tool operation. Three cuts are needed for each cut line given the thickness of the wafer. Slower speed is also used when cutting through the glass layer into the thicker base layer. Once the cuts are finished, the wafer is submerged in acetone to free the dicing tape and the glued-on dummy wafer support. This releases the individual frame dies; for an extra layer of cleanliness, the frames can then be ashed to remove any residue from dicing. This concludes the fabrication of the thruster frames.

6.2 Valve manufacture

Fabrication of the electrowetting valves developed in [14] follow very similar steps to that work, with a few slight changes noted here.

6.2.1 Valve fabrication process

The current electrowetting valve fabrication process is shown in a cross-sectional view in Figure 38.

Figure 37: Frames after dicing and acetone bath.

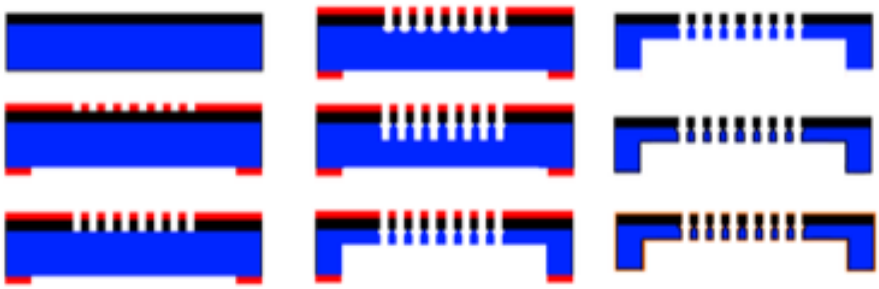

Figure 38: Cross sectional overview of electrowetting valve fabrication flow. [14]

The valve fabrication begins with a 675 μm thick single-side-polished test wafer. The wafers are cleaned of organics via piranha before depositing 0.75 μm of oxide on the polished side using CVD to eventually form the capillary lip feature. This oxide thickness may soon be increased to enhance the strength of the lip feature. The polished surface is coated with 6 μm of thick resist and the opposite side with 10 μm. The thinner resist on the polished side is to better facilitate pattern transfer resolution. Thicker resist tends to create aliasing when maskless photolithography is done in the single micron range. A high laser flux is needed to ensure thorough development of the rough side mask (a

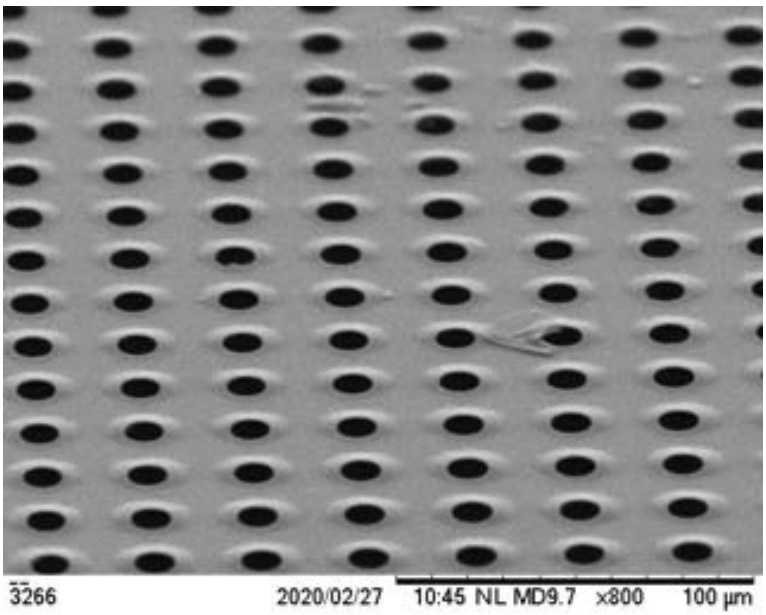

Figure 39: Valve capillaries with lip undercuts.

simple square pattern.)

A cycled dry plasma etch at 450W and 2 Torr, 4 cycles of 2 minute etching by CHF_3 with 2 minute cooling cycles is sufficient to cut through the oxide layer and preserve the resist mask. To form the oxide lip feature, the an isotropic SF_6 etch undercuts the thin oxide layer. This 30 second etch creates a two μm undercut ledge that is shown in an SEM image in Figure 39

To etch the capillaries into the wafer, DRIE is used on the top side of the wafer. While exact depth is not critical, approximately 250 μm of etching is done for the capillaries. The wafer back side (square pattern) is then etched to exposed the capillaries that were just etched. Following all other fab processes, the photoresist is stripped via ashing in O2 plasma and then a piranha dip. With the wafer thoroughly cleaned, they are ready for 2 μm of thermally grown oxide. This requires two long duration stints in the furnace with a cooling step in between. This typically requires two days to complete. The 2 μm oxide layer is strictly to prevent breakdown of the silicon during activation and subsequent thruster operation.

The oxidized wafers are now ready to be diced. Simple mounting to dicing tape and second layer on top of the wafer is all that is needed for this step to protect the capillaries and lips. Once diced and any dicing tape residue removed via acetone and/or ashing, one valve edge is metallized to enable mounting of a grounding wire to the valve. 50nm of titanium followed by 50nm of silver is deposited via a sputter coater. This edge is then covered in kapton to protect it for the final step.

The final step for valve fabrication is depositing the hydrophobic fluoropolymer layer using PECVD. An approximately 400nm thick layer of fluoropolymer has reliable resisted wetting of the surface for months. The exact process for this deposition varies based on atmospheric conditions that day, since the passivation step of DRIE used is not meant for long durations. Dialing in the depostion rate is necessary on junk silicon or glass to then be verified via profilomtery. The valves are now complete.

6.3 Flow controller manufacture

As outlined earlier, the need for active control of wetting *and* de-wetting was deemed necessary for electrospray thrusters. Simple modifications to the existing electrowetting valve architecture resulted in the following preliminary flow-regulating valve design.

6.3.1 Preliminary flow controller design

The flow controller begins with the same 675 μm test wafer (now double-side-polished given crucial channel geometries) and is cleaned prior to deposition of 1 μm of oxide on the polished side. The preliminary design includes the same number of capillaries, condensed slightly to maintain the same foot print. The top polished side first receives 6 μm of thick resist and the bottom then receives 6 μm. Once baked, the maskless aligner is used to expose the capillaries on the top side and the flow channels on the bottom side. The resist is then hard baked for etching.

The oxide is first etched with a cycled dry plasma at 450W and 2 Torr; 4 cycles of 2 minute etching with CHF_3 followed by 2 minute cooling cycles in between. The oxide

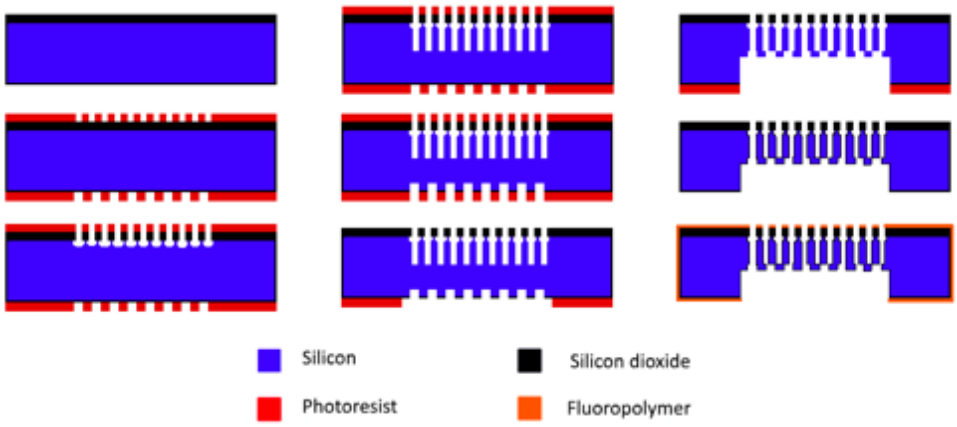

Figure 40: Flow controlling valve fabrication process flow.

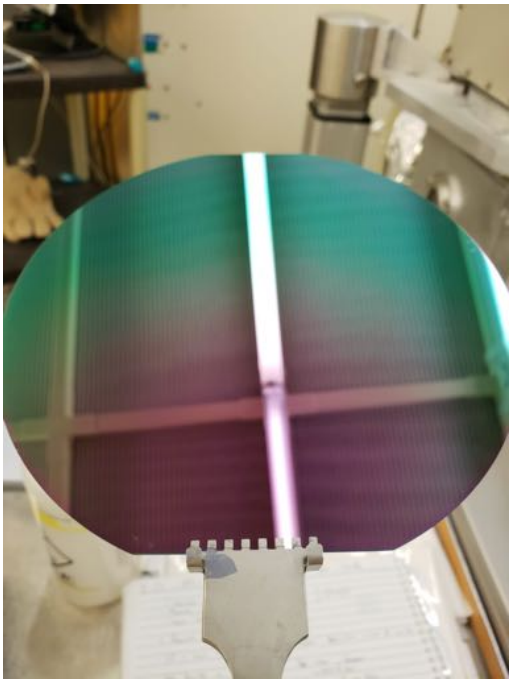

Figure 41: Oxide depositon on valve wafer.

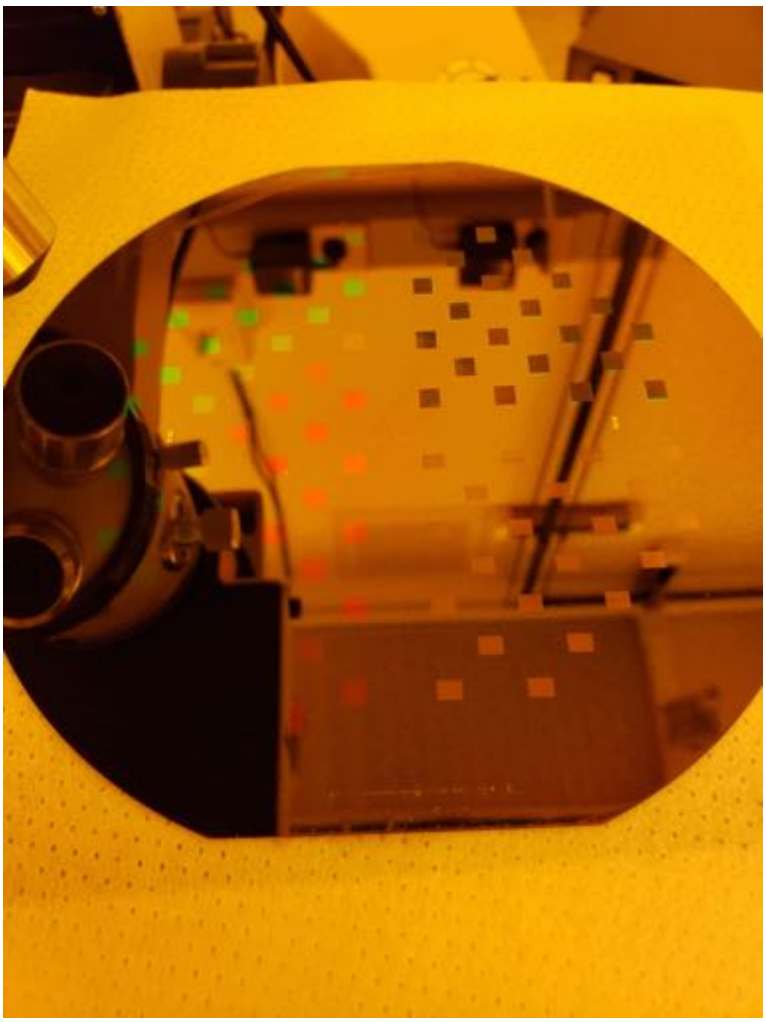

Figure 42: Flow controlling valve wafer back side. Note half of wafer is used to produce single-use electrowetting valves in parallel.

layer is then undercut with a 30 second isotropic SF_6 etch. The capillaries are then etched approximately 250 μm deep. The wafer is flipped over and the channels are etched to a depth that provides a square channel cross-section. This is currently about 10 μm deep. The wafers are then ashed in O2 plasma before being dipped in piranha to remove the resist. The second photo step can now take place.

The final mask for the preliminary flow controlling valve serves a similar purpose to the square pattern on the electrowetting valve. This mask provides a region for the wicking material to be pinned and allows the channels to be etched down to meet the capillaries, exposing them. 10 μm of thick resist is needed for this back side etch. The etched chan-

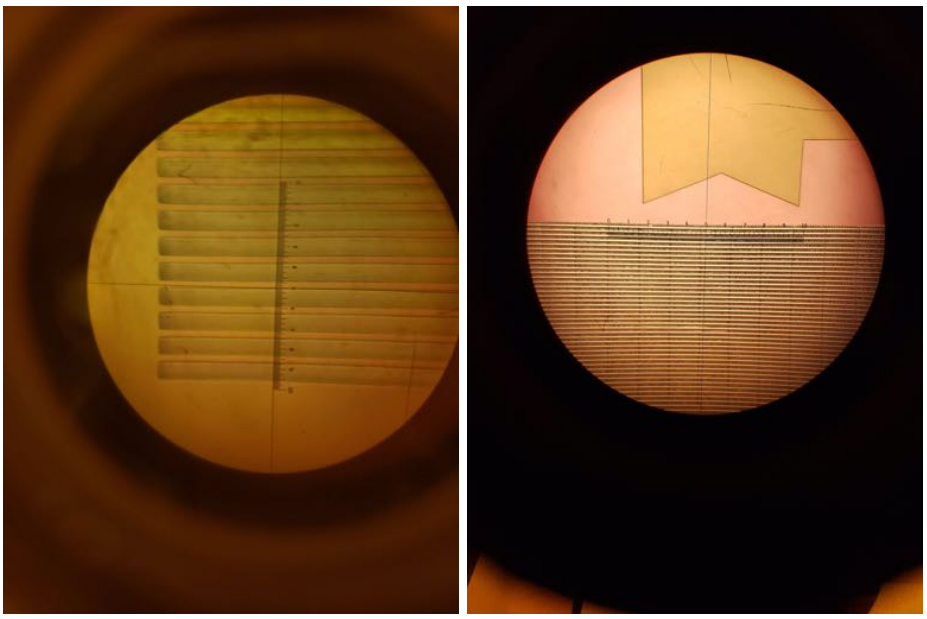

Figure 43: Flow controlling valve channels and wicking material ledge feature.

nels are so shallow that they do not interfere with the resist deposition. Once baked, the laser flux on the maskless aligner is then increased to ensure thorough development. Following a development and hard baking, the wafers can then move back to DRIE.

An approximate 2.5 hour DRIE of the back side of the wafers drives the channels as well as the valve border down approximately 425 μm to expose the capillaries. Once the etch exposes the capillaries fully, the wafers are removed and ready to be cleaned for oxide growth.

Again, a 2 μm thermally grown oxide is applied to the wafers over the course of 2 days. This keeps the valve safe from breakdown during subjection to operational voltages. Once diced, the edges are metallized as described above. The developmental valves are then ashed and prepared for deposition of an approximately 400nm coating of fluoropolymer. Once complete, the flow controlling valves are now ready for testing with wicking material inserted.

7 Material Research and Development

7.1 Motivation

The material currently used for the thruster's emitter substrates is a porous borosilicate glass, with varying sized of base frit.

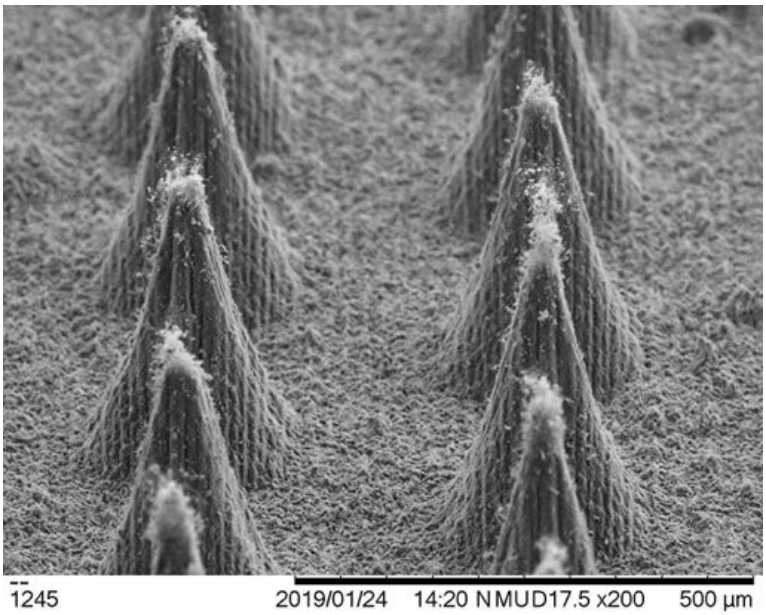

Figure 44: A tip array in borosilicate glass. Note how large and irregularly sized the pieces of glass are that make up the frits.

The pore size is roughly 500-1000 nanometers in diameter, as measured both visually by SEM and additionally by inference through bubble testing. [14] This allows a good flow rate of liquid through the pores, but unfortunately is not without downsides. The major issue is the polydispersity of the beads and the resulting inhomogeneity of the sintered material; during laser ablation of the tip arrays, there tends to be a great deal of debris and "stray tips", small peaks that are not part of the main pattern. This presents a twofold danger. First, and more obviously, any stray tip or piece of debris can potentially produce an auxiliary emission site, which will be emitting ions directly into the extractor, damaging it or, worse, forming a liquid bridge that shorts the thruster. Secondly, the increased topographical roughness of the emitter caused by the stray tips means that there are more sites that menisci can form. Like menisci

(i.e. both concave upwards, in this case) can interact and climb; if that happens on the emitter chip surface, the chip could flood with ionic liquid and vastly increase the risk of shorting the emitter to the extractor. As such, pains must be taken to clean the spaces between the tips by hand using a tungsten needle and single-hair brush. This is not a user-friendly material, although being commercially available is an obvious advantage. A major research thrust of this thesis work is to develop a monodisperse (uniform grain size and dispersion) porous silica ceramic. Some off-the-shelf materials were investigated as possible candidates.

7.2 "Mystery glass"

A vendor was located to supply an alternative material (known affectionately as "mystery glass" due to the initial recalcitrance of the vendor regarding its composition). The pore size was measured as being approximately 100 nm, checked both by bubble test and by SEM imaging, and the material was later confirmed as being comprised of 99% fused silica. This produced a slight issue with bonding the glass to the extractor, as the fused silica has a coefficient of thermal expansion (CTE) of approximately 0.5 μm K^{-1}, an order of magnitude lower than the silicon frame's 3.5 μm K^{-1}. This mismatch induces a lot of residual stress thanks to the elevated temperatures at which the Ferro glass sealing paste is employed, so the bonding had to be carefully managed in order to reduce the likelihood of the bond failing.

While the material had promising results in wetting and laser ablation, firing provided insights into several issues. Primarily, the hydraulic impedance of this material was far too high to compete with the borosilicate glass. What is more, the vendor could not reliably reproduce the material upon request. [14]

7.3 Coral glass

Another promising candidate for a commercially available material was a porous glass material by the name of "Coral." A Japanese material manufacturer proved reliable production of this material up to 0.5 mm thick substrates. Hydraulic impedance is

estimated be close to that of carbon aerogel in the 10^{15} kg m^{-4} s^{-1} range. Tip radii were less than 10 microns once the laser was dialed in appropriately. These results are shown in Figure 45.

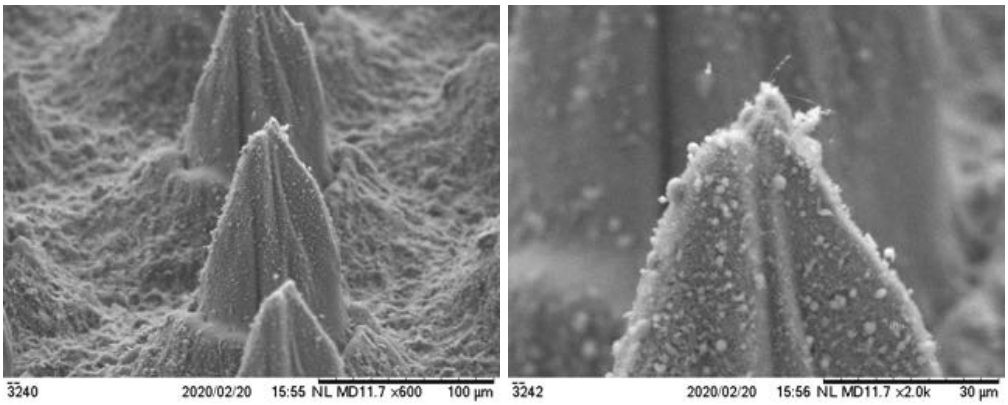

Figure 45: A tip in "coral" glass. Note the wider base of the tip, but fine tip resolution.

While future testing and development work will certainly continue with this material, initial firing trials, once mounted in a thruster, startup voltage was, on average, approximately 1 kV plus or minus 150 V. However, once the thruster began firing, its emitted current trickled down to zero quickly. Suggesting high hydraulic impedance may be at play somewhere in the material or tips themselves. This couples with an observation made during thruster assembly where the ionic liquid droplets applied to the back of the chip took several hours to wet the material completely. Again, further testing will tell the viability of this material in future thruster applications.

7.4 Monodisperse silica ceramic

Building off the successful aspects of the "mystery glass", it was decided to attempt to manufacture a new silica-based material in-house, with larger pores to mitigate the main failing of the previous material. To do this, mono-dispersed silica beads of varying sizes were suspended in a UV-curable resin. This resin and silica suspension is then formed into 1cm square chips of varying thickness via UV-cast molding. The resulting cured resin and silica chips are then fired to burn away the resin and sinter the silica spheres slightly to keep the porous structure. This follows a similar approach used in [14] and [6] with the biggest difference being the casting method. Trial results from [14] showed very good tip geometry (shown in Figure 46); the substrates themselves, rarely

came out in unfractured square chips, however.

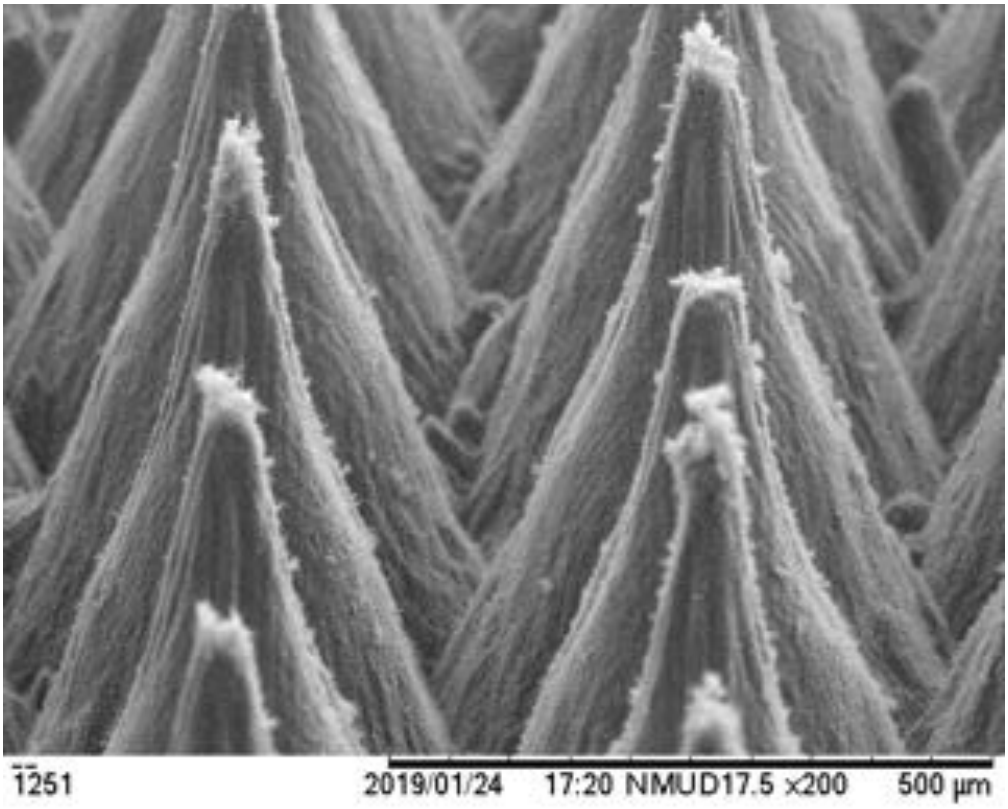

Figure 46: A tip array test pattern etched in sintered silica from the work of [14]. The small flecks of material clinging to the tips were easily removed with a 15 second buffered oxide etch (BOE)

The evolution of this new approach to creating monodisperse silica substrates is described in the following sections.

7.4.1 3D printing

Stereolithographic (SLA) 3D printing has proven the efficacy of printing structures using a UV-laser to cure various material suspensions in a photopolymer resin.[17] Such a technology showed promise to print ceramic substrates for laser ablation into emitter arrays. The possibility of printing other parts of the thruster such as frames was also attractive. This would eliminate the need to make molds and develop casting processes to ensure monolithic end results. All SLA printing done in this work utlized a Formlabs Form 2 printer unit. A thorough trial of several commercially available pre-made ce-

ramic resins showed that they were not comprised of monodisperse particles, but rather a slurry of varying frit sizes. This is shown in Figure 47.

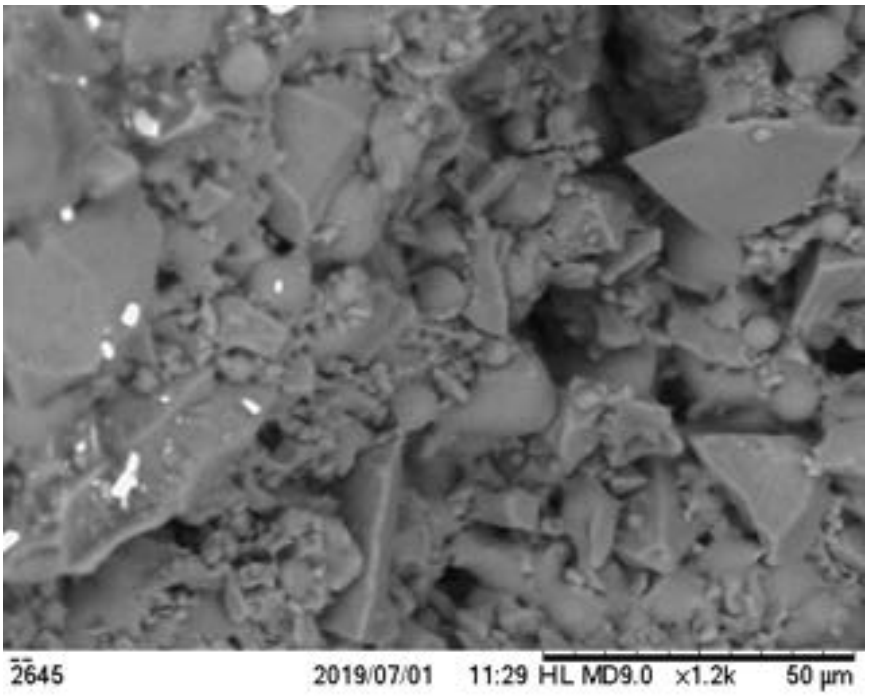

Figure 47: SEM image of one commercial ceramic resin for use in SLA 3D printing. Note the various particle dimensions.

Because of this non-uniform porosity, commercially available resins were not an option. Therefore, in order to enable 3D printing of monodisperse porous ceramics, a new photocurable resin with single diameter silica spheres would need to be developed.

7.4.2 UV-curable resin suspensions

One major hurdle overcome in this material development is the choice of UV-curable resin. As a starting point, alumina suspensions in photocurable resins from a previous work were used to create similar suspensions for the silica nanospheres. [16] Similar ratios prescribed in this work for Di-TMPTA, HDoDA, ACMO, 1-Hydroxycyclohexyl phenyl ketone photo initiator, KH560 silane coupling agent, and NPG2PODA were used as a baseline. A spreadsheet is used to calculate the appropriate ingredient masses for a prescribed total batch mass and mass loading fraction (see Figure 48). While this resin showed full uv-curing for 1mm substrates within 1 hour of ambient exposure, they lacked

Inputs	
Total Batch Mass (g)	20.000
Proportion Powder	0.750
Proportion NPG2PODA	0.700
Silica Particle Size (microns)	1.500
1 for Modified, 0 for Unmodified	1.000
UV-Curable Resin	**Mass (g)**
Total	5.000
Powder	**Mass (g)**
Silica Monodispersed Powders	14.700
KH560	0.300
Ethanol	4.204
Total	15.000
Grand Total (Check)	20.000

Figure 48: Spreadsheet used to calculate the respective ratios for photocurable resin/silica suspensions.

the viscosity necessary to prohibit the nanospheres from precipitating to the bottom of the mix. Even at high mass loading fraction of 85 percent, the spheres showed clumping characterstics that could prove troublesome.

However, due to the proliferation of hobbyist SLA printing, there are several commercially available photocurable resins available for suspension creation. Tethon 3D's Genesis developmental base resin was found to be very suitable for this particular application as its load tolerance for powdered materials was very high compared to the initial trial resin made in-house. This allowed the material development effort to be focused on molding, curing, sintering and post-processing.

To facilitate a uniform dispersion of silica in the suspension prior to UV-curing, a surfactant was needed. KH560 and ethanol is mixed into the bead and resin slurry to keep the beads from binding to the resin and forming clumps and impacting uniformity.

Given that the ideal monodisperse porous ceramic would be completely uniform as seen by the incoming liquid, mass loading fraction needed to be maximized. This would

force the packing density up to facilitate better uniformity post-curing. This required a substantial amount of mixing to ensure the resin combined thoroughly with the beads to act as temporary adhesive during UV-curing. A combination of tumbler mixing and magnetic bead vortex mixing proved to be most effective for this step.

7.4.3 Molding

Given that this material development is motivated by the need to make monodisperse emitter tips, chip blanks must first be made. Once the preceding steps to form the silica/resin suspension are complete, the resin can be molded into shape. Seeing as how the silica loaded resin chips will be quite brittle after curing, a flexible mold is needed to keep the chips intact. Utilizing the SLA 3D printer, positive ABS plastic molds were created to make negative PDMS molds. PDMS is an excellent material for this application due to its largely UV-transparent nature and its flexibility. An ABS mold and its PDMS counterpart are shown in Figure 49.

With minor filleting and chamfering of the corners and edges in these molds, it was found that batch yield increased and micro-cracks in the chips edges could be effectively eliminated. Another caveat of this molding approach is scaleability. Chips 2cm by 2cm were created with minimal warping as well, suggesting with diligent dimensional ratio constraints, even larger chips could be made with sufficient UV source penetration.

7.4.4 UV curing

Given SLA is simply the process of layering photocurable resin suspensions and curing them with a UV source in pre-determined patterns to build up a structure, the approach to curing monolithic chips is that of one big "layer." Using the PDMS molds, the thoroughly mixed silica resin suspension is poured slowly into the molds to minimize air bubble formation. The PDMS mold is then covered with glass slides (lower UV transparency, but mold edges permit enough UV to cure) and placed into a UV light source for 10 minutes. This process is shown in Figures 50 and 51.

The UV source used for this step was a commercially available 80 watt UV nail polish

Figure 49: ABS and PDMS positive and negative molds used for casting the silica/resin suspension into chips.

curer. This was sufficiently strong to cure the approximately 1mm chips all the way through. For thicker substrates, a stronger source may be used to ensure penetration of the light into the chip core.

After curing, the chips are removed from the PDMS mold individually and checked for any obvious faults. The chips are then ready for the sintering oven to both remove the supporting polymer and fuse the silica spheres together slightly to form a porous structure.

7.4.5 Sintering

Perhaps the most delicate step in this whole process, sintering is a 24 hour long period of careful heat introduction to the cured chips. As a baseline, the commercially avail-

Figure 50: UV curing of the resin mix into solid chips. From left to right, the PDMS mold (gray) is filled with uncured resin (white), a glass slide (yellow) is used to keep the curing chips from warping, the UV source (purple) is activated and the chips are cured for 10 minutes.

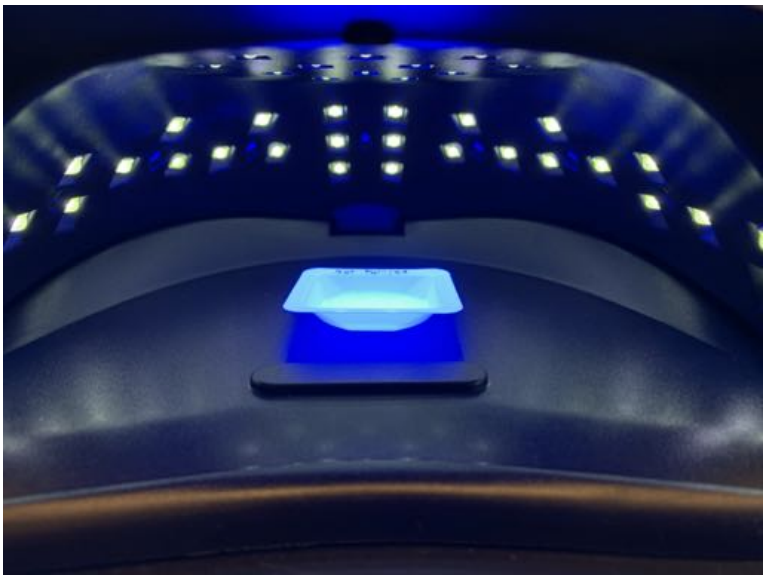

Figure 51: First trial of commercial UV source on a resin batch in an open-top teflon dish.

able SLA printer-compatible ceramic resins offered suggested sintering profiles for their cured resins. These generally consisted of a slow ramp up to a "burnout" temperature. This slow rate is necessary to not induce any thermal stress in the brittle chips. Once the burnout temperature is reached, a hold occurs to allow for all the supporting cured polymer to burn away, leaving only the silica nanospheres in their soon-to-be fixed state. Another ramp up occurs to sintering temperature for a short period determined by the chips desired thickness (for 1mm, 5 minutes was suggested) and then ramped down to ambient temperature. This ramp rate is also slow, again to avoid and thermal gradients inducing stesses on the chips. Several day long trials were conducted over weeks to determine the optimal sintering temperature. The two qualities used to determine this

were geometric overlap (with an SEM, one can see the extent of sintering by looking at the individual spheres) and relative chip strength. An undersintered chip would appear porous, but effectively turn to dust when handled. An oversintered chip would appear molten and the chip would be very strong. Two comparison SEM images of these conditions are shown in Figure 52. With several of these trials completed, the ideal sintering temperature for material handling strength and porosity was found to be 1125 C for 5 minutes. Shrinkage of this material during sintering was found to be approximately 18 +/- 2 percent in all three directions. The final product of this sintering process is shown in Figure 53.

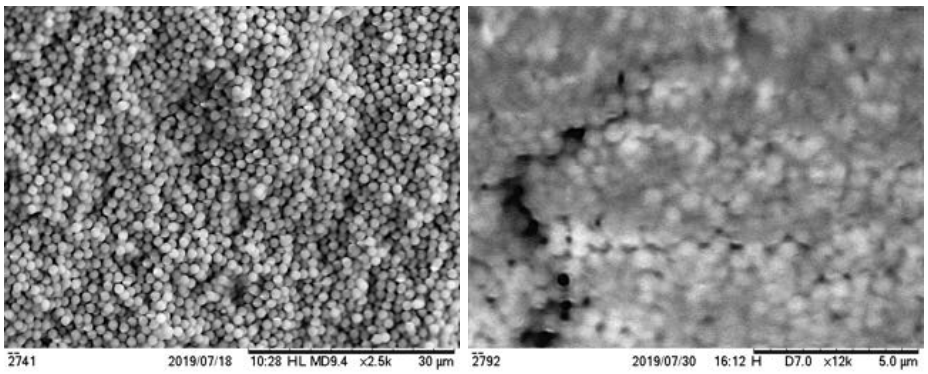

Figure 52: Shown left is a sintering trial resulting in under-fused spheres at a 1050 C hold temperature for 5 minutes. The chip did not retain its solid structure when handled. Shown right is an over-fused chip where the spheres melted together to form a solid ceramic. This chips was no longer porous after being held at 1200 C for 5 minutes.

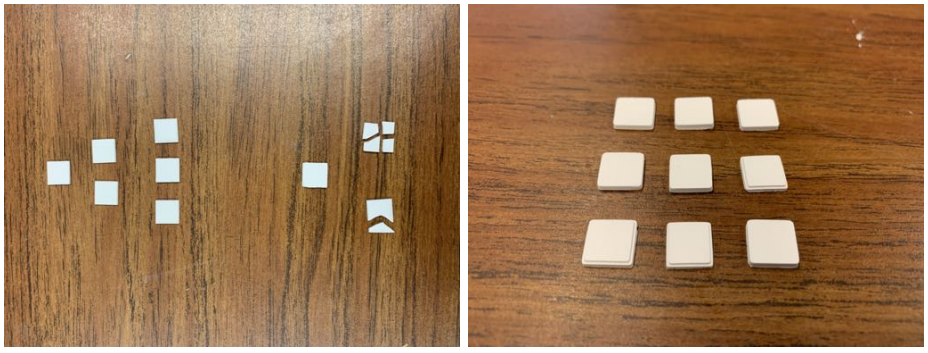

Figure 53: Sintered chips out of the oven. Note the fractured pieces during more aggressive temperature ramp trials.

7.4.6 Process flow

All of the trial-and-error of these different steps culminated in a final batch process flow as follows:

1. Calculate batch mass and input masses using pre-mix ratios.
2. Measure out an appropriate mass of silica powder, taking note to use the correct particle size (typically .75 micron diameter spheres).
3. Mix an appropriate mass of ethanol and KH560 into beaker.
4. Add silica to the beaker containing the ethanol-surfactant solution and mix until well incorporated.
5. Cover the beaker in parafilm, using electrical tape to secure the film around the mouth. Place in an ultrasonic bath for 60 minutes at 60 C.
6. After removing it from the ultrasonic bath, measure an appropriate amount of resin base into a clean plastic jar. For ratio development, Tethon3D's Genesis High Load Development Resin Base is used
7. Add the modified silica powder to the jar, using a stainless steel stirrer to mix the solution and break up any large chunks.
8. Once the silica is incorporated, add the stainless steel balls used in tumbler to the jar and seal tightly with a lid. Shake the jar vigorously for 5-10 minutes to remove the remainder of the small chunks.
9. Place the jar in its foam enclosure within the tumbler and ball-mill for 3-5 hours. The larger the batch the longer this process should be, however even microscopic chunks are typically eliminated within only a couple hours.
10. Remove the jar with the resin from the tumbler and put it on a Vortex mixer for 30 seconds.
11. Remove the lid from the UV source and place the PDMS mold within. Using a pipette, draw up more resin than needed to fill the chip wells, ensuring not to introduce any bubbles. Slowly deposit the resin into the chip wells in a continuous motion without allowing any air to reenter the pipette.

12. Place glass slides atop the wells to form a seal with the PDMS and eliminate the meniscus on each, ensuring that the upward-facing surface will be flat.

13. Replace the lid of the UV source and activate for 10 minutes, flipping the mold halfway through to allow curing of the bottom surface.

14. Delicately remove the cured chips from the PDMS molds, placing each on a flat surface and using a blade to remove any lip that forms from excess.

15. Place all cured chips immediately in a beaker with deionized water and place in the ultrasonic bath at room temperature for 30 seconds.

16. Place 9 - 12 chips on platinum film in a firing furnace. The chips should not touch each other or the ceramic surface of the furnace.

17. Fire according to pre-determined firing profile for resin base used and desire porosity. A typical firing profile is shown in Figure 54.

18. Use a diamond lapping wheel to polish chip surface for mounting and subsequent laser ablation.

From this point onward, the chip may be used much as the previous borosilicate material, being mounted to a frame with either epoxy or glass sealing paste and then patterned with a laser. Alternatively, chips can be mounted to a soda lime glass slide using Kapton tape for test patterning.

7.5 Batch evolution

This material development effort began in June of 2019. It took weekly batch trials for about 8 months to come to the point where this work discusses. Important variables were dialed in with each batch. Mixing, molding, UV curing, sintering, and general handling evolved with each batch trial. Figures 55, 56, 57, and 58 show this progress with notes on each of the noteworthy batches.

7.6 Laser ablation

Given the point of developing this material for use in electrospray thrusters, their ability to provide good tip geometry via laser ablation is crucial. While other means of forming

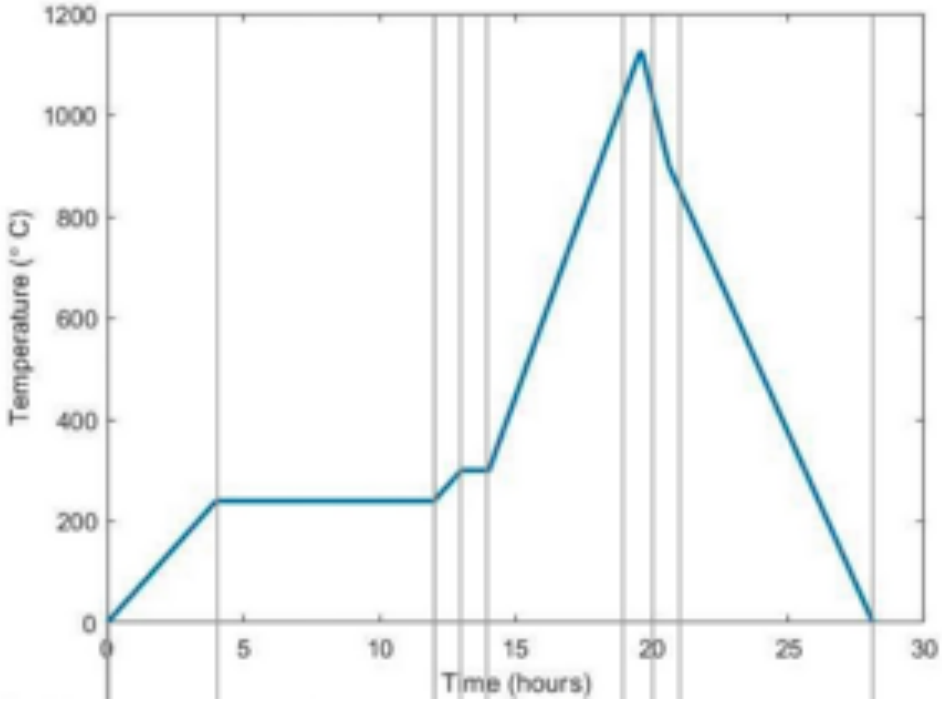

Figure 54: Sintering temperature profile for firing furnace. Note thickness of chips, desired porosity, base resin formulation, and nanoparticle diameter will alter profile regions.

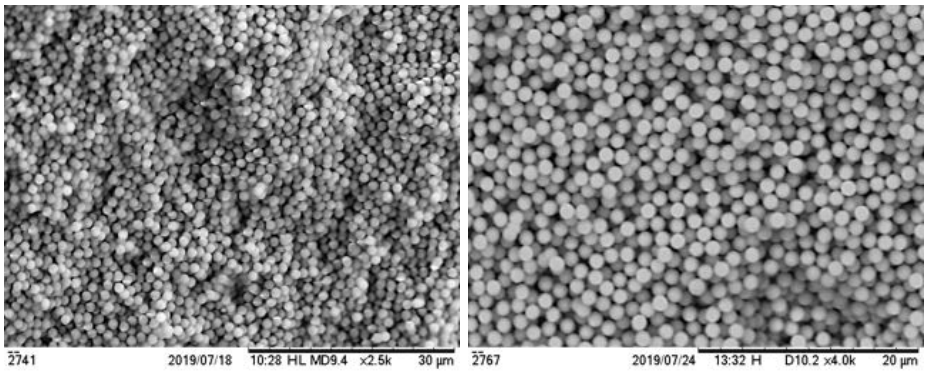

Figure 55: Left: first trial batch with Genesis resin. Underfused and nonuniform density dispersion. Right: third batch with improved mass loading, but still underfused and presenting edge uniformity issue in the chip.

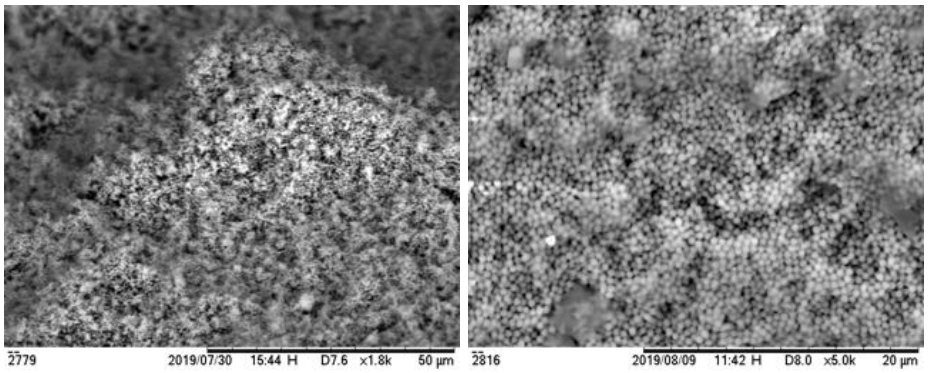

Figure 56: Left: Batch 6 fused well, but still fragile. Macroscopic voids pointed to issues with air bubble formation. Right: Batch 7 voids still present, and sintering temperature too high.

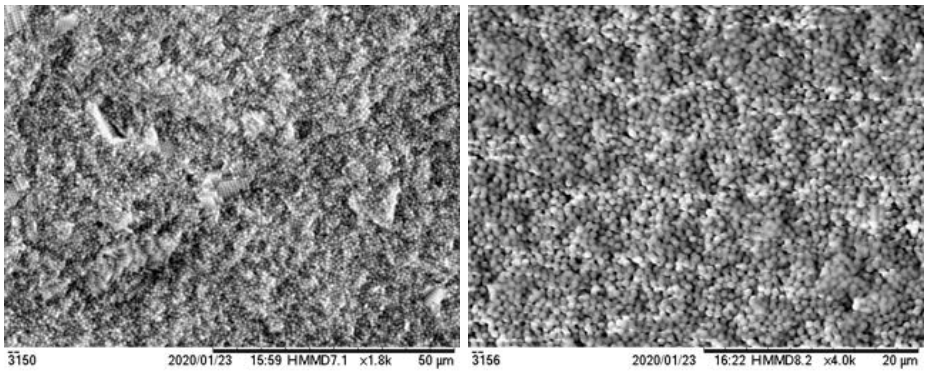

Figure 57: Left: batch 10 including ultrasonic mixing of silica nanospheres with surfactant. Much better uniformity with inclusion of perfect sphere packing in some regions (photonic crystals.) Right: penultimate batch including vortex mixing. Microscopic and macroscopic uniformity is much improved and the chip is easily handled without sacrificing wetting ability.

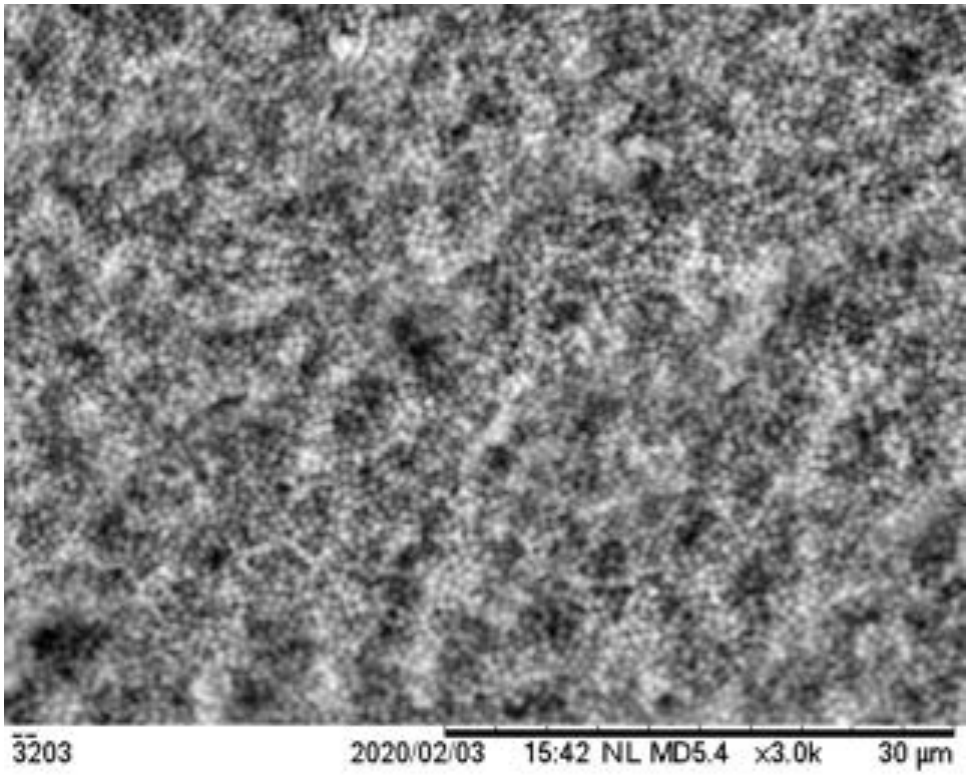

Figure 58: Final batch cross section of broken chip. Includes updated mold edge filets (0.25mm radius). Sintering is just enough to keep handling strength, wets easily with water and isopropyl alcohol. No edge uniformity issues or hairline cracks present.

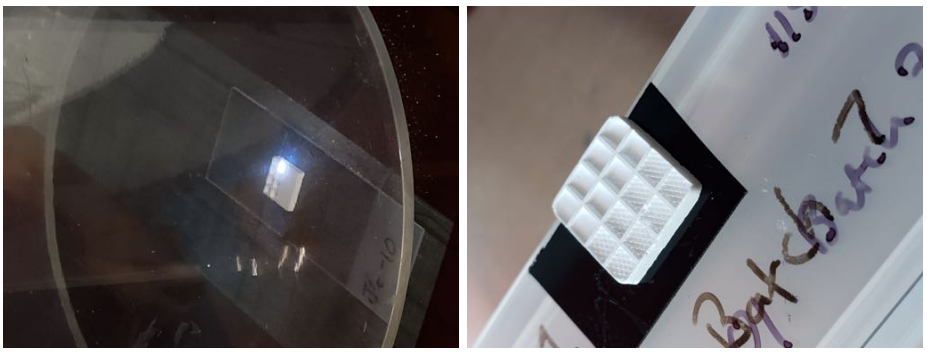

Figure 59: Left: test patterns being run on a sintered silica chip prior to thruster emitter ablation. Right: final test pattern result.

tips may be viable with this approach, the intial focus is on replacing borosilicate glass for use in laser ablation. Using a picosecond infrared laser in the 1-3 Watt range, several tip patterns were tested on batches 6, 8, and 10. The material was designated "JG" to appease the author's ego. This process is shown in Figure 59.

During the initial trials for batch 6, the ablation rate for the material was quite high. Visible debris was generated at the 3 watt power level. This debris interacted with the laser, reducing the resolution of the laser pattern and therefore affecting the tips as well. This is how the conclusion that batch 6's sintering temperature was slightly too low and allowed for the laser to break off many spheres at a time due to the low sintering bond strength. The ablation rate for this batch was roughly three times that of borosilicate glass. This first attempt at laser ablation is shown in Figure 60.

Following the lessons learned from batch 6 laser ablation trials, batch 8 found a better sintering temperature of 1100 C. This batch was sent back to the laser to run a 9 variation test pattern on a single chip. The best looking tips are shown in Figure 61. These chips showed much better tips in the center region where the uniformity was consistent. Near the edges of the chips, density appeared to be different. This was thought to be due to mold and UV curing issues. A combination of mold fillets and higher mass loading in batch 10 appeared to alleviate this. The narrow tip geometry indicates a high ablation rate, so lower laser power and more passes was the next logical step.

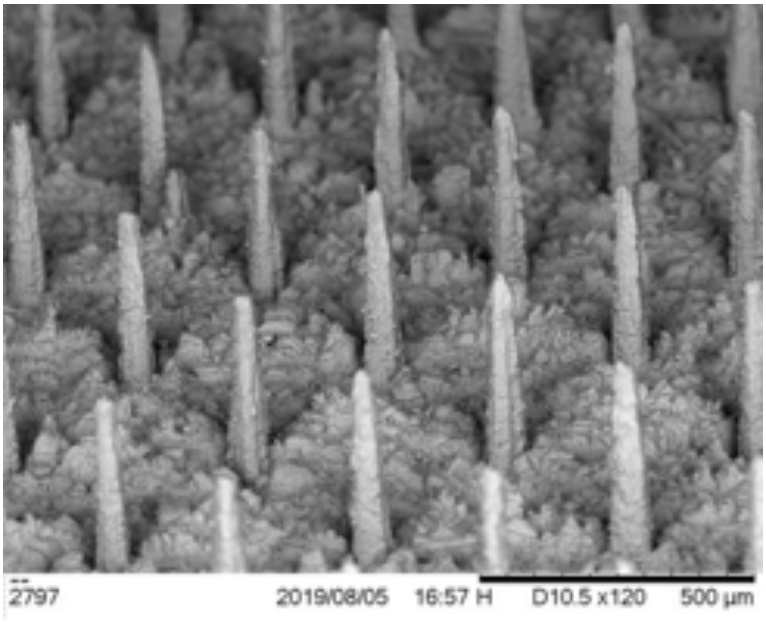

Figure 60: First trial of monodisperse sintered silica laser ablation (batch 6).

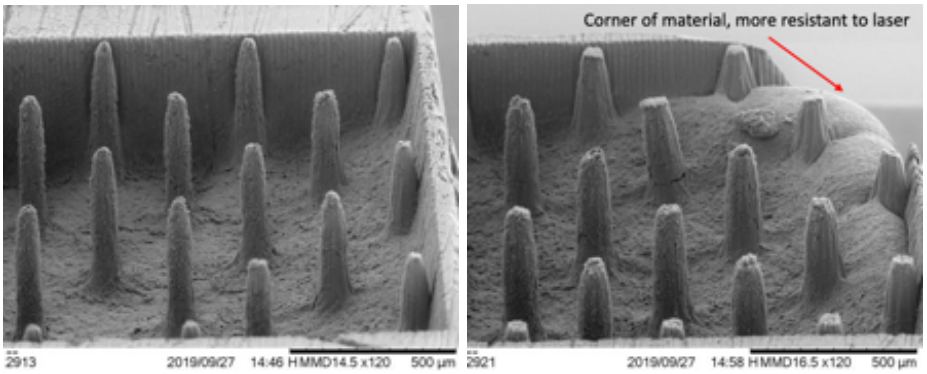

Figure 61: Batch 8 laser ablation results for test patterns. Note the edge density changes due to mixing and molding issues later resolved in batch 10.

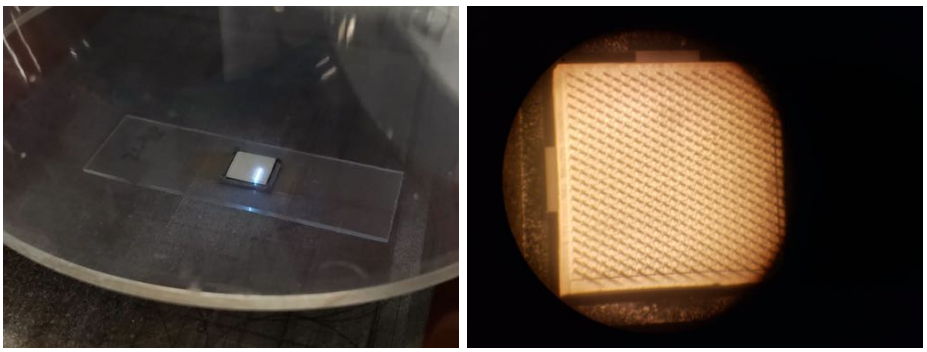

Figure 62: Patterning of JG emitters on thruster frames from batch 10.

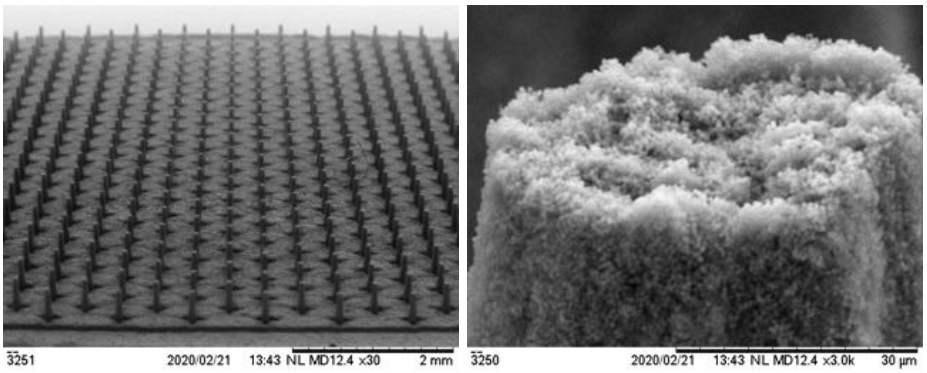

Figure 63: Left: a patterned JG emitter. Right: A tip of a JG emitter. Note the blunt edge due to laser pattern not closing the tip point fully. Post ablation BOE dip smooths these features well.

Following the largely successful ablation of batch 8 chips, a second development trial was conducted. The batch 10 chips incorporated filleted mold edges, and an ultrasonic mix of the silica and surfactant to decrease sphere clumping. The sintering temperature was also increased to 1125 C to further decrease the ablation rate to the point of negligible debris interference. Two full emitter arrays were made following another test patterning. This process and the outcome is shown in Figures 62, 63, and 64.

The current state of this porous sintered silica ceramic is quite promising. Deemed "JG", the tip geometry achieved via laser ablation suggests much tighter tip packing can be achieved due to the higher aspect ratio of each respective tip. The wetting of this material is on par with borosilicate glass. The thoroughly mixed resin holds suspension for several hours, possibly opening the door to more complex molding tasks. This material, when sintered fully, may offer a replacement for current thruster frames. Additionally,

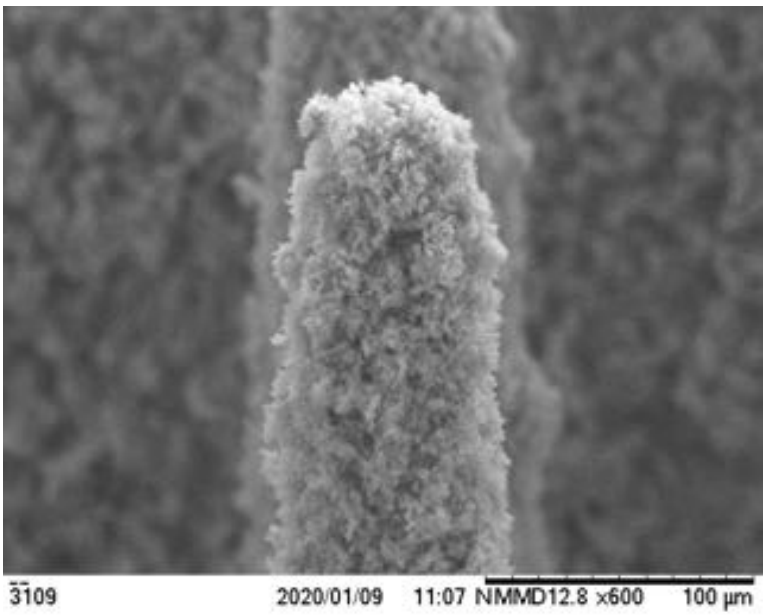

Figure 64: A patterned JG test chip. No plateau is present for this particular pattern. Tip radius is approximately 15 μm.

the cost of producing this JG material is almost negligible, and any decrease in cost for materials trickles down to any system it inhabits. All of these characteristics culminate in a successful first thruster firing that will be discussed in further detail in the thruster firing section of this thesis.

8 Thruster firing results

With the new monodisperse silica ceramic developed far enough to be laser ablated into emitter tips, thruster firing was the next step. A patterned array from batch 10 in December 2019 was coupled with an extractor after cleaning to be test fired. It should be noted that this emitter chip had nearly two thirds of its tips lost due to improper handling, but could still fire and provide useful insights.

8.1 Thruster firing data

When characterizing electrospray thruster performance, it is important to first note the start-up voltage. This is the voltage at which the meniscus at the emitter tip is under sufficient electric force to begin the extraction of ions. Tip material has little effect on this value. It is largely driven by tip geometry and chemistry of the propellant utilized. The tip geometry refers to sharpness (radius of curvature of the tip), the spacing between that tip and the extractor grid aperture, and the pore size. The smaller the radius of curvature, the lower the start-up voltage. The closer the tip is to the extractor, the lower the start-up voltage. The pore size directly controls the hydraulic impedance which, in turn, correlates to start-up voltage; larger pores tend to enable lower start-up voltage. For the current iEPS thruster PPU, a start-up voltage in the high hundreds of volts gives headroom for more thrust with higher voltages.

By recording a sweep of voltage in both polarities and measuring both emitted current and electrode intercepted current, an "I-V" curve can be plotted. The emitted current is the ions leaving the emitter while the intercepted current is ions that hit the electrode of the thruster and are effectively power/efficiency losses. It will be made apparent that the positive and negative bias operational differ in their emitted and intercepted current values. This is largely due to different masses of the positive and negative ions present in the ionic liquid. For the purpose of this thesis, 1-Ethyl-3-methylimidazolium tetrafluoroborate (EMI-BF4) is the ionic liquid used for thruster firings.

8.1.1 Time-of-flight spectroscopy

TOF spectroscopy is conducted based on the fact that at a constant potential, various species of ions present in ionic liquids will be accelerated to different velocities governed by the following equations:

$$t_{arrival} = \frac{L}{\sqrt{\frac{2q_i}{m_i}V}} \tag{4}$$

$$v_i = \sqrt{\frac{2q_i}{m_i}V} \tag{5}$$

$$\tag{6}$$

where L is the distance between the thruster emitter and the TOF detector, q_i is the ion species charge, m_i is the ion species mass, and V is the accelerating potential applied. Once the thruster is activated at a fixed voltage, the various ion species will arrive at the detector at varying times (on the order of microseconds generally). This, in turn, varies the current measured on an oscilloscope. This would be simple if startup transient behavior was negligible in electrospray thruster. Since it is not, the thruster is activated for a few seconds while pointing at a gate that is then "opened" to transmit the beam to the detector without any transient behaviors being seen. The gate used in the SPL setup is an electrostatically actuated one. This action can be repeated at very high frequencies to give a smooth averaged plot of flight times. Shown in Figure 65 is a schematic depicting the SPL TOF spectroscopy setup. [14]

The general procedure to operate this diagnostic system is noted in [14]. Voltage is cycled on-and-off at 100 Hz which gives 5 ms per 'on' period. This is long enough to capture any droplets which can have flight times on the order of 1 ms.

8.2 JG silica

To characterize the performance of the first patterned partial JG emitter, both IV curve data and TOF data was captured during firing. The JG thruster used in this work was not ideal, however, due to time constraints and all physical presence in the lab being

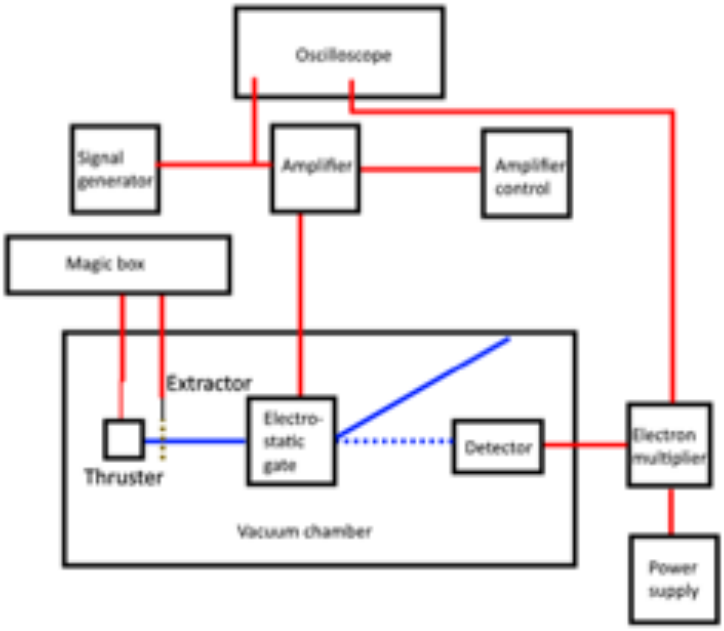

Figure 65: A depiction of the TOF diagnostic system. Coaxial connections are shown in red and the ion beam in blue. The dashed line represents the beam path once the gate is opened. The "magic box" is a system that applies voltages and measures currents on multiple channels implemented by Fernando Mier-Hicks. [14]

restricted around the time of firings. The thruster used was initially made during a laser ablation development day and was unfortunately damaged in handling. That being said, approximately one third of the thruster tips remained and the beam quality should not be impacted by number of tips. The height between the extractor and the tips did vary slightly, so intercepted current was likely to be a bit high from the start. The tips that did survive were quite good though. This will show in the following data sets collected.

8.2.1 JG IV curve

The JG silica ceramic thruster initially began emitting ions at approximately 1400 Volts and showed stable operation down towards approximately 900 Volts. This can be attributed to some warm-up behavior in the tip wetting, and the startup voltage was closer to the 900 V point for subsequent firings. Shown in Figure 66, the slight hump at 1400 Volts is due to the emission spike upon initial start-up. Following start-up, the emitted current reached approximately 400 μA before signal saturation occurred. This is quite promising given the number of tips present and their less-than-prestine condition. The

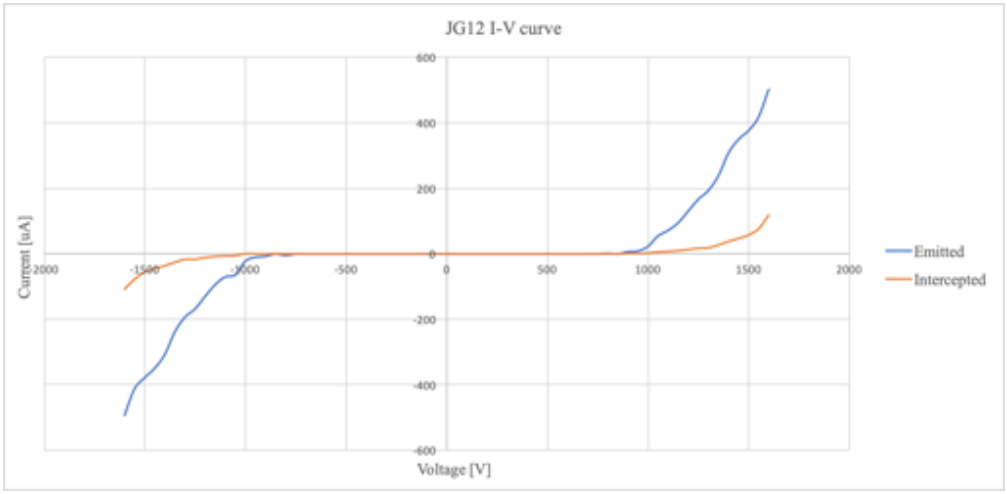

Figure 66: JG silica ceramic partial array thruster IV curve. The intercepted current is quite high, nearing 10-15 percent for higher voltages.

thruster showed very similar behavior in the negative polarity, with start-up occurring a bit lower around 1000 Volts.

The maximum current was recorded at just over 1600 volts. After approximately 30 minutes of relatively stable firing, the thruster began to show signs of small shorts forming. These small short-lived shorts developed into a life-ending short most likely due to the intercepted current and/or a liquid bridge reaching the extractor. Given a tighter laser pattern and possible post-cleaning BOE dip, these tips can be sharpened, further reducing the start-up voltage. Overall, a very promising IV curve performance from the little bullied thruster was achieved. By comparison, a full-array borosilicate emitter provides current emissions around 150 μA typically.

8.2.2 JG12 time-of-flight attempt

An attempt to gather time-of-flight spectroscopy results proved unreliable due largely to the thruster developing shorts around the time the data was collected, limiting the thruster to negative polarity operation only. Time-of-flight will dictate whether or not these new tips are firing in the purely ionic mode or include droplet emission. It should also be noted that this thruster was discolored after firing (shown in Figure 67.) Future tests of full arrays with sharpened tips will provide the insight needed to properly char-

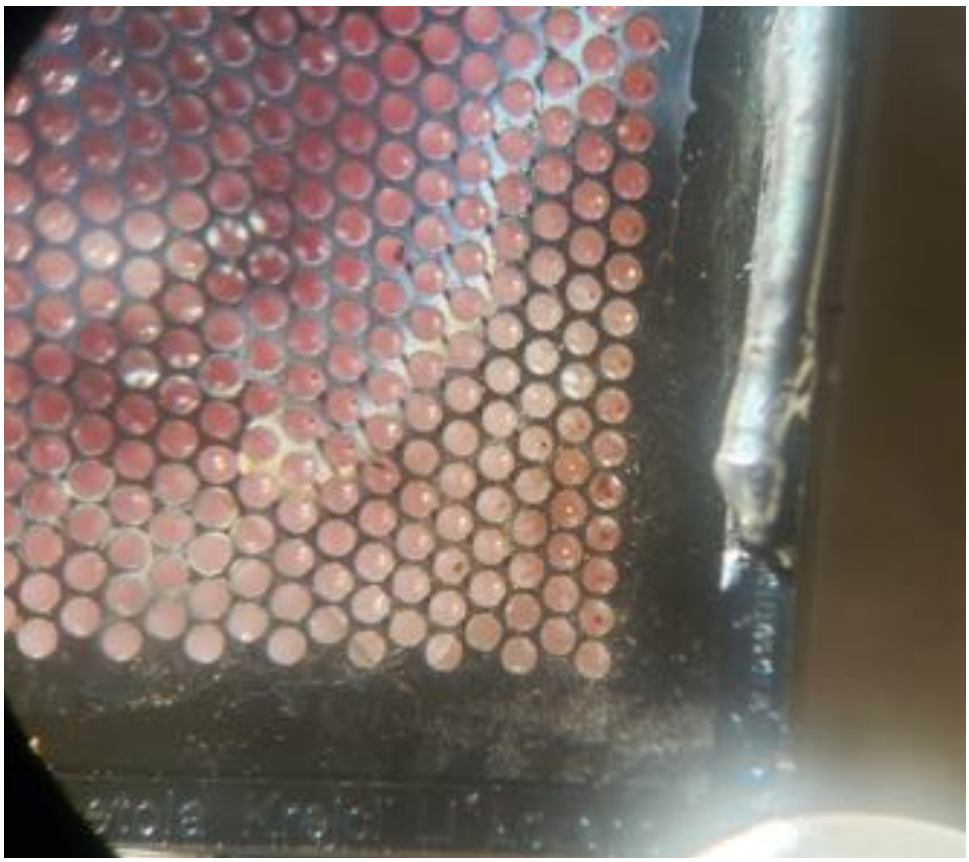

Figure 67: The JG12 partial-array thruster after firing shows signs of discoloration.

acterize the emitter performance. Further material testing is also needed to verify the viability of the material as an emitter substrate candidate.

9 Conclusions and Continued Research

This thesis covered a range of development work applicable to the ion electrospray propulsion system. Frame fabrication was altered to attain a 100% post-dicing yield. A new flow regulating electrowetting valve has been designed and fabrication procedures tested and drafted. A new monodisperse porous silica ceramic material was developed to enable casting of emitter substrate chips for laser ablation. Some important conclusions should be noted relevant to the tests carried out.

Firstly, fabrication procedural changes to the fabrication of the thruster frames enabled a significant yield improvement. Through improved photolithography and cleaning steps, the wafers were better prepared for anodic bonding. The bonding step, in particular, incorporated a final switch in polarity during the last bond layer to hypothetically smooth the charge layer. This switch in polarity provided a 100% post-dicing yield with only one post loss due to handling. This is an improvement of approximately 20% compared to prior fabrication processes for the frames.

Secondly, a new flow regulating electrowetting valve. After many design iterations and several etch trials, a final development valve wafer design was settled on. Its capillaries and channels fully etched, time constraints kept the final etch from being completed. Once completed, the valve designs on the wafer can be diced, PTFE coated, and tested to verify against on-going simulations of expected flow characteristics. The potential performance gains in reliability and thruster throttling ability would be significant. Further development of fabrication and testing trials will inevitably refine this component.

Lastly, a major success in material development of a highly-tunable photoactive porous ceramic resin process was reported. This monodisperse ceramic can be mixed, cast, sintered, and laser ablated in the course of week for mere pennies per chip. Utilizing commercially available photoactive polymers, UV curing, in-house 3D printing, and a number of very ambitious undergraduate researchers, this material shows great promise. Incorporation of larger spheres to form a dual dispersion structure will enable further porosity control in future emitter tips. Laser ablation results of the current monodis-

perse recipe showed good geometry with possibly much sharper tips attainable through laser pattern alterations. Firing data proved this emitter material is capable of flowing a great deal of propellant and providing a similar start-up voltage to borosilicate glass. Additional testing of TOF, retarding potential analyzer tests, and measurement of beam divergence will offer further insights into this material's performance and whether it can provide purely ionic emission. Furthermore, should the 3D printed cyanate ester frames not prove to be a suitable MEMS frame replacement, this material can also be sintered fully to give solid silica structures of any castable shape. Preliminary trials show this material may be a suitable frame material candidate.

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Appendix - Fabrication Process Flows

L1 full process flow				
Materials: 150mm x 1mm DSP <100>N-type Si wafer				
Step	**Process**	**Machine**	**Time**	**Comments**
0.0	**RCA Clean**	**RCA wet station**		
.1	SC1		10	5:1:1 DI water : NH_4OH : H_2O_2 at 75°C
.2	Rinse and dry		15	5 dump/rinse cycle, spin dry
.3	Oxide removal		1	50:1 DI water:HF
.4	Rinse and dry		15	5 dump/rinse cycle, spin dry
.5	SC2		10	6:1:1 DI water: HCl: H_2O_2 at 75°C
.6	Rinse and dry		15	5 dump/rinse cycle, spin dry
1.0	**Wet Thermal Oxidation**	THERMCO furnace	272	Grow 500 nm; 2x 100 minute runs
2.0	**Nested Mask Patterning**			
.1	HMDS	HMDS machine	22	Use process 1 for SPR-700
.2	Thin resist coating	Coater-TRL	2	Top side, 1.3 μm SPR-700 at 2kRPM
.3	Soft bake resist	prebake oven	30	30 minutes 95°C
.4	Expose pattern	EV-620	3	Mask: top side, L1 Pedestal, 3 second exposure
.5	Develop		2	2 minutes in MF-CD-26
.6	Rinse and dry	SRD	11	Rinse and dry in SRD
.7	Inspect pattern	Fluoroscope	1	Ensure proper development and quality
.8	Hard bake resist	postbake oven	30	30 minutes at 120°C
3.0	**Oxide Patterning**	**acid-hood**	**30**	
.1	Buffered oxide etch		10	Straight from bottle, use plastic only
.2	Rinse and dry	SRD	5	
.3	Strip resist		10	Piranha, use quartz only
.4	Rinse and dry	SRD	5	
4.0	**Photolithography**			
.1	HMDS	HMDS machine	22	Use process 0, for AZ-4620
.2	Thick resist coating	coater-TRL	6	Top side: 10 μm, back side: double layer 10 μm ea. Bake 8 min. between coatings
.3	Soft bake resist	prebake oven	60	60 minutes at 95 °C
.4	Expose pattern	EV-620	10	Top side: Moat and well mask, 22s constant exposure. Back side: Through etch mask, 3x 15s on, 20s off.
.5	Develop		4	Develop in AZ435, roughly 4 min, until excess sloughs off.
.6	Rinse and dry	SRD	10	
.7	Inspect pattern	Fluoroscope	1	Ensure proper development and quality
.8	Hard bake resist	prebake oven	30	30 minutes at 95°C, \textbf{not} 120°C
5.0	**DRIE**			
.1	Etch alignment marks	STS-2	4	Top and back side: 20s etch, pure SF_6 etch
.2	Tape alignment marks			Use kapton tape, protect alignment marks and any scratches on back side and edges.
.3	Deep feature etch	STS-2	240	Back side, etch 750 μm.
.4	Check depth	Microscope		Ensure etch is deep enough; check fringes in scope
.5	Tape back side			Use blue tape, cut relief points around etches; protect top side alignment marks. Protect wafer edges.
.6	Moat and well etch	STS-2	120	Top side, etch through.
.7	Remove tape	prebake oven		Bake 5 min. at 95 °C to weaken adhesive.
.8	Ash	asher	30	30 minute ash to remove fluoropolymer
.9	Strip resist	acid-hood	10	Piranha
.10	Rinse and dry	SRD	5	
.11	Tape back side			Use Kapton tape, protect alignment marks
.12	Etch pedestals	STS-2	20	20 minute etch, etch 30-40 μm.
.13	Remove tape	prebake oven		Bake 5 min. at 95 °C to weaken adhesive.

Table 2: Detailed L1 process flow

Insulating layer full process flow				
Materials: 150 mm x 0.5 mm Corning 7740 Borosilicate wafer				
Step	**Process**	**Machine**	**Time**	**Comments**
0.0	**Cleaning**	**acid-hood**		
.1	Organic clean		10	Piranha
.2	Rinse and dry	SRD	5	
1.0	**Alignment mark masking**			
.1	HMDS	hmds machine	22	
.2	Thin resist coating	coater-trl	3	Coat both sides, 1 μm SPR-700
.3	Soft bake resist	prebake oven	30	30 minutes at 95°C
.4	Expose pattern	EV-620	3	Both sides: insulating layer mask, expose 3.5s
.5	Develop		2	75 s in MF-CD-26
.6	Inspect pattern	Fluoroscope		Check pattern development and resolution
.7	Hard bake resist	postbake oven	30	30 minutes at 120°C
2.0	**Alignment mark etch**			
.1	Buffered oxide etch	acid-hood	10	Use plastic beaker.
.2	Rinse and dry	SRD	5	
.3	Strip resist	acid-hood	10	Piranha, use quartz beaker.
.4	Rinse and dry	SRD	5	
3.0	**Polysilicon deposition**	**LPCVD**	**360**	**Deposit 250 nm; staff run process**
4.0	**Hard mask photolithography**			
.1	HMDS	hmds machine	22	
.2	Thin resist coating	coater-trl	3	Coat both sides, 1 μm SPR-700
.3	Soft bake resist	prebake oven	30	30 minutes at 95°C
.4	Expose pattern	EV-620	3	Both sides: insulating layer mask, expose 3.5s
.5	Develop		2	75 s in MF-CD-26
.6	Inspect pattern	Fluoroscope		Check pattern development and resolution
.7	Protect alignment marks			Dispense SPR-700 into dish, paint onto alignment marks and edges
.8	Hard bake resist	postbake oven	30	30 minutes at 120°C
5.0	**Hard mask etching**	**STS-1**	**10**	**Both sides, 20s pure SF6**
6.0	**Wet etching**	**acid-hood**		
.1	HF through etch		60	55 minutes in HF (from botttle). Use plastic ware.
.2	Rinse and dry	SRD	5	
.3	Strip resist		10	10 min. piranha
.4	Rinse and dry	SRD	5	
.5	Strip polysilicon		10	HNA wet etch; 20:20:1 CH_2COOH:HNO_3:HF. Add acetic first, then nitric, then hydrofluoric. Use plastic ware and ensure free of contamination.
.6	Rinse and dry	SRD	5	

Table 3: Insulating layer detailed process flow.

L3 full process flow				
Materials: 150 mm x 0.5 mm DSP <100>N-type Si wafer				
Step	**Process**	**Machine**	**Time**	**Comments**
0.0	**RCA Clean**	**RCA wet station**		
.1	SC1		**10**	5:1:1 DI water : NH_4OH : H_2O_2 at 75°C
.2	Rinse and dry		**15**	5 dump/rinse cycle, spin dry
.3	Oxide removal		**1**	50:1 DI water:HF
.4	Rinse and dry		**15**	5 dump/rinse cycle, spin dry
.5	SC2		**10**	6:1:1 DI water: HCl: H_2O_2 at 75°C
.6	Rinse and dry		**15**	5 dump/rinse cycle, spin dry
1.0	**Wet Thermal Oxidation**	THERMCO furnace	272	Grow 500 nm; 2x 100 minute runs
2.0	**Nested Mask Patterning**			
.1	HMDS	HMDS machine	22	Use process 1 for SPR-700
.2	Thin resist coating	Coater-TRL	2	Both sides, 1 μm SPR-700 at 3kRPM. Bake 8 min. between coatings
.3	Soft bake resist	prebake oven	30	30 minutes 95°C
.4	Expose pattern	EV-620	3	Mask: top side, alignment crosses. 3.5 second exposure.
.5	Develop		2	75 seconds in MF-CD-26
.6	Rinse and dry	SRD	11	Rinse with water in sink, dry lightly with N_2
.7	Inspect pattern	Fluoroscope	1	Ensure proper development and quality
.8	Hard bake resist	postbake oven	30	30 minutes at 120°C
3.0	**Oxide Patterning**	**acid-hood**	**30**	
.1	Buffered oxide etch		10	Straight from bottle, use plastic only
.2	Rinse and dry	SRD	5	
.3	Strip resist		10	Piranha, use quartz only
.4	Rinse and dry	SRD	5	
4.0	**Etch alignment marks**	**STS-2**	**4**	**Top side: 20s etch, pure SF_6 etch**
5.0	**Photolithography**			
.1	HMDS	HMDS machine	22	Use process 0, for AZ-4620
.2	Thick resist coating	coater-TRL	6	Both sides: 10 μm. Bake 8 min. between coatings
.3	Soft bake resist	prebake oven	60	60 minutes at 95 °C
.4	Expose pattern	EV-620	10	Top side: Post pedestals masks, 4x 15s on, 15s off. Back side: L3 through masks, 7x 30s on, 30s off.
.5	Develop		4	Develop in AZ435, roughly 4 min, until excess sloughs off.
.6	Rinse and dry	SRD	10	
.7	Inspect pattern	Fluoroscope	1	Ensure proper development and quality
.8	Hard bake resist	prebake oven	30	30 minutes at 95°C, \textbf{not} 120°C
6.0	**Oxide Patterning**	**acid-hood**	**30**	
.1	Buffered oxide etch		10	Straight from bottle, use plastic only
.2	Rinse and dry	SRD	5	
.3	Strip resist		10	Piranha, use quartz only
.4	Rinse and dry	SRD	5	
7.0	**DRIE**			
.1	Tape alignment marks			Use kapton tape, protect alignment marks and any scratches on top side and wafer edges.
.2	Deep feature etch	STS-2	75	Top side, etch at least 150 μm
.3	Check depth	Microscope		Ensure etch is deep enough; check fringes in scope
.4	Tape top side			Use blue tape, cut relief points around etches; protect back side alignment marks and wafer edges. Can also mount to handle wafer.
.5	Through etch	STS-2	120	Back side, etch through
.6	Remove tape	prebake oven		Bake 5 min. at 95 °C to weaken adhesive.
.7	Ash	asher	30	30 minute ash to remove fluoropolymer
.8	Strip resist	acid-hood	10	Piranha
.9	Rinse and dry	SRD	5	
.20	Tape back side			Use blue tape, protect alignment marks
.12	Etch pedestals	STS-2	20	15 minute etch, etch 30-40 μm.
.13	Remove tape	prebake oven		Bake 5 min. at 95 °C to weaken adhesive.

Table 4: Aligmnent layer detailed process flow.

Detailed valve process flow				
Materials: 150 mm X 0.675 mm SSP Test wafer				
Step	**Process**	**Machine**	**Time**	**Comments**
0.0	**Cleaning**	**acid-hood**		
.1	Organic clean		10	Piranha
.2	Rinse and dry		5	
2.0	**Thick oxide deposit**	**STS-CVD**		**Deposit 1 μm**
3.0	**Photolithography**			
.1	HMDS	HMDS machine	22	
.2	Thick resist	coater-trl		Top side: 6 μm AZ-4620 Back side: 10 μm AZ-4620
.3	Soft bake resist	prebake oven	30	Bake 30 min. at 95°C
.4	Expose patterns	MLA	5	Top side: Valve capillaries Back side: Field squares
.5	Develop		4	Develop in AZ435 until excess sloughs off, roughly 4 mins.
.6	Rinse and dry	SRD	5	
.7	Inspect pattern	Fluoroscope		
.8	Hard bake resist	post-bake oven		
4.0	**Dry oxide etch**	**LAM-570**	**20**	4x 2 minute etch, 2 minute cool cycles
5.0	**DRIE**			
.1	Protect align marks			T
.2	Undercut oxide	STS-1	10	Topside: 30s. SF_6 isotropic etch
.3	Etch 200 μm		120	Topside: etch 120 mins, approx. 200 μm.
.4	Tape back side			Use blue tape, cut relief holes around dies.
.5	Etch through	STS-1	150	Expose capillaries
.6	Remove tape	pre-bake oven	5	Bake 5 mins. at 95°C to soften adhesive.
6.0	**Post clean**			
.1	Ashing	asher	30	
.2	Strip resist	acid-hood	10	Piranha
.3	Rinse and dry	SRD	5	
7.0	**Thick oxidation**	**THERMCO furnace**	**272**	Deposit 1 μm, Allow furnace to cool overnight before second oxidation
8.0	**Thick oxidation**	**THERMCO furnace**	**272**	Deposit 1 μm
9.0	Dicing			
.1	Mount on dicing tape		3	
.2	Protect dies		3	Use another layer of dicing tape
.3	Dice wafer	diesaw-3240	150	Black glass blade, two passes per cut.
.4	Dismount dies		30	Acetone and UV

Table 5: Detailed valve process flow.

Wafers: Prime silicon, 150mm, DSP, 675um thick

1. Cleaning
    a. TRL acidhood, 10 min piranha
2. Thick oxide CVD
    a. STS-CVD, deposit 1 micron
3. Photolithography
    a. TRL HMDS
    b. Coat 6um thick resist both sides
    c. Prebake 1hr
    d. Expose on MLA
    e. Develop
    f. Postbake
4. Oxide etch
    a. LAM590, 9 minute CF4 etch @ 850 W
5. Deep feature etch
    a. TRL STS1, 1hr topside etch
6. Photolithography
    a. TRL HMDS
    b. Coat 6um thick resist both sides
    c. Prebake 1hr
    d. Expose on MLA
    e. Develop
    f. Postbake
7. Deep feature etch
    a. TRL STS1, 2hr topside etch
    b. Mount to handle wafer
    c. TRL STS1, 3 hr backside etch
8. Cleaning
    a. TRL asher, 30 min
    b. TRL acidhood, 10min piranha
    c. TRL asher, 30 min
9. Secondary thick conformal oxidation
    a. TRL wet thermal oxidation, tube B1, 1um oxide deposition
    b. TRL wet thermal oxidation, tube B1, 1um oxide deposition
10. Dicing

Figure 68: Basic development process for flow controlling valve based on electrowetting valve process with added photo and DRIE steps.