Electrical System Design for Wafer-like Satellite

by

Xavier Alexander Zapien

B.Sc., Massachusetts Institute of Technology (2019)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Master of Engineering in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

May 2020

Author .....
Department of Electrical Engineering and Computer Science
May 19, 2020

Certified by .....
Rebecca Masterson
Principal Research Scientist
Thesis Supervisor

Accepted by .....
Katrina LaCurts
Chair, Master of Engineering Thesis Committee

Electrical System Design for Wafer-like Satellite

by

Xavier Alexander Zapien

Submitted to the Department of Electrical Engineering and Computer Science
on May 19, 2020, in partial fulfillment of the
requirements for the degree of
Master of Engineering in Electrical Engineering and Computer Science

Abstract

The miniaturization of electronics and reduced budgets for satellites have propelled the small-sat revolution for the past two decades[1]. The rapid growth of Small satellites has been driven by the increasing capability of Commercial Off the Shelf (COTS) products and their reduced Size, Weight, and Power (SWaP). This success could potentially be expanded by the use of microelectromechanical systems (MEMS) and microelectronics fabrication processes. MEMS processes have revolutionized the implementation of electronics in silicon wafers, greatly reducing the mass and area needed for components. MEMS could reduce the SWaP of a satellite to drive cost reduction and rapid manufacturing. WaferSat is a MIT Lincoln Laboratory project, with collaboration from the MIT Aero Astro Department, that is developing a wafer-scale satellite bus using microfabrication.. One of the first stages of developing WaferSat is proving the concepts and subsystems in a printed circuit board (PCB) form, named PCBSat. PCBSat contains the potential Power, Thermal, and computer subsystems of WaferSat. Designing the system in a PCB allows the student group at MIT to rapidly develop and test the systems that may be introduced into the wafer. If successful, many swarms of WaferSat could be in Low Earth Orbit (LEO) and conduct science with interferometry and other inter-satellite communication protocols. This thesis introduces the high level requirements of the WaferSat bus for exemplar sensing mission, and dives deeper into the design choices and trade-offs taken while designing the power system of the spacecraft. The Maximum Power Point Tracker, Battery Management Systems, and the Power Conversion circuits are designed in this thesis. The main challenges to this miniaturization are found in the power and thermal subsystems. The small form factor greatly limits the volume to store energy and the area to collect solar energy, creating a focus on efficiency in the power electronics of the system. These systems are developed to leverage past CubeSat designs with modern power efficient architectures and methods. Lastly, the efforts of this project set up the continued development of PCB-like satellites in the field.

Thesis Supervisor: Rebecca Masterson
Title: Principal Research Scientist

Acknowledgments

This work was supported by the MIT Lincoln Laboratory Technology Office, funded by the Office of the Under Secretary of Defense for Research and Engineering. It is released under Distribution Statement A: Approved for public release. Distribution is unlimited. This material is based upon work supported by the Under Secretary of Defense for Research and Engineering under Air Force Contract No. FA8702-15-D-0001. Any opinions, findings, conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the Under Secretary of Defense for Research and Engineering. I would like to start by thanking my Advisor, Dr. Rebecca Masterson for allowing me to join WaferSat and be part of the SSL family for this year. It has been a great experience for me and I've been able to grow as a person and as a researcher. Also thanks to Michael, Daniel, and Melissa for making WaferSat an enjoyable and challenging project to work on. Lastly, I am very thankful to all of the UROPs that worked with us over the past year. It has been a great time to work with you all and seeing you develop throughout your MIT career.

Contents

List of Figures

List of Tables

Abbreviations and Symbols

ΔI_L	Inductor Ripple Current
C_{in}	Input Capacitance
C_{out}	Output Capacitance
D	Duty Cycle
f_s	Switching Frequency
I^2C	Inter-Integrated Circuit
I_{MPP}	Maximum Power Point Current
I_{sp}	Specific Impulse
L	Inductance
SW	Switch
V_{in}	Input Voltage
V_{MPP}	Maximum Power Point Voltage
V_{out}	Output Voltage
AC	Alternating Current
ADC	Analog-to-Digital Converter
ADCS	Attitude Determination and Control System

ARM	Advanced RISC Machine
BJT	Bipolar Junction Transistor
BMS	Battery Management System
COTS	Commercial of the Shelf
CPU	Central Processing Unit
DC	Direct Current
DET	Direct Energy Transfer
DETRB	Direct Energy Transfer with a Regulated Bus
EP	Electric Propulsion
EPPS	Electrical Propulsion Power Supply
EPS	Electric Propulsion System
GEO	Geostationary Orbit
IC	Integrated Circuit
IMUSDA	IMU and EEPROM I^2C Bus
IV Curve	Current-Voltage Characteristic Curve
LCR	Inductor-Capacitor-Resistor Circuit
LEO	Low Earth Orbit
Li-Ion	Lithium Ion
LT	Linear Technology
MEMS	Micro-Electro-Mechanical Systems
MITLL	MIT Lincoln Laboratory

MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPPT	Maximum Power Point Tracker
MPPTBS	Maximum Power Point Tracker with Battery Bus
NASA	National Aeronautics and Space Administration
P&O	Perturb and Observe
PCB	Printed Circuit Board
PDM	Power Distribution Model
PLECS	Power Electronics Simulation Software from Plexim
PV	Photovoltaics
PWM	Pulse Width Modulation
PWRMGTSDA	Power Management I^2C Bus
SA	Solar Array
SEU	Single-Event-Upsets
SPL	Space Propulsion Laboratory
SSL	Space Systems Laboratory
SWaP	Size Weight and Power
SWaP-Sat	Size, Weight, and Power Development Satellite
TI	Texas Instruments
TID	Total Ionizing Doze
TMPSDA	Temperature Sensor I^2C Bus
WaferSat	Wafer Satellite

Chapter 1

Introduction

1.1 Motivation

The miniaturization of electronics and reduced cost or resource budgets for satellites have propelled the small-sat revolution for the past two decades[1]. The rapid growth of small satellites has been driven by the increasing capability of Commercial Off the Shelf (COTS) products and their reduced Size, Weight, and Power (SWaP). Ever since their conception at Stanford and Cal Poly in 1999, CubeSats have become prevalent in universities, startups, and commercial missions. The 10 cm cubes have been flown over 1000 times to Low Earth Orbit (LEO) and launched as far as Mars, accompanying the Insight Mars Lander in 2018[6]. CubeSats are considered nanosatellites (1kg - 10kg) and are much lighter than regular satellites (1000kg - 3000kg)[1]. Their low mass is an attractive feature since they can be launched as secondary payloads in rocket launches, reducing overall program cost. The success of CubeSats and the shrinking of electronics raises the question of whether satellites can be further downsized. This miniaturization could give rise to femtosatellites (100 g - 1kg) that could be created with printed circuit boards (PCB) or with Microelectromechanical systems (MEMS) and microelectronics processes [7]. These microfabrication processes reduce the involvement of human labor in the satellites, shortening the build-to-launch time and reducing labor costs. The manufacturability of this process also reduces the cost

[1]Based on data from the Nanosatellite Database https://www.nanosats.eu/

at large, despite high capital costs of the manufacturing facilities[7]. Femtosatellites open the door to low-cost swarm constellations that may enable satellite functions that have not been explored, such as the use of relay communication, interferometry, and sustained satellite maintenance. However this scaling may raise many challenges and limitations to the power, thermal balance, and capability of the satellites. The lack of mass results in rapid and difficult temperature swings for all subsystems. Limited volume also reduces the amount of storage that can be used for energy. These critical restrictions in turn will set a cap on potential femtosatellite payloads.

This project entails the design and testing of the initial revision of PCBSat, a printed circuit board femtosatellite prototype. PCBSat is part of the effort to developing WaferSat, a wafer-scale satellite bus manufactured with microfabrication processes. WaferSat is a joint effort from MIT Lincoln Laboratory (MITLL), MIT Space Systems Lab (SSL), MIT Space Propulsion Laboratory (SPL). WaferSat aims to go beyond other femtosatellite efforts by leveraging new technologies in electric propulsion, intelligent power systems, and smart thermal systems, while maintaining low cost and mass.

1.2 Literature Review

Femtosatellite development advanced considerably over the past decade and exhibited a future in which these devices can effectively collect data. Despite this progress, there are still some challenges to overcome. An effort in femtosatellite concept was attempted by the Surrey Space Center in 2015. This proposal introduced a satellite with two printed circuit board (PCB) satellites. This satellite included an electrical power system, an imager as the payload, attitude control, and passive thermal control[8]. Surrey' efforts demonstrated that a small satellite could be built for about $ 300 per unit. Cornell developed KickSat back in 2011, a crowd-funded CubeSat carrying chip satellites named "Sprites" with no on-board battery, that consisted of antennas, a microcontroller, solar cells, a gyroscope, and a magnetometer[9]. During its first flight, the Sprites were not released from KickSat while in orbit. It is

believed that there was an issue in the release timer of KickSat. Despite this issue, the project was extended and successfully launched in 2019. This time around, the Sprites communicated with the mothershipwith the help of the NASA Ames and Carnegie Mellon. KickSats's long term goals are to study weather patterns, animal migrations, and other terrestrial trends. In order to do complete these goals, KickSat must add more functionality in order to support more capable payloads. Some of these functionalities are attitude control, power storage, and a higher performance science instrument. One of the barriers to making femtosatellites scientifically useful and functionally similar to CubeSats is the inability to control their attitudes and orientations while in orbit. Due to their small size and tiny frontal area, there are few options that remain in propelling such spacecrafts. One of the most recent technologies that might enable this propulsion is Electrospray Propulsion (EP) . Electrospray Propulsion is a type of electric propulsion that has high specific impulse I_{sp} and is well matched to small satellites, since lower thrust is required to accelerate a smaller mass. Electric propulsion modules can also provide a much higher thrust to weight ratio than chemical propulsion systems due in part to the small form factor[10]. The thrust is a result of the acceleration created by ionizing gas and propelling these through a high voltage electric field. One downside of EP is its inability to thrust rockets beyond earth's gravity (10^7 N). On the contrary, it is a proper solution for steering or adjusting small satellites in orbit ($100mN$). One common type of EP is the ion engine, which ejects a small amount of gas flow out of perforations on a small plate and covers the tips of small silicon cones. A model of this type of engine is pictured in Figure 1-1. The bottom plate of the engine is connected to the cathode of a high voltage supply ($>$ 900 V) while a top plate, with small perforations above each cone, is connected to the anode of the same power supply. This 900 V electric field ionizes the fuel and causes the ions to flow out of the top plate and provide hundreds of millinewtons of thrust[11].

The small amounts of thrust and low power consumption are a good compromise for an efficient and capable propulsion system. Electric Propulsion's technology maturity has achieved a NASA TRL-6 level and has been used in many missions such

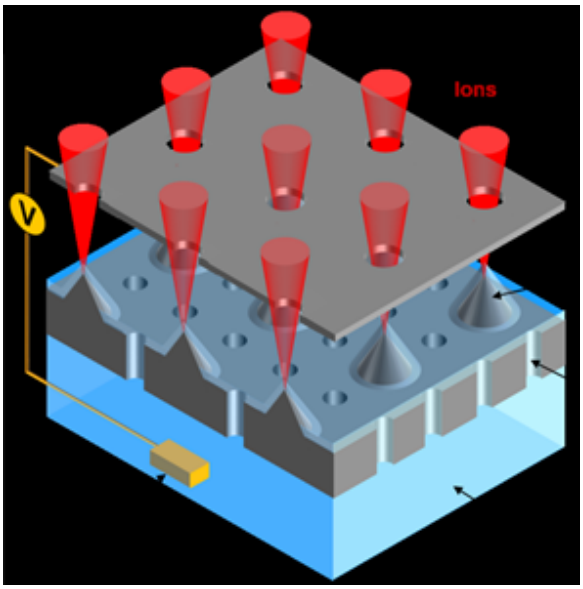


Figure 1-1: Ion Engine Model

as the Dawn and BepiColombo[11] [12] [13]. Continued development of EP will aid the transition of its use in more space missions. One of the issues regarding Electric Propulsion Systems (EPS) is the need for a large potential across their nodes (500V - 1.5 kV). This high voltage is commonly generated with a series of step converters including resonant Inductor-Capacitor-Resistor (LCR) circuits and capacitor multipliers. These circuits can be heavy, occupy a large surface area, and lead to more constraints on the power system due to their magnetics and capacitive components. One example of this high voltage converter was developed by the MIT Research Lab of Electronics to power an aircraft with no moving parts. Much like the process in electric propulsion, the large voltage ionizes the air between the plane's wings to generate a current of flowing ions and thus generate thrust[14]. This step is completed by using a series-parallel resonant converter, followed by a high-voltage transformer, and lastly, connected to a series of Cockroft-Walton voltage multipliers. As seen in Figure 1-2, there are three stages for this voltage converter: resonant inverter, transformer, and Cockroft-Walton voltage multiplier. It steps up from a 177 V bus upwards to a 38 kV output at 500W. The voltage multiplier design is a great way to keep a small form factor (506 g) for a 200x voltage gain. However it requires voluminous and heavy components that could not be used in a silicon wafer. For instance, the inductor was

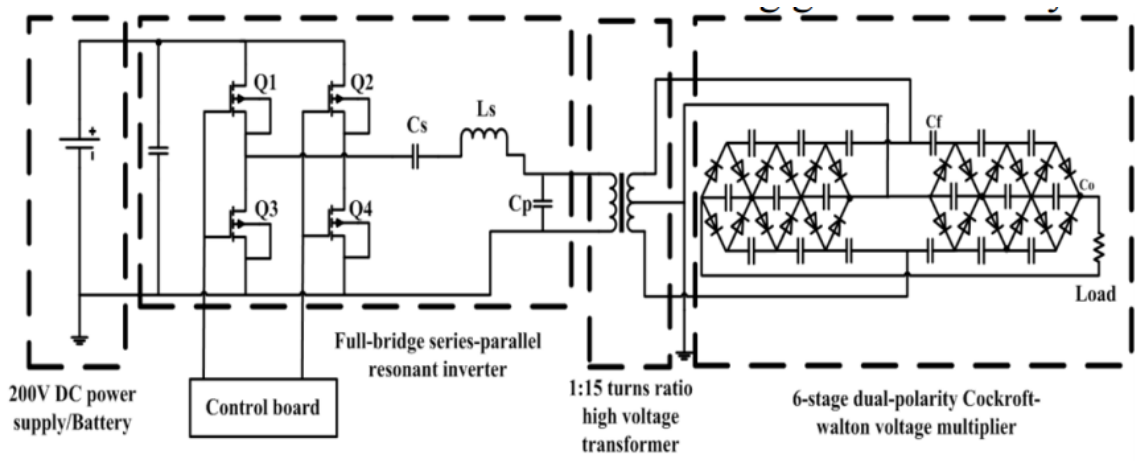


Figure 1-2: Topology of a 500 W DC - DC Converter

15.8% (80 g) of the total mass and the transformer was another 33.6 % (170 g) of the total mass[14]. This type of low mass and yet high voltage conversion opens the possibility of achieving similar scaling with much less mass. Since WaferSat is expected to use electric propulsion it is important to be familiar with the requirements needed to achieve such large voltage. Furthermore, it is important to note that a satellite such as WaferSat will not need a power converter of this voltage gain, so the transformer stage could potentially be removed and the capacitor multipliers decreased.

1.3 Research Objective

The design challenge to create a wafer-like satellite sets constraints that are not common to many satellites. The volume, mass, and power constraints restrict part selection and technological approaches that can be used in this effort. The nature of the satellites miniature size hampers the storage and harnessing of energy, increasing the need for a highly efficient and effective power system. Power electronics historically leverage the use of magnetics, in the form of inductors and transformers, to convert energy effectively but in this case the use of these components need to be minimized. The objective of this thesis is to explore the feasibility of a high efficiency-low-power system by evaluating different commercially available components and integrating them into a fully-functioning system using iterative testing, trade-off analysis, and

prototypes.

1.4 Thesis Roadmap

The thesis is organized into five chapters. Chapter 1 introduces the motivation for WaferSat and presents the power challenges. A summary of past efforts by different research centers is discussed.

In Chapter 2, the previous work completed prior to my arrival with the WaferSat team is explored. The design goals and challenges of WaferSat and the development philosophy is discussed. Lastly, a background on the electrical systems used in small satellites is covered.

In Chapter 3, the design methodology is explained, beginning with the requirements needed for each subsystem and their unique design criteria. A power budget is compiled from these insights and a trade-off analysis is explored to validate these decisions. The second half of the chapter dives into the power electronics design of the circuits used in the prototype board.

In Chapter 4, the designs of Chapter 3 are highlighted in the PCB prototype. The software, testing, and results of the PCB are discussed.

Chapter 5 contains the conclusions from the research and offers recommendations for the further development of wafer-scale spacecrafts. Insight towards the future research of the WaferSat effort is expanded by the work of this thesis.

Chapter 2

Background

2.1 WaferSat Team Background

2.1.1 WaferSat Project Overview

WaferSat started in early 2017 by MIT Lincoln Laboratory (MITLL), in collaboration with the MIT Space Systems Laboratory (SSL) and the MIT Space Propulsion Laboratory (SPL). WaferSat's goal is to develop a wafer-scale satellite bus that can accept a range of sensor payloads and be fabricated for <$5000 per unit at scale. The low cost is enabled by the combination of highly-parallelized, batch fabrication processes and low mass ($\tilde{5}$0g), therefore low launch costs. The WaferSat concept will enable swarms of satellites to operate in LEO, increasing the collective capability of these satellites. An artist's rendition of a WaferSat cluster is shown in Figure 2-1[1]. There are still many ideas as to what their payloads might be, and their survivability is still to be determined. The concept will enable swarms of satellites to operate in LEO, increasing the collected capability of these satellites. There are still many ideas as to what their payloads might be, but their survivability is still to be determined.

Figure 2-2 shows the WaferSat subsystems and the roles that the collaborators are playing. LL is leader to this effort and the SSL developed the power and thermal subsystems. Each group is responsible for developing prototypes for their respective

[1]Image provided by Casey Reed, MIT Lincoln Laboratory

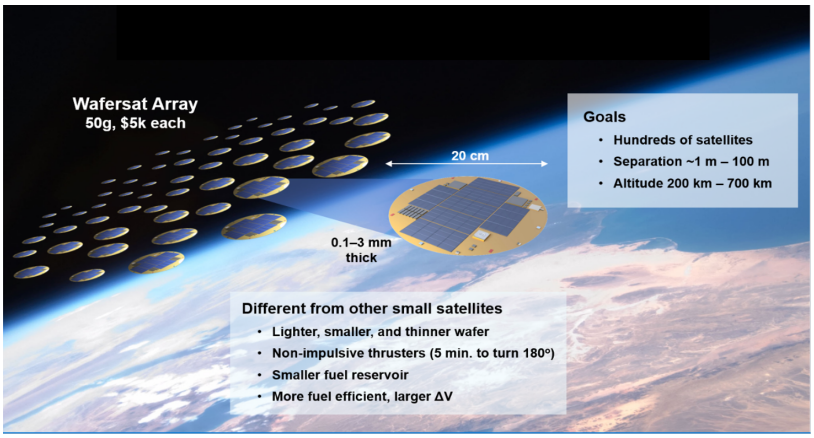


Figure 2-1: Artists Rendition of WaferSat

subsystem and collaborate with the other subsystems to generate a set of requirements and interface documents.

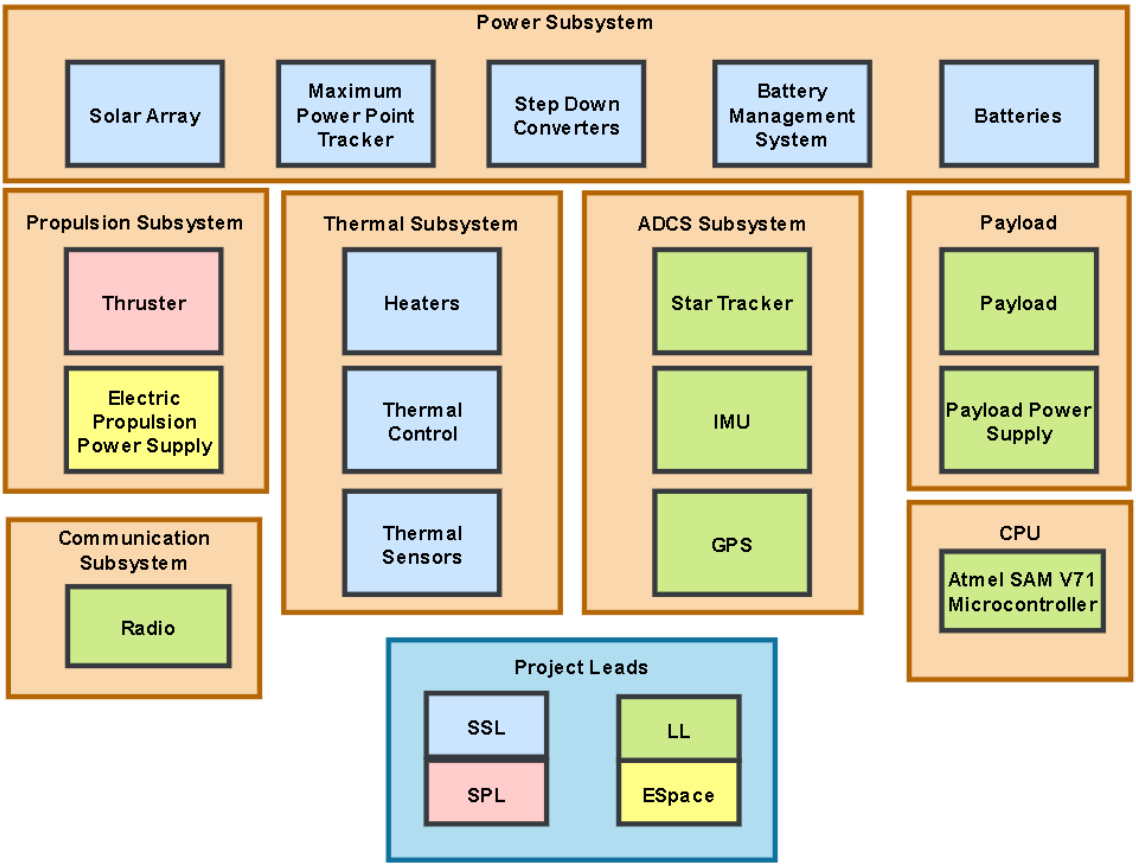


Figure 2-2: WaferSat Subsystems and Leads

2.1.2 WaferSat Design Goals

An exemplar WaferSat mission is planned to operate in a 400 km orbit with an estimated inclination of about 50°, resulting in an orbital period of 90 minutes. The spacecraft is expected to last approximately one year, undergo 5800 orbits, and endure temperatures between (-30 C - 70 C). The time of orbit of the spacecraft and the rapid changes in temperature give rise to a challenging environment. In order to ensure the orbital lifetime, the mass and thickness of the satellite need to be minimized to decrease drag in orbit. At this time, the wafer is expected to be created from 200mm diameter wafers, but the size may change depending on the capabilities of the target microfabrication facilities in which it is manufactured. While 200mm is the most common, high-volume microelectronics facilities accommodate 300mm wafers, while MEMS facilities typically work at the 100 or 150mm size. Lastly, it is estimated that the satellite needs more than 2W of power in order to operate continuously while maintaining a temperature that allows the electronics to survive. These design goals are summarized in Table 2.1.

Table 2.1: WaferSat Program Design Goals

Characteristic	**Desired Values**
Mass	<100g
Orbital Lifetime	6 Months - 12 Months
Temperature	-30C - +70 C
Thickness	< 6 mm
Diameter	20.32 cm
Microntroller	Radiation Hardened and Programmable
Power Generation	> 2 W
Part Selection	bare-die or compatible with silicon
Part Count	Minimized

Since the long term plan of WaferSat is to have all of the circuits to be embedded in silicon, it is key to select components that are available as bare die, in silicon compatible form factors. Furthermore, this design goal further limits the amount of components that can be chosen and minimizes the total mass consumed by electronics.

2.1.3 WaferSat Development Philosophy

Since WaferSat is a novel project with a new take on satellite development, there is a need to test out and mature the designs prior to integration and further development. The WaferSat effort is broken down into three stages: SWaP-Sat, PCBSat, and WaferSat. SWaP-Sat is the prototype and modular concept phase where candidate parts are tested and validated. PCBSat is the integration of the candidate parts validated in SWaP-Sat. The PCBSat deliverable is a PCB that contains the power and thermal subsystems and can be tested in a thermal chamber. Lastly, WaferSat takes the concepts and designs developed in PCBSat and transfer them into a silicon wafer. These three stages are pictured in Figure 2-3.

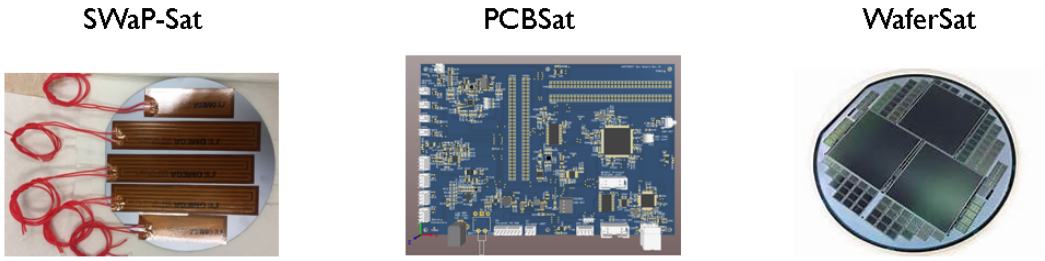


Figure 2-3: Stages of WaferSat

In design process, each contributor is concentrated to work on the subsystem level, allowing each subsystem to have its own independent developments and tests. The purpose of this stage is to find parts that could potentially work on the next stages of WaferSat and mature the designs prior to integration. The modularization is great for the student group, as each student or a small team of students can research and develop a small section of the project for future integration of the system, see Figure 2-4. Furthermore, this effort is a great way to isolate systems and learn how they work independently. The student team was set to focus on the development of the solar arrays, Maximum Power Point Tracker, Batteries, Battery Management System, Temperature control and Heaters. As seen in Figure 2-4, these components will interact with each other.

Despite being an isolated system, the team had to still keep in mind which com-

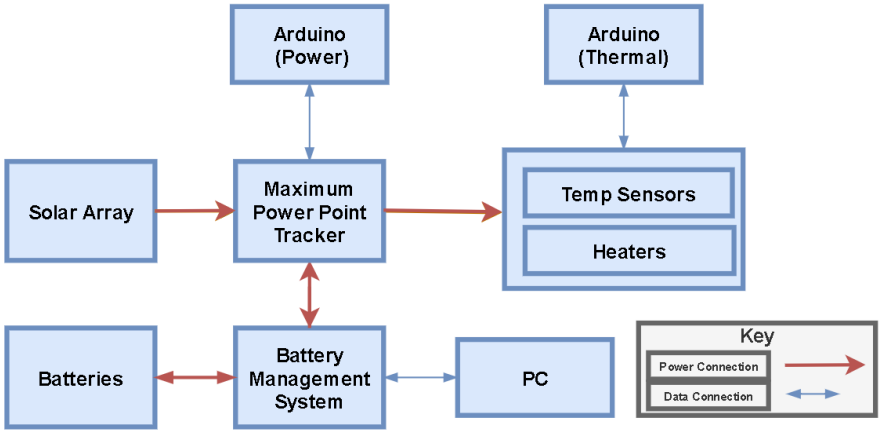


Figure 2-4: Block Diagram of SWaP-Sat

ponents were going to be used for SWaP-Sat .The student team prioritized selection of parts that are available in bare die format or can be easily depackaged. Either of these two characteristics allows the team to further integrate these components later on in the WaferSat effort, and minimizes the number of modifications to the electrical systems. The more components that PCBSat uses that are bare die, the easier it will be for WaferSat to implement these. Having to find new parts for the WaferSat effort might require rerouting or changing design constraints to accommodate newer parts. Once the evaluation boards for the individual components were able to work independently, the integration process began. The components in Figure 2-5 can be considered a "Flat Sat" - where the functions and interfaces are tested, but not required to fit in a certain volume or mass.

PCBSat is the development board that the student effort will use to develop and verify the power and thermal subsystems. PCBSat's purpose is to serve as the evaluation board for the tests that the student team uses to mature their design before moving forward to WaferSat. Furthermore, the PCB allows the team to further enhance their software development. The development of the project from SWaP-Sat to PCBSat is described more in detail in Chapter 3 and Chapter 4.

Lastly, once the design of PCBSat has been matured and qualified, the design will be moved on to a silicon-based wafer design. One differentiating factor of the WaferSat stage is that the main goal is to have a functioning satellite at the end

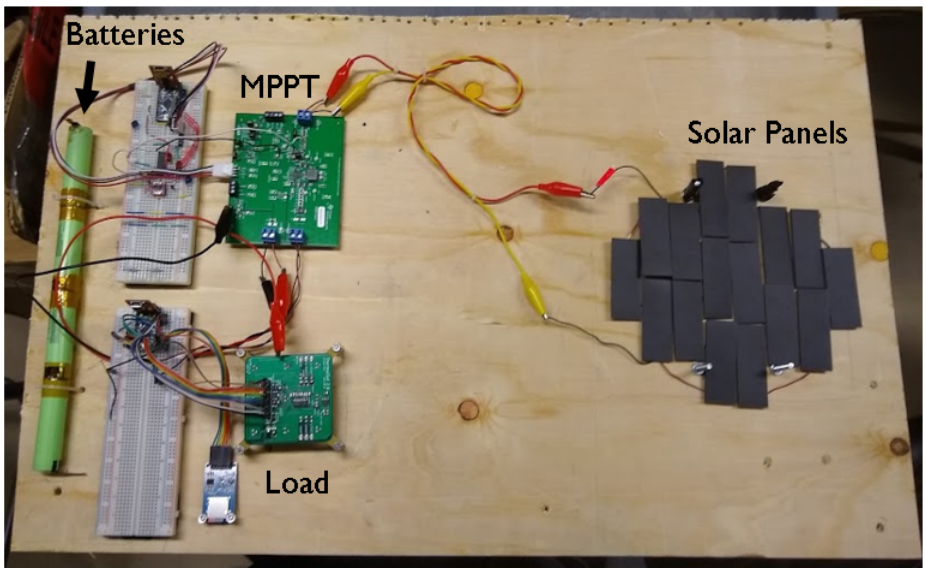


Figure 2-5: SWaP-Sat Power Subsystem Evaluation Boards

of this cycle, whereas in the previous two stages the goal was to prove a concept. WaferSat will encounter many challenges but hopefully the knowledge gained from SWaP-Sat and PCBSat will greatly reduce the quantity of issues.

2.2 Electrical Systems in Small Satellites

Even though satellites come in all shapes, forms and sizes, they all share one common element, the electrical power system. This system performs three main functions: generation, storage, and distribution. A simple model of these functions are pictured in Figure 2-6. The red arrows represent the direction of energy, where it is unidirectional except for the batteries and their management system. Solar panels are some of the most common generation sources for most satellites. Solar panels are the main generator for CubeSats. In terms of storage, there have been many different battery chemistries that have been explored, but the Li-Ion cells are the top candidate for CubeSat and small satellite missions due to their high energy to weight ratio. Lastly, distribution is the most varied of these subsystems, as some satellites have central distribution networks while others have distributed systems. Regulation, monitoring, and wiring are commonly included in the distribution section of power systems.

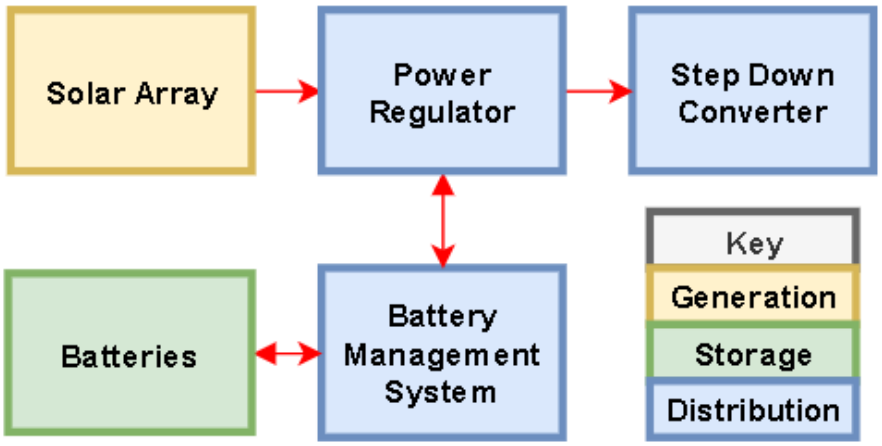


Figure 2-6: Basic Model of the Power System of a Small Spacecraft

2.2.1 Power Storage: Batteries

Batteries are vital in spacecraft since they not only power the spacecraft through its most intense power demands, but also allow the spacecraft to function while in eclipse. There are many options for the primary storage units of energy in spacecrafts, as shown in Figure2-7. Battery types and functions are differentiated by their effective burst power and their longevity.

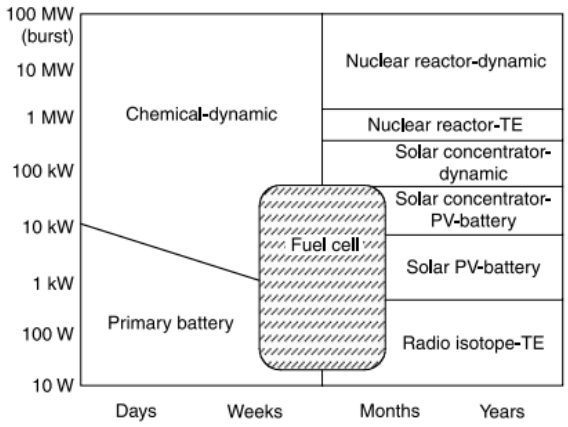


Figure 2-7: Energy Sources for Various Power Levels
[2]

Despite the numerous options for large satellites, CubeSats usually have two types of batteries choices: primary and secondary. Primary batteries are non-rechargeable and are used for specific long term instruments or high demand-quick burst applica-

tions. Primary batteries can last from hours to weeks and are mostly used during launch or the initial steps of program. Secondary batteries are rechargeable and are meant for long-term operation of the spacecraft. The most popular chemistry for secondary batteries is Li-Ion, since they have great energy densities in comparison to other technologies as observed in Figure 2-8. In the past, many spacecraft used

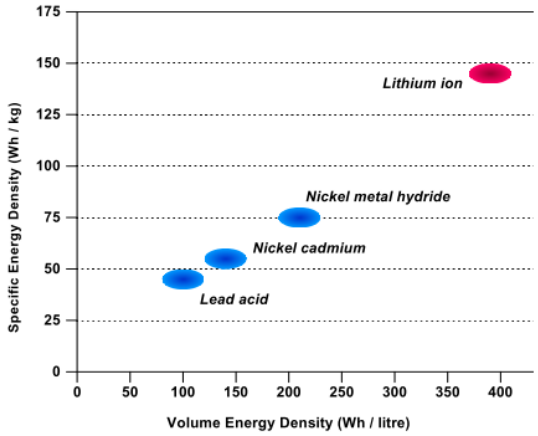


Figure 2-8: Volume Densities for Different Battery Chemistries[2]

the Lead Acid batteries but with advancements in technology, spacecrafts have been able to use batteries that have better capacity and volume. Older battery types have undesirable features such as self-discharge, short shelf-life, or storage orientation constraints. These features made the use of Li-Ion much more attractive, since these have longer shelf-life, lower rate of self-discharge, and utilize lighter and less volume in the spacecraft. One major drawback of the Li-Ion cells is their need for constant individual cell monitoring. It is critical to observe voltages, current, charging cycles, and temperature Li-Ion cells. Unlike other battery types, Li-Ion batteries can quickly go into thermal runaway, destroying the cells and potentially damaging the spacecraft by releasing lithium gas and flames when overcharged[2]. Thermal runaway is the disastrous self-accelerated degradation of the cells[15].

2.2.2 Power Generation: Solar Cells

The most common source of power for satellites, especially those orbiting Earth is the solar array, also called Photovoltaics Arrays (PV) . These arrays convert energy from the sun's rays into electrical energy. Their efficiencies range from $15 - 25\%$ and keep improving every decade. The arrays are commonly constructed with Crystalline silicon or gallium arsenide for higher efficiencies during solar conversion[16]. Solar Arrays have a unique current-voltage characteristic curve (IV Curve) and can be modeled as a constant current source as shown in Figure 2-9[3]. The model shows how solar cells behave similarly to a current source that is in parallel to a diode and a resistor. The current source provides the current that flows out of the cell, while the diode sets a voltage across the resistor R_p and current source I_{ph}. The diode's voltage is mostly adjustable until it reaches a breakdown voltage that shorts it. The IV plot is shown in Figure 2-10.

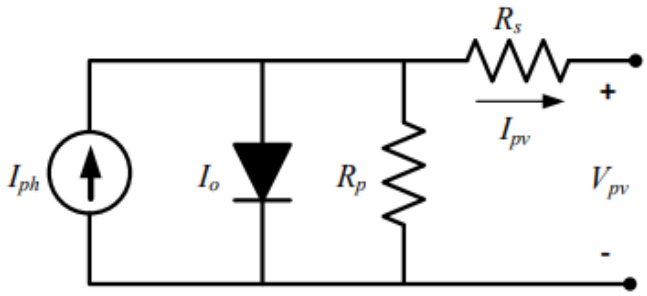


Figure 2-9: Circuit Equivalent of a Solar Cell[3]

Solar cells have a maximum power point, which varies depending on the temperature and light irradiance they are exposed to. As the solar panels get warmer, their IV curve shift upwards in current and decreases in voltage. This phenomenon can be observed in Figure 2-10. Beginning with the nominal red curve, an increase of temperature moves the graph to the grey curve. The increase in temperature increases the maximum current supplied and minimizes the voltage supplied by the array. The maximum power point current (I_{MPP}) shifts upwards as the maximum power point voltage (V_{MPP}) decreases. This shifting can be observed in Figure 2-10 from Surrey[4]. In order to maximize the power obtained from these solar panels, there needs to be a

power system that can find the MPP for each array as operating conditions change. These circuits will be looked into further in a later section.

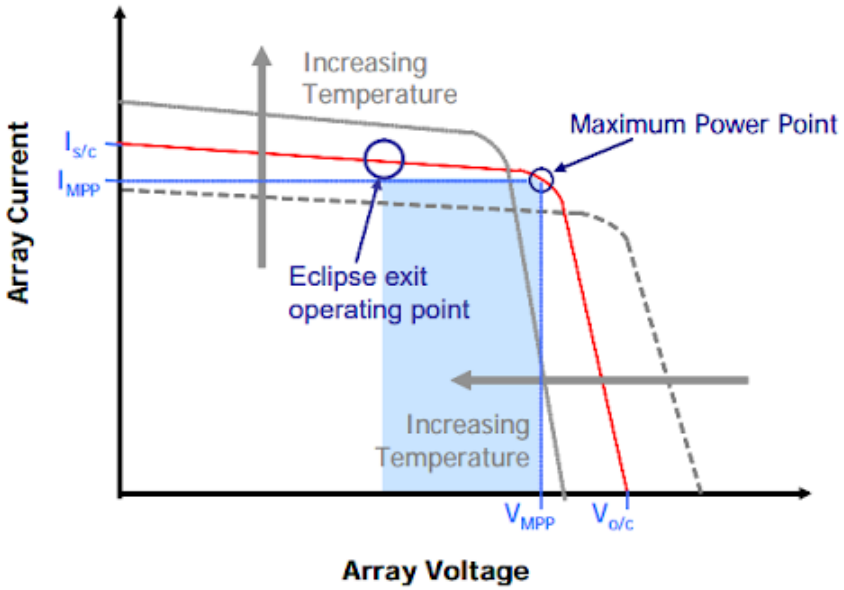


Figure 2-10: Effect of Increasing Temperature to Maximum Power Point in Solar Arrays[4]

2.2.3 Power System Background

While the solar panels and batteries generate and store power, respectively, the power processing system regulates and distributes this power to the spacecraft. Small satellite's power regulation and distribution systems take one of three forms in most cases:

- Direct Energy Transfer (DET)
- Direct Energy Transfer with Regulated Bus (DETRB)
- Maximum Power Point Tracker with Battery Bus (MPPTBS)

The first topology is the Direct Energy Transfer (DET), where the power output of the solar panels is connected directly to the battery and the spacecraft power bus. The battery bus is the node connected to the batteries meanwhile the spacecraft power bus is the node that is connected to the rest of the spacecraft. The DET

with Regulated Bus (DETRB) is similar to DET but it has an extra power regulator between the battery and the regulated bus. The extra regulator controls the voltage that charges the battery. This variable voltage can better control the charge curve of the battery and decouples the solar panels from the battery since they are no longer connected directly. Lastly, the Maximum Power Point Tracker with Battery Bus (MPPTBS) adds regulators directly on the solar panel outputs and controls the power drawn from every string of cells. The MPPTBS also removes the regulator between the battery and the bus, meaning that the bus is now the battery bus. The introduction of the MPPT optimizes the power drawn from each string and tunes it to the voltage that is needed to charge the battery.

Researchers at Clyde Space Ltd. conducted a trade study to understand the benefits and use cases of each of these systems and evaluated their performance by comparing part count, mass, volume, efficiency, and power margin [4]. The first system to be analyzed was the DET, which is the simplest and tends to have the lowest mass among the other systems, pictured in Figure 2-11. The figure has a model depicting a solar cell array of three cells being connected directly to a battery bank on the lower right. The battery bus is then connected to the Power Distribution Module (PDM), which then distributes power to the rest of the spacecraft .

This potential change in V_{MPP} and I_{MPP} greatly reduces the efficiency of the system because a decrease in temperature raises the V_{MPP} and destabilizes the bus with the maximum voltage. The optimal point of this system is only achieved when the batteries are fully charged and the solar panel is warm enough from its solar exposure to provide the V_{MPP} that matches the battery voltage. Nevertheless, this state is suboptimal as it leads to a surplus of power and rarely used in formal operations since this operating point occurs once per orbit.

The next option for the power system is a Direct Energy Transfer with a Regulated Bus (DETRB). This system is similar to a DET but can regulate the voltage obtained from the batteries, see Figure 2-12. Despite the addition of a battery voltage regulator, there are still some drawbacks when operating in LEO. The changes in temperature and solar irradiance cause the solar cells' IV curve to move. This movement renders

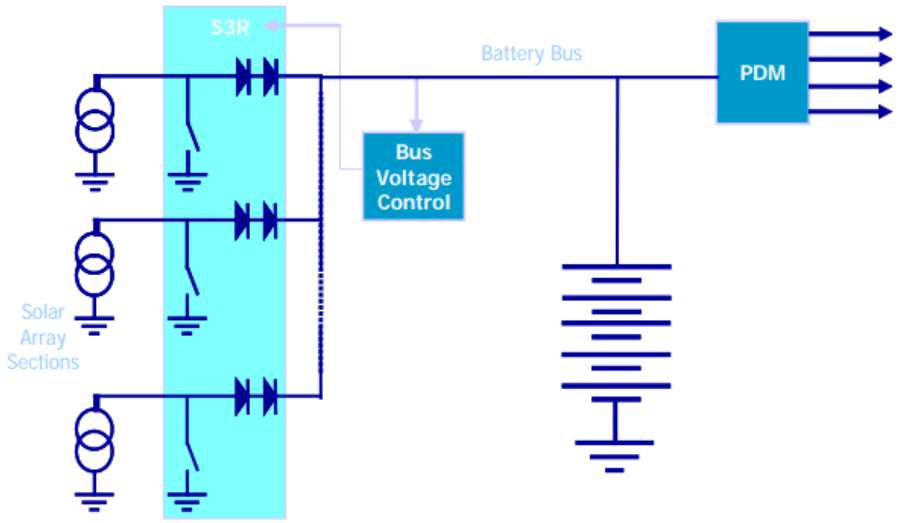


Figure 2-11: DET with Battery Bus[4]

the solar panels incompatible with the bus voltage which cannot vary as much as the solar cells can. The electric bus is limited by the charging ranges of the batteries, whereas the solar cells' voltage depends on the solar input and temperature. The DETRB is commonly used in satellites that occupy the Geostationary Orbit (GEO), which have a much longer orbital period of 24 hours.

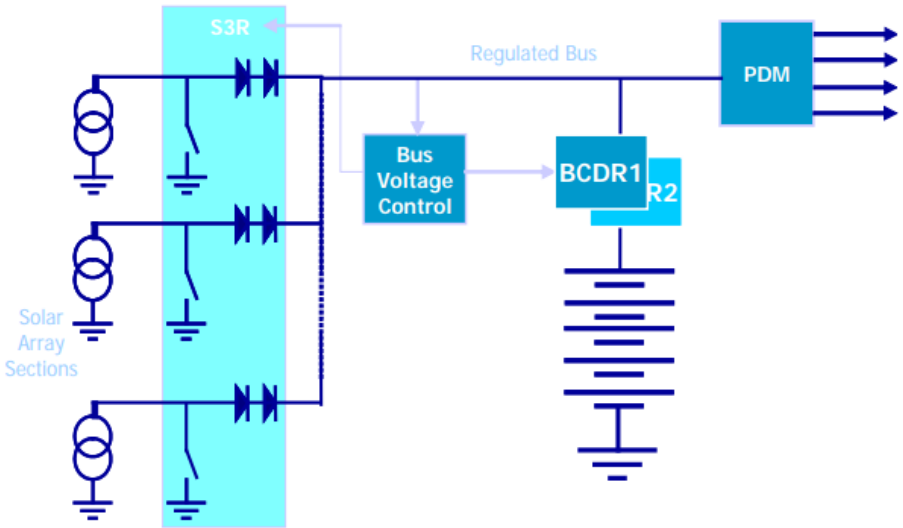


Figure 2-12: DET with Regulated Bus[4]

Given the issues in the last two electrical systems, Clyde Space explored the option of using a Maximum Power Point Tracker (MPPT). The varying maximum power point in most solar cells introduces the need to include a MPPT to fully optimize the system in a LEO orbit. The MPPT is placed between the solar panel and the bus of the spacecraft. The MPPT is composed of a DC/DC converter that converts the power of the solar panels into a voltage and respective current that operate with the regulated bus. As observed in Figure 2-13, multiple MPPTs can exist in a single array. The MPPT's use different kinds of algorithms to track where the maximum power point is in each cell, thus tuning the voltage and current generated from each cell. MPPTs give systems lots of versatility so spacecraft can operate at a much higher efficiency during most of the sunlit section of the orbit. The MPPT's major advantage is its ability to tune the power generated from every solar cell based on their unique parameters. One downside of this operation is that this extra circuitry is only active during half of the orbit. While in eclipse, the MPPT circuitry is not in operation since there is no maximum power point to be found in the solar cells. The MPPT can not only be used to find the maximum power point, but also be programmed to adjust to the power intake to the demands of the system. For instance, if the batteries are fully charged and the system is only consuming 1.5 W at a 15 V intake, while the solar panels are generating 2 W of power at 20 V, the operating point of the MPPT can be "backed off" so that the solar panels are only providing the 1.5 W required by the system. The flexibility of the system is a key advantage because it can reduce the need for extra shunts, which are used in discharging excess power[4]. Some of the drawbacks of this system include the need for extra components for the DC/DC converter, and the introduction of bulky and heavy magnetic components. The efficiency of the MPPT can be as high as 95%, which may be suitable for a long term programs. Another drawback of this process is the need for feedback control, which adds sensors and a computing element to the power system. These presence of feedback control requires the constant need of monitoring which might not be possible on certain spacecraft.

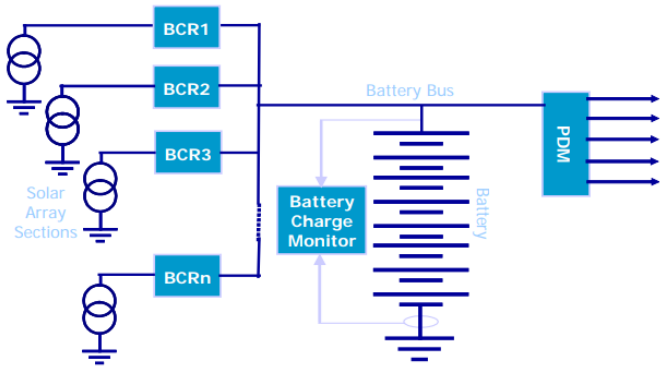


Figure 2-13: DET with MPPT in Battery Bus[4]

2.2.4 Power Distribution

Distribution in small satellites is not as complex as in larger spacecraft. In large spacecraft (>100 kg) there are distribution voltages that are higher than the operating voltages of the subsystems[2]. The distribution is set at a high value to limit the current flowing through the spacecraft, thus reducing losses in the copper and magnetic interference. In contrast to large satellites, there is no need to have regulators spread out across the spacecraft since there are no large distances (>1 m) to flow power from. Distribution in FlatSats and CubeSats is conducted with copper traces in PCBs or in some cases with external harnessing between PCBs.

Chapter 3

PCBSat Power System Design

This chapter contains the design methodology for the development of the power system of PCBSat. In order to design these system, a better understanding of the spacecraft had to be defined. This understanding is expanded in the Preliminary Design and Requirement section, where the subsystems are defined, the states of operations are defined, and a power budget is compiled. The components and interfaces are introduced. Furthermore the electrical designs are expanded and looked into with detail in the design section.

3.1 Preliminary Design and Requirement Definition

PCBSat is a development testbed for WaferSat. PCBSat will contain 1) the processor needed for all of the power and thermal algorithms, 2) sensors needed for attitude determination (Star Tracker), 3) heaters to maintain temperature while in eclipse, and 4) the power circuitry to recharge the batteries based on solar input. PCBSat contains power and data interfaces only for thrusters, GPS, and payload. Those components are being developed and tested separately. The design will not contain the following components but will have power and data connections to: Thrusters, GPS, or, Payload. The distinction between PCBSat's components and their connections can be observed in Figure 3-1.

The two main systems within PCBSat are the power and thermal subsystems.

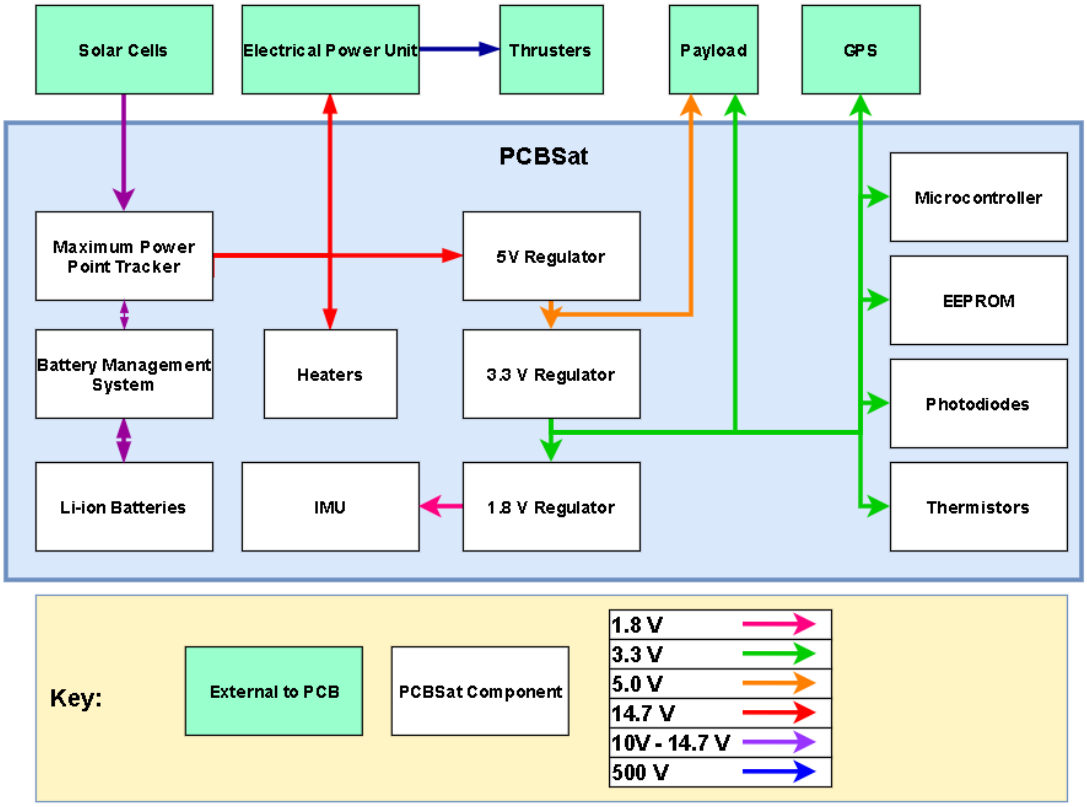


Figure 3-1: PCBSat Power Diagram

PCBSat's goal is to integrate these systems and provide power and thermal control to one PCB, where the interdependencies of heating and power are tested. These systems can all be observed in the power diagram in Figure 3-1. Power is first generated in the solar cells and is distributed and controlled by the Maximum Power Point Tracker. The MPPT is a type of DC-DC converter that converts the DC input from the solar panels into a pulsed AC voltage. This AC signal is then converted back to a DC voltage that is matched to that of the battery. The conversion is adjusted based on both the illumination level and the desired battery voltage. The MPPT distributes power to the spacecraft from the solar panels and to or from the batteries. The batteries are regulated and protected by a battery management system (BMS). Three components connect to the spacecraft powerline: Electrical Propulsion Power Supply (EPPS), Heaters, and a 5 V regulator. The EPPS powers the electric propulsion ion thrusters. The 5 V voltage stepped down to 3.3V and 1.8V by two cascaded step-

down regulators. Even though the thruster, Attitude Control (ADCS), and payload subsystems are being developed by other teams in the PCBSat effort, their capability, software, component selection, and power consumption still need to be considered into the design of the power and thermal system.

3.1.1 Operational Modes

Clear definition of spacecraft modes are needed to define a power system that can meet the program requirements. The state of operation and subsystem table describes these inter-dependencies in Table 3.1. Science mode is when the science payload is powered on and the ADCS and thermal system are adjusted accordingly. Survival mode keeps the payload and comms modes off since it is consuming the least amount of power as possible. Eclipse mode is defined as transition to the dark side of earth, so thermal control should be kept on to keep the satellite warm. No science or communications occur during the eclipse. Lastly, Sun Charge is the state where the satellite is facing the sun but it is not using its payload. This state is used for battery charging and sending data back to earth. The states of operation are explained in Table 3.2. Furthermore, the seperation of states of operation allows the designers to understand how they should develop their algorithms and state machines, so that they do not interfere with each other.

Table 3.1: WaferSat States of Operation and Subsystem Breakdown

	Subsystem				
State	**Power**	**Thermal**	**ADCS**	**Payload**	**Comms**
Science	A1	D1	D1	A1	A0
Survival	A1	D1	D1	A0	A0
Eclipse	A1	A1	D1	A0	A0
Sun Charge	A1	D1	D1	A0	D1

A1 = Always On
D1 = Dependant On
A0 = Always Off

Table 3.2: States of Operation Described

State of Operation	Description
Science	Payload is on and data is recorded to memory
Survival	Only essential subsystems are on, thermal control is prioritized
Eclipse	Heaters will be needed in the shadow of earth, no attitude control used
Sun Charge	While facing the sun, charge batteries, can beam data down, payload is off

3.1.2 Components

Maximum Power Point Tracker

The power generation of this system is completed by solar cells that cover one side of the wafer in the WaferSat design. Variance in the incident solar irradiance - due to orbital conditions, seasonal variation - requires the system to have a maximum power point tracker, to optimize the power drawn from the solar panels. The MPPT needs to be efficient (> 90 %), since its efficiency drives the total electrical efficiency of the system. The MPPT tolerates varying solar irradiance conditions in space due to its algorithm.

Maximum Power Point Trackers are usually Buck, Boost, or Buck-Boost converters that step down, step up, or step up and down voltage for the output desired. MPPTs are designed based on the expected size of the solar panel. In most cases, the larger the solar panels, the higher the voltage generated (directly correlated to cells connected in series), but the voltage needs to be stepped down to the desired bus voltage. In some cases, the desired bus voltage might be higher or lower than the input voltage, which might mean that the system will need a converter that will step up or step down voltage. The simplest of converter that accomplishes this is the non-inverting buck-boost converter, shown in Figure 3-2. The Buck-Boost converter allows the flexibility of the stepping up and down voltage as well as limiting the amount of inductors that are needed. For example, if you were to have both a Buck and a Boost converter, the power system would need two inductors, one for each converter. In contrast, the Buck-Boost converter can be designed to have both

of the Buck and Boost functions while using only one inductor. Halving the potential need of a massive ferrous loop -needed for inductors- is advantageous.

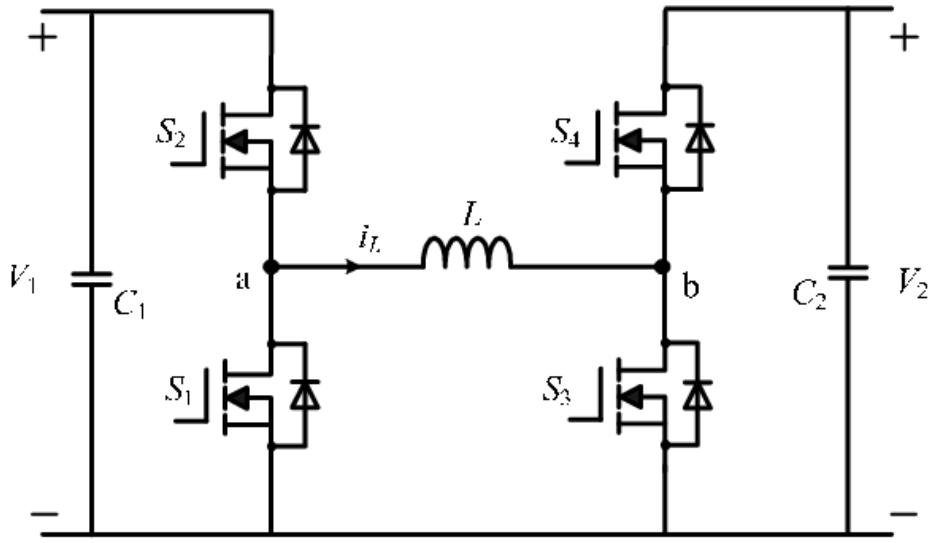


Figure 3-2: Non-inverting Buck-Boost Converter

Due to the small size of WaferSat, there is no need to have multiple MPPTs or have MPPTs with complex algorithms[3]. One of the main concerns of the spacecraft is that there is a desire to use the least number of parts as possible as well as minimizing mass. It is also important to select parts that can easily be integrated into a silicon wafer. The compatibility of these parts have influenced the students research in COTS parts . Prior to selecting an IC, the main responsibilities of the MPPT are outlined: as seen on Table 3.3.

The MPPT has to connect with the solar cells and tolerate the ranges of voltages that these solar cells might provide. For a solar array the size of WaferSat is expected that the solar array provides a minimum of 3V and a maximum of 25V. Secondly, in order to minimize the component count, the MPPT should provide a way to charge the batteries directly, without the need of another IC and sub circuits. The output voltage of the MPPT should be within the range of the batteries, which is expected to be within 9 - 20V. On this note, the MPPT needs to be accessible by the microcontroller, specially to be able to read the telemetry values of interest for maintenance.

Since the electronics in PCBSat are mostly miniaturised, the amount of magnetic

components will be reduced as much as possible. The MPPT should use a topology that minimizes these and if it does include them, the ripple current through the inductors should be less than 100 mA [5]. To help reduce the size of magnetic components, the switching frequency of the MPPT should be above 800 kHz, as inductor size is inversely proportional to inductor size, see Table 3.3.

Table 3.3: MPPT Design Drivers

Characteristics	**Details**
Interface with Solar Cells	Allow a higher voltage input than the bus, which results in lower currents for desired power. Optimal to reduced conduction losses
Charge Batteries	Provide a charging sequence that will be effective for the Li-Ion batteries
Contain telemetry measurements	Necessary for maximum power point tracking and protection management.
Programmable	Allow the user to create a custom MPPT algorithm based on the requirements of the spacecraft
Magnetic Components	As minimized as possible
Input and Output Voltage Requirements	V_{in}: 3 - 25V V_{out}: 9 -20V
Switching Frequency	$>$ 800 KHz
Inductor Current Ripple	$<$ 100mA

Regulators

In order to power the electrical components of the spacecraft, a 5V step down converter, a 3.3V switching converter, as well as a separate 1.8V regulator have been added to support the microcontroller and other ICs in the PCBSat. These converters are connected in series to decrease the step down losses from a high bus voltage. Similarly to the MPPT, their is a preference towards ICs that have small inductors and low part count.

Battery Management System

The Battery Management system needs to monitor the state of the batteries and control the charging between individual cells. Furthermore, it needs to be low in

power consumption and part count. Lastly, it must be compatible with different battery chemistries. If possible, a bare die part is preferred.

Microcontroller

The microcontroller is the brain of PCBSat and its limitations constrain the design of the PCB and its future iterations. For that reason, the microcontroller should have multiple input/output ports (>30), I^2C communication, internal memory, fast operating frequency ($>$ 100 MHz), and offer PWM functionalities. The microcontroller needs to be able to be embedded onto a silicon wafer. Lastly, electrical failure is common in space due to radiation, the microcontroller needs to be available in a radiation hardened package. Electronics, specially computing elements, are known to fail in space due to radiation effects such as Single Event Upsets (SEU) or Total Ionizing Dose (TID). Table 3.4 summarizes the design drivers.

Table 3.4: Microcontroller Design Drivers

Characteristics	**Details**
Input/Output Ports	>30
Communication Protocol	Include I^2C
Internal Memory	$>$ 2000 kbytes
Operating Frequency	$>$ 100 MHz
PWM Functionality	Required for Heater system
Input Voltage	3.3V or 5V
Package	Compatible with bare silicon
Radiation Hardening Ripple	Must have

3.1.3 Interfaces

Thermal Subsystem

Since PCBSat will be going through temperature extremes ($-40C - 85C$) , there needs to be a way to keep a safe temperature range for the system, without adding much cross-sectional surface area or volume. For this version of PCBSat, the heaters were designed to be kept external, and the temperature sensors were populated across

the board in multiple locations. The microcontroller has access to these sensors based on the I^2C Communication protocol and monitors their temperature data.

The heater power estimate is dependant on the thermal properties of the wafer. The thermal properties are characterized by both the emissitvity and the absorptivity of the solar cells and the silicon, as these factors will drive the rate at which the satellite can absorb and dissipate heat. These models have been developed by Michael Fifield, PhD Candidate in the SSL, and Ceylan Ceylan, undergraduate student in the SSL[17]. The current model assumes the use of passive heaters that consume 1W to 2W of power. The power drawn by the thermal system will be drawn from the system voltage, planned to be 14.7V - 18V.

The power system and microcontroller must be able to control the actuation of these heaters and be able to read the temperature of different sections of the PCB. For these reason, it is expected to use four heaters, one for each quadrant of the PCB. Consequently, eight temperature sensors are used to monitor the temperature on both sides of each quadrant. The design drivers are summarized in Table 3.5

Table 3.5: Thermal Power Design Drivers

Characteristics	**Details**
Voltage Provided	14.7V - 18V
Power Provided	$>$ 1.5 W
Communication	Access to I^2C data and clock lines
Switches	Controlled by microcontroller
Heaters Count	4
Temperature Sensor Placement	On each midline of PCB, Both Sides
Temperature Sensor	Accessible via I^2C data line

Propulsion

In order to fully quantify the power consumption of WaferSat, the propulsion power requirements need to be considered. The EPS has two sets of requirements: the power consumed by the thrusters and the inputs to the EPPS. The propulsion system is being developed by the SPL. Based on models from Noah Siegel and Daniel

Freeman[1], an estimate on the power consumed by this system is as follows: Assuming about 1000 emitters per array, 100 nA per emitter, at 1 kV, results in 100 mW per thruster[18]. WaferSat will have six thrusters, but will only have three firing at once max, with a conservative efficiency of 50% the total power consumption results in 600 mW. The attitude control algorithm developed by Noah Siegel estimates a 33% duty cycle, resulting in a time-average power consumption of 200mW for all six thrusters. Furthermore, there is a need for a high voltage to power the EPS. It is estimated that the EPS needs a voltage between $500V - 1000V$, at a very low current draw of .3mA - .6mA. With these values, it is estimated that the EPPS consumes 300 mW. The net total for the propulsion system is about 500 mW[2]. The EPPS is expected to boost its desired voltage of 500 - 1000 V from a voltage of 14V-18V that should be provided by the power subsystem. Lastly, the propulsion system will communicate with the microcontroller through an I^2C data line. These design goals are compiled in Table 3.6.

Table 3.6: Propulsion Power Design Drivers

Characteristics	**Details**
Voltage Provided	14V - 18V
Power Provided	500mW
Communication	Access to I^2C data and clock lines

Payload

The payload for PCBSat has not been defined as of this thesis but placeholder design goals have been created to accommodate future potential payloads, see Table 3.7. It was determined that the power subsystem has to be able to provide two voltage lines to the payload: 5V and 3.3V. These voltage values are standard for powering most electronic components. The power provided for the Payload is limited to 75mW for the time being. Furthermore, the payload will communicate with the on-board microcontroller and will be needed a I^2C communication bus.

[1]Daniel Freeman is the Systems Engineer for WaferSat

[2]Based on documentation provided by Daniel Freeman (LL) and Edmund Chin (LL)

Table 3.7: Payload Power Design Drivers

Characteristics	Details
Voltage Provided	5V and 3.3V
Power Provided	75mW
Communication	Access to I^2C data and clock lines

3.1.4 Power Budget

After all of the subsystems have been defined, the power demands can be compiled. The power budget is calculated assuming max power intake for every component in PCBSat, outlined in Table 3.8. In order to make a robust electrical system, it is assumed that all of the components will be on at once. This is known as the worst case scenario that the power system has to endure. Every subsystem is broken down by their main components and their respective voltage and maximum current draws. For instance, PowerSat includes the MPPT, power regulators, BMS, OpAmps, memory, and some supporting circuitry that is expected. Then for each component, the maximum current draws were extracted from their respective datasheets. The rest of the subsystem power estimates are sourced from the previous subsections of these section.

Based on the power budget in Table 3.8, PCBSat consumes a maximum of 2.7 W, where about 2 W are being consumed to keep the satellite at a safe operating temperature. It is good practice to assume that all of the components will be consuming more power than expected (+10%). It is common to add contingency in the power budget of about 10%[19], but the percentage might decrease as the system becomes better defined. The thermal value might decrease after a more in-depth look into the thermal system. The remaining 70 mW is consumed by the rest of the spacecraft. The solar panels are estimated to generate $>$ 2W in sunlight based on previous lab tests.

3.1.5 Trades

The presence of electric propulsion raises many challenges to the power subsystem, the largest of which is a requirement for over 1kV in order to ionize the liquid that fuels the

Table 3.8: PCBSat Power Budget

Subsystem	*Component*	$V_{in}(V)$	$I_{in}(mA)$	$P(mW)$
Power Sat				
	MPPT	3.30	1.00	3.30
	Microcontroller	3.30	10.00	33.00
	LDO	14.70	0.01	0.09
	BMS	14.70	0.33	4.85
	3.3V Regulator	14.70	0.09	1.25
	OpAmp Therm	3.30	0.55	1.82
	OpAmp Photo	3.30	8.00	26.40
	EEPROM	3.30	0.40	1.32
	Multiplexer (x2)	3.30	0.50	1.65
			Total (mW)	**73.67**
Payload		$V_{in}(V)$	$I_{in}(mA)$	$P(mW)$
	Instrument	3.30	22.70	74.91
			Total (mW)	**74.91**
Comms and ADCS		$V_{in}(V)$	$I_{in}(mA)$	$P(mW)$
	IMU	3.30	4.00	13.20
			Total (mW)	**13.20**
Thermal		$V_{in}(V)$	$I_{in}(mA)$	$P(mW)$
	Thermistors (8x)	3.30	0.01	0.26
	Heater	14.70	136.00	1999.20
			Total (mW)	**1999.46**
Thrusters		$V_{in}(V)$	$I_{in}(mA)$	$P(mW)$
	Thruster	14.70	13.60	199.92
	Thruster Power Supply	14.70	20.00	294.00
			Total (mW)	**493.92**
			Total Power (W)	**2.66**

electric thrusters. This large voltage has to be boosted from the solar panel voltage in an efficient and sizable manner. Most electric propulsion systems use inductors or staged DC/DC converters to elevate the output voltage to these high values, but these choices lead to high mass and large cross sectional areas due to the magnetic components. The increases in area increase drag the spacecraft encounters, forcing it to deorbit faster. In order to reduce the need of large magnetics, a relatively high bus voltage (>3x the logic level voltage) should be selected, as well as a low SWaP DC/DC converter for the electric propulsion system. Then again, the bus voltage cannot be too high since that will require more batteries and solar panels in series to

achieve such high voltage. For instance, the spacecraft is expected to use Li-ion cells that have a nominal voltage of 3.7 V, which sets a strict step function based on the cell count. The resulting voltages are 3.7 , 7.4, 11.1, 14.8, and 18.5.

Prior to selecting a bus voltage, the most efficient bus voltage needs to be determined. Based on previously mentioned design choices, there are constraints on the power intake, and based on the power budget a load can be determined, as seen in Table 3.9.

Table 3.9: MPPT Converter Constraints

Constraint	**Value**	**Explanation**
V_{in}	13.6 V - 21.6 V	Based on the data sheet of IXYS Solar Cells
P_{out}	2.655 W	Based on Power Budget
R_{load}	82Ω	Based on Power Budget and Bus Voltage

Given the boundaries of V_{in}, the MPPT will step down the voltage during the majority of its operation. For that reason, the design will be validated using the model of a Buck converter for continuous voltage step down. The Buck converter is a valid model since the non-inverting buck-boost converter is equivalent to a buck converter when operating in buck mode. The simplest model of a Buck converter is composed of an inductor (L), Capacitors, (C_{in} and C_{out}), a switch (SW), and a diode (D). This model is observed in Figure 3-3.

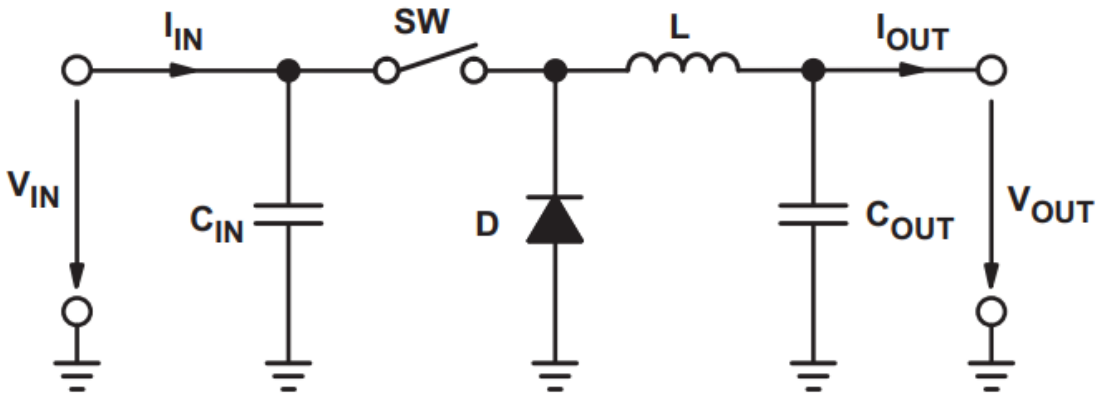


Figure 3-3: Buck Converter Model[5]

The input voltage and output voltage follow the relation in Equation 3.1 in an ideal situation, where D is the duty cycle of the switch. The duty cycle can vary from

0 - 1 and can only step down the voltage, meaning that $V_{out} < V_{in}$ always.

$$V_{out} = V_{in} \times D \tag{3.1}$$

One of the main design criteria to be considered in power converters, is the inductor ripple current, ΔI_l. This value is important since this is the amount of current that will be oscillating in the inductor of the buck converter, and will be sent to the output load. It is the goal of the designer to minimize the ripple to about 10% - 20% of the DC average current I_L for an efficient design[3]. For this preliminary design, a switching frequency of 200 kHz is used for f_s. The inductor ripple current can be calculated with the following expression:

$$\Delta I_l = \frac{(V_{in(max)} - V_{out}) \times D}{f_s \times L} \tag{3.2}$$

By combining Equations 3.1 and Equation 3.2, the minimum inductor size can be calculated with Equation 3.3:

$$L_{min} \geq \frac{V_{out} \times (V_{in} - V_{out})}{\Delta I_l \times f_s \times V_{in}} \tag{3.3}$$

Based on the power budget, the expected power draw is $2.7W$ with a current draw of $180mA$. With an expected current ripple of 10% of the max current draw, there is a desired limit of $36mA$. With these constraints Table 3.10 was compiled that compares the ΔI_l based on the input voltage ranges and selected voltage constraints. The adjusted variable is V_{bus} and the value optimized is ΔI_l.

In Table 3.10, the bus voltages are compared to the four potential bus voltages : $3.7, 7.4, 11.1, 14.8, 18.5$. For these calculations, the V_{in} is set at the minimum and maximum voltages expected for the solar array ($14V - 21.6V$). With these constraints, Equation 3.1 was used to determine the Duty Cycle and Equation 3.2 was used to

[3]Ripple percentages are based on design practices from Texas Instruments

Table 3.10: Bus Voltage Trade-Off Analysis

V_{in}	V_{bus}	$L(uH)$	$C(uF)$	$Duty$	$Mode$	ΔI_l
14.0	*3.7*	*425.86*	*0.11*	*0.26*	Buck	32.0
21.6	3.7	425.86	0.11	0.17	Buck	36.0
14.0	7.4	675.67	0.11	0.53	Buck	25.8
21.6	7.4	675.67	0.11	0.34	Buck	36.0
14.0	11.1	749.42	0.11	0.79	Buck	15.3
21.6	11.1	749.42	0.11	0.51	Buck	36.0
14.0	14.8	647.12	0.40	0.05	Boost	5.8
21.6	14.8	647.12	0.40	0.69	Buck	36.0
14.0	18.5	500.30	1.31	0.24	Boost	34.0
21.6	18.5	500.30	1.31	0.86	Buck	26.5

derive the current ripple, ΔI_l. These two were then used to calculate the Inductance (L) with Equation 3.3. From the table, there is a trend where increasing the V_{bus} leads to a larger inductor and a smaller current ripple. The shrinking inductor current ripple is desirable but the increase in inductor value is not, as a larger inductor results in a larger volume. In the $14.8V$ V_{bus} section of the table, highlighted in green, there is a minimum current ripple of $5.85mA$ and a max of $36mA$, which meets both the maximum requirement (36mA), and has the smallest minimum value from all scenarios. Note that this converter will have to boost voltages when below the 14.8 input voltage threshold, which is possible thanks to the buck-boost configuration. Lastly, the size of the inductor in the $3.7V$ case has a smaller size by 34 % (425 μH vs 647 μH) but has a minimum ripple that is 472% more than the $14.8V$ case. Due to these calculations, the $14.8V$ for V_{bus} is the best choice.

The 14.8 V for V_{bus} is also a great choice when considering the efficiency of the MPPT, since it is dependent on the net voltage difference within the bus voltage and the solar cell voltage. Keeping this voltage difference to a minimum is key to decreasing the switching losses of the switches in the MPPT and in the inductor.

3.2 Power Electronics Design

The power subsystem consists of four main components: solar cell array (SA) , batteries, battery management system, and the Maximum Power Point Tracker (MPPT).

The system has been developed to maximize the area that will be available in an 8" wafer.

3.2.1 Solar Array Design

PCBSat has a solar array that will has a similar surface area to Wafersat in order to tune the MPPT electronics to the small area and power of the solar cells in WaferSat. Since PCBSat is expected to be composed of mainly COTS components, it was important for the team to find solar cells that were appropriate for this application while reducing costs. The cells used in PCBSat will not be for flight and low-cost terrestrial cells are explored in PCBSat. Lincoln Lab is planning on embedding these solar panels into the silicon wafer with the goal of achieving an efficiency of 25%. In the PCBSat effort, a couple of undergraduates, Makita Erni and Mason Dumez, were tasked with researching Silicon based solar cells.

Table 3.11: Solar Array Design Criteria

Constraint	**Consideration**
Mass	Minimized for available surface area
Surface Area	cover enough area to provide 2.7 W of power
Efficiency	Above 20 % , depends on available COTS
P_{out}	Total array able to output over 2.7 W

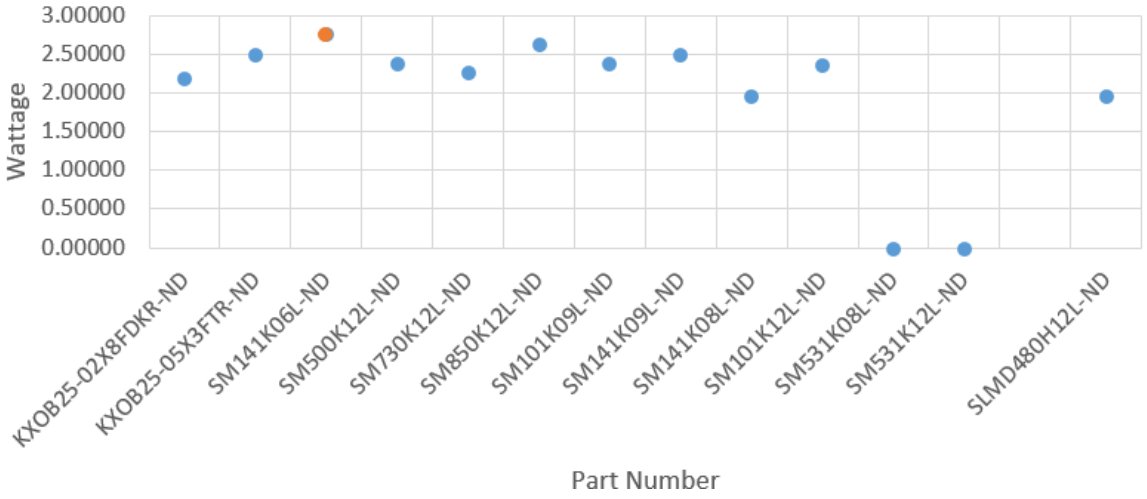


Figure 3-4: Solar Power Generated with 75 % Coverage

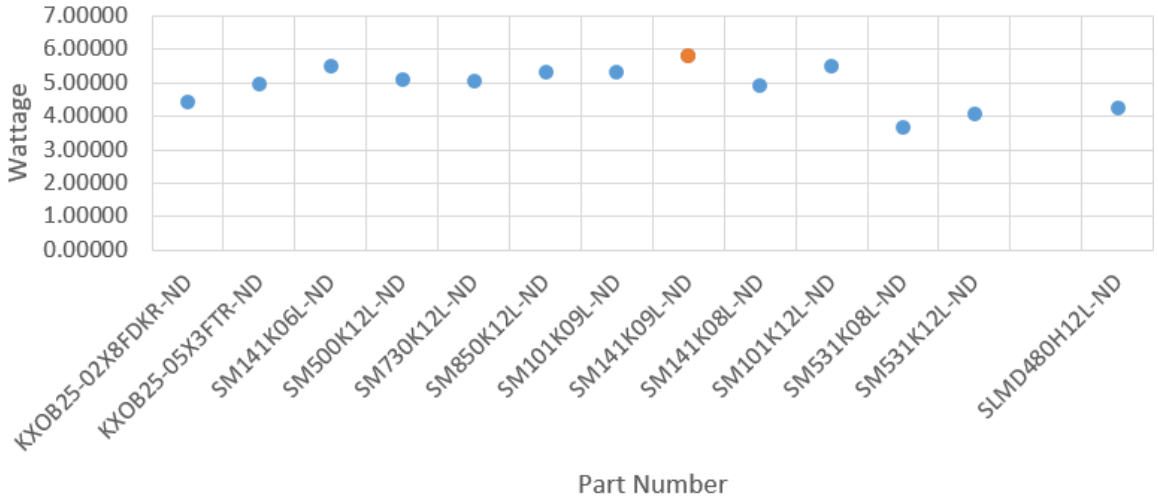


Figure 3-5: Solar Power Generated with 100 % Coverage

Based on the desired characteristics in Table 3.11, the solar cells in Figures 3-4 and 3-5 were considered and compared to each other based on the power delivered and percent of area covered. Based on the figures, it is clear that the SM141K06L-ND and the SM141K09L-ND Solar Cells will be the best choices for the largest power generation. This preliminary design allowed the students to better understand what power ranges are expected for these arrays. The physical dimensions of all solar cells are considered in Figures 3-4 and 3-5, meaning the the power generated is based on an integer number of cells that are used in an 8" circle of area. Upon further investigation, the students deduced that the SM141K09L-ND were a better option after iterating through their physical arrangement in the area provided. Based on the configuration in as seen in Figure 3-6[4]. With this configuration there could be a total of four cell strings in parallel, each composed of four series cells, resulting in 16 total cells 3-7 [5]. Inspecting the data sheet of the SM141K09L - ND, Table 3.12 can be generated.

From the table and the outlined connection diagram in Figure 3-7, a voltage of 20.08 V and a current draw of 220.4 mA are expected. These values result in a power of 4.42 W, which is well above the requirement in the power budget. This excess power

[4]Adapted from PDF from Makita Erni
[5]Adapted from PDF created by Mason DuMez

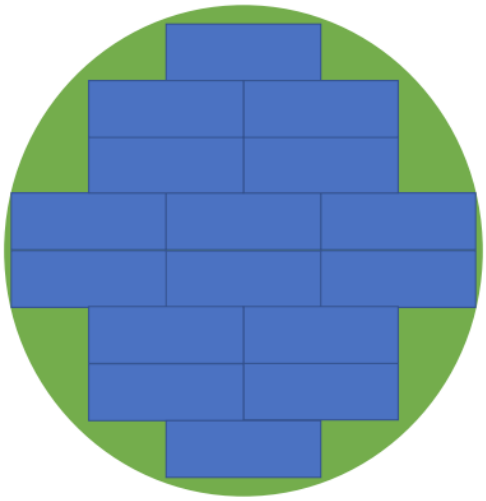


Figure 3-6: Configuration of SM141K09L-ND Solar Cell in 8" Wafer

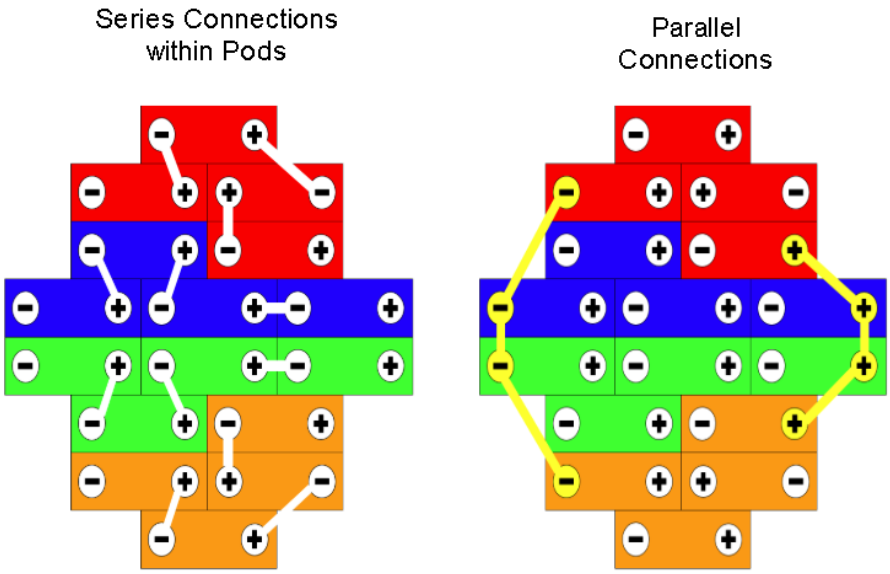


Figure 3-7: SM141K09L-ND Electrical Connections

might be a constraining feature, as this power needs to consumed in the system, and might be used to charge the batteries or might be dissipated in the heaters. In order to validate the power drawn by the solar panels, the IXYS cells were purchased and tested in the SSL. The cells were connected with the MPPT to validate at which point they operate at the maximum power point. Due to the requirements on the MPPT algorithm, the batteries and BMS are connected so that the power generated

Table 3.12: SM141K09L-ND Datasheet Facts

Characteristic	Value
Open Circuit Voltage	6.22 V
Short Circuit Current	58.6 mA
Typical Voltage at MPP	5.02 V
Typical Current at MPP	55.1 mA
Dimensions (W x L x H)	62 x 23 x 1.8 mm
Weight	5.5 g
Solar Efficiency	25 %

by the solar cells can be used to charge the batteries. Lastly, the variable load is used to consume the remaining power not used by the batteries.

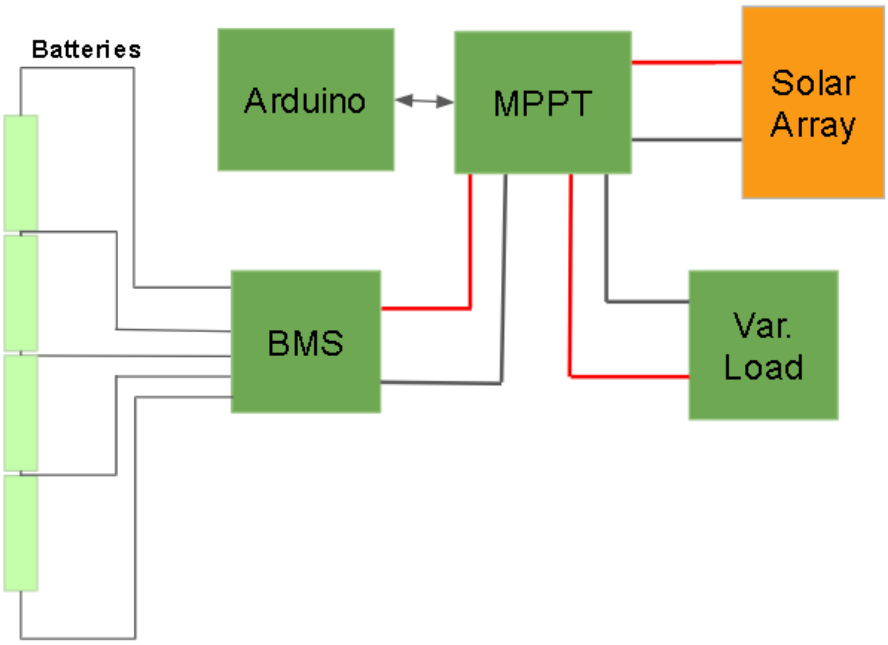


Figure 3-8: Solar Cell Maximum Power Point Testing

Furthermore, testing in the lab demonstrated that this array was not able to supply the 4.42 W. The input power may have not been as high as expeced since the light source was not calibrated. Based on the data from the solar simulator in the SSL, there was a max of about 2.5 W power draw. There needs to be further testing to be done in order to quantify the effectiveness of these solar cells.

Based on the Output Voltage to Irradiance chart provided in the IXYS datasheet, see Figure 3-10, there is a natural inefficiency in the cells. Based on our power tests

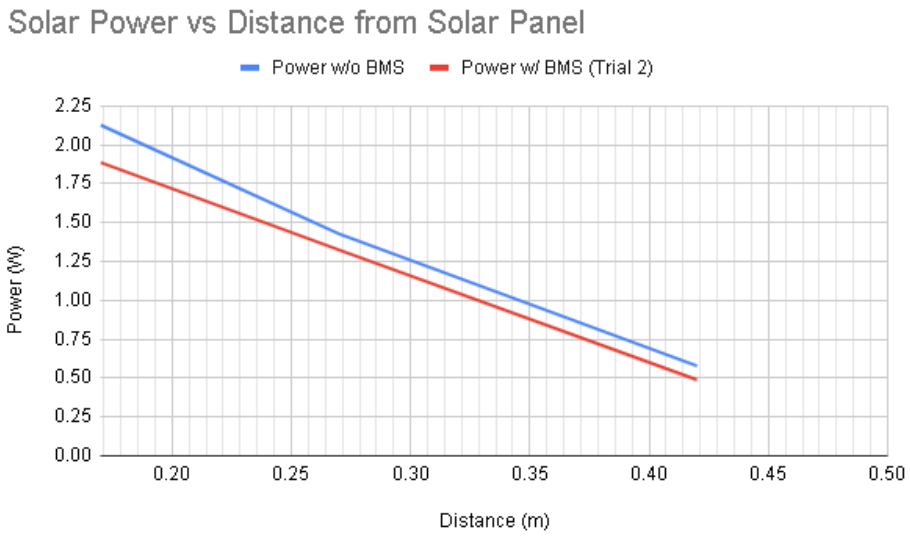


Figure 3-9: Solar Panel Power draw as a function of distance from Solar Simulator

from Figure 3-9, we can deduce that at a solar cell voltage of 16.9 V, resulting in 4.22 V per cell, which is .678 of the V_{oc}, we are expected to be operating with an irradiance of about 650 W/m^2. The 650 W/m^2 is based on the voltage fraction obtained from the solar cell testing according to Figure 3-10. Based on an irradiance meter, the measured irradiance on the center of the solar cells was measured to be 640 W/m^2, fairly similar to the model provided in the datasheet. With these results, it is expected to obtain a voltage of 4.35 V per cell (17.4 V per string) at the terrestrial average irradiance of 1000 W/m^2. With an expected current output of 55.1 mA per string (220 mA for the array), the total power produced by the array should total 3.85 W.

3.2.2 Battery Selection

One of the most constraining components in the WaferSat are the batteries. Despite the advances in battery development over the past decades, batteries still remain as one of the heaviest and most voluminous components of most small satellites [20]. Due to the small nature of WaferSat and PCBSat, there is a large incentive to find batteries that are both light and thin. It is important to also note that WaferSat will not have any chassis or enclosure that will contain the batteries, meaning that the batteries will have to sit on top of the wafer or protrude from the surface. This situation is

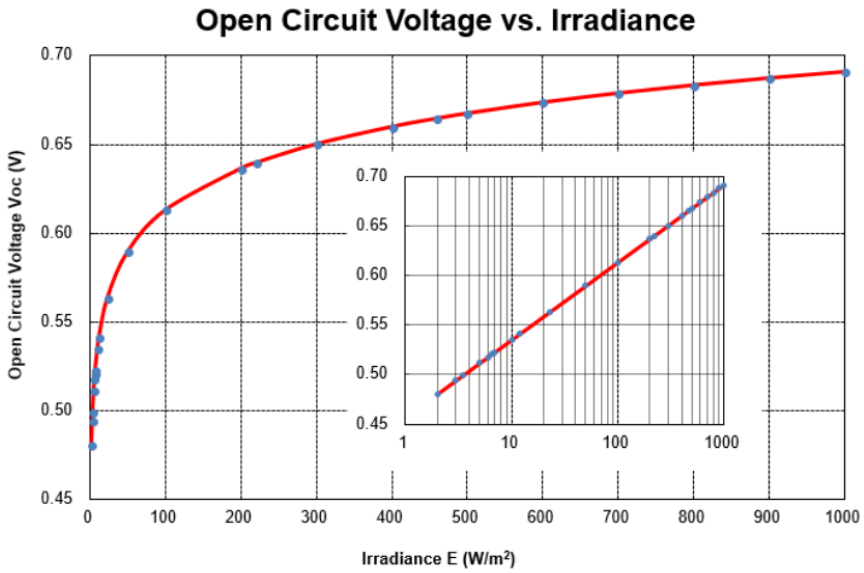


Figure 3-10: IXYS Solar Cell Open Circuit Voltage vs. Irradiance

depicted in Figure 3-11. Having the batteries outside of the wafer will increase the frontal area and as a result increase drag and a decrease orbital lifetime. The increase in drag and consequential loss of altitude can be counteracted with attitude control but that results in the need for more propulsion (mass) and ACS on-time (higher power/orbit). Furthermore, these batteries will be exposed to the harsh environment of space, meaning that they will be cycling through extreme temperature ranges (-30 C to + 70 C). The wide temperature ranges reduce the selection pool for batteries and adds a high demand in power for the electrical system to provide in order to heat up these batteries.

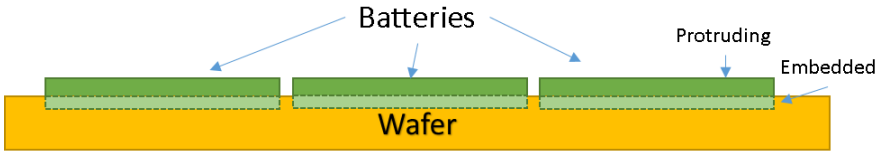


Figure 3-11: Cross Sectional view of a Wafer with Partially Embedded Batteries

Based on the power requirements and the bus voltage determined in the previous sections, there is a need to get a string of batteries that will have a nominal voltage of approximately 14.8 V and have a current draw of 180 mA at the worst case. With

a cell voltage of about 3.7 V, there will be a total of four cells needed in order to power the system.

For the purpose of PCBSat, it is assumed that a total power draw of 1.9 W [6] will be enough to keep the batteries in a warm enough condition for them to operate through the eclipse region of each orbit. For the time of the writing of this thesis, there has not been any final decision of the total power required to maintain the batteries heated to a safe temperature.

The PGEB014461 battery from General Electronics was selected as the prototype battery for PCBSat. The Polymer Lithium-Ion batteries are COTS and have desirable characteristics that could make it ideal for a flat satellite. These characteristics are outlined in Table 3.13

Table 3.13: PGEB014461 Datasheet Specifications

Parameter	**Value**
Nominal Capacity	210 mAh
Nominal Voltage	3.7 V
Max charging current	1C
Max Discharging Current	2C
Dimensions (W x L x H)	44 x 60 x 1 mm
Weight	6 g
Impedance	180 $m\Omega$
Operating Temperature	-20 - 45 C for 1 Month -30 - 35 C for 6 Months

One specification that sticks out on the PGEB014461 is that it is flat, at almost 1 mm in thickness. This short thickness is promising for this battery model and for other candidates. The datasheet also provides insight on the lifespan of the batteries depending on the temeprature ranges they are exposed. While exposed to higher temperatures, the PGEB014461 appears not last as long.

3.2.3 Battery Management System Design

Since more than one battery cell is present in this system, there is a need to include a battery management system (BMS) in order to extend the lifespan of these batteries

[6]Based on heat power estimate from Michael Fifield

and prevent over/under voltages and voltage mismatches between them. Due to the great benefits of the high energy to weight ratio that Lithium-Ion batteries have, it was decided to look for a Battery Management System that would have many control parameters for how the battery were to be charged:

- Variable battery chemistries
- Temperature sensing
- Charge balancing
- Charge cutoff
- Charge monitor
- 1 - 4 Cell adaptable
- I^2C Compatible

After some research, the BQ40Z50 was the chosen candidate for our application, as the chip met all of the above requirements and was available in a small form factor (4 mm x 4 mm) and with low power consumption (5 mW). A couple of things to note from the schematic in Figure 3-12 is the presence of three high power switches, that control the charge and discharge of the BMS. It also includes four temperature sensors: TS1, TS2, TS3, and TS4 that monitor each cell's individual temperature. Monitoring the individual temperature of each battery is key to know the health of the batteries over time.

3.2.4 Maximum Power Point Tracker Design

The Maximum Power Point Tracker is one of the essential power converters in this system. There are two COTS chips that satisfy the design criteria listed in Table 3-2: Texas Instruments' (TI) BQ25703A and the Linear Technology's' (LT) LTC4015. Both of these chips have a solar cell interface, multi-chemistry digitally configurable battery charging, power monitoring, and a digital interface. The BQ25703A has an

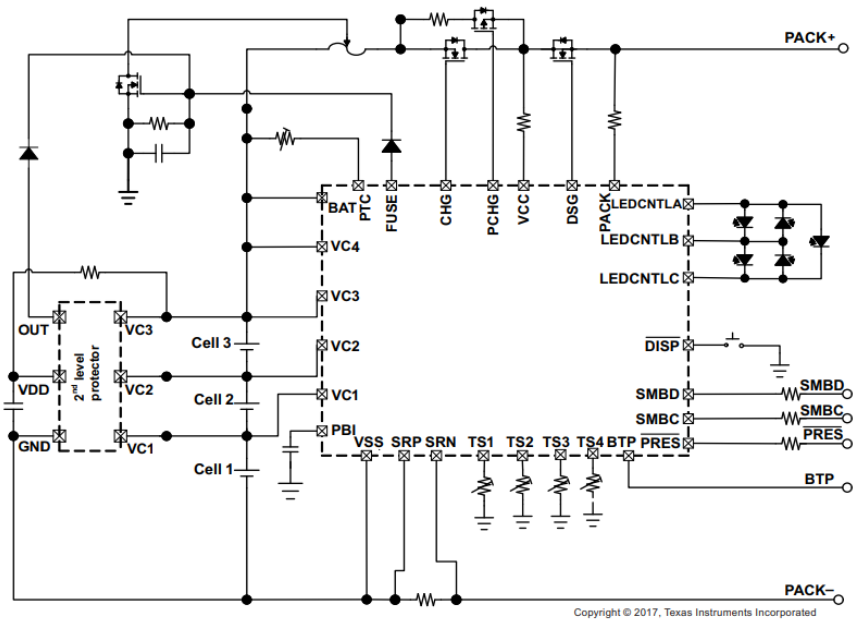


Figure 3-12: Schematic taken from BQ40z50 Datasheet from Texas Instruments

input range of $3.5-26V$ and an output range of $3.2-19.5V$, making it appropriate for the desired inputs and outputs. It also includes an advanced power path management, meaning it can keep a constant output voltage meanwhile it dynamically charges the battery at varying voltages. It also has the capability to connect the battery directly to the bus, allowing for the battery to send bursts to the spacecraft when high power applications were needed. The LTC4015 has an input range of 4.5 - 36V and an output of $0-35V$, also meeting our requirements. The LTC4015 has a coulomb counter that allows the system to know the state of charge of the battery system. The coulomb counter is important for the long term stability of the batteries, as knowing how much they charge and discharge per cycle can inform the system of its degradation. It also has a built-in MPPT algorithm, reducing the complexity needed to program it. Lastly, it is able to adjust the power balance between the battery system and the solar panels, especially when they are in the same voltage range, which maximizes efficiency. The different features and summarized in Table 3.14.

The BQ25703A was selected since it was able to power the system when the battery is depleted, has a buck-boost topology, and has better power management

Table 3.14: Comparison of MPPT IC Chips BQ257 and LTC4015

	MPPT Chips	
Feature	**BQ25703**	**LTC4015**
Solar Cell Interface	Yes	Yes
Power Monitoring	Yes	Yes
Multi-Chemistry Battery Charging	Yes	Yes
Advanced Power Path Management	Yes	No
Battery-Bus Direct Connect	Yes	No
Built-in MPPT algorithm	No	Yes
Coulomb Counter	No	Yes
Topology	Buck-Boost	Buck
V_{in}	$3.5V - 26V$	$4.5V - 36V$
V_{out}	$3.2V - 19.5V$	$0V - 35V$

that notifies the system of too much power consumption. The BQ25703A provided more versatility and had features that were desired for this application.

The BQ257 has a topology similar to a Buck-Boost converter but has a additional resistors that allow it to measure the current flowing into and out of the controller. As seen in Figure 3-13, there are four switches (Q1, Q2, Q3, and Q4), an Inductor (L), and input and output capacitors. There is an extra switch on the output that serves as a connection to charge the batteries connected to this controller.

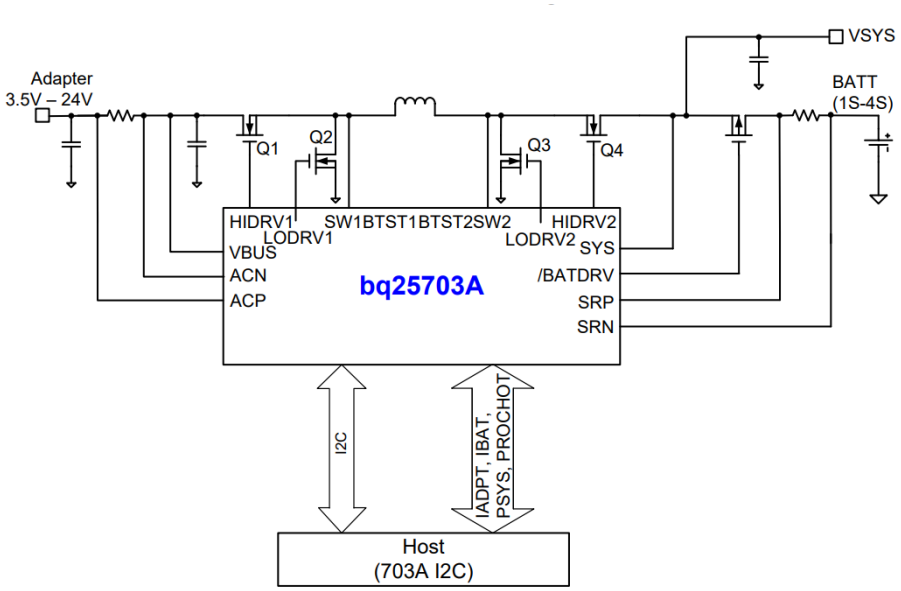


Figure 3-13: Schematic taken from BQ257 Datasheet from Texas Instruments

The first step in designing the power components that support the MPPT is fully understanding the system inputs and outputs. The power inputs, P_{in}, V_{in}, and I_{in}, are all set by the solar panel and are variable within a range. These ranges are based on the solar exposure that is expected in orbit. The output voltage V_{out} is bounded by the charging voltages of the battery. P_{out} and I_{out} are matched according to the expected current and power draw from the system. These values are listed in Table 3.15

Table 3.15: MPPT Electrical Interface Requirements

Parameter	**Value**	**Description**
f_s	750 kHz - 1.5 MHz	Frequency range expected for limiting component size
P_{in}	2.2 W - 3.85 W	Estimated power range from solar array
V_{in}	10.04 V - 17.4V	Estimated voltage range from solar array
I_{in}	220 mA	Estimated current from solar array
P_{out}	2.2 W - 3.85 W	Assuming 90% efficient, steady state at 2.65 W
V_{out}	14.8 V $\pm$ 10 %	Desired for battery charging
I_{out}	180 mA	Expected output current

From the datasheet of the BQ257, it can be observed that there are two fixed frequencies in which to operate: 800 kHz or 1.2 MHz. It is preferred to operate at higher frequencies, since these lead to smaller component values and sizes. For instance, in a buck converter, the inductor size is inversely proportional to the switching frequency f_S, as seen in Equation 3.4 (Assuming all other values in the equation remain the same).

$$L = \frac{V_{out} \times (V_{in} - V_{out})}{\Delta I_L \times f_S \times V_{in}} \tag{3.4}$$

Inductor Selection

One of the most important components to choose in the design of the MPPT is the inductor. The inductor will limit the amount of current ripple and thus voltage ripple that will be observed in the output. The BQ25703 datasheet provides four possible operating inductor values: 1.1 μH, 1.5 μH, 2.2 μH, 3.3 μH. The 1.1 μH, 1.5 μH will operate at 1.2 MHz while the 2.2 μH, 3.3 μH operate at 800 kHz. When selecting an inductor, there should be some computation to determine the limits of the inductor,

more specifically its saturation current. If the application demands the inductor to go above its saturation current, it will not be able to operate properly. This saturation current is calculated as shown in the following equation:

$$I_{sat} \geq I_{chg} + \frac{1}{2} I_{ripple} \tag{3.5}$$

From the power budget section, it was determined that the average I_{CHG} is .182 A, and can be used in this equation. In order to calculate a realistic ripple current, both the buck and boost ripple currents should be determined as follows:

$$D_{buck} = \frac{V_{out}}{V_{in}} \tag{3.6}$$

$$I_{ripple-buck} = \frac{V_{in} \times D_{buck} \times (1 - D_{buck})}{f_S \times L} \tag{3.7}$$

$$D_{boost} = 1 - \frac{V_{in}}{V_{out}} \tag{3.8}$$

$$I_{ripple-boost} = \frac{V_{in} \times D_{boost}}{f_S \times L} \tag{3.9}$$

With these equations, the minimum ripple current can be calculated based on the ranges of input voltage and inductor size combinations. The results of these calculations are outlined in Figures 3-14 and 3-15.

Based on these results, the 3.3 μH inductor operating at 800 kHz, generated the smallest maximum current ripple of 1.76 A, which might seem large but it is feasible for small periods of time. With this result, it can be calculated that our minimum saturation current I_{SAT} has to be greater than 1.062 A. The inductor of choice was the Wurth Electronics 74438323033 3.3 μH that is rated for 1.25 A and has an I_{SAT} of 2.1 A (97 % higher than our required limit). It also has a relatively small resistance of 220 $m\Omega$ and a small form factor of 4.2mm x 2.7mm. The Buck-Boost MPPT was simulated in PLECS, a power electronics simulation software, at the operating frequency of 800 kHz, in order to prove the current ripple requirements mentioned above.

From the simulation in Figure 3-17, it can be concluded that our output will be

MPPT Inductor Design Buck

V_in (V)		V_out (V)	F_s (kHz)	D	L (uH)	I_ripple (A)
Minimum	15.00	14.80	1200.00	0.99	1.00	0.16
Estimated MPP	17.00	14.80	1200.00	0.87	1.00	1.60
Datasheet MPP	20.00	14.80	1200.00	0.74	1.00	3.21
Max	21.60	14.80	1200.00	0.69	1.00	3.88
Minimum	15.00	14.80	1200.00	0.99	1.50	0.11
Estimated MPP	17.00	14.80	1200.00	0.87	1.50	1.06
Datasheet MPP	20.00	14.80	1200.00	0.74	1.50	2.14
Max	21.60	14.80	1200.00	0.69	1.50	2.59
Minimum	15.00	14.80	800.00	0.99	2.20	0.11
Estimated MPP	17.00	14.80	800.00	0.87	2.20	1.09
Datasheet MPP	20.00	14.80	800.00	0.74	2.20	2.19
Max	21.60	14.80	800.00	0.69	2.20	2.65
Minimum	15.00	14.80	800.00	0.99	3.30	0.07
Estimated MPP	17.00	14.80	800.00	0.87	3.30	0.73
Datasheet MPP	20.00	14.80	800.00	0.74	3.30	1.46
Max	21.60	14.80	800.00	0.69	3.30	1.76

Figure 3-14: Inductor Ripple Analysis for Buck Converter

Figure 3-15: Inductor Ripple Analysis for Boost Converter

MPPT Inductor Design Boost

V_in (V)	V_out (V)	F_s (kHz)	D	L (uH)	I_ripple (A)
14.00	14.80	1200.00	0.05	1.00	0.63
14.70	14.80	1200.00	0.01	1.00	0.08
14.00	14.80	1200.00	0.05	1.50	0.42
14.70	14.80	1200.00	0.01	1.50	0.06
14.00	14.80	800.00	0.05	2.20	0.43
14.70	14.80	800.00	0.01	2.20	0.06
14.00	14.80	800.00	0.05	3.30	0.29
14.70	14.80	800.00	0.01	3.30	0.04

close to the 14.8 V requirement and will have a voltage ripple of only .014 mV, which is small and desirable. The output current in the middle plot of Figure 3-17 is also the expected value for the 2.65 W power output.

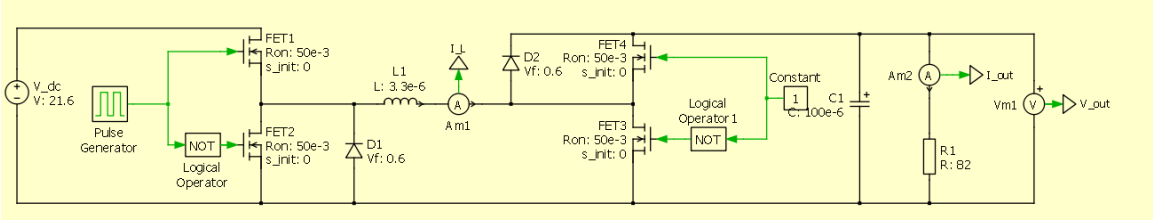


Figure 3-16: PLECS Model of the MPPT

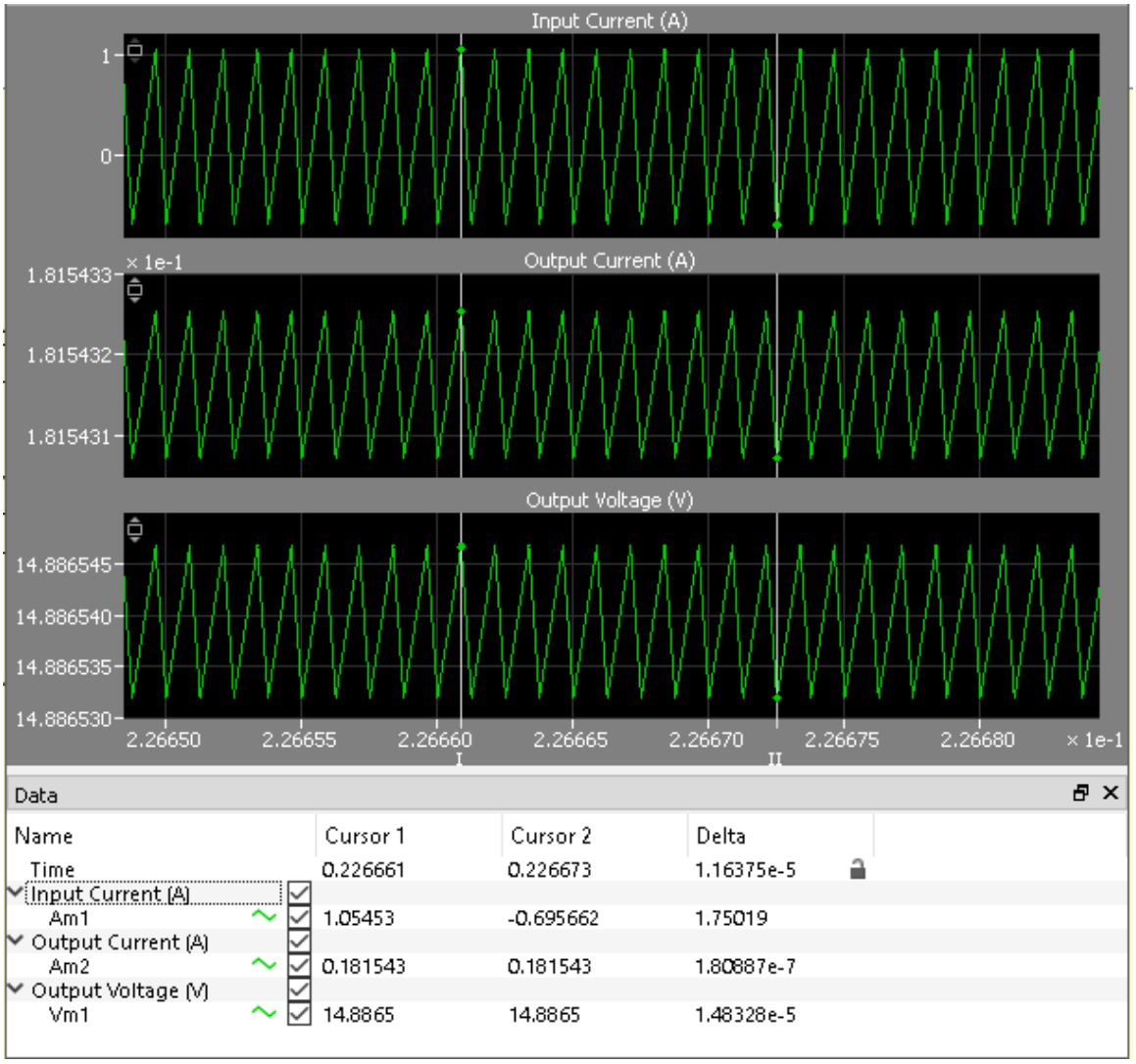


Figure 3-17: Inductor Ripple Analysis for Boost Converter

MOSFET Selection

After selecting the inductor, the switches need to be determined. The switching requirements are outlined in Table 3.16. The switches need to be able to operate

at the switching frequency set by the MPPT. Furthermore the switches need to be able to sustain over 25 V across them without breaking down. The series resistance R_{DS} is the desired to be as low as possible since this leads to lower power loss in the switches. Lastly, the switches are expected to handle the inductor current. The switches of choice was the Vishay Si3424CDV-T1-GE3 n-channel Power MOSFETs. The Vishay part was chosen since it met all of the necessary requirements and it was available in a small form factor.

Table 3.16: Power MOSFET Electrical Requirements

Feature	**Value**
F_{Smin}	800 kHz
V_{DS}	$>$ 25 V
R_{DS}	$<$ 100 mΩ
I_{DSmax}	$>$ 2 A

Table 3.17: Vishay Si3424CDV-T1-GE3 Electrical Characteristics

Feature	**Value**	**Requirement Met?**
F_S	10 MHz	Yes
V_{DS}	30 V	Yes
R_{DS}	32 mΩ	Yes
I_{DSmax}	8 A	Yes

3.3 Microcontroller - ATSAM V71

One of the most critical components of any spacecraft is the Central Processing Unit (CPU). The CPU hosts all of the algorithms and processes all of the actions that the spacecraft takes. It is important to have a CPU that can meet the needs of the spacecraft. Initially, it was expected to have the MSP430 as the microcontroller used in PCBSat. The microcontroller's main constraint is operating the ADCS control loop, as that is expected to be the most intensive software loop. There is a requirement on the ADCS control loop which should run at 1 Hz, but expected to operate at 10 Hz (or complete a cycle in 100 ms). We are expected to go through 60 trig functions and about 200 other computations. With the MSP430 running at 8MHz, it is expected

to complete a loop in 10ms, which fulfills the requirement. Despite meeting this requirement, there may be a need to incorporate position control, previously had only used angular control, which might double the processing requirement, thus making it not sustainable for this processor. The lack of processing power motivated the search of a processor that could handle these computations. The Atmel SAM V71 came up as a worthy candidate after it was determined that it could handle the processing power for the ADCS algorithm, which was estimated to require a total of 2.88 kbits (360 bytes) [7]. Furthermore, the ATSAM V71 that has many expandable capabilities that can enable future developments in the PCBSat effort. Below is a list of the features that made the ATSAM V71 the choice for this project.

- Operating Frequency up to 300 MHz
- 16 Kbytes of ICache
- 2048 Kbytes of Embedded Flash
- 16 Kbytes ROM
- Low Power Sleep Mode
- Three I2C ports with SleepWalking support
- Two PWM
- 114 I/O lines
- Single supply voltage of 3.3V

The microcontroller was evaluated on its ability to reduce the part count of the power system. For instance, the ATSAM V71 has 4 internal Analog-to-Digital Converters (ADC) which are used to read voltages of interest in the PCB. Having these inside of the microcontroller reduce the part count by 6 - 7 parts per ADC.

Lastly, the microcontroller's ability to communicate and control the power chips (BMS and MPPT) is very important, so a processor with lots of processing power

[7] Adapted from a report created by Daniel Freeman and Edmund Chin

was picked. Since the ATSAM V71 is able to handle the computing process of the ADCS, it was found adequate to also process the MPPT and BMS algorithms since they are not as computationally demanding.

3.4 Summary

This chapter explored the design of the power subsystem of PCBSat. The research and selection of the solar array, batteries, battery management system, MPPT, and microcontroller were investigated and developed for their implementation in PCBSat. The following chapter goes further into the schematic design, PCB design, and testing of these systems.

Chapter 4

Implementation on PCBSat

The schematics and PCB layout are explored in this chapter, focusing on the decisions made in implementing the subsystems. All subsystems are further analysed by their component size, requirements and interactions with each other. Furthermore, the software development is discussed, highlighting the PCB's functionality.

4.1 Preliminary Designs Implemented in PCBSat

The design of the schematics of PCBSat were a joint effort by Xavier Zapien and Edmund Chin from Lincoln Lab. Xavier designed the initial version and Edmund revised and expanded the designs for implementation on the PCB. These can be found in Appendix A and will be referenced throughout this chapter. The layout of the PCB was conducted by Edmund Chin. The schematics were initially derived from multiple sources: datasheets from the ICs, past schematics from students, and from our past experiences.

4.1.1 Maximum Power Point Tracker

The MPPT is contained within Label G, with the solar power connector labeled in A. The MPPT takes up 50.8 mm x 37.2 mm. This size could be decreased further by investing in a higher density output capacitor bank or increasing the capacitor

count to reduce height, which would reduce the area and height of C_{out}. Besides the BQ25703 MPPT Chip, the largest components is the inductor (4.2mm x 2.7mm). The inductor is constrained based on our expected current demands. As observed in Figure 4-1, the capacitor C151 is 100 uF, which for this design is acceptable, but it can be equivalently be created with five 20 uF capacitors in parallel. The larger number of capacitors can increase the area covered by the net capacitor but greatly reduce potential drag. Furthermore, Port P171 will not be present in the next version of PCBSat as this is a selector between one and four batteries. Once the total battery count is finalized, this port will not be required and the resistors will be connected without future adjustments.

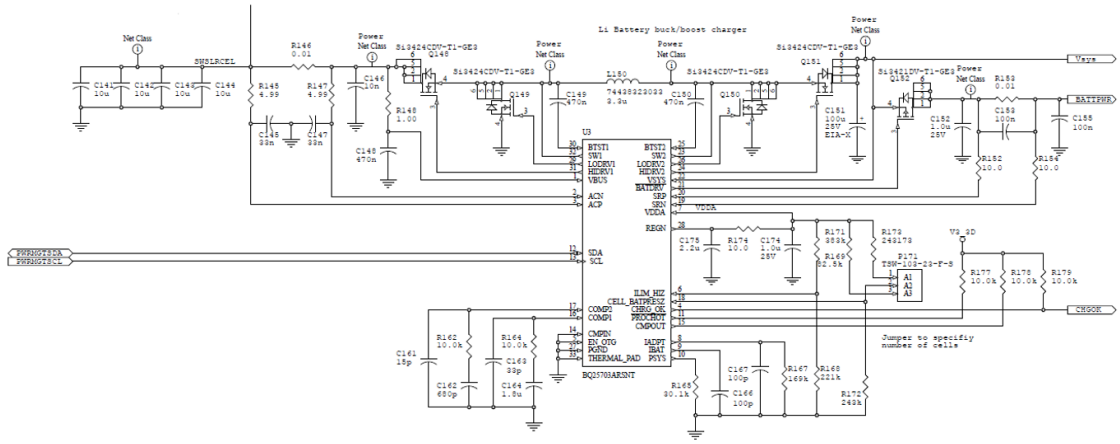


Figure 4-1: PCBSat MPPT Schematic

4.1.2 Power Regulators

As seen in Figure 4-2, the power regulators can be set to take power from the BATTPWR or from an external power source, depending on where Switch S6 is set to. BATTPWR is the bus with regulated output voltage from the MPPT. BATTPWR supplies power to charge the batteries and power the board. The switch was added to allow the board to be debugged without the need of a working MPPT, batteries, BMS, or solar cells. This bypass makes it easy for the board to be programmed with the use of a lab power supply, suggested by Edmund Chin. This switch enables the

designer to ensure that the microcontroller, IMU, heaters, temperature sensors, and GPS can still be tested without implementing two algorithms (MPPT and BMS).

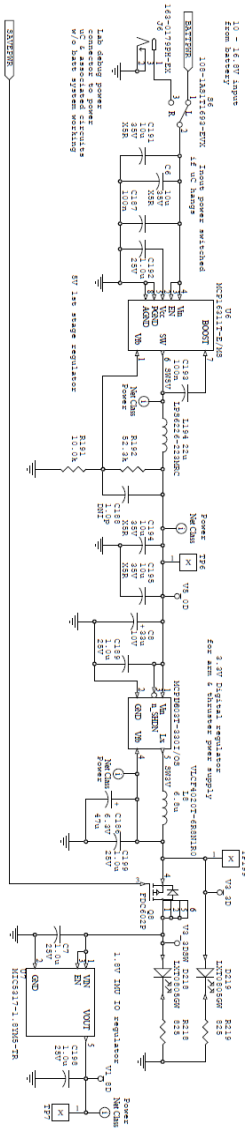


Figure 4-2: PCBSat Power Regulators 5V, 3.3V and 1.8V Schematic

The power step down stage is composed of cascaded 5V, 3.3V, and 1.8V power regulators, occupying an area of 51.5 mm x 18.5 mm. The multi-stage step down is required due to the varying input demands from the several ICs and potential extra peripherals. If power is provided to the 5V regulator, it will simultaneously output 5V and supply power to the 3.3V regulator. Two LEDs (D218 and D219) are connected to the output of the 3.3V regulator. If the board is on and both power regulators are

on, D219 will light up. D218 is blocked by a MOSFET (Q8) . Q8 has to be turned on by the microcontroller by pulling the SAVEPWR signal to low on start up. Once SAVEPWR is low the V3.3DSW line is powered on, Diode D218 turns on, and the 1.8 voltage regulator powers on. This switch is able to power cycle the I^2C bus if an issue arises where the bus is "hung up". When the bus is "hung up", the voltage floats in a middle range and does not allow any signals to go through it. The I^2C bus needs pull-up resistors connected to 3.3V in order to function, so dropping this voltage and restarting to 3.3V might solve the bus issues.

4.1.3 Battery Management System

The BMS (32.4 mm x 26.9mm) schematic is found in Figure 4-3 and includes the Watchdog Timer (28.2 mm x 18 mm). The BQ40z50 is represented by the U2 IC, and uses four switches (Q107, Q113, Q112, and Q111) to source power from four batteries. It then uses three more switches (Q121, Q125, and Q128) to source power back to the batteries. One key feature that this BMS has is the ability to conduct separate temperature measurements for each cell.

4.1.4 Thermal Subsystem

The thermal subsystem schematic is found in Figure 4-4 and is composed of four BJTs (Q271, Q272, Q273, Q274) that get powered on by the HTREN signals from the ATSAM V71. The heaters control the energy dissipated in four external heaters, that are not included in the PCB. The heaters were left as external to the board for this revision of PCBSat since there was a need to complicate the system with embedded heater traces. There are eight temperature sensors across the board (U20 - U27). There are four sensors on the top sides and four more on the bottom sides of the board. These temperature sensors were placed in these locations to get an average of the board temperature and to see how well the heat gets distributed on both sides of the PCB. These share the same I^2C data and clock lines and have their addresses labeled next to them.

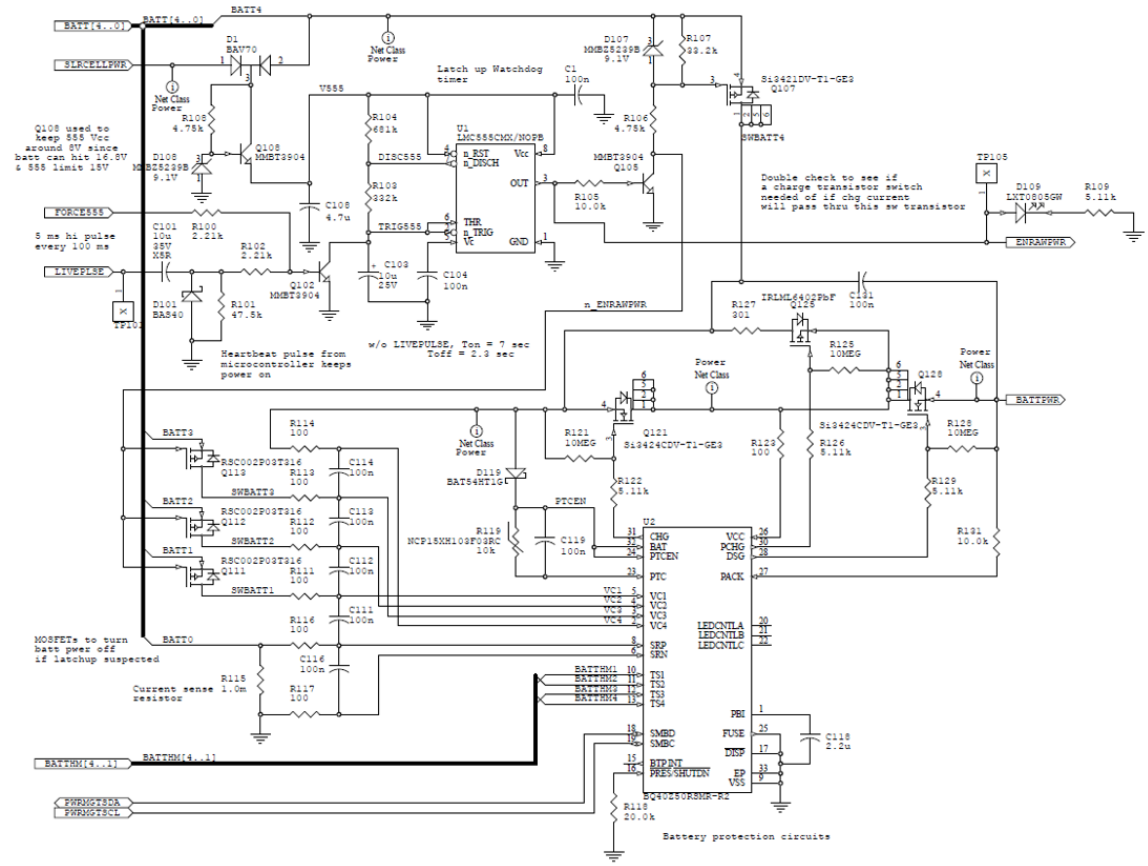


Figure 4-3: Battery Management System and Watchdog Timer Schematic

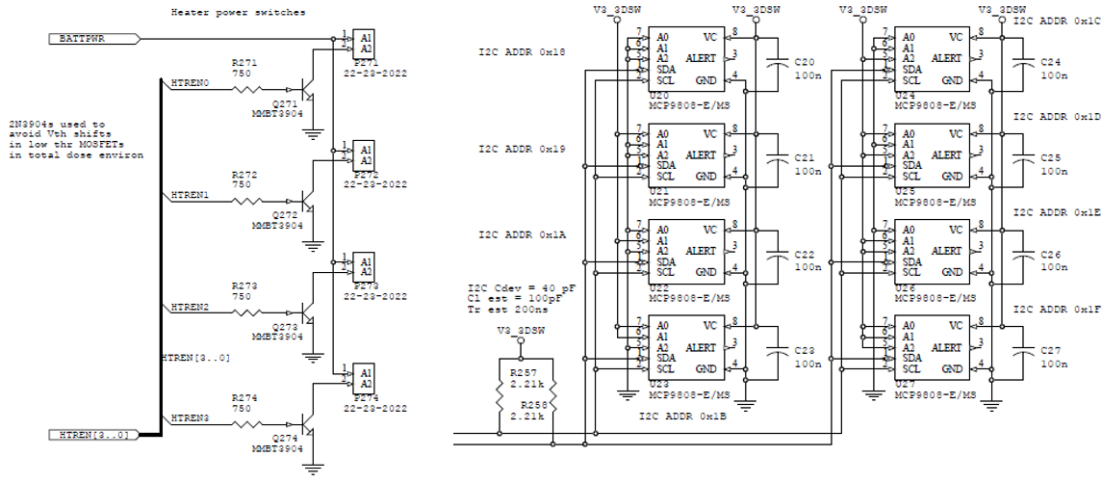


Figure 4-4: Thermal Subsystem Schematic

4.1.5 Microntroller

The ATSAM V71 is by far the largest IC on the board (40 mm x 39.4 mm). Furthermore, the microcontroller limits lots of routing, since its 144 pins each need a line

coming out of them, which means that no vias or other communication lines can pass through those sections of the board.

4.1.6 Physical Layout

Measuring at 19 cm x 12.6 cm, PCBSat was designed as a two layer board, but with almost all of the components on the top side, with only a couple of temperature sensors spread on its underside. The board was designed to have some versatility, as the off-board components can be easily connected and disconnected and could be replaced. For instance, there is an universal connector for the batteries. The universal connector allows PCBSat to be tested with different types of batteries, without altering the layout or components on the board. Furthermore there are multiple ports that can be used to monitor or debug the signals on the PCB. In Figure 4-5, the majority of the ports, subsystems, switches, and chips are labeled for the readers advantage and their explanation is found in Table 4.1.

Table 4.1: PCBSat Board Layout Description and Schematic Sheet Location

Label	**Component**	**Schematic Page**
A	Solar Cell Connector	1
B	External Heater Connectors	1,7
C	Battery Connectors	1,2
D	BMS	2
E	Watchdog Timer	2
F	External Power Switch	4
G	MPPT Charge Controller	3
H	5V and 3.3V Regulators	4
I	Payload Connector	1
J	Embedded Breadboard	9
K	Analog Multiplexer	7
L	IMU	6
M	Temperature Sensor (1/8)	6
N	I^2C Multiplexer	6
O	GPS Connectors	1
P	USB Debugger Ports	8
Q	I^2C BEAGLE Debugger	5
R	ATSAM V71 Microcontroller	1,4,5
S	Reset Button	4

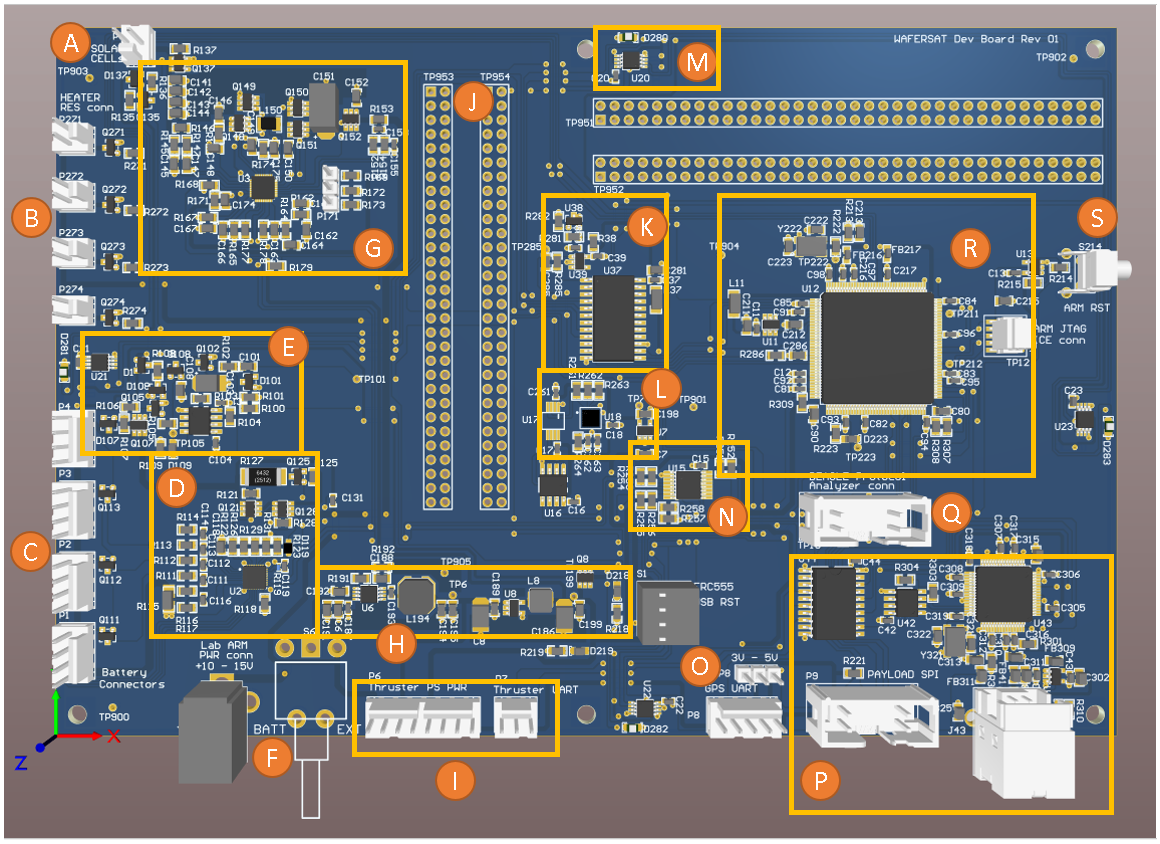


Figure 4-5: Subsystems of PCBSat

4.2 Software Development

There are three main algorithms running in the microcontroller: ADCS Thruster control loop, MPPT perturb and observe algorithm, and the heater closed-loop control. These three are controlled within the flight software package that will run on the Microchip ARM microcontroller. Currently, these three algorithms do exist in three separate Arduinos and are functional in the prototypes of SWaP-Sat. One of the main difficulties going forward is being able to integrate these all into one microcontroller and be able to have them run concurrently and have the same efficiency and speed.

To begin development, the functions were implemented individually on the SAM. Meaning that the SAM will have to be reprogrammed every time a new algorithm is tested. Current plans are to create an operating system that can run all four algorithms on the SAM V71. One of the initial functions of the code will be to communicate with the peripheral chips of the SAM V71. This communication is

done through the I^2C communication protocol. The I^2C bus is expected to be operating at 400 kHz, which is compatible with all of the peripheral chips. PCBSat uses a splitter on its I^2C lines to reduce capacitive loading on the data and clock line. Capacitance loading is proportional to copper length, meaning that the shorter the patch for signals to travel, the better. The I^2C communication diagram is present in Figure 4-6 and allows the SAM V71 to communicate to three channels labeled as: PWRMGTSDA , IMUSDA, TMPSDA. PWRMGTSDA is a dedicated channel for the Power Management subsystem consisting of both the BMS and the MPPT. The splitter has the option to enable or disable one or all channels at once, so limiting the number of channels that are enabled at any given time is critical to maintaining signal integrity on the I^2C bus. The IMUSDA channel contains the IMU and the EEPROM, since both are not accessed as frequently as the other two channels. The IMU is assisting the determination and orientation of the satellite, meanwhile the EEPROM is used as a memory bank in the case of any shutdowns. Future code will be written to have the current state of the SAM V71 to be stored in the EEPROM for use on reboots. Lastly, the TMPSDA channel is used to read the eight temperature sensors. Since the sensors are physically distributed across the board, the I^2C lines (Data and Clock) gain capacitance, making this channel the slowest of all three. Luckily the temperature sensors do not need to be sampled at high speeds so a small latency will not affect its performance.

4.2.1 MPPT Software

The MPPT is one of the most critical components in PCBSat and its algorithm's efficiency drives the total efficiency of the power system. The datasheet of the manufacturer provided a starting point for the software development. From this datasheet, all of the commands, register addresses, and requirements were compiled. Prior to developing software, it is important to develop a block diagram of the intended program. Block diagrams like in Figure 4-7 give any engineer in the team a visual way to understand the algorithms of the system, as these can be complex. Being able to explain an algorithm without stepping through each line of code is key to the success

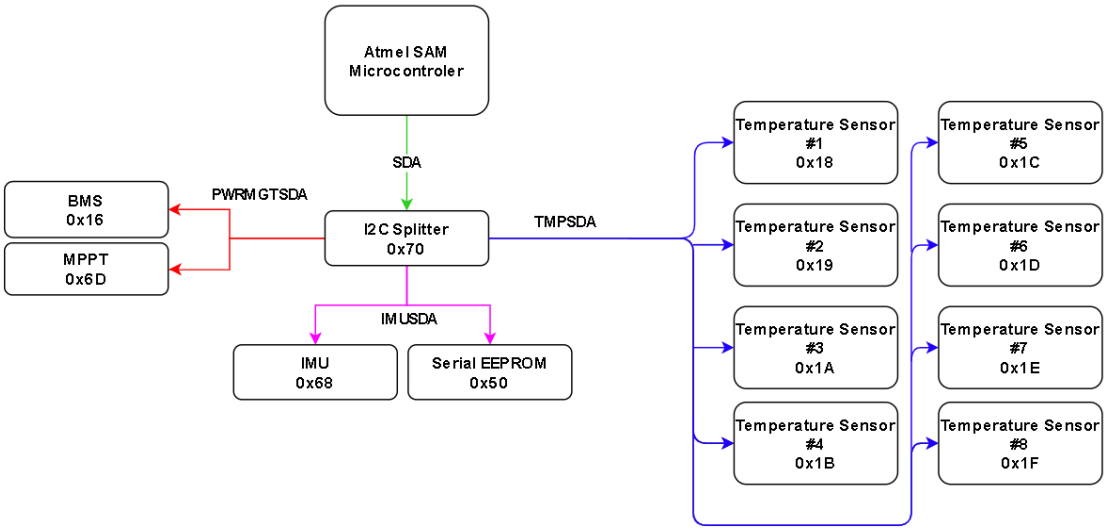


Figure 4-6: I^2C Communication Diagram for PCBSat

of its implementation. Block diagrams reduce the amount of confusion and increase the chances to catch a methodical error prior to implementation. Lastly, the block diagram really helps in the structure of the program, as it allows the programmer to not go too deep into the implementation without first understanding the big picture and the purpose of the program.The block diagram in Figure 4-7 was developed to implement the Perturb and Observe algorithm for the MPPT.

The setup initializes all of the parameters that are specific for this application: Battery count, over voltage in input, desired output voltage, desired output current, and etc. Peripherals are also initialized in this step, such as any external Analog-to-Digital Converters (ADCs). After this step, the MPPT moves onto the Kickstart state, where it uses the ADC to measure the input voltage (solar cell voltage), connects to the input source, and determines the initial value for vSetpoint. If there are no errors it continues towards the Perturb and Observe algorithm stage. If it finds any errors with the input, it restarts and goes back to the setup stage. When it reaches the Perturb and Observe stage, it branches towards the top right flow chart of Figure 4-7, where it uses an ADC to sample and read an average voltage from the solar input. It then also measures the input current and multiplies it with the voltage to

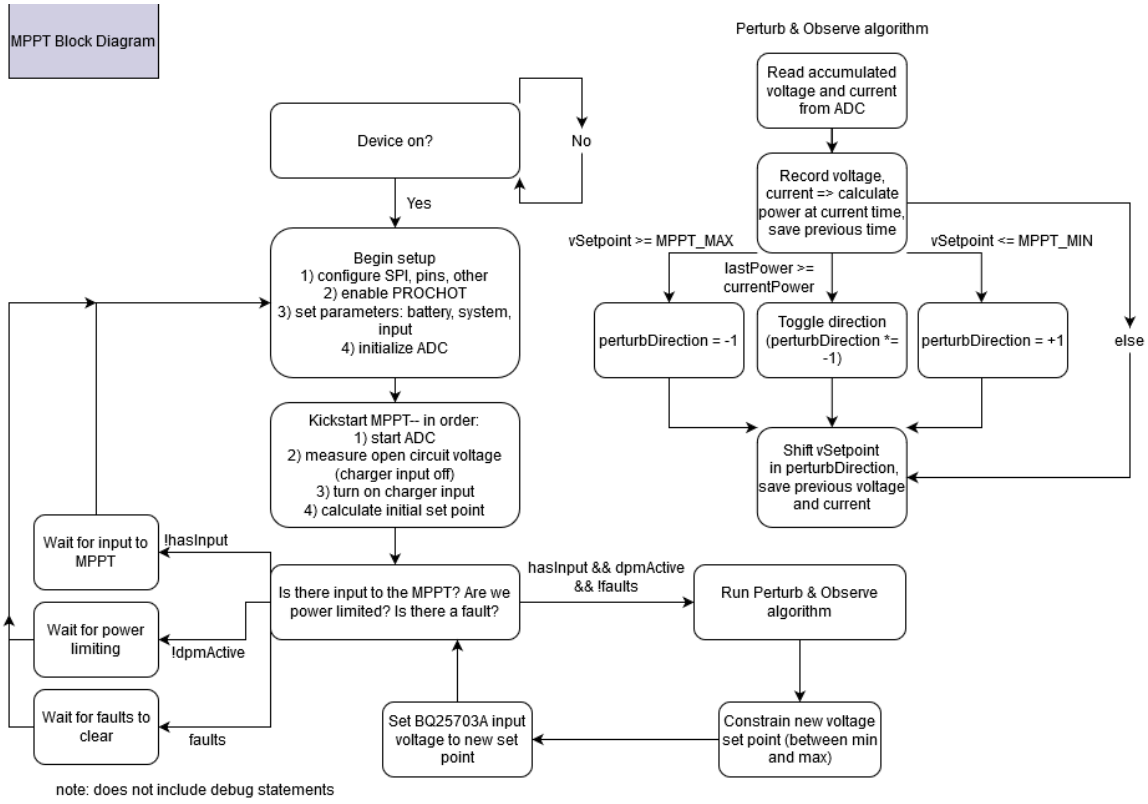


Figure 4-7: MPPT Software Block Diagram

calculate the input power.

$$P_{in} = V_{in} \times I_{in} \tag{4.1}$$

The MPPT is able to control the voltage over the operating range of the solar array so the power point moves along the I-V curve of the solar panels based on a voltage setpoint (**vSetpoint**). Due to the nature of the IV curve in solar cells, there is a range of voltages where the MPPT can operate. Going above a certain operating point in voltage and the solar cells will not provide enough current to power the board. Going too low on the IV curve and the solar cells are shorted and damaged permanently. For this reason, the **vSetpoint** is checked to see if its within the **MPPTMAX** and **MPPTMIN** preset values. The **vSetpoint** is initialized at point A, as seen in Figure 4-8. Next, the algorithm lowers the **vSetpoint** by a δV to point B. In this case, the power in point B is higher than in Point A so it continues to decrease the **vSetpoint**. The voltage keeps decreasing until point G is reached, where the previous power, point F, is higher. At point G, the **vSetpoint** is now increased

and is set to point F. In the next time step the **vSetpoint** is increased once again to point E. The algorithm keeps oscillating between points E, F, and G from there on.

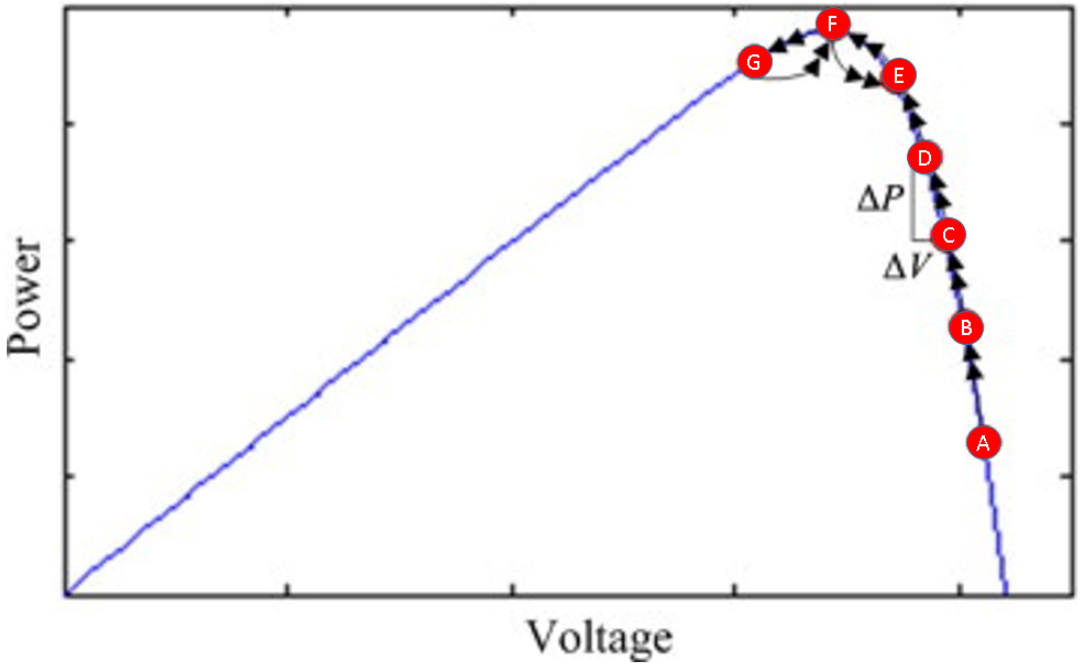


Figure 4-8: Maximum Power Point Tracking with Perturb and Observe Algorithm in Power Curve

The Perturb and Observe (P&O) algorithm is a commonly used algorithm that does not need many sensors or processing speed to work. One down side of the algorithm is that it cannot hold a static value. It must continuously perturb the operating power point. The oscillation leaves some room for losses in the system. If this MPP moves as the solar irradiance changes, it will be able to keep following it properly.

4.2.2 Heater Control Software

Another main subsystem in PCBSat is temperature control. This temperature system is simpler than the future control system where embedded heaters are used for optimal sectional heating. The heaters are controlled by Bipolar Junction Transistors (BJT). In heater operation, the BJT closes the circuit and supplies current and dissipates heat. The control loop, seen in Figure 4-9, for the heaters is completed by first

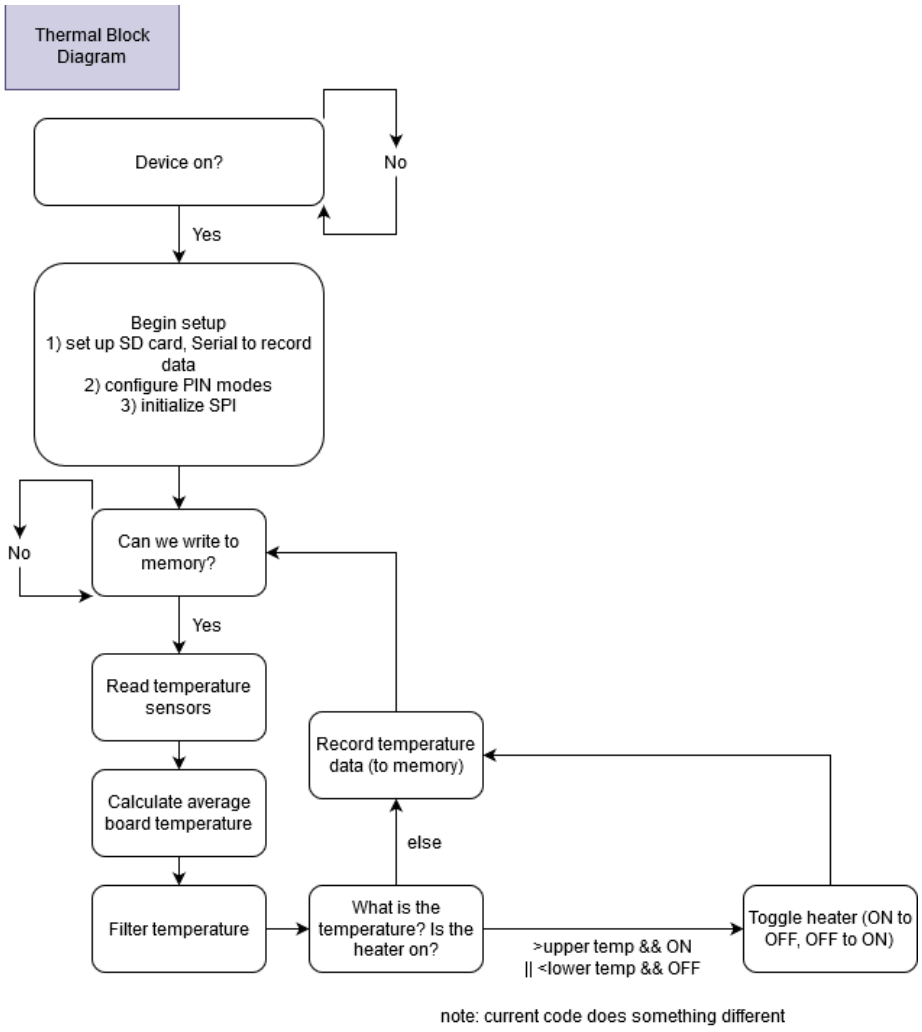


Figure 4-9: Thermal Subsystem Software Block Diagram

initializing the setup, then setting up a local memory to store the temperatures that are read one by one, an average temperature is calculated, and the heaters are turned on or off accordingly. The heaters are turned on with a Pulse Width Modulation (PWM) scheme to vary their power intake. The PWM will allow the heaters to be turned on and off at a duty cycle that will correspond to a safe range of temperature. This closed loop control might implement a PI or PID controller but that is yet to be determined.

4.3 Results and Testing

4.3.1 Test Preparation

Prior to testing, there are a couple of tasks that need to be completed: creation of a safe-to-mate procedure, initial board bring up procedure, and a functional testing document. The safe-to-mate procedure is key to prevent any damages from happening when connecting to a power supply or other components. This test is focused on measuring the resistances of every port or header in the PCB. The measured resistances are then compared to the expected values based on the design and a decision is made whether this port was properly manufactured. If an issue is discovered, it can be further revised prior to connection. Furthermore, the bring up procedure includes all of the functionalities that allow a test engineer to fully test the PCB. Some of these features are: required tools and software, schematics, and voltage reading procedure. The document should explain how to power on and program the PCB, with illustrations or references to the schematic and board layout for ease of the engineer. The software included should be basic enough to power on an LED or have some sort of feedback that the PCB is powered on and able to be programmed. Lastly, the functional testing document should include the safe-to-mate and expand on the full ranges of testing that need to be completed to evaluate the PCB. The tests included should dive deeper than the bring up procedure and explore the functionalities of every subsystem. The PCBSat tests plans can be found in Appendix A for the PCBSat project.

4.3.2 Testing

Testing a PCB consists of the following stages: safe-to-mate, board-bring-up, and software tests. These stages are developed in this section. The final design of PCBSat was tested and the power levels of the 5V, 3.3V, and the 1.8V rails were adequate and within 10% of the expected value, see Figure 4-10.

The first test conducted on PCBSat was the "Hello World" where the ATSAM V71

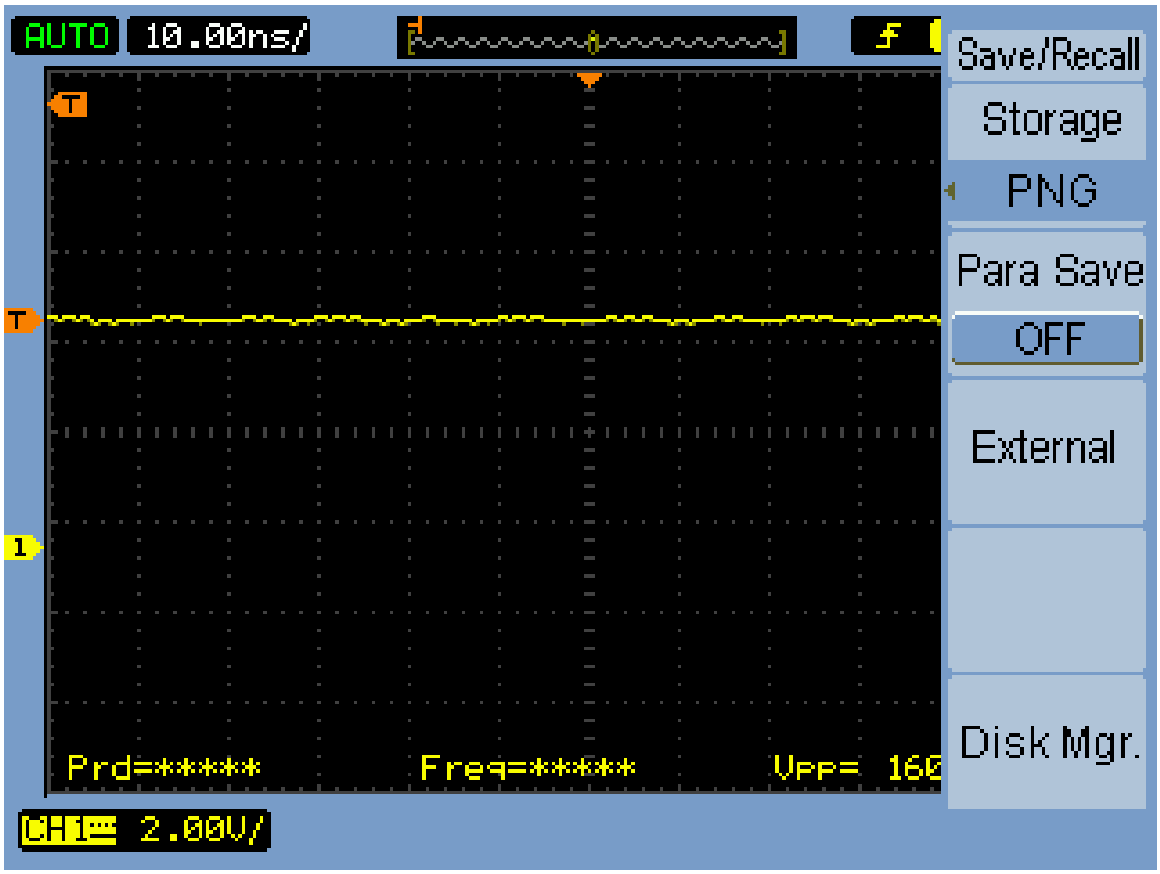


Figure 4-10: 5V Bus Output in PCBSat

is programmed with the Atmel ICE programmer. The "Hello World" program that flashes D223 every second and proves that Atmel board was programmed successfully. The LED can be seen light up in Figure 4-11.

The second test was concerned with the I^2C communication from the microcontroller towards the temperature sensors (Test included in the appendix). The ATSAM V71 had to send commands to the splitter to activate its second channel, and then communicate with the temperature sensors. The I^2C communication worked until after the splitter. The signal is illustrated in 4-12. The ATSAM V71 did not receive any feedback from the temperature sensors initially. After some further research, it was discovered that the data and clock line of the temp sensors had been connected incorrectly. This is an issue that can be solved with rework but has yet to be done.

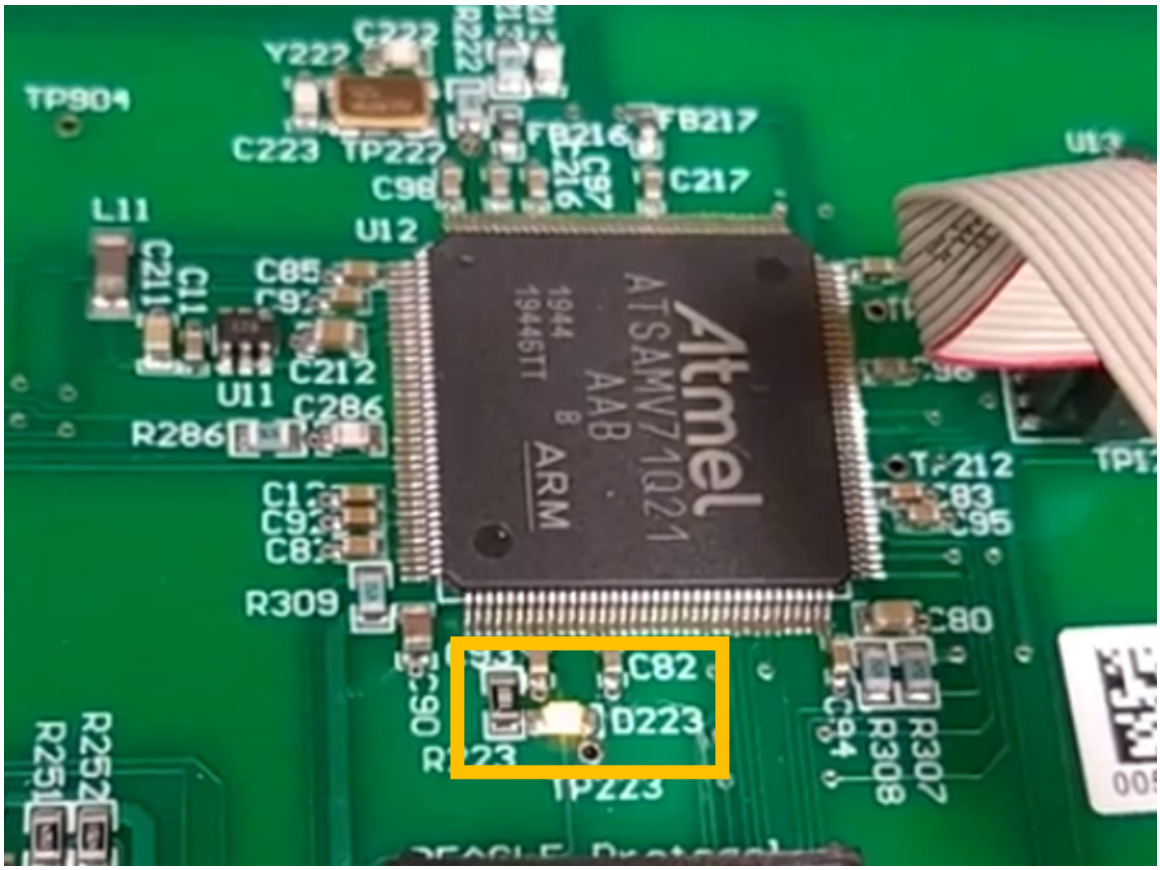


Figure 4-11: LED 223 Flashing for Hello World Program

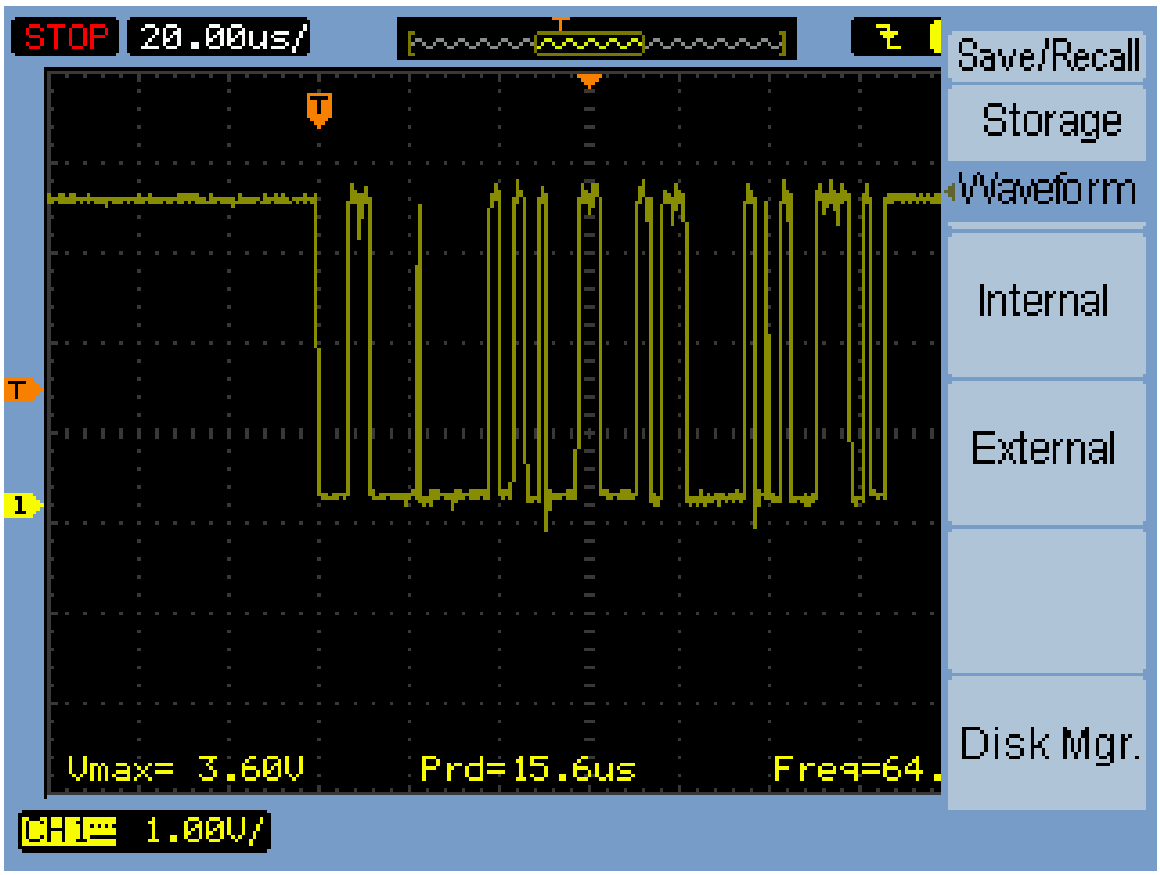


Figure 4-12: I^2C Communication in PCBSat Data Bus

Chapter 5

Conclusion

The design, development, and creation of PCBSat will move the WaferSat group much closer to answering the question of whether a power system can be designed to meet the demands of a science payload, active propulsion, and thermal control in LEO. There are hopes that PCBSat is enough to prove that a small satellite is capable of performing in extreme temperatures and low power. The results of these tests will lead to the development of a silicon wafer satellite. The many benefits of the silicon wafer can be fully explored and maximized for the future use of these satellites.

At the start of this project, the SWaP-Sat effort was just coming to a conclusion, and the PCBSat stage was about to start. The team included me and Michael Fifield as the grad student. Michael and I were able to recruit 19 undergraduate students over the year to help on the development of PCBSat. Leading these students was a challenging yet rewarding task.

5.1 Developing Power Systems for Small Satellites: Tips and Tricks

5.1.1 Ease of Debugging

It is important to design ways to debug the Power System when developing boards where there are multiple power levels or many different components that might depend

on each other. Having the ability to program the microcontroller without having a fully-programmed power subsystem is helpful, specially when trying to do a "Hello World" script to ensure that the microcontroller works. It is also key to make sure that the design includes reset switches, exposed test points, debugging connectors, replaceable chip ports, or even an embedded breadboard. Test points or exposed vias are essential in main power lines such as 5V and 3.3V. Being able to read essential voltages in the board is key for debugging. These components might make the final board design much larger and heavier than originally planned, but increases the ability to diagnose and solve issues that arise on PCBSat. On further iteration, some of these parts can be removed.

There are situations when a reset needs to be made in the components, specially in digital communication, where signals can be damaged or "hung up". For this reason it is important to add components that can power cycle certain IC's or communication buses. These resets can be completed with a physical button or automatically triggered by a software interrupt. It is also important to include a way to save the current state of the satellite prior to these software power cycles. It is recommended to add an on-board memory that can store the last state of operation.

5.1.2 Manufacturing and Testing

Since these satellites are trying to reduce surface area covered by electronics and weight, the electrical components chosen will be in form factors that are too small for a student team to solder. It is highly recommended to have a PCB fabrication company or an experienced technician populate the PCB components. When sending the board to be manufactured, make sure to have an accurate list of the components in the Bill of Materials. Lastly, plan for delays in the PCB manufacturing and populating. In our case, the PCBs were delayed over a month due to the COVID-19 pandemic.

It is important to also double-check all of these connections with a Safe-to-mate procedure, that should be created by the designer of the PCB schematics and layout. When designing the PCB, it is important to write a test plan, so that when the PCB arrives, the team can immediately begin to test it out. Furthermore, have a small

team develop test code, including a "Hello World" script that turn on LEDs on the board that proves that it is able to be programmed. It is also important to be able to include test points, specially in critical signal or power paths. It is not optimal to not be able to probe a signal when it is barely exposed.

5.1.3 Flexibility to Allow a Response to Unforeseen Circumstances

It is difficult to plan for unforeseen circumstances but these might appear when you least expect them. Due to the COVID-19 pandemic, the PCBs were delayed substantially and resulted in a minimized amount of test time in the MIT SSL. Due to the outbreak of COVID-19 in the US and the subsequent school shut downs, the testing of PCBSat in the SSL was cut short, allowing only two weeks of testing to be completed. Luckily, I was able to borrow an oscilloscope, power supply, and other small amounts of lab equipment to continue testing the PCB in an apartment in Cambridge. Even though situations like this may or may not recur, it is important to plan out for these delays or pauses. Being away from the lab allowed me to think more about how the ATSAM V71 was programmed and how it could be further enhanced with Atmel Studio 7 or MPLAB.

In the case of a quarantine or a stay at home order, it is recommended to develop a schedule where the team members can work remotely but can still work on the hardware testing. In our case, I was able to test out algorithms that were being developed from students located outside of the state.

5.2 PCBSat Readiness for Space

Currently, the plan is to have a fabricated PCB tested over a range of feasibility, survivability, and temperature tests. One of these tests consists of having the MPPT operate through a full cycle of sunlight at constant current demands. This test will prove if the system can sustain enough power through a dynamic range of solar fluxes.

Furthermore, the PCB will be bench tested to test its safe-to-mate characteristics. Once this is completed, there will be tests conducted for the MPPT peak power algorithm. Furthermore, this testing will allow the PCBSat to be characterized to the power curves that are desired in the preliminary design. Another advantage of having an integrated system will be that the subsystem coupling will be present, especially driven by the thermal system. There will be tests conducted that will monitor the peak heat generated when all of our circuitry is running. This peak power will allow the thermal system to learn how much heat it should supply at different states. The system might also be improved with more specific operational temperatures in a vacuum, thus narrowing down the component selection.

Appendix A

WAFERSAT Spring 2020
PCBSat Safe-To-Mate Procedure

Instructions:

- You will be needing to work with a partner to verify all of your measurements.
- You will need to print out this sheet in order to annotate the measurements you take and sign your name to every sheet.
- If you have questions while conducting the test either Xavier Zapien or Michael Fifield will be available to assist you:
    - Xavier Zapien: xzapien@mit.edu
    - Michael Fifield: mfifield@mit.edu

Materials:

The materials will be available in the lab in the Space Systems Laboratory (37-372). Before you begin the lab please confirm that all of these items are available.

PCBSat	_____
PCBSat Schematics	_____
Digital Multimeter	_____
ATMEL ICE	_____
Lab PC, Win 10, w/ SW	_____
20 V Power Supply ~ 1 A	_____

Step	Description	Initials

Procedure (3 pts)
In this test, you will be ensuring that the PCB was fabricated properly and all of its connections match those of the schematics as expected. This procedure will result in a detailed inspection of the board and all of its interfaces to other boards and power converters. In order to conduct this test, you will need to be familiar with a multimeter and be able to read electrical schematics; if you are not familiar with these, then ask for help.

Part 1 Setup: In this section you will get the equipment set up to complete the lab.

Step	Description	Initials
1.1	**<u>Procedure Start</u>**: Record the following information: Date/Time procedure started: _____ Location (Facility): _____ Student #1(name): _____ Student #2 (name): _____	
1.2	Verify that PCBSat is not missing any components and or ports.	
1.3	Make sure to be familiar with the multimeter and have it on the resistance measurement. As shown in the image below. Ensure that the black lead is connected to **COM** and the red lead is connected to **V.** Verify that the HOLD setting is not on in the Fluke multimeter. If hold is on, it will keep the maximum value recorded at all times, and give erroneous results to this test. This is an example reading of an open connection:  	

Step	Description	Initials
	This is an example reading of a closed (shorted) connection:  	

Part 2 Inspection: In this section you visually inspect PCBSat to ensure that there have been no damages to the board since the last test and that there are no visible shorts or opens.

Step	Description	Initials
2.1	Install the jumpers in the following location **Location** / **Pins** / **Note** TP-8 / 1-2 / GPS power: 5V S6 / N/A / Set switch to J6 Source	
2.2	Visually inspect the board with a microscope if available	
2.3	Using the Digital Multimeter in resistance measurement, check these values referenced to ground (J6-2 or J6-3) Signal / Location / Expected Range / Value / Notes BATT4 / P4-1 / 1 MΩ / / SLRCELLPWR / P5-1 / 1 MΩ / /	

Step	Description	Initials

NetC149-1	L150-1	3 MΩ		Charger Inductor
BATTPWR	S6-1	1 MΩ		
NetC6-1	S6-3	450 kΩ		5V Reg Input
V5_0D	TP6	1 MΩ		
V3_3D	TP199	50 kΩ		
V3_3SW	Q8-1	16.9kΩ		
V1_8D	TP7	60 kΩ		
ARMCORE	C12-1	4 kΩ		
ADCREF	C212-1	13.7 kΩ		
USBREGIN	U41-1	1 MΩ		
V3_3USB	C302-1	1 MΩ		
V1_8USB	C315-1	50 kΩ		

Step	Description	Initials

Part 3 Power On Inspection: Now you will be powering on the board and will be measuring the voltages are described in the steps below

<table>
<tr><th>Step</th><th>Description</th><th>Initials</th></tr>
<tr><td>3.1</td><td>Set power supply to 14 V (+/- .5V), current limit at 50mA.
With power turned off, plug in power cable into J6 on PCBSat</td><td></td></tr>
<tr><td>3.2</td><td>Power on power supply and take the following measurements
<table>
<tr><th>Signal</th><th>Location</th><th>Expected</th><th>Measured</th><th>Notes</th></tr>
<tr><td>V5_0D</td><td>TP6</td><td>5 V</td><td></td><td></td></tr>
<tr><td>V3_3D</td><td>TP199</td><td>3.3 V</td><td></td><td></td></tr>
<tr><td>V3_3DSW</td><td>Q8-1</td><td>3.3 V</td><td></td><td></td></tr>
<tr><td>V1_8D</td><td>TP7</td><td>1.8 V</td><td></td><td></td></tr>
<tr><td>ARMCORE</td><td>C12-1</td><td>1.234 V</td><td></td><td></td></tr>
<tr><td>ADCREF</td><td>C212-1</td><td>2.04 V</td><td></td><td></td></tr>
</table></td><td></td></tr>
<tr><td>3.3</td><td>If the voltages match the expected and the board LED D219 turned on. The board is set to be programmed.</td><td></td></tr>
</table>

WAFERSAT Spring 2020
PCBSat Test 1 ADC

Instructions:

- You will be needing to work with a partner to verify all of your measurements.
- You will need to print out this sheet in order to annotate the measurements you take and sign your name to every sheet.
- If you have questions while conducting the test either Xavier Zapien or Michael Fifield will be available to assist you:
    - Xavier Zapien: xzapien@mit.edu
    - Michael Fifield: mfifield@mit.edu

Materials:

The materials will be available in the lab in the Space Systems Laboratory (37-372). Before you begin the lab please confirm that all of these items are available.

Atmel SAM V 71 Xplained Pro Board	_____
Breadboard with Potentiometer	_____
Digital Multimeter	_____
Alligator Clips (x2)	_____
Lab PC, Win 10, w/ SW	_____
Data Micro USB Cable	_____

Step	Description	Initials

Procedure (3 pts)
In this test, you will be programming the Atmel board to complete the read analog values.From the start, you will complete the Safe-to-mate procedure located in the drive under *Wafersat/Power/Integration and Testing/ PCBSat/Safe_To_Mates*

Part 1 Setup: In this section you will get the equipment set up to complete the lab.

Step	Description	Initials
1.1	**Procedure Start**: Record the following information: Date/Time procedure started: _____ Location (Facility): _____ Student #1(name): _____ Student #2 (name): _____	
1.2	Verify that PCBSat is not missing any components and or ports. Print and conduct the safe to mate in the following folder: *Wafersat/Power/Integration_and_Testing/Safe_To_Mates*	

Part 2 LED Code Review: We will be running the code for the evaluation board that reads an analog value and send it back to the PC.

Step	Description	Initials
2.1	Read through the LED code example and understand the locations and functions of the pins we are working with. Note: The original code was meant for the SAM Xplained pro header	
2.2	After connecting a potentiometer to the ADC inputs and running the program, The board was able to send values for the analog voltage being read from the potentiometer. The scaling factor needs to scale our output values to real external values is 1266.26. *Real voltage = Output / 1266.26*	

Name	**Location**	**Description**
IO1_LIGHT_SENSE	PD30	Light sensor value
IO1_LED_PWM	PC19	PWM output for LED
LED_1	PC9	

Step	Description	Initials

Part 3 Next Steps: This section will outline what steps are needed to further improve this relationship with the ADC

Step	Description	Initials
3.0	We need to inspect just how fast the ADC can sample Also, learn just how much error it can obtain from its readings based on voltage values	
3.1	Notes: 12 bit ADC SAM V71 has 24 channels ADCs are connected to an Analog Fron-End Controller (AFEC) Possible gains of 1,2,4 (Only for single end use) Offset is only available in Single-ended mode Field AOFF must be configured to 512 + n Limits of ADC are within the bounds of the VDD (0 - 3.3V)	

Part 4 BQ257 ADC Notes: This section will highlight some facts from the ADC in the BQ charger and how it is integrated with the rest of the PCBSat System

Step	Description	Initials
3.0	Notes from the datasheet	

I2C Address	Register Name	Type	Description
3B/3Ah	ADCOption()	R/W	ADC Option
27/26h	ADCVBUS/PSYS()	R	8-bit digital output of input voltage, 8-bit digital output of system power PSYS: Full range: 3.06 V, LSB: 12 mV VBUS: Full range: 3.2 V - 19.52 V, LSB 64 mV
29/28h	ADCIBAT()	R	8-bit digital output of battery charge current, 8-bit digital output of battery discharge current ICHG: Full range 8.128 A, LSB 64 mA IDCHG: Full range: 32.512 A, LSB: 256 mA
2B/2Ah	ADCIINCMPIN()	R	8-bit digital output of input current, 8-bit digital output of CMPIN voltage POR State - IIN: Full range: 12.75 A, LSB 50 mA

Step	Description	Initials

			CMPIN: Full range 3.06 V, LSB: 12 mV
2D/2Ch	ADCVSYSVBAT()	R	8-bit digital output of system voltage, 8-bit digital output of battery voltage VSYS: Full range: 2.88 V - 19.2 V, LSB: 64 mV VBAT: Full range : 2.88 V - 19.2 V, LSB 64 mV

NOTE: ADC not available in Low Power Mode

8.6.1.7 ADCOption Register (I2C address = 3B/3Ah) [reset = 2000h]

Figure 29. ADCOption Register (I2C address = 3B/3Ah) [reset = 2000h]

7	6	5	4-0
ADC_CONV	ADC_START	ADC_ FULLSCALE	Reserved
R/W	R/W	R/W	R/W

7	6	5	4	3	2	1	0
EN_ADC_ CMPIN	EN_ADC_ VBUS	EN_ADC_ PSYS	EN_ADC_ IIN	EN_ADC_ IDCHG	EN_ADC_ ICHG	EN_ADC_ VSYS	EN_ADC_ VBAT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The ADC registers are read in the following order: VBAT, VSYS, ICHG, IDCHG, IIN, PSYS, VBUS, CMPIN. ADC is disabled in low power mode. When enabling ADC, the device exit low power mode at battery only.

Table 17. ADCOption Register (I2C address = 3Bh) Field Descriptions

I2C 3Bh	FIELD	TYPE	RESET	DESCRIPTION
7	ADC_CONV	R/W	0b	Typical ADC conversion time is 10 ms. 0b: One-shot update. Do one set of conversion updates to registers REG0x27/26(), REG0x29/28(), REG0x2B/2A(), and REG0x2D/2C() after ADC_START = 1. 1b: Continuous update. Do a set of conversion updates to registers REG0x27/26(), REG0x29/28(), REG0x2B/2A(), and REG0x2D/2C() every 1 sec.
6	ADC_START	R/W	0b	0b: No ADC conversion 1b: Start ADC conversion. After the one-shot update is complete, this bit automatically resets to zero
5	ADC_ FULLSCALE	R/W	1b	ADC input voltage range. When input voltage is below 5 V, or battery is 1S, full scale 2.04 V is recommended. 0b: 2.04 V 1b: 3.06 V <default at POR>
4-0	Reserved	R/W	00000b	Reserved

Table 18. ADCOption Register (I2C address = 3Ah) Field Descriptions

I2C 3Ah	FIELD	TYPE	RESET	DESCRIPTION
7	EN_ADC_CMPIN	R/W	0b	0b: Disable <default at POR> 1b: Enable
6	EN_ADC_VBUS	R/W	0b	0b: Disable <default at POR> 1b: Enable
5	EN_ADC_PSYS	R/W	0b	0b: Disable <default at POR> 1b: Enable
4	EN_ADC_IIN	R/W	0b	0b: Disable <default at POR> 1b: Enable
3	EN_ADC_IDCHG	R/W	0b	0b: Disable <default at POR> 1b: Enable
2	EN_ADC_ICHG	R/W	0b	0b: Disable <default at POR> 1b: Enable
1	EN_ADC_VSYS	R/W	0b	0b: Disable <default at POR> 1b: Enable

Step	Description	Initials

Table 18. ADCOption Register (I2C address = 3Ah) Field Descriptions (continued)

I2C 3Ah	FIELD	TYPE	RESET	DESCRIPTION
0	EN_ADC_VBAT	R/W	0b	0b: Disable <default at POR> 1b: Enable

8.6.9 ADCVBUS/PSYS Register (I2C address = 27/26h)

- PSYS: Full range: 3.06 V, LSB: 12 mV
- VBUS: Full range: 3200 mV to 19520 mV, LSB: 64 mV

Figure 40. ADCVBUS/PSYS Register (I2C address = 27/26h)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 39. ADCVBUS/PSYS Register (I2C address = 27h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of Input Voltage

Table 40. ADCVBUS/PSYS Register (I2C address = 26h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of System Power

8.6.10 ADCIBAT Register (I2C address = 29/28h)

- ICHG: Full range: 8.128 A, LSB: 64 mA
- IDCHG: Full range: 32.512 A, LSB: 256 mA

Figure 41. ADCIBAT Register (I2C address = 29/28h)

7	6	5	4	3	2	1	0
Reserved	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
Reserved	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 41. ADCIBAT Register (I2C address = 29h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R		Not used. Value ignored.
6-0		R		7-bit Digital Output of Battery Charge Current

Table 42. ADCIBAT Register (I2C address = 28h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R		Not used. Value ignored.
6-0		R		7-bit Digital Output of Battery Discharge Current

8.6.11 ADCIINCMPIN Register (I2C address = 2B/2Ah)

- IIN: Full range: 12.75 A, LSB: 50 mA
- CMPIN: Full range: 3.06 V, LSB: 12 mV

Figure 42. ADCIINCMPIN Register (I2C address = 2B/2Ah)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 43. ADCIINCMPIN Register (I2C address = 2Bh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of Input Current

Table 44. ADCIINCMPIN Register (I2C address = 2Ah) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of CMPIN voltage

Step	Description	Initials
	8.6.12 ADCVSYSVBAT Register (I2C address = 2D/2Ch) • VSYS: Full range: 2.88 V to 19.2 V, LSB: 64 mV • VBAT: Full range: 2.88 V to 19.2 V, LSB: 64 mV **Figure 43. ADCVSYSVBAT Register (I2C address = 2D/2Ch) (reset =)** 7 6 5 4 3 2 1 0 R R R R R R R R 7 6 5 4 3 2 1 0 R R R R R R R R LEGEND: R/W = Read/Write; R = Read only; -n = value after reset **Table 45. ADCVSYSVBAT Register (I2C address = 2Dh) Field Descriptions** BIT | FIELD | TYPE | RESET | DESCRIPTION 7-0 | | R | | 8-bit Digital Output of System Voltage **Table 46. ADCVSYSVBAT Register (I2C address = 2Ch) Field Descriptions** BIT | FIELD | TYPE | RESET | DESCRIPTION 7-0 | | R | | 8-bit Digital Output of Battery Voltage	
3.1		

WAFERSAT Spring 2020
PCBSat Test 3 Digital Sensor

Instructions:

- You will be needing to work with a partner to verify all of your measurements.
- You will need to print out this sheet in order to annotate the measurements you take and sign your name to every sheet.
- If you have questions while conducting the test either Xavier Zapien or Michael Fifield will be available to assist you:
    - Xavier Zapien: xzapien@mit.edu
    - Michael Fifield: mfifield@mit.edu

Materials:

The materials will be available in the lab in the Space Systems Laboratory (37-372). Before you begin the lab please confirm that all of these items are available.

Atmel SAM V 71 Xplained Pro Board	_____
Breadboard with Potentiometer	_____
Digital Multimeter	_____
Alligator Clips (x2)	_____
Lab PC, Win 10, w/ SW	_____
Data Micro USB Cable	_____

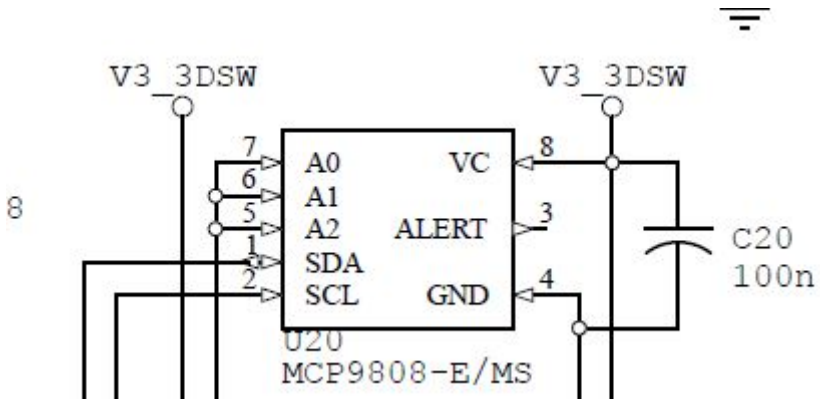
Step	Description	Initials

Procedure (3 pts)
In this test, you will be programming the Atmel board to complete the read analog values.From the start, you will complete the Safe-to-mate procedure located in the drive under *Wafersat/Power/Integration and Testing/ PCBSat/Safe_To_Mates*

Part 1 Setup: In this section you will get the equipment set up to complete the lab.

Step	Description	Initials
1.1	**Procedure Start**: Record the following information: Date/Time procedure started: _____ Location (Facility): _____ Student #1(name): _____ Student #2 (name): _____	
1.2	Verify that PCBSat is not missing any components and or ports. Print and conduct the safe to mate in the following folder: *Wafersat/Power/Integration_and_Testing/Safe_To_Mates*	

Part 2 Familiarize with the Digital Sensor Review: We will be running the code for the evaluation board that reads an analog value and sends it back to the PC.

Step	Description	Initials
2.1	The digital sensor of use is the MCP9808 From Schematic:  	

Temp Sensor ID	**Address**
U20	0x18
U21	0x19

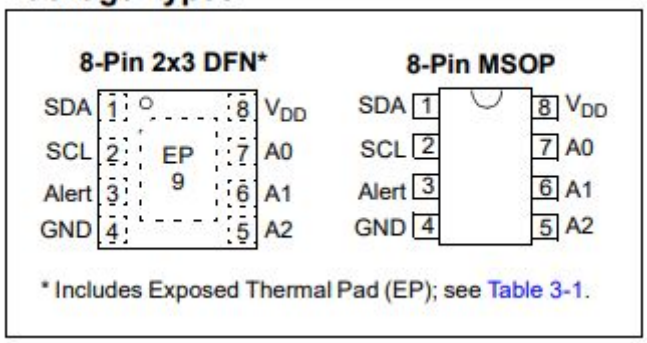
Step	Description	Initials

	U22	0x1A
	U23	0x1B
	U24	0x1C
	U25	0x1D
	U26	0x1E
	U27	0x1F
2.2	Details about the MCP9808 Datasheet	

Features

- Accuracy:
  - ±0.25 (typical) from -40°C to +125°C
  - ±0.5°C (maximum) from -20°C to 100°C
  - ±1°C (maximum) from -40°C to +125°C
- User-Selectable Measurement Resolution:
  - +0.5°C, +0.25°C, +0.125°C, +0.0625°C
- User-Programmable Temperature Limits:
  - Temperature Window Limit
  - Critical Temperature Limit
- User-Programmable Temperature Alert Output
- Operating Voltage Range: 2.7V to 5.5V
- Operating Current: 200 µA (typical)
- Shutdown Current: 0.1 µA (typical)
- 2-wire Interface: I²C™/SMBus Compatible
- Available Packages: 2x3 DFN-8, MSOP-8

Package Types



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Step	Description	Initials
	Absolute Maximum Ratings † V_{DD} ..... 6.0V Voltage at All Input/Output Pins ..... GND – 0.3V to 6.0V Storage Temperature .....-65°C to +150°C Ambient Temperature with Power Applied ....-40°C to +125°C Junction Temperature (T_J) ..... +150°C ESD Protection on All Pins (HBM:MM)..... (4 kV:400V) Latch-up Current at Each Pin (+25°C) ..... ±200 mA **TABLE 3-1: PIN FUNCTION TABLE**	

DFN	MSOP	Symbol	Pin Function
1	1	SDA	Serial Data Line
2	2	SCL	Serial Clock Line
3	3	Alert	Temperature Alert Output
4	4	GND	Ground
5	5	A2	Slave Address
6	6	A1	Slave Address
7	7	A0	Slave Address
8	8	V_{DD}	Power Pin
9	—	EP	Exposed Thermal Pad (EP); must be connected to GND

2.3	Note on Writing to registers in C Use pointers.	

Step	Description	Initials
		
2.4	Code for the temp sensing Note: This was completed using the Xplained pro evaluation board	

Step	Description	Initials

```c
#include <atmel_start.h>
/** This code is going to be modified to the following:
    Allow the eval board to read temp values from a MCP9808 temperature sensor */

/** Slave address */
#define MCP9808_SLAVE_ADDRESS 0x18
#define MCP9808_TEMP_REG_ADDRESS 0x05
#define ZEROS_ThirtyTwo 0x0000
#define BAUDRATE_FOUR_HUNDRED 0x190

int main(void)
{
    struct io_descriptor *I2C_0_io;
    uint16_t              read_data[2];

    /* Initializes MCdU, drivers and middleware */
    atmel_start_init();

    i2c_m_sync_get_io_descriptor(&I2C_0, &I2C_0_io);
    i2c_m_sync_set_baudrate(&I2C_0, ZEROS_ThirtyTwo , BAUDRATE_FOUR_HUNDRED);
    i2c_m_sync_enable(&I2C_0);
    i2c_m_sync_set_slaveaddr(&I2C_0, MCP9808_SLAVE_ADDRESS, I2C_M_SEVEN);
    delay_ms(1);

    /* read device temp */
    i2c_m_sync_cmd_read(&I2C_0, (uint8_t)MCP9808_TEMP_REG_ADDRESS, &read_data, 2);
    delay_ms(1);


    /* Replace with your application code */
    while (1) {
        gpio_set_pin_level(LED0, false);
        delay_ms(1000);
        gpio_set_pin_level(LED0, true);
        delay_ms(1000);
        i2c_m_sync_cmd_read(&I2C_0, (uint8_t) MCP9808_TEMP_REG_ADDRESS, &read_data, 2);
        delay_ms(1000);
    }
}
```

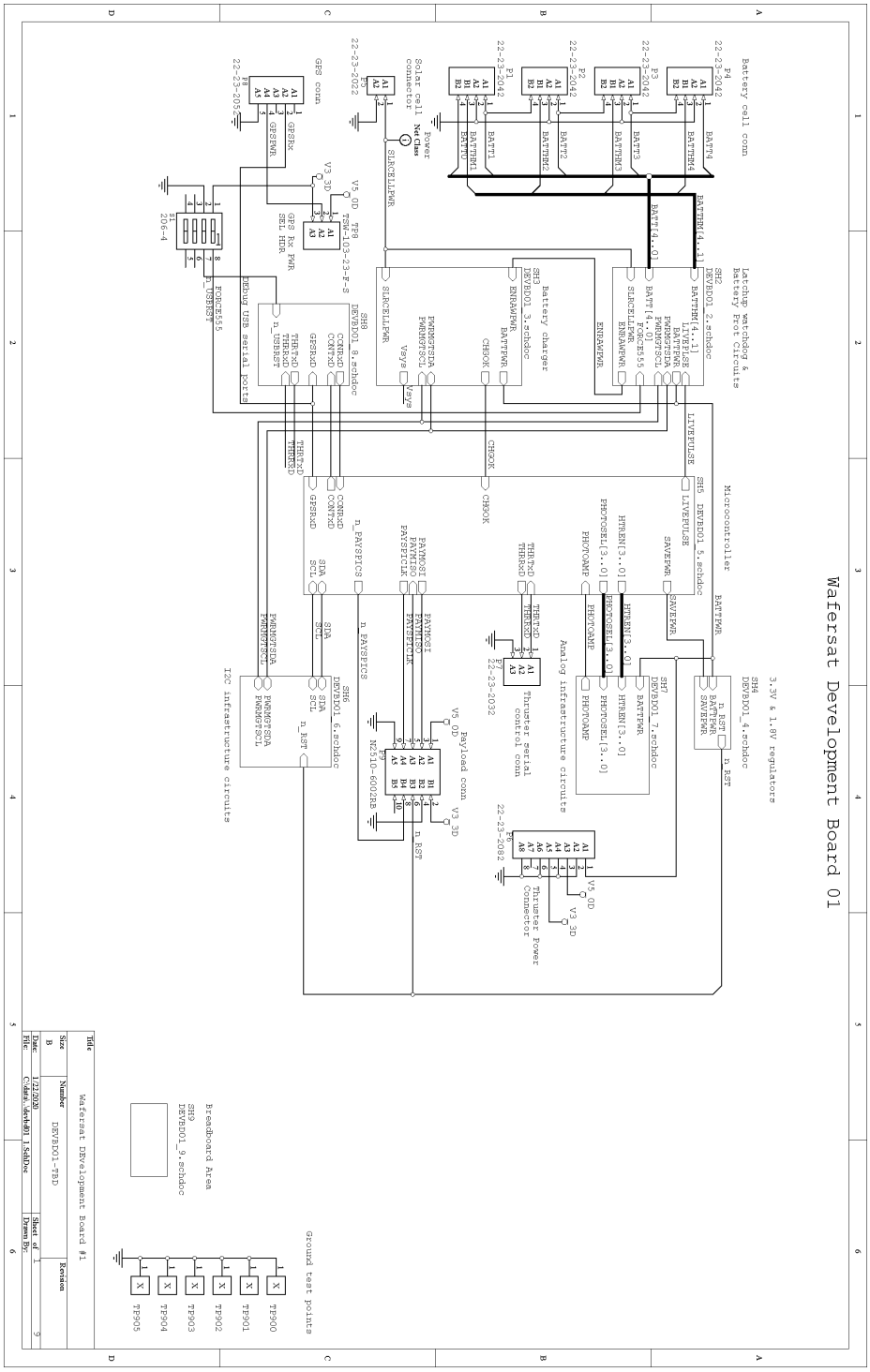


Figure A-1: devbd01 Page 1

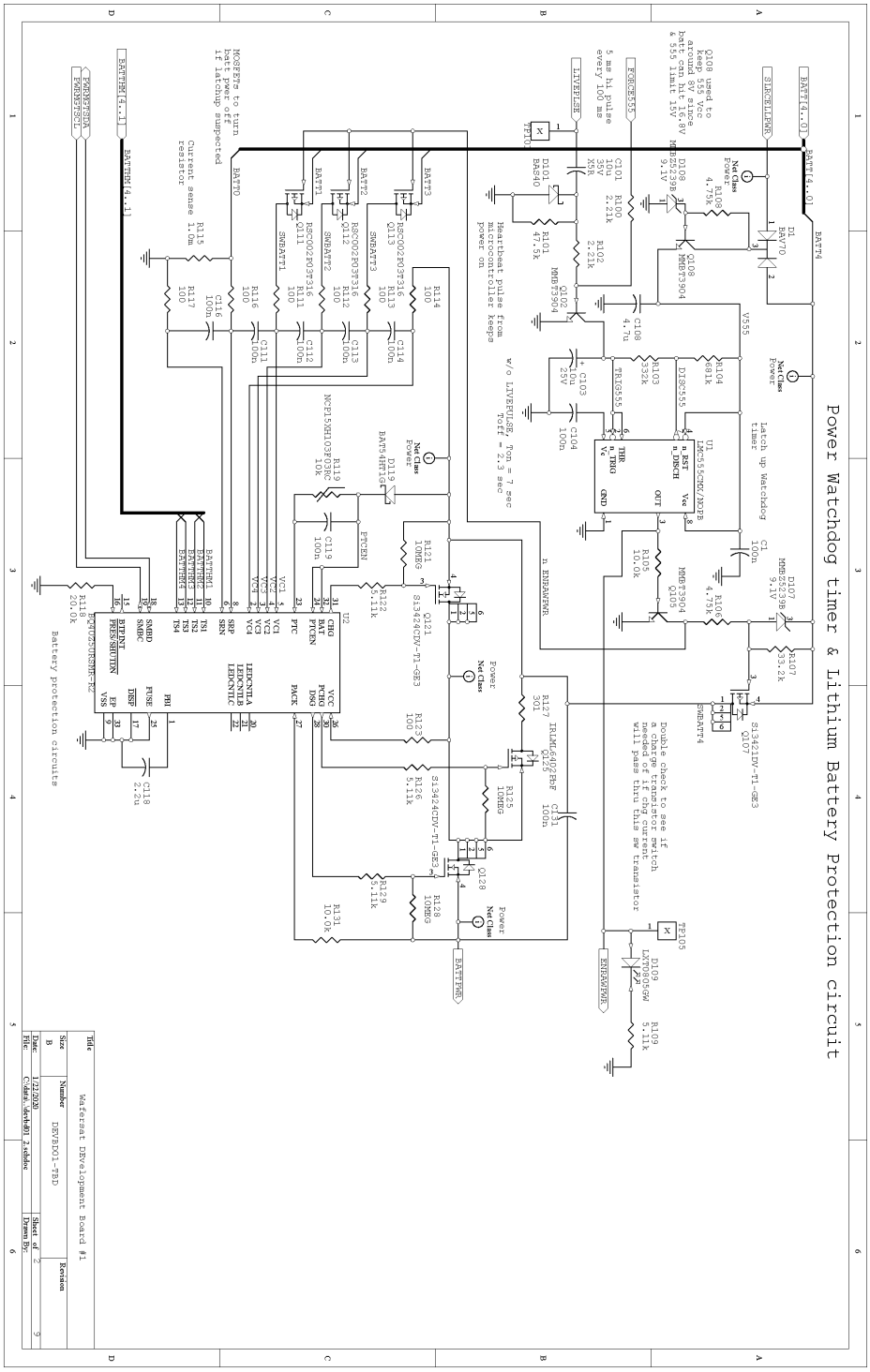


Figure A-2: devbd01 Page 2

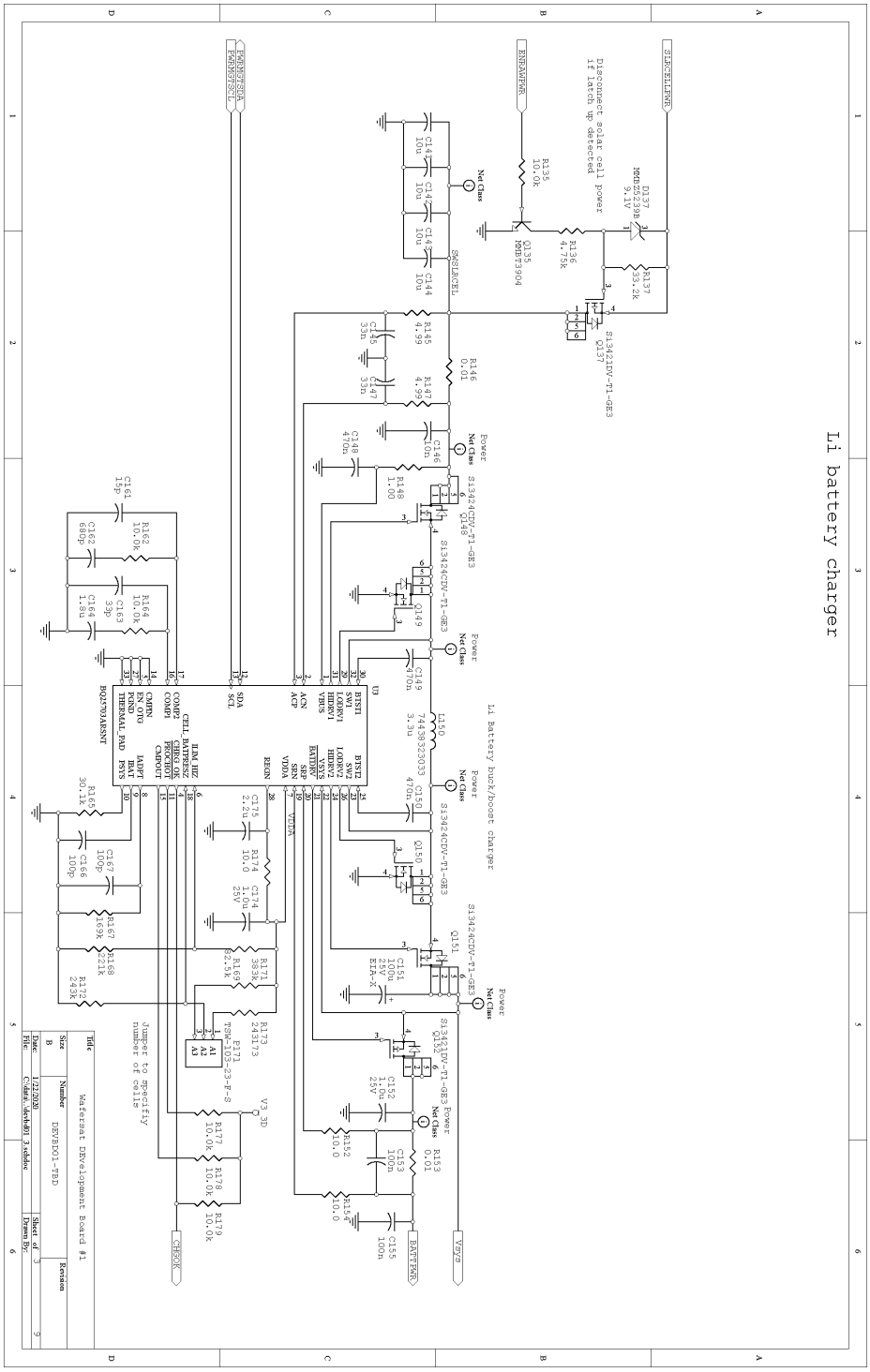


Figure A-3: devbd01 Page 3

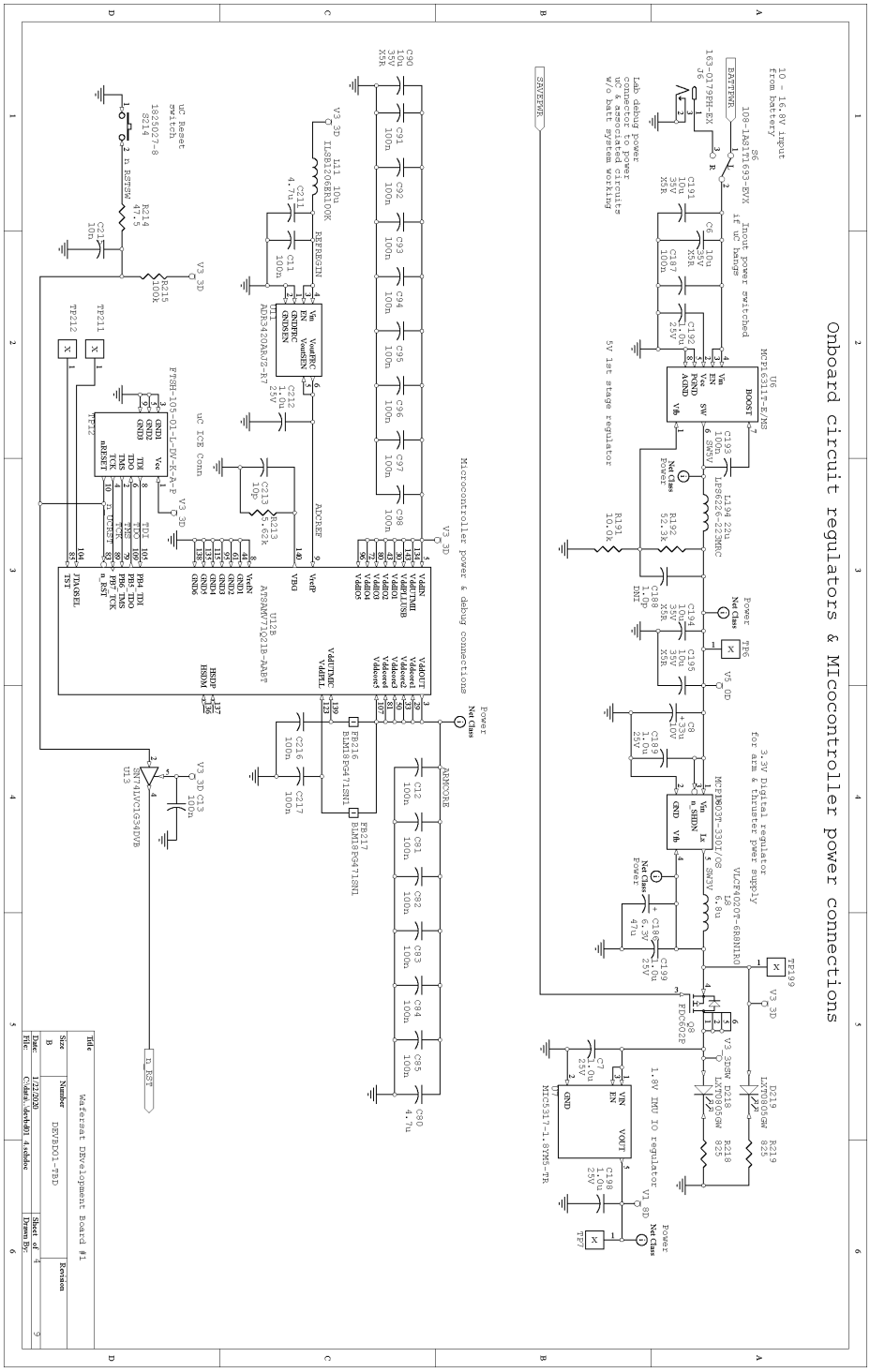


Figure A-4: devbd01 Page 4

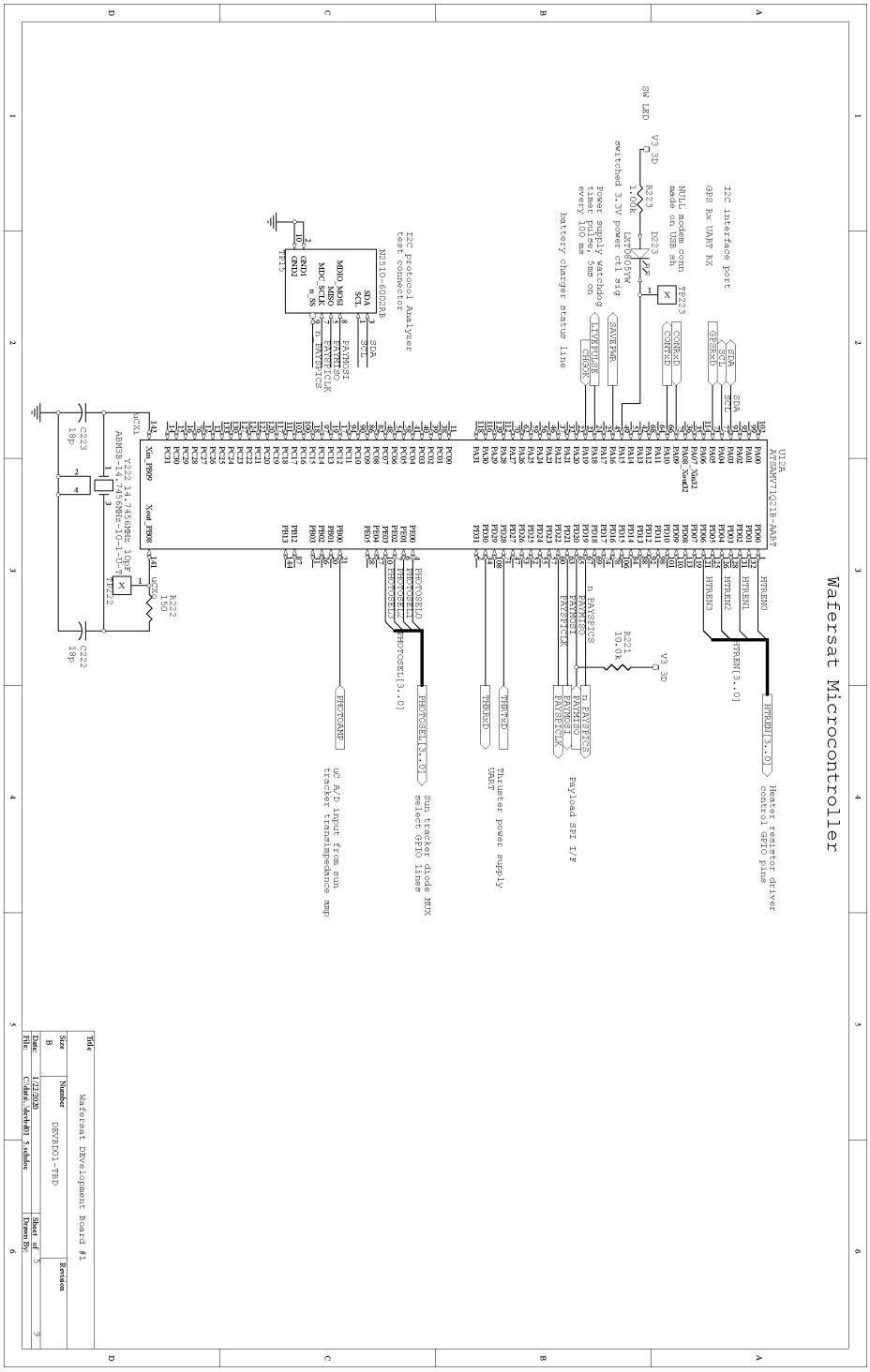


Figure A-5: devbd01 Page 5

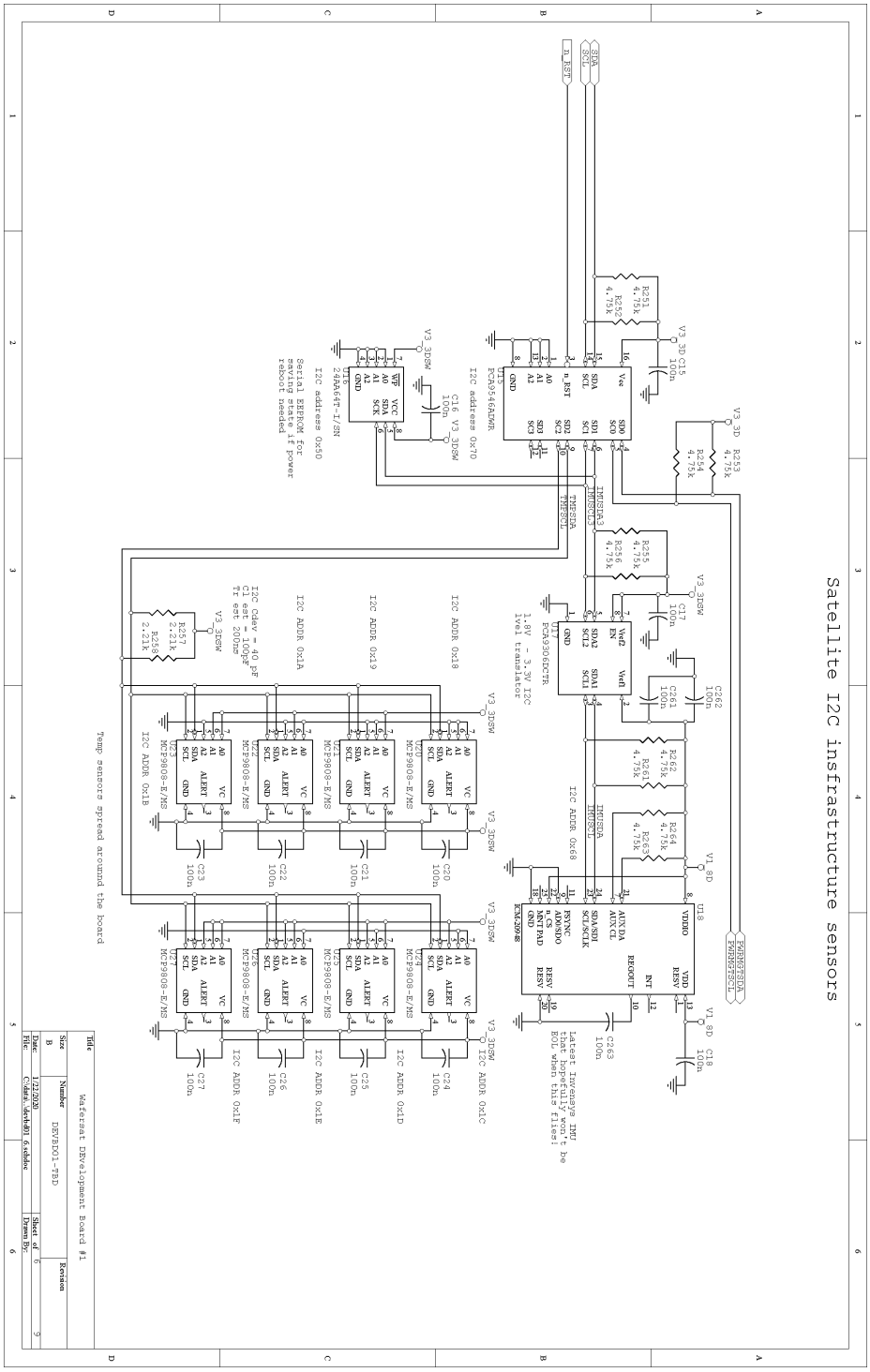


Figure A-6: devbd01 Page 6

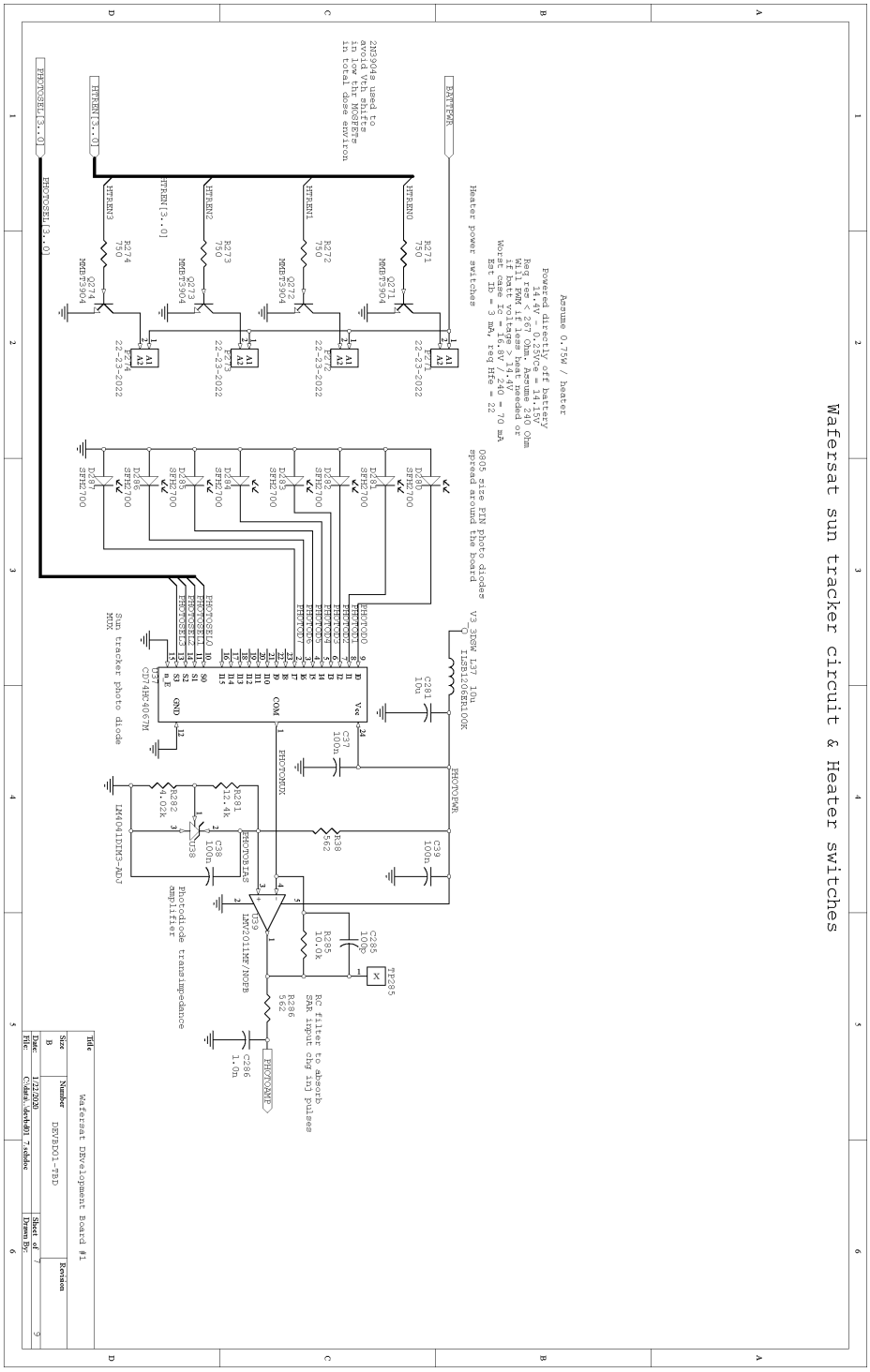


Figure A-7: devbd01 Page 7

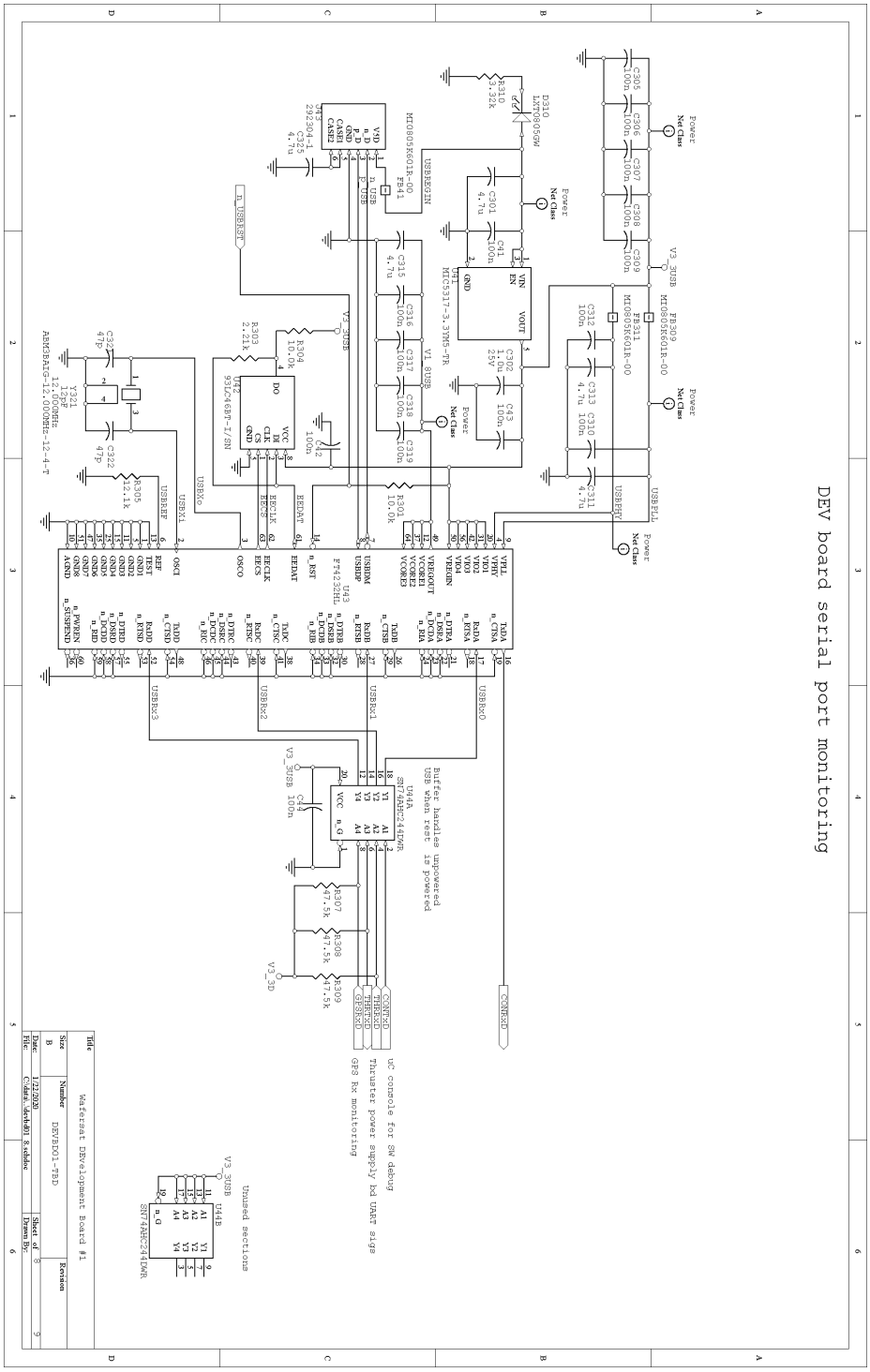


Figure A-8: devbd01 Page 8

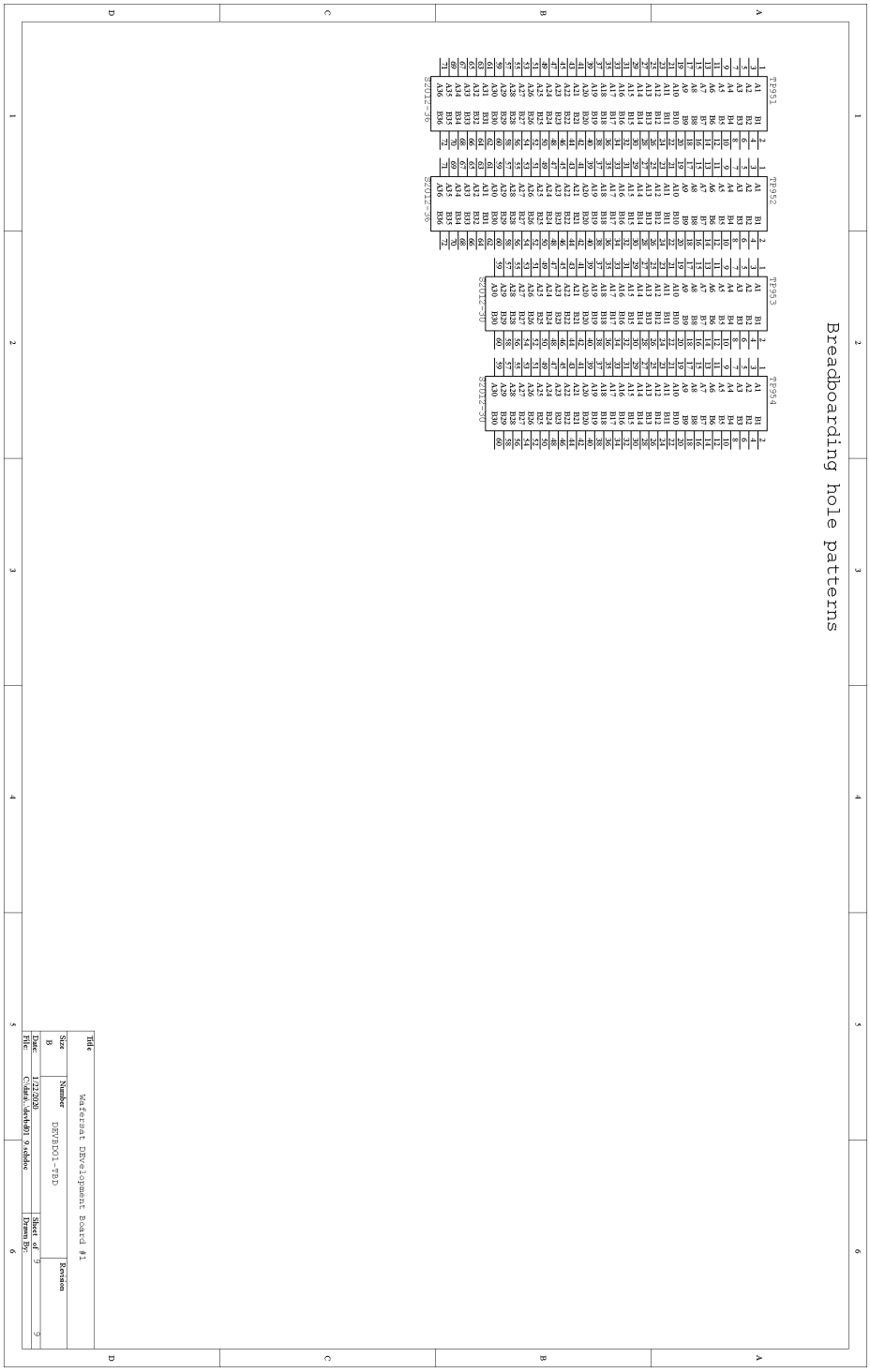


Figure A-9: devbd01 Page 9

Bibliography

[1] Kristen Redd Wilkinson, Rex Megill, Frank Redd, Rudy Panholzer, Eric Hoffman, Amnon Ginati, Bob Meurer, and Ron Woll. SSC06-I-1 From the Perspective of the Pioneers : The Small Sat Revolution. (435).

[2] Mukund R Patel. SPACECRAFT POWER SYSTEMS. Technical report.

[3] Mehdi Seyedmahmoudian, Ben Horan, Rasoul Rahmani, Aman Maung Than Oo, and Alex Stojcevski. Efficient photovoltaic system maximum power point tracking using a new technique. *Energies*, 9(3):1–18, 2016.

[4] Craig S. Clark and Alejandro Lopez Mazarias. Power system challenges for small satellite missions. *European Space Agency, (Special Publication) ESA SP*, 625 SP, 2006.

[5] Brigitte Hauke. Basic Calculation of a Buck Converter's Power Stage. Technical report, 2011.

[6] David Sternberg, John Essmiller, Cody Colley, Andrew Klesh, and Joel Krajewski. Attitude Control System for the Mars Cube One Spacecraft. *IEEE Aerospace Conference Proceedings*, 2019-March:2–11, 2019.

[7] I. C. Bell, B. E. Gilchrist, S. G. Bilen, and J. K. McTernan. The potential of miniature electrodynamic tethers to enhance capabilities of femtosatellites. pages 41–2, 2013.

[8] David J. Barnhart, Tanya Vladimirova, and Adam Baker. A Low-Cost Femtosatellite To Enable Distributed Space Missions. 298(0704), 2006.

[9] Zachary Manchester, Mason Peck, and Andrew Filo. KickSat : A Crowd-Funded Mission To Demonstrate The World's Smallest Spacecraft. *Annual AIAA/USU Conference on Small Satellites*, (August 2013):SSC13–IX–5, 2013.

[10] Igor Levchenko, Kateryna Bazaka, Yongjie Ding, Yevgeny Raitses, Stéphane Mazouffre, Torsten Henning, Peter J. Klar, Shunjiro Shinohara, Jochen Schein, Laurent Garrigues, Minkwan Kim, Dan Lev, Francesco Taccogna, Rod W. Boswell, Christine Charles, Hiroyuki Koizumi, Yan Shen, Carsten Scharlemann, Michael Keidar, and Shuyan Xu. Space micropropulsion systems for Cubesats and small satellites: From proximate targets to furthermost frontiers, 3 2018.

[11] John Steven Snyder, Dan M. Goebel, Richard R. Hofer, James E. Polk, Neil C. Wallace, and Huw Simpson. Performance evaluation of the T6 ion engine. *Journal of Propulsion and Power*, 28(2):371–379, 2012.

[12] John R. Brophy, Charles E. Garner, and Steven Mikes. Dawn ion propulsion system: Initial checkout after launch. *Journal of Propulsion and Power*, 25(6):1189–1202, 2009.

[13] David Anderson, Hani Kamhawi, Mike Patterson, Eric Pencil, Luis Pinero David-JAnderson, and John Dankanich. STATUS OF PROPULSION TECHNOLOGY DEVELOPMENT UNDER THE NASA IN-SPACE PROPULSION TECHNOLOGY PROGRAM. Technical report.

[14] Yiou He. Design and implementation of a lightweight high-voltage power converter for electro-aerodynamic propulsion. *IEEE 18th Workshop on Control and Modeling for Power Electronics*, 2017.

[15] Andrey W. Golubkov, David Fuchs, Julian Wagner, Helmar Wiltsche, Christoph Stangl, Gisela Fauler, Gernot Voitic, Alexander Thaler, and Viktor Hacker. Thermal-runaway experiments on consumer Li-ion batteries with metal-oxide and olivin-type cathodes. *RSC Advances*, 4(7):3633–3642, 12 2014.

[16] Doody Dave Fisher, Diane. Basics of Space Flight Section II. Space Flight Projects.

[17] Michael G Fifield. Evaluation of Phase Change Material Thermal Control Architectures for a WaferSatellite using Integrated Design and Optimization Techniques by. 2019.

[18] Noah W Siegel. Silicon Wafer Integration of Ion Electrospray Thrusters by. (2018), 2020.

[19] Matthew Landano. Design , Verification / Validation and Operations Principles for Flight Systems (D-17868), Rev . 2. pages 1–56, 2006.

[20] Chris Pearson, Carl Thwaite, and Nick Russel. Small cell lithium-ion batteries: the responsive solution for space energy storage. *3rd Responsive Space Conference*, pages 3–2005, 2005.