A 12-Bit 500 MHz GaAs MESFET Digital-to-Analog Converter with p^+ Ohmic Contact Isolation

by

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Abstract

Digital GaAs MESFET processes have recently achieved both extremely high levels of integration (1.2 million transistors) and sub-100 psec gate delays. However, analog GaAs MESFET circuit performance in these processes has been limited because of the threshold non-uniformity, sidegating/backgating, and frequency-dependent output conductance effects characteristic of MESFET devices. Several GaAs MESFET process improvements have been put forth that mitigate these effects including low temperature MBE-grown insulating buffer layer and oxygen proton implant isolation. While these process techniques do improve device performance, none of these techniques are compatible with a high-density, high-volume, low-cost digital GaAs MESFET process.

In order to achieve this capability, p^+ ohmic bulk biasing with n^+ ohmic guard ring isolation process technology and source-to-bulk bootstrapped cascode circuit design techniques were developed. High-performance analog and mixed-mode circuits were then able to be produced in an existing high-performance digital GaAs MESFET process. The performance-limiting physics of the digital GaAs MESFETs employed in analog circuit topologies were examined, modeled, and confirmed through experiments. A set of process enhancements and circuit techniques were developed to support high-performance analog and mixed-mode GaAs MESFET designs. These techniques were modeled and experimentally confirmed. Finally, a 12-Bit GaAs MESFET digital-to-analog converter based on the developed techniques was designed, fabricated, and tested.

Thesis Supervisor: Jesús A. del Alamo

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This thesis is dedicated to Margaret who makes it all worthwhile

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Chapter 1

Introduction

1.1 Limitations of GaAs MESFET Devices for Analog and Mixed-Mode Circuits

The high-electron-mobility material properties of gallium arsenide (GaAs) based devices have enabled high-speed, low-power, and high-density digital circuits to be realized. Mobility of electrons in undoped GaAs is a factor of five higher than silicon (Si) -- 8000 cm^2/volt-sec compared to 1500 cm^2/volt-sec at room temperature. This high-electron-mobility property leads to a speed-power product for GaAs digital integrated circuits that are fabricated with metal-semiconductor-field-effect-transistor (MESFET) devices that are a factor of four higher than the most advanced silicon bipolar or metal-oxide-semiconductor-field-effect-transistor (MOSFET) process. However, the hole mobility of GaAs is slower than Si: 300 cm^2/volt-sec compared to 450 cm^2/volt-sec, which constrains high-speed circuit designs to use only n-channel FETs. Digital GaAs MESFET circuits are therefore built in an n-channel MOS (NMOS)-like circuit design methodology known as direct-coupled-FET-logic (DCFL). Using DCFL design methodologies, circuit designers have achieved VLSI circuit densities.

The high-speed, low-power, and high-density properties demonstrated by GaAs digital designs are process-technology prerequisites for high-speed analog and mixed-mode circuits, including analog-to-digital conversion and signal processing topologies. In addition to these properties, analog circuit designs require device isolation, threshold uniformity, flat transconductance and output conductance. Unfortunately, GaAs MESFET

devices suffer from local (100 x 100 μm) and global (across wafer) threshold non-uniformity, backgating/sidegating effects, and frequency-dependent output conductance. In order to realize high-performance-analog and mixed-mode GaAs MESFET circuits, process enhancements and circuit design methodologies that eliminate these problems must be developed.

1.2 GaAs MESFET Threshold Uniformity

A GaAs-MESFET structure with improved threshold uniformity was achieved by adding a beryllium (Be)-implanted p^- layer buried under the n-channel.[1] The n-channel/p^- layer junction formed in this structure provides a controllable interface of uniform thickness and, therefore, uniform threshold control, in contrast to the conventional n-channel/ intrinsic GaAs junction, which forms a fluctuating tail region that results in large threshold fluctuation. However, the increase in control and uniformity of the channel achieved with a buried p^- implant, through the increase in substrate conductivity, adversely increases both the backgate/sidegate and device crosstalk sensitivity.

1.3 GaAs MESFET Isolation

The use of a low-temperature-molecular-beam-epitaxy (MBE)-grown insulating buffer layer[2] is effective as an isolation technique, but current MBE costs are too high for volume production. An oxygen-proton-implant-isolation process is also effective at isolating devices, but it corrupts threshold uniformity.[3] After channel formation, any subsequent process step that damages the channel/substrate interface will adversely affect threshold uniformity. This, therefore, eliminates the use of an oxygen-proton-implant isolation process step. Finally, biasing a buried p^- implant layer to the lowest potential will reduce the cross talk between devices that are spaced far enough apart so that the resistance

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[1] Y. Umemoto et al., "GaAs MESFETs with a Buried p-Layer for Large Scale Integration," *IEEE GaAs IC Symposium Technical Digest*, 1982.

[2] F. W. Smith et al., "Sidegating Reduction for GaAs Integrated Circuits by Using a New buffer Layer," *IEDM*, 1988, p. 838.

[3] W. M. Paulson et al., "The Effects of Implanted Oxygen on the Backgating Characteristics of GaAs ICs," *IEEE GaAs IC Symposium Technical Digest*, 1987.

connecting the backgates is much greater than the resistance from device to device. However, for any reasonable p^- implant dopant concentration, diffusion depth, and wafer thickness, the required spacing between devices becomes incompatible with a tightly packed transistor layout design.

1.4 GaAs MESFET Frequency-Dependent Output Conductance

The small signal output conductance, g_o, of a GaAs MESFET depends on both frequency and temperature. Typically, an increase of 5 times in output conductance is found between 10 Hz and 100 kHz depending on temperature and other process parameters. This phenomenon has been attributed to the emission time constant of electrically active defects in the semi-insulating substrate near the channel/substrate interface.[4] The variable output conductance produces a step response behavior that contains two exponential terms: a fast exponential (order of τ=1e-11s) followed by a much slower exponential (order of τ=1e-6s), resulting in undesirably long settling-time characteristics similar to that of a lag-compensated linear network.[5]

1.5 Overview

Each of the above performance limitations of GaAs MESFET process technology for developing mixed-mode circuits was considered in detail leading to the synthesis of a GaAs-MESFET-analog and mixed-mode process technology that incorporates p^+ ohmic bulk biasing with n^+ ohmic guard ring isolation and a design methodology that incorporates source-to-bulk bootstrapped cascode topology, which combined reduces or eliminates each of these effects. GaAs MESFET device physics were analyzed to develop relationships between frequency-dependent output conductance, backgating, crosstalk isolation, device hysteresis, duty-cycle modulation and circuit performance. A large-signal and small-signal device model was developed that accurately represents frequency-dependent output

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[4] E. P. Finchem, "Reduction of the Backgating Effect in GaAs MESFETs by Charge Confinement at the Backgate Electrode," *IEEE GaAs IC Symposium Technical Digest*, 1988.

[5] P. Nuytkens laboratory experiments, 1985.

conductance, substrate backgating, and device crosstalk. HSPICE, with the incorporation of this large-signal and small-signal device model, was then used to model the performance of this mixed-mode process enhancement and design methodology. Test structures were designed and fabricated to verify both the GaAs-MESFET process enhancements and design methodology and the analytical, large-signal, and small-signal device model. Finally, a 12-bit digital-to-analog converter based on the process enhancements, design methodology, and device models was designed, fabricated, and tested.

Chapter 2

GaAs MESFET Device and Circuit Modeling

2.1 GaAs MESFET Device Physics

The GaAs MESFET was first demonstrated in 1967 by Hooper and Lehrer[1] after being proposed by Mead in 1966.[2] The operation of the MESFET can easily be understood by examining the underlying physics of the depletion-mode device with subsequent modification of the doping levels to attain an enhancement-mode device. Consider the gateless depletion-mode device in Figure 2.1. The conducting channel allows current to flow as the drain-source bias potential is increased. The I-V relationship is linear for low bias potential directly following the velocity-field characteristics, which become quadratic as the saturation condition is approached. The electric field is uniform along the conducting channel. If the gate electrode is now connected to the source electrode as in Figure 2.2, a depletion region is formed under the gate metal that nearly pinches the channel at the source side of the gate electrode. If a further reverse bias is applied, the channel resistance increases until the device turns completely off. For modern processes, the conducting channel has sub-micron nominal printed gate lengths, and the depletion region that forms under the Schottky contact efficiently controls the flow of current in the

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[1] W. Hooper et al., "An Epitaxial GaAs Field-Effect Transistor," *Proc. IEEE*, Vol. 55, 1967.

[2] C. Mead, "Schottky Barrier Gate Field-Effect Transistor," *Proc. IEEE*, Vol. 54, 1966.

thin channel layer. The device, therefore, behaves as a voltage-controlled switch that can be modulated at high rates. A complete description of MESFET physics is given by Sze.[3]

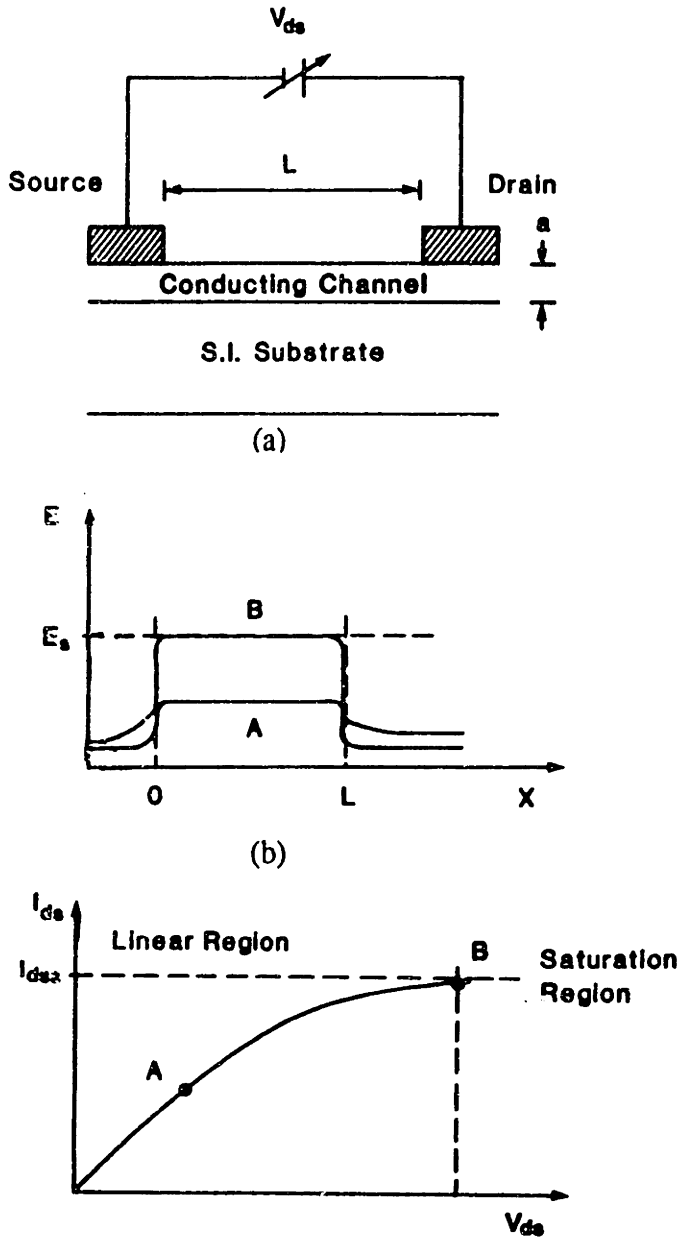

Figure 2.1 - (a) cross-sectional view of a gateless FET; (b) internal electric field for the structure biased in the linear and saturation regions; (c) the IV characteristic for the device.[4]

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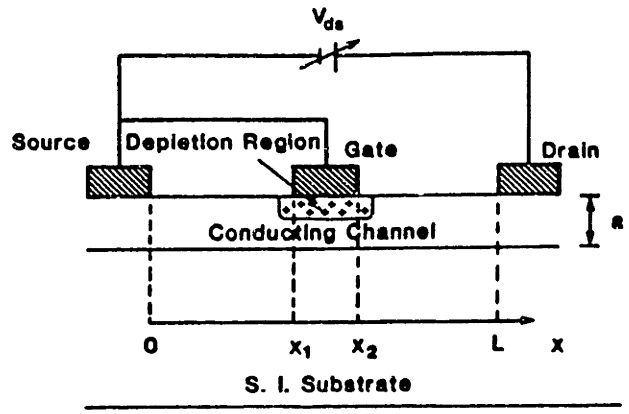
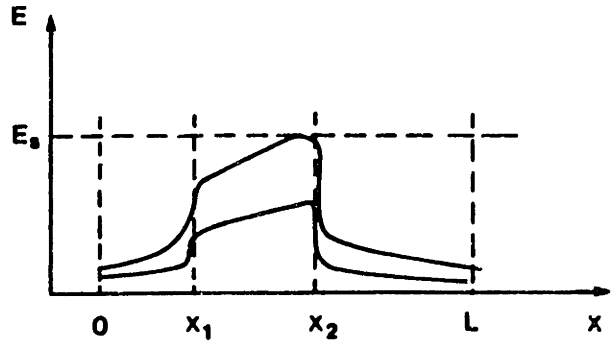
[3] S. Sze, *Physics of Semiconductor Device* , 2nd ed., Wiley & Sons, NY, 1981.

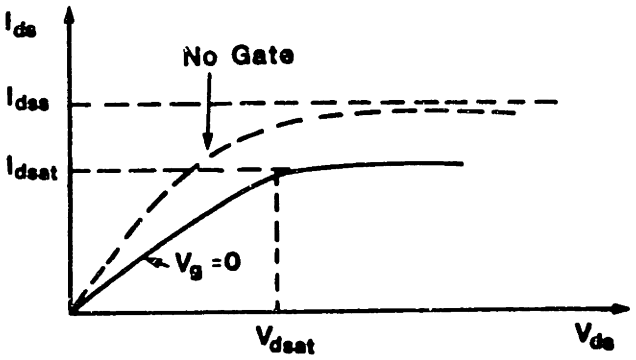
[4] I. Bahl et al., *Microwave Solid State Circuit Design*, John Wiley & Sons, NY, 1987.



(a)



(b)



(c)

Figure 2.2 - (a) cross-sectional view of biased FET; (b) internal electric field for the structure biased in the linear and saturation regions; (c) the IV characteristic for the device.[5]

For an ideal MESFET operating in the linear region, the drain current I_{DS} is given by Equation 2.1, and in the saturation region I_{DS} is given by Equation 2.3:

MESFET linear operation region: $V_{DS} < V_{DSAT}$, $V_{GS} > V_T$;

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[5] I. Bahl et al, *Microwave Solid State Circuit Design*, John Wiley & Sons, NY, 1987.

$$I_{DS} = (W/L)q\mu N_d t\{V_{DS} - 2/3 \cdot V_P^{-1/2} \cdot [(V_{DS} + V_{BI} - V_{GS})^{3/2} - (V_{BI} - V_{GS})^{3/2}]\} \quad 2.1$$

where L is the gate length, W is the gate width, t is the channel thickness, V_{BI} is the built in junction potential, V_{GS} is the gate to source voltage, V_{DS} is the drain to source voltage, V_T is the threshold voltage (V_{BI} - V_P). The pinch-off voltage, V_P, follows from Poisson's Equation and is given by:

$$V_P = qN_d t^2/2\varepsilon_s \quad 2.2$$

where q is the charge on an electron, N_D is the doping concentration, t is the channel thickness, ε_s is the permeability of GaAs.

MESFET saturation operation region: $V_{DS} > V_{DSAT} = V_{GS} - V_T$;

$$I_{DS} = (W/L)q\mu N_d t\{V_P/3 - (V_{BI} - V_{GS}) + 2/3 \cdot (V_{BI} - V_{GS})^{3/2} / V_P^{1/2}\} \quad 2.3$$

For circuit design, two useful MESFET expressions are the small-signal-equivalent transconductance, g_m, and output conductance, g_o. For the ideal MESFET expression of Equation 2.1, the partial derivative, $\partial I_{DS}/\partial V_{GS}$, leads to the saturation transconductance given by:

$$g_m = \partial I_{DS}/\partial V_{GS} = (W/L)q\mu N_d t\{1 - (V_{GS} + V_{BI})^{1/2}/V_P\} \quad 2.4$$

The saturation-output conductance, g_o, is proportional to the channel-length modulation, λ, and the bias current, I_{DS}, is given by:

$$g_o = \partial I_{DS}/\partial V_{DS} = 1/\lambda I_{DS} \quad 2.5$$

These approximations are only valid for computing the static (dc) behavior of a GaAs MESFET where it is assumed that the channel is controlled primarily by the depletion region under the gate electrode. In fact, even the dc operation is a strong function of the potential of the bulk electrode, which acts as a backside channel gate, hence the name backgate. Equations 2.1 and 2.3 can be modified to accurately model the dc-static-backgate effect through a simple linear threshold adjustment given by Equation 2.6, where V_{BS} is the bulk-to-source potential, and k is the backgate transconductance parameter: [6]

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[6] N. Scheinberg, "A Low Frequency GaAs MESFET Circuit Model," *IEEE Journal of Solid State Circuits*, Vol. 23, No. 2, April 1988.

$$V_T = V_{To} - kV_{BS} \quad (2.6)$$

where V_{To} is V_T at zero V_{BS}. However, for accurate modeling of transients and spurious response of circuits, it is necessary to develop a model that incorporates the physical dynamics of the bulk potential. Dynamic substrate modeling enhancements of the intrinsic HSPICE model are described in sections 2.3 and 2.4.

2.1.1 Enhancement/Depletion GaAs MESFET Process

The Vitesse enhancement/depletion mode MESFET foundry process selected for this research is tailored for the fabrication of high-performance GaAs VLSI digital circuits. To achieve these characteristics, high-performance, self-aligned MESFETs are used with multiple levels of interconnect. Two active devices exist in the process: an enhancement-mode MESFET and a depletion-mode MESFET. Schottky-barrier diodes are built from either depletion mode or enhancement mode MESFETs and can be used as references and level-shifting in current-mode-logic (CML) buffer topologies. Two passive devices exist in the process: an n^+ diffused resistor and a metal-insulator-metal capacitor. The nominal sheet resistance is 200 ohms per square. Implant resistors of this type have been constructed and show performance of relative matching of less than 0.5 percent.[7]

The choice of the mean value of the enhancement-mode threshold (V_{TE}) and depletion-mode threshold (V_{TD}) in the Vitesse process is optimized for the direct-coupled-FET-logic (DCFL) family. The thresholds are centered at values that give the lowest propagation delay and power. Nominal V_{TE} is 250 mV for an enhancement-mode device, and nominal V_{TD} is -800 mV for the depletion-mode device.[8] The amount of variation in the threshold voltage, σV_T, determines the relative size of the gate widths of the transistors and switching speed of the logic.

In addition to the n-channel MESFET devices, a p^+ ohmic contact process has been developed that allows localized biasing of the substrate. The ability to bias the substrate

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[7] P. Nuytkens, laboratory data, 1989.

[8] *Vitesse Foundry Design Manual*, Verison 4.0, 1991.

provides control of the backgate potential and, therefore, the threshold as well as transconductance of the device. Since GaAs is a semi-insulating material, two circuits located within distances of 100 μm from each other typically "talk" to each other through the substrate. By using the p^+ ohmic contact, a designer can isolate various circuit topologies from one another. Chapter 3 develops the p^+ ohmic process technology, while Chapter 4 shows test circuit performance of the process that demonstrates a reduction of gate crosstalk between two adjacent circuits by more than 30 dB. Finally, Chapter 5 describes performance of p^+ ohmic-ring-isolated current sources of the digital-to-analog converter design. Here, the p^+ ohmic-ring-biased current sources show increased isolation from substrate transients generated by the current switches and input receivers and also show improved relative matching.

In addition to improving isolation, use of the p^+ ohmic contact reduces device hysteresis. This phenomena is shown in Figure 2.3, which graphs the I_{DS} versus V_{DS} characteristics of a differential transistor pair (gate width of 10 μm and gate length of 1.2 μm) with both an applied bulk bias and without an applied bulk bias (floating). Even at very low sub-hertz measurement frequencies, hysteresis is present for devices in which the bulk floats. The data indicates that when a p^+ contact backgate is electrode biased, the slow charge build up of the substrate in the p^- buried layer, due to device-to-bulk leakage, is removed. This eliminates I_{DS} versus V_{DS} device hysteresis.

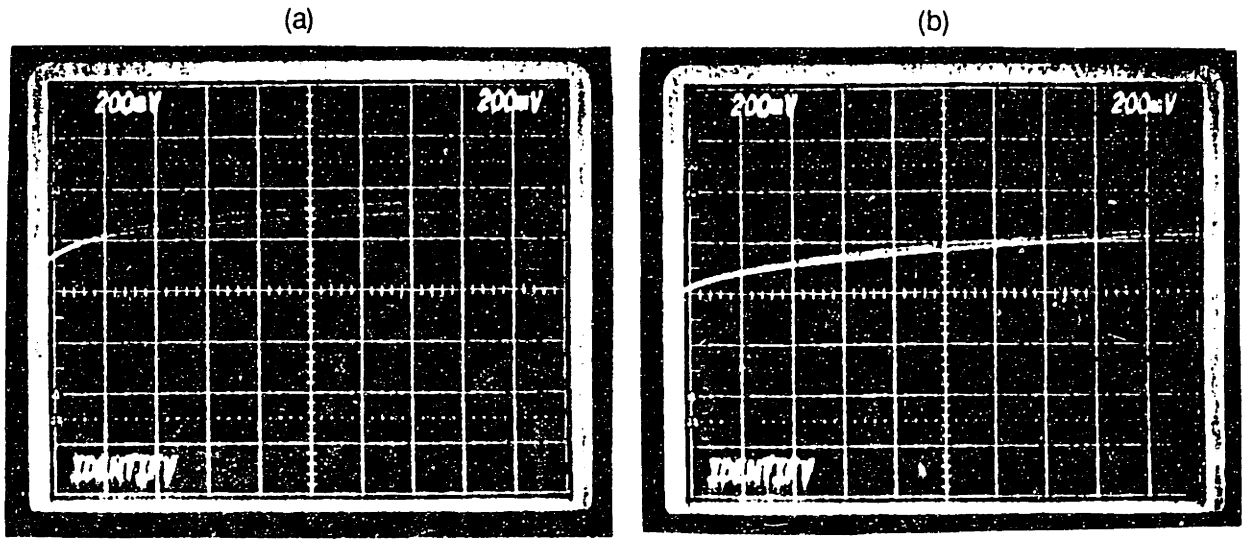

Figure 2.3 - MESFET IV hysteresis characteristics comparing (a) floating substrate to (b) p^+ ohmic contact biased substrate.

2.2 Large-Signal and Small-Signal Model

HSPICE[9] has developed a GaAs MESFET model for circuit simulations of the Vitesse enhancement-mode/depletion-mode digital MESFET process circuits that is a variation of the Statz model.[10] The improvement HSPICE has made over the published model is to design model inputs as process parameters. The primary advantage of this approach is the ability to implement statistical design procedures based on known parameter variations. The model is developed from process parameters and, therefore, attains high correlation with actual chip-test parameters. The corresponding equivalent circuit models used to describe the MESFET are shown in Figure 2.4. The controlled source determines the channel current as a function of V_T and the applied bias potentials. The resistances rs and rd represent the total series resistance between the channel and the specified external contact. As predicted by the device physics, the Schottky gate diode is divided into a gate-source and gate-drain component. Capacitors cgs and cgd are the voltage-dependent

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[9] Meta Software HSPICE User's Manual Version H9001 1990.

[10] H. Statz et al., "GaAs FET Device and Circuit Simulation in SPICE," *IEEE Transactions on Electron Devices*, Vol. ED-34, No. 2, February 1987.

capacitors associated with the Schottky barrier gate. Noise sources inrd and inrs model the equivalent current noise source of gate to drain and gate to source diodes. Noise source ind models the equivalent channel current themal noise component.

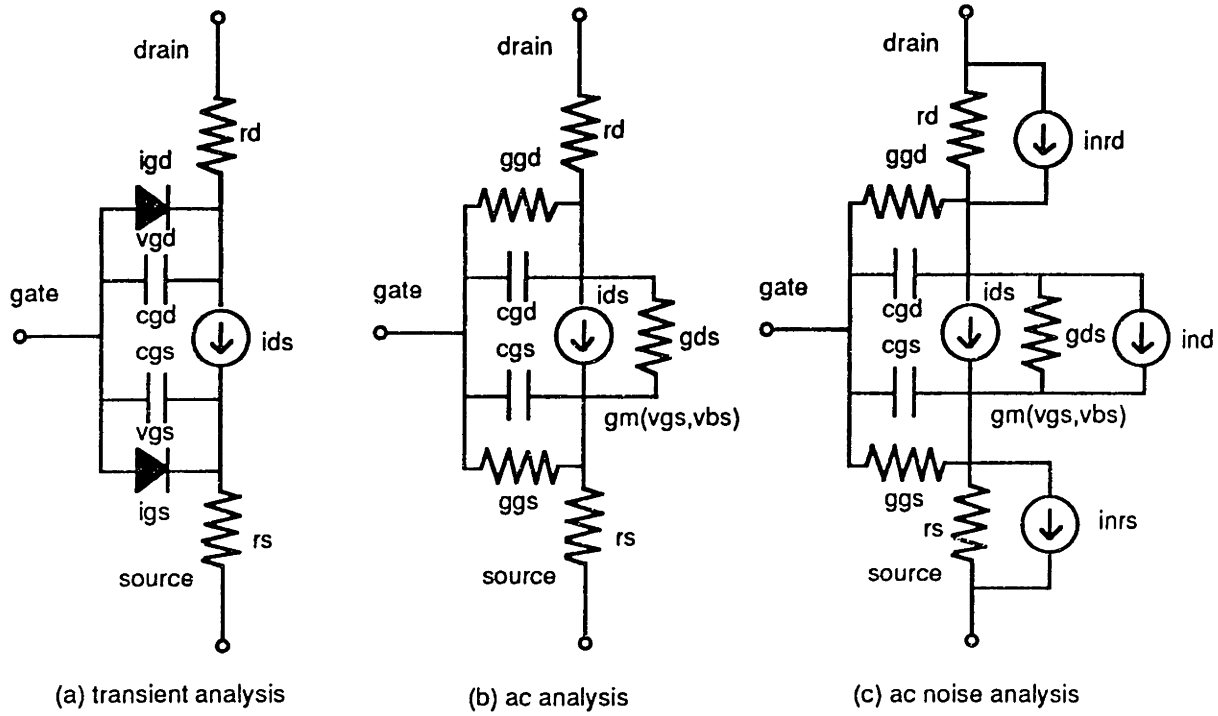

Figure 2.4 - HSPICE models for (a) Transient, (b) ac, and (c) ac noise analysis.

The HSPICE model is similar to that proposed by Statz, Newman, Smith, Busell, and House, but it contains several important differences. The I_{DS} equations and two orders of derivatives are continuous, and, hence, functions describing I_{DS}, gm, and V_{DS} are continuous over the bias range of interest. This tends to eliminate HSPICE convergence problems. The main differences between the HSPICE and the Statz model are the method of including velocity saturation and the use of V_T, which is function of the V_{BS}, V_{GS}, length, and width rather than a constant voltage. The advantage of using this form is that a good fit is attained between the model and measured data of the MESFET I_{DS} verses V_{DS} characteristics in the transition region from linear to saturated behavior. A comparison of the calculated and measured I_{DS} versus V_{DS} for various gate dimensions and threshold voltages is extremely good in this model.

The process enhancements and circuit design techniques, described in Chapter 3, that simultaneously improve threshold uniformity, reduce backgating, increase isolation, and reduce frequency-dependent output conductance of GaAs MESFET devices were all modeled using HSPICE.

2.2.1 Threshold Voltage Model

The threshold voltage of a MESFET is a function of bias conditions including backgating, device geometry, temperature, doping concentration and the built in voltage of the Schottky barrier gate. In HSPICE, the threshold voltage for MESFET is expressed:

$$V_{TO}=V_{BI} - V_P \qquad 2.7$$

where V_P and V_{BI} are the pinch-off voltage, and built-in potential as earlier defined.

However, in HSPICE, V_{TO} is a model input parameter and may be derived from experimental data. As such, V_P and V_{BI} are not required inputs. In order to calculate the DC I_{DS} - V_{DS} curves for a device as a function of V_{GS} and temperature, V_{TO} is modified according to:

$$V_{T0} = V_{T0} +(GAMDS \bullet V_{DS}) +(k \bullet V_{BS}))-(TCV \bullet \Delta T) \qquad 2.8$$

where GAMDS is a multiplication factor that accounts for bias dependence, $k(V_{BS})$ is the functional relationship for the backgating effect, and TCV is the temperature coefficient of the threshold voltage. The V_{DS} dependence is primarily due to the voltage variation with short-channel effects. The values of GAMDS and k are determined from experimental data using a least-squares-optimization curve fit. TCV was experimentally determined for discrete enhancement-mode and depletion-mode transistors of width 10 μm and length 1.0 μm as 0.95 mV - 1.1mV/°C over the commercial temperature range 0°C to +70°C.

2.2.2 Channel Current Model

The HSPICE MESFET model to be employed in the proposed research is similar to that developed by Statz, Newman, Smith, Busell and Haus,[11] but it contains several important differences. The expression used to describe the controlled current source, I_{DS}, is given by:

$$I_{DS} = \beta_{eff}(V_{GS}-V_{TO})VGEXP(1+\lambda V_{DS})[1-(1-ALPHA \cdot V_{DS}/3)^{SATEXP}] + I_{SUB} \qquad 2.9$$

where ALPHA determines the slope of the linear region of the I_{DS} versus V_{DS} curve and λ is the channel-length-modulation parameter described in Equation 2.6. The original Statz model sets VGEXP = 2 and SATEXP = 3. These factors were changed to VGEXP = 2.4 and SATEXP = 3.2 to give the best curve fit as determined by a least-squares-curve optimization. The choice of these values is critical when designing 12-bit precision circuits.

Velocity saturation occurs at high V_{GS} and V_{DS} biases where channel scattering reduces the electron mobility. This effect is accounted for in the expression for β_{eff} given by:

$$\beta_{eff} = (\beta \cdot W/L)/[1+VCRIT \cdot (V_{GS}-V_{TO})] \qquad 2.10$$

where VCRIT represents the critical field for the onset of mobility degradation. The factor $(V_{GS}-V_{TO})$ is used to reduce the approximately square law dependence at high V_{GS} potential. The combined effect of VGEXP and velocity saturation results in a slightly superlinear dependence of I_{DS} on V_{GS} and a compression of the transconductance. This shows that true velocity saturation is occurring over only a portion of the channel length. As the gate length decreases (for equal bias conditions) the composite power law behavior will tend toward unity.

Finally, subthreshold current is modeled in empirical form as given by:

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[11] H. Statz et al., "GaAs FET Device and Circuit Simulation in SPICE," *IEEE Transactions on Electron Devices*, Vol. ED-34, No. 2, February 1987.

$$I_{SUB} = I_o e^{ND \cdot V_{DS}} \cdot e^{-NG \cdot V_{GS}} \qquad 2.11$$

where Io is a constant that depends on geometry and ND and NG are empirically determined parameters.

For this HSPICE model there is excellent comparison of the calculated and measured I_{DS} versus V_{DS} for various gate dimensions and threshold voltages. Figure 2.5 compares HSPICE simulated and measured dc characteristics of I_{DS} versus V_{DS} for V_{GS} = 0.1 to 0.6 volts of a 10 μm-wide by 1.0 μm-long enhancement-mode MESFET with the bulk biased at the source voltage.

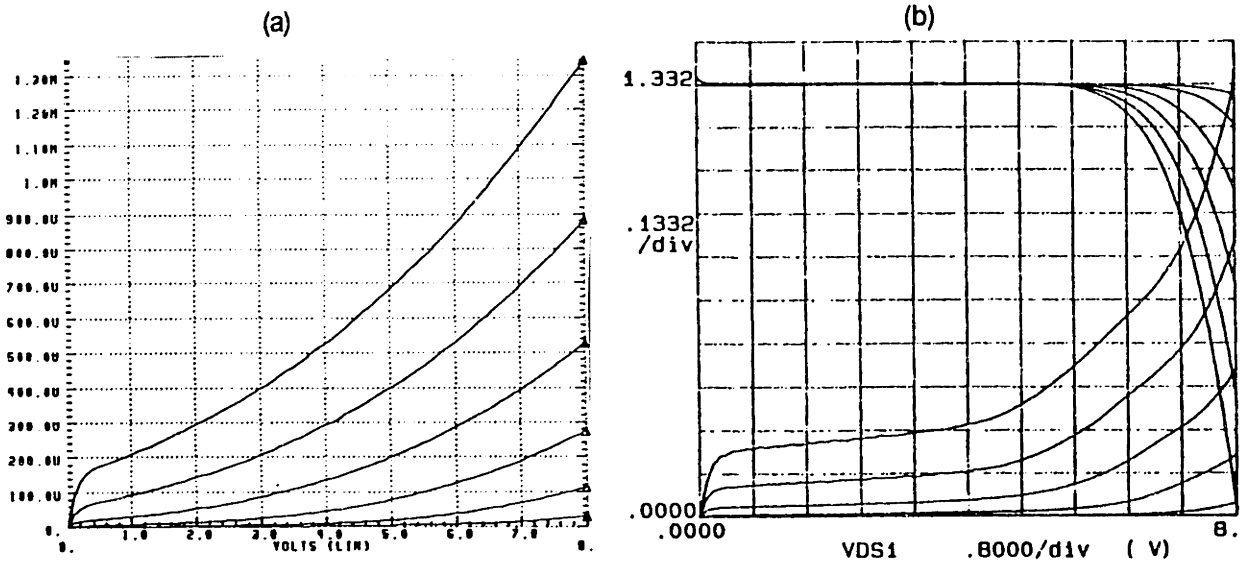

Figure 2.5 - Comparison of I_{DS} vs V_{DS} for V_{GS} = 0.1 to 0.6 for a 10 μm-wide by 1.0 μm-long enhancement-mode MESFET with the bulk biased at the source voltage between (a) HSPICE simulation and (b) measured data.

For design calculations, the simpler physics expressions are used. HSPICE expressions and simulations are used to only to predict final physical layout performance and confirm analytical circuit calculations. Useful expressions that predict first-order performance are as follows: For gate voltage near threshold, I_{DS} can be approximated by the square-law relationship given by:

$$I_{DS} = (W/L)N_d \mu\varepsilon/2t(V_{GS} - V_T)^2 \qquad 2.12$$

The ideal transconductance, $g_m = \partial I_{DS}/\partial V_{GS}$, is proportional to the incremental gate bias and is given by:

$$g_m=(W/L)N_d\mu\varepsilon/2t(V_{GS} - V_T) \quad 2.13$$

2.2.3 Capacitance Model

The HSPICE capacitance model uses the normal expressions for diode capacitances under both forward- and reverse-junction bias conditions shown in Equations 2.14 - 2.17. C_{GS} and C_{DS} reverse bias condition:

$$C_{GS} = C_{GSo} \cdot (1-V_{GS}/V_{BI})^N \quad 2.14$$

$$C_{DS} = C_{DSo} \cdot (1-V_{DS}/V_{BI})^N \quad 2.15$$

C_{GS} and C_{DS} forward bias condition:

$$C_{GS} = TT \cdot \partial I_{GS}/\partial V_{GS} + C_{GSo} \cdot (1-V_{GS}/V_{BI})^N \quad 2.16$$

$$C_{DS} = TT \cdot \partial I_{GD}/\partial V_{GD} + C_{DSo} \cdot (1-V_{DS}/V_{BI})^N \quad 2.17$$

where TT is the junction transit time, C_{GSo} and C_{DSo} are the zero bias junction capacitances, and V_{BI} is the junction potential. A more complicated option is available that includes the effects of velocity saturation and subthreshold biases on C_{GS} and C_{GD}. However, these expressions were found to give optimistic capacitance values and, therefore, were not employed in the device modeling. Instead, the model capacitance values employed are based on extracted S-parameter data measured with a Cascade Microtech probe station.[12]

2.3 Frequency-Dependent Output Conductance Model

For mixed-mode conversion circuits, the large-signal MESFET circuit model must accurately predict dc, ac, and transient-analysis-frequency-dependent output conductance. For ac analysis, the drain lag effect describes in section 1.4 can be modeled by a simple pole-zero network connected in parallel with the drain and source regions. However, this model is insufficient for transient analysis of pulse waveforms because the MESFET will

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[12] P. Nuytkens, laboratory measurements, 1991.

not shut off at low gate biases. In order to accurately model the transient response, a nonlinear device with the correct linear frequency on performance is placed in parallel with the intrinsic MESFET. An equivalent circuit model, shown in Figure 2.6, that exhibits these characteristics employs a series capacitor, C, and resistor-, R, loaded cascoded MOSFET in parallel with the intrinsic MESFET.[13] The parasitic MOSFET acts only as a parallel conduction during ac and transient operation. The MOSFET's intrinsic capacitances are set small compared to the MESFET's intrinsic capacitances, and the W/L ratio is set so the series on resistance is small compared to R. The ac-output conductance is set by selection of R with 1/RC determining the break-point frequency into the ac region and $1/Cr_o$ determining the break-point frequency out of the dc region of operation. Figure 2.7 compares the HSPICE step response of the foundry-supplied SPICE parameters and the enhanced HSPICE large-signal model. As Figure 2.7 indicates, the response of this nonlinear-lag-network mechanization accurately represents measured transient and ac performance.

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[13] L. Larson, "GaAs MESFET Equivalent Circuit Model," *IEEE Journal of Solid State Circuits*, Vol. SC-22, No. 4, August 1987, p. 572.

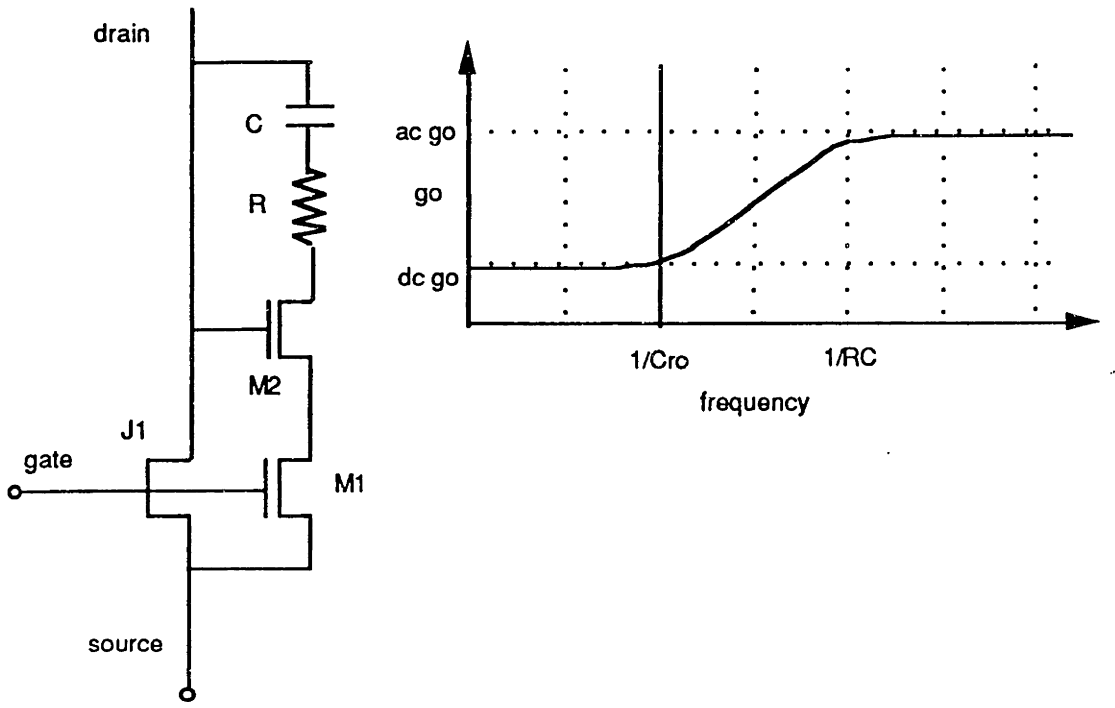

Figure 2.6 - Enhanced HPSICE frequency-dependent-output-conductance-MESFET model.

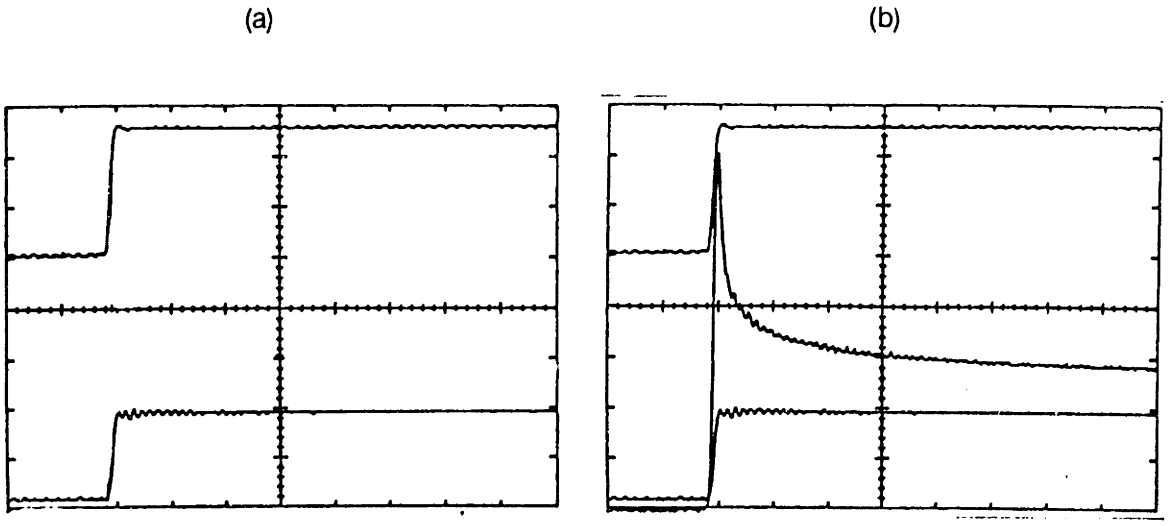

Figure 2.7 - Transient response of HSPICE model and frequency-dependent-output-conductance-enhanced-HSPICE-MESFET model.

2.4 Device-to-Substrate Model

The HSPICE GaAs MESFET model incorporates the backgate effect on both the depletion-mode and enhancement-mode devices by modifying the threshold voltage, V_T, of each device proportional to bulk-to-source voltage, as given by:

$$V_T = V_{To} + [GAMDS \cdot vds + k(vbs)] \tag{2.18}$$

where V_{To} is threshold voltage at zero V_{BS}, GAMDS is the drain voltage induced threshold voltage lowering coefficient, vgs is the internal gate-source voltage, vbs is the internal bulk-to-source voltage, vds is the internal drain-to-source voltage, k is the threshold-voltage sensitivity to bulk voltage. This equation accurately expresses the backgate effect on a discrete device assuming the bulk voltage is predetermined and set to a known value. However, in the absence of a bulk-voltage source, the HSPICE model incorrectly drives this voltage to the highest power supply potential and produces erroneous simulation results. In fabricated circuits, this voltage is either set to the lowest potential by biasing the bulk electrode to V_{SS} (the most negative power supply voltage) or is left floating where the substrate charge drives the bulk potential to a voltage between V_{SS} and one diode drop above V_{SS}. For the floating case, this voltage can be accurately determined by modeling and adding each transistor's contribution to the bulk charge. The charge contribution of a single inverter stage composed of a common source enhancement-mode transistor, J_1, and depletion-mode load transistor, J_2, can be modeled through the addition of diodes D_1, D_2, and D_3 and capacitor C as shown in Figure 2.8. In this circuit, D_1 models the n^+/p^- source-to-bulk diode of J_1, D_2 models the n^+/p^- drain-to-bulk diode of J_1 in parallel with the n^+/p^- source-to-bulk diode of J_2, and diode D_3 models the n^+/p^- drain-to-bulk diode of J_2. Capacitor C includes the bulk-to-V_{DD} and bulk-to-V_{SS} parallel plate capacitances. Resistor R models the substrate conductivity between devices.

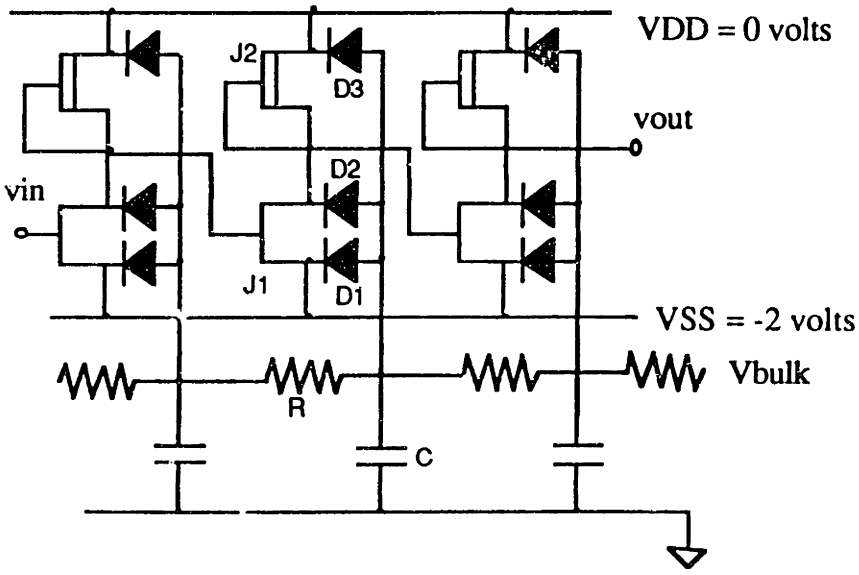

Figure 2.8 - Inverter stage with source-to-bulk and drain-to-bulk diodes.

This model can be used for understanding and demonstrating both crosstalk and duty-cycle modulation effects observed in digital GaAs MESFET circuits. Since all of the backgates of a digital GaAs MESFET circuit are connected to each other through the resistivity of the p^- implanted buffer layer, the connection may be modeled with discrete resistors, R, sized in proportion to the distance a device is located from its nearest neighboring devices. Crosstalk can be reduced by either increasing the resistivity of the p^- buffer layer or ac-grounding the bulk. As described earlier, increasing the resistivity of the p^- buffer layer decreases threshold uniformity, which in turn limits integration size by reducing noise margins. Ac-grounding the bulk by either biasing the back of the die to V_{SS}, or directly biasing the p^- implant layer through a p^+ ohmic contact to V_{SS}, reduces device crosstalk at the cost of increased backgating of devices biased above V_{SS}. It is therefore necessary to develop a process technology that provides a heavy, p^- buried layer implant and at the same time isolates devices. This is accomplished by adding n^+ ohmic guard rings that isolate p^+ ohmic biased regions. This device and circuit isolation technique is described in Chapter 3. Input duty-cycle modulation of output levels observed in digital

GaAs MESFET circuits can be seen through the small signal equivalent inverter model of Figure 2.9.

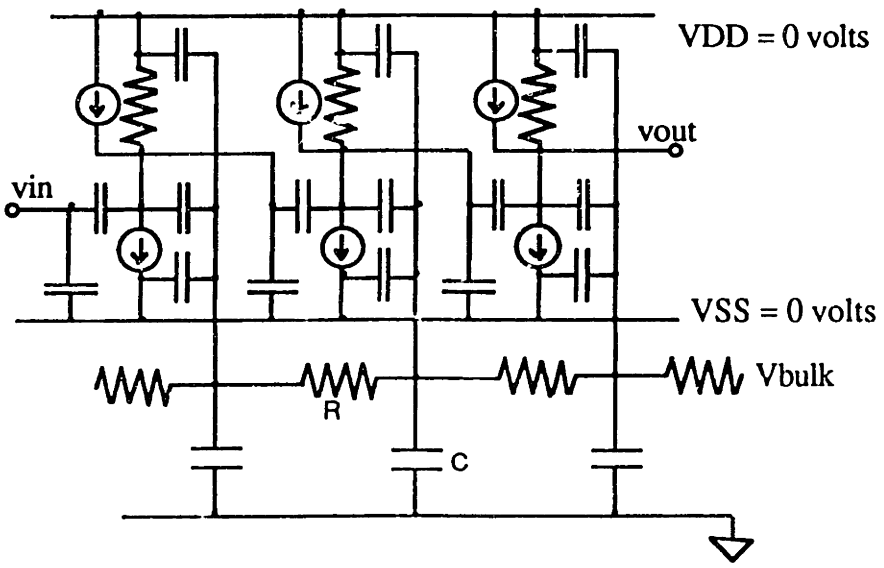

Figure 2.9 - Inverter stage with source-to-bulk and drain-to-bulk diodes small signal equivalent.

The voltage switching transients charge and discharge the diode capacitances, which are filtered by the low pass filter formed from the p^- layer resistance and capacitance. This low-pass filter averages the switching transients to produce a dc-bulk-voltage potential proportional to the input wave form duty-cycle. An HSPICE simulation comparing the inverter stage bulk node with (a) 25 % high - 75% low periodic pulse train, (b) 50 % high - 50% low periodic pulse train, and (c) 75 % high - 25% low periodic pulse train, is shown in Figure 2.10. The bulk voltage of -1.575 in Figure 2.10 (a) reduces the pulse swing in by 25 mV while the bulk voltage of -1.500 in Figure 2.10 (c) increases the pulse swing by 25 mV over the nominal voltage pulse swing of Figure 2.10 (b).

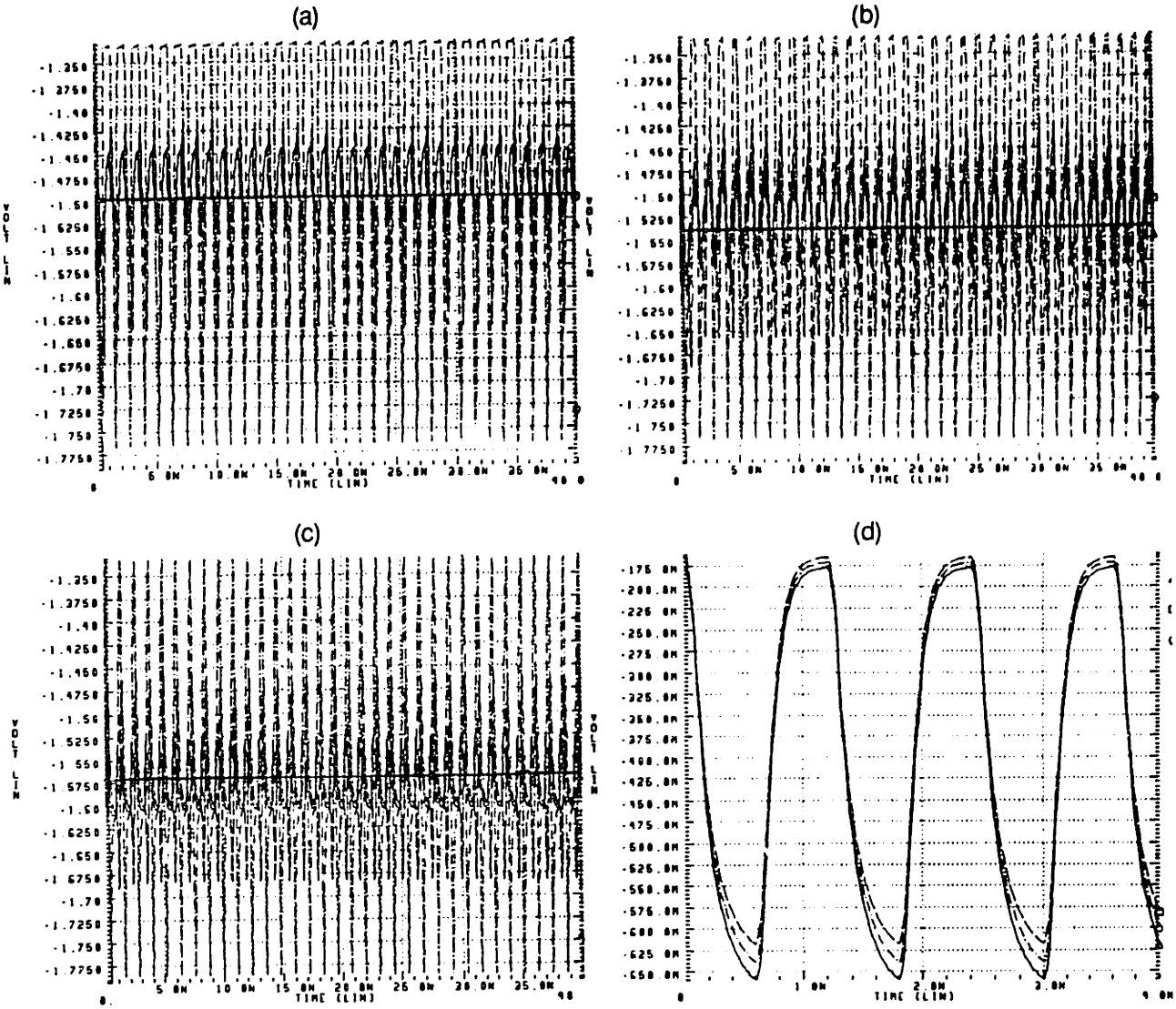

Figure 2.10 - HSPICE simulation showing the inverter stage bulk node with (a) 25 % high - 75% low periodic pulse train, (b) 50 % high - 50% low periodic pulse train, and (c) 75 % high - 25% low periodic pulse train and (d) output level shifts due to modulation.

Input duty-cycle modulation of output levels can be eliminated by ac-grounding the bulk through either biasing the back of the die to V_{SS} or directly biasing the p^- implant layer through a p^+ ohmic contact to V_{SS}.

The complete, enhanced HSPICE model that incorporates reverse-bias diodes for the MESFET's channel substrate interface to accurately model the dynamic backgating effect and parallel MOSFET and RC to accurately model frequency-dependent output

conductance is shown in Figure 2.11. Capacitor cds has a fixed value determined primarily by the layout and parasitics. Capacitors cbs and cbd are the capacitances due to the channel substrate p-n junction. Capacitor csd2 and resistor rds2 in the ac and ac noise model are the are the small signal equivalent of R and C of the transient model. This four-terminal model was used to simulate critical circuit performance of the digital-to-analog converter including glitch energy of the switching transients, settling time, and switch-to-current-source crosstalk.

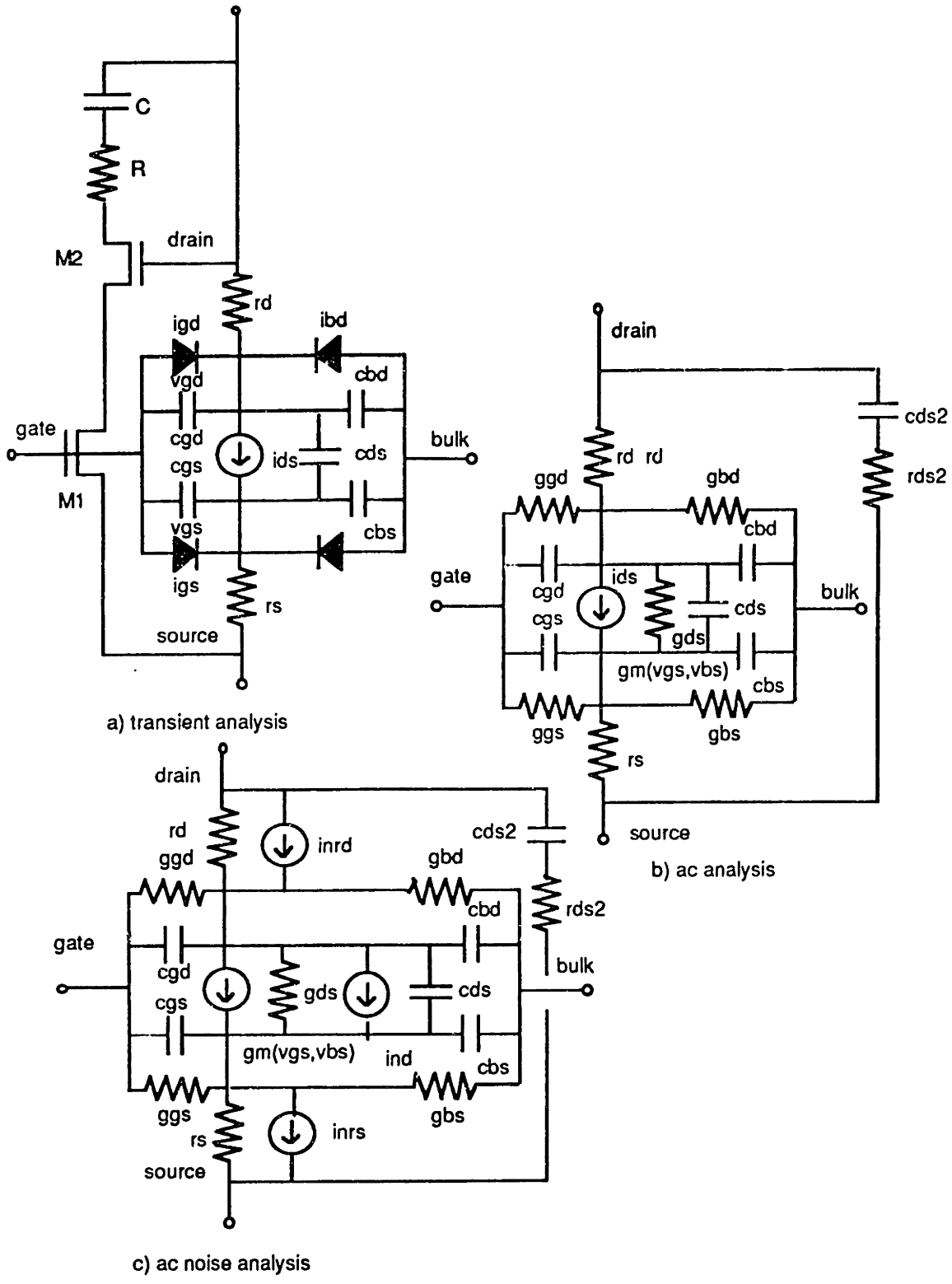

Figure 2.11 - Enhanced HSPICE models for (a) transient analysis, (b) ac analysis, and (c) ac noise analysis.

The measured test structures described in Chapter 3 resulted in the HSPICE model parameters for the Vitesse GaAs MESFET process as shown in Table 2.1.

Table 2.1 - Large- and Small-Signal GaAs MESFET HSPICE Model Parameters (for 1 μm gate lengths)

Parameter	Enhancement-mode*	Depletion-mode**
V_T	250 mV	800 mV
σV_T (local 100 x 100 μm)	15 mV	45 mV
I_{DSS}	60 mA/mm	60 mA/mm
σI_{DSS}	2.5%	6.3%
g_m	240 ms/mm	150 ms/mm
σg_m	2%	4.2%
cgs	1.2 pF/mm	1.9 pF/mm
cgd	330 fF/mm	300 fF/mm
cds	200 fF/mm	210 fF/mm
rgs (1/ggs)	2.2 kΩ•mm	28 kΩ•mm
rgd (1/ggd)	32 kΩ•mm	40 kΩ•mm
r_os (1/gds,1/go)	180 mΩ•mm	100 mΩ•mm
a_{vo}	23 V/V	16 V/V
f_T	15.5 GHz	16.5 GHz

Bias Conditions:

* V_{GS} = 0.5 V, VDS = 1.0 V

** V_{GS} = 0.0 V, VDS = 1.0 V

Chapter 3

GaAs MESFET Process Enhancements and Design Methodology for Mixed-Mode MESFET Circuits

3.1 GaAs MESFET Process Enhancements

Based on the device physics and circuit analysis presented in Chapter 2, process enhancements and circuit design methodology for simultaneously reducing backgating, increasing isolation, and maintaining high threshold uniformity of GaAs MESFET devices were designed. These include: 1) an additional buried p^- implant inserted prior to active area patterning of the transistor to control device-threshold uniformity and short-channel effects, 2) a p^+ ohmic contact process step in the circuit design that can be used to bias the p^- buried layer background implant and isolate bulk regions, and 3) an n^+ ohmic contact ring placed around the p^+ contact regions and biased to a positive potential to form a depletion region through the p^- layer to the semi-insulating substrate that increases device isolation.

The digital direct-coupled-FET-logic (DCFL) and complementary-level-FET-logic (CLFL) cells, biased with depletion transistor loads connected to ground (V_{CC}) and enhancement-mode switches connected to -2 volts (V_{TT}), are isolated with p^+ ohmic contact rings connected to V_{TT} to prevent turn-on of the bulk-to-source diode of the enhancement-mode transistor. In both the DCFL and CLFL circuit topologies, the enhancement-mode source is always connected to V_{TT} setting V_{BS} equals zero, which eliminates backgate of this device. The high-voltage output of either a DCFL or CLFL circuit stage is clamped by the next stage's enhancement-mode input transistor's gate-to-source Schottky diode to 0.6 volts above V_{TT}. For a logic-high-voltage level, the driving

stage's depletion-mode load source-to-bulk voltage is therefore limited to -0.6 volts, which is above the depletion-mode threshold of -0.8 volts. For a logic-low-voltage level, the driving stage's depletion-mode load source to bulk voltage is limited to -0.1 volts (I_{DSS} of the depletion-mode load multiplied by the enhancement-mode on resistance), which is significantly above the depletion-mode threshold of -0.8 volts. Thus, for the depletion-mode load, there is a positive backgate effect. It is therefore necessary to size the enhancement-mode device large enough to handle the worst-case depletion current occurring during a logic low. This design constraint limits the minimum circuit β ratio, defined in Equation 3.1, to 10 in order to have sufficient negative voltage-level noise margins.[1]

$$\beta \text{ ratio} = (W_E/L_E)/(W_D/L_D) \qquad 3.1$$

The 0.5 volt depletion-mode backgate modulation does reduce switching speed because the load current is reduced as the device switches from logic low to high in a conventional inverter stage. However, circuits employing feedback in the output stage overcome the switching speed limitation and are discussed in Chapter 4.

The analog cell's discrete transistors are isolated with p^+ ohmic contact rings connected to the source of the transistor forcing V_{BS} equal to zero independent of source voltage bias. To reduce the substrate currents generated in analog circuits with transistor sources biased at large voltages differences (greater than 1 volt), an n^+ ohmic contact ring placed around the p^+ contact regions and biased to the drain of the transistor is used to form a depletion region through the p^- layer to the semi-insulating substrate. This depletion region increases the device isolation and reduces the substrate current, thereby allowing higher transistor packing over prior art. Analog transistors biased at the same source potential are grouped within a single p^+ ohmic ring bulk bias and n^+ ohmic guard ring. The combination of concentric p^+ ohmic and n^+ ohmic ring topology is similar to a well-

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[1] *Vitesse Foundry Design Manual*, Version 5.0, 1991.

isolated CMOS process. In a further development, the initial p^- buried implant could be patterned only under the active area of the MESFET, which would reduce the need for an n^+ ohmic isolation ring at the cost of an additional mask step. However, removal of the n^+ ohmic isolation is not an advantage in analog circuit designs where device density is not a priority.

A cross section of the GaAs MESFET p^+ ohmic ring bulk bias and n^+ ohmic ring isolation mixed-mode process technology is shown in Figure 3.1 (a). The layout of a generic mixed-mode system containing digital macro cells isolated with p^+ ohmic contact rings biased to V_{TT} and analog cells with discrete transistors isolated with concentric n^+ ohmic contact guard rings surrounding p^+ ohmic bulk biased to the source of the individual transistors is shown in Figure 3.1 (b). With this methodology, an acceptably high digital device density is achieved while maintaining high isolation. The increase in device isolation reduces jitter and phase noise characteristics of digital clock, comparator, latch, and switch circuits. In addition, backgate uniformity is improved because the substrate is pinned to a known reference. This improves relative matching of current sources. High-performance clocks, comparators, latches, switches, and current sources are all required components in the development of high-precision and high-speed analog and mixed-mode circuits. The design rationale for using each of the bulk-biasing and isolation techniques employed in this mixed-mode process is examined in the next sections including use of the buried p^- layer implant, p^+ ohmic contact bulk bias and isolation, p-well isolation and n^+ ohmic guard ring isolation. All of these techniques except p-well isolation were used in the design of the 12-bit digital-to-analog converter. The p-well isolation technique is included here for completeness.

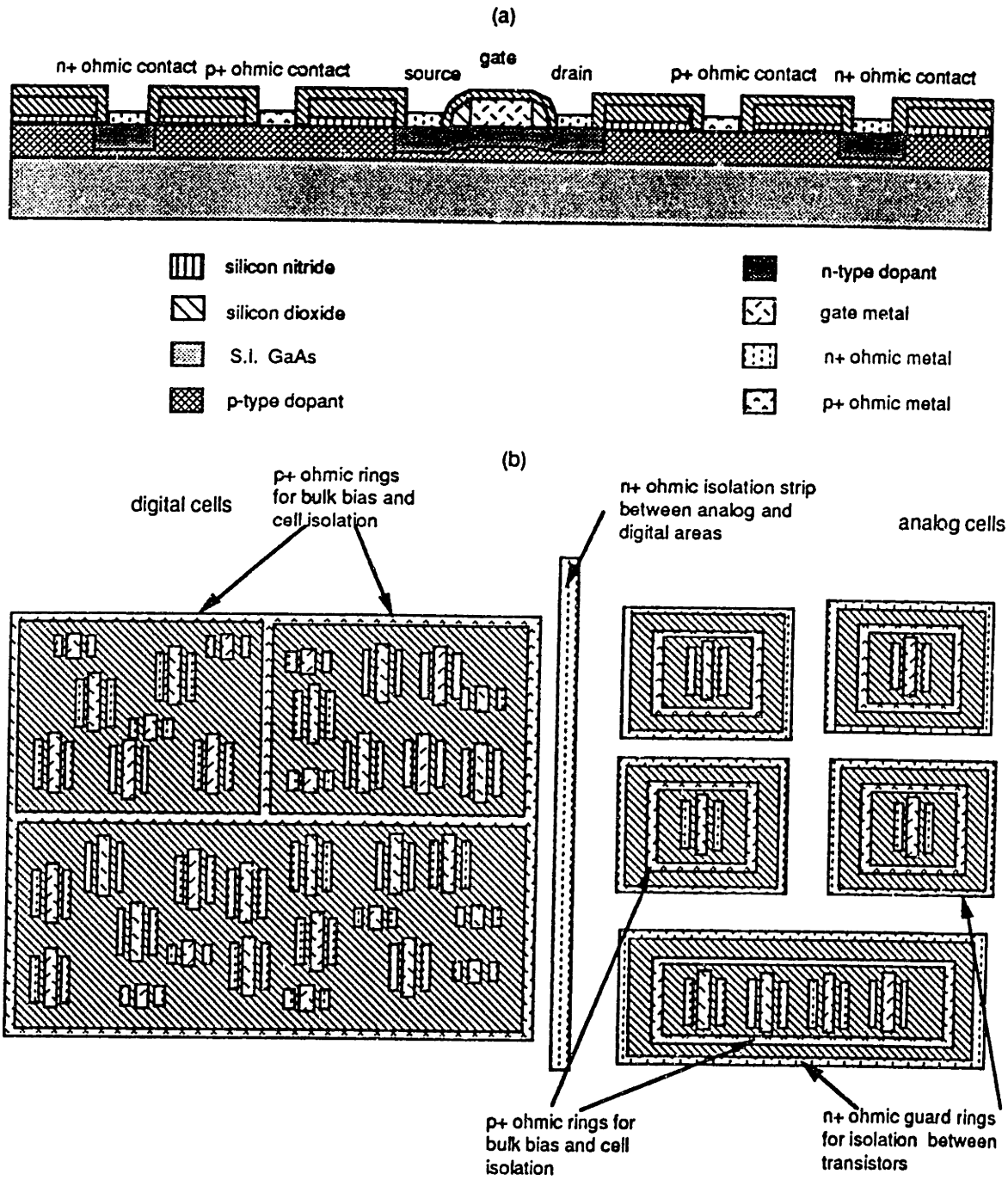

Figure 3.1 - GaAs MESFET analog and mixed-mode process technology: (a) horizontal view of self-aligned gate MESFET process with p+ ohmic and n+ ohmic ring isolation; (b) top view of layout showing analog and digital cell isolation and bulk bias.

3.1.1 Buried p^- Buffer Layer

The use of an ion-implanted buried p^- layer implant to control the short-channel effects in GaAs MESFETs was proposed by Yamasaki and Hirayama in 1983.[2] Both Mg and Be p-type dopants have been successfully employed as the p^- buffer layer. The p^- buffer layer has also been shown to reduce threshold spreads by mitigating the effects of background acceptor concentrations and variations of the base wafer. Figure 3.2 shows a cross section of a self-aligned gate GaAs MESFET process with a p^- buried implant layer. The bulk is biased by plating the back of the wafer.

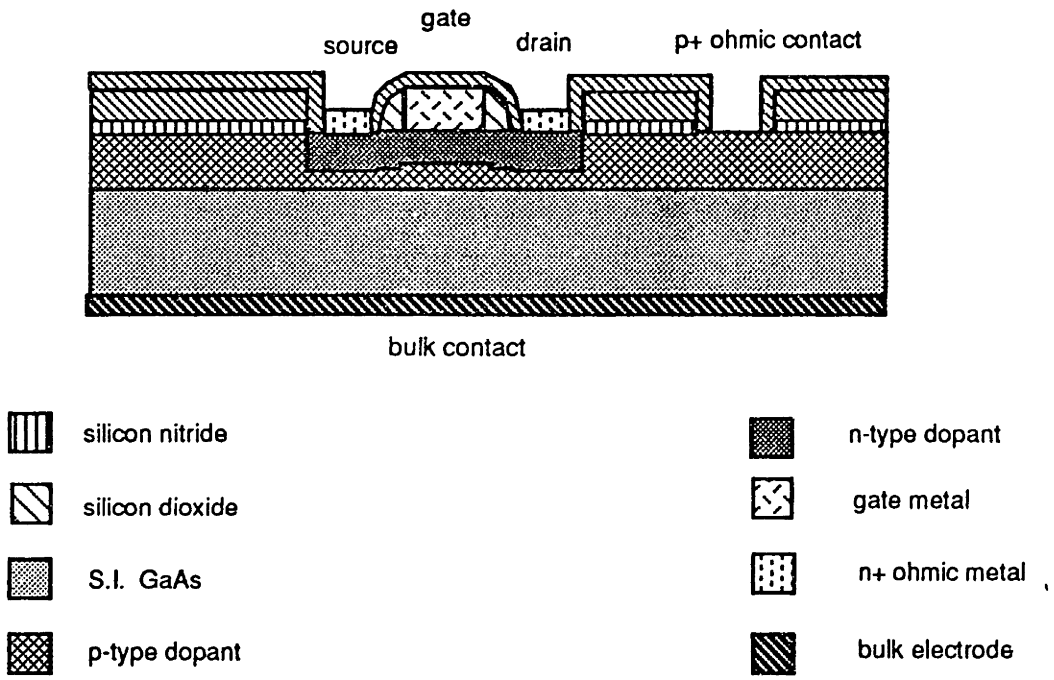

Figure 3.2 - Self-aligned GaAs MESFET process with p^- buried implant.

A high-dose buried p^- layer implant has resulted in an enhancement-mode MESFET (σV_T) of 8 mV across a 3 inch wafer.[3] Large variations in enhancement-mode V_T directly reduce noise margins. Therefore, reducing and controlling σV_T across the wafer and from wafer

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[2] K. Yamasakai et al., "Theoretical Approach in Gate Shortening of n+ Self-Aligned GaAs FETs," in *Proceedings of Japan IECE National Conference on Semiconductors*, 1983.

[3] R. Sadler et al., "A High-Yield Buried p-Layer Fabrication Process for GaAs LSI Circuits," *IEEE Transactions on Electron Devices*, Vol. 38, No. 6, 1991.

lot to wafer lot is the single most important requirement necessary to achieve high yields of VLSI direct-coupled-FET-logic circuits. In mixed-mode applications, small σV_T increases comparator resolution, reduces operational amplifier offsets, and reduces glitch energy of switches in a digital-to-analog converter. An adverse effect of employing a p^- buffer layer is the increased gate-to-bulk, source-to-bulk, and drain-to-bulk parasitic capacitances, which reduce switching speed, increase gate delay, and reduce amplifier bandwidth. A second negative effect of employing a high p^- buffer layer implant is a reduction in device isolation, which causes an increase in crosstalk because the substrate resistivity has been decreased up to two orders of magnitude over that of the base wafer. This increased substrate conductivity causes increased phase noise in analog circuits and a reduction of noise margin in digital circuits. The increased substrate conductivity enables the local charge pumping of the substrate to undesirably affect adjacent cell backgates. This is analyzed for ring oscillators in Chapter 4.

The effect of a 150-keV Mg buried p^- implant on a device's electron concentration profile is shown in Figure 3.3 where the channel has been implanted with Si at 90-keV. Without the p-buried implant at all, the n(x) profile is broad and has a fluctuating tail region caused by the overlap of the adjacent n^+ region in the self-aligned device structure. The extent of this tail is not controlled, which results in variations in MESFET threshold and I_{DSS}. With the p^- buried implant, the electron concentration profile is sharpened, resulting in a steeper tail and higher peak concentration, which clearly defines the channel depth and therefore threshold.

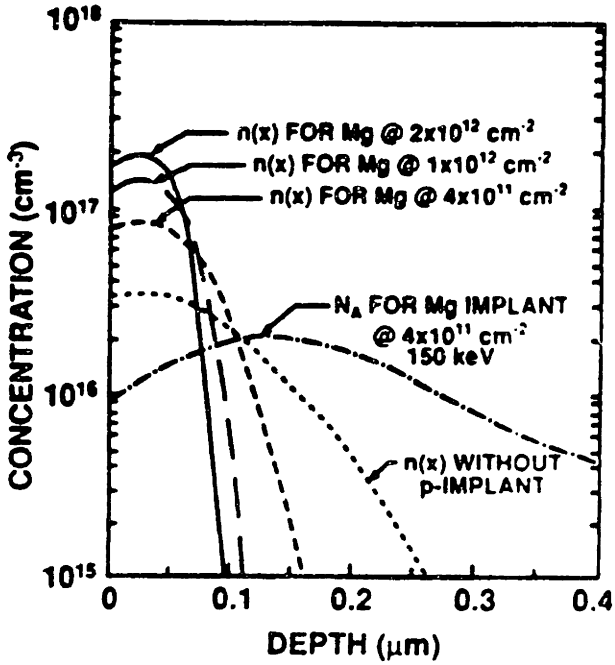

Figure 3.3 - Mg acceptor concentration profile $N_A(x)$ and resulting electron concentration profile n(x) for various doses.[4]

[4] R. Sadler et al., "A High-Yield Buried p-Layer Fabrication Process for GaAs LSI Circuits," *IEEE Transactions on Electron Devices*, Vol. 38, No. 6, 1991.

3.1.2 P+ Ohmic Contact Isolation

A p^+ ohmic-ring contact is used to both dc-bias and ac-ground the p^- buried buffer layer. This enables the p^- buried buffer to be used in order to increase MESFET threshold uniformity, while at the same time maintaining device isolation. Without the p^+ ohmic contact bias, the p^- buried implant layer potential would be charge pumped to a value between V_{SS} and V_{SS} + 1 diode drop, depending upon the dc-average of the duty cycle, clock risetime/falltime, and β ratio of digital gates of all the switching circuits of a specific design. Since the p^- buried buffer layer is not a perfect conductor, the averaging of the charge pumping is both a localized area- and device-geometry-dependent effect. The backgate potential contains higher frequency components that crosstalk to adjacent devices causing close-in side band modulation. The p^+ ohmic contact rings ac-short the substrate and attenuate the crosstalk modulation. The p^+ ohmic contact rings also enable the backgates of large areas of one circuit to be biased at one potential that is several volts different from a second area on the same die. This feature is particularly useful in combining 2-volt DCFL circuits with 5 volt SCFL circuits. SCFL and DCFL circuits are often combined in high-speed, time-division multiplexers that contain a single high-speed SCFL input, which sequentially drives an array of lower-speed DCFL outputs. A cross section and layout of the p^+ ohmic ring isolation process is shown in Figure 3.4.

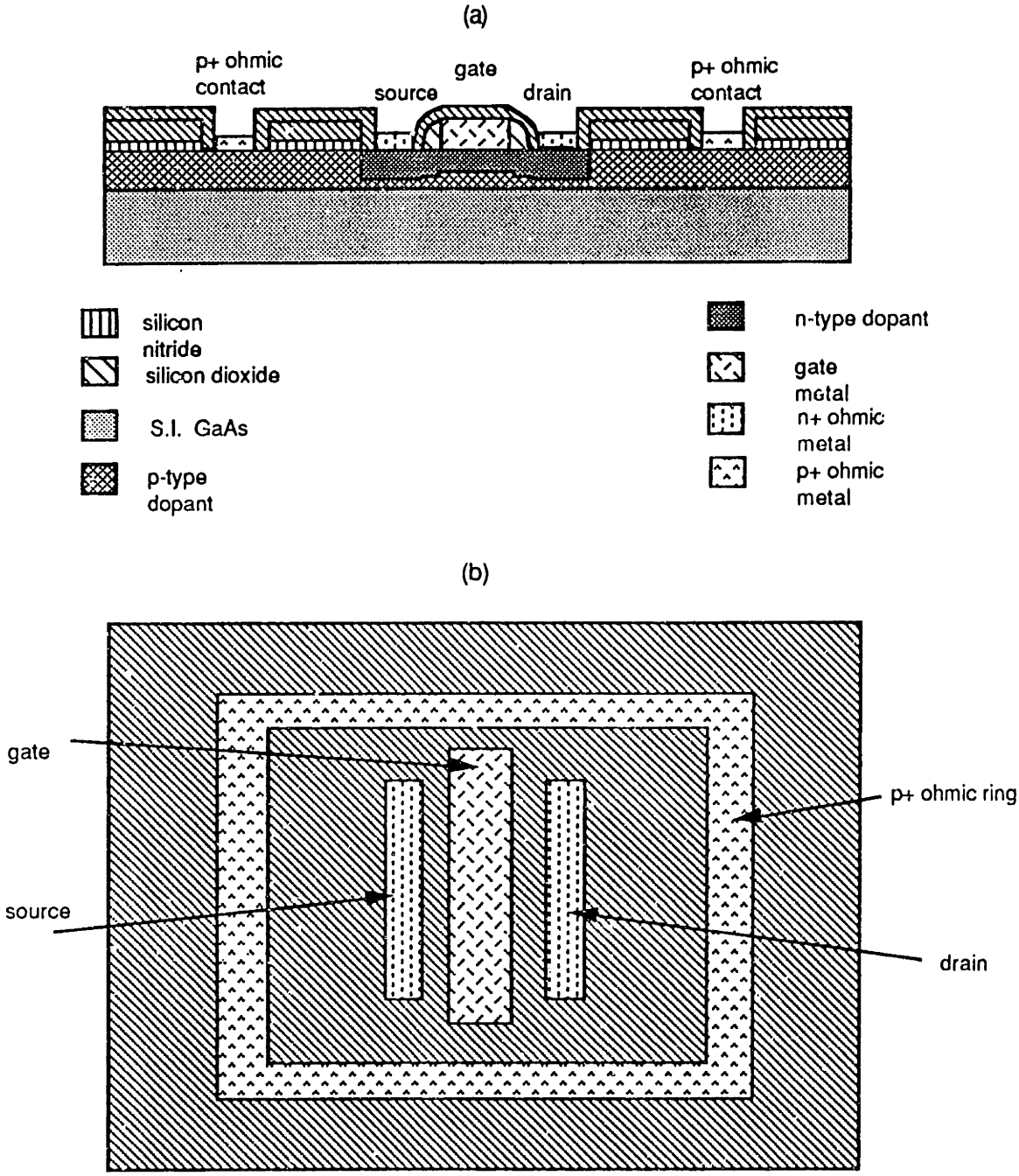

Figure 3.4 - GaAs MESFET p^+ ohmic isolation process (a) horizontal view of Self-Aligned Gate MESFET Process with p^+ ohmic isolation; (b) top view of transistor layout showing p+ ohmic ring isolation and bulk bias.

3.1.3 P-Well Isolation

Adding the p^- buffer layer only under the active area of the transistor and biasing this p-well to the source of the transistor can be used as an effective technique to reduce the backgate effect in analog circuits.[5] The source-to-bulk connection insures that this n^+ ohmic/p^- buffer layer junction neither becomes forward biased nor modulated by gate-to-source or drain-to-source voltage transients. As mentioned in section 1.4, MESFET frequency-dependent output conductance has been attributed to the charging and discharging of EL2 traps in the substrate. This topology also insures that the channel to p-well potential is independent of changes in the charge states of the EL2 traps. A more subtle effect and advantage of the p-well isolation is the bootstrapping of parasitic substrate capacitances in circuits, including unity-gain-buffer and current-source-load circuits. High-frequency designs of these topologies employ bootstrapping techniques to clamp V_{DS} and V_{GS} to reduce the effect of C_{DS} and C_{GS} and to achieve high bandwidths that are limited by the parasitic source-to-p^- buffer layer and drain-to-p^- buffer layer capacitances. Actively driving the p^- buffer layer reduces these capacitances to that of the p^- buffer-layer-to-bulk-parallel-plate capacitance. This p-well structure is similar to the p-well NMOS device used in silicon CMOS processes. Two problems associated with this process and circuit technique are first, the requirement of an additional mask and processing step to pattern the p^- buried layer implant and, second, the resulting reduction in digital-device density due to the area requirement of the p^+ ohmic biasing contact. A cross section and layout of the p-well isolation process is shown in Figure 3.5.

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[5] P. Canfield et al., "A p-Well GaAs MESFET Technology for Mixed-Mode Applications," *IEEE Journal of Solid State Circuits*, Vol. 25, No. 6, December 1990.

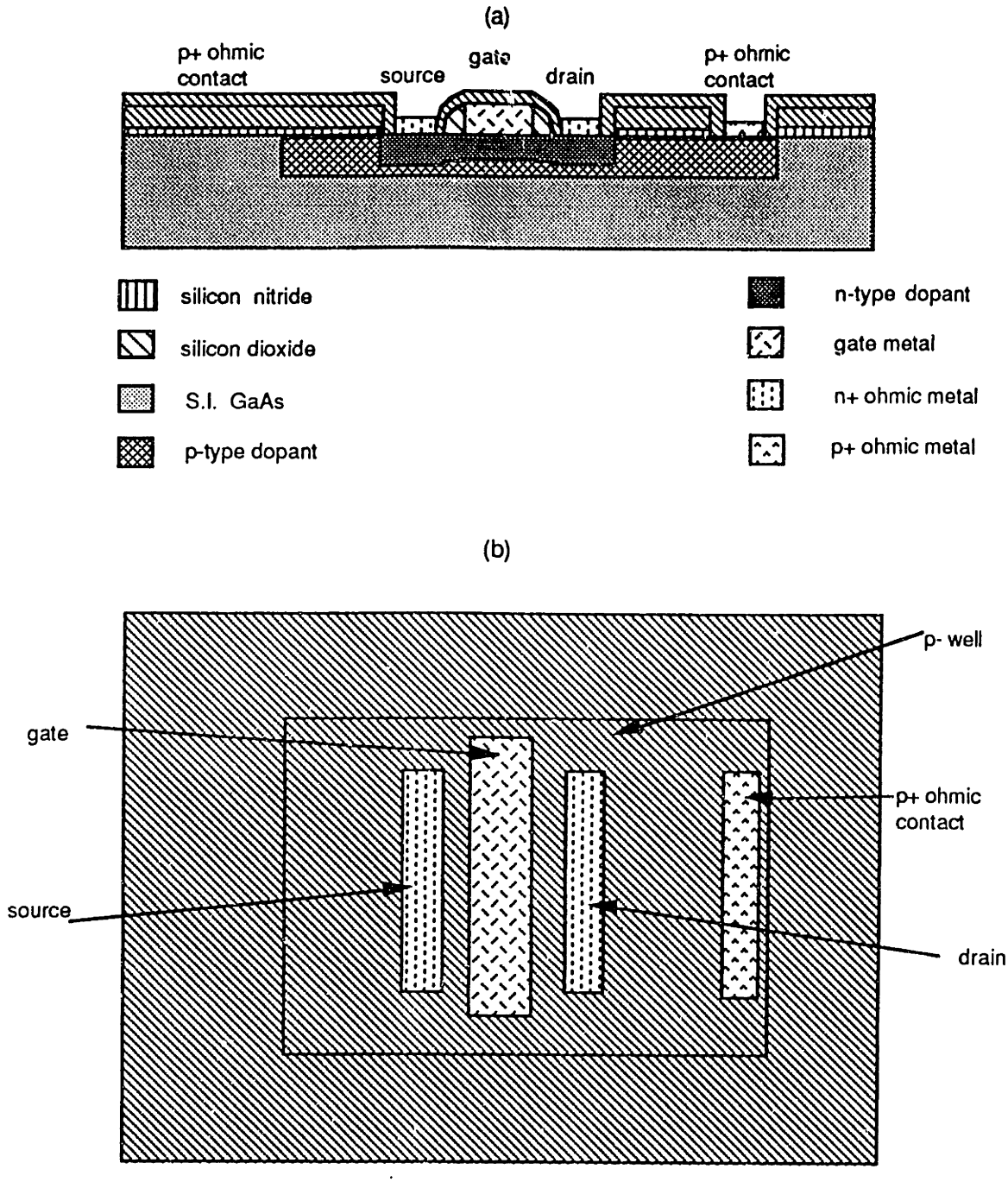

Figure 3.5 - GaAs MESFET p-well isolation process: (a) horizontal view of self-aligned gate MESFET process with p-well isolation; (b) top view of transistor layout showing p- well isolation and bulk bias.

3.1.4 N^+ Ohmic Contact

An n^+ ohmic contact cell ring was placed concentrically around the p^+ ohmic cell ring to provide a second ac-ground shield and increase the substrate resistivity between analog cells. The n^+ ohmic guard rings are made at the same time and with the same implant as the source/drain implants and therefore do not require an additional processing step. The n^+ ohmic ring acts like a two-dimensional Faraday shield, which terminates horizontal electric field lines generated by external-cell circuits, thereby reducing electromagnetic coupling between cell circuits. In a similar fashion, radiating electric fields produced by the cell itself are terminated on the n^+ ohmic ring. N^+ ohmic metal was selected to provide the shield instead of gate metal, metal 1, metal 2, or metal 3 because when the n^+ ohmic metal is biased to a positive potential, a depletion region forms under the vertical n^+ohmic/p^- buffer layer diode. For sufficient applied-positive n^+ ohmic-to-bulk voltage, the depletion region extends through the p^- buffer layer to the semi-insulating substrate, increasing the sheet resistance between cells two orders of magnitude back to that of the original semi-insulating substrate without the p^- buffer layer. A cross section and layout of the p^+ ohmic bulk bias and n^+ ohmic guard ring isolation process is shown in Figure 3.6.

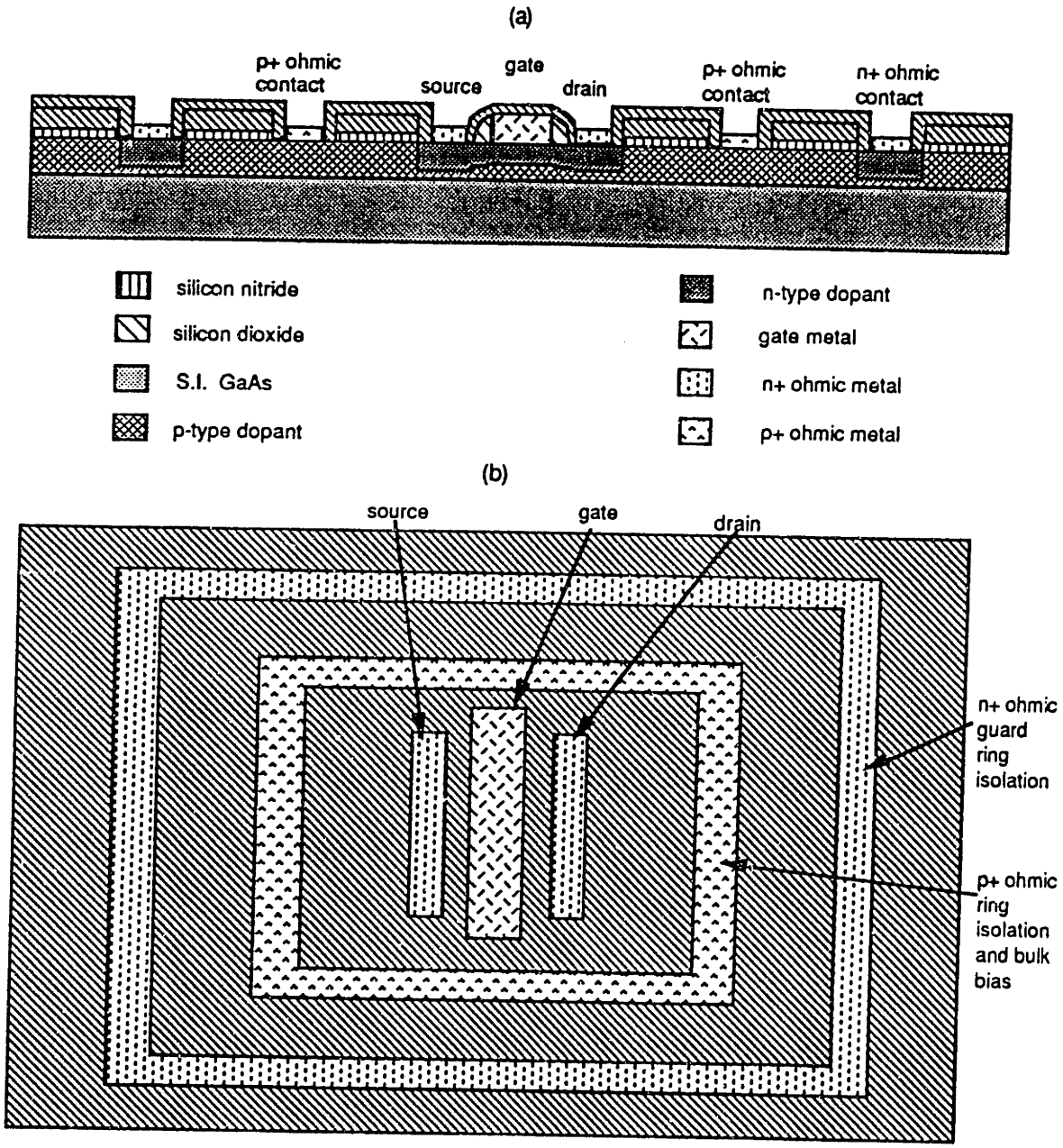

Figure 3.6 - GaAs MESFET analog and mixed-mode process technology: (a) horizontal view of self-aligned gate MESFET process with p+ ohmic bulk bias and n+ ohmic guard ring isolation; (b) top view of layout showing single analog transistor isolation and bulk bias.

3.2 GaAs MESFET Circuit Design Methodology

The p^+ ohmic ring bulk isolation and n^+ ohmic guard ring process enable circuit topologies incorporating cascode and self-bootstrap techniques to achieve high performance. The combined cascode and self-bootstrap techniques hold V_{DS} of the primary transistor constant, which reduces the frequency-dependent output conductance. Connecting the bulk to source of transistor sets V_{BS} to zero. It is important to note that only the *combination* of the bulk isolation process and the cascode/self-bootstrap circuit technique act to reduce the frequency-dependent output conductance. It is necessary to hold constant both V_{DS} and V_{BS} to reduce frequency-dependent output conductance. Clamping one without the other results in marginal performance. The circuit performance of a current source, cascode transistor current switch, and voltage-level shifter are examined in this process. Each topology shows improved performance over prior art and forms the core technology on which the 12-bit digital-to-analog converter described in Chapter 5 was developed.

3.2.1 Current Source

High-precision analog and mixed-mode circuits all require current sources with high output impedance, low- temperature and process sensitivity, precise scaling and matching, and positive and negative voltage biasing. GaAs MESFET enhancement-mode/depletion-mode processes lacking a p-channel device are limited to NMOS-like current-source topologies. The simplest current source is a singie depletion-mode transistor with its gate and source connected together and biased at V_{DS} to be greater than V_{SAT}, which results in a current source output impedance of $1/\lambda I_{bias}$ where λ is defined as the channel length modulation parameter. The ideal $1/\lambda I_{bias}$ output impedance occurs only when this current source is operated from the negative voltage rail where V_{BS} is equal to zero. This current source suffers from the backgate effect when operated from the positive voltage rail where V_{BS} is not zero. Figures 3.7 (a) and (b) show the simple current source IV characteristics operating under both described bias conditions, while

Figure 3.7 (c) simulates a third condition where the substrate is biased to the source node of the simple depletion mode transistor connected to a positive voltage rail. Note that Figures 3.7 (a) and 3.7 (c) are linear and symmetric around ground, while that of 3.7 (b) has a significant nonlinear tail as V_{DS} is increased above 1 volt.

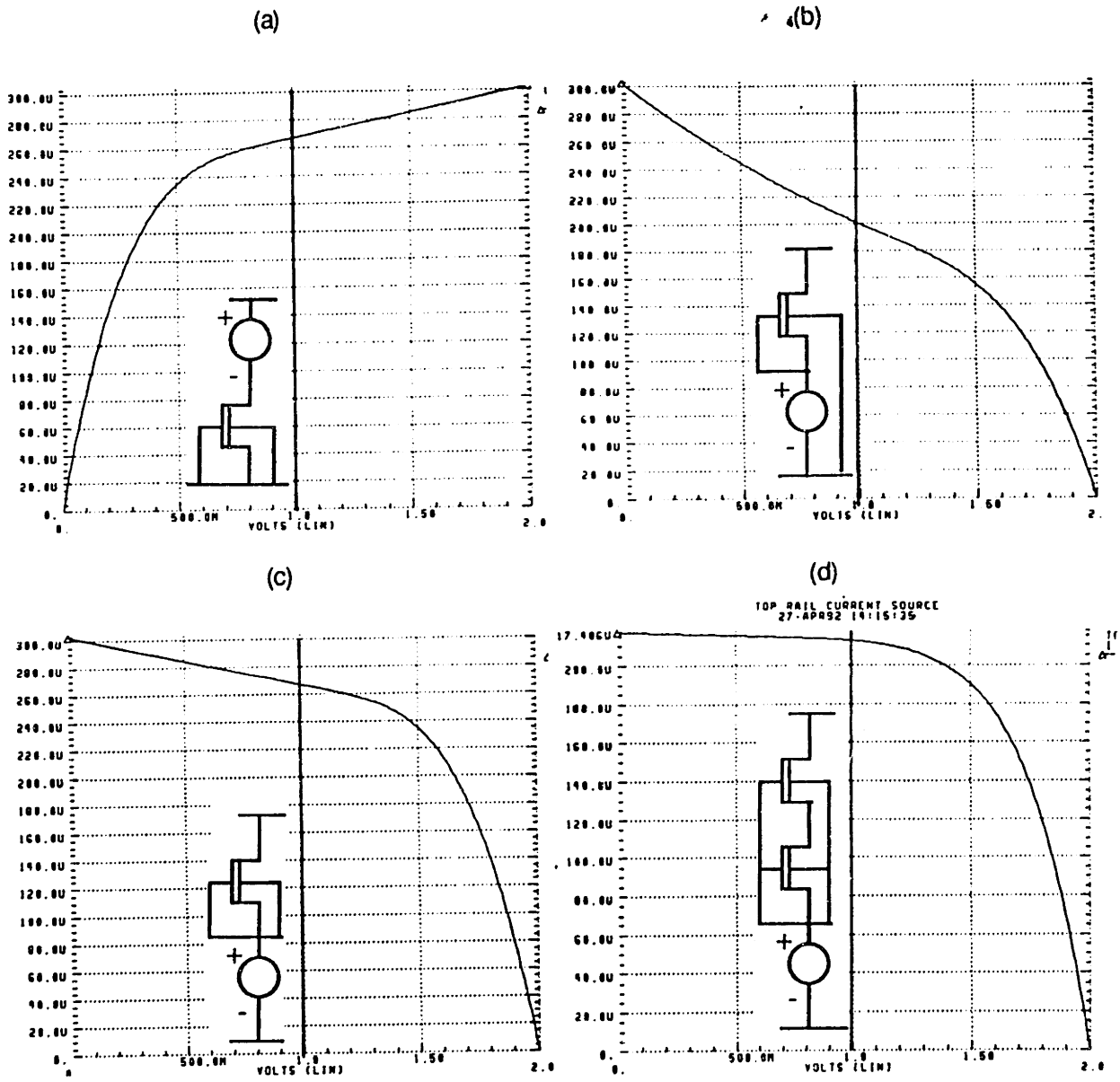

Figure 3.7 - Depletion-mode transistor current source I-V characteristics (a) negative voltage rail biased depletion current source (V_{BS}=0); (b) positive voltage-rail-biased depletion current source showing backgate effect (V_{BS} dependent on bias); (c) positive voltage rail biased depletion current source without backgate effect (V_{BS}=0); (d) cascode depletion current source (V_{BS}=0).

The simple current source output impedance can be improved by using the two-transistor (J_1, J_2) self-bootstrapped current source methodology shown in Figure 3.7 (d). The circuit is self-bootstrapped because V_{GS1}=0 and, therefore, I_{DS1}=I_{DSS}; J_2 is now biased at a constant I_{DS}, and, for J_2 operating in early saturation, V_{GS2} is constant, which in turn clamps V_{DS1}. The circuit relies on the early-saturation phenomenon to maintain J_1 and J_2 in saturation.[6] The widths of transistors J_1 and J_2 are chosen to operate both devices in the saturation region, which increases the output impedance of the current source by 1+ gm_1r_{o1}. All of the top voltage rail current sources impedances are increased through the source-substrate technique. Also, matching between positive and negative voltage-rail biased current sources is significantly improved through the source-biased-substrate technique. This results in higher performance current mirrors, which are an integral building block of analog designs.

3.2.2 Cascode Amplifier

Examining the simple model of frequency-dependent output conductance developed in section 2, it becomes clear that cascoded-MESFET circuit topologies that clamp the drain-to-source voltage of the primary device to a constant voltage will reduce the frequency-dependent output conductance. Several possible topologies are shown in Figure 3.8.

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[6] L. Larson, "Comparison of Amplifier Gain Enhancement Techniques for GaAs MESFET Analog Integrated Circuits," *Electron Letters*, Vol. 22, No. 21, October 1986.

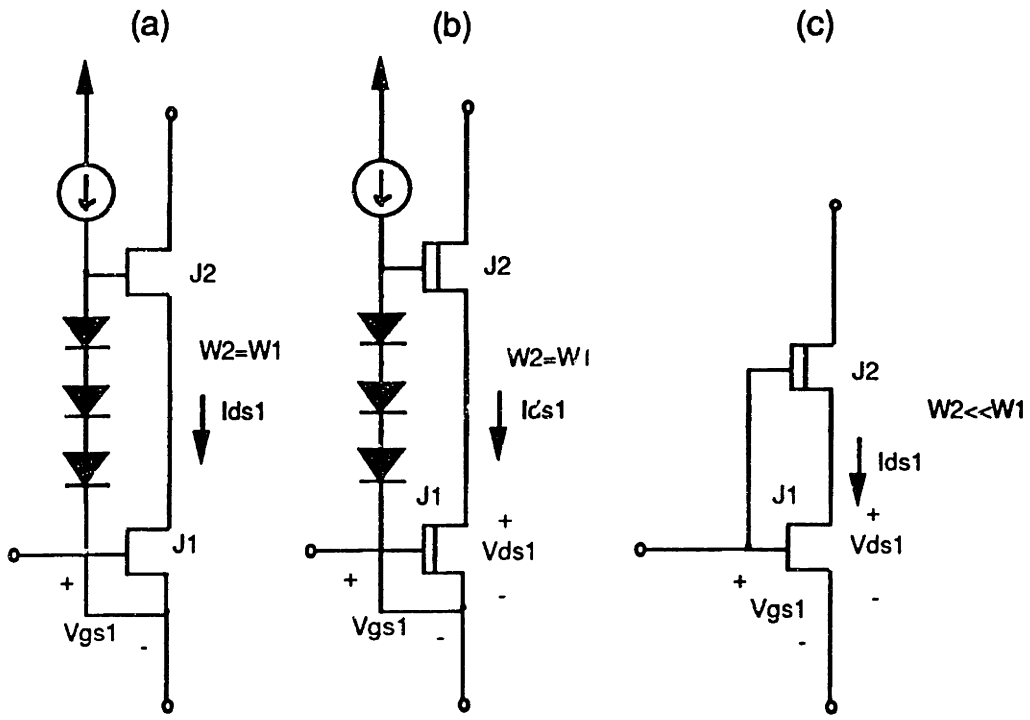

Figure 3.8 - Cascoded transistor topologies: (a) enhancement-mode/enhancement-mode; (b) depletion-mode/depletion-mode; (c) enhancement-mode/depletion-mode.

All of these topologies employ a form of localized negative feedback to reduce the frequency-dependent output conductance. The primary transistor, J_1, operates in saturation with the cascode transistor biased near its high transconductance region to provide the composite transistor with high extrinsic g_m. The third topology couples the gate of the cascode transistor directly to the input gate. For the primary transistor to operate in saturation, its threshold must be higher than the cascode transistor. This can be accomplished by either using a larger device than the cascode or, as is shown, an enhancement-mode transistor as the primary device with a depletion-mode transistor as the cascode transistor. Examining the feedback loop of the last topology, an increase in V_{GS1} causes an increase in I_{DS1}, which is approximately equal to I_{DS2}. This increase in I_{DS2} forces an increase in V_{GS2}, which in turn keeps V_{DS1} constant because V_{G2} equals V_{G1}. The enhancement-mode/depletion-mode cascode has two additional advantages over those in Figures 3.8 (a) and (b). First, it requires no additional current source to bias the

cascode, and, second, the depletion mode device's geometry can be scaled much smaller than an enhancement-mode device sized at the equivalent I_{DSS} current. This minimizes the capacitance at the drain node of the composite transistor. The small-signal-equivalent circuits for the cascode topologies are shown in Figure 3.9.

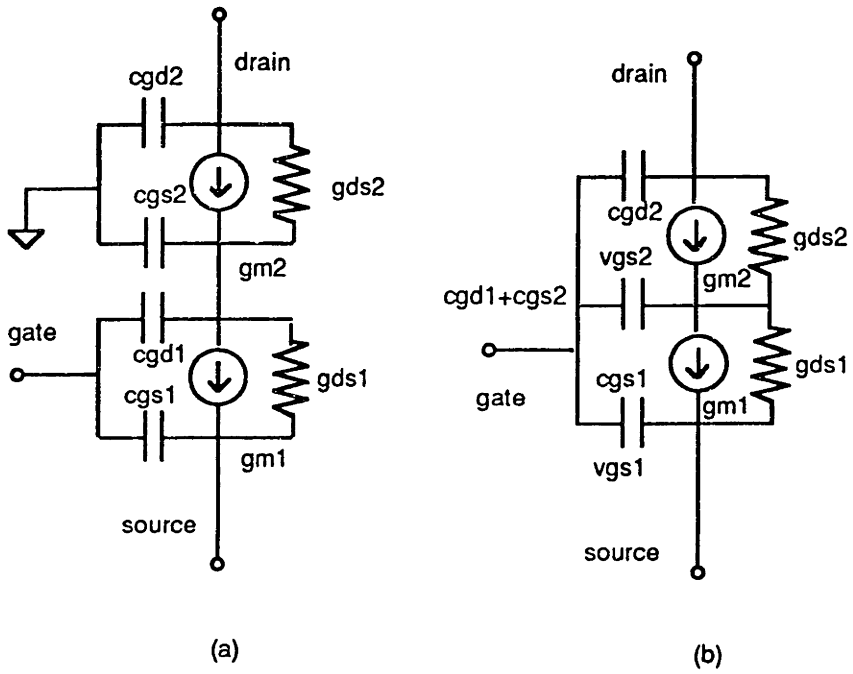

Figure 3.9 - Cascoded transistor small-signal equivalent.

3.2.3 Current Switch

A MESFET source-coupled differential pair driven in a complementary fashion with data pulses having symmetric rise and fall times produces a fast current switch. Depletion-mode transistors are employed in the current-source switch instead of enhancement-mode transistors for two reasons: First, for a given operating current, depletion-mode MESFETs are of smaller geometry, resulting in less parasitic capacitance, and, second, depletion-mode MESFETs produce more output current for a given gate-to-source voltage than enhancement-mode MESFETs, which improves charging of parasitic capacitance and

therefore increases current-switching speed. The simplified MESFET equation for saturation operation is given by:

$$I_{DS} = \beta (V_{GS}-V_T)^2 \qquad 3.2$$

For the source-coupled differential pair composed of transistors J_1 and J_2 and biased at I_o shown in Figure 3.10:

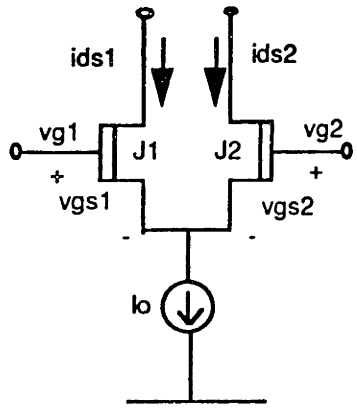

Figure 3.10 Source-coupled differential pair biased at Io.

$$I_o = I_{DS1} + I_{DS2} = \beta_1 (V_{GS1}-V_{T1})^2 + \beta_2 (V_{GS2}-V_{T2})^2 \qquad 3.3$$

and for identical geometry transistors $\beta_1 = \beta_2$ and $V_{T1} = V_{T2}$, which leads to:

$$I_{DS1} = I_o/2 + \beta/2(V_{G1} - V_{G2})[2I_o/\beta - (V_{G1} - V_{G2})^2]^{1/2} \qquad 3.4$$

$$I_{DS2} = I_o/2 - \beta/2(V_{G1} - V_{G2})[2I_o/\beta - (V_{G1} - V_{G2})^2]^{1/2} \qquad 3.5$$

It is important to note that $I_{DS1}$and I_{DS2} are independent of both V_S and V_T and that the differential transconductance, g_{md}, depends only on β and the bias current I_o. For example, for $I_o = 0.25$mA and $\beta = 2$mA/V^2, $g_{md} = 1$mS, enabling all I_o to switch from one side to the other for a differential input voltage of less than 0.5 volts.

In this topology, high-speed operation is achieved if the drain voltage of the on-state transistor is greater than V_{DSsat}, which reduces the gate-to-drain capacitance and the discharging time of the amplifier. The gate-to-drain capacitance is reduced for V_{DS} greater than V_{DSsat} because the gate-to-drain Schottky diode is reverse biased, reducing the

depletion capacitance below the zero-bias-gate-drain capacitance. Insuring that both transistors operate with V_{DS} greater than V_{DSsat}, reduces the discharging time because the discharging current through the switching cycle is dominated by the saturation current instead of the smaller triode current.[7]

Finally, in order to simultaneously achieve high switching speeds at minimum input drive requirements and ease of coupling between input driver and current switch, J1 and J2 are scaled to make I_{DSS} of each transistor equal to $I_O/2$.

In the current-switch layout, a p^+ ohmic guard ring is placed around the differential pair to shield its backgate from other switches' transients and to confine the substrate currents it generates from other differential pairs and the I_O bias current source backgates. Switching transients modulate the backgates of both transistors causing increased glitch energy and phase noise.

3.2.4 Voltage-Level Shift Buffer

The voltage-level shift buffer, shown in Figure 3.11, is composed of a source follower (J_1) driving a current-source (J_2)-loaded diode stack (D_1-D_4) and can be used to provide a voltage-shifted, low-impedance-output-signal form of the input signal. In this topology, the source-follower circuit is essentially a current amplifier of the type frequently used in emitter-coupled-logic circuitry to ensure that desired output-voltage levels are maintained at the output of a logic device.

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[7] S. Katsu et al., "A Source-Coupled-FET-Logic. A New Current Mode Approach to GaAs Logics," *IEEE Transactions on Electron Devices*, Vol. ED-32, No. 6, June 1985.

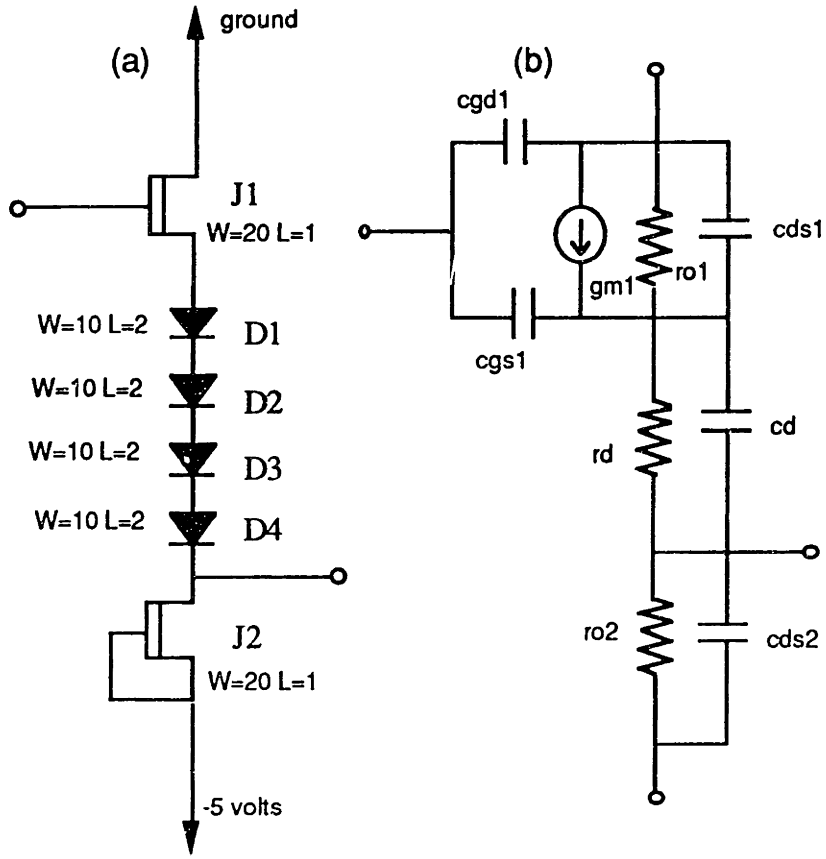

Figure 3.11 - Voltage-level shift buffer: (a) schematic and (b) small-signal equivalent.

The low-impedance output enables the voltage-level shifter buffer to drive the large currents necessary to achieve fast switching times at current switch stage. This is important in overcoming the gate- and parasitic capacitance of the current switch. To achieve near unity gain, the current source must be sized to match the source follower. Mismatches in the follower current source with respect to the follower transistor's current capability results in a variation in the output voltage level. Because $V_{GS} = 0$ of the depletion-mode current source, any variation in the threshold voltage affects the current through the source-follower MESFET by a power of two, which is derived from the simplified saturation current by expression:

$$I_{DS}=ß(V_{GS} - V_T)^2 \qquad 3.6$$

The resistance of the active load is, therefore, highly sensitive to the threshold voltage. The nominal threshold voltage of the depletion-mode device varies considerably due to process

and temperature variations, which are difficult to control. However, adding a source-degeneration resistor can improve control and matching of the current source by forcing a non-zero V_{GS}, which reduces the V_T contribution to I_{DS} as shown by Equation 3.6.

In addition to current source variations due to V_T variations, backgating can significantly influence carrier flow within the channel of a MESFET. By effectively changing the threshold of a device to a value that is different from that of a physically identical neighboring MESFET's, the backgate effect can prevent a device from turning on and force it into "lock up." In the past, because backgating is a function of layout, temperature, and is substrate dependent, the accepted manner for controlling the incidence of backgating has been to maintain sufficient distance between MESFETs that share a common substrate. Unfortunately, this design methodology increases parasitic capacitances through the increase of metal interconnect. Using the p^+ ohmic-ring-isolation technique reduces device crosstalk and increases matching of both identical geometry current sources and source-follower gain. For the voltage-level shift buffer with V_{DS1} biased equal to V_{DS2}, the small signal gain calculated from Figure 3.10 (b) is given by:

$$Av = v_o/v_i = g_{m1}.(r_{o1}||r_d+r_{o2})/[1+g_{m1}.(r_{o1}||r_d+r_{o2})]\ [r_d/(r_d+r_{o2})] \qquad 3.7$$

where $r_{o1}||r_d+r_{o2}$ is the parallel combination of r_{o1} and r_d+r_{o2}. For the geometries delineated in Figure 3.10 (a), Av = 0.9. This implies that an input voltage swing of 1.11 volts is required to produce a desired 1-volt output voltage swing.

The voltage-level shift buffer can sink a maximum current equal to the quiescent current of the current source and source a maximum current equal to the difference between the source follower operating at V_{GS} = 0.65 volts (limited by the forward-biased diode) and the quiescent current of the current source.

Chapter 4

GaAs MESFET Mixed-Mode Process and Design Test Structures

Simple test structures were designed to extract performance of the process enhancements and design methodology. The HSPICE model was compared with S-parameter test structure data to ensure that linear circuits could be accurately simulated. The S-parameter data was measured with a Cascade Microtech probe station.

No measurement data existed on the effect of p^+ contact rings isolation on the frequency-dependent output conductance. Experiments were run to determine the relationship between substrate-biasing hysteresis, gate delay, and frequency-dependent output conductance. An analytical model was developed to explain the experimental results.

Finally, circuit techniques were investigated including the use of cascode and self-bootstrap circuit topologies to reduce the frequency-dependent output conductance, which enabled development of high-performance analog and mixed-mode circuit in a digital GaAs MESFET process.

4.1 Diffused Resistors

In order to make high-performance analog circuits in a digital GaAs MESFET process, circuit techniques are employed that extract precision performance from basic process technology. Diffused resistors are the only choice for the resistor for the digital-to-analog converter in this technology. The problem with diffused resistors is that they have a poor reputation for use in precision applications. Among the chief disadvantages of

diffused resistors are that they have a high temperature coefficient (approximately 1500 ppm/°C), and they are pressure sensitive and have a high voltage coefficient, which means that they are nonlinear with applied voltage. Further, they are not trimmable, and by reputation they match poorly.[1]

However, diffused resistors do have advantages. They are built in the standard GaAs MESFET process, so they are simple and compatible with the high-volume manufacturing techniques. They are also inherently stable because they are diffused at a very high temperature. They are not altered by trimming, which would disturb long-term stability. Diffused resistors track tightly with temperature since they are fabricated simultaneously, in close proximity and also in the same material. Finally, diffused resistors require no burn-in to achieve stability. The key to producing uniform diffused resistors is to pay careful attention to layout. Both common centroid layout and averaging layout techniques must be employed to achieve high relative precision.[2] Table 4.1 summarizes diffused resistor characteristics.

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[1] D. Hodges, "Analog Switches and Passive Elements in MOS LSI," in *Analog MOS Integrated Circuits*, IEEE, 1980.

[2] C. G. Conroy et al., "Statistical Design Techniques for D/A Converters," *IEEE Journal of Solid State Circuits*, Vol. 24, August 1989.

Table 4.1 Diffused Resistor Characteristics[3]

Advantages	Disadvantages
• Part of standard Vitesse GaAs process	• High temperature coefficient
• Simple and compatible	• Pressure sensitive voltage coefficient
• Stable--thermally oxidized	• High voltage coefficient
• Single crystal material	• Not trimmable
• Contact resistance tracking	• Poor absolute tolerance
• Tight temperature tracking	
• No burn-in requirement	
• Match as well as thin film	

Several resistor arrays were designed to measure resistor matching and statistical properties of the Vitesse digital GaAs MESFET process. The nominal sheet resistance of the n^+ diffused resistors is 200 ohms/square.[4] As shown in Figure 4.1, the discrete resistor values were designed as 800 ohms (20 x 80 μm geometry) with binary fractions designed as multiple copies of identical resistors in parallel or series. Assuming the resistor values are functions of statistically independent random variables, including doping concentration and ohmic contact resistance, then the effective relative accuracy can be increased by employing multiple copies of these identical resistors in parallel or series to design a weighted-resistor array.

Adding in series n copies of gaussian distributed resistor elements of mean value μ_r and standard deviation σ_r increases the mean value μ_n to $n \cdot \mu r$, while σ_n only increases to $n^{1/2} \cdot \sigma_r$. For matched resistors composed of n identical resistor copies in parallel, the

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[3] J. A. Schoeff, "An Inherently Monotonic 12-bit DAC," *IEEE Journal of Solid State Circuits*, Vol. SC-14, No. 6, December 1979.

[4] *Vitesse Foundry Manual*, Version 4.0, 1991.

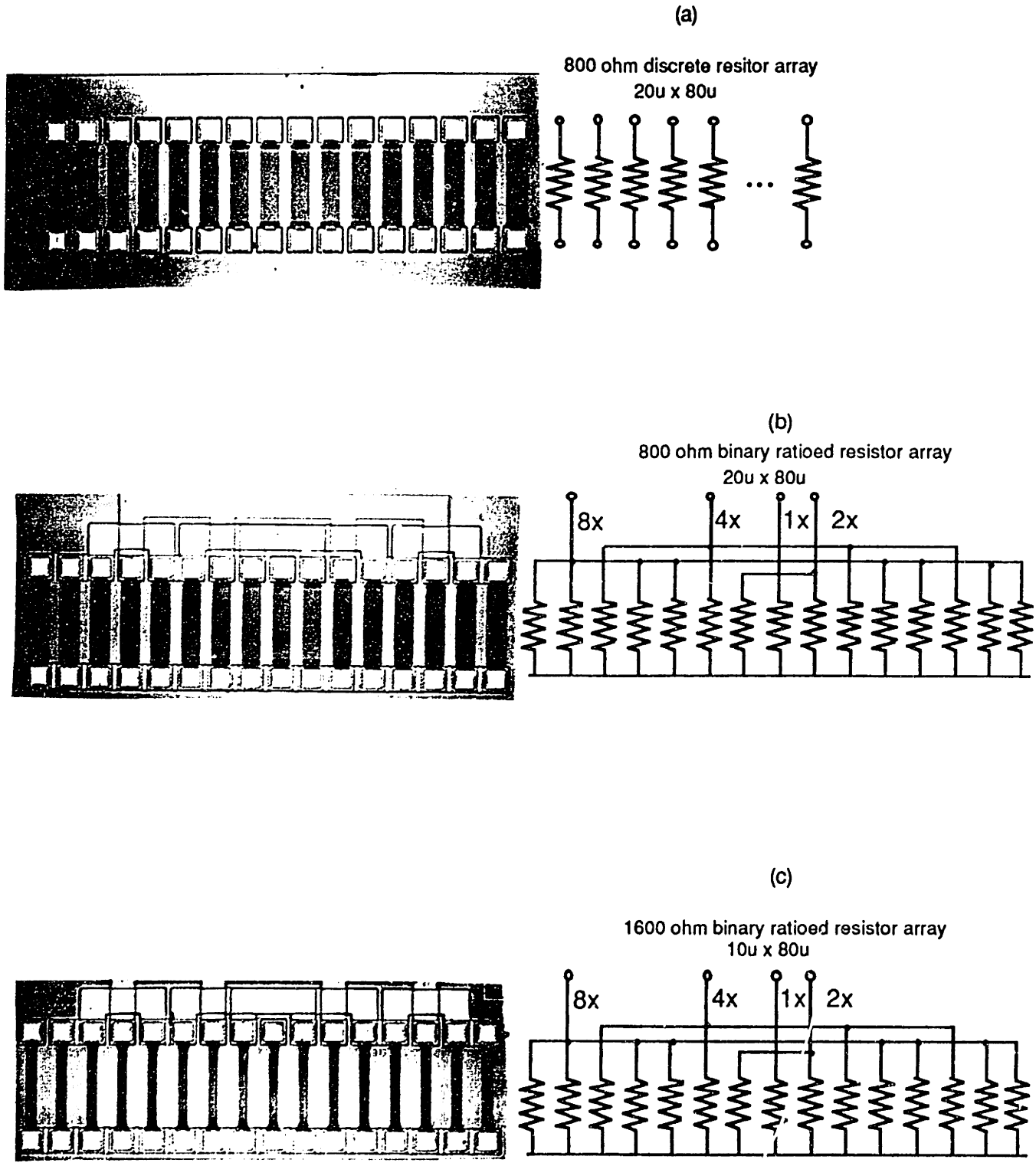


Figure 4.1 - Resistor arrays: (a) discrete 800 ohm; (b) binary ratio 800; 400, 200, 100; (c) binary ratio 1600, 800, 400, 200.

relative matching ratio between resistors is improved by the same ratio $n/n^{1/2}$. This statistical averaging technique can be extended to any semiconductor parameter that is gaussian distributed. Also, the central limit theory can extend this averaging technique to non gaussian distributed processes. In fact, transistors composed of n identical copies in parallel I_{DS} matching improves by the same $n/n^{1/2}$ ratio. This is described in section 4.2 and 4.3. Good matching performance of resistor values and transistor I_{DS} are key process attributes and are a requirement for a high resolution digital-to-analog converter designs. As such, both discrete resistor arrays and binary ratioed resistor arrays were designed as test structures. The transistor array structures are described in section 4.2 and 4.3.

The 800 ohm resistor array test structure showed local matching of 0.5%. This is five times worse than that of diffusion resistors in a conventional NMOS process. It is was an unexpected result. The resistors at the end of the array match considerably poorer than those in the middle flanked by identical surrounding components. This measured data trend shows the value of inserting dummy components on the ends of the array. This procedure was followed in the design of the current sources of the digital to analog converter described in Chapter 5.

Similar statistical measurements were made of the binary ratioed resistor array test structure. Both centroided and non-centroided array structures were measured. Large gradients (2%) were observed in the non-centroided structures. The gradients observed in the asymmetric resistor array point out the need to employ common centroiding to eliminate this effect.

4.2 Single Transistor Devices

The discrete devices were composed of four different MESFETs: 80 μm x 1.0 μm depletion-mode, 20 μm x 1.0 μm depletion-mode, 80 μm x 1.0 μm enhancement-mode, and 20 μm x 1.0 μm enhancement-mode transistors made up of identical paralleled 10 μm x 1.0 μm devices. The four devices were tested on each of 35 reticles of a 4 inch wafer. Each MESFET had a p^+ ring isolation implant connected to ground as shown in Figure 4.2.

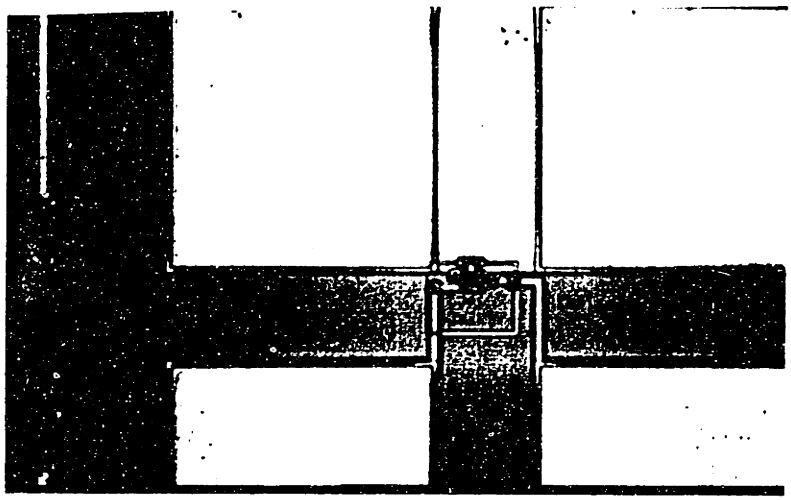


Figure 4.2 - Discrete 20 μm x 1.0μm depletion-mode transistor with p^+ ohmic ring isolation.

Table 4.2 statistics are derived from all 35 reticles. The reticles that contributed the majority of the statistical outliers were the fifteen on or near the edge of the wafer. In Table 4.3, data from these reticles has been omitted. The standard deviations are noticeably improved but at the cost of assuming a 40% reduction in yield. The 80 μm devices match noticeably better than the 20 μm devices but not by a factor of 2 as predicted by gaussian statistics described in section 4.1.

Table 4.2 - Single Transistor Threshold Measurement Statistics on 35 Reticles

Device	Mean V_T	Std Dev
80 μm x 1.0 μm depletion-mode	-1.125V	242 mV
20 μm x 1.0 μm depletion-mode	-1.072V	177 mV
80 μm x 1.0 μm enhancement-mode	+0.120V	81 mV
20 μm x 1.0 μm enhancement-mode	+0.143V	59 mV

Table 4.3 - Single Transistor Threshold Measurement Statistics on 35 Reticles with Outliers Removed

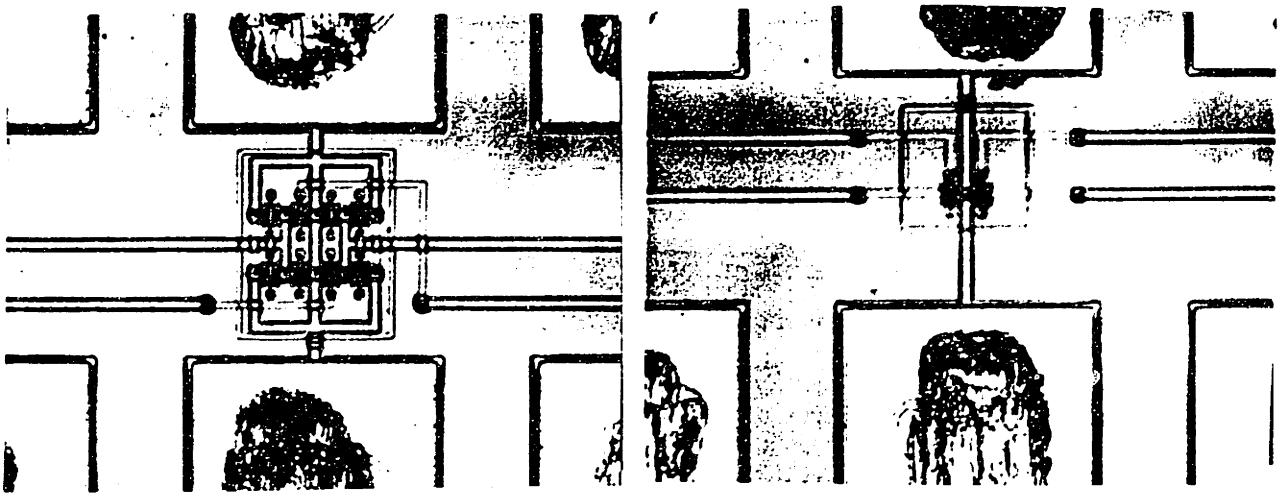
Device	Mean V_T	Std Dev
80 μm x 1.0 μm depletion-mode	-1.145V	87 mV
20 μm x 1.0 μm depletion-mode	-1.063V	102 mV
80 μm x 1.0 μm enhancement-mode	+0.127V	38 mV
20 μm x 1.0 μm enhancement-mode	+0.163V	55 mV

The raw measurement data on which the statistics were based show concentric gradients in which the center of the wafer exhibits a higher threshold for both the depletion and enhancement mode devices. This pattern is probably the result of a photo-resist radial-thickness gradient caused by a spin-on process step. It is important to note that for a specific reticle site, even with this concentric gradient, the 20 μm and 80 μm devices match much better locally than the overall wafer statistics. This is confirmed in the next section where differential pairs composed of common centroided transistors have differential voltages that match better than 10 mV.

4.3 Differential Transistor Pairs

In addition to discrete devices, common centroided differential pair test structures enclosed in a single p^+ ohmic guard ring were measured. The four MESFET differential pairs were composed of: 40 μm x 1.0 μm depletion-mode, 10 μm x 1.0 μm depletion-mode, 40 μm x 1.0 μm enhancement-mode, and 10 μm x 1.0 μm enhancement-mode

transistors. The 40 μm x 1.0 μm transistors were made up of identical paralleled 10 μm x 1.0μm devices. Each differential pair was enclosed by a p^+ ohmic ring connected to the common source shown in Figure 4.3



(a) (b)

Figure 4.3 - Differential pairs with p^+ ohmic ring isolation: (a) 40 μm x 1.0μm depletion-mode and (b) 10 μm x 1.0μm depletion-mode.

Table 4.4 statistics are derived from all 35 reticles. The reticles that contributed the majority of the statistical outliers were the 15 on or near the edge of the wafer. The 40 μm devices match noticeably better than the 10 μm devices by approximately a factor of two, as predicted by gaussian statistics described in section 4.1. The improved local matching is significant because it determines the minimum offset voltage of comparators and operational amplifiers that use differential input stages.

Table 4.4 - Differential Transistor Pair Threshold Measurement Statistics on 35 reticles

Differential pair	Mean V_T difference	Std Dev
40 μm x 1.0 μm depletion-mode	15.8 mV	11.1 mV
10 μm x 1.0 μm depletion-mode	27.5 mV	23.8 mV
40 μm x 1.0 μm enhancement-mode	6.8 mV	4.8 mV
10 μm x 1.0 μm enhancement-mode	14.9 mV	17.3 mV

4.4 Dual Gate MESFET

A dual-gate MESFET contains a second gate inserted between the gate and drain of a single-gate structure. The second gate provides two principal advantages over a single gate device: 1) gain control of the primary transistor and 2) modulation of the primary transistor. This makes this structure particularly well suited to input-amplifier-gain-control and mixer applications. A 200 μm x 1.0 μm dual gate MESFET test structure was designed with a surrounding p^+ ohmic ring bulk bias and a n^+ ohmic guard ring and is shown in Figure 4.4.

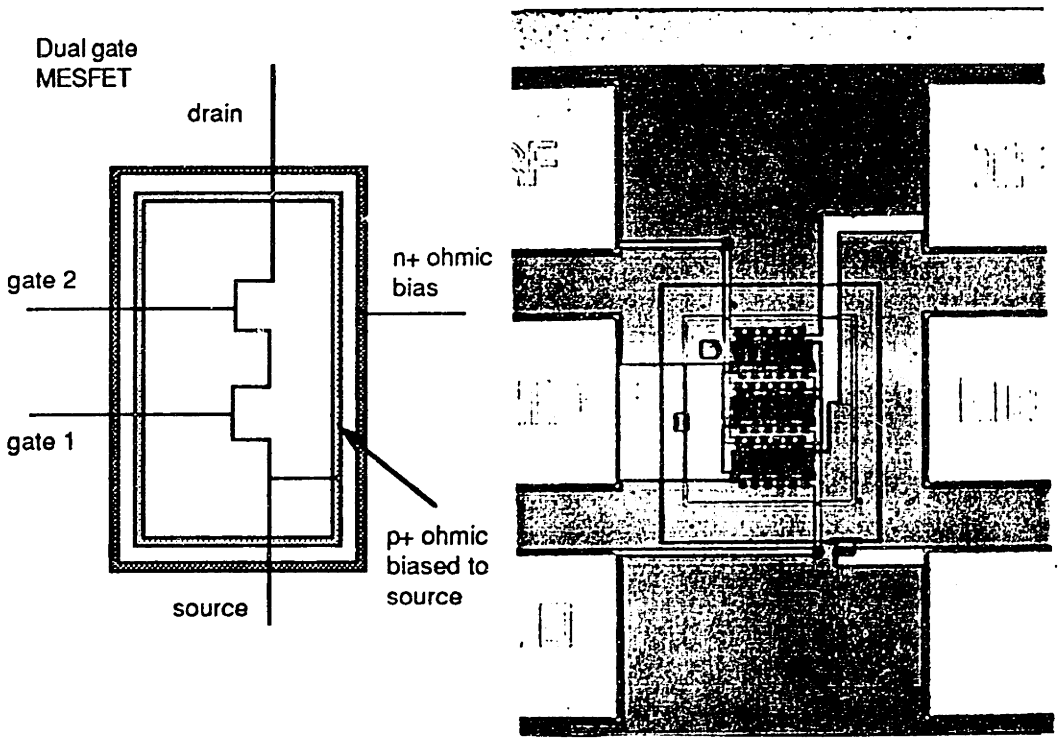


Figure 4.4 - Dual gate MESFET with p^+ ohmic ring bulk bias and n^+ guard ring isolation.

The operation of the dual-gate MESFET depends on the operating characteristics of each MESFET, specifically the voltages V_{D1S1}, V_{D2S2}, V_{G2D1}, and V_{G1S1}, but the actual applied signal voltages consist of V_{D2S1}, V_{G1S1}, and V_{G2S1}. The internal and external voltage relationships are given by:

$$V_{D2S1} = V_{D1S1} + V_{D2S2} \quad 4.1$$

$$V_{G2D1} = V_{G2S1} - V_{D1S1} \quad 4.2$$

The exact operation condition of this circuit is difficult to characterize because the internal voltage at D1 cannot be measured. However, if the I-V characteristics of each MESFET are plotted together on a single graph, the operating point can be inferred. Figure 4.5 shows a simulation of the overlapping of each MESFET I-V characteristic for a constant V_{DS}. The corresponding dual-gate drain currents are found at the intersection of the two MESFET curves because the drain currents are equal when both MESFETs are biased in the linear or saturation regions.

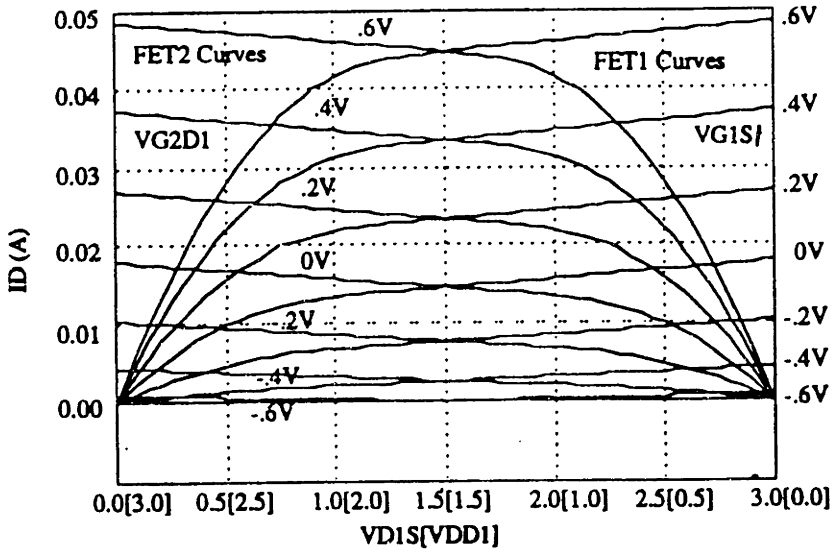


Figure 4.5 - I-V characteristics of J_1 and J_2.

The curves of Figure 4.5 are not physically measurable. A clearer method is shown in Figure 4.6 in which Figure 4.5 is overlaid with constant V_{G2S1} curves. This results in individual operating points of J_1 and J_2 as a function of applied voltage. The measured test structure performance confirmed HSPICE simulations of the device with both J_1 and J_2 bulk potential biased at V_{S1}. Prior to this experiment, there was some speculation that J_2's bulk would float higher than J_1's bulk. This did not occur; the p^+ ohmic bias pinned the bulk voltage to the source of J_1.

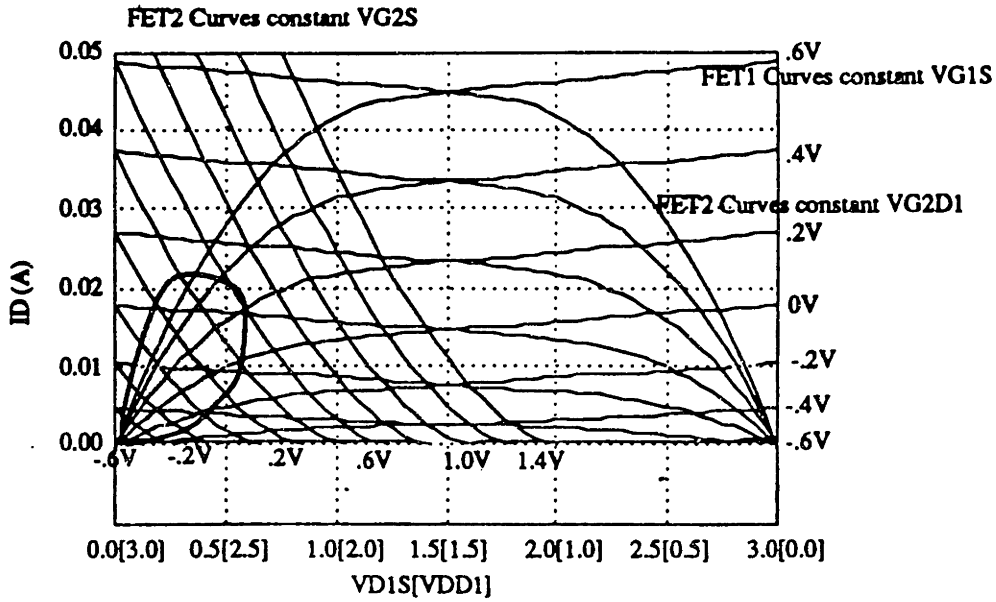


Figure 4.6 - I-V characteristics of J_1 and J_2 with $V_{bulk1} = V_{bulk2} = V_{S1}$.

4.5 High-Impedance Current Source

A high-impedance current source was designed as a source-degenerated cascode circuit. The circuit, shown in Figure 4.7 (a), is composed of a source-degenerated enhancement mode primary transistor cascoded with a depletion mode transistor whose gate is connected to the gate of the enhancement mode transistor. The small-signal equivalent circuit, shown in Figure 4.7 (b), leads to an output resistance given by:

$$R_o \cong (g_{m2}.r_{o2})(g_{m1}.r_{o1}).R_S \qquad 4.3$$

where g_{m1} and g_{m2} are the transconductances of J_1 and J_2, r_{o1} and r_{o2} are the output resistance's of J_1 and J_2, and R_S is the source degeneration resistor.

This current source topology has good voltage swing and simple cascode biasing and can be accurately biased in a closed-loop feedback network, shown in Figure 4.7 (c). In this topology, the amplifier drives the enhancement mode source voltage to the applied reference. This increases the output resistance by the gain of the amplifier, a, and is given by:

$$R_o \cong a(g_{m2}.r_{o2})(g_{m1}.r_{o1}).R_S \qquad 4.4$$

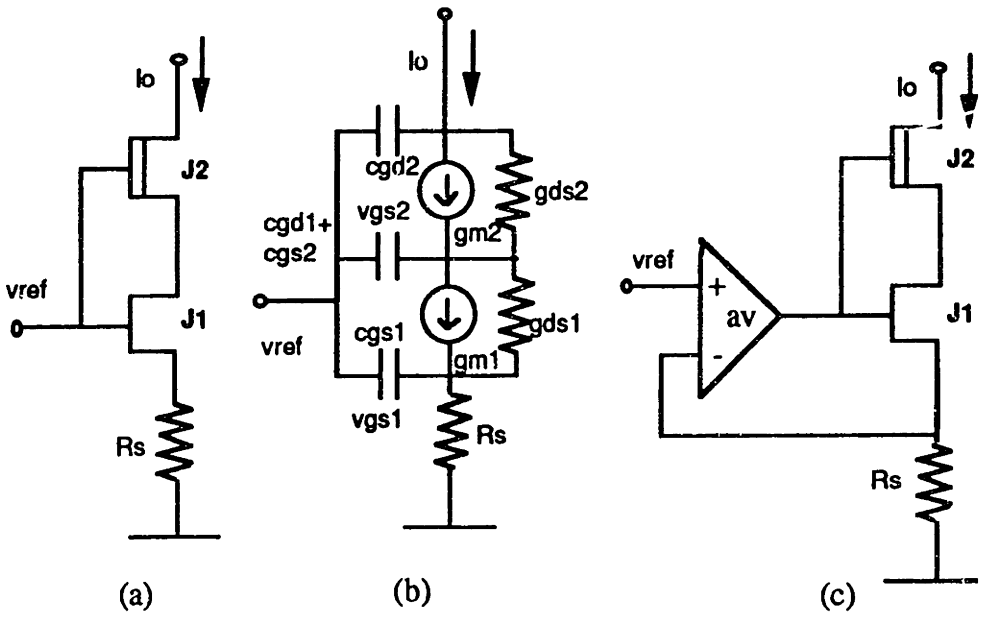


Figure 4.7 - (a) source-degenerated cascode current source schematic;
(b) source-degenerated cascode current source small signal equivalent circuit;
(c) active source-degenerated cascode current source schematic.

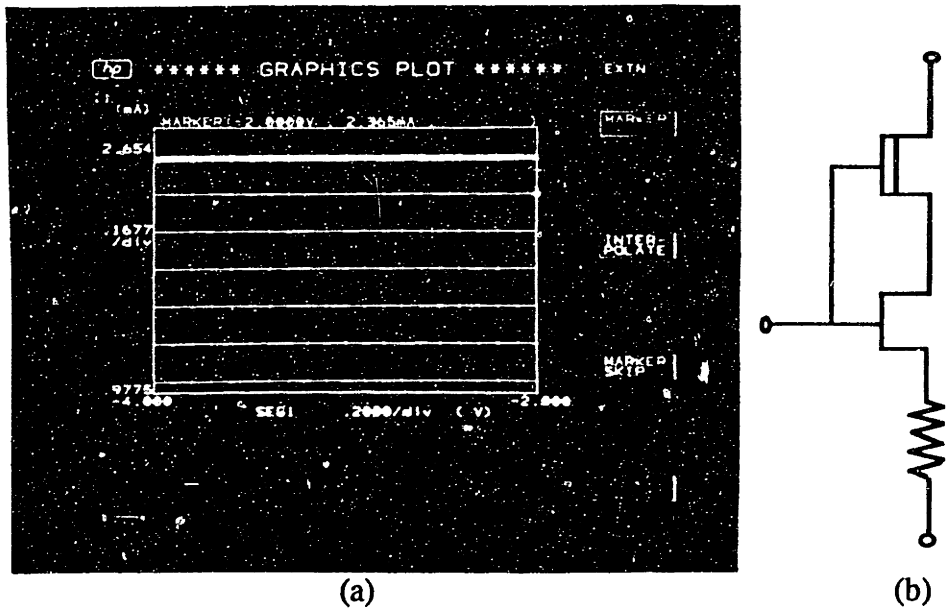
An array of eight of these current sources was designed, fabricated, and tested to develop a statistical process data base from which system performance of digital-to-analog converter designs could be predicted. Table 4.5 shows both the mean, and maximum percent deviation for 10 test reticles arranged in 2 rows of 5 in the center of a four-inch wafer. Each reticle contains 8 identical source-degenerated cascode current sources. It is important to note that the measured performance of the 12-bit digital-to-analog converter based on the source-degenerated cascode current sources topology yielded less than 0.1% variation. The large difference between the monolithic performance and the discrete performance is probably due to the differences of the surrounding substrate during each measurement. During the operation of the integrated converter all current sources are biased at the same potential. This was not possible during the discrete current source measurement due to a limited number of bias probes. Here the surrounding current sources were left floating while a measurement was taken on a single current source.

Table 4.5 Source-Degenerated Cascode Current Source Measurement Statistics

reticle	% variation of I	μ_I
1	1.07	1.859
2	2.13	1.873
3	2.09	2.006
4	1.26	2.218
5	0.29	2.338
6	0.86	1.852
7	0.62	1.941
8	1.03	2.042
9	0.72	2.222
10	0.46	2.369

note all current values in mA

To achieve 12-bit performance in an upper 3-bit segmented digital-to-analog converter architecture, assuming a full scale current of 20 mA, these eight current sources must match to better than 1 part in 512 (2^9), or less than 0.2% matching variation. The above data indicates that for this current-source topology to achieve 12-bit performance, an upper 4-bit segmented digital-to-analog converter architecture, which requires relative matching of 0.4%, should be used instead of the 3-bit segmented digital-to-analog converter architecture. Figure 4.8 shows the measured dc-output impedance of the current source to greater than 2×10^6 ohms, the resolution of an HP 4145 semiconductor parameter analyzer. This high impedance insures that switching transients of a current source differential pair biased by this current source will not modulate the current output.



(a) (b)

Figure 4.8 - (a) source-degenerated cascode current source dc output impedance > 2 x 10^6 ohms and (b) source-degenerated cascode current source schematic.

4.6 Split-Current-Source Loads

A split-load test structure composed of three cascoded MESFETs was designed to determine substrate bias voltages between and under large MESFETs. The structure, shown in Figure 4.9, was also used to measure substrate currents between isolated p^+ regions. Prior to development of this test structure, there was speculation that the bulk under large transistors (>200 μm) would rise to the source potential of the device. This theory suggested that large transistors spaced several ten's of microns apart would not suffer backgate effects. The test results indicate that to some extent this is true. However, the use of a p^+ ohmic-ring bulk bias within a n^+ ohmic-contact guard ring that encompasses the individual transistors is more effective. Designs using the latter methodology could place device active areas within 5 μm of each other, while non-isolated designs required greater than 70 μm spacing to achieve V_{BS} of -100 mV.

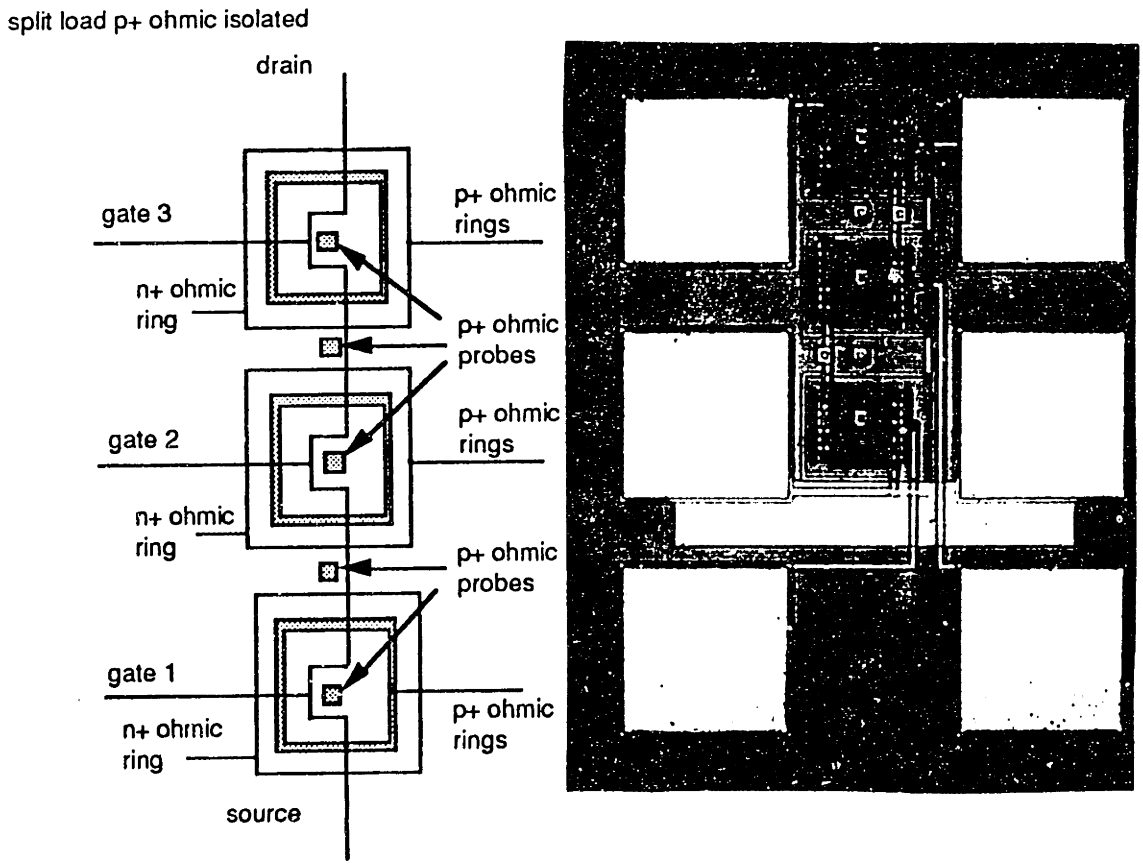


Figure 4.9 - Split load test structure composed of three cascoded MESFETs.

4.7 Unity Gain Buffer

A bootstrapped unity gain buffer was designed to measure performance of the p^+ ohmic process. Gain dispersion, due to the MESFET frequency-dependent output conductance, will degrade the accuracy of the buffer. Since the low frequency intrinsic gain of the MESFET is greater than its high-frequency gain, the step response will exhibit that of a lag network. This slow transient introduces an effective gain variation. The design technique applied to this problem was first suggested by Poulton,[5] who employed a bootstrap-source-follower topology that forced the drain of the primary transistor (J1) to follow its source. The bootstrap buffer circuit and layout is shown in Figure 4.10.

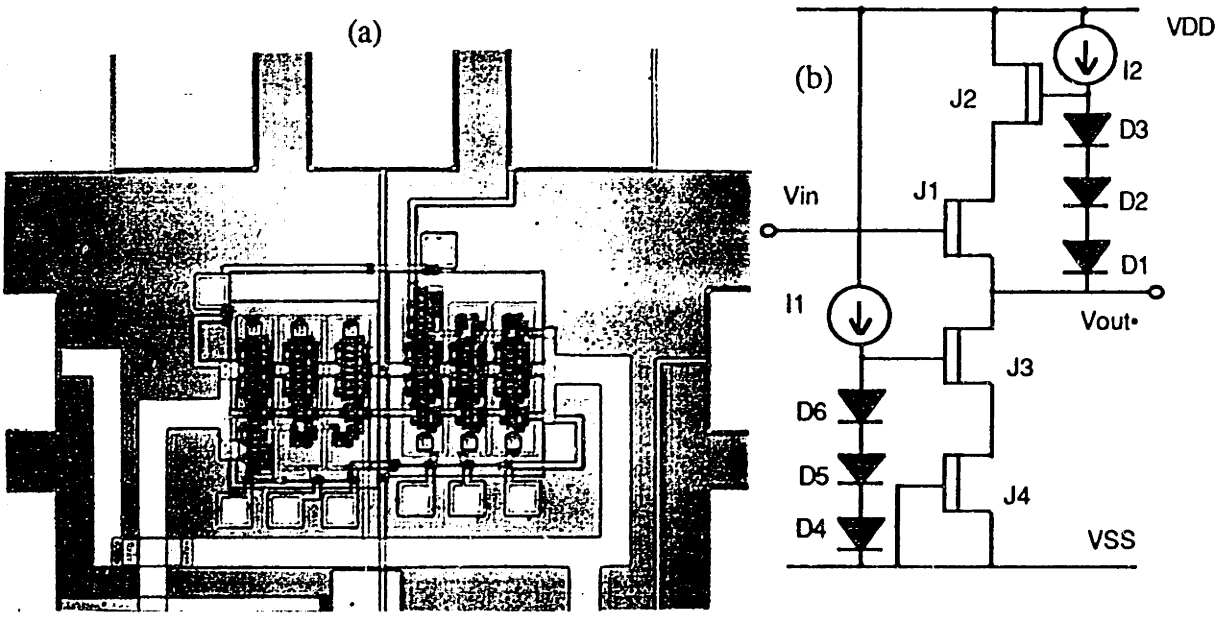


Figure 4.10 - Bootstrapped unity gain buffer (a) layout and (b) circuit.

The simulated transfer characteristics of this topology, with and without p+ contact bulk isolation, is shown in Figure 4.11. The ac magnitude and phase responses of the isolated bulk devices exhibit higher bandwidth and lower gain dispersion.

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[5] K. Poulton et al. "A 1GHz 6-Bit ADC System," *IEEE Journal of Solid State Circuits*, Vol. SC-22, No. 6, December 1987.

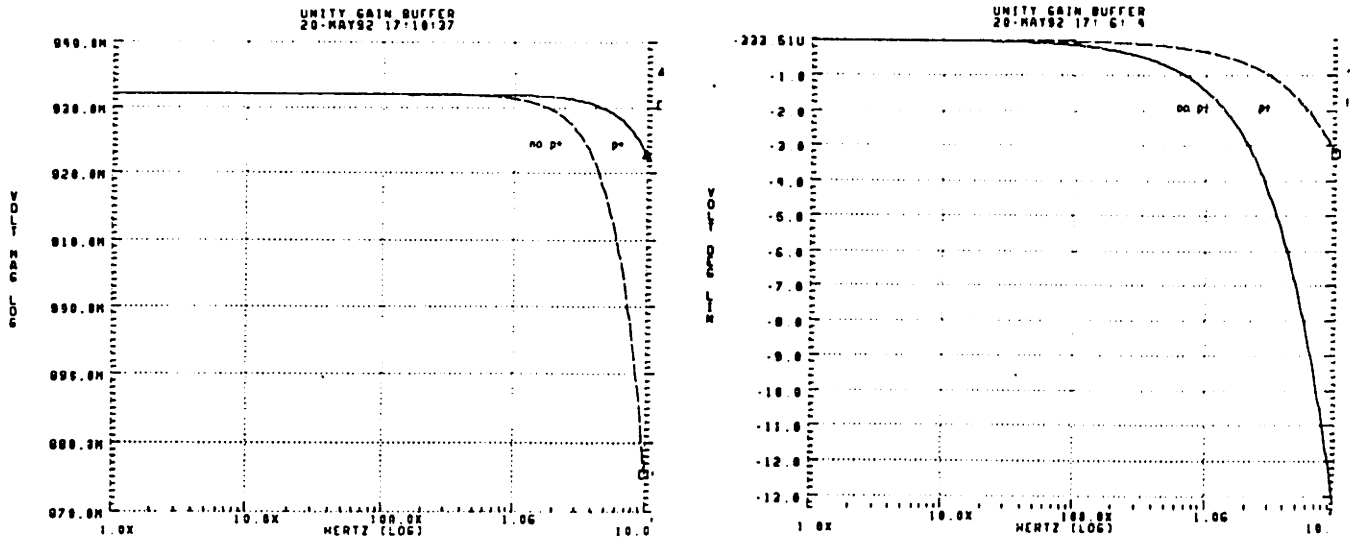

Figure 4.11 - Bootstrapped unity gain buffer (a) magnitude response and (b) phase response with and without p^+ contact isolation.

4.8 Ring Oscillator

Two ring-oscillator test circuits were designed: one with a biased p^+ ohmic contact and an isolated bulk and the other with a non-isolated floating bulk. The ring oscillators were composed of seven DCFL inverter stages, each with ß = 10.4. The ring oscillators were used to characterize p^+ ohmic isolation process ac performance including switching speed and spurious response. Figure 4.12 shows the seven-stage DCFL ring oscillator used for tests. The oscillator's output is fed into an output driver that provides current gain and DCFL-to-ECL level shifting, enabling the oscillator to drive a 50 ohm load at frequencies up to 1.5 GHz. On three of the wafers, one-third of the ring oscillator circuits were built using a p^+ implant to isolate the circuit from the rest of the substrate and the rest of the wafer. Figures 4.13 shows the time-domain transient simulation of two stages of a ring oscillator without p^+ isolation output and the stages associated charge pumping of the substrate. Figure 4.14 is a blow up of the high voltage level output of the ring oscillator. Evident is the phase modulation due to the substrate cross talk. This time-domain phase modulation shows up as spurious response in the frequency domain and increases oscillator noise. This same noise mechanism is present in digital dividers and analog comparators. Therefore any process that reduces this noise effect is desirable.

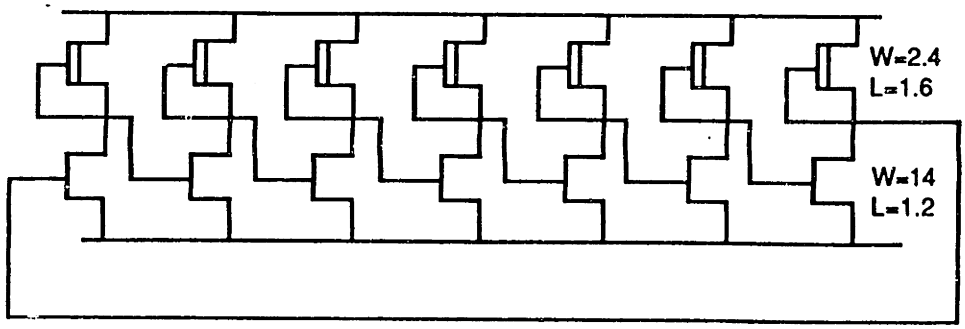

Figure 4.12 - Ring oscillator.

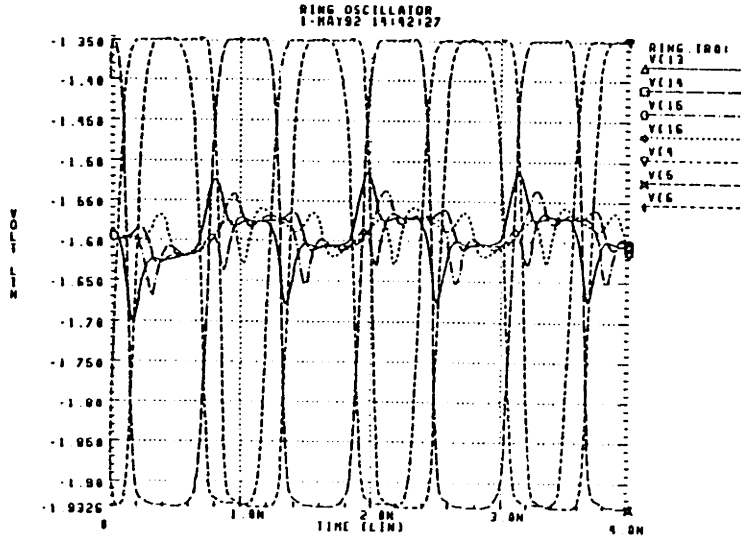

Figure 4.13 - Transient simulation of two stages of the ring oscillator without p^+ ohmic ring isolation showing outputs and bulk charge pumping.

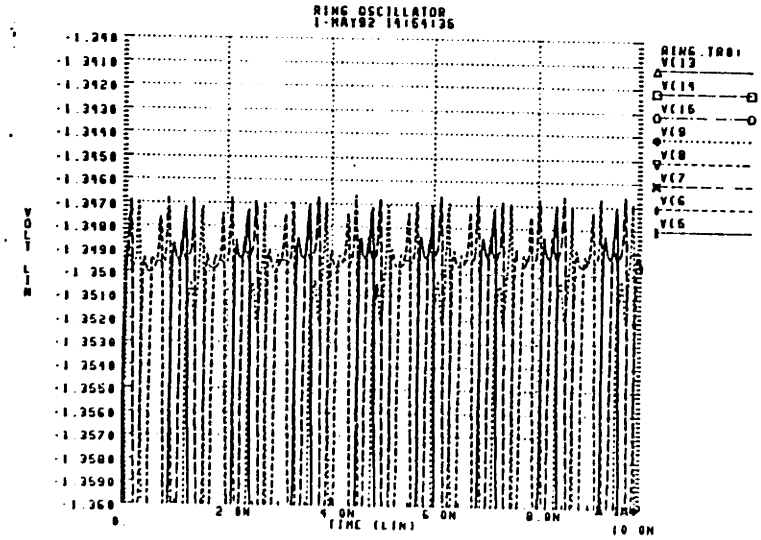

Figure 4.14 - Enlargement of transient simulation of Figure 4.13 showing phase modulation of high logic level output.

The ring oscillator circuits were tested and compared on an RF microwave probe station using the configuration shown in Figure 4.15. The first step was to compare the performance of the circuits with and without the p^+ ohmic contact. Fifteen circuits on the same wafer were tested and compared. It was found that the oscillators with the p^+ ohmic contact provided an additional 30 dB of close-in sideband noise suppression as compared to those without the p^+ ohmic contact. Figures 4.16 and 4.17 show this difference between a typical oscillator with the p^+ ohmic contact and one without. Additional ring oscillators were tested and characterized. The three wafers with the p^+ ohmic contact circuits were compared to the two wafers without; the results were found to be consistent--the oscillators with p^+ ohmic contact consistently had better close-in noise performance than those without bulk bias and isolation.

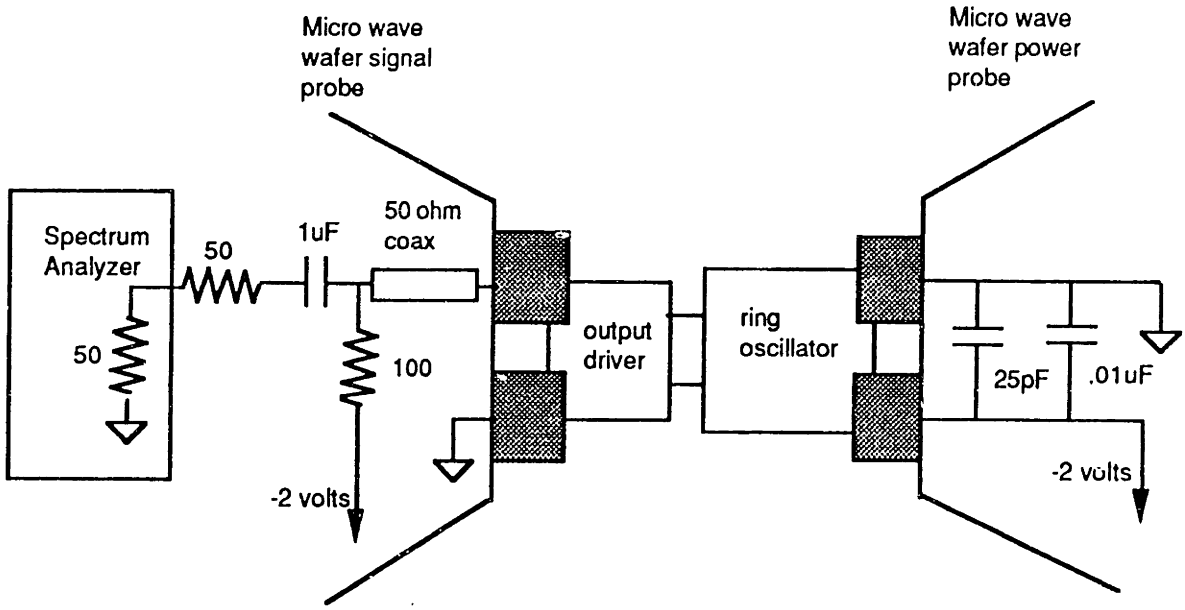

Figure 4.15 - Ring oscillator ac probe test configuration.

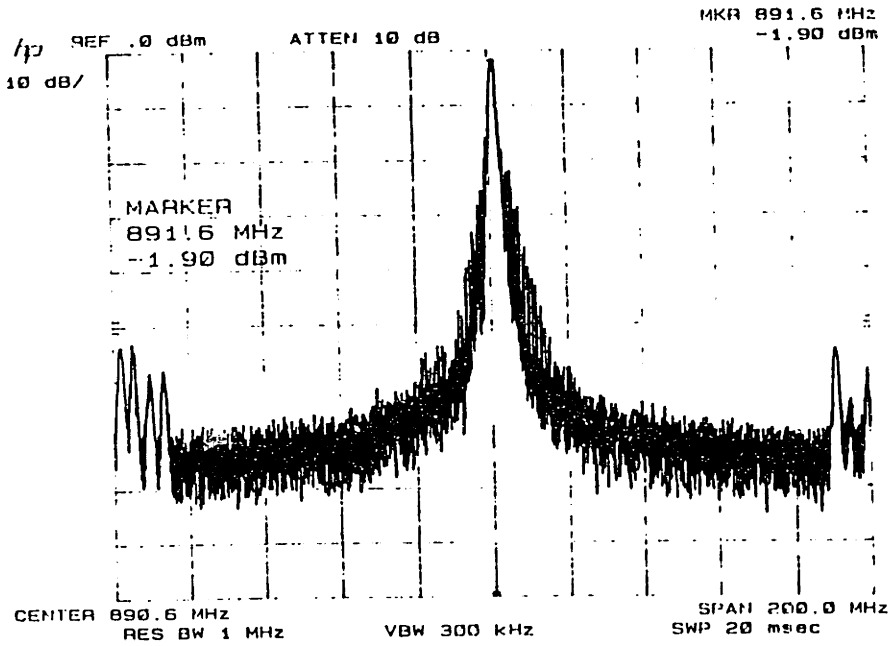

Figure 4.16 - Ring oscillator ac performance without p+ ohmic ring isolation.

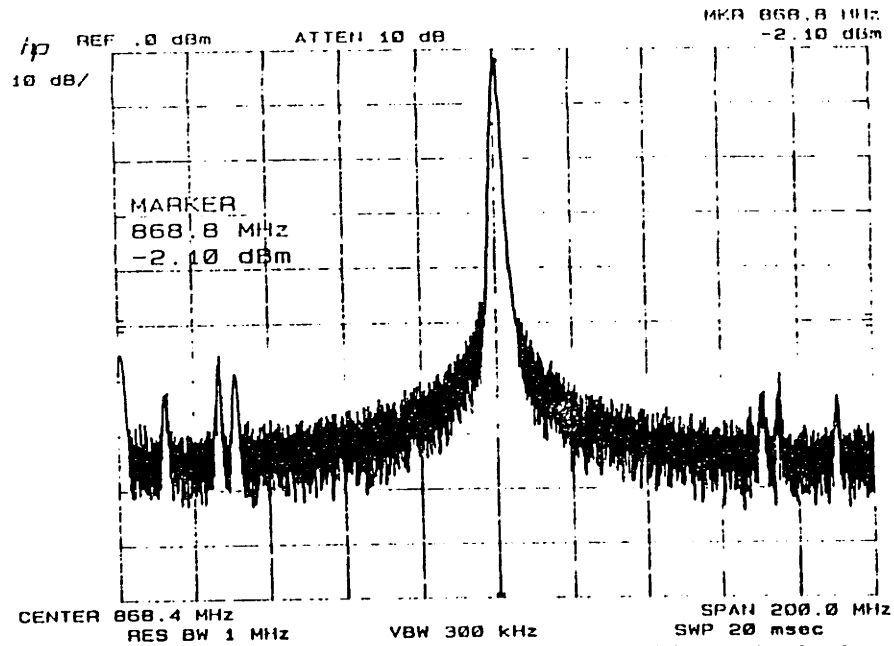

Figure 4.17 - Ring oscillator ac probe test performance with p+ ohmic ring isolation.

The next investigation that was conducted was to test the speeds of the ring oscillator circuits in an attempt to see if there was any correlation between the circuit's location on the wafer and its speed of performance. All five wafers were examined in this test. Every third circuit was tested, and its speed was noted. Thus, the oscillators that were built with the ohmic contact were the only ones tested on the three wafers where they were included. This facilitated both an examination of the speed distribution across a single wafer and a comparison between the oscillators with and without the implant.

The results consistently showed that the circuits along the edge of the wafer were the fastest and that the speeds decrease somewhat parabolically as the middle of the wafer was approached.

Figures 4.18 and 4.19 show a three-dimensional graph of the speed of the ring oscillators as a function of their position on the wafer.

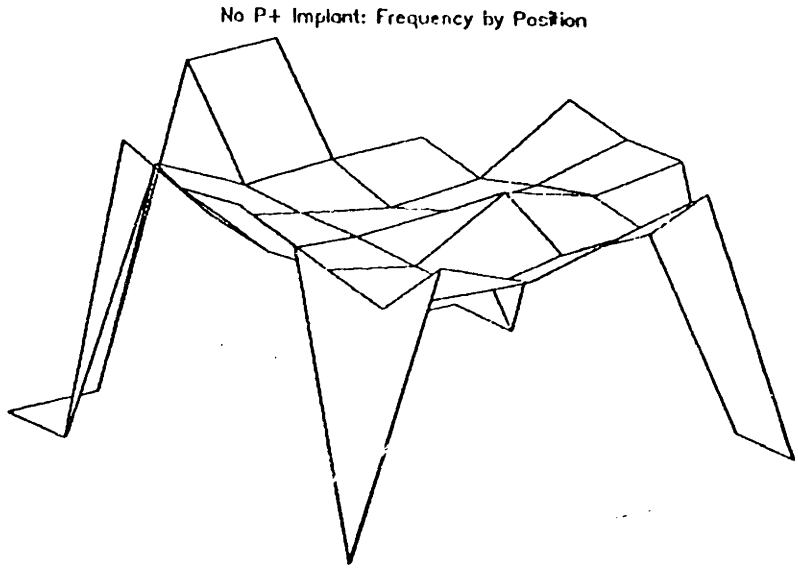

Figure 4.18 - Ring oscillator frequency as a function of position without p^+ ohmic ring isolation.

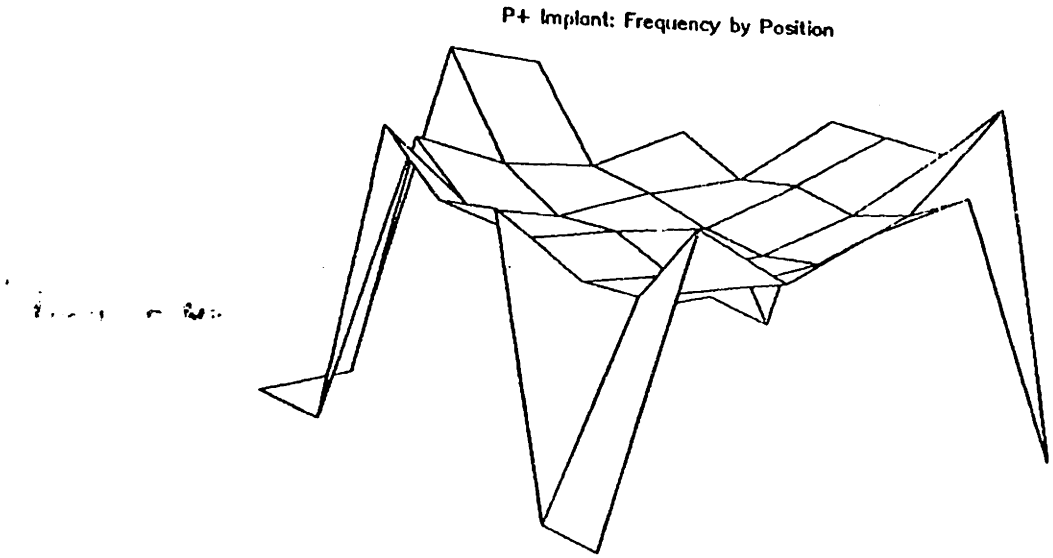

Figure 4.19 - Ring oscillator frequency as a function of position with p^+ ohmic ring isolation.

To facilitate display of the same data on a two-dimensional graph, the averaged data was normalized to show frequency as a function of radial distance from the center of the wafer. The resulting graph is shown in Figure 4.20. Note the parabolic upward trend as the distance increases.

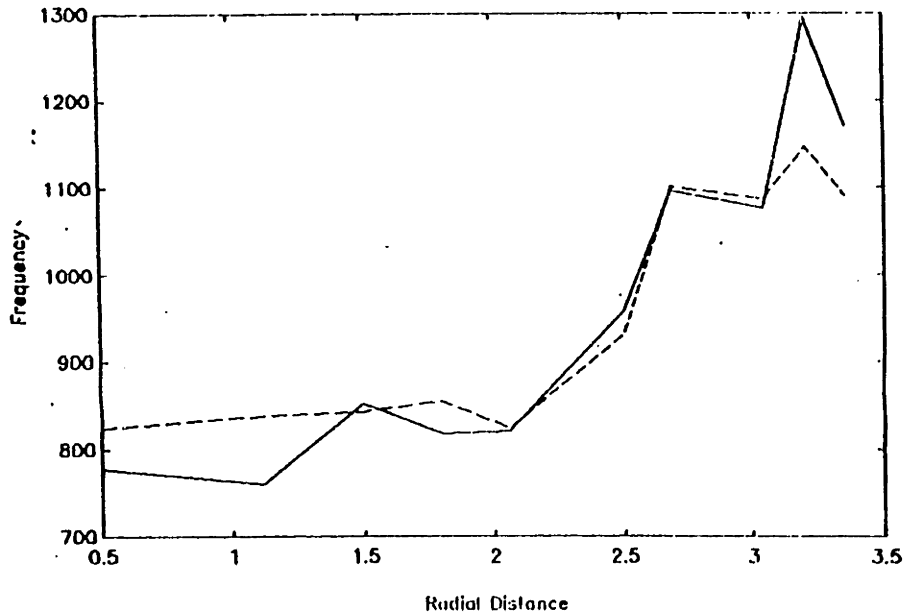

Figure 4.20 - Ring oscillator frequency as a function of radial distance.

This graph also provides a comparison of the speeds of the oscillators with p^+ implants to those without. As the graph shows, the speeds of the two different types of circuits are very similar. The average speed of the oscillators with the implant was 920 MHz, with a standard deviation of 187.4 MHz; without the implant, the mean was 931.3 MHz, with a standard deviation of 169.1 MHz. The difference in average speed between the p^+ implant and non-p^+ implant is too small to have any statistical significance.

This investigation of the performance of a ring oscillator circuit shows that the p^+ ohmic-bulk-isolation processing step improves close-in sideband noise performance by 30 dB while having no appreciable effect on the speed of the circuit. Additionally, it was found that the speed of the circuits on a Vitesse wafer appear to be radially distributed such that the fastest circuits are found on the edges of the wafer and the slowest are found towards the middle. For maximum yield, the speed distribution should be uniform across the wafer.

Chapter 5

500 MHz 12-bit GaAs MESFET Digital-to-Analog Converter

5.1 Design Goals

The design goals of this digital-to-analog converter are summarized in Table 5.1. The prime design goal is to make the converter component tolerant and inherently monotonic yielding 0.025 percent performance with 0.1 percent matching of components over commercial temperature range of 0° C to 70° C. The second most important goal is for the design to be monolithic and require no trimming of component values to achieve the 12-bit accuracy. The third most important goal is to use only standard ECL supplies of ground, -2 volts, and -5.2 volts to minimize power and circuit complexity.

5.2 Architecture Overview

The design of current-output 12-bit digital-to-analog converters have traditionally required precision thin film resistors and laser trimming methods to achieve the required precise binarily weighted current source array. The currents are derived from either an R-2R ladder network or a segmented ladder in most high-speed, high-resolution converters to provide monotenicity and differential linearity. Recently, converters using dynamic element matching have been put forth to increase resolution of the binary scaled currents. However, these topologies require high supply voltage rails and external passive low pass filters. The dynamic range of the current source array can be extended by dividing the most

Table 5.1 Design Goals for the Digital-to-Analog Converter

- Differential current type architecture capable of driving 50 and 25 ohm loads
- 12 bit differential linearity
- Ground, -5.2 volt and -2 volt supply voltage
- Less than 2 watt power dissipation
- Integrated 2:1 data multiplexer
- ECL-level input interface
- Inherently monotonic .025 percent matching performance with 0.1 percent matching components over full temperature range.
- No laser trimming or dynamic error correction
- No special thin film resistor technology
- Integrated voltage reference and op amp
- GaAs MESFET enhancement/depletion digital process technology

significant current bits into smaller segments and adding these to produce binary ratioed current source outputs. The performance of each of these architectures is examined in the following sections. The final 12-bit architecture developed for this converter is a unique synthesis of many of the features of prior art.

5.2.1 R-2R Topology

The dominant design approach used in most digital-to-analog converters is the R-2R ladder. This requires precise resistor tracking to maintain monotenicity. For the 12-bit specifications, it is desirable to have all 4,096 converter output levels separate and distinct. This requires resistor and transistor component matching to 0.025 percent. The

conventional converter consists of 12 binary current sources that are used in all possible binary combinations to produce 4,096 analog output levels.

The main advantage of the R-2R technique is that it uses a minimum number of components. The most critical resistor in the circuit is the most significant bit resistor. This resistor must match to within 0.0125 percent, which must also be maintained over the entire operating range. Clearly, the 0.1 percent resistor matching data presented in Chapter 4 does not support a 12-bit R-2R current source topology.

5.2.2 Segmented 2^NR Topology

The segmented 2^NR approach[1] requires fewer resistors, and initial resistor matching can be of the order of 0.1 percent for a 12-bit design. The accuracy requirements of the R-2R approach are relaxed by a factor of two for each doubling of the number of segments. For example, a 12-bit digital-to-analog converter design in which the top three bits are segmented reduces the resistor matching requirements by a factor of eight (2^3) enabling a 12-bit accuracy with 0.1 percent resistor component matching.

The key to the inherent monotenicity of the segmented approach can be seen by examining the major carry transition (0111...to 1000...). Rather than switching in an entirely different current source at the major carry as an R-2R converter does, the current from the segment prior to the major carry is retained, and the current to create additional steps is added to it in the form of increments of the bit below the carry. Thus, the converter is monotonic regardless of the relative slopes of the eight most significant current segments. The only critical resistor matching occurs at the major carries or other points of the eight segments, and the tolerances are equivalent to those of a 9-bit digital-to-analog converter, or *eight* times lower than an equivalent R-2R approach. In essence, the segmented architecture has broken the problem into eight separate problems, each with tolerances eight times lower than those of a 12-bit R-2R digital-to-analog converter.

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[1] S. Urquhart, "A 12-bit Monolithic 70 ns DAC," *IEEE Journal of Solid State Circuits*, Vol. SC-18, No. 3, June 1983.

The segmentation generation for the three most significant bits reduces the resistance matching and tracking requirements so that diffused resistors are adequate. However, the approach does incur the overhead of a decode segment that has to do a priority encode--taking three bits and turn on the appropriate number of identical current sources up to seven--but it does reduce the resistor tolerance required for the most significant bit by a factor of eight.

5.2.3 Multiple Current Source Array Topology

The segmented architecture can be improved by adding *averaging* techniques used in layout.[2] This converter architecture is physically divided into two main current source arrays: an MSB array and an LSB array. The MSB contains the three significant bits like the segmented approach with the lower bit array broken into a master-slave array.[3] Both of the arrays use redundancy and multiple current source approach. The key method put forth includes redundancy where errors are spread between multiple copies of identical current sources. Dynamic matching errors are averaged out in time. This architecture can be fabricated in a standard digital process containing only diffused resistors.

5.2.4 Dynamic Element Matching Topology

Dynamic element matching has been described by Van de Plassche,[4] and using this concept he realized a 14-bit converter in bipolar technology. Dynamic element current source matching time division multiplexes a single reference current source between an array of switches. The dc filtered output of these switches is simply the time-weighted duty cycle average of the switches' pulse train. Clocks referenced from crystals produce stable, precisely ratioed duty cycles. These clocks in turn can drive counters whose outputs can be designed to be binary ratios. Dynamic element matched current source

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[2] K. C. Hsich et al, "A 12-bit 1-Gword/s GaAs Digital-to-Analog Converter System," *IEEE Journal of Solid State Circuits*, Vol. XC-22, No. 6, December 1987.
[3] G.S. LaRue, "A GaAs Digital-to-Analog Converter," *IEEE GaAs IC Symposium Technical Digest*, 1983
[4] Van de Plassche, "A Monolithic 14-bit A/D Converter," *IEEE Journal of Solid State Circuits*, Vol. SC-17, December 1982.

topologies can therefore attain performance of the order of 14 bits. The problem is that each duty- cycle modulated current source requires low pass filtering that must attenuate clock switch ripple to the desired resolution. To date, this has been accomplished with external RC low pass filters because of the extremely low cut off frequency required for high resolution. Capacitors on the order of hundreds of nano farads with resistors on the order of kilo ohms are required to filter clock frequencies of 10 MHz for 12-bit performance, which prohibits monolithic design.

5.3 12-bit Multiplexed Current Digital-to-Analog Converter Architecture

For the 12-bit GaAs MESFET digital-to-analog converter, the segmentation approach has been adopted and modified into a multiple current source techniques. The converter is physically divided into two main current source arrays: an MSB array and an LSB array. This approach is shown in the system block diagram of Figure 5.1. The MSB contains the three significant bits, and the LSB is broken into a master-slave array. The segmentation generation for the three most significant bits reduces the resistance matching and tracking requirements so that diffused resistors are adequate. An on-chip operational amplifier provides closed-loop reference tracking. Video Blank and Sync signals are inputs enabling use of the digital-to-analog converter in high-resolution video applications. The low spurious response and glitch impulse characteristics of this design make it appropriate for high-fidelity waveform generation and direct-digital frequency synthesizers.

The digital-to-analog converter was designed as a fully monolithic component packaged in a high-performance 52-pin ceramic LDCC. The device sinks up to 40.96 mA through 50Ω, both on chip and off chip, yielding 1.024 volts. The 12-bit digital-to-analog converter was designed for high-performance applications such as high-resolution graphics, direct-digital synthesis, and arbitrary waveform generation. Multiplexed inputs enable data to be latched into the digital-to-analog converter at a 250-MHz data rate while maintaining a high 500-MHz output rate. The digital-to-analog converter was designed for high ac linearity applications. Due to current segmentation circuitry, which minimizes

glitch impulse to 25 pV-s, the device is capable of at least -56 dBc total signal-to-noise ratio. The signal-to-noise ratio specification includes all harmonic distortions but excludes aliased components that are filtered out in typical applications. The digital-to-analog converter selects 12-bit ECL-level inputs at up to a 1-GHz rate and produces true and complementary proportional current outputs (1LSB=10μA) that settle within 1ns.

The architecture shown in the functional block diagram of Figure 5.1 is composed of a digital section consisting of input receivers, multiplexers, registers, segment decoders, a flip-flop, and a clock driver. An analog MSB current source array, LSB current source array, differential current switches, and an operational amplifier comprise the analog section. In data bus *A (DA0-DA11)* and *B (DB0-DB11)*, high-speed ECL level signals are input into two sets of 12 parallel receivers that convert the ECL signal levels to internal logic levels, which then drive a 12-bit wide, 2-to-1 bus selection multiplexer.

The outputs of the multiplexer are determined from the polarity of the *Select A/B In* signal. A high logic level on *Select A/B In* produces A-bus data on the output of the multiplexer, while a low logic level selects B-bus data. The *Select A/B In* data is clocked through a flip-flop to produce *Select A/B Out* and *Select A/B Out*. *Select A/B Out* drives the multiplexer, while *Select A/B Out* is driven off-chip to provide a data synchronization signal. For automatic alternating, bus selection *Select A/B Out* can be connected to *Select A/B In* with a 50 ohm termination resistor tied to V_{TT}. In this configuration, the clock input is divided by two to provide alternating "ping-pong" data bus selection.

The multiplexer outputs drive MSB and LSB symmetric master-slave latches. The outputs of the MSB register are decoded into a 3-to-8 thermometer segment decoder to steer current to *I Out*, *I Out complement*, or the LSB current source array. The approach incurs the overhead of a priority encoder, taking three bits and switching in the appropriate number of identical current sources (up to seven). However, it has the advantage of reducing the resistor tolerance required for the most significant bit by a factor of eight as

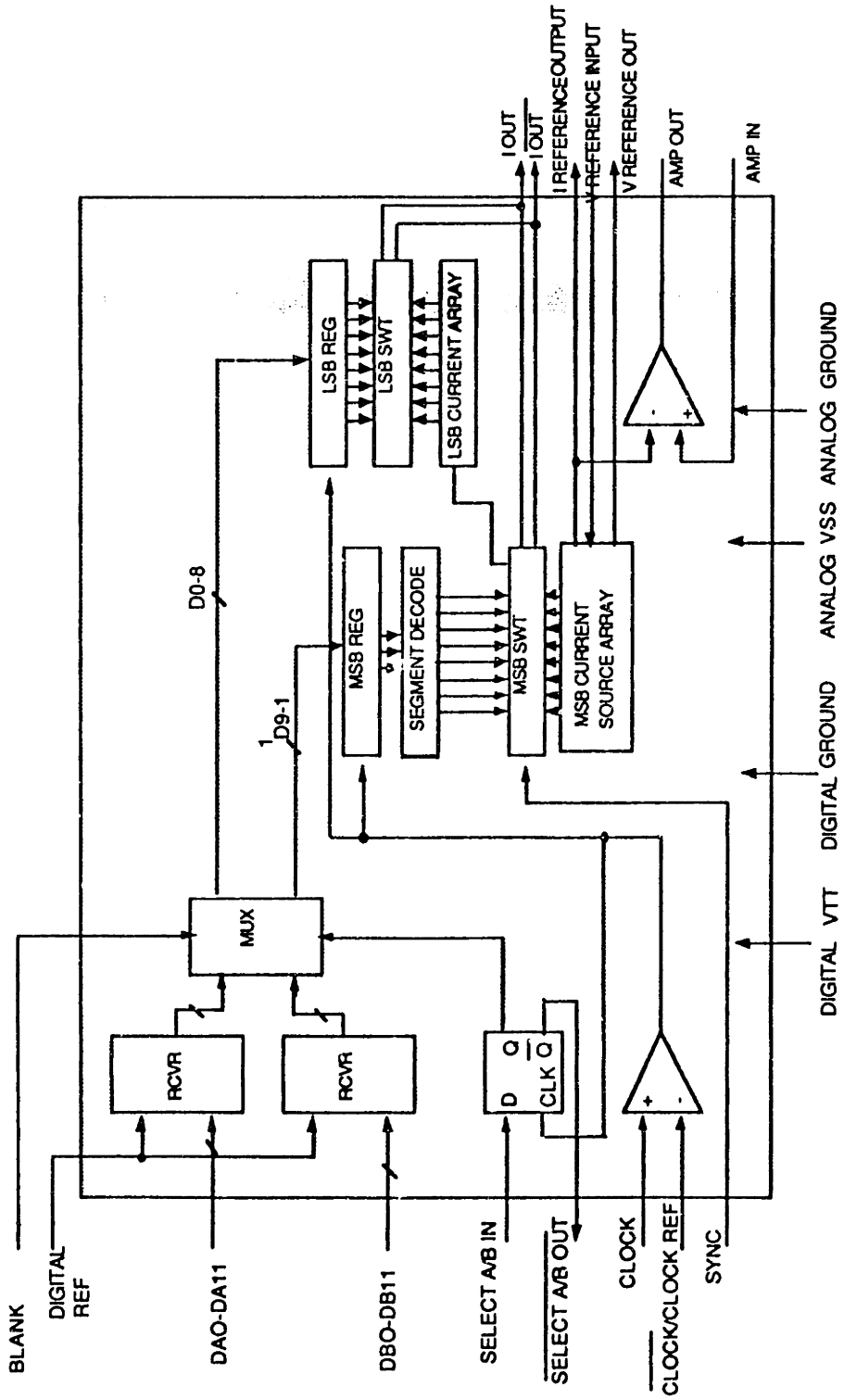

Figure 5.1 - Digital-to-analog converter functional block diagram.

well as reducing the maximum glitch impulse by a factor of four. Because the LSB currents are derived by splitting successive selected MSB segment currents, the architecture is inherently monotonic and capable of low glitch transients.

The outputs of the LSB register directly drive LSB current switch drivers. The switch drivers are scaled proportional to the current switch to equalize the fan out and minimize glitch energy. These current switches are connected to the composite segmented and binarily weighted current source arrays. The outputs of the MSB and LSB switches are tied together to form *I Out* and *I Out complement*, are reverse-terminated to 50 ohms on-chip, and require 50 ohm termination off-chip.

5.4 Circuits

5.4.1 Input Receiver

The differential input receiver, shown in Figure 5.2, is composed of a differential pair with current source biasing followed by complementary source followers, level shifters, and current mirror. An external reference signal, nominally -1.3 volts, is passed through a resistor divider on-chip to generate an internal ECL reference. This signal drives the complementary FET of the differential pair. The level-shifted signal drives into a symmetric output buffer. The design of the receiver output buffer implementation maintains symmetry through a cross-coupled push-pull complementary level FET logic (CLFL) topology.[5] This drives the input of the master-slave latch, still biased at directed coupled DCFL levels. The receiver has been simulated to run in excess of 1.2 GHz. The receiver operates off a 2-volt rail (V_{TT}=-2 volt to V_{CC}=0) to minimize power. The design has an ECL-compatible interface[6] accepting a -.8 volt high level to a -1.8 low level with a reference voltage of -1.3 volts.

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[5] M. Passlack et al., "Theoretical Evaluation of a Novel Design for digital GaAs ICs," *IEEE Journal of Solid State Circuits*, No. 5, October 1988, p. 1249-1256.
[6] Motorola, Inc., *Motorola MECL System Design Handbook*, 2nd edition, 1983.

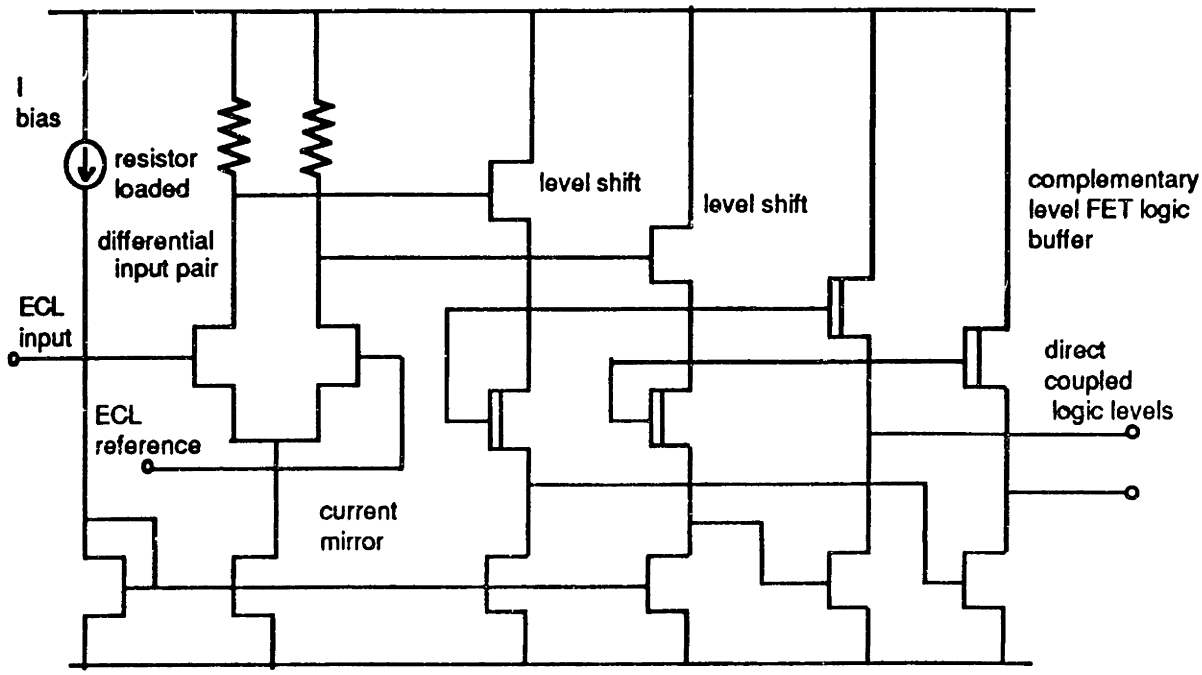

Figure 5.2 - ECL input receiver.

5.4.2 Multiplexer

Each input receiver drives a 2-1 multiplexer latch. This on-chip multiplexer placed after the ECL receivers makes it possible to obtain the full conversion rate by interleaving two half-speed (half-clock) input data streams applied to the A-word and B-word inputs. This is an important test feature because current RAM access times for moderate-density RAMs (4kx4) are 5 nsec, which would force circuit applications to provide three levels of off-chip multiplexing: 125, 250, and 500 MHz to achieve continuous 500 MHz operation. The 500 MHz multiplexer rate is difficult to achieve on a glass epoxy printed circuit board. The on-chip input multiplexer relaxes this requirement to only 2 levels of on-chip multiplexing at 125 and 250 MHz rates.

5.4.3 DCFL Pass Transistor Latch

Each multiplexer output drives a master-slave latch. This latch is a symmetric differential design based on pass transistor technology and functions similar to P 1 cells.

The latch contains two identical stages: two pass transistors drive into cross-coupled inverters to provide the basic latching function. When the pass transistor is on, the signal flows through and drives the cross-coupled inverters. When the pass transistor is off, the inverters regenerate the edge and hold the value. To increase the speed of this latch, parallel inverter cells without the feedback resistors on them are incorporated to drive the next pass transistor stage. The master-slave latch operates on the same 2-volt rail as the input receivers to minimize power.

The slave latch pass transistor stage drives into a buffer CLFL stage that is ratioed and scaled to drive the binarily ratioed current switch drivers. The set of switch drivers are similarly scaled to drive the switches that are binarily ratioed from 160 μm switches to 20 μm switches. No switch smaller than 20 μm is allowed because the switch amplitude of the small switches in quite minimal anyhow and matching characteristics are better for larger geometry devices.[7] The buffer stage prior to the switch is used to help equalize the fan outs and ensure all switches transition at the same time (i.e., within 20 psec). By ensuring that all switches transition at the same time, the total glitch impulse, which is a direct result of the short-lived transient code combinations, is ensured to be as small as possible. The symmetric master-slave latches employed reduces and minimizes the skew of all control switching signals to minimize the glitch impulse. These latches have the added advantage of a mechanism for synchronizing all digital-to-analog converter transitions with the master clock. The differential linearity of the switch drive is important to minimize the clock skew and therefore the glitch impulse. The worst glitch energy is simulated to be less than 30 psec-volts, which occurs at the most significant bit major carry transition. Biasing all of the input receivers and RAM latches, as well as switch drivers, from the -2 volts-to-0 power supply voltages decouples the current source array from the digitally induced switching transients and ensures minimum clock feedthrough to the

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[7] F. Weiss, "A 1 Gs/s 8-bit GaAs DAC with On-Chip Current Sources." *IEEE Journal of Solid State Circuits*, Vol. SC-22, No. 6, December 1986.

current sources. In simulating all the transitions from the input receiver cell through the latches to the switch drivers and, finally, current switch, all parasitic capacitances and resistances were included and modeled within the simulation environment.

5.4.4 Current Source Array

The current source architecture contains a segmented approach employing eight identical current sources for the three most significant bits. The next nine bits are composed of a master-slave current source array. The 9-bit digital-to-analog converter and the segmented converter uses a master-slave ladder arrangement, whereby the top four most significant bits are generated by a weighted cascode LSB generated from the binary-weighted MSB array. The remaining five LSBs are split by active current splitting into their appropriate weights. The advantage of this architecture is that it allows the middle four MSBs to be cascoded as well as the final five LSBs. This is coupled with the three most significant bits, which are matched using a segmented approach. In review of the current source, the 12-bit digital-to-analog convert actually incorporates three philosophies:

1. Active current scaling in the slave network for the five LSBs where accuracy may be traded for area savings.
2. Binary ratioed current division of the master ladder where up to nine bits accuracy is required, taking advantage of the precision diffused resistors and averaging plus common centroid layout affects using multiple copies.
3. Segment generation for the three most significant bits where resistor matching and tracking of diffused resistors would not be adequate.

Figure 5.3 shows the schematic of the MSB and LSB current source array and switches. Detailed schematics of the MSB segments and LSB current splitting circuits are shown in Figure 5.4 and 5.5.

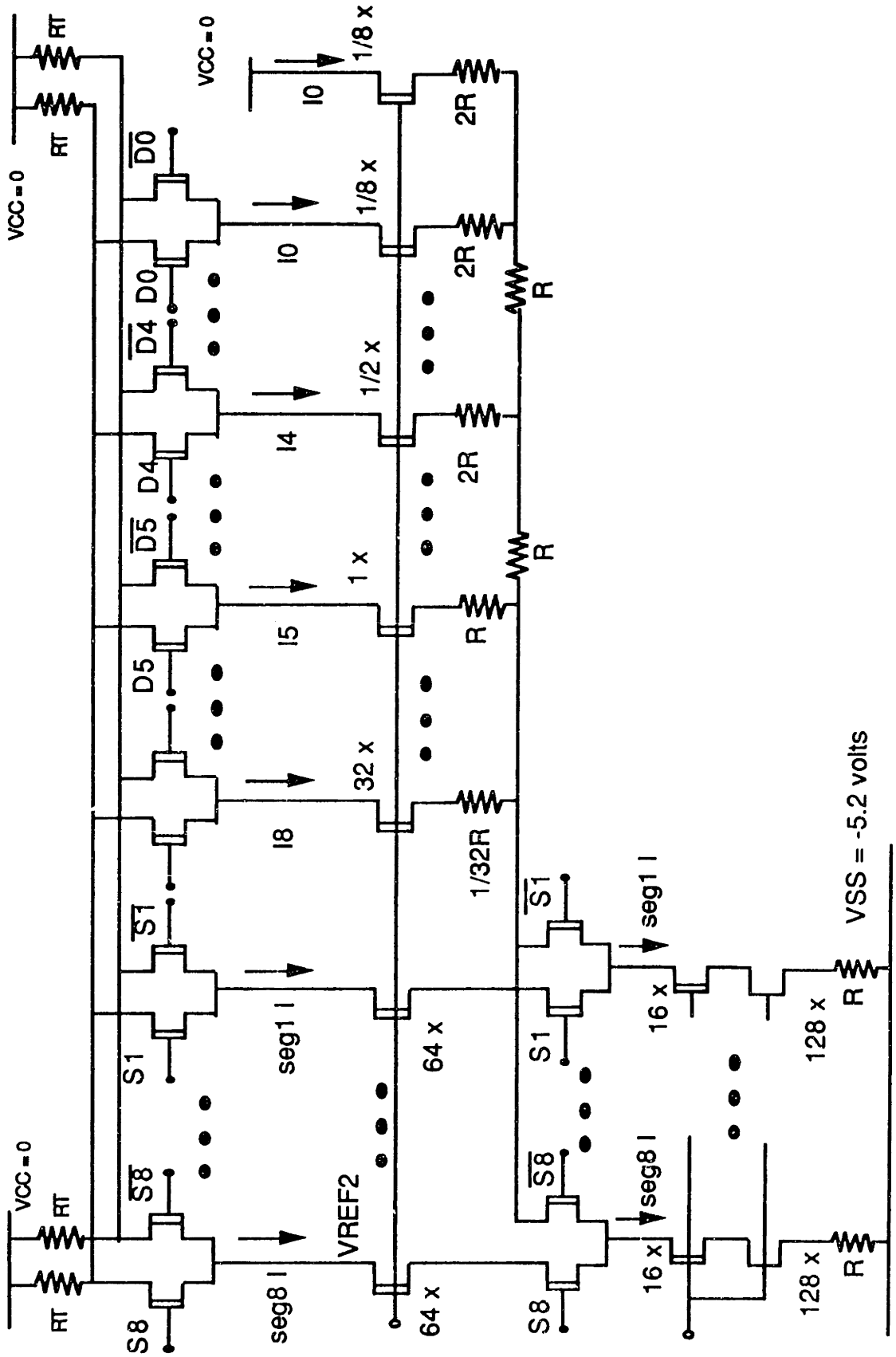

Figure 5.3 - MSB and LSB current source array and switches.

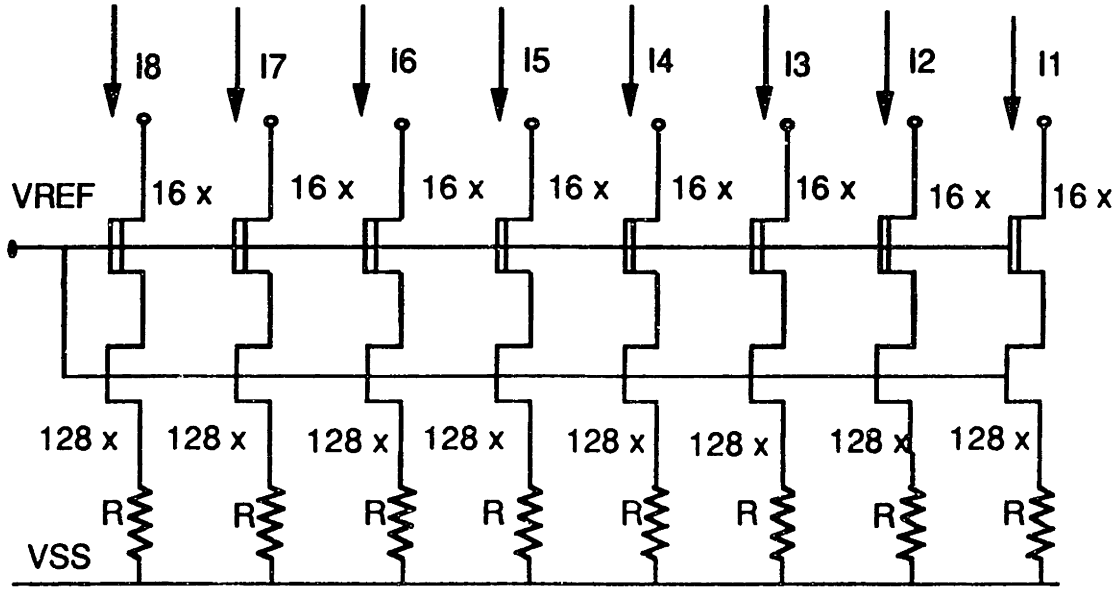

Figure 5.4 - MSB current source array.

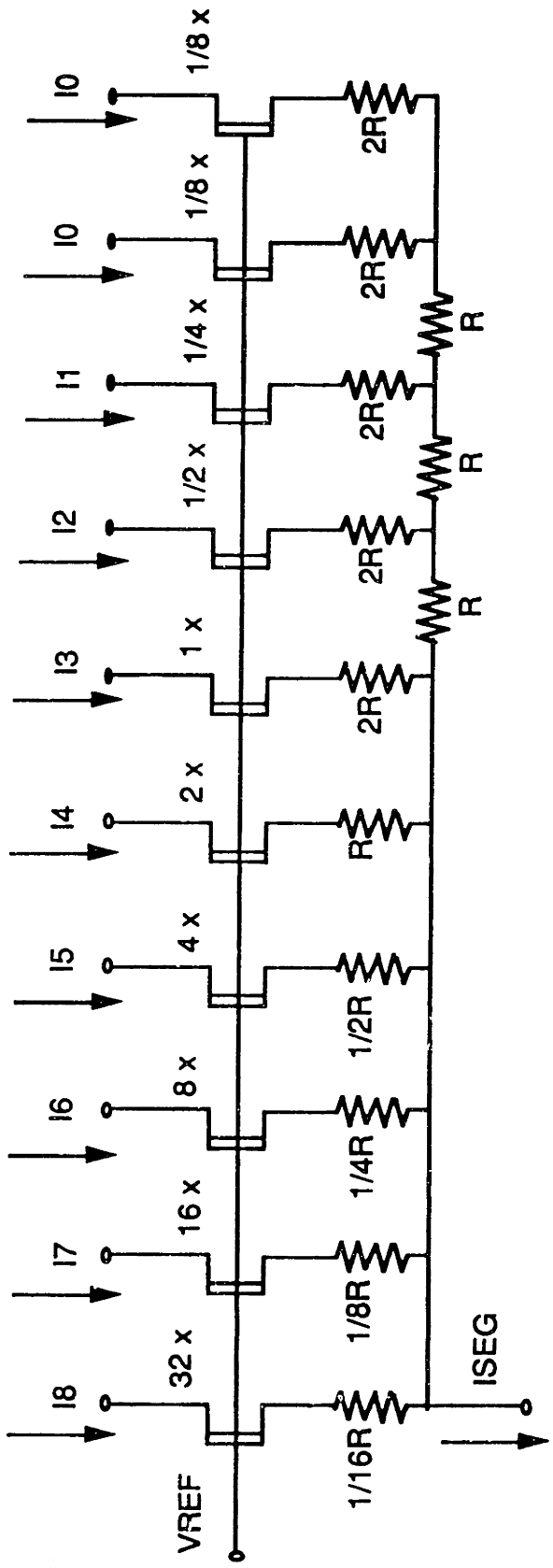

Figure 5.5 - LSB current source array.

The key to the most significant bit current source array is that all the MESFETs must be matched and scaled well to ensure high accuracy. The current sources must be laid out symmetrically around a common centroid point. Potential sources of error are the random or systematic variation of the resistor and transistor parameters. In general, the variation of the parameters occurs along local gradients across a slice of wafer. One way to get around this is to use interdigitation of multiple copies of the current sources of the design to offset process parameter gradients and possible temperature gradient effects. The key is that all transistors in the current source array are parallel, identical layouts with identical voltage drops to avoid field effects and potential nonlinearity. The transistors in a GaAs MESFET process traditionally have had worse matching than in Si MOSFET technology because of the purity and uniformity of the base wafer. To achieve better resistor matching, the same type of multiple copies of the transistor are used in all the current switching transistors and cascoding of the current sources. In addition, dummy components operating at the same bias condition as the rest of the array are used at the ends of the resistor arrays and transistors to ensure identical conditions for all operational components. The Vitesse GaAs MESFET process with three layers of metalization is used to achieve a compact layout and minimize parasitic interconnect resistance. A final key to having a precise current source array is to minimize the voltage distribution of the negative rail. Low voltage drops are achieved through the use of Metal 3 wide tracks as well as double metal layers (i.e., putting Metal 3 on top of Metal 2 and connecting them). In addition, multiple bond wires are used at both ends of the most significant bit array to reduce voltage drops to the central current sources.

5.4.5 - Operational Amplifier

The current source reference operational amplifier, shown in Figure 5.6, is designed for high dc gain and large drive capability. The differential mode gain of the amplifier is 2000. The 3 dB frequency is 135 MHz, and the slew rate is 75 V/μs. The common mode rejection ratio (CMRR) is greater than 80 dB at 10 MHz and over 60 dB at

100 MHz. The input resistance is approximately 1 megohm, and the output resistance is 110 ohms. The output stage can drive large capacitive loads and can swing in excess of 2.5 volts peak-to-peak with little distortion.

The amplifier is a two-stage design with internal frequency compensation. The input stage is an actively loaded source-coupled pair biased at low current to achieve a high input impedance. Matched depletion-mode source followers serve as buffers and level shifters to the first-stage current mirror. Both the first and second stage employ cascode transistors loaded with bootstrapped current source loads to boost each stage's gain. Without the p^+ ohmic bulk bias and n^+ ohmic guard ring, the gain of the amplifier is reduced to 900 due to the backgate effect, which reduces the output impedance of the depletion-mode loads.

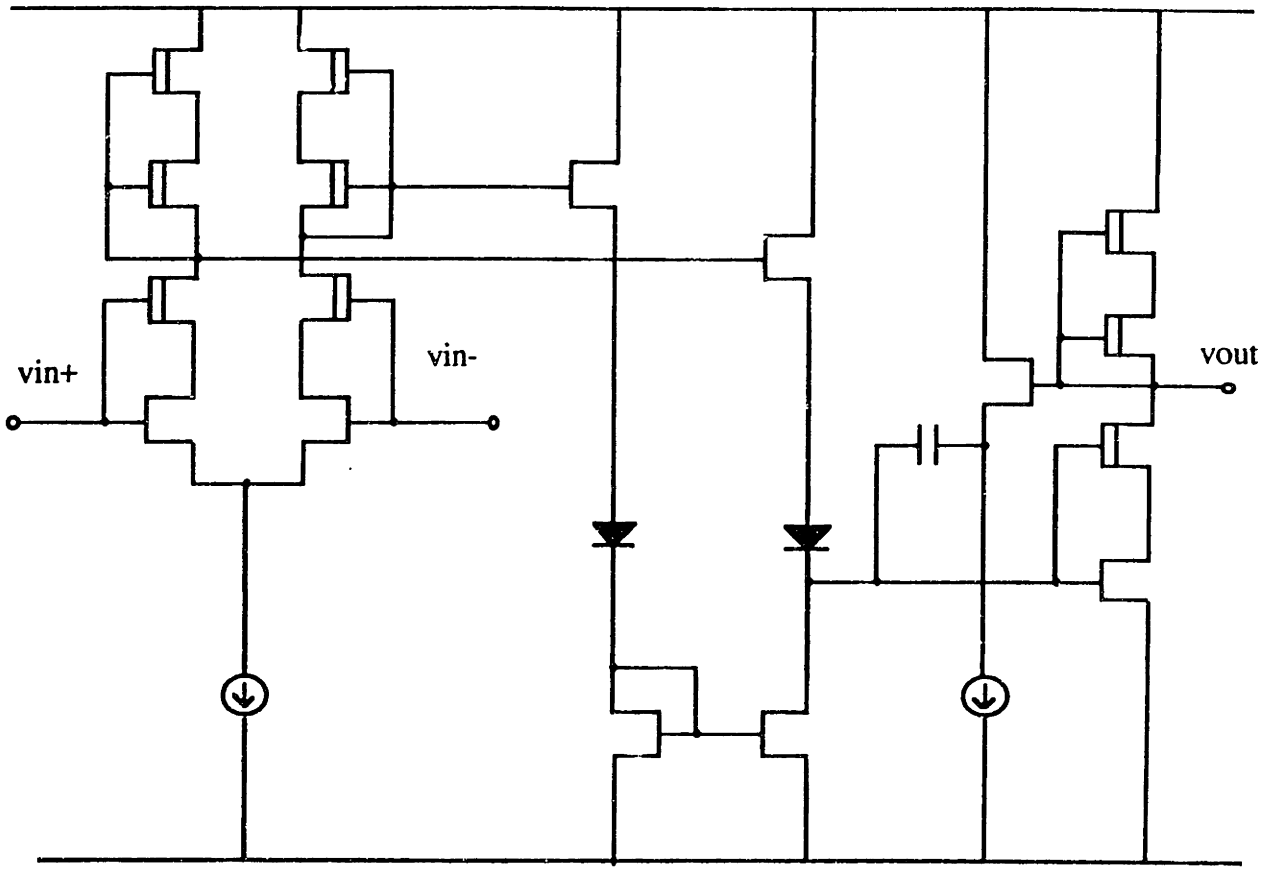

Figure 5.6 - Current source reference operational amplifier.

5.4.6 Voltage Reference

A circuit that produces a stable reference voltage over temperature is a required analog building block for low-drift circuits. The most controlled parameter of the digital MESFET process is the threshold voltage. As stated in Chapter 2, the threshold voltage of a MESFET is a function of pinchoff voltage, built in voltage, and other process-dependent parameters.

Subtracting the depletion-mode threshold from the enhancement-mode threshold yields a voltage in which many of the process-sensitive terms cancel. The difference is mainly fixed by the magnitude of the implanted charge. It is, therefore, possible to build a stable reference as shown in Figure 5.7. Here the voltage developed at the output of the amplifier is VSS + 0.95 volts for an enhancement-mode threshold voltage of 0.25 volts and a depletion-mode threshold voltage of -0.8 volts.

The primary advantage of this approach is that the temperature coefficients of the two threshold voltages cancel to first order. This circuit is used in the digital-to-analog converter to form an internal voltage reference of -4.05 volts. This voltage is then scaled by a resistor divider network to form the internal current source voltage reference.

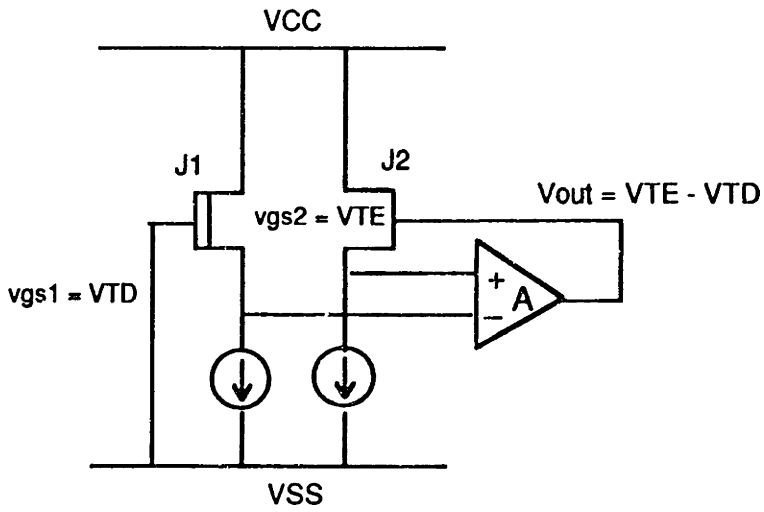

Figure 5.7 - Delta V_T voltage reference circuit.

5.5 Die Layout and Package

The 12-bit digital-to-analog converter die layout is shown in Figure 5.8. The current outputs are shielded and reverse terminated to 50 ohms on chip. In a future version of the digital-to-analog converter these resistors should be placed off chip because of the poor control of absolute resistor values (25%) of the process. Figure 5.9 shows the layout of a 9-bit digital-to-analog converter die and process test structures. The test structures are described in Chapter 4.

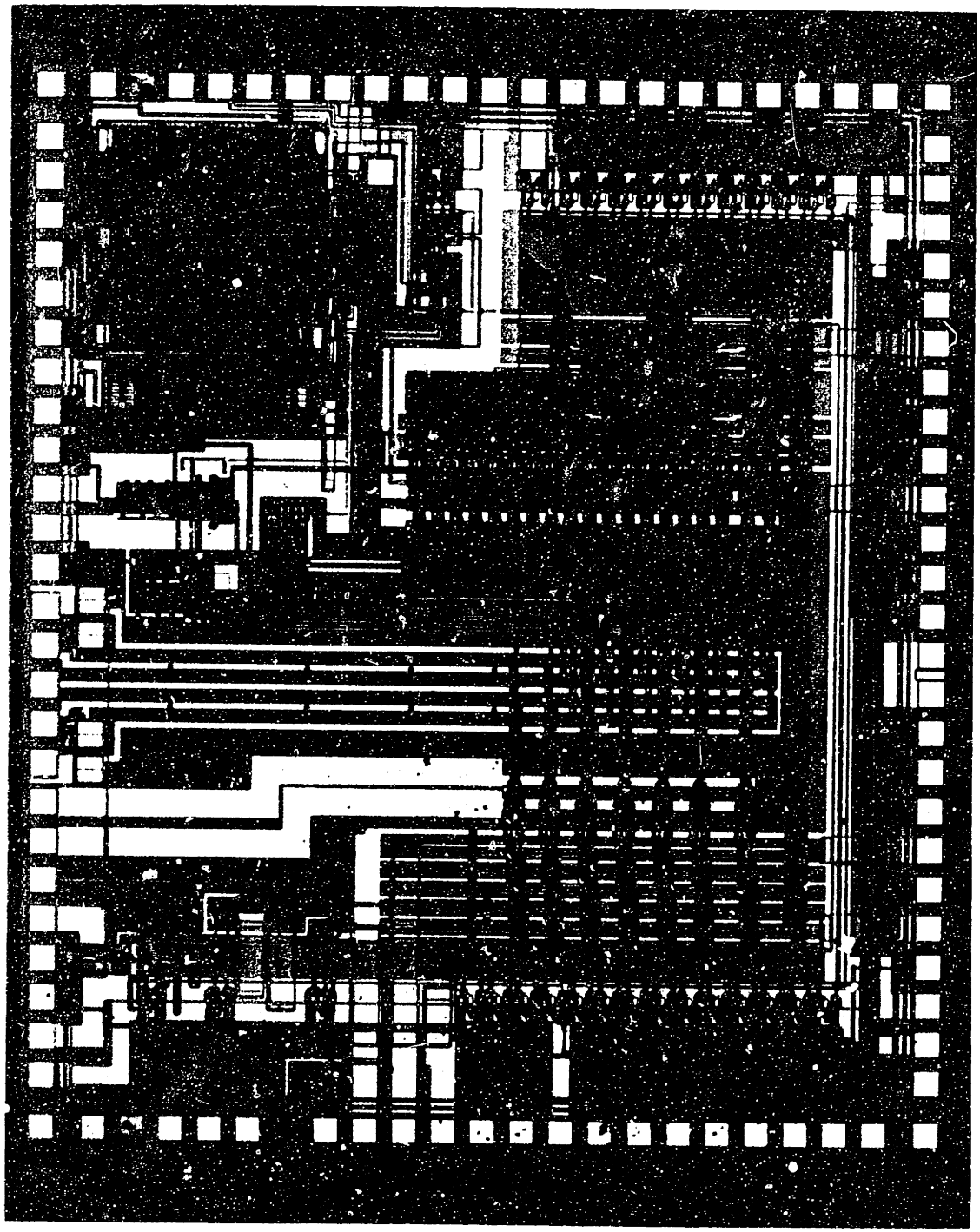

Figure 5.8 - 12-bit digital-to-analog converter.

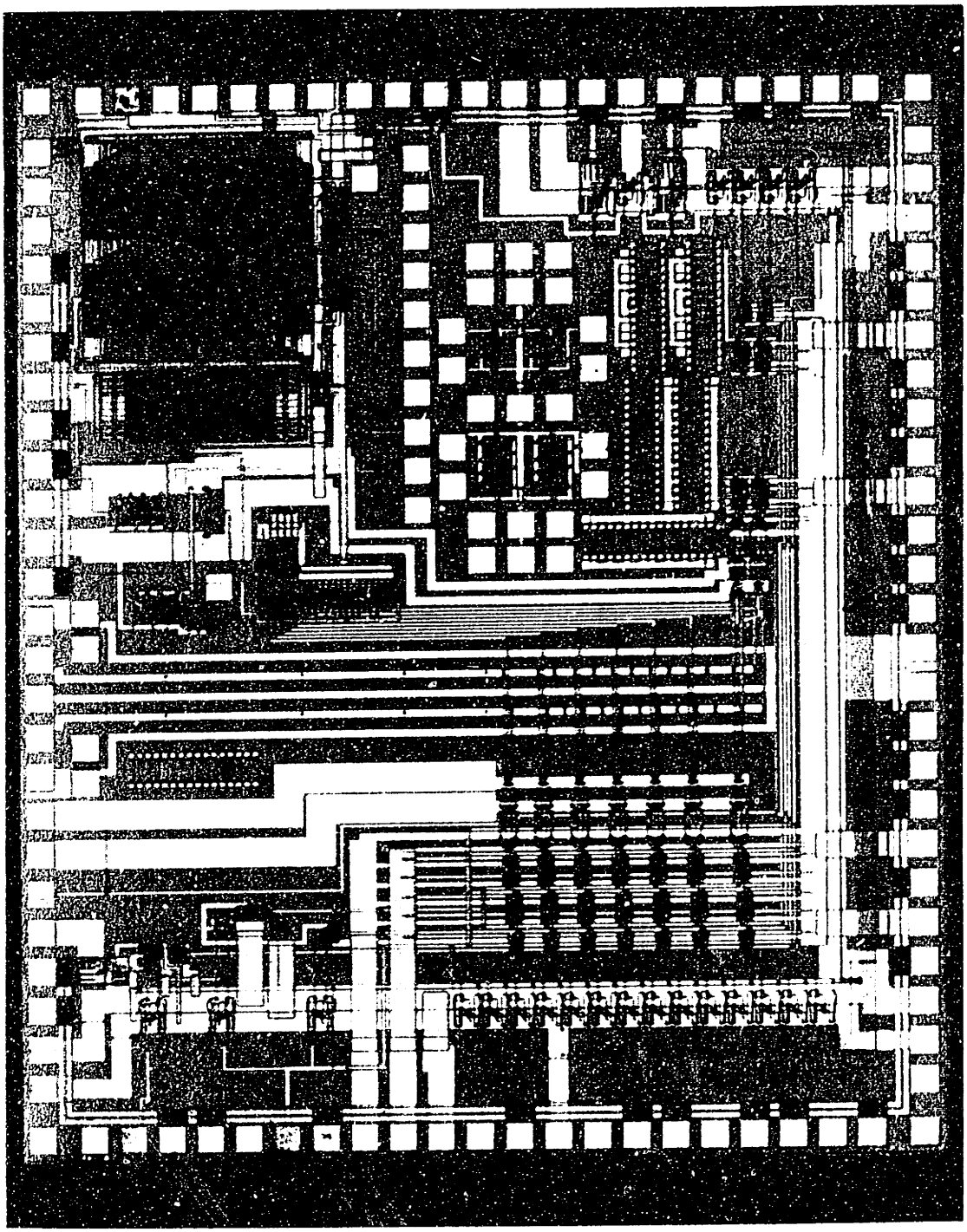

Figure 5.9 - 9-bit digital-to-analog converter and test structures.

The digital-to-analog converter is packaged in a 52-pin leaded chip (shown in Figure 5.10), contains a V_{TT} -2.0 volt power plane, V_{SS} -5.2 volt power plane, and a ground plane. The ground plane of the package is designed in a concentric circle closest to the die to minimize bondlead lengths of ground connections. On the same tier but insulated by ceramic from the ground ring are the signal lands, which are designed as 50 ohm transmission lines that connect bondwire signals to outside the package. The leads of the package form a soldered microstrip interface to the top layer of the printed circuit board on which the package is attached. This requires the top layer of the printed circuit board to be designed as a 50 ohm microstrip. Figure 5.11 shows a close up of the 12-bit digital-to-analog converter packaged in 52-pin leaded chip carrier highlighting the double wirebonds on power and ground. Table 5.2 shows the pin assignments for the packaged digital-to-analog converter.

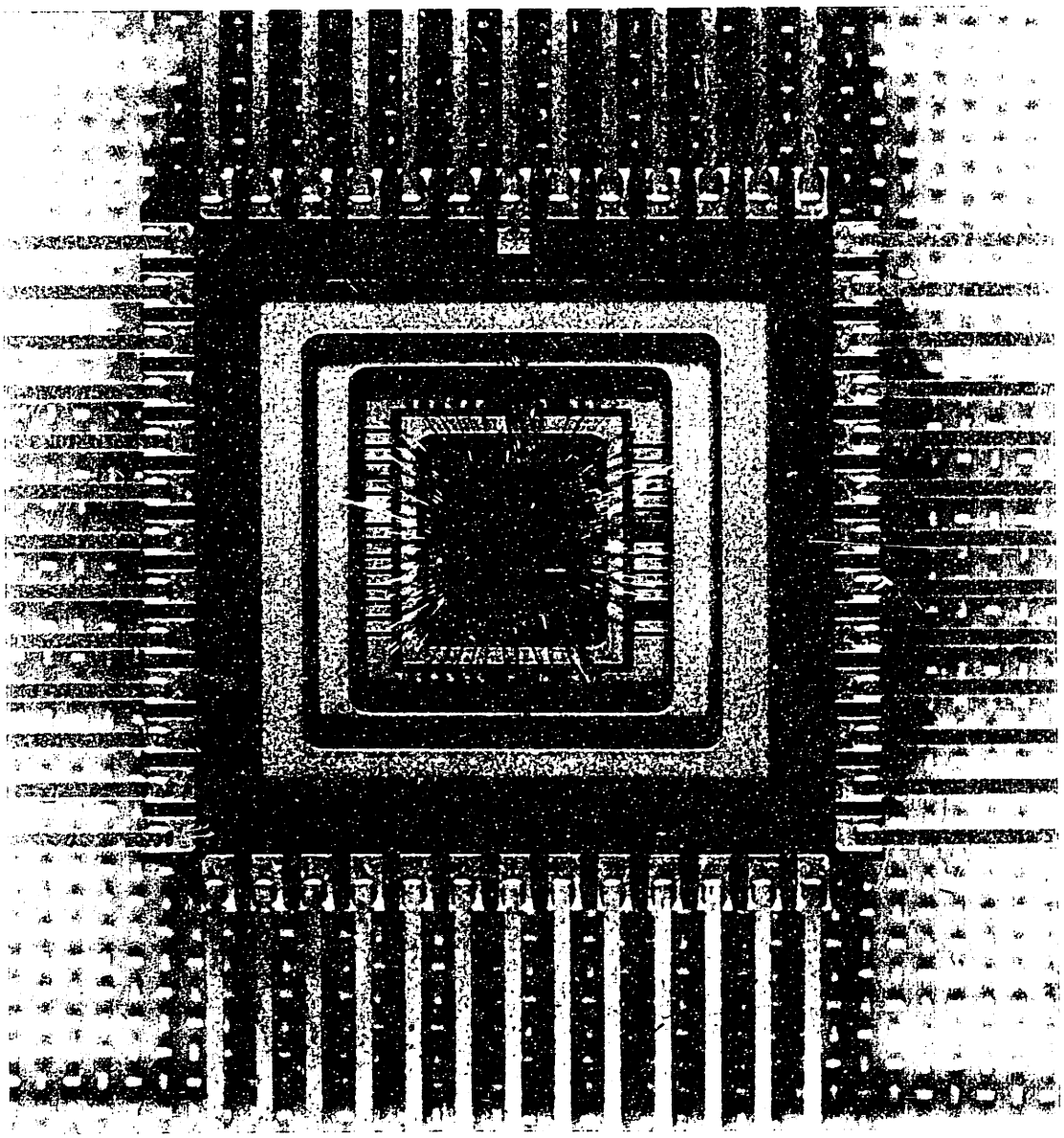

Figure 5.10 - 12-bit digital-to-analog converter packaged in 52-pin leaded chip carrier.

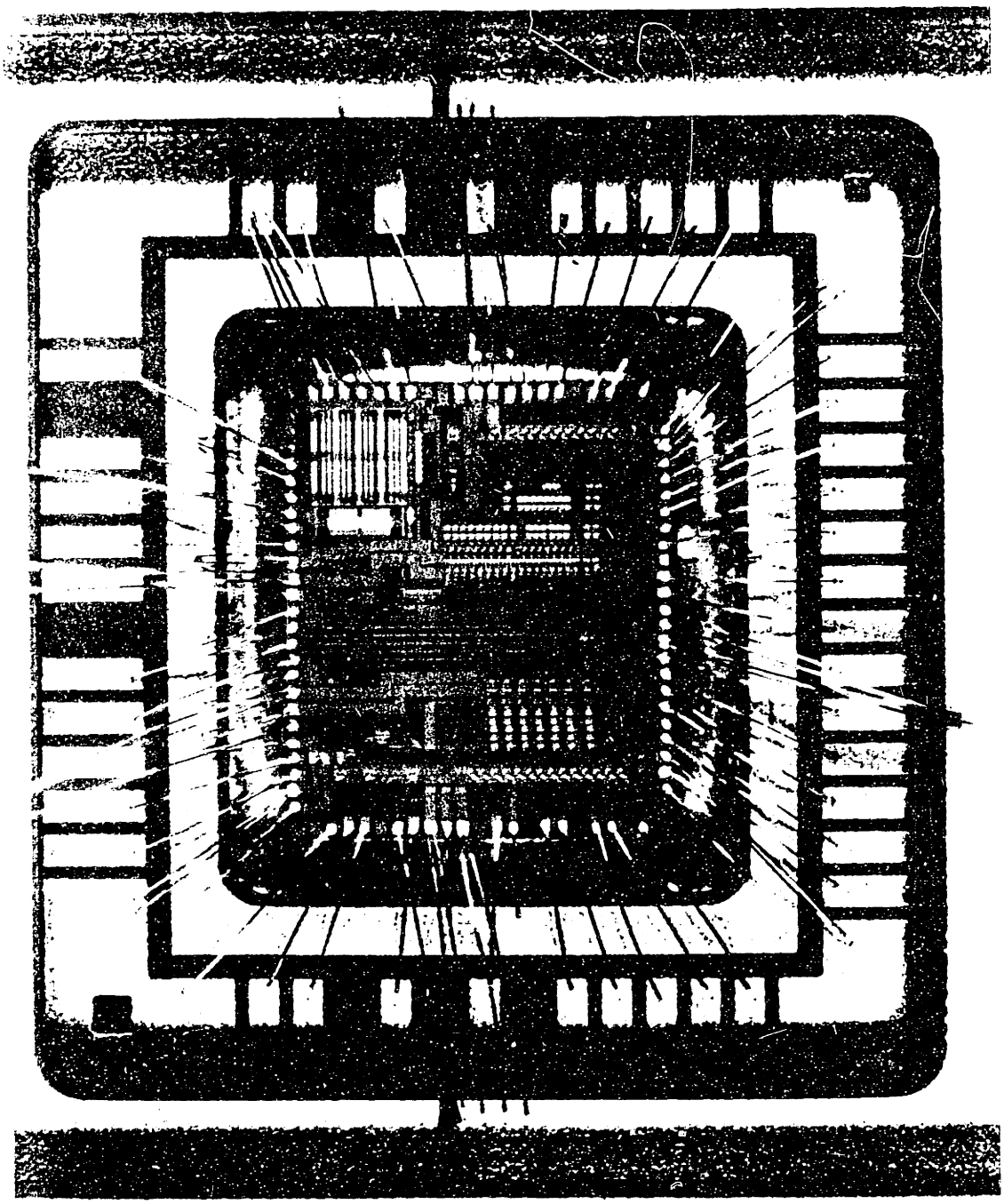

Figure 5.11 - 12-bit digital-to-analog converter packaged in 52-pin leaded-chip carrier showing double wirebonds on power and ground.

Table 5.2 - Digital-to-Analog Converter Pin Assignments

Pin #	Name	I/O	Description
45-44, 42-37 35-34, 32-31	DAO-DA11	I	12 ECL-level input bits. D_{11}=Most Significant Bit (MSB) D_0=Least Significant Bit (LSB)
9-6, 6-5, 3-1 52-50, 48-47	DB0-DB11	I	12 ECL-level input bits. D_{11}=Most significant bit (MSB) D_0=Least Significant Bit (LSB)
26	Digital reference		ECL digital reference; norminally -1.3V
7,46	Digital VTT		Negative digital supply pin; nominally -2V
4, 49, 43, 36 30, 10	Digital Ground		Digital Ground Return
33, 26	Analog VSS		Negative analog supply pin; nominally -5.2V
27,23,19,16	Analog Ground		Analog Ground Return
19	I Out	O	Analog current output; full scale occurs with digital inputs all "1".
17	I Out	O	Complementary analog current output; zero scal output occurs with all digital inputs "0".
25	I Reference Output	O	Connection for external current reference output.
12	Clock	I	Conversion clock (ECL level)
13	Clock/Clock Ref		Complementary conversion clock (ECL level) or clock ECL reference; nominally -1.3V
11	Blank	I	Video Blank (all ones)
29	Sync	I	--
14	Select A/B In	I	Select A/B In
15	Select A/B Output	O	Select A/B Out
22	Amp Out	O	Operational amplifier Output
20	Amp In	I	Operational amplifier Input
21	V ReferencOutput	O	Connection for external voltage sense Output
24	V Reference Input	I	Connection for Voltage Reference Input

5.6 High-Speed Printed Circuit Board

The high speed multi-layer printed circuit board was designed to perform ac test of the packaged parts. The top conductor layer forms the microstrip signal layer. The second conducting layer provides a return path for the microstrip waveguide. The third layer is a power conductor layer, which is segmented into -2 volt V_{TTC}, -2 volt V_{TTD}, and -5.2 volt V_{SS} power planes. V_{TTC} provides isolated power to the digital-to-analog converter from V_{TTD}, which feeds 50 ohm ECL termination resistors. This decouples the data-transition-induced -2 volt power supply noise from the digital-to-analog converter internal power supply. This design also enables the V_{TTD} power supply to be biased at the ECL voltage reference of -1.3 volts for those test generators that have a sourcing and sinking drive capability. The fourth layer is a power supply ground return. Having a separate microstrip ground and power ground eliminates signal-to-power supply coupling and is a requirement for printed circuit board designs operating at 500 MHz. The power supply filtering and decoupling circuits use a combination of ferrite beads and multiple capacitor values to provide good broadband bypassing for the power supply.

The printed circuit board is fabricated with one-ounce copper conducting layers and glass epoxy (FR4) insulating layers. The glass epoxy has a relative dielectric of 4.8. These two parameters, combined with the requirement of a 50 ohm microstrip impedance, constrain the width of the conductor and the height of the dielectric by:

$$Z_0 = 87/ (\varepsilon_r + 1.41)^{1/2} \ln[(5.58 \cdot h)/(0.8w+t)] \qquad 5.1$$

where Z_0 is the microstrip characteristic impedance, ε_r is the relative dielectric, h is the dielectric height in mils, t is the conductor thickness in mils, and w is the conductor width in mils. For a t of 1.4 mil (1 ounce copper) and an h of 10 mil, the width becomes 16 mils. The microwave design practices employed in the design of the printed circuit board include using reverse termination for the current outputs and covering open areas of the microstrip layer two run widths away from signal paths with ground plane. Vertical SMA connectors were used as the external signal interface to conserve board area at the cost of a slight

reduction in bandwidth (15 GHz compared to 18 GHz). The schematic of the high-speed test board is shown in Figure 5.12 with the corresponding microstrip layout shown in Figure 5.13.

5.7 Performance

5.7.1 Dynamic Test

A simple, low-cost, digital-to-analog converter dynamic test strategy compares the output of the 12-bit digital-to-analog converter with a precise reference digital-to-analog converter of higher resolution and accuracy (16-bit digital-to-analog converter).[8] A differencing opamp circuit provides a measure of the error between the digital-to-analog convert under test and the reference digital-to-analog converter. The error is amplified and applied to a 5-bit analog-to-digital converter whose LSB corresponds to 1/4 LSB of the digital-to-analog converter under test. The digital-to-analog converter under test is first adjusted to eliminate zero and full-scale errors followed by a bit scan where both the reference digital-to-analog converter and digital-to-analog converter under test are dynamically driven and compared. Figure 5.14 shows a block diagram of this digital-to-analog converter dynamic test. This test apparatus can measure all static linearity and dynamic errors greater than the accuracy and settling time performance of the reference digital-to-analog converter. This configuration was used to measure dynamic performance of the packaged converter.

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[8] Analog Devices, Inc. *Analog Conversion Handbook*, 1987.

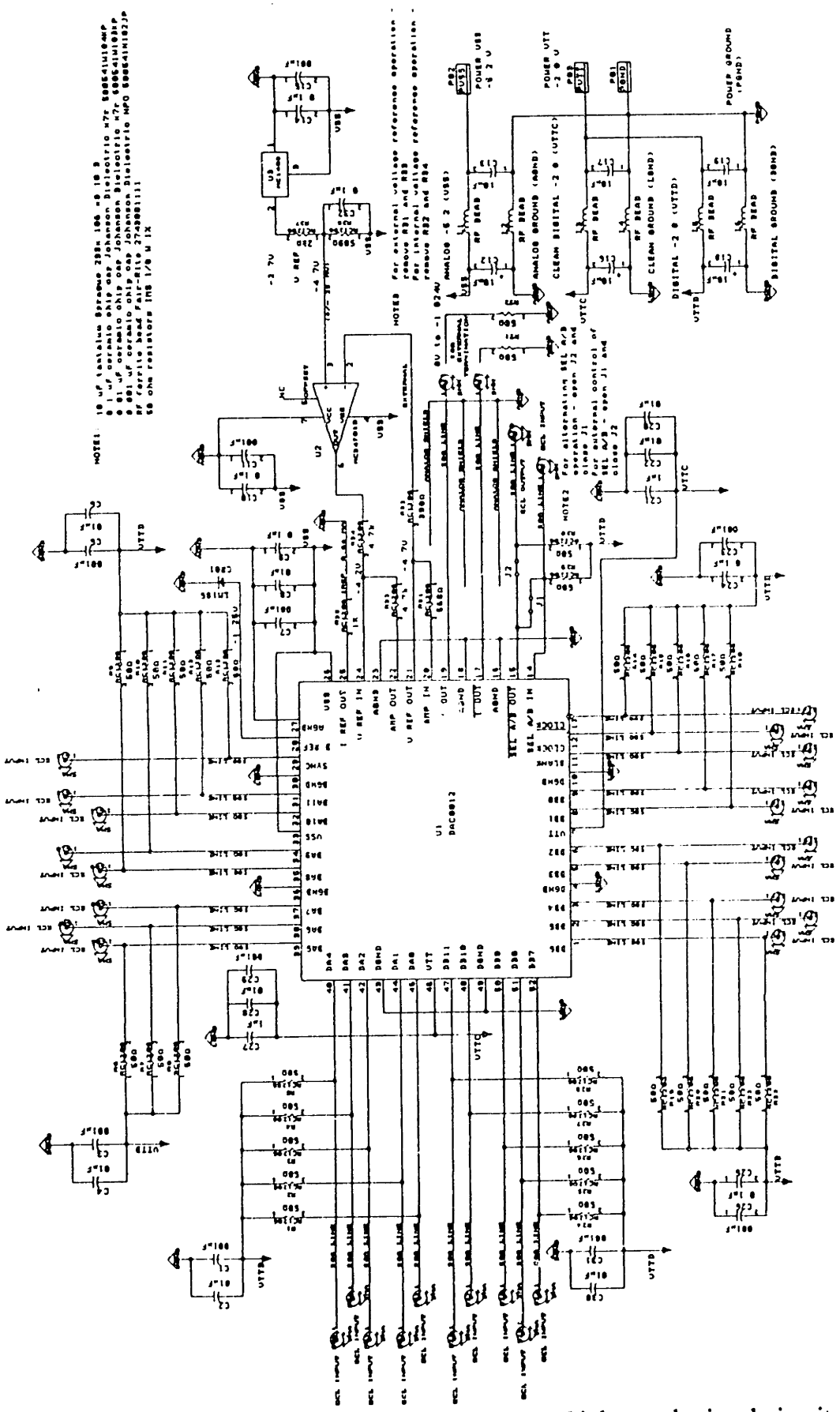

Figure 5.12 - 12-bit digital-to-analog converter high-speed printed-circuit-board schematic.

Figure 5.13 - 12-bit digital-to-analog converter high-speed printed-circuit-board layer 1.

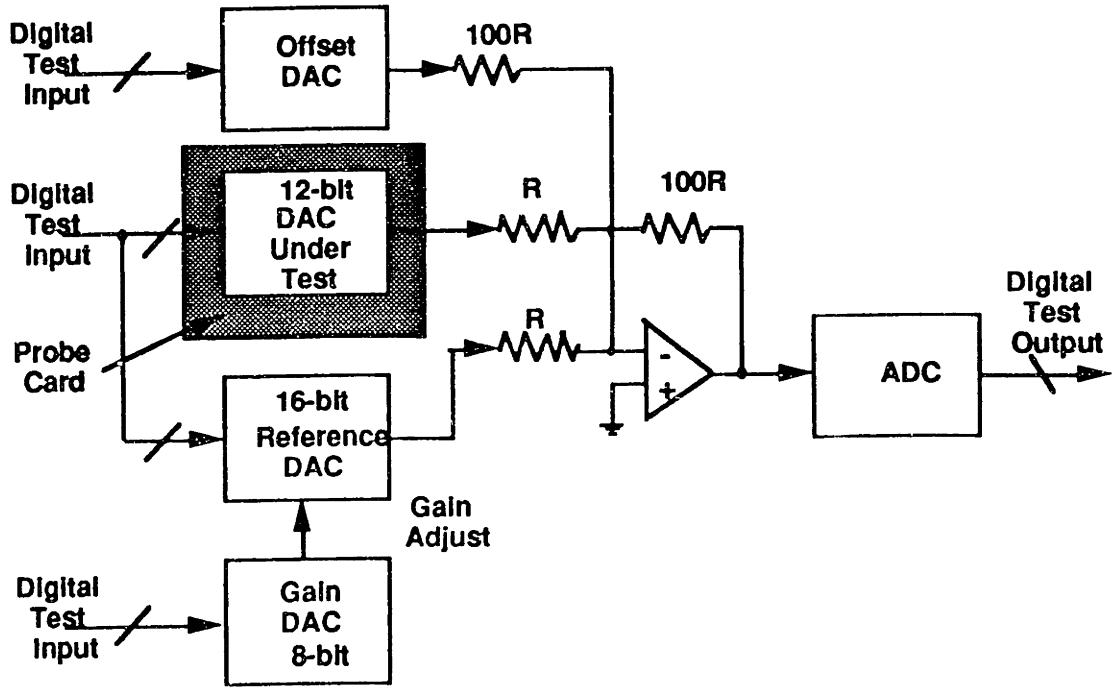

Figure 5.14 - Digital-to-analog converter dynamic test.

5.7.2 Settling Time

The high-speed digital-to-analog converter settling time performance was measured by the circuit topology shown in Figure 5.15.[9] Settling time is defined as the time required for the output to approach ±1/2 LSB of a final value for a step in input. The final value voltage (all ones) is set by the reference voltage source V_{REF}. The ±1/2 LSB error band window is set by adjusting the current source I1, which develops the window voltage across the 1 ohm resistor. The digital-to-analog converter is switched and the settling time is measured as shown in Figure 5.16. The propagation delay of the comparator (tpd) must be subtracted in order to obtain the correct settling time measurement.

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[9] Analog Devices, Inc. *Analog Conversion Handbook*, 1987.

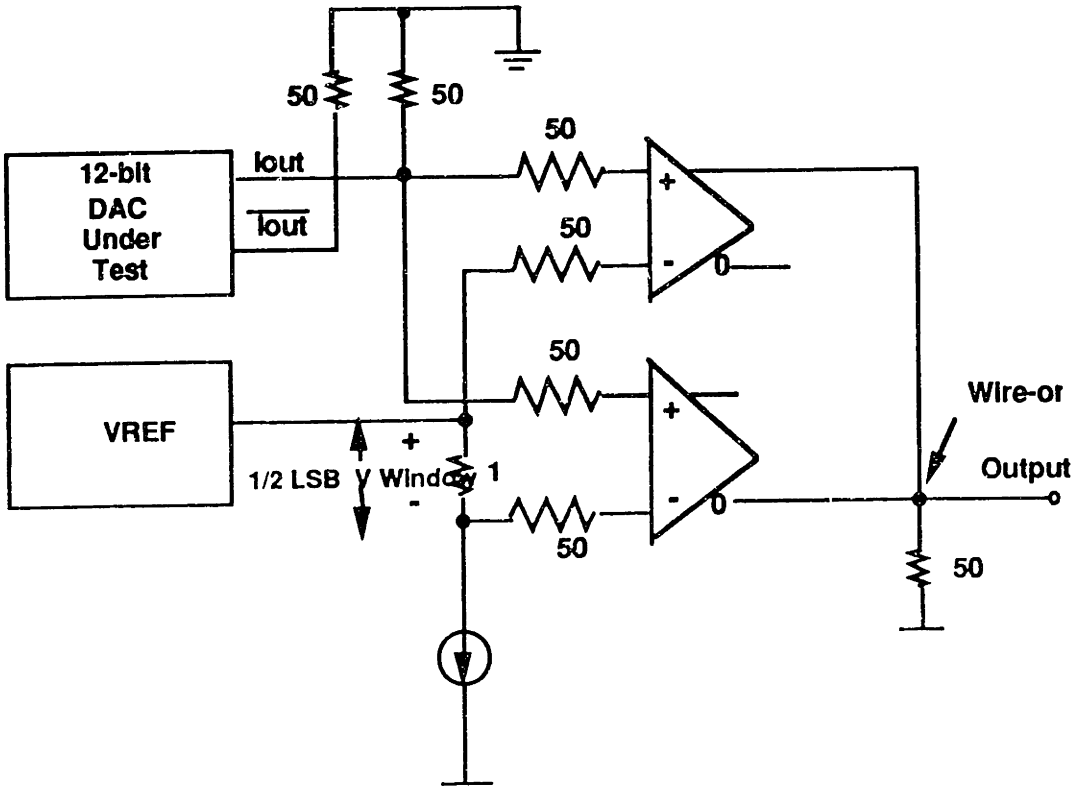

Figure 5.15 - Digital-to-analog converter settling time test.

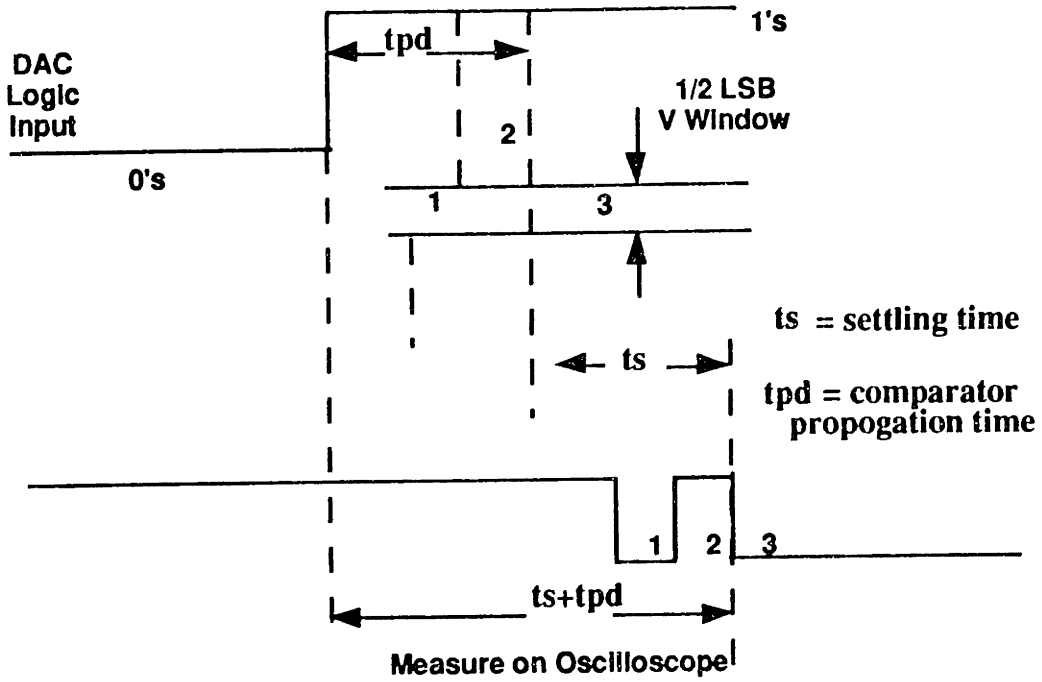

Figure 5.16 - Settling time diagram.

5.7.3 AC Test

The 500 MHz 12-bit digital-to-analog converter can form an integral part of low spurious response direct-digital-frequency synthesizer systems that are employed in function generators and digital communication systems. An ideal 12-bit digital-to-analog converter should enable a direct-digital-frequency synthesizer to produce a digital sinewave whose phase and amplitude distortion is -73.8 dBc (6dB*12+1.8dB) due to random distributed quantization noise. The usable bandwidth of the synthesizer is from 0 Hz to 1/3 the clock frequency limited by the presence of the principal spur, formed by the alias of the fundamental and clock frequency. Therefore, it is desirable to operate a digital frequency synthesizer at the highest possible clock frequency. At present, 500 MHz digital-to-analog converters are limited to 10-bit resolution resulting in -61.8 dBc phase and amplitude distortion.

In addition to being an application of the digital-to-analog converter, the direct-digital-frequency synthesizer system itself is a useful ac test fixture that can be used to determine dynamic performance of the digital-to-analog converter. The sinewave-direct-digital frequency synthesizer functional block diagram shown in Figure 5.17 is the architecture most often used for direct-digital synthesizer design. It has proved to be the most efficient design for applications that require *multi-octave* tuning and low output spurious PM and spurious AM outputs. The frequency resolution of the output is obtained by setting the value of K equal to one. The remaining performance characteristics are determined by the implementation of the sine ROM, the digital-to-analog converter, and the choice of the output filter transfer function. The performance of this design is summarized by Rheinhart in equations 5.2 through 5.5.[10] The output frequency, f_o, is given by:

$$f_o = f_{clock}\, k / 2^N \qquad 5.2$$

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[10] V. Rheinhart, "A Comparison of Direct Digital Frequency Synthesizer Architecture Performance," Hughes Aircraft Co. internal report, 1987.

where f_{clock} = clock frequency, K is the frequency control word, and N is the number of accumulator bits. The frequency resolution, F, is given by:

$$F = f_{clock}/2^N \qquad 5.3$$

The spurious phase modulation sidebands level, S_P, is given by:

$$S_P = 10 \text{ Log } [(\pi^2 2^{-2L})/3] \qquad 5.4$$

where L is the number of sine ROM/RAM bits.

The spurious amplitude modulation sidebands level, S_A, is given by Equation 5.5:

$$S_A = 10 \text{ Log } [(1/6) 2^{-2M}] \qquad 5.5$$

Finally, M is the number of digital-to-analog converter bits.

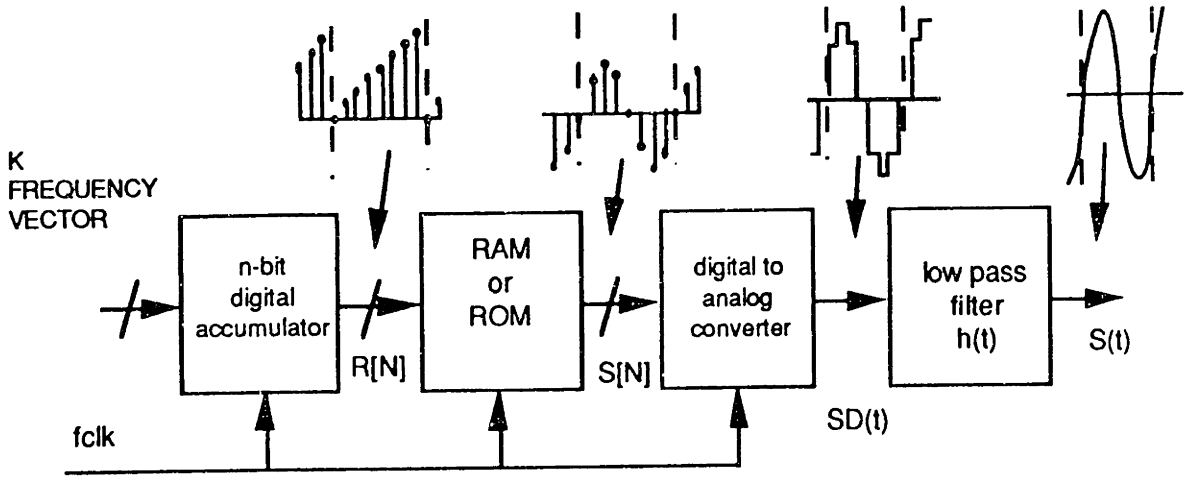

Figure 5.17 - Functional block diagram of sinewave direct digital frequency synthesizer.

This system was used to drive the digital-to-analog converter at high clock frequency and data rates to obtain the oscilloscope generated time-domain waveforms and spectrum analyzer generated frequency responses shown in Figures 5.18 through 5.35.

Samples of the fabricated devices were measured to be 12-bit monotonic with integral nonlinearity of 2 LSBs and differential nonlinearity of 1 LSB. The device's full dynamic range was tested at a maximum clock of 500 MHz. Discrete bits were tested at rates as high as 1 GHz. Settling time to 0.5 % of final value was less than 2 nsec. A larger

set of devices were measured to be 10-bit monotonic with integral nonlinearity of 2 LSBs and differential nonlinearity of 1 LSB. To increase 12-bit performance yields it is recommended that the 3-bit segmented/9-bit slave current source architecture be modified into a 4-bit segmented/8-bit slave current source architecture. This relaxes the segmented current source matching requirements to 8 bit relative accuracy. The added design complexity for this change is in the segment decoder which now must perform a 4 to 16 priority decode. Finally, additional testing of the sample wafer lot with full characterization of the test structures is recommended to predict yield performance over multiple wafer lots.

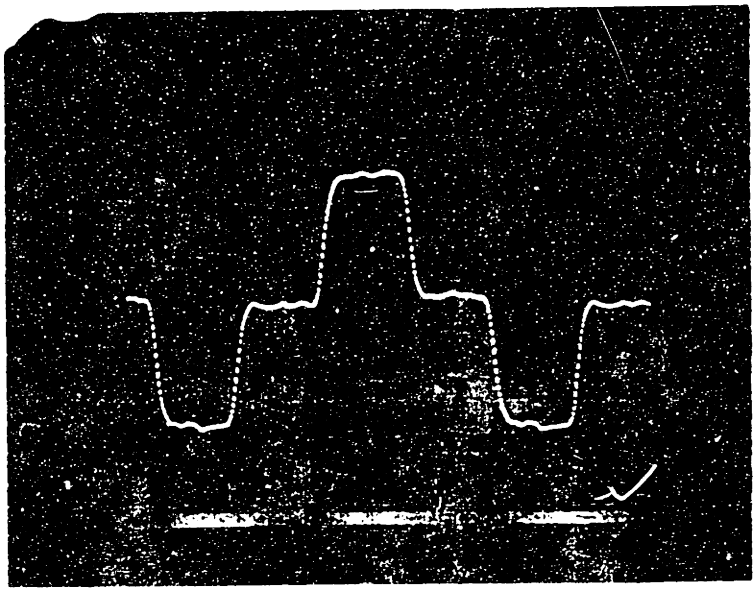

Figure 5.18 - Clock frequency 300 MHz 4 step sine wave.

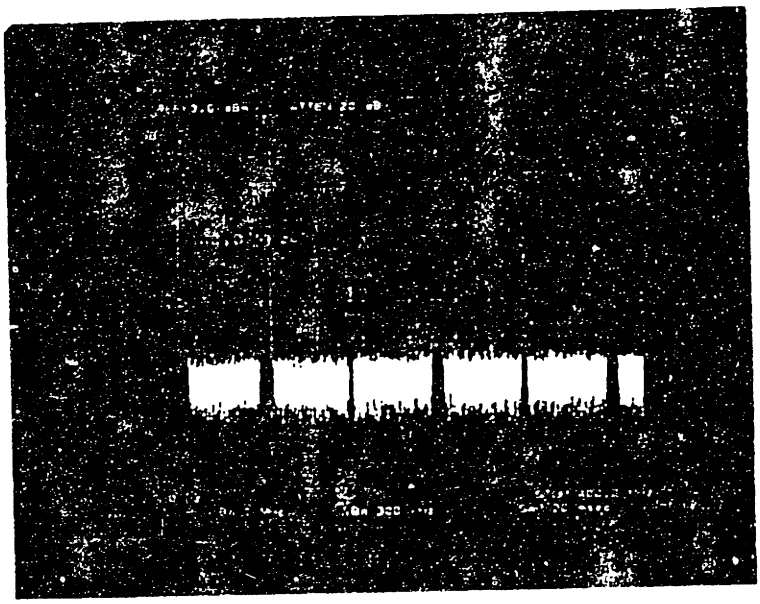

Figure 5.19 - Clock frequency 100 MHz 2nd Harmonic -46 dB.

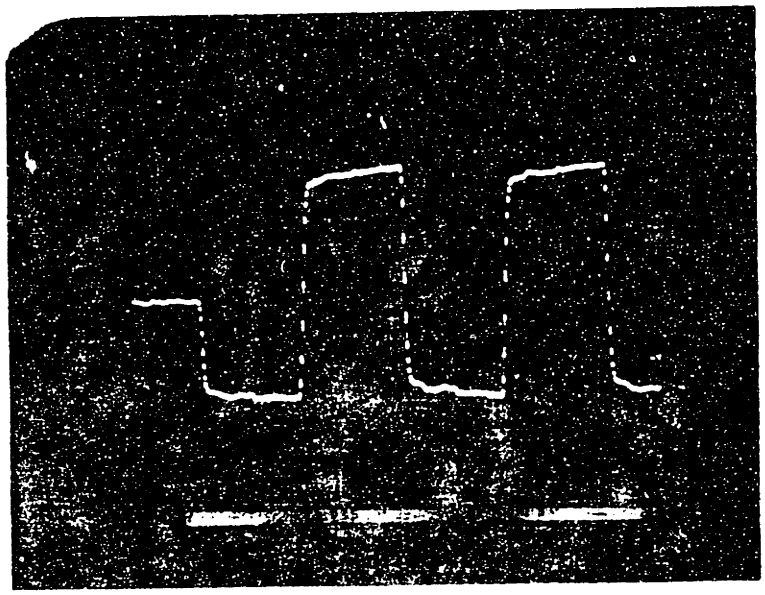

Figure 5.20 - Clock frequency 100 MHz square wave using only three most significant bits.

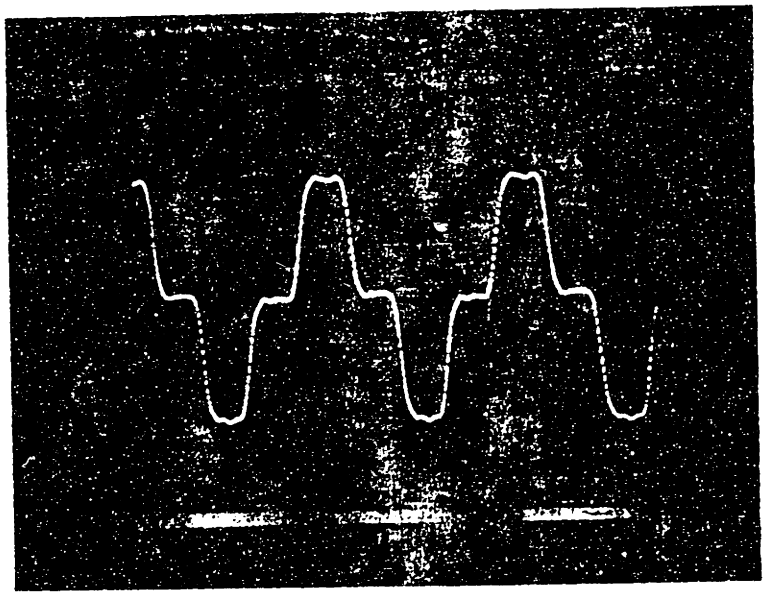

Figure 5.21 - Clock frequency 510 MHz 4 step sine wave.

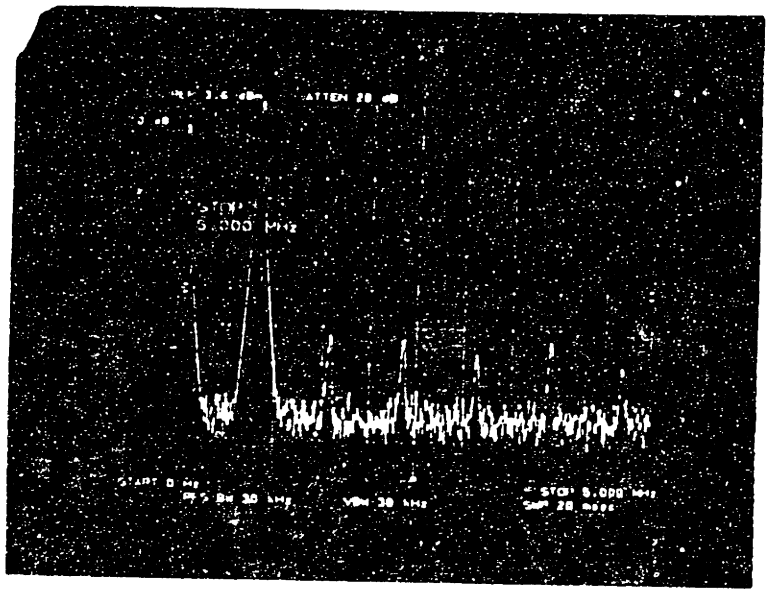

Figure 5.22 - Clock frequency 50 MHz 64 step sine wave.

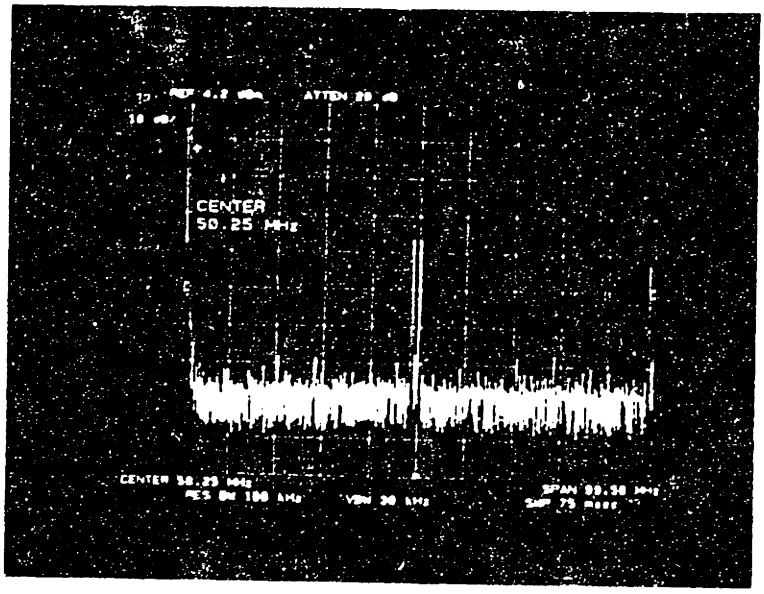

Figure 5.23 - Clock frequency 100 MHz 64-step sine wave.

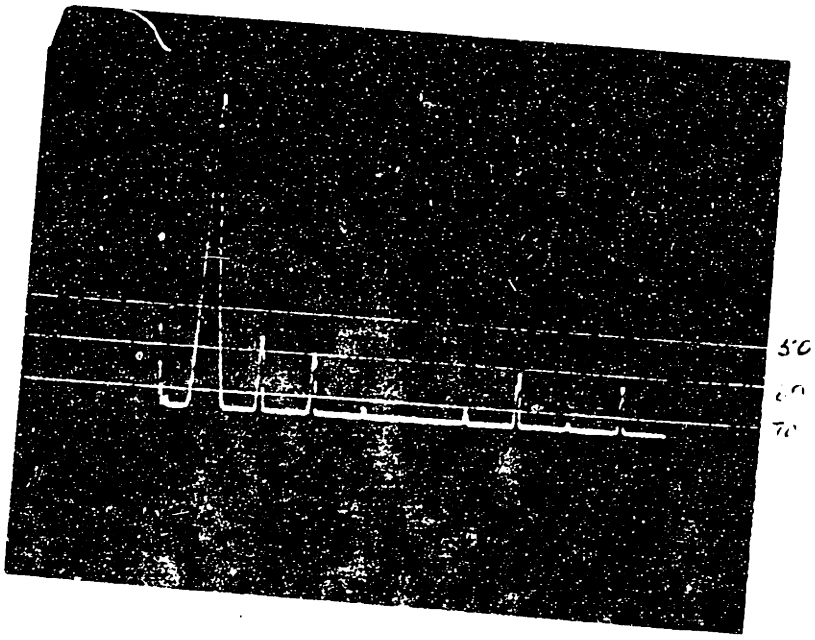

Figure 5.24 - Clock frequency 128 kHz 64-step sine wave.

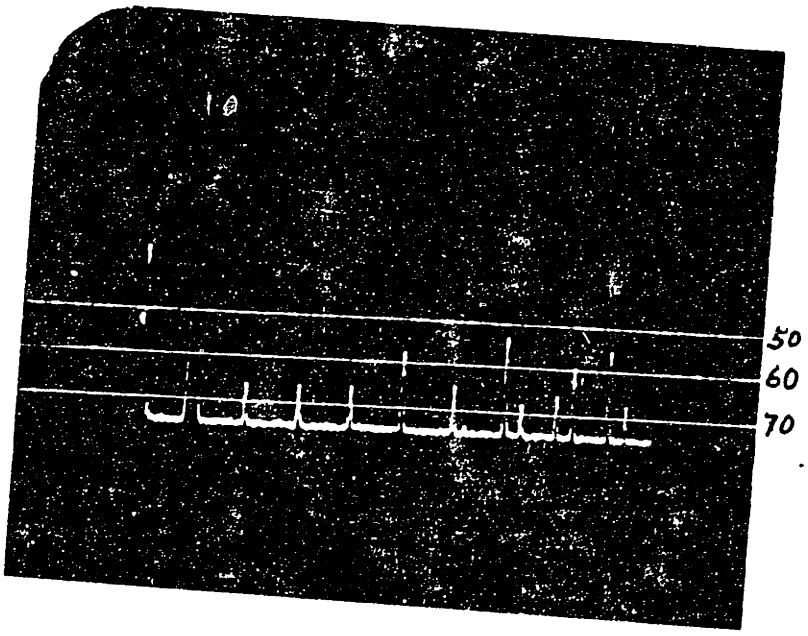

Figure 5.25 - Clock frequency 80 kHz 16 step sine wave.

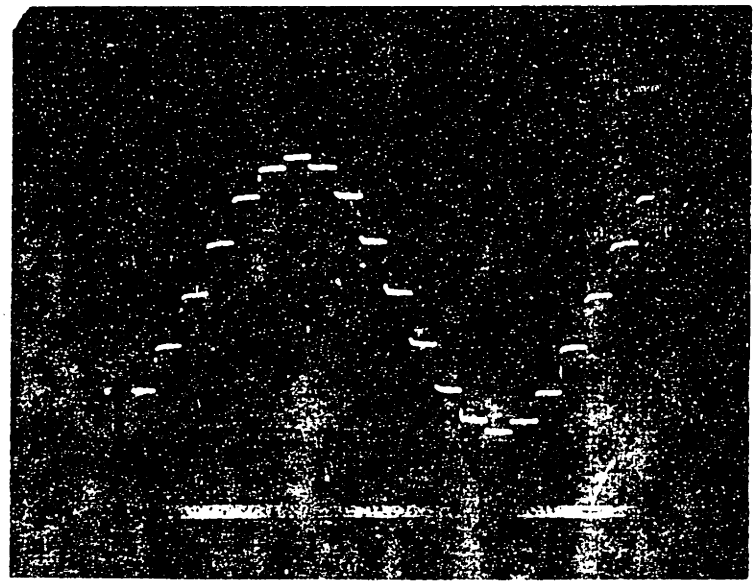

Figure 5.26 - Clock frequency 10 MHz 16-step sine wave.

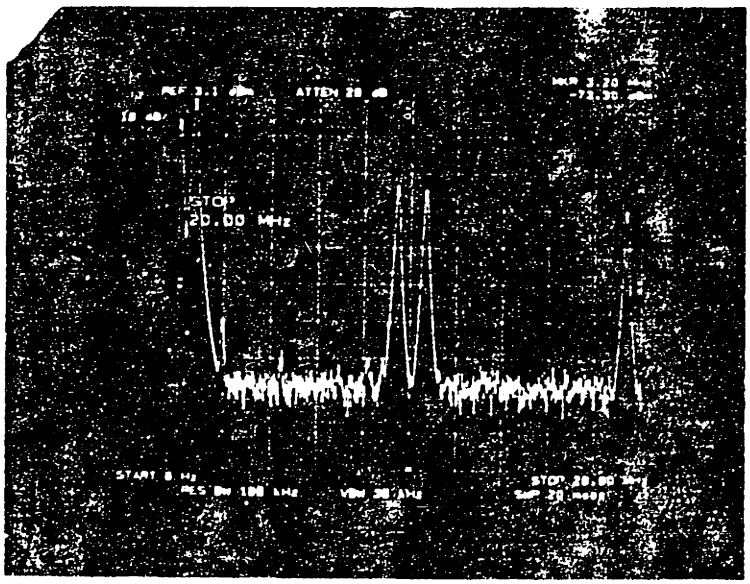

Figure 5.27 - Clock frequency 625 kHz 6th Harmonic -51 dB.

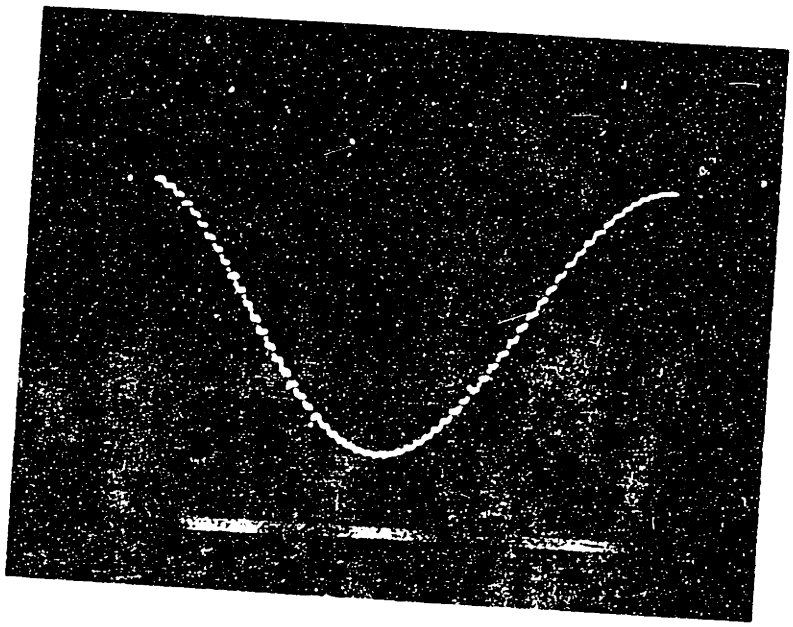

Figure 5.28 - Clock frequency 300 MHz 64-step sine wave.

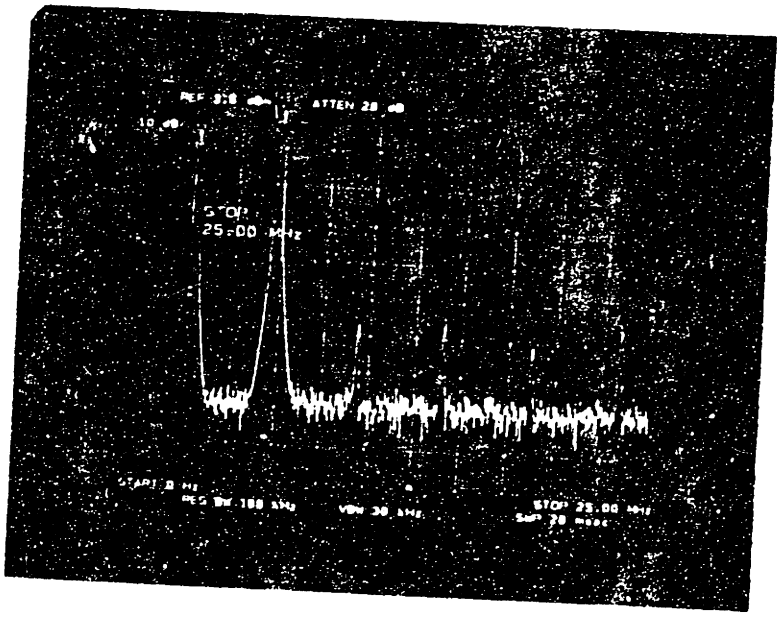

Figure 5.29 - Clock frequency 4.68 MHz, 2nd Harmonic -56 dB.

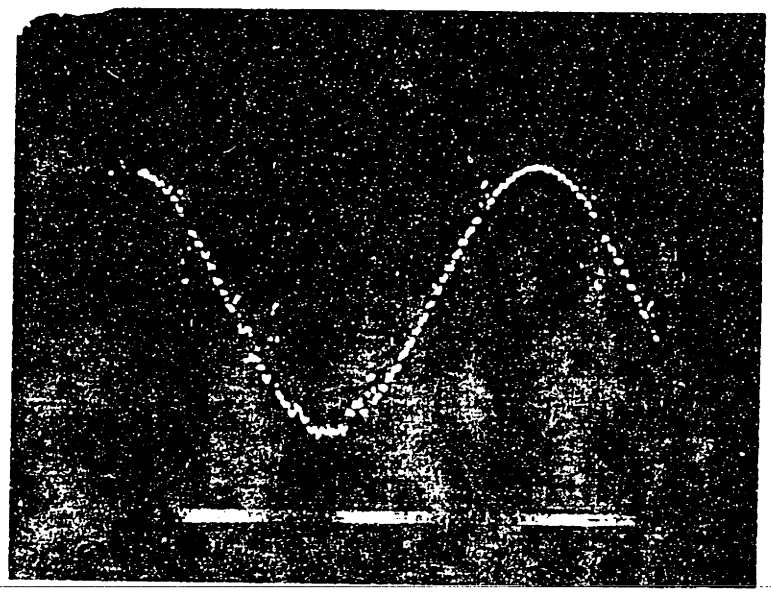

Figure 5.30 - Clock frequency 400 MHz 64-step sine wave.

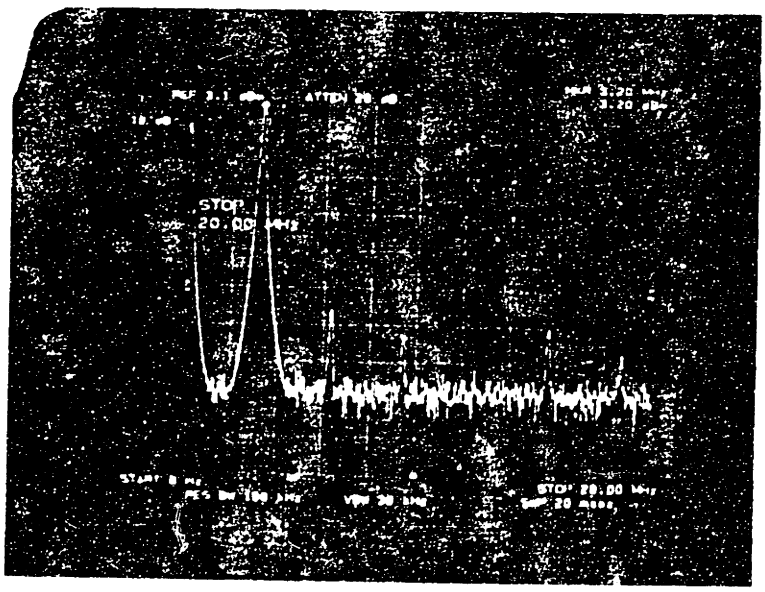

Figure 5.31 - Clock frequency 200 MHz 64-step sine wave.

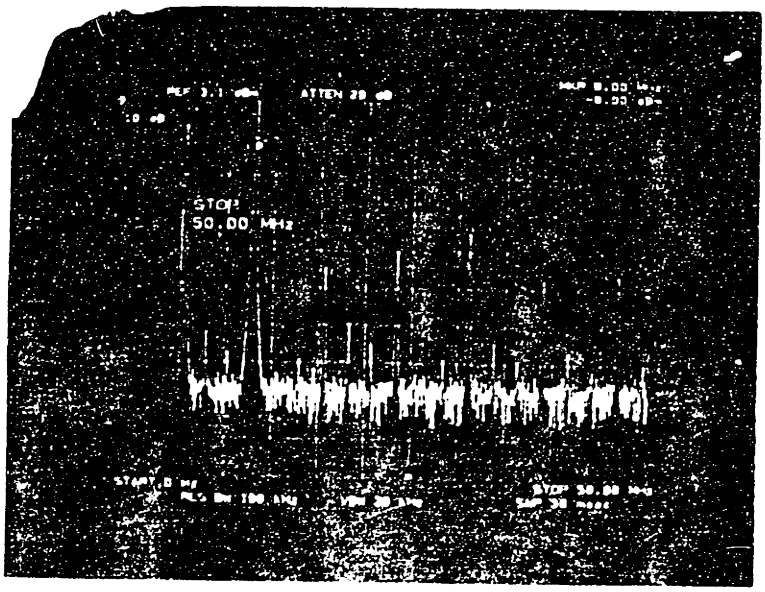

Figure 5.32 - Clock frequency 500 MHz 64-step sine wave.

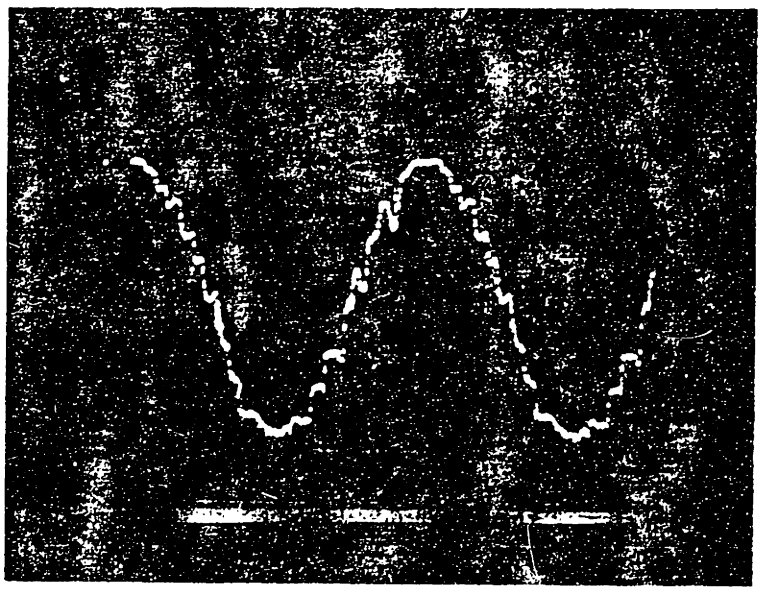

Figure 5.33 - Clock frequency 600 MHz 16-step sine wave.

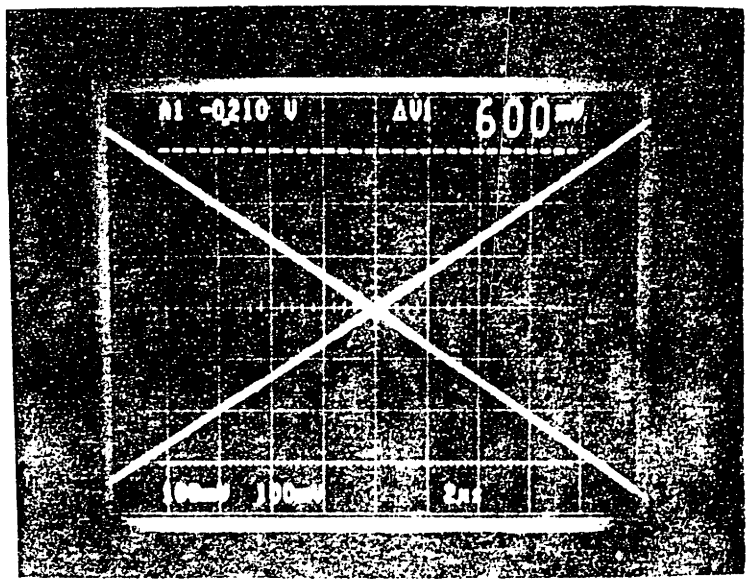

Figure 5.34 - Clock frequency 120 MHz 4096 step triangle wave.

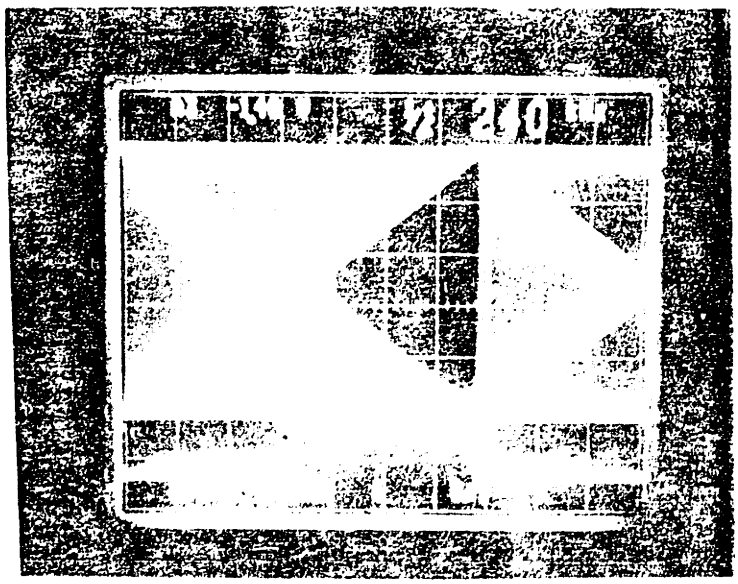

Figure 5.35 - Clock frequency 120 MHz 4096-step triangle wave with alternating 60 MHz blanks.

A summary of the digital-to-analog converters best performance is presented in Table 5.3. The data is taken from a sample size of ten devices from one 4-inch wafer composed of 114 reticles.

Table 5.3 - 12-bit Digital-to-Analog Converter Best Performance

Param.	Description	Min	Typ	Max	Units	Condition
D_{su}	Data Setup Time	500			ps	With respect to clock rising edge
D_H	Data Hold Time	150			ps	
S_{su}	Select A/B in Setup Time	500			ps	
S_H	Select A/B in Hold Time	150			ps	
$SYNC_{su}$	Sync Setup Time	500			ps	
$SYNC_H$	Sync Hold Time	150			ps	
$BLANK_{su}$	Blank Setup Time	500			ps	
$BLANK_H$	Blank Hold Time	150			ps	
T_{cs}	Clk to Select A/B Out Delay			850	ps	
VF_{max}	Output Update Rate	500	700	1000	msps	
$t_{settling}$	Output Settling	0.6	0.8	1.0	ns	$R_L = 50\Omega$
t_{pd}	Output Propagation Delay	3.2	3.2	3.4	ns	
G_i	Glitch Impulse	23	25	27	pv•s	
SR_D	Analog Output Slew Rate	2300	2380	2440	v/μs	
t_{rt}	Analog Output Rise Time	400	420	480	ps	
t_{ft}	Analog Output Fall Time	400	420	460	ps	
c_i	Input Capacitance	2	2.0	3.0	pF	
Sp	Max spur @ $f_o = f_{clk}/256$	-78	-56	-46	dBc	
f_{clk}	Clock Frequency	500	700	1000	MHz	

Chapter 6

Mixed-Mode Process Circuits Applications

The p^+ ohmic contact bulk bias with n^+ ohmic guard ring GaAs MESFET process can be applied to circuits operating with input/output signal voltage swings and voltage power supply levels significantly above an individual device's breakdown voltage. Two circuit applications were selected that previously were difficult designs for a standard GaAs MESFET process. These circuit designs are: 1) a high-voltage current source described in section 6.1 and 2) a high-voltage comparator described in section 6.2. Each design was simulated with the HSPICE models developed in Chapter 2 to predict performance of the p^+ ohmic contact bulk bias with n^+ ohmic guard ring GaAs MESFET process.

6.1 High-Voltage Current Source

A high-voltage-swing current source composed of a series of boot-strapped current sources was designed to overcome the Vitesse GaAs MESFET process 4 volt breakdown voltage limitation. Figure 6.1 shows the schematic of the high voltage swing current source implemented with a series of isolated current sources whose design is described in section 4.2. Figure 6.2 shows the simulated voltage drops across each current source as the load voltage is swept from -4 volts to +8 volts. Notice that the maximum voltage drop across any one of the source bootstrapped current sources is 4 volts. Figure 6.3 shows the output current of the circuit as the voltage is swept from -4 volts to +8 volts. In each simulation case the top supply rail voltage is +12 volts.

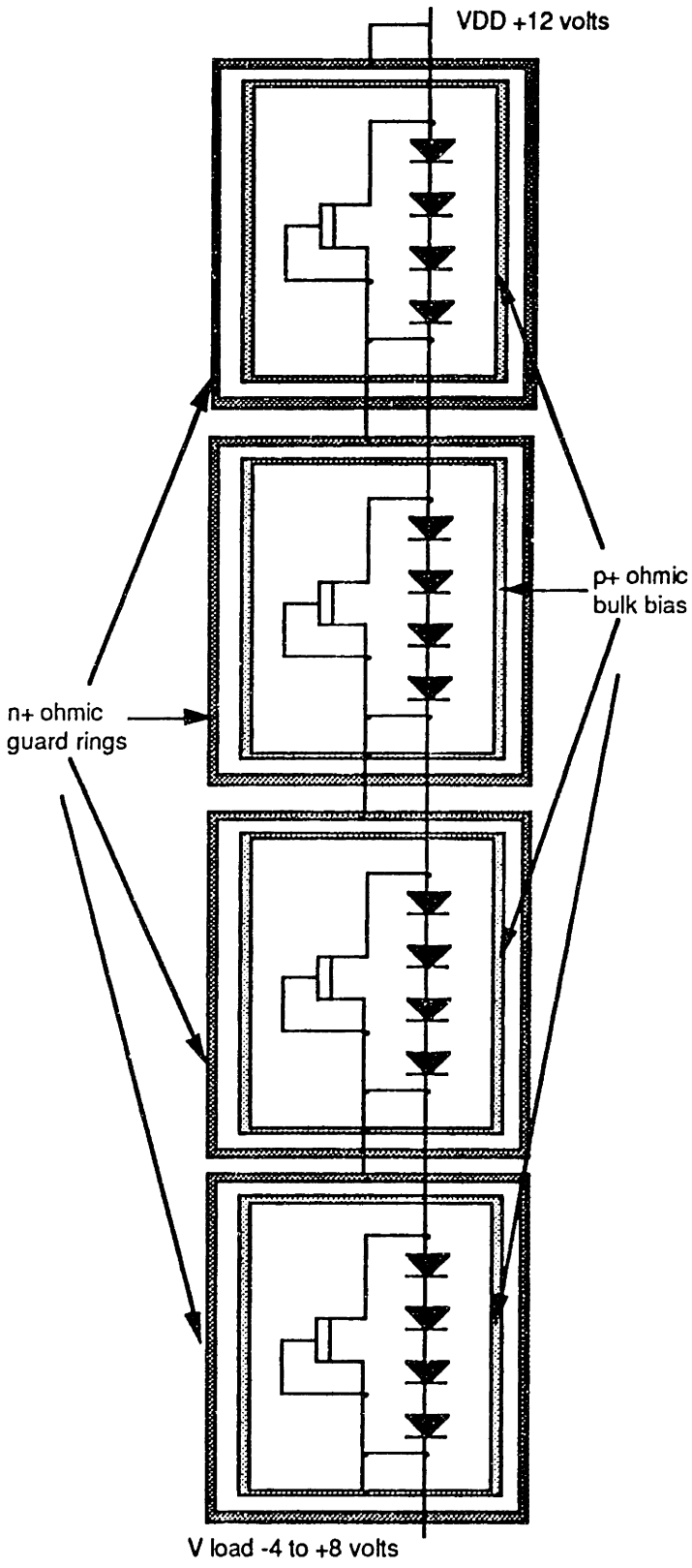

Figure 6.1 High voltage current source schematic composed of a series of isolated current sources

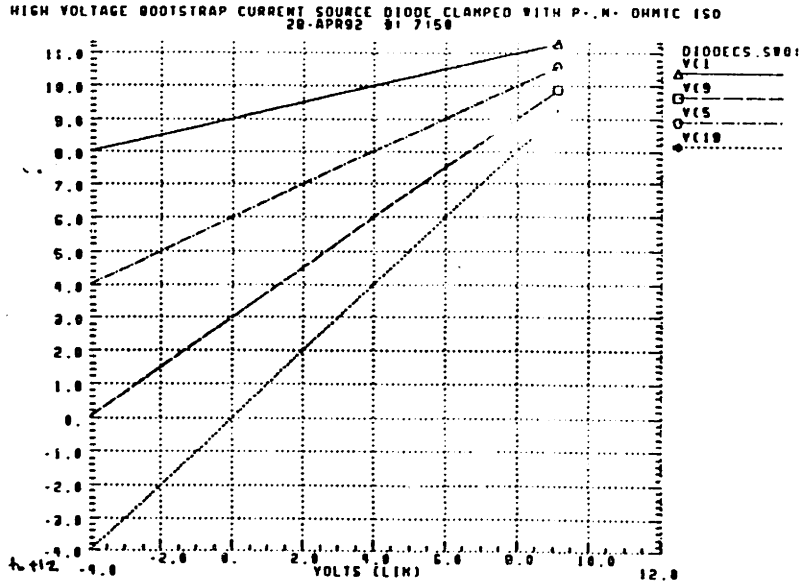

Figure 6.2 - Voltage drops across each of the stacked current sources as the load voltage is swept from -4 to +8 volts

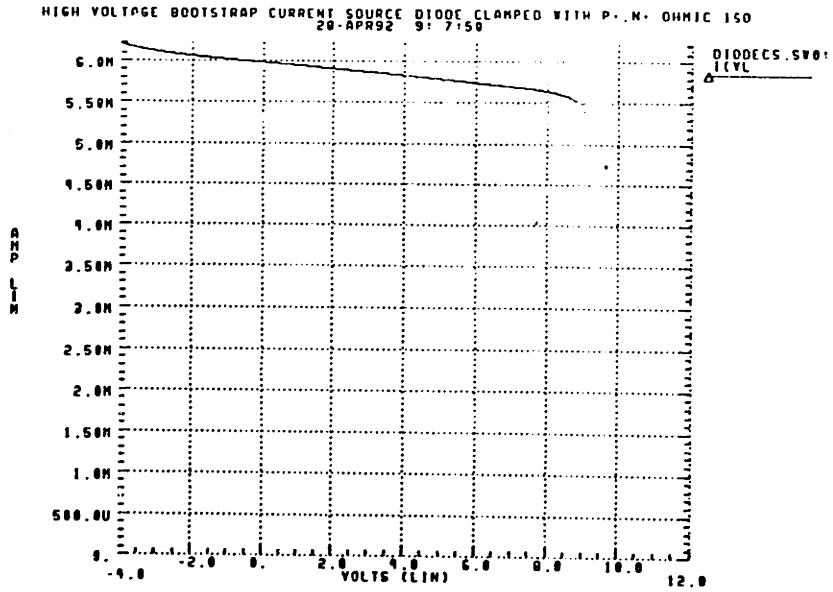

Figure 6.3 - Current output of the stacked current sources as the load voltage is swept from -4 to +8 volts

If the individual current sources were perfectly matched, the small clipping diodes would not be required because the voltage drop developed across each current source would be equal. The size and number of clipping diodes are set by the maximum expected

current mismatch between devices and the maximum voltage drop allowed across each current source. To demonstrate how the diodes insure that a maximum voltage drop of 4 volts is maintained across each current source, the widths of the depletion-mode device of the each current source were varied by 5 % . Figure 6.4 shows the resulting nonlinear voltage drops across each current source and can be compared to that of Figure 6.2. Figure 6.5 shows the current output of the mismatched circuit and can be compared to that of figure 6.3. The large backgate effect found in a conventional GaAs MESFET process would make this circuit current output versus load voltage and impedance versus voltage highly nonlinear. These high nonlinearities would make use of the conventional GaAs MESFET process circuit impractical in most designs. The use of p^+ ohmic contact bulk bias and n+ ohmic guard ring process isolation opens up the possibility high voltage GaAs MESFET design. Several circuit design techniques were developed based on this topology and were applied to the design of a high voltage receiver comparator described in section 6.2.

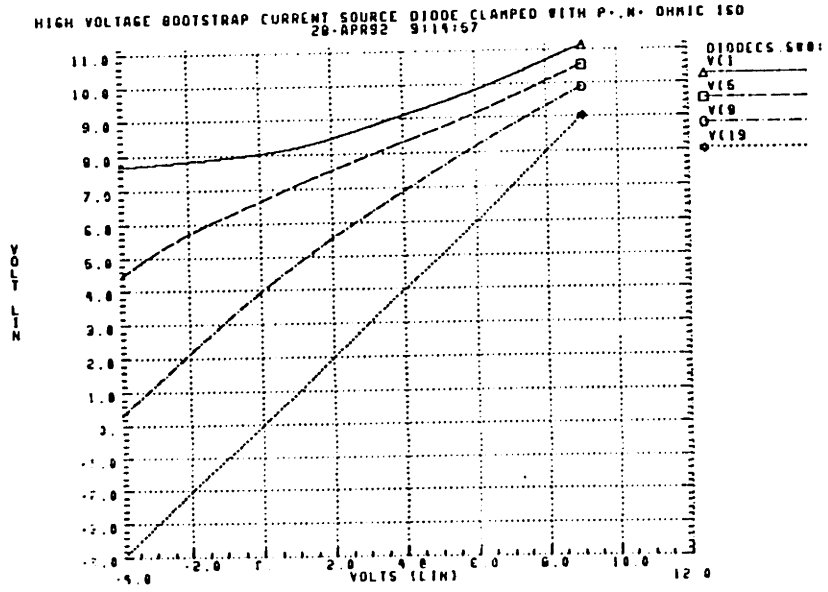

Figure 6.4 - Voltage drops across each of the 5% mismatches stacked current sources as the load voltage is swept from -4 to +8 volts

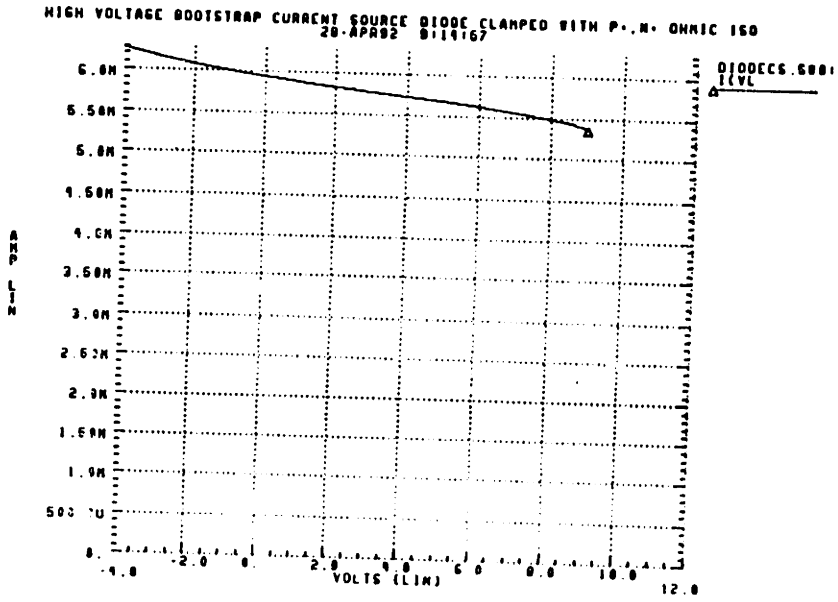

Figure 6.5 - Current output of the 5% mismatched stacked current sources as the load voltage is swept from -4 to +8 volts

6.2 High Voltage Swing 10 mV Resolution Comparator

A 10 mV comparator resolution can be achieved in the enhanced GaAs MESFET process technology by employing averaging and centroiding layout techniques. Enhanced process differential pair threshold data was taken on a single wafer with p^+ ohmic contact isolation. Table 4.4 shows the average and standard deviation of the difference in threshold voltage of 40 and 10 μm wide by 1.2 μm enhancement mode and depletion mode differential pairs designed as identical copies of 10 μm wide by 1.2 μm long discrete devices connected in parallel and arranged in a common centroid pattern. The measured data shows that a 40 μm enhancement-mode MESFET V_T's will match to 6.8 mV with a standard deviation of 4.8 mV. Designing the comparator with a 250 μm wide by 1.2 μm long enhancement mode differential input pair with each transistor of the pair composed of 25 identical copies of 10 μm wide by 1.2 μm long devices connected in parallel and arranged in a common centroid pattern will further reduce the standard deviation of the measured 40 μm wide by 1.2 μm long differential input pair data by $(4/25)^{1/2}=2/5$. This

analysis assumes that the discrete device thresholds have a gaussian distributions and that the common centroiding reduces the effects of thermal gradients. It also assumes that the differential pairs backgates are uniformly biased at the common source voltage potential. Note that the large differential pair device geometry is not a detriment to this approach because the large miller capacitance of the input pair is eliminate through the use of cascode topology where the cascode transistor is much a smaller depletion mode device.

A detail schematic of the averaging and common centroid offset cancellation type comparator is shown in Figure 6.6. The current source loads and tail current are designed with the above described high voltage swing current sources. The enhancement mode differential pair V_{DS} is constrained by the series floating depletion-mode cascode transistors. HSPICE simulations of this topology with the reference voltage set at -2, 0, +2, and +4 volts are included in Figures 6.7 - 6.10. Notice in all cases this stage of the comparator exhibits again greater than 200 (2/0.01) with a unity gain bandwidth greater than 2 GHz. The internal node voltage around each current source transistor are displayed to show that no transistor's V_{DS} exceeds 4 volts.

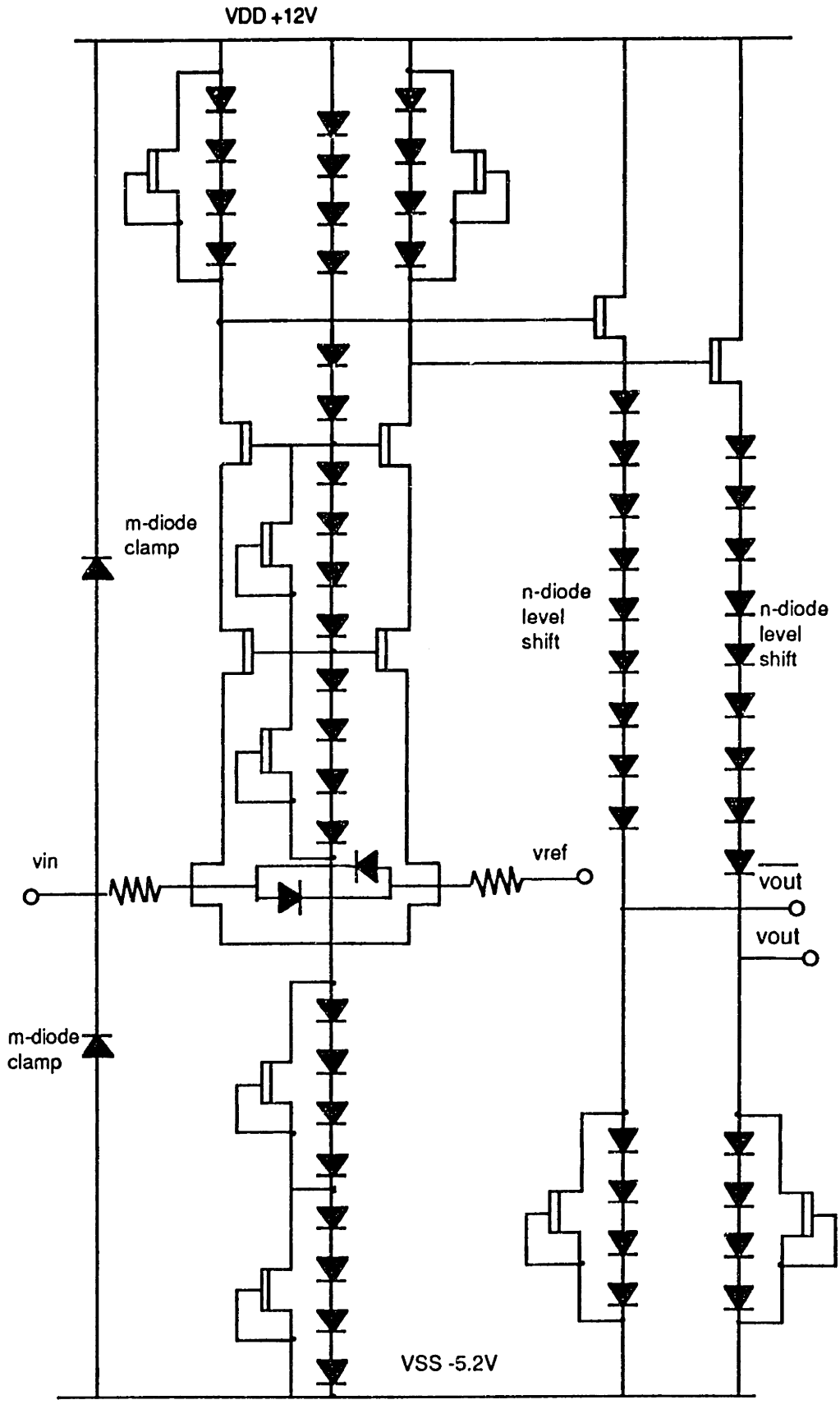

Figure 6.6 - Comparator topology.

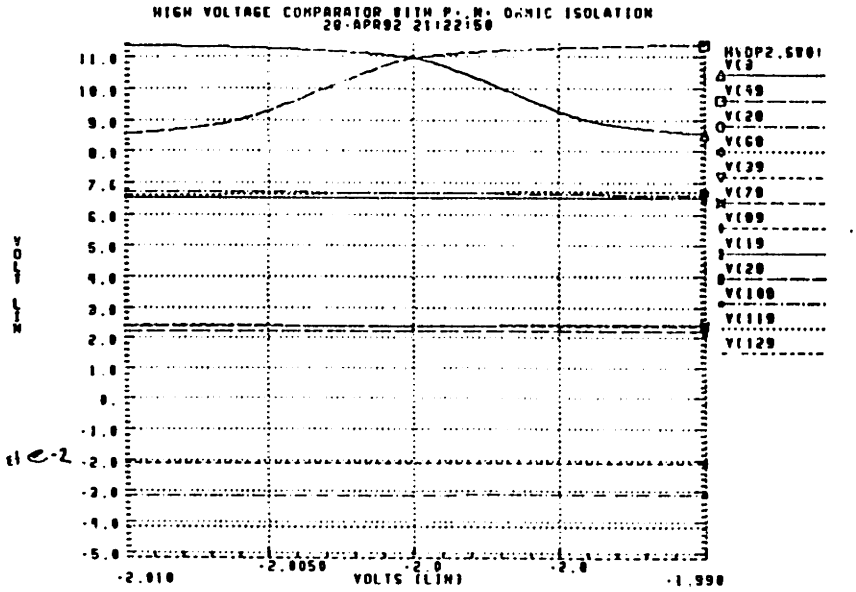

Figure 6.7 - Comparator output and internal node voltages for reference voltage of -2 volts.

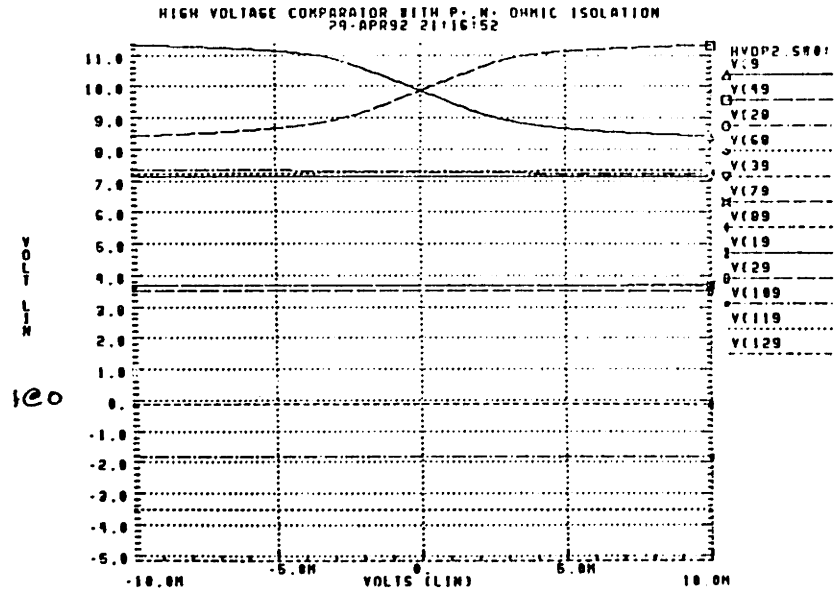

Figure 6.8 - Comparator output and internal node voltages for reference voltage of -0 volts.

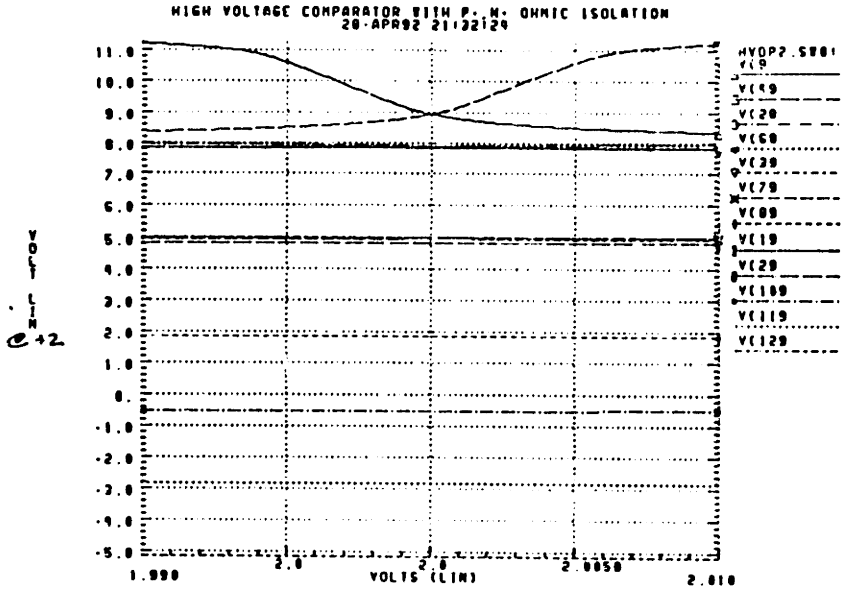

Figure 6.9 - Comparator output and internal node voltages for reference voltage of +2 volts.

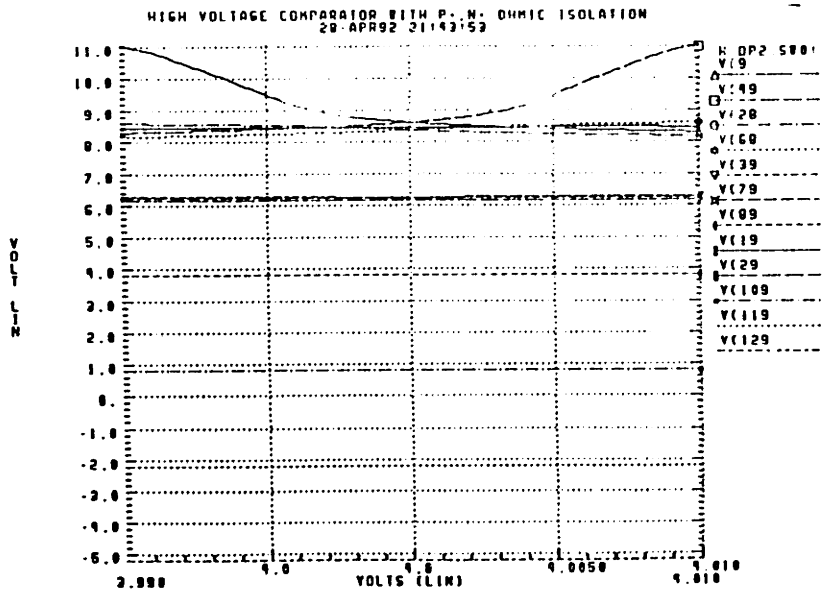

Figure 6.10 - Comparator output and internal node voltages for reference voltage of +4 volts.

In a final comparator topology the common mode rejection ratio would be increased through use of bootstrapped current sources that have improved performance. However,

the results to date are encouraging and do indicate that a 6 volt input range can be achieved. Figures 6.11 and 6.12 show the comparator gain and phase.

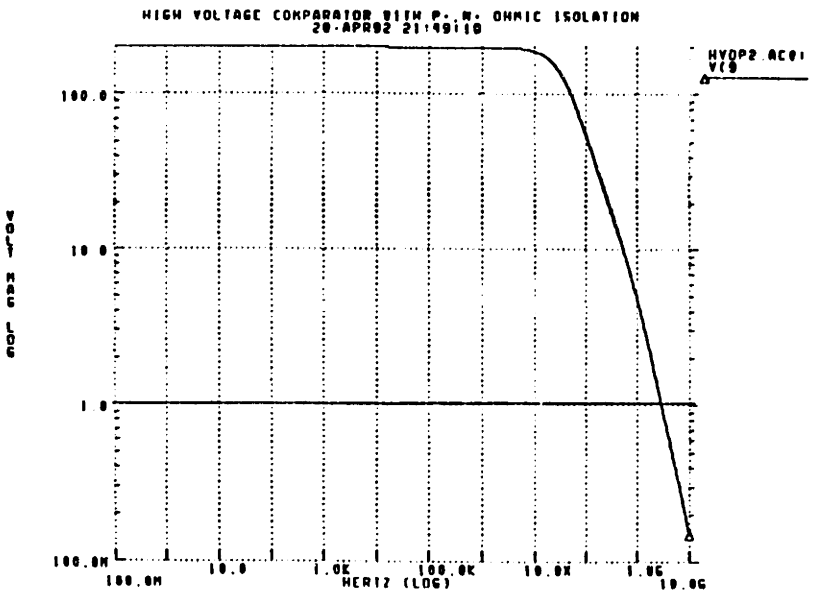

Figure 6.11 - Comparator small signal magnitude response showing a 2 GHz bandwidth

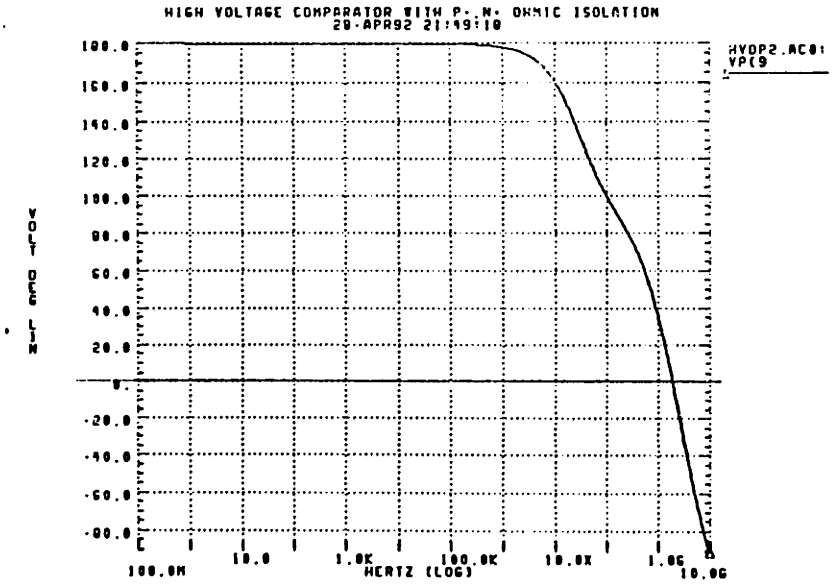

Figure 6.12 - Comparator small-signal phase response.

Chapter 7

Conclusion

The performance limiting attributes of a digital GaAs MESFET application to mix-mode circuit design were examined. A p^+ ohmic contact bulk bias and n^+ ohmic guard ring isolation GaAs MESFET process was developed that eliminates these limitations. Test circuits were designed, simulated, and fabricated in this process that show improved bulk isolation and reduced frequency-dependent output conductance. Using these process isolation and circuit techniques, a monolithic 12-bit digital-to-analog converter was designed in the Vitesse digital gallium arsenide (GaAs) MESFET process. Samples of the fabricated devices were measured to be 12-bit monotonic with integral nonlinearity of 2 LSBs and differential nonlinearity of 1 LSB. The device's full dynamic range was tested at a maximum clock of 500 MHz. Discrete bits were tested at 1 GHz. The 1.6 watt digital-to-analog converter was designed using the p^+ ohmic contact ring isolation and n^+ ohmic guard ring isolation GaAs MESFET process with power supply voltages of ground, -2 volts, and -5.2 volts. In addition to the digital-to-analog converter design, a high-voltage comparator and high-voltage current source circuit were designed. Both circuits operate at supply voltages of 16 volts, which is a factor of four higher than the nominal transistor breakdown voltage.

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Biography

Peter Nuytkens is on leave from the Charles Stark Draper Laboratory, Inc., in Cambridge, MA, where he was Chief of the Sensor Systems Microelectronics Section. At Draper, he was also the program manager and principal designer of the Enhanced Direct Digital Frequency Synthesizer (EDDS) program, leading the research and development effort from his initial architectural concept (U.S. Patent #4,933,890) through GaAs VLSI device implementation.

He graduated with distinction with a B.S.E. in Biomedical Engineering from Duke University in 1981.

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U.S. Patents

Direct Sequence Digital Receiver Architecture #4,841,544

Direct Digital Frequency Synthesizer #4,933,890

U.S. Patents Pending

A GaAs MESFET Dual 10-bit Phase Shifter with 1 psec Resolution

A 2-volt Enhancement and Depletion Mode MESFET GaAs Opamp

Negative Resistance Voltage Controlled Oscillator

Heterojunction Acoustic Charge Transport (HACT) Automatic Calibration

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Awards

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