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**The Globalization of R&D's Implications for Technological Capabilities in MNC Home Countries:  
Semiconductor Design Offshoring to China and India**

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**Abstract:**

This paper addresses the empirical question of the impact of the offshoring of semiconductor design to India and China on the generation of semiconductor design skills in the offshoring multinational corporations' (MNCs) home countries. There are four main findings. First, there is a specific technology skill ladder for training "design leads" or design managers within this industry that entails direct exposure to a wide range of design activities. Thus, offshoring has potentially serious implications for development of further design leads. Second, the paper also finds that the impact on skills activities and thus potential skills generation at home from offshoring to India has been limited and gradual and from offshoring to China has been even more limited although the activities done in each country by MNCs have risen over time. Third, the fuzzy set qualitative comparative analysis pinpoints that the operations with design leads and large design teams in 2003-2007 in conjunction with other attributes are generally the ones that pursued the most extensive offshoring of semiconductor design during the subsequent 2009-2013 period. Finally, the evidence for a gradual process of offshoring from the second and third points suggests that offshoring in semiconductor design will most likely not displace the large amount of design activities in the home countries of the MNCs in the near future.

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**Key Words:** China; India; semiconductors; globalization; R&D; outsourcing

## Introduction

This paper addresses the empirical questions of the impact of the offshoring of semiconductor design<sup>1</sup> to India and China on the generation of semiconductor design skills in the developed home country of the offshoring multinational corporation (MNC) and the development of technical skills in the host country. This paper refers to both moving a company's own activities abroad and the outsourcing of technical activities to external actors abroad as offshoring. However, the analysis differentiates between internal offshoring and outsourcing. The offshoring companies in the study are fabless design firms and integrated device manufacturers (IDMs)<sup>2</sup> headquartered in developed economies. The offshoring sites under study are India and China because these developing world locations are near the top in the hierarchy of foreign R&D locations (Contractor et al 2010; D'Agostino et al. 2013) as well as being major locations for semiconductor R&D offshoring in the developing world (Brown and Linden 2009).

The core issue of the paper is the effect of offshoring on innovation capabilities in the original home base using the case of semiconductor design. Much of the debate over the impact of offshoring on innovation has arrayed a group of proponents of globalization optimistic about the benefits of offshoring outweighing the costs (Bhagwati 2004; Mann 2003) against those more pessimistic about the costs of offshoring on wages and employment opportunities at home (Freeman 2005; Gomory 2010; Gomory and Baumol 2000; Hira 2003, 2005; Samuelson 2004). There have been empirical studies that explore the impacts of offshoring on advanced OECD economies' workforces from the wider perspective of globalization's effects on employment (Autor *et al.* 2013; Kletzer 2001; Feenstra and Hanson 1996),

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<sup>1</sup> This paper will use the terms semiconductor, integrated circuit (IC) and chip interchangeably to describe the industry and product category under study although the author recognizes the technically broader meaning of semiconductor vis-à-vis IC.

<sup>2</sup> Fabless design firms are firms that design but do not fabricate (manufacture) chips. IDMS are firms that combine the design and fabrication functions in-house.

and ones that directly investigate the connections between offshoring to employment outcomes in advanced economies (A.T. Kearney 2004; Hira 2003, 2005; Sturgeon 2006). Other studies have taken a global labor supply perspective by evaluating the numbers of engineers trained and their quality across offshoring countries and major sites of offshoring, such as China and India (Gereffi and Wadhwa 2005; Freeman 2005; McKinsey Global Institute 2005; Simon and Cao 2009). Brown and Linden (2005; 2009) have addressed both the employment and foreign supplies of engineering talent issues for the semiconductor industry specifically. Others have addressed the issue in terms of the extant or imminent loss of competitiveness and/or the ability to innovate on the part of the outsourcing country, particularly the United States, although there are disagreements over whether offshoring is the cause or the effect of eroding competitiveness and declining innovation capabilities (Gomory 2010; Grove 2010; SIA 2009; AEA 2005; NAS 2005, 2010).

There is also a very large literature on the motivations for offshoring<sup>3</sup> with recent examples emphasizing the expanding scope of service offshoring (Kenney *et al.* 2009). For the semiconductor industry, scholars generally have acknowledged a mix of some of the same factors that traditionally determine location of activities including proximity to customers/markets, cost advantages and access to skilled labor motivate offshoring in semiconductor design (Brown and Linden 2009; Ernst 2004). Ernst (2004) for the semiconductor industry and Lewin and his colleagues (2009) and Thursby and Thursby (2006) for a wider scope of innovation activities emphasize the demand for skilled labor emanating from multinational corporations (MNCs) combined with the increasing supply of quality engineers in many Asian offshoring sites as important drivers behind offshoring of innovation activities. Contradicting claims about the globalization of R&D, Macher and his colleagues (2007) have questioned the extent of

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<sup>3</sup> See Lewin et al (2009) for extensive review of this literature on the causes of offshoring.

globalization of semiconductor R&D based on analysis of R&D investment and US patent data, but their data analysis stops at 2001 and 2003 for investment and patents, respectively.

The debate over the impact of offshoring for innovation, especially in semiconductor design, has generally not focused on the micro-level investigation of innovation activities within firms' offshoring sites. Micro-level research is particularly important for assessing what specific activities are being moved offshore because it is precisely these activities that are hard to observe from more macro-level data of flows of investment, patents and employment.<sup>4</sup> Furthermore, a micro-level analysis can provide leverage on the issue of whether specific activities placed offshore are actually displacing specific activities at home that are critical for future skills generation there. In effect, the micro-level analysis gives insight into whether or not training regimes at home continue despite offshoring.

The paper has four main findings. First, from interview interlocutors, the paper uncovered a technology skills ladder within the IC design industry in which a design engineer progresses through a number of steps in order to become a design lead, effectively a manager in charge of whole design projects. Progression up this ladder requires hands-on exposure to a wide range of design activities. Second, the paper also finds that the impact on skills activities and thus potential skills generation at home from offshoring to India has been limited and gradual and from offshoring to China has been minimal although the activities done in each country by MNCs have risen over time. Third, to the extent that there has been a significant increase in sophisticated offshore IC design, it is driven by firms with existing design leads and substantial design operations offshore. This finding helps to explain why more extensive offshoring has occurred in India due to the greater MNC activities at an earlier date there than China and demonstrates that the offshoring of design activities by MNCs is typically a quite gradual

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<sup>4</sup> An excellent example of this type of analysis is Fuchs and Kerchain (2005) although they analyze the impact of offshoring in a manufacturing sector.

process in which local subsidiary capabilities accumulate over relatively long periods of time. This gradual process points to a final finding that offshoring of design to India and China will most likely not displace the large amount of design activities in the home countries of the MNCs any time soon. In other words, the slight shifts of activities from MNC home bases to India and China that have occurred are best measured in decades or half-decades rather than years and further shifts in the future will likely take equally long. Given the relatively high speed of the product life cycle in the IC industry, it is particularly striking how relatively slow the offshoring has been.

In India, MNCs have offshored wholly owned operations and outsourced to local firms, but these MNCs have kept design functions up and down the ladder at home as well. Among the MNCs, American ones are the most active in offshoring activities to India, but this pattern of keeping design functions at home holds true for non-American firms as well. Furthermore, the ability of local teams in India to undertake design leadership remains relatively weak if improving. Therefore, offshoring does not seem to have heavily impacted the training and skills regime at home thus far. For China, the MNCs have been quite wary about outsourcing to local firms and have been cautious in deepening the technical capabilities of their own design operations in China.

This paper proceeds as follows. The first section addresses the methodology and data. The second section describes the skill ladder in semiconductor design. The third section describes MNCs' activities in India and China in 2007-2008, assesses the impact of these 2007-2008 activities on whatever subsequent shift in activities from the MNC home countries towards China and India occurred in the 2009-2013 period and consequently the impact on skill ladders in IC design in the MNC home countries. This section employs interview data, patent data and fuzzy set qualitative comparative analysis (fsQCA). The conclusion, drawing on the smaller set of follow-up interviews in 2014-2015, discusses the issue of how sustainable skills ladders in offshoring MNC home countries are in the medium-term in the face of the developing industry activities in India and China.

## 1. Methodology and Data

This paper presents both qualitative data gathered from semi-structure interviews and quantitative data on US utility patent holdings. In terms of the qualitative data, the research employed the grounded theory approach to data gathering and analysis of institutions (Glaser and Strauss, 1967; Strauss, 1987; Strauss and Corbin, 1990). The purpose of this approach is to explore social phenomenon in order to build theory. Theory building encompasses a range of analytic tasks including concept creation, identifying causal relationships and patterns of behavior. The qualitative grounded theory approach provides opportunities to create new understandings rather than a method to provide rigorous, empirical testing of existing theories, an area where various quantitative methods may be more useful. Out of our qualitative research we came up with the concept of the technology skills ladder in IC design.

From 2007 to 2008, our team interviewed in China and India 21 of the top 75 global publicly listed semiconductor firms by 2006 sales revenue<sup>5</sup> and 19 of the top 50. We also interviewed critical suppliers for IC design, such as intellectual property vendors and electronic design automation (EDA) tool vendors. Given the sensitive nature of the topics covered in the interviews, our team promised to keep the interview subjects' individual and corporate identities anonymous in any research output. However, it can be stated that our interviews with the IC design operations of MNCs were all conducted with high-level managers of these operations. Through this set of interviews with diverse industry participants, we were able to triangulate data in order to ensure reliability. Our interview data provided

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<sup>5</sup> List of top firms is from Hurtarte *et al.* (2007), pp. 235-237. This list excludes pure-play foundries and assembly and testing firms as well as IC industry suppliers, such as EDA tool vendors and semiconductor capital equipment makers.

information with wider generalizability for two additional reasons. In India, we took a census approach and were able to interview 28 of the 42 firms listed as being active in IC design in India as of 2007 according to the Indian Semiconductor Association (2007:5). In China, there was no comprehensive list of industry participants so we could not undertake a census. Nevertheless, the firms we interviewed employed 4,153 members of the IC design population, which is approximately 40% of the total population of such workers during 2007-2008.<sup>6</sup> In 2007-2008, we interviewed 19 MNCs in India and 10 MNCs in China. The smaller number of MNCs interviewed in China reflects the smaller role these firms play in China's industry as demonstrated in past research (Bhaumik et al. 2009). There were follow-up interviews in 2014-2015 with 13 and 8 MNCs in India and China, respectively.<sup>7</sup>

Most of MNCs interviewed are from the United States although MNCs from Europe, Japan and Korea were also interviewed. This apparent selection bias can at least be partially explained by the facts of the large size of the US industry and its relatively fragmented organization of production vis-à-vis the more vertically integrated firms of Europe, Japan and Korea (Macher *et al.* 1999). With a large size and fragmented production, there are more American MNCs active in this industry as both integrated device manufacturers (IDMs) and the numerous American fabless design firms (Hurtarte *et al.* 2007) have

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<sup>6</sup> If we estimate that the population of IC designers was approximately 10,000 in 2007-2008 given the figures of 7000 in 2004 and 15,000 in 2011, then our team covered 41.5% of the population of IC designers. Furthermore, the wider set of 87 interviews conducted with industry in China in the 2007-2008 period provide confidence that most of the MNCs with significant design operations at that time were identified and interviewed (Fuller 2014).

<sup>7</sup> The fsQCA analysis only makes use of the MNCs initially interviewed in 2007-2008 because the paper aims to capture the effects of the design activities in offshore operations in this period on subsequent development of activities in the same offshore operations. The MNCs interviewed in 2014-2015 but not previously interviewed in 2007-2008 are unlikely to yield accurate data about the situation of the MNCs' Chinese and Indian operations in 2007-2008 due to faulty recollections of events seven or eight years before and the rarity of having the same senior management in place over seven or eight years because of the typical relatively rapid turnover of such personnel in MNC design operations. Even for the MNCs interviewed in both periods, the interviews in 2007-2008 are likely to yield more accurate information given the two reasons stated above.



offshore design activities. MNCs from Europe, the US, Japan, Korea and Taiwan still dominate the industry with the top 20 firms in sales in both 2006 and 2016 hailing from these countries.<sup>8</sup> The local firms in India and China tend to be much smaller than the MNCs in terms of revenues and employment (Fuller 2014).

The patent data employed in this paper is US Patent and Trademark Office utility patent data for 2003-2007 and 2009-2013. The paper uses this data to compare the design activities ending at the start of the interview period (2007-2008) with the design activities that occurred in the subsequent, post-main interview period of 2009-2013. The patents not only provide an external check to the interview data regarding firm-level activities, but also contribute critically to the fsQCA in Section 3. The fsQCA method is useful in exploring different causal recipes for an outcome combining set theoretic quantitative methods and qualitative insights of the researcher (Ragin 2008). Section 3 employs fsQCA in order to see what attributes of MNC design subsidiaries lead to greater offshoring in the post-interview period of 2009-2013. Section 3 explains the details of the fsQCA methodology employed in this paper.

## **2. Technology Skill Ladder in Semiconductor Design**

Before discussing the technology skill ladder in IC design, an explanation of the processes involved in designing an integrated circuit (IC) is in order. The design flow generally follows along the following path. The path goes from a conception of how the chip will operate within a larger electronics system (architecture stage) through to the use of various design languages to define the circuitry moving from greater to lesser levels of abstraction [behavioral to register transfer level (RTL) to gate level design]

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<sup>8</sup> The 2006 data are from Hurtarte et al. 2006 and the 2016 data are for the first half of 2016 and downloaded from <http://www.analog-ectimes.com/news/amd-mediatek-show-good-form-chip-vendor-ranking> on September 1, 2016.

in the process. These processes along with the architectural level are commonly referred to as front-end design. The back-end of design consists of the processes of implementation of these abstract designs into a design for real physical components and connectors embedded in silicon. Generally, the front-end is considered more technically sophisticated than the back-end. As Hurtarte and his colleagues (2007: 50) put it in reference to fabless design firms, “In fact, the architecture and RTL implementation of the device is usually the core differentiating aspect of the company’s design.”

Drawing on the experience of two electrical engineering professors who are part of our research team and co-authors, our concept of a technology skill ladder in semiconductor design developed through our initial interviews in 2007-2008. Our subsequent interviews in 2014-2015 served to provide confirmation from interview subjects that the technology skill ladder concept reflected actual industry practices as experienced industry participants understood them.

Based on the research and industry knowledge of our team, we conceptualized the skill ladder or “apprenticeship” system for training skilled designers and design managers in the IC industry as one that followed these approximate steps on the design skill ladder:

- **Entry-level:** initial two years of design work with entry at any point in the design flow
- **Independent responsibilities:** 2+ years: independent work on one or more segment of the design flow discussed above
- **Assistant design team lead (co-lead):** 4+ years: with previous exposure to multiple segments across the design flow, the engineer can now assist in managing the team covering the whole design flow
- **Design lead:** 5+ years: with direct experience or managerial experience across the design flow, the engineer can now manage a chip project along the entire design flow to completion (see footnote 9)

Following information provided by interview subjects, this paper defines design leads as those managers in charge of chip design teams with the task of overseeing the full and complete design flow of a chip from architectural definition to (at least)<sup>9</sup> post-layout verification. Design leads need at least five years of experience and often require much more.

The experienced required for each of these steps, particularly the co-lead and design lead steps, depends on the technical complexity of the chip to be designed. The interviews suggested that the design leads overseeing large, complex chips tend to need closer to ten years' experience **in large part because they need the time to acquire deep knowledge of the bigger technical challenges of front-end design that are entailed in this large chips.** Also, analog and mixed signal (AMS) chip design require much more experience (minimum of eight to ten years) to become a design lead **as advanced analog or mixed analog-digital designs require greater design-for-manufacturing knowledge and analog design is less software coding-enabled than digital design.** Under these design leads, there usually are one or more assistant design managers or co-leads as they are often referred in the industry terminology. These co-leads have at least four years of experience, but like design leads, they usually have much more experience (seven or eight years minimum) when involved in co-leading complex chips. Generally speaking, designs have increased in complexity over time so the experience needed to become a design lead has increased over time.

What is important to note is that an engineer gains a broader skill set based on exposure and experience across the design functions discussed above as the engineer moves up the technology skills ladder in IC design. **Experience is necessary to move up to assistant design and design lead because**

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<sup>9</sup>Depending on the organization of a given firm, some design leads take charge of shepherding the chip through fabrication and assembly and testing in addition to the design of the chip.

time is simply needed to expose the engineer to a number of functions either as an engineer directly involved in that function or, in the case of moving up to design lead, as an assistant design lead having indirect exposure via helping to manage a function as part of the design flow. The different skills required along the design flow thus also require a manager who has direct experience across a number of these functions and at least indirect experience via managing as an assistant design lead to bring a chip project to completion. In other words, the cross-functionality necessary to design a chip means engineers need time to garner experience across these functions before leading such a design project. Conceivably, one could start one's training in chip design from any of these separate design functions, but it is rare to start from the architecture stage due to its inherent greater complexity and need to have a wider perspective of the system and how chip design fits into that system that only usually comes with experience. It is also important to note that graduate training in electrical engineering, typically two years for a master's and six years for a doctorate, counts as partial experience within this skill ladder so a graduate with a master's degree could quickly ascend to independent capabilities and a holder of a PhD would at least start at the independent capabilities level given their experience and exposure to IC design within their graduate training.

The cumulative and cross-functional characteristics of the technology skills ladder in IC design suggests that the ladder may be a delicate one dependent on the continued existence of the full array of design functions at home in order to provide the opportunities to gain the varied experience necessary to become a design lead. Conceivably, if certain design activities were moved offshore completely, then the skill ladder would no longer continue to function to produce design leads and other experienced design professionals necessary to maintain the home country's competitive edge in semiconductors. For without exposure across a number of functions, an engineer is very unlikely to have the requisite training to be able to manage the cross-functional process inherent to designing chips.

In the bifurcated labor market for experienced engineers in the US that Brown and Linden (2009) document, the experienced engineers selected for training and managerial positions are the engineers recognized as design leads and co-leads in this paper. Other experienced engineers in the US semiconductor design face bleaker prospects of atrophying skills because they have not been selected for in-house training as firms prefer hiring new graduates to training experienced engineers in new skills (Brown and Linden 2009: 122-123). In the terminology of this paper, the latter engineers are the ones stuck at the independent responsibilities rung of the skills ladder when firms are reluctant to invest in them through the provision of the wider training and exposure across the design activities needed to allow them to become effective design leads.

### **3. MNC Offshore Design Activities' Impact on the Technology Skill Ladder at Home**

This section first provides an account of the design activities conducted by MNCs and their suppliers in China and India. Then the section considers these activities in the context of the maintenance of the technology skill ladders in home countries of the MNCs. Finally, the section employs fsQCA to examine which causes are propelling what limited offshoring is occurring in IC design.

Before discussing the activities in detail, we must place why MNCs have moved activities to India and China in its specific industrial context. In addition to the other drivers of globalization mentioned in the introduction, the central pressure facing MNCs involved in semiconductor design is that chip designs are becoming increasingly complex. The greater the complexity of a given chip the more engineering hours required to design said chip. The way to meet the challenges presented by the increasing complexity of designs is to hire more engineers or access them indirectly through outsourcing. To meet the challenge complexity and keep costs under control, firms want to access engineers in relatively low wage locations (Brown and Linden 2009: 68-69; Hurtarte et al 2007: 63-64). Thus, the MNCs have

become increasingly interested in India and, to a lesser extent, China as design locations since at least the start of this century.

The search for cheap engineer talent has led MNCs to India and China, but the impact of MNCs has had on India and China has been somewhat different. Both India and China are improving their technical capabilities at a swift pace and thereby narrowing their respective gaps with the international technology frontier in chip design. However, India has advanced further towards the international technology frontier than China has. One reason for India's better technical performance is the fact that MNCs have been willing to offshore more design work earlier to India than to China as our interview subjects confirmed. None of our interviewee subjects in India reported worrying about IP protection in India. In contrast, every interview subject in China in the 2007-2008 period claimed that protection of IP in China remained a concern. Some measurements of intellectual property rights (IPR) also indicate China still lags India in this area (Gwartney *et al.* 2006). Consequently, MNCs play only a supporting if growing role in China's industry (Fuller 2014).

### *3.1 Design Activities in India and China based on the 2007-2008 Interviews*

Several metrics serve to demonstrate how much more extensive activities of the MNCs are in India: the number of the design leads, the number of lead inventor patents, the number of designers, and the number of significant analog/mixed signal (AMS) teams.

Most significant semiconductor companies with design activities have a verified design presence in India whereas the number of active MNC design centers in China is limited.<sup>10</sup> Given our larger number of interviews in China, our research has a built-in bias of interviewing relatively more MNCs with activities in China. Therefore, it is still surprising that there were 19 MNCs (15 American ones) interviewed with design activities in India and only 8 such firms in China (5 American ones). However, the smaller fraction of MNC design centers as a share of semiconductor industry activity there is in line with interviewee's views of the industry in each country as well as patent data showing that the MNCs are much more active in India's semiconductor industry. For example, USPTO data on lead inventors for active patenting firms shows 83 patents from China from 2003 to 2007 and 333 patents from India in the same period (USPTO 2008ab). Brown and Linden's (2009) compilation of MNC design centers in China and India based on press reports about these MNC operations and some interviews finds a similar pattern of more MNC design activity. Of the 19 MNC design operations our interviews covered in India, ten were founded before 2000 whereas only four of the 8 MNCs in China were.

With the larger commitment of MNCs' to India in terms of both the number of MNCs that have design operations and the earlier start of many of these operation, MNCs' Indian design activities were unsurprisingly more technologically advanced and larger than the MNCs' Chinese ones in general in 2007-2008. Comparing design leads, five of the eight Chinese operations had design leads whereas fourteen of the nineteen Indian operations of MNCs did. The number of design leads and co-leads in MNCs' Chinese operations that had any design leads were smaller than their Indian counterparts. The size of the Indian design teams was also larger than the Chinese ones. Twelve MNC design teams in India employed more than 100 designers whereas in China only four MNCs did. Finally, only one MNC

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<sup>10</sup> It is important to remember that the returnee, foreign-invested but locally based firms are not included as MNCs. In any event, only one such firm was interviewed in India, as there are not many such firms in India.

had a large analog/mixed signal (AMS) design in China in contrast to six MNCs having had such teams in India.

### *3.2 Patent Data*

One can rightfully challenge the evidence from the interview data on several grounds. The data is self-reported and it comes from seven to eight years ago. The rest of this section will offer an empirical assessment what has happened since the 2007-2008 interviews based on external patent data. The patent data show that there has been an increase in the amount of R&D done in the host countries vis-à-vis such activity in the headquarters country of a given MNC for all of the Indian MNCs with design leads except one firm where the level of activity has remained flat and for most of the Chinese firms. The amount of activity happening among the leading MNCs in India is substantially higher than that in China although the 2003-2007 period already showed more such activity in India. This data suggest a slowly increasing impact on the home countries' design activities, and thus potentially their skill generation activities, from offshoring to India, but a much more minimal impact from offshoring to China.

<insert Table 1>

<insert Table 2>

Both tables show the absolute number of patents in which the lead inventor of the patent was based in the respective host economy, India or China, and then compare those patents as a percentage of the lead inventor patents created in the same time period in the MNC's home country. For India, three of the nineteen MNCs were excluded from the comparison for the following reasons. Two firms were large conglomerates that had many businesses outside of the semiconductor industry so their



patents would not likely reflect solely or even mainly their semiconductor industry activity in India.<sup>11</sup> Another firm was excluded because it was a creator of intellectual property blocks rather than full IC designs. For China, one of the same conglomerates excluded from the India sample was excluded. For China, the numbers for the MNCs also included in Table 1 were repeated (i.e. MNC 3 is the same firm in Tables 1 and 2). For India, there was a general correspondence to the depth of activities and the amount of lead inventor activity relative to such activity in the HQ country for the firm, especially in the second (post-interviews) period (2009-2013). For China, there were fewer firms and more of these firms were still doing very little or no such patenting activity even in the second period. For all the firms with operations in both India and China, the Indian operations were producing more patents in the second period as shown in Table 3. While both host countries witnessed movement of more patenting activities onshore relative to the activities undertaken in the MNCs' home economies, for China the base line of the earlier period was so low that such a shift does not yet suggest much more than a minimal impact.

<insert Table 3>

### *3.3 Implications for Skill Ladders Derived from Interviews and Patent Data*

While clearly more and more sophisticated work has been moved to India, the data we have collected through our research suggests that MNC offshoring of IC design activities to India and China has not displaced the skills ladder in the MNCs' respective home countries. The discussion here will focus on MNCs' Indian design activities because these activities are much larger and more sophisticated.

There are two principal reasons the MNCs have not displaced parts of the skill ladder at home: workforce recruitment and retention, and labor supply constraints.

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<sup>11</sup> One of these firms had both design leads and a large design team of over one hundred engineers so Table 2 only shows 13 such firms whereas the data mentioned earlier in the paper mentioned 14 such firms.

Although 14 of the 19 MNCs had design leads in India, this did not mean that these firms were getting rid of specific activities and skills onshore. Not one firm appeared to be offshoring anything approaching an entire functional category of work overseas. Even for the four MNCs' operations that had reached a high-level of maturity in which they "owned" chips i.e. were responsible for the design of a line of chips, there was no evidence of any such movement. Furthermore, three of these four firms interacted extensively with non-Indian personnel in designing the chips "owned" by the local design center. The one subsidiary that had its own independent line of chip products (it had even achieved the distinction of being its own independent profit and loss unit) and did not interact much at all with the rest of its parent MNC abroad did so because its product line is a legacy memory chip no longer at the core of the MNC's strategy. As one manager for a firm with design operations in India and China put it "we are not doing a 'replace" model where we move whole functions to Asia." This insistence by one manager is not in and of itself convincing, but the fact that each and every firm reported keeping a wide range of activities onshore is telling.

Furthermore, the fact that only three of the 19 MNC design operations had even reached the stage of having both their own chips and the ability to do complete design flows demonstrates that en masse movement of design functions offshore even within individual companies has not happened. Semiconductor Industry Association (SIA) data in Brown and Linden (2009: 92-93) on total engineering workforces in surveyed semiconductor companies also supports the idea that semiconductor employment at home is not plummeting even as the number of designers grows overseas.

The compelling logic that has prevented wholesale moving of a given function overseas is workforce recruitment and retention. Simply put, a MNC strategy predicated on doing one function or two in India is also not be viable in terms of workforce recruitment and retention because engineers are attracted to MNCs by the training opportunities as much as the relatively high salaries. A number of the

MNCs emphasized that they were trying to provide opportunities for broadening their engineers' experience as a key tool of retention despite MNCs paying the highest wages in India's IC sector. This strategy was strikingly similar to that of the larger Indian design service firms where the firms tried to avoid having their workforce focus on just one or two functions along the design flow. In the MNCs the strategy was not to move whole functions over to India to do en masse while getting rid of these functions in the MNC home base because such a strategy would not be a good recruitment strategy i.e. doing whole functions in India would not offer the broad range of design experiences Indian engineers seek **in order to move up the technology skill ladder.** Providing such broad experience in India as a recruiting tool also provides the training needed for developing new design leads in India. The emerging trend of India-based design leads underscores that offshoring in IC design is no longer limited to relatively low-skilled and rote tasks.

**The labor supply situation also suggests that whatever other incentives and motives MNCs have in offshoring production, they simply are going to be constrained from doing so due to the supply issue that may not be easily resolved in the short to medium-term.** Despite the hype, the combined design workforces of India and China are still approximately only sixty percent the size of America's (Fuller 2014). Therefore, it is unlikely that the MNCs will be able to add sufficiently large numbers of designers to their firms or through outsourcing to design service firms in those economies in order to be able to reduce dramatically their home base engineering team. With China's IP issues still something of a hindrance to luring MNCs, China continues to offer even less of a solution to rising design costs, and, unlike India, semiconductor design is not as relatively lucrative as other employment options for electrical engineers in China according to our interviews in both countries. Taking these factors into consideration, the potential supply of offshore designers in emerging economies shrinks considerably unless new sources emerge. Broader evidence examining quality as well as quantity of university grades,

and science and engineering (S&E) graduates in particular, in India and China discount the impressive nominal figures due to problems with the quality of graduates churned out by many of these institutions (Gereffi and Wadhwa 2005; McKinsey Global Institute 2005; Simon and Cao 2009)<sup>12</sup>. This paper will revisit this issue in the conclusion.

### *3.4 Fuzzy Set Qualitative Comparative Analysis of the Drivers of Increasing Offshore Design Capabilities*

In this sub-section, we will employ fsQCA (Ragin 2000) based on the interview data and patent data discussed above in order to derive the drivers of increasing the relative share of significant IC design done within India/China vis-à-vis the MNC HQ country. The outcome or dependent variable is the increase in a given MNCs' USPTO patents that came from its Indian or Chinese operations vis-à-vis its home country operations (expressed as the proportion of patents produced by the MNC in the host country over the patents produced in the MNC's home country) in the 2009 to 2013 period compared to the same figure for the 2003 to 2007 period. In other words, the outcome measure is the second-to-last column of Tables 1 and 2 subtracted from the last column of Tables 1 and 2. The fsQCA calculation focuses on this outcome variable because it is the variable most likely to capture how fast or slow the Indian or Chinese operations of a given MNC are able to grow vis-à-vis the established IC design operations of the MNCs and potentially indicates the likelihood of these Indian and Chinese operations displacing home country IC design operations of these MNCs. The fsQCA analysis shows that presence or absence of design leads in conjunction with other metrics of the scope and sophistication of a given MNC's offshore design operations (see Tables 1 and 2 above) play a major role in determining whether or not a given MNC has increased its patenting abroad in the 2009 to 2013 period.

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<sup>12</sup> Simon and Cao (2009) are somewhat more optimistic than McKinsey and Gereffi and Wadhwa on the quality issue given the explosion in size of China's 4-year undergraduate and post-graduate student population i.e. the absolute quantity of quality S&E graduates is still impressive.

In order to employ fsQCA, the outcome variable had to be calibrated for the fuzzy set into a range from zero to 1 as discussed in Ragin (2000, 2008). In other words, it was transformed from a percentage multiplied by 100 into a figure ranging from 0 to 1 with 1 representing the most complete transfer of patenting activity to the Indian or Chinese design site vis-à-vis the home country operations. In order to avoid relying on one calibration and its concomitant assumptions, three different calibrations (referred to below as Scenarios 1, 2 and 3) were used for the outcome variable were used.<sup>13</sup> These three different calibrations were based on the authors' judgment of what were the plausible distributions that reflect the underlying relative patenting performance which combine the increase in patenting with the authors' own sense of performance based on knowledge of the industry, and thus combines "the researcher's own accumulated knowledge" with "collective social scientific knowledge" in the form of the link between patenting and technological output as Ragin (2008:82) advocates.<sup>14</sup>

First, we examined whether four causal factors (the number of patents from the firm's operation in India or China from 2003 to 2007, the presence/absence of design leads, the presence/absence of design teams larger than 100 designers, and the presence/absence of large AMS teams) met the criteria of being necessary to explain the increase in share of the firm's patenting from the Indian/Chinese operations (as measured as a percentage of MNC home country patenting). According to fsQCA, necessary conditions are those where the set membership value of causal variable X is always greater than the set membership value of outcome variable Y (the instances of the outcome variable are a subset of the instances of the causal variable). In fsQCA, the metric of consistency measures not only

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<sup>13</sup> With the direct method calibration, the researcher must set the thresholds for full membership, full non-membership and the crossover point (Ragin 2008: 89-94). For Scenario 1, these values were 1.55, 0.9 and 1.2. For Scenario 2, they were 1.55, 0.2 and 0.9. For Scenario 3, they were 1.55, 0.5 and 0.99.

<sup>14</sup> As Ragin (2008: 82) states, "The external criteria that are used to calibrate measures and translate them into set membership scores may reflect standards based on social knowledge..., collective social scientific knowledge...or the researcher's own accumulated knowledge, derived from the study of specific cases."

whether or not the posited relationship between variables  $x$  and  $y$ <sup>15</sup> holds but also weights large misses more than narrow misses. A consistency score of one indicates that the relationship between the variables holds in all cases. As the number of instances where the relationship does not hold between the variables and the misses become larger, the consistency score moves farther from 1 and closer to 0 (Ragin 2006). The standard of consistency for a variable to be considered “necessary” or “almost always necessary” is 0.9 (Schneider *et al.* 2010).

As shown in Table 4, only design leads as a single variable passed the 0.9 threshold across any of the different scenarios. Design leads alone passed the threshold in Scenario 1 and barely missed it in the other two scenarios. As for combinations, only the combination of design leads and having more than one hundred designers passed the 0.9 threshold and in fact achieved a perfect score of 1 across two of the three scenarios.<sup>16</sup>

Coverage indicates whether or not the necessary causal variable is trivial (i.e. occurs in all or most cases regardless of the outcome). Coverage captures how much of the outcomes  $Y$  covers the causal variable  $X$ . Coverage rates close to zero indicate that the necessary causal variable is trivial (i.e. the causal variable  $X$  exists in many instances when the outcome  $Y$  does not occur) and coverage rates closer to one indicate that the outcome holds for an increasing portion of the cases where the causal condition holds (Ragin 2008).<sup>17</sup> For design lead as a single variable and the design lead-one hundred-plus

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<sup>15</sup> Testing the necessary condition can be done between a combination of causal variables and an outcome variable rather than simply one causal and one outcome variable.

<sup>16</sup> For testing necessary conditions, combinations of variables refer to the situation where one of the two variables or both variables are present.

<sup>17</sup> A helpful example from Ragin (2008: 63) is childhood milk drinking as a posited cause for adult heroin addicts in the US. Most adult heroin addicts drank milk as children, but milk drinking has low coverage because the outcome, heroin addiction, only occurred in a very small portion of the childhood milk drinkers i.e. childhood milk drinking does not lead to adult heroin addiction in the vast majority of cases.

designers combination that crossed the threshold for being deemed necessary conditions, the high coverage scores in Table 4 indicate that these are non-trivial necessary causal conditions.

<insert Table 4>

The sufficient causal variables were also examined in order to arrive at different causal recipes (also referred to in this paper as causal paths) that were common in leading to an increase in patenting activities in the subsidiaries abroad. Causal conditions are considered to be sufficient in fsQCA when the fuzzy set membership value of causal variable X does not exceed the fuzzy set membership value of outcome variable Y. Constructing truth tables from the data in Tables 1 and 2 and then running the fuzzy set truth table algorithm in fs/QCA 2.5 software found solutions for the three different calibrations (i.e. Scenarios 1, 2 and 3 in footnote 13) of the percentage increase in local patenting in India/China as a percentage of home country patenting. This paper follows Ragin's (2008) advice in using the intermediate solution<sup>18</sup> for interpretation. The intermediate solution can be viewed as the middle solution between the most parsimonious solution, which allows a full range of counterfactuals, and the most complex, which allows only a few counterfactuals to be considered.

The intermediate solution of the fuzzy set analysis for each calibration of increasing patenting had design leads as part of the solution for each scenario as shown in Table 5. Each of the three scenarios had the same two causal paths in the intermediate solution: 1) AMS teams and one hundred plus designers and design leads and 2) one hundred plus designers and design leads and patents from 2003

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<sup>18</sup> The intermediate solution is a compromise between the complex solution where only empirically existing causal combinations are used in the reduction process and the parsimonious solution where the remainders (the logical causal combinations without empirical cases) are included. For the intermediate solution, the counterfactuals included have to be stated (Ragin 2008), and here we included those with the assumption that either the presence or absence of each of the four of the causal variables would lead to the solution of increased patenting in the offshore site as a percentage of total patenting by the firm.

to 2007. In other words, these two unique paths of three causal variables each led to the outcome of increasing patenting. Importantly, each causal path had the previously identified necessary condition (design leads) or combination of conditions (design lead and one hundred designers) as part of its causal path. These two causal paths had positive unique coverage not overlapping with other causal recipes so these paths/recipes should be considered empirically important (Ragin 2008). They also exhibited very high consistency where the causal recipes all were well over the .9 consistency threshold. Furthermore, the solution coverage (the combined coverage of the two causal paths, which had some overlap) explained over half the outcome in two of the three scenarios and high levels of consistency (marked solution consistency in Table 5).

Both the analysis of necessary and sufficient conditions point to the key role of design leads and large design teams of over one hundred designers in propelling the development of offshore IC design capabilities. The fuzzy set analysis pinpoints that the MNC operations with design leads and large teams in conjunction with other attributes measuring the scale and capabilities of local design teams in the earlier period (large AMS teams and patenting activity in 2003-2007) are the ones that most ramped up their extensive offshoring of semiconductor design vis-à-vis MNC home country during the 2009-2013 period. This finding helps to explain why there are more MNCs moving to extensive offshoring in India as a simple function of their previous greater accumulated capabilities as suggested in the review of the interview data in the first half of Section 3. The evidence for gradually increasing design activities offshore being generally dependent upon previous design activities of MNCs in the same offshore locations also demonstrates that offshoring in semiconductor design will most likely not displace the large amount of design activities in the home countries of the MNCs any time soon. The prominent role played by design leads in determining the amount of further offshoring also lends support to the



concept of design leads sitting atop a technology skill ladder derived from our qualitative works as described in Section 2.

<insert Table 5>

### **Conclusion: Sustainability of Skill Formation in the Home Countries**

As mentioned earlier, one way to meet the challenges presented by the increasing complexity of designs is to hire more engineers or access them indirectly through outsourcing in relatively low wage locations. This cost reduction has been a major motivation for MNCs to offshore to India and China (Brown and Linden 2009: 68-69; Hurtarte et al 2007: 63-64) and has raised concerns about the loss of IC design expertise in the home countries of the MNCs. Despite these concerns, the gradual movement of design activities to India and China thus far suggests that in the short-term (the next decade) the skill ladders in the home countries of the MNCs and thus design skill formation will remain sustainable. After all, even the MNCs with greatest portion of patenting from India and China under study, still had less than ten percent of their lead patenting activity from India and China. The firm patenting the most in relative and absolute terms from the host economies is MNC 3 and its total lead patenting from India and China combined accounted for a mere eight percent of the total from those two countries and MNC 3's home country.<sup>19</sup>

This paper has presented compelling evidence that there is not going to be any “giant sucking sound” from India and China pulling enough of the IC design jobs out of the major IC MNCs’ home bases to undermine the skills ladder in these home countries in the short-term (i.e. within the next decade).

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<sup>19</sup> India+China= the equivalent of 8.9 percent of the home country total for MNC 3 so the percentage of India+China/(India+China+home)= 8.9/108.9=8.17%. And this calculation does not include other wealthy (i.e. high wage) economies where MNC 3 has lead patent activity so India and China’s share of MNC 3’s total lead patenting is even smaller.

The real issue is whether or not these offshoring locations will continue to offer in terms of low cost, skilled or at least trainable designers that could potentially replace the IC design workforces in the MNC home countries over somewhat longer time horizons. Follow-up interviews in 2014 and 2015 with industry participants in India and China points to the fact that industry wages have risen dramatically relative to the established developed world locations for design. Whereas in both India and China, IC designers were averaging ten percent of the compensation of their US peers in 2002, interviews reported that in India, compensation was by now 20 to 25 percent of that of US peers for early to somewhat experienced engineers and was nearly equal for senior technical staff with gaps of 1:1.15 or 1.2. For China the compensation by 2014 was between one third and a quarter of US peer salaries for early career engineers, had reached parity with wages for comparable engineers in Taiwan until a hiring splurge by Mediatek in Taiwan drove Taiwanese wages a bit higher in 2015 according to interviewees who run operations in both Taiwan and China, and had reached near parity for senior technical staff. The narrowing gap in engineering cost with the US has meant that MNCs are less likely to view moving offshore to India and China as an easy solution to controlling design costs.

On the supply side, India and China have both expanded their educational programs for IC design. In China, this has been done through the formal university system according to interviewees in 2014 and 2015. Despite of investment in such programs at top universities in the interior, MNCs view these programs as providing less direct experience with actual IC design than equivalent programs at the major universities in the coastal areas. Moreover, both MNCs and local firms mentioned that IC design has become less attractive for electrical engineers, especially those graduating from the best universities on the coast, with many opting for more lucrative jobs in either software and non-engineering jobs, such as working for Big Four accounting firms. Of course, in India, there is one similarity in that India's elite Indian Institutes of Technology BSc. graduates eschew entry into the IC industry at home for study

abroad or work in other fields, but the profession of IC design remains attractive due to its relative high pay.

In India, beyond the formal university system, there are “finishing” schools, such as RV VLSI in Bangalore, that have played an important role in providing training for designers who then typically work for design service firms to gain experience before being deemed fit to work for MNCs. Between the finishing schools, additional training provided by the design service firms and the formal university system in combination with the relatively high wages paid for IC design compared to other technical work in India (only the Web 2/3.0 start-ups and MNCs, such as Amazon and Google, pay more than the IC MNCs) have created a healthier dynamic for future growth in the Indian industry.

Nevertheless, even for India with its more favorable labor supply situation for the industry, any dynamics and trends in favor moving more activities to India do not yet presage the imminent end of such activities in the MNCs’ home countries, especially the US as the home of many MNCs involved in IC design. A manager who had worked in the US for many years before returning to India in the mid-2000s to work at one of the largest MNCs in this industry which also had a long history in India (MNC 4) acknowledged in April 2015 that over the past decade regarding IC design “ [the] technical pool has increased significantly—people and talent.” However, he also acknowledged that there is still a gap with the MNCs’ operations in its corporate home, the United States. “Even though we have come a long way, they are much more capable and bigger. We’re becoming more competitive but there is still a gap.” A manager at another prominent MNC (MNC 5) in a division that was not the MNC 5’s core product claimed in February 2014, “Definitely will happen that twenty years from now [we] will have more design leads here [in India as compared to the MNC home base].” However, another manager from MNC5 but from the division that represents the firm’s core product interviewed on the same day said of design leads moving to India, “Quite unlikely to happen...GPU (graphics processing unit) has core

graphics function in XXXX [excluding the name of the US site to protect firm anonymity].” He then pointed out that MNCs were actually moving away from doing end-to-end products in India due to two factors. The first was the very increase in chip complexity that originally drove firms to seek engineering resources offshore was requiring ever larger numbers of engineers that firms might not necessarily have even in India. He mentioned that design for relatively large graphics chipsets a decade ago would have required fifty full-time front-end design engineers and require more than 200 today. The second was corporate politics where the most glamorous, sophisticated design jobs remained at the US headquarters, not even shared with other locations in the United States.

In the medium-term, two threats to the IC skills ladder in advanced economies where the IC industry MNCs are generally headquartered potentially loom larger than offshoring of activities within the internal operations of MNCs. First, firms may begin to offshore more and more complete designs to Indian design service firms as the latter enhance their capabilities. In contrast to moving activities offshore but within the firm<sup>20</sup>, firms may start to move many design activities outside of the firm to Indian firms and this outsourcing to Indian firms poses a greater risk of removing or weakening rungs on the home design skills ladder. Moving whole activities to design service firms (something advocated by the Global Semiconductor Association-approved Hurtarte *et al.* 2007) in India across a number of firms would pose a greater risk to home country skill ladders because the ability of firms to provide training in or at least exposure to these functions for engineers in their home countries would be much more limited. Given the current capabilities of the design service firms, such an event is still quite a long way off. As far as the most extreme scenario of complete outsourcing of chip design except for architectural definition, the design service firms can do complete designs, but it is not evident that they can do

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<sup>20</sup> Internal offshoring would be much less of a threat because keeping the design functions in-house but overseas still provides the ability to provide home staff some exposure in these skills.

complete complex designs. And again, the issue of the limited labor supply makes this scenario very unlikely. Furthermore, in interviews in 2014-2015, several of India's leading design service firms indicated that their ambitions to upgrade the tasks they undertake have effectively stalled since 2008 given pushback from MNCs which want to retain as much value as they can from the design process.

The second threat to the technology skill ladder in the developed world's IC design sector is the emerging fabless firms in China, perhaps in alliance with Taiwanese firms. The fabless design firms in China may eventually have an advantage for designing-in for products manufactured in China's very large industrial economy. If these fabless firms are able to do chip definition for the Chinese marketplace, they could displace a significant share of foreign IC firms' market. Some of these Chinese fabless firms will be successful, but the changing dynamics of the industry's structure suggest that it will be harder and harder for start-ups to compete against established firms as chip design costs soar (Hurtarte *et al.* 2007). While the Chinese government's new mega-project for the IC industry announced in 2014 has involved providing copious funds for Chinese firms to buy foreign design houses, the corporate vehicles chosen for such investment, such as state-owned Tsinghua Unigroup, may not be effective at creating innovative firms from the disparate local and foreign firms they buy given their lack of experience in the industry. Therefore, this scenario may also not amount to much. However, if the Taiwanese design firms, which are more mature and of sufficient scale, are able to take full advantage of the Chinese marketplace and Chinese engineers, then this scenario would be more likely to be realized. Arguably, Taiwan's Mediatek is doing just this strategy in the mobile phone chip market in China. In any event, some migration of IC design industry activities to locations with skilled technologists at still lower wages in Asia and elsewhere will continue as the industry matures, and the industry already shows signs of maturation from renewed industrial consolidation (Hurtarte *et al.* 2007) to increased price sensitivity for the consumers of chips (Brown and Linden 2009).

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**Table 1 MNC Activities in India and Levels of Design Activity in Host and Home Countries**

Source: Compiled by author from data from the United States Patent and Trademark Office (USPTO).

<b>Firm</b>	<b>Design Leads (2007-2008)</b>	<b>100+ Designers (2007 - 2008)</b>	<b>Large AMS Team (2007-2008)</b>	<b>2003-2007 Lead Inventor Patents in India</b>	<b>2009-2013 Lead Inventor Patents in India</b>	<b>2003-2007 Indian Lead as % of HQ Lead Patents</b>	<b>2009-2013 Indian Lead as % of HQ Lead Patents</b>
<b>MNC 1</b>	<b>X</b>	<b>X</b>	<b>X</b>	10	19	<b>2.07</b>	<b>3.7</b>
<b>MNC 2</b>	<b>X</b>	<b>X</b>	<b>X</b>	0	89	<b>0</b>	<b>8.4</b>
<b>MNC 3</b>	<b>X</b>	<b>X</b>	<b>X</b>	141	262	<b>4.23</b>	<b>8.7</b>
<b>MNC 4</b>	<b>X</b>	<b>X</b>	<b>X</b>	16	95	<b>0.2</b>	<b>1.61</b>
<b>MNC 5</b>	<b>X</b>	<b>X</b>	<b>X</b>	0	36	<b>0</b>	<b>3.09</b>
<b>MNC 6</b>	<b>X</b>	<b>X</b>		15	94	<b>1.7</b>	<b>6.04</b>
<b>MNC 7</b>	<b>X</b>	<b>X</b>		0	19	<b>0</b>	<b>2.84</b>
<b>MNC 8</b>	<b>X</b>	<b>X</b>		1	45	<b>0.08</b>	<b>0.93</b>
<b>MNC 9</b>	<b>X</b>		<b>X</b>	8	11	<b>0.78</b>	<b>1.63</b>
<b>MNC 10</b>	<b>X</b>			27	65	<b>1.43</b>	<b>1.43</b>
<b>MNC 11</b>	<b>X</b>			0	11	<b>0</b>	<b>0.58</b>
<b>MNC 12</b>	<b>X</b>			0	5	<b>0</b>	<b>1.45</b>
<b>MNC 13</b>	<b>X</b>			22	25	<b>3.02</b>	<b>4.71</b>
<b>MNC 14</b>		<b>X</b>		0	7	<b>0</b>	<b>1.02</b>
<b>MNC 15</b>		<b>X</b>		0	10	<b>0</b>	<b>3.75</b>
<b>MNC 16</b>		<b>X</b>		0	0	<b>0</b>	<b>0</b>

**Table 2 MNC Activities in China and Levels of Design Activity in Host and Home Countries**

Source: Compiled by author from data from the United States Patent and Trademark Office (USPTO).

<b>Firm</b>	<b>Design Leads (2007-2008)</b>	<b>100+ Designers (2007-2008)</b>	<b>Large AMS Team (2007-2008)</b>	<b>2003-2007 Lead Inventor Patents in China</b>	<b>2009-2013 Lead Inventor Patents in China</b>	<b>2003-2007 Chinese Lead as % of HQ Lead Patents</b>	<b>2009-2013 Chinese Lead as % of HQ Lead Patents</b>
<b>MNC 3</b>	<b>X</b>			<b>0</b>	<b>6</b>	<b>0</b>	<b>0.2</b>
<b>MNC 6</b>	<b>X</b>	<b>X</b>		<b>0</b>	<b>34</b>	<b>0</b>	<b>2.18</b>
<b>MNC 11</b>		<b>X</b>		<b>2</b>	<b>0</b>	<b>0.07</b>	<b>0</b>
<b>MNC 14</b>	<b>X</b>	<b>X</b>		<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>
<b>MNC 17</b>	<b>X</b>	<b>X</b>	<b>X</b>	<b>5</b>	<b>37</b>	<b>0.67</b>	<b>4.09</b>
<b>MNC 18</b>	<b>X</b>			<b>0</b>	<b>29</b>	<b>0</b>	<b>0.86</b>
<b>MNC 19</b>				<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>

**Table 3 MNCs' Operations in China and India Compared**

Source: Compiled by author from data from the United States Patent and Trademark Office (USPTO).

<b>Firm</b>	<b>Design Leads (2007-2008)</b>	<b>100+ Designers (2007 - 2008)</b>	<b>Large AMS Team (2007-2008)</b>	<b>2003-2007 Lead Inventor Patents in Host Country</b>	<b>2009-2013 Lead Inventor Patents in Host Country</b>	<b>2003-2007 Host Lead as % of HQ Lead Patents</b>	<b>2009-2013 Host Lead as % of HQ Lead Patents</b>
MNC 3 China	X			0	6	0	0.2
MNC 3 India	X	X	X	141	262	4.23	8.7
MNC 6 China	X	X		0	34	0	2.18
MNC 6 India	X	X		15	94	1.7	6.04
MNC 11 China		X		2	0	0.07	0
MNC 11 India	X			0	11	0	0.58
MNC 14 China	X	X		0	0	0	0
MNC 14 India		X		0	7	0	1.02

**Table 4 Analysis of Necessary Conditions**

	Consistency	Coverage
<b>Design Leads (Scenario 1)</b>	<b>0.904602</b>	<b>0.600556</b>
AMS (Scenario 1)	0.491213	0.838571
Patents0307 (Scenario 1)	0.420084	0.718169
Hundred (Scenario 1)	0.837657	0.667333
<b>Design Leads+Hundred (Scenario 1)</b>	<b>1.000000</b>	<b>0.543182</b>
Design Leads (Scenario 2)	0.880935	0.690556
AMS (Scenario 2)	0.448618	0.904286
Patents0307 (Scenario 2)	0.392629	0.792561
Hundred (Scenario 2)	0.781715	0.735333
<b>Design Leads+Hundred (Scenario 2)</b>	<b>1.000000</b>	<b>0.641364</b>
Design Leads (Scenario 3)	0.884297	0.653889
AMS (Scenario 3)	0.463561	0.881429
Patents0307 (Scenario 3)	0.398948	0.759657
Hundred (Scenario 3)	0.804658	0.714000
<b>Design Leads+Hundred (Scenario 3)</b>	<b>1.000000</b>	<b>0.605000</b>

**Table 5 Intermediate Solutions of Fuzzy Set Truth Table Algorithms**

Scenarios	Variables	Raw Coverage	Unique Coverage	Consistency	Solution Coverage	Solution Consistency
<b>Scenario 1</b>	AMS*Hundred*Design	0.488703	0.250209	0.973333		
	Hundred*Design*Pat0307	.328033	0.089540	0.987406		
					0.578243	0.973239
<b>Scenario 2</b>	AMS*Hundred*Design	0.416726	0.215450	0.980000		
	Hundred*Design*Pat0307	0.279235	0.077959	0.992443		
					0.494685	0.983099
<b>Scenario 3</b>	AMS*Hundred*Design	0.441022	0.227648	0.978333		
	Hundred*Design*Pat0307	0.294515	0.081142	0.987406		
					0.522164	0.978873

Note: The frequency threshold used was 1 instance (event) for each possible configuration of variables and the consistency threshold used was 0.75 as recommended in Ragin (2008: 142-143).