# GaN Electronics for High-Temperature Applications

by

Mengyang Yuan

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

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Signature redacted

Author .....
Department of Electrical Engineering and Computer Science
January 30, 2020

Signature redacted

Certified by .....
Tomás Palacios
Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Signature redacted

Accepted by .....
Leslie A. Kolodziejski
Professor of Electrical Engineering and Computer Science
Chair, Department Committee on Graduate Students

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## Abstract

Gallium nitride is a promising candidate for high-temperature applications. However, despite the excellent performance shown by early high-temperature prototypes, several issues in traditional lateral AlGaN/GaN HEMTs could cause early degradation and failure under high-temperature operation (over 300°C). These include ohmic degradation, gate leakage, buffer leakage, and poor passivation. Besides, enhancement-mode HEMTs are preferred from the application point of view by reducing the circuit complexity and cost. At the same time, the two-dimensional electron gas induced by AlGaN/GaN heterostructures makes HEMTs be naturally depletion-mode devices.

This thesis aims to demonstrate devices capable of high-temperature operation without extra cooling systems by combing gate injections transistors (GITs) with ion-implanted refractory metal contacts. The Si ion implantation in AlGaN/GaN heterostructures was comprehensively studied here regarding implantation conditions, activation annealing conditions, metallization schemes. A self-aligned gate-first process, together with etch-stop process, was developed and optimized to improve fabrication efficiency and device uniformity for large-scale integration. Basic logic building blocks, including inverters, NAND gate, NOR gate, SRAM, and ring oscillator, have been demonstrated and characterized at both room temperature and high temperature.

Thesis Supervisor: Tomás Palacios
Title: Professor of Electrical Engineering and Computer Science

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# Chapter 1

# Introduction

In the past few decades, there have been increasing demands for microelectronics working reliably in the harsh environment, including extremely high temperature over 300°C on a large variety of applications, such as automotive, aerospace, petroleum, geothermal industry and other industrial systems. Conventional semiconductors such as Silicon (Si) and Gallium Arsenide (GaAs) are physically limited by their bandgaps and show limitations in high-temperature operation.

Traditionally, for operating electronics above specified temperature range, additional thermal management approaches, including either active or passive cooling systems, are required to maintain the normal operation. Extra cost, complexity, unwanted size, weight, noise, and lower reliability [2, 3] introduced by these cooling approaches become major obstacles for high-temperature applications. Devices capable of high-temperature operations without external cooling are desirable to reduce the cost and improve system reliability.

## 1.1 Applications of High-Temperature Electronics

High-temperature electronics are commonly required in applications where the high ambient temperature is present, and self-heating effects may also be taken into account for systems with high power dissipation and dense packaging.

The underhood temperature of traditional automotive could easily reach 140 °C

either on the engine or in the transmission [4, 5]. The integration of power electronics with electric motors will increase the operating temperature above 200°C. With the proliferation of hybrid, fuel cell, and fully electric automobiles, it also drives incremental demand for higher temperature electronics.

Similar to the automotive industry, high-temperature electronics are also critical in aerospace. It is desirable to put the monitor and control section close to the jet engine in order to reduce the complexity of interconnections [6] with the ambient temperature above 225°C, and to improve the system efficiency and reliability. Besides, space exploration brings more challenging goals such as Venus exploration with the surface temperature above 465°C [7].

Deep oil/gas extraction is one of the most traditional applications of high-temperature electronics. The operating temperature of electronics used to in-situ monitor or control drilling operation will increase with the underground depth of well and could exceed 200°C for deep wells with high pressure involved. In such applications, cooling systems are usually not efficient and quite complex, and therefore it is quite challenging to ensure the system reliability, considering the high cost of potential failure. With high-temperature electronics, it is feasible to drill deeper and avoid redundant cooling systems.

Geothermal energy, as one of the renewable energy resources, has been widely used around the world. It was reported in 2015 that the amount of energy used was 587,786 TJ/year, with an annual growth rate of 6.8% [8]. The critical point of water occurs at 374°C and 22.2mPa, while the critical point of seawater is even higher at 407°C and 29.8mPa with salt dissolved [9]. An Iceland Deep Drilling Project (IDDP) study showed that a geothermal well producing supercritical fluid with a temperature over 400°C would have one order of magnitude higher power-producing potential than a conventional geothermal well producing steam [10]. With the help of high-temperature electronics, it is possible to access hotter and deeper geothermal resources and further improve the power output of the existing geothermal fields.

## 1.2 Challenges of High-Temperature Electronics

Commercially available electronics based on SOI technology are limited to 200-250 °C maximum [6]. At extremely high temperature above 300 °C, several fundamental limitations of traditional semiconductors should be taken into concerns, which make Si-based device operation inherently impossible. Those limiting factors are well summarized by several review papers [2, 3, 6] in the past few decades and will be briefly illustrated below.

### 1.2.1 Increasing Intrinsic Carrier Density with Temperature

One of the most dominant physical limitations for high-temperature operation is the increasing number of thermal electron and hole carriers, also as known as intrinsic carriers in the semiconductor crystal. Free electron and hole carriers introduced by intentionally doping impurities into designed regions is the fundamental of traditional semiconductor devices operation. Typically, the concentration of free electrons or holes is roughly equal to the dopant concentration due to small ionization energies with trap assistance and high activation ratios at room temperature. Depending on the specific structure and design, the doping level might vary between $10^{13}$ $cm^{-3}$ to $10^{18}$ $cm^{-3}$. When the temperature increases, the concentration of intrinsic carriers ($n_i$ in $cm^{-3}$) also increases exponentially [11],

$$n_i = \sqrt{N_c N_v} exp\left(-\frac{E_G}{2kT}\right) \tag{1.1}$$

where $T$ is the temperature in Kelvin, $k$ is the Boltzmann constant ($8.62 \times 10^{-5} eV/K$), $E_G$ is the energy bandgap in $eV$, $N_C$ and $N_V$ are, respectively, effective density of states of the conduction/valence band in $cm^{-3}$ and they both have a weaker temper-

ature dependence [11],

$$N_C = 2\left(\frac{2\pi m_{de}^* kT}{h^2}\right)^{3/2} \tag{1.2}$$

$$N_V = 2\left(\frac{2\pi m_{dh}^* kT}{h^2}\right)^{3/2} \tag{1.3}$$

where $h$ is the Planck constant ($4.14 \times 10^{-15} eV \cdot s$), $m_{de}^*$ and $m_{dh}^*$ are the density of state effective mass for electrons and holes in $eV \cdot s^2/cm^2$. Notice that, both $m_{de}^*$ and $m_{dh}^*$ are not quite constant in temperature but much less dominant because $N_C$ and $N_V$ don't exactly follow $T^{3/2}$.

In summary, the temperature dependence of intrinsic carrier concentrations could be simplified in terms of Eq. 1.1. Intrinsic carrier concentrations from different materials are shown in Fig. 1-1. For standard Si devices working at room temperature, the $n_i$ around $10^{10} cm^{-3}$ is negligible compared to the doping levels mentioned above. When the temperature increases well beyond 300°C, the device will gradually move to the intrinsic region where intrinsic carriers become dominant, and show an undesirable influence on lightly-doped regions. Wide bandgap materials have much lower intrinsic carrier concentrations with much wider bandgaps ($> 3eV$) compared to the bandgap of silicon ($1.1eV$), as seen from Fig. 1-1.

### 1.2.2 Increasing Junction Leakage with Temperature

As a consequence of low energy bandgap and high intrinsic carrier concentration, the increase of junction leakage currents of traditional semiconductors will further degrade device performance. Almost all the devices have junctions like PN junctions or Schottky junctions. They strongly rely on the rectifying property of junctions, which is conducting current at forward bias and blocking current at reverse bias, for regular operation. For example, for power diodes or power transistors in buck/boost converters, low leakage currents are required at a high reverse bias to achieve designed performance and improve power efficiency. The ideal current-voltage (I-V) characteristics of the most common p-n diode structure with a "long" diode assumption can be

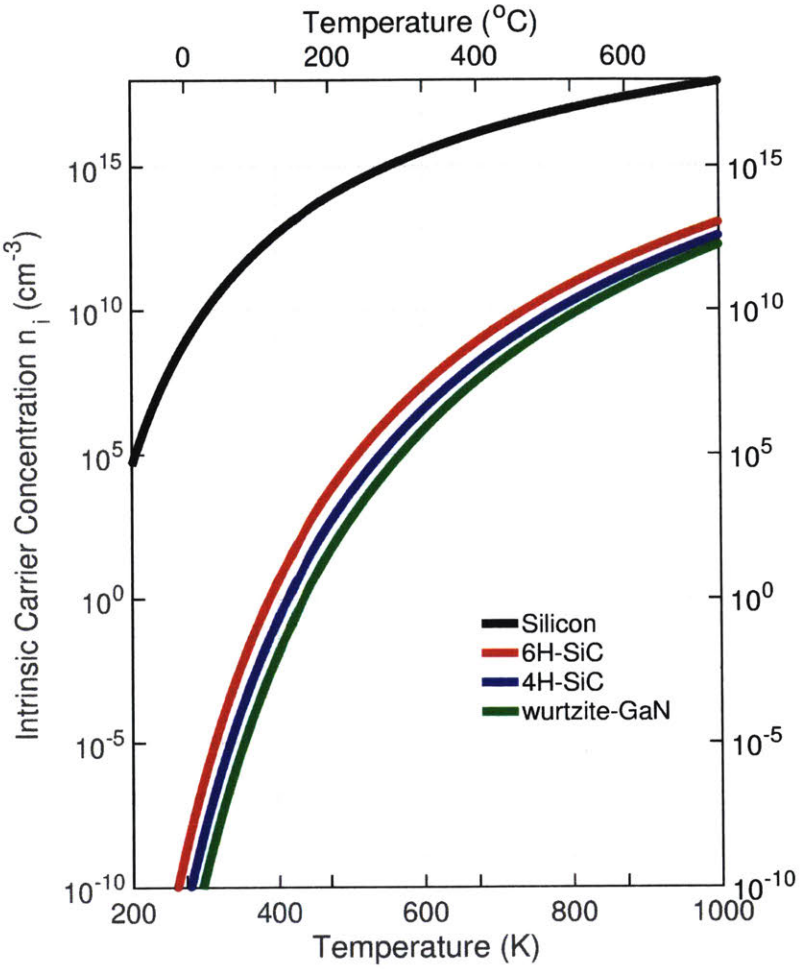



Figure 1-1: Semiconductor intrinsic carrier concentration ($n_i$) versus temperature for silicon, 6H-SiC, 4H-SiC and wurtzite GaN which has a weaker polytype dependence.

modeled approximately as [11],

$$J = (J_{es} + J_{hs}) \left[ \exp\left(\frac{qV}{kT}\right) - 1 \right] \tag{1.4}$$

$$= qn_i^2 \left( \frac{1}{N_A}\sqrt{\frac{D_e}{\tau_e}} + \frac{1}{N_D}\sqrt{\frac{D_h}{\tau_h}} \right) \left[ \exp\left(\frac{qV}{kT}\right) - 1 \right] \tag{1.5}$$

where $J_{es}$ and $J_{hs}$ are, respectively, the saturation currents of electrons and holes, $V$ is the bias voltage applied, $N_A$ and $N_D$ are acceptor and donor concentrations, $D_e$ and $\tau_e$ are diffusion coefficient and minority carrier lifetime for electrons in the

p-doped region and vice versa.

With space charge generation and recombination taken into account, the upper limit of space charge region (SCR) current in the p-n diode can be computed by assuming that the maximum recombination rate applies everywhere [11],

$$J_{SCR,max} = \frac{qn_i x_{SCR}}{2\sqrt{\tau_{eo}\tau_{ho}}} \left[\exp\left(\frac{qV}{2kT}\right) - 1\right] \tag{1.6}$$

where $x_{SCR}$ is the width of space charge region (depletion region), $\tau_{eo}$ and $\tau_{ho}$ are constants scaling inversely with trap concentration. And the total current of p-n diode is the sum of Eq. 1.5 and Eq. 1.6.

Other than the p-n junction, another junction structure is the metal-semiconductor junction, also known as the Schottky junction. A Schottky diode is a majority-carrier device as opposed to the p-n diode driven by minority carrier injection. The I-V characteristics could be described by a thermal emission model in which the current is limited by the electron emission process over the tip of the energy barrier at metal-semiconductor interface [11],

$$J = A^* T^2 \exp\left(\frac{-q\varphi_B}{kT}\right) \left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{1.7}$$

where $A^*$ is Richardson constant, $\varphi_B$ is the effective barrier height between metal and semiconductor.

From Eq. 1.5-1.6, we see a strong relationship between reverse saturation current and intrinsic carrier concentration $n_i$, which means that the leakage current will increase exponentially with temperature and greatly influence the normal operation of devices with such structure. From Eq. 1.7, we know the leakage current could be kept relatively low by increasing junction barrier height, which is more feasible with wide bandgap materials. Again, with wider bandgaps and lower intrinsic carrier concentrations, wide bandgap materials are considered to be more potential candidates capable of high-temperature operation over 300°C.

### 1.2.3 Decreasing Carrier Mobility with Temperature

Sheet resistance is one of the dominant components of device on-resistance and scales inversely with the carrier mobility in most of the cases. For a non-zero temperature, the atoms in the lattice of a semiconductor vibrate around their equilibrium positions. The vibration is usually quantized as a phonon (an acoustic phonon or an optical phonon) to simplify the energy-exchange process between lattice and electrons. The interaction between phonons and electrons is known as phonon (lattice) scattering. At higher temperature, phonon scattering is the dominant scattering mechanism over ionized impurity scattering, which dominates at low temperature. When the temperature increases, the phonon scattering tends to increase with more phonons generated, leading to lower mobilities for both traditional semiconductors and wide bandgap materials [12, 13, 14].

### 1.2.4 Other Issues

In the previous section, several physical limitations on device operation have been discussed. However, the development of high-temperature electronics is not only a problem at the device level which could be solved right away by choosing proper materials and structures, but a system problem involving growth, fabrication, packaging techniques, device models of a wide temperature range for circuit design, and reliability evaluation.

## 1.3 Wide Bandgap Materials for High-Temperature Applications

As discussed above, wide bandgap materials show fundamental advantages over standard semiconductors such as Si and GaAs for high-temperature operation. Silicon Carbide (SiC), III-nitride (III-N), Gallium Oxide ($Ga_2O_3$), Diamond are the most common wide bandgap materials [2, 3, 6, 15, 16, 17] and properties of SiC and GaN compared to that of Si are shown in Fig. 1-2 [18, 19]. Due to the difficulty in crys-

tal growth, low material quality, lack of process technology, and difficulty in making p-channel devices, $Ga_2O_3$- and Diamond-based devices are not considered to be ideal candidates for high-temperature operation in the near future. Here the discussion will be mainly focused on the comparison between SiC and Gallium Nitride (GaN) regarding materials properties, growth technology, process technology.

In the past few decades, SiC was considered to be a superior choice and has been intensively studied not only because SiC has a slightly better thermal conductivity which drops quickly with temperature, but also relying on better technological infrastructure and maturity together with the possibility for vertical power devices. SiC is known to have great wafer quality such as very low micropipe density [20], which is good for device operation and to improve the yield for both large area and vertical devices. 4-inch SiC wafers have been commercialized more than a decade, and 6-inch SiC wafers are now also available in the market, while 8-inch SiC wafers might not happen shortly. There are currently several kinds of SiC diodes and switches available [21, 22], including SiC Schottky diode, junction barrier Schottky (JBS) diode, PIN diode, JFET and MOSFET. A commercialized SiC MOSFET with operating temperature up to 200°C was demonstrated by General Electric (GE) [23] in 2014. Besides, stable operation of 6H-SiC JFETs and ICs at 500°C up to 3000 h in air ambient was reported by NASA Glenn Research Center [24] in 2008.

Meanwhile, Gallium Nitride is first known as a wide bandgap material for high brightness blue light-emitting diode (LED). Due to its high critical electric field, it then becomes a promising candidate for electrical devices as well. As shown in Fig. 1-2, even both SiC and GaN show better performance than Si, GaN still has a higher breakdown electrical field than SiC. Besides, the polarization nature of GaN [18] enables the invention of AlGaN/GaN high electron mobility transistors (HEMTs) by forming a high-quality two-dimensional electron gas (2DEG) in the heterojunctions.

Most common AlGaN/GaN HEMTs are grown in the Ga-face with the wurtzite crystal structure, which is inherently asymmetrical. The intrinsic asymmetry of wurtzite lattice and difference of spontaneous polarization between AlGaN and GaN lead to a net spontaneous polarization charge in the AlGaN/GaN interface, as shown

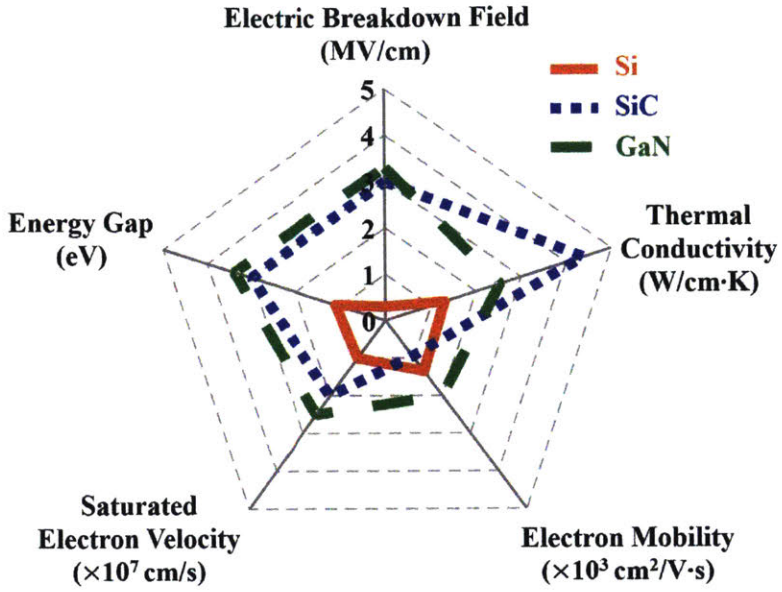



Figure 1-2: Materials properties of Si, SiC and GaN.

in Fig. 1-3. Besides, AlN is known to have a smaller lattice constant than GaN and the same for AlGaN, which could be approximated by linear interpolation between lattice constants of AlN and GaN. Thus, the AlGaN layer grown on the GaN channel is typically under tensile stress, and a piezoelectric polarization charge is then induced by such mechanical stress inside the AlGaN layer, while there is no piezoelectric polarization present from the relaxed GaN channel due to the lack of strain. The piezoelectric polarization induced by tensile stress in AlGaN is parallel to the spontaneous polarization, which means that both of them have negative signs along the axis [0001], as shown in Fig. 1-3. The net charge in the interface is then the sum of charges induced by both spontaneous polarizations from AlGaN and GaN and piezoelectric polarization from AlGaN[1],

$$\sigma = \left(P_{SP,GaN} - P_{SP,Al_xGa_{(1-x)}N}\right) - P_{PZ,Al_xGa_{(1-x)}N} \tag{1.8}$$

where $\sigma$ is the net polarization charge in the interface, $x$ is the Al composition, $P_{SP}$ and $P_{PZ}$ are spontaneous and piezoelectric polarization, respectively. By substituting

the parameters in the table 1.1 and linear interpolation,

$$\sigma = \left(P_{SP,GaN} - P_{SP,Al_xGa_{(1-x)}N}\right) - P_{PZ,Al_xGa_{(1-x)}N} \tag{1.9}$$

$$= \left[P_{SP,GaN} - (1-x)\,P_{SP,GaN} - xP_{SP,AlN}\right] - 2\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) \tag{1.10}$$

$$= \left\{5.2x - 2\frac{0.077x}{3.189 - 0.077x}\left[-11x - 49 - (73x+73)\frac{5x+103}{-32x+405}\right]\right\} \times 10^{-6} C/cm^2 \tag{1.11}$$

$$\approx \left[5.2x + \left(3.32x + 1.65x^2\right)\right] \times 10^{-6} C/cm^2 \tag{1.12}$$

where $a_0$ is the lattice constant of AlGaN in the thermal equilibrium, $a$ is the lattice constant of the AlGaN grown on the GaN channel which is equal to the equilibrium lattice constant of GaN, in this case, $e_{31}$ and $e_{33}$ are piezoelectric coefficients, $C_{13}$ and $C_{33}$ are elastic constants. All the $Al_xGa_{(1-x)}N$ parameters above are approximated by linear interpolation. Considering x is in the range of $[0, 1]$, Eq. 1.11 could be simplified to Eq. 1.12 by using linear approximation (first-degree Taylor Polynomial). With an assumption of $x = 0.2$ in this case, the net polarization charge is positive, which means there will be the same amount of free electrons in the AlGaN/GaN interface to compensate the fixed polarization charge, and the charge density $\frac{\sigma}{q}$ is around $1.1 \times 10^{13} cm^{-2}$. The unique 2DEG shows a high peak drift velocity and a high electron mobility, allowing for high voltage and low on-resistance applications.

Table 1.1: Spontaneous and piezoelectric parameters of AlN and GaN [1].

| **Parameters** | $P_{SP}$ $[C/cm^2]$ | $a_0$ [Å] | $e_{31}$ $[C/cm^2]$ | $e_{33}$ $[C/cm^2]$ | $C_{13}$ [GPa] | $C_{33}$ [GPa] |
|---|---|---|---|---|---|---|
| **GaN** | $-2.9 \times 10^{-6}$ | 3.189 | $-49 \times 10^{-6}$ | $73 \times 10^{-6}$ | 103 | 405 |
| **AlN** | $-8.1 \times 10^{-6}$ | 3.112 | $-60 \times 10^{-6}$ | $146 \times 10^{-6}$ | 108 | 373 |

GaN is mostly grown on SiC, sapphire, and silicon substrates. Among all those possible substrate materials, Si is the most attractive choice due to its large wafer diameter (8-inch and beyond) and lower cost compared to other candidates. However, due to the large mismatches in lattice constants and coefficients of thermal expansion

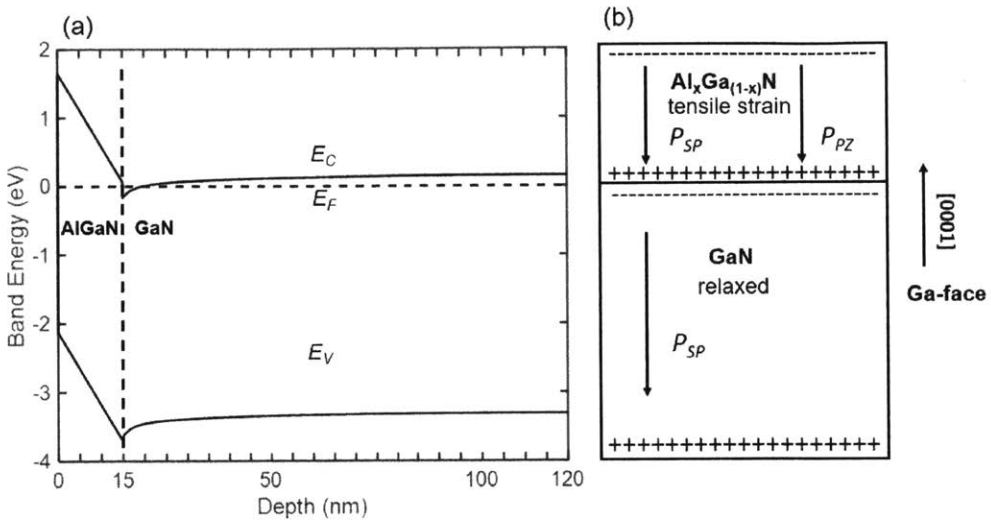



Figure 1-3: (a) Band diagram of the most common Ga-face AlGaN/GaN heterostructure; (b) Directions of spontaneous and piezoelectric polarization in the same structure.

(CTE) between GaN and Si (111) substrate, it is quite challenging to grow high-quality GaN buffers on large Si substrates. 650V GaN-on-Si e-mode devices in a 200 mm CMOS fab were demonstrated by IMEC in 2015 [25, 26]. Meanwhile, 750V fully vertical GaN-on-Si power diodes were reported by MIT in 2018 [27], which shows the potential and possibility of fully vertical GaN devices. Recently, p-channel GaN transistors were also successfully demonstrated with the capability of integration with n-channel e-mode GaN HEMTs on one chip [28]. Stable operation of GaN-based devices up to 1000°C was also reported [29, 30]. Given the rapid development in recent years of GaN technology in the aspects mentioned above, we need to reconsider GaN as a potential enabler in the field of high-temperature electronics.

## 1.4 Challenges of Gallium Nitride and Scope of Thesis

Despite the excellent performance shown by early high-temperature prototypes[31, 32, 29], several issues in traditional lateral AlGaN/GaN HEMTs could cause early

degradation and failure under high-temperature operation (over $300^oC$). These include ohmic degradation, gate leakage, buffer leakage, and poor passivation.

Besides, to enable digital circuit processing, it is critical to have normally-off or enhancement-mode HEMTs, while two-dimensional electron gas (2DEG) induced by AlGaN/GaN heterostructure makes HEMTs be natural depletion-mode devices. Two main approaches have been proposed to achieve the enhancement-mode behavior: recess-gate metal-insulator-semiconductor HEMTs (MISHEMTs) [33] and gate injection transistors (GITs) [34].

This thesis aims to solve the problems mentioned above, including ohmic contact reliability, e-mode operation, and large scale integration for possible high-temperature integrated circuits (ICs). A new ohmic contact scheme, GITs suitable for high-temperature operation and large scale integration, and logic building blocks for ICs will be developed and optimized. In particular, the thesis is divided into the following parts:

- **Chapter 2**: Study of ion-implanted tungsten contacts on HEMTs structure for high-temperature operation;

- **Chapter 3**: Self-aligned gate-first enhancement-mode Gate injection transistors (GITs) with the etch stop process for large scale integration and high-temperature operation;

- **Chapter 4**: Logic building blocks such as NAND/NOR gate performance based on transistor technology demonstrated above and high-temperature degradation test.

Chapter 2 introduces a comprehensive study conducted on the ion-implanted refractory metal contact on AlGaN/GaN HEMTs, including the high-temperature degradation of AlGaN/GaN heterostructure; the optimization of implantation condition based on the SRIM simulation results, the optimization of activation annealing condition; the influence of different metals on contact performance; ohmic recess technology to improve contact performance.

Chapter 3 presents self-aligned gate-first enhancement-mode GITs with the etch-stop process. The wafer structure was first designed based on the TCAD simulation, following with a study of the etch-stop process to selectively remove p-GaN. The effects of different gate metals on threshold voltages and gate leakage currents will be discussed. Finally, the results of high-temperature measurements on the devices with those optimized processes will be shown.

In chapter 4, compact modeling for both E/D-mode HEMTs will be demonstrated based on MIT Virtual Source GaN (MVSG) model [35]. The experimental results of the fabrication and characterization of several critical logic building blocks, including inverter, NAND/NOR gate, SRAM, and ring oscillators, will be presented. A comparison between E/D-mode and E/E-mode direct-coupled FET logic (DCFL) will also be included.

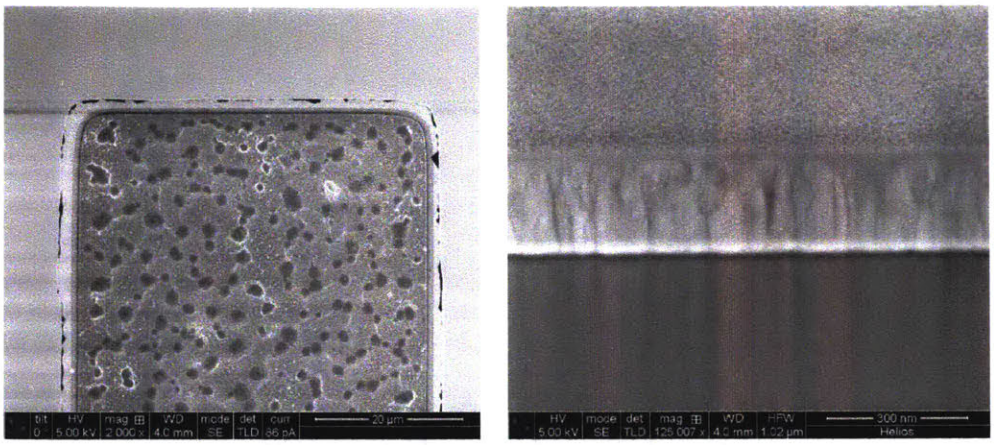
# Chapter 2

# Study of the Ion-implanted Refractory Metal Contact

## 2.1 Introduction

Ohmic contacts in AlGaN/GaN HEMTs are typically made of Ti/Al/(Ni, Ti, Pt, Mo, etc.)/Au metal stacks annealed around 800°C [36] to obtain a low ohmic contact resistance around $1 \times 10^{-6}\ \Omega \cdot cm^2$. Although these contacts have shown excellent performance at room temperature, they are typically unstable above 250°C, due to the diffusion of Ti, Al, and Au into the structure [37]. This metallization scheme leads to a rough surface morphology as shown in Fig. 2-1 and has been linked to degradation and failure[37, 38].

There are several potential approaches to replace the traditional alloyed contact including the ion-implanted metal contact [39, 40, 41], which locally dopes the materials n-type by implantation and reduces the contact resistance, and regrown ohmic contact, which selectively remove the AlGaN in the contact region and regrown n-type (Al)GaN [42]. Considering the negligible dopant diffusion under 600°C in wide bandgap materials [3] and potential defects in regrown surface, ion implantation is considered to be a superior choice for high-temperature operation. Besides, benefiting from the n-doped ohmic region, a large variety of Si CMOS compatible metals could be used as contacts, and better surface morphology could be achieved as well



(a) Top view of conventional Ti/Al/Ni/Au contacts by SEM.

(b) Tilt view of ion implanted tungsten (W) contacts by FIB-SEM.

Figure 2-1: Comparison of contact surfaces between traditional alloyed contact and implanted refractory metal contact.

to improve the subsequent photo-lithography performance without post-annealing. However, unlike the ion implantation technology ubiquitously used in Si-based devices, ion implantation technology in the AlGaN/GaN heterostructure requires further optimizations in many aspects: doping profile, implantation energy, dose, dopant activation, and damage recovery.

Implantation energy, dose, and ion beam incident angle need to be carefully engineered to obtain the desired doping profile and best contact performance. Moreover, dopant activation is also a crucial step in ion implantation technology due to the inert nature of AlGaN and GaN. A successful activation annealing at 1500°C in nitrogen was reported [39], which is well beyond the capabilities of typical Si processing tools and higher than the growth temperature of GaN by either metal-organic chemical vapor deposition (MOCVD) or molecule beam epitaxy (MBE) [43]. Besides, the massive differences in coefficients of thermal expansion (CTE) between AlGaN, GaN, and Si substrate would degrade the heterostructure integrity and reduce the 2DEG density and mobility at high annealing temperature [44]. Thus, it is preferable to have a lower annealing temperature to preserve the crystalline integrity and achieve a similar dopant activation ratio.

## 2.2 Degradation of AlGaN/GaN Heterostructure and Activation Annealing Capping Layer

In standard AlGaN/GaN HEMTs, the on-resistance mainly consists of two parts: contact resistance and channel resistance, which includes access resistance from source- and drain-to-gate region and channel resistance at the gated region. The former could be improved by increasing the activation ratio of the implanted Si-ions usually by increasing activation annealing time and temperature, while the latter has a strong dependence on sheet resistance. The sheet resistance is proportional to the product of mobility and carrier density of 2DEG, and tends to increase after high-temperature activation annealing.

Before we start to test the effects of activation annealing conditions on dopant activation, we first need to figure out the degradation of 2DEG density and mobility caused by the activation annealing in order to keep a low sheet resistance.

### 2.2.1 Device Structure

The epitaxial structures investigated here were grown by metal-organic chemical vapor deposition (MOCVD) on both the sapphire substrate from Arizona State University (ASU) and the silicon substrate from Lincoln Lab (LL). The epitaxial structure of GaN-on-sapphire wafer has a 15 nm $Al_{0.2}Ga_{0.8}N$ barrier layer, while the epi-structure of GaN-on-Si wafer has a 17 nm $Al_{0.2}Ga_{0.8}N$ barrier layer. It is worth mentioning that wafers from LL compared with wafers from ASU has an additional AlN spacer at AlGaN/GaN interface in order to increase the mobility. Fig. 2-2 shows the epi-structure of GaN HEMTs. The 2DEG density and Hall mobility at room temperature of GaN-on-sapphire samples were $8.2 \times 10^{12}\ cm^{-2}$ and 1732 $cm^2V \cdot s$ and those of GaN-on-Si samples were $\sim 1 \times 10^{13}\ cm^{-2}$ and $\sim 2000\ cm^2V \cdot s$, respectively.

The fabrication started with the deposition of 60 nm $SiO_2$ by plasma-enhanced chemical vapor deposition (PECVD) at 350°C. No implantation was performed on the samples to avoid possible influence on the subsequent measurements of carrier

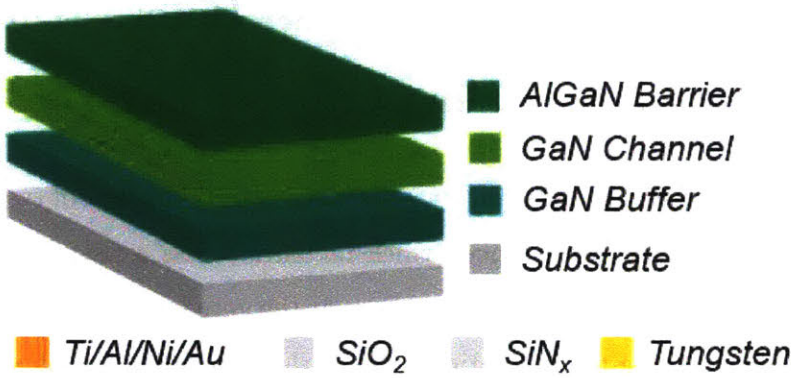



Figure 2-2: Epi-structure of standard AlGaN/GaN HEMTs.

density and mobility. Samples were annealed at different combinations of time and temperatures by rapid thermal annealing (RTA). After activation annealing, thermal annealed $SiO_2$ was then removed by buffered oxide etch (BOE). The standard Ti/Al/Ni/Au (20/100/25/50 nm) metal stack was subsequently e-beam evaporated and lifted off, following with 800°C post-annealing for 30 s in $N_2$ ambient by RTA to form ohmic contacts. $\sim$ 140 nm mesa isolation was carried out by $BCl_3/Cl_2$ based electron cyclotron resonance reactive-ion etching (ECR-RIE). Van der Pauw structures were made to characterize carrier density and mobility.

### 2.2.2 Results and Discussion

Table 2.1 shows the different activation annealing conditions for both GaN-on-sapphire and GaN-on-Si samples. Ideally, GaN-on-sapphire samples should have less built-in stress compared to GaN-on-Si samples due to the smaller difference between lattice constants of GaN and sapphire, and were annealed longer at the beginning. Besides, our main interest was focused on GaN-on-Si samples, and more activation annealing conditions were tested subsequently. Hall measurements were conducted at room temperature to characterize the 2DEG densities and mobilities of both samples, as shown in Fig. 2-3 and Fig. 2-4.

Both GaN-on-sapphire and GaN-on-Si samples show degradations of 2DEG densities and mobilities, implying damage to the lattice integrity caused by activation

annealing. As expected, increasing temperature and extending annealing time would further degrade both mobility and carrier density.

Compared with GaN-on-sapphire samples, GaN-on-Si samples shows less degradation on mobility due to the AlN spacer between AlGaN and GaN, which significantly reduces the alloy disorder scattering. At room temperature or above, phonon scattering is usually the dominant scattering mechanism limiting the 2DEG mobility [12, 13, 14, 45]. However, the decrease of mobility indicates an increase in scattering mechanisms which could be explained by several reasons: increase of charged ion impurity due to the increase of vacancies and dislocations caused by nitrogen out-diffusion in the bulk, alloy and charged dislocations at the interface due to AlN interlayer degradation, more interface roughness, increase of piezoelectric scattering due to the decrease of 2DEG density. All the aspects mentioned above will permanently reduce the 2DEG mobility at room temperature. Similarly, the degradation of lattice integrity, which influences both spontaneous polarization and piezoelectric polarization, will also have a negative impact on polarization charge density.

Besides, cracks were also observed on both the GaN surface and on the $SiO_2$ surface, as shown in Fig. 2-5. Microcracks were observed after activation annealing at 1200°C for 30 s. After replacing the $SiO_2$ layer with a zero stress $SiN_x$ deposited by mixed frequency PECVD, no microcracks were observed.

Based on the results shown in Fig. 2-3 and Fig. 2-4, activation annealing at $1200^oC$ for 30 $s$ in $N_2$ ambient was selected as a preferred annealing condition in the following sections. Activation annealing effect on contact performance will be discussed in the following sections.

## 2.3 Study of the Si-ion Implanted Refractory Contact

The idea of the ion-implanted ohmic contact is to n-dope the ohmic region to help electrons tunnel through the metal-semiconductor junction and form a direct electrical

Table 2.1: Different activation annealing conditions[1].

| Sample | Temperature | Time |
|---|---|---|
| **GaN-on-sapphire** | 1100°C | 15 s |
| | | 30 s |
| | 1200°C | 10 s |
| | | 30 s |
| **GaN-on-Si** | 1100°C | 5 s |
| | | 15 s |
| | 1200°C | 5 s |
| | | 10 s |
| | | 30 s |
| | | 45 s |
| | | 15 s×2[2] |
| | | 15 s×3[3] |

[1] All the activation annealings were performed in $N_2$ ambient.
[2] Sample was first heated up to 1200°C for 15 s, cooled down to 700°C and then heated up to 1200°C for 15 s again.
[3] Similar to the previous condition, sample was heated up to 1200°C for 15 s for three times.

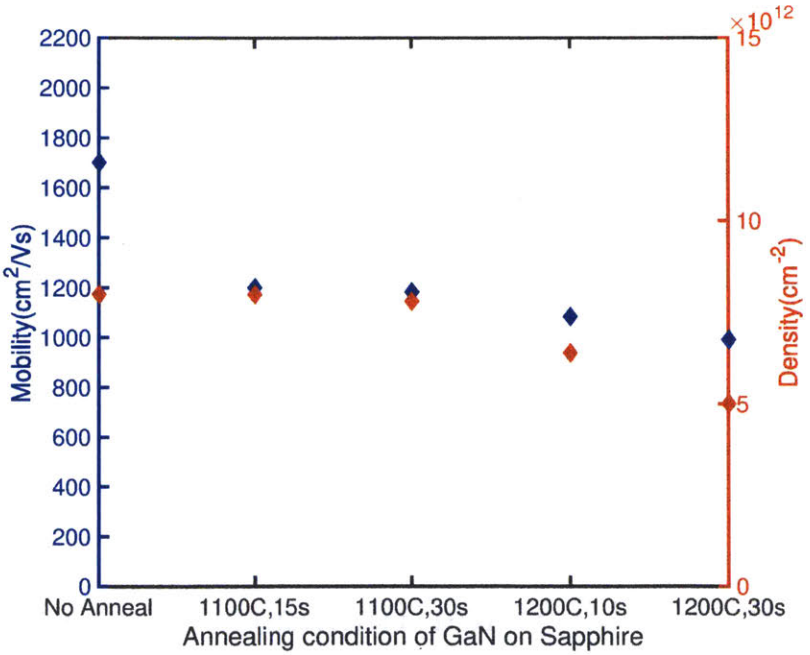



Figure 2-3: 2DEG density and mobility versus activation annealing condition for GaN-on-sapphire samples.

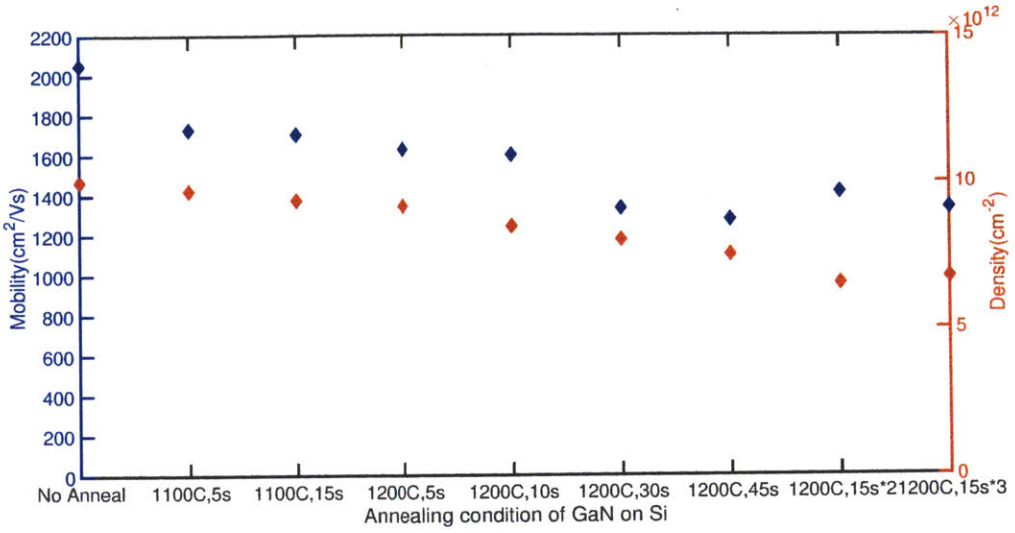



Figure 2-4: 2DEG density and mobility versus activation annealing condition for GaN-on-Si samples.

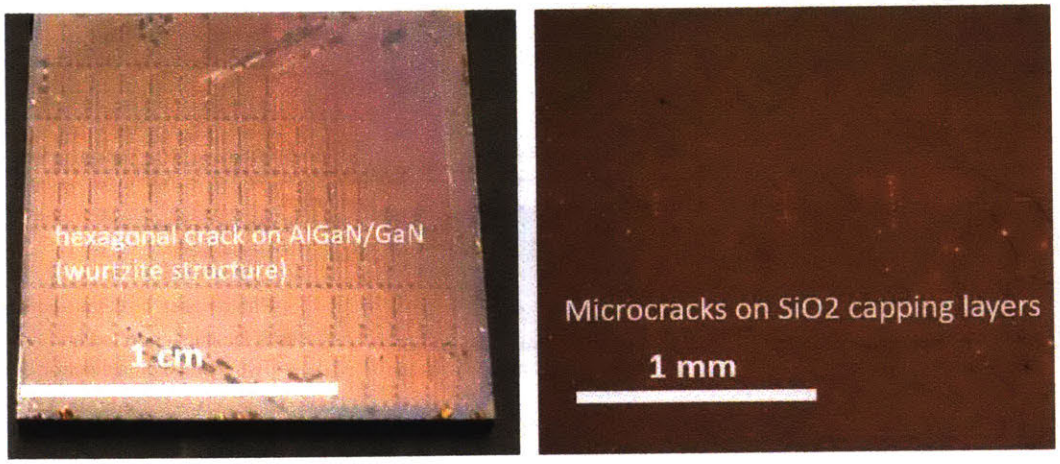



Figure 2-5: (Left) Cracks on the sample surface caused by large CTE difference; (Right) Microcracks of $SiO_2$ after activation annealing.

path to the 2DEG at the AlGaN/GaN interface. Silicon and Germanium are common n-type dopants in the GaN. In this work, silicon would be used due to its smaller atomic number, and thus lower energy is required to have a similar doping profile, while less damage is expected from Si implantation.

Doping profile and dopant concentration are critical to successful ion implantation, which is determined by implantation energy and dose. First, a Monte Carlo

simulation was conducted to estimate the ion distribution through a software named Stopping and Range of Ions in Matter (SRIM) [46]. Single energy implantation would give us a Gaussian profile, while a box profile could be obtained with double energy implantation. Besides, to avoid ion channeling, the incident beam was tilted 7 degrees following the standard rules of implantation for Si-based devices.

### 2.3.1 Epitaxial Structure and Fabrication

The epitaxial stack used in this work was grown by MOCVD on a 6 inch Si (111) substrate. The structure from top to bottom is 2 nm GaN, 17 nm $Al_{0.2}Ga_{0.8}N$, GaN channel, carbon-doped GaN buffer, and Si (111) substrate. The 2DEG density and hall mobility at room temperature were $\sim 1 \times 10^{13}\ cm^{-2}$ and $\sim 2000\ cm^2V \cdot s$, respectively.

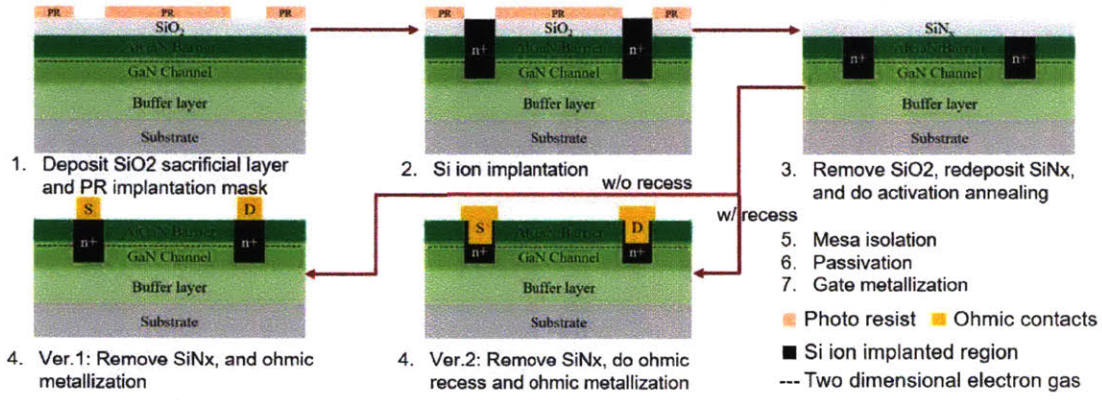



Figure 2-6: Pseudo-process flow.

Given the pseudo-process flow shown in Fig. 2-6, the fabrication was started with 40 nm $SiO_2$ deposition by PECVD to avoid possible contamination during implantation, and to randomize implanted ions incident angle and to adjust peak position of doping profile. Different Si-ion implantation conditions were simulated by SRIM, as listed in Tab.2.2, 2.3, and 2.4. Key simulation results are shown in Fig. 2-8. Two peak locations of doping profiles were chosen: either at the top surface or AlGaN/GaN interface. There are three implantation schemes summarized in Fig. 2-7: (1) No implantation, used as a reference; (2) All implanted (including both ohmic and channel

region); (3) Selective implantation in the ohmic region. After implantation, $SiO_2$ was removed by BOE, and 40 nm $SiN_x$ was then deposited by PECVD on top to protect the sample surface and prevent possible nitrogen diffusion. Activation annealing was carried out at 1200°C for 30 s in $N_2$ ambient by RTA, following with $SiN_x$ removal by BOE. 20 nm ohmic recess was partially performed by ICP-RIE on a Si holder to test the effect of ohmic recess, which should reduce the resistance induced by the AlGaN region. The recess depth was examined by atomic force microscope (AFM). After ohmic recess, two different metal schemes were adopted: tungsten metal contacts were sputtered and dry-etched by RIE with $SF_6/O_2$ mixture; Ti/Al metal contacts were defined by e-beam evaporation. There was no post-annealing process for both contact schemes. $\sim$ 140 nm mesa isolation was then performed by ECR-RIE with $BCl_3/Cl_2$.

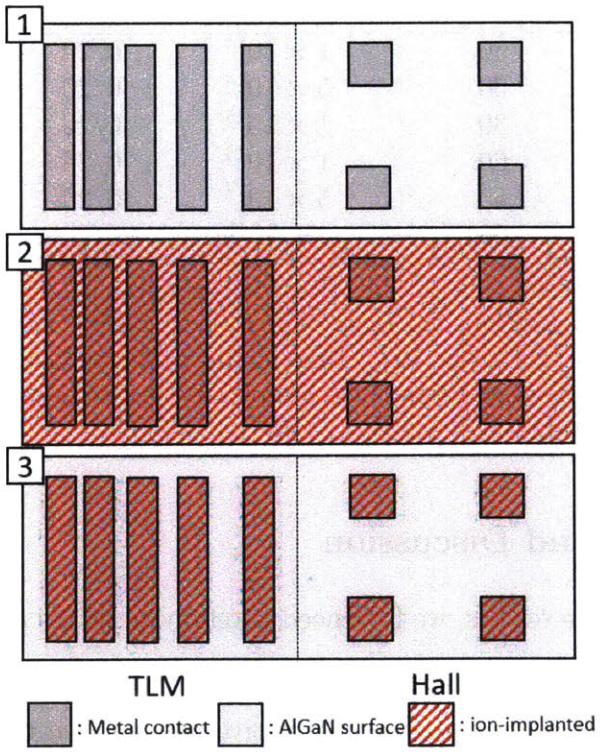



Figure 2-7: TLM and Hall patterns with different implantation schemes: (1) No implantation, used as a reference; (2) All implanted (including both ohmic and channel region); (3) Selective implantation in the ohmic region.

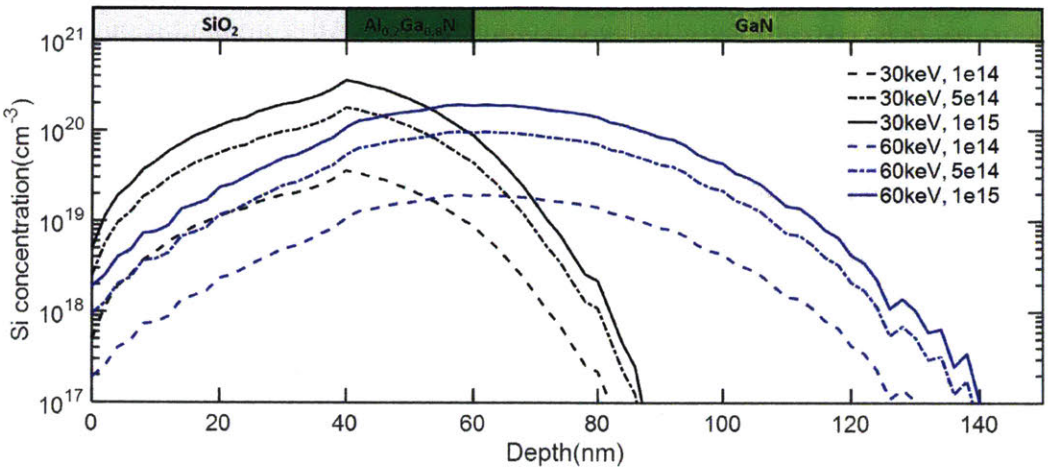



Figure 2-8: Doping profiles simulated by SRIM.

Table 2.2: Ion implantation parameters of samples in the $1^{st}$ batch.

| **Sample** # | $1^{st}$**-Energy** [keV] | $1^{st}$**-Dose** $[cm^{-3}]$ | **Recess** [nm] | **Contact** |
|---|---|---|---|---|
| 1 | 30 | $1 \times 10^{14}$ | 0/20 | Ti/Al[2] |
| 2 | 30 | $5 \times 10^{14}$ | 0/20 | Ti/Al |
| 3 | 30 | $1 \times 10^{15}$ | 0/20 | Ti/Al |
| 4 | 60 | $1 \times 10^{14}$ | 0/20 | Ti/Al |
| 5 | 60 | $5 \times 10^{14}$ | 0/20 | Ti/Al |
| 6 | 60 | $1 \times 10^{15}$ | 0/20 | Ti/Al |

[1] Implanted ion species was Si. Tilt/Twist angles were all 7/23 degrees, and implantation were all performed at room temperature. All the activation annealings were performed at 1200°C for 30 s. Same for the following batches.
[2] Ti/Al (20/100 nm) were defined by e-beam evaporation. No post-annealing was conducted afterward.

### 2.3.2 Results and Discussion

Before we dive into the results, we first need carefully to define the contact resistance of implanted contacts. General contact resistance is typically referred to as the total resistance from metal contact to the conductive channel. In the case of selectively implanted contact, the situation becomes complicated due to the large additional resistance between the implanted contact region and the 2DEG channel without implantation, as shown in Fig. 2-9. Contact resistance, in this case, could be divided into two components:

Table 2.3: Ion implantation parameters of samples in the $2^{nd}$ batch.

| **Sample** # | $1^{st}$-**Energy** [keV] | $1^{st}$-**Dose** $[cm^{-3}]$ | **Recess** [nm] | **Contact** |
|---|---|---|---|---|
| 7 | 60 | $7 \times 10^{14}$ | 20 | Tungsten[1] |
| 8 | 60 | $1 \times 10^{15}$ | 20 | Tungsten or Ti/Al |
| 9 | 60 | $2 \times 10^{15}$ | 20 | Tungsten |
| 10 | 60 | $3 \times 10^{15}$ | 20 | Tungsten |

[1] 100 nm Tungsten was sputtered and dry etched. No post-annealing was performed. The Resistivity of Tungsten film is $\sim 0.158\ \mu\Omega \cdot m$ measured by 4 point probe measurement. Same for the subsequent experiment.

Table 2.4: Ion implantation parameters of samples in the $3^{rd}$ batch.

| **Sample** # | $1^{st}$-**Energy** [keV] | $1^{st}$-**Dose** $[cm^{-3}]$ | $2^{nd}$-**Energy** [keV] | $2^{nd}$-**Dose** $[cm^{-3}]$ | **Recess** [nm] | **Contact** |
|---|---|---|---|---|---|---|
| 11[1] | 60 | $2 \times 10^{15}$ | \ | \ | 20/30/40 | Tungsten |
| 12 | 60 | $1.5 \times 10^{15}$ | 30 | $0.5 \times 10^{15}$ | 20 | Tungsten |

[1] Implantation at 60 keV with a dose of $2 \times 10^{15}$ and 20 nm ohmic recess was performed on multiple samples to test the repeatability.

$R_{c1}$: Contact resistance in the metal/semiconductor surface.

$R_{c2}$: Access resistance in the transition region from implanted region to 2DEG channel caused by lattice damage.

### Method to Extract $R_c$, $R_{c1}$ and $R_{c2}$

$R_{c1}$ can be extracted by TLM measurements from the patterns shown in Fig. 2-7 (2) with both ohmic and channel implanted. In this case, doped AlGaN/GaN serves as channel and no $R_{c2}$ is present. $R_c$ can be directly measured by the structure in Fig. 2-7 (3) with selectively implanted ohmic region. $R_{c2}$ could be approximated by $R_c - R_{c1}$.

The goal of contact optimization is to reduce both $R_{c1}$ and $R_{c2}$ by choosing proper implantation and activation conditions.

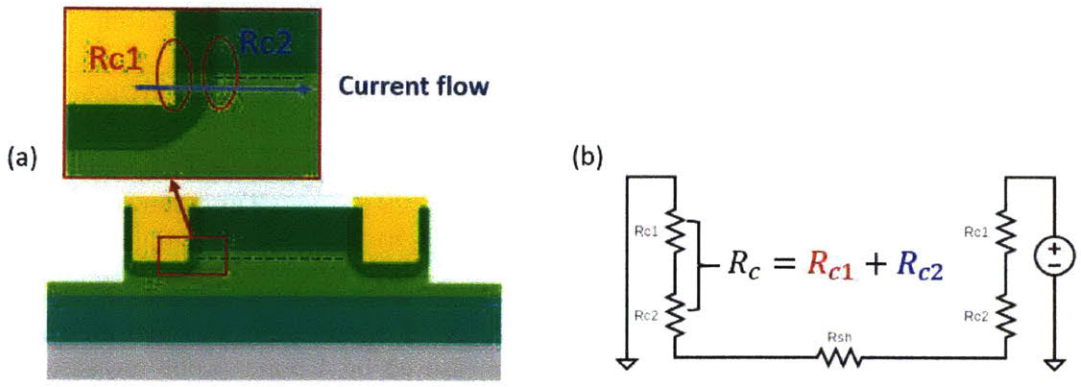



Figure 2-9: (a) Cross-section of selectively implanted contacts; (b) Circuit schematic. $R_{c1}$ is the contact resistance in the metal/semiconductor surface, while $R_{c2}$ is the access resistance in the transition region from the implanted region to the 2DEG channel.

### Effects of Ohmic Recess and Implantation Energy

A preliminary study of ohmic recess and implantation energy effect was conducted on batch 1 samples. The TLM IV curves without ohmic recess from sample 1, which was implanted at 30 keV with a dose of $1 \times 10^{14}\ cm^{-2}$, are shown in Fig. 2-10. Schottky behaviors can be observed, indicating that the dose and activation ratio are not high enough to help electrons tunneling through the Schottky barrier in the metal/semiconductor interface and form a good ohmic contact. As expected, similar behaviors can also be observed from Fig. 2-11 for sample 4 implanted at 60 keV with a dose of $1 \times 10^{14}\ cm^{-2}$ and no ohmic recess involved, which proves our assumption.

Compared with sample 1, sample 4 shows a higher contact resistance, which means that without ohmic recess, shallower implantation (30 keV) would help reduce ohmic contact due to higher doping concentration close to the interface with the same dose.

The results from sample 2-3 and 5-6 in Tab. 2.5 indicate that a better contact performance can be obtained by implantation at 60 keV and ohmic recess. Ohmic recess will remove the AlGaN barrier, which has a higher resistivity and bandgap, and form a direct contact to the GaN underneath where the peak doping concentration is located. It is worth noting that the contact resistance of standard alloyed Ti/Al/Ni/Au is $\sim 0.5\ \Omega \cdot mm$ [39].

Besides, a further study was conducted on sample #11 about the contact resistance dependence on recess depth. A low $R_c$ of $\sim 0.3\ \Omega \cdot mm$ was obtained when the sample was implanted at 60 keV with a dose of $2 \times 10^{15}\ cm^{-2}$ and a recess depth of 20 nm. As can be seen in Fig. 2-12, similar $R_c$ can be achieved with different recess depths. A small increase of $R_c$ can be observed with a recess depth of 40 nm. The results indicate that the ohmic recess technique demonstrated here has a high tolerance for recess depth with the help of ion implantation.

In summary, for single energy implantation, the optimum implanted contact scheme is to set the peak of the doping profile close to the AlGaN/GaN interface, and perform ohmic recess. In this case, Si implantation at energy of 60 keV and 20 nm recess is preferred, and there is no strict requirement on ohmic recess depth, which could range from 20 nm to 40 nm.

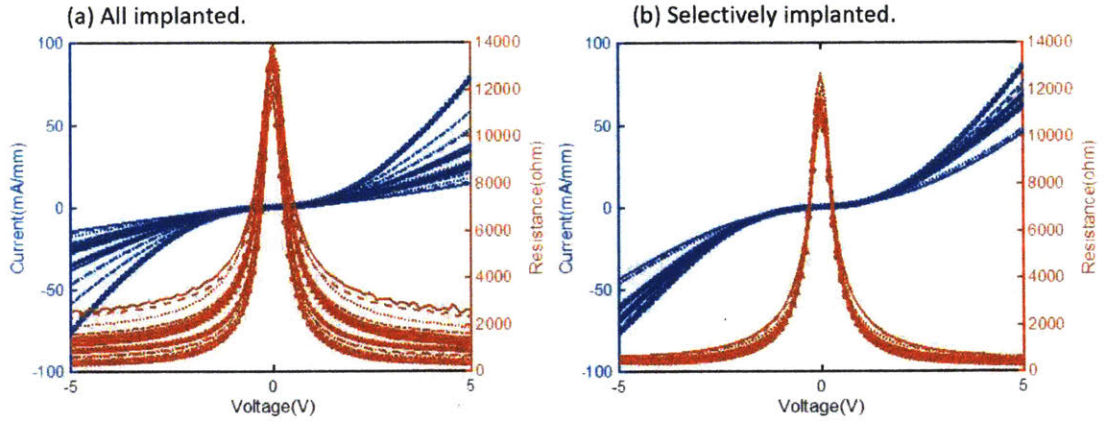



Figure 2-10: (a) TLM IV curves with the distance ranging from 2 to 42 um for sample #1 all implanted at 30 keV with a dose of $1^{14}\ cm^{-2}$; (b) Same parameters as (a), but sample was selectively implanted.

### Effects of Different Ohmic Metals

Alloyed Ti/Al/Ni/Au is the most common contact scheme in AlGaN/Gan HEMTs with several disadvantages, such as bad surface morphology, requirements of a specific metal stack, and post-annealing. It is appealing to use Si CMOS compatible metals as contacts. With the help of a highly doped ohmic region, many metals become

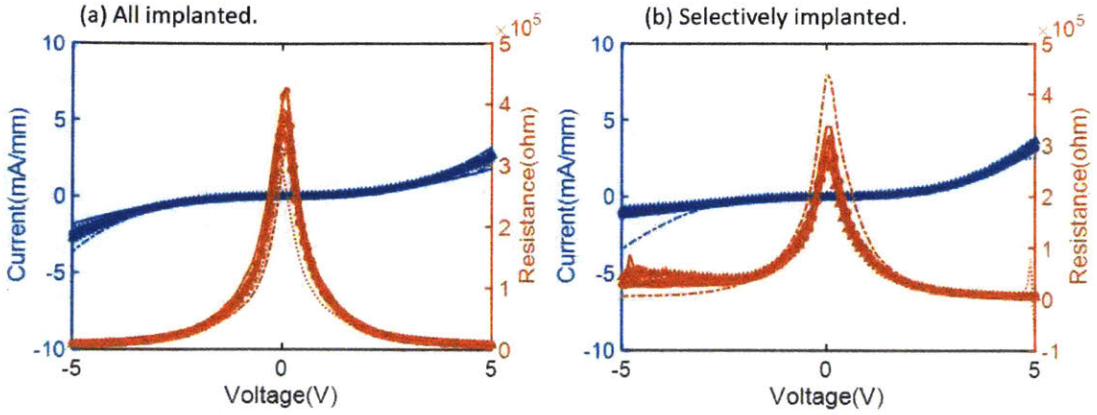



Figure 2-11: (a) TLM IV curves with the distance ranging from 2 to 42 um for sample #4 all implanted at 60 keV with a dose of $1^{14}$ $cm^{-2}$; (b) Same parameters as (a), but sample was selectively implanted.

Table 2.5: $R_c$ of samples in the $1^{st}$ batch.

| **Sample** # | $1^{st}$-**Energy** [keV] | $1^{st}$-**Dose** $[cm^{-3}]$ | **Recess** [nm] | **Contact** | $R_c$ $[\Omega \cdot mm]$ |
|---|---|---|---|---|---|
| 2 | 30 | $5 \times 10^{14}$ | 0 | Schottky | 3.83 |
| | | | 20 | Ohmic | 1.84 |
| 3 | 30 | $1 \times 10^{15}$ | 0 | Ohmic | 2.56 |
| | | | 20 | Ohmic | 2.05 |
| 5 | 60 | $5 \times 10^{14}$ | 0 | Schottky | 4.45 |
| | | | 20 | Ohmic | 1.68 |
| 6 | 60 | $1 \times 10^{15}$ | 0 | Schottky | 2.67 |
| | | | 20 | Ohmic | 0.65 |

available, and tungsten, also known as a kind of refractory metal, was chosen here for high-temperature applications.

Sample # 8 was designed to compare the difference of $R_c$ between non-alloyed Ti/Al and tungsten contacts. It can be observed from Fig. 2-13 that all three contact schemes have similar $R_c$. It shows the possibility of an Au-free CMOS compatible process.

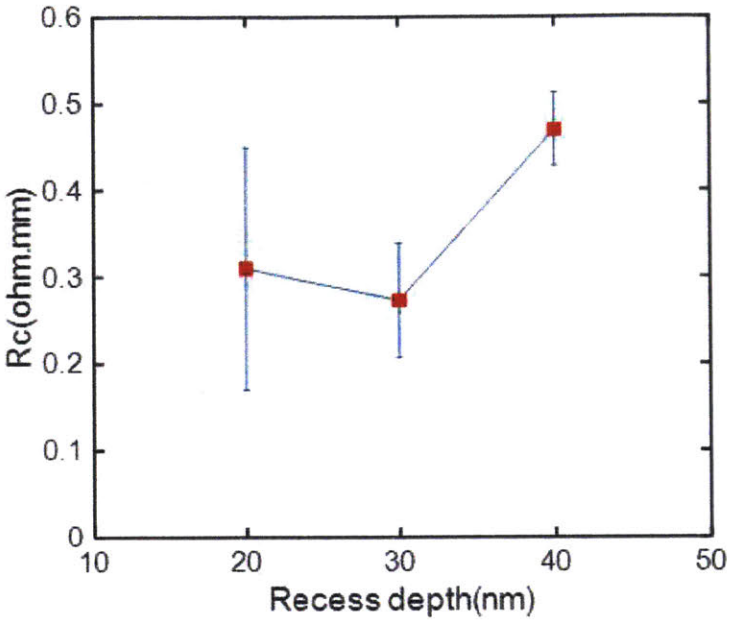



Figure 2-12: Contact resistance versus recess depth. The sample here was implanted at 60 keV with a dose of $2 \times 10^{15}\ cm^{-2}$

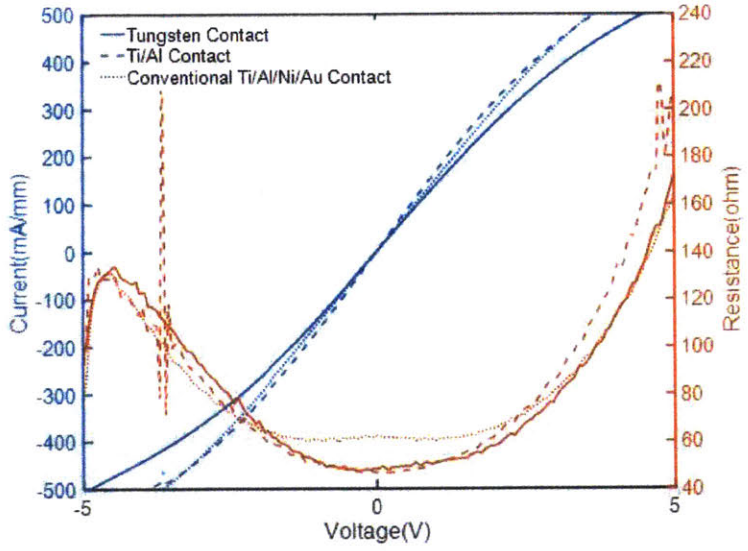



Figure 2-13: IV curve of a TLM pattern with a distance of 4 um from Tungsten contact, non-alloyed Ti/Al contact and alloyed Ti/Al/Ni/Au contact, respectively.

### Effects of Implantation Dose on $R_c$ and Activation ratio

A comprehensive dose test was performed at batch 2 based on the results from batch 1. Implantation energy and ohmic recess depth were set as 60 keV and 20 nm, respectively. The dose was ranging from $7 \times 10^{14}\ cm^{-2}$ to $3 \times 10^{15}\ cm^{-2}$. TLM results are shown in Fig. 2-14. $R_{c1}$ decreases with dose, while $R_{c2}$ shows a minimal value with a dose of $1 \times 10^{15}\ cm^{-2}$. A best $R_c$ of $\sim 0.3\ \Omega \cdot mm$ was obtained with a dose of $2 \times 10^{15}\ cm^{-2}$.

The activation ratios shown in Fig. 2-15 are estimated by the number of activated ions over the number of implanted ions:

$$\text{Activation Ratio} = \frac{\#\text{ of Activated Ions}}{\#\text{ of Implanted Ions}} \tag{2.1}$$

where the number of activated ions can be estimated by subtracting the 2DEG density from the measured Hall density, the number of implanted ions is the integral of the Si doping concentration in AlGaN/GaN structure based on the results from TRIM simulation.

A linear dependence of the activation ratio on the dose in AlGaN/GaN in log scale can be observed, and the highest activation ratio could increase up to $\sim 40\%$. With a fixed activation annealing condition at 1200°C for 30 s, the linear dependence in log scale can be fitted as:

$$\text{Activation Ratio} = \left[30 + 29 \log\left(\frac{\text{dose}}{1 \times 10^{15}\ cm^{-2}}\right)\right] \% \tag{2.2}$$

The linear dependence of activation ratio on dose indicates that the vacancies and interstitials created by implantation might enhance the electrical activation of the ions implanted.

The decrease of $R_{c1}$ versus dose could be explained by the increase of dose and activation ratio. While $R_{c1}$ is defined as the contact resistance between metal/semiconductor. The increasing number of free electrons close to the interface will help electrons tunneling through the Schottky barrier and thus reduce the $R_{c1}$. $R_{c2}$ is the access resistance

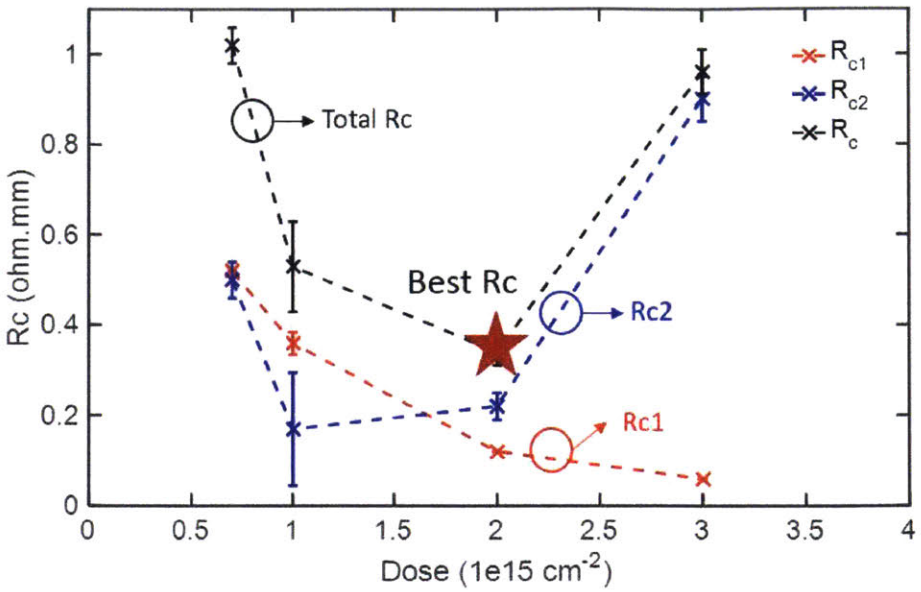



Figure 2-14: $R_c$, $R_{c1}$ and $R_{c2}$ versus dose.

between the 2DEG channel and the implanted region. On the one hand, increase doping level would help to reduce the resistance, on the other hand, the increase of lattice damage and charged impurities would degrade 2DEG density and mobility close to the implanted region and thus increase the resistance, which explains the well curve of $R_{c2}$.

### Repeatability Test

To test the repeatability of this implanted ohmic scheme, the same implantation scheme was conducted on multiple samples, and the results are shown in Fig. 2-16. The mean value is $\sim 0.3\ \Omega \cdot mm$, while the large variation is introduced by large sheet resistance.

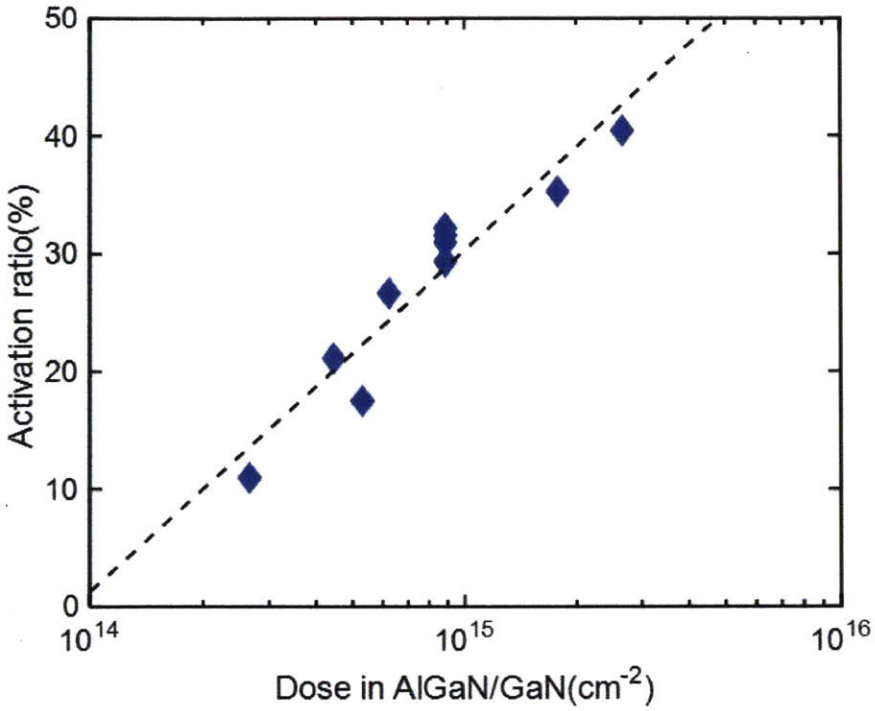



Figure 2-15: Activation Ratio versus dose in AlGaN/GaN heterostructure.

### Effects of Activation Annealing Conditions

In section 2.2, the effect of activation annealing condition on 2DEG carrier density and mobility was studied. It shows that high temperature and "long" time annealing by RTA would cause irreversible lattice degradation and thus increase sheet resistance. In this section, activation annealing condition on the activation ratio would be studied.

Activation annealing temperature effect on contact resistance was fist studied. The AlGaN/GaN structure had a 20 nm $Al_{0.25}Ga_{0.75}N$ barrier layer. The 2DEG sheet density and mobility at room temperature were $8.8 \times 10^{12}$ $cm^{-2}$ and 1704 $cm^2V \cdot s$, respectively. Device fabrication was started with the deposition of 40 nm $SiO_2$ by PECVD as a protection layer. Si ions were then implanted with a dose of $2 \times 10^{15}$ $cm^{-2}$ at an energy of 20 keV and 60 keV. Activation annealing was performed under 1100°C or 1200°C in $N_2$ ambient for 5 s. After annealing and removing the $SiO_2$, different metallization schemes were carried out, including non-alloyed Ti/Al/Ni/Au and tungsten contact without ohmic recess. After device isolation by ECR-RIE,

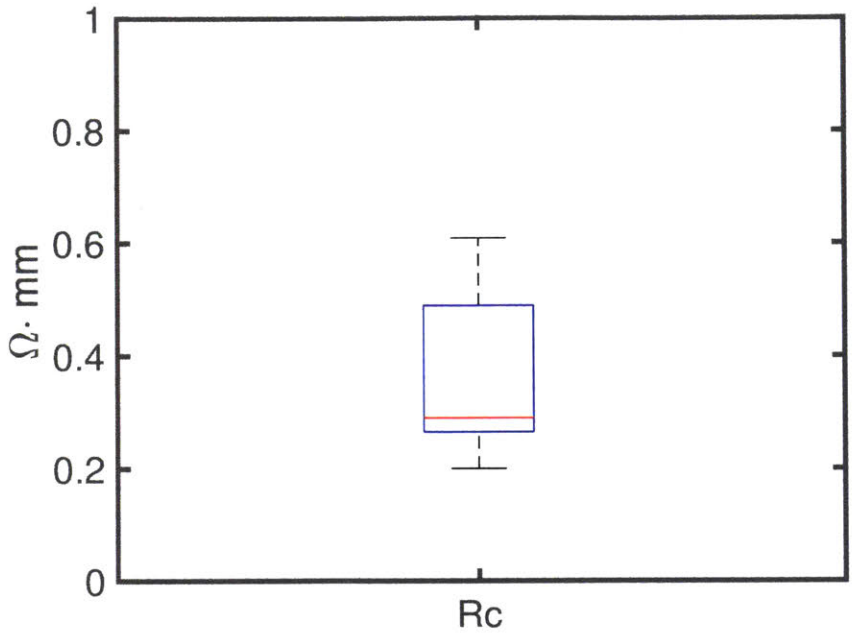



Figure 2-16: Contact resistance of sample #11 which is implanted at 60 keV with a dose of $2 \times 10^{15}$ $cm^{-2}$ and annealed at 1200°C for 30 s.

the transmission line method (TLM) was then performed to determine the contact resistance and sheet resistance. The results in Fig. 2-17 shows that 1200 °C is critical to have dopant activated.

The effect of Activation annealing time was then studied with the same process and similar sample structure. The results are shown in Fig.2-18. The only difference is that the samples studied here were annealed multi-times to compare the $R_c$. As expected, longer activation time would noticeably reduce the contact resistance, implying a higher activation ratio.

### 2.3.3 High Temperature Degradation Test

It is critical to perform high-temperature degradation tests on this contact scheme to prove the capability of implanted refractory metal for high-temperature operation. Here, samples were selectively implanted at 60 keV with a dose of $2 \times 10^{15}$ $cm^{-2}$. No ohmic recess and $SiN_x$ passivation were performed in this case. Both in-situ and

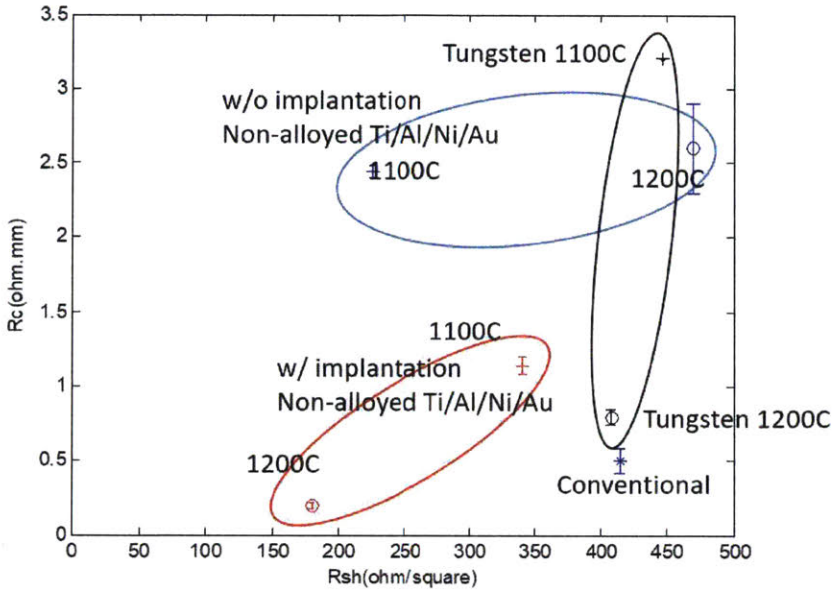



Figure 2-17: $R_c$ v.s. $R_{sh}$ with different combinations of metals and activation annealing conditions. The contact activated at 1200°C shows much better performance. It is worth noting that only samples with tungsten contacts were selectively implanted, while the samples with non-alloyed Ti/Al/Ni/Au contacts were all-implanted which means that the measured contact resistance is $R_{c1}$ in this case.

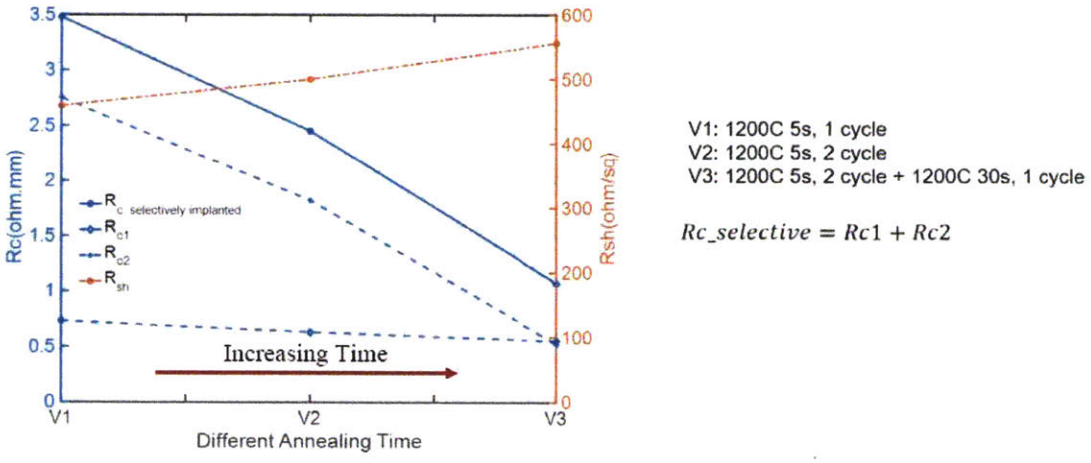



Figure 2-18: $R_c$ and $R_{sh}$ versus annealing condition.

ex-situ measurements were then conducted to observe the potential degradation.

A high-temperature probe station built with a hot plate was used for in-situ measurement. The sample was characterized from room temperature up to 300 °C in

air ambient. At each temperature, the sample stayed for more than one hour until the sample surface reached the set temperature, and TLM was then performed to extract the contact resistance. The implanted contacts show great thermal stability up to 300°C without degradation, as seen in Fig. 2-19 (top).

For the ex-situ measurement, the sample was first put in a furnace and then heated to 500°C in $N_2$ ambient. The sample stayed in the furnace for up to 10 hours until it was taken out for the TLM measurement at room temperature. As shown in Fig. 2-19 (bottom), this contact scheme presents excellent thermal stability even after stayed at 500°C for 10 hours.

## 2.4 Conclusion

Ion implanted refractory metal contact has been developed for AlGaN/GaN HEMTs and other AlGaN/GaN-based devices, which shows high repeatability and high performance. A best $R_c$ of $\sim 0.3\ \Omega \cdot mm$ was achieved when the sample was Si-ion implanted at 60 keV with a dose of $2 \times 10^{15}\ cm^{-2}$ and annealed at 1200°C for 30 s. This contact scheme shows excellent thermal stability verified by in-situ measurement up to 300°C in air and ex-situ measurement up to 500°C for 10 hours in $N_2$.

The doping profile, determined by implantation energy and dose, activation annealing temperature and time, activation capping layer, ohmic recess, ohmic metal, and thermal stability of the final contacts, were comprehensively studied and optimized in this section.

For single energy implantation, the optimum doping profile is to set the peak close to the AlGaN/GaN interface with ohmic recess to achieve better performance. The contact resistance could be divided into two parts: $R_{c1}$ and $R_{c2}$. The former is inversely proportional to the dose, while the latter has a well shape versus dose. To achieve minimal $R_c$, a dose of $2 \times 10^{15}\ cm^{-2}$ is suggested. Besides, the activation ratio shows a linear dependence on dose in log scale, and an activation ratio of $\sim 40\%$ could be achieved with a dose of $2 \times 10^{15}\ cm^{-2}$.

Activation annealing temperature and time are critical to achieving low contact

resistance. Increasing temperature and time would decrease contact resistance. However, further increase of temperature and time would cause unwanted degradation of 2DEG density and mobility, possible cracks due to the difference between lattice constants and CTEs of GaN and substrates, resulting in a larger on-resistance and lower yield.

Moreover, with the help of implantation, better surface morphology could be achieved, and there is no specific metal stack requirement enabling a CMOS compatible process. Ohmic recess, which is to selectively remove the AlGaN and part of GaN in the ohmic region, shows high tolerance for recess depth and simplifies the etching process during fabrication.

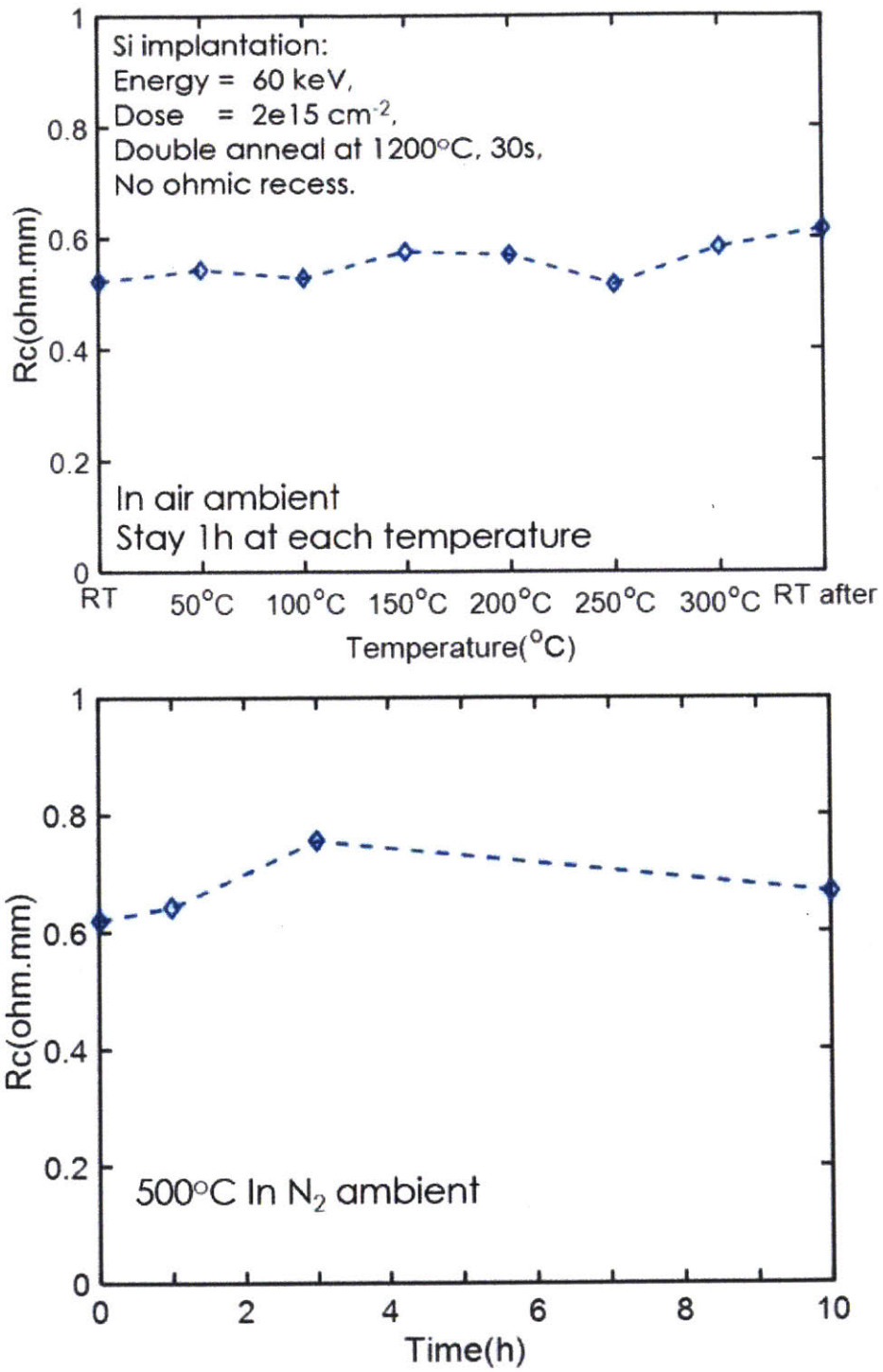



Figure 2-19: (top) In-situ contact resistance measured in air ambient versus temperature. (bottom) ex-situ contact resistance measured in $N_2$ ambient versus time stayed at 500°C.

# Chapter 3

# Self-Aligned Gate-First Gate Injection Transistors (GITs) with Etch-Stop Process

## 3.1 Introduction

Thanks to the rapid development of GaN-on-Si growth technology, GaN becomes more and more attractive in the market because of the availability of larger wafers and lower cost compared with SiC, which is more expensive and lack of large wafers (8-inch and beyond). AlGaN/GaN HEMTs, due to the polar nature of wurtzite (Al)GaN, have built-in two-dimensional electron gas in the interface without intentional doping during lattice growth, which shows a high critical electric field, a high carrier density, and a high electron mobility. While the high-quality 2DEG makes AlGaN/GaN HEMTs a perfect candidate for high voltage, high frequency, and high-temperature applications, it also makes AlGaN/GaN HEMTs a naturally depletion-mode (D-mode, or normally-on) devices.

Several approaches have been proposed to realize enhancement-mode (E-mode, or normally-off) operation including recess-gate metal-insulator-semiconductor HEMTs (MISHEMTs) [33], fluorine-implanted HEMTs [47] and gate injection transistors (GITs)

[34] as listed in Fig. 3-1.

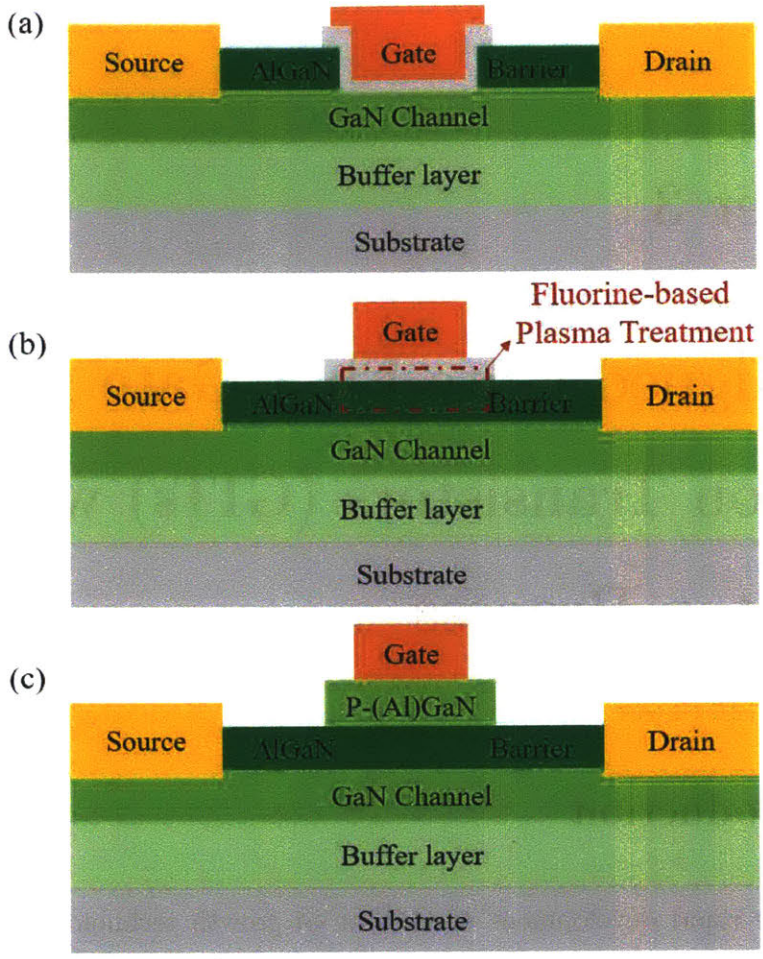



Figure 3-1: (a) Cross-section of MISHEMTs. Gate recess depths might vary from a partial removal of AlGaN to a full removal of AlGaN with partial removal of GaN underneath. (b) Cross-section of fluorine implanted HEMTs. Fluorine-based plasma treatment can also etch part of AlGaN depending on the etching process. Insulation layer is not required. (c) Cross section of GITs. The top layer could be p-doped AlGaN or GaN.

The key step of recess-gate MISHEMTs is to fully or partially recess the AlGaN barrier layer in the gated region by either wet etching or dry etching to eliminate 2DEG and thereby obtain normally-off behavior. However, it is challenging to reduce the interface defect density and obtain high-quality gate dielectrics due to etching damage. Besides, the threshold voltages of recess-gate MISHEMTs are sensitive to the AlGaN barrier thickness, and few nanometers variance over the wafers could result in

a significant difference in threshold voltages[48], which requires well-optimized wafer growth and etching technology. Moreover, the threshold voltages of MISHEMTs are usually limited by the conduction mechanism due to the lack of external p-type dopants in the channel.

The fluorine-implanted HEMTs use fluorine-based plasma treatment in the gate region to implant negatively charged fluorine ions and shift the threshold voltage positively. The AlGaN barrier could be partially removed, depending on the process. A post-gate annealing would then be conducted to recovering from plasma-induced damage. Similar to the MISHEMTs, the threshold voltages of fluorine-implanted HEMTS are also limited to a relatively low value even with AlGaN partially removed. The thermal stability of this implanted scheme is another concern.

Compared with recess-gate MISHEMTs, GITs have several advantages, such as no hysteresis after applying forward bias, lower on-resistance at gate region, higher threshold voltage uniformity. The additional p-GaN layer in the gated region lifts the potential in the AlGaN/GaN interface and deplete 2DEG by injecting holes like junction field-effect transistor (JFET) to achieve normally-off operation as illustrated in Fig. 3-2. The key step is to remove the p-GaN layer without damaging the AlGaN barrier selectively. It has also been reported use of hydrogen-based plasma to passivate implanted Mg ions instead of etching [49]. Besides, threshold voltage and gate leakage current could be engineered by gate metal with different work function except for change p-GaN doping and thickness. For high-temperature applications, gate metal needs to be carefully chosen to obtain better thermal stability and suppress the gate leakage current.

Considering the high uniformity and higher threshold voltage, GITs will be studied and optimized in this work for high-temperature operation.

## 3.2 Simulation of GITs Epitaxial Structure

Before device fabrication, it is important to carefully engineer the thickness and doping of p-GaN, the thickness, and the Al composition of AlGaN. The former determines

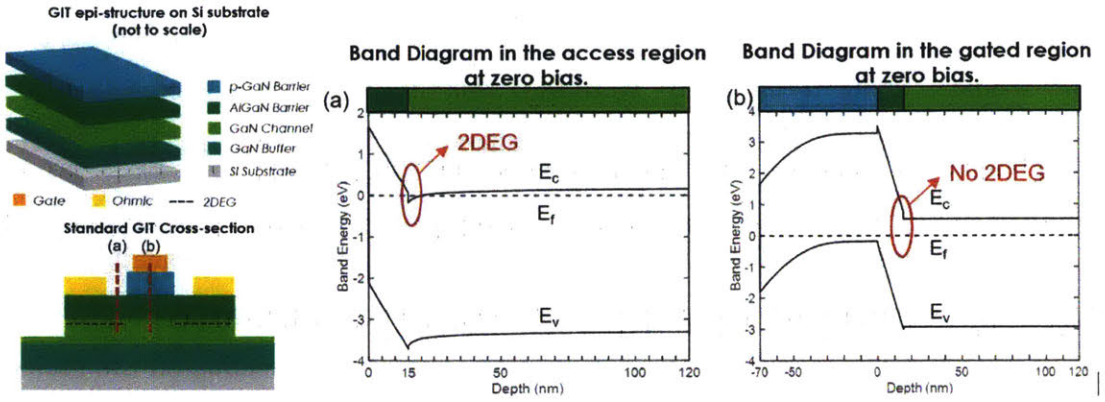



Figure 3-2: Schematic of GITs wafer structure and cross section of GITs; Band diagram at (a) access and (b) gated region.

the hole injection level, and the latter determines the polarization-induced electron density of 2DEG. Both of them play significant roles in the threshold voltage of the final devices. TCAD simulations were performed at both room temperature (300 K) and 600 K with different combinations, as shown in Fig. 3-3 and Fig. 3-4. The activated p-type doping in this simulation was set as a uniform distribution with a concentration of $8 \times 10^{17}\ cm^{-3}$, corresponding to an activation ratio of 1.6% with a real doping concentration of $5 \times 10^{19}\ cm^{-3}$.

As can be seen here, the 2DEG density under the gated region will slightly increase when the temperature increase. Both AlGaN and p-GaN show significant impacts on 2DEG density. Finally, 70 nm p-GaN and 15 nm $Al_{0.2}Ga_{0.8}N$ was chosen here in order to achieve e-mode operation in a wide temperature range without sacrificing current density.

## 3.3 Optimization of GIT's Process

### 3.3.1 Etch-Stop Process of p-GaN

As described in section 3.1, the key step of GITs fabrication is to selectively remove p-(Al)GaN without damaging the AlGaN barrier in order to maintain the high-quality 2DEG in the access region. Several methods have been proposed to etch away or

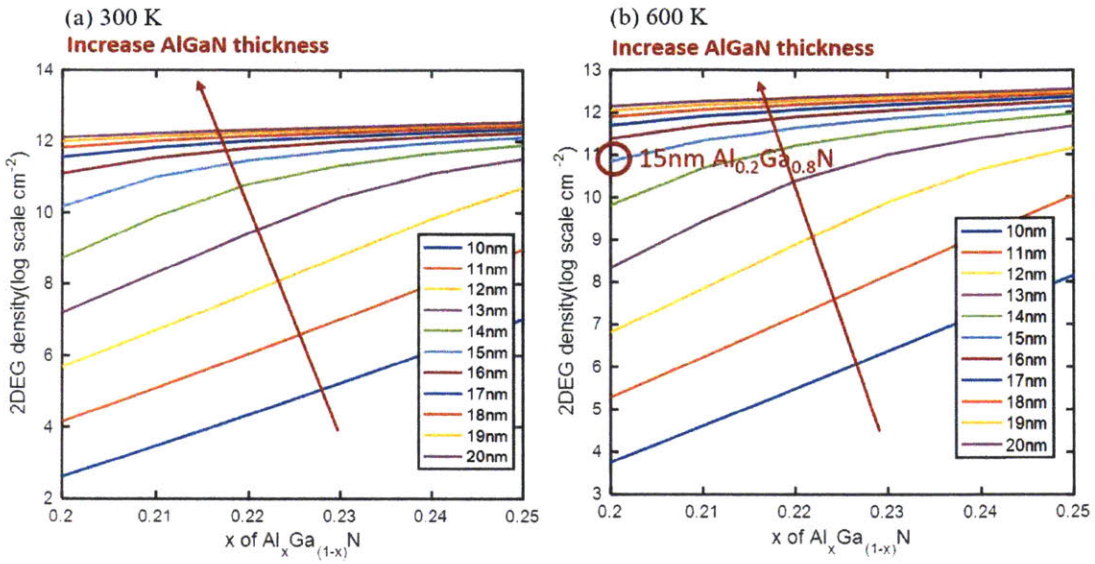



Figure 3-3: (a) 2DEG density with different AlGaN thickness and mole fraction under 300 K with 110 nm p-GaN cap; (b) 2DEG density with different AlGaN thickness and mole fraction under 600 K with 110 nm p-GaN cap.

passivate p-(Al)GaN layers. They can be categorized as: wet etching [50, 51], dry etching including time-controlled etching, selective etching (as known as etch-stop) [52], digital etching (or atomic layer etching) [53], and plasma treatment [49]. Despite selective removal of p-GaN, selective growth of p-doped (Al)GaN is also an option [54, 55], which requires growth capability and might suffer from surface traps.

The wet etching shows self-termination performance [51]. However, wet etching is less appealing for large volume fabrication.

The time-controlled etching is the easiest way to remove the p-(Al)GaN, while the performance of the time-controlled etching strongly relies on the tool performance. Careful calibration is required because device performance is sensitive to the etching depth.

The digital etching offers higher control than the time-controlled etching, which uses separate $BCl_3$ and $O_2$ plasma to remove GaN sequentially. The etch rate could be as low as a few nanometers per cycle. However, similar to the time-controlled etching, those two etching techniques might suffer from the inherent variations of p-GaN thickness across the wafer due to the limitations of growth technology, causing

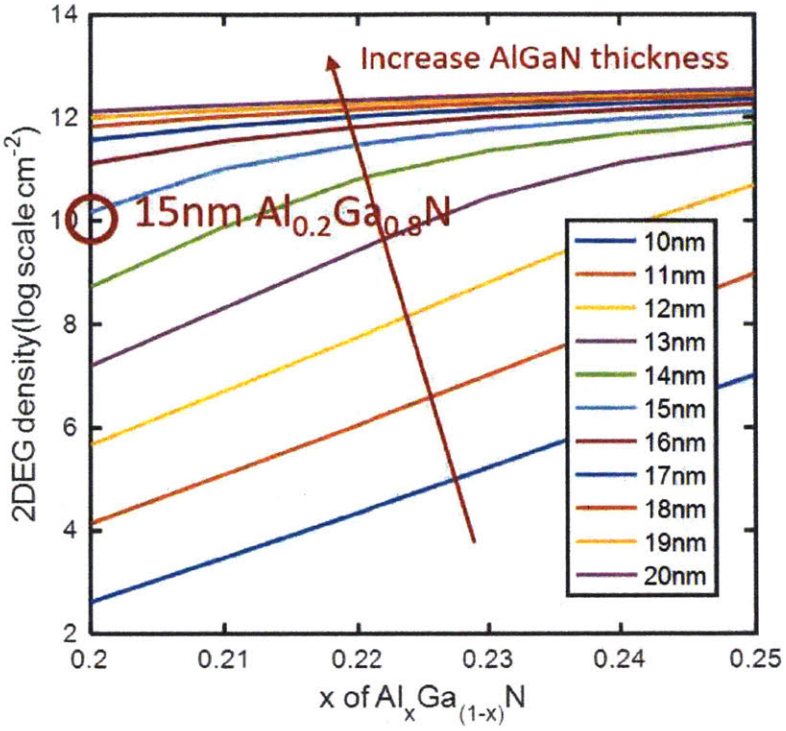



Figure 3-4: 2DEG density with different AlGaN thickness and mole fraction under 600 K with 70 nm p-GaN cap.

unwanted over/under etching even with perfect etch rates.

Another dry etching method is to use either fluorine or oxygen-based gas, which will react with Al and form an etch rate reduction layer such as $Al_xF_y$ or $Al_2O_3$, mixed with $BCl_3$ to obtain the etch-stop performance as explained in Fig. 3-5. The etch-stop technique allows a much higher tolerance for wafer structure and tool performance.

Hydrogen plasma treatment aims to passivate the unwanted p-GaN region with a self-aligned process, and depth could be precisely controlled by implantation energy. However, thermal stability is a huge concern for this scheme. Heavy-ion implantation, which has been widely used in mesa isolation, might be a better option.

After comparison among those etching techniques, the etch-stop process is considered to be the most suitable option for large scale fabrication and would be mainly studied here. An etch-stop process has been developed on an ECR-RIE tool.

The parameters for the etch-stop process in ECR-RIE are listed in Tab. 3.1. The

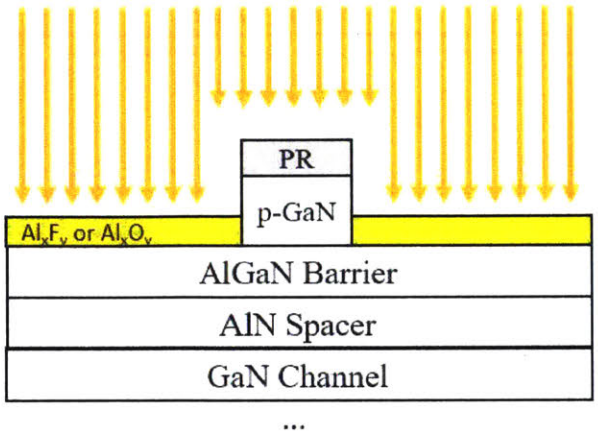



Figure 3-5: Schematic of the etch-stop technique.

first three steps are fixed steps in order to remove part of p-GaN before the etch-stop and stabilize the gas flow. Step 4 to 6 aim to perform the etch-stop process. $BCl_3/SF_6$ was used in the test. The epitaxial structure of tested samples from top to bottom is as follows: $\sim$ 770 nm p-GaN, 15 nm $Al_{0.2}Ga_{0.8}N$, GaN channel, GaN buffer, and Si (111) substrate. The results of the etch- are shown in Fig. 3-6, where the x-axis is the time in step 6. The etch depth was measured by atomic force microscope (AFM). An excellent etch-stop performance can be observed, and a minimum selectivity of 14 is achieved here due to AlGaN is not fully etched away.

Table 3.1: Parameters for the etch-stop process.

| **Step** | $BCl_3$ [sccm] | $SF_6$ [sccm] | **Base Pressure** [mTorr] | **ECR Power** [Watts] | **RF Bias** [V] | **Time** [s] |
|---|---|---|---|---|---|---|
| 1 | 15 | 0 | 10 | 0 | 0 | 30 |
| 2 | 15 | 0 | 10 | 50 | 15 | 5 |
| 3 | 15 | 0 | 10 | 100 | 15 | 200 |
| 4 | 12 | 26 | 35 | 0 | 0 | 30 |
| 5 | 15 | 26 | 35 | 50 | 30 | 5 |
| 6 | 15 | 26 | 35 | 110 | 100 | $x$ |

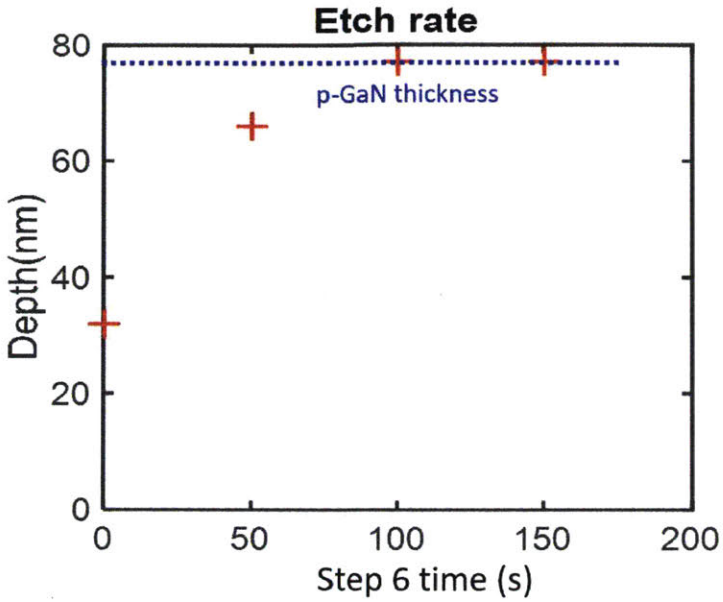



Figure 3-6: Etching depth versus time in step 6.

### 3.3.2 Self-Aligned Gate Metallizations

Gate metal plays an important role in determining the threshold voltage by forming either a Schottky or ohmic contact on p-(Al)GaN. Several gate metal such as TiN, Ti/Al, Ti/Au, Ni/Au, Mo, W, Pd, WSiN have been studied in multiple works [34, 25, 56, 57]. Here a preliminary experiment was conducted to compare the effects of gate metals. Notice that the Schottky barrier height ($\Phi_B$) is

$$\Phi_B = E_g - (\Phi_m - \chi_s) \tag{3.1}$$

where $\Phi_m$ is the work function of the metal, $E_g$ is bandgap, and $\chi_s$ is the electron affinity of the semiconductor.

A similar wafer structure, as described in section 3.3.1, was used in this work. The process of the samples with Ti/Al gate or Ni/Au gate will be illustrated here, while the self-aligned process of samples with tungsten (W) gate will be described in the next section.

The fabrication started from the selective removal of p-GaN by $SF_6/BCl_3$-based

ECR-RIE to define the gate region. A short oxygen plasma treatment was then conducted following with a 1 min TMAH dip to remove the fluorine contamination. A standard Ti/Al/Ni/Au metal stack was then e-beam evaporated and lifted off. After the post-annealing at 800°C for 30 s, mesa isolation was then performed. Ti/Al (20/100 nm) gate and Ni/Au (30/80 nm) gate were e-beam evaporated and lifted off separately on different samples.

The measurement results are shown in Fig. 3-7. As can be seen here, the device with Ti/Al gate, which has lower work function (~4.3 eV/4.06-4.26 eV) than Ni/Au gate (5.04-5.35 eV/5.1-5.47 eV), has the highest threshold voltage of $\sim$ 3.5 V compared to $\sim$ 1.7 V of the device with Ni/Au gate. The subthreshold swings (SS) of devices with Ti/Al and Ni/Au gates are 250 mV/dec and 160 mV/dec, respectively. The low threshold voltage of GITs with tungsten gate is possibly caused by the post-annealing effect, where gate metal was first deposited and then annealed together with the ohmic contact. However, due to the possible gate sidewall contact as a consequence of misalignment, the gate leakage current of device with either Ti/Al or Ni/Au gate is relatively large at high $V_{DS}$. Another drawback of those contact metal schemes is the weak thermal stability. Ni/Au is known to form an ohmic contact with p-GaN after annealed in $O_2$ at 450°C or higher [58], while Al has a melting point as low as 660°C. Therefore, gate metallization has to be done after the annealing of ohmic contact in this case, which makes the self-aligned process impossible.

To enable high-temperature operation and realize the self-aligned process, it is appealing to use a refractory metal as a gate metal and also a hard mask for selective removal of p-GaN. Here, tungsten will be studied and used as a gate metal for GITs.

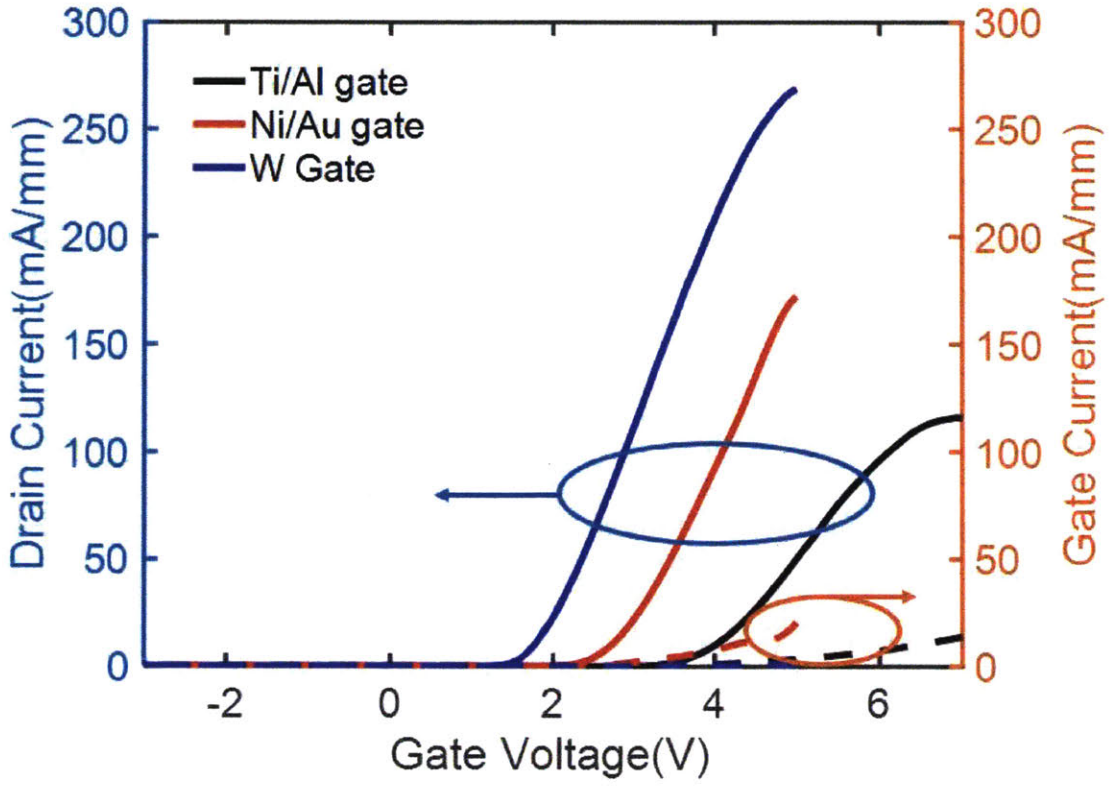



Figure 3-7: Transfer characteristics of GITs with Ti/Al, Ni/Au and W gate.

## 3.4 Fabrication of GITs

### 3.4.1 Device Structure

The epitaxial structure used in this work was grown by Enkris Semiconductor, INC., on a 6 inch Si (111) substrate using MOCVD. The stack has already been described in section 3.3.1.

The fabrication started with the sputtering of 100 nm tungsten as a gate metal with a resistivity of $\sim 0.16\ \mu\Omega \cdot m$. A subsequent photo-lithography defined the gate region. The photoresist served as a soft mask for both etching of gate metal and selective removal of p-GaN underneath, allowing for a self-aligned process. Tungsten was then dry-etched by $SF_6/O_2$-based RIE, following with the etch-stop process described in section 3.3.1. A short oxygen plasma treatment was then conducted following with

a 1 min TMAH dip to remove the fluorine contamination. A standard Ti/Al/Ni/Au contact was then e-beam evaporated and lifted off. $\sim$ 140 nm mesa isolation was performed afterward by $BCl_3/Cl_2$-based ECR-RIE.

### 3.4.2 Results and Discussion

The output characteristics and transfer characteristics at room temperature are shown in Fig. 3-8. A threshold voltage of $\sim$ 1.34 V is extracted by linear extrapolation. A saturation current over 300 $mA/mm$ at $V_{GS} = 5\ V$ and $V_{DS} = 3\ V$, while $I_g$ is $\sim 0.8\ mA/mm$. The transconductance ($g_m$) at $V_{DS} = 0.5\ V$ is $\sim 67\ mS/mm$, and a maximum value of 104 $mS/mm$ is achieved at $V_{DS} = 5$ V. A nearly ideal subthreshold swing (SS) of $\sim 70\ mV/dec$ is extracted and a high ON/OFF ratio of $> 10^9$ is obtained at room temperature, indicating a great gate control with this self-aligned gate first process. The on resistance of $\sim 8\ \Omega \cdot mm$ is extracted at $V_{DS} = 0.5V$ where $I_D = 60$ mA/mm.

A high-temperature degradation test was then performed on the same sample. A high-temperature probe station built with a hot plate was used for in-situ measurement. The sample was characterized from room temperature up to 300 °C in air ambient. Both on-current and off-current decrease with temperature due to the decreasing mobility, while the on/off ratio is still over $10^6$ even at 300°C, as seen in Fig. 3-9, proving the potential of GITs with the self-aligned process for high-temperature operation.

The sample was first put in the furnace and then heated up to 500 °C in $N_2$. After stressed at 500°C in $N_2$ ambient for up to 24 hours, the sample was then taken out and characterized at room temperature. No obvious degradation of device performance is observed, as seen in Fig. 3-10, implying that a good thermal stability can be achieved with this process.

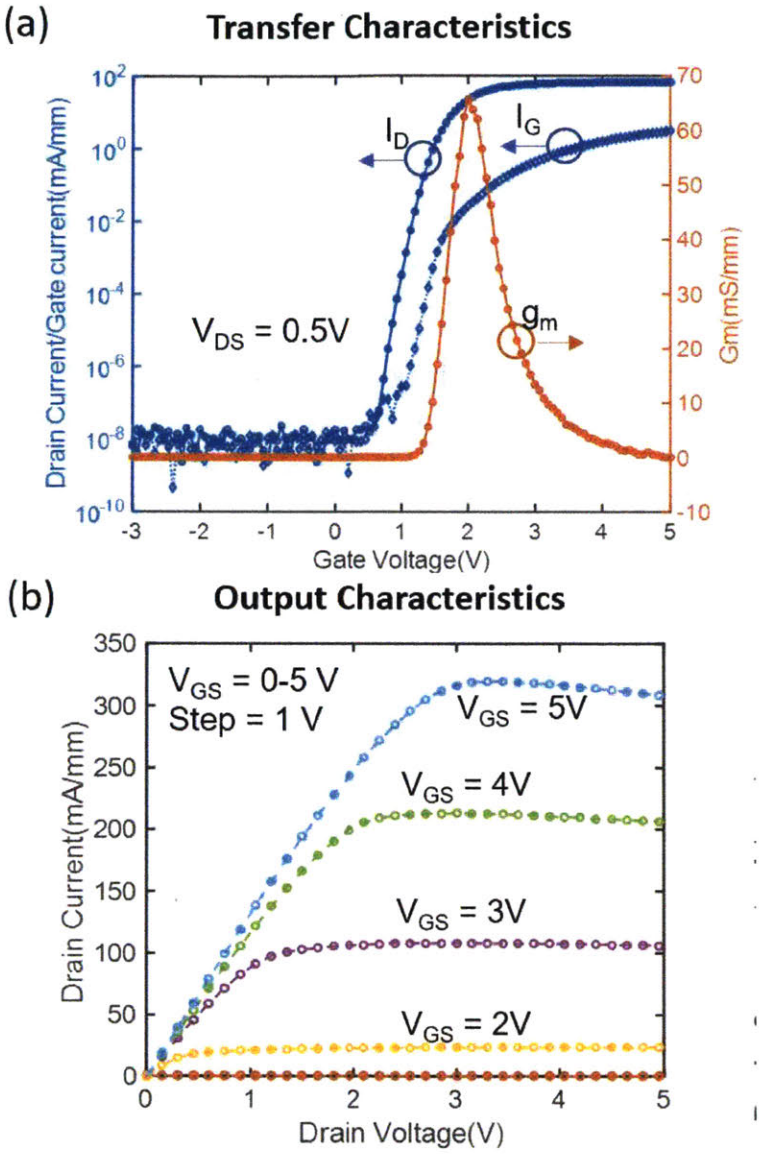



Figure 3-8: Transfer characteristics at $V_{DS} = 0.5V$ and output characteristics at $V_{GS}$ from 0 V - 5 V with step = 1 V at room temperature. $L_G = L_{GD} = L_{GS} = 2\ \mu m$.

## 3.5 Conclusion

In this chapter, several critical techniques for normally-off gate injection transistors have been studied and optimized, including selective removal of p-GaN and choosing a proper gate metallization scheme for the self-aligned process. The etch-stop process developed shows great stability and selectivity. GITs with different gate metals were

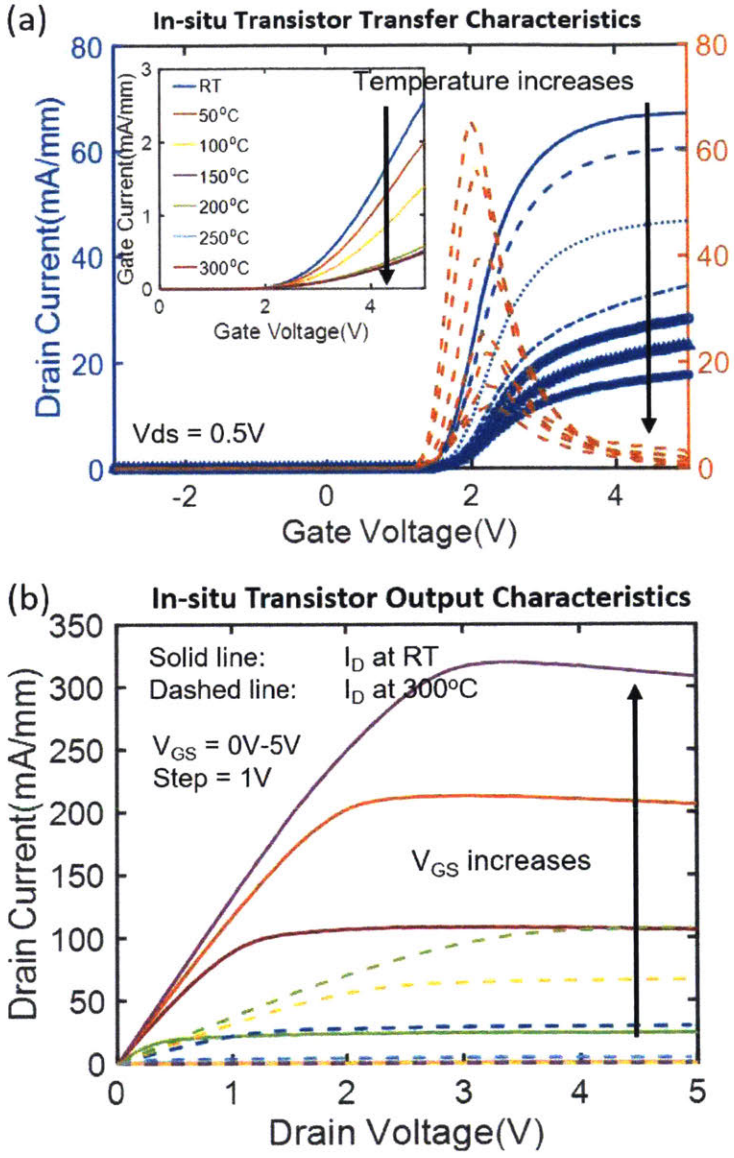



Figure 3-9: (a) Transfer characteristics at $V_{DS} = 0.5V$ and output characteristics at (b) $V_{GS}$ ranging from 0 V - 5 V with step = 1 V at room temperature to 300°C. $L_G = L_{GD} = L_{GS} = 2\ \mu m$.

also studied and compared. With the self-aligned gate-first process, a device with a low $R_on$ of $\sim 8\ \Omega \cdot mm$, an ideal SS of $\sim 70\ mV/dec$, high $V_{TH}$ of 1.34V and high ON/OFF ratio of $> 10^9$ was fabricated. Both in-situ and ex-situ measurements were performed on GITs, showing the good thermal stability of the fabricated GITs verified by in-situ measurement up to 300°C in air and ex-situ measurement up to 500°C for

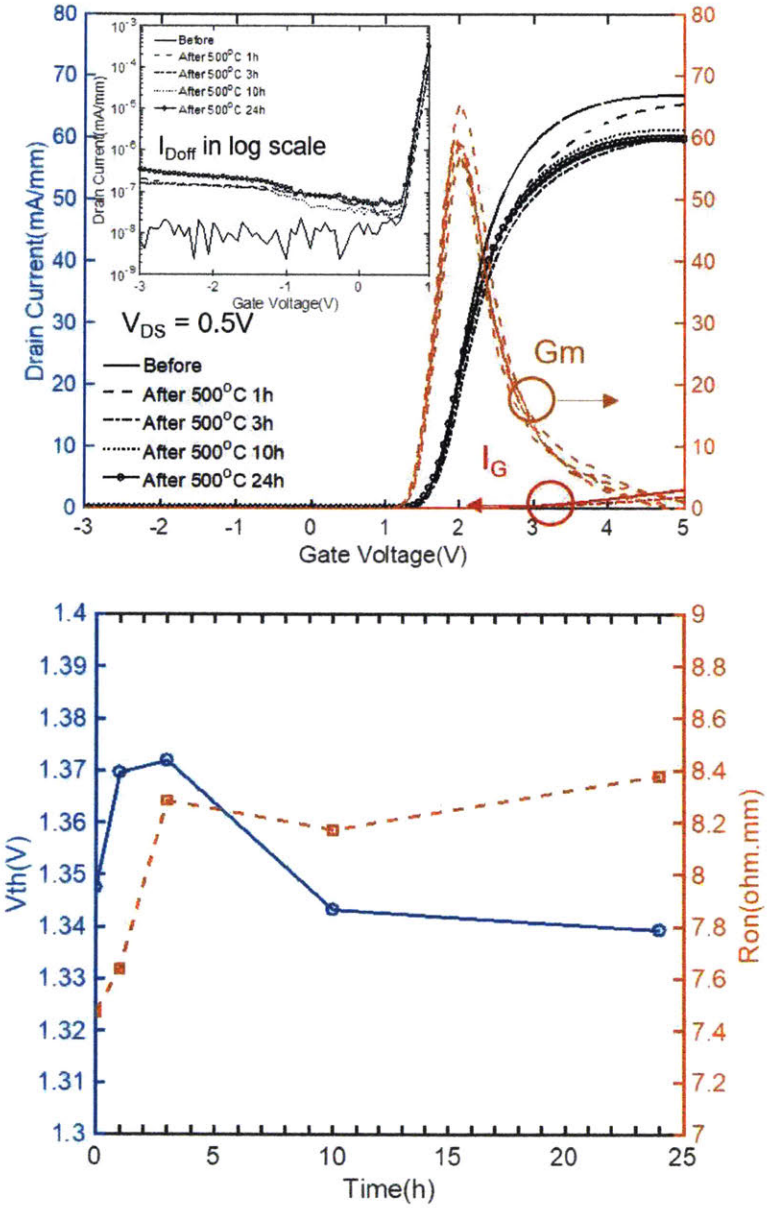



Figure 3-10: (a) Transfer characteristics at $V_{DS} = 0.5V$ and (b) output characteristics at $V_{GS}$ ranging from 0 V - 5 V with step = 1 V at room temperature to 300°C. $L_G = L_{GD} = L_{GS} = 2\ \mu m$.

24 hours in $N_2$.

# Chapter 4

# Logic Building Blocks Based on GaN Electronics for High-Temperature Operation

In chapter 3, a self-aligned gate first process of E-mode GITs was demonstrated with low on-resistance, high threshold voltage, and potential for high-temperature operation. A monolithic integration process of E/D-mode HEMTs will be demonstrated here together with a uniformity test for large scale circuit applications. To enable circuit design, MIT virtual source GaN (MVSG)compact model [35] was used here to fit experimental data and capture the electrical behaviors of GITs. With e-mode technology available, two different direct-coupled FET logic configurations, which monolithically integrate either E/D-mode HEMTs or E/E-mode HEMTs as shown in Fig. 4-1, would be tested to realize logic building blocks for high-temperature GaN microprocessors, including inverter, NAND/NOR gate, ring oscillator, SRAM at both room temperature and high temperature up to 300°C.

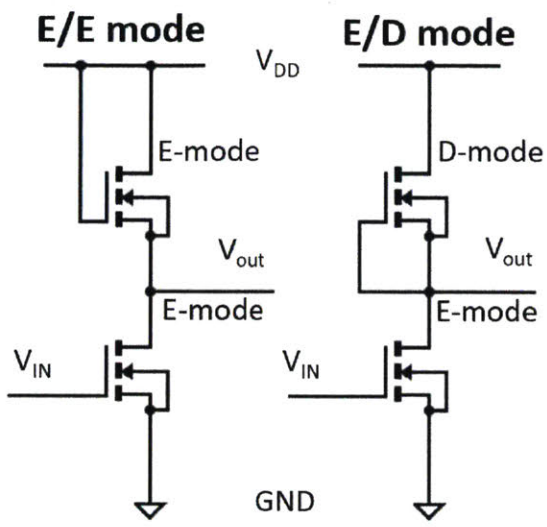



Figure 4-1: Circuit diagram of E/E-mode and E/D-mode inverter.

## 4.1 Monolithically Integration of E/D-mode HEMTs and Uniformity Test

### 4.1.1 Device Structure

The same wafer structure, as described in section 3.3.1, was used here. 100 nm W was first sputtered on the sample surface with a resistivity of $\sim 0.16\ \mu\Omega \cdot m$, following with the dry etching of tungsten by $SF_6/O_2$-based ECR-RIE and the selective removal of p-GaN by $SF_6/BCl_3$-based ECR-RIE. A short oxygen plasma treatment was then conducted following with a 1 min TMAH dip to remove the fluorine contamination. A standard Ti/Al/Ni/Au (20/100/25/50 nm) contact was then e-beam evaporated and lifted off. $\sim$ 140 nm mesa isolation was performed afterward by $BCl_3/Cl_2$-based ECR-RIE. After mesa isolation, Ni/Au gate metallization was performed by e-beam evaporation and lift-off, following with 200 nm PECVD $SiN_x$ passivation. Fig. 4-2 shows the cross-section of the integrated E/D-mode GaN HEMTs, and the design rule is shown in Fig. 4-3.

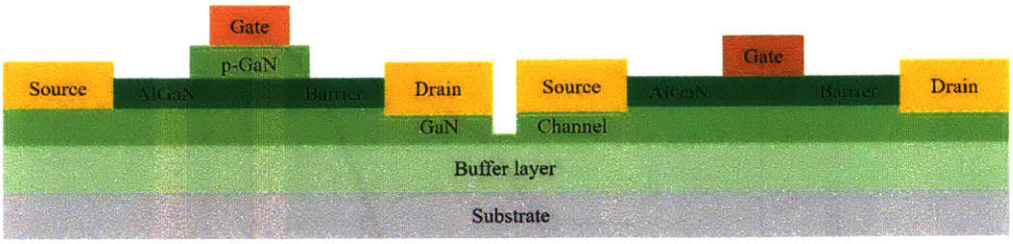



Figure 4-2: Cross section of monolithically integrated E/D mode GaN HETMs.

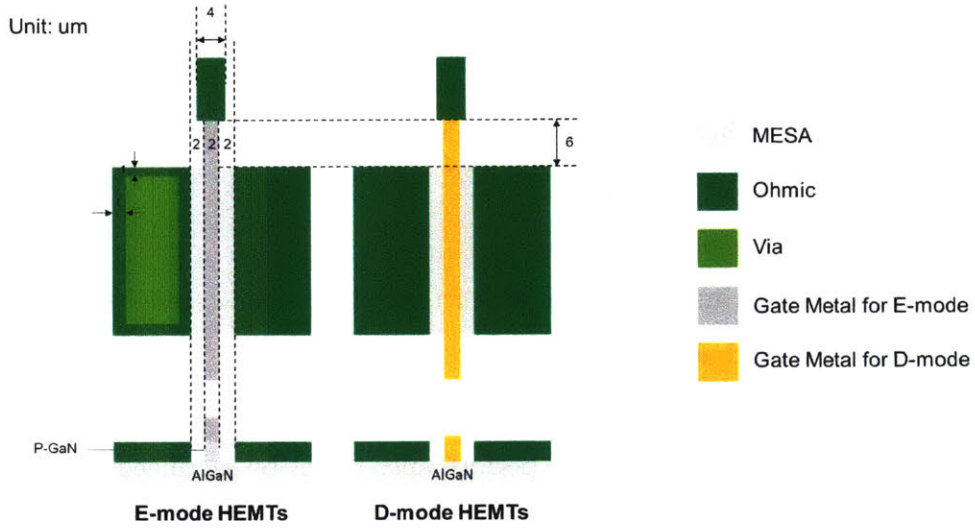



Figure 4-3: Design rule of integrated E/D mode GaN HEMTs.

### 4.1.2 Results of E/D-mode HEMTs

Fig. 4-4 shows the transfer characteristics of the fabricated E/D-mode device with $L_g = L_{gs} = L_{gs} = 2\ \mu m$ at $V_{DS} = 5$ V, which present threshold voltages of -1.3 V for D-mode HEMT and 1.48V for GIT. On-resistance of 6.5 $\Omega \cdot mm$ for GIT and 7.2 $\Omega \cdot mm$ for D-mode HEMT are extracted at $V_{DS} = 1$ V. It shows the possibility of monolithic integration of E/D-mode GaN HEMTs with the self-aligned process and etch-stop technology.

A lower saturation current density is observed in D-mode transistor compared with that of E-mode transistor, which is mainly caused by etching damage induced by the etch-stop process. Considering a DCFL configuration, the D-mode pull-up

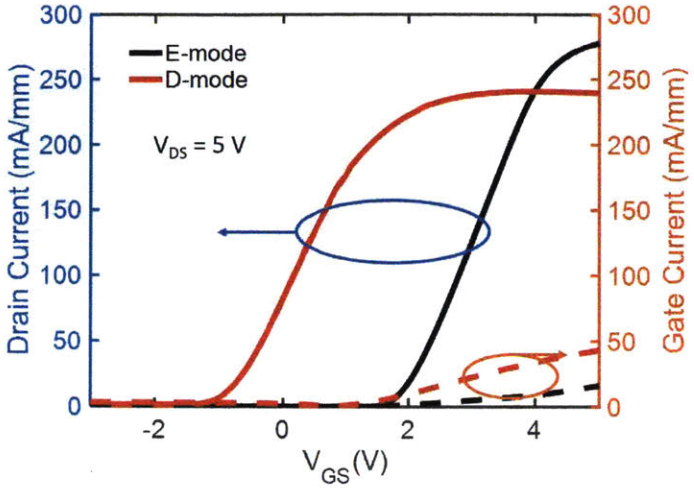



Figure 4-4: Transfer characteristics of monolithically integrated E/D mode GaN HETMs with $L_g = L_{gs} = L_{gs} = 2\ \mu m$ at $V_{DS} = 5$ V.

transistor usually has a much smaller width than the E-mode transistor to provide higher on-resistance and achieve a lower $V_{OL}$. A wider D-mode device could be used here to achieve similar voltage swing, due to the lower saturation current density, and help match the width, while transient performance might be sacrificed due to higher on-resistance.

### 4.1.3 Comparison of E/D-mode Inverter and E/E-mode Inverter

E/E-mode inverter and E/D-mode inverter with width ratio ($W_{pull-up}/W_{pull-down}$) of 12 $\mu m$/36 $\mu m$ based on DCFL configuration were also demonstrated in Fig. 4-5. Both inverter were biased at $V_{DD} = 5$ V with voltage transfer curve shown in Fig. 4-6. The threshold voltage, where $V_{IN} = V_{OUT}$ of E/D-mode inverter is $\sim 1.94$ V, while $V_{TH}$ of E/E mode inverter is $\sim 2.14$ V. Both of the $V_{TH}$ is close to $\frac{V_{DD}}{2} = 2.5$ V enabling a good transition and large noise margin.

Similar to resistor-transistor logic (RTL), a pull-up transistor is set as always-on to serve as a pull-up resistor with matched characteristics in DCFL configuration. Comparing to E/D-mode configuration, E/E-mode inverters short gate and drain

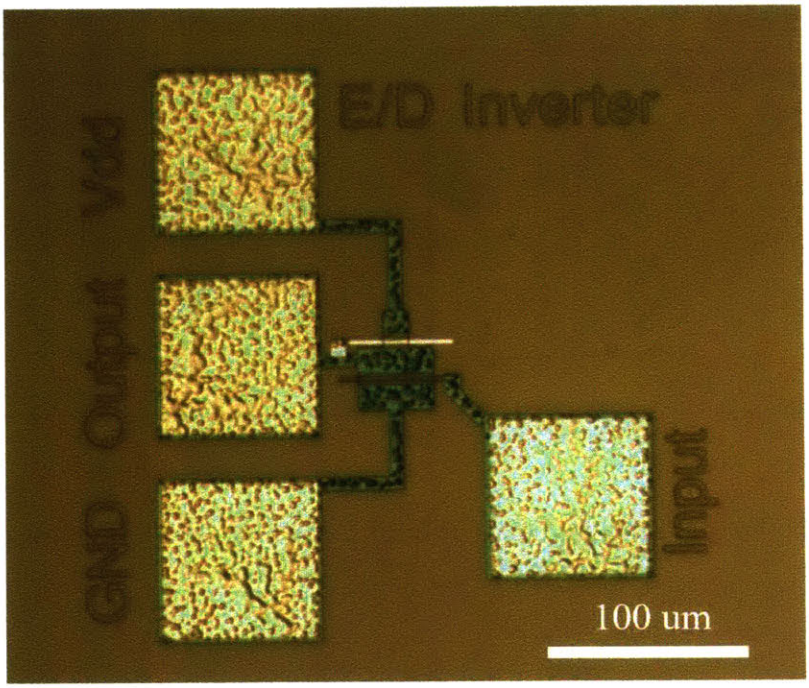



Figure 4-5: Top view of E/D-mode inverter in optical microscope.

together ($V_{GS} = V_{DS}$) to achieve always-on operation. However, when $V_{DS} < V_{TH}$, the pull-up transistor will gradually turn off, which means the highest voltage of E/E-mode transistor can not increase above $\sim (V_{DD} - V_{TH})$ comparing to E/D-mode inverters. As we can observe here, E/E-mode inverter can hardly go over 4.1 V, which is slightly higher than the predicted value due to the subthreshold conduction, while E/D-mode shows much better voltage swing with $V_{OH} = 5$ V and $V_{OL} = 0.4$ V.

Meanwhile, gain ($A_v = \left|\frac{dV_{out}}{dV_{in}}\right|_{V_{in}=V_{out}}$) of E/E mode inverter mostly depends on the square root of width ratio ($\sim 1.73$ in this case) with the assumption that two transistors have similar parameters except for the width when both transistors work

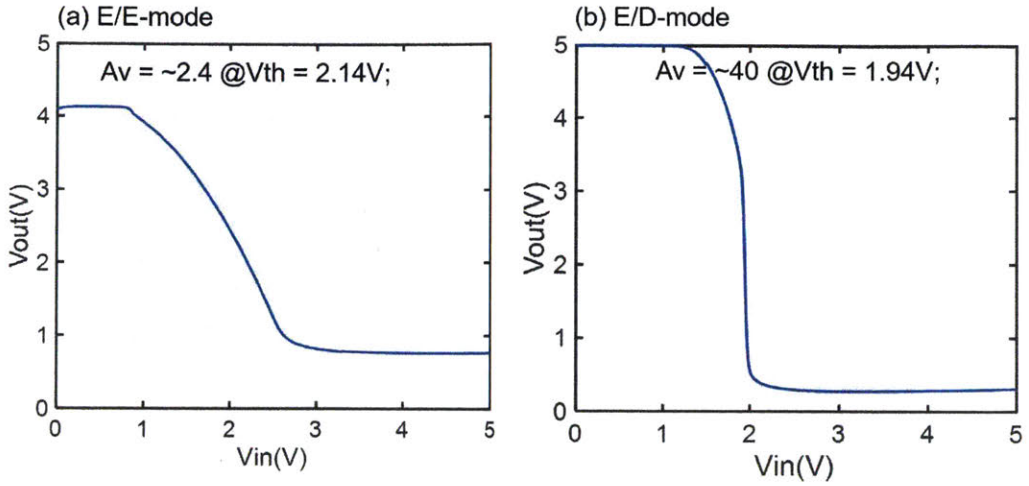



Figure 4-6: Voltage transfer curve of both E/E-mode and E/D-mode inverters.

in the saturation region,

$$I_{D\_down,sat} = I_{D\_up,sat} \tag{4.1}$$

$$I_{D\_down,sat} = \frac{1}{2}\mu C\frac{W_{down}}{L}(V_{in} - V_T)^2 \tag{4.2}$$

$$I_{D\_up,sat} = \frac{1}{2}\mu C\frac{W_{up}}{L}(V_{DD} - V_{out} - V_T)^2 \tag{4.3}$$

$$\left.\frac{dV_{out}}{dV_{in}}\right|_{V_{in}=V_{out}} \approx -\sqrt{\frac{W_{down}}{W_{up}}} \tag{4.4}$$

where the simplest quadratic saturation current model is used here, $C$ is the normalized gate capacitance, $\mu$ is the channel mobility.

The gain of E/D-mode inverter is much higher in theory if we ignore the self-heating effects and assume a constant current can be achieved in the saturation region. The output characteristics of E-mode GIT and the load line of D-mode HEMT are shown in Fig. 4-7. A gain of 2.4 $\frac{V}{V}$ for E/E-mode inverter and a gain of $\sim$ 40 $\frac{V}{V}$ for E/D-mode inverter are extracted from Fig. 4-6, which is mainly determined by secondary effects. The static noise margin of E/D-mode inverters are extracted by definition of $\frac{dV_{out}}{dV_{in}} = -1$ with logic-low noise margin $(NM_L) = 0.96$ V and logic-high noise margin $(NM_H) = 2.6$ V.

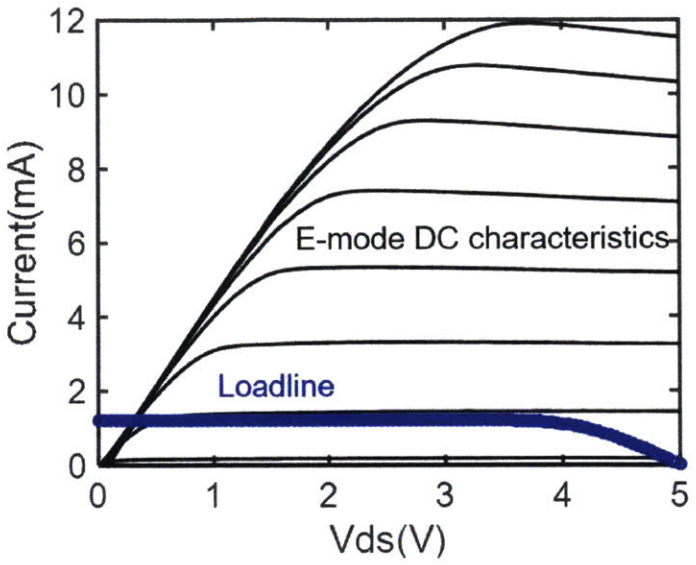



Figure 4-7: Measured output characteristics and load line of E/D-mode inverter with $W_E = 36\ \mu m$ and $W_D = 12\ \mu m$.

### 4.1.4 Uniformity Test

Due to the higher noise margin, voltage swing and gain, E/D-mode DCFL configuration is chosen for the following logic building blocks. The uniformity tests of E-mode devices and E/D-mode inverters were then performed on a different sample. As seen in Fig. 4-8, the distribution of threshold voltage of GITs is limited within 0.2 V and Fig. 4-8 (a) proves the potential of E/D mode inverters for large scale integration.

### 4.1.5 High Temperature Degradation Test

A preliminary high-temperature measurement was conducted following the same process as described in section 3.4.2. The results were shown in Fig. 4-9. Several observations could be made here. First, $I_{DD}$ slightly decreases at higher $V_{IN}$ due to the self-heating effect of the pull-up D-mode transistor. Second, Fig. 4-9 (b) indicates that the threshold voltage has great thermal stability, and is independent of operating temperature. Third, a higher voltage swing is observed in Fig. 4-9 (a), which could be attributed to the decrease of $V_{OL}$ at higher temperature. When $V_{IN}$ increase, the

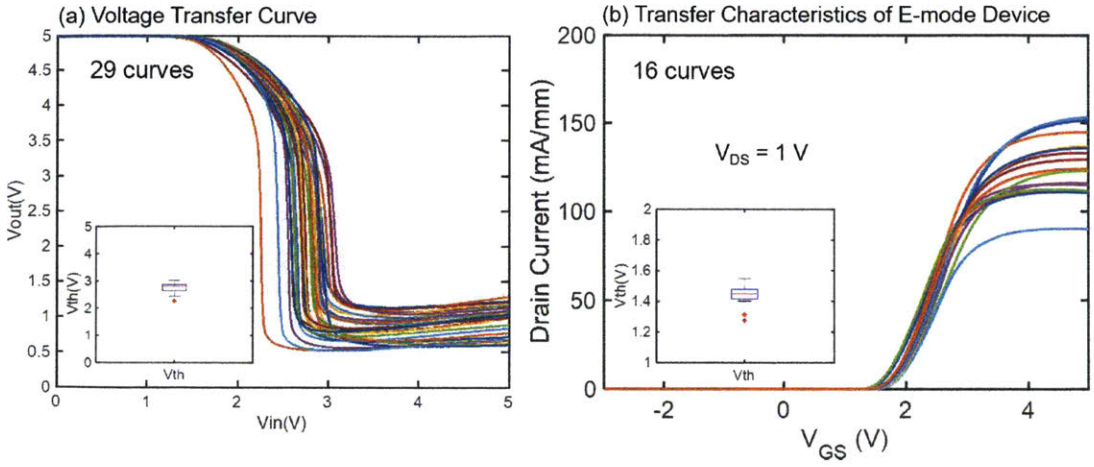



Figure 4-8: (a) Different voltage transfer curves on one piece at room temperature; (b) Different transfer characteristics on one piece at room temperature.

pull-down transistor will turn on, which will work in the linear region and form a voltage divider with the pull-up D-mode transistor in the saturation region. $V_{OL}$ can be approximated as

$$V_{OL} = I_{D,SAT} \cdot R_{E,on} \tag{4.5}$$

where $I_{D,SAT}$ is the saturation current of D-mode device at $V_{GS} = 0$ V, $R_{E,on}$ is the on-resistance of E-mode device working in the linear region. $I_{D,SAT}$ mainly depends on self-heating and mobility, which will keep decreasing at elevated temperature. $R_{E,on}$ depends mostly on mobility, which determines sheet resistance, and not affected by self-heating due to low power dissipation in the linear region. As can be observed in Fig. 4-9 (c)-(d), inverter resistance, which is inversely proportional to the $I_{D,SAT}$ increases faster than $R_{E,on}$ leading to a lower $V_{OL}$ and a higher voltage swing (~4.5 V at $V_{DD} = 5$ V) at high temperature.

Besides, high-temperature transient measurements of the E/D-mode inverter were performed by AFG3102 dual-channel function generator from Tektronix and DSO6054A oscilloscope from Agilent Technologies. As seen in Fig. 4-10, the input signal is a 10 kHz square wave with a duty cycle of 50%, and a $V_{DD}$ of 5 V. There is negligible difference between the rise/fall time of input and output signals, implying a minimal

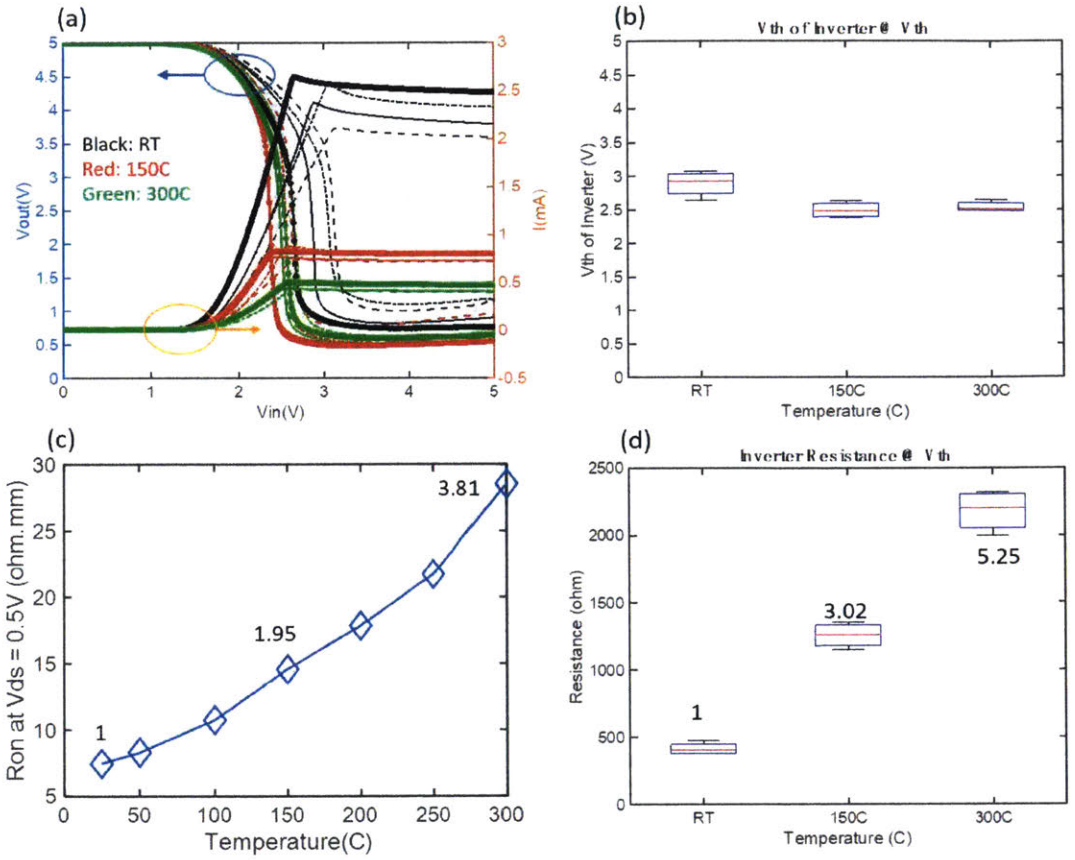



Figure 4-9: (a) 4 voltage transfer curves of E/D-mode inverters from room temperature to 300°C with $I_{DD}$ plotted on the right side; (b) $V_{TH}$ of VTCs in (a) from room temperature to 300°C; (c) On-resistance of E-mode transistor from RT to 300°C; (d) Inverter resistance ($\frac{V_{DD}}{I_{DD,max}}$) from room temperature to 300°C.

propagation delay of the E/D-mode inverter. The output voltage at each temperature point shows similar voltage swing as measured in DC measurement. A high voltage swing of 4.5 V ($V_{DD}$ = 5 V) is observed at 300°C showing the potential of this monolithic integration process for high-temperature applications.

## 4.2 Compact Modeling of E/D-mode HEMTs

MVSG model is a charge-based physical model that can be used for GaN-based devices [35]. First, the IC-CAP simulator would be used to extract and optimize parameters from IV and CV measurements. A Verilog-A model will then be generated based on

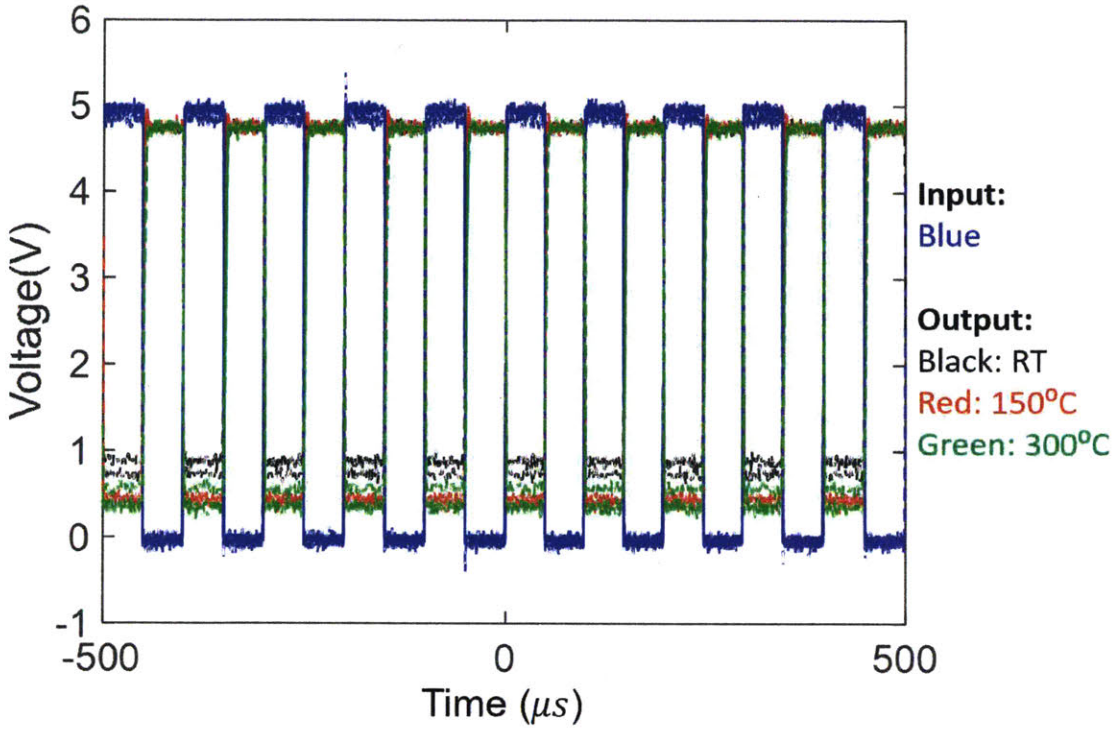



Figure 4-10: Transient characteristics of the E/D mode inverter with a 10 kHz square wave input.

those parameters to fit experimental data. The entire optimization procedure might need several iterations from optimizing parameters to fitting the experimental data.

Based on the results measured and shown in previous sections, compact modeling of both E/D-mode GaN HEMTs at room temperature was then conducted. An excellent fit was achieved, as shown in Fig. 4-11. Fig. 4-11(a) shows a comparison of output characteristics of GITs and load line of D-mode HEMTs between experimental data and simulation results based on the fitted compact model. Fig. 4-11 (b)-(c) shows the simulated and experimental results of the transfer characteristics in linear scale and log scale, respectively. There is an excellent agreement between simulated and experimental data at both linear region and saturation region. The simulated subthreshold swing and threshold voltage also precisely match the data measured. This Verilog-A model is very useful in enabling future circuit design.

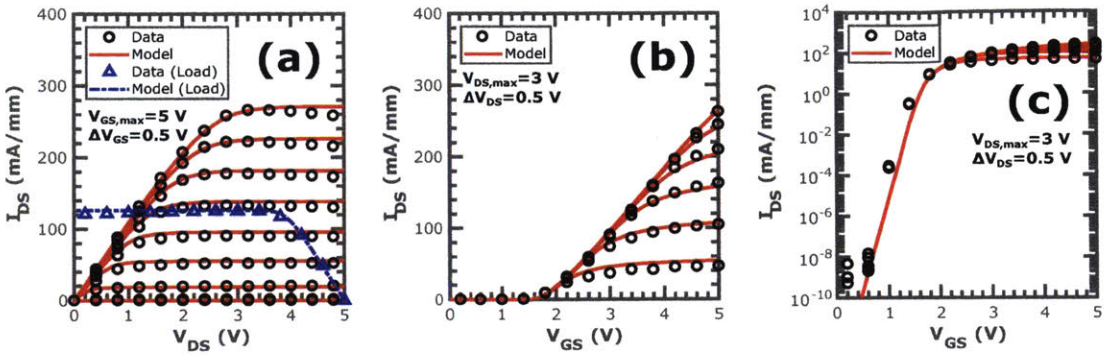



Figure 4-11: (a) Output characteristics of the E-mode transistor and load lines of the D-mode transistor based on both simulation and experimental results; (b) Simulated and measured transfer characteristics of the E-mode transistor in linear scale; (c) Simulated and measured transfer characteristics of the E-mode transistor in log scale.

## 4.3 Logic Building Blocks for High-Temperature Operation

### 4.3.1 Epitaxial Structure and Fabrication

Based on the results in section 4.1.3, E/D-mode DCFL configuration will be adopted in other logic building blocks, including NAND/NOR gates, ring oscillator, and SRAM. Most of the process flow has already been described in section 4.1.1. After 200 nm PECVD $SiN_x$ passivation, via structures were patterned and dry-etched by $CF_4$ plasma, following with e-beam evaporation and lift-off of Ti/Au metal interconnects. The top view of the fabricated logic building blocks was shown in Fig. 4-12.

### 4.3.2 NAND/NOR Gates

The circuit schematics of NAND and NOR gate are shown in Fig. 4-13. The widths of D/E-mode transistors are 12 $\mu m$/36 $\mu m$ with $L_g = L_{gd} = L_{gs} = 2\ \mu m$. The measurement was performed by an AFG3102 dual-channel function generator from Tektronix and an oscilloscope from Agilent Technologies with the help of a B1505 device analyzer from Keysight Technologies.

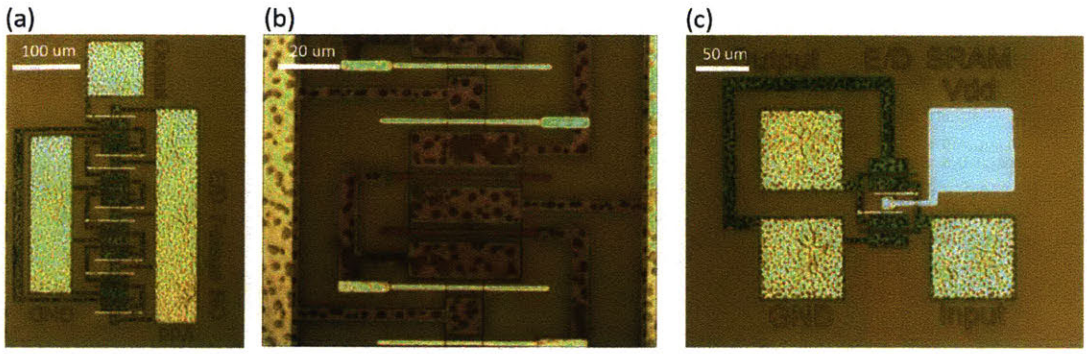



Figure 4-12: (a) Top view of a E/D-mode 7-stage ring oscillator in optical microscope; (b) Zoomed-in top view of the same ring oscillator in (a); (c) Top view of SRAM in optical microscope.

As seen in Fig. 4-14, the input signals are 1 kHz and 2 kHz square waves with $V_H$ = 5 V, $V_L$ = 0 V and a duty cycle of 50%. Both NAND/NOR gates are biased $V_{DD}$ = 5 V. The output voltage of the NAND gate is close to 5 V ($V_{DD}$, logic state 1) when either of input voltages is 0 V (logic state 0) as illustrated in table 4.1. When either of pull-down transistors is not conducting, the pull up transistor will pull the voltage up to $V_{DD}$ due to the series connection of two pull-down transistors. A logic state 0 of ~0.5 V is only achieved when both inputs are at logic state 1. Two pull-down transistors and the pull-up transistor work together as a voltage divider, and the logic state 0 could then be engineered by the width ratio of E/D-mode transistors. Similarly, a logic state 1 of the NOR gate can only be achieved when both inputs are at logic 0. A logic state 0 of ~ 0.5 V can be obtained in the rest situations. Both gates show voltage swings around 4.5 V when $V_{DD}$ = 5 V.

Both NAND/NOR gates were then tested at 150°C in air. As can be seen in Fig. 4-16 and Fig. 4-17, the output voltages of both gates almost remain unchanged. Similar voltage swings of ~4.5 V can be achieved in both cases. The difference in the rise/fall time is caused by the lower sampling rate. The noise of the input signal comes from the interference induced by adapters for signal splitting.

Considering NAND and NOR gates are the basic logic units and can be constructed to any other logic gate (AND, OR, XOR, etc.), the successful demonstration of NAND/NOR gates at both room temperature and high temperature shows the

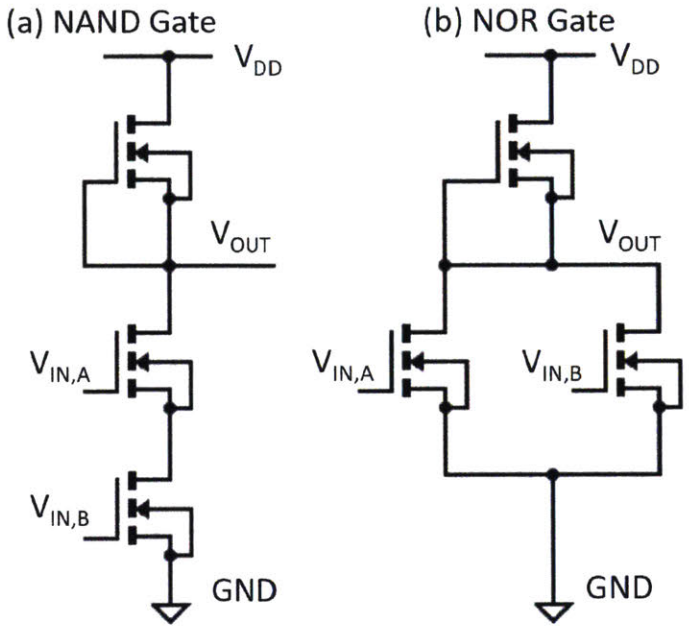



Figure 4-13: (a) Circuit diagram of NAND gate; (b) Circuit diagram of NOR gate.

Table 4.1: Table of inputs and outputs of NAND/NOR.

| A | B | $\overline{A+B}$[1] | $\overline{A \cdot B}$[2] |
|---|---|---|---|
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 |

[1] NOR.
[2] NAND.

possibility of more complicated digital circuits with the self-aligned gate-first process for high-temperature operation.

### 4.3.3 SRAM

Static random-access memory (SRAM) is a kind of random-access memory using flip-flop to store bit information (logic state 1 or 0). A typical SRAM structure has six

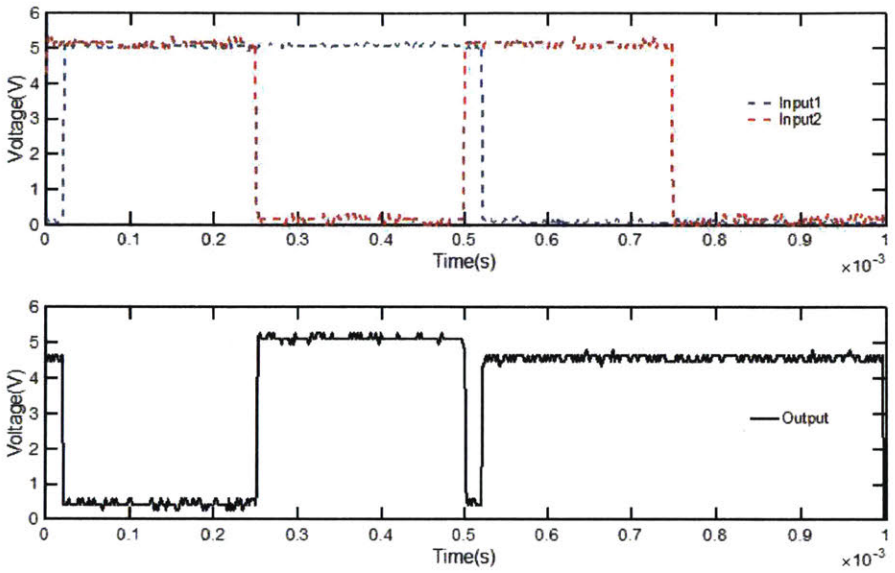



Figure 4-14: Input and output signals of a NAND gate at room temperature.

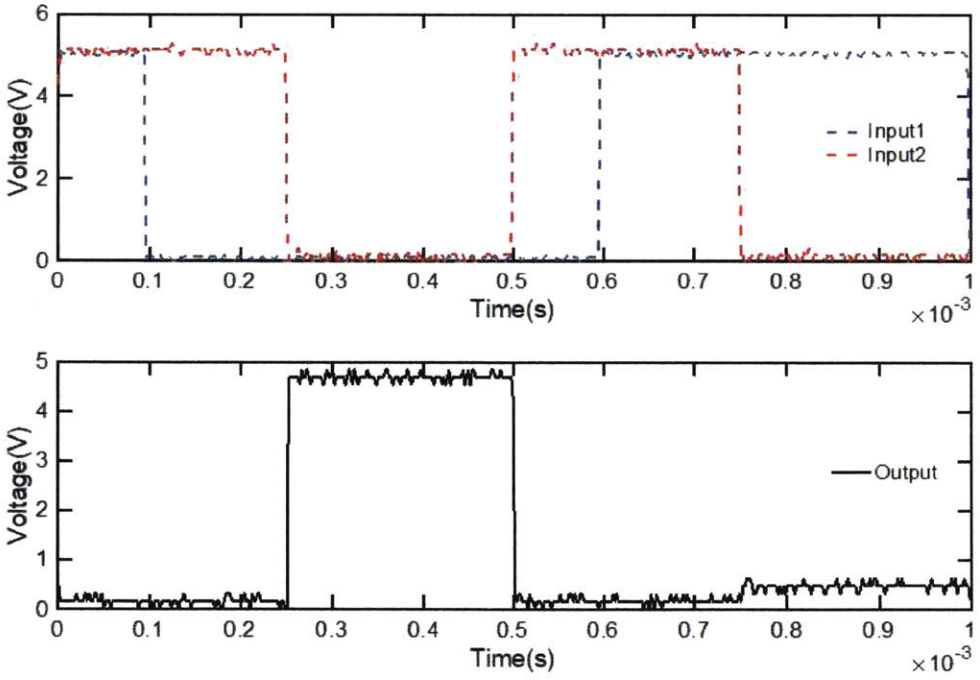



Figure 4-15: Input and output signals of a NOR gate at room temperature.

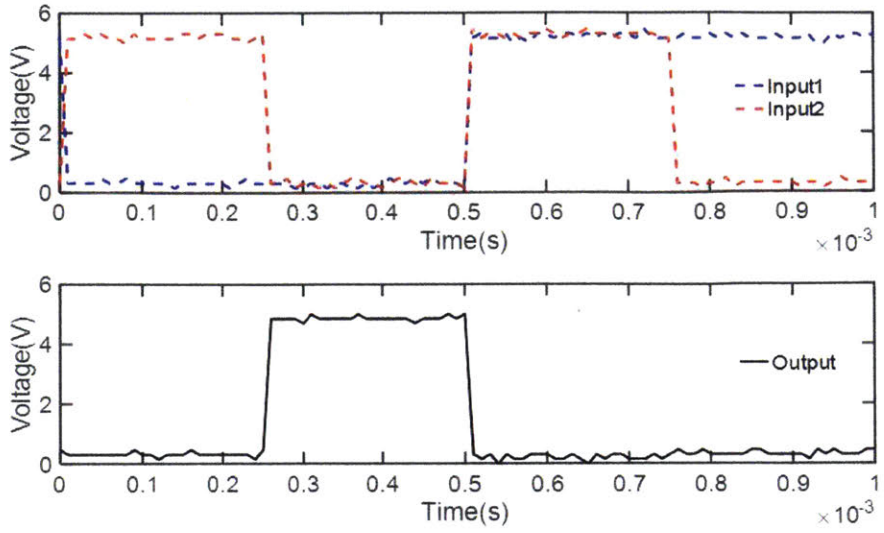



Figure 4-16: Input and output signals of a NAND gate at 150°C, where the output signal is relative to the minimum output voltage.

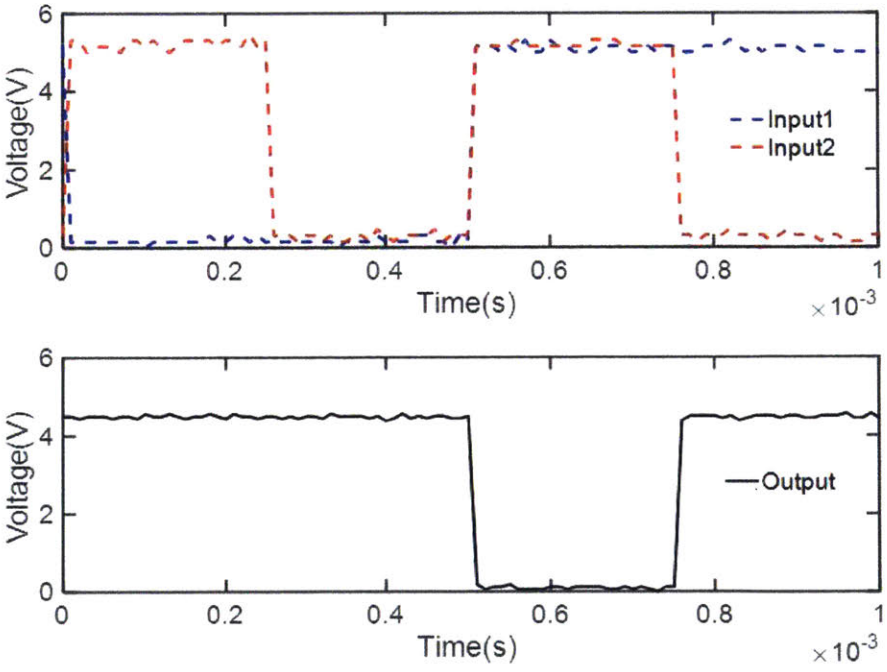



Figure 4-17: Input and output signals of a NOR gate at 150°C, where the output signal is relative to the minimum output voltage.

transistors, where four transistors are responsible for bit storage, and the rest two transistors control the data access. In this work, a simplified 4-transistor SRAM, as shown in Fig. 4-18 was fabricated. Instead of using two more transistors to control read or write, manual control of probes were used here to characterize SRAM performance.

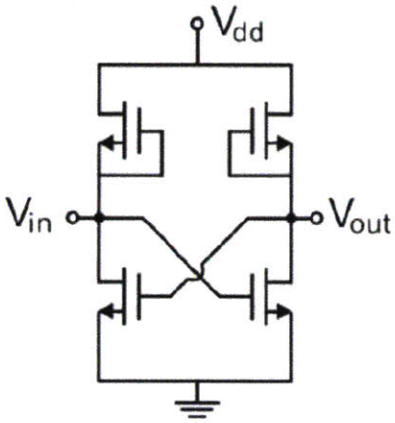



Figure 4-18: Circuit schematic of simplified SRAM.

As shown in Fig. 4-19 (a), a square wave with $V_{DD} = 5$ V was applied at input terminal to simulate writing a logic state. From T = [-60, 0) ms, $V_{out}$ is around 0.5 V (logic state 0) by applying a logic state 1 at input terminal. At T = 0 s, $V_{in}$ is set to logic state 0 driving $V_{out}$ into logic state 1. Similarly, the reverse transition also works properly as shown in Fig. 4-19 (b). The lower logic state 1 is attributed to the large gate leakage current at high $V_{out}$.

A further experiment was conducted to verify the capability of SRAM to store bit information. The input $V_{in}$ is first set to logic state 0 and then opened, while the output remains at logic state 1 as shown in Fig. 4-20 (a). Similarly, when input changes from logic state 1 to open, the output remains at logic state 0.

Both of the measurement results demonstrated here imply a stable operation of GaN-based SRAM, which shows the possibility of on-chip memory.

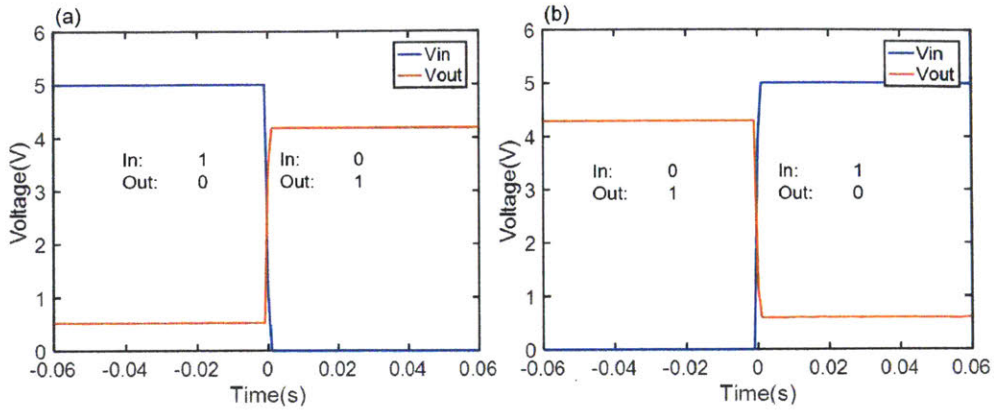



Figure 4-19: Output and Input voltage of SRAM; (a) Input changes from logic state 1 to 0; (b) Input changes from logic state 0 to 1.

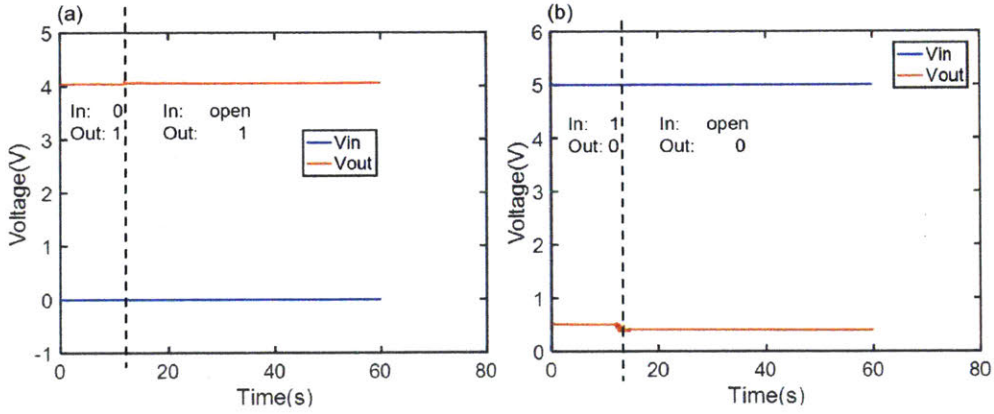



Figure 4-20: Output and Input voltage of SRAM; (a) Input changes from logic state 0 to open; (b) Input changes from logic state 1 to open.

### 4.3.4 Ring Oscillator

5- and 7-stage ring oscillators with the schematic shown in Fig. 4-21 were fabricated and characterized by DSO6054A oscilloscope from Agilent Technologies. 5 or 7 inverters were series-connected in a loop to flip over the signal, and one more stage was connected to the output to isolate the interference from measurement set up. The period of the ring oscillator is how long it will take for the signal to flip twice (from

0 to 1 and back to 0). The frequency of N-stage ring oscillator can be written as

$$f_N = \frac{1}{2N\tau_{pd}} \tag{4.6}$$

where N is the number of stages and has to be an odd number to start oscillation, $\tau_{pd}$ is the propagation delay per stage. From Fig. 4-22, a propagation delay ($\tau_{pd}$) of 0.2 ns/stage is extracted at room temperature and increases to 0.72 ns/stage at 300 °C.

Due to the impedance mismatch of measurement set-up, the measured voltages suffered from severe attenuation, and the voltage swing was much smaller than expected. To prove the fidelity of frequency, another measurement was conducted on different locations, as shown in Fig. 4-23. The blue line represents a 50 MHz square wave generated by function generator with inherent rise/fall time around 4 ns with impedance matched properly. Yellow and green lines represent signals from a 7-stage ring oscillator measured at different locations.

As expected, the yellow line is asymmetrical due to the odd number of inverters in the loop, and difference of propagation delay from high to low ($\tau_{p,HL}$) and low to high ($\tau_{p,LH}$) for single inverter induced by conduction mechanisms of E/D-mode DCFL configuration. In this case, considering a signal starts from logic state 0. When signal travels from the first inverter to the $7^{th}$ inverter, it has been flipped from logic state 0 to 1 for 4 times and flipped from logic state 1 to 0 for 3 times. The total time signal takes to flip from 0 to 1 ($\tau_{pN,LH}$) is

$$\tau_{pN,LH} = 4\tau_{p,LH} + 3\tau_{p,HL} \tag{4.7}$$

$$= \left(\frac{N+1}{2}\tau_{p,LH} + \frac{N-1}{2}\tau_{p,HL}\right)\Big|_{N=7} \tag{4.8}$$

Similarly, $\tau_{pN,HL}$ can be derived as

$$\tau_{pN,HL} = \left(\frac{N+1}{2}\tau_{p,HL} + \frac{N-1}{2}\tau_{p,LH}\right)\Big|_{N=7} \tag{4.9}$$

$$T_N = \tau_{pN,HL} + \tau_{pN,LH} \tag{4.10}$$

$$= N(\tau_{p,HL} + \tau_{p,LH}) \tag{4.11}$$

$$= NT \tag{4.12}$$

where T is the period per stage. Eq. 4.8 and Eq. 4.9 show the compositions of $\tau_{pN,HL}$ and $\tau_{pN,LH}$. In this case, $\tau_{p,HL}$ is different from $\tau_{p,LH}$ due to the DCFL configuration. Therefore, yellow line is asymmetrical when $\tau_{pN,HL}$ is different from $\tau_{pN,LH}$. Similarly, green line is symmetrical with one more stage involved.

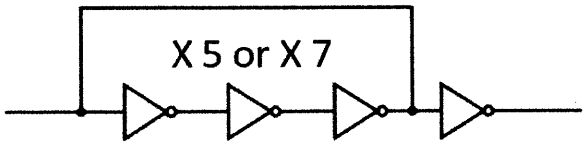



Figure 4-21: Circuit schematics of 5- and 7-stage ring oscillators.

Besides, a voltage dependence of 7-stage ring oscillator was also measured ranging from $V_{DD}$ = 3, 3.5, 4, 5 V. The frequency as shown in Fig. 4-24 is inversely proportional to the bias, which is different from CMOS and another GaN-based ring oscillator reported [59]. Frequency could be further increased by lowering $V_{DD}$.

As illustrated in Eq. 4.10, the period (T) of ring oscillators consists of $\tau_{HL}$ and $\tau_{LH}$. In the case of E/D-mode DCFL configuration, $\tau_{HL}$, just like in CMOS, is inversely proportional to the $V_{DD}$,

$$Q_L \propto C_L V_{DD},\ I_{Dsat,E} \propto (V_{in} - V_{TH,E})^2 \approx (V_{DD} - V_{TH,E})^2 \tag{4.13}$$

$$\tau_{HL} \propto \frac{Q_L}{I_{Dsat,E}} \propto \frac{V_{DD}}{(V_{DD} - V_{TH,E})^2} \tag{4.14}$$

where $Q_L$ is the charge on the load capacitor, $V_{TH}$ is the threshold voltage, $V_{in}$ in this case is $\sim V_{DD}$ during transition and $I_{Dsat,E}$ is the discharging current through

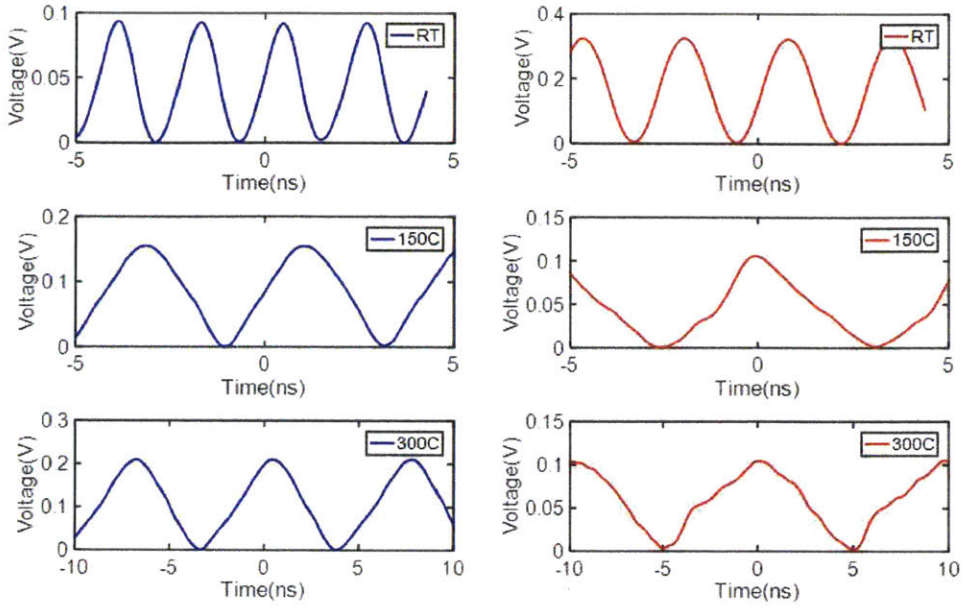



Figure 4-22: Output signals of 5- and 7-stage ring oscillators from room temperature to 300°C. It is worth noting that voltages are relative to the minimum output voltage.

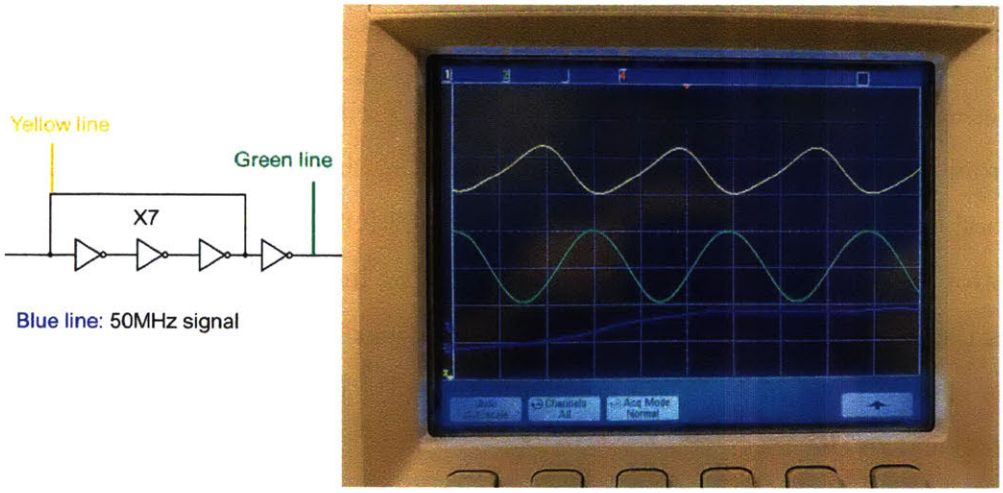



Figure 4-23: Output signals measured at different locations of a 7-stage ring oscillator.

E-mode transistor working in the saturation region.

$\tau_{LH}$, on the contrary, is proportional to the $V_{DD}$ due to the constant saturation

current of the pull-up transistor,

$$Q_L \propto C_L V_{DD} \tag{4.15}$$

$$I_{Dsat,D} \propto (V_{GS,D} - V_{TH,D})^2 = (0 - V_{TH,D})^2 \sim constant \tag{4.16}$$

$$\tau_{LH} \propto \frac{Q_L}{I_{Dsat,D}} \propto V_{DD} \tag{4.17}$$

where $V_{GS,D} = 0$ V and $I_{Dsat,D}$ can be treated as a constant if all the secondary effects are ignored.

In this case, $I_{Dsat,D}$ is designed to be smaller than the $I_{Dsat,E}$ in order to achieve a low $V_{OL}$. Period ($T$) is thus dominated by $\tau_{LH}$ and proportional to the $V_{DD}$.

When the $V_{DD}$ keeps decreasing, the ring oscillator will stop working because $V_{DD}$ is close to $V_{TH}$ of inverter inside, making it impossible to flip the signal.

Ring oscillators fabricated here showed the capability of stable operation at a wide temperature range up to 300°C. A high switching frequency of $\sim$ 500 MHz was achieved with 5-stage ring oscillators at room temperature, and can be further increased by minimizing the gate length. The temperature dependence of the ring oscillator makes it a potential candidate for temperature sensors.

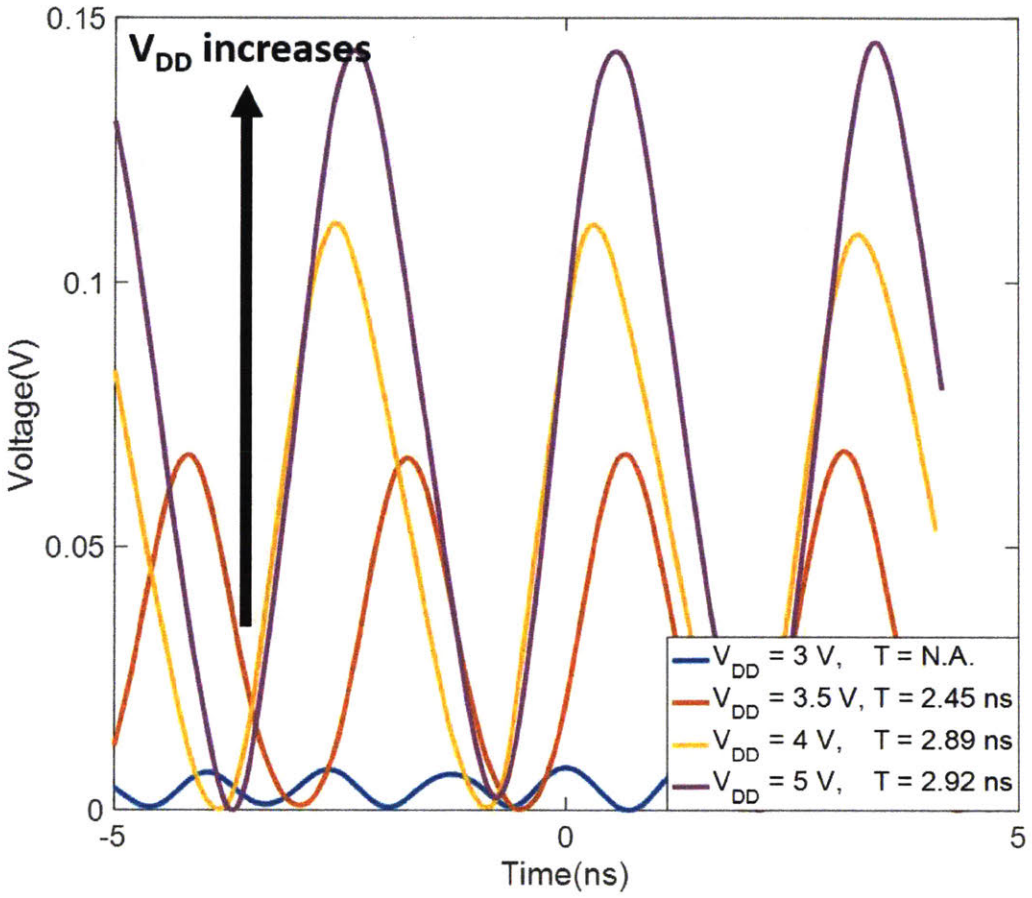



Figure 4-24: Output signals of a 7-stage ring oscillator at different bias from 3 V, 3.5 V, 4 V, 5 V. It is worth noting that voltages here are relative to the minimum measured voltage.

# Chapter 5

# Conclusion and Future Work

## 5.1 Thesis Conclusion

This thesis aims to address some of the problems of GaN-based electronics during high-temperature operation.

Chapter 1 introduced the background and applications of high-temperature electronics. The temperature range of each application was listed. The fundamental physical limitations of standard semiconductors like Si, GaAs were discussed and compared with those of wide bandgap materials. SiC and GaN were introduced and compared regarding material properties, technology infrastructures, and potential applications, explaining why GaN would be a superior choice for high-temperature operation.

Chapter 2 demonstrated an ion-implanted CMOS compatible refractory metal contact scheme in AlGaN/GaN HEMTs on Si (111) substrate with smooth surface morphology. A comprehensive study of contact resistance and activation ratio dependences on implantation condition including energy and dose, activation annealing condition including capping layer, time and temperature, and metalization scheme were conducted on AlGaN/GaN heterostructure. A high-performance contact scheme was obtained and characterized up to 300°C for in-situ measurement and 500°C for ex-situ measurement.

Chapter 3 compared several kinds of E-mode GaN HEMTs and showed the ad-

vantages of gate injection transistors over other candidates. A self-aligned gate first process was developed together with the etch-stop technology for better efficiency, uniformity, and tolerance. The effects of different gate metallizations were studied. The fabricated devices showed low on-resistance, high threshold voltage, and high on-off ratio with stable operation up to 300°C for in-situ measurement and 500°C for ex-situ measurement.

Chapter 4 demonstrated a process for monolithic integration of E/D-mode devices based on the GITs process optimized in chapter 3. The uniformity of fabricated devices was also tested here. E/E-mode and E/D-mode DCFL inverters were compared, showing why E/D-mode DCFL configuration could be a superior option. Additionally, particular attention was focused on demonstrating basic logic building blocks, including inverter, NAND/NOR gates, SRAM, and ring oscillator. All the logic building blocks were characterized up to 300°C with stable operation, implying the potential applications in high-temperature microcontrollers.

## 5.2 Future Work

In this thesis, work has been done to prove the potential of GaN electronics in high-temperature digital circuits. With the potential ohmic degradation issue and e-mode operation issue solved, there is still plenty of space left for further optimization towards the goal: high-temperature microcontroller. Ideas for future work will be summarized here.

- Si-ion implanted refractory metal contact proposed in this work has several advantages over traditional alloyed metal contact, as introduced in the previous section. However, AlGaN/GaN heterostructure degradation induced by activation annealing is inevitable, especially for GaN on Si samples. Further exploration is needed to minimize the 2DEG degradation while maintaining compatible $R_c$. A high access resistance is found between the implanted region and 2DEG channel. More study is required to understand the underlying physics and mechanisms.

- GITs developed in this work showed a high gate leakage current, which was independent of gate width, suggesting a potential sidewall leakage path. The high gate leakage current will degrade the logic unit performance, such as lowering the output voltage of logic state 1 in SRAM. It is desirable to continue optimizing the process in order to achieve a lower gate leakage current and improve the voltage swing.

- High-temperature characterization should be more thoroughly performed for an extended time at a higher temperature (500$^o$C) to verify the reliability of this contact scheme and GITs.

- With implanted contact and GITs process ready, we should combine those two technologies to achieve better high-temperature stability, which is currently ongoing.

- Compact modeling is critical to enable circuit design. Compact modeling performed in the previous chapter was only for room temperature operation. A compact model working at a wider temperature range should be demonstrated to properly simulate the change of device performance with the increase of operating temperature.

- Despite logic building blocks demonstrated here, more complicated circuits like ALU, ring oscillator with more stage, memory array should be fabricated and characterized to show the capability of GaN electronics.

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