Towards Lightweight High-Voltage Power Conversion

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Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

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Abstract

An emerging application, electroaerodynamic (EAD) propulsion, has stimulated the needs for light-weight high voltage dc-dc and dc-ac power converters. Weight reduction of these converters in the operating range of interest has seldom been studied and is limited by lossy switching devices, the size of energy storage components and isolation requirements. Achieving light weight while meeting demands for efficiency, temperature, and isolation requires an understanding of limitations and weight profiles of components and circuit building blocks, as well as advances on multiple subsystems and overall system architecture.

The thesis will present a lightweight high-frequency high voltage dc-dc converter with greatly improved weight density compared with conventional designs; an investigation on losses and temperature rises of high voltage diodes and a circuit technique to use these diodes more effectively; a design study and implementation of a lightweight high voltage dc-ac converter for use in dielectric barrier discharge ion generation; and an demonstration of the first EAD-propelled flight using developed light weight power converters.

Thesis Supervisor: David J. Perreault
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Professor of Electrical Engineering and Computer Science

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Lastly, Mom and Dad, thank you for your unconditional love. I feel sorry that I have not gone home often and I took your love for granted. I have grown maturer and stronger.

At the end of the tunnel looking back, I feel that the graduate school journey truly amplifies a person's weakness and strength, and through all the support, I was able to know myself a bit better and polish myself towards the person I want to become. For all the kindness I received, I am grateful and will carry them along. I hope, you have received something back from me.

Contents

Chapter 1

Introduction

In the past few decades, power conversion, the technology that converts one form of electricity to another, has become part of the backbone of our modern world. Numerous applications, such as electric vehicles, renewable energy, data centers, and many others, have driven advances in power electronics towards higher efficiency and better performance. In return, innovations in power electronics have enabled the wide spread of these applications and sometimes support entirely new applications.

The primary accomplishment of this thesis – enabling lightweight high voltage power conversion – is driven by an emerging solid-state electric propulsion technology for aeroplanes, electroaerodynamic (EAD) propulsion. An EAD-propulsion aeroplane has no moving parts; instead, the surrounding air is ionized and accelerated by high voltages to generate an ionic wind as the propulsive force. No aeroplane with EAD propulsion had ever flown until the collaborative work in this thesis (Chapter 6), partly due to heavy weights of existing high voltage power converters, and partly due to limited understanding of using EAD phenomenon effectively for aircraft propulsion. The developments on both fronts have been tightly integrated and conducted by a cross-disciplinary MIT team. This thesis focuses on two main challenges:

- Develop lightweight high voltage power electronics for the EAD application (addressed in Chapter 2, 3, 4, 5). Though the requirements on the power electronics are set by the EAD technology, much of the research would be relevant

to lightweight high voltage power converters in other applications.

- Facilitate the demonstration and the improvement of using EAD for aircraft propulsion (addressed in Chapter 6).

The requirements on the high voltage power system of an EAD aeroplane include:

- A lightweight high voltage dc-dc converter to ionize the air through corona discharge, which was the only method of ion production and thrust generation for EAD propulsion until the collaborative work in this thesis (Chapter 6). The demonstration of the first EAD-propelled flight in Chapter 6 and [1] is the proof-of-concept of corona-based EAD for aircraft propulsion.

- A lightweight high voltage dc-ac converter to ionize the air through dielectric-barrier discharge as an addition to corona discharge, which was identified in the collaborative work (Chapter 6) as a means to improve the performance and the efficiency of EAD propulsion.

In this chapter, Section 1.1 reviews the EAD propulsion technology and the requirements on high voltage power electronics. Section 1.2 and 1.3 review the state-of-the-art of high voltage dc-dc and dc-ac converters respectively. Section 1.4 outlines the remaining chapters in this thesis.

1.1 Electroaerodynamic propulsion

An electroaerodynamics (EAD) thruster generates propulsive force from the interaction of a group of unipolar ions with neutral molecules in the working fluid (the air in the following content). We consider an EAD thruster with two electrodes: an emitter electrode, where ions are injected, and a collector electrode, where ions are neutralized, separated by an air gap. Ions are propelled and "drift" along electric field lines by an applied electric field between the two electrodes. These ions collide with neutral air molecules along the field lines. The "friction" from these ion-neutral collisions, which acts in the opposite direction to the ion drift, is transferred via the ions and the electric field onto the electrodes: this forms the propulsive thrust force [2–5].

1.1.1 Corona discharge based EAD thruster

In EAD propulsion thrusters developed to date, the source of the unipolar ions is by a dc corona discharge. A dc potential difference is applied between two electrodes. When the electric field strength at an electrode exceeds a certain critical field strength, a chain of electron-impact ionization events creates a self-sustaining source of ions in the vicinity of the electrode. If that electrode is an anode, then the ions are positively charged and a positive corona is formed, vice versa for the negative corona. In order to ensure that ions are only produced at one electrode – the emitter – there must be an asymmetry in the electrode geometry so that the electric field strength at the emitter is greater than the critical field strength, and that at the collector is not. As an example, Figure 1-1a shows a wire-to-cylinder geometry used for EAD propulsion.

The high voltage dc required to excite a corona discharge largely depends on electrode geometries, gas properties, etc. The work at MIT by Gilmore [2, 3] and Xu [6] has identified the desired voltage to be at medium-to-high tens of kV which provides hundreds of watts for the EAD propulsion system of interest. The specific power of the high voltage dc-dc converter needs to be $\geqslant$1 kW/kg and still higher is preferable as technology allows.

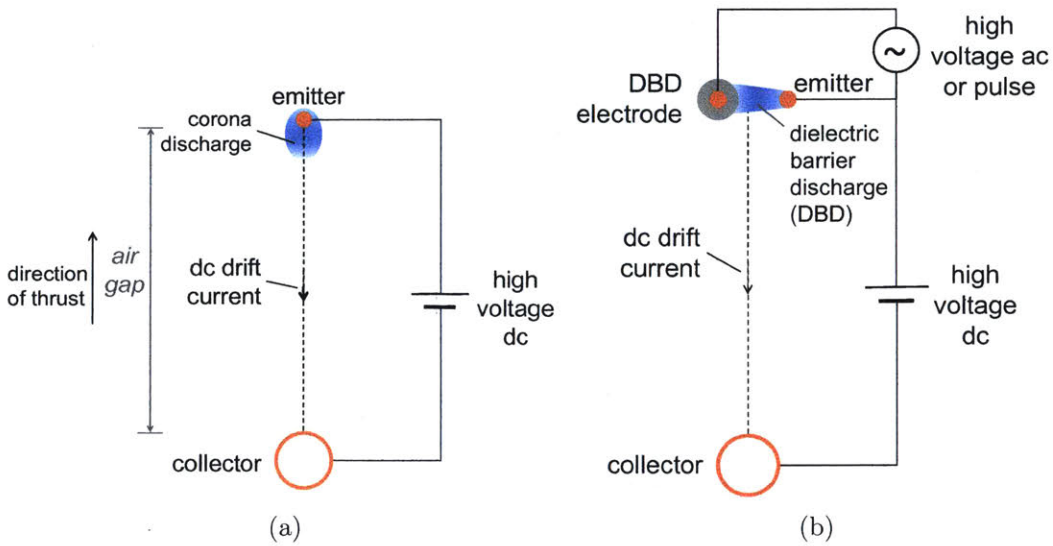
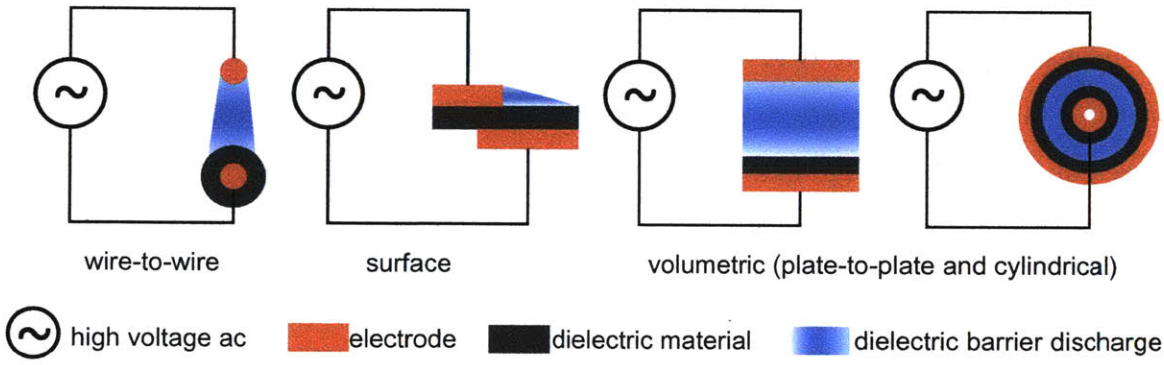


Figure 1-1: Cross-sectional schematics and electrical requirements of (a) a wire-to-cylinder corona-based EAD thruster and (b) decoupled EAD thruster in [7].

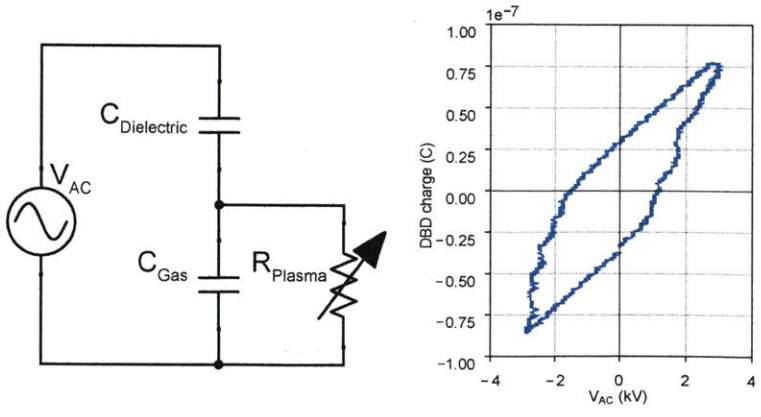
1.1.2 Dielectric barrier discharge and decoupled thruster

The collaborative work in Chapter 6 and [7] reveals that adding a separate dielectric-barrier-discharge (DBD) ion source in addition to the corona-discharge ion source can improve the thrust generation and thus the performance of EAD thrusters, as shown in Figure 1-1b. We call it the "decoupled thruster" in this thesis.

DBD is a form of gas discharge that uses alternating-current (ac) or pulsed high voltage to generate ionized gas at atmospheric pressure [8–11]. A basic DBD setup consists of a set of metal electrodes with one or both electrodes covered by a dielectric layer (such as glass and kapton or inert gases), as shown in Figure 1-2a. The form of DBD is versatile: the wire-to-wire structure in [7], the surface structure in [12, 13] and the volumetric structures in [14].



(a)



(b)

Figure 1-2: (a) Examples of dielectric barrier discharge configurations [15] and (b) an equivalent electrical circuit model.

DBD has been widely used in industrial processes such as surface treatment and sterilization [16], ozone [17] and UV [18–20] generation. Recent studies in [12, 21, 22] also use DBD as a flow actuator to control air flow at the surface of airplane wings.

The equivalent electrical circuit model of a DBD is capacitive before ignition and a capacitive/resistive hybrid after ignition [12, 23–25], as shown in Figure 1-2b. $C_{Dielectric}$ represents the capacitance of the dielectric layers, C_{Gas} represents the capacitance of the gas gap, and R_{Plasma} is infinite before ignition and a voltage-dependent resistor after ignition. There is no conclusive governing equation for R_{Plasma}. In practice, a Lissajous loop shown on the right of Figure 1-2b [7] is used to show the charge-voltage relationship of the DBD or an empirical power equation $P = fV_{AC}^{n}$, where n ranges from 2 to 3.5 [12], is used to predict the power draw of the DBD. Both the shape of the Lissajous loop and the power equation vary with DBD configurations, waveform, gas properties, etc.

A wide range of high voltage ac waveforms or pulses (including different shapes, frequencies (generally several to hundreds of kHz), amplitude (generally several to tens of kV), etc) can be used to generate the DBD [12, 26]. How they affect the efficiency of the thrust generation of the "decoupled thruster" is not conclusive and is being studied by the MIT EAD team at the time of this writing. A preliminary requirement on the high voltage ac (Chapter 6 and [7]) is a sinusoidal wave at several kV, several to low tens of kHz and providing low hundreds of watts.

1.2 High voltage dc-dc power converters

This section reviews the state of the art of high voltage dc-dc power converters, especially focusing on their weight (or equivalently specific power, defined as power delivered per unit of weight (kW/kg)) and topologies.

High voltage dc-dc power converters are essential in many industrial, medical and aerospace applications. Such a converter is most commonly used as a pulsed power source [27–46] and sometimes as a dc power source [47–52].

In a pulsed power system, the high voltage dc-dc converter powers the load on

and off in a short pulse and sometimes repetitively. The power and voltage scale of such a system vary widely: space and airborne radio-frequency accelerators and microwave weapon platforms [30–35] require 100 kV+ and 100 kW to 1 MW; x-ray machines [36–41] and industrial electrostatic precipitators [42, 43] require medium-to-high tens of kV to 100 kV and tens of kW; industrial magnetron/microwave [44] for food and material processing and communication equipment require low tens of kV and tens to hundreds of kW; micro and nano communication satellites [45, 46] requires several kV and several to hundreds of W.

In a dc power system, the high voltage dc-dc converter is expected to power the load for a longer period of time. Example applications include: DC microgrids [47,48] require tens of kV and hundreds of kW to hundreds of MW; space ion thrusters [49,50] require hundreds of V to several kV and several kW; their miniaturized counterpart microthrusters [51, 52] require similar voltage level but several to tens of W.

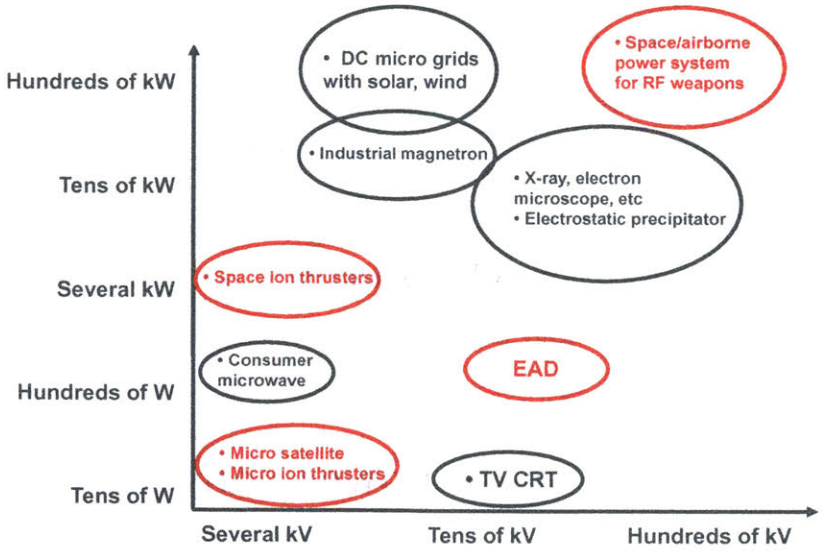


Figure 1-3: Applications of high voltage power converters at various power and voltage levels. The applications circled by red are weight sensitive.

Figure 1-3 summarizes the power and voltage ranges of these applications. Some applications, especially for space and aircraft [30–35, 45, 46, 49–52] (circled by red in Figure 1-3), are weight sensitive and therefore have driven research on converters with high specific power. Whereas in other applications where weight has not been

a critical concern, there has been less research looking into weight reduction of the power converter. The EAD propulsion system of interest [2,3,6] requires high voltage dc at medium-to-high tens of kV and hundreds of W, falling into a unique high-voltage low-power region.

1.2.1 Specific power

The specific power of existing high voltage dc-dc power converters depends strongly on the voltage and power level. For mega-watt, hundreds-of-kilovolt, power converters, it can reach as high as 10 kW/kg [34]. For tens of kV and tens of kW, 1 kW/kg has been achieved in research papers [34, 53]. However, there has been less research in reducing the converter weight in the sub-kW and medium-to-high tens of kV range.

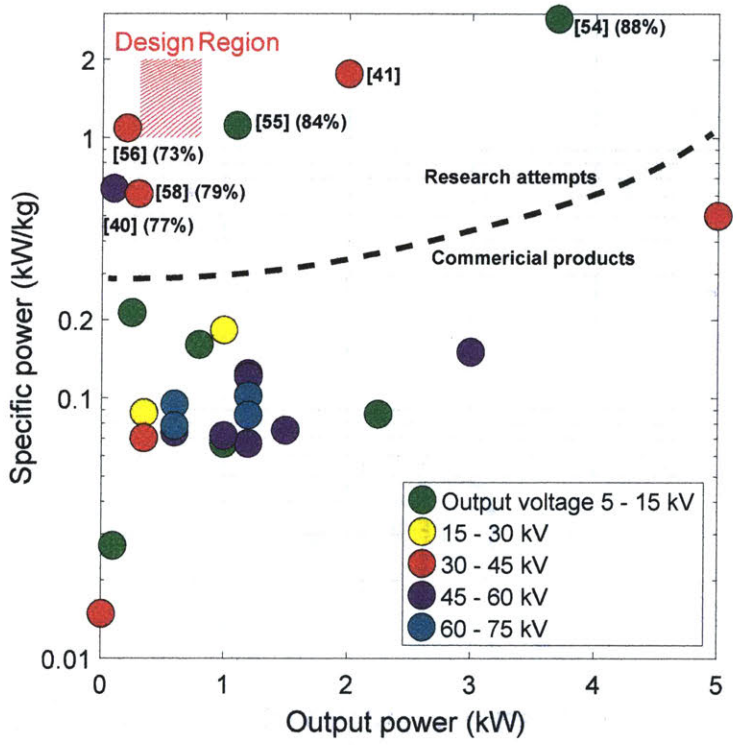


Figure 1-4: Specific power of commercial high voltage dc-dc converters and academic designs at low to moderate power levels. The reported efficiencies of the academic designs are listed next to the citations. Efficiency of commercial products are seldom published thus are not included. The design region marks the requirements of the high voltage dc-dc converter for the EAD propulsion system of interest.

In Figure 1-4, a review of commercial products and academic designs in this range

reveals that the specific power is typically around 0.1 kW/kg. In commercial HVPCs in this power and voltage range, the switching frequency typically lies around 100 kHz or lower, resulting in bulky magnetics and capacitors.

There have been research attempts ([41,54,55] and the ones published after this work [40,56,57]) to increase the switching frequency and thus the specific power, but these have largely focused on cases of low output voltage (<= 20 kV) [54, 55, 57], and/or out of the power range of interest (>= 2 kW [41, 54] or <= 200 W [40, 56]). The detailed list of products and academic papers in this comparison is provided in Table A.1. Precise weight information of academic designs in [41, 54, 55, 58] is not documented thus the author estimated these numbers from the papers.

1.2.2 Topologies

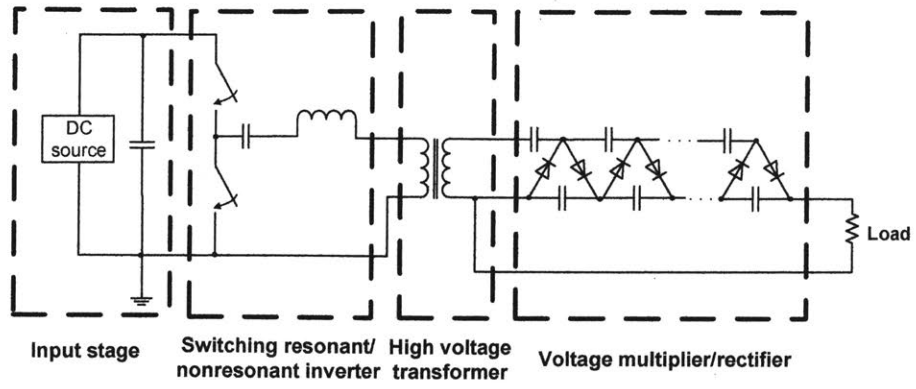
High-voltage dc-dc power converters achieve large step-up voltage conversions utilizing 1) resonant and/or multi-level inverter topologies; 2) large-turns-ratio transformers and/or resonant transformers; 3) voltage multiplying rectifier topologies; and/or 4) parallel-input, series-output connected conversion blocks.

Common circuit topologies used by existing high voltage dc-dc converters are summarized in Figure 1-5 [59, 60]. The simplest topology (Figure 1-5a) consists of a switching resonant or nonresonant inverter, with a step-up high voltage transformer, and a voltage multiplier or a bridge rectifier. To achieve higher power and higher voltage, multiple copies of partial (Figure 1-5b) or full converter (Figure 1-5c) are often connected parallel at the input and series at the output [61].

1.3 High voltage dc-ac converters for DBD

This section reviews the state of the art of high voltage dc-ac power converters for dielectric-barrier discharge (DBD), focusing on their specific power and topologies.

A high voltage inverter [13, 14, 62–67] or a high voltage pulse generator [68–71] is commonly used to drive the DBD (the pulse generator often uses a high voltage dc-dc converter, similar to those mentioned in Section 1.2).



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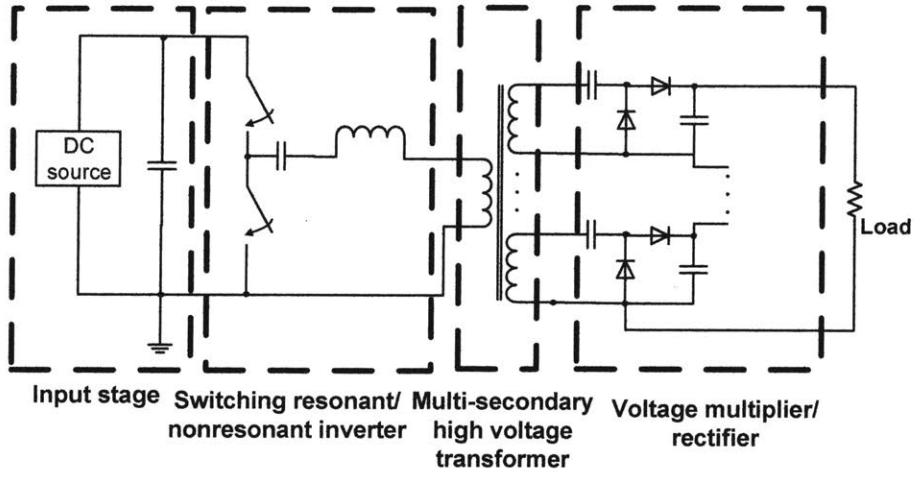

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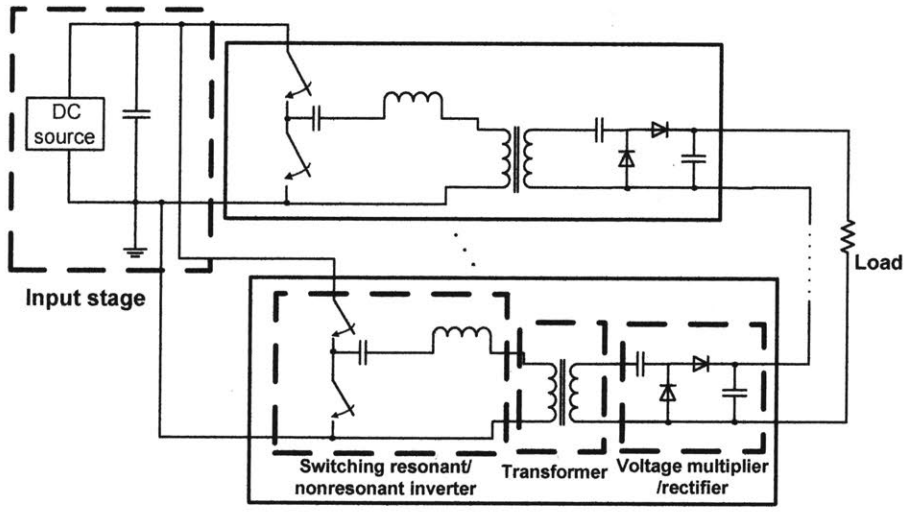


(c)

Figure 1-5: Typical topologies of high voltage dc-dc converters (a) three-stage converter; (b) and (c) Parallel-input series-output topologies.

1.3.1 Specific power

Figure 1-6 shows a review of commercial and academic high voltage inverters and pulsers for DBD applications in the range of interest (several kV, several to low tens of kHz and low hundreds of W). It reveals that the specific power of commercial products lies in 0.01–0.2 kW/kg range. There has been sparse information on the weight of such converters in academic papers. Saleh [13] presents a 1.5 kV 750 W inverter at a specfic power of 0.69 kW/kg. Raymond [70] has designed a 2 kV 100 W high voltage pulser switching at 27.12 MHz with high power density (no weight information is provided in the paper, I estimate the specific power to be ~2 kW/kg).

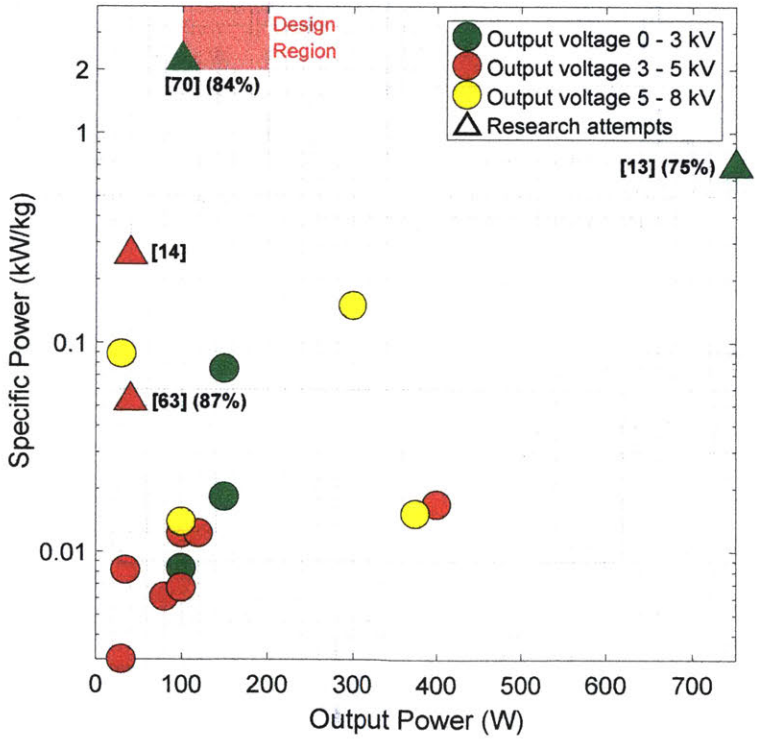


Figure 1-6: Specific power of commercial high voltage inverters or pulse generators and academic designs at hundreds of W. The reported efficiencies of the academic designs are listed next to the citations. Efficiency of commercial products are seldom published thus are not included. The design region marks the requirements of the high voltage dc-ac converter for the EAD propulsion system of interest.

1.3.2 Topologies

Here we review the topologies of high voltage inverters for DBD applications. They generally fall into two categories, as shown in Figure 1-7:

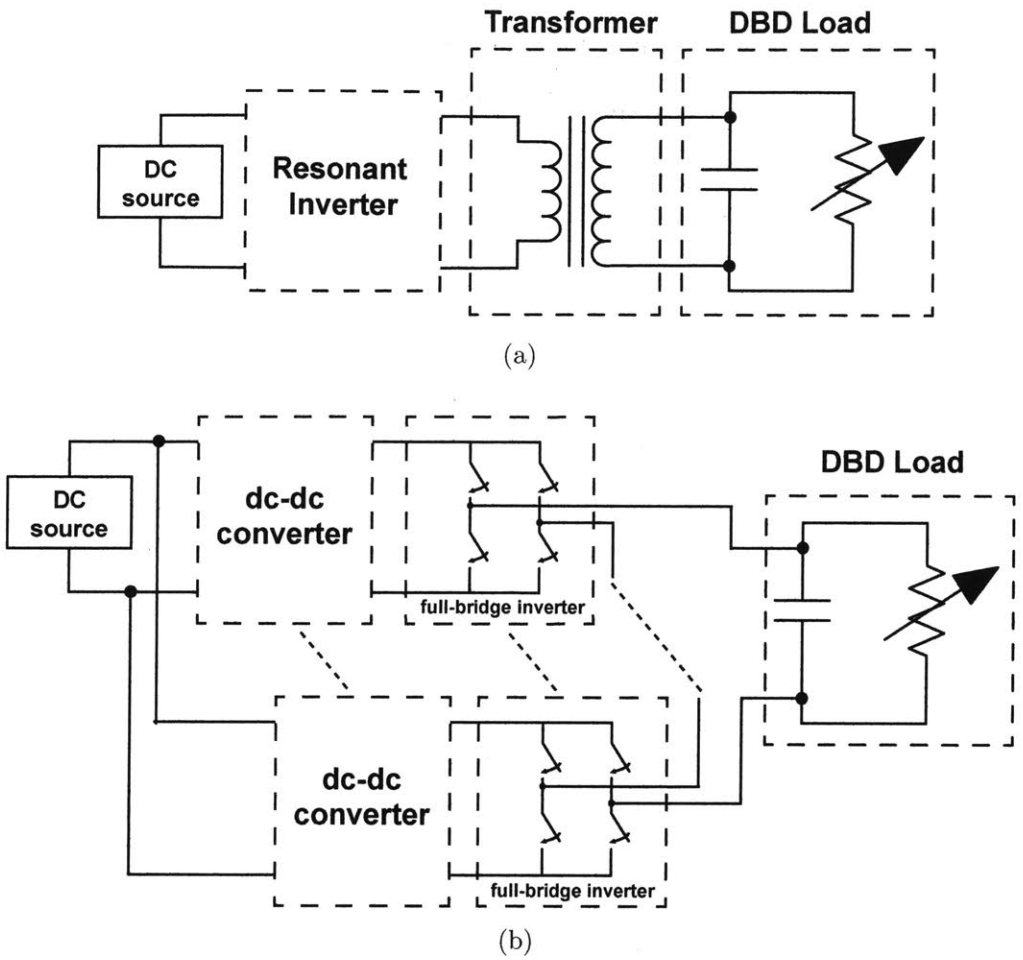


Figure 1-7: Simplified diagrams of two topology categories of high voltage inverters/pulse generators for DBD (a) resonant topologies and (b) non-resonant topologies.

- Resonant topologies, where the inductance in the system resonates with the capacitances in the system near the DBD frequency. The inductance can be standalone, or the leakage inductance of a transformer [14, 62–64, 68, 69], or magnetizing inductance of a transformer [62,65], or both [66]. The capacitance can be a combination of the DBD capacitance, the transformer parasitic capacitance, and/or external capacitors. The resonance, and/or the transformer step-up ratio, contributes to the voltage gain.

- Non-resonant topologies where an inverter operates as a voltage source and "hard charges" the DBD capacitive load. The dc-dc stage is usually present for higher voltage gain, regulation and/or isolation purposes, and there are diversified implementations (such as a boost converter in [13], a flyback converter in [72], a Marx generator in [73]). The switching frequency of the dc-dc converter can be much higher than the DBD frequency. The same copies of the converter can be stacked in series at the output to achieve a higher voltage, and/or to form a multi-level output waveform.

1.4 Thesis outline

Chapter 2, 3 and 4 describe the development of lightweight high voltage (HV) dc-dc converters. Chapter 5 illustrates the development of lightweight high voltage dc-ac converter. Chapter 6 presents the interdisciplinary and collaborative work with members of the MIT Department of AeroAstro on the EAD team.

Below, I briefly review the contents of each of the thesis chapters.

1.4.1 1st-generation lightweight HV dc-dc converter

Weight reduction of dc-dc converters for high voltage and low power applications (tens of kV and hundreds of W) has seldom been studied. Chapter 2 first studies the weight of each building block of a high voltage dc-dc converter. Such a converter generally comprises an inverter, a step-up transformer and a rectifier, with the large needed voltage gain distributed among these stages. Several means of realizing these stages are compared in terms of weight. The weight of the converter is minimized by properly selecting and optimizing the design and the voltage gain of each stage within the constraints of device limitations and losses. A prototype circuit is developed based on this approach and used to drive an EAD-propulsion aeroplane in Chapter 6. It operates from a 160–200 V dc input and provides a dc output of up to 600 W at 40 kV. It operates at around 500 kHz and achieves a specific power of 1.15 kW/kg. This is considerably lighter than comparable industrial and academic designs at this power

level. Part of the work has been published [74].

1.4.2 Evaluation of HV diodes and series diode balancing

Chapter 2 has identified that miniaturization of high voltage dc-dc converters is severely limited by the availability of fast-switching, low-loss high-voltage diodes.

Chapter 3 explores techniques for using discrete low-voltage diodes in series as one high voltage diode in high-frequency applications (e.g., hundreds of kHz and above). We identify that when series connecting diodes, the parasitic capacitance from the physical diode interconnections to common can result in voltage and temperature imbalance among the diodes, along with increased loss. We quantify the imbalance and propose two related compensation techniques. To validate the approaches, a full-bridge rectifier is tested with each branch consisting of four 3.3 kV SiC diodes in series. Experimental results show the imbalance and demonstrate the effectiveness of the compensation techniques. Additionally, we characterize the performance of a range of diodes for use in high-frequency, high-voltage converters. The proposed technique and evaluation results will be valuable for the design of lightweight and miniaturized high voltage power converters. The work has been published [75, 76].

1.4.3 Design study of 2nd-generation lightweight HV dc-dc converter

After proving the feasibility of an EAD-propelled aeroplane by the first flight demonstration, the MIT EAD team targets at improving the performance of such a system and proving its practicality when used in missions.

Two major changes to the high voltage power electronics for the 2nd-generation EAD system include 1) a higher-voltage dc-dc converter with higher specific power and 2) an additional high voltage dc-ac inverter to power a separate dielectric-barrier discharge ion source (addressed in Chapter 5).

In Chapter 4, we improve the specific power of the high-voltage dc-dc converter by incorporating insights learned about high voltage diodes in Chapter 3 in the design

of voltage multipliers, and explore more flexible high voltage transformer designs that may yield lower weight, including customized core size and core shape, different winding patterns, and various high voltage wires. A final design is selected: the converter operates from a 200 V dc input and provides a dc output of up to 600 W at 60 kV. It is designed to switch at 1 MHz and achieve a specific power of 2 kW/kg ideally and 1.5 kW/kg with safety margin.

The construction of a hardware prototype and the experimental demonstration have not been finished and will be continued after this thesis.

1.4.4 Lightweight HV dc-ac converter

Chapter 5 explores designs of a lightweight high voltage dc-ac converter to power the dielectric-barrier discharge for the 2nd-generation "decoupled thruster".

This chapter first studies the weight profile of two common high voltage inverter topology categories in Fig. 1-7 by quantifying the achievable weight and specific power of an example converter in each category. We then propose three lightweight converter designs: a) high-frequency transformer based converter with frequency conversion, b) high-frequency transformer based converter with burst-mode control, c). switched-capacitor multi-level inverter based solution. The latter two proposed approaches are demonstrated with preliminary experimental results. A prototype switched-capacitor multi-level inverter is built and tested to convert a 300 V dc input to $\pm$2.88 kV 10 kHz ac, delivering 91 W at 86% efficiency. At the time of thesis writing, the prototype is continuing to be tested to the full design range: $\pm$4 kV and 200 W. At the designed full power, the prototype is expected to achieve a specific power of 1.45 kW/kg.

The work on switched-capacitor multi-level inverter is collaboratively done with Suzanne O'Meara and is continued by her as part of her Master of Engineering thesis.

1.4.5 Integration with EAD system

Chapter 6 presents the collaborative work with other members on the MIT EAD team, including the integration tests of the developed 1st-generation dc-dc converter

with the EAD aeroplane prototypes, the demonstration of the first flight of the EAD plane, as well as the development of a "decoupled" EAD thruster using dielectric barrier discharge. The work has been published [1, 7].

Part I

Lightweight High-Voltage DC Power Conversion

Chapter 2

First generation lightweight high voltage dc-dc power converter

This chapter explores the design of a lightweight high-voltage dc-dc power converter suitable for the electro-aerodynamic (EAD) propulsion system, and other potential aerospace and medical applications.

The preliminary design space of the converter for the EAD application is set at a dc input of 200 V, a dc output of 40 kV and 700 W, and a specific power of $\geqslant$ 1 kW/kg. The development of other components in the EAD system (including the thruster and the battery system) was conducted along-side this work, during which the design space had been refined[1].

A high voltage converter typically consists of three stages: a dc-ac inverter stage, an isolation/transformation stage and an ac-dc rectifier stage. Each stage provides a voltage gain to build up the required output voltage.

This chapter firstly compares different approaches and topologies to realize each stage in terms of the resulting weight. Furthermore, the overall weight of a converter based on the best identified approach is optimized by sweeping through combinations

[1]The 200 V was chosen because 1) building a 200 V battery pack seems manageable, 2) it is within the voltage limit of available GaN MOSFETs. The 40 kV was chosen to balance the development risks and the performances of the propulsion system. The corona EAD thrusters tested at the time design decisions were made were small-scale and thus had a lower arcing limit of $\sim$ 40 kV. Their performance seemed reasonable to achieve a free flight. Meanwhile, the engineering difficulty of building a high-specific-power 40 kV high voltage power converter seemed manageable.

of voltage gains for the different stages with considerations of device limitations and losses. An optimized prototype converter is designed, constructed and tested at 40 kV and up to 565 W. At the peak output voltage and power, it switches at ~500 kHz, at least 5 times higher than that of most conventional designs. It achieves an efficiency of 85 % and a specific power of 1.15 kW/kg, substantially higher than conventional designs in its power and voltage class. The prototype is used to drive an EAD aeroplane and demonstrated the first flight of such an airplane (Chapter. 6 and [1]).

Section 2.1 explores the design goals at a high level, analyzing trade-offs of different approaches and topologies to realize each stage. Narrowing down to the specific design target of the EAD application, Section 2.2 selects and optimizes the topology of the converter, taking into consideration the practical constraints of available devices. Section 2.3 describes practical issues in building such a lightweight high voltage dc-dc converter prototype, and presents experimental results of the prototype converter.

2.1 Topology comparison

High voltage dc-dc converters achieve a large step-up voltage ratio using a combination of: (1) resonant and/or multi-level inverters; (2) large-step-up-ratio isolation stage; (3) voltage multiplier rectification stage; and (4) parallel-input series-output structures [77].

In conventional designs, two major sources of the overall weight of the converter are the passive components in the isolation stage (e.g. transformer core and windings) and rectifier stage (e.g. high voltage capacitors, diodes and potentially the required mechanical structures for support and cooling). Increasing the switching frequency of the converter can reduce the weight of both the transformer and the high voltage capacitors, however the feasibility of doing so is limited by the performance of available high-frequency high-voltage diodes.

This section compares the weight of different topologies/approaches to realize each stage. Section 2.1.1 compares the weights of 4 voltage multiplier topologies considering the characteristics of available high voltage capacitors and diodes. Section 2.1.2

compares the weight of conventional cored transformers, resonant transformers and piezoelectric transformers. Section 2.1.3 briefly analyzes the trade-offs of each resonant inverter topologies.

Based on the weight study and engineering considerations such as risks and practicality, a cored-transformer and a series-parallel resonant inverter are chosen. The voltage multiplier topology and the voltage gain distribution among three stages are further selected and optimized in Section 2.2.

2.1.1 Voltage Multiplier

The weights of voltage multipliers in different topologies substantially depend on available high voltage capacitors and diodes. We have conducted a study of some available high voltage diodes (Table. D.1) and capacitors (Table. D.2), as shown in Appendix. D.1.1.

High voltage capacitor selection

Mica, film and ceramic capacitors are commonly used in high voltage power converters. For tens of kV and hundreds of watts applications, the rated voltage, the capacitance and the weight of the capacitors are three main considerations. Whereas the ESR and the current carrying capability of the capacitors are less important because of the relatively small output current.

Capacitor weight varies widely across rated voltage, capacitance, materials, package, and manufacturer. When the rated voltage is below ~4–5 kV, there are SMT options in all three materials, among which ceramic capacitors with similar capacitance yield slightly lower weight. When the rated voltage is above 8 kV, there are limited options. Ceramic capacitors with leads offer medium capacitance (up to 1 nF) and relatively high rated voltage (up to 15 kV), and are much lighter options compared with ceramic screw-mount capacitors, Mica and film capacitors at these voltage ratings (the latter three have a bigger package and thus heavier weight).

To realize a capacitor blocking a high voltage, the two lightest options are 1) using

ceramic SMT capacitors rated below 5kV in series and parallel 2) using one single ceramic through-hole capacitor.

Among the investigated parts, Murata DHR series ceramic through-hole capacitors have the least weight in the 6.3–15 kV range, and KEMET C0G ceramic SMT capacitors offer a wide range of capacitances and packages in the 1–3 kV range, thus they are used in the following analysis. At a given rated voltage, the weight of the capacitor is shown to be proportional to its capacitance, thus a linear relationship is extrapolated for other capacitances at this voltage rating[2] , see Fig. 2-1 for examples in the range of 10–15 kV. See Appendix. D.1.1 for the linear relationships at other voltage ratings.

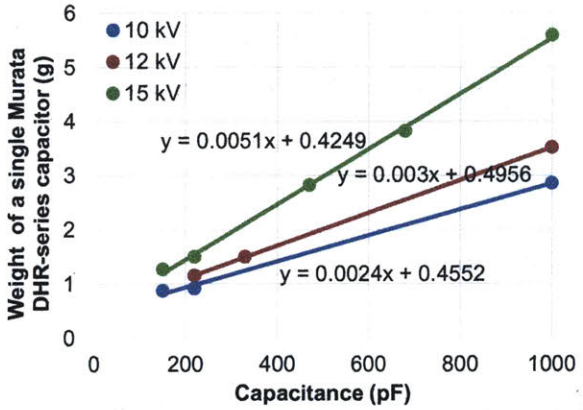


Figure 2-1: Capacitance and voltage dependency of Murata DHR series high-voltage capacitors (the dots are the measured weights and the lines are their linear fits.)

High voltage diode selection

High voltage diodes are a key limitation in building a high frequency high voltage converter at tens of kV and hundreds of watts. Traditional silicon high-voltage diodes ($>$ 8 kV) have longer recovery times compared to their low-voltage counterparts, thus are typically used at frequencies below 100 kHz. Commercially available and affordable high voltage SiC schottky diodes are mostly rated under 3.3 kV. They

[2]In the same family and from the same manufacturer. Note that the linear relationships may vary significantly for other manufacturers, series and materials

have less or no recovery time[3] but a big parasitic capacitance since they are mainly designed for high current applications and have a large die size.

Some representative high voltage diodes are summarized in Appendix. D.1.1. Cree's C4D02120A, GeneSiC's GAP3SLT33-214 and VMI's X150FF3 are considered in later studies in Section 2.2 because of their small recovery time and relatively low parasitic capacitance. There have been also emerging SiC PiN diodes rated at 8 kV (GAP05SLT80-220 from GeneSiC) and 15 kV (GA01PNS150-201 GeneSiC) that could be interesting to explore if at a more affordable price.

The design frequency is chosen to be 500 kHz considering a non-zero "switching time" listed in the datasheet of GAP3SLT33 (no definition of this "switching time" is found) and the 30 ns recovery time of the X150FF3.

Weight study of various voltage multiplier topologies

The typical topologies of the voltage multipliers (VM) used in high voltage converters include half-wave (HW) and full-wave (FW) Cockroft-Walton (CW) and half-wave (HW) and full-wave (FW) Dickson, as shown in Fig. 2-2. All flying capacitors are odd-indexed and all output capacitors are even-indexed.

We approximate the weight of the voltage multiplier as the weights of its capacitors. The weights of multipliers in each topology achieving a 40 kV 700 W output at different input voltages (thus different voltage gains) are compared in Fig. 2-3a.

At the power and voltage level in this application, and with the device considerations described above, Cockroft-Walton topologies yield similar weight with Dickson topologies but have easier implementation[4]; when the required voltage gain is lower than 10, full-wave topologies yield lower total weight (owing to interleaving reducing output capacitance), and so are strongly preferred; when the required voltage gain is higher than 25, half-wave topologies yield lower total weight (because they provide the same voltage gain with a halved number of stages, and a further halved flying

[3]There is a non-zero "switching time" listed in the datasheet of some of these diodes (for example, the 3.3 kV SiC schottky diode GAP3SLT33-214).

[4]In CW topologies, capacitors and diodes block the same voltage other than the flying capacitor in the 1st stage. Whereas in Dickson topologies, the blocking voltage increases in higher stages.

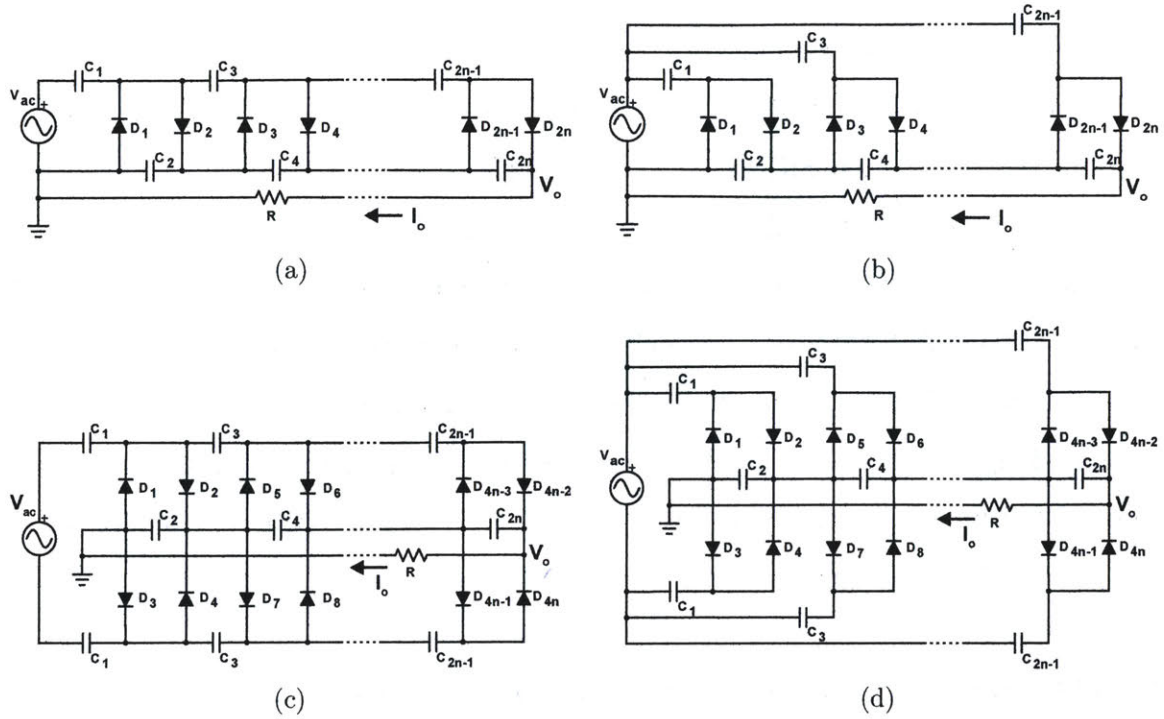


Figure 2-2: Four basic voltage multiplier topologies (a) Half-wave Cockcroft-Walton, (b) Half-wave Dickson, (c) Full-wave Cockcroft-Walton, and (d) Full-wave Dickson.

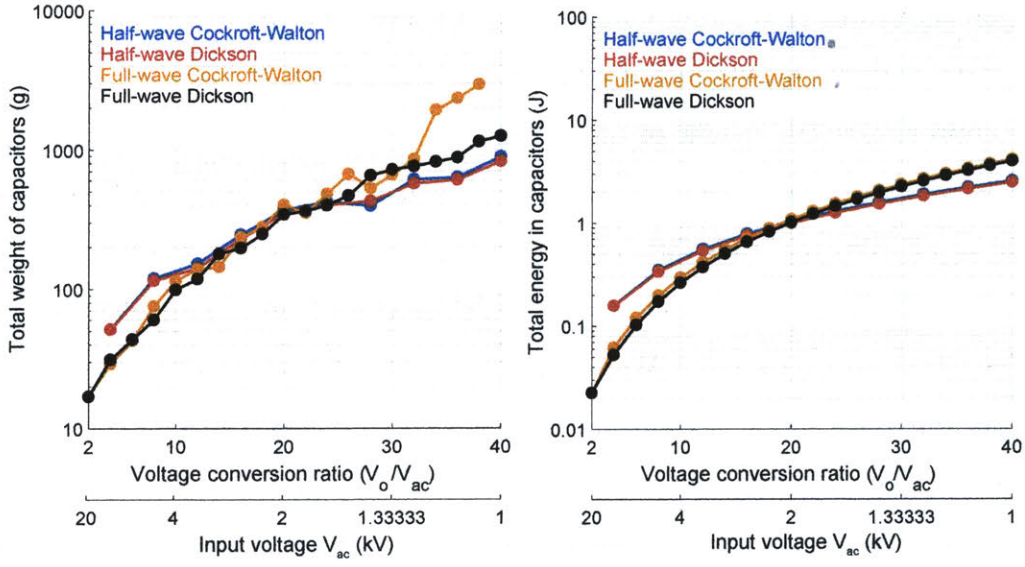


Figure 2-3: (a) Total weight of the capacitors and (b) total energy stored in the capacitors of the Cockroft-Walton and Dickson voltage multipliers as a function of converstion ratio (20 kV 350 W output)

capacitor count, compared with their full-wave counterparts). This trend coincides with the total energy storied in the capacitors in each topology (Fig. 2-3b). The variations between the weight and the energy can be explained by the discrete nature of the capacitors' energy density.

The process of the weight comparison is illustrated below: we first consider a bipolar (or interleaved) voltage multiplier (VM) – i.e., with its electrical ground at the center point of its output – with each polarity containing n stages to process half of the desired power and voltage. Fig. 2-4 shows an example of a bipolar half-wave CW VM with each polarity containing 2 stages.

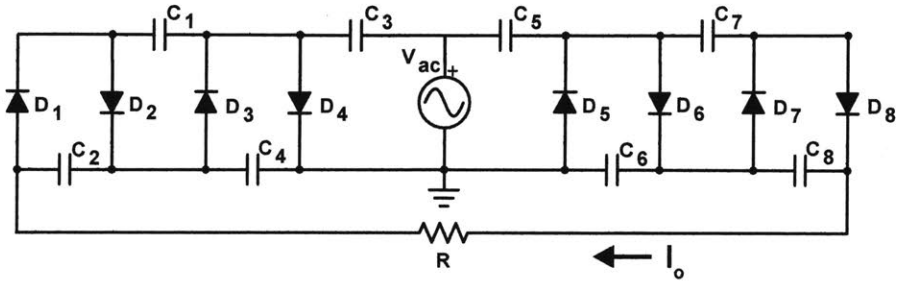


Figure 2-4: A bipolar half-wave Cockcroft-Walton Voltage Multiplier with each polarity containing 2 stages.

Then, we pick a topology and calculate the weight of each capacitor in the selected topology. To do so, we identify the voltage across each capacitor (summarized in Table. D.4), and calculate their capacitances following two specifications below. An assumptions is made to simplify the calculation: in a given topology, all flying capacitors (odd-indexed) are the same and all output capacitors (even-indexed) are the same. For example, in HW CW VM, $C_1 = C_3 = ... = C_{2n-1} \triangleq C_{odd}$, $C_2 = C_4 = ... = C_{2n} \triangleq C_{even}$.

- The even-indexed capacitors (output capacitors) in half-wave topologies are sized such that the voltage ripple is less than 100 V (see Table. 2.1 for the voltage ripple as a function of even-indexed capacitances). For full-wave topologies, if the two half-wave are exactly identical, their ripples would cancel each other and virtually no output capacitors are needed. However, in practice, some capacitances are still desired at the output to account for non-idealities such

as switching transients of diodes. These even-indexed capacitors are sized such that the RC time constant of the effective total output capacitance and the load is 20 times the switching period[5].

- The odd-indexed capacitors (flying capacitors) in all topologies are then sized such that the voltage droop due to the capacitor charge loss (i.e., the losses in the slow-switching limit (SSL) [78]) is less than 2.5 % of 20 kV (5 % for the full converter outputting 40 kV). See Table. 2.1 for the voltage droops as functions of capacitances.

Type	**Voltage gain**	$\mathbf{V_{droop}}$	$\mathbf{V_{ripple}}$
Half-wave CW	$2n$	$\left(\frac{n(n+1)(2n+1)}{6C_{odd}} + \frac{n(n-1)(4n-5)}{12C_{even}}\right)\frac{I_o}{f}$	$\frac{n^2 P_o}{2fV_oC_{even}}$
Half-wave Dickson	$2n$	$\left(\frac{n}{C_{odd}} + \frac{n(n-1)(4n+1)}{12C_{even}}\right)\frac{I_o}{f}$	$\frac{n^2 P_o}{2fV_oC_{even}}$
Full-wave CW	n	$\left(\frac{n(n+1)(2n+1)}{12C_{odd}}\right)\frac{I_o}{f}$	~ 0
Full-wave Dickson	n	$\left(\frac{n}{2C_{odd}}\right)\frac{I_o}{f}$	~ 0

Table 2.1: The voltage gain, voltage droop and output ripple of a n-stage voltage multiplier in the slow-switching limit. I_o is the output current, f is the switching frequency. See the derivation in Appendix. D.1.2.

Then, for each capacitor, we calculate its weight following the linear relationships in Fig. 2-1 and Fig. D-2 with 2 assumptions: 1) the rated voltage of the capacitor is twice its blocking voltage. 2) allow up to 4 discrete capacitors to connect in series and 20 in parallel to achieve the desired blocking voltage and capacitance. Lastly, we sum up the capacitor weight and double it (due to the bi-polar design) to obtain the "total weight" of the VM. The total energy stored in capacitors is calculated in the same fashion. See Appendix. D.1.2 for details of all designs.

[5]The effective total output capacitance is C_{even}/n, which is set to $RC_{even}/n = 20/f, \therefore C_{even} = 20nP_o/(fV_o^2)$, where P_o and V_o are the output power and voltage respectively.

2.1.2 Isolation Stage

Three isolation methods are compared in terms of weight: full-core transformers, air-core resonant transformers and piezoelectric transformers.

Full-core transformers have dominated the isolation stage design in traditional high-voltage converters. A study in [34] for high-power low-frequency transformers (0.1–100 MW, tens of kHz, no voltage insulation requirements were considered) shows the theoretical specific power of transformers roughly scales with its frequency f and power P as $f^{0.75}P^{0.25}$, indicating that specific power improves with higher power.

Air-core resonant transformers (e.g., Tesla coil) eliminate the use of a heavy core and could potentially be light. However, it is a highly tuned structure, sensitive to parasitic inductance and capacitance, and may be relatively large in size [79, 80]. These aspects suggest that it has potential as an approach, but might represent higher risk for an application where both size and weight are important considerations.

Piezoelectric transformers can achieve a power density of 40 W/cm^3 [81], especially suitable for high voltage low power (e.g., tens of watts) applications. They have been used in space applications at below 20 kV and 200 W [82]. However when scaling up in power, one needs to connect existing piezoelectric transformers in series and in parallel and the advantage in power density are gradually exceeded by the cored transformer as power levels rise.

To illustrate these tradeoffs, isolation stages were designed using these methods and the resulting weights were compared, as shown in Table. 2.2. Core-based transformer and Tesla coil were both designed to step up an input voltage of 500 V in amplitude 500 kHz ac to an output voltage of 10 kV in amplitude, delivering 1 kW. The detailed design processes are described in Appendix D.2.

The core-based transformer design uses an ETD49 core with TDK N49 material, 20 turns of AWG17 wire for the primary, 400 turns of AWG31 wire for the secondary. The choice of the insulation material around the secondary wire and the core affects the total weight and the winding's parasitic capacitance. Here we give a lower bound for the total weight of 250 g where glass-filled Nylon 6/6 is used and an upper bound

Type	Rated power (kW)	Rated voltage (kV)	Total weight (g)	Specific power (kW/kg)
Core-based transformer	1	10	250 - 320 †	3.13 - 4
Tesla coil	1	10	135 - 152 ‡	6.57 - 7.4
Piezoelectric transformer	Use STEMiNC SMMTF53P2S40 2W 1.2 kV piece, 9S60P to get 1 kW 10 kV [83]		1080	0.93
	Use Face Transornor 1.5 kV piece, 7S17P to get 1 kW 10 kV [84]		1095††	0.92

Table 2.2: Weight comparison of different isolation stages.
† Bounds correspond to different insulation materials (see Appendix D.2).
‡ Bounds correspond to whether to include a supportive structure (see Appendix D.2).
†† The unit weight is estimated with the same density as [83] and a dimension of $120 \times 8 \times 5.7$mm. Assume 7 in series 17 in parallel to calculate the total weight.

for the total weight of 320 g where glass-filled PTFE is used. The specific power is between 3.13–4 kW/kg. As a comparison, the theoretical equations in [34] suggests 65 g and 15 kW/kg can be achieved, which is far more than realistic (likely due to lack of proper loss modeling at high frequency and insulation design).

The air-core resonant transformer is designed following instructions [79, 80], uses 39 turns of AWG 24 wire for the primary and 820 turns of AWG 29 for the secondary and has a coupling coefficient of 0.6. The windings yields a weight of 135 g and with additional supportive structure, the total weight can reach 152 g and higher. The air-core resonant transformer shows doubled specific power compared with the full-core transformer, but is less efficient. This requires increased weight in the front-end battery packs, making the advantage of coreless less obvious. In addition, it is large in size, less robust in construction and requires narrow-band operation, which makes this option less appealing.

Piezoelectric transformers are designed to provide the same output voltage, 10 kV in amplitude, and output power, 1 kW, by connecting existing piezoelectric transformers from Transonor [84] and STEMiNC [83] in series and in parallel. Since each product works under different input voltages (not 500 V), we leave the input voltage parameter uncontrolled. As an example, we explain the weight calculation using the

STEMiNC part SMMTF53P2S40 (rated for 2 W 1.2 kV output) to achieve 10 kV and 1 kW: we measured the weight of a single off-the-shelf part to be 2 g. Its dimension is 35.8 × 8.8 × 3.8mm, yielding a density of 1.67 g/cm^3 (much lighter than that of the pure PZT-5H material 7.7 g/cm^3 [85]). To achieve 10 kV and 1 kW, we need 9 modules in series and 60 in parallel, yielding a total weight of 1080 g and a specific power of 0.93 kW/kg.

Considering both feasibility and achievable specific power, full-core transformers are compact, robust, and more flexible in use than air-core resonant transformers or piezoelectric transformers at the targeted voltage and power level, so are preferred. In the first prototype dc-dc converter, the transformer is chosen to be center-tapped so that it handles a bi-polar output voltage rather than a unipolar output voltage, which reduces the isolation voltage requirement by half.

2.1.3 Resonant topology selection

High voltage transformers have a large number of secondary turns, resulting in large parasitic capacitances. To usefully incorporate this capacitance into circuit operation, a parallel resonant inverter or a series-parallel resonant inverter is employed. A full-bridge series-parallel resonant inverter is chosen because: 1) it provides a factor of 2 in the voltage gain with negligible weight gain; 2) it shows high efficiency in both light load and heavy load; 3) it has a series capacitor to block dc voltage and thus prevent saturation of the transformer [86, 87].

Based on the constraints above, for the EAD application, a preferred solution for a lightweight high voltage dc-dc converter comprises a series-parallel resonant inverter, a full-core transformer and a multi-stage voltage multiplier. To simplify, we only consider the transformer to have one sectionized secondary in this Chapter. The combination of multi-secondary transformers and multi-stage voltage multipliers may result in more optimal cases, which will be considered in Chapter 4.

2.2 Design Optimization

Different distributions of voltage gains among the inverter, the transformer and the voltage multiplier can result in different overall weights. Section 2.2.1 explains that in our design, the available diodes set the secondary voltage of the transformer, which decouple the voltage multiplier stage from the overall optimization. Section 2.2.2 comprehensively designs the inverter and transformer stages to minimize the total weight of the inductor and transformer while maintaining a good efficiency.

2.2.1 Finalizing the voltage multiplier

In practice, the parasitic capacitance of the high voltage transformer and the junction capacitance of the high voltage diodes are reflected to the transformer primary with a multiple of the square of the turns ratio. This yields a large parallel capacitance in the inverter resonant tank, resulting in large circulating current and lower efficiency.

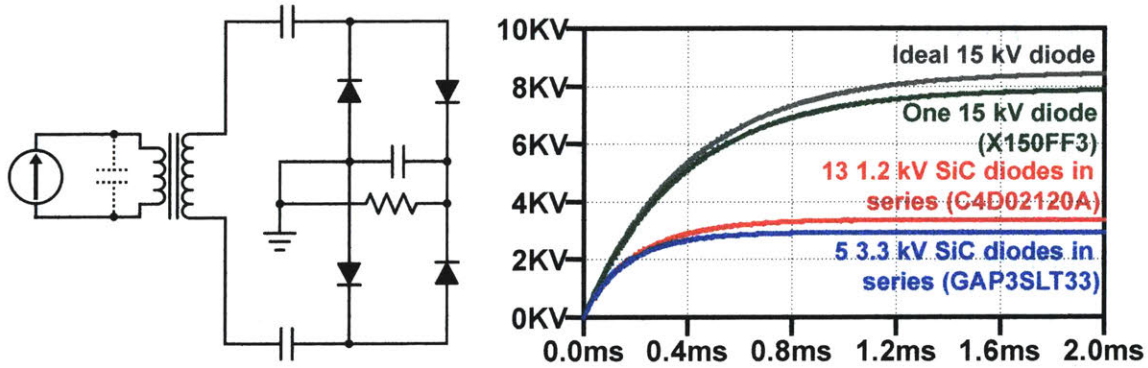


Figure 2-5: (a) Simulation schematics and (b) the output voltage of three single-stage full-wave cockroaft-walton multipliers using three different diodes. In the schematic, the dashed-line capacitor represents the parasitic capacitance reflected to the transformer primary.

Using Cree's C4D02120A, GeneSiC's GAP3SLT33-214 and VMI's X150FF3 respectively, a single-stage full-wave Cockcroft-walton voltage multiplier (VM) is simulated in LTspice (Fig. 2-5a). Each VM is driven by a 500 kHz 0.5 A current source (to simulate the inductor in the series-parallel inverter) and uses the same transformer.

The diode in the VM consists of either one 15 kV X150FF3, or 13 1.2 kV C4D02120A or 5 3.3 kV GAP3SLT33, yielding a diode blocking voltage of ~15 kV. As a reference, a VM with ideal 15 kV diodes that have no forward voltage drop or parasitic capacitance is also simulated.

The simulation results in Fig. 2-5 show that the voltage droop, defined as the difference between the output voltage when using ideal diodes and the output voltages when using investigated diodes, is the lowest with X150FF3 diodes (due to the lower parasitic capacitance). Using multiple SiC diodes theoretically reduces the overall parasitic capacitance, but since their junction capacitance[6] is much larger than that of X150FF3, the simulation still shows unacceptably large droop. In addition, series-connecting multiple SiC diodes can potentially require balance circuits and add more complexity. Therefore, in this Chapter, the X150FF3 is selected as the most effective available diode. To simplify the design, we do not consider connecting multiple of X150FF3 in series as an equivalent higher voltage diode, which sets the output of the transformer to be less than ~7.5 kV (considering a 50% voltage derating).

Referring back to the voltage multiplier weight study in Fig. 2-3a, a 3-stage bipolar (6-stage total) full-wave Cockcroft-Walton voltage multiplier can convert 7.5 kV to 40 kV and yield a light weight. Compared to a 3-stage full-wave Dickson, it requires easier implementation because most flying capacitors have the same capacitances and block the same voltages, thus is chosen.

2.2.2 Weight study of the inverter and the transformer

With the diode and the voltage multiplier topology chosen, the series-parallel inverter and the transformer stages (Fig. 2-6) are to convert V_{DC} = 200 V dc to V_{Sec} = 7.5 kV ac at a switching frequency of f_s =500 kHz. To account for the losses in the voltage multiplier, we design at P_{Sec} = 750 W rather than 700 W. To simplify the weight analysis, we use the Fundamental Harmonics Approximation [86] method to analyze the inverter operation and assume the resonant tank output voltage V_{Pri} to be sinusoidal.

[6]Note these two diodes are already the smallest current-carrying diodes and offer small junction capacitances in the SiC diode family.

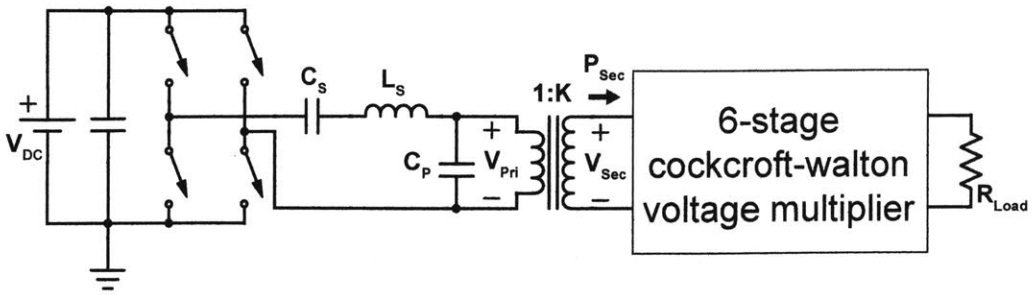


Figure 2-6: The diagram of the inverter and the transformer stages. The resonant tank input is a square wave of amplitude V_{DC} containing no dc component.

The weight of the two stages is dominated by magnetic components, thus the design space of the two stages is explored to minimize the total weight of the inductor and the transformer while maintaining good efficiency[7]. The optimization process contains five steps:

- Select a set of operating variables: the resonant tank quality factor Q, the tank natural frequency f_0, the series and parallel resonant capacitance ratio $A = C_P/C_S$, and the transformer voltage step up ratio K (same as turns ratio). Then the inductance and capacitances of the resonant tank (L_S, C_S, C_P), the tank voltage gain $G = V_{Pri}/V_{DC}$ and the tank current $I_{L_{max}}$ can be calculated (see Appendix D.3 for detailed equations). We keep the sets that yield a transformer output voltage $V_{Sec} = V_{DC} \times G \times K \in [7.5kV, 9kV]$)[8].

- Design the lightest weight transformer that satisfies an input voltage of $V_{DC} \times G$, turns ratio K, output power P_{Sec} =750 W and a set of constraints on efficiency, temperature rise and packing factor. See the detailed design method in Appendix D.3 and Appendix B.

- Design the lightest inductor that has an inductance of L_S and a maximum current of $I_{L_{max}}$ and a set of constraints on efficiency, temperature rise and packing factor. See the detailed design method in Appendix D.3 and Appendix C.

- Sweep all sets of operating variables and compare the sum of the inductor and

[7]The transformer is to be at least 95 % efficient and the inductor is to be at least 98 % efficient
[8]We set K as a free variable to start with because it is used to calculate the tank gain G.

the transformer to find the lightest weight combination. The design space we explored is: $0.2 \leqslant Q \leqslant 10$, $0.1 \leqslant A \leqslant 10$, $450\,\text{kHz} \leqslant f_0 \leqslant 500\,\text{kHz}$, $5 \leqslant K \leqslant 30$.

- Refine the lightest designs by checking the parasitics of the transformer: 1) if the leakage inductance of the transformer is not negligible compared with L_s, then redesign the inductor. 2) if the parasitic capacitance of the transformer is larger than C_P, then sectioning the transformer secondary winding to reduce its parasitic capacitance. Section 2.2.4 explains this in more detail.

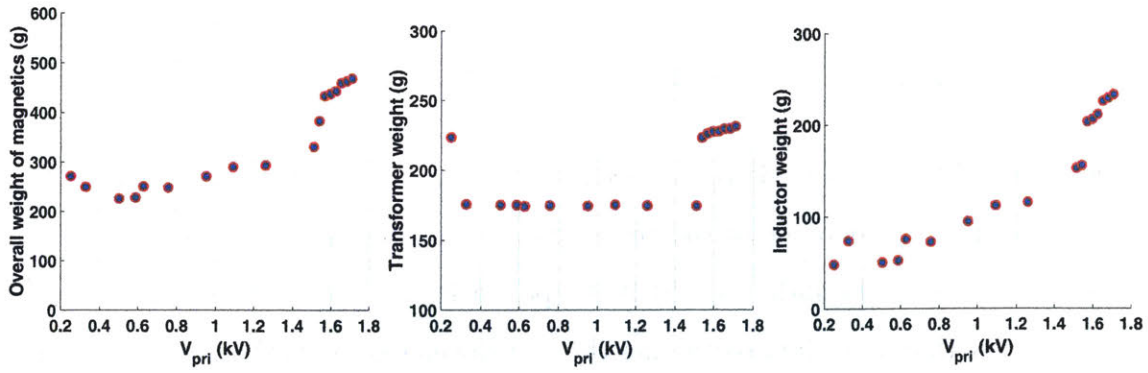
To simplify the study, we consider: 1) center-leg winding on E-type cores for both the transformer and the inductor to ensure good coupling[9]; 2) only off-the-shelf core sizes. Customized cores may yield more optimal designs and will be discussed in Chapter 4; 3) the secondary wire fixed as Teledyne Reynolds AWG28 18 kV FEP insulated wire (P/N 178-5790, this is the smallest gauge high voltage wire we found in a time limited search that offers an insulation voltage above 15 kV. Its voltage rating and gauge size may be conservative for $V_{sec} = 7.5\,\text{kV}$ and $P_{sec} = 750\,\text{W}$ but it provides good design margin).

2.2.3 Optimal weight and voltage gain distribution

In Fig. 2-7, we plot the lightest overall weights of magnetic components and their corresponding inductor and transformer weights against the transformer primary voltages V_{Pri} in the range of 200–1800 V, which is a function of Q, A, f_0, K. The lightest overall weight shows a clearer trend with V_{Pri} than any of Q, A, f_0, K, thus is plotted. Details of the designs corresponding to these lightest weights are included in Appendix D.3 (Fig. D-10 and Table D.9 through Table D.11).

Figure 2-7a suggests the overall weight of magnetic components first decreases and then increases with V_{Pri}. It reaches the lowest when V_{Pri} is around 400–600 V. For this range of V_{pri}, the resonant tank provides a gain of $G \sim 2 - 3\times$ and the transformer provides a gain of $K \sim 18 - 12\times$. A valley point is reached because:

[9]This also makes the leakage inductance of the transformer much smaller compared with L_s



(a) (b) (c)

Figure 2-7: Lightest overall weights of (a) both the inductor and the transformer, (b) the corresponding inductor weights and (c) the corresponding transformer weights against the transformer primary voltages V_{Pri}.

- The weight of the transformer (Fig. 2-7b) first decreases then increases with V_{Pri}. All designs are temperature limited (see Table D.11).

  - When V_{pri} $\leqslant$400 V, larger turns ratio of the transformer requires a larger amount of windings and a bigger core to fit these windings, yielding a heavier weight.

  - When V_{pri} is in 400 V – 1.5 kV, the volt-second on the core keeps increasing, but the transformer weight stays relatively flat because 1) to keep the maximum flux density B_m low, a higher primary number of turns N_p is needed according to (2.1). But higher V_{pri} results in lower turns ratios, yielding unchanged (or even reduced) number of secondary turns, thus the copper volume and weight stay relatively flat.

$$B_m = \frac{V_{pri}}{2\pi f_s N_p A_c} \tag{2.1}$$

    Where N_p is the primary turns and A_c is the core cross-sectional area.

    2) the core volume and weight also remain unchanged because no bigger A_c is needed to balance the increasing volt-second, and similar cores can be used to fit the relatively unchanged winding volume.

  - When V_{pri} $\geqslant$1.5 kV, the volt-second keeps increasing, the original core

height is not enough to fit the increasing amount of primary number of turns N_p, thus a larger core with bigger window height is needed, yielding a heavier weight. All designs yield 1 layer of the primary windings, because more number of layers results in either 1) increasing primary copper loss due to the proximity effect, driving the design over the preset efficiency and/or temperature limits; or 2) thicker winding width, together with the necessary insulations, approaching the core window width.

- The weight of the inductor (Fig. 2-7c) increases with V_{Pri}, especially when $V_{pri} \geqslant 0.8\,\mathrm{kV}$ (corresponding to the tank voltage gain $G \geqslant\sim 5$ and tank quality factor $Q \geqslant\sim 3$). All designs are also temperature limited (see Table D.10). At higher tank gain G, to keep the maximum flux density $B_{L_{max}}$ low (eq (2.2)), more turns and bigger core cross-sectional area are required, yielding to both heavier core and copper weights.

$$B_{L_{max}} \sim C_1 \frac{G}{A_c N_L} \tag{2.2}$$

Where A_c is the cross-sectional area of the inductor core, N_L is the number of turns. C_1 is constant for a given operating condition. See the derivation in Appendix D.3.4.

Figure 2-7a through Fig. 2-7c show discrete simultion results due to our assumptions to use discrete off-the-shelf core shapes and wires, as well as discrete operating variables Q, A, f_0, K. Customized cores and wires as well as finer-meshed variables can yield to a more accurate optimal operating point and a lighter overall weight, as will be discussed in Chapter 4.

For the final design, we pick V_{Pri} to be at $\sim$500 V, the resonant tank Q is $\sim$ 2, the tank voltage gain $G \sim 2.5$ and the transformer turns ratio $K = 15$.

The final converter topology is shown in Fig. 2-8. It comprises a series-parallel resonant inverter, a 1:15 ferrite-cored high voltage transformer and a 6-stage bi-polar full-wave Cockcroft-Walton multiplier. The three stages are designed to give us a voltage gain of $\sim 2.5, \sim 15, \sim 6$ respectively.

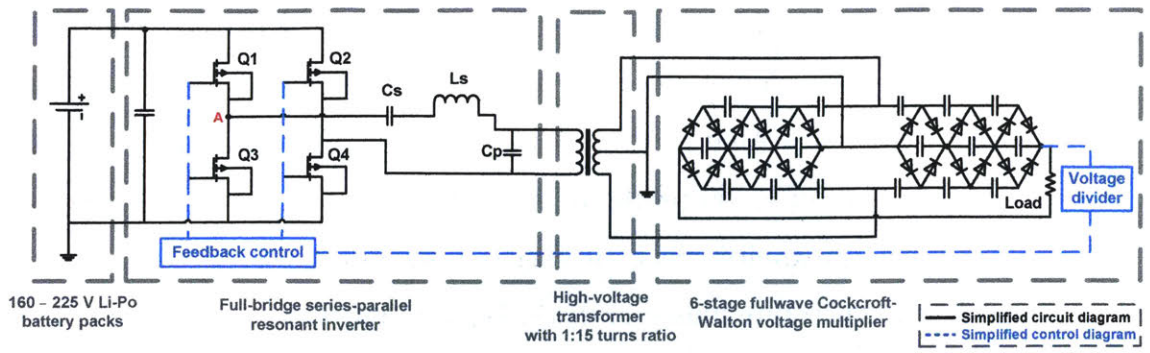


Figure 2-8: Final design of the developed high voltage dc-dc converter. Node A marked in red corresponds to the switching node waveform in Fig. 2-10.

2.2.4 Sectioning the transformer secondary winding

When designing the transformer, an important criterion is to use its parasitic capacitance as part of the parallel resonant capacitance C_p.

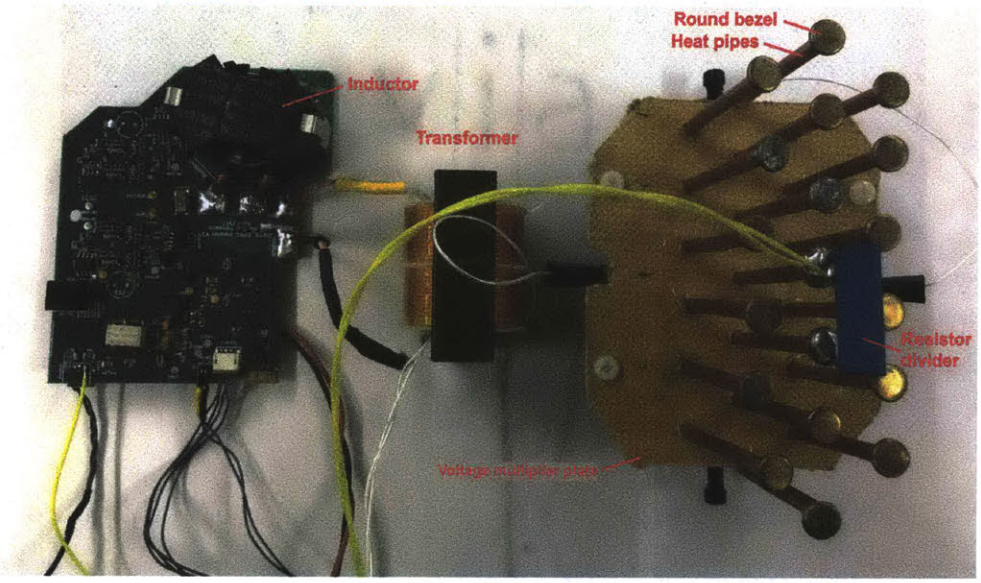
The parasitic capacitance reflected to the transformer primary is dominated by 1) the turn-to-turn and layer-to-layer capacitance of the secondary windings, which increases with the secondary number of turns, the number of turns per layer and the number of layers [88], 2) secondary winding to core capacitance [88] and 3) the diode capacitance in the voltage multiplier reflected to the transformer primary. Due to a large number of secondary turns and a large turns ratio, the parasitic capacitance is usually much higher than needed.

A multi-section secondary is a common solution to reduce the self-capacitance of the winding. A rule of thumb is that with n-sections, the self-capacitance can be reduced to $1/n$ [88]. The winding-to-core capacitance is considered to be not affected by any sectioning. See Section D.3.2 for detailed equations.

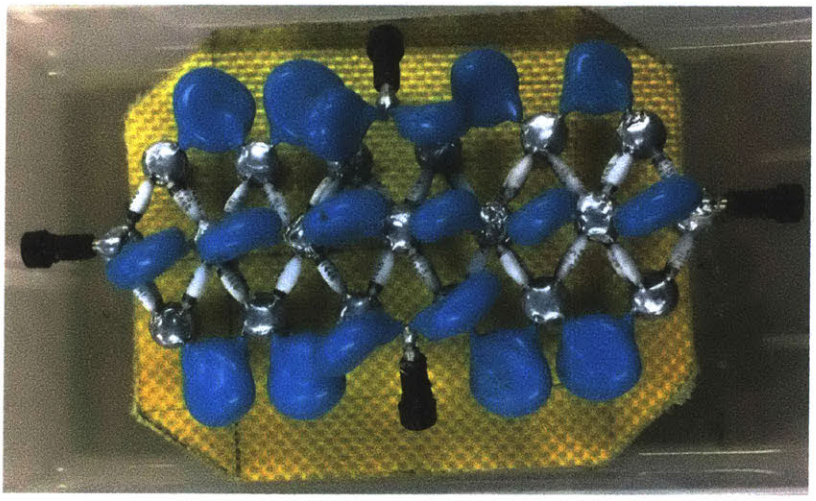
In this study, we consider one multi-section secondary and the section number is swept between 1 and 4. In the final design, the transformer secondary is sectioned into 2 sections. No higher number of sections is needed.

2.3 Experimental results

A prototype converter with closed-loop voltage feedback control based on the optimized design in Fig. 2-8 was built, as shown in Fig. 2-9. All the sensing, control and driver circuits are integrated on the printed circuit board and it needs no additional components other than a logic power supplied by a 3.7 V LiPO battery for the EAD flight demonstrations.



(a)



(b)

Figure 2-9: 200 V to 40 kV high voltage dc-dc converter prototype. (a) Three stages of the converter and (b) top view of the voltage multiplier.

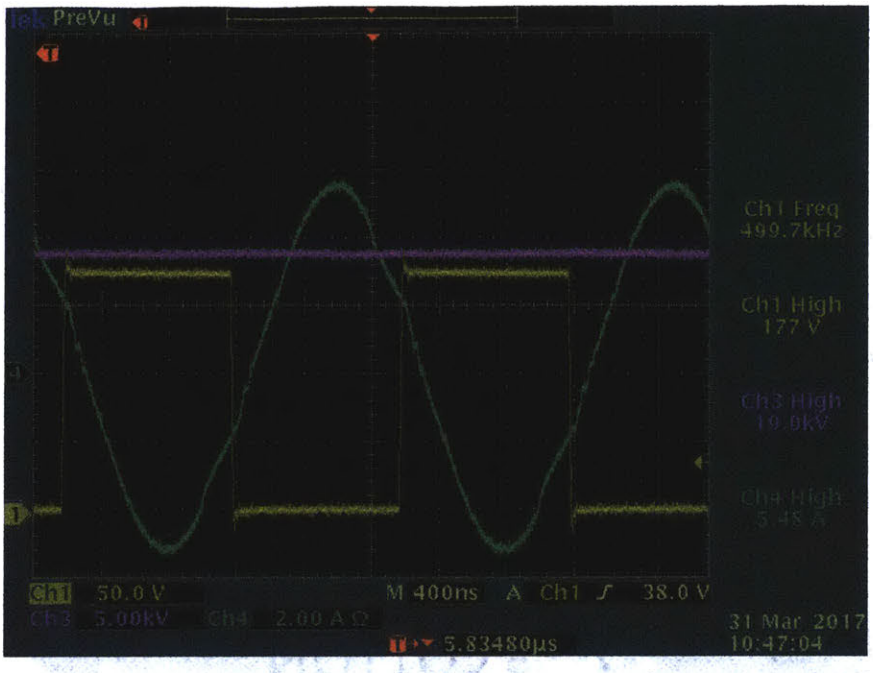


Figure 2-10: Experimental waveforms of the developed high voltage dc-dc converter prototype outputting ~480 W 38 kV (Ch1 (yellow): half-bridge switching node voltage (Node A marked in red in Fig. 2-8); Ch3 (pink): half of the output voltage; Ch4 (green): resonant tank current)

Fig. 2-10 shows the waveforms of the converter running at 500 kHz and converting 177 V to 38 kV at ~480 W.

The converter achieves an efficiency of 83 % at 480 W 38 kV and 82 % at 300 W 40.4 kV. We were not able to push to above 550 W output before the MOSFETs GS66504B overheated. A previous version of the inverter using EPC 2025 MOSFETs were tested at 565 W 39 kV output, achieving 85% efficiency. EPC 2025 went obsolete therefore we switched to GS66504B. See Appendix D.4 for the details of the efficiency measurement and build process of the converter.

The prototype was used to drive electrode thrusters of an EAD aeroplane and demonstrated the first flight of such an airplane. See Chapter. 6 and [1] for details. The finalized component values in the converter[10] and the weight breakdown of the converter are listed in Table 2.3. The prototype achieves a specific power of 1.15 kW/kg (565 W/491 g), meeting the targeted 1 kW/kg.

[10]Since the load power and the battery voltage has changed, the resonant tank passive values have been tuned differently with the original design.

Stage	Component	Manufacturer and Part Number	Value/Description	Weight	Weight % in V2
Inverter	MOSFETs	GaN system GS66504B	-	56 g	11.4%
	C_s	TDK C3216C0G Series	19.6 nF		
	C_p	Parasitic capacitance	~5 nF		
	Inductor L_s†	RM14I core in TDK N49; MWS wire AWG14(150/36)	11 turns, air gap 0.87 mm, 33.2 µH	80 g	16.3%
Transformer	Core ‡	ETD49/25/16, Ferroxcube 3F35		124 g	In total, 170 g. 34.6%
	Primary†	MWS AWG 16 (350/42)	10 turns, 1 layer; Total length 0.52 m; Unit weight 18.45 g/m	9.6 g	
	Secondary†	Teledyne Reynolds AWG28 18kV FEP wire (P/N 178-5790)	150 turns, 2 section. In each section, 5 layer 15 turns per layer; Total length 12.5 m; Unit weight 2.68 g/m.	34 g	
	Bobbin	ABS 3D printed	-	2.4 g	
Voltage Multiplier	C_{odd}	Murata DHR4E4B102K2BB	1 nF. Unit weight 3.3 g. Qty. 12.	40 g	In total, 115.3 g 23.5%
	C_{even}	Murata DHR4E4B681K2BB	0.68 nF. Unit weight 2.3 g. Qty. 6.	14 g	
	Diodes	VMI X150FF3	Unit weight 0.51 g. Qty. 48.	25 g	
	Bezel joints	Metalliferous BR8818	Unit weight 0.8 g with solders. Qty. 19.	31 g	
	Divider	OHMITE SM204RD-0009	100M/100k 1000:1 resistor, 1%	1.7 g	
	Connectors	Pomona Electronics 5936-0 and 5935-0	Unit weight 0.6 g. Qty. 6.	3.6 g	
	Output wire	Teledyne Reynolds AWG22 30kV Silicone coated FEP wire (P/N 178-8781)		-	-
Heat sink	V1: copper pipes	Mcmaster 101 Copper 0.032" Tube Wall, 3/16" OD, 4cm long.	Unit weight 4.6 g. Qty. 19.	89 g	-
	V2: heat pipes	Wakefield-Vette 121686_R EV1. 7mm long 4mm OD.	Unit weight 3.6 g. Qty. 19.	69 g	14%
Total weight of V2 (using heat pipes)				491 g	100%

Table 2.3: Specifications and component weight breakdown of the prototype high voltage power converter. The total weight here does not include that of the supportive structures and the peripheral circuits which are necessary for the flight.
‡ The same core in TDK N49 would yield to slightly lower loss but not available.
† The primary turns is reduced to 10 and the secondary correspondingly to 150 (1:15), compared with the designed 13 and 196 (1:15) due to imperfection in hand-winding and added insulation thickness in the practical construction.

There are two key considerations in construction of the voltage multiplier, which turns out to strongly affect the performance and the weight of the overall system:

The physical layout of the voltage multiplier

The full-wave Cockcroft-Walton topology is by nature symmetric, thus keeping symmetry in the physical layout is desirable for best operation. Other considerations include 1) keeping the leads of the diodes short to minimize their thermal resistance; 2) to avoid corona discharge, keeping each node sufficiently separated from nodes at other potentials and making sure surfaces are sufficiently smooth.

One key design decision made regarding to the physical construction of the VM is to use air-isolated rather than potting. Potting and oil immersion are two popular methods used in building high voltage power converters to provide insulation (oil immersion also increases the heat conduction capability). However, both approaches would add extra mass and a more complex manufacturing process as compared to an air-insulated design (where one is possible). A PDMS-potted (also known as Polydimethylsiloxane, a type of silicone) single-stage VM was built and compared with an air-isolated single-stage VM[11]. At the same input voltage, output voltage and power, the PDMS-potted VM heated up to 74 °C, whereas the air-insulated VM to only 50 °C. Potting also makes diagnosis and repair more difficult. In addition, for a full 6-stage VM, the potting material would add ~30 g of weight. Thus an air-isolated structure was chosen as it can provide adequate insulation and thermal properties with careful design while yielding lighter weight.

Heatsink design for the voltage multiplier

Using Si high voltage diodes at above 500 kHz can significantly increase their switching loss[12] and thus their temperature rise. A single-stage full-wave cockcroft-walton voltage multiplier[13] was built and tested at various switching frequencies[14]. As shown in Fig. 2-11, when switching at 615 kHz without any cooling, the maximum temperature of diodes hits 100 °C at only ~30 W output power (where each diode blocks

[11] PDMS was chosen instead of Epoxy because its lighter weight and easier manufacturing process

[12] [89] indicates as the frequency increases, VMI's diode loss is dominated by the switching loss.

[13] In the following tests, each diode in the VM is two VMI's X150FF3 diodes in parallel. Single diode cases were also tested but yield to even higher temperature rises.

[14] For tests at different frequencies, the load resistance and the resonant tank designs were changed.

6 kV (40% of rating) and carries 2.7 mA (5.4% of rating)). With some heat sinking[15] and still at 615 kHz, the maximum temperature hits 100 °C at ~70 W output power (where each diode blocks 5.4 kV (36% of rating) and carries 14.6 mA (29% of rating)).

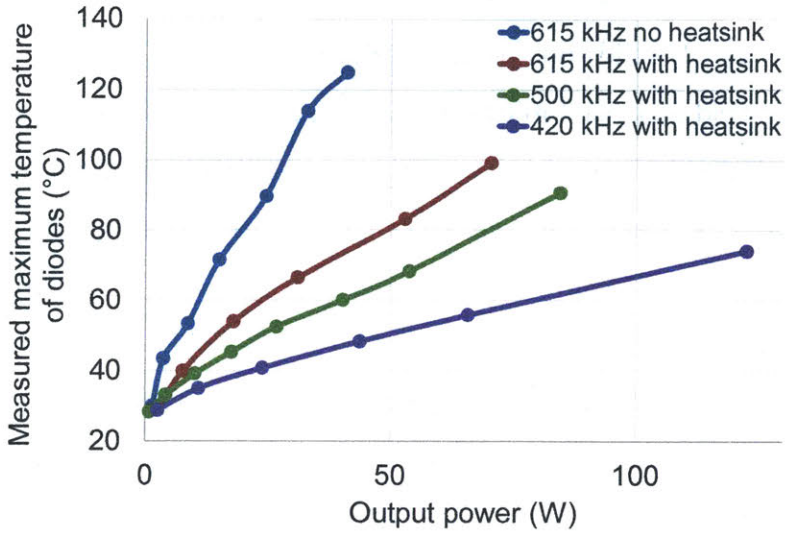


Figure 2-11: Temperature of diodes operating at different frequency in a 1-stage full-wave Cockcroft-walton voltage multiplier.

For the 6-stage VM to process the designed power at 500 kHz, special heatsink for the diodes is required despite the additional weight. A particular challenge of designing such a heatsink is to keep the electric field low to avoid corona discharge between heatsinks or between heatsink and devices.

Copper rods, hollow copper pipes and commercially available cylindrical heat pipes (sealed metal pipes partially filled with heat-carrying vapor) are all considered as the heatsink. Round smooth surfaces of these heatsinks also help to reduce the local electric field. The surface-to-surface distance between the adjacent two pipes are set by the length of the diode package to minimize the thermal resistance from diode junction to the heatsink. Rods and hollow copper tubes are easy to machine, flexible in the tube diameter, but heavier compared with heat pipes (machinable copper tubes usually has a thicker wall thickness compared with the heat pipes), whereas off-the-shelf heat pipes are only offered in several diameters and lengths, but lighter and potentially have better heat transfer.

[15] 1/16" OD 5 cm long copper pipes soldered at joints of the voltage multiplier.

FEA thermal analysis (Fig. 2-12) in Solidworks for pipes with different length, diameter and wall thickness reveals that 1) there is an optimal weight of the pipes providing the best trade-off of heat transfer and mass. Further increasing the weight (either by elongating or enlarging) does not seem to result in a justifiable reduction in the temperature. 2) solid rods seem not effective and add additional weight.

FEA electric field analysis (an example shown in Fig. 2-13) in Quickfield for pipes with different diameters reveals that the strongest electrical field appears on the two ends of the VM, where the voltage is the highest. It needs to be kept below approximately 10 kV/cm (1 MV/m), as a conservative rule of thumb to avoid corona.

Eventually, two versions of the voltage multipliers (VMs) with different heatsink designs were built: version 1 was with hollow copper pipes (Mcmaster 101 Copper 0.032" Tube Wall, 3/16" OD, 4 cm long), yielding a heatsink weight of 90 g and a maximum temperature in the VM to be ~70 °C at an output of 565 W 39 kV; version 2 was built with off-the-shelf heat pipes (Wakefield-Vette 121686_REV1, 7 mm long 4 mm OD), yielding a similar temperature rise in the VM but a 20 g weight reduction. Version 2 was used in the flight demonstrated in Chapter 6.

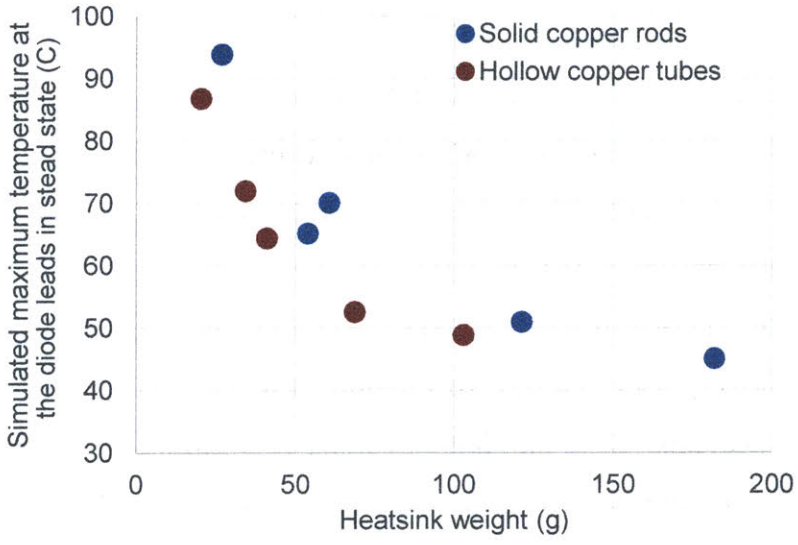


Figure 2-12: Thermal simulation: maximum temperature at the diode leads in steady state against the heat sink weight.

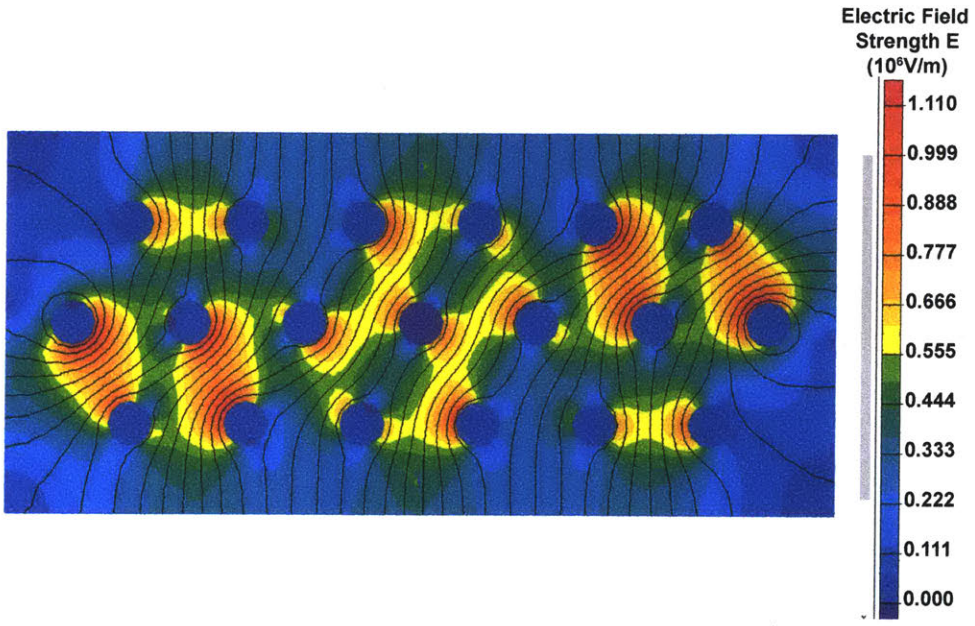


Figure 2-13: An example electric-field simulation of the voltage multiplier structure (each diode blocks 7.5 kV and the heat sink diameter is 3/16").

Chapter 3

Evaluation of High Voltage Diodes and Series-Diode Balancing

As mentioned in Chapter 2, miniaturization of high voltage power converters motivates increasing switching frequencies from a few hundred kHz and below to the high hundreds of kHz and MHz range. One of the bottlenecks to achieving high frequency at high output voltage while preserving high efficiency is the lack of low-loss high-voltage diodes capable of operation at high frequency [74, 90].

Si Schottky diodes are appealing in high frequency applications but they are mostly rated below 250 V [91]; commercially available Silicon Carbide (SiC) Schottky diodes exhibit low loss and can block up to 3.3 kV; however, above 5 kV, the only presently affordable and available diodes are Si high-voltage diodes [91]. These diodes have rarely been used in the high hundreds of kHz and MHz range, and have not been characterized for operation at such frequencies.

To better explore the range of diodes that might be useful in such applications, we have tested a range of diodes (from 400 V to 15 kV) in a full-bridge rectifier topology at 600 kHz and 1 MHz. The evaluation results are shown in Section 3.1. Most of the tested Si high voltage diodes are not suitable for operation at or above 600 kHz at even a fraction of their ratings without heat sinks. Nonetheless, low voltage fast recovery diodes (400–600 V) and SiC Schottky diodes (650 V to 3.3 kV) are promising candidates for building high-voltage, high-frequency systems.

One can use such high-frequency, low-loss low-voltage diodes in various ways to achieve a high-voltage output. One can (1): have multiple transformer windings or multiple resonant tanks that are separately rectified and stacked in series (e.g., [92–94]); (2): Use the diodes in voltage multiplying rectifier topologies (e.g., [74, 95–98]); and/or (3): Series connect discrete low-voltage diodes to construct an approximate equivalent to a high-voltage diode (e.g., [99]).

Each method has limitations: the losses of a voltage multiplier increase drastically with the number of stages [96, 100]. The complexity (and often-times the loss) of a transformer increases with more secondaries as does its nonideality of operation, especially when high insulation levels are needed between outputs. Series connection of devices leads to questions about how the individual devices actually act, and the impact on their voltage sharing during the off-state and their losses owing to switching and conduction.

Section 3.2 explores design considerations in the use of series-connected low-voltage diodes as a single high voltage diode for high-frequency applications. We observe that there are serious off-state voltage and temperature imbalance issues that can arise when series-connecting such diodes. We present a theoretical model showing that significant voltage imbalance and loss differences can be caused by parasitic capacitances to common of the diode interconnection points.

Section 3.3 describes two related compensation techniques to mitigate voltage imbalance and loss owing to these interconnect capacitances. The proposed techniques function by adding external low-loss capacitors to restore voltage balance and reduce diode losses. We present analytical solutions as well as theoretical limitations of these techniques. To validate the approaches, a full-bridge rectifier is tested with each branch consisting of four 3.3 kV SiC diodes in series. Experimental results in Section 3.4 showcase the imbalance and demonstrate the effectiveness of the compensation techniques. The proposed technique and evaluation results will be valuable for the design of lightweight and miniaturized high voltage power converters.

3.1 Thermal Characterization of High Voltage Diodes

To identify suitable diodes operating at high voltage and high frequency, we tested 37 off-the-shelf diodes in a full-bridge rectifier topology. We use "maximum temperature rise in the rectifier" as a metric to evaluate the diodes in all tests for two reasons: (1) the temperature rise correlates well with power losses and can be measured in a non-intrusive way; and (2) the maximum temperature rise data can be used to decide whether cooling devices (e.g., heat sinks) are needed, which is an important factor in realizing miniaturized and lightweight designs.

We conducted tests from three perspectives:

- Compare diodes when a single diode is used within a fixed range of voltage and current de-rating factors. We refer to these tests as "single diode tests".
- Compare across selected diodes when multiple diodes are connected in series as a single higher-voltage diode to meet a given blocking voltage requirement. We refer to these tests as "multi-diode tests".
- Repeat and compare the above tests at 600 kHz and 1 MHz while holding other test conditions constant.

The diodes under test include Si fast recovery diodes (both low voltage and high voltage) and SiC Schottky diodes. The nominal blocking voltages of these diodes range from 400 V to 15 kV, and the nominal average forward currents range from 30 mA to 5 A. All tests start at room temperature 25–28 °C and the temperature of the hottest spot in the rectifier is recorded to calculate the "maximum temperature rise". The specifications of diodes, the details of all test conditions, experimental setup and error estimations are explained in Appendix E.1 and Table E.2.

3.1.1 Single diode tests

Test conditions

In single diode tests, each leg of the full-bridge rectifier consists of a single diode. The rectified dc voltage is 45–50 % of the nominal diode rated voltage and the rectified dc

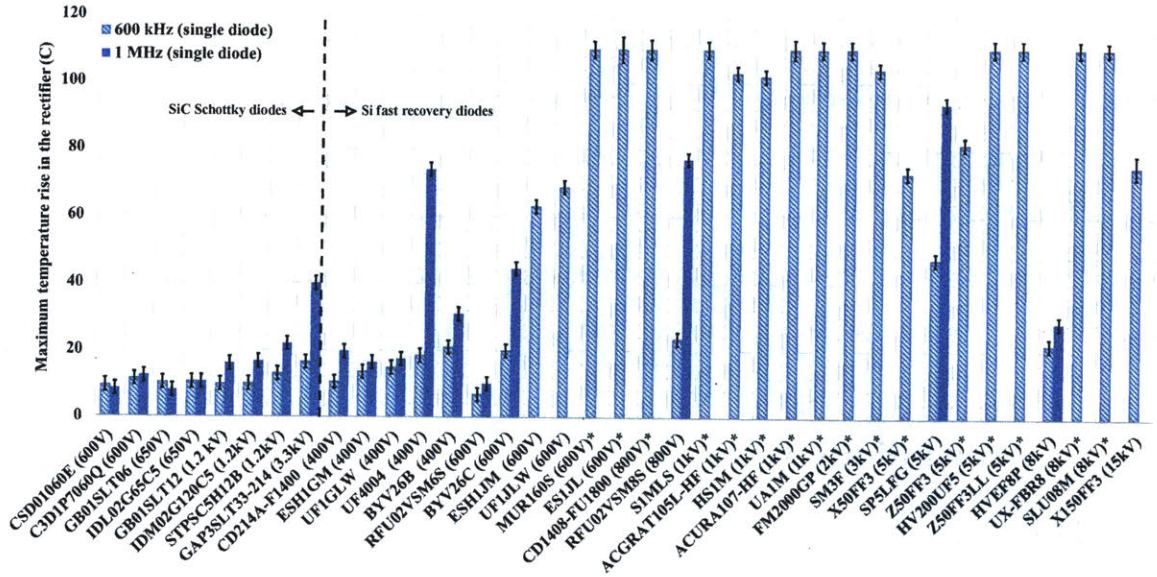
current is approximately 10–20 % of the nominal diode rated current (which means that the average diode current is 5–10 % of its nominal rated dc current). When testing the same diode at two different frequencies, the rectified dc voltage and the dc current are kept the same. Diodes listed without an asterisk were tested for 10 min such that they reached thermal equilibrium and the maximum temperature rise on the rectifier was recorded; diodes listed with an asterisk did not reach thermal equilibrium before the temperature became too high, these tests were cut off earlier when the maximum temperature rise in the rectifier reached roughly 100 °C.

Results

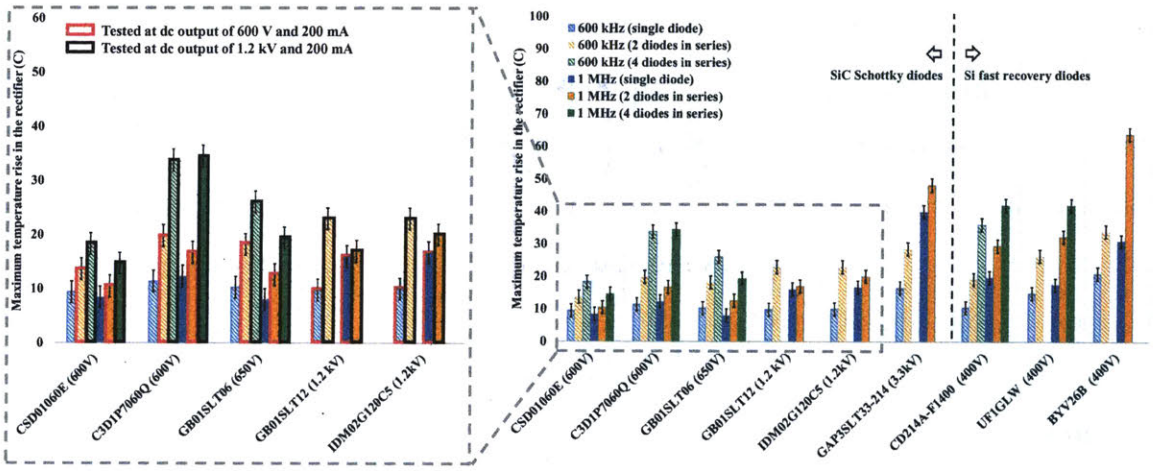
Figure 3-1a shows the maximum temperature rise results of the single diode tests (Table E.2 in Appendix E.1 shows full specifications of the diodes under test and the test conditions). The results reveal that at 600 kHz, SiC Schottky diodes (650 V to 3.3 kV) and several low voltage Si fast recovery diodes (400–800 V) show significantly lower maximum temperature rises compared to most high voltage Si fast recovery diodes (3–15 kV). One exception is an 8 kV diode (HVEF8P), which is tested at ~4 kV output voltage and ~5 mA average output current. It shows promise when used at high frequency for high-voltage low-current applications.

For diodes with a maximum temperature rise lower than ~80 °C, we further characterize the diode losses themselves. This is accomplished using dc signals to develop measured relations between diode dissipation and maximum temperature rise. The details are explained in Appendix E.1 and it is concluded that the maximum temperature rise and the total diode losses are closely correlated as expected.

Three aspects that could contribute to the higher losses and higher maximum temperature rises shown in most high-voltage Si fast recovery diodes are: (1) the conventional ways to boost the blocking voltage (e.g. multi-junction, single deep-diffused junction, or glass passivated) raise the forward voltage of the diode, proportionally increasing the conduction losses; (2) as the off-state voltage increases, the switching losses tend to increase rapidly; (3) higher blocking voltage introduces larger leakage current [101], resulting in more severe heating thus even worse tolerance of losses [89].



(a)



(b)

Figure 3-1: Maximum temperature rise in the rectifier when diodes are tested in a full-bridge rectifier topology at 600 kHz and 1 MHz in **(a)** single diode tests and **(b)** multi-diode tests.

Figure 3-1a also suggests that increasing the switching frequency from 600 kHz to 1 MHz in general increases the temperature rise, however, the magnitude of the increment varies case by case and shows no obvious trends. Among those that show promises in the 600 kHz tests, the 3.3 kV SiC diode (GAP3SLT33) and several Si fast recovery diodes (UF4004, BVY26C, and RFU02VSM8S) show significantly higher maximum temperature rise at 1 MHz, suggesting that the total losses of these diode in the frequency range of interest are dominated by switching losses. As listed in Table E.2, these diodes have a non-zero "reverse recovery time" or "switching time", which helps explain the increased switching losses at high frequency even in the case of SiC schottky diodes.

3.1.2 Multi-diode tests

Test conditions

In multi-diode tests, each leg of the rectifier consists of multiple diodes connected in series. The rectified dc voltage is 45–50 % of the rated voltage of the leg and the rectified dc current is approximately 10–20 % of the diode rated current (which means that the average diode current is 5–10 % of its nominal rated dc current). Each test lasted 10 min and the maximum temperature rise in the rectifier was recorded. As with single-diode tests, when testing the same combination across frequencies, the rectified dc voltage and current are kept the same.

Results

Figure 3-1b presents the maximum temperature rise results of the multi-diode tests (Table E.2 in Appendix E.1 shows full specifications of the diodes under test and the test conditions). The results suggest that for both Si fast recovery diodes and SiC Schottky diodes, connections of more diodes in series lead to higher maximum temperature rises of the diodes, even though their nominal carrying and blocking requirements stay the same. This presents a challenge when using series connections of low-voltage diodes to realize "high-voltage equivalent" diodes in high voltage

applications. For example, looking across tests with 1.2 kV and 200 mA dc rectifier output, 4 GB01SLT06 diodes in series presents higher maximum temperature rise than 2 GB01SLT12 diodes in series, even though in the single diode tests GB01SLT06 performs better than GB01SLT12.

As will be explained in the next section and demonstrated in the experimental results in Fig. 3-8, the maximum temperature rises in the multi-diode tests are usually at the diodes closer to the ac node. In Section 3.2, we explore the causes of the increased "maximum temperature rise" when multiple diodes are connected in series. Owing to both the increased losses and poor voltage sharing, additional efforts are required if high-performing low-voltage diodes are to be series connected and utilized for high-voltage rectification at high frequency. We introduce compensation means for addressing these challenges in Section 3.3.

3.2 Challenges when series connecting diodes

Series connection of diodes to attain higher effective blocking voltages is well known, and issue of voltage imbalance due to the variation among diodes has been observed [102]. The common solution is to parallel balancing resistors with the diodes to ensure that each diode reaches the same dc state [102]. This static "resistive" balancing approach may be most effective for low switching-frequency conditions (i.e., where off-state times are long as compared to the RC time constants involved). Here we identify that the net effective parasitic capacitance to common at the connection nodes between the diodes also contributes to voltage imbalance and to increased loss. The effect of these capacitances becomes increasingly important as operating frequency rises, and becomes a major consideration in achieving high performance at the high operating frequencies considered here.

3.2.1 Parasitic capacitance causing voltage imbalance

Figure 3-2 shows a circuit diagram of a full-bridge rectifier. Each branch consists of M series-connected diodes $D_1, D_2, ..., D_M$. Each node has its parasitic capacitances

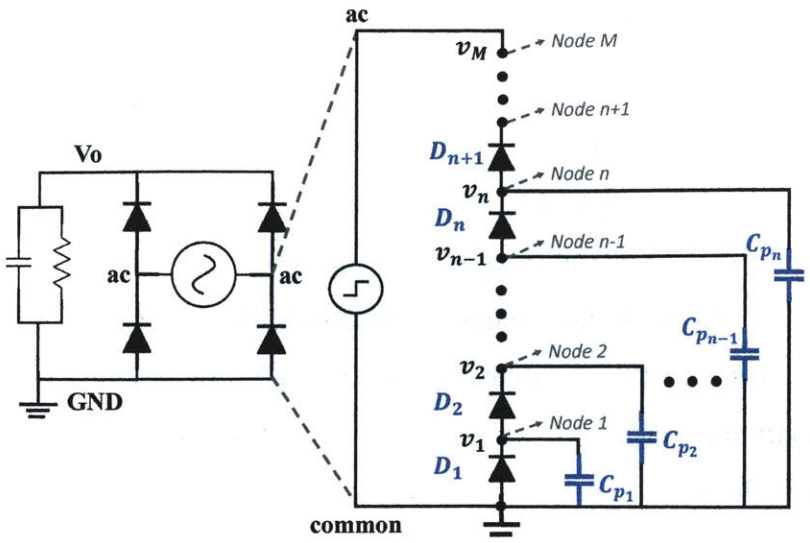
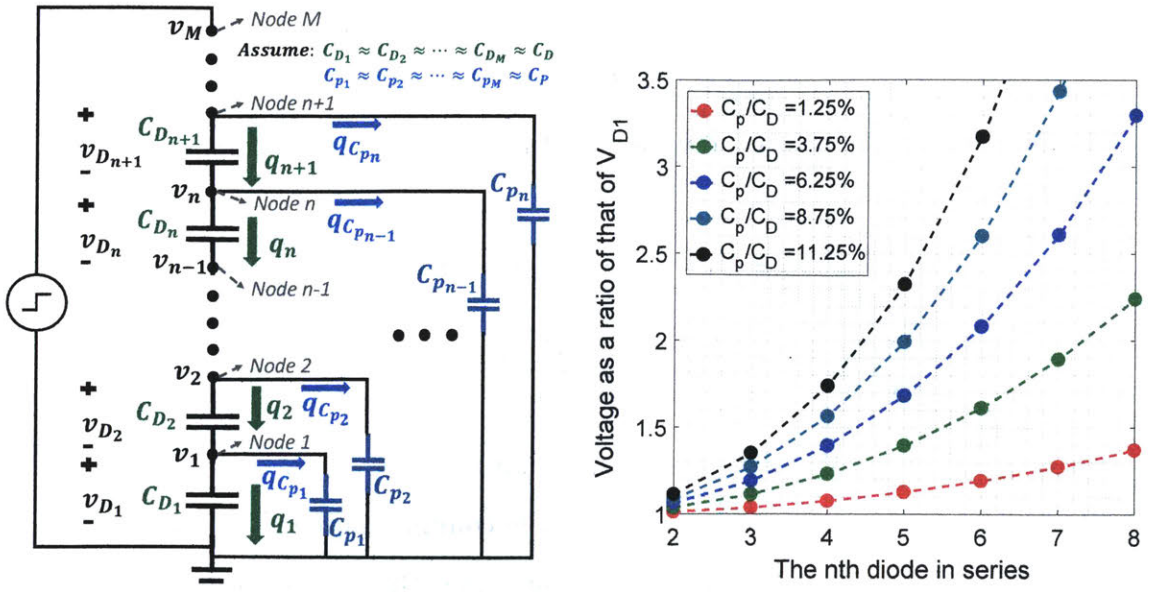


Figure 3-2: Circuit model of multiple diodes connected in series as a single diode, showing a net parasitic capacitance from each node to common.

to the ac node and to a common node (referring to a node with fixed dc voltage with respect to ground, in this case either the ground or the high voltage dc output). For a high-frequency, high-voltage application, one usually minimizes the area of the ac node to prevent the ac noise from coupling to other nodes, and/or implements grounded shielding around the circuits. In practice, these techniques usually yield a significantly larger capacitance from the diode interconnections to common than that to the ac node. Therefore we simplify the parasitic capacitance at each node as a net capacitance to common, shown as $C_{p1}, C_{p2}, ..., C_{pM}$ in Fig. 3-2. These capacitances sink or source charge from each node.

At high frequencies, the voltage distribution among diodes is mostly determined by the capacitances. As a first order analysis, we assume each diode has the same capacitance C_D across it (this includes the diode junction capacitance and the parasitic capacitance between the two nodes to which the diode is connected). We likewise assume the net parasitic capacitance from each diode connection node to common has the same value C_P. Thus we simplify Fig. 3-2 to Fig. 3-3a.

In the following analysis, we consider an incremental increase in the source voltage applied between the ac node and common; this increment will inject an incremental amount of charge into the diode chain.



(a) (b)

Figure 3-3: Simplified ac circuit model for multiple diodes connected in series and the voltage ratio due to the presence of net parasitic capacitances from each node to common. **(a)** Simplified ac circuit model of Fig. 3-2 at high frequencies. **(b)** Voltages across the nth diode as a ratio of that across the 1st diode.

To charge the voltage v_{D_1} at Node 1 from zero to v_1, the charge going through the parasitic capacitance of D_1 (C_{D_1}) is $q_1 = v_1 C_D$, and the charge going through C_{p_1} is $q_{Cp1} = v_1 C_P$. Since both charges come from D_2, the charge going through the parasitic capacitance of D_2 (C_{D_2}) is $q_2 = q_1 + q_{Cp1} = v_1 C_D + v_1 C_P$. If we want $V_{D1} \approx v_{D2}$, we must make sure $q_2 \approx q_1$, thus $q_1 \gg q_{Cp1}$ (equivalently $C_D \gg C_p$).

To generalize, at Node N, $q_n = v_{Dn} C_D$ and $q_{Cpn} = v_n C_P$. If we want $v_{Dn+1} \approx v_{Dn} \ldots \approx v_{D1}$, or equivalently $v_n \approx n v_{D1}$, we must make sure $q_n \gg q_{Cpn}$, equivalently $C_D \gg n C_p$. To provide approximate voltage balancing among the diodes, we require $C_D \gg n C_p$. As any of n increases, C_D decreases, or C_P increases, this constraint becomes more difficult to meet. In practice, this constraint often cannot be met, resulting in voltage imbalances among the diodes. Intuitively, the diode closest to the ac node needs to carry all the charge going down the diode chain and that going through all the parasitic capacitances. If all diodes are identical (and thus have identical capacitances), then this diode passes more charge through its capacitance C_D than diodes below it, and thus needs to block higher voltage. (As shown in

Fig. 3-3a, $v_{D_i} = C_D \times q_i$, because $q_1 > q_2 > ... > q_M$, we have $v_{D_1} > v_{D_2} > ... > v_{D_M}$).

As shown in Appendix E.2, a closed form expression for the n-th diode voltages in Fig. 3-3a in terms of the bottom diode voltage v_{D1} can be found as:

$$\frac{v_{Dn}}{v_{D1}} = \frac{1}{\sqrt{a(a+4)}} \left\{ \left(\frac{a+2+\sqrt{a(a+4)}}{2} \right)^n \left(\frac{a+\sqrt{a(a+4)}}{2} \right) - \left(\frac{a+2-\sqrt{a(a+4)}}{2} \right)^n \left(\frac{a-\sqrt{a(a+4)}}{2} \right) \right\} \tag{3.1}$$

where $a = C_P/C_D$. We plot these voltages for different values of C_P/C_D in Fig. 3-3b. It can be seen that the diode closest to the common potential blocks the lowest voltage, and as the number of series diodes increases, the off-state voltage imbalance increases; in addition, when C_P/C_D gets bigger, the voltage imbalance gets worse.

The voltage imbalance suggests the switching loss among diodes is also imbalanced: the diodes closer to the ac node must carry higher capacitive switching currents and are charged/discharged to larger off-state voltages and thus exhibit higher loss. In stating this, we recognize that the currents carried through diode capacitances (and associated device voltage swings) induce significant loss in the diodes. These losses may be due to joule heating and/or may represent other loss phenomena, as observed with capacitance losses in other device types [103–105]. Based on this, if each diode has a similar thermal path to ambient, then diodes closer to the ac node would show higher maximum temperature rises as well as higher off-state voltages than diodes closer to a dc potential. The experimental results "before compensation" in Fig. 3-8 and Fig. 3-9a in Section 3.4 demonstrate this predicted voltage and temperature imbalance.

3.3 Compensation techniques for achieving voltage balance

With the series diode connection, the charge going through each diode is different due to the presence of parasitic capacitance to the external environment at each connection

node, Moreover, additional losses are introduced owing to the lossy nature of the device capacitances carrying the currents associated with these external parasitics. We can redistribute the charge flows through the diodes and mitigate some of the associated voltage imbalances and losses by adding low-loss external capacitors. Two related compensation techniques are proposed in this section.

3.3.1 Independent compensation

Figure 3-4a illustrates the first compensation technique, which we refer to as "independent" compensation. Taking Node 1 as an example, C_{p_1} draws charge from the node having voltage v_1. Instead of providing this charge $q_{C_{p_1}}$ from D_2, we can inject the charge directly to Node 1 through an additional capacitor C_{c_1} connected between Node 1 and the ac node. In this way, we guarantee $q_1 = q_2$ thus $v_{D1} = v_{D2}$. The amount of charge needs to be injected as the diode voltage charges from zero to its final off-state value v_1 is $q_{Cp1} = v_1 C_P$. Since, after compensation, C_{c_1} blocks $(M-1)v_1$, where M is the number of series-connected diodes (assuming after adding the compensation, all diode voltages balance), the required capacitance of C_{c_1} is $\frac{1}{M-1}C_P$. Similarly for Node n, we can inject the charge directly from the ac node to the nth parasitic capacitance through C_{c_n}.

These additional compensation capacitors solely provide charge to the corresponding parasitic capacitance, and can be independently adjusted. Their values are calculated as below.

$$C_{c_1} = \frac{1}{M-1}C_P, ..., C_{c_n} = \frac{n}{M-n}C_P, ..., C_{c_M} = (M-1)C_P \tag{3.2}$$

The lower and the upper bound of the compensation capacitances are $\frac{1}{M-1}C_P$ and $(M-1)C_P$ respectively. As M increases, the lower bound decreases approximately inversely with the number of series-connected diodes and is eventually limited by the smallest physical capacitance that one can accurately implement; the upper bound increases approximately linearly with the number of series-connected diodes and is limited by the increased losses and the load regulation effect associated with the total

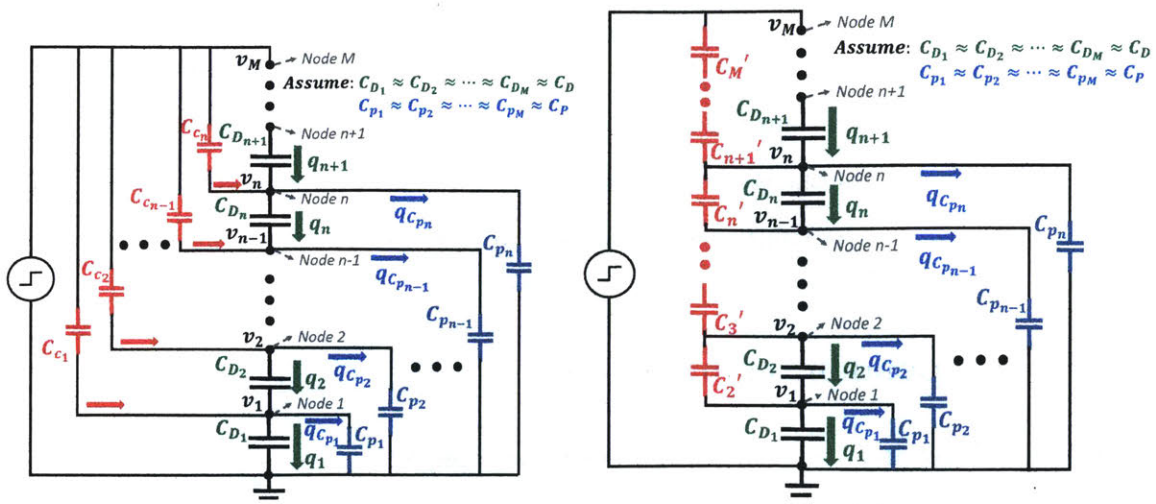


Figure 3-4: Circuit diagram of two related compensation techniques **(a)** Independent compensation: adding compensation capacitors to each node. **(b)** Coupled compensation: adding compensation capacitors across each diode.

capacitance between the ac node and common [106]. A benefit of this technique is that each compensation capacitance may be selected/adjusted based on the voltage distribution impact at a single node. At the same time, each of the compensation capacitances blocks a different voltage making their implementation more cumbersome.

3.3.2 Coupled compensation

An alternative compensation approach is to add a low-loss capacitor across each diode to carry the charge for the parasitic capacitances. A benefit of this implementation, which we refer to as "coupled" compensation, is that each compensation capacitor blocks the same voltage; a disadvantage is that the charges going through them (and the capacitor values) are coupled. All the charges are carried by the top compensation capacitor, and they trickle down the chain to each parasitic capacitance. Consequently, the value of each compensation capacitor is a function of the parasitic capacitances of all of the nodes down the chain.

The capacitance of each compensation capacitor is calculated and listed in (3.3). C_n' provides the sum of charges for $Q_{C_{p_1}}$, $Q_{C_{p_2}}$,..., $Q_{C_{p_{n-1}}}$. Since $Q_{C_{p_i}} = iV_1C_P, i =$

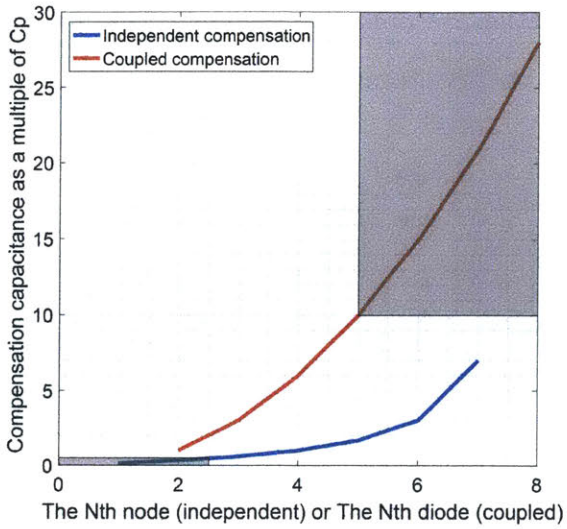


Figure 3-5: Compensation capacitance required at each node normalized to parasitic capacitance C_P. The compensation capacitance required at any node should not be too small, as limited by the physically realizable capacitance, nor too big, as limited by the physical capacitor size and parasitics. These limits are conceptually illustrated by the two gray areas.

$1, 2, ..., n-1$, the sum of the charges is

$$V_1[C_P + 2C_P + ... + (n-1)C_P] = \frac{n(n-1)}{2} V_1 C_P$$

Therefore

$$C'_n = \frac{n(n-1)}{2} C_P$$

$$C'_2 = C_P, ..., C'_n = \frac{1}{2}n(n-1)C_P, ..., C'_M = \frac{1}{2}M(M-1)C_P \tag{3.3}$$

With coupled compensation, the largest required capacitance increases quadratically with the number of diodes in series.

3.3.3 Comparison

Figure 3-5 shows the compensation capacitances needed for each node or each diode in the two compensation implementations. One limiting factor in practical realizations is that a given compensation capacitance should be neither too small nor too large

for practical implementation, as illustrated qualitatively with the two gray areas.

The total capacitive energy storage is identical in either implementation:

$$E_{independent} = \sum_{1}^{M} \frac{1}{2} C_{c_n} V_{C_{cn}}^2 = \frac{C_P V_1^2}{2} \sum_{1}^{M} n(M-n)$$

$$E_{coupled} = \sum_{1}^{M} \frac{1}{2} C'_n V_{C'_n}^2 = \frac{C_P V_1^2}{2} \sum_{1}^{M} \frac{n(n-1)}{2}$$

$$E_{independent} = E_{coupled} = \frac{C_P V_1^2}{2} \frac{M^3 - M}{6}$$

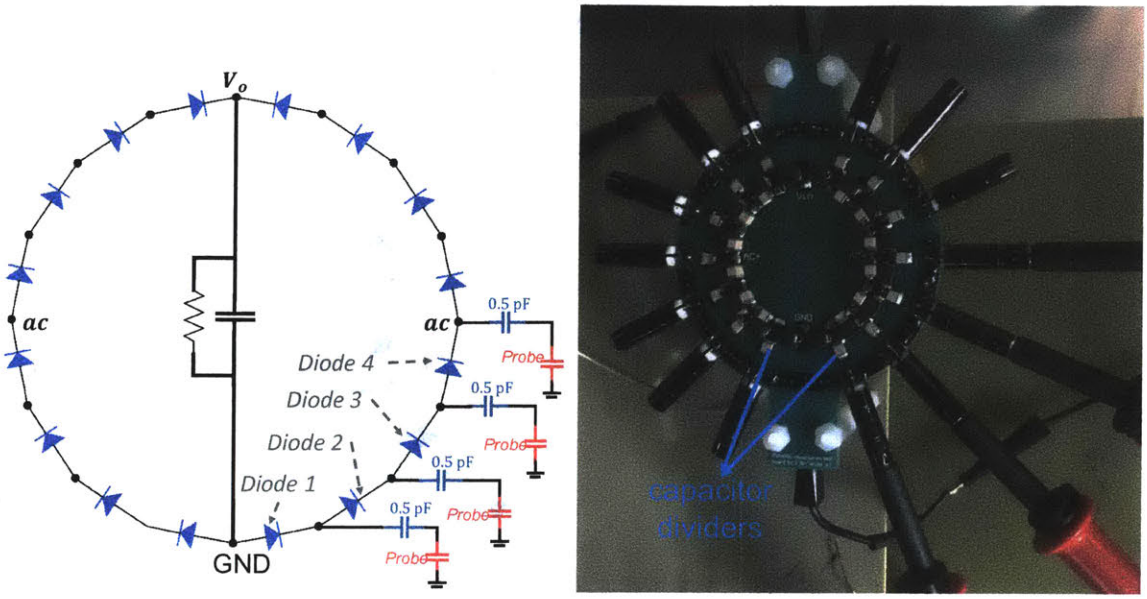
However, the facility with which such injection can be implemented with available components or PCB structures (in terms of capacitance values and voltages) will determine the best method to select in a given application. The independent method requires smaller capacitances but higher voltage rating of each compensation capacitor (one could use low-voltage capacitors in series, but it adds complexity in the physical layout of these capacitors). In the coupled method, each compensation capacitor is rated at the same voltage, but higher capacitances are required for larger number of stages. Often, the coupled compensation is easier to implement with discrete components or by PCB design.

In practical applications, the parasitic capacitances $C_{p_i} (i = 1, 2, ..., M)$ may not be equal as assumed above. However, the concept remains valid and the compensation capacitances can be calculated for the general case as well. See Appendix E.3 for the detailed derivation of the compensation capacitances in the general case.

3.4 Experimental results

3.4.1 Setup and measurement techniques

The experimental setup is shown in Fig. 3-6. Four 3.3 kV GeneSiC diodes (GAP3SLT33-214) are connected in series for each leg of a full-bridge rectifier. The rectifier is driven from a custom-built inverter and high-voltage transformer with an approximately trapezoidal voltage waveform at 600 kHz. The rectifier outputs 3.6 kV and



(a) (b)

Figure 3-6: The full-bridge rectifier circuit for testing the compensation techniques. **(a)** measurement diagram showing divider capacitors and probes. **(b)** a photograph of the experimental test board.

20 mA (P_o =72 W) into a resistive/capacitive load. The details of the driving circuit and the load are described in Appendix E.1. We measure the voltages at four nodes on one leg of the rectifier using four Teledyne LeCroy PPE4KV probes, as shown in Fig. 3-6b. For sensing, we add a 0.5 pF NP0 capacitor at each node as a divider capacitor to reduce the effect of the probe capacitance on the voltage distribution. We also add a capacitor divider and a probe adapter at all other nodes to minimize the differential effects of the probes at the four measurement nodes. By subtracting the voltage readings from four probes, we obtain four voltages that are proportional to the ac component of voltages across Diodes 1 to 4. In terms of voltage balancing, we only care about the ratio of these voltages instead of their absolute values. The 0.5 pF NP0 capacitor (C_{NP0}) and the probe capacitance (C_{Probe}) form a capacitor voltage divider. We note the probe reading as V_{Probe} and the corresponding node voltage as V_{node}, then $V_{node}/V_{probe} = C_{Probe}/C_{NP0}$. The probe capacitance is estimated to be 10.5 pF, the sum of 6 pF from the PPE4kV probe and 4.5 pF from the probe-to-board adapter. Therefore the diode off-state voltages are approximately 21 (10.5/0.5) times

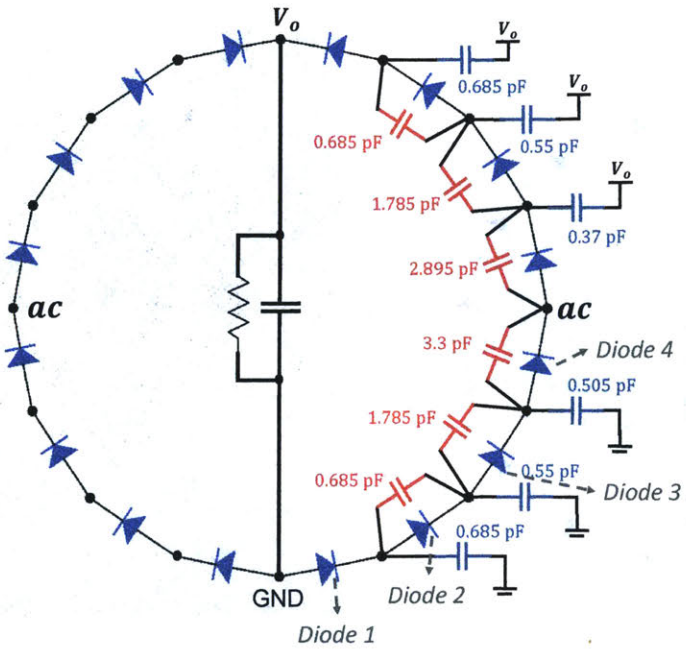


Figure 3-7: The estimated parasitic capacitance of each node to common (in blue) and the required compensation capacitance across each diode (in red). The capacitances are symmetric across the V_o-GND axis. We implement these using the available capacitors with the closest available capacitance values.

the peak-to-peak values of the measured voltages.

3.4.2 Implementation the compensation capacitance

Several CAD and FEA tools [107] are used to simulate the parasitic capacitances of the PCB layout in Fig. 3-6. The process gives us a capacitance matrix consisting of a parasitic capacitance between every two nodes. We simplify the matrix down to only the capacitances between each node and common (GND or V_o), as shown in blue in Fig. 3-7. See Appendix E.3 for detailed simulation and the simplification process.

We choose to implement the coupled compensation because of the availability of discrete capacitors at the required voltage rating. Following the concept in Section 3.3, we can calculate the required compensation capacitances, shown in red in Fig. 3-7. See Appendix E.3 for the detailed calculation process. In the experiments, we used Vishay Vitramon Quad HIFREQ series capacitors to obtain the closest discrete capacitances available: 0.5 pF (VJ1111D0R5VXRAJ), 1.5 pF (VJ1111D0R5VXRAJ

and VJ1111D1R0BXRAJ) and 3 pF (VJ1111D1R0BXRAJ and VJ1111D2R0BXRAJ) respectively. These are NP0 capacitors. They have low loss at high frequencies and small voltage dependencies. Generally, capacitors with small voltage dependencies and stable capacitance values are desirable; as such required capacitances are small, NP0/C0G capacitor types are one good choice.

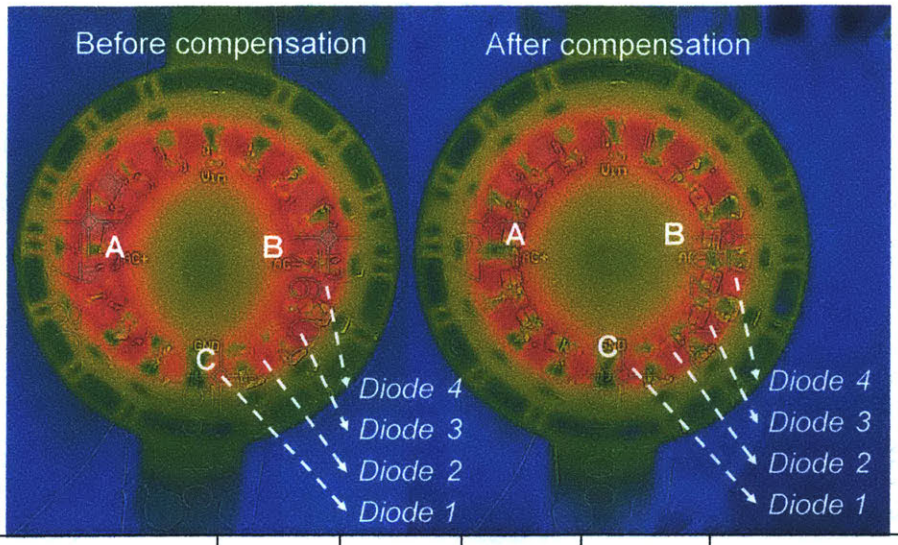
3.4.3 Experimental results

Figure 3-8 shows the temperature profiles of before and after compensation at three different locations in the rectifier (denoted as Nodes A, B and C). Nodes A and B mark two diodes closer to the ac node and Node C marks one diode closer to common. Figure 3-9 presents the divided-down and ac-coupled voltage waveforms across Diodes 1 to 4 before and after compensation. Each waveform is proportional to the actual off-state voltage of an individual diode.

Before compensation, Node A shows the maximum temperature rise in the rectifier (Node B is very similar), Node C remains ~20 °C cooler than Nodes A and B. Correspondingly, in Fig. 3-9a the amplitudes of the diode off-stage voltages decrease in the order of Diode 4 to 1 and the worst-case discrepancy (i.e., the ratio of the maximum diode voltage over the minimum diode voltage) is 2.91. This imbalance in temperature and voltage is especially undesired when the diodes closer to ac nodes reach a certain temperature (~80–90 °C at the package): thermal runaway [108] of the hotter diodes provides positive feedback that can greatly further worsen the discrepancy and overall performance.

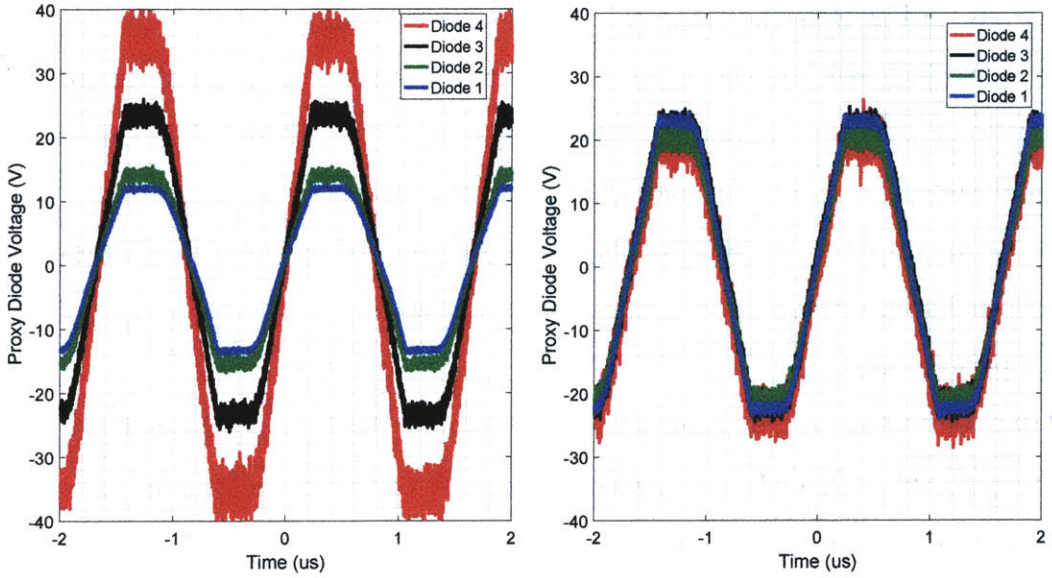
After compensastion, by contrast, temperature at Node A and Node B reduces by ~10 °C and that at Node C increases - the diode temperature become more balanced. The temperature discrepancy between the hottest and the coldest diodes drops from 20 °C to 7 °C. Moreover, the average temperature of Nodes A, B and C drops from 70 °C to 64 °C, indicating decreased overall losses. Correspondingly in Fig. 3-9b, the amplitudes of the off-stage voltages across Diodes 1 to 4 become more balanced and the worst-case discrepancy (ratio of highest to lowest off-state voltage) drops to 1.15.

The above comparison coincides with the analysis in Section 3.2 that the voltage



Conditions	Node A (C)	Node B (C)	Node C (C)	Average (C)	Maximum Delta (C)
Before Compensation	77.8	76	56.1	~70	77.8 – 56.1 ≈ 20
After Compensation	67.4	62.1	61	~64	67.4 – 61 ≈ 7

Figure 3-8: Temperature profile before/after compensation. In both cases, the rectifier operates at 600 kHz and outputs 3.6 kV at 20 mA (72 W).



(a) (b)

Figure 3-9: Proxy (divided down and ac coupled) diode voltages (a) before and (b) after compensation. In both cases, the rectifier operates at 600 kHz and outputs 3.6 kV 20 mA (72 W). The voltage ratio of Diode 1 to 4 is 1 : 1.16 : 1.94 : 2.91 before compensation, and 1 : 0.89 : 0.97 : 0.87 after compensation. The worst-case voltage discrepancy as a percentage is 2.91/1 = 291% and 1/0.87 = 115%.

imbalance is the main factor driving loss and temperature imbalances and resulting in increased maximum and average temperature rises in the rectifier when multiple diodes are connected in series. It also demonstrates the effectiveness of the compensation technique for substantially mitigating the voltage and temperature imbalance. See Appendix E.3 for an accuracy analysis of the proposed methods.

Chapter 4

Design study of a second-generation high-voltage dc-dc power converter

The first flight of an electro-aerodynamic (EAD) propelled aeroplane (Chapter 6) has proven the feasibility of an EAD propulsion system. For the next stage, the EAD team at MIT targets improving the performance of such a system and proving its practicality when used in missions.

The team has identified three directions to improve the performance of the propulsion system: more advanced thruster physics, more integrated system-level design and optimization, and improved high-voltage power electronics. We identify two major changes of the high voltage power electronics for the second-generation EAD system:

- A high voltage dc-dc converter with higher performance, defined by:
  - Higher output voltage at 40–60 kV or even higher.
  - Similar output power of up to 500–600 W
  - Higher specific power (thus lighter weight) above 1.5 kW/kg.
  - Similar (85%) or higher efficiency
- An additional high voltage dc-ac inverter to power a separate dielectric-barrier

discharge ion source (discussed in Chapter 5).

In this chapter, we explore ways to improve the specific power of the high-voltage dc-dc converter.

- First, we incorporate insights learned about high voltage diodes in Chapter 3 in the design of voltage multipliers. This allows us to:
  - Remove cooling fixtures and their associate weights
  - Increase the switching frequency of the converter to 1 MHz, which further reduces the size and weight of passive components in the converter (inductor, transformer and capacitors).
- Second, we explore more flexible high voltage transformer designs that may yield lower weight, including customized core size and core shape, different winding patterns, and various high voltage wires.
- Lastly, we optimize the weight of the inverter, the transformer and the voltage multiplier stages comprehensively.

Section 4.1 presents updated analysis of the voltage multiplier stage with less-lossy diodes. Section 4.2 studies various contributors to the weight of the high voltage transformer in more details. Section 4.3 presents a comprehensive optimization of the three stages. A final design is selected for future construction.

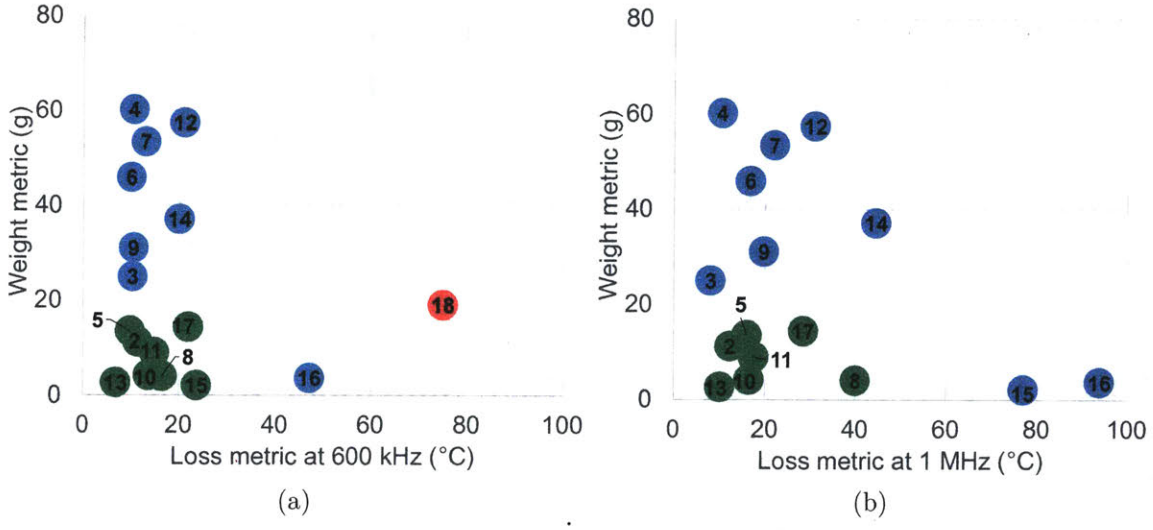
4.1 Improved voltage multiplier design

High voltage diodes are a key limitation in building a high-frequency high-voltage converter at tens of kV and hundreds of watts, especially if we target increasing the switching frequency from 500 kHz to 1 MHz. In this section, we first discuss the selection of high voltage diodes that can switch at 1 MHz, then update the weight study of voltage multipliers with the selected diodes and improved weight model.

4.1.1 Lighter and less-lossy diodes at 1 MHz

In Chapter 3, we tested 37 off-the-shelf diodes in a full-bridge rectifier switching at both 600 kHz and 1 MHz (we call these "single diode tests" in the following context). In these tests, each diode blocks 50 % of their rated voltage and carries an average current 5–10 % of their rated dc current. We identified 17 of them with a maximum temperature rise lower than 100 °C at both frequencies. These diodes are promising candidates for the second-generation voltage multiplier.

We want to narrow down the selections to the diodes that are both lighter weight and less lossy. We use the temperature rises of each diode at 600 kHz and 1 MHz in the single diode tests as their loss metrics. We define a weight metric for each diode as the unit weight of the diode multiplied by the number of diodes needed in series to block a dc voltage V (with a 50% derating on the rated diode blocking voltage) then the number of diodes needed in parallel to carry a dc current I (with a 10% derating on the diode average forward current). Here we pick $V = 60\,\text{kV}$ and $I = 20\,\text{mA}$ to represent our high-voltage and low-current application.



(a) (b)

Figure 4-1: The defined weight metric (lower is better) of each diode plotted against the defined loss metric at a) 600 kHz and b) 1 MHz for realizing an effective rectifier device for use at 60 kV and 20 mA.

Figure 4-1a and Fig. 4-1b plot the defined weight metric against the defined loss metric at 600 kHz and 1 MHz respectively. Each data point is labeled with the diode

index. Diode No. 18 (X150FF3) is used in the 1st-gen high voltage dc-dc converter. Details of these diodes are listed in Table F.1.

We prefer diodes with a temperature rise $\leqslant 40\,^{\circ}\mathrm{C}$ and a weight metric $\leqslant 20\,\mathrm{g}$ at both frequencies (highlighted in green). We pick $40\,^{\circ}\mathrm{C}$ as the temperature rise limit because 1) this temperature rise is likely a conservative estimate of the actual temperature rise of the diodes when connected in series and/or used in a multi-stage voltage multiplier where the diode current has higher rms then in a full-bridge rectifier; 2) when it is above $40\,^{\circ}\mathrm{C}$, a heat sink is likely required. We pick $20\,\mathrm{g}$ as the weight metric limit because there seems a clear separation between $20\,\mathrm{g}$ and the next lightest diode. All the limits can be adjusted for other applications.

In addition, in Chapter 3 we also tested these diodes in the same full-bridge rectifier, but with each rectifier leg consisting of several diodes connected in series (each diode still blocks 50 % of their rated voltage and carries an average current 5–10 % of their rated dc current). Higher temperature rises are observed compared to the single diode tests, due to the imbalance in voltage distribution among the series-connected diodes. Diodes No.10 (Taiwan Semiconductor's ESH1GM) and 13 (ROHM's RFU02VSM6S) exhibit much severer temperature rise imbalance and voltage imbalance when connected in series, thus are removed.

We narrow down to 5 diodes (No. 2, 5, 8, 11, 17) as candidates, which are Infineon's C3D107060Q, GeneSiC's GB01SLT12 and GAP3SLT33-214, Taiwan Semiconductor's UF1GLW and Dean Technology's HVEF8P.

4.1.2 Improvements on the voltage multiplier weight study

We still consider 4 typical voltage multiplier (VM) topologies (Fig. 4-2) as in Chapter 2: half-wave (HW) and full-wave (FW) Cockroft-Walton (CW) and half-wave (HW) and full-wave (FW) Dickson.

Two updates are made on the basis of the analysis in Chapter 2 and are discussed in order in this section:

- Improving the accuracy of the weight model of the VMs by

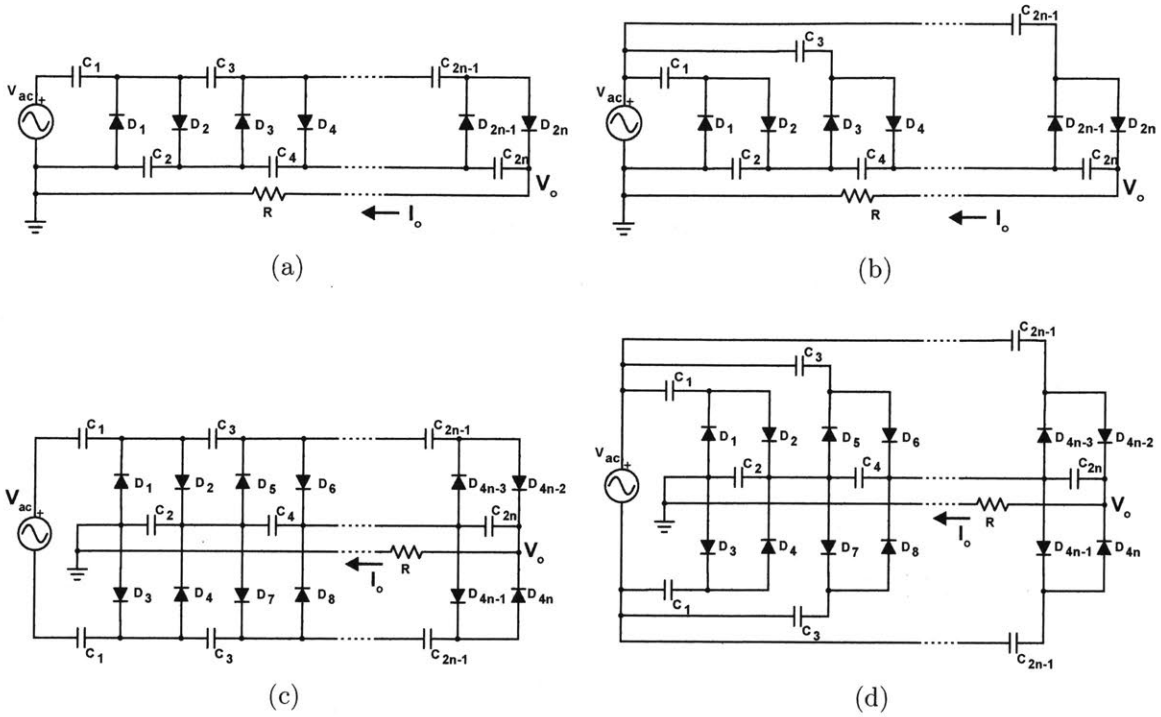


Figure 4-2: Four basic voltage multiplier topologies (a) Half-wave Cockcroft-Walton, (b) Half-wave Dickson, (c) Full-wave Cockcroft-Walton and (d) Full-wave Dickson

- Estimating the VM weight as the sum of that of the capacitors, the diodes and the printed-circuit board.
- Implementing each capacitor and diode with discrete components (diodes in Section 4.1.1 and selected capacitors in Table. D.2) and calculating the weight, rather than estimating the weight with extrapolated relationships.

- Estimating the loss of the VMs and using this in the design of the front-end stages of the converter.

Updated weight estimation of voltage multipliers

The weight of a voltage multiplier (VM) is estimated as the sum of that of the capacitors, the diodes and the printed circuit board (PCB). We consider using a PCB because 1) many candidate diodes and capacitors are surface mount, 2) a PCB offers faster prototyping and more robust structures, which are preferred for the second-generation EAD aeroplanes.

Figure 4-3a compares the overall weight of 4 VM topologies when designed to output 30 kV and 300 W at different input voltages. We consider a uni-polar $n-$stage VM for all topologies ($n = 1, 2, ...$). An $n-$stage full-wave VM provides n voltage gain and an $n-$stage half-wave VM provides $2n$ voltage gain. All designs are at 1 MHz and hold the output voltage ripple to less than 100 V and produce a capacitor charging loss less than 5%. See the details of the weight study process in Appendix F.1.

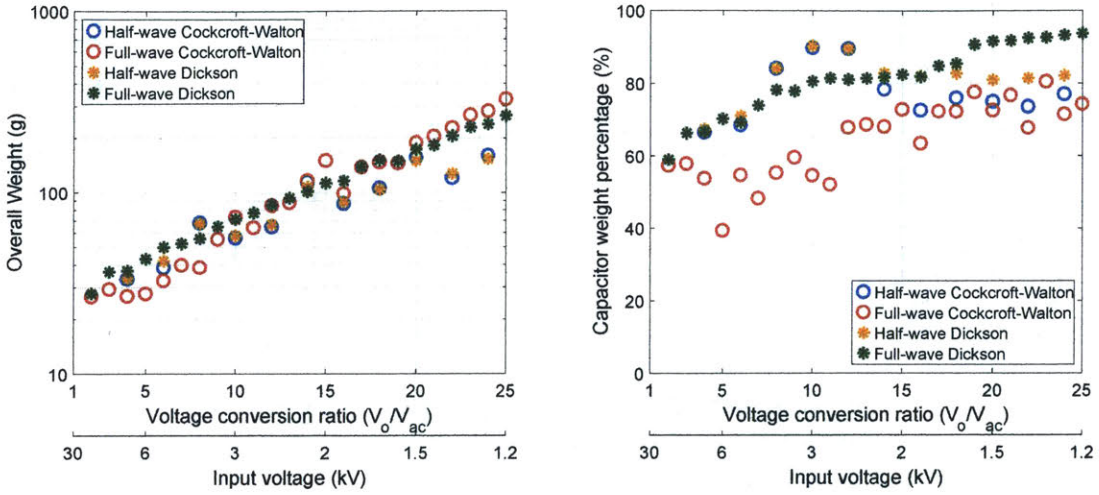


Figure 4-3: a) Overall weight, b) percentage of the capacitor weight in the overall weight of the 4 voltage multiplier topologies. c) normalized total capacitor weight and normalized total energy stored in capacitors of full-wave cockcroft-walton multipliers.

At the design point, when the required voltage gain is lower than 4, there are no

data points for half-wave topologies because only full-wave topologies are available – this is due to diodes in half-wave topologies block twice the input voltage and no available high-voltage diodes are found for them. When the required voltage gain is higher than 15, half-wave topologies yield lower total weight (because they provide the same voltage gain with a halved number of stages, and a further halved flying capacitor count, compared with their full-wave counterparts). When the required voltage gain is between 4 and 15, there is no clear trend that one topology is consistently better or worse than others.

Figure 4-3b shows capacitors account for 40–90 % of the overall weight and in general, the percentage increases as the required voltage gain increases, corresponding to higher number of stages.

The weight study in Fig. 4-3 shows more discreteness compared to that shown in Chapter 2. One reason is that in Chapter 2, we use extrapolated linear relationships to estimate the capacitor weight whereas here we select the lightest discrete capacitor to implement each flying/output capacitor. As an example, we plot the discrete weights of 4 capacitors in the same series and their extrapolated weight relationship in Fig. 4-4. The linear extrapolation "balances out" the heavier and the lighter individual capacitor in this group. Thus, "hand-picking" the lightest individual capacitor may offer significant weight benefits despite increased engineering complexity.

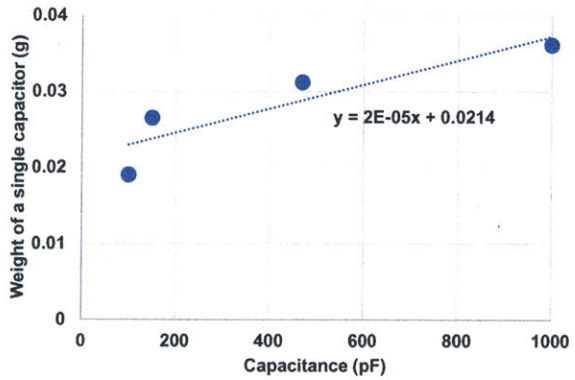


Figure 4-4: Extrapolation among 4 discrete capacitors in KEMET C1206CXXX-JDGACTU series where XXX represents the capacitance (101, 151, 471 and 102). All 4 capacitors are in the same size (surface mount 1206).

Figure 4-3c shows normalized energy stored in capacitors and normalized total

weight of capacitors (estimated by either discrete capacitors or extrapolated weight relationships as in Chapter 2) of the full-wave cockcroft-walton topology. All data is normalized against that of the single-stage VM. The extrapolated normalized capacitor weight increases as the voltage gain in a similar trend to the normalized total capacitor energy. However, by implementing each capacitor with the most appropriate discrete capacitor, we can estimate the weight with higher accuracy and access lighter weights especially when the required voltage gain is high (where capacitors account for most of the overall weight).

Loss model of the voltage multiplier

Type	Voltage gain	R_{Loss} in SSL	Loss
HW CW	$2n$	$\left(\frac{n(n+1)(2n+1)}{6C_o} + \frac{n(n-1)(4n-5)}{12C_{even}}\right)\frac{1}{f_s}$	$I_o^2 R_{Loss} + 2nV_D I_o + 2nP_{sw}$
HW Dick-son	$2n$	$\left(\frac{n}{C_{odd}} + \frac{n(n-1)(4n+1)}{12C_{even}}\right)\frac{1}{f_s}$	$I_o^2 R_{Loss} + 2nV_D I_o + 2nP_{sw}$
FW CW	n	$\left(\frac{n(n+1)(2n+1)}{12C_{odd}}\right)\frac{1}{f_s}$	$I_o^2 R_{Loss} + 2nV_D I_o + 4nP_{sw}$
FW Dick-son	n	$\left(\frac{n}{2C_{odd}}\right)\frac{1}{f_s}$	$I_o^2 R_{Loss} + 2nV_D I_o + 4nP_{sw}$

Table 4.1: Voltage gain, load regulation impedances R_{Loss} in SSL and estimated loss of 4 voltage multiplier topologies as a function of the number of stage n (we assume all flying capacitances as C_{odd}, all output capacitances as C_{even}, the switching frequency as f_s, the diode forward drop as V_D, and the diode switching loss as P_{sw}.)

We estimate the loss of the VMs by summing up the capacitor charging loss and the diode losses. Table 4.1 lists the estimated loss of 4 topologies as a function of the number of stages n. The capacitor charging loss is calculated as the loss on the load-regulation impedance R_{Loss} when the VM operates in the slow-switching-limit (SSL) region, the same as derived in Chapter 2.

The diode switching loss may be derived theoretically for general cases. Here we use the experimentally measured loss data when these diodes are tested in a full-bridge inverter at 1 MHz. The estimated loss of the VMs is highly subject to the diode chosen and shows no clear dependency on the number of stages n (if using the

same diode across all designs, when n increases, the conduction loss increases linearly, however each diode blocks a lower voltages therefore its switching loss reduces).

The developed weight and loss model of the voltage multipliers are used in optimizing the converter in Section 4.3.

4.2 Updates on high-voltage transformers

A transformer is an essential mean to provide large step-up gain and galvanic isolation in a high voltage converter. In this section, we identify 2 factors affecting the achievable weight and specific power of a high-voltage transformer: available high-voltage wires and core sizes. Core shapes and winding pattern show some, but not significant, effects on the achievable weight.

Section 4.2.1 explores high voltage wires and their effect on the transformer weight. Section 4.2.2 analyzes the effect of the core sizes, shapes and winding patterns. The analysis in this section will be used in Section 4.3 for a systematic optimization of the high-voltage dc-dc converter.

4.2.1 High voltage wires

Unlike low-voltage wires, high voltage insulated wires are offered at limited sizes and voltage ratings. The insulation jackets also take up the window area of the transformer core and add to the total weight. Therefore, available high-voltage wires limit the design of a lightweight high-frequency high-voltage transformer. In this section, we discuss in order the limitation of wire size, single strand conductor size, insulation jacket, and their effects on the transformer weight.

In a time-limited search, we survey 50 high voltage wires from Teledyne Reynolds rated between 3–40 kV, and ~140 triple-insulated wires from Rubadue. Both single conductor wires and litz wires are surveyed. The wires from Rubadue are all rated at 1 kV or 1.5 kV on their datasheets but have a breakdown voltage ranging between 4.5–13 kV, presumably because they are rated following different compliance requirements. In the following analysis, we assume the dc rated voltages of Rubadue wires to

be 25% of their breakdown voltages, i.e. 1.125–3.75 kV (one of the wires with 13 kV breakdown voltage was tested at 4 kV with no issues. Here we make this assumption to access higher voltages without running into severe risks of arcing or breakdown). Wires from other makers, such as AXON [109] and Druflon [110], could be included for future research.

As labeled in Fig. 4-6, for litz-wire-based high voltage wires, we refer the "wire size" as the equivalent size of the litz bundle, and "the single-strand conductor size" as the litz wire size; for single-conductor high voltage wires, we refer both the "wire size" and "single strand conductor size" as the size of the conductor.

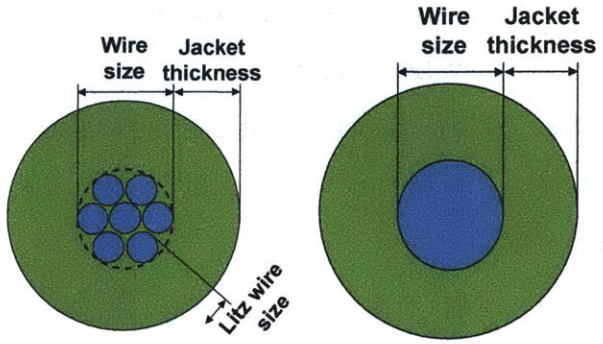


Figure 4-5: Diagrams of (a) Litz wire and (b) single conductor wire.

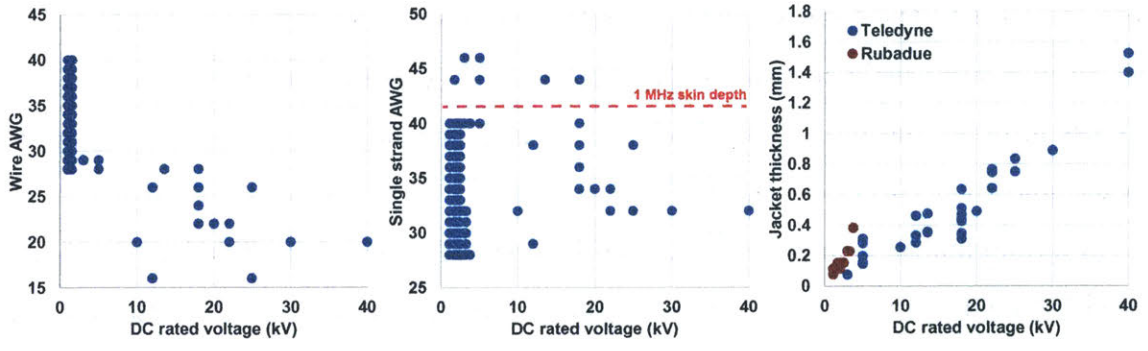


Figure 4-6: (a) Wire gauge, (b) single strand conductor gauge and (c) insulation jacket thickness of surveyed high voltage wires at various voltage ratings.

Wire size

We find that the smallest available wire size increases with the wire rated voltage (Fig. 4-6). Between 1–3 kV, the smallest offered wire is AWG 40; between 3–25 kV, it is around AWG 28 (AWG 29 to AWG 26); above 25 kV, it is AWG 20. There is no available wire rated higher than 40 kV.

We consider the average current carrying capability of these wires – assuming the current carried by the wire is evenly spread across the cross-section of either the litz bundle or the single conductor (we ignore the proximity effect or the skin effect that cause the current crowding at the surface of a conductor for now). The currents carried by AWG 40, AWG 28 and AWG 20 wires are 25 mA, 0.6 A and 3.9 A respectively at an average current density of 500 A/cm^2, which is a rule-of-thumb for designing transformers with reasonable copper losses. For high voltage and low-medium power applications, for example, consider a transformer outputting 10 kV and 500 W with a secondary current of 50 mA: if we want to use wires rated at or above 10 kV (preferred for safety reasons and insulation purposes), the smallest wires we can get are AWG 28 wires which can carry 600 mA. We will be using them inefficiently at a lower current density – the wire takes up space and adds to the weight; if we use wires rated lower than 3 kV, we can get wires that are designed to carry ~50 mA and fully utilize the wire's copper area, but face increased risk of arcing and engineering complexity (such as sectioning the windings and designing additional insulations).

Single strand conductor size

Similarly, we find smallest single strand conductor sizes of high voltage wires also increase with the wire rated voltage (Fig. 4-6b). For high-frequency designs, it is preferred to use a single strand conductor size at or smaller than the skin depth [111] because larger sizes increase copper losses owing to proximity effect, takes up more window area and adds to the total weight. The higher the frequencies and the voltage, the fewer the wire options, thus more limitations on the designs of such a transformer.

Insulation jacket

The secondary wire insulation jackets are commonly made in various fluoropolymer compounds (TEFLON, TEFZEL, etc), silicones, and others. The effective dielectric strength of these materials seems not necessarily consistent when used in high voltage wires – this makes the insulation thicknesses, though generally increasing with voltage, vary even for wires rated at the same dc voltage from the same manufacturer (Fig. 4-6c). For example, 18 kV wires have an insulation thickness range between 0.3–0.65 mm, corresponding to an effective dielectric strength between 30–60 kV/mm.

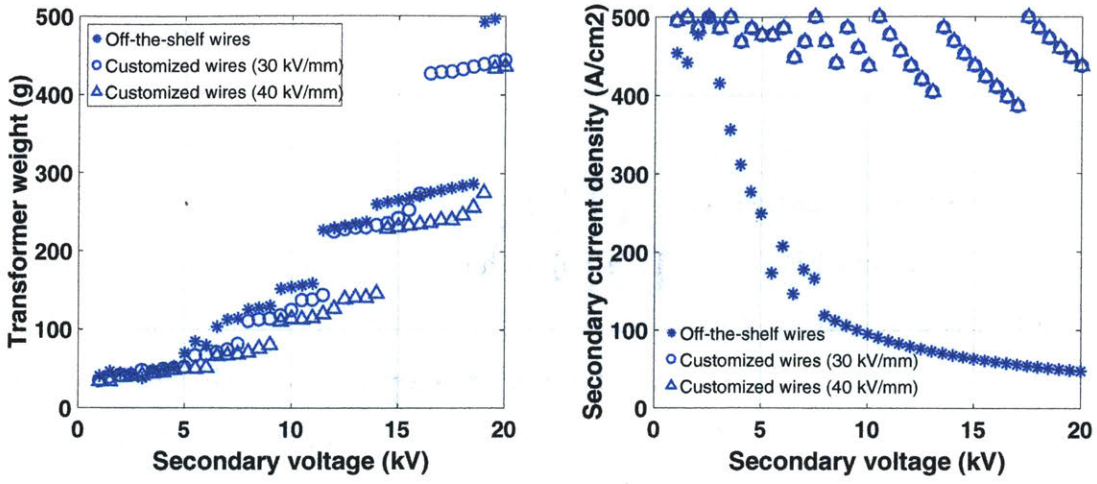
In the transformer designed for the 1st-generation high voltage dc-dc converter, which converts 500 V in amplitude to 7.5 kV, the insulation jacket of the secondary wire accounts for ~15% of the transformer weight. Thus thinner jacket thickness is preferred from the weight perspective.

Effects on the weight

All three limitations mentioned above are mismatched across available wires. For example, the wire with the smallest wire size in Fig. 4-6a does not have the smallest litz size in Fig. 4-6b or the thinnest jacket thickness in Fig. 4-6c. Therefore, the compounded inefficiencies of three factors may result in additional weight, and designing a high-voltage transformer with the most appropriate off-the-shelf wire or with customized wires (if possible) is preferred.

Figure 4-7 shows a comparison of transformer weights (Fig. 4-7a) and current density of secondary wires (Fig. 4-7b) when a transformer is designed using off-the-shelf wires or customized wires with two effective dielectric strengths (30 kV/mm and 40 kV/mm). The transformer converts 500 V in amplitude to 1–20 kV in amplitude at 1 MHz and outputs 600 W. Four assumptions made across designs are: 1) consider only Ferroxcube off-the-shelf core sizes; 2). use Ferroxcube 3F46 as the core materials; 3) secondary wires are rated at 6 times the layer-to-layer secondary voltages; 4) for customized wires, use AWG48 as both the minimal available litz size and the minimal available wire size. The current density refers to the average current density of the

wire assuming uniform distribution and ignoring skin or proximity effect.



(a) (b)

Figure 4-7: (a) Transformer weight and (b) secondary peak current density of high voltage transformers designed with off-the-shelf wires or customized wires.

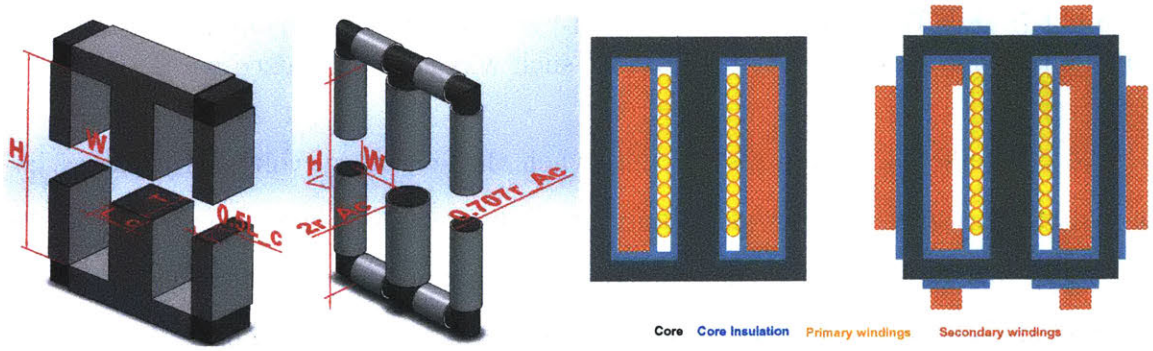
We conclude from these results that when the secondary voltage is below 5 kV in amplitude, the weights are not significantly different by using either wire. As the secondary voltage increases, the transformer weight increases discretely – this is a compounded effect of both the wires and the core sizes (the latter will be discussed in Section 4.2.2). Comparing across different types of wires, off-the-shelf wires are used at a much lower current density, taking up the winding space, driving up the core sizes and yielding heavier designs compared to the customized wires. Similarly, comparing across different effective dielectric thickness, customized wires with a higher effective dielectric strength yield lower weights.

4.2.2 Core sizes, shapes and winding patterns

As shown in Fig. 4-7a, the transformer weight increases discretely with the secondary voltage. This is mainly because manufacturers offer limited and discrete core sizes which fit general designs but may not be optimized for high voltage designs. In this section, we discuss the limitation of transformer core sizes, shapes, winding patterns, and their effects on the transformer weight.

We survey off-the-shelf E-type ferrite cores from Ferroxcube, including square-legged cores (EE, EFD cores) and round-legged cores (RM, ER, EC, ETD, PQ cores). We find that fewer cores are offered in more sparse sizes when the core volume is bigger than $20\,\mathrm{cm}^3$, presumably because soft ferrite cores used in their typical applications are small in sizes (low-medium power low-voltage applications where the switching frequency is between hundreds of kHz and several MHz).

EE (Fig. 4-8a) and ER cores (Fig. 4-8b) with customizable sizes are considered in the study. EE cores are easy to machine and customize; ER cores are favorable for high voltage designs because they have fewer sharp corners. For both core shapes, we assume that each side leg has half the cross sectional area of the center leg. For ER cores, we also compare center-leg winding and double-leg winding (Fig. 4-8c).

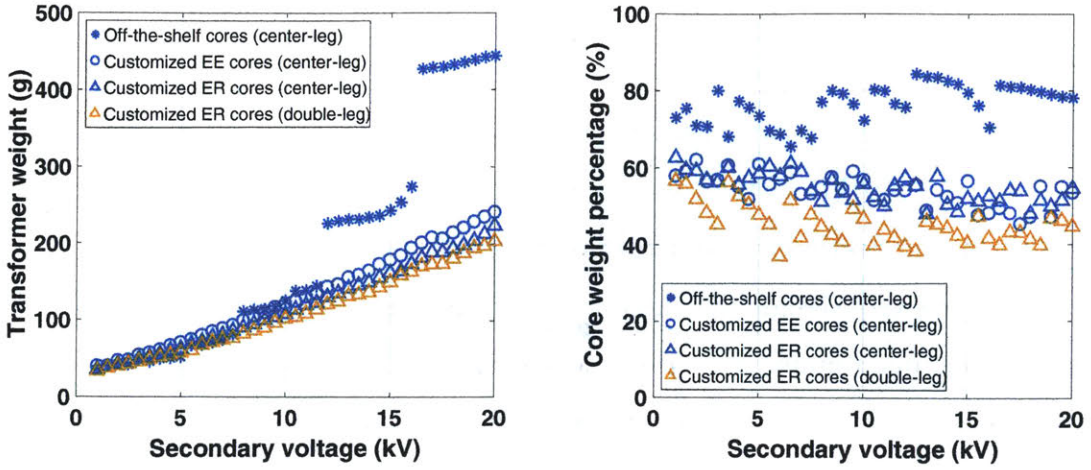


(a) (b) (c)

Figure 4-8: (a) EE cores and (b) ER cores (c) front-view of center-leg (left) and double-leg (right) winding considered in the weight study.

Figure 4-9a compares transformer weight when designed using off-the-shelf cores or customized cores. We hold the same assumptions as the study above and design the transformer to convert 500 V in amplitude to 1–20 kV in amplitude at 1 MHz and outputs 600 W. To separate the effect of the wires, we consider using customized wires with an effective dielectric strength of 30 kV/mm across all designs (thus the data with asterisks in Fig. 4-9 corresponds to the data with circles in Fig. 4-7).

As the secondary voltage increases (especially above ~10 kV in amplitude), bigger cores are needed to accommodate the increasing number of secondary turns and the increasing volume of insulation – this is when customized core sizes become more



(a) (b)

Figure 4-9: (a) Transformer weight and (b) percentage of core weight in the transforer weight when designing high voltage transformers with off-the-shelf cores or customized EE/ER cores.

beneficial as there are fewer and more sparse off-the-shelf core sizes. Among the customized designs, as the voltage increases, the copper and the insulation takes up more and more of the weight, the percentage of the core weight reduces from 60% to 50% as the voltages increases from 0-5 kV to 15-20 kV in amplitude (Fig. 4-9b).

Figure 4-9 also suggests different core shapes (EE and ER) and different winding patterns (either center-leg winding or double-leg winding) have some but not much influence on the achievable transformer weight.

In summary, the achievable weight of the transformer, especially in high-frequency high-voltage and low-medium power applications ($\geqslant$500 kHz, $\geqslant$10 kV in amplitude and hundreds of watts), depends on the available high voltage wires and core sizes but not so much on the core shapes and winding patterns. With customization, a transformer weighing 10 g/kV appears possible for an 5–20 kV in amplitude 600 W output from an input of 500 V in amplitude.

4.3 System optimization

Different distributions of voltage gains among the inverter, the transformer and the voltage multiplier (VM) can result in different overall weights of the high voltage dc-dc converter. In this section, we incorporate the improved weight study of voltage multipliers in Section 4.1 and that of high voltage transformers in Section 4.2, and comprehensively design the three stages to minimize the overall weight of the converter while maintaining a good efficiency.

Section 4.3.1 describes the optimization methods and Section 4.3.2 presents the simulation results of the overall weight of the converter.

4.3.1 Optimization methods

For the overall converter topology, we consider

- A full-bridge series-parallel resonant inverter [86,87] because: 1) it can incorporate the parasitic capacitance from the high voltage transformer; 2) it provides a factor of 2 in the voltage gain with negligible weight gain; 3) it shows high efficiency in both light load and heavy load; 4) it has a series capacitor to block dc voltage and thus prevent saturation of the transformer.

- A transformer containing X secondaries, and the turns ratio of the primary and each secondary is $1 : \frac{K}{X}$. Each secondary is connected to a bi-polar voltage multiplier (VM) with each polarity providing a voltage gain of Y. The outputs of each multiplier are then connected in series as the full output voltage.

- Half-wave and full-wave cockcroft-walton multipliers as the VM topology because of their ease of implementation. Each diode in the voltage multiplier can be a single diode or several diodes in series.

We consider both multi-secondary transformer and connecting several diodes in series so that we can design the voltage multipliers with the identified low-voltage diodes, which may yield lower weight and lower losses. Figure 4-10 shows the schematics of the converter configuration to be optimized.

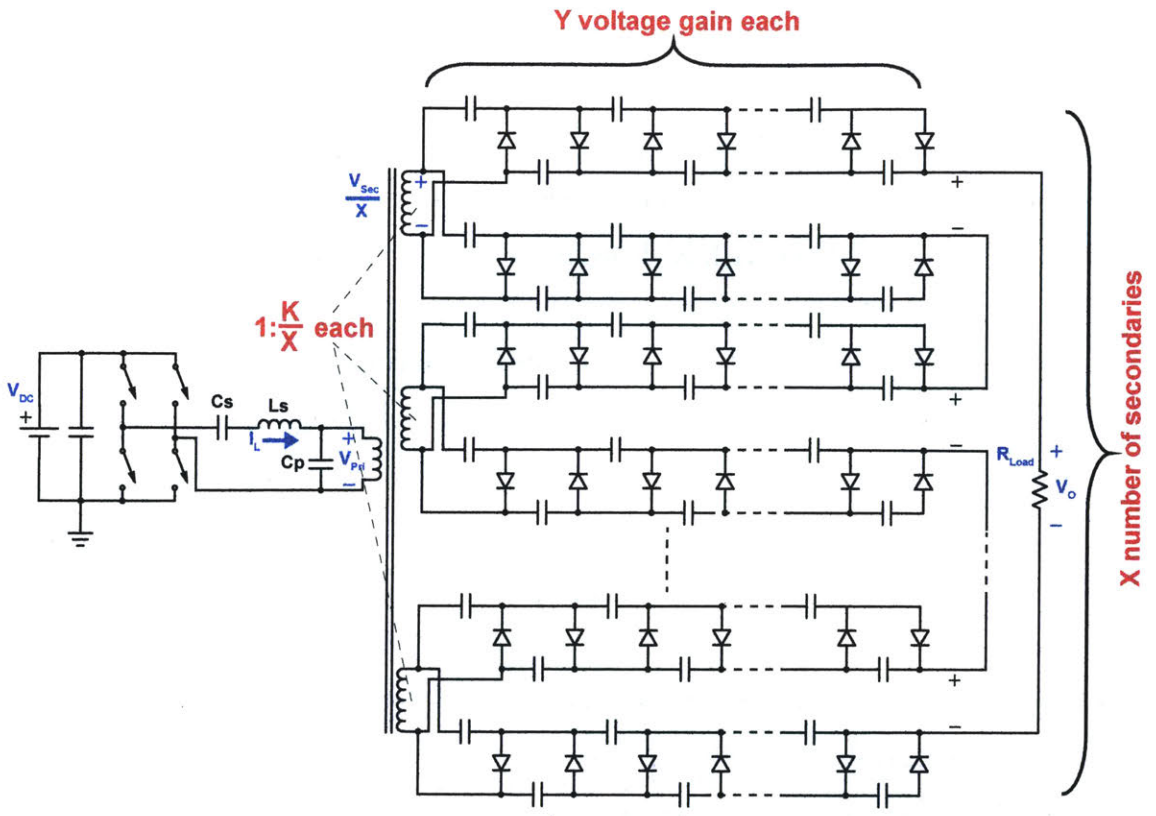


Figure 4-10: Schematics considered in the optimization of the high voltage dc-dc converter. It shows half-wave voltage multiplier as an example implementation.

In this study, we consider V_{DC} =200 V, V_o =60 kV and P_o =600 W. This operating point is preliminary at the time of the thesis and may be refined as the system optimization of the aircraft continues. The weight study presented here also feeds into the aircraft optimization.

The overall weight of the converter is the sum of that of the resonant inductor L_s, the transformer and the voltage multiplier. The optimization process is:

- Select a set of operation variables: the resonant tank quality factor Q, the tank natural frequency f_0, the series and parallel resonant capacitance ratio $A = C_P/C_S$, and the equivalent transformer step up ratio K, and the voltage multiplier voltage gain Y. The tank parameters (voltage gain G, maximum inductor current $I_{L_{max}}$, inductances and capacitances L_S, C_S, C_P), the transformer primary voltage V_{Pri} and equivalent secondary voltage V_{Sec} can then be calcu-

lated. We keep the sets that satisfies $V_{DC} \times G \times K \times Y \in [60kV, 1.05 \times 60kV]$)[1]. To simplify the design, we assume the number of transformer secondaries X only affects the voltage multiplier weight but not the transformer weight (i.e., a one-secondary transformer converting V_{Pri} to V_{Sec} weighs the same as a two-secondary transformer with each secondary producing $0.5V_{Sec}$).

- Design the lightest weight voltage multiplier: we consider the number of transformer secondaries X from 1 to 5. At each X, we design the VM to provide a voltage gain of Y at an input of $\frac{V_{Sec}}{X}$ and times the weight by X. Then we select the lightest VM design across X. The loss of the VM is also calculated and fed to the design of the transformer.

- Design the lightest weight transformer that converts V_{Pri} to V_{Sec} and satisfies a set of constraints on efficiency, temperature rise and packing factor. The transformer output power is the sum of P_o and the loss of the VM.

- Design the lightest inductor, given the inductance and maximum current, that satisfies a set of constraints on efficiency, temperature rise and packing factor.

- Sweep all sets of operating variables and find the combination that yields the lightest overall weight. The design space we explored is: $1 \leqslant Q \leqslant 5$, $0.1 \leqslant A \leqslant 0.5$, $f_0 = 1\,\text{MHz}$, $5 \leqslant K \leqslant 40$, $2 \leqslant Y \leqslant 40$.

- Refine the transformer design by checking its parasitics and insulation designs: 1) if the leakage inductance of the transformer is not negligible compared with L_s, then redesign the inductor; 2) the parasitic capacitance of the transformer should be smaller than C_P. If exceeded, each secondary should be sectioned; 3) if transformer secondaries are biased at different potentials due to the series connection at the output of each voltage multiplier, additional insulations are added between adjacent secondaries.

[1]We set K and Y as free variables to start with because it is used to calculate the tank gain G.

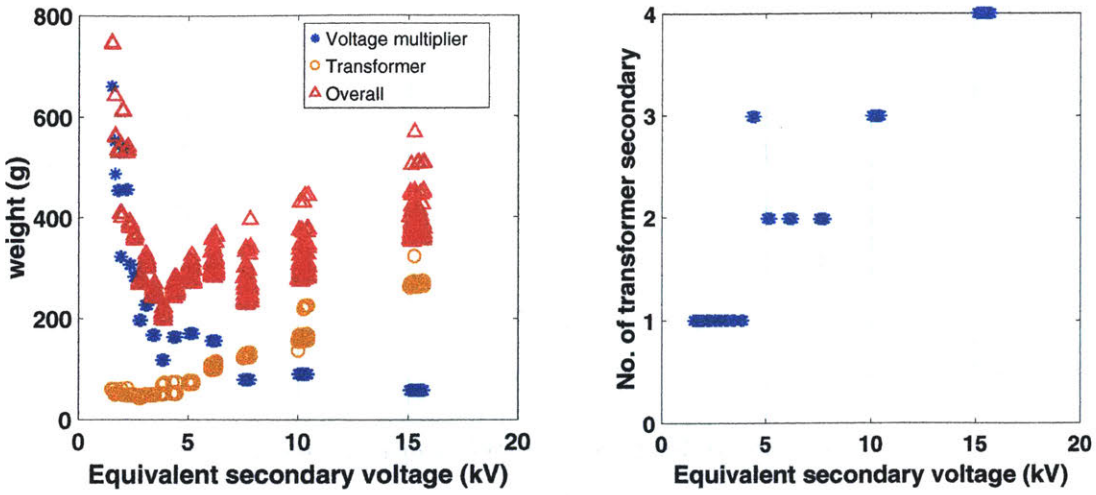
4.3.2 Optimal weight and voltage gain distribution

In this section, we provide a conservative design that balances the engineering risk, development time and the project timeline. We set several limits to ensure the practicality of the design: 1). use single diode with the necessary voltage rating and not consider connecting several diodes in series as an equivalent high voltage diode; 2) for the transformer, we consider off-the-shelf core sizes with center-leg winding and off-the-shelf high voltage wires.

For future designs, especially for higher output voltage, we can relax the limits to: 1) consider connecting several diodes in series as an equivalent high voltage diode but limit the number of diodes in series to 3; 2) for the transformer, we consider customizing core sizes with center-leg winding and remain using off-the-shelf high voltage wires. The upgraded design will likely provide higher specific power because 1) as mentioned in Section 4.2, customized core can yield lower weight; 2) for higher output voltage, multiple low-voltage transformer secondaries driving multiple low-voltage multipliers may be heavier than one high-voltage transformer secondary driving one high-voltage voltage multiplier due to added insulation between secondaries and added supportive materials such as PCB.

Figure 4-11a plots the weights of the voltage multiplier, the transformer and the overall converter against the equivalent transformer secondary voltage in amplitude ($V_{Pri} \times K$, the sum of voltages of all secondaries). As this voltage increases, the voltage multiplier weight decreases due to fewer stages (despite more secondaries) whereas the transformer weight increases due to higher turns ratio and more secondaries.

Across most designs, diode HVEF8P (an 8 kV 30 mA Si high voltage diode, No.17 in Fig. 4-1b) is selected because of its light weight and high blocking voltage. It sets each secondary of the transformer to only output up to 4 kV in amplitude, 50% of the rated voltage of HVEF8P (Fig. 4-11b). The overall weight reaches a minimum at around 4 kV in amplitude with one transformer secondary. In these designs, the voltage multipliers are all a bipolar full-wave cockcroft-walton multiplier with each polarity containing 8 stages. Such a high number of stage may introduce higher



(a) (b)

Figure 4-11: (a) Weights of the transformer, the voltage multiplier and the overall weight change against equivalent transformer secondary voltage in amplitude ($V_{Pri} \times K$, the sum of voltages of all secondaries) and (b) the number of transformer secondaries vs the equivalent secondary voltage.

engineering risk (such as unbalance heating between stages). To mitigate the development risk, we finalize the design at the next lightest weight group (two transformer secondaries, each output ~4 kV in amplitude, yielding an equivalent transformer secondary voltage ~8 kV in amplitude). The voltage multiplier is a bipolar full-wave cockcroft-walton multiplier with each polarity containing 4 stages.

We also find that the overall weight reaches minimal when the tank gain G is 1.5 to 3.5, corresponding to a tank quality factor Q of 1 to 2 and the transformer primary voltage between 400 and 700 V in amplitude. This is consistent with Chapter 2.

Figure 4-12 shows the final design and Table 4.2 lists the specifications. The design weighs 300 g, ~ 40% in transformer, ~ 30% in the voltage multiplier, and ~ 30% in the inverter with the inductor. The simulated efficiency of the converter is 89%.

If we consider an overhead of 100 g, the design still yields a specific power of 1.5 kW/kg. This overhead is a rough estimation to account for 1) potential redesign of the inductor to achieve voltage regulation across a range of input voltages; 2) potential underestimation of the parasitic capacitance from the transformer and the diodes. If happens, we may add more sections in the transformer secondary; if the actual

parasitic capacitance is at a similar level as the magnetizing impedance, we may also consider increase the primary number of turns; both measures would add additional weight to the transformer; 3) weight of solder joints on the voltage multiplier PCBs.

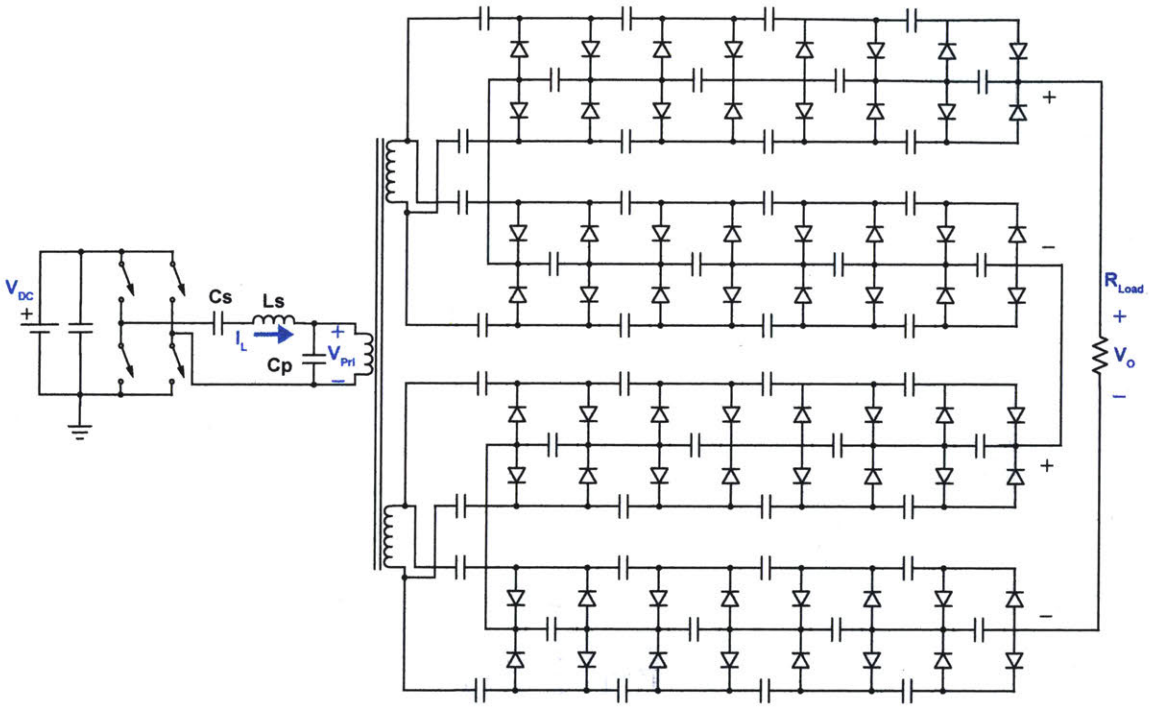


Figure 4-12: Final design of the second-generation high voltage dc-dc converter.

Stage	Component	Description	Estimated Weight	Estimated voltage gain
Inverter	C_s	13.2 nF	60 g ‡ (20%)	~ 2
	C_p	1.32 nF		
	Inductor L_s	RM10 core in Ferroxcube 3F46; AWG14 wire; 11 turns, air gap 0.648 mm, ~21 µH	25 g (~10%)	
Transformer	Core ††	ETD44/22/15, Ferroxcube 3F46	90 g (30%)	Two 1 : 10
	Primary	AWG 16 litz wire, 6 turns, 1 layer	4 g	
	Two secondaries	Teledyne Reynolds AWG28 18kV FEP wire (P/N 178-5790); 126 turns total, each secondary has 60 turns, 2 section, 5 layer 6 turns per layer per section.	30 g (10%)	
Voltage Multiplier	C_{odd}	KEMET C1808C471JGGAC7800, 4S7P, 800 pF per equivalent capacitor	45 g (15%)	16. (Two bipolar FWCW VM. † 4 stage per polarity)
	C_{even}	KEMET C1206C221JGGACAUTO, 4S1P, 60 pF per equivalent capacitor		
	Diodes	Dean Technology HVEF8P, 1S2P per equivalent diode	14 g (5%)	
	PCB	-	28 g (10%)	
Total weight of the design			300 g (100%)	~320

Table 4.2: Final design of the second-generation high voltage dc-dc converter
†† Another possible core is EC52 in Ferroxcube 3F46 material. Turns ratio is 5:125.
‡ Estimated from the 1st-generation converter.
† FWCW VM is short for full-wave cockcroft-walton voltage multiplier.

Part II

Lightweight High-Voltage AC Power Conversion

Chapter 5

Lightweight high voltage inverters for dielectric-barrier discharge

As identified in Chapter 6, one way to improve the efficiency and the practicality of the electro-aerodynamic (EAD) propulsion technology is to increase the efficiency of the ion source. Collaborative work by the author and colleagues in [7] (see Chapter 6 for details) reveals that adding a separate dielectric-barrier-discharge (DBD) ion source in addition to the corona-discharge ion source can improve the thrust generation and thus the performance of EAD thrusters [1,6]. In this chapter, we call this DBD-corona combined thruster as a "decoupled thruster".

A wide range of high voltage ac waveforms or pulses (including different shapes, frequencies, amplitude, etc) can be used to generate the DBD [12, 26]. How they affect the efficiency of the thrust generation is unclear and being studied by the MIT EAD team. They also largely affect the weight of the converters required to power the DBD, which in turn influences the overall performance of the EAD propulsion system. Thus, the development of the high voltage inverter or pulse generator needs to be tightly integrated with the characterization of the decoupled thruster.

The goal of this chapter is to 1) quantify the achievable weight and specific power, defined as power delivered per unit of weight (kW/kg), of commonly used high voltage converters for DBD applications. 2) develop and demonstrate lighter-weight converters to power the DBD and the decoupled thruster.

As mentioned in Chapter 1, the topologies of high voltage inverters for DBD applications generally fall into two categories, as shown in Figure 5-1:

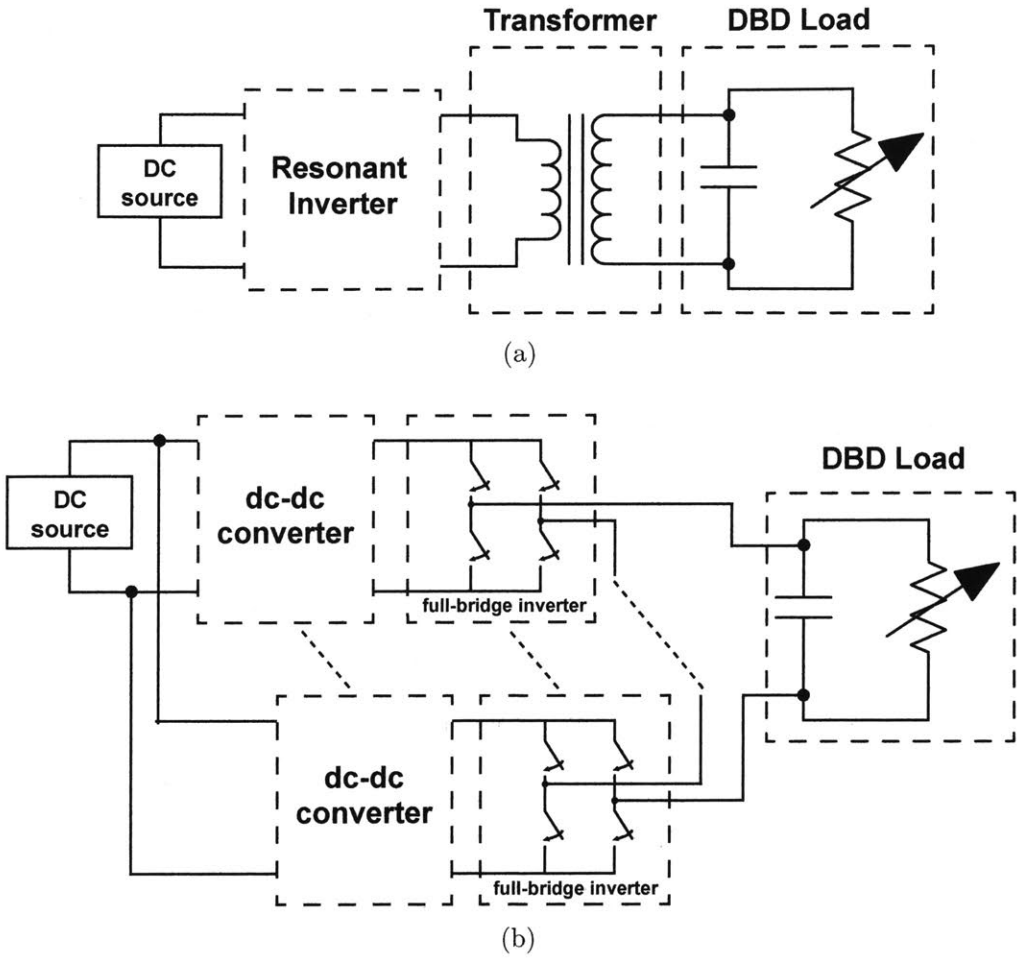


Figure 5-1: Simplified diagrams of two topology categories of high voltage inverters/pulse generators for DBD (a) resonant topologies and (b) non-resonant topologies.

- Resonant topologies where the inductance in the system resonates with the capacitances in the system near the DBD frequency.

- Non-resonant topologies where an inverter operates as a voltage source and "hard charges" the DBD capacitive load. The dc-dc stage is usually present for higher voltage gain, regulation and/or isolation purposes. The switching frequency of the dc-dc converter can be much higher than the DBD frequency. The same copies of the converter can be stacked in series at the output to achieve a higher voltage, and/or to form a multi-level output waveform.

Section 5.1 and 5.2 estimates the achievable weight of an example converter in each of the topology category. In these sections, we study the weight of the converters in the following range and identify how it changes against each operating parameter:

- DC input voltage, V_{DC}, from 100–400 V
- DBD voltage amplitude, V_o, from 1–10 kV, DBD frequency, f, of 1–100 kHz, DBD power, P_o, of 10–1000 W

A preliminary set of requirements on the converter to drive the decoupled thruster, as identified in Chapter 6, is to produce a $\pm$4 kV 10 kHz ac power supply that can deliver $\sim$200 W to the DBD load. A specific power of 2 kW/kg is desired based on the system weight budget for a second generation EAD aircraft. Following these specifications, Section 5.3 proposes three lightweight converter designs: a) high-frequency transformer based converter with frequency conversion; b) high-frequency transformer based converter with burst-mode control; c). switched-capacitor multi-level inverter based solution. Section 5.4 demonstrates the latter two proposed approaches with experimental results. The work on switched-capacitor multi-level inverter is collaboratively done with Suzanne O'Meara and is continued by her as part of her Master of Engineering thesis.

5.1 Resonant topologies

As an example implementation of resonant topologies, we choose a parallel resonant tank cascaded with a transformer (Fig. 5-2) and study its weight and specific power. The resonant inductance L is a standalone inductor. The resonant capacitance C is a combination of the DBD capacitance, the transformer parasitic capacitance, and/or external capacitors. L and C resonate at the DBD frequency f.

The weight of the converters based on resonant topologies is dominated by magnetic components, i.e. the inductor and/or the transformer, especially at low DBD frequencies. Therefore in this section, we approximate the total weight of the converter as the weight of the magnetics.

Section 5.1.1 studies the lightest achievable weight of the resonant inductor. We analyze how the weight of the inductor changes with four operating parameters: f, V_{in}, G, and P_T. f is the tank resonant frequency (same as the DBD frequency); V_{in} is the sinusoidal exciting voltage ($V_{in} = 4/\pi V_{DC}$); G is the tank gain (V_T/V_{in}, where V_T is the sinusoidal output voltage at resonance); P_T is the output power of the tank.

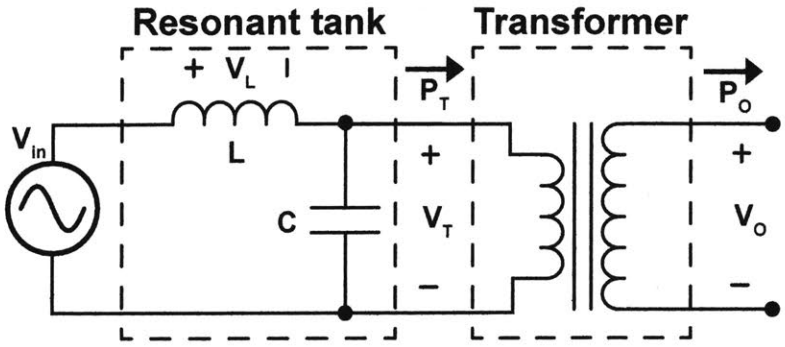


Figure 5-2: An example implementation of resonant topologies.

Section 5.1.2 studies the lightest achievable weight of the transformer changing with f, V_T, V_o, and P_o. V_T and V_o are the sinusodial input and output voltage respectively. f and P_o is the DBD frequency and DBD power respectively.

Section 5.1.3 combines Section 5.1.1 and 5.1.2 and find the lightest achievable weight of all magnetics when varying V_{in}, V_o, f and P_o.

In each of the sub-sections, the weight study is a four 1-dimension study. A more informative study would be a 4-dimension study, which was not pursued due to limitations on time and computational power.

The essence of the weight study for both the inductor and the transformer is: for each operating point, a range of designs are swept. All designs are passed through a set of fixed constraints (including efficiency, thermal and physical constraints) and the lightest design satisfying all is selected. Then we sweep the operating conditions to see how the lightest design changes with each operating parameter.

Appendix G.1 includes more details about the weight study method and all simulated designs in this section. Below we only present and interpret the weights of these designs.

5.1.1 Inductor

The inductance, L, and the airgap, g, of the resonant inductor in Fig. 5-2 are calculated based on V_{in}, G, f and P_o. See Appendix G.1 for derivations.

$$L = \frac{GV_{in}^2}{4\pi f P_o}, I_{L_{max}} = \frac{2P_o}{V_{in}} \tag{5.1}$$

$$B_{max} \simeq \frac{\mu_0 N I_{L_{max}}}{g}, g \simeq \frac{\mu_0 A_c N^2}{L} \tag{5.2}$$

Substituting (5.1) in (5.2), we have

$$B_{max} \simeq \frac{GV_{in}}{2\pi f A_c N} \tag{5.3}$$

Where A_c is the cross-sectional area of the core, N is the number of turns, $I_{L_{max}}$ is the maximum inductor current and B_{max} is the maximum flux density.

Figure 5-3 shows the lightest achievable weight of the inductor changing with V_{in}, G, f and P_T.

Figure 5-3a suggests that as f increases, the weight at first decreases sharply, then hits a plateau and decreases slowly. This is because the inductor is first saturation limited (in this example, <25 kHz), then loss limited (25–400 kHz), then temperature limited (>400 kHz). This general trend is consistent with other inductor designs sized vs. frequency [103].

Figure 5-3b shows that the weight increases linearly with voltage gain G. All designs are saturation limited, higher gain results in more windings N and a bigger core (larger A_c) to maintain the same B_{max} as shown by (5.3).

Figure 5-3c shows that the weight increases with P_T. Higher power increases the inductor current linearly (see (5.1)), driving up the copper loss and the temperature. A bigger core is needed to dissipate the loss, which in turn drives up the core loss. A balance is reached when a core size can accommodate both the loss and the temperature limit.

Figure 5-3d suggests that the weight increases with V_{in}. Similar with Fig. 5-3b, the

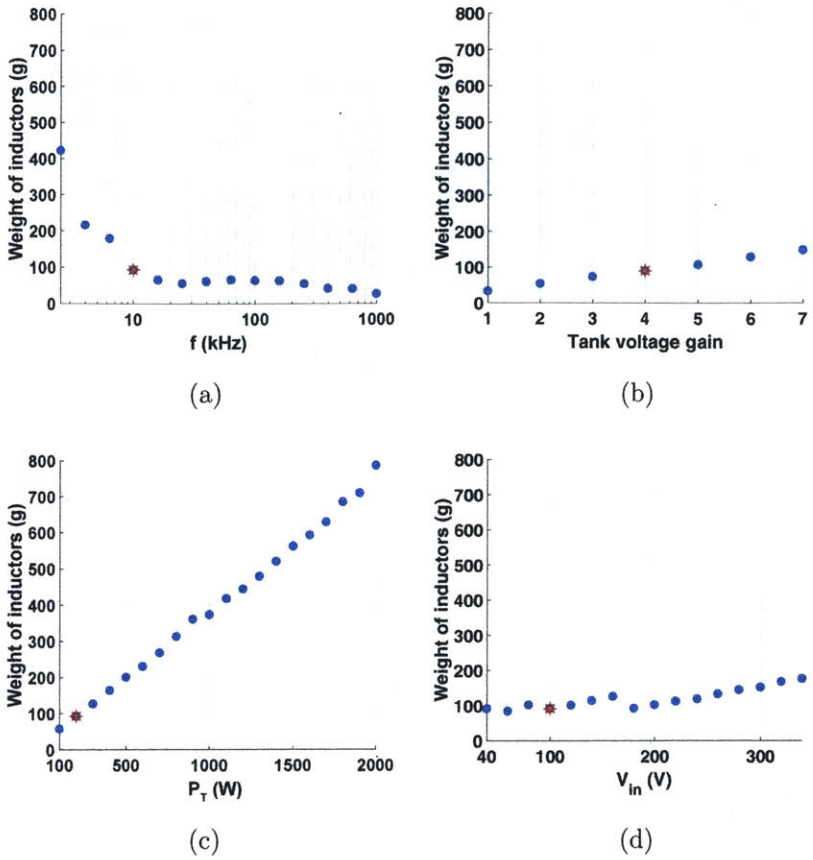


Figure 5-3: Weight of the resonant inductor as functions of (a) f, (b) G, (c) P_T, and (d) V_{in}. When sweeping one variable, the others fix at $V_{in} = 100\,\text{V}$, $G = 4$, $f = 10\,\text{kHz}$, $P_T = 200\,\text{W}$.

designs are saturation limited – more windings and a bigger core are needed at higher V_{in} (see (5.3)). The difference is that higher V_{in} yields a smaller inductor current (see (5.1)) and thinner wires can be used (in fact, the discontinuity at V_{in} =60 V, 100 V and 180 V is because of using a smaller wire.).

5.1.2 Transformer

The transformer satisfies the electrical requirements defined by V_T, V_o, f and P_o:

$$\frac{N_s}{N_p} = \frac{V_o}{V_T} \tag{5.4}$$

$$B_{max} \simeq \frac{V_T}{2\pi f N_p A_c} \tag{5.5}$$

Where A_c is the cross-sectional area of the core, N_p and N_s are the number of primary and secondary turns respectively, B_{max} is the maximum flux density.

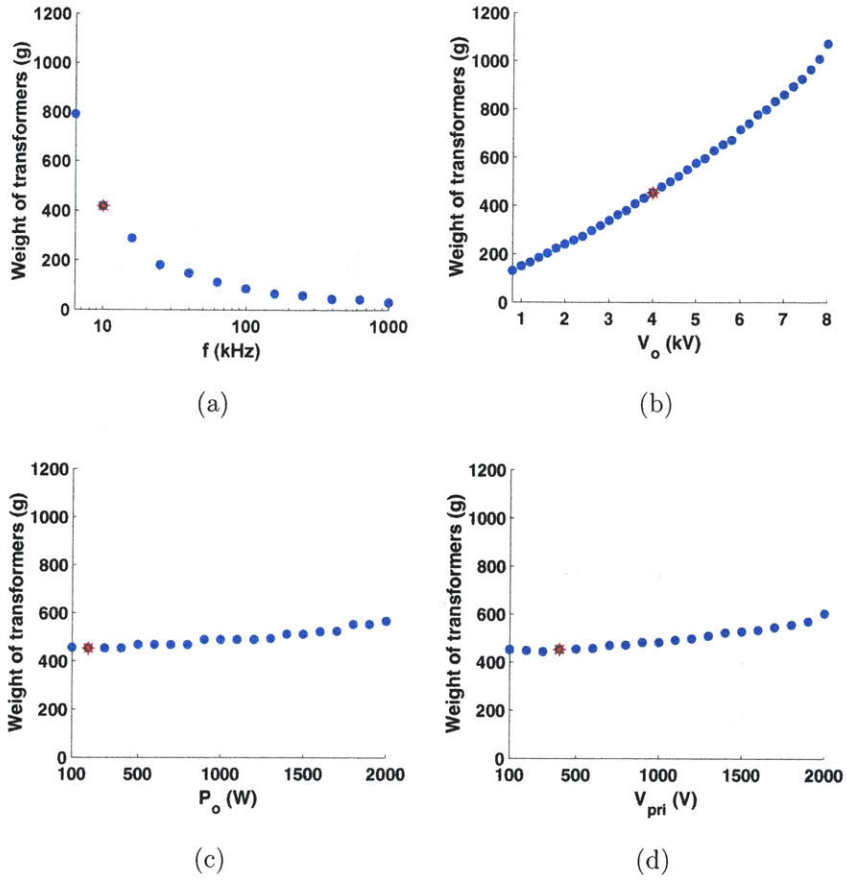


Figure 5-4: Weight of a high voltage transformer as functions of (a) f, (b) V_T, (c) V_o and (d) P_o. The red asterisk marks the same reference point: $V_T = 400\,\mathrm{V}$, $V_o = 4\,\mathrm{kV}$, $f = 10\,\mathrm{kHz}$, $P_o = 200\,\mathrm{W}$.

Figure 5-4 shows the lightest achievable weight of a high voltage transformer changing with V_T, V_o, f and P_o. See Table. G.4 for the details of all simulations.

Figure 5-4a shows that the weight decreases with f but the trend saturates at high frequency. Similar as in [111], this is because the product of the window area and the cross-sectional area (thus the core size) of the transformer reduces as the frequency increases. The transformer is saturation limited at low frequency and loss/temperature limited at high frequency.

Figure 5-4b suggests that the weight increases as V_o. High V_o means high turns ratio and a larger number of secondary turns N_s, therefore a bigger core is required

to fit the windings. This trend is more than linear at even higher voltage because a larger portion of the window is taken by insulation materials.

Figure 5-4c suggests that the weight increases with P_o but does not strongly depend on it. This is because: 1) the increase in P_o here only means an increase in the primary and secondary current (not V_T and V_o). 2) the increased current results in an increase in the current density of the wire and the copper loss, but not the wire size[1]. 3) at $f = 10\,\text{kHz}$, all designs are saturation limited and the core size is set by the saturation limit. Therefore, core size, wire size and number of turns do not have big changes as P_o increases.

Figure 5-4d suggests that weight increases with V_T. These designs are saturation limited therefore more windings and a bigger core are needed at higher V_T (eq. (5.5)).

5.1.3 Overall converter

The weight of the converter is approximated as the sum of that of the inductor and the transformer. We assume $P_T = P_o$ for simplicity[2]. For each operating point defined by V_{in}, V_o, f and P_o, the intermediate voltage V_T is swept between $2V_{in}$ and $V_o/2$ and the lightest design is selected.

Figure 5-5 shows that the lightest achievable weight of all magnetics decreases with f, increases with V_o and P_o. These are the compounded effect of both inductor and the transformer. It also suggests that the weight remains almost unchanged with V_{in} – the tank gain of these designs remains at 2, higher V_{in} results in a heavier inductor, but it also drives V_T higher, which reduces the transformer step-up ratio and yields to a lighter transformer.

Mirroring Fig. 5-5, the achievable specific power is plotted in Fig. 5-6. The specific power as a function of V_{in} was not plotted since the weight does not change much with V_{in}. To drive a DBD at 10 kHz, 4 kV and 200 W (the preliminary requirement of

[1]As explained in Appendix G.1.4, the litz wire diameter is set by the maximum of either twice the skin depth or the minimal available litz wire. At $f = 10\,\text{kHz}$, the litz size is set to twice the skin depth. Since $V_o = 4\,\text{kV}$, the secondary current is small and the litz size is much larger than needed to carry the current.

[2]This is reasonable because we constrain the transformer loss to be $< 5\%$.

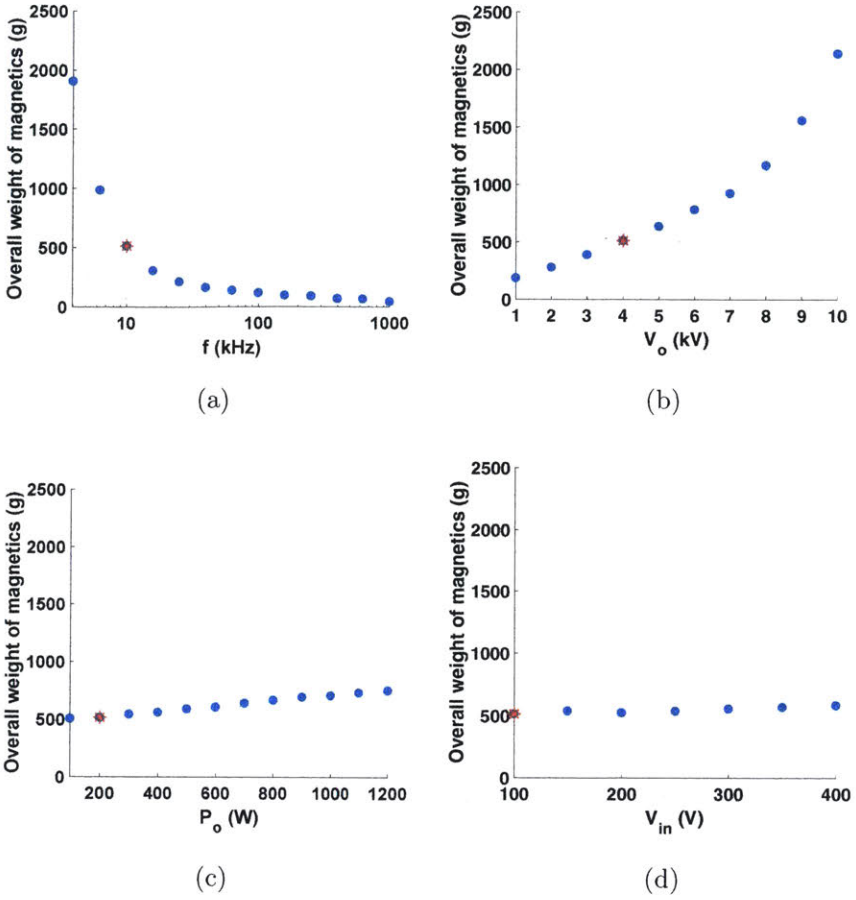
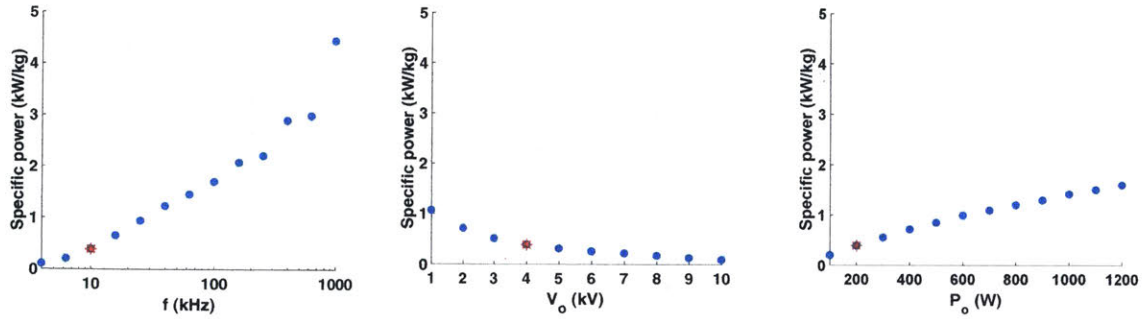


Figure 5-5: Overall weight of an example converter with resonant topologies as functions of (a) f, (b) V_{in}, (c) V_o and (d) P_o. The red asterisk marks: $V_{in} = 100\,\mathrm{V}$, $V_o = 4\,\mathrm{kV}$, $f = 10\,\mathrm{kHz}$, $P_o = 200\,\mathrm{W}$.



(a) vs DBD frequency f (b) vs DBD voltage V_o (c) vs DBD power P_o

Figure 5-6: The achievable specific power of an example converter with resonant topologies as functions of f, V_o and P_o. The red asterisk marks: $V_{in} = 100\,\mathrm{V}$, $V_o = 4\,\mathrm{kV}$, $f = 10\,\mathrm{kHz}$, $P_o = 200\,\mathrm{W}$.

the decoupled thruster), the overall converter weights ~500 g and the specific power is ~0.5 kW/kg. It is more "weight efficient" to use the resonant topologies for high-frequency high-power DBD where the specific power significantly increases.

5.2 Non-resonant topologies

Converters based on non-resonant topologies can be modular and often stacked in series for higher voltage and in parallel for higher power. In addition, magnetics are not designed to resonate at the DBD frequency, but in each dc-dc converter module to operate at a higher switching frequency than the DBD frequency.

As an example implementation of non-resonant topologies, we choose a resonant-transition boost converter (RTC) [112, 113] operating at 1–2 MHz as the dc-dc converter (Fig. 5-7) for its high frequency operation, good regulation capability and reasonably wide range of gain.

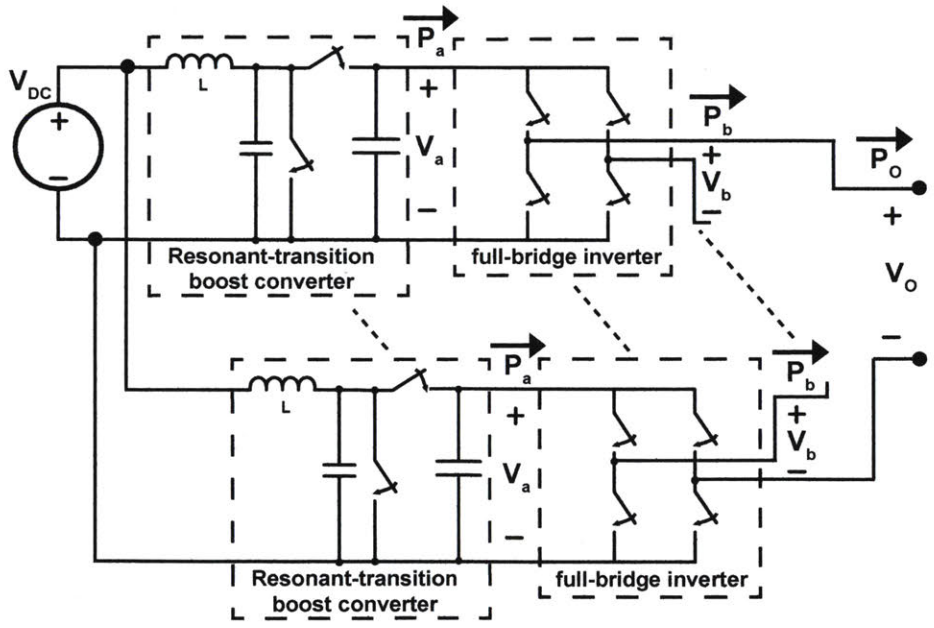


Figure 5-7: An example implementation of non-resonant topologies.

This section studies the achievable weight of the example converter in Fig. 5-7 and compares it with that for resonant designs in Section 5.1. We only explore how the weight scales with the dc input voltage V_{DC}, DBD voltage V_o and DBD power P_o and

assume it is insensitive to the DBD frequency f up to 100 kHz. f largely depends on the switching frequency of the full-bridge inverter, which can be in MHz range with proper switch, gate driving, and control implementations.

Section 5.2.1 studies the weight of the RTC changing with V_{DC}, voltage gain $G_a = V_a/V_{DC}$, and P_a (labeled in Fig. 5-7).

Section 5.2.2 studies the weight of the full-bridge inverter stage, as commonly used in the literature [13, 72].

Section 5.2.3 combines Section 5.2.1 and 5.2.2 and finds the overall converter weight when varying V_{DC}, V_o, and P_o.

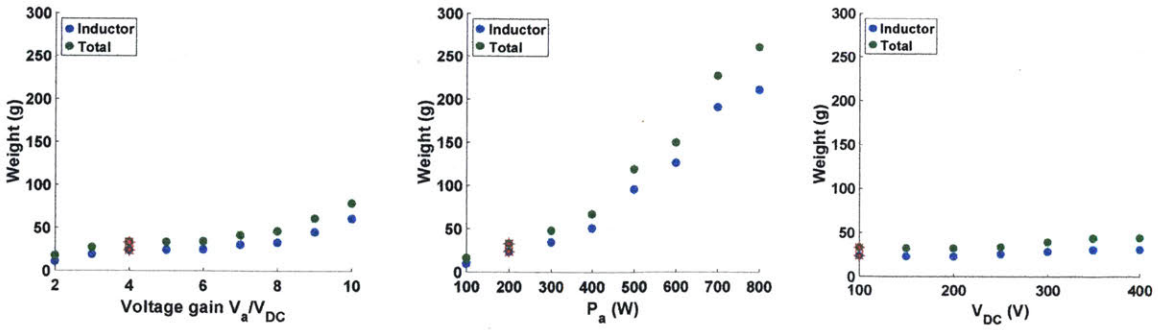
5.2.1 Dc-dc regulation stage

The weight of a RTC is dominated by its inductor and printed circuit board (PCB). The design of the RTC inductor references the work in [112, 113]. See Appendix G.3 for all simulated designs in this section. Below we only present and interpret the weights of these designs.

The weight study of the RTC inductor is similar to that in Section 5.1 except: 1) the inductance and the maximum current are calculated following the operating principles of the RTC. 2) since the inductor current is dc-biased, we include dc-current in the copper loss calculation.

In addition, we assume the output capacitance is set by the ripple requirement (10%) and calculate the capacitor weight by assuming a density of 0.01 g/nF (a medium density of capacitors rated at 1 kV, see Fig. 5-9c). We calculate the PCB weight by assuming the PCB area is 3 times that of the inductor area and the density is 4.39 mg/mm^2, that of a standard 4-layer PCB. We use a 4-layer PCB because the high-frequency RTC requires complicated PCB layouts for its gate driving circuits.

Figure 5-8 shows that the weight of the RTC is dominated by the inductor as expected and increases with V_{DC}, G_a and P_a. Compared with the inductor in the resonant tank, the RTC inductor weight increases more than linearly with power. This is because the inductor is dc-biased and operates at ~1–2 MHz, resulting in severer core and copper losses, a larger core is needed to dissipate the loss. Thus in



(a) (b) (c)

Figure 5-8: Weight of a resonant transition boost converter as functions of (a) RTC voltage gain V_a/V_{DC}, (b) P_a and (c) V_{DC}. The red asterisk marks the same reference point across all sweeps: $V_{DC} = 100\,\text{V}$, $G = 4$ and $P_a = 200\,\text{W}$.

the case of high power and high voltage gains, one should consider other topologies such as resonant dc-dc converter where the inductor is carrying ac current for the weight optimized design.

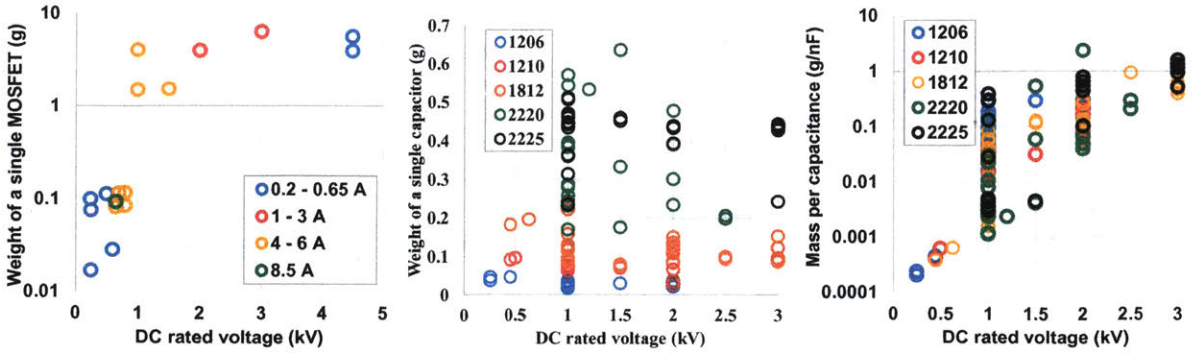
5.2.2 Inverter

We estimate the weight of a full-bridge inverter as the sum of that of the PCB, capacitors and MOSFETs.

Weight survey of MOSFETs and capacitors

Figure 5-9a shows a weight survey of selected MOSFETs in the range of 0.2 to 4.5 kV and 0.2 to 8.5 A. The weight of the MOSFET increases from on average 0.1 g to 2 g then to 5 g as its voltage rating jumps from $< 1\,\text{kV}$ to $> 1\,\text{kV}$ then to $> 3\,\text{kV}$. This is mainly due to changes in the packaging, and in the range of interest, the packaging depends strongly on the voltage rating and not so much on the current rating.

Figure 5-9b and Fig. 5-9c shows the mass and the mass per capacitance (g/nF) of selected capacitors in the range of 0.2 to 3 kV and 0.1 nF to 0.47 µF. The weight varies widely across packaging, capacitance and manufacturers, but in general, capacitors with higher rated voltage exhibit higher mass per capacitance.



(a) (b) (c)

Figure 5-9: Weight of selected off-the-shelf (a) MOSFETs plotted against their rated voltages and grouped by their rated currents; (b) weight and (c) weight per capacitance of selected off-the-shelf capacitors plotted against their rated voltages and grouped by their package size. See Table. G.6 and Table. G.7 in Appendix G for a list of all MOSFETs and capacitors considered.

Weight of a full-bridge inverter

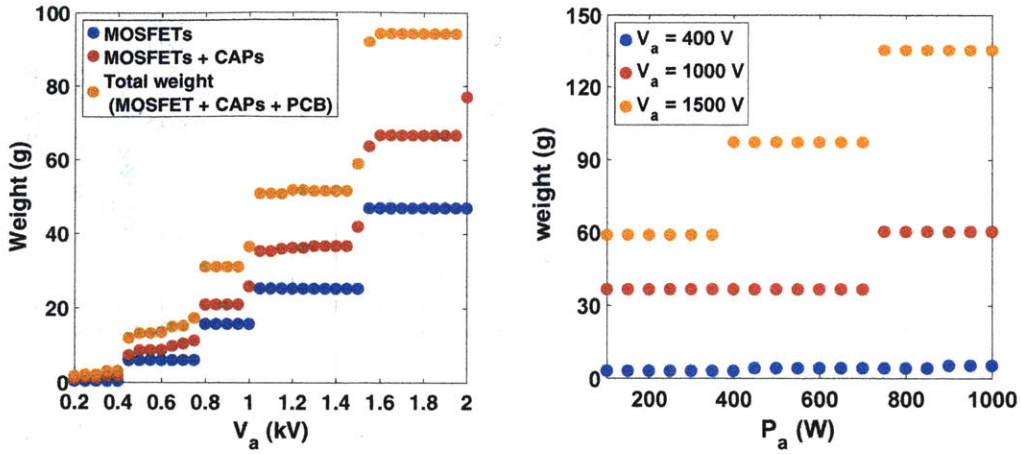
In this section, we only estimate the weight of one full-bridge inverter. For an input voltage V_a, MOSFETs with a DC rated voltage $\geqslant 2V_a$ are selected. For a certain P_a, MOSFETs with a DC rated current $\geqslant 4P_a/V_a$ are selected[3]. If none is available, we consider paralleling MOSFETs to carry the full current[4]. We assume an output capacitor of 1 µF across all designs.

For each operating point, we select the lightest MOSFET and capacitors from the pool in Fig. 5-9 and add up their weights. We calculate the PCB weight by assuming the PCB area is twice the area taken by MOSFETs and capacitors and the density is 3.3 mg/mm^2, that of a standard 2-layer PCB. We use a 2-layer PCB because the full-bridge inverter has relatively simple PCB layouts.

Figure 5-10a shows at a fixed power (P_a =200 W), the weight of a full-bridge inverter increases with its input voltage discretely, with each step corresponding to

[3]We de-rate the MOSFET voltage rating by 50% and the DC current rating by 75%. We de-rate more for the current because the current carrying capability of a MOSFET largely depends on its thermal design. Here we consider no special cooling design.

[4]Here we only consider paralleling MOSFETs to carry more current but not stacking them in series to block more voltage since it is practically easier to design the driving circuits for the former than the latter.



(a) (b)

Figure 5-10: Weight of one full-bridge inverter scaling with (a) inverter input voltage V_a when holding $P_a = 200\,\mathrm{W}$; (b) P_a at different V_a. Both figures suggest the weight depends heavily on the MOSFETs.

a change in MOSFET packaging. Figure 5-10b shows the weight stays relatively flat with power at low input voltages (because low-voltage lightweight MOSFETs are used), but increases at high voltage and high power (have to parallel heavy high-voltage MOSFETs).

Figure 5-10 suggest that 1) the weight of a full-bridge inverter depends heavily on available MOSFETs. 2) for the same output voltage, stacking several low-voltage inverters in series may weigh less than one high-voltage inverter (compare $V_a = 0.5\,\mathrm{kV}$ and $V_a = 1\,\mathrm{kV}$ in Fig. 5-10a).

5.2.3 Overall converter

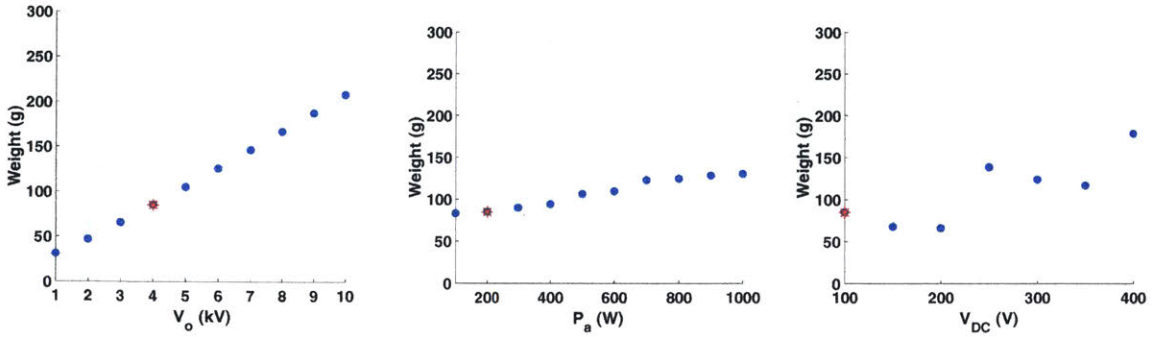
The above analysis indicates that in the range of interest, the weight of a RTC scales up more than linearly with its output power, and the weight of a full-bridge inverter scales up more than linearly with its output voltage. Thus intuitively, stacking multiple modules of low-voltage low-power dc-dc converters and full-bridge inverters can potentially yield a lighter overall weight than one high-voltage high-power converter.

We verify this by analyzing the overall weight of the converter. For each operating point defined by V_{DC}, V_o, and P_o, the intermediate bus voltage V_a is swept between

$2V_{DC}$ and V_o. When $V_a < V_o$, we assume V_o/V_a modules (each module contains a RTC and a full-bridge inverter) are stacked in series at the output. Each RTC and each inverter processes only a fraction of the total output power $P_a = P_o V_a/V_o$. The lightest designs of the RTC and the inverter are selected. In addition, for a design with more than one module, more supportive materials such as connectors and cables are needed for communications among modules. We assume an additional 3 g per module is added[5]. The overall weight of the converter is the sum of all modules and all supportive materials.

Figure 5-11 and Fig. 5-12 plots the lightest achievable weight and the specific power of the overall converter respectively, changing across each operating parameter. All designs choose to keep V_a as small as possible (at $2V_{DC}$, the smallest in the sweep), thus P_a as small as possible, and stack these low-voltage low-power converters in series. As a result, the supportive materials account for a major part of the overall weight.

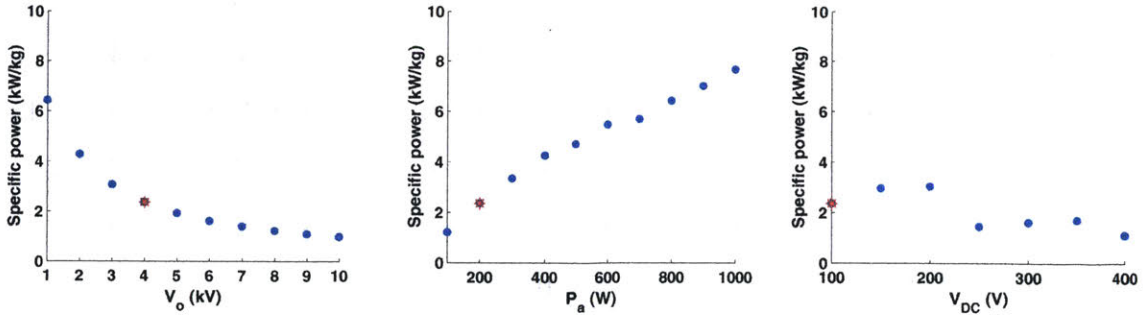
The overall weight increases linearly with V_o (Fig. 5-11a) due to the linear increase in the number of modules. At V_o =10 kV, the lightest design that yields ~210 g is 50 of 200 V modules stacked in series at the output. In practice, this may be undesirable because of 1) the complexity of the communications among modules. 2) the feasibility of building such a converter with robust structure.



(a) (b) (c)

Figure 5-11: Overall weight of an example converter with non-resonant topologies (Fig. 5-7) as functions of (a) DBD voltage V_o, (b) DBD power P_o and (c) dc input voltage V_{DC}. The red asterisk marks the same reference point across all sweeps: V_{DC} = 100 V, V_o = 4 kV, f = 10 kHz, P_o = 200 W.

[5]This is the weight of a 4-line cable (Digikey P/N 455-3038-ND) with associated headers.



(a) (b) (c)

Figure 5-12: Mirroring Fig. 5-11, specific power of an example converter with non-resonant topologies (Fig. 5-7) as functions of (a) DBD voltage V_o, (b) DBD power P_o and (c) dc input voltage V_{DC}. The red asterisk marks the reference point: $V_{DC} = 100\,\text{V}$, $V_o = 4\,\text{kV}$, $f = 10\,\text{kHz}$, $P_o = 200\,\text{W}$.

The overall weight increases slowly with P_o, as shown in Fig. 5-11b. In these designs, V_o is fixed at 4 kV and 20 200 V modules are stacked in series at the output. The power processed by each module increases from 5 to 50 W, driving up the weight of the RTC slowly. In addition, the weight of MOSFETs and thus the inverter stay relatively flat as the current increases in the range of interest.

Figure 5-11c shows that the overall weight of the converter increases discretely with V_{in}. The discontinuity is due to the change of MOSFET in the inverter to a higher voltage rating and heavier package. With in each group, for example, 250 to 350 V, higher V_{DC} requires fewer modules thus lower overall weight to achieve the same V_o.

To drive a DBD at 10 kHz, 4 kV and 200 W, the overall converter consists of 20 modules, weighs ~90 g and the specific power is ~2.2 kW/kg. However, if we were to limit the number of modules to 10, the lightest design becomes ~145 g and the specific power is ~1.4 kW/kg.

5.3 Proposals of lightweight DBD converters

Section 5.1 and Section 5.2 show that in the range of interest,

- Resonant topologies are more "weight efficient" at high frequency and/or high

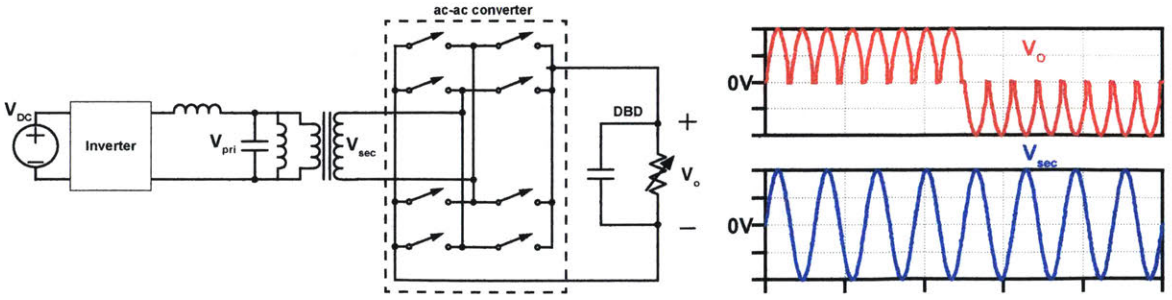
power compared to the non-resonant topologies

- Non-resonant topologies are in general more "weight efficient" than resonant topologies, especially at low input voltage, low output voltage and high power. But the achievable weight highly depends on available MOSFETs and the number of modules allowed. In addition, for a high frequency DBD in the MHz range, non-resonant topologies may be infeasible due to the limited switching frequency of MOSFETs.

In this section, we propose three alternative converter designs inspired by both topology categories for the DBD applications. All designs operate as voltage sources and are especially "weight efficient" when powering low-frequency DBDs. The reference design point remains at $V_{DC} = 100\,\mathrm{V}$, $V_o = 4\,\mathrm{kV}$, $f = 10\,\mathrm{kHz}$, $P_o = 200\,\mathrm{W}$.

5.3.1 High-frequency transformer with frequency conversion

Inspired by the "resonant topologies", instead of designing the magnetics at the DBD frequency, we consider the use of a high-frequency resonant tank and transformer with an additional ac-ac converter on the secondary of the transformer, which converts the high-frequency ac to the DBD frequency (a lower frequency). An example implementation is a cyclo-converter [114] (see Fig. 5-13).



(a) Schematics

(b) An example when an ac is converted to one-fourth of its frequency.

Figure 5-13: Schematics and waveforms of the proposed frequency conversion solution (as an example, the ac-ac converter is implemented as a cycloconverter).

The weight of magnetics is reduced by switching at a higher frequency. In Fig. 5-5a, at the reference design point, a converter with the traditional resonant topologies

weights 500 g. If we were to switch at 500 kHz, the weight can be reduced to ~70 g.

However, the switches in the ac-ac converter add additional weight. They need to be active-controlled switches and rated for the DBD voltage and power. A back-of-the-envelope calculation using the weight survey in Fig. 5-9a suggests that to drive a 4 kV and 200 W DBD, all switches would add ~30–100 g[6].

Overall, this solution yields ~100–170 g and a specific power of ~ 1.2–2 kW/kg. One challenge of this option is that the switches, the associated gate driving and control circuits in the ac-ac converter are all referenced to a high ac voltage with high dV/dt, which may inject non-negligible noises in the system.

5.3.2 High-frequency transformer with burst-mode control

Similarly inspired by the "resonant topologies", we consider the use of a high-frequency resonant tank and transformer with burst-mode control. The converter topology is the same with Fig. 5-1a. The burst-mode is implemented in the control of the inverter to pulse the output on and off. An example waveform is shown in Fig. 5-14. While the output frequency content is quite dispersed with this technique, it can yield the desired DBD ion generation. See Appendix G.2 for more detailed explanation and characterization of this approach.

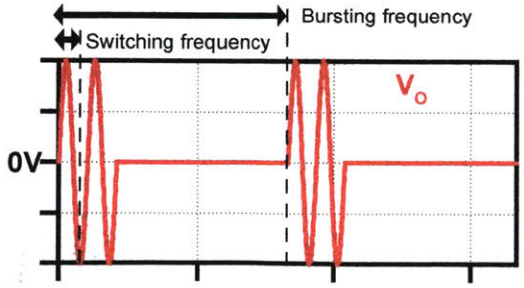


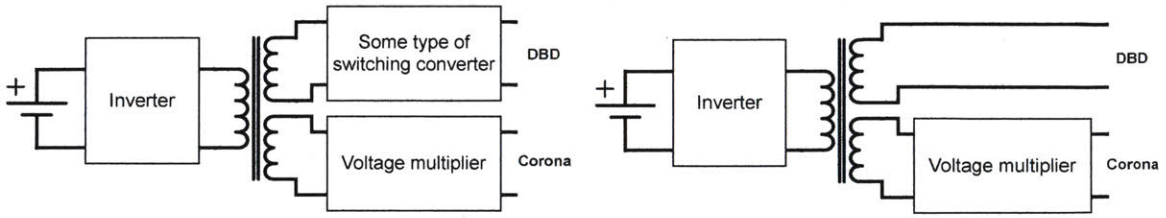
Figure 5-14: An example waveform of the proposed burst-mode solution. The inverter drives the resonant tank at high frequency for a few cycles and stop for some cycles.

If we were to switch the transformer at 500 kHz, the weight of magnetics components is reduced to ~70 g and no additional weight will be added. Overall, this

[6]The upper bound is calculated by assuming 8 pairs of two 4.5 kV-rated MOSFETs in series are used. The lower bound is calculated by assuming 8 pairs of 10 800 V-rated MOSFETs in series are used. Both bounds include the PCB weight and a margin to account for miscellaneous ICs.

solution yields a specific power of ~2.8 kW/kg.

Another benefit of the two high-frequency transformer based solutions is that the transformer can be shared with the high voltage dc-dc converter for the corona thruster (Fig. 5-15), further reducing the weight by integrating magnetics. Overall, the hybrid solutions seem promising for powering the decoupled thruster.



(a) Hybrid converter with switching converters on the transformer secondary

(b) Hybrid converter with burst-mode control in the inverter.

Figure 5-15: Hybrid converter for the decoupled thruster. The transformer can be shared between the DBD thruster and the Corona thruster.

The burst-mode solution is especially attractive, though with a few challenges in the implementation: 1) depending on the requirement of the thruster, separate controls of the DBD and the corona may need to be developed; 2) when designing the integrated magnetics, one needs to take into consideration the dynamics of both plasma loads; 3) likely additional weight will be added to facilitate the control.

5.3.3 Switched-capacitor multi-level inverter based solution

Inspired by the "non-resonant topologies", we use a dc-dc stage cascaded with a multi-level switched-capacitor inverter which can potentially provide additional voltage gain at a reduced weight.

We choose the multi-level switched-capacitor topology in [115] among other variations [116–118] because it can produce both a unipolar and a bipolar output with a small number of switches per stage. A detailed weight and efficiency study of this option will be presented in Suzanne O'Meara's master's degree thesis[7].

[7]The weight surveys in Fig. 5-9 are used. The weight of ICs in the driver circuits are also taken into considerations for a more accurate estimation.

We further analyze the combined weight of the switched capacitor multi-level inverter (SCMLI) and a front-end resonant transition boost converter (RTC). For a fixed V_{DC},V_o and P_o, we adjust the intermediate bus voltage V_a (between the RTC and the SCMLI) to find the lightest design.

For $V_o = 4\,\text{kV}$ and $P_o = 200\,\text{W}$, the total weight of the converter changing with V_{DC} and V_a is shown in Fig. 5-16. Across all simulated V_{DC}, the intermediate bus voltage V_a should be set in between 300 to 400 V. Higher than this voltage would require heavier MOSFETs with higher voltage rating; lower than this voltage would require a large voltage gain from the SCMLI (more stages and higher device count). In addition, we set V_{DC} to be in between 100 to 160 V[8].

Figure 5-17 shows the finalized schematics of the RTC with an 11-stage switched-capacitor multi-level inverter. The RTC converts 100 to 150 V to an intermediate 400 V and the 11-stage SCMLI multiplies and inverts it to a 4 kV ac. Overall, this solution yields to an estimated weight of ~90 g and a specific power of ~2.2 kW/kg.

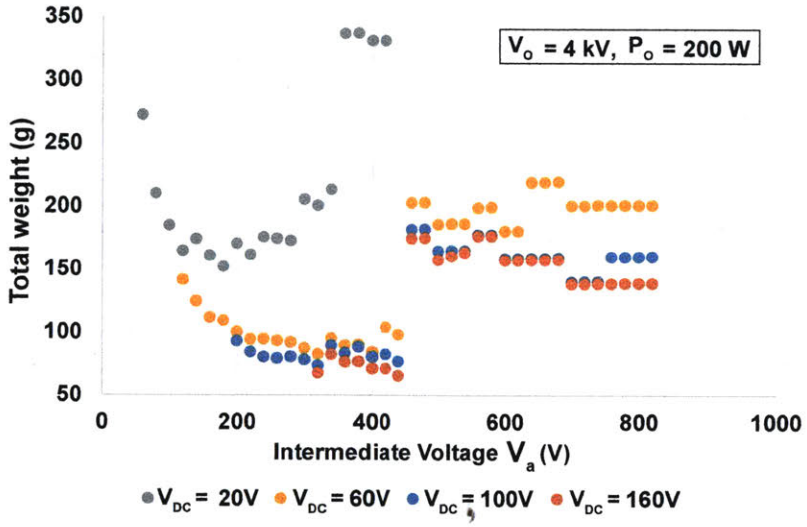


Figure 5-16: Weight of a resonant transition boost converter cascading with a switched-capacitor multi-level inverter

[8]In practice, V_{DC} may be set by external requirements or a system-level weight study combining the battery packs and the converter.

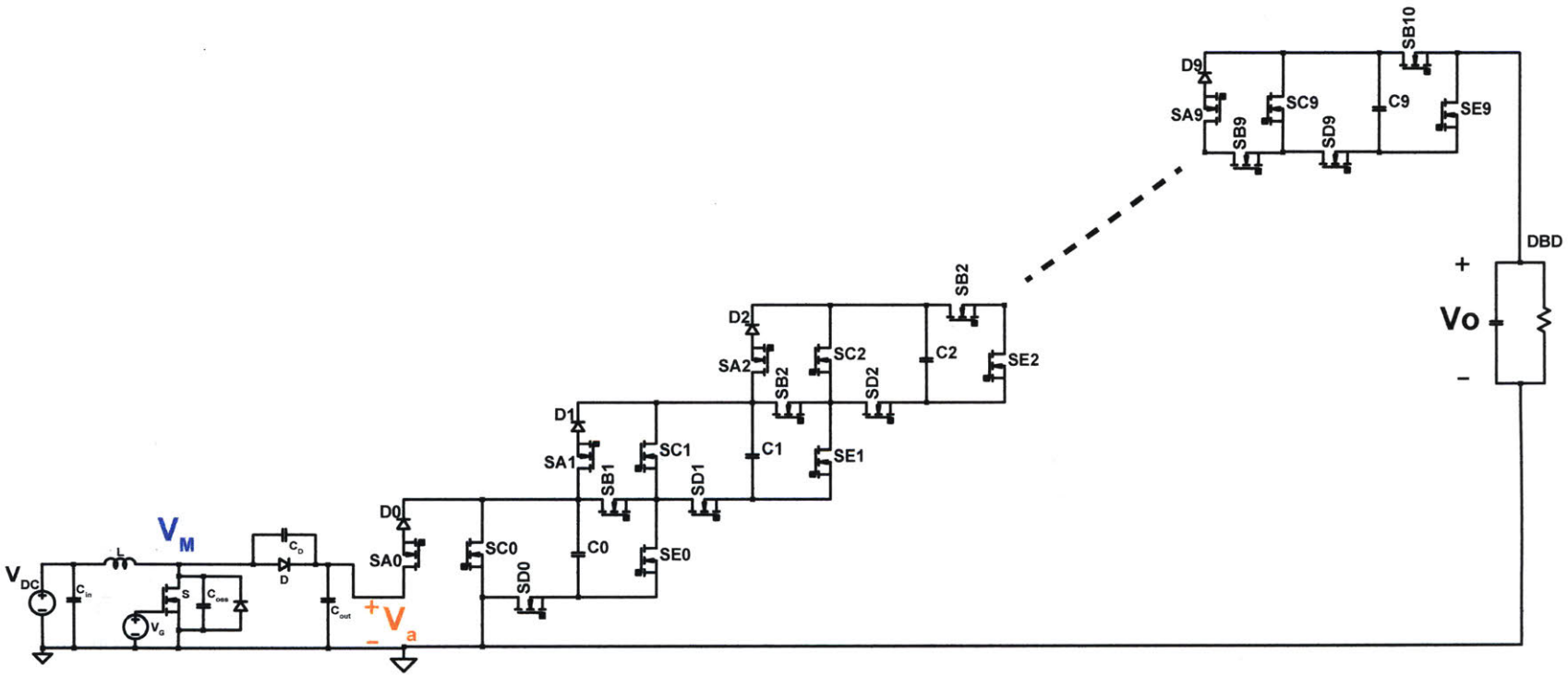


Figure 5-17: Schematics of a resonant-transition boost converter cascade with an 11-stage switched capacitor multi-level inverter. We start indexing the stage from 0. Stage 0 contains SA_0, SC_0, SD_0, SE_0. Stage i ($i = 1, 2, ..., 9$) contains 5 switches $SA_i, SB_i, SC_i, SD_i, SE_i$. The last stage only contains switch B SB_{10}.

5.4 Experimental results

In this section, we build and test both the high-frequency transformer based converter with burst-mode control ("burst-mode solution" for short in the following content) and the switched-capacitor multi-level inverter based solution ("SCMLI solution" for short) with a DBD load. Preliminary experimental results show both solutions can drive the DBD load. More integration tests of the DBD and the developed prototypes is in progress and will be carried out and recorded in the Master's degree thesis of Suzanne O'Meara.

5.4.1 Burst-mode solution

The inverter and the high-voltage transformer built in Chapter 2 are reprogrammed to drive a DBD load in burst-mode. The DBD load is built in the same way as in Chapter 6. The inverter switches at 590 kHz and bursts at 200 Hz to 12 kHz.

The power draw of the DBD is measured across all tests and compared to the power draw when driven by a sine wave and they show consistency (see Fig. 5-18). This consistency is the preliminary proof that the burst-mode operation can generate ions similar to a sine-wave DBD. Further tests of whether these ions produce similar thrust compared with a sine wave DBD are undergoing.

See Appendix G.2 for the details of the driving circuit, the load, experimental waveforms and the power measurements.

5.4.2 Switched-capacitor multi-level inverter based solution

A prototype converter of a RTC cascaded with a 11-stage SCMLI was built, as shown in Fig. 5-19. The RTC is designed to take 100–150 V input voltage and converts to 300–400 V (see details in Appendix G.3). Figure 5-20a shows the RTC switching node voltage (V_M in Fig. 5-17) when it converts 70 V to 300 V, outputting 112 W. At this operating point, the RTC switches at 1.5 MHz and the efficiency is 98 %[9].

[9]The inductor used in this test is bigger than needed. A new inductor with smaller form factor is being constructed.

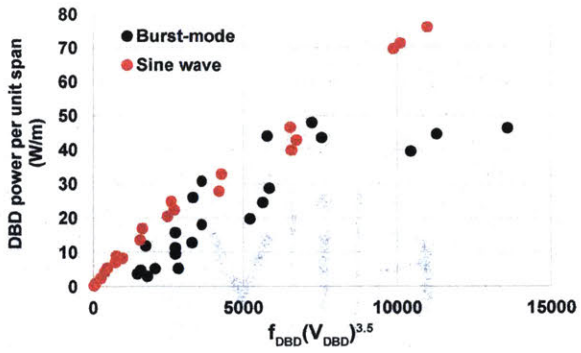
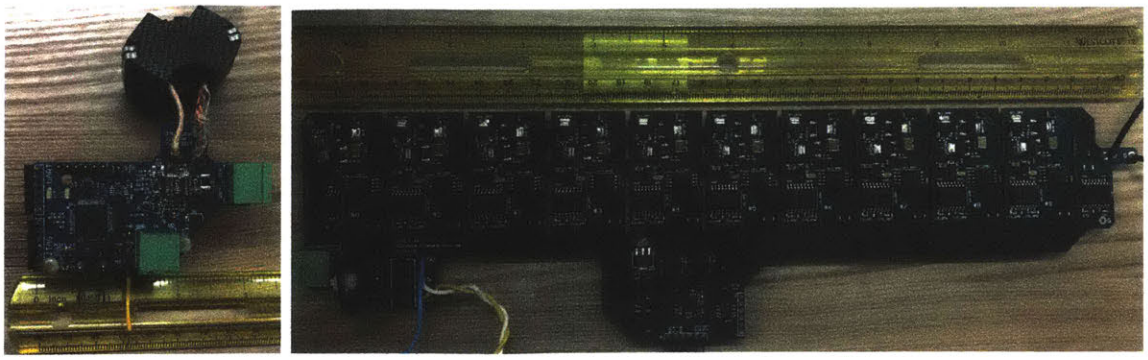


Figure 5-18: Unit power draw of a DBD load when driven by an inverter and a transformer in burst-mode. The general trend is consistent with the power draw of a sine-wave DBD. The x axis plots the frequency of the DBD times the voltage of the DBD to the power of 3.5 (a metric commonly used to characterize the DBD power draw across literature.)

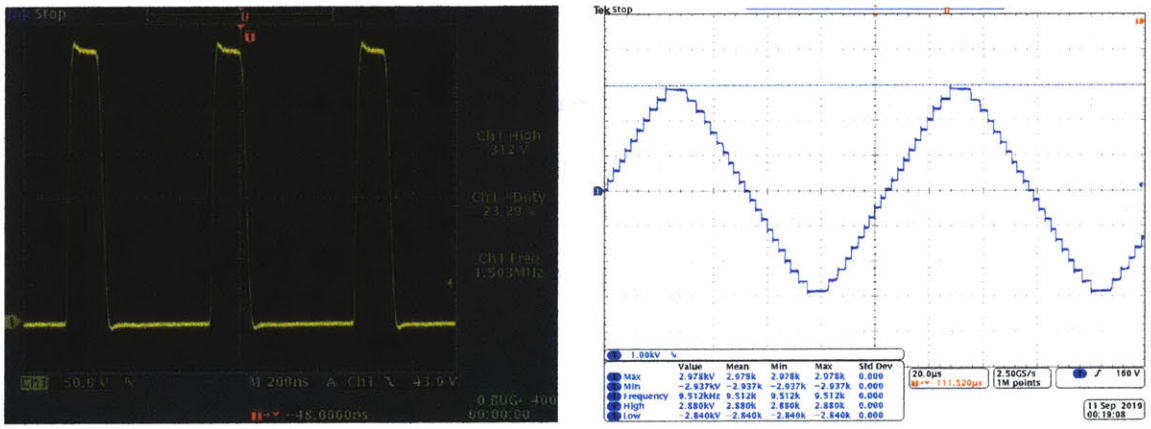
The design and implementation of the SCMLI was collaboratively done with Suzanne O'Meara. Part of the implementation details is explained in Appendix G.4. Figure 5-20b shows the converter outputting a 2.88 kV 10 kHz ac at 91 W from a 300 V dc input. The efficiency of the SCMLI at this operating point is 86%. The weight distribution of both the RTC and the SCMLI are listed in Table 5.1.

A few challenges identified when building this SCMLI include: 1) the switches in one stage do not necessarily switch in a complementary pattern, and each stage cascades to the previous stage, so one needs to take extra care when designing the gate driving circuits. See Appendix G.4 for more details; 2) the parasitic capacitance to several flying nodes introduces unwanted charges and results in voltage build-up across some MOSFETs (see Appendix G.4.4 for more details); 3) The floating power supplies needed to drive each stage take increasing isolation voltage as the output voltage and numbers of stages increase; the weight and lifetime tradeoffs associated with this design choice remain to be fully explored for the general design case.



(a) (b)

Figure 5-19: Prototypes of (a) the resonant transition boost converter (RTC) and (b) the switched-capacitor multi-level inverter. The inductor in the RTC boost is outdated and a new one with smaller form factor is under construction.



(a) (b)

Figure 5-20: Experimental waveform of (a) the RTC switching node voltage when converting 70 V to 300 V and outputting 112 W and (b) the SCMLI generating ~3 kV 91 W at 10 kHz.

Prototype	Parts	Weight (g)	Percentage (%)
RTC	Inductor†	25	18
	PCB	8	6
	The rest	10	7
SCMLI	PCB	57	41
	Components	38	27
Total		138	100

Table 5.1: Weight breakdown of the RTC and the SCMLI prototype
† This inductor is the small one under construction.

Part III

Integration with the Electro-Aerodynamic (EAD) Technology

Chapter 6

Collaboration work on the first flight of an EAD aircraft and improved EAD thruster

The design, optimization and construction of the EAD thruster and EAD-propelled aircraft have been carried out alongside this thesis work by colleagues in the MIT Laboratory of Aviation Environment (LAE). One objective of the thesis is to integrate the developed electrical system with the aircraft and demonstrate the feasibility of the EAD technology.

In December 2017, we demonstrated the first flight propelled by EAD. We flew a fixed wing EAD airplane with 5 m wingspan 10 times and showed that it achieved steady-level flight. The work has been published in [1]. All batteries and the converter in Chapter 2 were carried on-board.

Furthermore, to improve the efficiency and the practicality of the EAD aircraft, we developed a second-generation EAD thruster with dielectric-barrier-discharge, further increasing the thrust per unit power generated.

Section 6.1 presents the integration work of the 1st-generation high voltage dc-dc power converter (HVPC) with the first-generation EAD aircraft. Section 6.2 presents the design and characterization of the second-generation EAD thruster.

The work in Section 6.2 (published in [7]) and another work at MIT by Xu [6] set

the electrical requirements of high voltage power converters for the second-generation EAD plane, which prompt the work in Chapter 4 and 5.

Additional miscellaneous collaboration work are summarized in Appendix H, including developing current measurement circuits and an isolation transformer for the EAD experiments, as well as a RF communication system.

6.1 First-generation EAD

Figure 6-1 shows that the first generation EAD aircraft consists of the EAD thruster (two sets of four parallel electrodes), airframe (nosecone, fuseslage, tail and wings) and electrical components (a 200 V battery pack and the 1st-generation HVPC developed in Chapter 2). The electrodes generate thrust purely based on corona discharge effect.

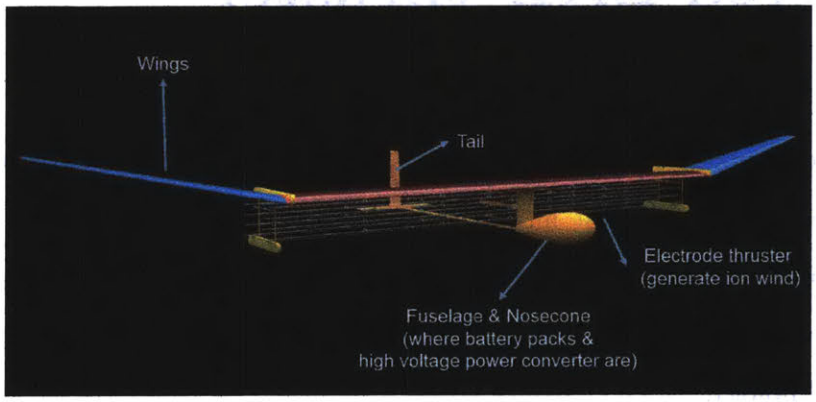


Figure 6-1: System breakdown of the 1st-gen EAD aircraft (by Kieran Strobel)

Due to the danger of the high voltage, before every flight test, intense integration tests were conducted to ensure safety and functionality of all sub-systems.

6.1.1 Integration tests of the 1st-gen HVPC with the 1st-gen EAD aircraft

The functionality of each sub-system has been tested individually before the integration tests. The objectives of these tests are to: 1) ensure inter-system functionality by simulating actual operations in the field; 2) conduct static laboratory thrust measurements to ensure the overall system can generate sufficient thrust for flight.

Functionality tests

The HVPC was tested on the benchtop with the battery pack and the full-scale EAD thruster step by step (details in Appendix H). The following three aspects of the HVPC were verified through tests:

- Accessory circuits in the HVPC that facilitate the flight, including: start up circuit, on-board data recording, LED indicator[1], receiver of a hand-held RC controller[2], and an emergency cut-off switch[3]. See Table D.13 for a detailed list of specifications.

- Sensing and close-loop control: three electrical data points (battery voltage, battery current and 1/6 of the total output voltage[4]) are measured and recorded on an on-board FRAM. The HVPC is also programmed to adjust the switching frequency to fix the output voltage at a set point.

- Shut off conditions: the HVPC is designed to shut off under the following conditions: overtime, battery pack under voltage, battery pack over current, RC controller throttle in "turn off" position, the emergency switch disconnects.

Static thrust tests

"Static thrust" refers to the thrust generated by the thruster while the aircraft is in stationary position. The difference between it and the actual thrust generated during flight ("dynamic thrust") is small and can be ignored.

The purpose of the static thrust tests is to 1) verify the thrust and thrust-to-power of the full-scale EAD thruster when powered by the HVPC; 2) create a map of the electrical and thrust data, which will be used to back out the thrust during flight.

[1]Green means high voltage (HV) off, blue means charging the input caps and red means HV on.
[2]A throttle of the controller controls the HVPC to start or stop outputting the high voltage.
[3]There is a push-button emergency switch mounted at the bottom of the fuselage and in line with the logic power. When the aircraft lands, the emergency switch is triggered and cuts off the logic power.
[4]The output voltage is calculated by multiplying the measured voltage across one of the 6-stage full-wave voltage multiplier by 6.

We followed a procedure similar to that proposed in [2, 119]: part or all of the aircraft was suspended vertically from a digital balance within a large insulating frame (Fig. 6-2). The balance is able to measure any net vertical force produced by the thrusters. The thruster was powered by either a benchtop high voltage power supply or the prototype HVPC. Tests were performed to determine the effect of various experimental factors on the accuracy of force measurements, including ground proximity, nearby object charging, and connector wire tension. None of these factors showed a significant effect with our experimental setup.

Figure 6-3 shows the static thrust as a function of the HVPC output voltage and input power (i.e., battery power). The optimal operating point is set at 40.3 kV, producing a static thrust of ~3 N. This value has been consistent with expected thrust required to achieve a steady-level flight of the EAD aircraft. Static tests were performed both before and after flight tests, to measure the impact of possible physical damage to the electrode during the flight tests.

Figure 6-2: Static thrust test stand (the HVPC is assembled with the aircraft)

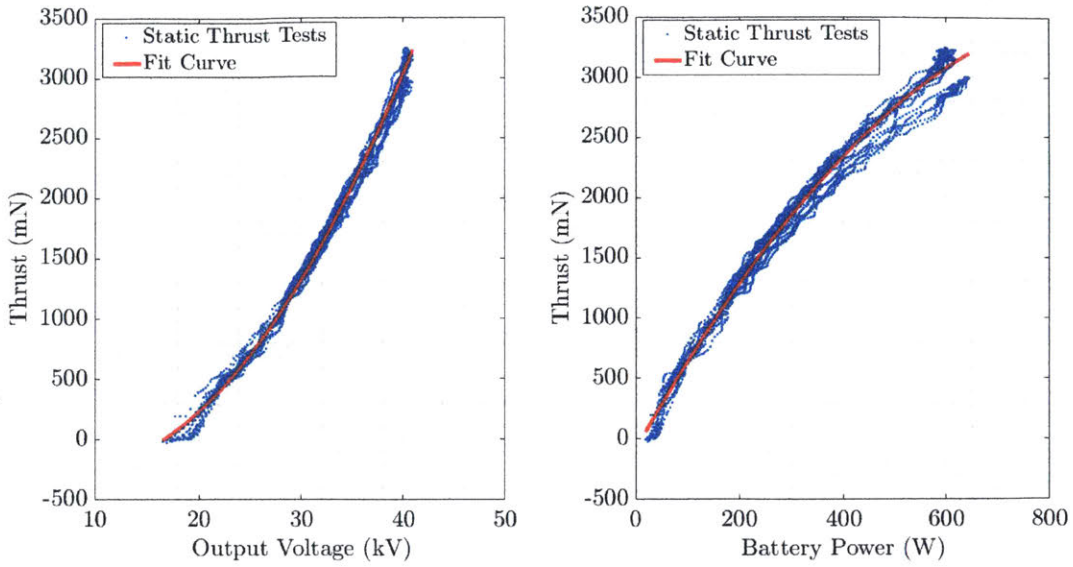


Figure 6-3: Static thrust measurements as a function of voltage (left) and battery power (right)

6.1.2 Flight tests

Flight tests were conducted in the Johnson Athletic Center at MIT. The indoor space was chosen so that the aircraft could be operated in a controlled environment, minimizing the effects of wind and temperature.

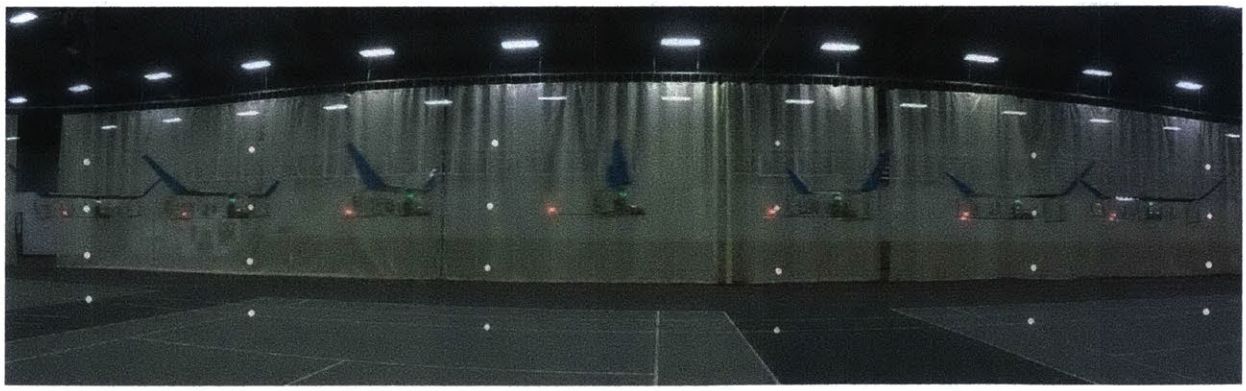
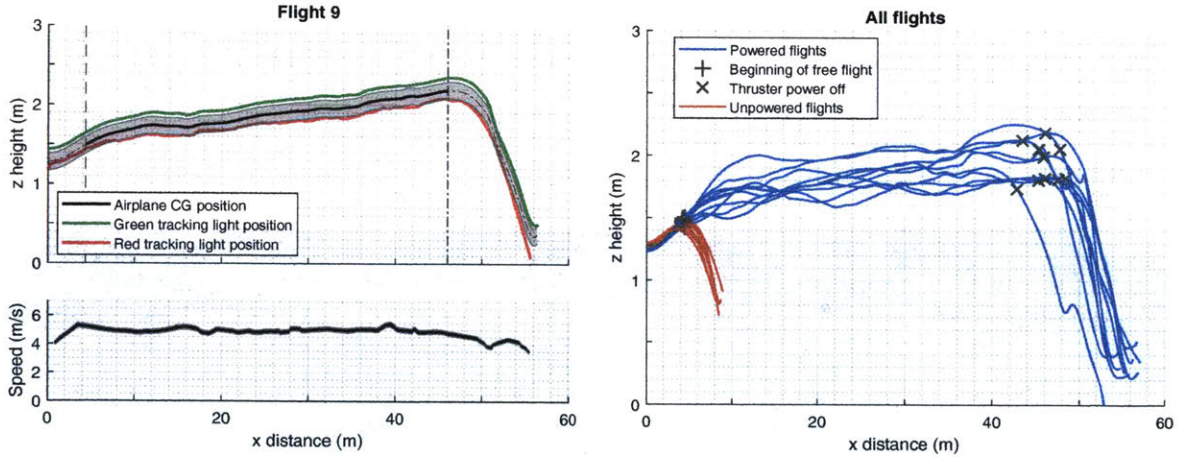


Figure 6-4: Time lapse of EAD aircraft in-flight. White reference markers are spaced 5m horizontally and 1m vertically. All results in Fig. 6-5 are presented in a Cartesian coordinate system with the x axis in flight direction, z axis upwards, and y axis pointing away from the camera (illustration by Haofeng Xu).

We performed ten flights with the full-scale EAD aircraft. Due to the limited length of the 60 m indoor space, we used a bungeed launch system to accelerate the

aircraft from stationary to a steady flight velocity of 5 m/s within 5 m, and performed free flight in the remaining 55 m of flight space. To demonstrate the effectiveness of an EAD thruster, we also performed 10 unpowered glides with the thrusters turned off, where the airplane flew for less than 10 m. We used cameras and a computer vision algorithm to track the aircraft position and determine the flight trajectory. The time lapse of one of the flight is shown in Fig. 6-4.

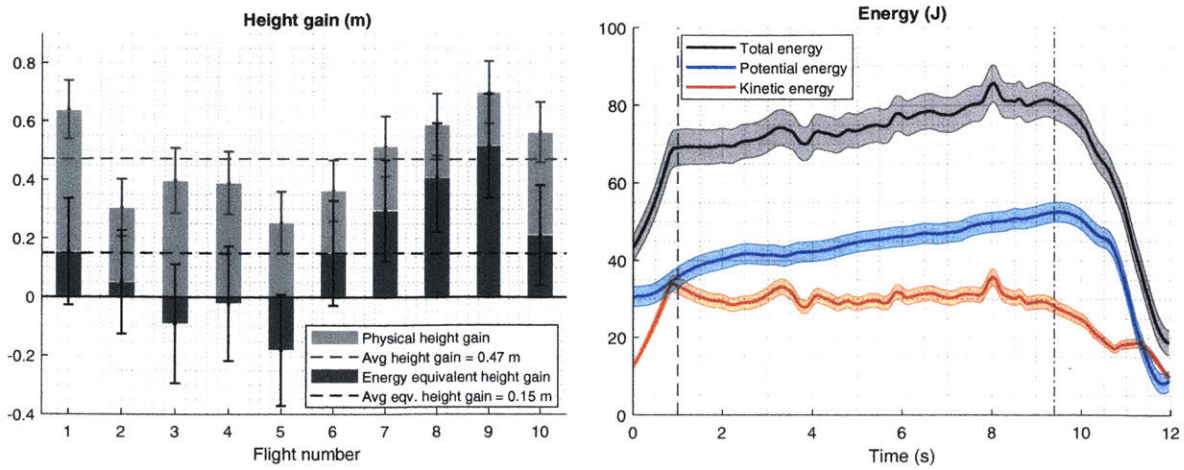
All flights gained height over the 8–9 s segment of steady flight, which covered a distance of 40–45 m (Fig. 6-5b). The average physical height gain of all flights was 0.47 m (Fig. 6-6a). However, for some of the flights, the aircraft velocity decreased during the flight. An adjustment for this loss of kinetic energy (Fig. 6-6b) results in an energy equivalent height gain, which is the height gain that would have been achieved had the velocity remained constant. This was positive for seven of the ten flights, showing that better than steady-level flight had been achieved in those cases.



(a) (b)

Figure 6-5: (a) Flight trajectory for a single flight. The segment of steady flight between launch and propulsion system power off is shown by the dark black line. The estimated position tracking error is shown in grey. (b) Trajectories for all 10 powered flights, and 10 unpowered glides. The steady segment of flight covered a distance of 40-45 m with a duration of 8-9 s.

In each flight, the HVPC was powered on 20 s before launch to allow the voltage to ramp up gradually from 0 to 40.3 kV, minimizing the risk of arcing. The aircraft was then launched and maintained on a straight and steady flight path. Around 5–10 m



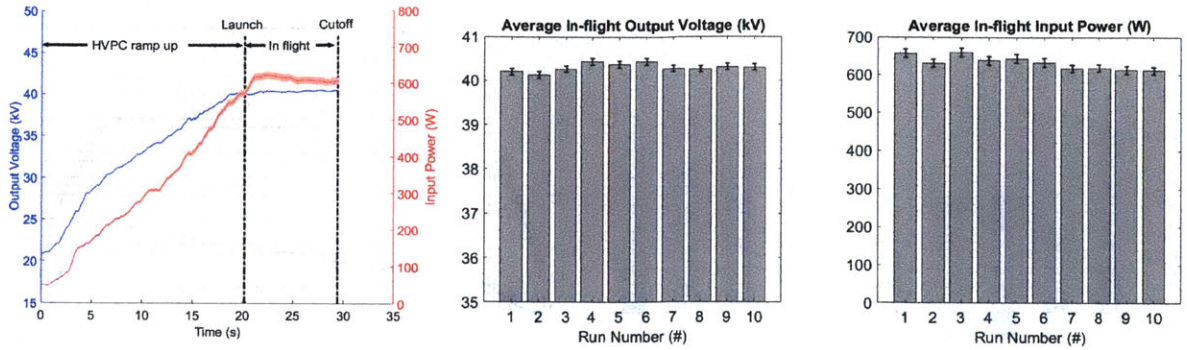
(a) (b)

Figure 6-6: Steady-level flight. (a) The physical height gain was positive for all flights, and the energy-equivalent height gain, which adjusts for the loss of kinetic energy during the flight, was positive for seven flights. Zero energy equivalent height gain indicates steady level flight; (b) The variation of kinetic, potential energy and total energy (which is the sum of kinetic and potential energies) during a particular flight: the potential energy increases substantially, while the kinetic energy remains approximately constant or decreases slightly.

from the end of the flight area, the HVPC was remotely powered off, and the aircraft glided to ground. The aircraft was then electrically grounded before being returned to the launcher in preparation for the next flight test. During the steady flight, the HVPC output around ~40.3 kV and drew an average of 600 W from the battery pack, as shown in Fig. 6-7b. The output voltage and battery power data recorded by the HVPC during an example flight is shown in Fig. 6-7a.

Using the static thrust data and the camera tracking data, we estimate that the thruster produced 3.2 N of thrust and flew at an average velocity of 4.8 m/s. Therefore, the aircraft realizes a thrust-to-power of 5 N/kW, which compares favorably with conventional airplane propulsion methods such as the jet engine. However, the overall efficiency was lower than typically achieved by conventional propulsion (and was not the objective here given the limited indoor test area for an uncertified airplane):

$$\eta = \frac{Tv}{P_{in}} = \frac{3.2 \times 4.8}{600} = 2.56\% \tag{6.1}$$



(a) (b)

Figure 6-7: (a) Output voltage and input power during one flight. (b) Averaged output voltage and input power for 10 flights.

Where T is the thrust, v is the average velocity of the aircraft in the direction of thrust and P_{in} is the average battery power. In order to obtain longer range and endurance for practical applications, future progress should be in the direction of increasing overall efficiency.

6.2 Second generation EAD thruster

We identified three research directions to improve the overall efficiency of an EAD aircraft: 1) more "weight efficient" electrical system (see Chapter 4). 2) more efficient thruster technology. 3) overall aircraft design that makes better use of the EAD technology.

In this section, we present collaborative work on the design and characterization of an improved EAD thruster. The EAD-propelled flying devices demonstrated thus far have used a direct current (dc) corona discharge to produce ions and the same dc field to accelerate them[5]. However, these corona discharge EAD devices are subject to a performance trade-off where increasing thrust reduces efficiency (thrust-to-power ratio). This is a key barrier to practical adoption.

We show that by using a dielectric barrier discharge (DBD) instead of a corona discharge to produce ions, while still using a dc field to accelerate them, higher thrust

[5]As used in the 1st-gen aircraft [1], tethered flight at the cm scale [120], and the untethered close-range hover by wireless power transmission [121]

and thrust-to-power can be achieved. We identify operating regimes for this thruster, optimize the electrical characteristics of the DBD ion source, and find that the thrust-to-power can reach up to 20 N/kW at a thrust per unit span of thruster of 50 mN/m, and up to 10 N/kW at 150 mN/m – in both cases approximately twice that of the equivalent corona discharge devices. With lower power draw for the same thrust, a DBD enhanced EAD thruster could increase the endurance of EAD airplanes, and begin to enable the design of practically useful solid-state aircraft.

6.2.1 The Trade-off of Existing EAD Devices

Two important figures of merit for an aircraft propulsion system are thrust-to-power and thrust density. High thrust-to-power, which is thrust force per unit input power, corresponds to lower energy storage and power supply requirements and therefore longer range and endurance. High thrust density, which is thrust force per unit span, area, or volume, reduces the size, weight, and aerodynamic drag of the propulsion system. The thrust-to-power of a corona discharge EAD propulsion system can be on the same order of magnitude as conventional propulsion such as the jet engine or helicopters rotors, however only at significantly lower thrust densities [4]. At higher thrust densities useful for airplane propulsion, the thrust-to-power decreases, and there exists a trade-off between high thrust-to-power and thrust density.

The thrust versus thrust-to-power trade-off in corona discharge EAD systems arises from the competing requirements of the ionization and acceleration processes. Both are necessary to produce a thrust force.

In a corona discharge thruster, a dc voltage of some tens of kilovolts is applied across two highly asymmetric electrodes, for example in a pin-to-mesh or wire-to-cylinder geometry. At sufficiently high voltage, a self-sustaining gas discharge which generates a supply of electrons and ions is formed at the smaller electrode (the emitter). For a positive corona, where the emitter is at a positive potential, positive ions travel under the applied electric field to the larger negative electrode (the collector). As ions travel from emitter to collector, they collide with neutral molecules and couple their momentum to the bulk fluid; this generates an ionic wind which produces a

thrust force in the opposite direction to ion flow.

The dc potential which forms the corona discharge for ion generation is the same dc potential which accelerates the ions for thrust generation. Using the same electric field for both processes reduces the engineering complexity and the weight of the power system.

The thrust force T produced can be calculated using a simplified one-dimensional model (developed in [122, 123] and verified through experimental results in [4, 5].)

$$T = \frac{Id}{\mu}, \tag{6.2}$$

where μ is the ion mobility, I is the total current, and d is the distance between electrodes. For a corona discharge, the current-voltage characteristic can be estimated by the semi-empirical Townsend relation [124]

$$I = I_{\text{corona}} = \begin{cases} 0, & V_a < V_0 \\ CV_a\left(V_a - V_0\right), & V_a \geqslant V_0, \end{cases} \tag{6.3}$$

where V_a is the applied dc voltage, V_0 is the corona inception voltage and C is a geometric parameter capturing the particular geometry of the electrodes. Thrust increases with higher applied dc voltage (and equivalently higher average electric field strength).

In contrast, the thrust-to-power is

$$\frac{T}{P} = \frac{T}{IV_a} = \frac{d}{\mu V_a} = \frac{1}{\mu \bar{E}} \tag{6.4}$$

where P is the electrical input power, and $\bar{E}$ is the average electric field between the electrodes. Thrust-to-power scales inversely with average electric field.

To summarize, thrust increases with higher average electric field strength, while thrust-to-power decreases with higher average electric field strength. This trade-off has been observed experimentally [2, 4, 5, 125].

6.2.2 Breaking the Trade-off with a Decoupled EAD Device

We propose a "decoupled" EAD device, where ions are produced by an independent ion source, removing the dependency of the current on the applied dc voltage. A decoupled thruster can produce more current, and hence thrust, than a corona discharge thruster with the same geometry and at the same applied dc voltage. Since the applied dc voltage determines the thrust-to-power, a decoupled thruster can produce more thrust at the same thrust-to-power (or equivalently the same thrust at higher thrust-to-power by lowering the applied dc voltage).

The independent ion source used in our decoupled thruster is the dielectric barrier discharge (DBD). We chose the DBD for its ability to produce an atmospheric plasma at relatively low power. Our implementation uses an alternating current (ac) electric field, orthogonal to the dc thrust-producing field, to generate the DBD (Fig. 6-8).

Similar decoupling techniques to separate the processes of ion generation and "drift" have been demonstrated in other applications, for example by Rutherford [126] who produced ions using X-rays, and more recently by Khomich and Yamshchikov [127] who produced ions using a water-cooled Dumanchin electrode (approximately an azimuthal DBD) for boundary layer flow control.

We apply this concept to thrust generation and optimize it for this application: we use a lightweight and low-drag wire-to-wire electrode design which is suitable for airplane propulsion, and we perform a parametric exploration of DBD voltage and frequency to identify the operational regimes and reduce the DBD power requirement.

6.2.3 Performance of the decoupled thruster

Figure 6-8 shows a schematic of the corona discharge thruster and the proposed decoupled thruster. In both thrusters, the emitter electrode was a tungsten wire with a diameter of 0.254 mm, the collector electrode is an aluminum tube with a diameter of 12.7 mm, 25.4 mm or 38.1 mm, the gap spacing d between the emitter and collector was varied between 50 mm and 150 mm (measured from the top of the collector to the bottom of the emitter), and the span of the electrodes (into the page)

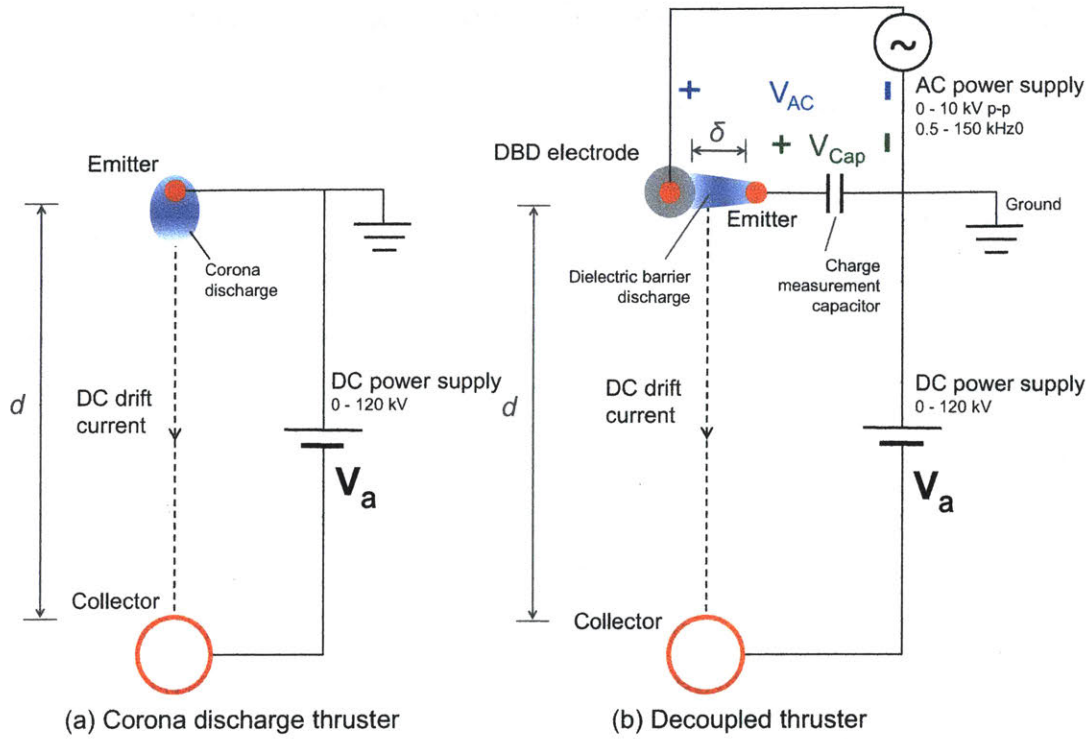


Figure 6-8: Cross sectional schematic and electrical circuit diagram of a corona discharge EAD thruster and a DBD decoupled thruster.

was 500 mm. In the decoupled thruster, a DBD electrode was spaced $\delta = 1$ mm from the emitter, forming a DBD field orthogonal to the dc field between the emitter and the collector. We use a fluorinated ethylene propylene (FEP) insulated high voltage wire as the DBD electrode, which has a conductor diameter of 0.4 mm and an overall diameter of 1.02 mm. The FEP insulation acts as the dielectric barrier. This DBD electrode system is significantly lighter than the plate electrodes or surface electrodes found in other applications. A charge measurement capacitor was placed in series with the DBD to measure DBD power draw. The decoupled thruster has two voltage sources: the applied dc voltage between the emitter and collector, and the DBD ac voltage across the emitter and the DBD electrode. Details of the electrical system and measurement setup are in Appendix H.2.2.

The thrust was measured for the decoupled thruster at different applied dc voltages over a range of DBD voltages and frequencies to explore the effect of the changing DBD parameters. All experiments are performed with a dc gap spacing d = 100 mm

and collector diameter 12.7 mm. Details of the thrust measurement apparatus are in Appendix H.2.1.

When the DBD is turned off, the decoupled thruster performs like a corona discharge thruster. Without an independent ion source, the device reverts to ion production via a corona discharge. Note the inception voltage of the "DBD off" cases in Fig. 6-9, consistent with that of a corona discharge.

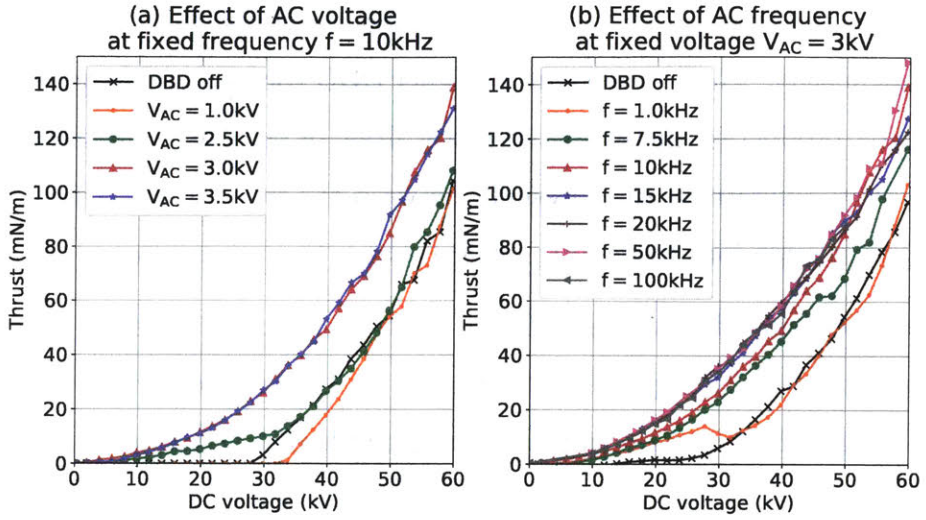


Figure 6-9: Thrust per unit span of the thruster produced by the decoupled thruster vs. dc voltage at different DBD voltages (AC amplitude) and frequencies. a) The frequency of the DBD is fixed at 10.0 kHz. Once the DBD voltage is above the inception voltage (in this case 2.5 kV), there is a significant increase in the thrust compared with that of the baseline corona discharge. b). The voltage of the DBD is fixed at 3.0 kV. When the DBD frequency is above certain threshold, there is a significant increase in the thrust compared with that of the baseline corona discharge.

When the voltage of the DBD ion source is increased and plasma inception of the DBD occurs (between 2.5 kV and 3.0 kV), the thrust at the same applied dc voltage is increased (Fig. 6-9a). Similarly the thrust is increased for higher DBD frequencies (Fig. 6-9b). At an applied dc voltage of 60 kV, the thrust is increased by 40% over the corona discharge. The percentage increase is higher at lower dc voltages.

This increase in thrust is dependent on the parameters of the DBD: there exist both a threshold AC voltage and a threshold AC frequency for the DBD operation, below which there is no increase in thrust. At low AC voltage, the DBD is below plasma inception voltage and produces no ions, and at low AC frequency, the DBD

does not produce enough ions. We find that for our paricular geometry, the threshold AC voltage is around 3.0 kV and the threshold AC frequency is approximately 10 kHz[6]. When the DBD voltage and frequency increase beyond these thresholds, the thrust does not further increase. The thrust generation becomes limited by space charge density instead of ion production.

Therefore we identify two regimes of operation: one where the thrust generation is limited by the rate of ion production, and one where the thrust generation is limited by space charge density. The latter occurs at higher DBD voltages and frequencies. Since increasing ion production increases the power draw of the DBD (see Section 6.2.4), it is desirable to operate on the threshold between the two regimes, where the DBD produces *just* enough ions to be in the space charge limited regime.

At our threshold DBD voltage of 3 kV and frequency of 10 kHz, we quantified the thrust and thrust-to-dc-power performance as a function of dc gap spacing (Fig. 6-10). The decoupled thruster, in green, produced higher thrust at fixed applied dc voltage, and at a fixed thrust-to-power. The approximate one-dimensional current density limit was calculated using an effective area of 0.08 m^2. The collector diameter was 38.1 mm for the 150 mm gap spacing and 25.4 mm for the others – this was sized to prevent reverse corona emission from the collector. The UV radiation emitted by the DBD resulted in UV photoemission of electrons from the aluminum collector; for these experiments, the collector was coated in a thin layer of organic UV absorbants to prevent electron emission without affecting the electrical conductivity.

The effect of increased thrust over the corona discharge at the same voltage holds across gap spacings from 50–150 mm. To generate the same thrust, a lower applied dc voltage is needed, which reduces the average accelerating electric field and improves the thrust-to-power. Fig. 6-10b, which relates the thrust and thrust-to-power, shows that the decoupled thruster is able to achieve higher thrust-to-power ratio at every thrust level compared to the corona discharge thruster.

[6]The threshold we have found here is dependent on our particular geometry and may be different for other geometries.

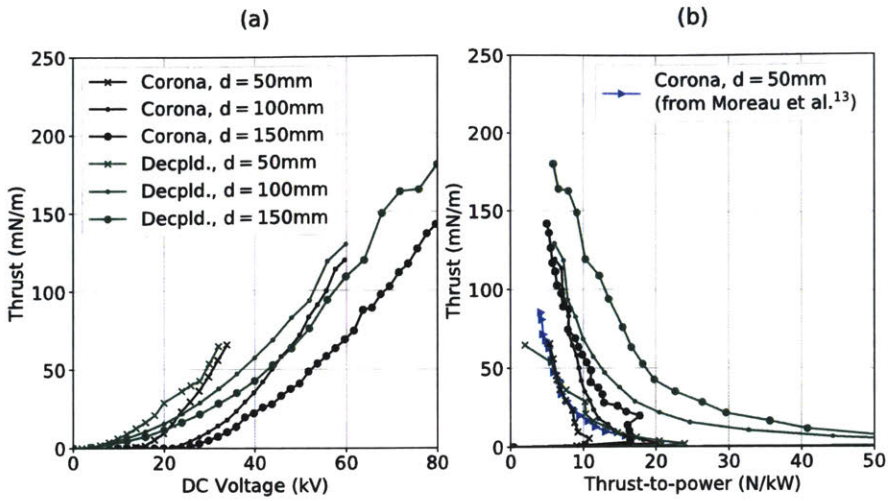


Figure 6-10: Decoupled thruster (V_{AC} =3 kV, f =10 kHz) thrust and thrust-to-power characteristics compared to corona discharge thruster.

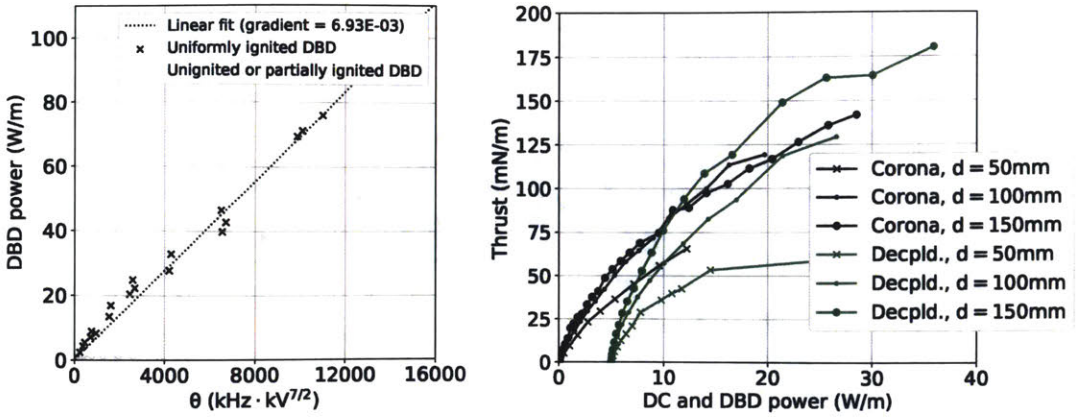
6.2.4 Power Draw Penalty of the DBD

The thrust and thrust-to-power results in Fig. 6-10 do not include the power required to drive the DBD, which incurs a power draw penalty.

The power draw of a DBD is a function of the applied AC waveform – voltage, frequency, waveform shape – and of the electrode geometry. We fixed the DBD geometry and the waveform shape. Fig. 6-11a shows the measured DBD power against θ, where $\theta = fV_{AC}^{7/2}$ (an empirical power equation from curve fitting [12]). f is the frequency and V_{AC} is the amplitude of the voltage. For the range of DBD voltages from 0 kV to 3.5 kV and frequencies from 1 kHz to 100 kHz, we found that the DBD power per unit span of the thruster, P, for our geometry scaled as

$$P \propto fV_{AC}^{7/2}. \tag{6.5}$$

This is consistent with the results found by Kriegseis et al. and others for surface DBDs [128–130]. At a DBD voltage of 3 kV and frequency of 10 kHz, the power draw of the DBD per unit span of the thruster was 5.4 W/m. This is the penalty in power draw that our particular decoupled thruster architecture incurs versus the corona discharge thruster.



(a) (b)

Figure 6-11: (a) DBD power increases linearly with $\theta = fV_{\mathrm{AC}}^{7/2}$. This holds over the broad range of tested frequencies, and for voltages over 2.5 kV, which was the approximate DBD inception voltage of our particular DBD geometry. (b) Thrust vs. total power (the sum of the dc power and the DBD power) of the decoupled thruster compared to the corona thruster at different dc gap spacings.

Including this power draw penalty, we find that the decoupled thruster is no longer advantageous at lower thrust levels (Fig. 6-11b). When the dc power draw is low, the increased thruster thrust-to-power is not sufficient to warrant the increased power required to drive the DBD. At higher thrust levels however, which is where EAD devices operate, the decoupled thruster simultaneously shows an improvement in both thrust-to-power and maximum achievable thrust per unit span of the thruster. 160 mN/m can be achieved at 5.4 N/kW, compared to 140 mN/m at 5 N/kW for the corona discharge.

In this study of the decoupled thruster, we have optimized DBD voltage and frequency. Optimization of other variables such as the spacing δ between the DBD electrode and the emitter, thickness of the dielectric layer, and dielectric material could further reduce the required DBD power draw [26] while still maintaining the same production of ions. With further optimization and reduction in power of the DBD ionization stage, we expect that decoupled thrusters have the potential to increase the flight performance of EAD aircraft.

Chapter 7

Conclusion

This thesis has presented a variety of contributions to lightweight high voltage (HV) power conversion and to the demonstration of using electroaerodynamic (EAD) for aircraft propulsion. While all HV dc-dc and dc-ac converters are developed in the context of the EAD propulsion application, their impacts extend beyond that context.

The thesis presents work on reducing the weight of HV converters by increasing the switching frequencies, topology optimizations, and innovative circuit techniques. Challenges of weight reduction eventually come down to component level – available HV diodes/MOSFETs, capacitors, wires, printed circuit boards, etc.

To address this, on the component level, the thesis presents weight data bases of available capacitors (blocking 1–15 kV), high voltage diodes (rated at 1–15 kV and 0.03–5 A), MOSFETs (rated at 0.25–4.5 kV and 0.2–8.5 A), high voltage wires (rated at 1–40 kV), magnetic cores and magentic materials (from 2 kHz to 10 MHz). These data bases can be useful for weight studies of other converters using these components.

Using the data bases, the thesis presents systematic weight study methods and results of building blocks for generic HV dc-dc and dc-ac converters, including: inductors operating in different conditions, high voltage transformers, full-bridge inverters, resonant-transition boost converter. The weight study method can be adopted for converters in other topologies and applications.

Lastly, the thesis documents practical techniques on building high voltage prototypes, which may be useful for other researchers.

We also identify several exciting opportunities in the future research of high voltage power conversion that is not limited to the EAD application:

- High-frequency high-voltage power converters: in recent decades, broader applications of high voltage converters, such as transmission system, dc microgrids, and others, have been driving the required volumetric power density of the employed converters higher and higher [131]. Miniaturizing these converters through high-frequency operation seems to be an unavoidable trend. Achieving reliable and high-performing high frequency designs will need to be facilitated by 1) advances in high voltage wide-band-gap switching devices (GaN, SiC, and others); 2) understanding of insulation materials, their performance, limitations and life time under high frequency operation; 3) innovative circuit architectures and/or isolation techniques. In recent years, there have been some research efforts in these areas, but many are still uncharted territories.

- Piezoelectric transformer based high voltage converters: as mentioned in Chapter 2, piezoelectric transformer are not competitive for high voltage medium-to-high power designs. However, for high voltage low power applications, the power density and specific power of a piezoelectric transformer may exceed that of a traditional transformer, making it a promising candidate. Moreover, piezoelectric transformers have been mostly developed for sensing, actuation and energy harvesting but seldom used power applications [132], making it an exciting research object. Promising research directions include: 1) characterize piezoelectric transformers for high voltage power delivering application; 2) innovative circuit techniques to use these components effectively.

Part IV

Appendix

Appendix A

Weight study of commercial products and academic designs

Company	Series	Output		Input	Weight	Specific power	Switching Frequency
		(kV)	(W)	(V)	(kg)	(kW/kg)	(kHz)
Matsusada	AU	60	1200	100/200 VAC	18	0.07	-
	WA	50	1200	100/200 VAC	9.7	0.12	-
	W	40	350	100 VAC	5	0.09	-
	W	20	350	100 VAC	4	0.07	-
TDK	ALE120A	20	1000	100/200 VAC	5.5	0.18	-
UltraVolt	C series	6	250	30 VDC	1.18	0.21	-
Glassman	EK	60	600	100 VAC	8.16	0.07	-
	EQ	60	1200	100/200 VAC	9.97	0.12	-
HiTek Power	OL1k	60	1000	200 VAC	14	0.07	-
Spellman	SLM	70	600	200 VAC	6.35	0.09	-
		70	1200	200 VAC	11.8	0.1	-
	SL150kV	150	1200	200 VAC	40.4	0.03	-
EMCO	4000 series	33	10	24 VDC	0.675	0.015	-
Keithley	Model 2290-10	10	100	100/200 VAC	3.7	0.027	-
iseg Spezialelektronik	HPS 2ND GENERATION	60	3000	230 VAC	20	6.67	-
		60	1500	230 VAC	20	0.075	-
D. Fu (2008, 88%) [54]		10	3700	600 VDC	1.3*	2.78*	700
S. Mao (2011) [41]		35	2000	-	1.1*	1.75*	400
N. Shafiei (2013, 84%) [55]		10	1100	100 VAC	0.99*	1.11*	127
W.C. Hsu (2017, 79%) [58]		40	300	400 VDC	0.5*	0.6*	80
S. Mao (2018, 80%) [57]		20	500	250 VDC	-	-	400
S. Park (2018, 73%) [56]		35	200	60 VDC	0.188	1.08	1250
S. Park (2019, 77%) [40]		54	100	45 VDC	-	0.64	3000 - 7000

Table A.1: Weight and specific power of commercial high voltage dc-dc power supplies and academic designs at low to medium power level, corresponding to Fig. 1-4. The reported efficiencies of academic designs are listed next to the citations.
* These are estimated from the paper

Company	Series	Output		Maximum Frequency	Weight	Specific power
		(kV)	(W)	(kHz)	(kg)	(kW/kg)
GBS Elektronik	minipuls 0.1	6	30	20	0.34	0.088
Matsusada	DOC	1	100	5	12	0.008
DEI	PVX4150	1.5	150	240	8.2	0.018
	PVX4140	3.5	100	30	8.2	0.012
	PVX4130	6	100	10	7.2	0.014
BEHLKE	GHTS 30	3	150	20	2	0.075
	GHTS 60	6	300	20	2	0.15
Eagle Harbor Tech	NSP-30-5	5	30	10	9.8	0.003
	NSP-120-5-F-500	5	120	10	9.8	0.012
Trek	609E6 model	4	80	13	13.2	0.006
	PDO6087	5	100	15	14.9	0.0067
	PDO5034	7.5	375	15	24.9	0.015
	5/80 model	5	400	60	24	0.017
Jordan Tof Products	D1040	3.5	35	200	4.3	0.008
Kinnares (2010, 87%) [63]		3.44	40	55	0.76*	0.053*
Bonnin (2014) [14]		3.7	40	1000	0.15*	0.26*
Raymond (2015, 84%) [70]		2	100	27120	0.045*	2.2*
Saleh (2018, 75%) [13]		1.5	750	20	1.09	0.69

Table A.2: Weight and specific power of selected commercial high voltage dc-ac power supplies and academic designs at hundreds of W, corresponding to Fig. 1-6. The reported efficiencies of academic designs are listed next to the citations.
* These are estimated from the paper.

Appendix B

Weight study of high voltage transformers

This appendix contains the essence of the weight study of high voltage transformers. The transformer weight studies in Chapter 2, Chapter 4 and Chapter 5 are all based on this chapter but with their own variations. The common thoughts and models they share are explained in this chapter, and the variations for each case are explained in their own appendices. The high voltage transformers considered in this chapter is ungapped, assuming to have a large enough magnetizing inductance. Whereas in Chapter 2, the parasitic capacitances of the transformer is modeled and used as part of the circuit operation, and in Chapter 4, the parasitic inductance is modeled and used as part of the circuit operation.

Figure B-1 shows a high-level flow chart of the weight study. Each operating point is defined by four parameters: transformer input voltage amplitude $\mathbf{V_{pri}}$, output voltage amplitude $\mathbf{V_o}$, frequency $\mathbf{f}$ and output power $\mathbf{P_o}$. At each operating point, we sweep core and winding designs, then we down-select these designs with a set of loss and physical constrains. Eventually we estimate the weight and find a few lightest designs for this specific operating point. Repeating this process for each operating point, we get a map of how the lightest design changes with each operating parameter.

Section B.1 presents the models of the core, covering shape, size and core loss estimation. Section B.2 presents the models of the winding, covering wire size, winding pattern and copper loss estimation. Section B.3 explains the loss and physical con-

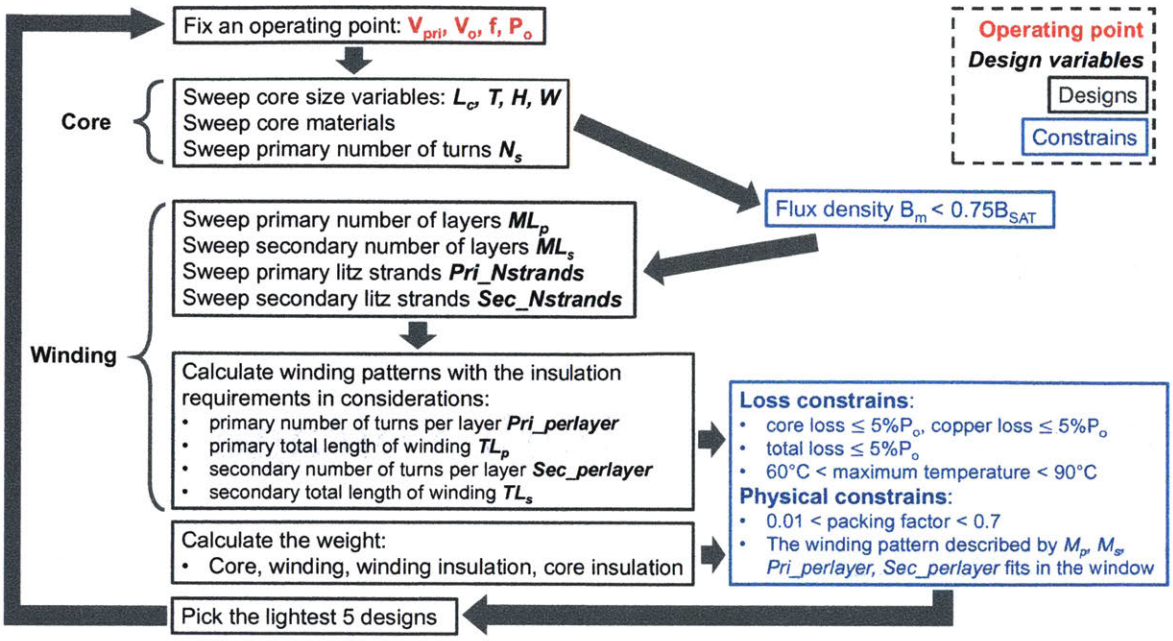


Figure B-1: Weight study flow chart for the high voltage transformers.

strains used to rule out "unqualified" designs. Section B.4 presents how the weight is calculated.

B.1 Core

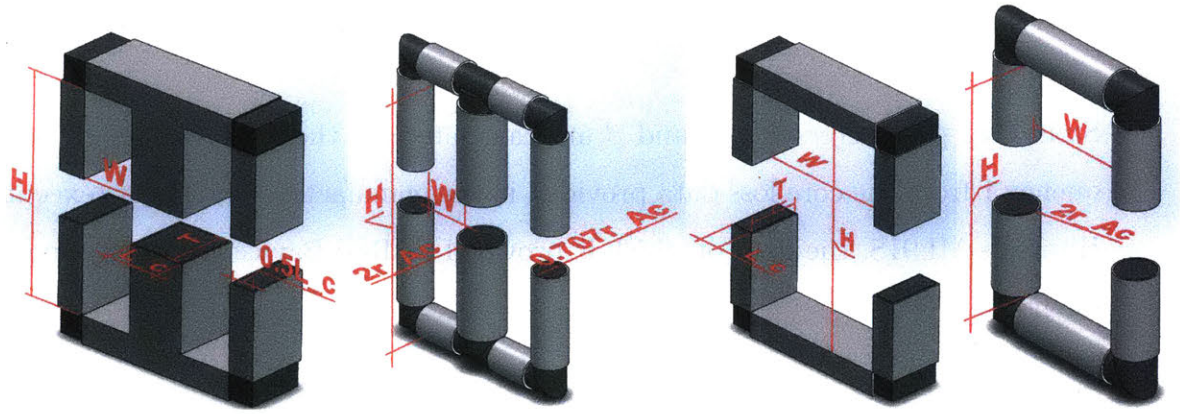
B.1.1 Core dimensions

We consider EE, ER cores across this thesis. But in this appendix, we also list equations for U and UR cores. All are shown in Fig. B-2. The variables defining each core and its size are also marked in Fig. B-2:

- Window height $\boldsymbol{H}$ and width $\boldsymbol{W}$
- EE/U core thickness $\boldsymbol{T}$ and center-leg width $\boldsymbol{L_c}$
- ER/UR core center-leg radius $\boldsymbol{r_{Ac}}$

From the above variables, we can calculate other dimensional parameters for future use (to calculate core loss, weight, etc):

- Core cross-sectional area $\boldsymbol{A_c}$: in EE core, $A_c = L_c T$, in ER core, $A_c = \pi r_{Ac}^2$



(a) EE core (b) ER core (c) U core (d) UR core

Figure B-2: Dimension annotations for EE/ER/U/UR core. EE and U cores are easy to customize and machine; ER and UR cores are favorable for high voltage designs because they have fewer sharp corners. For E cores (EE or ER), we assume the center-leg cross sectional area is split in half to each side-leg.

- Core effective length $\boldsymbol{L_e}$: in EE core, $L_e = 2(H + L_c) + 2(W + L_c)$, in ER core, $L_e = 2(H + 2r_{Ac}) + 2(W + 2r_{Ac})$
- Core window area $\boldsymbol{W_a} = HW$
- Core volume $\boldsymbol{V_{core}} = A_c L_e$

In Chapter 2, off-the-shelf pre-made core sizes are considered, as listed in Table. B.1. In Chapter 5 and Chapter 4, customizable dimensions are considered.

B.1.2 Core material and losses

Different core materials are considered in different chapters. In common, we estimate the core loss as follow:

- Use standard Steinmetz equations to estimate the core loss $\boldsymbol{P_{core}}$

$$P_{core} = CoreLossMultiple \times V_{core} \times K_1 \times f^{\alpha} \times B_m^{\beta} \tag{B.1}$$

- Calculate the maximum B field assuming the voltages in and out are both sinusoidal,

$$B_m = \frac{\lambda}{2N_p A_c}, \lambda = \frac{V_{pri}}{\pi f} \tag{B.2}$$

- Increase the core loss estimation by 1.5 times by setting ***CoreLossMultiple*** to 1.5[1].
- Steinmetz parameters K_1, α and β are calculated for the operating point frequency f from the core loss data provided in the manufacture datasheet (except Hitachi's ML91S, the data of which is provided by Rod Bayliss from his experiments) [2].

[1]This is because from the author's empirical experiences, the core loss estimation using Steinmetz equations is $40 - 60\%$ of the actual core loss.

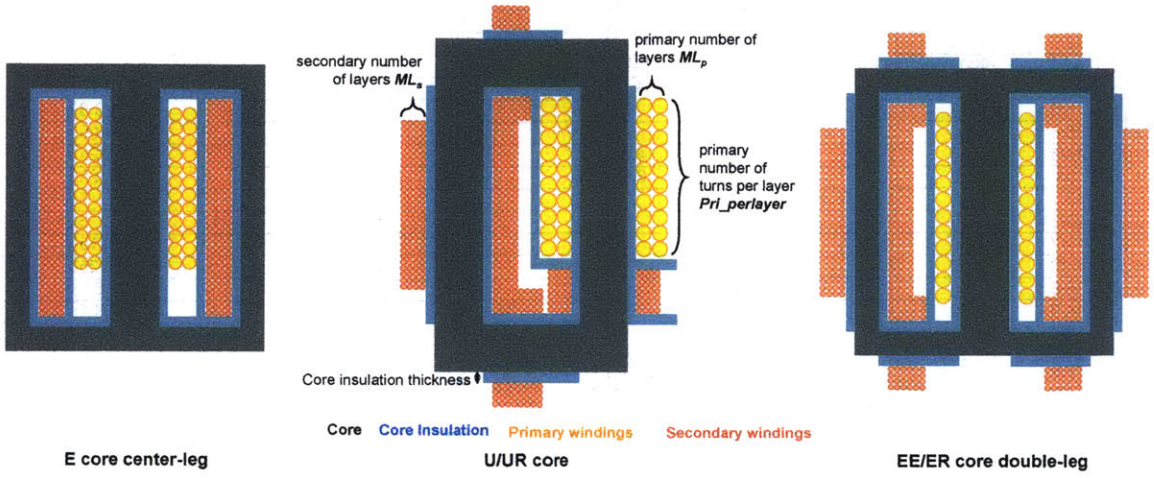
[2]Most loss data in the datasheets is measured at discrete frequencies, therefore the author uses the Steinmetz parameters from adjacent loss curves (in the range of **0.6f** to **1.4f**) for f.

No.	Properties	Ve (mm3)	Ae (mm2)	Le (mm)	Center leg width (mm)	Center leg thickness (mm)	Side leg width (mm)	Side leg thickness (mm)	Window Width (mm)	Window Height (mm)
1	E5.3/2.7/2	33.3	2.66	12.52	1.4	2	0.75	2	1.2	3.8
2	E6.3/2.9/2	40.6	3.30	12.30	1.4	2	1.35	2	1.1	3.7
3	E8.8/4.1/2	78.0	5.00	15.60	1.9	2	1.8	2	1.65	4
4	E13/6/3	281	10.1	27.82	3.2	3	1.75	3	3.15	8.2
5	E13/6/6	559	20.2	27.67	3.2	6	1.75	6	3.15	8.2
6	E13/7/4	369	12.4	29.76	3.7	4	2.05	4	2.6	9
7	E16/8/5	750	20.1	37.31	4.7	5	2.35	5	3.3	11.4
8	E16/12/5	1070	19.4	55.15	4	5	2	5	4	20.5
9	E19/8/5	900	22.6	39.82	4.7	5	2.35	5	4.8	11.4
10	E19/8/9	1650	41.3	39.95	4.75	9	2.335	9	4.79	11.38
11	E20/10/5	1340	31.2	42.95	5.2	5	3.6	5	3.8	12.6
12	E20/10/6	1490	32.0	46.56	5.9	6	3	6	4.05	14
13	E20/14/5	1513	24.4	62.01	4.55	5	3	5	4.725	22.3
14	E25/10/6	1930	37.0	52.16	6.35	6	3.1	6	6.225	12.8
15	E25/13/7	2990	52.0	57.50	7.5	7	3.75	7	5	17.4
16	E25/13/11	4500	78.4	57.40	7.5	11	3.75	11	5	17.4
17	E30/15/7	4000	60.0	66.67	7.2	7	5.25	7	6.15	19.4
18	E31/13/9	5150	83.2	61.90	9.4	9	4.55	9	6.25	17.2
19	E32/16/9	6180	83.0	74.46	9.5	9	4.65	9	6.6	22.4
20	E34/14/9	5590	80.7	69.27	9.3	9	4.25	9	8.1	19.6
21	E35/18/10	8070	100	80.70	10	10	5.25	10	7.25	25
22	E36/21/12	12160	126	96.51	10.2	12	5.75	12	7.15	31.5
23	E41/17/12	11500	149	77.18	12.45	12	6.2	12	8.075	20.8
24	E42/21/15	17300	178	97.19	12.2	15	6.25	15	8.65	29.6
25	E42/21/20	22700	233	97.42	12.2	20	6.25	20	8.65	29.6
26	E42/33/20	34200	236	144.92	12.2	20	6.25	20	8.65	52
27	E47/20/16	20800	234	88.89	15.6	16	7.3	16	8.4	24.2
28	E55/28/21	44000	353	124.65	17.2	21	8.75	21	10.15	37
29	E55/28/25	52000	420	123.81	17.2	25	8.75	25	10.15	37
30	E56/24/19	36000	337	106.82	18.8	19	9	19	9.6	29.2
31	E65/32/27	79000	540	146.30	20	27	10.4	27	12.1	44.4
32	E71/33/32	102000	683	149.34	22	32	11.5	32	13	43.8
33	E80/38/20	72300	392	184.44	19.8	20	10.45	20	19.65	56.4
34	E100/60/28	202000	738	273.71	27.5	28	13.425	28	22.825	93.7
35	EC35	6530	84.3	77.46	9.5	9.5	6.125	9.5	6.625	24.6
36	EC41	10800	121	89.26	11.6	11.6	6.97	11.6	7.73	27.8
37	EC52	18800	180	104.44	13.4	13.4	9.5	13.4	9.8	31.8
38	EC70	40100	279	143.73	16.4	16.4	12.75	16.4	14.05	45.5
39	EFD10/5/3	171	7.2	23.75	4.55	3	1.175	3	1.55	7.5
40	EFD12/6/3.5	325	11.4	28.51	5.4	3.5	1.5	3.5	1.8	9.1
41	EFD15/8/5	510	15.0	34.00	5.3	5	2	5	2.85	11
42	EFD20/10/7	1460	31.0	47.10	8.9	7	2.3	7	3.25	15.4
43	EFD25/13/9	3300	58.0	56.90	11.4	9	3.15	9	3.65	18.6
44	EFD30/15/9	4700	69.0	68.12	14.6	9	3.8	9	3.9	22.4
45	ER28/14/11	5260	81.4	64.62	9.9	11	3.125	11	5.925	19.5
46	ER28/17/11	6140	81.4	75.43	9.9	11	3.125	11	5.925	25.3
47	ER35/21/11	9710	107	90.75	11.3	11	4.425	11	7.425	29.5
48	ER40/22/13	14600	149	97.99	13.3	13	5.2	13	8.15	30.9
49	ER42/22/16	19200	194	98.97	15.5	16	6	16	7.25	30.9
50	ER42/22/15	16800	170	98.82	15	15	5.8	15	7.7	31.2
51	ER48/21/21	25500	255	100.00	18	21	5	21	10	29.4
52	ER48/18/18	20300	231	87.88	17.6	18	5.6	18	9.6	22.9
53	ER54/18/18	23000	250	92.00	17.9	18	6.675	18	11.375	22.2
54	ETD29/16/10	5470	76.0	71.97	9.8	10	3.5	10	6.1	22
55	ETD34/17/11	7640	97.1	78.68	11.1	11	4.2	11	7.25	23.6
56	ETD39/20/13	11500	125	92.00	12.8	13	4.85	13	8.25	28.4
57	ETD44/22/15	17800	173	102.89	15.2	15	5.75	15	8.65	32.2
58	ETD49/25/16	24000	211	113.74	16.7	16	6.45	16	9.7	35.4
59	ETD54/28/19	35500	280	126.79	18.9	19	6.4	19	11.15	40.4
60	ETD59/31/22	51500	368	139.95	21.65	22	7.15	22	11.525	45

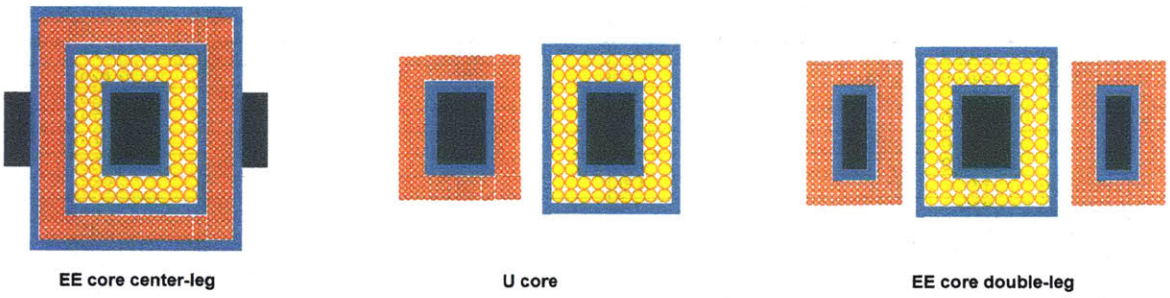
Table B.1: A list of off-the-shelf core size considered in the transformer weight study in some Chapters.

B.2 Winding

B.2.1 Wires and winding patterns



(a) Front view



(b) Top view (only showing EE and U core here, ER and UR core are similar)

Figure B-3: Front and top view of the winding patterns in considerations. For E core center-leg, the secondary can only be wound in the $\boldsymbol{H}$ direction around the primary. For U core or E core double-leg, the secondary can be wound on both the $\boldsymbol{H}$ and the $\boldsymbol{W}$ direction of the core. For E core double-leg case, we limit the secondary on 3 sections of the side legs, not on the center leg. See Fig. B-4 for more details. (The illustration here does not show sectioning the secondary winding to reduce capacitance, which is considered in Chapter D)

There are three winding patterns we consider in this thesis, as shown in Fig. B-3: E core center-leg winding, E core double-leg winding, and U core. There are 12 parameters defining each winding pattern, five of which are swept as variables, and the rest can be calculated from the already defined variables:

- Sweeping variables (5):

- Primary the number of turns $\boldsymbol{N_p}$
- Primary number of layers $\boldsymbol{Ml_p}$
- Secondary number of layers $\boldsymbol{Ml_s}$
- Primary wire, the number of strands of litz in the wire, ***Pri_Nstrands***, swept from *MinPriNstrands* to *MaxPriNstrands* with one strand incrementally:

$$MinPriNstrands = floor(\frac{\frac{2P_o}{\eta V_{pri} J_{wmax}}}{\pi \frac{ds^2}{4}}) + 1; \tag{B.3}$$

$$MaxPriNstrands = floor(\frac{\frac{1.2\times 2P_o}{\eta V_{pri} J_{wmax}}}{\pi \frac{ds^2}{4}}) + 1; \tag{B.4}$$

- Secondary wire, the number of strands of litz in the wire, ***Sec_Nstrands***, swept from *MinSecNstrands* to *MaxSecNstrands* with one strand incrementally:

$$MinSecNstrands = floor(\frac{\frac{2P_o}{V_o J_{wmax}}}{\pi \frac{ds^2}{4}}) + 1; \tag{B.5}$$

$$MaxSecNstrands = floor(\frac{\frac{1.2\times 2P_o}{V_o J_{wmax}}}{\pi \frac{ds^2}{4}}) + 1; \tag{B.6}$$

- In the above equations, η is the targeted transformer efficiency (set to 95%, corresponding to the loss constrains in Section B.3), J_{wmax} is the maximum current density in the wire (set to 500 A/cm^3), ds is the diameter of a single strand litz, where ds = max(skin depth at f, minimal available litz diameter).

- Calculated parameters (7):

  - Primary numbers of turns per layer $\boldsymbol{Pri\_perlayer} = floor(\frac{N_p}{Ml_p}) + 1$
  - Secondary the number of turns $\boldsymbol{N_s} = N_p \frac{V_o}{V_{pri}}$
  - Secondary numbers of turns per layer ***Sec_perlayer***:
    - For EE/ER center-leg or U/UR, $Sec_{perlayer} = floor(\frac{N_s}{Ml_s}) + 1$
    - For EE/ER double-leg, we only consider one of the window due to symmetric: $Sec_{perlayer} = floor(\frac{N_s}{2Ml_s}) + 1$

– Primary wire diameter $\boldsymbol{Pri_{WireSize}}$ and overall diameter $\boldsymbol{Pri_{FullWireSize}}$: primary wire consists of $Pri_{Nstrands}$ strands of litz wire as a bundle and a jacket that can sustain V_{pri}. $\boldsymbol{Pri_{WireSize}}$ is calculated such that it yields the same area as the sum of all litz, with a discount factor representing the inefficiency of twisting litz wires into a bundle[3]; and adding the jacket thickness[4] gives the $\boldsymbol{Pri_{FullWireSize}}$.

$$Pri_{WireSize} = 2\sqrt{\frac{Pri_{Nstrands}\frac{ds^2}{4}}{LitzFactor}}$$

$$Pri_{FullWireSize} = Pri_{WireSize} + 2\frac{V_{pri}}{DielectricStrength}$$

– Secondary wire diameter $\boldsymbol{Sec_{WireSize}}$ and overall diameter $\boldsymbol{Sec_{FullWireSize}}$

$$Sec_{WireSize} = 2\sqrt{\frac{Sec_{Nstrands}\frac{ds^2}{4}}{LitzFactor}}$$

$$Sec_{FullWireSize} = Sec_{WireSize} + 2\frac{V_o}{DielectricStrength}$$

From the above 12 parameters, we can calculate two more parameters for future use (to calculate copper loss, weight, etc): primary winding total length $\boldsymbol{TL_p}$ and secondary winding total length $\boldsymbol{TL_s}$ considering core insulation, see Table B.2 (recommend referring Fig. B-3b to derive/understand the equations)[5].

[3] *LitzFactor* is set to 0.8 as an empirical estimation

[4] We assume all insulation materials used (around wire or core) are TEFLON with a density of 2.2 g/cm^3. For the wire and the core insulation, we assume the *DielectricStrength* is 200 kV/cm and 100 kV/cm [133] respectively. The reason is that the wire is manufactured professionally in a dust-free environment (the wire catalog in Table confirms that 200 kV/cm is the average dielectric strength of the off-the-shelf wires), whereas the core insulation is manufactured by ourselves therefore requires a bigger margin.

[5] In all equations, $T_{CoreInsu}$ is the core insulation thickness, calculated as $T_{CoreInsu} = \frac{V_o}{DielectricStrength}$. We assume all insulation materials used is TEFLON with a *DielectricStrength* of 100 kV/cm [133]

Core shape	Winding pattern	Total length of windings
EE core	center-leg	$TL_p = 2N_p(L_c + T + 4T_{CoreInsu} + 2Ml_pPri_{FullWireSize})$
		$TL_s = 2N_s(L_c + T + 4Ml_pPri_{FullWireSize} + 8T_{CoreInsu} + 2Ml_sSec_{FullWireSize})$
	double-leg	$TL_p = 2N(L_c + T + 4T_{CoreInsu} + 2Ml_pPri_{FullWireSize})$
		$TL_s = 2N_s(0.5L_c + T + 4T_{CoreInsu} + 2Ml_sSec_{FullWireSize})$
ER core	center-leg	$TL_p = 2\pi N_p(r_{Ac} + T_{CoreInsu} + 0.5Ml_pPri_{FullWireSize})$
		$TL_s = 2\pi N_s(r_{Ac} + 2T_{CoreInsu} + Ml_pPri_{FullWireSize} + 0.5Ml_sSec_{FullWireSize})$
	double-leg	$TL_p = 2\pi N_p(r_{Ac} + T_{CoreInsu} + 0.5Ml_pPri_{FullWireSize})$
		$TL_s = 2\pi N_s(\sqrt{2}r_{Ac} + T_{CoreInsu} + 0.5Ml_sSec_{FullWireSize})$
U core	-	$TL_p = 2N_p(L_c + T + 4T_{CoreInsu} + 2Ml_pPri_{FullWireSize})$
		$TL_s = 2N_s(L_c + T + 4T_{CoreInsu} + 2Ml_sSec_{FullWireSize})$
UR core	-	$TL_p = 2\pi N_p(r_{Ac} + T_{CoreInsu} + 0.5Ml_pPri_{FullWireSize})$
		$TL_s = 2\pi N_s(r_{Ac} + T_{CoreInsu} + 0.5Ml_sSec_{FullWireSize})$

Table B.2: Equations to calculate primary and secondary winding ($\boldsymbol{TL_p}$ and $\boldsymbol{TL_s}$) total length for different core shape and winding patterns

B.2.2 Copper loss

Copper loss is estimated using Dowell's equations for litz wires, same as in [111]. The ratio of ac resistance versus dc resistance for each winding is:

$$Fr_{Pri} = X_{Pri}\left(\frac{sinh(2X_{Pri}) + sin(2X_{Pri})}{cosh(2X_{Pri}) - cos(2X_{Pri})} + \frac{2(Ml_p^2Pri_{Nstrands} - 1)}{3}\frac{sinh(X_{Pri}) - sin(X_{Pri})}{cosh(X_{Pri}) + cos(X_{Pri})}\right)$$

$$Fr_{Sec} = X_{Sec}\left(\frac{sinh(2X_{Sec}) + sin(2X_{Sec})}{cosh(2X_{Sec}) - cos(2X_{Sec})} + \frac{2(Ml_s^2Sec_{Nstrands} - 1)}{3}\frac{sinh(X_{Sec}) - sin(X_{Sec})}{cosh(X_{Sec}) + cos(X_{Sec})}\right)$$

Where

$$X_{Pri} = \frac{ds}{2skindepth\sqrt{\pi K_{Pri}}}, K_{Pri} = \frac{\sqrt{\pi Pri_{Nstrands}}ds}{2Pri_{WireSize}}$$

$$X_{Sec} = \frac{ds}{2skindepth\sqrt{\pi K_{Sec}}}, K_{Sec} = \frac{\sqrt{\pi Sec_{Nstrands}}ds}{2Sec_{WireSize}}$$

Therefore the loss in each winding and the total copper loss are:

$$Rac_{Pri} = Rdc_{Pri}Fr_{Pri} = Fr_{Pri}\frac{\rho TL_p}{\frac{\pi Pri_{WireSize}^2}{4}}$$

$$Rac_{Sec} = Rdc_{Sec}Fr_{Sec} = Fr_{Sec}\frac{\rho TL_s}{\frac{\pi Sec_{WireSize}^2}{4}}$$

$$Pcopper = I_{p_{rms}}^2 Rac_{Pri} + I_{s_{rms}}^2 Rac_{Sec}$$

B.3 Constrains

B.3.1 Loss and thermal constrains

Losses: core loss P_{core}, copper loss P_{copper} and total loss $P_{core} + P_{copper}$ all less than 5% of P_o, corresponding to the targeted efficiency $\eta > 95\%$ mentioned in Section B.2.

Current density: as mentioned in Section B.2, we impose a current density limit of 500 A/cm^3 on both primary and secondary wires.

Flux density: the maximum flux density B_m needs to be smaller than 75% of the saturation flux density of the core material B_{SAT}.

Steady state temperature is calculated in the same way as in [111], using the parameters for the pot core. This would be an overestimation for E and U core, but provides a safe margin.

$$R_{th} = 0.01631(A_c W_a)^{-0.405}$$
$$T_{absolute} = R_{th}(P_{copper} + P_{core}) + 25$$
$$60°C \leqslant T_{absolute} \leqslant 90°C$$

B.3.2 Physical constrains

Overall packing factor: defined as the percentage the area taken by the wires (both copper and wire jackets) in the window area

$$Overallpackingfactor = \frac{\pi(N_p Pri^2_{FullWireSize} + N_s Sec^2_{FullWireSize})}{4W_a}$$
$$0.01 \leqslant Overallpackingfactor \leqslant 0.7$$

Primary and secondary windings fit the window in both $\boldsymbol{H}$ and $\boldsymbol{W}$ directions considering insulation. The constrains vary for different winding patterns and core shapes, see Table B.3 for each case. See Fig. B-4 to help understanding the derivation for E core double-leg winding and U core winding.

Core shape	Winding pattern	Direction	Winding	Constrains
EE/ER core	center-leg	***H***	Pri	$Pri_{perlayer} \times Pri_{FullWireSize} <= H - 2T_{CoreInsu}$
			Sec	$Sec_{perlayer} \times Sec_{FullWireSize} <= H - 2T_{CoreInsu}$
		W	Both	$Ml_p \times Pri_{FullWireSize} + Ml_s \times Sec_{FullWireSize} <= W - 3T_{CoreInsu}$
	double-leg	***H***	Pri	$Pri_{perlayer} \times Pri_{FullWireSize} <= H - 2T_{CoreInsu}$
			Sec	$(N_{s3} + 2Ml_s) \times Sec_{FullWireSize} <= H - 2T_{CoreInsu}$
		W	Both	$Ml_p \times Pri_{FullWireSize} + N_{s2} \times Sec_{FullWireSize} <= W - 3T_{CoreInsu}$
U/UR core	-	***H***	Both	$Pri_{perlayer} \times Pri_{FullWireSize} + N_{s1} \times Sec_{FullWireSize} <= H - 3T_{CoreInsu}$
		W	Both	$Ml_p \times Pri_{FullWireSize} + N_{s2} \times Sec_{FullWireSize} <= W - 3T_{CoreInsu}$ and $Ml_s \times Sec_{FullWireSize} + N_{s2} \times Sec_{FullWireSize} <= W - 2T_{CoreInsu}$

Table B.3: Constrains on primary and secondary winding to fit in the window area

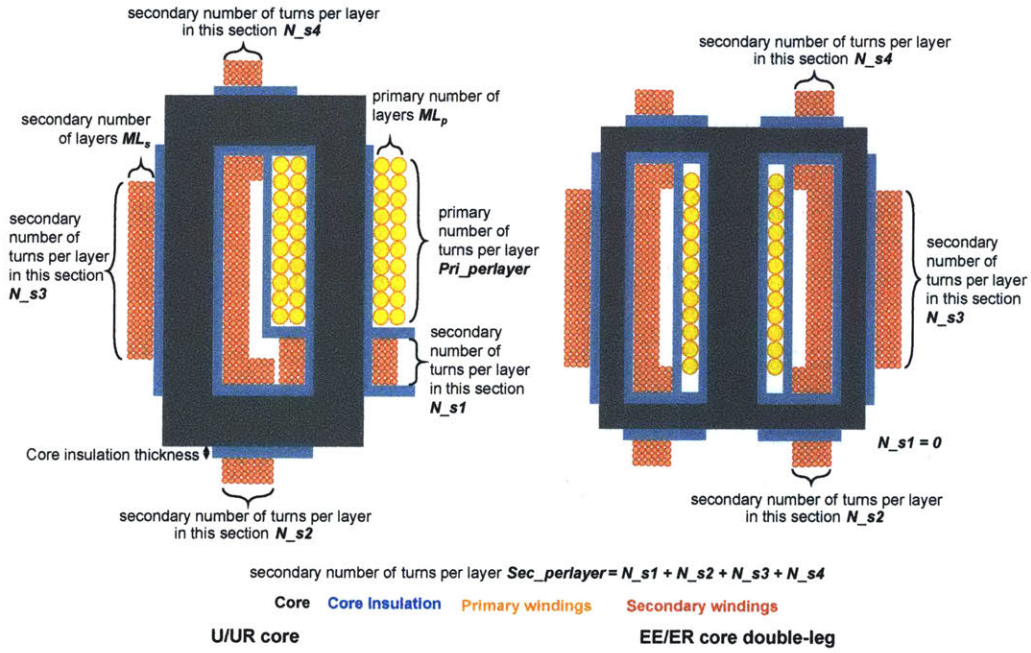


Figure B-4: Annotations of the winding for E core double-leg and U core. For E core double-leg, we limit $N_{s1} = 0$ and $N_{s2} = N_{s4}$ for simplicity.

B.4 Weight estimation

- Core weight: density $4.8\,\mathrm{g/cm^3}$, weight is $W_{core} = \rho_{core} V_{core}$

- Wire copper weight: density $8.96\,\mathrm{g/cm^3}$, primary and secondary wire weights

are

$$W_{pri_{wire}} = \rho_{copper}\pi\frac{Pri^2_{WireSize}}{4}$$
$$W_{sec_{wire}} = \rho_{copper}\pi\frac{Sec^2_{wiresize}}{4}$$

- Wire insulation weight: assume TEFLON, densitys 2.2 g/cm^3 [133], primary and secondary wire insulation weights are

$$W_{pri_{insu}} = \rho_{TEFLON}\pi\frac{Pri^2_{FullWireSize} - Pri^2_{WireSize}}{4}$$
$$W_{sec_{insu}} = \rho_{TEFLON}\pi\frac{Sec^2_{FullWireSize} - Sec^2_{WireSize}}{4}$$

- Core insulation weight: assume TEFLON, density 2.2 g/cm^3 [133], weight is $W_{CoreInsu} = \rho_{TEFLON}V_{CoreInsu}$ where core insulation volume is defined as $V_{CoreInsu}$
  - EE core, $V_{CoreInsu} = T_{CoreInsu}(2H(L_c+2T)+4W(L_c+2T)+H(2L_c+2T))$
  - U core, $V_{CoreInsu} = T_{CoreInsu}(2H(2L_c+2T)+2W(2L_c+2T))$
  - ER core, $V_{CoreInsu} = T_{CoreInsu}(2H\sqrt{2}\pi r_{Ac}+4W\sqrt{2}\pi r_{Ac}+H2\pi r_{Ac})$
  - UR core, $V_{CoreInsu} = T_{CoreInsu}(2H2\pi r_{Ac}+2W2\pi r_{Ac})$

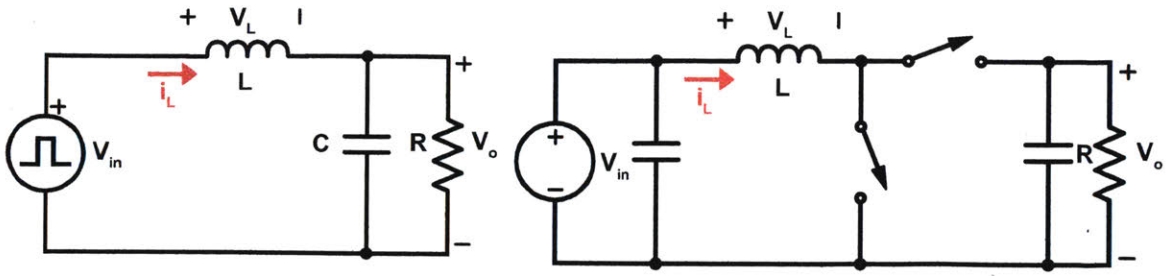
Appendix C

Weight study of inductor

Similar with Appendix B, this appendix contains the core of the weight study of inductors in Chapter 2, Chapter 4 and Chapter 5. For clarity, we mirror the sections in Appendix B here with updated assumptions and equations for an inductor - some may be repetitive since most of the models and constrains used for transformers apply to inductors too.

The inductor considered in this thesis is EE-core or ER-core based and gapped in the center leg. We consider two operating conditions of the inductor in this thesis: a) In Chapter 2, 4 and part of Chapter 5, we assume the inductor L resonates with a capacitor C in a parallel resonant tank driven by a 50%-duty-ratio square-wave ac source (Fig. C-1a). We estimate the core loss with the standard Steinmetz equations. b) In Chapter 5 the Resonant-Transition Boost Converter (RTC) section, we assume the inductor L operates in the RTC (Fig. C-1b) and include the dc current loss when estimating the copper loss.

Similar with Fig. B-1, Fig. C-2 shows a high-level flow chart of the weight study. Each operating point is defined by four parameters: inductor maximum current $\mathbf{I_{Lmax}}$, inductance $\mathbf{L}$, frequency $\mathbf{f}$ and output power $\mathbf{P_o}$ of either the resonant tank or the RTC.



(a) Inductor in a resonant tank (b) Inductor in a RTC boost converter

Figure C-1: Inductor schematics

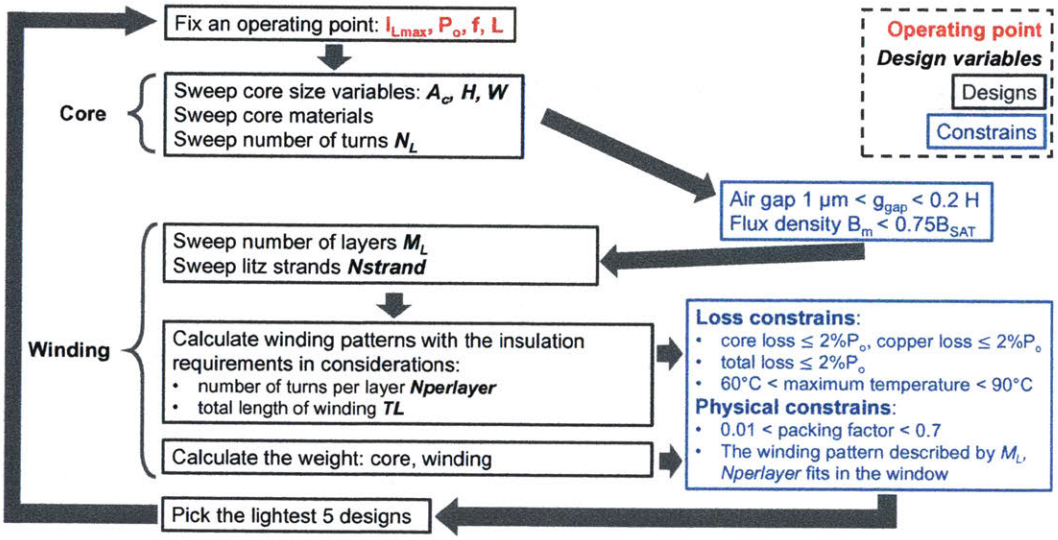


Figure C-2: Weight study flow chart for the inductor.

C.1 Core

C.1.1 Core dimensions

We consider EE and/or ER cores for inductor design, same as the ER core shown in Fig. B-2. The parameters defining the core size is the same as in Chapter B. One additional parameters for the inductor is the airgap:

- For the resonant tank inductor, we calculate the airgap from the inductance and other core-size related parameters $\boldsymbol{g_{gap}} = \frac{\mu_0 A_c N_L^2}{L} - \frac{L_e}{\mu_r}$.
- For the inductor in a resonant transition boost converter, we do vise versa: sweep the airgap between 0.1 mm to 10 mm, and calculate the inductance.

C.1.2 Core material and losses

The core loss $\boldsymbol{P_{core}}$ is estimated using:

- Standard Steinmetz equations in the case where the inductor only sees ac current

$$P_{core} = CoreLossMultiple \times V_{core} \times K_1 \times f^{\alpha} \times B_m^{\beta} \tag{C.1}$$

- In the above equations, B is instantaneous B field and B_m is the maximum B field where

$$B_m = \frac{\mu_0 N_L I_{Lmax}}{L_e \mu_e}, \mu_e = \frac{\mu_r}{1 + \frac{\mu_r g_{gap}}{L_e}} \tag{C.2}$$

- ***CoreLossMultiple*** is set to 1.5 and Steinmetz parameters K_1, α and β are calculated for the operating point frequency f from the manufacture datasheet.

C.2 Winding

C.2.1 Wires and winding patterns

We consider center-leg winding for the inductor design (Fig. B-3). There are 6 parameters defining the winding pattern, 3 of which are swept as variables, and the rest are calculated:

- Sweeping variables (3):
  - Number of turns $\boldsymbol{N_L}$
  - Number of layers $\boldsymbol{Ml}$
  - The number of strands of litz in the wire, ***Nstrand***, swept from *MinNstrands* to *MaxNstrands* with one strand incrementally:

$$MinNstrands = floor(\frac{\frac{2I_{L_{max}}}{J_{wmax}}}{\pi\frac{ds^2}{4}}) + 1; \tag{C.3}$$

$$MaxNstrands = floor(\frac{\frac{1.2\times 2I_{L_{max}}}{J_{wmax}}}{\pi\frac{ds^2}{4}}) + 1; \tag{C.4}$$

- In the above equations, η is the targeted inductor efficiency (set to 98%), J_{wmax} is the maximum current density (set to 500 A/cm^3), ds is the diameter of a single strand litz, where ds = max(skin depth at f, minimal available litz diameter).

- Calculated parameters (3):

  - Numbers of turns per layer $\boldsymbol{Nperlayer} = floor(\frac{N_L}{Ml}) + 1$
  - Wire diameter ***WireSize*** and overall diameter ***FullWireSize***:

$$WireSize = 2\sqrt{\frac{Nstrand\frac{ds^2}{4}}{LitzFactor}}$$

$$FullWireSize = WireSize + 2\frac{V_{Lmax}}{DielectricStrength}$$

We further calculate the winding total length $\boldsymbol{TL} = 2\pi N_L(r_{Ac} + T_{LCoreInsu} + 0.5Ml \times FullWireSize)$ for future use (to calculate copper loss, weight, etc)[1].

C.2.2 Copper loss

Copper loss is estimated using the same Dowell's equations as for the transformer.

$$F_r = X(\frac{sinh(2X) + sin(2X)}{cosh(2X) - cos(2X)} + \frac{2(Ml^2 N_{strand} - 1)}{3}\frac{sinh(X) - sin(X)}{cosh(X) + cos(X)})$$

$$X = \frac{ds}{2skindepth\sqrt{\pi K}}, K = \frac{\sqrt{\pi N_{strand}}ds}{2WireSize}$$

Therefore in the case where the inductor current only contains ac component, the copper loss is:

$$P_{copper} = I_{L_{rms}}^2 R_{ac}$$

$$R_{ac} = R_{dc}F_r = F_r\frac{\rho TL}{\frac{\pi WireSize^2}{4}}$$

[1] $T_{LCoreInsu}$ is the core insulation thickness, calculated as $T_{LCoreInsu} = \frac{V_{Lmax}}{DielectricStrength}$. We assume all insulation materials used is TEFLON with a $DielectricStrength$ of 100 kV/cm [133]. $V_{Lmax}$is the maximum inductor voltage, which can be calculated from I_{Lmax}

In the case where the inductor current has dc bias, the copper loss is:

$$Pcopper = I_{L_{ave}}^2 Rdc + I_{L_{ac_{1rms}}}^2 R_{ac}$$

Where $I_{L_{ave}}$ is the average inductor current and $I_{L_{ac_{1rms}}}$ is the rms of the fundamental of the inductor current ac component.

C.3 Constrains

C.3.1 Loss and thermal constrains

Losses: core loss P_{core}, copper loss P_{copper} and total loss $P_{core} + P_{copper}$ all less than 2% of P_o, corresponding to the targeted efficiency $\eta > 98\%$.

Current density: as mentioned in Section C.2, we impose a current density limit of 500 A/cm^3 on wires.

Flux density: the maximum flux density B_m needs to be smaller than 75% of the saturation flux density of the core material B_{SAT}.

Steady state temperature is calculated in the same way as for transformer.

$$R_{th} = 0.01631(A_c W_a)^{-0.405}$$

$$T_{absolute} = R_{th}(P_{copper} + P_{core}) + 25$$

$$60°C \leqslant T_{absolute} \leqslant 90°C$$

C.3.2 Physical constrains

Overall packing factor: defined as the percentage the area taken by the wires (both copper and wire jackets) in the window area

$$Overallpackingfactor = \frac{\pi N_L FullWireSize^2}{4W_a}$$

$$0.01 \leqslant Overallpackingfactor \leqslant 0.7$$

Windings fit the window in both $\boldsymbol{H}$ and $\boldsymbol{W}$ directions considering insulation:

- For the $\boldsymbol{H}$ direction, $N_{perlayer} \times FullWireSize <= H - 2T_{LCoreInsu}$
- For the $\boldsymbol{W}$ direction, $Ml \times FullWireSize <= W - 3T_{LCoreInsu}$

C.4 Weight estimation

- Core weight: density $4.8\,\mathrm{g/cm^3}$, weight is $W_{core} = \rho_{core} V_{core}$
- Wire copper weight: density $8.96\,\mathrm{g/cm^3}$, $W_{wire} = \rho_{copper} \pi \frac{WireSize^2}{4}$
- Wire insulation weight: assume TEFLON, densitys $2.2\,\mathrm{g/cm^3}$ [133], $W_{WireInsu} = \rho_{TEFLON} \pi \frac{FullWireSize^2 - WireSize^2}{4}$
- Core insulation weight: assume TEFLON, density $2.2\,\mathrm{g/cm^3}$ [133], same as in Chapter B.

Appendix D

First generation HVDC

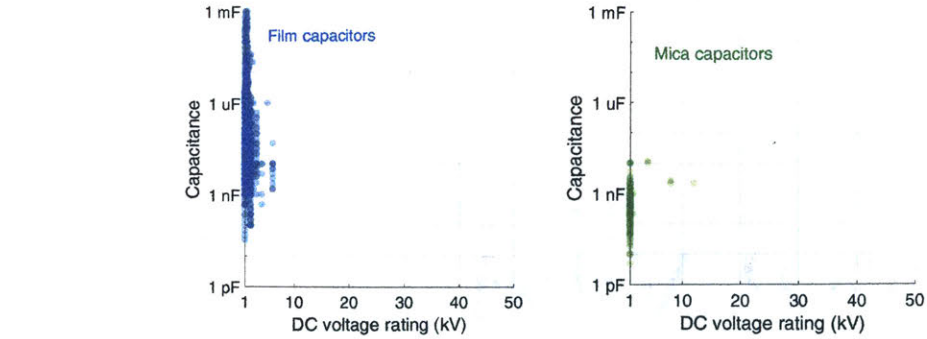
This appendix contains the detailed weight study of the voltage multiplier in Section D.1 and that of the core-based and the air-core transformers in Section D.2. Section D.3 explains the details of the weight optimization of the inverter and the transformer stage. Section D.4 includes the build process of the hardware. Section D.5 details how to set up a high voltage experimental apparatus in general.

D.1 Voltage multiplier

D.1.1 Diodes and capacitors

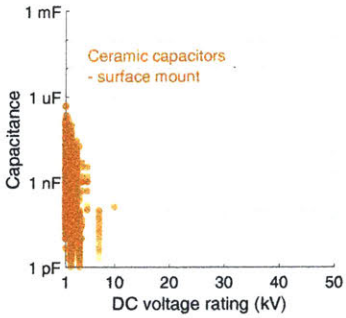
Capacitors from Digikey that block in between 1 to 15 kV are surveyed. They are divided into 5 groups according to their type and form factor (two main factors driving the weight). Their capacitances and dc voltage rating are plotted in Fig. D-1. The weight of selected capacitors is measured as in Table. D.2. Linear relationships for ceramic SMT capacitors rated in 1–6.3 kV are plotted in Fig. D-2. Together with Fig. 2-1, these linear relationships are used in the weight study of voltage multiplier.

Several diodes that block between 1 to 15 kV are surveyed and listed in Table. D.1.

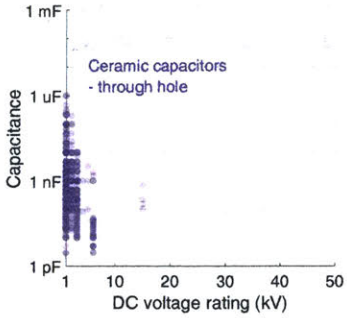


(a) Film capacitors

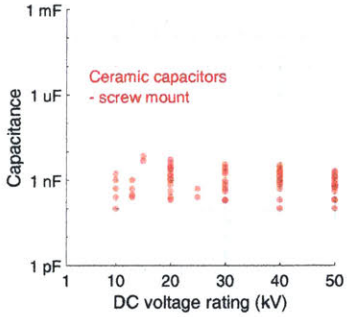
(b) Mica capacitors



(c) Ceramic SMT



(d) Ceramic through-hole



(e) Ceramic screw-mount

Figure D-1: Capacitances and dc rated voltages of different types of high voltage capacitors (1 - 15 kV) from Digikey (active and in stock in Nov. 2019).

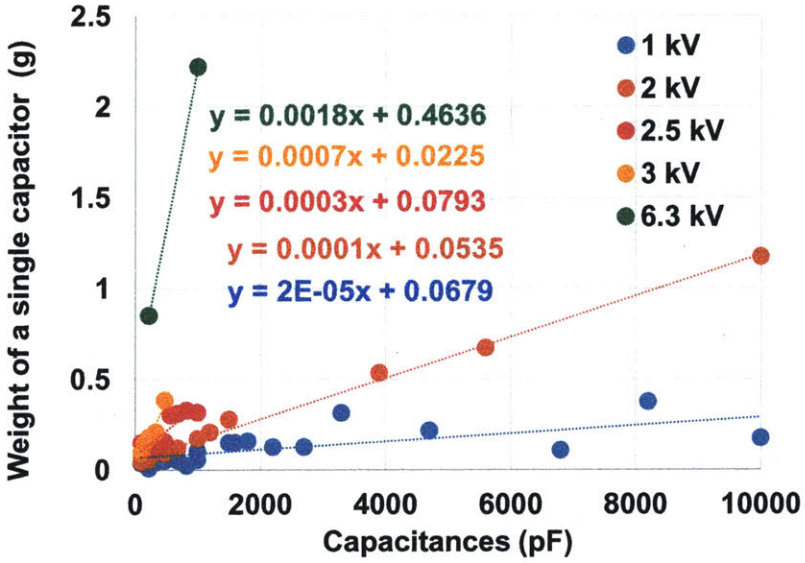


Figure D-2: Capacitance and voltage dependency of high-voltage capacitors in 1–6.3 kV (the dots are the measured weights and the lines are their polynomial fits.)

Manufacturer	Part No.	Vbr (kV)	Vfr (V)	Cj0 (pF) @ 50V	Recovery		Weight (g)
					Trr (ns)	Qrr/Qc (nC)	
Cree	C4D02120A	1.2	1.8	35	-	11	
	C3D10170H	1.7	2	150	-	96	
Rohm	SCS205KG	1.2	1.6	55	-	17	
Infineon	IDH02SG120	1.2	1.8	25	-	7.2	
VISHAY	BYG2T-M3	1.3	1.39	5 (@20V)	75		0.64
	SF1200/1600	1.2/1.6	3.4	5	75		0.469
GeneSiC	GB01SLT12-214	1.2	1.8	20	-	13	0.088
	GAP3SLT33-214	3.3	1.7	14	-	52	0.065
	GAP05SLT80-220	8	4.6	12	-	8	-
Dean technology	SP8SG	8	18	0.8	75		
	UX-F15B	15	16	3.7	50		
Voltage Multipliers	1N6533/SMF6533	5	9	1	70		
	Z100FF3	10	25	8.5	30		
	X100FF3	10	25	2	30		0.5
	X150FF3	15	37.5	2	30		0.51

Table D.1: List of high voltage diodes considered in the voltage multiplier study for 1st generation high voltage dc-dc power converter.

Manufacturer	Part No.	Material	Mounting	Rated Voltage (kV)	Capacitance (pF)	Weight (g)	Energy Stored per gram (mJ/g)
Vishay	VJ1206A221JXGAT5Z	Ceramic C0G	SMT	1	220	0.03	3.67
Vishay	VJ1210A222JXRAT5Z	Ceramic C0G	SMT	1.5	2200	0.07	35.36
KEMET	C0603C221JDGACAUTO	Ceramic C0G	SMT	1	220	0.0045	24.44
KEMET	C0805C821JDGACAUTO	Ceramic C0G	SMT	1	820	0.0137	29.93
KEMET	C1206C101JDGACTU	Ceramic C0G	SMT	1	100	0.019	2.63
KEMET	C1206C151JDGACTU	Ceramic C0G	SMT	1	150	0.0265	2.83
KEMET	C1206C181JDGAC7800	Ceramic C0G	SMT	1	180	0.0187	4.81
KEMET	C1206C331JDGAC7800	Ceramic C0G	SMT	1	330	0.0224	7.37
KEMET	C1206C471JDGACTU	Ceramic C0G	SMT	1	470	0.0312	7.53
KEMET	C1206C681JDGAC7800	Ceramic C0G	SMT	1	680	0.0328	10.37
KEMET	C1206C102JDGACTU	Ceramic C0G	SMT	1	1000	0.0361	13.85
KEMET	C1210C222JDGACTU	Ceramic C0G	SMT	1	2200	0.0936	11.75
KEMET	C1210H272JDGACTU	Ceramic C0G	SMT	1	2700	0.0937	14.41
KEMET	C1210C682JDGACAUTO	Ceramic C0G	SMT	1	6800	0.0758	44.85
KEMET	C1812C152JDGACTU	Ceramic C0G	SMT	1	1500	0.0934	8.03
KEMET	C1812C472JDGACTU	Ceramic C0G	SMT	1	4700	0.1589	14.79
KEMET	C1812C103JDGACAUTO	Ceramic C0G	SMT	1	10000	0.1174	42.59
KEMET	C1825C332JDGAC7800	Ceramic C0G	SMT	1	3300	0.202	8.17
KEMET	C2225C822JDGAC7800	Ceramic C0G	SMT	1	8200	0.236	17.37
KEMET	C1206C101JGGACTU	Ceramic C0G	SMT	2	100	0.0229	8.73
KEMET	C1206C151JGGAC7800	Ceramic C0G	SMT	2	150	0.0313	9.58
KEMET	C1206C221JGGACAUTO	Ceramic C0G	SMT	2	220	0.0365	12.05
KEMET	C1210C331JGGACTU	Ceramic C0G	SMT	2	330	0.066	10.00
KEMET	C1808C471JGGAC7800	Ceramic C0G	SMT	2	470	0.0541	17.38
KEMET	C1808C681JGGAC7800	Ceramic C0G	SMT	2	680	0.0829	16.41
KEMET	C1812C102JGGACTU	Ceramic C0G	SMT	2	1000	0.1164	17.18
KEMET	C1812H122JGGACTU	Ceramic C0G	SMT	2	1200	0.1507	15.93
KEMET	C1825C152JGGACTU	Ceramic C0G	SMT	2	1500	0.1657	18.11
KEMET	C2225C392JGGACTU	Ceramic C0G	SMT	2	3900	0.3946	19.77
KEMET	C2824C562JGGACAUTO	Ceramic C0G	SMT	2	5600	0.5029	22.27
KEMET	C3040H103JGGACT050	Ceramic C0G	SMT	2	10000	0.8705	22.98
KEMET	C1808C221JZGACTU	Ceramic C0G	SMT	2.5	220	0.0795	8.65
KEMET	C1808C331JZGAC7800	Ceramic C0G	SMT	2.5	330	0.0779	13.24

Manufacturer	Part No.	Material	Mounting	Rated Voltage (kV)	Capacitance (pF)	Weight (g)	Energy Stored per gram (mJ/g)
KEMET	C1812C101JZGAC7800	Ceramic C0G	SMT	2.5	100	0.0935	3.34
KEMET	C1812C471JZGACTU	Ceramic C0G	SMT	2.5	470	0.1	14.69
KEMET	C1825C561JZGACTU	Ceramic C0G	SMT	2.5	560	0.1911	9.16
KEMET	C1825C821JZGACTU	Ceramic C0G	SMT	2.5	820	0.2168	11.82
KEMET	C2220C681JZGACTU	Ceramic C0G	SMT	2.5	680	0.1989	10.68
KEMET	C2220C102JZGACTU	Ceramic C0G	SMT	2.5	1000	0.2067	15.12
KEMET	C1808C101JHGAC7800	Ceramic C0G	SMT	3	100	0.0581	7.75
KEMET	C1812C151JHGACTU	Ceramic C0G	SMT	3	150	0.0926	7.29
KEMET	C1812C221JHGACAUTO	Ceramic C0G	SMT	3	220	0.1231	8.04
KEMET	C1812C331JHGAC7800	Ceramic C0G	SMT	3	330	0.1536	9.67
KEMET	C2225C471JHGACTU	Ceramic C0G	SMT	3	470	0.2445	8.65
Murata	DEBE33D102ZA2B	Ceramic E	Leads	2	1000	0.32	6.25
Murata	GR455DR73D103KW01L	Ceramic X7R	SMT	2	10000	0.29	68.97
Murata	DECB33J221KC4B	Ceramic B	Leads	6.3	220	0.85	5.14
Murata	DECB33J102KC4B	Ceramic B	Leads	6.3	1000	2.22	8.94
Vishay	615R100GAST50	Ceramic Y5R	Leads	10	500	2.89	8.65
Murata	DHR4E4A151K2BB	Ceramic ZM	Leads	10	150	0.873	8.59
Murata	DHR4E4A221K2BB	Ceramic ZM	Leads	10	220	0.92	11.96
Murata	DHR4E4A102K2BB	Ceramic ZM	Leads	10	1000	2.86	17.48
Murata	FD-10AU	Ceramic Y5P	Screw	10	250	16.89	0.74
Murata	DHR4E4B221K2BB	Ceramic ZM	Leads	12	220	1.156	13.70
Murata	DHR4E4B331K2BB	Ceramic ZM	Leads	12	330	1.5	15.84
Murata	DHR4E4B102K2BB	Ceramic ZM	Leads	12	1000	3.52	20.45
Vishay	615R150GATD10AM	Ceramic Y5R	Leads	15	1000	18.48	6.09
Murata	DHR4E4C221K2BB	Ceramic ZM	Leads	15	220	1.5	16.50
Murata	DHR4E4C471K2BB	Ceramic ZM	Leads	15	470	2.82	18.75
Murata	DHR4E4C681K2BB	Ceramic ZM	Leads	15	680	3.82	20.03
Murata	DHR4E4C102K2FB	Ceramic ZM	Leads	15	1000	5.6	20.09
Murata	DHS4E4D881MHXB	Ceramic ZM	Screw	20	880	39.3	4.48
Murata	UHV-224A	Ceramic Z5T	Screw	20	1000	50.64	3.95
KEMET	746F110GY00M	Film	Leads	2	1100	0.69	3.19
MWS	152MWS402KG	Film	Leads	4	15000	3.289	36.49
MWS	152MWS103KT	Film	Leads	10	15000	8.8	85.23

Table D.2: List of capacitors considered in the voltage multiplier study for 1st generation high voltage dc-dc power converter. Energy stored per gram is calculated by $0.5C(RatedVoltage)^2/weight$. Please note that the part numbers ends with "AUTO" usually have lower weight at the same voltage and capacitance, presumably because they are designed for automotive industry where weight is also a critical for system performance.

D.1.2 Analysis of the voltage multipliers (VMs) in the slow-switching limit

We decide the capacitance values by assuming the VM is in slow-switching limit (SSL) (assume the capacitor's voltage shows obvious charge and discharge in each switching state and result in losses (i.e., a voltage droop at the load terminal compared with no load cases).

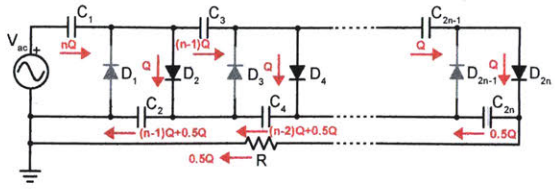
Type	Elements	Stage 1	Stage 2	...	Stage n-1	Stage n
Half-wave CW	Odd Caps	$C_1 : nQ$	$C_3 : (n-1)Q$	...	$C_{2n-3} : 2Q$	$C_{2n-1} : Q$
	Even Caps	$C_2 : (n-0.5)Q$	$C_4 : (n-1.5)Q$	...	$C_{2n-2} : 1.5Q$	$C_{2n} : 0.5Q$
	Diodes	$D_1, D_2 : Q$	$D_3, D_4 : Q$	...	$D_{2n-3}, D_{2n-2} : Q$	$D_{2n-1}, D_{2n} : Q$
Half-wave Dickson	Odd Caps	$C_1 : Q$	$C_3 : Q$	...	$C_{2n-3} : Q$	$C_{2n-1} : Q$
	Even Caps	$C_2 : (n-0.5)Q$	$C_4 : (n-1.5)Q$	...	$C_{2n-2} : 1.5Q$	$C_{2n} : 0.5Q$
	Diodes	$D_1, D_2 : Q$	$D_3, D_4 : Q$	...	$D_{2n-3}, D_{2n-2} : Q$	$D_{2n-1}, D_{2n} : Q$
Full-wave CW	Odd Caps	$C_1 : 0.5nQ$	$C_3 : 0.5(n-1)Q$	...	$C_{2n-3} : Q$	$C_{2n-1} : 0.5Q$
	Even Caps	$C_2 : 0$	$C_4 : 0$	...	$C_{2n-2} : 0$	$C_{2n} : 0$
	Diodes	$D_1 - D_4 : 0.5Q$	$D_5 - D_8 : 0.5Q$	...	$D_{4n-7} - D_{4n-4} : 0.5Q$	$D_{4n-3} - D_{4n} : 0.5Q$
Full-wave Dickson	Odd Caps	$C_1 : 0.5Q$	$C_3 : 0.5Q$	...	$C_{2n-3} : 0.5Q$	$C_{2n-1} : 0.5Q$
	Even Caps	$C_2 : 0$	$C_4 : 0$	...	$C_{2n-2} : 0$	$C_{2n} : 0$
	Diodes	$D_1 - D_4 : 0.5Q$	$D_5 - D_8 : 0.5Q$	...	$D_{4n-7} - D_{4n-4} : 0.5Q$	$D_{4n-3} - D_{4n} : 0.5Q$

Table D.3: Charge flow through each diode/capacitor in four VM topologies (a summary of Fig. D-3)

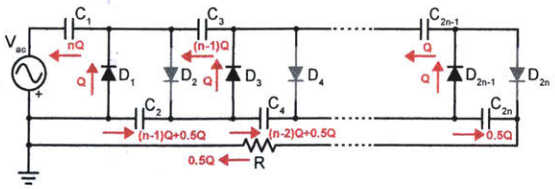
Type	Elements	Stage 1	Stage 2	...	Stage n-1	Stage n
Half-wave CW	Odd Caps	$C_1 : V_{ac}$	$C_3 : 2V_{ac}$	...	$C_{2n-3} : 2V_{ac}$	$C_{2n-1} : 2V_{ac}$
	Even Caps	$C_2 : 2V_{ac}$	$C_4 : 2V_{ac}$	...	$C_{2n-2} : 2V_{ac}$	$C_{2n-2} : 2V_{ac}$
	Diodes	$D_1, D_2 : 2V_{ac}$	$D_3, D_4 : 2V_{ac}$	...	$D_{2n-3}, D_{2n-2} : 2V_{ac}$	$D_{2n-1}, D_{2n} : 2V_{ac}$
Half-wave Dickson	Odd Caps	$C_1 : V_{ac}$	$C_3 : 3V_{ac}$	...	$C_{2n-3} : (2n-3)V_{ac}$	$C_{2n-1} : (2n-1)V_{ac}$
	Even Caps	$C_2 : 2V_{ac}$	$C_4 : 2V_{ac}$	...	$C_{2n-2} : 2V_{ac}$	$C_{2n-2} : 2V_{ac}$
	Diodes	$D_1, D_2 : 2V_{ac}$	$D_3, D_4 : 2V_{ac}$	...	$D_{2n-3}, D_{2n-2} : 2V_{ac}$	$D_{2n-1}, D_{2n} : 2V_{ac}$
Full-wave CW	Odd Caps	$C_1 : 0.5V_{ac}$	$C_3 : V_{ac}$	...	$C_{2n-3} : V_{ac}$	$C_{2n-1} : V_{ac}$
	Even Caps	$C_2 : V_{ac}$	$C_4 : V_{ac}$	...	$C_{2n-2} : V_{ac}$	$C_{2n-2} : V_{ac}$
	Diodes	$D_1 - D_4 : V_{ac}$	$D_5 - D_8 : V_{ac}$	...	$D_{4n-7} - D_{4n-4} : V_{ac}$	$D_{4n-3} - D_{4n} : V_{ac}$
Full-wave Dickson	Odd Caps	$C_1 : 0.5V_{ac}$	$C_3 : 1.5V_{ac}$	...	$C_{2n-3} : (n-1.5)V_{ac}$	$C_{2n-1} : (n-0.5)V_{ac}$
	Even Caps	$C_2 : V_{ac}$	$C_4 : V_{ac}$	...	$C_{2n-2} : V_{ac}$	$C_{2n-2} : V_{ac}$
	Diodes	$D_1 - D_4 : V_{ac}$	$D_5 - D_8 : V_{ac}$	...	$D_{4n-7} - D_{4n-4} : V_{ac}$	$D_{4n-3} - D_{4n} : V_{ac}$

Table D.4: Voltage stresses across each diode/capacitor in four VM topologies

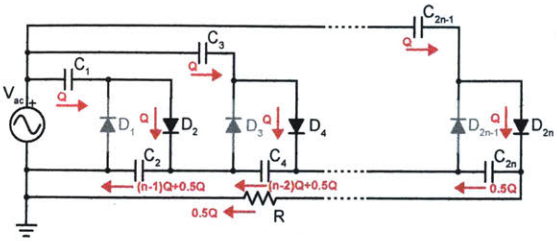
See Fig. D-3 for the charge flow of the 4 VM topologies. The charge flowing through each capacitor and diode is summarized in Table D.3 and the voltage blocked by each capacitor and diode is listed in Table D.4.



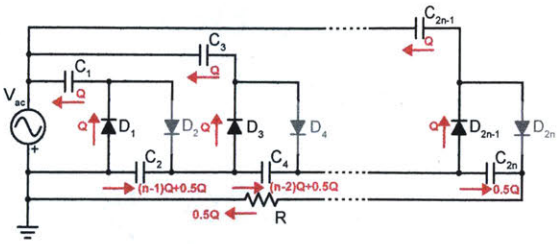
(a) n-stage half-wave CW multiplier: state 1



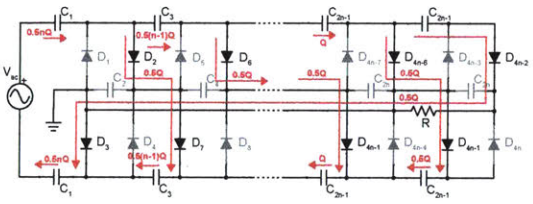
(b) n-stage half-wave CW multiplier: state 2



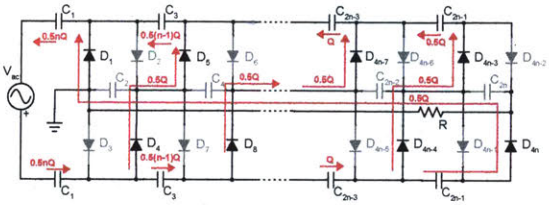
(c) n-stage half-wave Dickson multiplier: state 1



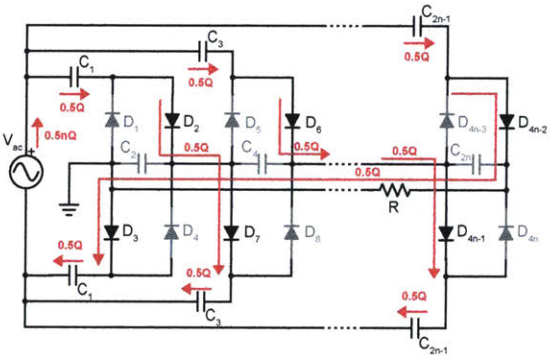
(d) n-stage half-wave Dickson multiplier: state 2



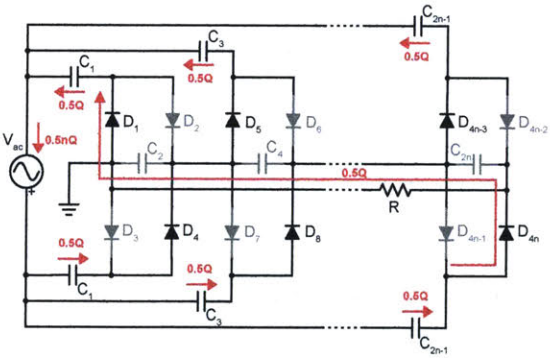
(e) n-stage full-wave CW multiplier: state 1



(f) n-stage full-wave CW multiplier: state 2



(g) n-stage full-wave Dickson multiplier: state 1



(h) n-stage full-wave Dickson multiplier: state 2

Figure D-3: The charge flow of 4 different voltage multiplier topologies. In the analysis, we consider the load as a current source which draws Q every cycle.

Table. D.3 and Table. D.4 are used to 1) size the diode voltage and current in each stage of each topology; 2) calculate the voltage droop due to the capacitors charging and discharging. The charge going through each capcitor listed in Table. D.3 is used to calculate the capacitor voltage at the end of each state, as listed in Table.D.5. These voltages are then used to calculate the voltage droop, as listed in Table. 2.1.

As an example, the load regulation characteristics of a n-stage half-wave CW voltage multiplier is derived below (given all odd-indexed capacitors are C_{odd} and all even-indexed caps are C_{even} shown in Fig. 2-2):

$$
\begin{aligned}
V_{OUT_{max}} &\simeq V_{C_{2(1)}} + V_{C_{4(1)}} + ... + V_{C_{2n-2(1)}} + V_{C_{2n(1)}} \\
&= V_{IN} + V_{C_1(1)} + V_{C_{3(1)}} + ... + V_{C_{2n-3(1)}} + V_{C_{2n-1(1)}} \\
&= V_{IN} + V_{C_1(1)} \\
&+ V_{IN} + V_{C_1(1)} - \frac{Q_2}{C_2} - \frac{Q_3}{C_3} \\
&+ V_{IN} + V_{C_1(1)} - \frac{Q_2}{C_2} - \frac{Q_3}{C_3} - \frac{Q_4}{C_4} - \frac{Q_5}{C_5} \\
&+ ... \\
&+ V_{IN} + V_{C_1(1)} - \frac{Q_2}{C_2} - \frac{Q_3}{C_3} - \frac{Q_4}{C_4} - \frac{Q_5}{C_5} - ... - \frac{Q_{2n-4}}{C_{2n-4}} - \frac{Q_{2n-3}}{C_{2n-3}} \\
&+ V_{IN} + V_{C_1(1)} - \frac{Q_2}{C_2} - \frac{Q_3}{C_3} - \frac{Q_4}{C_4} - \frac{Q_5}{C_5} - ... - \frac{Q_{2n-4}}{C_{2n-4}} - \frac{Q_{2n-3}}{C_{2n-3}} - \frac{Q_{2n-2}}{C_{2n-2}} - \frac{Q_{2n-1}}{C_{2n-1}} \\
&= n(V_{IN} + V_{C_1(1)}) - (n-1)(\frac{Q_2}{C_2} + \frac{Q_3}{C_3}) - (n-2)(\frac{Q_4}{C_4} + \frac{Q_5}{C_5}) - ... \\
&- 2(\frac{Q_{2n-4}}{C_{2n-4}} + \frac{Q_{2n-3}}{C_{2n-3}}) - (\frac{Q_{2n-2}}{C_{2n-2}} - \frac{Q_{2n-1}}{C_{2n-1}}) \\
&= 2nV_{IN} - \left[\frac{n(n+1)(2n+1)}{6C_{odd}} + \frac{n(n-1)(4n-5)}{12C_{even}}\right] Q
\end{aligned}
$$

Since $Q = \frac{I_{Load}}{f}$, we have

$$
V_{OUT_{max}} = 2nV_{IN} - \left[\frac{n(n+1)(2n+1)}{6C_{odd}} + \frac{n(n-1)(4n-5)}{12C_{even}}\right] \frac{I_{Load}}{f}
$$

Table D.5: Capacitor voltages in SSL of four voltage multiplier topologies

Type	Odd	Voltages at the end of		Even	Voltages at the end of	
		State 1	State 2		State 1	State 2
Half-wave CW	C_1	$V_{IN} - \frac{Q_{C_1}}{C_1}$	V_{IN}	C_2	$V_{IN} + V_{C_1(1)}$	$V_{IN} + V_{C_1(1)} - \frac{Q_{C_2}}{C_2}$
	C_3	$V_{C_2(2)} - \frac{Q_{C_3}}{C_3}$	$V_{C_2(2)}$	C_4	$V_{C_3(1)}$	$V_{C_3(1)} - \frac{Q_{C_4}}{C_4}$
	C_5	$V_{C_4(2)} - \frac{Q_{C_5}}{C_5}$	$V_{C_4(2)}$	C_6	$V_{C_5(1)}$	$V_{C_5(1)} - \frac{Q_{C_6}}{C_6}$
	...	...	...	...	...	...
	C_{2n-3}	$V_{C_{2n-4}(2)} - \frac{Q_{C_{2n-3}}}{C_{2n-3}}$	$V_{C_{2n-4}(2)}$	C_{2n-2}	$V_{C_{2n-3}(1)}$	$V_{C_{2n-3}(1)} - \frac{Q_{C_{2n-2}}}{C_{2n-2}}$
	C_{2n-1}	$V_{C_{2n-2}(2)} - \frac{Q_{C_{2n-1}}}{C_{2n-1}}$	$V_{C_{2n-2}(2)}$	C_{2n}	$V_{C_{2n-1}(1)}$	$V_{C_{2n-1}(1)} - \frac{Q_{C_{2n}}}{C_{2n}}$
Half-wave Dickson	C_1	$V_{IN} - \frac{Q_{C_1}}{C_1}$	V_{IN}	C_2	$V_{IN} + V_{C_1(1)}$	$V_{C_2(1)} - \frac{Q_{C_2}}{C_2}$
	C_3	$V_{C_3(2)} - \frac{Q_{C_3}}{C_3}$	$V_{C_1(2)} + V_{C_2(2)}$	C_4	$V_{C_3(1)} - V_{C_1(1)}$	$V_{C_4(1)} - \frac{Q_{C_4}}{C_4}$
	C_5	$V_{C_5(2)} - \frac{Q_{C_5}}{C_5}$	$V_{C_3(2)} + V_{C_4(2)}$	C_6	$V_{C_5(1)} - V_{C_3(1)}$	$V_{C_6(1)} - \frac{Q_{C_6}}{C_6}$
	...	...	...	...	...	...
	C_{2n-3}	$V_{C_{2n-3}(2)} - \frac{Q_{C_{2n-3}}}{C_{2n-3}}$	$V_{C_{2n-5}(2)} + V_{C_{2n-4}(2)}$	C_{2n-2}	$V_{C_{2n-3}(1)} - V_{C_{2n-5}(1)}$	$V_{C_{2n-2}(1)} - \frac{Q_{C_{2n-2}}}{C_{2n-2}}$
	C_{2n-1}	$V_{C_{2n-1}(2)} - \frac{Q_{C_{2n-1}}}{C_{2n-1}}$	$V_{C_{2n-3}(2)} + V_{C_{2n-2}(2)}$	C_{2n}	$V_{C_{2n-1}(1)} - V_{C_{2n-3}(1)}$	$V_{C_{2n}(1)} - \frac{Q_{C_{2n}}}{C_{2n}}$
Full-wave CW	C_1	$V_{IN} - \frac{Q_{C_1}}{C_1}$	V_{IN}	C_2	$V_{C_1(1)}$	$V_{C_1(1)} - \frac{Q_{C_2}}{C_2}$
	C_3	$V_{C_2(2)} - \frac{Q_{C_3}}{C_3}$	$V_{C_2(2)}$	C_4	$V_{C_3(1)}$	$V_{C_3(1)} - \frac{Q_{C_4}}{C_4}$
	C_5	$V_{C_4(2)} - \frac{Q_{C_5}}{C_5}$	$V_{C_4(2)}$	C_6	$V_{C_5(1)}$	$V_{C_5(1)} - \frac{Q_{C_6}}{C_6}$
	...	...	...	...	...	...
	C_{2n-3}	$V_{C_{2n-4}(2)} - \frac{Q_{C_{2n-3}}}{C_{2n-3}}$	$V_{C_{2n-4}(2)}$	C_{2n-2}	$V_{C_{2n-3}(1)}$	$V_{C_{2n-3}(1)} - \frac{Q_{C_{2n-2}}}{C_{2n-2}}$
	C_{2n-1}	$V_{C_{2n-2}(2)} - \frac{Q_{C_{2n-1}}}{C_{2n-1}}$	$V_{C_{2n-2}(2)}$	C_{2n}	$V_{C_{2n-1}(1)}$	$V_{C_{2n-1}(1)} - \frac{Q_{C_{2n}}}{C_{2n}}$
Full-wave Dickson	C_1	$V_{IN} - \frac{Q_{C_1}}{C_1}$	V_{IN}	C_2	$V_{C_1(1)}$	$V_{C_1(1)} - \frac{Q_{C_2}}{C_2}$
	C_3	$V_{C_2(2)} - \frac{Q_{C_3}}{C_3}$	$V_{C_2(2)}$	C_4	$V_{C_3(1)}$	$V_{C_3(1)} - \frac{Q_{C_4}}{C_4}$
	C_5	$V_{C_4(2)} - \frac{Q_{C_5}}{C_5}$	$V_{C_4(2)}$	C_6	$V_{C_5(1)}$	$V_{C_5(1)} - \frac{Q_{C_6}}{C_6}$
	...	...	...	...	...	...
	C_{2n-3}	$V_{C_{2n-4}(2)} - \frac{Q_{C_{2n-3}}}{C_{2n-3}}$	$V_{C_{2n-4}(2)}$	C_{2n-2}	$V_{C_{2n-3}(1)}$	$V_{C_{2n-3}(1)} - \frac{Q_{C_{2n-2}}}{C_{2n-2}}$
	C_{2n-1}	$V_{C_{2n-2}(2)} - \frac{Q_{C_{2n-1}}}{C_{2n-1}}$	$V_{C_{2n-2}(2)}$	C_{2n}	$V_{C_{2n-1}(1)}$	$V_{C_{2n-1}(1)} - \frac{Q_{C_{2n}}}{C_{2n}}$

D.1.3 Weight study of voltage multipliers

Details of weight simulations

The details of all simulations in Fig. 2-3 are listed in Table. D.6.

Topology	Number of stage	Total weight (g)	Total capacitance (nF)	Flying cap energy (mJ)	Output cap energy (mJ)	Output impedance (kohm)	Flying capacitance in each stage (pF)	Flying Capacitor Blocking Voltage in Stage x (x = 1, 2, ...)																				Output capacitance in each stage (pF)	Output cap blocking voltage in each stage (V)
								1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		
Half-wave CW	1	25.67	0.56	3.8	75.0	26.7	75	10000																				375	20000.0
	2	59.61	4.37	23.4	150.0	27.3	375	5000	10000																			1500	10000.0
	3	75.96	13.58	52.5	225.0	28.7	1050	3333	6667	6667																		3375	6666.7
	4	122.53	34.13	91.4	300.0	30.3	2250	2500	5000	5000	5000																	6000	5000.0
	5	183.43	69.84	140.3	375.0	32.0	4125	2000	4000	4000	4000	4000																9375	4000.0
	6	211.73	126.05	199.1	450.0	33.7	6825	1667	3333	3333	3333	3333	3333															13500	3333.3
	7	197.58	207.40	267.9	525.0	35.4	10500	1429	2857	2857	2857	2857	2857	2857														18375	2857.1
	8	305.37	320.47	346.6	600.0	37.2	15300	1250	2500	2500	2500	2500	2500	2500	2500													24000	2500.0
	9	316.33	485.87	435.4	675.0	38.9	21375	1111	2222	2222	2222	2222	2222	2222	2222	2222												30375	2222.2
	10	442.57	680.00	534.2	750.0	40.7	28875	1000	2000	2000	2000	2000	2000	2000	2000	2000	2000											37500	2000.0
	11	396.74	962.50	643.0	825.0	42.4	37950	909	1818	1818	1818	1818	1818	1818	1818	1818	1818	1818										45375	1818.2
	12	515.16	1280.00	761.7	900.0	44.2	48750	833	1667	1667	1667	1667	1667	1667	1667	1667	1667	1667	1667									54000	1666.7
	13	691.52	1686.60	890.5	975.0	45.9	61425	769	1538	1538	1538	1538	1538	1538	1538	1538	1538	1538	1538	1538								63375	1538.5
	14	889.15	2170.00	1029.2	1050.0	47.7	76125	714	1429	1429	1429	1429	1429	1429	1429	1429	1429	1429	1429	1429	1429							73500	1428.6
	15	1107.93	2700.00	1178.0	1125.0	49.5	93000	667	1333	1333	1333	1333	1333	1333	1333	1333	1333	1333	1333	1333	1333	1333						84375	1333.3
Half-wave Dickson	1	25.67	0.56	3.8	75.0	26.7	75	10000																				375	20000.0
	2	57.58	3.78	18.8	0.2	28.7	150	5000	15000																			1500	10000.0
	3	70.43	10.91	43.8	0.2	30.5	225	3333	10000	16667																		3375	6666.7
	4	114.19	25.83	78.8	0.3	32.3	300	2500	7500	12500	17500																	6000	5000.0
	5	175.10	49.37	123.8	0.4	34.1	375	2000	6000	10000	14000	18000																9375	4000.0
	6	200.21	86.92	178.8	0.5	35.9	450	1667	5000	8333	11667	15000	18333															13500	3333.3
	7	213.30	135.13	243.8	0.5	37.7	525	1429	4286	7143	10000	12857	15714	18571														18375	2857.1
	8	285.45	199.54	318.8	0.6	39.5	600	1250	3750	6250	8750	11250	13750	16250	18750													24000	2500.0
	9	303.18	294.19	403.8	0.7	41.3	675	1111	3333	5556	7778	10000	12222	14444	16667	18889												30375	2222.2
	10	411.02	389.04	498.8	0.8	43.1	750	1000	3000	5000	7000	9000	11000	13000	15000	17000	19000											37500	2000.0
	11	397.56	533.10	603.8	0.8	44.8	825	909	2727	4545	6364	8182	10000	11818	13636	15455	17273	19091										45375	1818.2
	12	473.17	671.75	718.8	0.9	46.6	900	833	2500	4167	5833	7500	9167	10833	12500	14167	15833	17500	19167									54000	1666.7
	13	560.56	858.54	843.8	1.0	48.4	975	769	2308	3846	5385	6923	8462	10000	11538	13077	14615	16154	17692	19231								63375	1538.5
	14	736.82	1066.53	978.8	1.1	50.2	1050	714	2143	3571	5000	6429	7857	9286	10714	12143	13571	15000	16429	17857	19286							73500	1428.6
	15	860.87	1293.30	1123.8	1.1	52.0	1125	667	2000	3333	4667	6000	7333	8667	10000	11333	12667	14000	15333	16667	18000	19333						84375	1333.3
	16	1029.02	1621.50	1278.8	1.2	53.7	1200	625	1875	3125	4375	5625	6875	8125	9375	10625	11875	13125	14375	15625	16875	18125	19375					96000	1250.0
Full-wave CW	1	8.46	0.15	3.8	0.0	26.7	37.5	10000																				37.5	20000.0
	2	14.56	1.13	23.4	0.0	26.7	187.5	5000	10000																			75	10000.0
	3	21.33	4.27	52.5	0.0	26.7	525	3333	6667	6667																		112.5	6666.7
	4	37.71	11.64	91.4	0.0	26.7	1125	2500	5000	5000	5000																	150	5000.0
	5	57.00	24.36	140.3	0.0	26.7	2062.5	2000	4000	4000	4000	4000																187.5	4000.0
	6	70.05	44.55	199.1	0.0	26.7	3412.5	1667	3333	3333	3333	3333	3333															225	3333.3
	7	71.89	80.05	267.9	0.0	26.7	5250	1429	2857	2857	2857	2857	2857	2857														262.5	2857.1
	8	117.79	128.73	346.6	0.0	26.7	7650	1250	2500	2500	2500	2500	2500	2500	2500													300	2500.0
	9	138.84	217.47	435.4	0.0	26.7	10687.5	1111	2222	2222	2222	2222	2222	2222	2222	2222												337.5	2222.2
	10	201.08	303.01	534.2	0.0	26.7	14437.5	1000	2000	2000	2000	2000	2000	2000	2000	2000	2000											375	2000.0
	11	176.15	445.50	643.0	0.0	26.7	18975	909	1818	1818	1818	1818	1818	1818	1818	1818	1818	1818										412.5	1818.2
	12	240.81	606.00	761.7	0.0	26.7	24375	833	1667	1667	1667	1667	1667	1667	1667	1667	1667	1667	1667									450	1666.7
	13	335.02	808.10	890.5	0.0	26.7	30712.5	769	1538	1538	1538	1538	1538	1538	1538	1538	1538	1538	1538	1538								487.5	1538.5
	14	263.88	1130.27	1029.2	0.0	26.7	38062.5	714	1429	1429	1429	1429	1429	1429	1429	1429	1429	1429	1429	1429	1429							525	1428.6
	15	330.56	1411.67	1178.0	0.0	26.7	46500	667	1333	1333	1333	1333	1333	1333	1333	1333	1333	1333	1333	1333	1333	1333						562.5	1333.3
	16	427.82	1824.53	1336.8	0.0	26.7	56100	625	1250	1250	1250	1250	1250	1250	1250	1250	1250	1250	1250	1250	1250	1250	1250					600	1250.0
	17	963.48	2385.96	1505.5	0.0	26.7	66937.5	588	1176	1176	1176	1176	1176	1176	1176	1176	1176	1176	1176	1176	1176	1176	1176	1176				637.5	1176.5
	18	1168.16	2892.24	1684.3	0.0	26.7	79087.5	556	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111			675	1111.1
	19	1467.73	3625.58	1873.0	0.0	26.7	92825	526	1053	1053	1053	1053	1053	1053	1053	1053	1053	1053	1053	1053	1053	1053	1053	1053	1053	1053		712.5	1052.6
	20	65535.00	0.00	2071.8	0.0	26.7	107625	500	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	750	1000.0
Full-wave Dickson	1	8.46	0.15	3.8	0.0	26.7	37.5	10000																				37.5	20000.0
	2	15.56	0.61	18.8	0.0	26.7	75	5000	15000																			75	10000.0
	3	21.75	1.33	43.8	0.0	26.7	112.5	3333	10000	16667																		112.5	6666.7
	4	30.08	2.17	78.8	0.0	26.7	150	2500	7500	12500	17500																	150	5000.0
	5	49.41	3.33	123.8	0.0	26.7	187.5	2000	6000	10000	14000	18000																187.5	4000.0
	6	59.07	4.52	178.8	0.0	26.7	225	1667	5000	8333	11667	15000	18333															225	3333.3
	7	89.42	6.55	243.8	0.0	26.7	262.5	1429	4286	7143	10000	12857	15714	18571														262.5	2857.1
	8	98.20	8.13	318.8	0.0	26.7	300	1250	3750	6250	8750	11250	13750	16250	18750													300	2500.0
	9	124.02	10.54	403.8	0.0	26.7	337.5	1111	3333	5556	7778	10000	12222	14444	16667	18889												337.5	2222.2
	10	171.31	13.45	498.8	0.0	26.7	375	1000	3000	5000	7000	9000	11000	13000	15000	17000	19000											375	2000.0
	11	181.20	16.07	603.8	0.0	26.7	412.5	909	2727	4545	6364	8182	10000	11818	13636	15455	17273	19091										412.5	1818.2
	12	199.64	17.63	718.8	0.0	26.7	450	833	2500	4167	5833	7500	9167	10833	12500	14167	15833	17500	19167									450	1666.7
	13	233.66	21.35	843.8	0.0	26.7	487.5	769	2308	3846	5385	6923	8462	10000	11538	13077	14615	16154	17692	19231								487.5	1538.5
	14	325.98	28.15	978.8	0.0	26.7	525	714	2143	3571	5000	6429	7857	9286	10714	12143	13571	15000	16429	17857	19286							525	1428.6
	15	359.14	30.62	1123.8	0.0	26.7	562.5	667	2000	3333	4667	6000	7333	8667	10000	11333	12667	14000	15333	16667	18000	19333						562.5	1333.3
	16	379.45	33.40	1278.8	0.0	26.7	600	625	1875	3125	4375	5625	6875	8125	9375	10625	11875	13125	14375	15625	16875	18125	19375					600	1250.0
	17	408.43	34.82	1443.8	0.0	26.7	637.5	588	1765	2941	4118	5294	6471	7647	8824	10000	11176	12353	13529	14706	15882	17059	18235	19412				637.5	1176.5
	18	438.45	37.11	1618.8	0.0	26.7	675	556	1667	2778	3889	5000	6111	7222	8333	9444	10556	11667	12778	13889	15000	16111	17222	18333	19444			675	1111.1

Table D.6: Detailed simulation results of the weight study of voltage multipliers.

Analytical analysis of energy stored in capacitors

With our method of weight study, the energy stored in capacitors in the n-stage full-wave Dickson (FWDS) voltage multiplier and the n-stage full-wave Cockroft-Walton (FWCW) voltage multiplier are very similar (likewise the n-stage half-wave Dickson voltage multiplier has comparable energy storage with the n-stage half-wave Cockroft-walton voltage multiplier). We show an analytical proof of FWCW and FWDS here. The "voltage droop" is set by flying capacitors C_{odd} in both topologies. For a fixed V_o, f and I_o and to achieve a fixed "voltage droop" V_{droop},

A n-stage full-wave Dickson,

$$\begin{aligned} C_{odd} &= \frac{nI_o}{2V_{droop}f} \\ E_{odd} &= \frac{C_{odd}}{2}\sum_{1}^{n}\frac{(i-0.5)^2V_o^2}{n^2} \\ &= \frac{nI_o}{4V_{droop}f}\frac{V_o^2}{n^2}\frac{4n^2+3n-4}{12} = \frac{4n^2+3n-4}{n}\frac{I_oV_o^2}{48V_{droop}f} \end{aligned}$$

A n-stage full-wave CW,

$$\begin{aligned} C_{odd} &= \frac{n(n+1)(2n+1)I_o}{12V_{droop}f} \\ E_{odd} &= \frac{C_{odd}}{2}((n-1)(\frac{V_o}{n})^2+(\frac{V_o}{2n})^2) \\ &= \frac{n(n+1)(2n+1)I_o}{24V_{droop}f}\frac{V_o^2}{n^2}\frac{4n-3}{4} = \frac{(n+1)(2n+1)(4n-3)}{2n}\frac{I_oV_o^2}{48V_{droop}f} \end{aligned}$$

As n increases, they fall on a very similar line as shown in Fig. D-4.

Other methods

In the paper published on this work [74], the voltage droop was calculated with a different equation, which is less accurate compared with the derivations in Table. 2.1 and therefore has been updated:

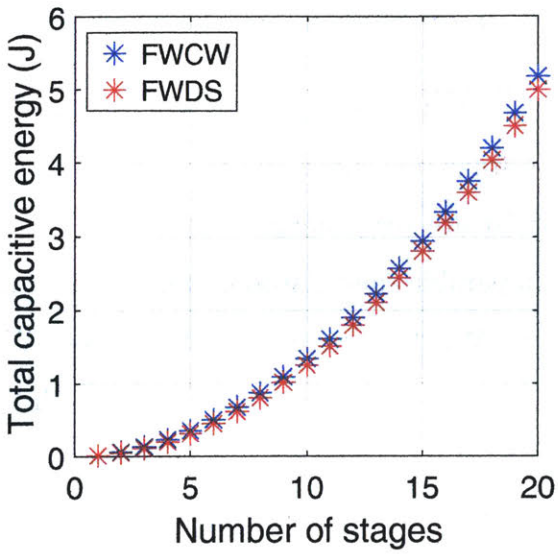


Figure D-4: Analytical analysis to prove the energy stored in both FWCW and FWDS are very similar with our method of weight study.

$$V_{droop} = \sum (i = 1, 2, 3,) \frac{Q_{C_i}}{C_i}$$

Where Q_{C_i} is the charge flowing through capacitor C_i.

D.2 Weight study of the isolation stage

D.2.1 10 kV 1 kW Transformer

For this rule-of-thumb design, we largely follow the transformer design method in [134] Chapter 7 (not Appendix B as in the rest of the thesis).

Step 1: select core size according to the area-product

The relationship between the area-product A_p of a transformer core and its power handling capability is

$$A_p \geqslant \frac{(P_{in} + P_o) \times 10^4}{k_u k_f B_m J f} [cm^4]$$

Where

- P_o is the output power in W, set to 1000 W

- P_{in} is the input power in W, set to 1000/0.95 W $\sim$ 1053 W
- f is the switching frequency in Hz, set to 500 000 Hz
- k_f is the waveform coefficient, for sine wave, set to 4.44

We start with an educated guess of B_{ac} and J to guide us to select a core:

- B_m is the maximum flux density in Tesla. It is set to 0.03 T (10% of the saturation limit of most ferrite cores) because for high frequency operation, the flux density is usually much lower than the core's saturation limit.
- J is the current density in the windings, set to 500 A/cm^2 as a rule of thumb.
- k_u is the packing factor, set to 0.1. For high voltage transformers, the packing factors are usually low due to added insulation materials.

These assumptions give us

$$A_p \geqslant \frac{2000 \times 10^4}{0.1 \times 4.44 \times 0.03 \times 500 \times 500000}[cm^4] \sim 6[cm^4]$$

We choose the ETD49 core in the Table.3-24 in [134] which has an area-product A_p of 7.25 cm^4. Some other dimensions are: cross-sectional area A_c = 2.11 cm^2, effective flux length L_e =11.4 cm, window area W_a = 3.434 cm^2, window height H = 3.54 mm (see the dimension definitions in Fig. B-2a), mean length per turn MLT = 10.3 cm.

Step 2: select wire and turns from the electrical requirements

Electrical requirements are

- Primary voltage amplitude (peak to zero) V_p = 500 V, thus primary current I_p = 4.2 A.
- Secondary voltage amplitude V_s = 10 kV, thus secondary current I_s = 0.2 A.

Pick wire and winding patterns as

- Primary number of turns N_p = 20, primary wire AWG 17 (litz bundle equivalent conductor area A_{wp} = 0.82 mm^2, yielding to a current density of 512 A/cm^2)

- Secondary number of turns $N_s = N_p \frac{V_s}{V_p} = 400$, secondary wire AWG 31 (litz bundle equivalent conductor area $A_{ws} = 0.04\,\text{mm}^2$, yielding to a current density of $500\,\text{A/cm}^2$)

Then we calculate the flux density and the packing factor as

- Maximum flux density

$$B_m = \frac{V_p}{k_f N_p A_c f} = \frac{500}{4.44 \times 20 \times 2.11 \times 10^{-4}} T = 0.054T$$

- Packing factor

$$k_u = \frac{N_p A_{wp} + N_s A_{ws}}{W_a} = \frac{20 \times 0.82 + 400 \times 0.04}{3.43 \times 10^2} = 0.094$$

These values are around our assumptions so we proceed.

Step 3: calculate losses and temperature rise

- Core loss: we use the loss data of TDK N49 material [135]. Core loss density at 500 kHz 50 mT is $80\,\text{mW/cm}^3$ [135], thus the core loss is

$$P_{core} = A_c L_e \times 80[\text{mW}] = 1.92[\text{W}]$$

- Copper loss: we use Fig.13.34 in the book [136] to get F_r, the ratio of ac resistance to dc resistance of the winding. We assume both the primary and the secondary windings are wound on the center leg in the height direction of the core[1], and can calculate the number of turns per layer and the number of layers M. We also assume the litz size is smaller than the skin depth at 500 kHz. The total copper loss is $P_{copper} = 1.5\,\text{W}$ (see the calculation details in Table D.7).

- Temperature rise: use the temperature calculation in [111]. The thermal resis-

[1]We assume 80% of the height can be wounded by windings, the other 20% is reserved for insulation.

Type	Wire area A_w (mm^2)	Wire diameter (mm)	Maximum turns per layer	Layer count M	F_r	R_{dc}	Copper loss (W)
Primary	0.82	1.022	$\frac{35.4\times0.8}{1.022} \sim 27$	1	~1.2	$\frac{\rho N_p MLT}{A_{wp}} = 0.043\,\Omega$	0.41
Secondary	0.04	0.23	$\frac{35.4\times0.8}{0.23} \sim 123$	4	~3	$\frac{\rho N_s MLT}{A_{ws}} = 17.5\,\Omega$	1.05

Table D.7: Wire and winding pattern design of the 10 kV transformer.

tance of a EE transformer is

$$R_{th} = 35.1 \times 10^{-3} \times V_{core}^{-0.54}$$

Where V_{core} is the volume of the core in m^3 and R_{th} is in °C/W. For ETD49, we have

$$R_{th} = 35.1 \times 10^{-3} \times (24 \times 10^{-6})^(- 0.54) = 10.96\,°\text{C/W}$$
$$T_{rise} = R_{th}(P_{core} + P_{copper}) = 3.5 \times 10.96 \sim 39\,°\text{C}$$

Both losses and temperature rise are reasonable and within our expectations. The designed transformer has a magnetizing impedance Z_c of

$$Z_c = \frac{2\pi f N_p^2}{R_c} = \frac{2\pi \mu_0 \mu_r A_c N_p^2 f}{L_e} = 5850\,\Omega$$

Step 4: calculate the weight including insulations

The overall weight of the transformer consists of the following three parts:

- Core weight: core density is 5 g/cm^3, thus

$$W_{core} = 5 \times 24\text{g} \sim 120\,\text{g}$$

- Copper weight: copper density is 8.96 g/cm^3, thus the conductor weighs

$$W_{copper} = 8.96 \times MLT \times (A_{wp}N_p + A_{ws}N_s) \sim 36\,\text{g}$$

- Insulation weight: we assume there is an insulation "sleeve" rated for 10 kV wrapped around the core and a sleeve rated for 5 kV[2] around the secondary wire conductor. The length of the winding sleeve and the core sleeve are

$$SleeveL_{wire} \sim MLT \times N_s \sim 4120\,\text{cm}$$

$$SleeveL_{core} \sim L_e = 11.4\,\text{cm}$$

Different insulation materials yield to different thickness of the sleeves T, thus different cross-sectional area of the sleeve. For a given T, we calculate the cross-sectional areas of wire and core sleeve as

$$SleeveA_{wire} \sim \frac{\pi}{4}((D_s + 2T_w)^2 - D_s^2) = \frac{\pi(2T^2 + 0.023T)}{2}\text{cm}^2$$

$$SleeveA_{core} \sim \frac{\pi}{4}((D_c + 2T_c)^2 - D_c^2) = \frac{\pi(2T^2 + 1.64T)}{2}\text{cm}^2$$

Where $D_s = 0.023\,\text{cm}$ is the secondary wire diameter, and $D_c = 1.64\,\text{cm}$ is the core diameter, T_w and T_c are the insulation sleeve thickness of the wire and the core respectively. We considered 8 insulation materials, and for each, we calculated the insulation thickness T with a 60% derating of the dielectric strength. The resulting weight of each material is listed below:

Among 8 materials, Nylon 6/6 (glass filled), Delrin and PTFE (glass filled) are promising options. We prefer PTFE (glass filled) for 3 additional practical considerations: 1) it has lower dielectric constant. In high voltage transformers, a large number of secondary turns results in high parasitic capacitance, which is often undesirable for the circuit operation. 2) has high melting temperature. A weight-optimized high voltage transformer tends to be small, compact and operate at high temperature. 3) most high voltage wires uses PTFE as the wire jacket. In summary, the overall weight of the designed transformer is ~250–320 g (lower bound is Nylon 6/6 (glass)

[2]Because the secondary wire has 4 layers, here we assume the wire sleeve only needs to be rated for half the voltage. This is subjected to change depending on different winding patterns.

Material	Dielectric strength (kV/cm)	Density g/cm^3	Insulation thickness T_w (cm)	Insulation thickness T_c (cm)	Wire sleeve weight (g)	Core sleeve weight (g)	Dielectric constant	Melting point (°C)
DAP Cosmic D72 [137]	149.6	1.82	0.08	0.17	187.1	10.8	4	260
DAP (Glass filled) [138]	177.2	1.87	0.07	0.14	140.1	9.1	4.2	204
Epoxy E4920 [139]	138	1.85	0.09	0.18	221.4	12.0	4.3	260
Nylon 6/6 [138]	152	1.13	0.08	0.16	113.3	6.6	4	232
Nylon 6/6(glass filled) [138]	208	1.38	0.06	0.12	76.4	5.6	4.5	260
PTFE (unfilled) [133]	112	2.16	0.11	0.22	382.8	18.0	2.1	260
PTFE (glass filled) [133]	200	2.25	0.06	0.13	134.7	9.5	2.4	260
Delrin [140]	197	1.38	0.06	0.13	85.0	5.9	2.7	150

and upper bound is PTFE (glass))[3].

D.2.2 Air-core resonant transformer

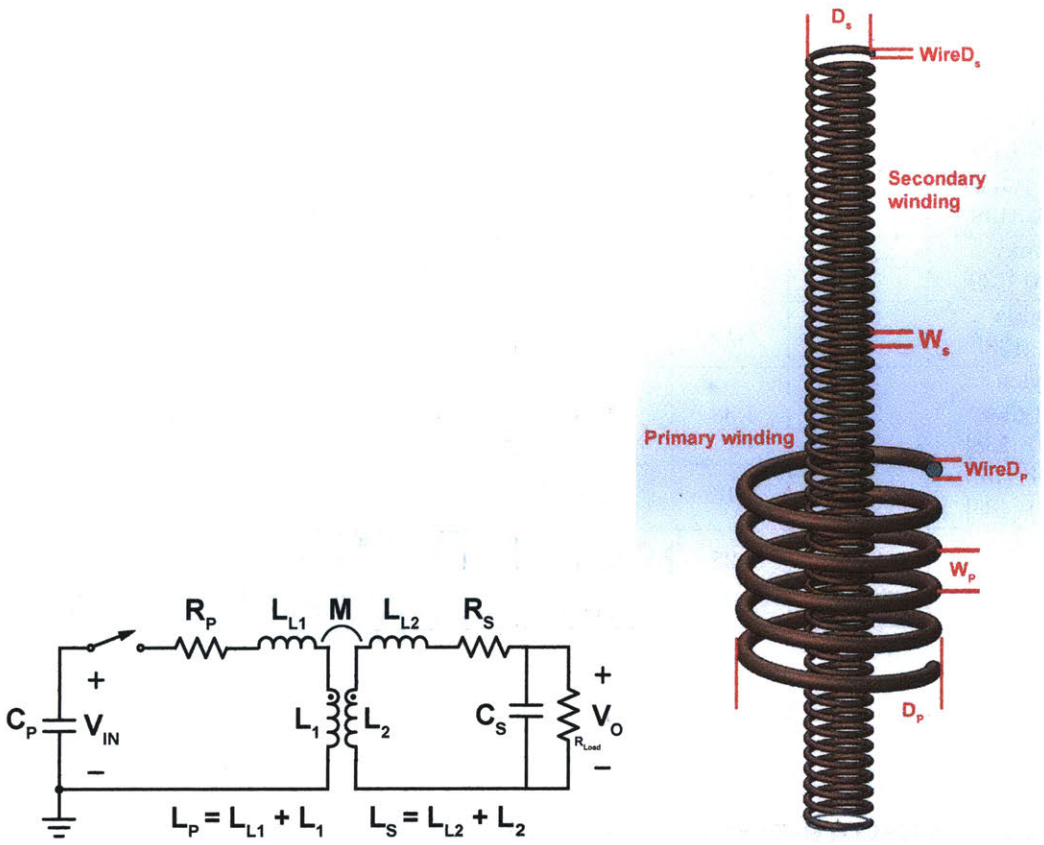
The air-core resonant transformer (i.e., Tesla coil) is designed following [79, 80]. We consider a simple Tesla coil set (two vertical concentric solenoids of which the inner one is the secondary and the outer one is the primary, see Fig. D-5b). We choose the simplest circuit model containing one LC pair each at the primary and the secondary (see Fig. D-5a)[4]. The operating point is at $V_{IN} = 500\,\text{V}$, $V_o = 10\,\text{kV}$, $P_o = 1000\,\text{W}$, resonating at f =500 kHz.

Four features of the Tesla coil are summarized from [79, 80]:

- The primary and the secondary windings can be designed as two separate inductors L_p and L_s. Intuitively, each of L_p and L_s contains two parts, of which L_{L1} (and L_{L2}) represents the flux that does not couple with the other winding and L_1 (and L_2) represents the flux that couples to the other winding. R_p and R_s are the winding resistance respectively. The placement of the two coils yields

[3] Added 20 g on each bound to account for margin.

[4] In practice, the secondary operates as a transmission line and there are various distributed or lumped circuit model for it.



(a) Schematic (b) CAD model and annotations

Figure D-5: A simplified circuit diagram and an CAD model of a Tesla coil

to different mutual inductance M and coupling coefficient $K = \frac{M}{\sqrt{L_p L_s}}$.

- The capacitor C_s consists of the secondary winding's self capacitance and additional external capacitors if needed; the capacitor C_p is usually external.

- Here we assume the resonant frequency of two sides are matched, that is, $2\pi f \sim \omega_p = \frac{1}{\sqrt{L_p C_p}} \sim \omega_s = \frac{1}{\sqrt{L_s C_s}}$.

- The secondary at resonance is said to act as a quarter-wavelength ($\lambda/4$ where λ is the wavelength at the frequency f) antenna, thus the total length of the secondary winding TL_s is an odd-integer multiple to this quarter wavelength [80].

For a given set of L_p, L_s, C_p, C_s, and ignoring R_p and R_s, [79] gives

$$Gain(t) = \frac{v_o(t)}{V_{IN}} = \frac{1}{2}\sqrt{\frac{L_s}{L_p}} \exp^{-\frac{t}{T}}(\cos(\frac{2\pi ft}{1-K}) - \cos(\frac{2\pi ft}{1+K})) \tag{D.1}$$

Where $T = \frac{4L_pL_s}{R_{L2}L_p+R_{L1}L_s}(1-K^2)$ is a damping constant.

We first layout the design equations for each winding in Step 1 and Step 2, then use them together with eq (D.1) to tune the physical dimension of each coil to achieve $V_o = 10\,\text{kV}$.

Step 1: The secondary coil

The total length of the secondary winding is

$$TL_s = \frac{(2i-1)\lambda}{4} = \frac{(2i-1)c}{4f} = \frac{(2i-1)3\times 10^8}{4\times 500000}[m] = 150(2i-1)[m], i = 1,2,3,...$$

Where λ is the wavelength of the frequency f and $c = 3\times 10^8$m/s is the speed of light. We choose $i = 1$ since this it's the shortest and lightest. We also have

$$TL_s = \pi D_s N_s$$

Where N_s is the number of secondary turns, D_s is the diameter of the secondary solenoid. We also define W_s as the distance between two turns, $H_s = W_sN_s$ as the height of the secondary solenoid and $WireD_s$ as the secondary wire diameter. All in meter.

The inductance of a solenoid is

$$L_s = \frac{\mu_0 N_s^2}{H_s}(\frac{\pi D_s^2}{4}) = \frac{\mu_0 \pi N_s D_s^2}{4W_s}[H]$$

The self-capacitance is [141]

$$C_s = \frac{2\pi D_s}{cosh^{-1}(\frac{W_s}{WireD_s})} \times 10^{-7}[F]$$

The secondary winding resistance is

$$R_s = \frac{1.3 \times 4\rho(TL_s)}{\pi(WireD_s)^2} = \frac{4.17 \times 10^{-6}}{(WireD_s)^2}[\Omega]$$

Where 1.3 is a rough estimate of the ac-to-dc resistance ratio.

Step 2: The primary coil and mutual inductance

The primary is also a solenoid therefore we follow the same equation above:

$$L_p = \frac{\mu_0 N_p^2}{H_p}(\frac{\pi D_p^2}{4}) = \frac{\mu_0 \pi N_p D_p^2}{4W_p}[H]$$

Where N_p is the number of primary turns, D_p is the diameter of the primary solenoid. We also define W_p as the distance between two turns, $H_p = W_p N_p$ as the height of the primary solenoid and $WireD_p$ as the primary wire diameter. All in meter.

The primary winding resistance is

$$R_p = \frac{1.3 \times 4\rho(TL_p)}{\pi(WireD_p)^2} = \frac{2.78 \times 10^{-8}(TL_p)}{(WireD_p)^2}[\Omega]$$

Where 1.3 is a rough estimate of the ac-to-dc resistance ratio. The mutual inductance of two coaxial concentric solenoids with $D_p > D_s$ is calculated with equation 86 on Page 71 in [142]:

$$M = 0.0501\frac{a^2 N_s N_p}{g}(1 + \frac{A^2 a^2}{8g^4}(3 - 4\frac{l^2}{a^2}))[\mu H]$$

Where $x = H_s/2, l = H_p/2, a = D_s/2, A = D_p/2, g = \sqrt{A^2 + x^2}$. All in inches. And the coupling coefficient is calculated as

$$K = \frac{M}{\sqrt{L_s L_p}}$$

Step 3: Design iterations

We use MATLAB and LTspice iteratively in this process, as shown in Fig. D-6.

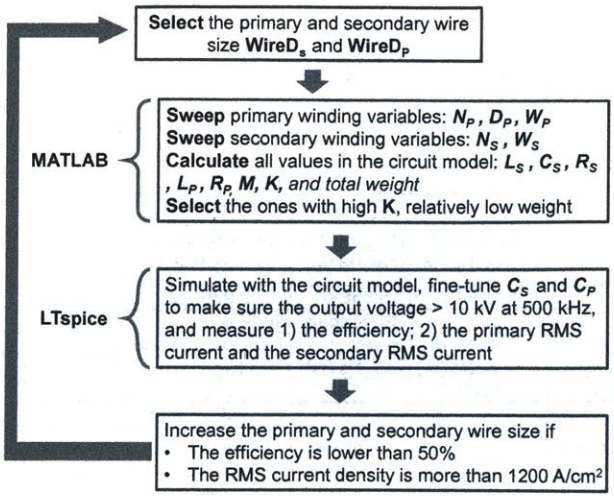


Figure D-6: Iterative design procedures of the Tesla coil

First, in MATLAB, we sweep N_p, D_p, W_p, N_s, W_s[5] and keep designs that satisfy three criterion:

- The adjusted voltage gain[6] is $\sim 20(10kV/500V)$, i.e., $\frac{max(V_o)}{V_{IN} \times K} \in [20, 20 \times 1.02]$.
- The primary winding is outside of the secondary winding, i.e., $D_p > D_s$.
- The coupling coefficient $0.6 < K < 0.85$ as suggested in [79].

There results many similar designs with slightly different geometries but similar weights. We pick the lightest one and simulate in LTspice to ensure 1) the output voltage reaches $V_o = 10\,\text{kV}$; 2) the wire RMS current is less than the chassis current rating in [143][7]. If they are not met, then we either simulate the next lightest design or increase the wire size and repeat the MATLAB design.

The total weight consists of that of the secondary conductor, the secondary wire insulation, the primary conductor and the supportive structure to wind the secondary on [79]. We assume PTFE as the wire insulation and a 0.1 mm thick Nylon 6/6 tube

[5]To start with, we borrow the core-based transformer design and pick AWG30 wire for the secondary ($WireD_s = 0.00254m$) and AWG18 wire for the primary ($WireD_p = 0.00102m$).

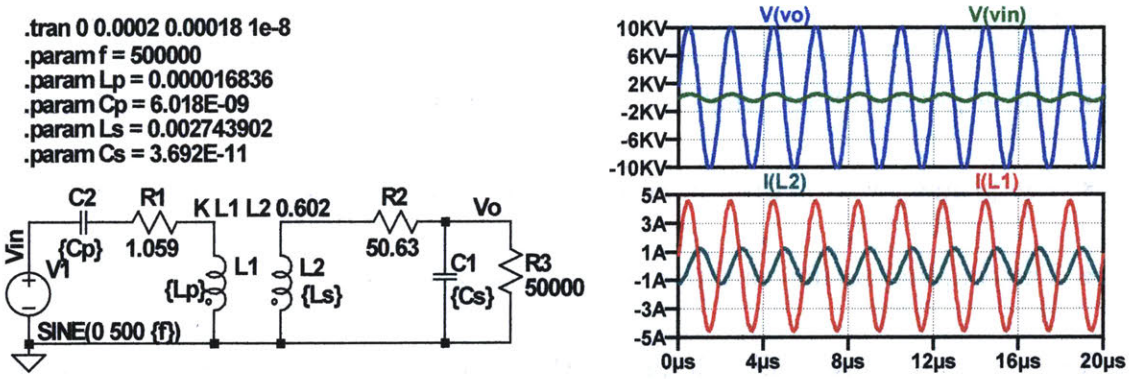
[6]The adjustment was because the mismatch between the gain eq (D.1) calculates and the LTspice simulation. K is the coupling coefficient.

[7]This current yields to a current density much higher than $500\,\text{A/cm}^2$. It is reasonable for air-core transformers because the windings are spread in a large area, resulting in much better thermal paths.

with the height H_s and diameter of D_s as the supportive structure. The final design is listed in Table D.8 and the LTspice simulation is in Fig. D-7. The output power is 1.06 kW and the input power is 1.17 kW, yielding an efficiency of ~90 %.

Primary winding								
Number of turns **Np**	Distance between turns **Wp** (m)	Diameter of the coil **Dp** (m)	Height of the coil **Hp** (m)	Total length of the winding **TLp** (m)	Wire AWG	**Rp** (ohm)	**Lp** (H)	**Cp** (F)
39	1.50E-02	8.10E-02	5.85E-01	9.92E+00	24	1.06	1.68E-05	6.02E-09
Secondary winding								
Number of turns **Ns**	Distance between turns **Ws** (m)	Diameter of the coil **Ds** (m)	Height of the coil **Hs** (m)	Total length of the winding **TLs** (m)	Wire AWG	**Rs** (ohm)	**Ls** (H)	**Cs** (F)
820	1.000E-03	5.82E-02	8.20E-01	1.50E+02	29	50.63	2.74E-03	3.69E-11
Mutual		**Weight (g)**						
Mutual inductance **M** (H)	Coupling coefficient **K**	Primary copper	Secondary copper	Secondary insulation	Total of windings	Supportive structure	Overall	
1.29E-04	0.602	23	111	0.43	135	17	152	

Table D.8: Design details of the Tesla Coil



(a) Schematics

(b) Waveform

Figure D-7: LTspice simulation of the Tesla coil design.

D.3 Inverter and transformer optimization

D.3.1 Design equations of the series-parallel resonant inverter

We simplify the resonant tank to Fig. D-8.

Once we select a set of operation variables: the resonant tank quality factor Q, the natural frequency f_0, the series and parallel resonant capacitance ratio $A = C_p/C_s$, and the transformer voltage step up ratio K. The inductance and capacitances of the

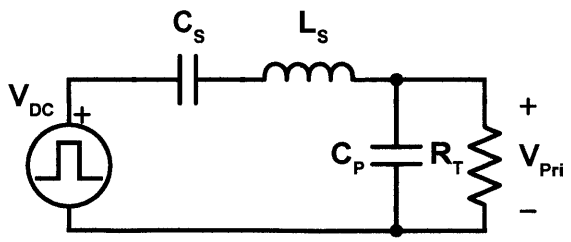


Figure D-8: The simplified resonant tank (The tank input is a bipolar square wave with the amplitude of V_{DC}. We assume the tank output voltage V_{Pri} is sinusoidal.

resonant tank can be calculated as:

$$L_s = \frac{R_T}{2\pi f_0 Q}, C_s = \frac{Q(A+1)}{A2\pi f_0 R_T}, C_p = \frac{Q(A+1)}{2\pi f_0 R_T}$$

Where R_T is the equivalent load resistance referred back to the resonant tank [86], considering we have a transformer with turns ratio K and a 6-stage voltage multiplier (V_o =40 kV and P_o =700 W).

$$R_T = \frac{R_{eq}}{K^2}, R_{eq} = \frac{8R_{Load}}{\pi^2 6^2} = \frac{8V_o^2}{\pi^2 6^2 P_o}$$

The tank voltage gain G_T is a function of the switching frequency f_s, as in [144]

$$G_T = \frac{V_T}{V_{DC}} = \frac{4}{\pi\sqrt{(1+A)^2(1-(\frac{f_s}{f_0})^2)^2 + \frac{1}{Q^2}(\frac{f_s}{f_0} - \frac{Af_0}{(A+1)f_s})^2}}$$

The maximum inductor current is

$$I_{L_{max}} = \frac{V_T}{\left|\frac{1}{R_T} + j2\pi f_s C_P\right|} = \frac{V_T}{R_T}\sqrt{1 + (\frac{f_s}{f_0})^2 Q^2 (A+1)^2} \quad \text{(D.2)}$$

D.3.2 Transformer weight study

Please refer to Appendix B for the core design procedures. This section only explains the variations made for this chapter. In short, once we have a fixed operating point of the transformer ($V_{Pri}, V_{Sec}, P_{Sec}, f_s$), we follow four steps to simulate the lightest achievable weight of the transformer:

- Sweep a range of designs. Each design is defined by: core size, core material, wire build (litz wire size and number of strands per wire) and winding pattern (number of turns and number of layers of the winding).

- Calculate electrical, thermal and mechanical parameters of each design. The electrical parameters include maximum flux density, inductance of the inductor, magnetizing impedance of the transformer. The thermal parameters include core loss (modeled with standard Steinmetz equations), copper loss (modeled with Dowell's equation as in [111]) and absolute temperature (modeled as in [111]). The physical parameters include packing factor (considering insulations), winding width and height.

- Rule out designs with constraints: maximum flux density $\geqslant$ 75% of saturation density, maximum temperature $\geqslant$ 90 °C, total loss $\geqslant$ 2% for inductors and $\geqslant$ 5% for transformers, overall packing factor[8] $\geqslant$ 0.7, and the windings need to fit in the window height and width.

- For each design that satisfies all constraints, we calculate the weight (consists of four parts: core, wire copper, wire insulation, and core insulation) and select the lightest one.

Core and wire selections

Core: we sweep a pool of off-the-shelf core sizes as listed in Table B.1, and two core materials that are known to have low loss at 0.5–1 MHz (Ferroxcube 3F35 and TDK N49). We use the standard Steinmetz equations to model the core loss.

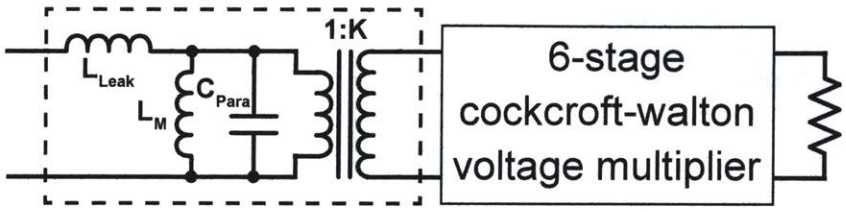
Wires: we fix the secondary wire as the Teledyne Reynolds AWG28 18 kV FEP insulated wire. When calculating the copper losses, we consider the litz wire size to be AWG 40 (diameter 0.050 24 mm) for both the primary and the secondary wire and we assume the peak current density of the wire to be 500 A/cm^2.

[8]Defined as the area of wire copper, wire insulation and core insulation divided by window area.

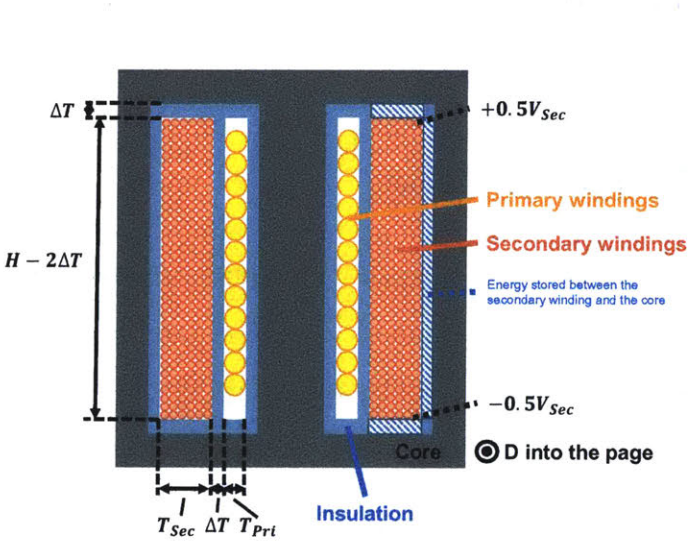
Impedances and parasitics

We model the transformer as in Fig. D-9a: an ideal 1:K transformer with a magnetizing inductance L_M, a leakage inductance L_{Leak}, and a shunt parasitic capacitance reflected to the primary C_{Para}.

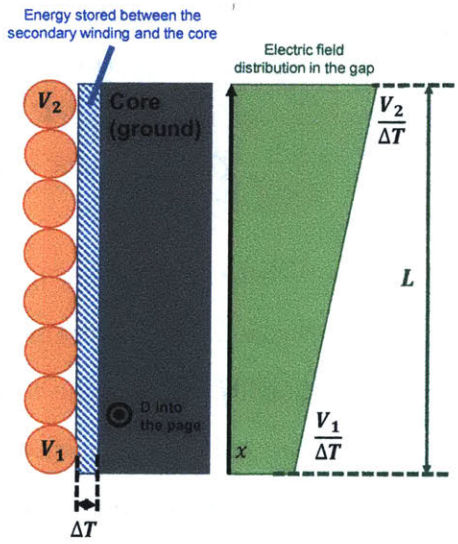
For all transformer designs, we make sure L_M is big enough to be neglected, and L_{Leak} and C_{Para} are used in the resonant tank operation: L_{Leak} is part of the resonant inductance L_S, C_{Para} is big enough so we use the full parasitic capacitance as the parallel resonant capacitance C_P without additional discrete capacitors. Each of these parasitics are calculated as:



(a) Transformer circuit model



(b) Dimensions used to calculate the parasitics.



(c) The electric field between an arbitrary section of winding and the core.

Figure D-9: Transformer circuit model and dimensions labels.

- Magnetizing inductance:

$$L_M = \frac{N_p^2}{R_M} = \frac{\mu_0 \mu_r A_c N_p^2}{L_e}$$

Where N_p is the primary number of turns, μ_r is the relative permeability, A_c is the core cross-sectional area, L_e is the effective flux path. It is controlled to be

$$X_{L_M} = 2\pi f_s L_M \geqslant 5X_{C_P} = \frac{5}{2\pi f_s C_P}$$

- Leakage inductance: calculated as in [134] equation 17-2:

$$L_{Leak} = \frac{\mu_0 N_p^2 MLT_{Sec}}{H - 2\Delta T}(\Delta T + \frac{T_{Pri} + T_{Sec}}{3})$$

Where N_p is the number of primary turns, MLT_{Sec} is the mean length per turn of the secondary winding. ΔT is the insulation thickness[9], T_{Sec} and T_{Pri} are the width of the secondary and primary winding respectively (See Fig. D-9b).

- Parasitic capacitance reflected to the primary is the sum of three parts (and doubled to account for margin):

  - the transformer secondary winding self capacitance $C_{Para_{self}}$, calculated following equation 8, 17, 18, and 19 in [88]:

$$C_{Para_{self}} = K^2 \frac{n_t(n_t+1)(2n_t+1)}{6n_t^2} \frac{4(n_L-1)}{n_L^2} \frac{1}{n_{section}} MLT_{Sec} C_{tt}$$

Where $n_{section}, n_L, n_t$ are the number of sections, the number of layers per section, and the number of turns per layer per section. K is the turns ratio and MLT_{Sec} is the mean length per turn of the secondary winding. C_{tt} is the unit length turn-to-turn capacitance following equation (8) with some adjustment on the first term in [88][10]:

$$C_{tt} = \epsilon_{eq}\epsilon_0 \theta^* ln^{-1}(\frac{d_e}{d_i}) + \epsilon_0 cot(\frac{\theta^*}{2}) - \epsilon_0 cot(\frac{\pi}{12})$$

  - the transformer secondary winding to core capacitance $C_{Para_{core}}$, estimated

[9] Assume PTFE as the insulation material with a dielectric strength of 200 kV/mm

[10] We use the 18kV FEP insulated Teledyne Reynolds wire, thus we assume in equation (8) $\epsilon_{eq} = 2.1$, $d_e = 1\,\text{mm}$ and $d_i = 0.4\,\text{mm}$. The first term was revised to $\epsilon_{eq}\epsilon_0$ (which was first published in [145]) instead of ϵ_{eq} (the author likely made a mistake.)

by calculating the energy stored between the winding and the core following equation (24) in [88] with some modifications:

* For an arbitrary section of winding starting at voltage potential V_1 and ending at V_2 (see Fig. D-9c), the energy stored in the gap is

$$E_{gap} = \frac{1}{2}\int \epsilon_r \epsilon_0 E(x)^2 dx$$
$$= \frac{1}{2}\epsilon_r \epsilon_0 \frac{DL}{\Delta T}(\frac{V_1^2 + V_1 V_2 + V_2^2}{3})$$

* For top and bottom, we assume the potential starts at $V_1 \sim 0$ and ends at $V_2 = +0.5V_{sec}$, thus

$$E_{top\&bottom} = 4 \times (\frac{1}{2}\frac{\varepsilon_0 \varepsilon_r D T_{sec}}{\Delta T}\frac{(0.5V_{Sec})^2}{3})$$

* For side with $n_{section}$ sections in the total window height ($0.5n_{section}$ sections in half the total window height), we have

$$E_{side} = 4 \times (\frac{1}{2}\frac{\varepsilon_0 \varepsilon_r D(0.5H - \Delta T)}{\Delta T}\frac{3n_{section}^2 - 2n_{section} - 4}{9n_{section}^2}(0.5V_{sec})^2)$$

* The total capacitance to core reflected to the primary is then

$$C_{Para_{core}} = \frac{2(E_{side} + E_{top\&bottom})}{V_{Pri}^2}$$

– the diode junction capacitances in the 6-stage full-wave cockcroft-walton voltage multiplier reflected to the transformer primary,

$$C_{Para_{diode}} = 6C_{Diode}K^2$$

Where C_{Diode} is the junction capacitance of each diode, assuming no paralleling diodes.

– The total parasitic capacitance reflected across the primary with a safety

margin of 2 is then

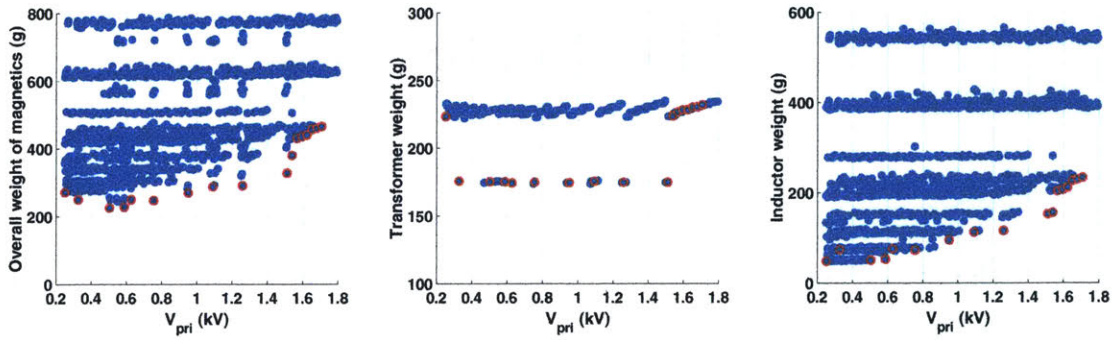
$$C_{Para} = 2(C_{Para_{self}} + C_{Para_{core}} + C_{Para_{diode}})$$

D.3.3 Inductor weight study

We follow a very similar method as for the transformer. Please refer to Appendix C for the detailed design procedures. The variations here are that 1) the inductance value is the resonant inductor value L_s. 2) the inductor peak current is $I_{L_{max}}$ as in eq (D.2). 3) the inductor core size is swept in the pool as listed in Table B.1. Two core materials (Ferroxcube 3F35 and TDK N49) are considered. 4) When calculating the copper losses, we consider the litz wire size to be AWG 44 (diameter 0.050 24 mm).

D.3.4 Detailed weight study results of two stages

All simulated weight results are plotted against V_{Pri} in Fig. D-10. We take the lowest bounds (the lightest weight) and plot in Fig. 2-7 (the details of these designs are listed in Table D.9, Table. D.10 and Table D.11).



(a) Combined (b) Transformer (c) Inductor

Figure D-10: All simulated weights of the inductor, the transformer and both plotted against the transformer input voltage V_{pri}. The points circled by red represent the designs yielding to lowest overall weights and are plotted in Fig. 2-7.

More explanation of the transformer results

When calculating the parasitic capacitance of each transformer design, we assume the diode capacitance C_{Diode} is 0.5 pF (see X150FF3 datasheet in [146]).

More explanation of the inductor results

The derivation of the simplified equation (2.2) is listed below. We use equations in Section D.3.1, and make several assumptions such as $f_s \sim f_0$, $A \ll 1$ and $G \sim Q$.

$$L_s = \frac{1}{2\pi f_0}\frac{R_T}{Q} = \frac{1}{2\pi f_0}\frac{R_{eq}}{QK^2} = \frac{R_{eq}}{2\pi f_0}\frac{V_{DC}^2 G^2}{QV_{sec}^2} \sim C_1\frac{G^2}{Q}$$

$$I_{L_{max}} = \frac{V_T}{R_T}\sqrt{1+(\frac{f_s}{f_0})^2Q^2(A+1)^2} \sim \frac{V_{DC}G}{\frac{R_{eq}}{K^2}}Q(A+1) \sim C_2\frac{Q}{G}$$

$$B_{L_{max}} \simeq \frac{L_s I_{L_{max}}}{A_c N_L} \sim \frac{C_1\frac{G^2}{Q}C_2\frac{Q}{G}}{A_c N_L} \sim C_3\frac{G}{A_c N_L}$$

The constants C_1, C_2, C_3 are only constants at a given V_{DC}, V_{Sec}, P_{Sec}. The simplified equation of $I_{L_{max}}$ suggests that it stays relatively unchanged as V_{Pri} increases, thus also the wire size. This trend is consistent with the results in Table. D.10.

Index	Vdc (V)	Vpri (V)	Vsec (V)	Po (W)	Q	Natural frequency f0 (kHz)	A (Cp/Cs)	Turns ratio K	Ls (uH)	Cs (nF)	Cp (nF)	Tank voltage gain	Switching frequency (kHz)	Overall weight of magnetics (g)
1	200	252.1	7563.0	750	0.9	500	0.1	30	20.22	55.11	5.51	1.26	500	271.15
2	200	327.9	7542.0	750	1	480	0.4	23	32.26	11.93	4.77	1.64	500	249.17
3	200	504.2	7563.0	750	1.8	500	0.1	15	40.45	27.55	2.76	2.52	500	225.26
4	200	588.2	7647.1	750	2.1	500	0.1	13	46.16	24.15	2.41	2.94	500	227.34
5	200	629.0	7547.8	750	1.9	500	0.3	12	59.87	7.33	2.20	3.14	500	249.68
6	200	756.3	7563.0	750	2.7	500	0.1	10	60.67	18.37	1.84	3.78	500	247.01
7	200	952.4	7619.1	750	3.4	500	0.1	8	75.28	14.80	1.48	4.76	500	269.10
8	200	1092.4	7647.1	750	3.9	500	0.1	7	85.72	13.00	1.30	5.46	500	287.48
9	200	1260.5	7563.0	750	4.5	500	0.1	6	101.12	11.02	1.10	6.30	500	290.44
10	200	1512.6	7563.0	750	5.4	500	0.1	5	121.35	9.18	0.92	7.56	500	327.34
11	200	1540.6	7703.1	750	5.5	500	0.1	5	119.14	9.35	0.94	7.70	500	379.40
12	200	1568.6	7843.2	750	5.6	500	0.1	5	117.01	9.52	0.95	7.84	500	429.98
13	200	1596.6	7983.2	750	5.7	500	0.1	5	114.96	9.70	0.97	7.98	500	434.28
14	200	1624.7	8123.3	750	5.8	500	0.1	5	112.98	9.87	0.99	8.12	500	439.76
15	200	1652.7	8263.3	750	5.9	500	0.1	5	111.06	10.04	1.00	8.26	500	456.13
16	200	1680.7	8403.4	750	6	500	0.1	5	109.21	10.21	1.02	8.40	500	459.76
17	200	1708.7	8543.4	750	6.1	500	0.1	5	107.42	10.38	1.04	8.54	500	465.00

Table D.9: Details of the weight study of the inverter stage and the transformer stage (Part 1 of 3, overall weight). The selected design (index 3) is highlighted in red.

Index	Inductance (uH)	Core				Wire and winding							Overall packing factor	Loss (W)			Max temperature (°C)	Weight (g)				
		Material	Shape	Air gap (mm)	Bmax (mT)	Turns	Conductor diameter (mm)	Overall diameter (mm)	Current density (A/cm2)	Number of Litz strands	Number of layers	Turns per layer		Core	Copper	Total		Core	Copper	Wire insulation	Core insulation	Total
1	20.22	N49	RM12	1.76	60.76	14	1.41	1.45	499.91	626	7	2	0.21	1.49	1.18	2.67	87.26	38.26	9.50	0.13	0.13	47.89
2	32.26	N49	RM14	2.33	56.81	18	1.38	1.42	499.42	602	9	2	0.18	1.93	1.60	3.53	89.65	60.00	13.34	0.19	0.24	73.58
3	40.45	N49	RM12	2.18	60.65	22	1.26	1.29	499.30	494	11	2	0.26	1.50	1.18	2.69	87.63	38.26	11.58	0.19	0.29	50.10
4	46.16	N49	RM12	2.68	58.52	26	1.24	1.28	499.54	491	13	2	0.31	1.34	1.39	2.72	88.49	38.26	13.61	0.22	0.30	5
5	59.87	N49	RM14	2.62	57.45	26	1.22	1.26	499.09	474	13	2	0.21	1.99	1.48	3.47	88.70	60.00	14.96	0.24	0.46	75.42
6	60.67	N49	EC41	4.57	53.70	43	1.21	1.25	499.60	465	21	2	0.25	1.42	1.94	3.35	89.55	51.84	19.88	0.33	0.54	72.26
7	75.28	N49	ER40/22/13	5.20	50.36	46	1.21	1.25	499.55	463	23	2	0.22	1.59	2.31	3.90	89.66	70.08	23.75	0.39	0.85	94.69
8	85.72	N49	EC52	4.15	54.55	40	1.21	1.25	499.18	463	20	2	0.16	2.58	2.02	4.60	89.80	90.24	20.82	0.34	1.06	112.12
9	101.12	N49	EC52	5.08	52.11	48	1.19	1.23	499.15	450	24	2	0.18	2.26	2.30	4.56	89.33	90.24	24.28	0.41	1.22	115.74
10	121.35	N49	ER48/21/21	5.05	47.87	44	1.19	1.23	499.48	447	22	2	0.18	2.40	2.69	5.09	88.84	122.40	28.48	0.48	1.87	152.74
11	119.14	N49	ER48/21/21	5.87	45.62	47	1.21	1.25	499.99	463	23	2	0.20	2.09	3.07	5.17	89.76	122.40	31.58	0.52	1.90	155.88
12	117.01	N49	ETD54/28/19	5.22	47.32	42	1.23	1.27	499.75	480	21	2	0.12	3.24	3.06	6.30	88.92	170.40	30.59	0.50	2.64	203.64
13	114.96	N49	ETD54/28/19	5.84	45.95	44	1.25	1.29	499.82	497	22	2	0.13	2.97	3.42	6.40	89.95	170.40	33.26	0.53	2.69	206.35
14	112.98	N49	ETD54/28/19	7.39	41.97	49	1.27	1.31	499.21	515	24	2	0.15	2.20	4.06	6.36	89.54	170.40	38.47	0.60	2.74	211.61
15	111.06	N49	EC70	5.74	48.80	43	1.30	1.34	499.87	532	21	2	0.09	3.99	3.37	7.36	89.94	192.48	30.96	0.48	2.80	226.24
16	109.21	N49	EC70	6.70	46.38	46	1.32	1.36	499.84	550	23	2	0.10	3.45	3.83	7.28	89.27	192.48	34.33	0.52	2.85	229.65
17	107.42	N49	EC70	7.74	44.25	49	1.34	1.38	499.21	569	24	2	0.11	3.01	4.34	7.36	89.94	192.48	37.93	0.56	2.90	233.30

Table D.10: Details of the weight study of the inverter stage and the transformer stage (Part 2 of 3, inductor). The selected design (index 3) is highlighted in red.

Index	Core			Turns		Primary wire and winding						Secondary wire			
	Material	Shape	Bmax (mT)	Primary	Secondary	Conductor diameter (mm)	Overall diameter (mm)	Current density (A/cm2)	Number of Litz strands	Number of layers	Turns per layer	Conductor diameter (mm)	Overall diameter (mm)	Current density (A/cm2)	Number of Litz strands
1	TDK N49	ETD54/28/19	57.32	5	151	1.41	1.46	498.53	258	1	5	0.38	1.016	214.37	19
2	TDK N49	ER48/21/21	58.48	7	162	1.24	1.30	499.41	198	1	7	0.38	1.016	214.97	19
3	TDK N49	ETD49/25/16	58.51	13	196	1.00	1.10	498.53	129	1	13	0.38	1.016	214.37	19
4	TDK N49	ETD49/25/16	59.16	15	196	0.93	1.05	496.61	111	1	15	0.38	1.016	212.01	19
5	TDK N49	ETD49/25/16	59.30	16	193	0.90	1.02	495.70	104	1	16	0.38	1.016	214.80	19
6	TDK N49	ER48/21/21	59.00	16	161	0.82	0.97	498.53	86	1	16	0.38	1.016	214.37	19
7	TDK N49	ETD49/25/16	59.86	24	193	0.73	0.92	493.43	69	1	24	0.38	1.016	212.79	19
8	TDK N49	ER48/21/21	59.29	23	162	0.68	0.90	494.70	60	1	23	0.38	1.016	212.01	19
9	TDK N49	ETD49/25/16	59.42	32	193	0.63	0.89	494.70	52	1	32	0.38	1.016	214.37	19
10	TDK N49	ETD49/25/16	60.05	38	191	0.58	0.88	498.53	43	1	38	0.38	1.016	214.37	19
11	TDK N49	ETD54/28/19	58.38	30	151	0.58	0.89	489.47	43	1	30	0.38	1.016	210.47	19
12	TDK N49	ETD54/28/19	57.52	31	156	0.57	0.88	492.17	42	1	31	0.38	1.016	206.71	19
13	TDK N49	ETD54/28/19	56.72	32	161	0.56	0.88	495.33	41	1	32	0.38	1.016	203.09	19
14	TDK N49	ETD54/28/19	57.72	32	161	0.56	0.88	498.96	40	1	32	0.38	1.016	199.58	19
15	TDK N49	ETD54/28/19	56.93	33	166	0.56	0.89	490.50	40	1	33	0.38	1.016	196.20	19
16	TDK N49	ETD54/28/19	57.90	33	166	0.55	0.89	494.70	39	1	33	0.38	1.016	192.93	19
17	TDK N49	ETD54/28/19	57.13	34	171	0.54	0.88	499.39	38	1	34	0.38	1.016	189.77	19

(a) Core and primary

Index	Overall Packing Factor	Loss (W)			Max temperature (°C)	Weight (g)						
		Core	Copper	Total		Core	Primary copper	Primary insulation	Secondary copper	Secondary insulation	Core insulation	Total
1	0.15	5.61	0.66	6.27	88.64	170.4	4.84	0.09	14.22	20.98	12.75	223.27
2	0.26	4.27	0.90	5.16	89.73	122.4	4.94	0.13	15.67	23.13	9.31	175.59
3	0.27	4.02	0.92	4.94	87.79	115.2	5.55	0.29	17.88	26.39	9.86	175.16
4	0.27	4.15	0.87	5.03	88.87	115.2	5.50	0.36	17.83	26.31	9.96	175.17
5	0.27	4.18	0.87	5.05	89.16	115.2	5.48	0.40	17.51	25.83	9.84	174.26
6	0.26	4.38	0.74	5.11	89.10	122.4	4.83	0.48	15.23	22.47	9.34	174.75
7	0.27	4.30	0.80	5.10	89.77	115.2	5.43	0.79	17.40	25.67	9.93	174.41
8	0.27	4.44	0.69	5.13	89.32	122.4	4.83	0.88	15.27	22.53	9.44	175.36
9	0.29	4.21	0.79	4.99	88.45	115.2	5.45	1.27	17.34	25.59	9.86	174.70
10	0.29	4.33	0.77	5.10	89.84	115.2	5.35	1.74	17.15	25.31	9.86	174.59
11	0.18	5.91	0.37	6.29	88.83	170.4	4.71	1.57	13.67	20.18	12.99	223.52
12	0.18	5.67	0.49	6.16	87.52	170.4	4.76	1.64	14.67	21.65	13.22	226.34
13	0.19	5.44	0.49	5.93	85.26	170.4	4.81	1.72	15.17	22.38	13.46	227.93
14	0.19	5.72	0.48	6.20	87.95	170.4	4.69	1.74	15.20	22.42	13.70	228.15
15	0.19	5.50	0.48	5.98	85.71	170.4	4.85	1.83	15.70	23.17	13.93	229.89
16	0.19	5.77	0.47	6.24	88.34	170.4	4.73	1.86	15.73	23.22	14.17	230.11
17	0.20	5.56	0.47	6.02	86.16	170.4	4.76	1.93	16.24	23.96	14.40	231.69

(b) Loss, temperature and weight

Index	Inductances					Secondary winding pattern and capacitances						
	Magnetizing Inductance Lm (uH)	Impedance ratio of Lm and Cp	Leakage inductance (uH)	Ratio of Magnetizing to Leakage	Ratio of tank Inductance Ls to Leakage	Number of sections	Number of layers per section	Turns per layer per section	Cpara from winding (nF)	Cpara to core (nF)	Cpara from diodes (nF)	Total Cpara (nF)
1	98.49	5.36	0.18	545.17	111.95	2	4	38	1.35	1.42	2.70	9.87
2	208.14	9.80	0.63	330.03	51.15	2	6	27	0.43	0.84	1.59	5.72
3	575.37	15.65	1.63	353.51	24.85	2	6	33	0.22	0.36	0.68	2.50
4	766.02	18.25	2.15	355.75	21.44	2	6	33	0.16	0.26	0.51	1.87
5	871.56	18.92	2.43	358.77	24.65	2	6	33	0.14	0.23	0.43	1.60
6	1087.43	19.72	3.11	349.95	19.53	2	6	27	0.08	0.16	0.30	1.08
7	1961.02	28.65	5.38	364.37	13.99	2	6	33	0.06	0.10	0.19	0.71
8	2247.08	28.83	6.37	352.83	13.46	2	6	27	0.04	0.08	0.15	0.53
9	3486.25	37.92	9.48	367.67	10.66	2	6	33	0.03	0.06	0.11	0.40
10	4916.16	44.56	13.35	368.16	9.09	2	6	33	0.02	0.04	0.08	0.28
11	3545.66	32.74	5.81	610.26	20.51	2	4	38	0.04	0.04	0.08	0.30
12	3785.97	35.59	7.39	512.01	15.82	2	5	38	0.03	0.04	0.08	0.28
13	4034.17	38.60	7.93	508.67	14.50	2	5	38	0.03	0.04	0.08	0.28
14	4034.17	39.28	7.98	505.37	14.15	2	5	38	0.03	0.04	0.08	0.28
15	4290.25	42.49	8.56	501.44	12.98	2	5	38	0.03	0.04	0.08	0.28
16	4290.25	43.21	8.61	498.22	12.68	2	5	38	0.03	0.04	0.08	0.28
17	4554.20	46.64	9.20	495.04	11.68	2	5	38	0.03	0.04	0.08	0.28

(c) Electric models and parasitics

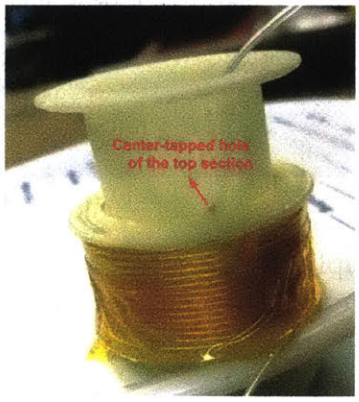
Table D.11: Details of the weight study of the inverter stage and the transformer stage (Part 3 of 3, transformer). The selected design (index 3) is highlighted in red.

D.4 Experimental

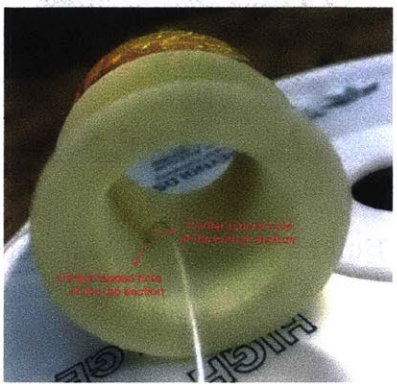
D.4.1 Construction details

Transformer bobbin and insulation

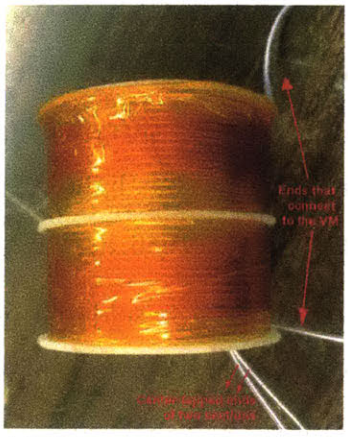
A customized bobbin with two-section secondary is made by 3D printing of ABS material, as shown in Fig. D-11 (we tried machining bobbins with PTFE and Delrin but with the required thickness, they seemed to lack stiffness). The bobbin is center-tapped so that the center node can be grounded to insure the symmetry. To increase the electrical insulation, PTFE tape, Kapton tape and high voltage dope are used on the bobbins and windings.



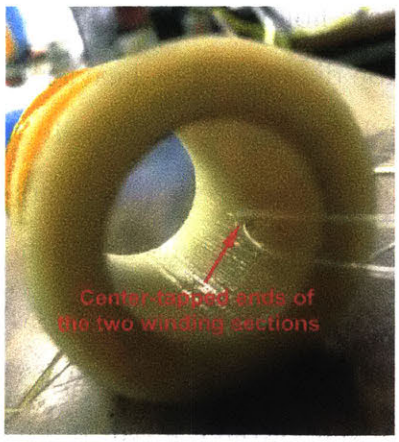
(a) Side view of half of the secondary winding



(b) Top view of half of the secondary winding



(c) Side view of the full secondary winding

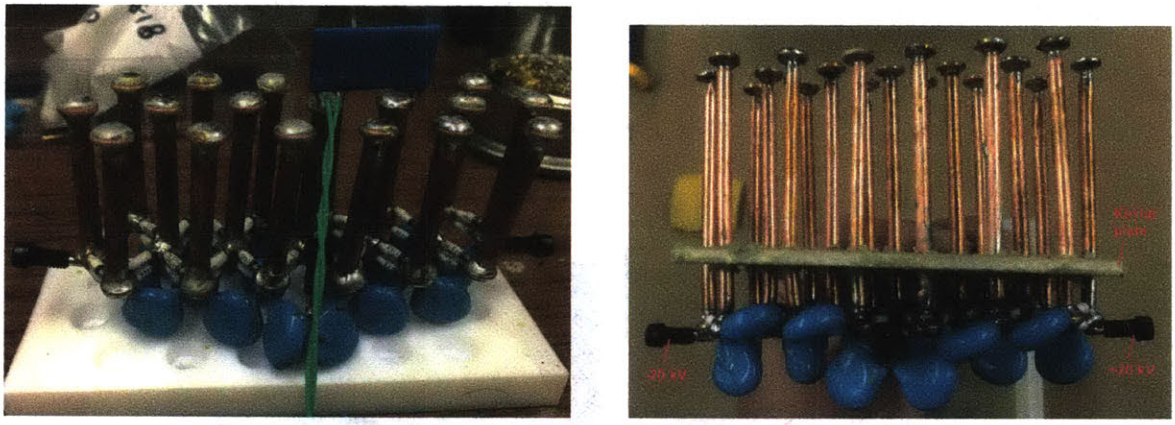


(d) Top view of the full secondary winding

Figure D-11: Building of the transformer

Voltage multiplier

The build of the voltage multiplier was time-consuming, owning to the complicated interconnections among 48 diodes (24 pairs of 2 diodes in parallel), 18 capacitors and 19 heat sink rods. To avoid sharp edges, round bezels was used at all joints to connect all leads.



(a) (b)

Figure D-12: Building of the voltage multiplier (a) version 1 with hollow copper tubes (b) side view of version 2 (built with help from Haofeng Xu of LAE)

Two version of the voltage multiplier was built, as shown in Fig. D-12. Version 1 (Fig. D-12a) uses hollow copper tubes as heat sinks, which are easy to machine, flexible in the tube diameter, but heavier[11]. Version 2 (Fig. D-12b) uses off-the-shelf heat pipes (sealed copper tubes partially filled with heat-carrying liquid or vapor), which are only offered in several diameters and lengths, but lighter and have better heat transfer. The final design uses Wakefield-Vette's 121686_REV1.

A 1000:1 voltage divider (OHMITE SM204RD-0009) is soldered on the opposite end of the heat pipes across one stage of the voltage multiplier. The divided-down voltage is brought out through a pair of high voltage wires to the microcontroller for the close-loop control.

[11]Machinable copper tubes usually has a thicker wall thickness compared with the heat pipes.

Connectors and wires

To reduce the overall weight, we choose to use lightweight banana-type connectors (Pomona Electronics 5936-0 and 5935-0) instead of those designed specifically for high voltage purposes, which are heavily insulated and large in size. We pay the price of the localized corona discharges at these connections, but in fact causes no noticeable reduction in efficiency nor electrical, visual, audible disruptions through our 1 year of testing (we could observe 2-3 minor discharging spots in a dark room). If one were to build a more robust industrial-grade converter, these should be upgraded accordingly.

The 18 kV FEP-insulated wires (Teledyne Reynolds 178-5790) was used where voltages were below 10 kV. The 30 kV Silicone-coated FEP-insulated wires (Teledyne Reynolds 178-8781) was used where voltages were above 10 kV.

Other high voltage wire makers include Rubadue [147], AXON [109], DRUFLON [110]. Other high voltage connector makers include Glenair [148] and Amphenol Alden [149].

D.4.2 Resistive load

Individual high voltage resistors that can handle tens to hundreds of watts are rare, expensive and often offered only discrete values. Thus we built the test loads by flexibly connecting many smaller resistors in series and parallel (Fig. D-13).

A PCB board has 24 pads (4 by 6), on each of which soldered 2 PCB micro jack (Keystone P/N 1682) to insert the lead of a through-hole resistor in. The PCB load board can accommodate Vishay RS/NS series through-hole resistors, OHMITE 20 series through-hole resistors, or others which have similar body length and lead size. One can easily plug and remove a resistor, and the resistor leads friction-fit in the micro jack and guarantees the electrical connection.

D.4.3 Efficiency measurement

The input current and the input voltage into the prototype high voltage dc-dc power converter are measured by two digital multimeter Agilent U3606A.

The output voltage is measured with Tektronix P6015A at the +20 kV terminal of

(a) Resistor load box enclosed. The leads of the load are brough out from the top of the box. Four fans are mounted on the sides of the box to blow air on the resistors.

(b) Resistor load printed-circuit board. One can easily swap different resistors in. PCBs can be stacked vertically on top of each other through four standoffs.

Figure D-13: Variable resistive load box

the voltage multiplier and multiplies by 2 to obtain the output voltage[12]. The output current was not measured directly because the full-wave interleaved nature of the voltage multiplier. The output power was calculated by the output voltage and the load resistance with a temperature coefficient adjustment (assumed to be 260 ppm ($260 \times 10^{-6}\Omega$) per °C temperature rise measured from 25 °C).

No	MOSFET	Load	Multimeter		Oscilloscope readings			Absolute temperature (°C)						Load resistance (Mohm)	Input power (W)	Output power (W)	Efficiency
			Vdc (V)	Idc (A)	Transformer input voltage (pk-pk) (V)	Inductor current (pk-0) (A)	Output voltage (kV)	MOSFET	Inductor	Transformer	Diodes	Load	Note				
1	GaN System GS66504B (final design)	5.33 Mohm resistor load (53 of Vishay Dale RS010100K0FE73 resistor (100 kohm, 10 W, 5% each))	24.15	0.36	127.00	0.93	6.04	34.00	26.30	26.00	26.70	27.50	Measured after 2 mins	5.33	8.77	6.84	0.78
2			40.23	0.59	208.00	1.49	10.00	35.40	27.00	26.00	28.80	30.00		5.34	23.62	18.74	0.79
3			60.32	0.88	312.00	2.22	15.04	36.70	30.60	28.30	34.60	40.90		5.35	53.26	42.26	0.79
4			80.39	1.22	430.00	3.02	20.60	41.20	33.60	31.10	39.00	53.50		5.37	98.00	79.03	0.81
5			100.51	1.42	520.00	3.66	25.20	49.30	40.30	36.00	44.60	66.00		5.39	142.22	117.89	0.83
6			120.64	1.67	620.00	4.38	30.00	59.70	46.60	40.00	50.00	83.60		5.41	201.71	166.32	0.82
7			140.76	1.87	716.00	5.00	34.40	69.20	56.00	45.00	59.00	90.00		5.42	263.22	218.33	0.83
8			160.88	2.26	800.00	5.90	40.40	84.50	66.50	50.00	70.00	105.00		5.45	363.59	299.74	0.82
9		3.05 Mohm resistor load (60 of OHMITE B20J50KE resistor in series (50 kohm, 20 W, 5% each))	177.00	3.29	906.00	5.48	38.00							3.00	582.33	481.33	0.83
10	EPC 2025 (obselete after 2016)	2.57 Mohm resistor load (one 40 Mohm resistor in parallel with 54 of OHMITE B20J50KE resistor in series (50 kohm, 20 W, 5% each))	40.30	0.79	199.00	1.67	8.12	DID NOT MEASURE				32.80	Measured after 1 min	2.58	32.00	25.60	0.80
11			120.59	2.23	588.00	4.88	24.20					95.50		2.62	268.92	223.77	0.83
12			168.80	3.38	852.00	6.85	35.60					142.00		2.65	570.04	478.58	0.84
13			176.82	3.77	916.00	7.15	38.90					180.00		2.68	667.14	564.58	0.85

Table D.12: Efficiency measurement of the prototype high voltage dc-dc converter.

Table D.12 lists several efficiency measurements. The ones with GaN system GS66504B FETs (No.1 to 9) are the final version presented in this Chapter and used in the flight test. Depending on the voltage and power, its efficiency ranges from 78% to 83%. With this prototype, we were not able to (nor needed) push to above

[12]Voltages at both the +20 kV and the −20 kV terminals were measured to ensure the symmetric. The −20 kV node voltage is slightly lower but the discrepancy is small enough to be neglected.

~550 W at the output for more than 1.5 min before the FETs overheat and blew up.

We also listed measurements 10 to 13, which was conducted on a previous prototype using EPC 2025 FETs. We were able to push to 565 W at 39 kV with an efficiency of 85%. Though the manufacturer stopped its production after 2016.

The input voltage, input current and output voltage are also measured and recorded by the microcontroller (which are used during flight tests in Chapter 6). These recordings were also calibrated against the measurement by the multimeter and the oscilloscope here.

Function	**Explanation**	**Components**	**Manufacturer**	**P/N**
Start-up	Function as a current limiter to charge the input capacitor	DPDT relay	TE connectivity	9-1462038-8
		SPST relay		1462041-7
		Relay driver	Diode Incorporated	DRDC3105F-7
		Zener diode	Nexperia	PLVA650A,215
		2 MΩ resistor	Yageo	311-2.0MERCT-ND
On-board data recording		RAM	Cypress	CY15B104Q
RC control, pair with the hand-held RC controller DX6i. The "Gear" signal is wired to the HVPC's MCU pin 42.		RC receiver	Sparkfun	AR6310
LED indicator		LED	OSRAM Opto	LE RTDUW S2W
		LED driver	On Semi	NDS331N
Mechanical emergency switch	Inline with the logic battery, mounted on the bottom of the fuselage.	On Semi	CAT6219	3.3 V output
Sensing & protection	measure battery current and over-current protection	current sensor	Allegro	ACS712ELCTR
		fuse	Littlefuse	04853.15DR
	measure battery pack temperature	thermal couple amplifier	Analog devices	04853.15DR
	measure battery voltage	499 kΩ	tt-electronics-welwyn	PCF0805R-499KBT1
		4.99 kΩ	Stackpole	RNCF0603TKY4K99
	measure output voltage	1000:1 resistor divider	OHMITE	SM204RD-0009

Table D.13: Component list of the accessory circuits in the 1st-generation dc HVPC

D.4.4 Accessory circuits

Accessory circuits are also included in the inverter board of the high voltage dc-dc power converter (dc HVPC) to facilitate the flight, including: start up circuit, on-

board data recording, LED indicator[13] and emergency switch. See Table D.13 for a list of components for each accessory function. These are tested in Chapter 6.

D.5 High voltage experimental apparatus

This section describes 1) how to set up a high voltage experimental apparatus like the one built for this project. 2) instrumentations for high voltage experiments.

D.5.1 High voltage enclosure and related setup

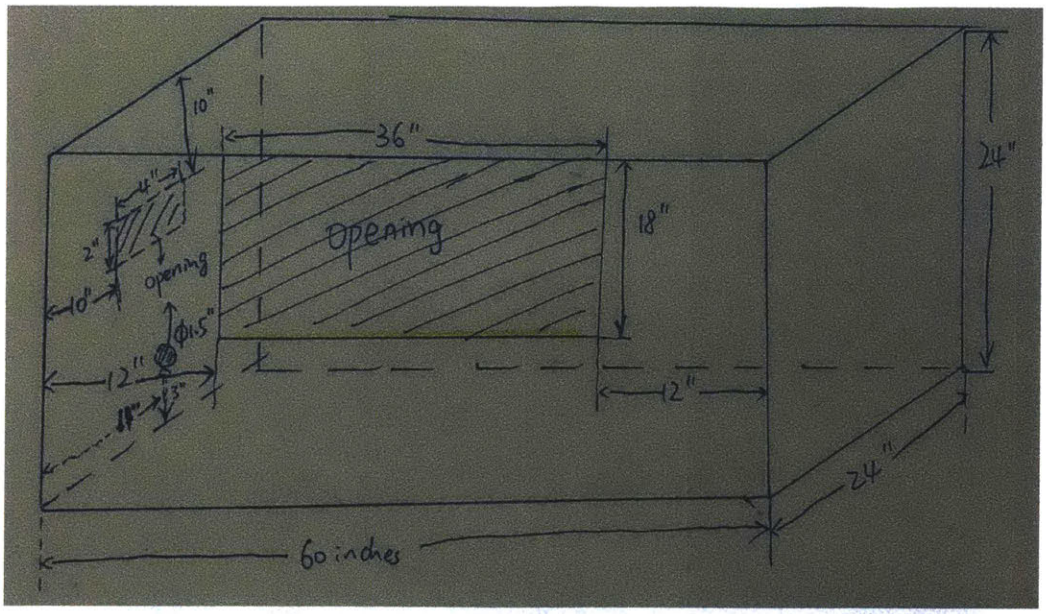
The high voltage apparatus consists of a grounded metal enclosure and a relay box. The developed high voltage prototypes were put in the enclosure and controlled to turn on and from outside of the enclosure. Several openings are made on the box to fit various cables connected to the prototype (power cables, measurement cables, etc). The enclosure should be closed during all experiments. The relay detects when the box is open and shuts off the power to the prototype and stop the experiments.

High voltage safety enclosure

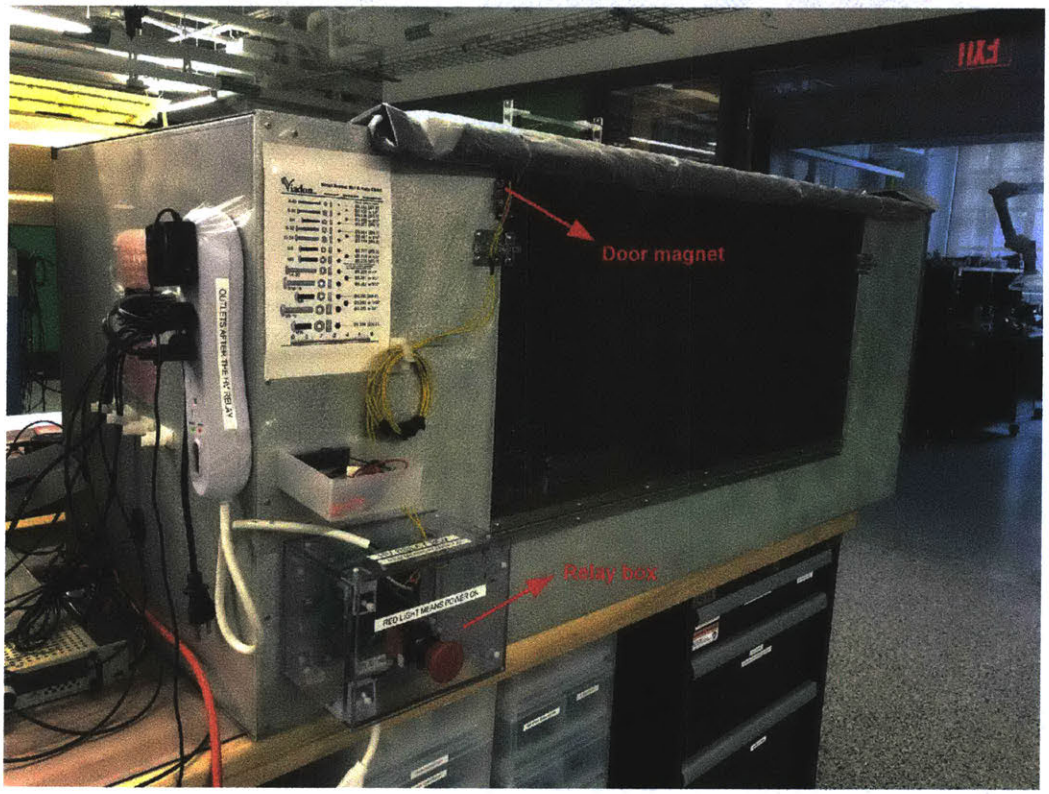
We design the enclosure to fit a prototype and associate high voltage load resistors with a clearance of 10 cm for 40 kV. One should adjust the clearance according to their own voltage level. The enclosure is 60" × 24" × 24" in size and built with .090 aluminum. See Fig. D-14 for the drawing and the photo. There are 3 openings on the enclosure wall:

- A cutout of 36" × 18" on the front panel, 0" from the top, 12" from each side. A window made with Lexan 0.250" thick with hinge to cover this cutout.
- A cutout of 4" × 2" on the left side panel, 10" from the top, 10" from each side
- A 1.5" diameter hole on the left side panel, 3" from the bottom, 11" from sides

[13]Green is power off, blue is charging input cap, red is high voltage on



(a) Drawing



(b) Photo

Figure D-14: Drawing and photo of the high voltage enclosure

Relay box

The purpose of the relay setup is to detect the front panel of the enclosure open and then cut off the power going into the box when the front window panel opens. This

protects the researcher from accidentally opening the window while the experiments are on. See Fig. D-15 for the photo of the relay and Table. D.14 for a BOM.

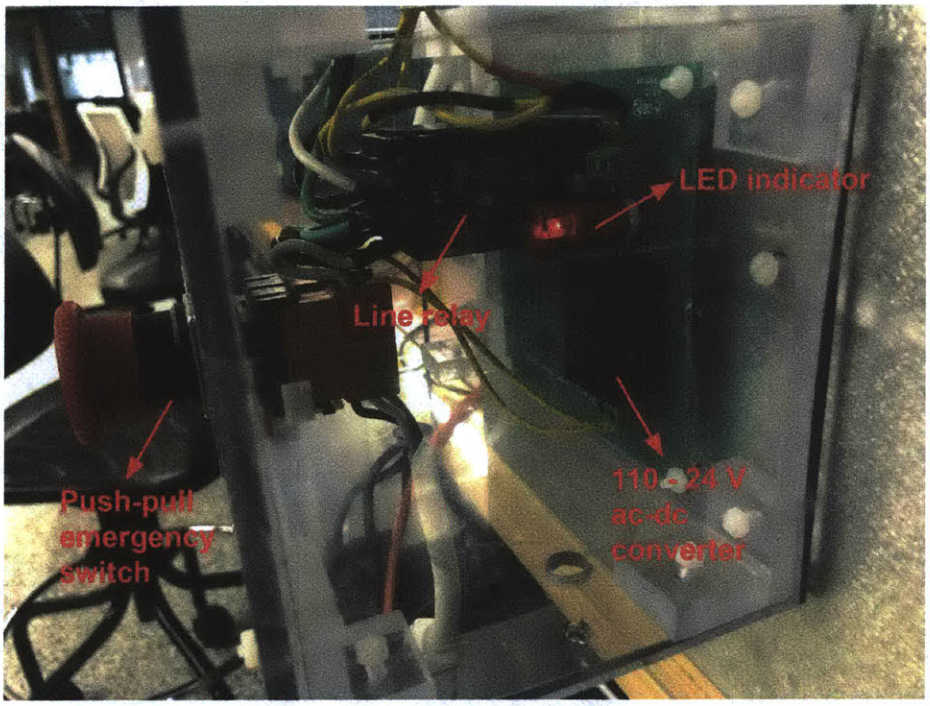


Figure D-15: Photo of the relay box

Function	Digikey P/N or Link
Door magnet	Amazon B0009SUF08
A DPDT 20 A line relay (controlled by 24 V)	PB624-ND
A 110 V push pull switch	SW1228-ND
A ac to 24 V power supply to power the relay	102-2585-ND
An 24 V indicator LED	679-3485-ND
Two terminal block connectors	277-1667-ND

Table D.14: BOM of the relay box

D.5.2 Other instruments

Grounding stick

One should use the grounding stick to discharge the circuits after the experiments are done before touching it. In the case when a person is shocked or physically touching the high voltage by accidents, DO NOT touch the person by hand; instead use the grounding stick to separate the person from the high voltage source.

We used the Groundstick-103 from http://www.hvrapc.com/groundstick.asp with a specification of 16 KJ energy in 10 mins, 50 kV.

AED equipment

A Phillips Heartstart FRx AED defibrillator was installed in 10-061, the MIT room with the high-voltage setup, in case an emergency were to happen.

High voltage probes

For high voltage dc measurement below 4–6 kV, Teledyne LeCroy PPE4KV or PPE6kV series are cheap and accurate. For high voltage dc measurements below 20 kV, Tektronix P6015A offers good quality. There aren't off-the-shelf reliable probes that measure higher than 20 kV thus one needs to build a resistor divider network. For high voltage ac differential measurement, we used the Keysight N2891A, which is rated for 7 kV differential with a bandwidth of 70 MHz.

Appendix E

Diode evaluations and balancing techniques

E.1 Temperature rise and loss measurements

E.1.1 Experimental setup

The specifications of all diodes under tests are listed in Table. E.2. We categorized them into 3 groups based on sizes and used 3 PCBs to conduct the tests, as shown in Fig. E-1: RFU02VSM6S, RFU02VSM8S, ESH1GM and ESH1JM were in one group; diodes blocking 5–15 kV were grouped together; all other diodes were grouped together. Within each group, the thermal path of the PCB is approximately the same. The layout of the PCBs are shown in Fig. I-3.

We drive all of the diode rectifiers with a custom-built inverter and transformer [74]; a simplified schematic for this system is shown in Fig. E-2. The specifications of the inverter, the transformer and the load are listed in Table E.1. C_s, L_s are external capacitors and inductors. C_p represents the parasitic capacitance of the transformer and the diodes reflected to the primary side. The resonant tank was tuned such that the current in L_s was near sinusodial at the frequency of interest, resulting in a trapezoidal voltage at the rectifier input.

The load of the rectifier is a custom-built variable resistor load. Output capacitors

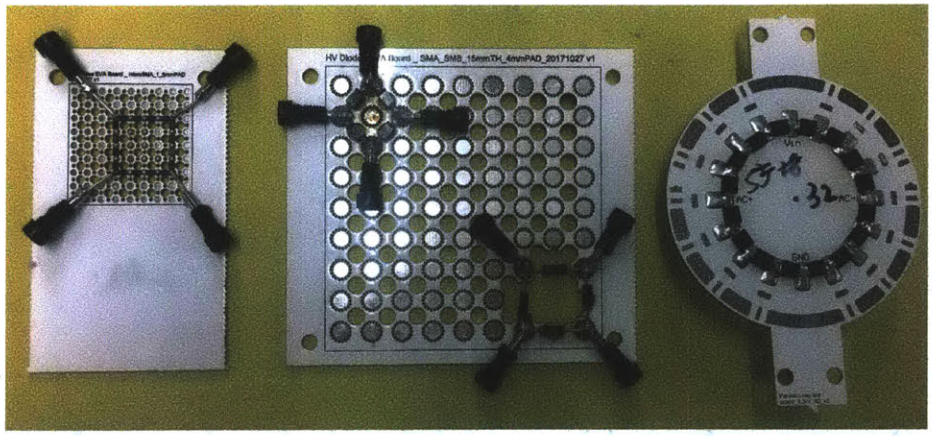


Figure E-1: Three PCBs for the diode tests. The left one is used for diode RFU02VSM6S, RFU02VSM8S, ESH1GM and ESH1JM; the middle one is used for diodes blocking 5–15 kV; the right one is for the rest. The layout of the PCBs are shown in Fig. I-3

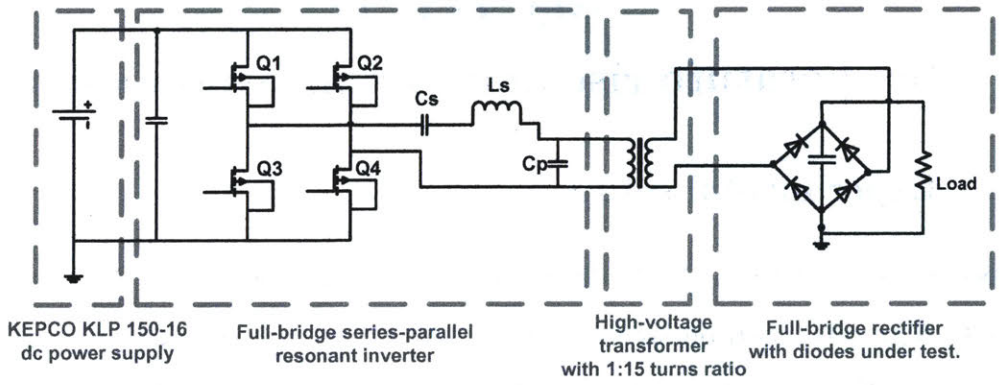


Figure E-2: A simplified schematic of the custom-built inverter and transformer to drive the diodes under test. The specifications of the inverter, the transformer and the load are listed in Table E.1.

were connected across the load to ensure the output voltage ripple $\leqslant 5\,\%$.

The rectified dc voltage was measured using a Tektronix 6015A probe. The load current was measured on the ground side using a Agilent 34410A digital multimeter in series with the resistor load. The temperature was measured by a FLIR E6 hand-held thermal camera placed at a fixed distance away from the PCB board.

See all test conditions in Table. E.2. The error of the temperature measurement is calculated as the maximum between $\pm 2\,^{\circ}\mathrm{C}$ and $\pm 2\%$ of the temperature reading.

Section	Component		Part Number or Value
Inverter	MOSFETs		GS66504B
	Series capacitor C_s		9.9 nF*, TDK C3216C0G Series
	Parallel capacitor C_p		~5 nF, parasitic capacitance of the transformer and diodes reflected to the primary side
	Inductor	Core size	RM14
		Material	TDK N49
		Windings	MWS AWG 14 (150/36)
		Value	13.4 uH*
Transformer		Core size	ETD49
		Material	Ferroxcube 3F35
		Primary	MWS AWG 14 (150/36)
		Secondary	Teledyne Reynolds 18 kV FEP wire
		Bobbin	ABS 3D print
		Turns	10:150 turns
Load	Resistor		Series and parallel 0.1–100 kΩ resistors, Ohmite B20 series (20 W) or Vishay Dale RS series (10 W)
	Output capacitor for V_o <=2 kV		One or more 15 nF 3 kV X7R capacitors, AVX 2225HC153KAT1A
	Output capacitor for V_o >2 kV		One of more 1 nF 12 kV ZM capacitor, Murata DHR4E4B102K2BB

Table E.1: Specifications of the custom-built inverter, transformer and load. The values marked with asterisk are for a specific operating point (the switching frequency is 1 MHz, the input voltage to the inverter is 40 V, the output voltage of the rectifier is 1.5 kV and the average output current is 30 mA). For each test in Table E.2, C_s, L_s, load resistor and output capacitor are tuned such that the resonant tank will provide the appropriate gain and frequency, the load will draw appropriate power and the output capacitor will ensure the output ripple voltage $\leqslant$5 % of the output voltage.

E.1.2 Loss characterization

For diodes with a maximum temperature rise lower than 80 °C in the 600 kHz and 1 MHz single diode tests (short for ac tests), we conduct a separate dc test: drive the same full-bridge rectifier with a dc source at various voltages and currents. We record the maximum temperature rise in each test after the rectifier reaches thermal equilibrium. We also record the dc current and dc voltage at thermal equilibrium, by multiplying which we get the loss of each diode. A mapping between maximum

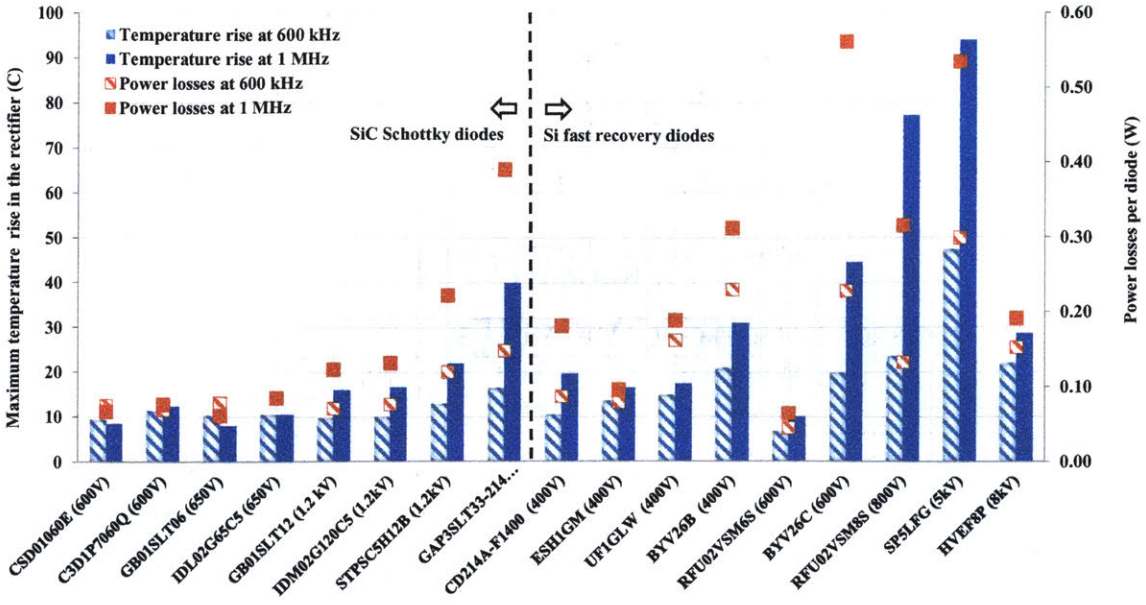


Figure E-3: The losses of selected diodes in the single diode tests

temperature rise and loss can be generated based on these tests. Then we back calculate the diode losses in ac tests by interpolating this temperature-loss map. In Fig. E-3, we show the maximum temperature rise of selected single diodes (same data as in Fig. 3-1a), and the loss corresponding to the maximum temperature rise.

E.2 Closed-form analytical solution of series diode voltages

We start with the charge equation at each node in Fig. 3-3a.

$$q_{n+1} = q_n + C_P v_n, ..., q_2 = q_1 + C_P v_1, q_1 = C_D v_1$$

Then we substitute q_i in the function of q_{i+1}'s function,

$$\begin{aligned} q_{n+1} &= q_n + C_P v_n \\ &= q_{n-1} + C_P v_{n-1} + C_P v_n = ... \\ &= q_1 + C_P(v_n + v_{n-1} + ... + v_1) \end{aligned}$$

Combine with

$$q_{n+1} = C_D(v_{n+1} - v_n)$$

We can solve for v_{n+1}

$$v_{n+1} = v_n + v_1 + \frac{C_P}{C_D}\sum_1^n v_i$$

Rearrange the equation, v_{n+1} is a function of v_n and v_{n-1},

$$\begin{aligned} v_{n+1} &= v_n + (-v_{n-1} + v_{n-1}) + v_1 + \frac{C_P}{C_D}\sum_1^{n-1} v_i + \frac{C_P}{C_D}v_n \\ &= v_n - v_{n-1} + (v_{n-1} + v_1 + \frac{C_P}{C_D}\sum_1^{n-1} v_i) + \frac{C_P}{C_D}v_n \\ &= v_n - v_{n-1} + v_n + \frac{C_P}{C_D}v_n = (\frac{C_P}{C_D} + 2)v_n - v_{n-1} \end{aligned}$$

We can find the closed-form solution of this series by solving the equation

$$x^2 = (\frac{C_P}{C_D} + 2)x - 1$$

Denote $a = \frac{C_P}{C_D}$, the roots to $x^2 - (a+2)x + 1 = 0$ are

$$x_1 = \frac{a + 2 + \sqrt{a(a+4)}}{2}, x_2 = \frac{a + 2 - \sqrt{a(a+4)}}{2}$$

Thus v_n is in the format

$$v_n = c_1 x_1^n + c_2 x_2^n$$

Where c_1 and c_2 are constants. The voltage drop across the nth diode is then

$$\begin{aligned} v_{Dn} = v_n - v_{n-1} &= c_1 x_1^n + c_2 x_2^n - (c_1 x_1^{n-1} + c_2 x_2^{n-1}) \\ &= c_1 x_1^{n-1}(x_1 - 1) + c_2 x_2^{n-1}(x_2 - 1) \end{aligned}$$

Plug in $n = 1$, we have

$$v_{D_1} = c_1(x_1 - 1) + c_2(x_2 - 1)$$

We also have initial condition

$$v_1 = c_1 x_1 + c_2 x_2$$

$$\begin{aligned} \because v_1 &= v_{D_1} \\ \therefore c_1 x_1 + c_2 x_2 &= c_1(x_1 - 1) + c_2(x_2 - 1) \\ \therefore c_1 + c_2 &= 0 \end{aligned}$$

Therefore, we have

$$\begin{aligned} \because v_1 &= v_{D_1} \\ \therefore c_1 x_1 + c_2 x_2 &= c_1(x_1 - 1) + c_2(x_2 - 1) \\ \therefore c_1 + c_2 &= 0 \\ \therefore c_1 = -c_2 &= \frac{v_1}{x_1 - x_2} \\ \therefore \frac{v_n}{v_1} &= \frac{x_1^n - x_2^n}{x_1 - x_2} \end{aligned}$$

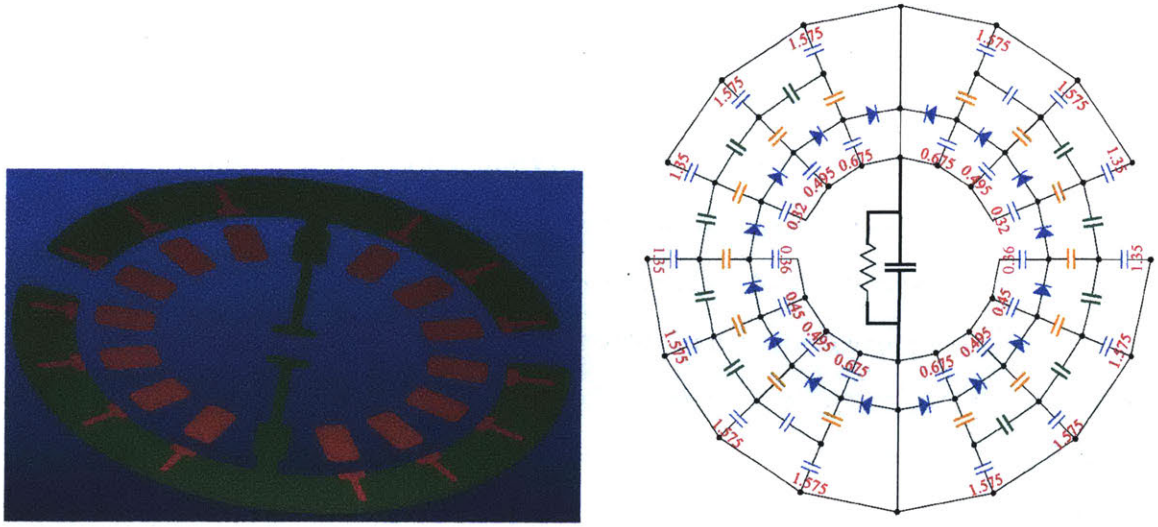
We can then get the closed-form analytical solution of each diode voltage in (3.1).

E.3 Implementation of compensation techniques

E.3.1 Parasitic capacitance of a PCB

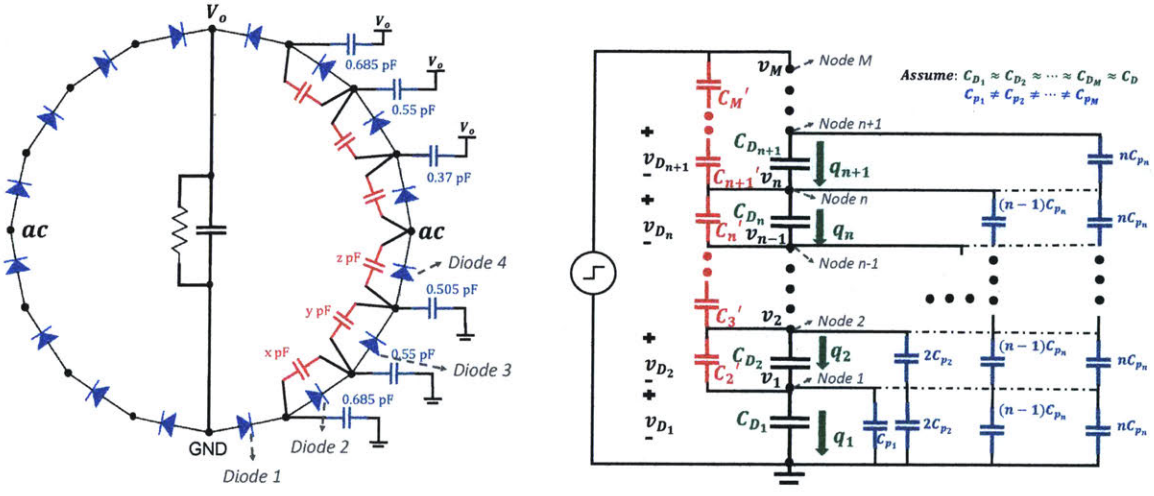
First, we export the PCB layout of the rectifier from Altium Designer to a .STEP file; then we import the .STEP file to FreeCAD, use a plug-in script provided by Fast Field Solver to process this geometry and save it as a net list file; lastly, we import the netlist file in the Fast Field Solver to solve for the capacitance between each two nodes in the geometry, as shown in Fig. E-4a.

The simulated capacitance matrix is shown in Fig. E-4b. We ignore the capacitance to ground from pads far away from the ground node (same for the V_o node). We further ignore the capacitances in green since they are very small, then combine the capacitances at each node, we get the simplified parasitic capacitances as shown in blue in Fig. E-5a.



(a) (b)

Figure E-4: a) The copper layout of the full-bridge rectifier used in the FEA simulation. In the Fast Field Solver [107], one can define a group of conductors (traces, pads, via, etc) as one node. In this geometry, ground node and V_o node are in green; rest of the nodes are in red. The square-shape pads are nodes connecting two diodes and the T-shape pads are nodes connecting to the probe adapters. b) The simulated capacitance matrix of the PCB layout in Fig. E-4a. All capacitances to common (GND or V_o) are in red and in pF. The capacitors in green are between two probe pads and are 0.002 pF; the capacitors in yellow are between each diode pad and probe pad and are 0.045 pF.



(a) (b)

Figure E-5: a) The estimated parasitic capacitance of each node to common (in blue); the capacitances are symmetric across the V_o-GND axis. The required compensation capacitors are marked in red. b) Schematic for calculation of compensation capacitances for the decoupled method in the general case where parasitic capacitances from each node to common are not equal.

E.3.2 Compensation capacitances in the general case

Figure E-5b shows a similar diagram to that of Fig. 3-4b. The only difference is that the parasitic capacitances from each node to common C_{p_n} have different values.

We split C_{p_i} into i capacitors in series, with the value of each as iC_{p_i} (for example, capacitor C_{p_2} is split into two capacitors each of value $2C_{p_2}$ connected in series and C_{p_n} is split into n capacitors each of value nC_{p_2} connected in series). We assume after compensation, $v_{D_1} = v_{D_2} = ... = v_{D_M}$, therefore the nodes on each dot-dash line in Fig. E-5b are at the same voltage potential, thus are virtually connected.

To ensure $v_{D_2} = v_{D_1}$, we need

$$C_2' = C_{p_1}$$

To ensure $v_{D_3} = v_{D_2}$, we need

$$C_3' = C_{p_1} + 2C_{p_2}$$

Following the trend, to ensure $v_{D_n} = v_{D_{n-1}}$, we have

$$C_n' = C_{p_1} + 2C_{p_2} + ... + (n-1)C_{p_{n-1}}$$

The compensation capacitances for the independent compensation method in the general case can be calculated in a similar fashion.

As an example, the capacitances x, y, z in Fig. E-5a are calculated as follows:

$$x = 0.685\,pF$$

$$y = 0.685 + 2 \times 0.55 = 1.785\,pF$$

$$z = 0.685 + 2 \times 0.55 + 3 \times 0.505 = 3.3\,pF$$

As mentioned in Section 3.4, capacitances x, y and z are implemented with discrete capacitors with values of 0.5 pF, 1.5 pF and 3 pF respectively.

The accuracy when using the proposed compensation methods in practical applications can be affected by: 1) the accuracy of the simplified diode model in Section 3.2

and 3.3 (it does not include non-ideality of diodes, such as voltage dependency of C_D, the leakage current and its temperature dependency, etc; 2) the accuracy of the simulated capacitance matrix of the PCB (include the tolerance of the FEA simulation process, the accuracy of the assumed dielectric constant of the PCB core, manufacture tolerances of the PCB board, etc); 3) the implementation of the compensation capacitances (availability of discrete capacitors, tolerance, voltage dependency of capacitors, etc). Note that as regards diode and compensation capacitor nonlinearity, it is typically possible to establish equivalent capacitance values for devices and capacitors (e.g., as done in [150]) that enable the methods developed here to be applied even when such nonlinearities are significant.

Table E.2: Specifications of diodes under tests and conditions of tests in Fig. 3-1a and Fig. 3-1b. See Section E.1 for error estimations of the temperature measurements. All data is updated in Sept. 2019.

* These tests did not reach thermal equilibrium and were cut off after the temperature became too high (cut off time varies between 30 to 90 seconds).
◇ Through-hole diodes. In all the tests in Section 3.1, the leads of these diodes were cut to <3 mm and soldered on one of the PCBs shown in Fig. E-1.
• Most high voltage diodes ($>= 5kV$) have unconventional packages. Here "diode body length (mm)" × "diode body width (mm)" is listed.
§ The names of following manufacturers are abbreviated: Taiwan is Taiwan Semiconductor, Dean is Dean Technology, VMI is Voltage Multiplier Inc.
†† For most Si diodes under tests, datasheets do not provide the temperature information of the "Forward Current".
† These reverse recovery times are defined as "Switching Time" in the corresponding datasheets.

Manufacturer PN	Manufacturer§	Type	Rated voltage (V)	Forward current†† (mA)	Reverse recovery (ns)	Capacitance @1 V (pF)	Package	Weight (mg)	No. of series diodes	Ave. output voltage (V)	Ave. output current (mA)	Temp. rise at 600 kHz (°C)	Temp. rise at 1 MHz (°C)
CSD01060E	Wolfspeed	SiC Schottky	600	1000 (T_c ~ 158 °C)	~0	80(@0 V)	TO-252-2	315.3	1	298	197.3	9.4	8.4
									2	598	200.3	13.7	10.5
									4	1200	187	18.3	14.7
C3D1P7060Q	Infineon		600	1700 (T_c ~ 150 °C)	~0	82.5(@0 V)	PowerQFN 3.3 × 3.3	32.9	1	301	198	11.4	12.3
									2	597	198.7	19.8	16.7
									4	1200	187	33.8	34.5
GB01SLT06	GeneSiC		650	1000 (T_c ~ 150 °C)	20†	76	DO-214AA	87.8	1	298	197.5	10.3	8
									2	599	199.1	18.2	12.6
									4	1190	186.3	26.1	19.4
IDL02G65C5	Infineon		650	2000 (T_c ~ 150 °C)	~0	70	ThinPak 8 × 8	184.4	1	300	199.5	10.5	10.5
GB01SLT12	GeneSiC		1200	1000 (T_c ~ 160 °C)	10†	71	DO-214	87.6	1	599	198.4	9.8	16
									2	1190	190.9	23	17
IDM02G120C5	Infineon		1200	2000 (T_c ~ 170 °C)	~0	182	TO-252-2	314.5	1	598	197.5	10	16.7
									2	1200	186.7	23	22
STPSC5H12B	ST		1200	5000 (T_c ~ 150 °C)	~0	450	DPAK	389.6	1	597	197.8	13	22

GAP3SLT33	GeneSiC		3300	300 (T_c ~ 125 °C)	10†	38	DO-214	65.4	1	1490	29.7	16.5	40
									2	3000	29.8	28.5	48.2
CD214A-F1400	Bourns		400	1000	25	17	DO-214AC	68.5	1	199	197.5	10.5	19.7
									2	401	198.4	19.2	29.5
									4	801	190	36	42
ESH1GM	Taiwan		400	1000	25	3(@4 V)	Micro SMA	6.2	1	201	201	13.6	16.5
UF1GLW	Taiwan		400	1000	20	25(@4 V)	SOD-123W	14.5	1	205	202.7	14.9	17.5
									2	400	202.2	16.4	32.3
									4	800	189	–	42
UF4004	ViSHAY		400	1000	50	17	DO-41 ◇	110.6	1	200	198	18.5	74
BYV26B	ViSHAY		400	1000	30	25	SOD-57◇	160.5	1	203	199.8	21	31
									2	400	202.5	34	64
RFU02VSM6S	ROHM		600	200	35	3	TUMD2SM	5.9	1	301	39.9	6.8	10.1
BYV26C	ViSHAY		600	1000	30	25	SOD-57 ◇	154.5	1	298	196	20	44.5
ESH1JM	Taiwan		600	1000	25	3(@4 V)	Micro SMA	6.3	1	301	200	63	–
UF1JLW	Taiwan		600	1000	25	15(@4 V)	SOD-123W	14.9	1	299	201	68.7	–
MUR160S	Taiwan		600	1000	50	50	DO-214AA	102.5	1*	298*	207*	110	–
ES1JL	Taiwan		600	1000	35	9.6	Sub SMA	20.2	1*	299*	197*	110	–
CD1408-FU1800	Bourns	Si	800	1000	35	16	1408	16.1	1*	300*	150*	110	–
RFU02VSM8S	ROHM		800	200	35	3	TUMD2SM	6.54	1	407	40	23.6	77
S1MLS	Taiwan		1000	1200	-	10	SOD-123HE	13.7	1*	500*	13*	110	–
ACGRAT105L-HF	Comchip		1000	1000	-	12	2010	23.1	1*	500*	5.6*	103	–
HS1M	Taiwan		1000	1000	75	18	DO-214AC	73.4	1*	400*	160*	102	–
ACURA107-HF	Comchip		1000	1000	75	18	DO-214AC	59.8	1*	400*	190*	110	–
UA1M	SMC Diode		1000	1000	75	-	DO-214AC	69.6	1*	400*	40*	110	–
FM2000GP	MCC		2000	500	500	30(@4 V)	DO-214AC	67.3	1*	800*	70*	110	–
SM3F	Dean		3000	350	65	6(@4 V)	SMA J-Lead	104.4	1*	1500*	80*	104	–

X50FF3	VMI		5000	75	30	3	6.6 × 4.3 ◇●	244	1*	2500*	17*	73	–
SP5LFG	Dean		5000	140	50	7.2(@0 V)	8.6 × 2.8 SMT●	102	1	2500	30	47.2	93.8
Z50FF3	VMI		5000	180	30	16	8.9 × 5.5 ◇●	1040	1*	2500*	36*	81.8	–
HV200UF5	Dean		5000	200	50	12(@0 V)	9 × 5 ◇●	591.2	1*	2500*	42*	110	–
Z50FF3LL	VMI		5000	400	50	18	10 × 5.5 SMT●	641.7	1*	2500*	60*	110	–
HVEF8P	Dean		8000	30	20	0.33(@0 V)	6.6 × 2.5 ◇●	82.2	1	3990	5.35	21.9	28.5
UX-FBR8	Dean		8000	420	40	7.5(@0 V)	9 × 5 ◇●	571.8	1*	4000*	40*	110	–
SLU08M	Dean		8000	400	40	7.5(@0 V)	14 × 3.8 SMT●	418	1*	4000*	50*	110	–
X150FF3	VMI		15000	25	30	1.2	9.1 × 4.3 ◇●	510	1*	5000*	3.5*	75	–

Appendix F

Design study of second generation HVDC

F.1 Updates on the voltage multiplier weight study

Diode index	Manufacturer	Part Number	Rated voltage (V)	Rated current (mA)	Type	Unit weight (g)	Length (mm)	Width (mm)	Temperature rise of one diode (°C)		Loss of one diode at 1 MHz (W)	Test current at 1M (mA)	Forward drop (V)	Capacitance at 0V (pF)
									600 kHz	1 MHz				
1	Wolfspeed	CSD01060E	600	1000	SiC Schottky	0.315	6.73	10.00	9.40	8.40	0.07			
2	Infineon	C3D1P7060Q	600	1700		0.033	3.30	3.30	11.40	12.30	0.08	200.00	2.4	82.5
3	GeneSiC	GB01SLT06	650	1000		0.088	5.59	3.94	10.3	8	0.06			
4	Infineon	IDL02G65C5	650	2000		0.184	8.10	8.10	10.5	10.5	0.09			
5	GeneSiC	GB01SLT12	1200	1000		0.088	5.60	3.95	9.8	16	0.12	200.00	2.4	71.0
6	Infineon	IDM02G120C5	1200	2000		0.315	6.73	10.00	10	16.7	0.13			
7	ST	STPSC5H12B	1200	5000		0.390	6.73	10.00	13	22	0.22			
8	GeneSiC	GAP3SLT33-214	3300	300		0.065	5.59	3.94	16.5	40	0.39	30.00	5.2	38.0
9	Bourns Inc.	CD214A-F1400	400	1000	Si	0.068	5.59	2.92	10.5	19.7	0.18			
10	Taiwan	ESH1GM	400	1000		0.006	2.70	1.35	13.6	16.5	0.10			
11	Taiwan	UF1GLW	400	1000		0.014	3.80	1.90	14.9	17.5	0.19	200.00	1.3	25.0
12	VISHAY	BYV26B	400	1000		0.161	4.00	3.60	21	31	0.31			
13	ROHM	RFU02VSM6S	600	200		0.006	2.50	1.40	6.8	10.1	0.06			
14	VISHAY	BYV26C	600	1000		0.155	4.00	3.60	20	44.5	0.56			
15	ROHM	RFU02VSM8S	800	200		0.007	2.50	1.40	23.6	77	0.32			
16	Dean	SP5LFG	5000	270		0.102	8.55	2.79	47.2	93.8	0.53			
17	Dean	HVEF8P	8000	30		0.082	10.20	2.50	21.9	28.5	0.19	6.00	20.0	0.3
18	VMI	X150FF3	15000	50		0.510	9.14	4.32	75					

Table F.1: Specifications of candidate diodes in the 2nd-gen voltage multiplier design. The ones highlighted in red are the most promising. Temperature data, loss data and the manufacturer abbreviation are all the same as in Fig.E-3 and Table E.2. The error estimation in the temperature and loss measurement is not included.

The process of the weight comparison of voltage multipliers (VM) is:

We pick a topology and calculate the weight of each capacitor in the selected topology. We identify the voltage across each capacitor and calculate their capacitances following the same method as in Chapter 2 but limiting the voltage droop on the SSL R_{Loss} to 5% of the output voltage and the voltage ripple requirement to

100 V. Then, knowing the capacitance and the blocking voltage of each flying/output capacitor, the lightest discrete capacitor in the candidate pool is selected as the implementation. We allow discrete capacitors to be connected in series up to 6 and parallel up to 10 to form one flying/output capacitor and the voltage derating is 50%. The weight is calculated accordingly.

Similarly, knowing the blocking voltage and carrying current of each diode in the VMs, the lightest discrete diode is selected from the pool and its loss is used to calculate the total loss. We allow discrete diodes to be connected in series up to 4 and parallel up to 6 to form one diode. The diode voltage derating is 50% and current derating is 10%.

We assume the PCB density is 3.3 mg/mm^2 (a standard 2-layer PCB). We calculate the PCB area taken by diodes as the area of all diodes (in practice, they can be soldered on both sides of the board, but we still want a 50% safety margin). We calculate the PCB area taken by capacitors as 50% of the area taken by all capacitors (assuming two layers of capacitors can be soldered on top of each other).

The adjustments include 1) assuming 80% of the measured losses is the switching losses and scales with the square of its blocking voltage. 2) if multiple diodes are connected in series and/or parallel as a higher-voltage diode, multiplying the loss of one diode accordingly.

F.2 System optimization

F.2.1 Updated inverter design equations

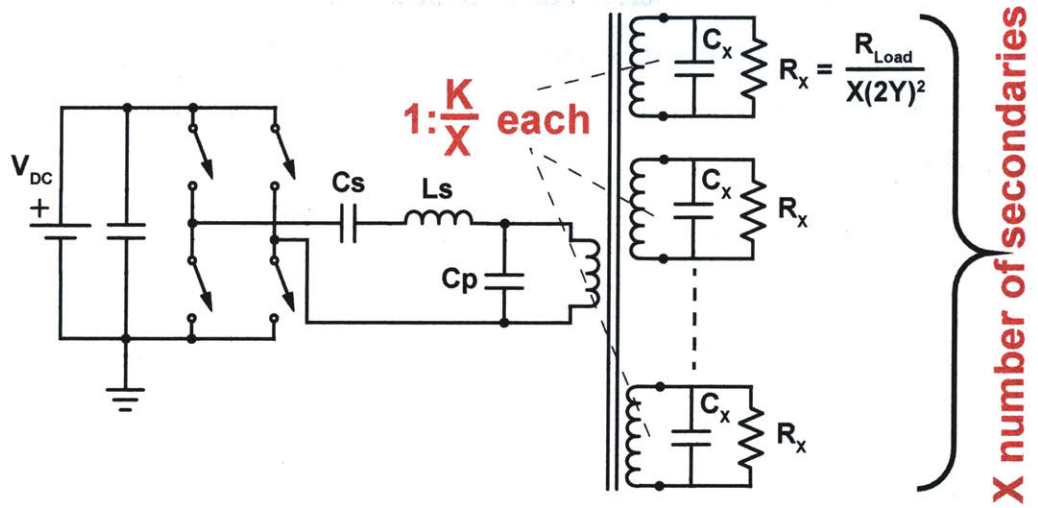
Appendix D presents the design equations for the series-parallel resonant inverter when connected with a $1 : K$ one secondary transformer and a 6 stage voltage multiplier. Here we consider multi-secondary transformer, which complicates the design equations and circuit models.

Figure F-1 shows step-by-step models to calculate the equivalent load resistance reflected at the resonant tank when a multi-secondary transformer is connected. One

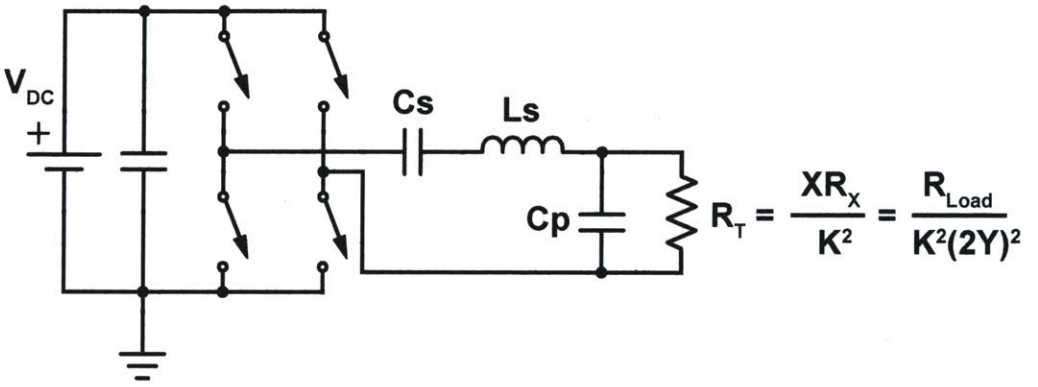
can replace R_T with eq (F.1) in equations listed in Section D.3.1 to design the series-parallel resonant inverter in this Chapter.

$$R_T = \frac{8}{\pi^2} \frac{R_{Load}}{K^2(2Y)^2}, R_{Load} = \frac{V_o^2}{P_o} \tag{F.1}$$

Where V_o, P_o are the output voltage and power of the converter. Y is the voltage gain of each voltage multiplier polarity.



(a)



(b)

Figure F-1: Step-by-step simplified circuit models from Fig. 4-10 to calculate the equivalent load resistance reflected at the resonant tank.

F.2.2 Updated equations for transformer parasitics

Section D.3.2 in Appendix D lists the equations used to estimate the parasitic capacitance of a high voltage transformer. In a multi-secondary transformer, one can reuse those equations to calculate the parasitic capacitance of each secondary winding reflected to the primary. The final capacitance should be X times that of a single winding because they are connected in parallel.

We give an example of calculating the diode body capacitance reflected to primary in the schematics in Fig. 4-10: a transformer with X secondaries, each secondary connects to a bipolar half-wave cockcroft-walton multiplier (each polarity has n stages). We assume each diode has a body capacitance of C_{Diode} – thus in a bipolar n-stage half-wave cockcroft-walton multiplier, the total diode capacitance is $4nC_{Diode}$.

With a X-secondary transformer (each winding has a turns ratio of $1 : \frac{K}{X}$), the final parasitic capacitance reflected back to primary is

$$C_{Para_{diode}} = X \times (4nC_{Diode} \times (\frac{K}{X})^2) = \frac{4nK^2}{X} C_{Diode}$$

Appendix G

Lightweight high-voltage inverter for dielectric-barrier discharge

G.1 Weight of magnetics in resonant topologies

Please refer to Chapter B and C for the core methods of the transformer and inductor weight study respectively. This section explains the variations/considerations for studying the magnetics in the resonant topologies, .i.e., as in Fig. 1-7a. In short, we follow four steps to simulate the lightest achievable weight of the magnetics at a fixed operating point:

- Sweep a range of designs. Each design is defined by: the core size, the core material, the wire build (the litz wire size and the number of strands per wire) and the winding pattern (the number of turns and the number of layers of the winding).

- Calculate electrical, thermal and mechanical parameters of each design. The electrical parameters include maximum flux density, inductance of the inductor, magnetizing impedance of the transformer. The thermal parameters include core loss (modeled with standard Steinmetz equations), copper loss (modeled with Dowell equations as in [111]) and absolute temperature (modeled as in [111]). The physical parameters include packing factor (considering insula-

tions), winding width and height.

- Rule out designs with constraints: maximum flux density $\geqslant$ 75% of saturation density, maximum temperature $\geqslant$ 90 °C, total loss $\geqslant$ 2% for inductors and $\geqslant$ 5% for transformers, overall packing factor[1] $\geqslant$ 0.7, and the windings need to fit in the window height and width.

- For each design that satisfies all constrains, we calculate the weight (consists of four parts: core, wire copper, wire insulation, and core insulation) and select lightest one.

G.1.1 Core size, wire build and winding pattern

We consider gapped EE cores for the inductor and ungapped EE cores for the transformer, center-leg winding in the height direction for both. The ranges of variables considered are summarized in Table. G.1.

	Inductor	**Transformer**
Core size	EE core window height $\boldsymbol{H}$ and width $\boldsymbol{W}$ 1 to 10 cm	EE core window height $\boldsymbol{H}$ and width $\boldsymbol{W}$ 1 to 15 cm
	Core thickness $\boldsymbol{T}$ and center-leg width $\boldsymbol{L_c}$ 0.1–2 cm	
Wire build	Set the litz wire diameter by the maximum of either twice the skin depth or the minimal available litz diameter.	
	Set the overall wire size by either the current density limit of 500 A/cm^3 or the minimal available wire size.	
	Minimal available litz size and wire size are both set to AWG44 (the diameter is 0.050 24 mm).	
Winding pattern	Number of turns 1 to 100, number of layers 1 to 10	Primary number of turns 1 to 100, primary and secondary number of layers are 1 to 10.

Table G.1: The range of variables on core size, wire-build and winding pattern considered in the weight studies of magnetics in the resonant topologies

[1]Defined as the area of wire copper, wire insulation and core insulation divided by the window area.

G.1.2 Core material and losses

We select 13 materials[2] in the range of 2 kHz to 10 MHz based on either their high performance factors ($PF = Bf$) in 2–500 kHz or high modified performance factors[3] (modified $PF = Bf^{\frac{3}{4}}$ [151]) in 0.1–10 MHz.

Manufacturer	Material Name	Type	Frequency Range*	Selectd properties	
				B_{SAT} (T)	μ_r
Ferroxcube	3C96	Ferrite	25 to 500 kHz	0.44	2000
	3F3	Ferrite	25 to 700 kHz	0.37	2000
	3F35	Ferrite	0.5 to 1 MHz	0.42	1400
	3F46	Ferrite	1 to 3 MHz	0.43	750
TDK	N49	Ferrite	0.5 to 1 MHz	0.4	1500
Magnetics	T	Ferrite	100 to 400 kHz	0.53	2000†
Vacuum-schmelze	VITROP-ERM 500Z	Nanocr-ystalline	2 to 200 kHz	1.2	2000†
FairRite	67	Ferrite	2 to 7 MHz	0.25	40
	61	Ferrite	2 to 20 MHz	0.25	125
Hitachi	MLX6A	Ferrite	50 to 500 kHz	0.41	2300
	ML91S	Ferrite	0.6 to 3 MHz	0.43†	1500†
	NL12S	Ferrite	1 to 5 MHz	0.45†	80†
DMEGC	DMR51	Ferrite	0.5 to 1.5 MHz	0.41	1100

Table G.2: Transformer core materials and selected properties. The ones used in the lightest designs shown in Section 5.1 are highlighted in red.
* This is the range in which core loss are provided in the datasheet.
† These parameters are estimated.

The 13 materials and some of their properties are listed in Table. G.2 and their PF and/or modified PF are plotted in Fig. G-1. Most of these PF and modified PF are calculated with core loss data from the manufacturer datasheets, except ML91S (experimental result provided by undergraduate research student Rod Bayliss of MIT).

Looking into the lightest designs in Fig. 5-3, Fig. 5-4 and Fig. 5-5, we find that VITROPERM 500Z is used in 10 to 100 kHz, T and 3C96 are used in 100 to 200 kHz, MLX6A in 200 to 400 kHz, DMR51 in 0.5 to 1 MHz and 3F46 above 1 MHz. These materials are highlighted in red in Table. G.2. We calculated the core loss using the standard Steinmetz equations as mentioned in Appendix B.

[2]Some other materials considered include Ferroxcube "3F45" "3F5", TDK "N97", Vacuumschmelze "VITROVAC 6030F" "VITROPERM 500F", Hitachi "PowerLite" "MAGAMP", and MK Magnetics "0.0007" Nano".

[3]Both at a loss density of 500 mW/cm^3. These performance factors are a first-order figure-of-merit to evaluate core materials when they are core-loss limited. High performance factor usually means less-lossy.

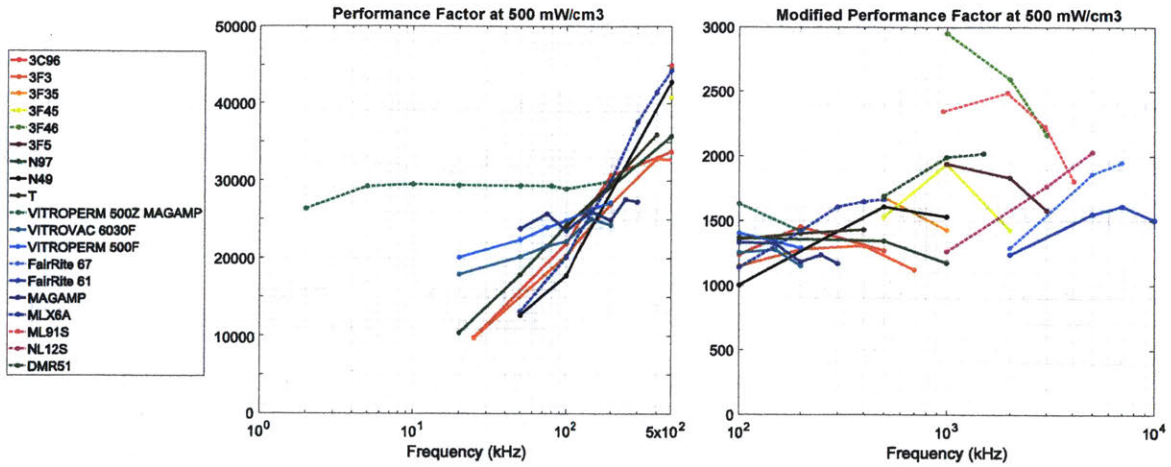


Figure G-1: Performance factor (PF) and modified PF of various core materials. The dotted lines mark the envelop of PF and modified PF. The envelope indicates that VITROPERM 500Z MAGAMP, MLX6A, DMR51, 3F46, ML91S, NL12S, FairRite 67 are potentially the best choices across the frequency spectrum.

G.1.3 Inductances and Impedances

We design the inductor and/or the transformer to satisfy an operating condition.

Inductor

The inductance is calculated based on V_{in}, G, f and P_o (therefore each point in Fig. 5-3 does not hold a constant inductance.). The resonant tank in Fig. 5-2 at resonance gives us

$$G = \frac{V_T}{V_{in}}, R = \frac{V_T^2}{2P_o}$$
$$L = \frac{R}{2\pi f \times G} = \frac{V_T V_{in}}{4\pi f P_o} = \frac{G V_{in}^2}{4\pi f P_o}$$

And the airgap is calculated as

$$airgap = \frac{\mu_0 A_c N^2}{L} - \frac{L_e}{\mu_r}$$

Where L_e is the length of the flux path in the core, A_c is the cross-sectional area of the core and N is the number of turns. We can then calculate the maximum inductor

current $I_{L_{max}}$ and therefore the maximum flux density B_{max} accordingly:

$$I_{L_{max}} = \frac{V_T}{R} \times G = \frac{2P_o}{V_{in}}$$
$$B_{max} = \frac{\mu_0 \mu_e N I_{L_{max}}}{L_e}, \mu_e = \frac{\mu_r}{1 + \frac{\mu_r \times airgap}{L_e}}$$

Transformer

In this study, we do not set limits on the magnetizing inductance, leakage inductances or the parasitic capacitances of the transformer. We assume the transformer has little leakage inductance and it can be modeled as an ideal transformer with a magnetizing inductance.

We do not impose any limit on the magnetizing impedance because it may be used in circuit operation and a hard limit will likely sacrifice the weight and specific power[4], though we still model and "observe" the magnetizing impedance, as shown in the next section (Fig. G-2 to Fig. G-5), with the equation:

$$L_c = \frac{N_p^2}{R_c} = \frac{\mu_0 \mu_r A_c N_p^2}{l_c}$$

G.1.4 Detailed simulation results and more interpretations

Inductor

Detailed simulation results for inductor sizing are shown in Table. G.3.

Current density of the wire: most designs have a current density of ~500 A/cm^2, which means the wire has been fully utilized. The exceptions are at high V_{in} and low frequency (the litz size is determined by the skin depth, which is larger than needed for carrying the current.)

[4]Note that our goal is to analyze the lightest achievable weight of the transformer in "general" resonant topologies, not to design the transformer with a certain impedance specification.

	Operation conditions				Core						Winding pattern			Wire build				L (mH)	airgap (mm)	Bmax (T)	Loss (W)			Max Temperature (C)	Overall Packing Factor	Weight (g)				
	PT (W)	Vin (V)	VT (V)	fs (Hz)	Core material	Center-Leg width (mm)	Thickness (mm)	Ac (mm2)	Window Height (mm)	Window Width (mm)	Num Of Turns	Turns per layer	Number of layers	Number of litz strands	Wire Copper Diameter (mm)	Wire Full Diameter (mm)	Current Density (A/cm2)				Core	Copper	Total			Core	Copper	Wire insulation	Core insulation	Total
Sweep Vin	200	40	160	10000	VITROPERM 500Z	7	15	105	25	10	27	13	2	5	1.91	1.92	437.09	0.25	0.33	0.90	1.30	1.19	2.48	72.60	0.31	49.39	41.14	0.08	0.16	90.68
	200	60	240	10000	VITROPERM 500Z	7	15	105	20	10	41	13	3	3	1.48	1.49	485.66	0.57	0.34	0.89	1.14	1.62	2.76	82.95	0.36	44.35	39.13	0.16	0.20	83.68
	200	80	320	10000	VITROPERM 500Z	7	15	105	20	10	54	13	4	3	1.48	1.49	364.24	1.02	0.33	0.90	1.16	1.87	3.03	88.58	0.47	44.35	56.59	0.30	0.27	101.21
	200	100	400	10000	VITROPERM 500Z	7	16	112	20	10	64	16	4	2	1.21	1.23	437.09	1.59	0.32	0.89	1.22	1.59	2.81	82.53	0.38	47.31	43.26	0.35	0.36	90.93
	200	120	480	10000	VITROPERM 500Z	7	19	133	15	10	64	12	5	2	1.21	1.23	364.24	2.29	0.26	0.90	1.30	1.71	3.02	89.65	0.51	49.80	50.51	0.50	0.42	100.72
	200	140	560	10000	VITROPERM 500Z	7	17	119	20	10	84	16	5	2	1.21	1.23	312.21	3.12	0.29	0.89	1.30	1.57	2.87	82.31	0.50	50.27	62.98	0.73	0.52	113.76
	200	160	640	10000	VITROPERM 500Z	7	20	140	20	10	81	16	5	2	1.21	1.24	273.18	4.07	0.24	0.90	1.55	1.26	2.81	77.42	0.49	59.14	65.83	0.87	0.68	125.64
	200	180	720	10000	VITROPERM 500Z	7	19	133	20	10	96	19	5	1	0.85	0.89	485.66	5.16	0.25	0.90	1.47	1.38	2.85	79.30	0.30	56.18	34.62	0.73	0.73	91.53
	200	200	800	10000	VITROPERM 500Z	9	16	144	20	10	99	19	5	1	0.85	0.89	437.09	6.37	0.23	0.89	1.73	1.12	2.84	77.52	0.31	66.36	34.76	0.82	0.75	101.87
	200	220	880	10000	VITROPERM 500Z	9	18	162	20	10	97	19	5	1	0.85	0.90	397.36	7.70	0.20	0.89	1.93	0.96	2.90	75.99	0.31	74.65	36.12	0.94	0.91	111.67
	200	240	960	10000	VITROPERM 500Z	9	19	171	20	10	100	20	5	1	0.85	0.90	364.24	9.17	0.19	0.89	2.05	0.86	2.91	75.07	0.32	78.80	38.33	1.09	1.03	118.16
	200	260	1040	10000	VITROPERM 500Z	11	17	187	20	10	99	19	5	1	0.85	0.91	336.22	10.76	0.16	0.89	2.43	0.72	3.16	77.42	0.32	93.35	38.02	1.17	1.08	132.45
	200	280	1120	10000	VITROPERM 500Z	11	19	209	20	10	95	19	5	1	0.85	0.91	312.21	12.48	0.14	0.90	2.73	0.63	3.37	78.46	0.31	104.33	38.50	1.28	1.26	144.10
	200	300	1200	10000	VITROPERM 500Z	11	20	220	20	10	97	19	5	1	0.85	0.91	291.39	14.32	0.13	0.89	2.86	0.58	3.44	78.54	0.32	109.82	40.38	1.44	1.40	151.61
	200	320	1280	10000	VITROPERM 500Z	13	18	234	20	10	97	19	5	1	0.85	0.92	273.18	16.30	0.11	0.90	3.29	0.51	3.80	82.70	0.32	125.80	40.45	1.55	1.45	167.70
	200	340	1360	10000	VITROPERM 500Z	13	19	247	20	10	98	19	5	1	0.85	0.92	257.11	18.40	0.11	0.89	3.46	0.47	3.93	83.27	0.33	132.79	41.94	1.71	1.60	176.33
Sweep G	200	100	100	10000	VITROPERM 500Z	4	12	48	15	10	37	12	3	2	1.21	1.23	437.09	0.40	0.17	0.90	0.40	0.49	0.89	53.69	0.29	15.21	17.75	0.15	0.05	33.01
	200	100	200	10000	VITROPERM 500Z	5	14	70	15	10	51	12	4	2	1.21	1.23	437.09	0.80	0.25	0.89	0.61	1.11	1.72	72.89	0.40	23.52	30.21	0.25	0.13	53.86
	200	100	300	10000	VITROPERM 500Z	7	15	105	15	10	51	12	4	2	1.21	1.23	437.09	1.19	0.25	0.89	1.02	1.23	2.25	78.05	0.40	39.31	33.39	0.27	0.21	72.91
	200	100	400	10000	VITROPERM 500Z	6	18	108	20	10	66	16	4	2	1.21	1.23	437.09	1.59	0.33	0.89	1.13	1.69	2.83	83.64	0.39	43.55	45.97	0.38	0.38	89.89
	200	100	500	10000	VITROPERM 500Z	7	19	133	20	10	67	16	4	2	1.21	1.23	437.09	1.99	0.33	0.89	1.46	1.82	3.28	87.62	0.40	56.18	49.46	0.41	0.51	106.15
	200	100	600	10000	VITROPERM 500Z	8	18	144	25	10	75	18	4	2	1.21	1.23	437.09	2.39	0.38	0.88	1.81	2.04	3.85	89.93	0.35	70.50	55.43	0.45	0.69	126.63
	200	100	700	10000	VITROPERM 500Z	8	18	144	35	10	86	28	3	2	1.21	1.23	437.09	2.79	0.42	0.90	2.22	1.63	3.85	81.67	0.29	84.33	59.31	0.49	1.03	144.66
Sweep PT	100	100	400	10000	VITROPERM 500Z	5	15	75	20	10	95	19	5	1	0.85	0.87	437.09	3.18	0.23	0.89	0.75	0.91	1.66	64.81	0.28	28.80	28.13	0.33	0.32	57.25
	200	100	400	10000	VITROPERM 500Z	7	17	119	20	10	60	15	4	2	1.21	1.23	437.09	1.59	0.29	0.89	1.30	1.54	2.84	81.73	0.35	50.27	41.79	0.34	0.37	92.43
	300	100	400	10000	VITROPERM 500Z	7	13	91	40	10	78	26	3	3	1.48	1.50	437.09	1.06	0.59	0.90	1.46	2.34	3.81	88.94	0.34	55.91	69.91	0.47	0.49	126.31
	400	100	400	10000	VITROPERM 500Z	9	15	135	30	20	53	17	3	4	1.71	1.73	437.09	0.80	0.53	0.89	2.28	2.96	5.24	88.69	0.21	88.13	75.01	0.43	0.61	163.75
	500	100	400	10000	VITROPERM 500Z	9	17	153	50	10	49	24	2	5	1.91	1.93	437.09	0.64	0.65	0.85	2.76	2.46	5.22	89.86	0.29	114.57	85.06	0.44	0.76	200.38
	600	100	400	10000	VITROPERM 500Z	9	17	153	50	20	47	23	2	6	2.09	2.11	437.09	0.53	0.71	0.89	3.32	3.15	6.47	85.75	0.16	129.25	100.01	0.47	0.91	230.18
	700	100	400	10000	VITROPERM 500Z	9	15	135	60	30	53	26	2	7	2.26	2.28	437.09	0.45	0.94	0.89	3.62	4.33	7.94	86.85	0.12	139.97	126.52	0.55	1.08	267.56
	800	100	400	10000	VITROPERM 500Z	9	17	153	60	40	47	23	2	8	2.41	2.43	437.09	0.40	0.95	0.89	4.45	5.10	9.55	87.87	0.09	173.32	138.33	0.57	1.33	312.99
	900	100	400	10000	VITROPERM 500Z	9	19	171	60	50	42	21	2	9	2.56	2.58	437.09	0.35	0.94	0.89	5.40	5.89	11.29	89.96	0.07	210.12	149.09	0.57	1.62	360.83
	1000	100	400	10000	VITROPERM 500Z	11	17	187	100	20	38	38	1	9	2.56	2.58	485.66	0.32	0.92	0.90	6.66	3.11	9.77	88.85	0.10	254.92	116.80	0.45	1.60	373.32
	1100	100	400	10000	VITROPERM 500Z	11	19	209	100	20	36	36	1	10	2.70	2.72	480.80	0.29	1.03	0.85	6.83	3.53	10.36	89.76	0.10	284.91	131.35	0.48	1.74	417.99
	1200	100	400	10000	VITROPERM 500Z	11	19	209	100	30	34	34	1	11	2.83	2.85	476.83	0.27	0.99	0.90	7.97	3.74	11.71	87.10	0.07	304.97	137.47	0.48	1.91	444.35
	1300	100	400	10000	VITROPERM 500Z	13	17	221	100	30	33	33	1	12	2.96	2.98	473.52	0.24	1.08	0.87	8.31	4.05	12.37	89.11	0.08	330.97	146.57	0.49	1.85	479.40
	1400	100	400	10000	VITROPERM 500Z	13	19	247	90	40	29	29	1	13	3.08	3.10	470.71	0.23	0.99	0.89	9.55	4.16	13.71	88.11	0.06	369.91	148.20	0.47	2.03	520.14
	1500	100	400	10000	VITROPERM 500Z	13	19	247	100	40	30	30	1	14	3.19	3.21	468.31	0.21	1.15	0.86	9.66	4.74	14.40	88.52	0.06	393.62	166.11	0.51	2.18	561.90
	1600	100	400	10000	VITROPERM 500Z	13	19	247	100	50	29	29	1	15	3.31	3.33	466.23	0.20	1.14	0.89	10.77	5.03	15.80	88.68	0.05	417.33	173.04	0.52	2.36	592.73
	1700	100	400	10000	VITROPERM 500Z	15	17	255	100	50	29	29	1	16	3.41	3.43	464.41	0.19	1.26	0.86	10.84	5.49	16.33	89.98	0.05	440.64	185.60	0.54	2.29	628.53
	1800	100	400	10000	VITROPERM 500Z	15	17	255	100	70	28	28	1	17	3.52	3.54	462.80	0.18	1.22	0.89	12.70	5.77	18.46	89.10	0.04	489.60	191.43	0.54	2.63	683.66
	1900	100	400	10000	VITROPERM 500Z	15	17	255	100	80	28	28	1	17	3.52	3.54	488.51	0.17	1.29	0.89	13.33	6.43	19.76	89.98	0.03	514.08	191.43	0.54	2.81	708.32
	2000	100	400	10000	VITROPERM 500Z	15	19	285	100	80	27	27	1	18	3.62	3.64	485.66	0.16	1.43	0.83	13.32	7.02	20.34	88.94	0.04	574.56	206.43	0.56	3.02	784.01
Sweep f	200	100	400	2512	VITROPERM 500Z	17	19	323	30	10	88	17	5	1	1.70	1.72	219.58	6.34	0.42	0.89	0.78	1.56	2.33	51.37	0.68	229.46	191.70	1.11	0.67	421.83
	200	100	400	3981	VITROPERM 500Z	11	17	187	30	10	96	19	5	1	1.35	1.37	348.02	4.00	0.48	0.89	0.75	2.11	2.86	65.33	0.47	111.30	103.52	0.76	0.54	215.37
	200	100	400	6310	VITROPERM 500Z	9	17	153	30	10	74	18	4	2	1.52	1.54	275.79	2.52	0.36	0.89	1.14	1.36	2.50	63.15	0.46	85.19	92.50	0.60	0.52	178.21
	200	100	400	10000	VITROPERM 500Z	7	17	119	20	10	60	15	4	2	1.21	1.23	437.09	1.59	0.29	0.89	1.30	1.54	2.84	81.73	0.35	50.27	41.79	0.34	0.37	92.43
	200	100	400	15849	VITROPERM 500Z	7	9	63	30	10	71	23	3	3	1.17	1.19	461.83	1.00	0.34	0.90	1.68	1.20	2.88	88.15	0.27	32.66	32.13	0.27	0.30	65.09
	200	100	400	25119	VITROPERM 500Z	5	7	35	50	20	81	40	2	5	1.20	1.22	439.17	0.63	0.38	0.89	2.79	0.82	3.61	86.66	0.10	26.88	28.19	0.23	0.41	55.47
	200	100	400	39811	VITROPERM 500Z	5	7	35	60	20	86	43	2	8	1.21	1.23	435.02	0.40	0.72	0.53	2.90	1.10	4.00	88.39	0.09	30.24	30.25	0.25	0.46	60.95
	200	100	400	63096	VITROPERM 500Z	5	9	45	50	20	83	41	2	12	1.18	1.20	459.64	0.25	1.46	0.27	2.37	1.61	3.98	86.37	0.09	34.56	30.66	0.26	0.49	65.70
	200	100	400	100000	T	5	11	55	40	20	69	34	2	18	1.14	1.16	485.66	0.16	2.00	0.17	1.89	2.08	3.96	86.65	0.09	36.96	26.50	0.23	0.49	63.96
	200	100	400	158489	3C96	5	7	35	100	10	82	82	1	29	1.15	1.17	477.75	0.10	2.83	0.14	2.87	0.93	3.80	89.88	0.09	40.32	22.31	0.19	0.61	63.24
	200	100	400	251189	MLX6A	5	7	35	80	20	66	66	1	45	1.14	1.16	487.97	0.06	2.93	0.11	2.98	1.00	3.97	81.03	0.04	36.96	17.55	0.15	0.57	55.08
	200	100	400	398107	MLX6A	5	5	25	80	20	66	66	1	72	1.15	1.17	483.36	0.04	3.33	0.10	2.76	1.19	3.95	88.81	0.04	26.40	15.29	0.13	0.46	42.14
	200	100	400	630957	DMR51	3	9	27	70	20	59	59	1	113	1.14	1.16	488.12	0.03	4.51	0.06	2.13	1.78	3.90	89.58	0.04	24.88	15.69	0.14	0.55	41.12
	200	100	400	1000000	3F46	3	5	15	70	30	59	59	1	179	1.14	1.16	488.37	0.02	3.84	0.07	1.73	1.91	3.63	89.70	0.03	15.26	11.35	0.10	0.40	27.01

Table G.3: Detailed simulation results of the tank inductor weight studies, corresponding to Fig. 5-3.

Transformer

Detailed simulation results for transformer sizing are shown in Table. G.4. Here we explain some of the trends in the data. More detailed graphs are provided in Fig. G-2 to Fig. G-5.

Core weight percentage: the core accounts for $\sim$ 50% of the total weight across all designs (see Fig. G-2b to Fig. G-5b). The copper in the wire and the insulation (including wire jacket and the insulation between core and windings) accounts for the remaining $\sim$ 50%. This is because the core ($\sim 5\,\mathrm{g/cm^3}$) has a smaller density compared with copper ($\sim 9\,\mathrm{g/cm^3}$)[5], naturally the weight optimized designs would yield to a bigger core and fewer windings.

Inefficient use of the secondary wire: for high voltage transformer, the current density in the secondary wire is usually smaller than a general rule-of-thumb $500\,\mathrm{A/cm^3}$ (see Fig. G-2d to Fig. G-4d), especially in the cases of low power, and/or high output voltage, and/or low frequency. This is because the litz wire diameter is set by the maximum of either twice the skin depth or the minimal available litz wire. At low power and high voltage, the secondary current is small and even the smallest available litz wire is more area than needed to carry the required current. This is worse at low frequency where the litz size is set to twice the skin depth, which is bigger than the minimal available litz size.

Core loss percentage: most designs in our investigation are core loss dominated. This is a compounded effect of the above two observation: bigger core contribute to higher core loss, and the inefficient use of winding makes the core loss dominate. Comparing Fig. G-4c to Fig. G-4d, Fig. G-3c to Fig. G-3d, and Fig. G-2c to Fig. G-2d., we can see high core loss percentage usually corresponds to less current density of the secondary wire.

Magnetizing impedance ratio is calculated with the equation (G.1)[6]. It is less intuitive to see any trends therefore we give one example: in Fig. G-4e, the increase

[5]The density of the insulation (assumed to be TEFLON) is $\sim 2\,\mathrm{g/cm^3}$.

[6]Please note that this does not mean the ratio linearly increases with f and P_o and goes reversely with V_{pri}^2 because for each design, N_p, A_c and l_c are different.

in P_o does not results in a big increase in A_c, l_c and N_p (because we fix V_{pri} and increase the current, which means the core does not change much and only the primary wire gets thicker), therefore the ratio increases roughly linearly with P_o. We show the ratio plots here to emphasize that the "limiting the magnetizing impedance may sacrifice the achievable weight": suppose we limit this ratio to a fixed number, then at lower power (smaller P_o), we need a significantly larger core (bigger A_c) (which may not be necessary if we can get away with using the small magnetizing impedance in the circuit operation.).

$$\frac{\omega L_c}{R} = \frac{2\pi f \frac{\mu_0 \mu_r A_c N_p^2}{l_c}}{\frac{V_{pri}^2}{2P_o}} = 4\pi \mu_0 \mu_r \frac{A_c N_p^2}{l_c} \frac{f P_o}{V_{pri}^2} \tag{G.1}$$

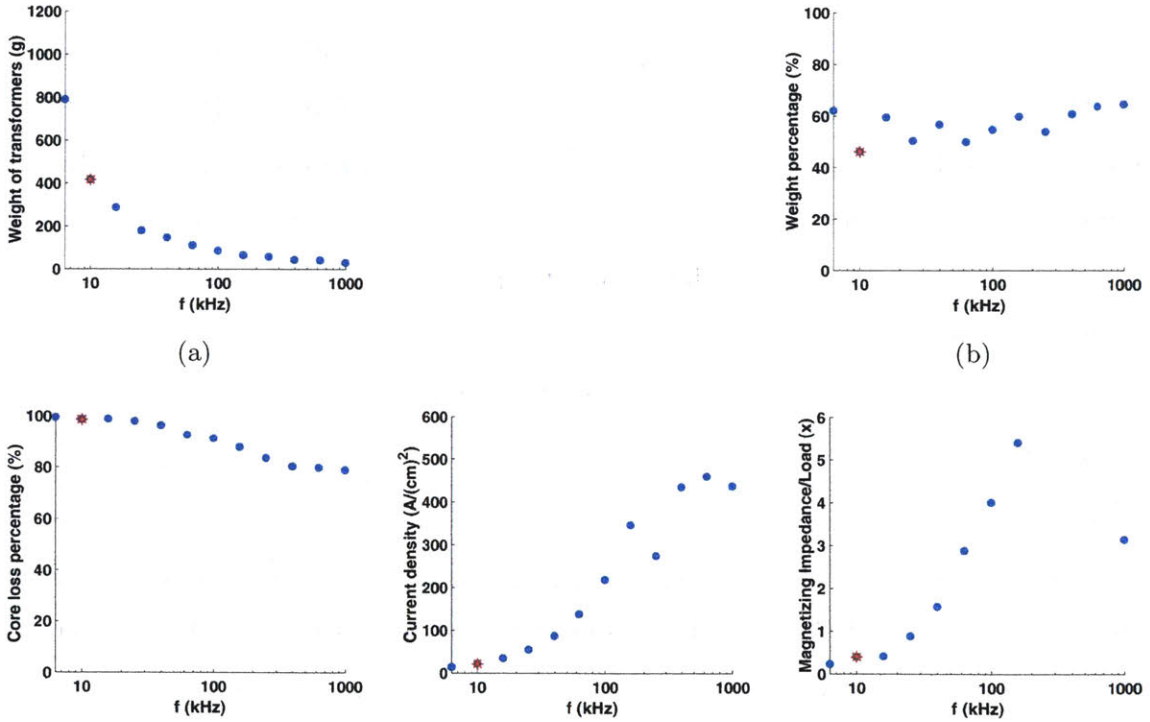


Figure G-2: Correspond to Fig. 5-4a, several features of transformers changing with f with the other 3 parameters fixed at (marked by red asterisk): $V_{pri} = 400\,\mathrm{V}$, $V_o = 4\,\mathrm{kV}$, $f = 10\,\mathrm{kHz}$, $P_o = 200\,\mathrm{W}$. (a) total weight. (b) core weight as a percentage of total weight. (c) core loss as a percentage of total loss. (d) current density of the secondary wire. (e) magnetizing impedance as a ratio of load resistance reflected to the primary.

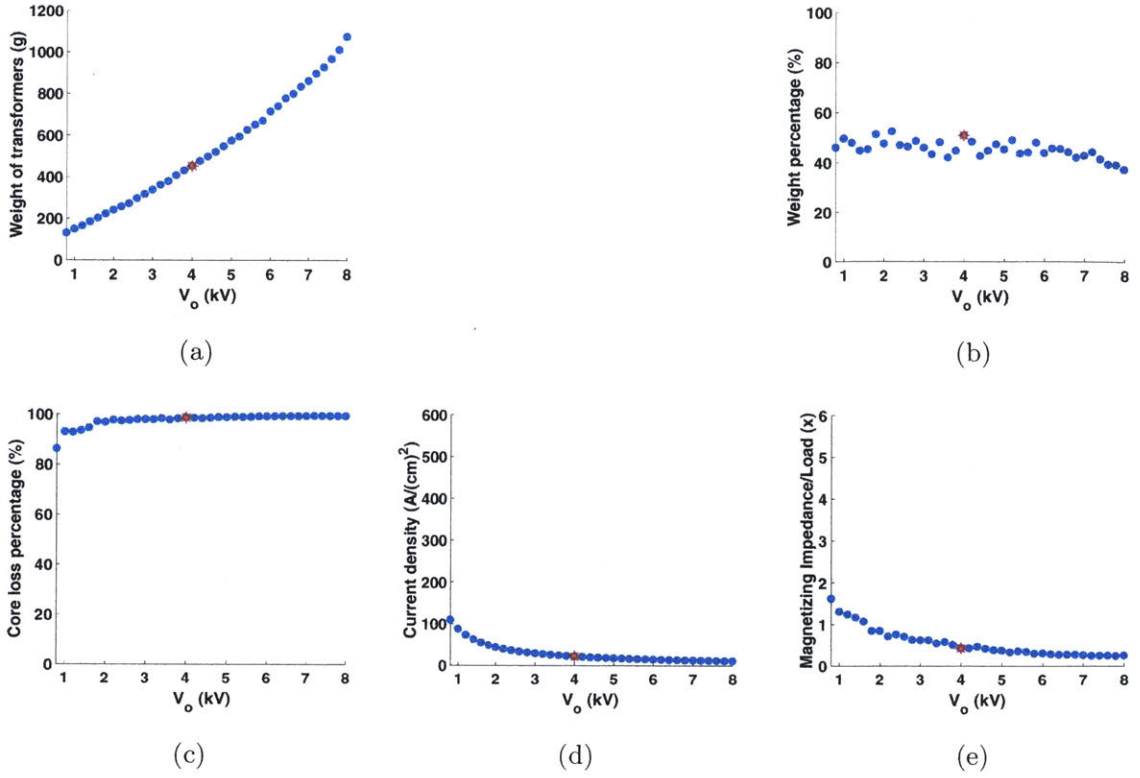


Figure G-3: Correspond to Fig. 5-4b, several features of transformers changing vs

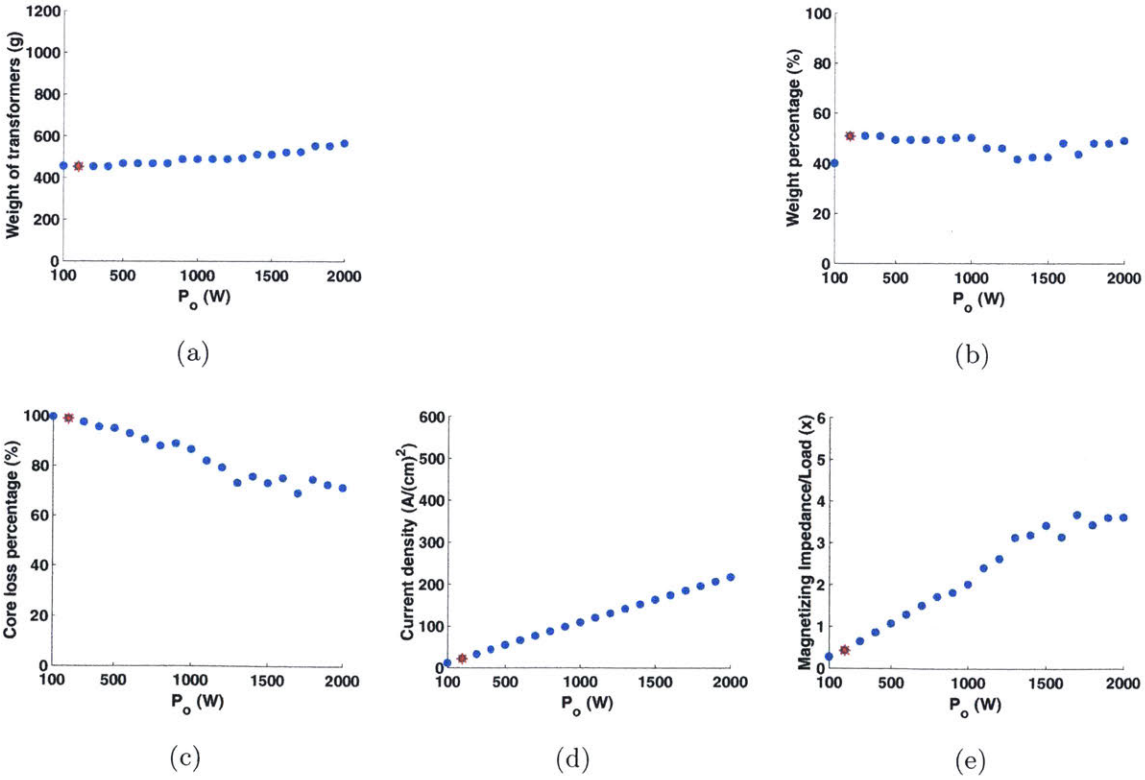


Figure G-4: Correspond to Fig. 5-4c, several features of transformers changing vs P_o.

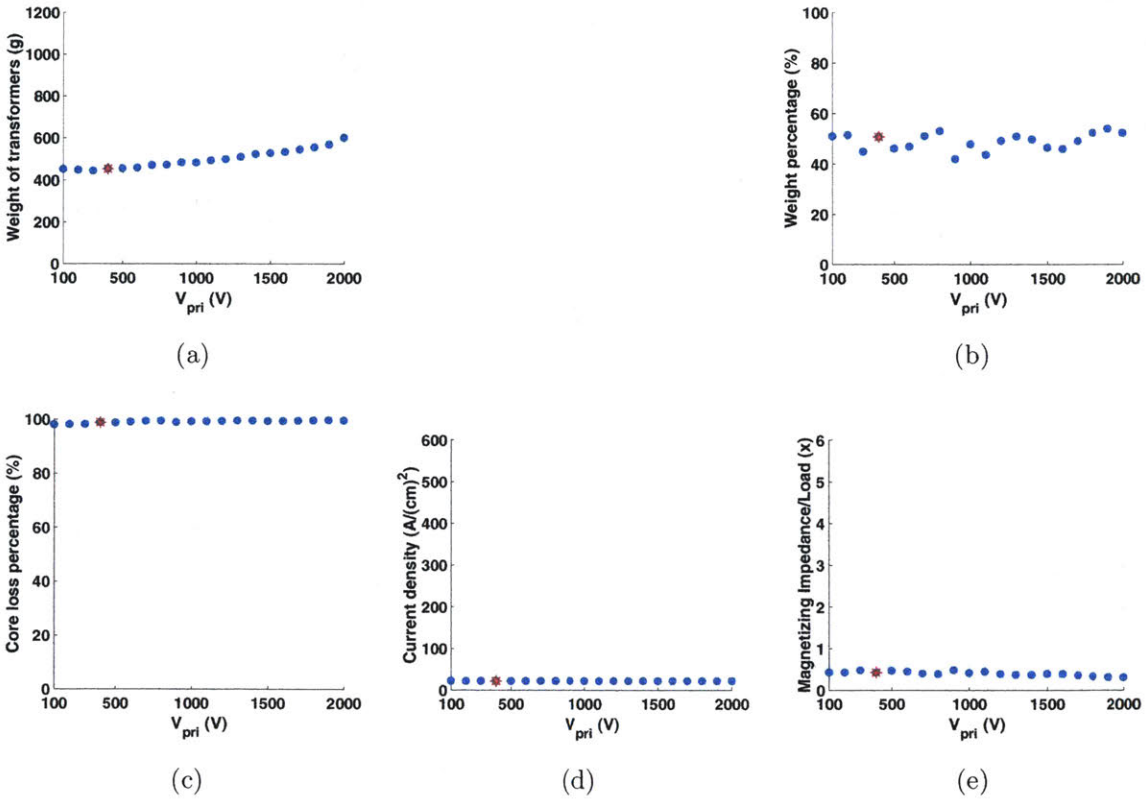


Figure G-5: Correspond to Fig. 5-4d, several features of transformers changing vs V_{pri}.

	Operating condition				Core						Winding pattern				Current density (A/cm2)		Magnetizing Inductance (mH)	Bmax (T)	Overall Packing Factor	Loss (W)			Max Temperature (C)	Weight (g)						
											Primary		Secondary											Primary			Secondary			
	Po (W)	Vpri (V)	Vo (V)	fs (Hz)	Material	Center-Leg Width (mm)	Thickness (mm)	Ac (mm2)	Window Height (mm)	Window Width (mm)	Number of turns	Number of layers	Number of turns	Number of layers	Primary	Secondary				Core	Copper	Total		Core	Copper	Insulation	Copper	Insulation	Core Insulation	Total
Sweep Vpri	200	100	4000	10000	VITROPERM 500Z	15	20	300	35	15	6	1	241	9	460	22	0.17	0.88	0.30	5.90	0.12	6.02	80.85	230.4	4.8	0.0	162.2	46.1	8.4	452.0
	200	200	4000	10000	VITROPERM 500Z	15	20	300	35	15	12	1	241	9	460	22	0.68	0.88	0.30	5.90	0.11	6.01	80.80	230.4	4.7	0.1	158.9	45.2	8.4	447.7
	200	300	4000	10000	VITROPERM 500Z	14	19	266	35	15	20	1	268	10	307	22	1.71	0.90	0.34	5.22	0.10	5.31	76.76	199.2	7.5	0.3	178.3	50.7	8.0	443.9
	200	400	4000	10000	VITROPERM 500Z	15	20	300	35	15	24	1	241	9	230	22	2.71	0.88	0.31	5.90	0.07	5.97	80.41	230.4	9.5	0.5	159.3	45.3	8.4	453.3
	200	500	4000	10000	VITROPERM 500Z	14	20	280	35	15	32	1	257	10	184	22	4.62	0.89	0.35	5.41	0.07	5.48	77.26	209.7	12.3	0.7	174.1	49.5	8.3	454.5
	200	600	4000	10000	VITROPERM 500Z	13	20	260	45	15	41	1	274	8	153	22	6.39	0.90	0.30	5.61	0.06	5.66	75.28	214.7	15.4	1.1	168.9	48.0	9.6	457.7
	200	700	4000	10000	VITROPERM 500Z	13	20	260	60	10	48	1	275	6	131	22	7.84	0.89	0.34	6.23	0.04	6.27	83.39	239.6	18.0	1.6	155.6	44.2	10.9	470.0
	200	800	4000	10000	VITROPERM 500Z	14	20	280	55	10	51	1	256	6	115	22	9.84	0.89	0.36	6.48	0.04	6.52	86.06	250.0	19.7	2.0	147.7	42.0	10.4	471.7
	200	900	4000	10000	VITROPERM 500Z	13	20	260	40	15	62	2	277	9	102	22	15.51	0.89	0.37	5.22	0.06	5.27	74.13	202.2	24.6	2.8	190.3	54.1	8.9	482.8
	200	1000	4000	10000	VITROPERM 500Z	15	20	300	35	15	59	2	237	9	92	22	16.40	0.90	0.38	6.05	0.05	6.10	81.61	230.4	24.7	3.2	168.1	47.8	8.4	482.5
	200	1100	4000	10000	VITROPERM 500Z	13	20	260	45	15	75	2	274	8	84	22	21.37	0.90	0.35	5.62	0.05	5.67	75.37	214.7	29.9	4.3	182.1	51.7	9.6	492.3
	200	1200	4000	10000	VITROPERM 500Z	15	20	300	40	15	71	2	238	8	77	22	22.36	0.90	0.36	6.40	0.04	6.44	81.64	244.8	29.8	4.7	163.4	46.4	9.2	498.4
	200	1300	4000	10000	VITROPERM 500Z	15	20	300	45	15	77	2	238	7	71	22	24.84	0.90	0.33	6.77	0.03	6.80	82.02	259.2	32.4	5.6	157.7	44.8	10.0	509.7
	200	1400	4000	10000	VITROPERM 500Z	15	19	285	50	15	87	2	250	7	66	22	28.53	0.90	0.32	6.82	0.03	6.85	81.21	259.9	35.8	6.7	163.5	46.5	10.5	522.9
	200	1500	4000	10000	VITROPERM 500Z	15	20	300	40	15	89	3	238	8	61	22	35.13	0.89	0.40	6.38	0.04	6.42	81.42	244.8	39.7	8.1	175.9	50.0	9.2	527.6
	200	1600	4000	10000	VITROPERM 500Z	15	20	300	40	15	95	3	239	8	58	22	40.03	0.89	0.42	6.37	0.04	6.41	81.36	244.8	42.5	9.3	177.2	50.3	9.2	533.4
	200	1700	4000	10000	VITROPERM 500Z	16	20	320	40	15	94	3	222	8	54	22	40.84	0.90	0.40	7.02	0.04	7.06	85.48	267.3	43.1	10.1	167.4	47.6	9.4	544.9
	200	1800	4000	10000	VITROPERM 500Z	17	20	340	40	15	94	3	210	7	51	22	42.42	0.90	0.40	7.59	0.03	7.63	88.73	290.5	44.2	11.1	155.6	44.2	9.6	555.3
	200	1900	4000	10000	VITROPERM 500Z	17	20	340	45	15	99	3	209	6	48	22	44.55	0.90	0.37	8.05	0.03	8.07	89.34	306.8	46.7	12.5	150.0	42.6	10.5	569.1
	200	2000	4000	10000	VITROPERM 500Z	18	20	360	35	20	99	4	199	8	46	22	48.72	0.89	0.35	8.18	0.04	8.22	88.02	314.5	50.4	14.3	165.8	47.1	10.0	602.1
Sweep Vo	200	400	800	10000	VITROPERM 500Z	8	19	152	15	10	47	3	95	7	230	109	10.29	0.89	0.43	1.55	0.25	1.80	61.48	59.8	15.9	0.8	50.5	2.4	0.7	130.1
	200	400	1000	10000	VITROPERM 500Z	10	14	140	25	10	51	2	129	5	230	87	8.32	0.89	0.32	1.92	0.15	2.06	60.20	73.9	14.7	0.7	55.3	3.4	1.0	149.0
	200	400	1200	10000	VITROPERM 500Z	9	19	171	20	10	42	2	127	7	230	73	7.90	0.89	0.38	2.03	0.16	2.18	62.60	78.8	13.9	0.7	65.2	4.8	1.3	164.6
	200	400	1400	10000	VITROPERM 500Z	9	18	162	25	10	44	2	155	7	230	62	7.44	0.89	0.36	2.14	0.15	2.29	61.86	82.4	14.1	0.7	78.6	6.9	1.7	184.4
	200	400	1600	10000	VITROPERM 500Z	9	20	180	25	10	40	2	161	7	230	55	6.83	0.88	0.37	2.35	0.13	2.48	63.21	91.6	13.7	0.7	85.7	8.6	2.1	202.3
	200	400	1800	10000	VITROPERM 500Z	10	17	170	40	10	42	1	190	5	230	49	5.38	0.89	0.27	2.96	0.09	3.05	64.81	114.2	12.7	0.6	82.8	9.5	2.9	222.8
	200	400	2000	10000	VITROPERM 500Z	10	17	170	40	10	42	1	211	6	230	44	5.38	0.89	0.30	2.96	0.10	3.06	64.88	114.2	12.8	0.6	97.3	12.5	3.3	240.7
	200	400	2200	10000	VITROPERM 500Z	11	19	209	35	10	34	1	188	6	230	40	4.53	0.90	0.31	3.51	0.08	3.59	70.49	134.4	11.4	0.5	93.2	13.3	3.6	256.6
	200	400	2400	10000	VITROPERM 500Z	11	18	198	35	10	36	1	217	7	230	36	4.81	0.89	0.36	3.31	0.09	3.40	69.01	127.4	11.7	0.6	111.1	17.5	3.8	272.1
	200	400	2600	10000	VITROPERM 500Z	11	18	198	40	10	36	1	235	7	230	34	4.48	0.89	0.35	3.56	0.09	3.65	69.69	136.9	11.8	0.6	121.4	20.9	4.6	296.1
	200	400	2800	10000	VITROPERM 500Z	12	18	216	40	10	33	1	232	7	230	31	3.99	0.89	0.35	3.99	0.08	4.07	73.17	153.4	11.2	0.5	123.3	23.1	5.0	316.6
	200	400	3000	10000	VITROPERM 500Z	11	19	209	45	10	34	1	256	7	230	29	3.94	0.90	0.35	4.04	0.08	4.12	72.07	154.5	11.5	0.6	137.2	27.8	6.0	337.6
	200	400	3200	10000	VITROPERM 500Z	11	18	198	50	10	36	1	289	7	230	27	3.93	0.89	0.36	4.05	0.08	4.13	71.31	155.9	11.9	0.6	153.2	33.5	6.7	361.7
	200	400	3400	10000	VITROPERM 500Z	12	20	240	45	10	30	1	256	7	230	26	3.44	0.88	0.36	4.66	0.07	4.73	76.19	182.0	10.8	0.5	144.7	34.0	7.2	379.3
	200	400	3600	10000	VITROPERM 500Z	12	20	240	35	15	30	1	271	10	230	24	3.67	0.88	0.34	4.37	0.09	4.46	70.30	170.5	10.9	0.5	174.7	43.8	7.1	407.5
	200	400	3800	10000	VITROPERM 500Z	13	19	247	40	15	29	1	277	9	230	23	3.22	0.89	0.31	4.96	0.08	5.04	72.92	192.1	10.5	0.5	173.1	46.3	8.1	430.6
	200	400	4000	10000	VITROPERM 500Z	15	20	300	35	15	24	1	241	9	230	22	2.71	0.88	0.31	5.90	0.07	5.97	80.41	230.4	9.5	0.5	159.3	45.3	8.4	453.3
	200	400	4200	10000	VITROPERM 500Z	15	20	300	35	15	24	1	253	10	230	21	2.71	0.88	0.34	5.90	0.08	5.98	80.46	230.4	9.5	0.5	175.2	52.8	8.9	477.2
	200	400	4400	10000	VITROPERM 500Z	14	19	266	40	15	27	1	298	10	230	20	2.94	0.89	0.36	5.45	0.08	5.53	76.03	211.9	10.1	0.5	202.0	64.3	9.6	498.5
	200	400	4600	10000	VITROPERM 500Z	15	19	285	40	15	25	1	289	10	230	19	2.63	0.89	0.35	6.05	0.07	6.12	79.98	232.6	9.7	0.5	200.5	67.4	10.3	520.8
	200	400	4800	10000	VITROPERM 500Z	15	20	300	45	15	24	1	289	9	230	18	2.41	0.88	0.32	6.64	0.07	6.70	81.20	259.2	9.5	0.5	197.2	69.8	12.0	548.2
	200	400	5000	10000	VITROPERM 500Z	15	19	285	50	15	25	1	314	9	230	17	2.36	0.89	0.32	6.76	0.07	6.83	81.00	259.9	9.7	0.5	212.7	79.1	13.1	575.0
	200	400	5200	10000	VITROPERM 500Z	17	19	323	45	15	22	1	287	9	230	17	2.09	0.90	0.34	7.61	0.06	7.67	87.43	291.5	9.0	0.4	201.8	78.8	13.1	594.7
	200	400	5400	10000	VITROPERM 500Z	15	19	285	55	15	25	1	339	9	230	16	2.24	0.89	0.33	7.12	0.07	7.18	81.68	273.6	9.7	0.5	233.3	95.4	15.1	627.6
	200	400	5600	10000	VITROPERM 500Z	15	20	300	55	15	24	1	337	9	230	16	2.17	0.88	0.34	7.38	0.06	7.44	82.49	288.0	9.6	0.5	237.1	101.5	16.3	653.0
	200	400	5800	10000	VITROPERM 500Z	17	20	340	50	15	21	1	306	9	230	15	1.90	0.89	0.35	8.38	0.06	8.44	89.43	323.1	8.9	0.4	223.2	99.8	16.4	671.8
	200	400	6000	10000	VITROPERM 500Z	15	19	285	70	15	25	1	376	8	230	15	1.95	0.89	0.31	8.19	0.06	8.25	84.01	314.6	9.8	0.5	253.5	118.3	20.3	717.0
	200	400	6200	10000	VITROPERM 500Z	17	20	340	50	20	21	1	327	10	230	14	1.81	0.89	0.29	8.80	0.06	8.86	85.24	339.5	8.9	0.4	251.9	122.5	19.0	742.3
	200	400	6400	10000	VITROPERM 500Z	17	20	340	55	20	21	1	337	10	230	14	1.73	0.89	0.28	9.23	0.06	9.29	85.72	355.8	8.9	0.4	261.5	132.4	21.0	780.1
	200	400	6600	10000	VITROPERM 500Z	17	20	340	55	20	21	1	348	10	230	13	1.73	0.89	0.30	9.23	0.06	9.29	85.72	355.8	8.9	0.4	272.1	143.3	21.6	802.2
	200	400	6800	10000	VITROPERM 500Z	17	19	323	60	20	22	1	375	10	230	13	1.72	0.90	0.30	9.23	0.06	9.29	84.90	353.5	9.2	0.4	291.5	159.5	22.9	837.0
	200	400	7000	10000	VITROPERM 500Z	17	20	340	60	20	21	1	369	10	230	12	1.65	0.89	0.30	9.65	0.06	9.71	86.28	372.1	9.0	0.4	292.7	166.3	24.4	864.9
	200	400	7200	10000	VITROPERM 500Z	18	20	360	60	20	20	1	361	10	230	12	1.56	0.88	0.30	10.27	0.06	10.32	88.68	400.9	8.8	0.4	292.2	172.1	25.6	900.0
	200	400	7400	10000	VITROPERM 500Z	17	20	340	65	20	21	1	390	10	230	12	1.58	0.89	0.31	10.07	0.06	10.13	86.91	388.4	9.0	0.4	313.9	191.6	27.3	930.7
	200	400	7600	10000	VITROPERM 500Z	17	19	323	70	20	22	1	419	10	230	12	1.58	0.90	0.32	10.04	0.06	10.10	86.17	384.5	9.2	0.4	335.3	212.0	28.7	970.1
	200	400	7800	10000	VITROPERM 500Z	17	19	323	75	20	22	1	430	10	230	11	1.52	0.90	0.31	10.45	0.06	10.51	86.86	400.0	9.2	0.4	346.6	226.7	31.0	1013.9
	200	400	8000	10000	VITROPERM 500Z	16	20	320	80	20	23	1	461	10	230	11	1.61	0.86	0.32	10.05	0.06	10.11	83.21	405.5	9.7	0.5	374.2	253.0	33.8	1076.7

(a)

Table G.4: Detailed simulation results of the transformer weight studies, corresponding to Fig. 5-4.

	Operating condition				Core						Winding pattern				Current density (A/cm2)		Magnetizing Inductance (mH)	Bmax (T)	Overall Packing Factor	Loss (W)			Max Temperature (C)	Weight (g)						
											Primary		Secondary												Primary			Secondary			
	Po (W)	Vpri (V)	Vo (V)	fs (Hz)	Material	Center-Leg Width (mm)	Thickness (mm)	Ac (mm2)	Window Height (mm)	Window Width (mm)	Number of turns	Number of layers	Number of turns	Number of layers	Primary	Secondary				Core	Copper	Total		Core	Copper	Insulation	Copper	Insulation	Core insulation	Total
Sweep Po	100	400	4000	10000	VITROPERM 500Z	12	20	240	40	15	30	1	301	10	115	11	3.44	0.88	0.34	4.66	0.02	4.68	70.07	182.0	10.9	0.5	197.5	56.1	8.7	455.7
	200	400	4000	10000	VITROPERM 500Z	15	20	300	35	15	24	1	241	9	230	22	2.71	0.88	0.31	5.90	0.07	5.97	80.41	230.4	9.5	0.5	159.3	45.3	8.4	453.3
	300	400	4000	10000	VITROPERM 500Z	15	20	300	35	15	24	1	241	9	345	33	2.71	0.88	0.31	5.90	0.16	6.06	81.22	230.4	9.5	0.5	159.3	45.3	8.4	453.3
	400	400	4000	10000	VITROPERM 500Z	15	20	300	35	15	24	1	241	9	460	44	2.71	0.88	0.31	5.90	0.28	6.18	82.36	230.4	9.5	0.5	159.3	45.3	8.4	453.3
	500	400	4000	10000	VITROPERM 500Z	15	20	300	35	15	24	1	241	9	288	55	2.71	0.88	0.34	5.90	0.32	6.22	82.71	230.4	19.3	0.6	162.8	46.3	8.4	467.8
	600	400	4000	10000	VITROPERM 500Z	15	20	300	35	15	24	1	241	9	345	66	2.71	0.88	0.34	5.90	0.46	6.36	84.00	230.4	19.3	0.6	162.8	46.3	8.4	467.8
	700	400	4000	10000	VITROPERM 500Z	15	20	300	35	15	24	1	241	9	403	76	2.71	0.88	0.34	5.90	0.62	6.52	85.54	230.4	19.3	0.6	162.8	46.3	8.4	467.8
	800	400	4000	10000	VITROPERM 500Z	15	20	300	35	15	24	1	241	9	460	87	2.71	0.88	0.34	5.90	0.81	6.71	87.30	230.4	19.3	0.6	162.8	46.3	8.4	467.8
	900	400	4000	10000	VITROPERM 500Z	15	20	300	40	15	24	1	241	8	345	98	2.55	0.88	0.32	6.27	0.79	7.06	87.06	244.8	29.3	0.8	159.3	45.3	9.2	488.7
	1000	400	4000	10000	VITROPERM 500Z	15	20	300	40	15	24	1	241	8	383	109	2.55	0.88	0.32	6.27	0.97	7.24	88.69	244.8	29.3	0.8	159.3	45.3	9.2	488.7
	1100	400	4000	10000	VITROPERM 500Z	14	19	266	45	15	27	1	271	8	422	120	2.77	0.89	0.32	5.78	1.28	7.05	87.06	224.7	31.3	0.9	173.6	49.3	9.5	489.2
	1200	400	4000	10000	VITROPERM 500Z	14	19	266	45	15	27	1	271	8	460	131	2.77	0.89	0.32	5.78	1.52	7.29	89.19	224.7	31.3	0.9	173.6	49.3	9.5	489.2
	1300	400	4000	10000	VITROPERM 500Z	12	20	240	50	15	30	1	301	8	498	142	3.05	0.88	0.32	5.25	1.94	7.19	88.21	205.1	33.9	0.9	189.7	53.9	10.1	493.6
	1400	400	4000	10000	VITROPERM 500Z	12	20	240	55	15	30	1	301	7	403	153	2.89	0.88	0.32	5.55	1.80	7.34	87.12	216.6	45.7	1.1	184.8	52.5	10.9	511.5
	1500	400	4000	10000	VITROPERM 500Z	12	20	240	55	15	30	1	301	7	431	164	2.89	0.88	0.32	5.55	2.06	7.61	89.37	216.6	45.7	1.1	184.8	52.5	10.9	511.5
	1600	400	4000	10000	VITROPERM 500Z	14	19	266	50	20	27	1	271	7	460	175	2.49	0.89	0.23	6.43	2.16	8.59	89.47	250.3	42.3	1.0	169.1	48.1	11.1	521.8
	1700	400	4000	10000	VITROPERM 500Z	12	20	240	55	20	30	1	301	7	489	186	2.74	0.88	0.24	5.84	2.65	8.49	88.93	228.1	45.7	1.1	184.8	52.5	11.8	524.0
	1800	400	4000	10000	VITROPERM 500Z	13	20	260	60	20	28	1	281	6	414	197	2.42	0.87	0.22	6.66	2.30	8.97	88.09	264.6	55.4	1.2	170.5	48.4	12.8	552.8
	1900	400	4000	10000	VITROPERM 500Z	13	20	260	60	20	28	1	281	6	437	208	2.42	0.87	0.22	6.66	2.57	9.23	89.94	264.6	55.4	1.2	170.5	48.4	12.8	552.8
	2000	400	4000	10000	VITROPERM 500Z	13	20	260	60	25	28	1	281	6	460	219	2.31	0.87	0.17	6.98	2.84	9.82	88.13	277.1	55.4	1.2	170.5	48.4	13.7	566.2
Sweep f	200	400	4000	7943	VITROPERM 500Z	14	20	280	50	20	32	1	321	9	183	17	3.68	0.89	0.26	4.99	0.07	5.06	62.22	263.4	15.6	0.7	272.5	67.6	11.5	631.2
	200	400	4000	10000	VITROPERM 500Z	13	20	260	60	10	28	1	281	6	230	22	2.67	0.87	0.32	6.04	0.06	6.10	81.81	239.6	10.5	0.5	158.3	45.0	10.9	464.9
	200	400	4000	15849	VITROPERM 500Z	10	16	160	40	20	28	1	281	8	365	35	1.97	0.90	0.18	6.31	0.09	6.40	89.61	122.9	5.3	0.3	89.9	33.7	7.7	259.9
	200	400	4000	31623	VITROPERM 500Z	5	12	60	50	20	49	1	491	9	364	69	2.26	0.68	0.17	4.53	0.18	4.71	89.64	46.1	6.4	0.4	62.2	36.1	6.1	157.2
	200	400	4000	63096	VITROPERM 500Z	5	12	60	40	20	49	1	491	10	484	138	2.59	0.34	0.15	3.96	0.35	4.31	89.68	40.3	4.8	0.3	30.0	27.6	5.3	108.3
	200	400	4000	125893	T	5	16	80	30	10	39	1	391	9	483	275	3.06	0.16	0.26	2.81	0.45	3.25	89.68	38.4	4.6	0.3	12.2	18.3	4.4	78.2
	200	400	4000	251189	MLX6A	5	12	60	30	10	39	1	391	9	482	274	2.64	0.11	0.26	2.23	0.64	2.87	89.16	28.8	3.8	0.3	11.0	16.4	3.4	63.7
	200	400	4000	501187	DMR51	4	12	48	30	10	37	1	371	8	480	365	0.95	0.07	0.22	1.74	0.85	2.59	88.41	22.1	3.4	0.2	7.2	13.3	3.3	49.6
	200	400	4000	1000000	3F46	1	13	13	70	30	56	1	561	5	489	437	0.19	0.09	0.05	2.38	1.00	3.38	88.72	12.7	4.6	0.3	7.4	15.6	7.9	48.6

(b) Continued

Table G.4: Detailed simulation results of the transformer weight studies, corresponding to Fig. 5-4.

	Index	Operating parameters					Transformer																							
							Core				Wire								Loss (W)				Weight (g)							
		Vin(V)	Vpri (V)	Vo (V)	Po(W)	fs(Hz)	Material	Ac (mm2)	Window Height (mm)	Window Width (mm)	Pri wire Dia(mm)	Sec wire Dia(mm)	Num Of Pri turns	Pri numberof layers	Num Of Sec turns	Sec number of layers	Overall packing factor	Bmax (mT)	Core	Copper	Total	Absolute temp (C)	Core	Pri copper	Pri insu	Sec copper	Sec insu	Core insu	Total
Sweep Vin	1	100	200	4000	200	10000	VITROPERM 500Z	255	60	10	0.85	0.85	14	1	281	6	0.30	891.62	6.35	0.11	6.46	85.61	244.8	5.1	0.1	155.0	44.0	10.3	459.3
	2	150	300	4000	200	10000	VITROPERM 500Z	255	60	10	0.85	0.85	21	1	281	6	0.31	891.62	6.35	0.08	6.42	85.33	244.8	7.6	0.3	155.2	44.1	10.3	462.3
	3	200	400	4000	200	10000	VITROPERM 500Z	255	60	10	0.85	0.85	28	1	281	6	0.32	891.62	6.35	0.06	6.41	85.18	244.8	10.2	0.5	155.5	44.2	10.3	465.4
	4	250	500	4000	200	10000	VITROPERM 500Z	255	60	10	0.85	0.85	35	1	281	6	0.33	891.62	6.35	0.05	6.40	85.10	244.8	12.7	0.8	155.7	44.2	10.3	468.5
	5	300	600	4000	200	10000	VITROPERM 500Z	255	60	10	0.85	0.85	42	1	281	6	0.34	891.62	6.35	0.05	6.39	85.04	244.8	15.3	1.1	155.9	44.3	10.3	471.7
	6	350	700	4000	200	10000	VITROPERM 500Z	255	60	10	0.85	0.85	49	1	281	6	0.35	891.62	6.35	0.04	6.39	85.00	244.8	17.9	1.6	156.1	44.4	10.3	475.0
	7	400	800	4000	200	10000	VITROPERM 500Z	255	60	10	0.85	0.85	56	1	281	6	0.36	891.62	6.35	0.04	6.39	84.97	244.8	20.4	2.1	156.4	44.4	10.3	478.4
Sweep Vo	8	100	200	1000	200	10000	VITROPERM 500Z	119	30	10	0.85	0.85	30	1	151	5	0.24	891.62	1.60	0.22	1.82	55.81	61.7	8.1	0.2	58.7	3.6	1.2	133.4
	9	100	200	2000	200	10000	VITROPERM 500Z	187	30	10	0.85	0.85	19	1	191	7	0.32	895.89	2.91	0.15	3.06	68.13	111.3	6.0	0.1	93.8	12.1	2.7	226.0
	10	100	200	3000	200	10000	VITROPERM 500Z	187	50	10	0.85	0.85	19	1	286	7	0.32	895.89	3.84	0.14	3.98	70.68	147.2	6.0	0.1	146.9	29.8	6.0	336.1
	11	100	200	4000	200	10000	VITROPERM 500Z	255	60	10	0.85	0.85	14	1	281	6	0.30	891.62	6.35	0.11	6.46	85.61	244.8	5.1	0.1	155.0	44.0	10.3	459.3
	12	100	200	5000	200	10000	VITROPERM 500Z	323	40	20	0.85	0.85	11	1	276	10	0.26	895.89	7.61	0.11	7.72	83.63	291.5	4.5	0.1	199.8	74.3	12.8	583.1
	13	100	200	6000	200	10000	VITROPERM 500Z	323	60	20	0.85	0.85	11	1	331	9	0.23	895.89	9.23	0.10	9.33	85.14	353.5	4.5	0.1	239.3	111.7	20.2	729.3
	14	100	200	7000	200	10000	VITROPERM 500Z	323	70	20	0.85	0.85	11	1	386	9	0.27	895.89	10.04	0.10	10.14	86.40	384.5	4.6	0.1	289.3	164.4	26.4	869.3
	15	100	200	8000	200	10000	VITROPERM 500Z	285	90	20	0.85	0.85	13	1	521	10	0.32	859.14	9.40	0.11	9.51	79.71	383.0	5.2	0.1	411.4	278.2	35.0	1112.9
	16	100	400	9000	200	10000	VITROPERM 500Z	247	140	20	0.85	0.85	31	1	699	9	0.31	831.42	10.30	0.07	10.37	77.86	441.0	11.9	0.6	533.7	422.2	54.1	1463.5
	17	100	400	10000	200	10000	VITROPERM 500Z	323	150	30	0.85	0.85	31	1	776	10	0.24	635.79	10.37	0.08	10.45	64.42	663.6	13.3	0.6	674.5	615.5	74.6	2042.1
Sweep Po	18	200	200	4000	100	10000	VITROPERM 500Z	209	50	20	0.85	0.85	17	1	341	9	0.22	895.89	4.82	0.04	4.86	65.19	184.6	5.8	0.1	207.4	58.9	10.4	467.2
	19	200	200	4000	200	10000	VITROPERM 500Z	255	60	10	0.85	0.85	14	1	281	6	0.30	891.62	6.35	0.11	6.46	85.61	244.8	5.1	0.1	155.0	44.0	10.3	459.3
	20	200	200	4000	300	10000	VITROPERM 500Z	255	60	10	1.21	0.85	14	1	281	6	0.32	891.62	6.35	0.14	6.49	85.97	244.8	10.4	0.2	159.1	45.2	10.3	469.9
	21	200	200	4000	400	10000	VITROPERM 500Z	255	60	10	1.21	0.85	14	1	281	6	0.32	891.62	6.35	0.26	6.61	87.02	244.8	10.4	0.2	159.1	45.2	10.3	469.9
	22	200	200	4000	500	10000	VITROPERM 500Z	255	60	10	1.48	0.85	14	1	281	6	0.33	891.62	6.35	0.31	6.66	87.55	244.8	15.8	0.2	162.2	46.1	10.3	479.3
	23	200	200	4000	600	10000	VITROPERM 500Z	255	60	10	1.48	0.85	14	1	281	6	0.33	891.62	6.35	0.45	6.80	88.85	244.8	15.8	0.2	162.2	46.1	10.3	479.3
	24	200	200	4000	700	10000	VITROPERM 500Z	323	30	20	1.71	0.85	11	1	221	10	0.27	895.89	6.80	0.69	7.50	88.96	260.5	18.5	0.2	161.4	45.9	8.7	495.2
	25	200	200	4000	800	10000	VITROPERM 500Z	255	40	20	1.71	0.85	14	1	281	10	0.26	891.62	5.71	1.07	6.78	81.66	220.3	21.3	0.2	193.7	55.0	9.2	499.7
	26	200	200	4000	900	10000	VITROPERM 500Z	255	40	20	1.91	0.85	14	1	281	10	0.27	891.62	5.71	1.27	6.98	83.37	220.3	26.9	0.3	196.0	55.7	9.2	508.4
	27	200	200	4000	1000	10000	VITROPERM 500Z	255	40	20	1.91	0.85	14	1	281	10	0.27	891.62	5.71	1.57	7.28	85.86	220.3	26.9	0.3	196.0	55.7	9.2	508.4
	28	200	200	4000	1100	10000	VITROPERM 500Z	255	40	20	2.09	0.85	14	1	281	10	0.28	891.62	5.71	1.82	7.54	87.99	220.3	32.6	0.3	198.1	56.3	9.2	516.8
	29	200	200	4000	1200	10000	VITROPERM 500Z	247	40	20	2.09	0.85	15	1	301	10	0.30	859.14	5.00	2.32	7.33	87.03	203.9	34.9	0.3	212.2	60.3	9.4	521.1
Sweep f	30	100	200	4000	200	3981	VITROPERM 500Z	361	100	20	1.35	1.35	25	1	501	9	0.32	885.94	3.65	0.11	3.75	43.80	547.6	27.3	0.4	1010.2	168.4	20.7	1774.5
	31	100	200	4000	200	6310	VITROPERM 500Z	361	50	20	1.07	1.07	16	1	321	10	0.29	873.42	4.85	0.11	4.96	57.91	374.3	10.9	0.2	391.8	85.0	12.4	874.5
	32	100	200	4000	200	10000	VITROPERM 500Z	255	60	10	0.85	0.85	14	1	281	6	0.30	891.62	6.35	0.11	6.46	85.61	244.8	5.1	0.1	155.0	44.0	10.3	459.3
	33	100	200	4000	200	15849	VITROPERM 500Z	165	40	20	0.96	0.68	14	1	281	8	0.17	869.44	6.37	0.10	6.46	89.45	129.9	5.4	0.1	91.7	34.4	7.6	269.0
	34	100	200	4000	200	25119	VITROPERM 500Z	95	40	20	0.93	0.54	18	1	361	9	0.17	741.06	5.00	0.16	5.16	89.31	63.8	6.1	0.1	70.7	35.4	7.7	183.8
	35	100	200	4000	200	39811	VITROPERM 500Z	75	40	20	0.86	0.43	21	1	421	9	0.16	507.66	4.51	0.23	4.74	89.97	50.4	5.1	0.1	45.2	30.5	6.3	137.5
	36	100	200	4000	200	63096	VITROPERM 500Z	45	50	30	0.83	0.34	29	1	581	9	0.09	386.58	4.60	0.34	4.94	89.57	38.9	4.9	0.1	32.1	29.5	5.7	111.2
	37	100	200	4000	200	100000	T	85	30	10	0.93	0.27	20	1	401	10	0.29	187.24	2.88	0.47	3.35	89.95	40.8	6.3	0.1	17.5	22.1	4.6	91.4
	38	100	200	4000	200	158489	3C96	65	30	10	0.83	0.21	22	1	441	10	0.26	140.45	2.25	0.69	2.94	88.48	31.2	4.6	0.1	10.5	18.7	3.7	68.8
	39	100	200	4000	200	251189	MLX6A	55	30	10	0.83	0.24	22	1	441	10	0.28	104.73	1.84	0.91	2.75	88.68	26.4	4.2	0.1	12.8	19.1	3.2	65.8
	40	100	200	4000	200	398107	MLX6A	45	30	10	0.82	0.19	21	1	421	9	0.23	84.61	1.49	1.01	2.50	87.71	21.6	3.5	0.1	6.8	14.3	2.8	48.9
	41	100	200	4000	200	630957	DMR51	55	30	10	0.83	0.19	15	1	301	7	0.16	61.15	2.03	0.76	2.79	89.64	26.4	2.8	0.1	4.5	9.9	3.2	46.9
	42	100	200	4000	200	1000000	3F46	33	30	10	0.82	0.19	14	1	281	6	0.16	68.90	1.47	0.77	2.24	88.87	14.6	2.3	0.1	4.0	8.4	2.9	32.3

(a)

Table G.5: Detailed simulation results of the combined weight of inductor and transformer, corresponding to Fig. 5-5.

	Index	Operating parameters					Inductor																			Combined Weight (g)
							Core			Wire build and winding				L (mH)	Bmax (mT)	Overall packing factor	Loss			Absolute temp (C)	Weight (g)					
		Vin(V)	Vpri (V)	Vo (V)	Po(W)	fs(Hz)	Ac (mm2)	Window Height (mm)	Window Width (mm)	Wire Dia (mm)	Num of litz strands	Num Of turns	Num of layers				Core	Copper	Total		Core	Copper	Wire insulation	Core insulation	Total	
Sweep Vin	1	100	200	4000	200	10000	85	10	10	1.21	2	42	5	0.80	891.62	0.50	0.63	1.44	2.08	87.93	24.48	29.57	0.24	0.12	54.18	513.48
	2	150	300	4000	200	10000	91	20	10	1.21	2	59	4	1.79	889.30	0.35	0.99	0.59	1.59	60.31	38.44	36.30	0.45	0.23	74.97	537.27
	3	200	400	4000	200	10000	75	20	10	0.85	1	95	5	3.18	893.50	0.30	0.75	0.91	1.66	64.96	28.80	28.33	0.67	0.32	57.45	522.81
	4	250	500	4000	200	10000	91	20	10	0.85	1	98	5	4.97	892.32	0.31	1.00	0.61	1.60	60.65	38.44	29.36	0.87	0.38	68.18	536.69
	5	300	600	4000	200	10000	117	20	10	0.85	1	91	5	7.16	896.90	0.30	1.41	0.42	1.83	61.75	53.91	29.26	1.05	0.49	83.66	555.39
	6	350	700	4000	200	10000	135	20	10	0.85	1	92	5	9.75	897.01	0.31	1.63	0.33	1.96	62.16	62.21	31.60	1.33	0.63	94.44	569.46
	7	400	800	4000	200	10000	153	20	10	0.85	1	93	5	12.73	894.82	0.32	1.84	0.27	2.11	63.05	70.50	33.99	1.64	0.79	105.28	583.67
Sweep Vo	8	100	200	1000	200	10000	85	10	10	1.21	2	42	5	0.80	891.62	0.50	0.63	1.44	2.08	87.93	24.48	29.57	0.24	0.12	54.18	187.57
	9	100	200	2000	200	10000	85	10	10	1.21	2	42	5	0.80	891.62	0.50	0.63	1.44	2.08	87.93	24.48	29.57	0.24	0.12	54.18	280.17
	10	100	200	3000	200	10000	85	10	10	1.21	2	42	5	0.80	891.62	0.50	0.63	1.44	2.08	87.93	24.48	29.57	0.24	0.12	54.18	390.31
	11	100	200	4000	200	10000	85	10	10	1.21	2	42	5	0.80	891.62	0.50	0.63	1.44	2.08	87.93	24.48	29.57	0.24	0.12	54.18	513.48
	12	100	200	5000	200	10000	85	10	10	1.21	2	42	5	0.80	891.62	0.50	0.63	1.44	2.08	87.93	24.48	29.57	0.24	0.12	54.18	637.27
	13	100	200	6000	200	10000	85	10	10	1.21	2	42	5	0.80	891.62	0.50	0.63	1.44	2.08	87.93	24.48	29.57	0.24	0.12	54.18	783.49
	14	100	200	7000	200	10000	85	10	10	1.21	2	42	5	0.80	891.62	0.50	0.63	1.44	2.08	87.93	24.48	29.57	0.24	0.12	54.18	923.45
	15	100	200	8000	200	10000	85	10	10	1.21	2	42	5	0.80	891.62	0.50	0.63	1.44	2.08	87.93	24.48	29.57	0.24	0.12	54.18	1167.12
	16	100	400	9000	200	10000	119	20	10	1.21	2	60	4	1.59	891.62	0.35	1.30	1.54	2.84	81.73	50.27	41.79	0.34	0.37	92.43	1555.92
	17	100	400	10000	200	10000	119	20	10	1.21	2	60	4	1.59	891.62	0.35	1.30	1.54	2.84	81.73	50.27	41.79	0.34	0.37	92.43	2134.53
Sweep Po	18	200	200	4000	100	10000	63	10	10	0.85	1	57	5	1.59	886.41	0.34	0.59	0.47	1.06	61.14	22.98	14.50	0.17	0.07	37.55	504.80
	19	200	200	4000	200	10000	85	10	10	1.21	2	42	5	0.80	891.62	0.50	0.63	1.44	2.08	87.93	24.48	29.57	0.24	0.12	54.18	513.48
	20	200	200	4000	300	10000	91	20	10	1.48	3	39	3	0.53	896.90	0.34	1.01	1.17	2.17	73.36	38.44	34.86	0.23	0.15	73.45	543.31
	21	200	200	4000	400	10000	105	20	10	1.71	4	34	3	0.40	891.62	0.40	1.15	1.79	2.94	86.64	44.35	45.22	0.26	0.17	89.74	559.61
	22	200	200	4000	500	10000	119	30	10	1.91	5	30	2	0.32	891.62	0.29	1.60	1.41	3.01	75.97	61.69	48.88	0.25	0.24	110.81	590.14
	23	200	200	4000	600	10000	133	30	10	2.09	6	27	2	0.27	886.41	0.31	1.77	1.81	3.58	82.93	68.95	57.32	0.27	0.27	126.53	605.87
	24	200	200	4000	700	10000	153	30	10	2.26	7	24	2	0.23	866.86	0.33	2.12	2.07	4.19	89.06	85.19	60.60	0.26	0.26	146.05	641.20
	25	200	200	4000	800	10000	119	40	20	2.41	8	30	2	0.20	891.62	0.17	2.19	3.07	5.26	84.83	84.54	83.18	0.34	0.37	168.09	667.84
	26	200	200	4000	900	10000	171	30	20	2.56	9	21	2	0.18	886.41	0.18	2.87	2.94	5.81	89.13	111.63	74.39	0.29	0.36	186.38	694.75
	27	200	200	4000	1000	10000	133	70	10	2.56	9	27	1	0.16	886.41	0.20	3.09	2.07	5.16	84.19	120.02	77.81	0.30	0.52	198.34	706.72
	28	200	200	4000	1100	10000	143	70	10	2.70	10	25	1	0.14	890.38	0.21	3.62	2.03	5.66	88.07	140.03	75.63	0.28	0.44	216.10	732.89
	29	200	200	4000	1200	10000	153	70	10	2.83	11	24	1	0.13	866.86	0.22	3.58	2.34	5.92	89.23	143.94	85.99	0.30	0.50	230.44	751.57
Sweep f	30	100	200	4000	200	3981	121	20	10	1.35	1	74	5	2.00	892.96	0.55	0.41	1.39	1.80	60.66	60.40	68.22	0.50	0.15	128.77	1903.31
	31	100	200	4000	200	6310	171	10	10	1.52	2	33	5	1.26	894.01	0.61	0.84	0.91	1.74	64.76	62.38	46.61	0.30	0.15	109.14	983.69
	32	100	200	4000	200	10000	85	10	10	1.21	2	42	5	0.80	891.62	0.50	0.63	1.44	2.08	87.93	24.48	29.57	0.24	0.12	54.18	513.48
	33	100	200	4000	200	15849	45	20	10	1.17	3	50	3	0.50	892.62	0.28	0.88	0.77	1.65	73.88	17.28	20.61	0.17	0.11	37.99	307.02
	34	100	200	4000	200	25119	45	20	10	1.20	5	32	2	0.32	880.01	0.19	1.75	0.36	2.11	87.52	17.28	12.39	0.10	0.11	29.77	213.60
	35	100	200	4000	200	39811	15	40	20	1.21	8	62	2	0.20	859.74	0.09	1.86	0.61	2.46	89.88	9.50	16.60	0.14	0.12	26.22	163.76
	36	100	200	4000	200	63096	15	40	30	1.18	12	64	2	0.13	525.51	0.06	2.04	0.84	2.88	89.42	10.94	16.05	0.14	0.14	27.14	138.30
	37	100	200	4000	200	100000	15	70	30	1.14	18	59	1	0.08	359.67	0.03	3.24	0.39	3.62	89.54	15.26	11.33	0.10	0.20	26.79	118.21
	38	100	200	4000	200	158489	15	80	20	1.15	29	65	1	0.05	205.99	0.04	2.74	0.53	3.27	89.98	15.26	12.71	0.11	0.19	28.17	96.93
	39	100	200	4000	200	251189	15	70	20	1.14	45	60	1	0.03	140.80	0.05	2.37	0.65	3.02	88.43	13.82	11.46	0.10	0.18	25.46	91.22
	40	100	200	4000	200	398107	9	80	30	1.15	72	67	1	0.02	132.60	0.03	2.29	0.81	3.10	89.41	10.02	10.45	0.09	0.15	20.63	69.58
	41	100	200	4000	200	630957	15	50	30	1.14	113	42	1	0.01	80.08	0.03	2.17	0.91	3.08	87.87	12.38	8.02	0.07	0.16	20.57	67.48
	42	100	200	4000	200	1000000	15	30	20	1.14	179	25	1	0.01	84.88	0.04	1.39	0.80	2.20	89.98	8.06	4.77	0.04	0.10	12.94	45.24

(b) Continued

Table G.5: Detailed simulation results of the combined weight of inductor and transformer, corresponding to Fig. 5-5.

Manufacturer	Manufacturer PN	DC voltage rating (kV)	DC current rating (A)	Rds_on (ohm)	Package	Length (mm)	Width (mm)	Area (mm2)	Mass (mg)
Diodes Incorporated	DMN24H3D5L-7	0.24	0.48	3.5	SOT23	3.1	3.3	10.2	99
Diodes Incorporated	ZVN4525E6TA	0.25	0.23	8.5	SOT-23-6	3.1	3.3	10.2	17
Diodes Incorporated	DMP25H18DLFDE-7	0.25	0.26	14	DFN2020-6	2	2	4.0	75
Infineon	BSP299H6327XUSA1	0.5	0.4	4	SOT-223	6.5	7	45.5	112
STMicroelectronics	STL3NM60N	0.6	0.65	1.8	POWERFLAT 3x3	3	3	9.0	28
STMicroelectronics	STL10N65M2	0.65	4.5	1	POWERFLAT 5X6 H	5	6	30.0	92
Vishay Siliconix	SIHJ6N65E-T1-GE3	0.65	5.6	0.868	POWERPAK SO-8L	4.9	6.15	30.1	81
STMicroelectronics	STL12N65M2	0.65	8.5	0.75	POWERFLAT 5X6 H	5	6	30.0	93
Infineon	IPN70R1K2P7SATMA1CT	0.7	4.5	1.2	SOT-223	6.7	7	46.9	115
Infineon	IPN80R1K2P7ATMA1	0.8	4.5	1.2	SOT-223	6.7	7	46.9	117
STMicroelectronics	STL8N80K5	0.8	4.5	0.95	8PWRFLAT	5	6	30.0	85
IXYS	IXFA4N100Q-TRL	1	4	3	TO-263	10	15.5	155.0	1492
IXYS	IXFT6N100F	1	6	1.9	TO-268	16.05	19.1	306.6	4015
IXYS	IXTA4N150HV	1.5	4	6	TO-263	10	15.5	155.0	1508
IXYS	IXTT3N200P3HV	2	3	8	TO-268	16.05	19.1	306.6	3945
IXYS	IXTH1N300P3HV	3	1	50	TO-247HV	16	30.5	488.0	6328
IXYS	IXTT02N450HV	4.5	0.2	750	TO268	16.05	19.1	306.6	3914
IXYS	IXTF02N450	4.5	0.2	750	I4PAK	20	30	600.0	5618

Table G.6: List of MOSFETs considered in the weight study of non-resonant topologies and the switched-capacitor multi-level inverter (credit to Suzanne O'Meara).

Manufacturer	Manufacturer PN	Capacitance (uF)	DC voltage rating (kV)	Package	Mass (mg)
TDK	CGA5K3X7T2E154M	0.15	0.25	1206	36
TDK	C3216X7T2E224K	0.22	0.25	1206	45
TDK	C3216X7T2W104M160AA	0.1	0.45	1206	46
TDK	C3225X7T2W224M200AA	0.22	0.45	1210	91
TDK	C4532X7T2W474K230KA	0.47	0.45	1812	183
KEMET	C1210V154KCRACTU	0.15	0.5	1210	96
TDK	C4532X7T2J304M	0.3	0.63	1812	196
TDK	C4532X7T2J304M250KA	0.3	0.63	1812	196
AVX	1825AC104KAZ1A	0.1	1	1825	416
AVX	2220AC124KAZ1A	0.12	1	2220	391
AVX	2225AC104KAZ2A	0.1	1	2225	513
AVX	2225AC104KAZ1A	0.1	1	2225	513
AVX	2225AC104KAT2A	0.1	1	2225	510
AVX Corporation	1206AA101JAT1A	0.0001	1	1206	29
AVX Corporation	1206AA221JAT1A	0.00022	1	1206	35
AVX Corporation	1206AA471JAT1A	0.00047	1	1206	31
AVX Corporation	1812AA102JAT1A	0.001	1	1812	85
AVX Corporation	1812AA222JAT1A	0.0022	1	1812	120
AVX Corporation	1825AA332JAT1A	0.0033	1	1825	281
AVX Corporation	HQCEAA122JAT6A	0.0012	1	3838	1322
Digikey HV Cap Kit	C3216X7S3A102K	0.001	1	1206	22
Digikey HV Cap Kit	C3216X7S3A222K	0.0022	1	1206	36
Digikey HV Cap Kit	C3225X7S3A472K	0.0047	1	1210	70
Digikey HV Cap Kit	C4532X7R3A472K	0.0047	1	1812	125
Digikey HV Cap Kit	C4532X7S3A103K	0.01	1	1812	130
Digikey HV Cap Kit	C5750X7S3A223K	0.022	1	2220	241
Digikey HV Cap Kit	C5750X7S3A473K	0.047	1	2220	385
Johanson Dielectrics	102S48W104KV4E	0.1	1	2225	362
KEMET	C1206C101JDGACTU	0.0001	1	1206	19
KEMET	C1206C151JDGACTU	0.00015	1	1206	27
KEMET	C1206C181JDGAC7800	0.00018	1	1206	19
KEMET	C1206C331JDGAC7800	0.00033	1	1206	22
KEMET	C1206C471JDGACTU	0.00047	1	1206	31
KEMET	C1206C681JDGAC7800	0.00068	1	1206	33
KEMET	C1206C102JDGACTU	0.001	1	1206	36
KEMET	C1210C222JDGACTU	0.0022	1	1210	94
KEMET	C1210H272JDGACTU	0.0027	1	1210	94
KEMET	C1210C682JDGACAUTO	0.0068	1	1210	76
KEMET	C1812C152JDGACTU	0.0015	1	1812	93
KEMET	C1812C472JDGACTU	0.0047	1	1812	159
KEMET	C1812C103JDGACAUTO	0.01	1	1812	117
KEMET	C1812X104KDRACTU	0.1	1	1812	125
KEMET	C1825C332JDGAC7800	0.0033	1	1825	202
KEMET	C1825C104KDRACTU	0.1	1	1825	384
KEMET	C1825X104KDRACTU	0.1	1	1825	385
KEMET	C2220C104KDRACAUTO	0.1	1	2220	397
KEMET	C2225C822JDGAC7800	0.0082	1	2225	236
KEMET	C2225C104KDRAC7800	0.1	1	2225	363
KEMET	C2225X104KDRAC7800	0.1	1	2225	365
KEMET	C2225C154KDRACTU	0.15	1	2225	461
KEMET	C2225X154KDRACTU	0.15	1	2225	466
Knowles Novacap	2225B104K102NT	0.1	1	2225	315
Knowles Syfer	1812Y1K00222JCT	0.0022	1	1812	91
Knowles Syfer	1812Y1K00104KSTWS2	0.1	1	1812	223

Manufacturer	Manufacturer PN	Capacitance (uF)	DC voltage rating (kV)	Package	Mass (mg)
Knowles Syfer	1812Y1K00154KXTWS2	0.15	1	1812	244
Knowles Syfer	2220J1K00562JGT	0.0056	1	2220	170
Knowles Syfer	2220Y1K00104KST	0.1	1	2220	259
Knowles Syfer	2220Y1K00104KXT	0.1	1	2220	245
Knowles Syfer	2220Y1K00474KXTWS2	0.47	1	2220	572
Knowles Syfer	2220Y1K00474KETWS2	0.47	1	2220	545
Knowles Syfer	222521K00122JQTAF9LM	0.0012	1	2225	472
Knowles Syfer	222521K00152JQTAF9LM	0.0015	1	2225	444
Knowles Syfer	222521K00332JQTAF9LM	0.0033	1	2225	436
Murata	GCJ55DR73A104KXJ1L	0.1	1	2220	281
Murata	GRJ55DR73A104KWJ1L	0.1	1	2220	288
Murata	KRM55TR73A224MH01K	0.22	1		609
Murata	GRM31A7U3A101JW31D	0.0001	1	1206	16
Murata	GRM31A7U3A151JW31D	0.00015	1	1206	16
Murata	GRM31A7U3A221JW31D	0.00022	1	1206	16
Murata	GRM31A7U3A331JW31D	0.00033	1	1206	17
Murata	GRM31B7U3A471JW31L	0.00047	1	1206	23
Murata	GRM31B7U3A561JW31L	0.00056	1	1206	24
Murata	GRM31C7U3A102JW32L	0.001	1	1206	34
Murata	GRM32D7U3A222JW31L	0.0022	1	1210	62
Murata	GRM43D7U3A472JW31L	0.0047	1	1812	117
Murata	GRM55D7U3A103JW31L	0.01	1	2220	233
Vishay	VJ1206A221JXGAT5Z	0.00022	1	1206	30
Vishay	VJ2225Y104KXGAT	0.1	1	2225	450
Yageo	CC1206JKNPOCBN101	0.0001	1	1206	31
Yageo	CC1206JKNPOCBN151	0.00015	1	1206	29
Yageo	CC1206JKNPOCBN221	0.00022	1	1206	30
Yageo	CC1206JKNPOCBN331	0.00033	1	1206	32
Yageo	CC1206JKNPOCBN471	0.00047	1	1206	31
Yageo	CC1206JKNPOCBN102	0.001	1	1206	31
Yageo	CC1812JKNPOCBN152	0.0015	1	1812	84
Knowles Syfer	2220Y1K20224KXTWS2	0.22	1.2	2220	535
AVX Corporation	1206SA101JAT1A	0.0001	1.5	1206	30
KEMET	C1812C561JFGAC7800	0.00056	1.5	1812	72
KEMET	C1812C681JFGACTU	0.00068	1.5	1812	79
KEMET	C2220C331JFGAC7800	0.00033	1.5	2220	177
KEMET	C2220C562JFGACTU	0.0056	1.5	2220	334
KEMET	C2225C104KFRACTU	0.1	1.5	2225	461
KEMET	C2225X104KFRACTU	0.1	1.5	2225	454
Knowles Syfer	2220Y1K50154KXTWS2	0.15	1.5	2220	638
Vishay	VJ1210A222JXRAT5Z	0.0022	1.5	1210	70
AVX Corporation	1206GA101JAT2A	0.0001	2	1206	30
AVX Corporation	1808GA221JAT1A	0.00022	2	1808	83
AVX Corporation	1812GA151JAT1A	0.00015	2	1812	87
AVX Corporation	1812GA471JAT1A	0.00047	2	1812	136
AVX Corporation	1812GA102JAT2A	0.001	2	1812	137
Digikey HV Cap Kit	C3216X7S3D101K	0.0001	2	1206	21
Digikey HV Cap Kit	C3216X7S3D221K	0.00022	2	1206	22
Digikey HV Cap Kit	C3216X7S3D471K	0.00047	2	1206	35
Digikey HV Cap Kit	C3225X7S3D102K	0.001	2	1210	83
Digikey HV Cap Kit	C3225X7S3D222K	0.0022	2	1210	108
Digikey HV Cap Kit	C4520X7R3D471K	0.00047	2	1808	62
Digikey HV Cap Kit	C4520X7R3D102K	0.001	2	1808	63
Digikey HV Cap Kit	C4532X7S3D222K	0.0022	2	1812	127

Manufacturer	Manufacturer PN	Capacitance (uF)	DC voltage rating (kV)	Package	Mass (mg)
Digikey HV Cap Kit	C5750X7S3D472K	0.0047	2	2220	302
Digikey HV Cap Kit	C5750X7S3D103K	0.01	2	2220	392
KEMET	C1206C101JGGACTU	0.0001	2	1206	23
KEMET	C1206C151JGGAC7800	0.00015	2	1206	31
KEMET	C1206C221JGGACAUTO	0.00022	2	1206	37
KEMET	C1210C331JGGACTU	0.00033	2	1210	66
KEMET	C1808C471JGGAC7800	0.00047	2	1808	54
KEMET	C1808C681JGGAC7800	0.00068	2	1808	83
KEMET	C1812C102JGGACTU	0.001	2	1812	116
KEMET	C1812H122JGGACTU	0.0012	2	1812	151
KEMET	C1825C152JGGACTU	0.0015	2	1825	166
KEMET	C2225C392JGGACTU	0.0039	2	2225	395
KEMET	C2824C562JGGACAUTO	0.0056	2	2824	503
KEMET	C3040H103JGGACT050	0.01	2	3040	871
Knowles Syfer	1812J2K00471JCT	0.00047	2	1812	120
Knowles Syfer	2220J2K00101JCT	0.0001	2	2220	235
Knowles Syfer	222522K00561JQTAF9LM	0.00056	2	2225	435
Knowles Syfer	222522K00681JQTAF9LM	0.00068	2	2225	440
Knowles Syfer	222522K00821JQTAF9LM	0.00082	2	2225	441
Knowles Syfer	222522K00102JQTAF9LM	0.001	2	2225	436
Murata	GR455DR73D103KW01L	0.01	2	2220	480
Murata Electronics Nor	GRM32A7U3D101JW31D	0.0001	2	1210	26
Murata Electronics Nor	GRM32B7U3D221JW31L	0.00022	2	1210	35
Yageo	CC1206JKNPODBN101	0.0001	2	1206	31
Yageo	CC1206JKNPODBN221	0.00022	2	1206	31
AVX Corporation	HQCCWA151JAT6A	0.00015	2.5	2325	406
AVX Corporation	HQCEWA561JAT6A	0.00056	2.5	3838	1332
AVX Corporation	HQCEWA681JAT6A	0.00068	2.5	3838	1328
KEMET	C1808C221JZGACTU	0.00022	2.5	1808	80
KEMET	C1808C331JZGAC7800	0.00033	2.5	1808	78
KEMET	C1812C101JZGAC7800	0.0001	2.5	1812	94
KEMET	C1812C471JZGACTU	0.00047	2.5	1812	100
KEMET	C1825C561JZGACTU	0.00056	2.5	1825	191
KEMET	C1825C821JZGACTU	0.00082	2.5	1825	217
KEMET	C2220C681JZGACTU	0.00068	2.5	2220	199
KEMET	C2220C102JZGACTU	0.001	2.5	2220	207
AVX Corporation	1812HA221JAT1A	0.00022	3	1812	87
Digikey HV Cap Kit	C4532C0G3F101K	0.0001	3	1812	96
Digikey HV Cap Kit	C4532C0G3F221K	0.00022	3	1812	124
KEMET	C1808C101JHGAC7800	0.0001	3	1808	58
KEMET	C1812C151JHGACTU	0.00015	3	1812	93
KEMET	C1812C221JHGACAUTO	0.00022	3	1812	123
KEMET	C1812C331JHGAC7800	0.00033	3	1812	154
KEMET	C2225C471JHGACTU	0.00047	3	2225	245
Knowles Syfer	222523K00271JQTAF9LM	0.00027	3	2225	431
Knowles Syfer	222523K00331JQTAF9LM	0.00033	3	2225	438
Knowles Syfer	222523K00391JQTAF9LM	0.00039	3	2225	447
Knowles Syfer	222523K00471JQTAF9LM	0.00047	3	2225	441
Yageo	CC1812JKNPOEBN101	0.0001	3	1812	90
Yageo	CC1812JKNPOEBN221	0.00022	3	1812	88
Murata Electronics Nor	GRM42A7U3F101JW31L	0.0001	3.15	1808	30
AVX Corporation	HQCEJA221JAT6A	0.00022	3.6	3838	1350
AVX Corporation	HQCEJA391JAT1A	0.00039	3.6	3838	1368
AVX Corporation	HQCEMA101JAT6A	0.0001	7.2	3838	1342

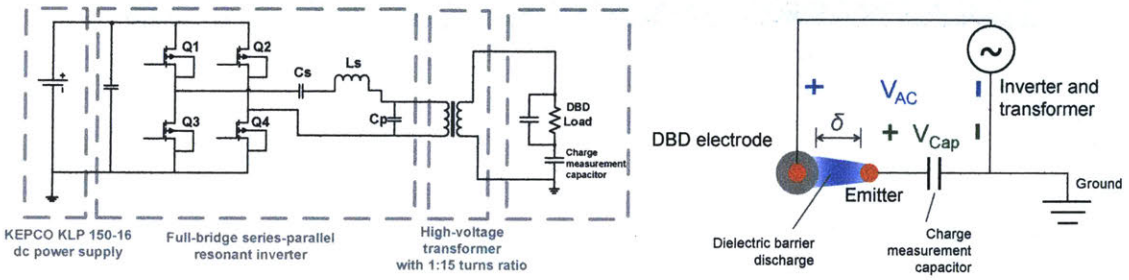
Table G.7: List of capacitors considered in the weight study of non-resonant topologies and the switched-capacitor multi-level inverter.

G.2 Implementation of the burst-mode solution

G.2.1 Hardware set up

We reuse the inverter and the high-voltage transformer built in Chapter 2 for the burst-mode operation (see the specifications in Table 2.3). Figure G-6a shows the schematics.

The diagram of the DBD set up is shown in Fig. G-6b. The emitter electrode was a tungsten wire with a diameter of 0.254 mm, the DBD electrode was a fluorinated ethylene propylene (FEP) insulated high voltage wire, which has a conductor diameter of 0.4 mm and an overall diameter of 1.02 mm. The two electrodes were spaced $\delta = 1$ mm apart. The span of the electrodes (into the page) was 750 mm. A 2.2 nF capacitor was placed in series with the DBD and the voltage across it was measured. The charge in the capacitor, which is calculated by multiplying the voltage and the capacitance, is the integral of the DBD current and was used to calculate the power draw (as in Fig. 1-2b).

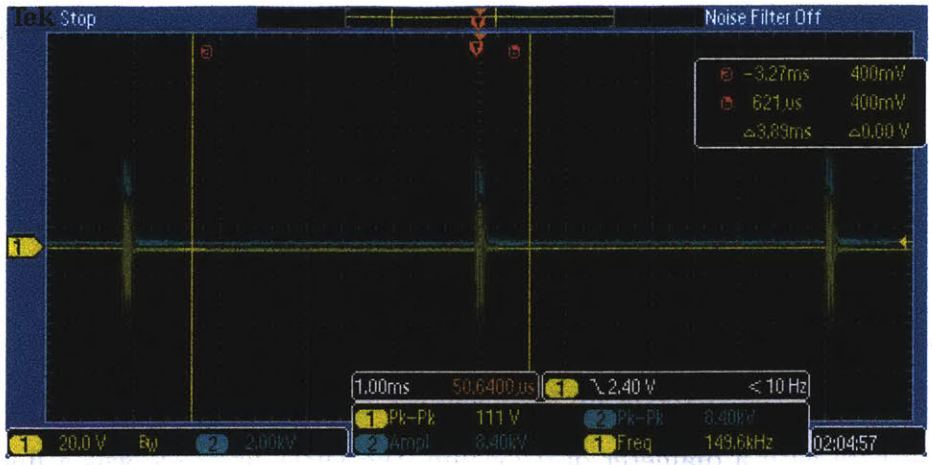


(a) Simplified schematics (b) Cross-sectional diagram of the DBD load

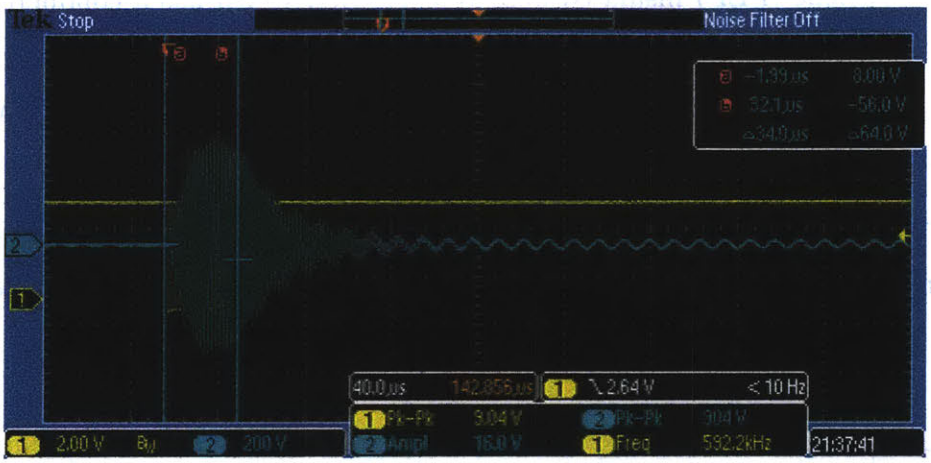
Figure G-6: Diagrams of the inverter/transformer and the DBD load used in the demonstration of the burst-mode solution.

G.2.2 Power measurements

Our goal is to compare the "efficiency" of the burst-mode DBD as a thruster with DBD driven by other more standard periodical waveform (such as sine wave, as used in our previous work in [7]). Two metrics characterizing the "efficiency" are "thrust"



(a) Burst-mode waveform



(b) Zoomed-in waveform at a lower DBD voltage V_{AC}

Figure G-7: Experimental waveform when the inverter and transformer is bursting at 250 Hz. a) CH1: charge capacitor voltage V_{CAP}; CH2: voltage across the DBD load V_{AC}. Both as labeled in Fig. G-6b. b) CH1: switching commands from the microcontroller; CH2: voltage across the DBD load V_{AC}.

and "power", intuitively, a thruster that can generate more thrust with less power is more desirable.

In this chapter, we conducted preliminary experiments to characterize the "power" of the burst-mode DBD. The thrust measurements will be carried out by Suzanne O'Meara.

We want to map "burst-mode" to an equivalent "sine-wave" and compare their power draw. First, we define three parameters for the burst-mode operation: the bursting duty cycle D, the switching frequency f_s and the number of pulses N_B. The

bursting frequency f_B is then $f_B = Df_s/N_B$.

Then, we define the frequency of the equivalent sine-wave DBD as f_{DBD}. f_B is not necessarily equal to f_{DBD} because: 1) in the sine wave case (see [7] and Chapter 6), we observe that once f_{DBD} is higher than a threshold, further increasing f_{DBD} does not change the thrust generated, but only increases the power draw. 2) therefore we assume one sine wave at f_{DBD} generates the same amount of "useful" ions as one sine wave at f_s, even if f_s is significantly higher than f_{DBD}. In fact, bursting a few cycles of f_s and resting for some period of time is a way to reduce power draw and not affect the thrust generation.

Thus, we assume bursting N_B number of f_s sine pulses, the equivalent ions generated is the same with N_B numbers of f_{DBD} sine pulses. To reduce the power draw, the f_s pulses should rest for $N_B T_{DBD} - N_B T_s$, which means the relationship between f_B and f_{DBD} is $T_B = T_{DBD} N_B$ and $f_{DBD} = f_B N_B$. As an example, if $f_s = 590\,\text{kHz}$ and we burst 2 pulses at $f_B = 250\,\text{Hz}$, we should compare the power draw to the sine wave DBD with $f_{DBD} = 500\,\text{Hz}$. Figure. G-7a shows an example waveform when bursting at 250 Hz[7].

The experimental details of burst-mode DBD in Fig. 5-18 is listed in Table. G.8. The sine wave experimental results are the same with Fig. 6-11a in Chapter 6.

G.2.3 Remaining issues

We identify two issues of the burst-mode solution that require future research efforts:

- Difficulty to generate "clean" pulses: due to the nature of the resonant tank, ringings occur during burst-mode operation and the peak amplitude of the ringing seems to be hard to control. These issues may increase losses in the circuit and result in inaccurate characterization of the DBD. See Fig. G-7b as an example.

- Severe audible noise compared with the sine wave. This may be caused by 1) the

[7]The cursor in the screen shot roughly measures the bursting period to be 4 ms (250 Hz). The "Freq" measurement of channel 1 in the screen shot is not accurate (possibly due to the waveform is a mix of both high frequency and low frequency).

No.	Switching Frequency (kHz) f_S	Number of pulses N_B	Duty (%) D	Bursting Frequency (kHz) f_B	Equivalent DBD freq (kHz) f_{DBD}	Vac (amp) (V)	Theta $f_{DBD}V_{ac}^{3.5}$	Power (W)	Power per meter span (W/m)
1	590	10	20	11.67	118	3160	6619	14.19	19
2	590	59	12.5	1.25	73.75	3360	5128	10.57	14
3	590	4	2	2.547	11.8	3640	1086	4.67	9
4	590	18	2	0.636	11.8	3480	928	2.62	5
5	590	11	20	10	118	3040	5780	22.01	44
6	590	5	10	10	59	3240	3612	15.39	31
7	590	2	5	10	29.5	3640	2714	4.73	9
8	590	23	20	5	118	3280	7541	21.79	44
9	590	11	10	5	59	3240	3612	9.04	18
10	590	5	5	5	29.5	3200	1729	5.96	12
11	590	59	20	2	118	3240	7224	23.98	48
12	590	29	10	2	59	3160	3309	13.02	26
13	590	14	5	2	29.5	3640	2714	7.85	16
14	590	11	20	10	118	3600	10446	19.77	40
15	590	5	10	10	59	3720	5858	14.38	29
16	590	2	5	10	29.5	3680	2820	2.63	5
17	590	23	20	5	118	3680	11281	22.35	45
18	590	11	10	5	59	3600	5223	9.91	20
19	590	5	5	5	29.5	3640	2714	5.65	11
20	590	59	20	2	118	3880	13577	23.17	46
21	590	29	10	2	59	3680	5641	12.28	25
22	590	14	5	2	29.5	3840	3273	6.39	13
24	590	5	2	2	11.8	3960	1458	1.85	4
25	590	11	2	1	11.8	4360	2042	2.60	5
26	590	23	2	0.5	11.8	4040	1564	2.39	5
27	590	59	2	0.2	11.8	4200	1792	1.50	3

Table G.8: Details of burst-mode DBD power measurements in Fig. 5-18.

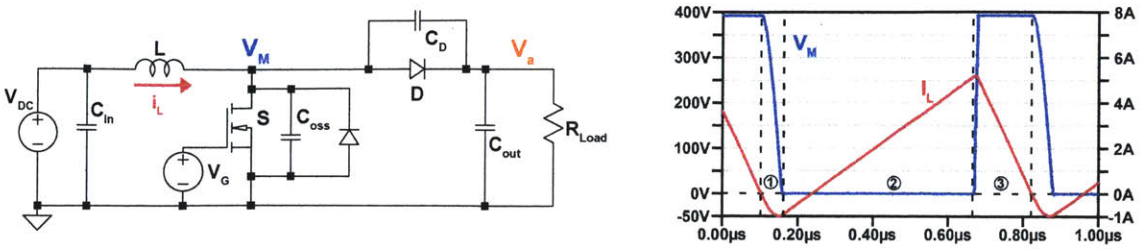
DBD electrodes vibrating more severely in burst-mode than sine wave mode. 2) electronics also generate more audible noise at burst-mode. Since "silence" is one of the most desirable features of the EAD thruster, this issue needs to be resolved if the burst-mode solution is to be used in practical application.

G.3 Weight study and implementation of the resonant transition boost converter (RTC)

Figure G-8a shows the circuit diagram of a RTC. Figure G-8b shows an example waveform of the switching node voltage and the inductor current.

Different from a standard boost converter, in a RTC, the inductor resonates with the switching node capacitance C_M near the switching frequency and achieves zero-voltage switching of the MOSFET. This is not a fixed frequency converter, rather, the switching frequency and the inductor current can be calculated from C_M, V_{in}, V_o

and P_o [113, 152].



(a) Schematic

(b) Example waveform

Figure G-8: RTC boost schematic and simulated waveforms when $V_{in} = 100V$, $V_o = 400V$ and $P_o = 200W$. The switching frequency is ~1.15 MHz.

G.3.1 Operation and gate driving circuits

Gate driving circuits

The driving circuit is shown in Fig. G-9. The driving circuit has two parts: the top part of the circuit is for zero-voltage-switching (ZVS) detection, which detects when the switching node voltage v_M is below a preset ZVS limit and turns on the MOSFET S; the bottom part of the circuit is for on-time control, which sets the on time of the MOSFET S.

Four signals highlighted in green, "ZVS_limit", "Ctrl", "Disable" and "ManualOn", are commanded from a microcontroller. In steady state operation, "Disable" and "ManualOn" are both logic low.

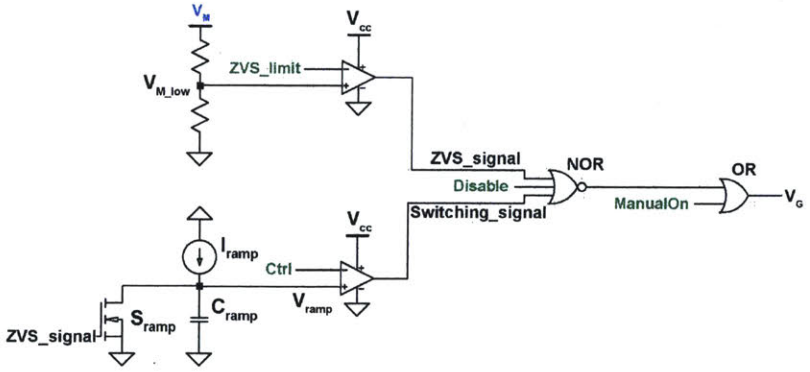


Figure G-9: RTC boost gate-driving circuits

Steady state operations

For a given set of V_{in}, V_a, P_a, inductor L and switching node capacitance C_M, we can calculate the timing of each period labeled in Fig. G-8b, the frequency, and the inductor peak current. See [113] by Dr. Gus Zhang for equations. Here we give a brief explanation of the operations of each period.

Period (1) For analysis purpose, we assume the circuit start with MOSFET S being off and diode D being on. Thus V_M is connected to V_O – the inductor L releases energy to the load. The inductor current i_L starts at some positive value and discharges to zero. At the moment when i_L hits zero, the diode D turns off, L, C_D and C_{OSS} form a LC resonant network where C_{OSS} discharges, C_D charges and i_L keeps going negative. During this resonant transient, v_M (i.e., the voltage across C_{OSS}) rings down from V_O.

v_M is divided down to $v_{M_{Low}}$ and compared with "ZVS_limit". When $v_{M_{Low}}$ decreases to lower than "ZVS_limit", the comparator output "ZVS_signal" goes from V_{CC} to zero. This results in **a)** the output of the NOR gate turns high (thus v_G turns high and MOSFET S turns on) and **b)** the switch S_{ramp} turns off. (Let's stop for a second and check the gate signal v_G before this resonant transition: $v_{M_{Low}}$ was higher than "ZVS_limit", thus "ZVS_signal" was high and the switch S_{ramp} was on, making the comparator output "Switching_signal" logic low. Therefore the NOR gate outputted low, keeping the MOSFET S off. This is consistent with the assumption we made.)

Period (2) After the MOSFET S turns on and the switch S_{ramp} turns off, the voltage on the capacitor C_{ramp} starts to build up at the rate

$$V_{C_{ramp}} = \int \frac{I_{ramp}}{C_{ramp}} dt$$

Once V_{ramp} increases to "Ctrl", the comparator output "Switching_signal" turns high. At this moment, the output of the NOR gate turns low, thus V_G turns low and the MOSFET S turns off.

Period (3) **and** (4) From the moment when MOSFET S turns off, the voltage

at v_M starts to ramp up, when it increases to "ZVS_limit", "ZVS_signal" turns high. This makes the switch S_{ramp} turns on, shorting the capacitor C_{ramp} to ground and making "Switching_signal" turn low. At this moment, the output of the NOR gate keeps low.

Start up procedures

The above gate driving operation is self-sustained during the steady state — once after the inductor current i_L builds up enough charge to be able to ring down v_M to below "ZVS_limit", the gate driving circuit "kicks" on by itself every cycle.

During the start up, we manually toggle MOSFET S to build up i_L and V_O until the driving circuit latches on a pulse itself. We do so by toggling "Disable" and "ManualOn". One should set "Ctrl" low enough so that it can trigger "Switching_signal" to toggle.

G.3.2 Weight study of the inductor

The timing calculation of the RTC is quite time-consuming. To make the simulation size manageable, we reduced the range of the core sizes to off-the-shelf cores in Table B.1.

We pick a inductor design (a combination of core size, wire build, winding pattern, and airgap) and calculate its inductance as

$$L = \frac{\mu_0 A_c N_p^2}{airgap + L_e/\mu_r}$$

Then we assume C_M =160 pF across all simulations[8] to calculate the timing and the inductor current (following equations in [113]). Once we know the inductor current and inductance, the core loss is calculated using standard Steinmetz equations (same as with the tank inductor) and the copper loss is calculated including the dc current:

[8]We assume two GS66502T in parallel (40 pF each), two SiC schottky diodes C3D1P7060 in parallel (10 pF each), then with a 50% margin to account for stray capacitances. This may vary during the actual design, but we hold it constant here for ease of simulation.

$$P_{copper} = I_{Lave}^2 R_{dc} + I_{Lac_{1rms}}^2 R_{ac}$$

Where $I_{L_{ave}}$ is the average inductor current and $I_{L_{ac_{1rms}}}$ is the rms of the fundamental of the inductor current ac component. R_{dc} and R_{ac} are the dc and ac resistance of the winding respectively.

Note that since the inductor is DC-biased, one can also use the general Steinmetz equations (GSE) [153] to model the core loss.

G.3.3 More experimental results and remaining work

Figure G-10 shows the thermal image of the RTC operating at $V_{DC} = 70V$, $V_o = 300V$ and $P_o = 112W$ for 5 min. The hottest spot in the RTC is one of the two parallel MOSFETs. Two MOSFETs exhibit different temperature rise because their thermal paths were not designed equally.

Remaining work on the RTC include: 1) test the prototype with smaller inductor; 2) test the prototype at 100 V input, 400 V and 200 W output. Redesign of the MOSFET thermal paths may be required; 3) integrate the RTC with the developed switch-capacitor multi-level inverter prototype to realize close-loop control of the output high voltage ac waveform.

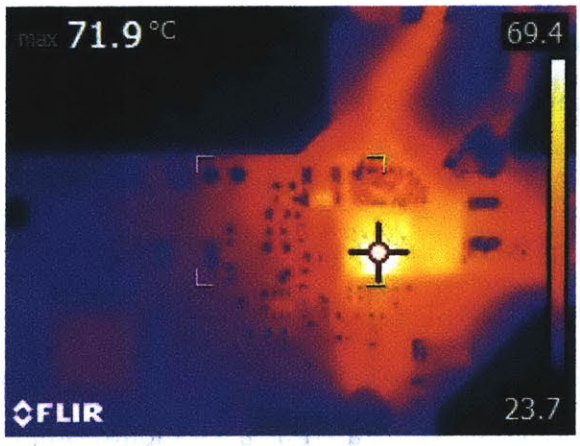


Figure G-10: Thermal image of the resonant transition boost converter prototype when it converts $V_{DC} = 70V$ to $V_o = 300V$ and outputs $P_o = 112W$.

	Operating parameters				Core		Wire build			Winding pattern		MISC				Loss (W)			Absolute Temp (C)	Weight (g)					
	Pa(W)	Vdc(V)	Va(V)	fs (MHz)	Material	Size	Number of litz strands	Wire diameter (mm)	Peak current density (A/cm2)	Number of turns	Number of layers	Bmax (mT)	L (uH)	Airgap (mm)	Packing Factor	Core	Copper	Total		Core	Copper	Inductor total	PCB	Caps	Overall
Sweep Vdc	200	100	400	1.65	ML91S	E30/15/7	303	1.158	674.57	13	1	43.3	5.9	2.1	0.12	1.04	0.88	1.92	87.3	19.2	4.10	23.47	9.35	0.08	32.90
	200	150	600	1.83	3F46	E30/15/8	225	0.945	835.51	17	1	38.7	8.4	2.5	0.11	0.93	1.06	2.00	89.8	19.2	3.50	22.95	9.35	0.03	32.34
	200	200	800	1.54	3F46	E30/15/9	142	0.819	950.63	21	1	46.2	14.5	2.2	0.10	1.06	0.93	1.99	89.6	19.2	3.22	22.75	9.35	0.02	32.12
	200	250	1000	1.11	3F46	E25/13/11	82	0.732	992.95	21	1	59.8	29.4	1.4	0.12	1.24	0.68	1.93	88.8	21.6	3.24	25.34	8.20	0.02	33.56
	200	300	1200	1.37	3F46	E31/13/9	84	0.669	1263.31	23	1	45.0	24.2	2.2	0.09	1.01	1.17	2.18	89.8	24.72	2.95	28.26	10.97	0.01	39.24
	200	350	1400	1.16	3F46	E34/14/9	61	0.620	1352.58	25	1	57.2	35.4	1.7	0.06	1.48	1.02	2.50	89.1	26.832	2.74	30.39	13.25	0.01	43.65
	200	400	1600	1.02	3F46	E34/14/9	47	0.580	1451.30	29	1	62.4	47.6	1.7	0.06	1.45	1.03	2.48	88.7	26.832	2.79	30.56	13.25	0.01	43.81
Sweep Va	200	100	200	2.16	3F46	E20/14/5	398	1.159	579.80	15	1	51.8	3.9	1.7	0.16	0.86	0.45	1.31	89.3	7.2624	3.40	10.72	6.56	0.23	17.51
	200	100	300	2.17	ML91S	E25/13/7	399	1.158	639.46	13	1	34.7	4.4	2.5	0.16	0.73	0.93	1.66	89.8	14.352	4.16	18.63	8.20	0.10	26.93
	200	100	400	1.65	ML91S	E30/15/9	303	1.158	674.57	13	1	43.3	5.9	2.1	0.12	1.04	0.88	1.92	87.3	19.2	4.10	23.47	9.35	0.08	32.90
	200	100	500	1.21	3F46	E30/15/9	223	1.158	695.27	14	1	57.6	8.3	1.7	0.13	1.18	0.81	1.98	89.4	19.2	4.43	23.83	9.35	0.07	33.25
	200	100	600	1.19	3F46	E30/15/9	219	1.158	753.24	16	1	51.3	7.8	2.4	0.15	0.84	1.15	2.00	89.8	19.2	5.07	24.52	9.35	0.05	33.92
	200	100	700	1.00	3F46	E31/13/9	185	1.158	782.92	12	1	59.1	8.9	1.6	0.12	1.13	1.05	2.19	89.8	24.72	4.76	29.83	10.97	0.04	40.84
	200	100	800	1.03	3F46	E34/14/9	191	1.160	852.38	13	1	53.7	7.8	2.1	0.09	1.02	1.49	2.51	89.2	26.832	5.16	32.47	13.25	0.03	45.74
	200	100	900	1.05	3F46	E35/18/10	194	1.160	929.00	12	1	45.4	6.9	2.5	0.07	0.98	1.91	2.89	89.4	38.736	5.16	44.57	15.90	0.02	60.49
	200	100	1000	1.01	3F46	E41/17/12	187	1.159	996.32	8	1	46.9	6.6	1.7	0.05	1.42	1.77	3.19	87.4	55.2	4.12	60.13	17.98	0.02	78.13
Sweep Pa	100	100	400	2.16	3F46	E20/14/5	199	0.819	846.74	19	1	47.8	6.2	1.7	0.10	0.73	0.58	1.31	89.2	7.2624	2.04	9.42	6.56	0.03	16.01
	200	100	400	1.65	ML91S	E30/15/9	303	1.158	674.57	13	1	43.3	5.9	2.1	0.12	1.04	0.88	1.92	87.3	19.2	4.10	23.47	9.35	0.08	32.90
	300	100	400	1.28	3F46	E34/14/9	353	1.419	608.78	12	1	48.5	6.1	2.3	0.12	1.17	1.31	2.48	88.7	26.832	7.26	34.32	13.25	0.15	47.72
	400	100	400	1.01	3F46	E35/18/10	373	1.638	574.55	13	1	47.8	6.4	3.2	0.15	1.05	1.83	2.88	89.1	38.736	11.52	50.55	15.90	0.25	66.70
	500	100	400	1.16	3F46	E42/21/15	532	1.831	569.61	8	1	38.5	4.6	3.0	0.08	1.66	2.50	4.15	88.7	83.04	11.73	95.26	22.96	0.27	118.48
	600	100	400	1.04	3F46	E42/21/20	575	2.005	555.87	8	1	33.4	4.4	4.1	0.10	1.23	3.49	4.72	89.9	108.96	16.49	126.04	22.96	0.36	149.36
	700	100	400	1.07	3F46	E56/24/19	689	2.167	549.69	6	1	30.3	3.8	3.9	0.08	1.59	4.06	5.65	89.5	172.8	16.79	190.27	35.91	0.41	226.59
	800	100	400	1.00	3F46	EC70	738	2.317	542.12	6	1	39.5	3.6	3.3	0.04	3.11	4.20	7.31	89.5	192.48	17.05	210.43	49.65	0.50	260.58
	900	100	400	1.47	ML91S	E80/38/20	1215	2.456	552.88	4	1	28.3	2.1	3.6	0.02	4.11	6.42	10.53	89.8	347.04	15.26	363.70	59.52	0.38	423.60
	1000	100	400	1.11	3F46	E80/38/20	1021	2.589	538.18	5	1	30.7	2.7	4.4	0.02	3.56	6.95	10.51	89.7	347.04	21.31	369.75	59.52	0.56	429.84

Table G.9: Detailed weight study of the RTC converter, corresponding to Fig. 5-8. The "peak current density" is calculated as the peak inductor current divided by the wire area, the average current density is smaller.

	Operating parameters			Number of modules stacked in series	Each resonant transition boost converter																						Each full-bridge inverter						Combined weight (g)			
					Operating			L (uH)	airgap (mm)	fs (MHz)	Core		Wire build		Winding pattern			Bmax (mT)	Overall packing factor	Loss (W)			Absolute Temp (C)	Weight (g)				Operating		Weight (g)							
	Vin(V)	Vo(V)	Po(W)		Vin(V)	Va(V)	Pa(W)				Material	Size	Wire Diameter (mm)	Num of litz strands	Peak current density (A/cm2)	Num of turns	Num of turns per layer	Num of layers			Core	Copper	Total		Core	Copper	Wire & core insu	Total	Va(V)	Pa(W)	MOSFETs	Capacitors	PCB	Total	Total RTC	Total inverter	Support materials	Overall
Sweep Vo	100	1000	200	5	100	200	40	12.20	0.3	2.14	3F46	E13/6/3	0.52	79	734	18	9	2	82.98	0.16	0.42	0.10	0.52	89.17	1.35	0.57	0.03	1.94	200	40	0.23	0.45	0.61	1.29	9.69	6.43	15	31.12
	100	2000	200	5	100	400	40	6.97	0.6	2.21	3F46	E13/6/6	0.52	82	1191	15	15	1	59.95	0.13	0.46	0.20	0.66	87.23	2.68	0.60	0.06	3.33	400	40	0.34	1.37	1.31	3.02	16.66	15.12	15	46.78
	100	3000	200	15	100	200	13.33	19.62	0.2	2.22	3F46	E6.3/2.9/2	0.30	28	958	32	10	3	102.88	0.65	0.11	0.05	0.16	89.81	0.19	0.22	0.01	0.42	200	13.33	0.11	0.45	0.37	0.94	6.35	14.03	45	65.38
	100	4000	200	20	100	200	10	22.27	0.1	2.17	3F46	E6.3/2.9/2	0.26	20	1079	25	12	2	122.72	0.38	0.14	0.01	0.16	89.38	0.19	0.11	0.01	0.31	200	10	0.11	0.45	0.37	0.94	6.14	18.71	60	84.85
	100	5000	200	25	100	200	8	20.88	0.1	2.33	3F46	E5.3/2.7/2	0.23	17	1204	27	13	2	118.00	0.29	0.13	0.01	0.15	87.58	0.16	0.09	0.01	0.26	200	8	0.11	0.45	0.37	0.94	6.38	23.38	75	104.77
	100	6000	200	30	100	200	6.67	17.90	0.1	2.57	3F46	E5.3/2.7/2	0.22	15	1279	25	12	2	102.39	0.24	0.14	0.01	0.15	88.20	0.16	0.07	0.01	0.24	200	6.67	0.11	0.45	0.37	0.94	7.13	28.06	90	125.19
	100	7000	200	35	100	200	5.71	16.50	0.1	2.71	3F46	E5.3/2.7/2	0.20	13	1387	24	12	2	92.38	0.20	0.13	0.01	0.14	84.66	0.16	0.06	0.01	0.22	200	5.71	0.11	0.45	0.37	0.94	7.86	32.74	105	145.59
	100	8000	200	40	100	200	5	13.86	0.1	2.97	3F46	E5.3/2.7/2	0.19	11	1597	22	11	2	82.52	0.16	0.14	0.01	0.15	88.24	0.16	0.05	0.01	0.21	200	5	0.11	0.45	0.37	0.94	8.41	37.41	120	165.82
	100	9000	200	45	100	200	4.44	13.86	0.1	2.97	3F46	E5.3/2.7/2	0.18	10	1657	22	11	2	77.81	0.15	0.12	0.01	0.13	79.53	0.16	0.04	0.01	0.21	200	4.44	0.11	0.45	0.37	0.94	9.25	42.09	135	186.34
	100	10000	200	50	100	200	4	13.86	0.1	2.97	3F46	E5.3/2.7/2	0.17	9	1748	22	11	2	73.88	0.13	0.10	0.01	0.11	72.75	0.16	0.04	0.01	0.20	200	4	0.11	0.45	0.37	0.94	10.06	46.77	150	206.82
Sweep Po	100	4000	100	20	100	200	5	13.86	0.1	2.97	3F46	E5.3/2.7/2	0.19	11	1597	22	11	2	82.52	0.16	0.14	0.01	0.15	88.24	0.16	0.05	0.01	0.21	200	5	0.11	0.45	0.37	0.94	4.20	18.71	60	82.91
	100	4000	200	20	100	200	10	22.27	0.1	2.17	3F46	E6.3/2.9/2	0.26	20	1079	25	12	2	122.72	0.38	0.14	0.01	0.16	89.38	0.19	0.11	0.01	0.31	200	10	0.11	0.45	0.37	0.94	6.14	18.71	60	84.85
	100	4000	300	20	100	200	15	15.05	0.2	2.54	3F46	E8.8/4.1/2	0.32	32	988	23	11	2	82.01	0.31	0.19	0.03	0.22	88.00	0.37	0.17	0.01	0.55	200	15	0.11	0.45	0.37	0.94	11.08	18.71	60	89.78
	100	4000	400	20	100	200	20	15.29	0.4	2.34	3F46	E8.8/4.1/2	0.37	43	876	32	10	3	71.39	0.57	0.11	0.11	0.22	89.35	0.37	0.39	0.02	0.77	200	20	0.11	0.45	0.37	0.94	15.30	18.71	60	94.01
	100	4000	500	20	100	200	25	15.71	0.3	2.15	3F46	EFD10/5/3	0.41	50	808	24	12	2	78.22	0.30	0.23	0.07	0.30	84.21	0.82	0.54	0.03	1.37	200	25	0.11	0.45	0.37	0.94	27.42	18.71	60	106.12
	100	4000	600	20	100	200	30	14.17	0.4	2.16	3F46	EFD10/5/3	0.45	60	780	26	13	2	74.88	0.39	0.21	0.10	0.32	87.25	0.82	0.70	0.03	1.54	200	30	0.11	0.45	0.37	0.94	30.77	18.71	60	109.47
	100	4000	700	20	100	200	35	12.20	0.3	2.26	3F46	E13/6/3	0.48	73	763	18	9	2	75.56	0.14	0.41	0.08	0.49	86.01	1.35	0.49	0.03	1.86	200	35	0.23	0.45	0.61	1.29	37.18	25.72	60	122.90
	100	4000	800	20	100	200	40	12.20	0.3	2.14	3F46	E13/6/3	0.52	79	734	18	9	2	82.98	0.16	0.42	0.10	0.52	89.17	1.35	0.57	0.03	1.94	200	40	0.23	0.45	0.61	1.29	38.76	25.72	60	124.48
	100	4000	900	20	100	200	45	10.42	0.5	2.28	3F46	E13/6/3	0.55	95	722	21	10	2	67.59	0.21	0.33	0.15	0.48	84.46	1.35	0.77	0.03	2.13	200	45	0.23	0.45	0.61	1.29	42.65	25.72	60	128.37
	100	4000	1000	20	100	200	50	10.42	0.5	2.18	3F46	E13/6/3	0.58	101	699	21	10	2	72.93	0.23	0.34	0.17	0.50	87.35	1.35	0.87	0.03	2.23	200	50	0.23	0.45	0.61	1.29	44.64	25.72	60	130.36
Sweep Vin	100	4000	200	20	100	200	10	22.27	0.1	2.17	3F46	E6.3/2.9/2	0.26	20	1079	25	12	2	122.72	0.38	0.14	0.01	0.16	89.38	0.19	0.11	0.01	0.31	200	10	0.11	0.45	0.37	0.94	6.14	18.71	60	84.85
	150	4000	200	14	150	300	15	17.79	0.2	2.58	3F46	E8.8/4.1/2	0.26	22	1310	25	12	2	81.30	0.26	0.20	0.03	0.23	89.53	0.37	0.13	0.02	0.51	300	15	0.11	0.78	0.43	1.33	7.13	18.56	42	67.68
	200	4000	200	10	200	400	20	22.64	0.3	2.31	3F46	E8.8/4.1/2	0.26	22	1417	34	11	3	82.33	0.37	0.14	0.08	0.22	88.76	0.37	0.20	0.03	0.58	400	20	0.34	1.37	1.31	3.02	5.80	30.24	30	66.04
	250	4000	200	8	250	500	25	22.94	0.3	2.31	3F46	EFD10/5/3	0.26	22	1575	29	14	2	75.46	0.19	0.26	0.06	0.33	89.44	0.82	0.26	0.06	1.11	500	25	5.97	2.68	4.56	13.20	8.90	105.64	24	138.54
	300	4000	200	7	300	600	30	24.23	0.4	2.25	3F46	EFD10/5/3	0.26	21	1736	34	17	2	73.46	0.24	0.23	0.09	0.32	87.01	0.82	0.30	0.08	1.16	600	30	6.03	2.75	4.76	13.54	8.12	94.76	21	123.88
	350	4000	200	6	350	700	35	24.57	0.5	2.23	3F46	EFD10/5/3	0.26	21	1853	38	19	2	71.85	0.28	0.21	0.11	0.32	88.60	0.82	0.34	0.10	1.21	700	35	6.03	4.47	4.75	15.25	7.26	91.50	18	116.76
	400	4000	200	5	400	800	40	19.63	0.4	2.46	3F46	E13/6/3	0.26	22	2086	26	13	2	67.99	0.09	0.42	0.10	0.52	89.56	1.35	0.20	0.10	1.61	800	40	15.78	5.24	10.09	31.10	8.07	155.52	15	178.59
Limit to 10 modules	100	4000	200	7	100	622.2	31.1			1.24	3F46	E16/8/5	0.46	36	1671	23	23	1	75.5	0.11	0.46	0.33	0.79	89.06	3.6	0.75	0.12	4.45	622.2	31.11	6.03	2.75	4.76	13.5	31.2	94.5	21	146.65

Table G.10: Detailed weight study of the combination of RTC converter and the full-bridge inverter, corresponding to Fig. 5-11. The "peak current density" is calculated as the peak inductor current divided by the wire area, the average current density is smaller.

G.3.4 Specifications

Table II lists the components used in the resonant transition boost converter.

Category	Function	Manufacturer	Part Number	Note
Power stage	MOSFET	GaN Systems	GS66502T	Two in parallel
	Diode	Wolfspeed	C3D1P7060Q	Two in parallel
Inductor†	Core	TDK	N49	RM12
	Winding	MWS	48/1000 litz	6 turns
	Airgap	center-leg, 1 mm, milled with hand		
	Value	6.8 µH		
Gate driving	Comparator	Linear Tech	LTC6752-1	Added hysterisis resistor
	Current source	Toshiba	2SA1873	Used a 5.6 kΩ resistor to set the current to be about 5 mA, the ramp capacitor is about 220 pF
	Switch S_{ramp}	TI	SN74LVC1G06	
	NOR gate	Nexperia	74LVC1G27	
	OR gate	Diodes Incorporated	74LVC1G32	
	Gate driver	TI	UCC27611	
Logic	Linear regulator	On Semi	CAT6219	3.3 V output
	Microcontroller (MCU)	Microchip	PIC32MZ0512EFE064	
	Isolator	Broadcom	HCPL-0931	Provide isolation for UART communication
	Level shifter	TI	TXB0102DCUR	Shift MCU's 3.3 V logic to 5 V for gate driving
	DAC	Linear Tech	LTC2602	Output an analog voltage, controlled by the MCU through an SPI interface

Table G.11: Component list of the resonant transition boost converter
† This inductor is the one shown in Fig. 5-19a. A smaller inductor made with 3F46 material is under construction.

G.4 Implementation of the SCMLI

Table G.12 lists the specifications of the 11-stage SCMLI. This section focuses on 1) control of the converter. 2). several "unexpected" issues of this converter during implementation.

Category	Function	Manufacturer	Part Number	Note
Power stage	MOSFET	Infineon	IPN80R1K2P7	
	Diode	On Semiconductor	ES1J	The diode in series with switch A
	Flying capacitor	TDK	C4532X7T2 J304K250KA	3 capacitors stack in parallel†
Gate driving	Gate driver	Maxim	MAX17601	
	Digital isolator	TI	ISO7720FDWV	Use 2 per stage
	Isolated power supply	Analog Devices	ADuM6000	
	Isolated power supply for SA_{0-9}	Analog Devices	ADUM5028-5BRIZ	
Logic	Linear regulator	STMicroelectronics	L7806CV	9 - 6 V LDO
	Linear regulator	Diode incorporated	AZ1117E	5 - 3.3 V LDO
	Microcontroller (MCU)	Microchip	DSPIC33FJ256GP510	
	isolator	Broadcom	HCPL-0931	Provide isolation for UART communication
	Latch	TI	CY74FCT841T	Unused

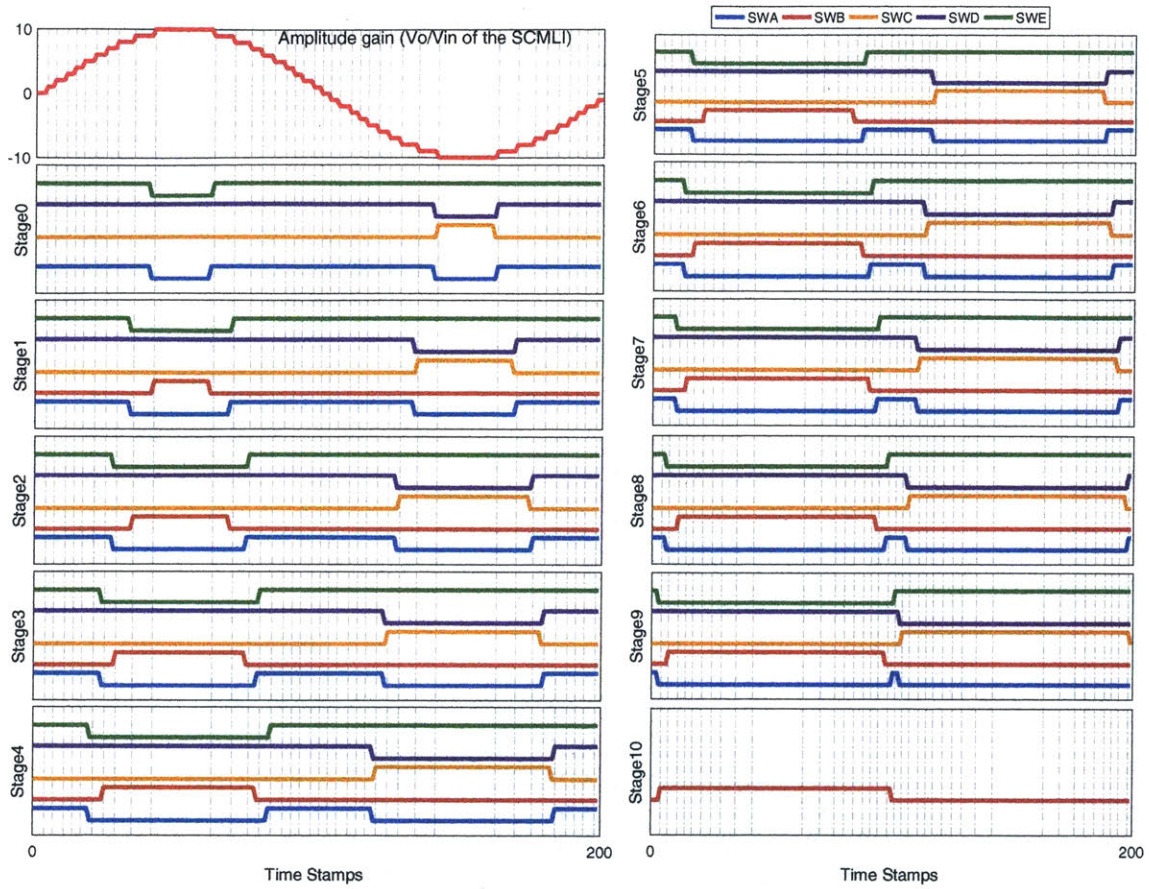
Table G.12: Component list of the 11-stage switched-capacitor multi-level inverter
† It is not necessary to use 0.9 µF capacitor. We have this for testing purposes.

G.4.1 Switching pattern and deadtime implementation

There are many ways to implement the switching sequence of this SCMLI topology. We choose the switching patterns in Fig. G-11 to ensure that the capacitor at each stage is connected to the input source for as long a time as possible — this makes sure the capacitors stay mostly charged, yielding a higher overall efficiency. For illustration purpose, the switching pattern without deadtime is listed in Table. G.13. The actual hardware runs the version with deadtime implementation.

Deadtime needs to be implemented between two "sets" of switching combinations as a transition. One way to implement the deadtime is to turn all switches off. The advantage is that this can be implemented in hardware circuit quite easily (for example, has a mux for each switching signal where one of the input to the mux is always connected to ground). However, the disadvantage is that the switching frequency is increased significantly. This seems not to be scalable if one wants to achieve higher output frequency.

Our implementation minimizes the times that a switch is switched in a cycle and



(a) Sine wave and Stage 0 to 4

(b) Stage 5 to 10

Figure G-11: Switching waveforms (with deadtime) of a 11-stage switched capacitor multilevel inverter when generating a sine wave. The switch label corresponds to Fig. 5-17. SWA to SWE corresponds to SA to SE of that stage.

avoids any possibilities that a capacitor in a stage is shorted during the deadtime. Capacitor in Stage i can be shorted when SB_{i+1} is on at the same time as SE_i (when $V_o > 0$), or when SD_i annd SC_i are on at the same time (when $V_o < 0$). We show two examples:

- Between Set 1 and Set 2 in Table G.13, $V_o > 0$, the capacitor in Stage 8 can be shorted at the transition, therefore we should turn off SE_8 first, then turn on SB_9. And these two steps should happen in order, not at the same time.

- Between Set 21 and Set 22 in Table G.13, $V_o < 0$, the capacitor in Stage 8 can be shorted, therefore we should turn off SD_8 first, then turn on SC_8.

Set	V_o	Stage No.										
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
0	0	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	-
1	V_{in}	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	D	B
2	$2V_{in}$	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	D	BD	B
3	$3V_{in}$	ADE	ADE	ADE	ADE	ADE	ADE	ADE	D	BD	BD	B
4	$4V_{in}$	ADE	ADE	ADE	ADE	ADE	ADE	D	BD	BD	BD	B
5	$5V_{in}$	ADE	ADE	ADE	ADE	ADE	D	BD	BD	BD	BD	B
6	$6V_{in}$	ADE	ADE	ADE	ADE	D	BD	BD	BD	BD	BD	B
7	$7V_{in}$	ADE	ADE	ADE	D	BD	BD	BD	BD	BD	BD	B
8	$8V_{in}$	ADE	ADE	D	BD	BD	BD	BD	BD	BD	BD	B
9	$9V_{in}$	ADE	D	BD	BD	BD	BD	BD	BD	BD	BD	B
10	$10V_{in}$	D	BD	BD	BD	BD	BD	BD	BD	BD	BD	B
11	$9V_{in}$	ADE	D	BD	BD	BD	BD	BD	BD	BD	BD	B
12	$8V_{in}$	ADE	ADE	D	BD	BD	BD	BD	BD	BD	BD	B
13	$7V_{in}$	ADE	ADE	ADE	D	BD	BD	BD	BD	BD	BD	B
14	$6V_{in}$	ADE	ADE	ADE	ADE	D	BD	BD	BD	BD	BD	B
15	$5V_{in}$	ADE	ADE	ADE	ADE	ADE	D	BD	BD	BD	BD	B
16	$4V_{in}$	ADE	ADE	ADE	ADE	ADE	ADE	D	BD	BD	BD	B
17	$3V_{in}$	ADE	ADE	ADE	ADE	ADE	ADE	ADE	D	BD	BD	B
18	$2V_{in}$	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	D	BD	B
19	V_{in}	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	D	B
20	0	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	-
21	$-V_{in}$	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	CE	-
22	$-2V_{in}$	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	CE	CE	-
23	$-3V_{in}$	ADE	ADE	ADE	ADE	ADE	ADE	ADE	CE	CE	CE	-
24	$-4V_{in}$	ADE	ADE	ADE	ADE	ADE	ADE	CE	CE	CE	CE	-
25	$-5V_{in}$	ADE	ADE	ADE	ADE	ADE	CE	CE	CE	CE	CE	-
26	$-6V_{in}$	ADE	ADE	ADE	ADE	CE	CE	CE	CE	CE	CE	-
27	$-7V_{in}$	ADE	ADE	ADE	CE	CE	CE	CE	CE	CE	CE	-
28	$-8V_{in}$	ADE	ADE	CE	CE	CE	CE	CE	CE	CE	CE	-
29	$-9V_{in}$	ADE	CE	CE	CE	CE	CE	CE	CE	CE	CE	-
30	$-10V_{in}$	CE	CE	CE	CE	CE	CE	CE	CE	CE	CE	-
31	$-9V_{in}$	ADE	CE	CE	CE	CE	CE	CE	CE	CE	CE	-
32	$-8V_{in}$	ADE	ADE	CE	CE	CE	CE	CE	CE	CE	CE	-
33	$-7V_{in}$	ADE	ADE	ADE	CE	CE	CE	CE	CE	CE	CE	-
34	$-6V_{in}$	ADE	ADE	ADE	ADE	CE	CE	CE	CE	CE	CE	-
35	$-5V_{in}$	ADE	ADE	ADE	ADE	ADE	CE	CE	CE	CE	CE	-
36	$-4V_{in}$	ADE	ADE	ADE	ADE	ADE	ADE	CE	CE	CE	CE	-
37	$-3V_{in}$	ADE	ADE	ADE	ADE	ADE	ADE	ADE	CE	CE	CE	-
38	$-2V_{in}$	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	CE	CE	-
39	$-V_{in}$	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	ADE	CE	-

Table G.13: Switching patterns without deadtime implementation of the SCMLI to synthesize a sine wave. This contains 40 sets of switching combinations and yields a longer charging time of capacitors in each stage. Each letter X means switch X in that stage is on ($X = A, B, C, D, E$), for example, "ADE" means switch SA, SD and SE of that stage are on. Reference to Fig. 5-17 for the switch labels.

G.4.2 Pin Map

Table G.14 presents the hardware mapping between the microcontroller and the switching signal of switches in each stage. We added hardware latches and "Latch Enable" pins thinking they could be useful in improving the coding efficiency, but they were not used in the experiments shown in this thesis.

Since there are more than 50 pins to switch, we first automate the coding process by MATLAB. We represent the information in Table G.14 in a port matrix and a pin matrix, as shown in Table G.15. The port matrix PORT and the pin matrix PIN are both a 5 by 11 matrix, the row of which is switch signal A through E, and the column of which is stage 0 to 10. We index PORTA to PORTG as 0 to 6; 7 in the port matrix indicates this port does not exist. Similarly we index pin using it's original pin number; 16 in the pin matrix indicates this pin does not exist. As an example, we want to switch all 11 stages of the inverter to generate a sine wave, the generated switching sequences are plotted in Fig. G-11.

The MATLAB code outputs a text file. We then copy the content of the text file to the microcontroller code main() function within the while(1) loop.

Stage n	**SWA_n**	**SWB_n**	**SWC_n**	**SWD_n**	**SWE_n**	**Latch Enable**
0	RD11	-	RD8	RD10	RD9	RF6
1	RD12	RD1	RD0	RD3	RD2	
2	RD7	RD4	RD13	RD6	RD5	RF7
3	RE0	RG0	RG1	RA7	RA6	
4	RE2	RG14	RE1	RG13	RG12	RF8
5	RE7	RE4	RE3	RE6	RE5	
6	RA0	RG7	RG6	RG9	RG8	RF2
7	RB3	RA13	RA12	RB4	RB5	
8	RB7	RB1	RB2	RB6	RB0	RF3
9	RB11	RB8	RA9	RB10	RB9	
10	-	RA1	-	-	-	-

Table G.14: Mapping between microcontroller pins and switching signals to each stage. Same colored blocks are controlled by the same latch, the enable pin of which is listed in the "Latch Enable" column.

$$PORT = \begin{bmatrix} 3 & 3 & 3 & 4 & 4 & 4 & 0 & 1 & 1 & 1 & 7 \\ 7 & 3 & 3 & 6 & 6 & 4 & 6 & 0 & 1 & 1 & 0 \\ 3 & 3 & 3 & 6 & 4 & 4 & 6 & 0 & 1 & 0 & 7 \\ 3 & 3 & 3 & 0 & 6 & 4 & 6 & 1 & 1 & 1 & 7 \\ 3 & 3 & 3 & 0 & 6 & 4 & 6 & 1 & 1 & 1 & 7 \end{bmatrix}$$

$$BIT = \begin{bmatrix} 11 & 12 & 7 & 0 & 2 & 7 & 0 & 3 & 7 & 11 & 16 \\ 16 & 1 & 4 & 0 & 14 & 4 & 7 & 13 & 1 & 8 & 1 \\ 8 & 0 & 13 & 1 & 1 & 3 & 6 & 12 & 2 & 9 & 16 \\ 10 & 3 & 6 & 7 & 13 & 6 & 9 & 4 & 6 & 10 & 16 \\ 9 & 2 & 5 & 6 & 12 & 5 & 8 & 5 & 0 & 9 & 16 \end{bmatrix}$$

$ENABLE_{PORT} = [5 \quad 5 \quad 5 \quad 5 \quad 5]$ $\qquad$ $ENABLE_{BIT} = [6 \quad 7 \quad 8 \quad 2 \quad 3]$

Table G.15: PORT and PIN matrix generated from Table G.14.

G.4.3 Achievable frequency

In the microcontroller code, we use the simplest for-loop in the main function to implement the switching pattern. An example assembly code is shown in List. G.1. Our microcontroller speed is 40 MIPS and consider each assembly command takes on average 2 instruction cycles. All switching commands (80 sets including deadtime) take $7 \times 200 + 9 \times 80 \sim 2120$ commands, which takes $2120 \times 2 = 4240$ instruction cycles. Therefore it should take about $4240/40000000 \sim 1.0 * 10^{-4} sec$, meaning 10 kHz is the highest achievable output frequency under these constraints.

Listing G.1: Pieces of C code compiled in assembly language

```
158:                          for (i = 0; i < 200; i++) {
CLR W0
MOV #0xC7, W3
INC W0, W0
SUB W0, W3, [W15]
BRA LE, 0x1C60
MOV W5, W0
BRA 0x1C60

160:                              if (i == StoredTime[count])
MOV #0xB22, W4
ADD W1, W1, W2
MOV [W4+W2], W2
SUB W2, W0, [W15]
BRA NZ, 0x1C86
161:                              {
162:                                  LATA = StoredLATA[count];
MOV #0x802, W11
ADD W1, W1, W2
MOV [W11+W2], W12
MOV W12, LATA
```

At the time of writing, Suzanne O'Meara is working on upgrading the codes to

further increase the frequency of the waveforms. Options include 1) more efficient coding. 2) identify complementary pairs of switches and use MCU's PWM function to drive them rather than IO. 3) a faster MCU.

G.4.4 Issue with the SCMLI

Voltage build-up issue

During the testing, we found there are voltage build-up issues on switch A in Stage 1 to 9 (see Fig. G-12 and Fig. G-13a). This severely increases the drain-to-source voltage of switch A and can cause voltage overshoot.

We identified the reason as: the stray capacitance to ground (including PCB traces, capacitance inside the gate driver and isolator) at the source node of switch A injects charges to switch A at certain switching transitions, resulting in the voltage build up. Figure. G-14 shows a step by step explanation of what causes the bump on SA_1. Following similar analysis, one can deduce how the voltage bumps across SA_{2-9} are formed. We developed equations of the amplitude of one "bump" as:

$$\Delta V_{DS} = \frac{C_{P_1}}{C_{Diode} + C_{P_1} + C_{oss}} V_2$$

Where C_{oss} is the body capacitance of SA_1, C_{Diode} is the body capacitance of the diode, and C_{p_1} is the parasitic capacitance from the source of FET A to ground. V_1 is the voltage across the flying capacitor in stage 0. Corresponding to Fig. G-13a, $V_2 =$ 200 V, $C_{oss} = 8$ pF, $C_{Diode} = 12$ pF, $C_{P_1} = 5$ pF, therefore each bump is ~40 V.

One measure to reduce the size of the bump is to increase C_{Diode} and/or C_{oss}. In Fig. G-13b, we added a 100 pF across all switch A, each bump reduces from 46.4 V to 11.6 V and the maximum V_{DS} across SA_9 reduces from 642 V to 298 V.

Thermal issue with the SCMLI

In addition to the voltage build-up issue, we also see severe heating on some of the MOSFETs, especially in the first few stages. Please see Suzanne O'Meara's master thesis for more explanations and solutions.

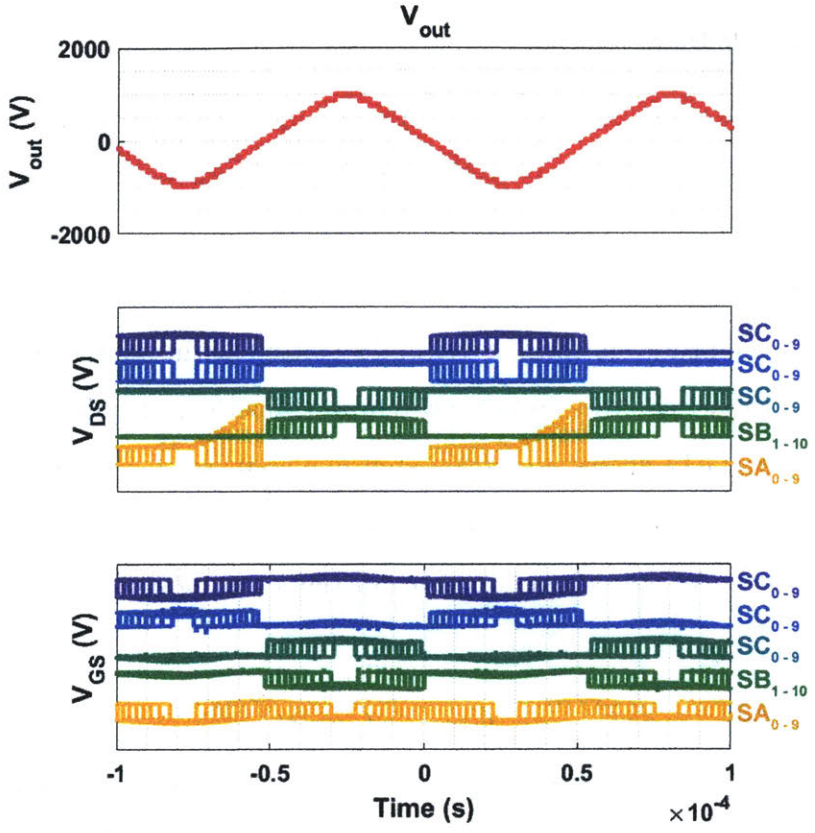
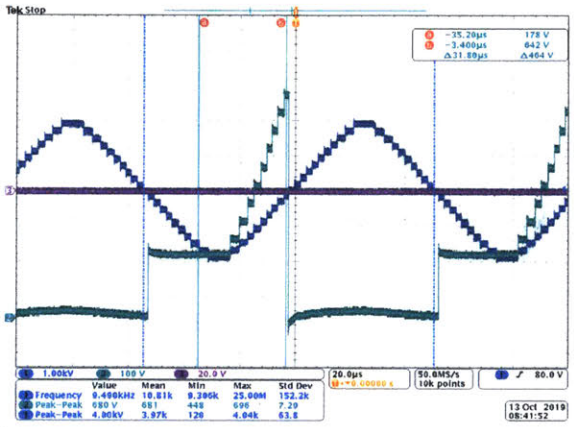
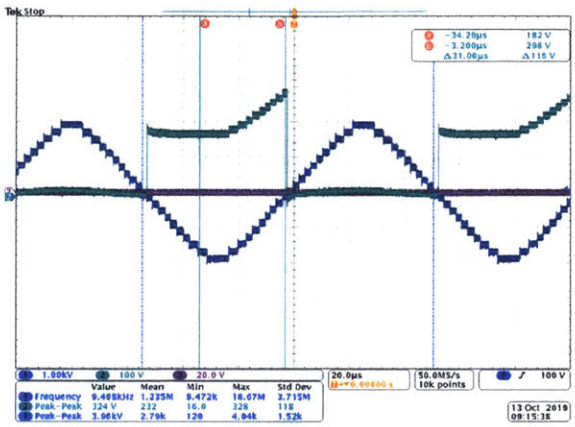


Figure G-12: The voltage build-up issue of FET A in all stages: the gate-to-source voltage V_{GS}, drain-to-source voltage V_{DS} of all 50 switches are measured with differential probes and theirs oscilloscope waveforms are plotted together here. The output waveform V_o is measured and used to synchronize all plots. V_{DS} of every switch A has a stair-case-like "voltage bump" at the transition when V_o changes from $-10V_{in}$ to 0. The higher number of stages, the more bumps there are (i.e., SA_9 has 9 bumps whereas SA_2 has 2 bumps.)

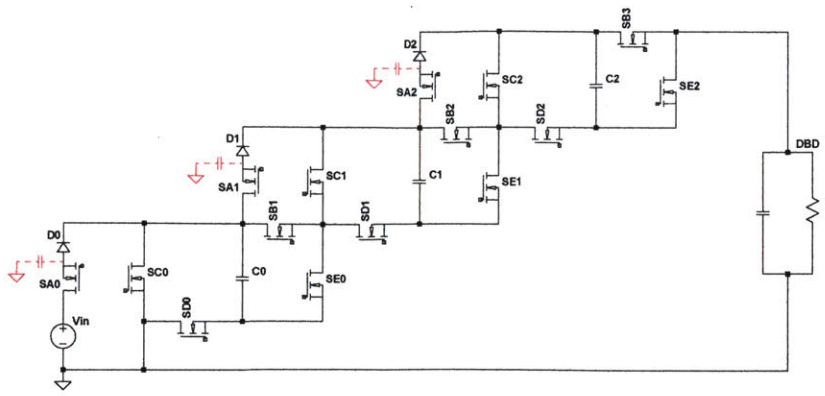


(a) Before adding external capacitors. Each voltage bump is ~46.4 V and the maximum V_{DS} across SA_9 reaches 642 V.

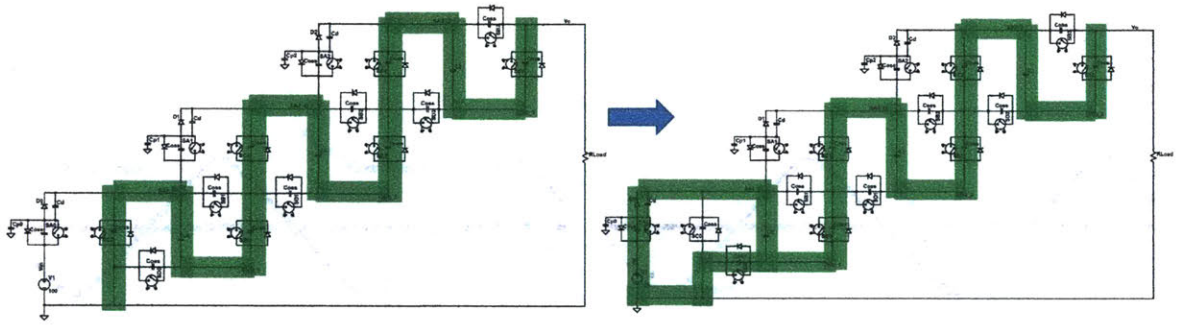


(b) After adding external capacitors. Each voltage bump is ~11.6 V and the maximum V_{DS} across SA_9 is reduced to 298 V.

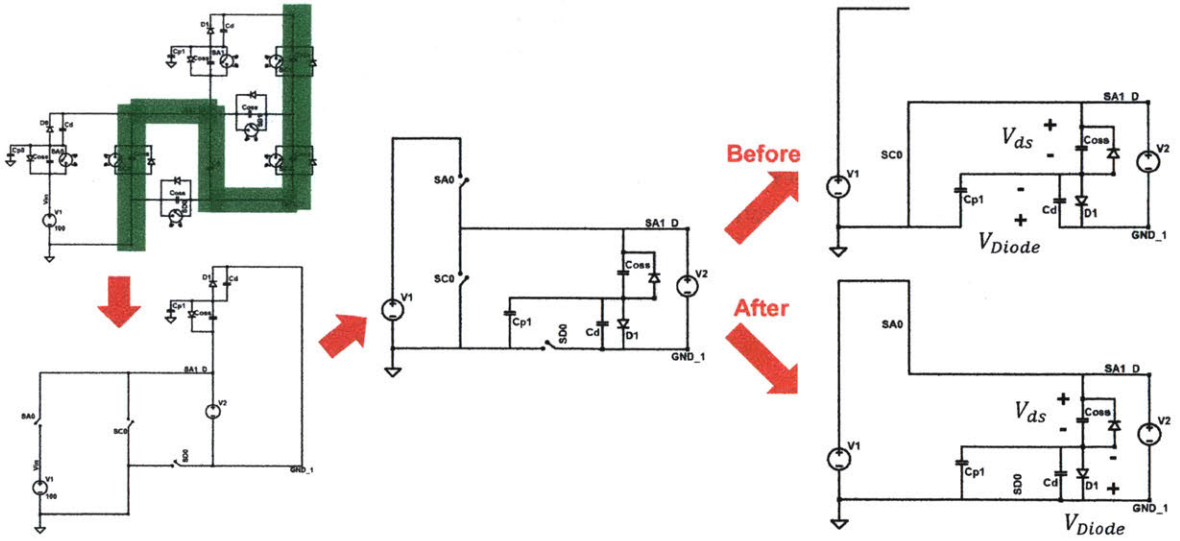
Figure G-13: Oscilloscope screenshots of V_{DS} of SA_9 before (a) and after (b) adding a 100 pF capacitor across all switch A. In both subplots, the converter takes an input of 200 V and converts to an ~2 kV 10 kHz ac. CH1: the output waveform of the SCMLI; CH2: V_{DS} of SA_9.



(a) Parasitic capacitance at the source of each switch A to ground in a 4-stage SCMLI.



(b) The transition when V_o changes from $-10V_{in}$ to $-9V_{in}$. The green highlighted path indicates the conducting switches.



(c) Simplify Stage 0 and Stage 1 of the SCMLI. Before and after the transition, the parasitic capacitance C_{p_1} is stacked first in parallel with SA_1, then in parallel with the diode D_1. C_{oss} is the body capacitance of SA_1, C_{Diode} is the body capacitance of the diode, C_{p_1} is the parasitic capacitance from the source of FET A to ground, V_2 is the voltage across the flying capacitor in Stage 0 (since this capacitor is big (0.9 µF), we assume it acts as a voltage source).

Figure G-14: Explanation of the voltage build up issue in a 4-stage SCMLI

Appendix H

Collaborative work on EAD

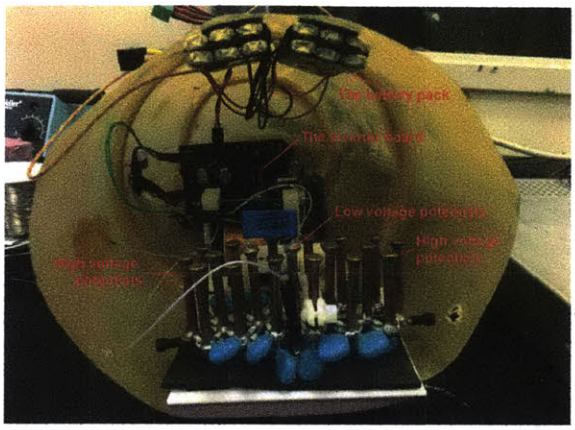
H.1 Integration of the 1st-gen HVPC and EAD

Before every flight test, the following integration tests were conducted in order to ensure the safety and the functionality of all sub-systems:

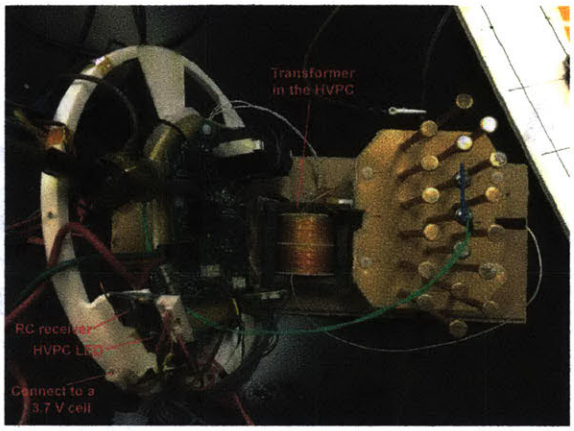
- Benchtop, the HVPC powers a 50 mm-span small EAD thruster at 30 kV.
- Benchtop, the battery pack and the HVPC power a 300W resistor bank at 40 kV.
- Benchtop, the battery pack (or a dc-dc power supply KLP-300-4) and the HVPC power the full-scale EAD thruster from 0 to 40 kV to verify the static thrust generation (see "static thrust tests" in Chapter 6).
- Benchtop, test for the insulation clearance in the fuselage. The battery and the HVPC are mounted in the fuselage and power the vertically suspended full-scale thruster at 40 kV.
- The battery pack and the HVPC are assembled in the fuselage and the whole aircraft is suspended vertically in the insulating frame. The HVPC powers on at 40 kV for at least 30 s to simulate the actual flight test.

Mounting structures for the battery pack and the HVPC can quickly add up the

weight. Extra cares were taken to mount the voltage multiplier (VM) in the HVPC because it is at high voltage potentials and has high localized electric fields.



(a) Back view of the 1st version fixture. A structure made from 3D printed ABS material fixes both the transformer and the VM on the same base plate. The base plate is then mounted on fuselage with a piece of foam sandwiched in between to provide some suspension. The fixture is only in contact with the VM at two lower voltage potentials.



(b) Top view of the final version fixture. A Kevlar plate was used to fix all heat pipes of the VM and screwed down to the fuselage. The kevlar is in contact with the VM at high voltage potentials, but since the Kevlar has higher dielectric-strength than ABS, no arcing or decrease in the converter efficiency or degradation of the fixture was observed.

Figure H-1: Mounting the battery pack and the high voltage power converter (HVPC) in the nose cone (with help from LAE colleagues).

The final assembled prototype is shown in Fig. H-1b. A Kevlar plate with holes to fix all heat pipes of the VM in place was used and screw-mounted to the bottom of the fuselage. The battery packs were taped to the celling of the nose cone. To save sapce, the inverter board of the HVPC were screw mounted on a vertical plate orthogonal to the bottom of the fuselage. The transformer was mounted with four small pieces of ABS plastics fixing its four corners.

When all subsystems were assembled, one can see from the outside of the fuselage the RC receiver, the HVPC LED indicator, and a port to connect to a 3.7 V battery cell that powers the logic of the HVPC, as shown in Fig.H-2.

Several suggested improvements on the HVPC are concluded from the tests:

- Address thermal concerns of the HVPC. We observed intensive heating of the MOSFETs in the inverter and were not able to keep running the HVPC after

Figure H-2: The assembled EAD aircraft sitting on the launcher. The HVPC LED indicator turns green when high voltage (HV) off, blue when charging the input caps and red when HV on. The emergency switch mounted at the bottom of the fuselage is in-line with the logic power to the HVPC. Landing triggers it and cuts off the logic power.

60 s. For future generation EAD aircrafts, the team will very likely target at extended flight time and longer distance. Thus the thermal issues of the HVPC should be resolved through 1) identifying the conduction and the switching loss of the GaN MOSFET, 2) using new GaN MOSFETs that can yield to a lower total loss, and/or 3) implementing better thermal management solutions.

- Increase the robustness and reduce the build complexity of the voltage multiplier. The voltage multiplier and its heat pipes were easily damaged in the tests, due to arcing, collisions, etc. Significant time was spent on repairing and rebuilding it. We propose to improve the robustness of the voltage multiplier in the 2nd-gen HVPC by 1) using lower-loss diodes and removing heat pipes. and/or 2) designing the voltage multiplier on a PCB. See Chapter. 4 for details.

- Develop a smarter data collection system. In the flight tests, two sets of microcontroller codes are flashed to the HVPC alternatively: one to run the HVPC during flight, another to read data off the on-board FRAM after each run. A

more automated data-collection system is desirable. Undergraduate students Luka Govedic and Pedro Acosta have started developing a RF-based data collection/communication system (see Section H.3) but more future efforts are needed.

H.2 Second generation EAD thruster

H.2.1 Thrust Measurement Setup

The thrust produced by thrusters were measured by hanging the system vertically from a Sartorius Entris 4202 balance with 10 mg resolution. A reduction in the measured 'weight' is equivalent to the thrust produced by the EAD device. The emitters and collectors were built on a glass fiber reinforced polymer (GFRP) rectangular frame which was 500 mm wide by 600 mm. The electrode span was 500 mm. Figure H-3 shows a photo of the DBD setup when the high voltage AC is applied.

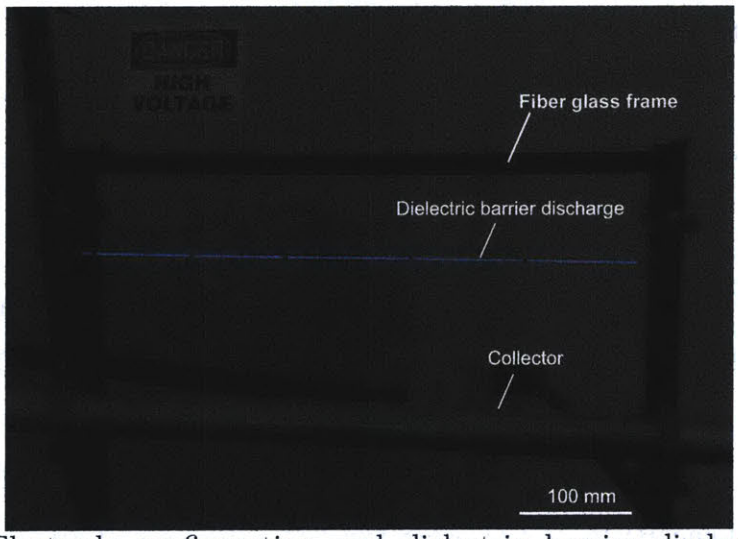


Figure H-3: Electrode configuration and dielectric barrier discharge ion source (V_{AC} =3 kV, f =10 kHz). The electrodes are fixed on a glass fiber frame and hung from a balance.

In our analysis, we do not include the effect of aerodynamic drag on the electrodes, and assume that this is small relative to the EAD thrust force.

H.2.2 Electrical System and Measurement Setup

The AC high voltage was generated by two different supplies. For frequencies of 20–150 kHz, a Redline Technologies Plasma Generator G2000 was used. The G2000 operates by resonating its internal inductance with the load capacitance and does not provide an internal matching network. Therefore, a set of fixed-value and tunable high voltage capacitors are connected in shunt with the DBD load to adjust the resonant frequency and the peak voltage (see Fig. H-4 and a list of capacitors in Table. H.1). The capacitance was adjusted on the fly during each test until the frequency and the voltage reach the desired value. For frequencies less than 20 kHz, a Trek 664 amplifier driven by a Agilent 33250A waveform generator was used. In both cases, the waveform was sinusoidal.

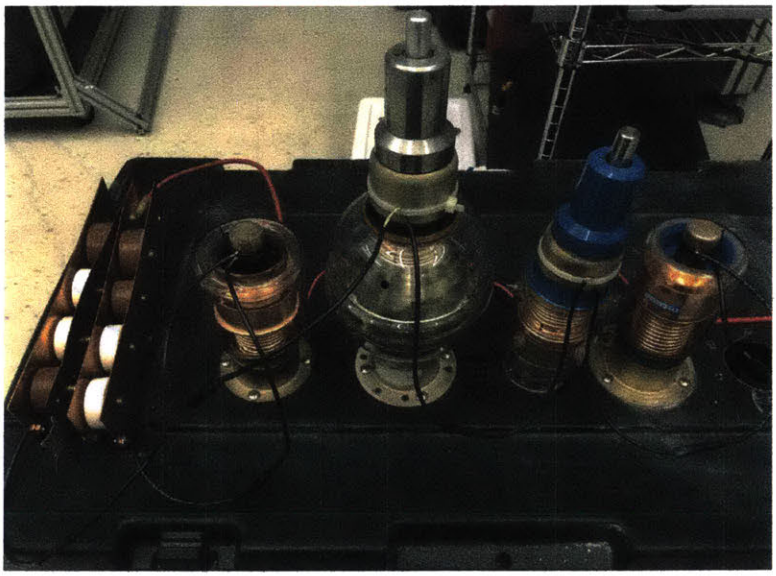


Figure H-4: Fixed and tunable high voltage capacitor setup

The DBD voltage was measured using a Tektronix 6015A high voltage probe. To measure the current of the DBD, a NP0 2.2 nF capacitor was connected in series with the DBD electrode. The voltage across this capacitor was measured using a Tektronics P2200 10x passive probe. The charge in the capacitor, which is calculated by multiplying the voltage and the capacitance, is the integral of the DBD current and was used to calculate the power draw, similar to Kriegseis et al. [128]. A Tektronix DPO2024B oscilloscope was used to read the measurements from both probes. Fig-

Supplier	Manufacturer	P/N	Capacitance	Rated voltage
Max-Gain System Inc.	Jennings	U-300-20S	10–300 pF	20 kV
		UCS-300-15S	10–300 pF	15 kV
		Capacitor holders: MGSFM-2, MGSFM-2D, MGSFM-0B		
	Dolinko & Wilkens	VVC-100-42-20	10–100 pF	20 kV
Digikey	TDK	UHV-2A	2500 pF	20 kV
		UHV-224A	1000 pF	20 kV
	Murata	DHS4E4C192MLXB	1900 pF	15 kV

Table H.1: Fixed and tunable high voltage capacitors used in the decouple thruster tests.

ure H-5 shows the oscilloscope waveform and the Lissajous loop of the DBD voltage and the DBD charge. We also tried to measure the current with a precision resistor, which did not yield to consistent and accurate readings because the plasma current was too noisy.

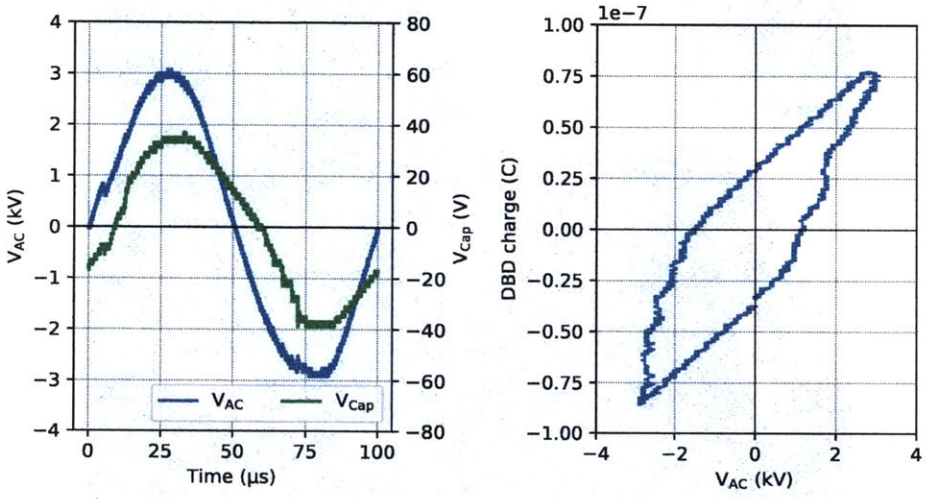


Figure H-5: Oscilloscope waveform of DBD voltage and the voltage across a 2.2 nF measurement capacitor and the according Lissajous loop (V_{AC} =3 kV, f =10 kHz)

A Matsusada AU120-N was used to apply the DC voltage V_a across the emitter and the collector. Note that in both of the devices tested, the collector was biased at a negative potential while the emitter was held at ground potential. In a flying airplane, the emitter would be biased positive relative to ground, and the collector negative to ground in a "floating" configuration. Operating in the floating configuration reduces non-ideal effects such as leakage current to the surroundings [6], but we were constrained to the "negative" configuration due to the use of a bench-top

AC supply with a common ground with the DC supply. The floating configuration is preliminarily explored in Section H.2.3 and will be studied in details in the future using battery-powered AC supplies.

H.2.3 Isolation transformer for testing the decoupled thruster at a floating potential

Work by colleagues in [6] shows that the thrust generated when the emitter is biased at the ground potential can be 25% less than that generated when the collector is grounded (even when the potential between the emitter and the collector is held the same)[1]. Changing the potential of the device to its surroundings changes the electric field distribution around the thruster, and therefore its current and thrust characteristics.

We expect the same effect for the decoupled thruster. Therefore, the potential of the thruster to surroundings should be controlled at a floating potential (usually half of the dc applied voltage) to simulate the actual flying condition.

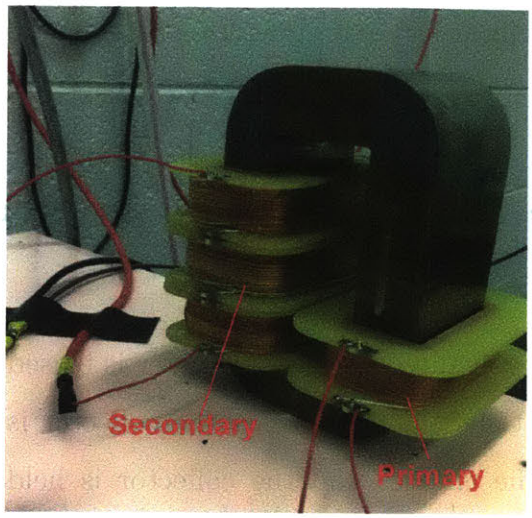
A high voltage transformer that can provide up dc isolation between the primary and the secondary is built and provides dc isolation between the bench-top ac power supplies and the DBD electrodes. The transformer and the wiring diagram is shown in Fig. H-6. The specifications of the transformer is listed in Table. H.2.

The transformer was able to provide up to 60 kV isolation. After 60 kV, the sharp point at the inter-section pin and jack connector starts to have streamers and potential arcing. Preliminary thrust tests show that biasing the decoupled thruster at a positive potential yields to a higher thrust, consistent with [6].

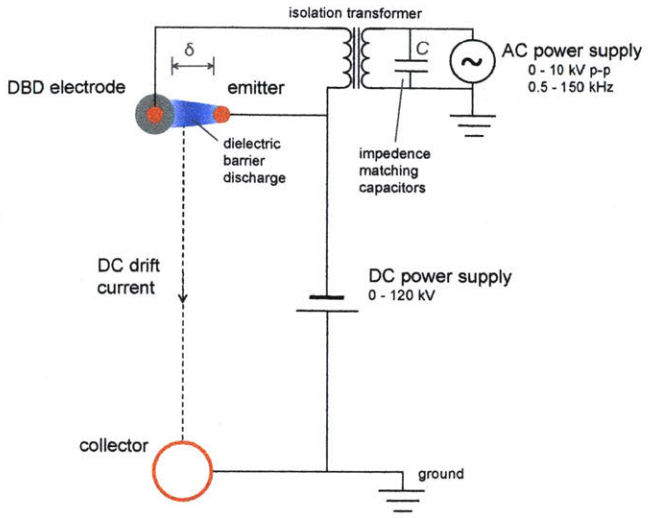
H.2.4 μA current measurement

Work by colleagues in [6] also quantifies the leakage current (the difference between the current going to the emitter and the collector) and analyzes its effect on the thruster characteristics. Currents going to both electrodes need to be measured. However, the bench-top high voltage power supply only has its internal current measurement

[1]This result is tested with the surrounding at least 2.5 m away from the EAD device.



(a) Isolation transformer



(b) Wiring diagram of the isolation transformer

Figure H-6: Using an isolation transformer to test the decoupled thruster at a floating potential to ground. The "impedance matching capacitors" are the fixed and tunable capacitor set in Fig. H-4.

Function	**Parts**	**Manufacturer**	**P/N**	**Note**
Core		Hitachi	AMCC 500	Metglas series
Same in the primary and the secondary	Wire	Teledyne Reynolds	178-5790	FEP 18kV wire
	Bobbin plate	Made from bare-bone 62 mil FR4 PCB. Glued to the bobbin insulation sleeve.There are copper areas on one edge of the plate where the winding terminal of this section is soldered to. †		
	Bobbin insulation sleeve	McMaster	A U-channel and a sheet of Arc-Resistant GPO3 Fiberglass are glued together using epoxy to form a square shape sleeve. The core is put through this sleeve. Each sleeve section is 2-9/16" long, 1-1/4" wide, 1" high, and 1/16" thick.	
	inter-section pin and jack	Keystone	1361-2 and 1682	Electrically connect the windings in two sections
Turns	Primary to Secondary is 57 to 342 (1:6)			

Table H.2: Specifications of the isolation transformer. († See the layout in Fig. I-6.)

on the "high" line but not the ground return.

In addition, many corona EAD devices and decoupled EAD devices tested in lab have a span of 10–750 mm, much shorter compared to the full-scale thruster on the aircraft. They operate between 10 to 80 kV and draw between 1 to 100 µA of current.

To measure the μA-level ground current, an independent current measurement circuit was made following the design in [154]. The collector is connected to ground through a 6.8 Ω precision resistor, the voltage across which is multiplied with an operational amplifier and read with a digital multimeter Agilent 34410A. See the specifications in [154].

H.3 Data collection and RF communication system

A smarter and real-time data streaming and control system is desired for the second-generation EAD aircraft including the following functionalities:

- Real-time adjust the voltage thus the thrust through controlling the 1st-gen HVPC
- Automated data collection system without manually copying after every flight
- Combine the electrical data collection and the acceleration data collection.

We plan the system to include three parts: an onboard embedded system for data collection, an onboard communication module, and a base station with a pairing communication module and real-time data plotting function. Undergraduate students Luka Govedic and Pedro Acosta have started the work.

A radio-based communication system was selected compared with the cellular for its 1) shorter latency (~5 ms vs ~100 ms), 2) lower power consumption (tens to a hundred of mA vs hundreds of mA), 3) less tendency to lose the signal (but might need line of sight)[2] and 4) reasonable bandwidth (hundreds of kbps vs 10 Mbps). A test-version data collection embedded system with microcontrollers and sensors were built. See Table H.3 for the parts and the testing progress. Future work include 1) finishing testing all the sensors 2) integrating the RF module with the embedded system and setting up a communication protocol. 3) coding a user-interface for the base-station to receive and send data.

[2]RFM69 has a expected range of ~ 500 m. Suggest testing in the future.

Function	Parts	Supplier	P/N	Progresss
Communi-cation	RF receiver and transmitter	Sparkfun	RFM69	Tested†
Data collection	Microcontroller	Microchip	PIC32MZ2048EFG064	Tested
	IMU sensor	ST	LSM9DS1	Not tested
	Micro SD holder	Adafruit	-	Not tested
	Micro SD card	Samsung	MB-ME128GA/AM	Not tested

Table H.3: Specifications and testing progress of the data collection/RF communication.
† Both receiving and transmitting functions are tested between two RFM69 modules on the bread board with two Teensy 3.6 as their command computers. The same setup was tested with the DBD powered on 1 m away and no obvious interference was observed.

Appendix I

PCB schematics and layouts

All PCBs are designed in Altium Designer. The Altium files and libraries can be found in the following Dropbox link: `https://www.dropbox.com/sh/qsi96p8vou5uma8/AACujlDNVSEbD-ivW04FJHtIa?dl=0`

Please email yiouhe@gmail.com if you have any questions.

This section lists the screen shots of PCB schematics and layouts:

- 1st-gen high voltage dc-dc converter
- boards for diode evaluations
- resonant transition boost converter
- switched-capacitor multilevel inverter
- boards for the isolation transformer built for EAD experiments in Section H.2.3

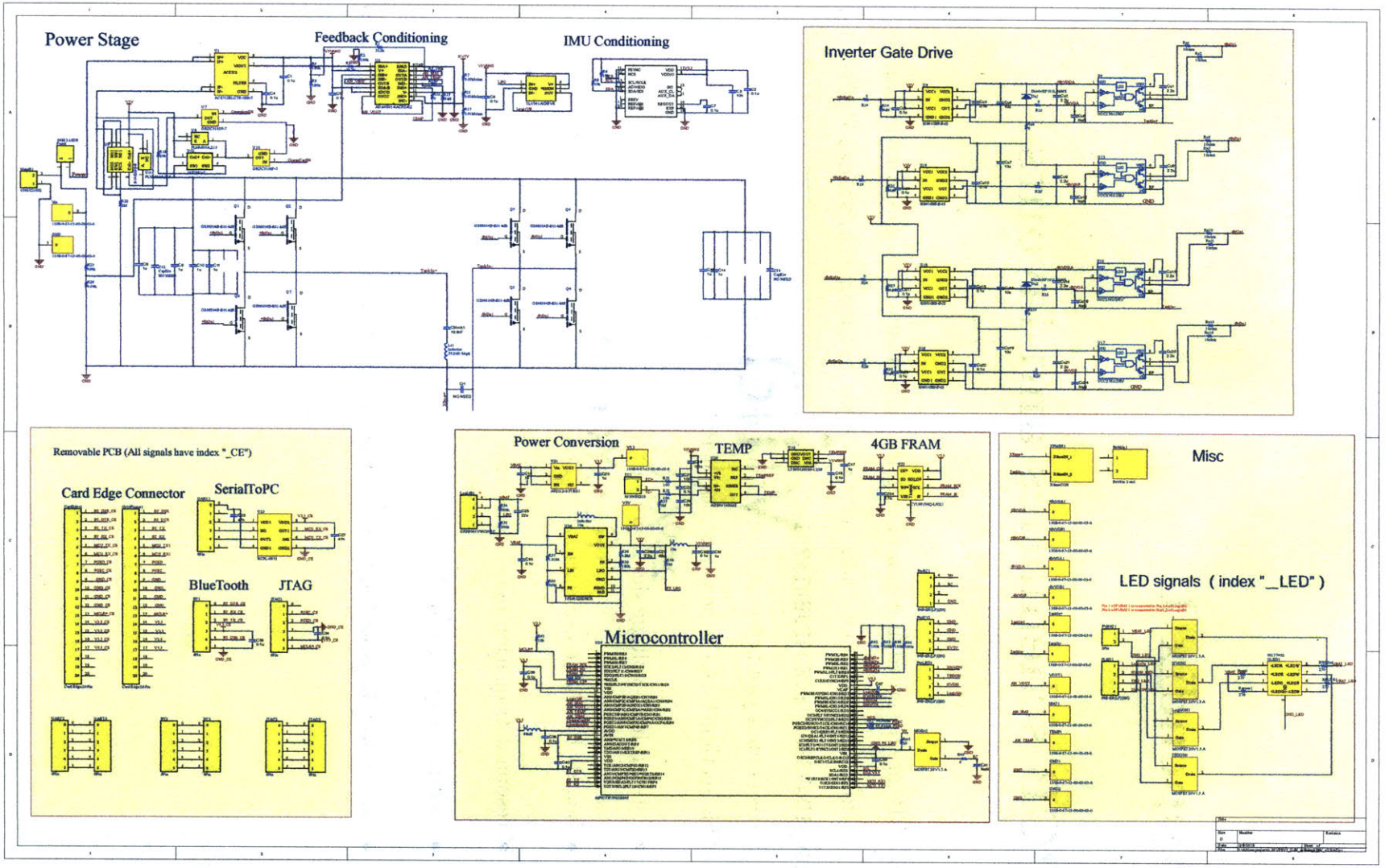
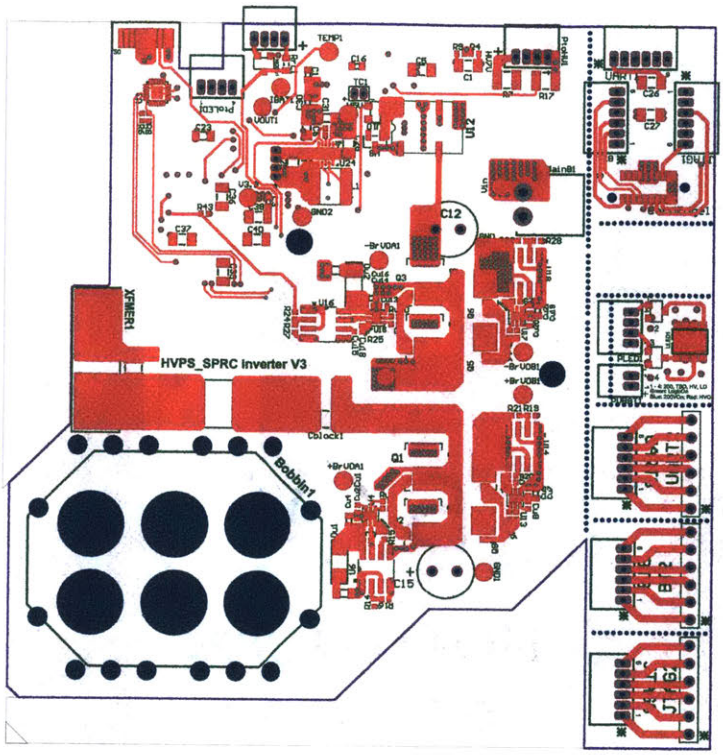
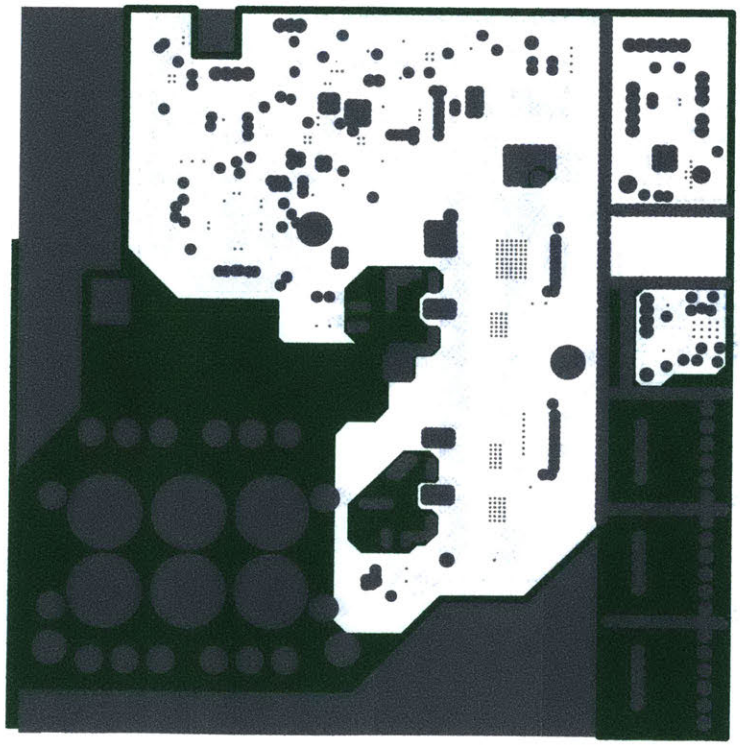


Figure I-1: 1st-gen HVDC schematic

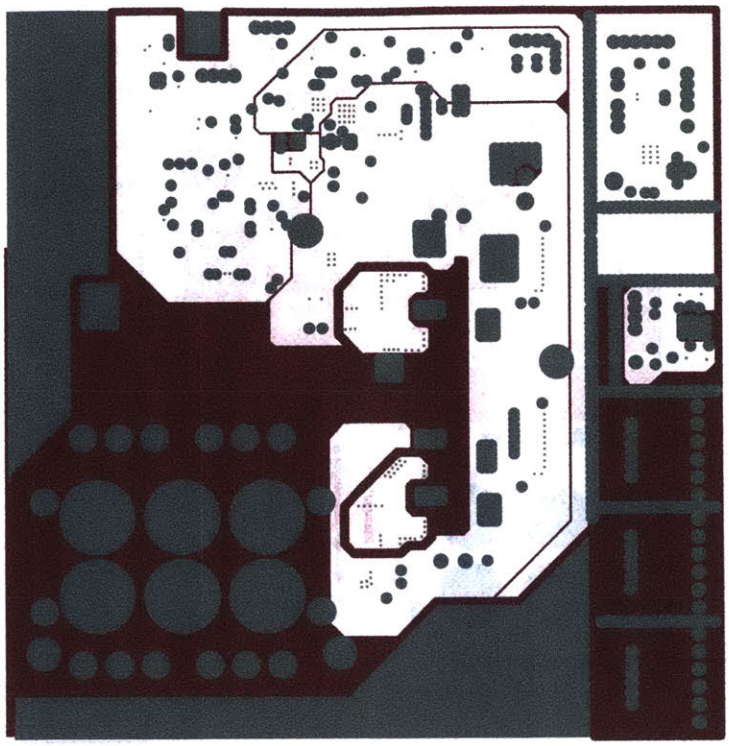


(a)

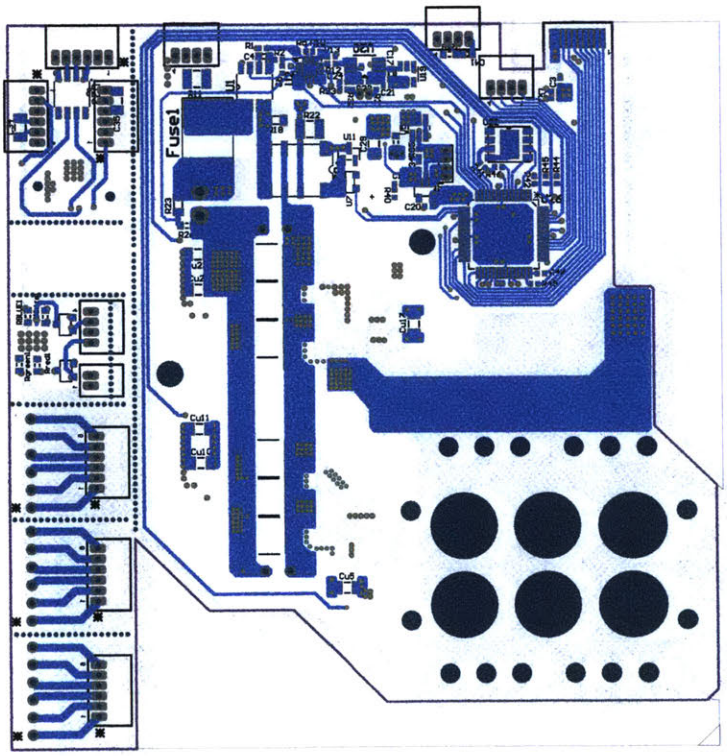


(b)

Figure I-2: PCB layout of 1st-gen HVDC (a) Top layer, (b) 2nd layer

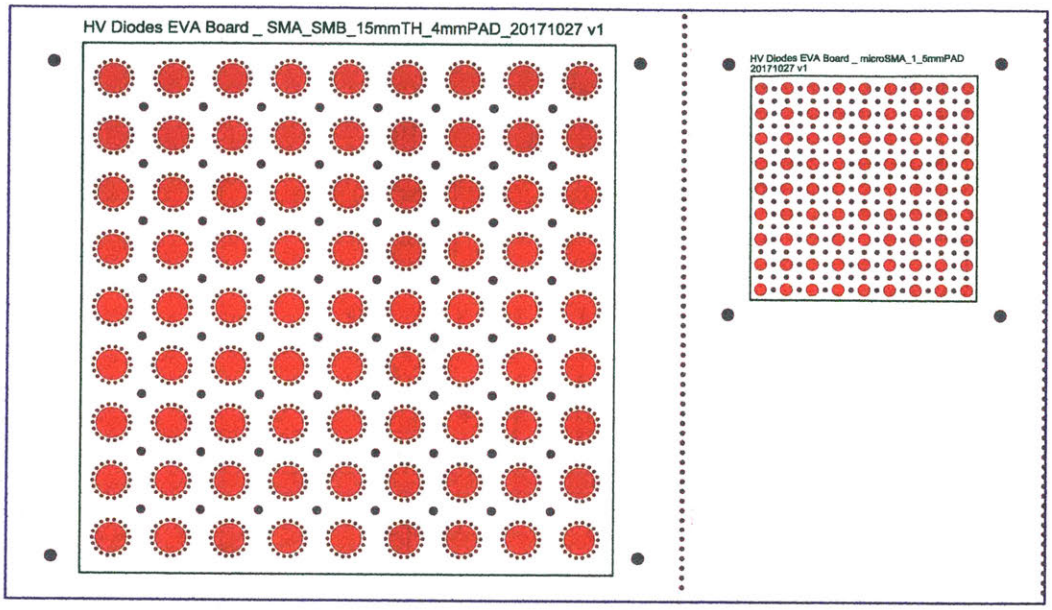


(c)

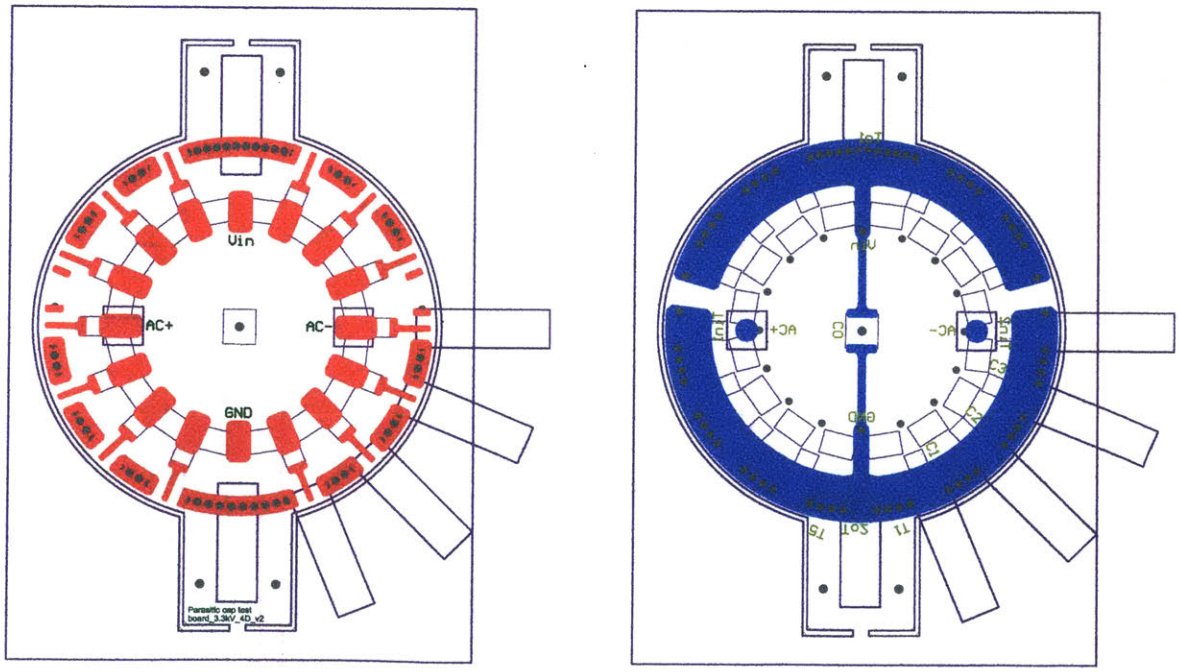


(d)

Figure I-2: PCB layout of 1st-gen HVDC (a) Top layer, (b) 2nd layer



(a)



(b)

(c)

Figure I-3: PCB layouts for diode evaluation and series diode balancing tests. a) The PCB layout of the left and middle board in Fig. E-1. b) and c). Top and bottom of the PCB layout of the board used in the diode evaluation (the right board in Fig. E-1) and for experiments in Section 3.4.

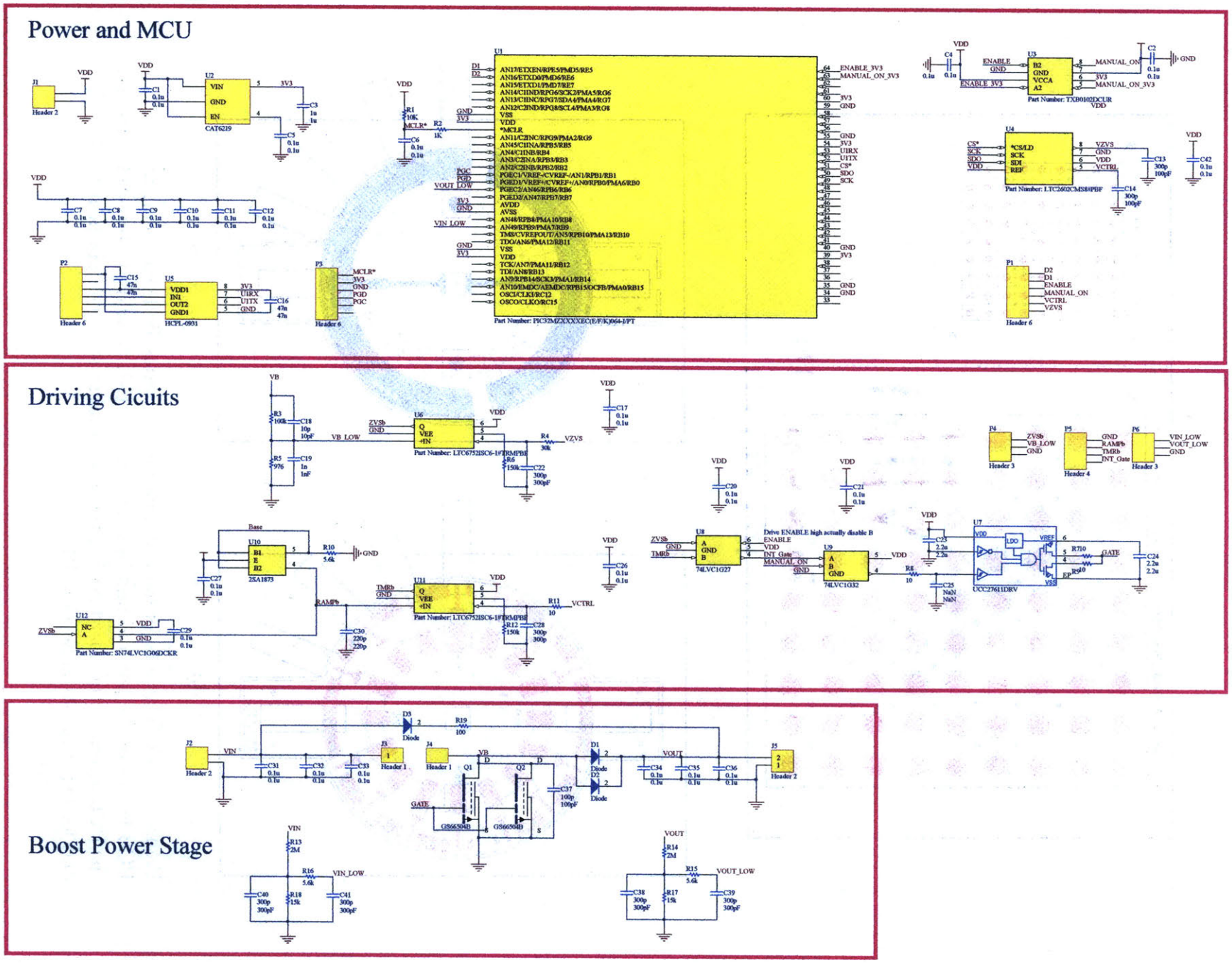
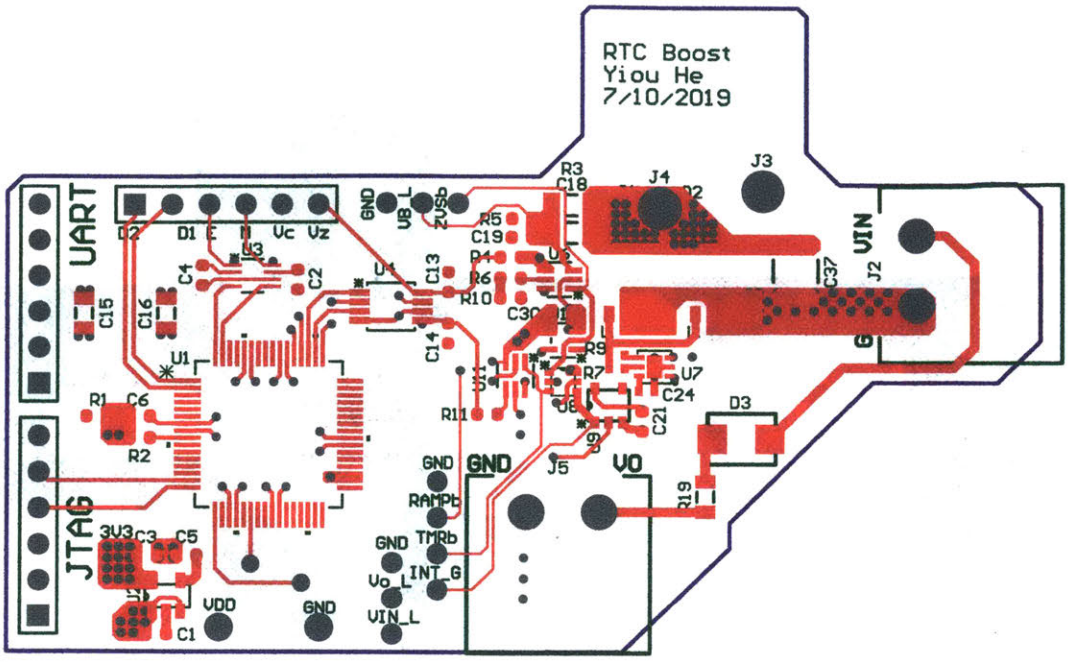
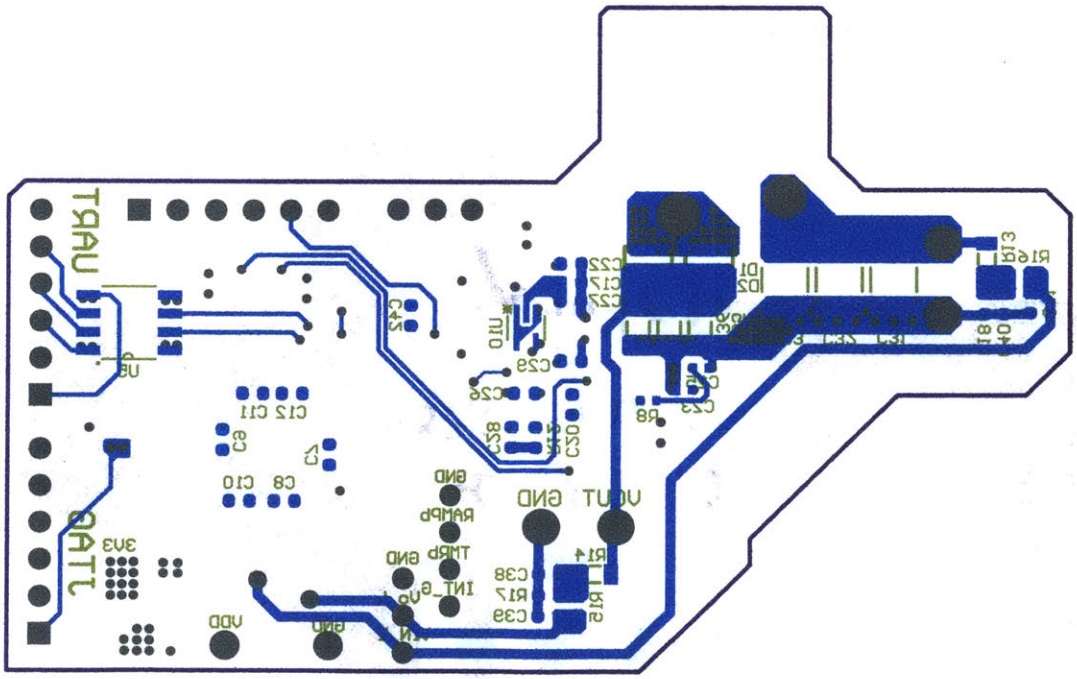


Figure I-4: RTC boost schematic

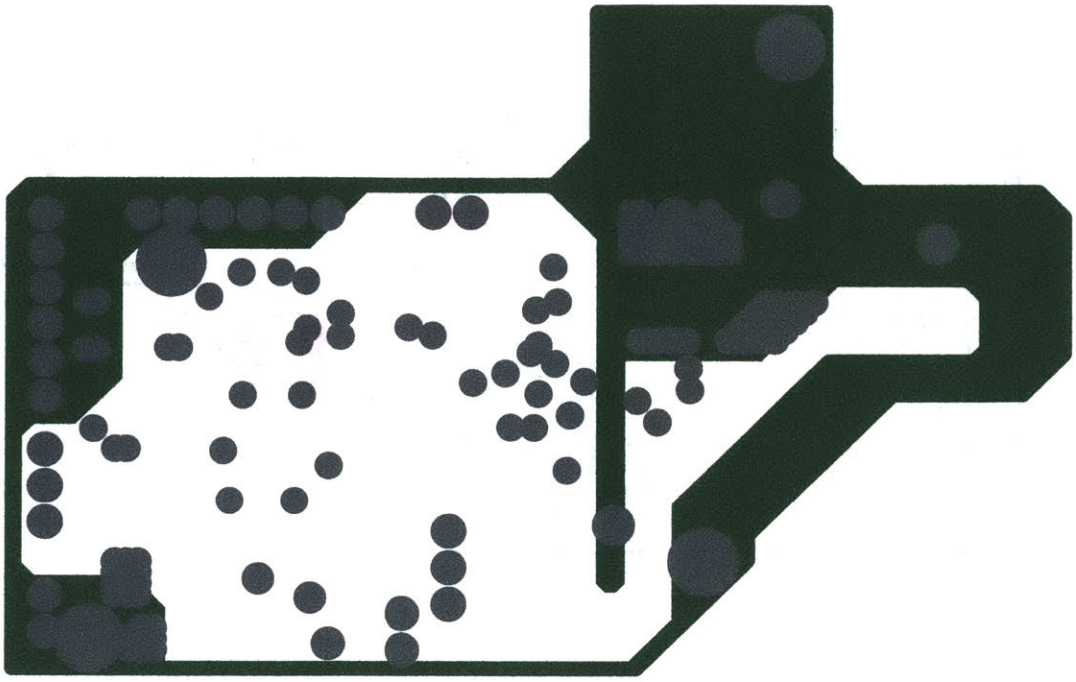


(a) Top layer

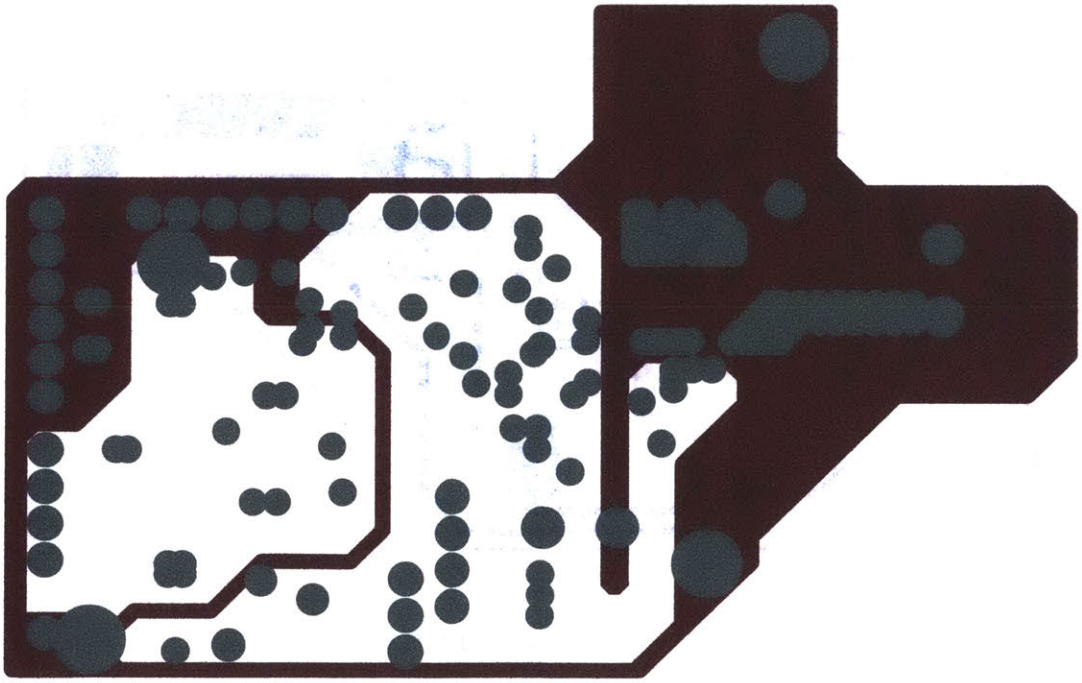


(b) Bottom layer

Figure I-5: RTC boost PCB layout

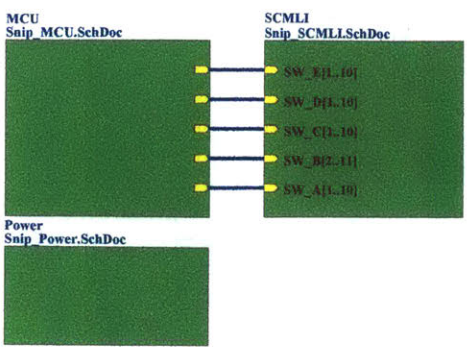


(c) Second layer (ground, negative)

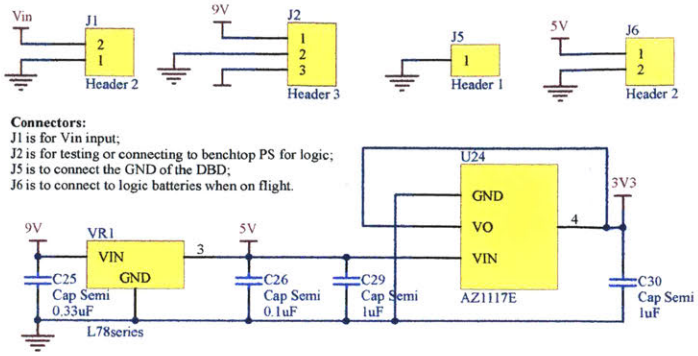


(d) Third layer (power, negative)

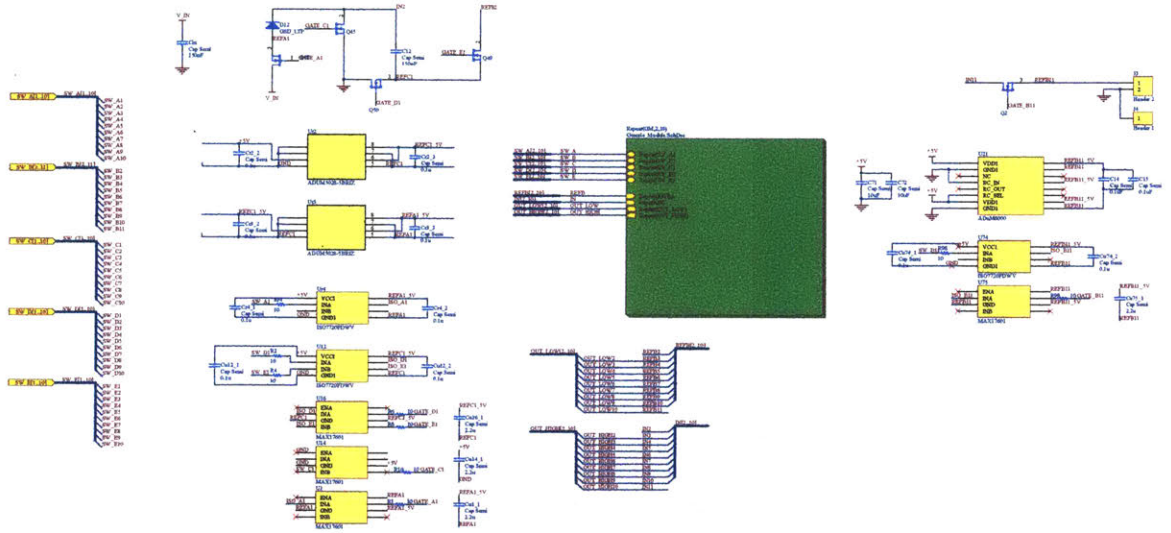
Figure I-5: RTC boost PCB layout



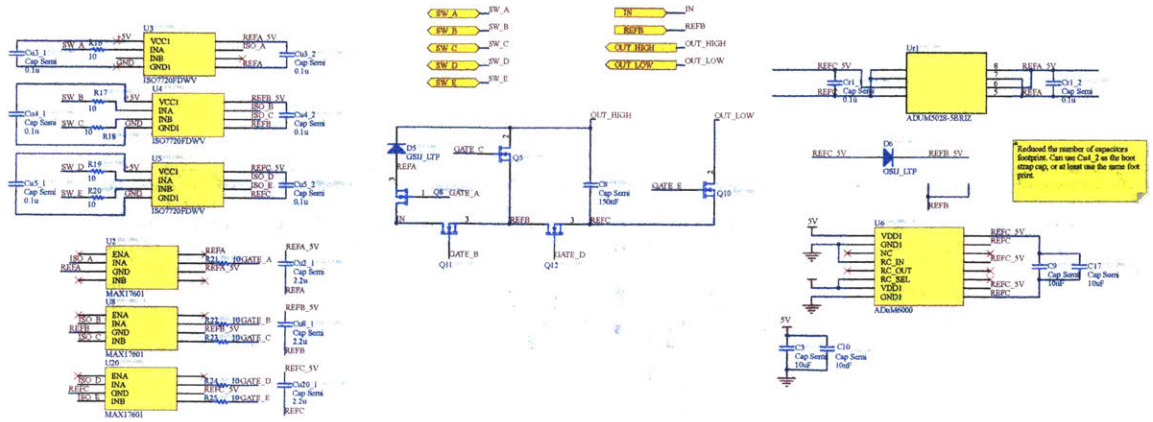
(a) Top sheet



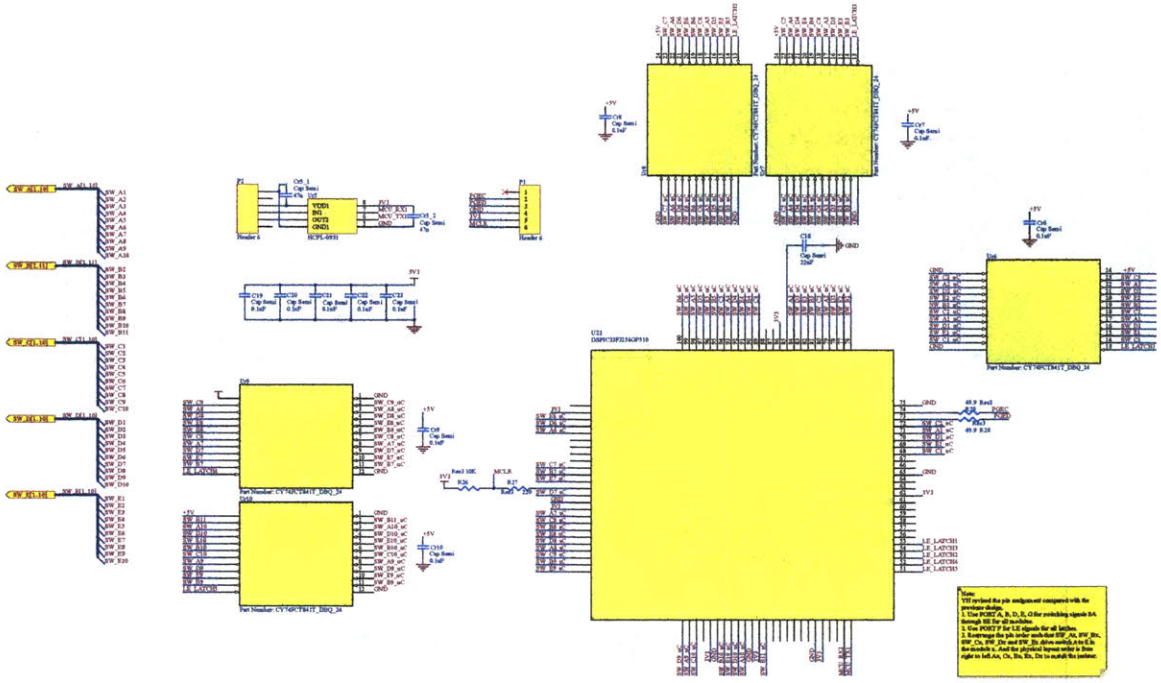
(b) Snip_Power.SchDoc, schematics of the logic power



(c) Snip_SCMLI.SchDoc, schematics of the 10-stage SCMLI. Module 1 and 10 are in this schematics, module 2 to 9 are detailed in Generic_Module.SchDoc

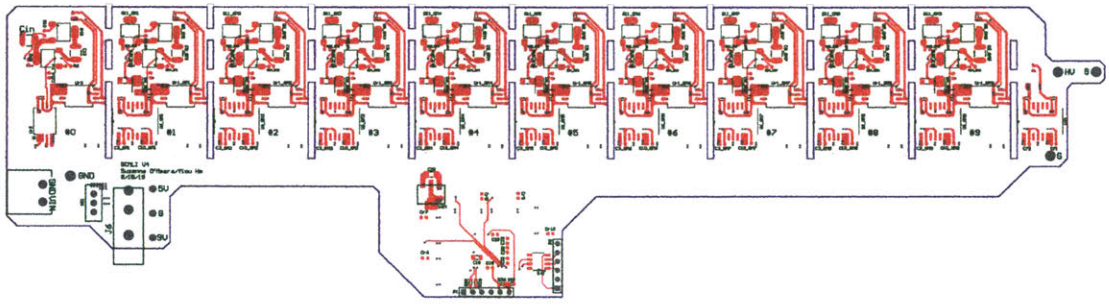


(d) Generic_Module.SchDoc, schematics of module 2 to 9 (same, repeat 8 times)

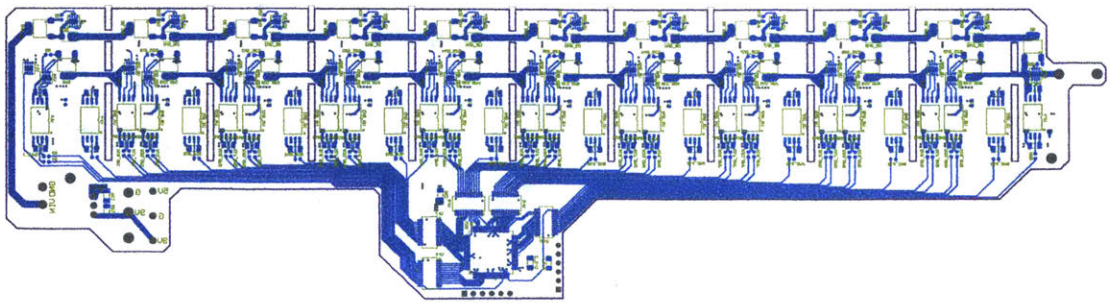


(e) Snip_MCU.SchDoc, schematics of the microcontroller and control circuits

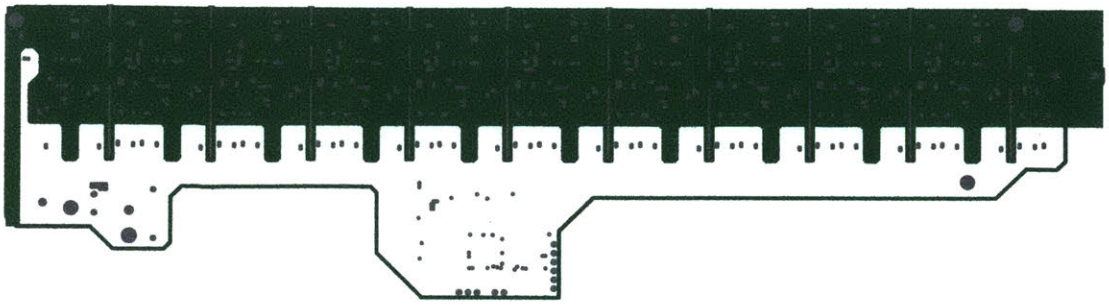
Figure I-5: Switched capacitor multi-level inverter schematic



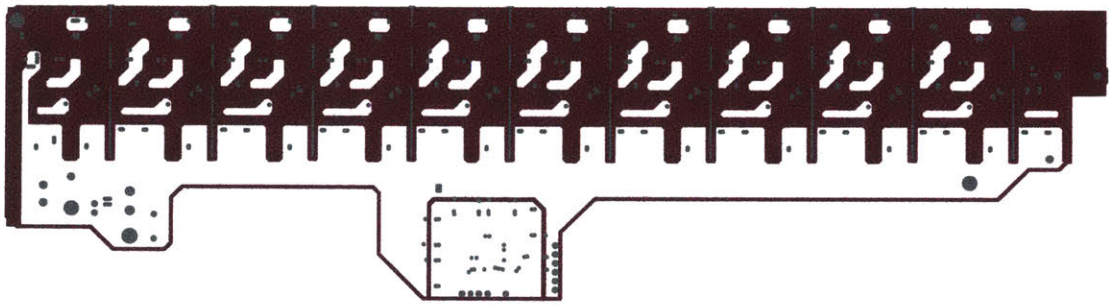
(a) Top layer



(b) Bottom layer



(c) Second layer (ground, negative)



(d) Third layer (power, negative)

Figure I-5: Switched capacitor multi-level inverter PCB layout

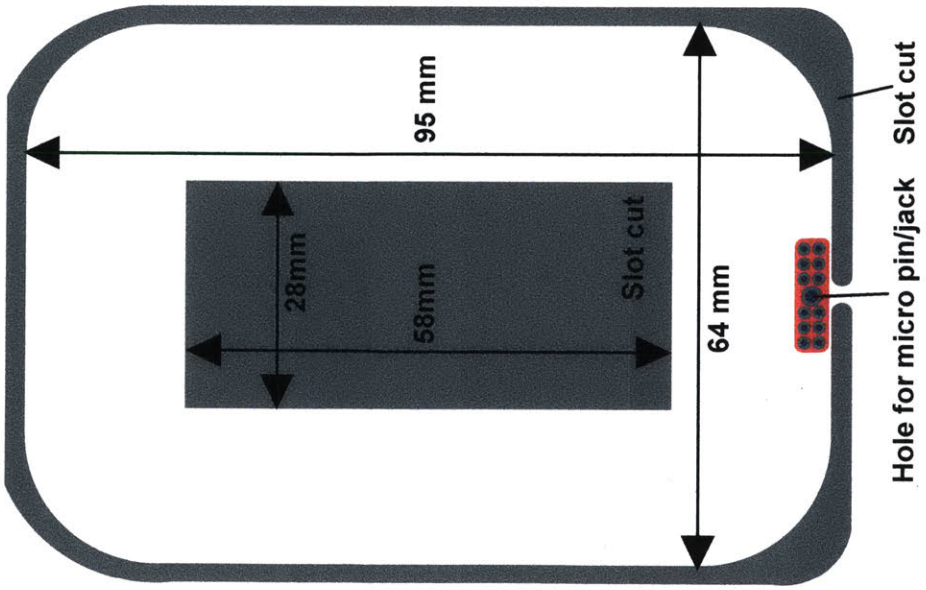


Figure I-6: Bobbin plate for the isolation transformer

Appendix J

Codes

All codes used in this thesis are downloadable through the Dropbox link: `https://www.dropbox.com/sh/hpqeg0g506cpws4/AAAVeMySyfIdYIAyBLjggJnXa?dl=0`

This section lists selected MATLAB and microcontroller codes due to limited pages.

- 1st-gen high voltage dc-dc converter:
  - 1st-gen high voltage dc-dc converter MATLAB design code
  - 1st-gen high voltage dc-dc converter microcontroller code
- High voltage dc-ac converter:
  - Non-resonant topologies MATLAB design code

Design codes for high voltage transformers in 1st-gen HVDC, 2nd-gen HVDC, and HVAC based on resonant topologies are very similar but have some different assumptions/variations. Same for the inductor design codes for each of these three converters. The codes may be hard to understand and inefficient – please email yiouhe@gmail.com if you have any questions.

J.1 1st gen HVDC

J.1.1 Voltage multiplier

Listing J.1: Main code to simulate the weight of voltage multipliers

```
%This script is to compare different VM topology and their weight
clc,clf,clear all
close all

% figure color
colorcodes = [0, 0.4470, 0.7410;...
    0.8500, 0.3250, 0.0980;...
    0.9290, 0.6940, 0.1250;...
    0,0,0];

%Save capacitance data
filename = 'Weight of different VM structure.xlsx';
%Create Structure
field0 = 'NumberOfStage';
field1 = 'TotalWeight';
field2 = 'FlyingCapacitorValue';
field3 = 'FlyingCapacitorVoltageRating';
field4 = 'NumberOfFlyingCapacitorInSeries';
field5 = 'NumberOfFlyingCapacitorInParallel';
field6 = 'OutputCapacitorValue';
field7 = 'OutputCapacitorVoltageRating';
field8 = 'NumberOfOutputCapacitorInSeries';
field9 = 'NumberOfOutputCapacitorInParallel';
field10 = 'TotalCapacitance';
field11 = 'FlyingCapEnergy';
field12 = 'OutputCapEnergy';
field13 = 'OutputImpedance';
HWCWinfo = struct(field0,{},field1,{},field2,{},field3,{},field4,{},...
field5,{},field6,{},field7,{},field8,{},field9,{},field10,{},field11,{},field12,{},
    field13,{});
FWCWinfo = struct(field0,{},field1,{},field2,{},field3,{},field4,{},...
field5,{},field6,{},field7,{},field8,{},field9,{},field10,{},field11,{},field12,{},
    field13,{});
HWDSinfo = struct(field0,{},field1,{},field2,{},field3,{},field4,{},...
field5,{},field6,{},field7,{},field8,{},field9,{},field10,{},field11,{},field12,{},
    field13,{});
FWDSinfo = struct(field0,{},field1,{},field2,{},field3,{},field4,{},...
field5,{},field6,{},field7,{},field8,{},field9,{},field10,{},field11,{},field12,{},
    field13,{});
global HWCWinfo FWCWinfo HWDSinfo FWDSinfo

%Design a voltage multiplier take input of whatever it can take to 20 kV.
Po = 375;
Vo = 20000; %half of output voltage
f = 500000;
alpha = 0.025;
deltaVo = 50; %half of voltage ripple
Stage = 20;

for n = 1:Stage %Number of stages
    HWCWinfo(n).NumberOfStage = n;
    FWCWinfo(n).NumberOfStage = n;
    HWDSinfo(n).NumberOfStage = n;
    FWDSinfo(n).NumberOfStage = n;
    HWCWVMfactor(n) = 2*n*2;
    FWCWVMfactor(n) = n*2;
    HWDSVMfactor(n) = 2*n*2;
    FWDSVMfactor(n) = n*2;
```

```
    %decide the capacitance based on the ripple value and voltage drop value:
    y = CapValuesWeight_updatedSSL(Po,f,Vo,n,alpha,deltaVo);
    CapHWCWWeight(n) = y(1);
    CapHWDSWeight(n) = y(2);
    CapFWCWWeight(n) = y(3);
    CapFWDSWeight(n) = y(4);
    if (~isempty(HWCWinfo(n).TotalCapacitance))
        HWCWCapacitance(n) = HWCWinfo(n).TotalCapacitance;
        HWCWEnergy(n) = HWCWinfo(n).FlyingCapEnergy + HWCWinfo(n).OutputCapEnergy;
        HWCWImpedance(n) = HWCWinfo(n).OutputImpedance;
    else
        HWCWCapacitance(n) = NaN;
        HWCWEnergy(n) = NaN;
        HWCWImpedance(n) = NaN;
    end
    if (~isempty(FWCWinfo(n).TotalCapacitance))
        FWCWCapacitance(n) = FWCWinfo(n).TotalCapacitance;
        FWCWEnergy(n) = FWCWinfo(n).FlyingCapEnergy + FWCWinfo(n).OutputCapEnergy;
        FWCWImpedance(n) = FWCWinfo(n).OutputImpedance;
    else
        FWCWCapacitance(n) = NaN;
        FWCWEnergy(n) = NaN;
        FWCWImpedance(n) = NaN;
    end
    if (~isempty(HWDSinfo(n).TotalCapacitance))
        HWDSCapacitance(n) = HWDSinfo(n).TotalCapacitance;
        HWDSEnergy(n) = HWDSinfo(n).FlyingCapEnergy + HWDSinfo(n).OutputCapEnergy;
        HWDSImpedance(n) = HWDSinfo(n).OutputImpedance;
    else
        HWDSCapacitance(n) = NaN;
        HWDSEnergy(n) = NaN;
        HWDSImpedance(n) = NaN;
    end
    if (~isempty(FWDSinfo(n).TotalCapacitance))
        FWDSCapacitance(n) = FWDSinfo(n).TotalCapacitance;
        FWDSEnergy(n) = FWDSinfo(n).FlyingCapEnergy + FWDSinfo(n).OutputCapEnergy;
        FWDSImpedance(n) = FWDSinfo(n).OutputImpedance;
    else
        FWDSCapacitance(n) = NaN;
        FWDSEnergy(n) = NaN;
        FWDSImpedance(n) = NaN;
    end
end
%%
% Plot
% Set figure and axis positions
figure(2);
set(gcf, 'Units', 'Normalized', 'OuterPosition', [0.2, 0.04, 0.5, 0.85]);
ax1 = axes('Position',[0.27 0.22 0.7 0.75]);
ax1.ActivePositionProperty = 'outerposition';
figure(3);
set(gcf, 'Units', 'Normalized', 'OuterPosition', [0.2, 0.04, 0.5, 0.85]);
ax1 = axes('Position',[0.27 0.22 0.7 0.75]);
ax1.ActivePositionProperty = 'outerposition';
%%
%-------------------------------------------------------------------------
% figure (2) plots voltage conversion ratio vs total capacitor weight of
% the full VM at 2*Po and 2*Vo
FXaxis = [HWCWVMfactor;HWDSVMfactor;FWCWVMfactor;FWDSVMfactor];
FYaxis = [CapHWCWWeight;CapHWDSWeight;CapFWCWWeight;CapFWDSWeight]*2;
FXaxis(isinf(FXaxis)) = NaN;
FYaxis(isinf(FYaxis)) = NaN;
xaxislabel = 'Voltage conversion ratio ({V_{OUT}}/{V_{IN}})';
yaxislabel = {'Total weight of capacitors (g)'};
x2axislabel = 'Input voltage (kV)';
Flegend = {'Half-wave Cockroft-Walton','Half-wave Dickson','Full-wave Cockroft-Walton
    ','Full-wave Dickson'};
legendx = 3;
```

```
roundXunit = 5;   %label X axis every 5 unit
roundYunit = 1;   %label Y axis every 10^(1) unit in log scale
figure(2);
Xplotrange = [min(min(FXaxis)),min(max(FXaxis,[],2))];
for i = 1:1:size(FXaxis,1)
    line(FXaxis(i,:),FYaxis(i,:),'Color',colorcodes(i,:),'linewidth',3);hold on;
    scatter(FXaxis(i,:),FYaxis(i,:),200,colorcodes(i,:),'filled','MarkerFaceAlpha',1,
        'MarkerEdgeAlpha',1);hold on;
end
hold off;grid;
set(gca,'FontSize',22);set(gca,'color','none');
% Set X axis
xlabel(xaxislabel);
xlim(Xplotrange);
xtick = round(linspace(Xplotrange(1),Xplotrange(2),5)/roundXunit,0)*roundXunit; %
    round to the next 5
xtick(find(xtick < Xplotrange(1))) = Xplotrange(1); %cap X axis minimal
xtick(find(xtick > Xplotrange(2))) = Xplotrange(2); %cap X axis max
xticklab = strsplit(num2str(xtick));
set(gca,'XTick',xtick,'XTickLabel',xticklab);
% Set Y axis
set(gca,'yscale','log');
ylabel(yaxislabel);
YPlotIndex = intersect(find(FXaxis >= Xplotrange(1)),find(FXaxis <= Xplotrange(2)));
Yplotrange = [floor(min(min(FYaxis(YPlotIndex)))/roundYunit)*roundYunit,(floor(max(
    max(FYaxis(YPlotIndex)))/roundYunit) + 1)*roundYunit];
Yplotrange = [1,4]; %uncomment for a fix range, in this case, log
% for log scale only
ylim(10.^Yplotrange);
ytick = logspace(Yplotrange(1),Yplotrange(2),4);
yticklab = strsplit(num2str(ytick));
set(gca,'YTick',ytick,'YTickLabel',yticklab);

% customize legend in log span
legendyspan = Yplotrange(2) - Yplotrange(1);
legendystart = legendyspan*0.97 + Yplotrange(1);
for i = 1:1:size(Flegend,2)
    text(legendx,10^(legendystart - 0.05*legendyspan*i),Flegend{i},'Color',colorcodes
        (i,:),'HorizontalAlignment','left','VerticalAlignment','bottom','fontsize'
        ,22);
end
% double x axis
b=axes('Position',[0.29 0.11 .68 1e-12]);
set(b,'Color','none');
set(b,'fontsize',22);
xlabel(b,x2axislabel)
set(b,'xlim',[min(min(FXaxis)),min(max(FXaxis,[],2))]); %same with before
xticklab = strsplit(num2str(2*Vo./xtick/1000));
set(b,'XTick',xtick,'XTickLabel',xticklab);
%-------------------------------------------------------------------------
% figure (3) plots voltage conversion ratio vs total capacitor energy of
% the full VM at 2*Po and 2*Vo
FXaxis = [HWCWVMfactor;HWDSVMfactor;FWCWVMfactor;FWDSVMfactor];
FYaxis = [HWCWEnergy;HWDSEnergy;FWCWEnergy;FWDSEnergy]/1e12*2;
FXaxis(isinf(FXaxis)) = NaN;
FYaxis(isinf(FYaxis)) = NaN;
xaxislabel = 'Voltage conversion ratio ({V_{OUT}}/{V_{IN}})';
yaxislabel = {'Total energy in capacitors (J)'};
x2axislabel = 'Input voltage (kV)';
Flegend = {'Half-wave Cockroft-Walton','Half-wave Dickson','Full-wave Cockroft-Walton
    ','Full-wave Dickson'};
legendx = 3;
roundXunit = 5;   %label X axis every 5 unit
roundYunit = 1;   %label Y axis every 10^(1) unit in log scale
figure(3);
Xplotrange = [min(min(FXaxis)),min(max(FXaxis,[],2))];
for i = 1:1:size(FXaxis,1)
    line(FXaxis(i,:),FYaxis(i,:),'Color',colorcodes(i,:),'linewidth',3);hold on;
```

```
    scatter(FXaxis(i,:),FYaxis(i,:),200,colorcodes(i,:),'filled','MarkerFaceAlpha',1,
        'MarkerEdgeAlpha',1);hold on;
end
hold off;grid;
set(gca,'FontSize',22);set(gca,'color','none');
% Set X axis
xlabel(xaxislabel);
xlim(Xplotrange);
xtick = round(linspace(Xplotrange(1),Xplotrange(2),5)/roundXunit,0)*roundXunit; %
    round to the next 5
xtick(find(xtick < Xplotrange(1))) = Xplotrange(1); %cap X axis minimal
xtick(find(xtick > Xplotrange(2))) = Xplotrange(2); %cap X axis max
xticklab = strsplit(num2str(xtick));
set(gca,'XTick',xtick,'XTickLabel',xticklab);
% Set Y axis
set(gca,'yscale','log');
ylabel(yaxislabel);
YPlotIndex = intersect(find(FXaxis >= Xplotrange(1)),find(FXaxis <= Xplotrange(2)));
Yplotrange = [floor(min(min(FYaxis(YPlotIndex)))/roundYunit)*roundYunit,(floor(max(
    max(FYaxis(YPlotIndex)))/roundYunit) + 1)*roundYunit];
Yplotrange = [-2,2]; %uncomment for a fix range, in this case, log 10^(-2) to 10^(2)
% for log scale only
ylim(10.^Yplotrange);
ytick = logspace(Yplotrange(1),Yplotrange(2),5);
yticklab = strsplit(num2str(ytick));
set(gca,'YTick',ytick,'YTickLabel',yticklab);
% customize legend in log span
legendyspan = Yplotrange(2) - Yplotrange(1);
legendystart = legendyspan*0.97 + Yplotrange(1);
for i = 1:1:size(Flegend,2)
    text(legendx,10^(legendystart - 0.05*legendyspan*i),Flegend{i},'Color',colorcodes
        (i,:),'HorizontalAlignment','left','VerticalAlignment','bottom','fontsize'
        ,22);
end
% double x axis
b=axes('Position',[0.27 0.11 .7 1e-12]);
set(b,'Color','none');
set(b,'fontsize',22);
xlabel(b,x2axislabel)
set(b,'xlim',[min(min(FXaxis)),min(max(FXaxis,[],2))]); %same with before
xticklab = strsplit(num2str(2*Vo./xtick/1000));
set(b,'XTick',xtick,'XTickLabel',xticklab);
```

Listing J.2: Code to simulate the weight of each voltage multiplier topology (called in List J.1)

```
%This function is to calculate the capacitance value a n stage VM need
%And also calculate how much weight is the capacitance in total
function y = CapValuesWeight_updatedSSL(Po,f,Vo,n,alpha,deltaVo)
clear OutputCapHW_result OutputCapFW_result
clear FlyingCapHWCW_result FlyingCapFWCW_result FlyingCapHWDS_result
    FlyingCapFWDS_result
global HWCWinfo FWCWinfo HWDSinfo FWDSinfo
% field0 = 'NumberofStage';
% field1 = 'TotalWeight';
% field2 = 'FlyingCapacitorValue';
% field3 = 'FlyingCapacitorVoltageRating';
% field4 = 'NumberOfFlyingCapacitorInSeries';
% field5 = 'NumberOfFlyingCapacitorInParallel';
% field6 = 'OutputCapacitorValue';
% field7 = 'OutputCapacitorVoltageRating';
% field8 = 'NumberOfOutputCapacitorInSeries';
% field9 = 'NumberOfOutputCapacitorInParallel';

Impedance = alpha*Vo/(Po/Vo); %maximum output impedance
```

```
% FET stress is always Vo/n, therefore use 2*Vo/n rated FET


%%Calculate output capacitors for different configuration
OutputCapHW = (n^2*Po)/(2*f*Vo*deltaVo)*10^12;
OutputCapHW_Vlimt = Vo/n;
OutputCapHW_result = CapacitorWeight(OutputCapHW, OutputCapHW_Vlimt);
if (~isempty(OutputCapHW_result))
    OutputCapHWWeight = OutputCapHW_result(1);
    HWCWinfo(n).OutputCapacitorValue = OutputCapHW_result(2);
    HWCWinfo(n).OutputCapacitorVoltageRating = OutputCapHW_result(3);
    HWCWinfo(n).NumberOfOutputCapacitorInSeries = OutputCapHW_result(4);
    HWCWinfo(n).NumberOfOutputCapacitorInParallel = OutputCapHW_result(5);
    HWDSinfo(n).OutputCapacitorValue = OutputCapHW_result(2);
    HWDSinfo(n).OutputCapacitorVoltageRating = OutputCapHW_result(3);
    HWDSinfo(n).NumberOfOutputCapacitorInSeries = OutputCapHW_result(4);
    HWDSinfo(n).NumberOfOutputCapacitorInParallel = OutputCapHW_result(5);
else
    OutputCapHWWeight = Inf;
end
OutputCapFW = (20*n*Po)/(f*Vo^2)*10^12; %was 20
OutputCapFW_Vlimt = Vo/n;
OutputCapFW_result = CapacitorWeight(OutputCapFW, OutputCapFW_Vlimt);
if (~isempty(OutputCapFW_result))
    OutputCapFWWeight = OutputCapFW_result(1);
    FWCWinfo(n).OutputCapacitorValue = OutputCapFW_result(2);
    FWCWinfo(n).OutputCapacitorVoltageRating = OutputCapFW_result(3);
    FWCWinfo(n).NumberOfOutputCapacitorInSeries = OutputCapFW_result(4);
    FWCWinfo(n).NumberOfOutputCapacitorInParallel = OutputCapFW_result(5);
    FWDSinfo(n).OutputCapacitorValue = OutputCapFW_result(2);
    FWDSinfo(n).OutputCapacitorVoltageRating = OutputCapFW_result(3);
    FWDSinfo(n).NumberOfOutputCapacitorInSeries = OutputCapFW_result(4);
    FWDSinfo(n).NumberOfOutputCapacitorInParallel = OutputCapFW_result(5);
else
    OutputCapFWWeight = Inf;
end
%% CW topology
%Calculate flying capacitors for different configuration
%Flying cap for CW half wave

FlyingCapHWCW = (n*(n+1)*(2*n+1)/6)/((Impedance*f - n*(n-1)*(4*n-5)/12/OutputCapHW))
    *10^12; %capacitance need for fullwave CW
for i = 1:n
    FlyingCapHWCW_Vlimt(1) = 0.5*Vo/n; %for HWCW, conversion ratio is 2n, so input is
        Vac = Vo/(2n);FET stress is 1*Vac
    if (i > 1)
        FlyingCapHWCW_Vlimt(i) = Vo/n;
    end
    %Weight, Capacitance, RatedVoltageIndex, NumberOfCapSeries, NumberOfCapParallel
    FlyingCapHWCW_result = CapacitorWeight(FlyingCapHWCW, FlyingCapHWCW_Vlimt(i));
    if ((~isempty(FlyingCapHWCW_result)) && (~isempty(OutputCapHW_result)))
        FlyingCapHWCWWeight(i) = FlyingCapHWCW_result(1);
        FlyingCapHWCWCAP(i) = FlyingCapHWCW_result(2);
        FlyingCapHWCWRVI(i) = FlyingCapHWCW_result(3);
        FlyingCapHWCWNOCS(i) = FlyingCapHWCW_result(4);
        FlyingCapHWCWNOCP(i) = FlyingCapHWCW_result(5);
    else
        FlyingCapHWCWWeight(i) = Inf;
        FlyingCapHWCWCAP(i) = NaN;
        FlyingCapHWCWRVI(i) = NaN;
        FlyingCapHWCWNOCS(i) = NaN;
        FlyingCapHWCWNOCP(i) = NaN;
    end
end
%RecordData
if (~isempty(OutputCapHW_result))
    CapHWCWWeight = sum(FlyingCapHWCWWeight) + OutputCapHWWeight*n;
    HWCWinfo(n).TotalWeight = CapHWCWWeight;
```

```
85      HWCWinfo(n).FlyingCapacitorValue = FlyingCapHWCWCAP;
86      HWCWinfo(n).FlyingCapacitorVoltageRating = FlyingCapHWCWRVI;
87      HWCWinfo(n).NumberOfFlyingCapacitorInSeries = FlyingCapHWCWNOCS;
88      HWCWinfo(n).NumberOfFlyingCapacitorInParallel = FlyingCapHWCWNOCP;
89      HWCWinfo(n).TotalCapacitance = n*OutputCapHW_result(2)*OutputCapHW_result(5)/
            OutputCapHW_result(4) + sum(FlyingCapHWCWCAP.*FlyingCapHWCWNOCP./
            FlyingCapHWCWNOCS);
90      HWCWinfo(n).FlyingCapEnergy = 0.5*sum(FlyingCapHWCW.*FlyingCapHWCW_Vlimt.^2);
91      HWCWinfo(n).OutputCapEnergy = 0.5*n*OutputCapHW*OutputCapHW_Vlimt^2;
92      HWCWinfo(n).OutputImpedance = (n*(n+1)*(2*n+1)/6/FlyingCapHWCW*10^12 + n*(n-1)
            *(4*n-5)/12/OutputCapHW*10^12)/f;
93  else
94      CapHWCWWeight = Inf;
95  end
96
97  %Flying cap for CW full wave
98  FlyingCapFWCW = (n*(n+1)*(2*n+1)/12)/((Impedance)*f)*10^12; %capacitance need for
        fullwave CW
99  for i = 1:n
100     FlyingCapFWCW_Vlimt(1) = 0.5*Vo/n; %for FWCW, conversion ratio is n, so input is
            Vac = Vo/n; FET stress is 0.5*Vac
101     if (i > 1)
102         FlyingCapFWCW_Vlimt(i) = Vo/n;
103     end
104     %Weight, Capacitance, RatedVoltageIndex, NumberOfCapSeries, NumberOfCapParallel
105     FlyingCapFWCW_result = CapacitorWeight(FlyingCapFWCW, FlyingCapFWCW_Vlimt(i));
106     if ((~isempty(FlyingCapFWCW_result)) && (~isempty(OutputCapFW_result)))
107         FlyingCapFWCWWeight(i) = FlyingCapFWCW_result(1);
108         FlyingCapFWCWCAP(i) = FlyingCapFWCW_result(2);
109         FlyingCapFWCWRVI(i) = FlyingCapFWCW_result(3);
110         FlyingCapFWCWNOCS(i) = FlyingCapFWCW_result(4);
111         FlyingCapFWCWNOCP(i) = FlyingCapFWCW_result(5);
112     else
113         FlyingCapFWCWWeight(i) = Inf;
114         FlyingCapFWCWCAP(i) = NaN;
115         FlyingCapFWCWRVI(i) = NaN;
116         FlyingCapFWCWNOCS(i) = NaN;
117         FlyingCapFWCWNOCP(i) = NaN;
118     end
119 end
120 %RecordData
121 if (~isempty(OutputCapFW_result))
122     CapFWCWWeight = 2*sum(FlyingCapFWCWWeight) + OutputCapFWWeight*n;
123     FWCWinfo(n).TotalWeight = CapFWCWWeight;
124     FWCWinfo(n).FlyingCapacitorValue = FlyingCapFWCWCAP;
125     FWCWinfo(n).FlyingCapacitorVoltageRating = FlyingCapFWCWRVI;
126     FWCWinfo(n).NumberOfFlyingCapacitorInSeries = FlyingCapFWCWNOCS;
127     FWCWinfo(n).NumberOfFlyingCapacitorInParallel = FlyingCapFWCWNOCP;
128     FWCWinfo(n).TotalCapacitance = n*OutputCapFW_result(2)*OutputCapFW_result(5)/
            OutputCapFW_result(4) + 2*sum(FlyingCapFWCWCAP.*FlyingCapFWCWNOCP./
            FlyingCapFWCWNOCS);
129     FWCWinfo(n).FlyingCapEnergy = 2*0.5*sum(FlyingCapFWCW.*FlyingCapFWCW_Vlimt.^2);
130     FWCWinfo(n).OutputCapEnergy = 0.5*n*OutputCapFW*OutputCapFW_Vlimt^2;
131     FWCWinfo(n).OutputImpedance = (n*(n+1)*(2*n+1)/12/FlyingCapFWCW)/f*10^12;
132 else
133     CapFWCWWeight = Inf;
134 end
135 %% Dickson topology
136 %Flying cap for DS half wave
137
138 FlyingCapHWDS = n/((Impedance)*f - n*(n-1)*(4*n+1)/12/OutputCapHW)*10^12; %
        capacitance need for fullwave Dickson
139 for i = 1:n
140     FlyingCapHWDS_Vlimt(i) = (2*i-1)/2*Vo/n; %for HWDS, conversion ratio is 2n, so
            input is Vac = Vo/(2n);FET stress is (2i-1)*Vac
141     %Weight, Capacitance, RatedVoltageIndex, NumberOfCapSeries, NumberOfCapParallel
142     FlyingCapHWDS_result = CapacitorWeight(FlyingCapHWDS, FlyingCapHWDS_Vlimt(i));
143     if ((~isempty(FlyingCapHWDS_result)) && (~isempty(OutputCapHW_result)))
```

```
144             FlyingCapHWDSWeight(i) = FlyingCapHWDS_result(1);
145             FlyingCapHWDSCAP(i) = FlyingCapHWDS_result(2);
146             FlyingCapHWDSRVI(i) = FlyingCapHWDS_result(3);
147             FlyingCapHWDSNOCS(i) = FlyingCapHWDS_result(4);
148             FlyingCapHWDSNOCP(i) = FlyingCapHWDS_result(5);
149         else
150             FlyingCapHWDSWeight(i) = Inf;
151             FlyingCapHWDSCAP(i) = NaN;
152             FlyingCapHWDSRVI(i) = NaN;
153             FlyingCapHWDSNOCS(i) = NaN;
154             FlyingCapHWDSNOCP(i) = NaN;
155         end
156 end
157
158 %RecordData
159 if (~isempty(OutputCapHW_result))
160     CapHWDSWeight = sum(FlyingCapHWDSWeight) + OutputCapHWWeight*n;
161     HWDSinfo(n).TotalWeight = CapHWDSWeight;
162     HWDSinfo(n).FlyingCapacitorValue = FlyingCapHWDSCAP;
163     HWDSinfo(n).FlyingCapacitorVoltageRating = FlyingCapHWDSRVI;
164     HWDSinfo(n).NumberOfFlyingCapacitorInSeries = FlyingCapHWDSNOCS;
165     HWDSinfo(n).NumberOfFlyingCapacitorInParallel = FlyingCapHWDSNOCP;
166     HWDSinfo(n).TotalCapacitance = n*OutputCapHW_result(2)*OutputCapHW_result(5)/
            OutputCapHW_result(4) + sum(FlyingCapHWDSCAP.*FlyingCapHWDSNOCP./
            FlyingCapHWDSNOCS);
167     HWDSinfo(n).FlyingCapEnergy = 0.5*sum(FlyingCapHWDS.*FlyingCapHWDS_Vlimt.^2);
168     HWDSinfo(n).OutputCapEnergy = 0.5*n*OutputCapHW*OutputCapHW_Vlimt^2;
169     HWDSinfo(n).OutputImpedance = (n/FlyingCapHWDS*10^12 + n*(n-1)*(4*n+1)/12/
            OutputCapHW*10^12)/f;
170 else
171     CapHWDSWeight = Inf;
172 end
173
174 %Flying cap for DS full wave
175 FlyingCapFWDS = n/2/((Impedance)*f)*10^12; %capacitance need for fullwave Dickson
176 for i = 1:n
177     FlyingCapFWDS_Vlimt(i) = (i-0.5)*Vo/n; %for FWDS, conversion ratio is n, so input
            is Vac = Vo/n;FET stress is (i-1)*Vac
178     FlyingCapFWDS_result = CapacitorWeight(FlyingCapFWDS, FlyingCapFWDS_Vlimt(i));
179     if ((~isempty(FlyingCapFWDS_result)) && (~isempty(OutputCapFW_result)))
180         FlyingCapFWDSWeight(i) = FlyingCapFWDS_result(1);
181         FlyingCapFWDSCAP(i) = FlyingCapFWDS_result(2);
182         FlyingCapFWDSRVI(i) = FlyingCapFWDS_result(3);
183         FlyingCapFWDSNOCS(i) = FlyingCapFWDS_result(4);
184         FlyingCapFWDSNOCP(i) = FlyingCapFWDS_result(5);
185     else
186         FlyingCapFWDSWeight(i) = Inf;
187         FlyingCapFWDSCAP(i) = NaN;
188         FlyingCapFWDSRVI(i) = NaN;
189         FlyingCapFWDSNOCS(i) = NaN;
190         FlyingCapFWDSNOCP(i) = NaN;
191     end
192 end
193 %RecordData
194 if (~isempty(OutputCapFW_result))
195     CapFWDSWeight = 2*sum(FlyingCapFWDSWeight) + OutputCapFWWeight*n;
196     FWDSinfo(n).TotalWeight = CapFWDSWeight;
197     FWDSinfo(n).FlyingCapacitorValue = FlyingCapFWDSCAP;
198     FWDSinfo(n).FlyingCapacitorVoltageRating = FlyingCapFWDSRVI;
199     FWDSinfo(n).NumberOfFlyingCapacitorInSeries = FlyingCapFWDSNOCS;
200     FWDSinfo(n).NumberOfFlyingCapacitorInParallel = FlyingCapFWDSNOCP;
201     FWDSinfo(n).TotalCapacitance = n*OutputCapFW_result(2)*OutputCapFW_result(5)/
            OutputCapFW_result(4) + 2*sum(FlyingCapFWDSCAP.*FlyingCapFWDSNOCP./
            FlyingCapFWDSNOCS);
202     FWDSinfo(n).FlyingCapEnergy = 2*0.5*sum(FlyingCapFWDS.*FlyingCapFWDS_Vlimt.^2);
203     FWDSinfo(n).OutputCapEnergy = 0.5*n*OutputCapFW*OutputCapFW_Vlimt^2;
204     FWDSinfo(n).OutputImpedance = (n/2/FlyingCapFWDS)/f*10^12;
205 else
```

```
206     CapFWDSWeight = Inf;
207 end
208 y = [CapHWCWWeight, CapHWDSWeight, CapFWCWWeight, CapFWDSWeight];
209 end
```

Listing J.3: Code to simulate the weight of each voltage multiplier topology (called in List J.2)

```
1  %This function is to calculate the capacitance value a n stage VM need
2  %And also calculate how much weight is the capacitance in total
3  function y = CapValuesWeight_updatedSSL(Po,f,Vo,n,alpha,deltaVo)
4  clear OutputCapHW_result OutputCapFW_result
5  clear FlyingCapHWCW_result FlyingCapFWCW_result FlyingCapHWDS_result
       FlyingCapFWDS_result
6  global HWCWinfo FWCWinfo HWDSinfo FWDSinfo
7  % field0 = 'NumberofStage';
8  % field1 = 'TotalWeight';
9  % field2 = 'FlyingCapacitorValue';
10 % field3 = 'FlyingCapacitorVoltageRating';
11 % field4 = 'NumberOfFlyingCapacitorInSeries';
12 % field5 = 'NumberOfFlyingCapacitorInParallel';
13 % field6 = 'OutputCapacitorValue';
14 % field7 = 'OutputCapacitorVoltageRating';
15 % field8 = 'NumberOfOutputCapacitorInSeries';
16 % field9 = 'NumberOfOutputCapacitorInParallel';
17
18 Impedance = alpha*Vo/(Po/Vo); %maximum output impedance
19 % FET stress is always Vo/n, therefore use 2*Vo/n rated FET
20
21
22 %%Calculate output capacitors for different configuration
23 OutputCapHW = (n^2*Po)/(2*f*Vo*deltaVo)*10^12;
24 OutputCapHW_Vlimt = Vo/n;
25 OutputCapHW_result = CapacitorWeight(OutputCapHW, OutputCapHW_Vlimt);
26 if (~isempty(OutputCapHW_result))
27     OutputCapHWWeight = OutputCapHW_result(1);
28     HWCWinfo(n).OutputCapacitorValue = OutputCapHW_result(2);
29     HWCWinfo(n).OutputCapacitorVoltageRating = OutputCapHW_result(3);
30     HWCWinfo(n).NumberOfOutputCapacitorInSeries = OutputCapHW_result(4);
31     HWCWinfo(n).NumberOfOutputCapacitorInParallel = OutputCapHW_result(5);
32     HWDSinfo(n).OutputCapacitorValue = OutputCapHW_result(2);
33     HWDSinfo(n).OutputCapacitorVoltageRating = OutputCapHW_result(3);
34     HWDSinfo(n).NumberOfOutputCapacitorInSeries = OutputCapHW_result(4);
35     HWDSinfo(n).NumberOfOutputCapacitorInParallel = OutputCapHW_result(5);
36 else
37     OutputCapHWWeight = Inf;
38 end
39 OutputCapFW = (20*n*Po)/(f*Vo^2)*10^12; %was 20
40 OutputCapFW_Vlimt = Vo/n;
41 OutputCapFW_result = CapacitorWeight(OutputCapFW, OutputCapFW_Vlimt);
42 if (~isempty(OutputCapFW_result))
43     OutputCapFWWeight = OutputCapFW_result(1);
44     FWCWinfo(n).OutputCapacitorValue = OutputCapFW_result(2);
45     FWCWinfo(n).OutputCapacitorVoltageRating = OutputCapFW_result(3);
46     FWCWinfo(n).NumberOfOutputCapacitorInSeries = OutputCapFW_result(4);
47     FWCWinfo(n).NumberOfOutputCapacitorInParallel = OutputCapFW_result(5);
48     FWDSinfo(n).OutputCapacitorValue = OutputCapFW_result(2);
49     FWDSinfo(n).OutputCapacitorVoltageRating = OutputCapFW_result(3);
50     FWDSinfo(n).NumberOfOutputCapacitorInSeries = OutputCapFW_result(4);
51     FWDSinfo(n).NumberOfOutputCapacitorInParallel = OutputCapFW_result(5);
52 else
53     OutputCapFWWeight = Inf;
54 end
55 %% CW topology
56 %Calculate flying capacitors for different configuration
```

```
%Flying cap for CW half wave

FlyingCapHWCW = (n*(n+1)*(2*n+1)/6)/((Impedance*f - n*(n-1)*(4*n-5)/12/OutputCapHW))
    *10^12; %capacitance need for fullwave CW
for i = 1:n
    FlyingCapHWCW_Vlimt(1) = 0.5*Vo/n; %for HWCW, conversion ratio is 2n, so input is
        Vac = Vo/(2n);FET stress is 1*Vac
    if (i > 1)
        FlyingCapHWCW_Vlimt(i) = Vo/n;
    end
    %Weight, Capacitance, RatedVoltageIndex, NumberOfCapSeries, NumberOfCapParallel
    FlyingCapHWCW_result = CapacitorWeight(FlyingCapHWCW, FlyingCapHWCW_Vlimt(i));
    if ((~isempty(FlyingCapHWCW_result)) && (~isempty(OutputCapHW_result)))
        FlyingCapHWCWWeight(i) = FlyingCapHWCW_result(1);
        FlyingCapHWCWCAP(i) = FlyingCapHWCW_result(2);
        FlyingCapHWCWRVI(i) = FlyingCapHWCW_result(3);
        FlyingCapHWCWNOCS(i) = FlyingCapHWCW_result(4);
        FlyingCapHWCWNOCP(i) = FlyingCapHWCW_result(5);
    else
        FlyingCapHWCWWeight(i) = Inf;
        FlyingCapHWCWCAP(i) = NaN;
        FlyingCapHWCWRVI(i) = NaN;
        FlyingCapHWCWNOCS(i) = NaN;
        FlyingCapHWCWNOCP(i) = NaN;
    end
end
%RecordData
if (~isempty(OutputCapHW_result))
    CapHWCWWeight = sum(FlyingCapHWCWWeight) + OutputCapHWWeight*n;
    HWCWinfo(n).TotalWeight = CapHWCWWeight;
    HWCWinfo(n).FlyingCapacitorValue = FlyingCapHWCWCAP;
    HWCWinfo(n).FlyingCapacitorVoltageRating = FlyingCapHWCWRVI;
    HWCWinfo(n).NumberOfFlyingCapacitorInSeries = FlyingCapHWCWNOCS;
    HWCWinfo(n).NumberOfFlyingCapacitorInParallel = FlyingCapHWCWNOCP;
    HWCWinfo(n).TotalCapacitance = n*OutputCapHW_result(2)*OutputCapHW_result(5)/
        OutputCapHW_result(4) + sum(FlyingCapHWCWCAP.*FlyingCapHWCWNOCP./
        FlyingCapHWCWNOCS);
    HWCWinfo(n).FlyingCapEnergy = 0.5*sum(FlyingCapHWCW.*FlyingCapHWCW_Vlimt.^2);
    HWCWinfo(n).OutputCapEnergy = 0.5*n*OutputCapHW*OutputCapHW_Vlimt^2;
    HWCWinfo(n).OutputImpedance = (n*(n+1)*(2*n+1)/6/FlyingCapHWCW*10^12 + n*(n-1)
        *(4*n-5)/12/OutputCapHW*10^12)/f;
else
    CapHWCWWeight = Inf;
end

%Flying cap for CW full wave
FlyingCapFWCW = (n*(n+1)*(2*n+1)/12)/((Impedance)*f)*10^12; %capacitance need for
    fullwave CW
for i = 1:n
    FlyingCapFWCW_Vlimt(1) = 0.5*Vo/n; %for FWCW, conversion ratio is n, so input is
        Vac = Vo/n; FET stress is 0.5*Vac
    if (i > 1)
        FlyingCapFWCW_Vlimt(i) = Vo/n;
    end
    %Weight, Capacitance, RatedVoltageIndex, NumberOfCapSeries, NumberOfCapParallel
    FlyingCapFWCW_result = CapacitorWeight(FlyingCapFWCW, FlyingCapFWCW_Vlimt(i));
    if ((~isempty(FlyingCapFWCW_result)) && (~isempty(OutputCapFW_result)))
        FlyingCapFWCWWeight(i) = FlyingCapFWCW_result(1);
        FlyingCapFWCWCAP(i) = FlyingCapFWCW_result(2);
        FlyingCapFWCWRVI(i) = FlyingCapFWCW_result(3);
        FlyingCapFWCWNOCS(i) = FlyingCapFWCW_result(4);
        FlyingCapFWCWNOCP(i) = FlyingCapFWCW_result(5);
    else
        FlyingCapFWCWWeight(i) = Inf;
        FlyingCapFWCWCAP(i) = NaN;
        FlyingCapFWCWRVI(i) = NaN;
        FlyingCapFWCWNOCS(i) = NaN;
        FlyingCapFWCWNOCP(i) = NaN;
```

```
118         end
119     end
120     %RecordData
121     if (~isempty(OutputCapFW_result))
122         CapFWCWWeight = 2*sum(FlyingCapFWCWWeight) + OutputCapFWWeight*n;
123         FWCWinfo(n).TotalWeight = CapFWCWWeight;
124         FWCWinfo(n).FlyingCapacitorValue = FlyingCapFWCWCAP;
125         FWCWinfo(n).FlyingCapacitorVoltageRating = FlyingCapFWCWRVI;
126         FWCWinfo(n).NumberOfFlyingCapacitorInSeries = FlyingCapFWCWNOCS;
127         FWCWinfo(n).NumberOfFlyingCapacitorInParallel = FlyingCapFWCWNOCP;
128         FWCWinfo(n).TotalCapacitance = n*OutputCapFW_result(2)*OutputCapFW_result(5)/
                OutputCapFW_result(4) + 2*sum(FlyingCapFWCWCAP.*FlyingCapFWCWNOCP./
                FlyingCapFWCWNOCS);
129         FWCWinfo(n).FlyingCapEnergy = 2*0.5*sum(FlyingCapFWCW.*FlyingCapFWCW_Vlimt.^2);
130         FWCWinfo(n).OutputCapEnergy = 0.5*n*OutputCapFW*OutputCapFW_Vlimt^2;
131         FWCWinfo(n).OutputImpedance = (n*(n+1)*(2*n+1)/12/FlyingCapFWCW)/f*10^12;
132     else
133         CapFWCWWeight = Inf;
134     end
135     %% Dickson topology
136     %Flying cap for DS half wave
137
138     FlyingCapHWDS = n/((Impedance)*f - n*(n-1)*(4*n+1)/12/OutputCapHW)*10^12; %
            capacitance need for fullwave Dickson
139     for i = 1:n
140         FlyingCapHWDS_Vlimt(i) = (2*i-1)/2*Vo/n; %for HWDS, conversion ratio is 2n, so
                input is Vac = Vo/(2n);FET stress is (2i-1)*Vac
141         %Weight, Capacitance, RatedVoltageIndex, NumberOfCapSeries, NumberOfCapParallel
142         FlyingCapHWDS_result = CapacitorWeight(FlyingCapHWDS, FlyingCapHWDS_Vlimt(i));
143         if ((~isempty(FlyingCapHWDS_result)) && (~isempty(OutputCapHW_result)))
144             FlyingCapHWDSWeight(i) = FlyingCapHWDS_result(1);
145             FlyingCapHWDSCAP(i) = FlyingCapHWDS_result(2);
146             FlyingCapHWDSRVI(i) = FlyingCapHWDS_result(3);
147             FlyingCapHWDSNOCS(i) = FlyingCapHWDS_result(4);
148             FlyingCapHWDSNOCP(i) = FlyingCapHWDS_result(5);
149         else
150             FlyingCapHWDSWeight(i) = Inf;
151             FlyingCapHWDSCAP(i) = NaN;
152             FlyingCapHWDSRVI(i) = NaN;
153             FlyingCapHWDSNOCS(i) = NaN;
154             FlyingCapHWDSNOCP(i) = NaN;
155         end
156     end
157
158     %RecordData
159     if (~isempty(OutputCapHW_result))
160         CapHWDSWeight = sum(FlyingCapHWDSWeight) + OutputCapHWWeight*n;
161         HWDSinfo(n).TotalWeight = CapHWDSWeight;
162         HWDSinfo(n).FlyingCapacitorValue = FlyingCapHWDSCAP;
163         HWDSinfo(n).FlyingCapacitorVoltageRating = FlyingCapHWDSRVI;
164         HWDSinfo(n).NumberOfFlyingCapacitorInSeries = FlyingCapHWDSNOCS;
165         HWDSinfo(n).NumberOfFlyingCapacitorInParallel = FlyingCapHWDSNOCP;
166         HWDSinfo(n).TotalCapacitance = n*OutputCapHW_result(2)*OutputCapHW_result(5)/
                OutputCapHW_result(4) + sum(FlyingCapHWDSCAP.*FlyingCapHWDSNOCP./
                FlyingCapHWDSNOCS);
167         HWDSinfo(n).FlyingCapEnergy = 0.5*sum(FlyingCapHWDS.*FlyingCapHWDS_Vlimt.^2);
168         HWDSinfo(n).OutputCapEnergy = 0.5*n*OutputCapHW*OutputCapHW_Vlimt^2;
169         HWDSinfo(n).OutputImpedance = (n/FlyingCapHWDS*10^12 + n*(n-1)*(4*n+1)/12/
                OutputCapHW*10^12)/f;
170     else
171         CapHWDSWeight = Inf;
172     end
173
174     %Flying cap for DS full wave
175     FlyingCapFWDS = n/2/((Impedance)*f)*10^12; %capacitance need for fullwave Dickson
176     for i = 1:n
177         FlyingCapFWDS_Vlimt(i) = (i-0.5)*Vo/n; %for FWDS, conversion ratio is n, so input
                is Vac = Vo/n;FET stress is (i-1)*Vac
```

```
    FlyingCapFWDS_result = CapacitorWeight(FlyingCapFWDS, FlyingCapFWDS_Vlimt(i));
    if ((~isempty(FlyingCapFWDS_result)) && (~isempty(OutputCapFW_result)))
        FlyingCapFWDSWeight(i) = FlyingCapFWDS_result(1);
        FlyingCapFWDSCAP(i) = FlyingCapFWDS_result(2);
        FlyingCapFWDSRVI(i) = FlyingCapFWDS_result(3);
        FlyingCapFWDSNOCS(i) = FlyingCapFWDS_result(4);
        FlyingCapFWDSNOCP(i) = FlyingCapFWDS_result(5);
    else
        FlyingCapFWDSWeight(i) = Inf;
        FlyingCapFWDSCAP(i) = NaN;
        FlyingCapFWDSRVI(i) = NaN;
        FlyingCapFWDSNOCS(i) = NaN;
        FlyingCapFWDSNOCP(i) = NaN;
    end
end
%RecordData
if (~isempty(OutputCapFW_result))
    CapFWDSWeight = 2*sum(FlyingCapFWDSWeight) + OutputCapFWWeight*n;
    FWDSinfo(n).TotalWeight = CapFWDSWeight;
    FWDSinfo(n).FlyingCapacitorValue = FlyingCapFWDSCAP;
    FWDSinfo(n).FlyingCapacitorVoltageRating = FlyingCapFWDSRVI;
    FWDSinfo(n).NumberOfFlyingCapacitorInSeries = FlyingCapFWDSNOCS;
    FWDSinfo(n).NumberOfFlyingCapacitorInParallel = FlyingCapFWDSNOCP;
    FWDSinfo(n).TotalCapacitance = n*OutputCapFW_result(2)*OutputCapFW_result(5)/
        OutputCapFW_result(4) + 2*sum(FlyingCapFWDSCAP.*FlyingCapFWDSNOCP./
        FlyingCapFWDSNOCS);
    FWDSinfo(n).FlyingCapEnergy = 2*0.5*sum(FlyingCapFWDS.*FlyingCapFWDS_Vlimt.^2);
    FWDSinfo(n).OutputCapEnergy = 0.5*n*OutputCapFW*OutputCapFW_Vlimt^2;
    FWDSinfo(n).OutputImpedance = (n/2/FlyingCapFWDS)/f*10^12;
else
    CapFWDSWeight = Inf;
end
y = [CapHWCWWeight, CapHWDSWeight, CapFWCWWeight, CapFWDSWeight];
end
```

J.1.2 Inverter and transformer optimization

Listing J.4: Main code to optimize the weight of the inverter and transformer in the 1st-gen high voltage dc-dc converter

```
clc,clf,clear all
close all

%Read the core loss xlsx
corelossfile = 'CoreLossData.xlsx';
[num,txt,raw1] = xlsread(corelossfile,'Freq');
[num,txt,raw2] = xlsread(corelossfile,'Bfield');
[num,txt,raw3] = xlsread(corelossfile,'Ploss');
[num,txt,raw4] = xlsread(corelossfile,'BSAT');
[num,txt,raw5] = xlsread(corelossfile,'MU');

%Read the core size xlsx
coresizefile = 'CoreSizeData.xlsx';
[num,txt,raw] = xlsread(coresizefile,'Ecore');

Date = 'xxx';
% Quality factor
Q_range = 0.1:0.1:10;
% Natural frequency
f0_range = 480000;
% Capacitance ratio
A_range = 0.1:0.1:10;
```

```
% Turns ratio
K_range = 5:1:30;
% DC input voltage range
Vin_range = 200;
% Peak amplitude of the output voltage that one hope to achieve (V)
Vo_range = 7500;
% Output power desired (W)
Po_range = 750;
% frequency of the transformer
fs_range = 500000;
% Winding Pattern Index: 1 inidcates center leg winding, 2 indicates double
Winding_Pattern = 1;
% Hypothesis: record why you want to run the sim
Hypothesis = [''];
% Notes: record any changes you made to the code
Notes = '';

filename_xfmer = strcat(Date,'_','xxx.xlsx');
filename_inductor = strcat(Date,'_','xxx.xlsx');
SheetNumber = 1;
Infosheetname = strcat('SimInfo',num2str(SheetNumber));
ResultDatasheetname = strcat('ResultsData',num2str(SheetNumber));

[Q,f0,A,K] = ndgrid(Q_range,f0_range,A_range,K_range);
Q = reshape(Q,[],1);
f0 = reshape(f0,[],1);
A = reshape(A,[],1);
K = reshape(K,[],1);

RT = 8/pi^2*40000^2/700/6/6./K.^2;
Ls = RT./(2*pi.*f0.*Q);
Cs = Q.*(A+1)./(A*2*pi.*f0.*RT);
Cp = Q.*(A+1)./(2*pi.*f0.*RT);
GT = 4/pi./(sqrt((1+A).^2.*(1-(fs_range./f0).^2).^2 + 1./Q.^2.*(fs_range./f0 - A.*f0
    ./((A+1).*fs_range)).^2));
Imax = Vin_range.*GT./RT.*sqrt(1 + (fs_range./f0).^2.*Q.^2.*(A + 1).^2);

KeepIndex = intersect(find(GT.*K >= Vo_range/Vin_range), find(GT.*K <= 1.2*Vo_range/
    Vin_range));
KeepIndex = intersect(KeepIndex,find(GT > 1));

Q = Q(KeepIndex);
f0 = f0(KeepIndex);
A = A(KeepIndex);
K = K(KeepIndex);
RT = RT(KeepIndex);
Ls = Ls(KeepIndex);
Cs = Cs(KeepIndex);
Cp = Cp(KeepIndex);
GT = GT(KeepIndex);
Imax = Imax(KeepIndex);

tic
parfor i = 1:1:length(Q)
    % Intermediate voltage
    Vpri = Vin_range.*GT(i);
    % Output voltage on the transformer
    Vsec = Vin_range.*GT(i).*K(i);
    Vinsulation_max = Vsec;
    %Run Xfmer design
    SuceedX = Ecore_actual_EEER_xfmer_LCC(raw,raw1,raw2,raw3,raw4,raw5,...
        Vpri, Vsec, Po_range, fs_range, Vinsulation_max, Winding_Pattern);

    SuceedL = Ecore_actual_EEER_inductor_LCC(raw,raw1,raw2,raw3,raw4,raw5,...
        Vin_range, GT(i), Po_range, fs_range, Ls(i), Imax(i), Winding_Pattern,...
        Q(i), f0(i), A(i), K(i), RT(i), Ls(i), Cs(i), Cp(i), GT(i));

    ResultX(i,:) = SuceedX;
```

```
    ResultL(i,:) = SuceedL;
end
toc
XfmerDesignTable = array2table(ResultX,'VariableNames',{'Po_W','Vppeak_V',...
    'Vspeak_V','Vinsulation_max_V','fs_Hz','matno','CoreMatFreq_Hz','CoreAc_m2',...
    'CoreWindowH_m','CoreWindowW_m','NumOfPri','NumOfSec','RealConversion',...
    'BcoreDensity_T','WirePriDia_m','WirePriFullDia_m','WireSecDia_m',...
    'WireSecFullDia_m','WirePri_Idensity_Aperm2','WireSec_Idensity_Aperm2',...
    'WirePriNstrands','WireSecNstrands','WirePri_per_layer','WirePri_Nlayer',...
    'WireSec_per_layer','WireSec_Nlayer','Ns1','Ns2','Ns3','Ns4','CopperPackingFactor',...
    'PackingFactor','LossCore_W','LossCopper_W','WeightCore_g','WeightPri_copper_g',...
    'WeightPri_Insu_g','WeightSec_copper_g','WeightSec_Insu_g','WeightCore_Insu_g',...
    'TotalWeight_g','TempAbsolute_C','CoreIndex'});
writetable(XfmerDesignTable,filename_xfmer,'Sheet',ResultDatasheetname);

InductorDesignTable = array2table(ResultL,'VariableNames',{'Po_W','Vin_V',...
    'Vpri_V','Vinsulation_max_V','fs_Hz','matno','CoreMatFreq_Hz',...
    'CoreCenterLegL_m','CoreCenterLegT_m','CoreAc_m2','CoreWindowH_m',...
    'CoreWindowW_m','NumOfPri','BcoreDensity_T','WirePriDia_m','WirePriFullDia_m',...
    'WirePri_Idensity_Aperm2','WirePriNstrands','WirePri_per_layer','WirePri_Nlayer',...
    'CopperPackingFactor','PackingFactor','LossCore_W',...
    'LossCopper_W','WeightCore_g','WeightPri_copper_g','WeightPri_Insu_g',...
    'WeightCore_Insu_g','TotalWeight_g','TempAbsolute_C','L','airgap_m','CoreIndex',...
    'Q','f0','A','K','RT','Ls','Cs','Cp','GT'});
writetable(InductorDesignTable,filename_inductor,'Sheet',ResultDatasheetname);

field1 = 'name';
value1_req = {'Date','Hypothesis','Notes',...
    'Q_range','f0_range','A_range','K_range',...
    'Vin_range','Vo_range','Po_range','fs_range','Winding_Pattern'};
field2 = 'data';
value2_req = {Date,Hypothesis,Notes,...
    Q_range,f0_range,A_range,K_range,...
    Vin_range,Vo_range,Po_range,fs_range,Winding_Pattern};

Requirement = struct(field1,value1_req,field2,value2_req);
Requirement_excel = squeeze(struct2cell(Requirement))';
xlswrite(filename_xfmer,Requirement_excel,Infosheetname);
```

Listing J.5: Code to simulate the weight of the high voltage transformer (called in List J.4)

```
function y = Ecore_actual_EEER_xfmer_LCC(raw,raw1,raw2,raw3,raw4,raw5,...
    Vppeak_range, Vspeak_range, Po_range, fs_range, Vinsulation_max_range,
        Winding_Pattern)

% Lowest allowed transformer efficiency
etaXfmer = 0.95;
% Max allowable temperature (C)
Tmax = 90;
% Min allowable temperature (C)
Tmin = 25;
% Max allowable current density in the wire (A/m^2)
Jwmax = 500*100*100;
% Minimal litz diameter one can get (m)
MinLitzDia = 0.07874/1000;% AWG 40. 0.05024/1000; %AWG44
% Dielectric strength of the insulation material (V/m), discount 50%
dielectricstrength_insulation = 0.5*200*1000*100; %TEFLON

% Minimum allowable core cross section radius (m)
```

```
MinPriWinding = 1;
% Maximum primary winding turns
MaxPriWinding = 100;
% Incremental pri winding
IncreNp = 1;
% Maximum layer of primary winding
MaxMlp = 10;
% Incremental pri layers
IncreMlp = 1;
% Maximum layer of secondary winding
MaxMls = 10;
% Incremental sec layers
IncreMls = 1;
% Minimal secondary wire diameter (m)
MinSecWireSize = 0.4/1000; %0.079 is AWG40, 0.4 mm is 178-5790
% Maximum allowable weight (g)
MaxWeight = 2000;
% g/m3, density of the core
CoreDensity = 4.8*1000*1000;
% g/m3, density of copper
CopperDensity = 8.96*1000*1000;
% g/m3, density of core insulation materials
CoreInsulationDensity = 2.2*1000*1000; %TEFLON
% g/m3, density of wire insulation materials
WireInsulationDensity = 2.2*1000*1000; %TEFLON

% all discount factors
% Bmax discount factor
BSAT_discount = 0.75;
% Actual core loss is always higher than the calculated.
CoreLossMultiple = 1.0;
% Maximum packing factor (copper area compared with total window area)
maxpackingfactor = 0.7;
% Minimum packing factor
minpackingfactor = 0.01;
% Winding factor of litz wire, assuming only 80% of wire size is copper
LitzFactor = 0.8;
% Weight of bobbin as a faction of the core insulation
BobbinWeightFactor = 0.5;

% Save design results
Design = zeros(1,43);
% Electrical constants. Normally there is no need to change
% ohm*m, resistivity of copper at 100C
rou = 2.3*1e-8;
% /(ohm*m), conductivity of copper
sigma = 1/rou;
% HA/m2, permeability of freespace
u0 = 4*pi*10^(-7);
% F/m, permittivity of freespace
ebsl0 = 8.854*1e-12;
%% MAIN BODY OF THE CODE STARTS FROM HERE
% ------------------------------------------------------------------------
% Read the material properties to get the P at different B and F map from
% the CoreLossData.xlsx file
% This map will be used to calculate core loss later on
[m1,n1] = size(raw1);
XCoreMAT = raw1(2:m1,2);
XCoreFreq = cell2mat(raw1(2:m1,3:n1));
[m1,n1] = size(raw2);
XCoreBfield = cell2mat(raw2(2:m1,3:n1));
[m1,n1] = size(raw3);
XCorePloss = cell2mat(raw3(2:m1,3:n1));
[m1,n1] = size(raw4);
XCoreBSAT = cell2mat(raw4(2:m1,3:n1));
[m1,n1] = size(raw5);
XCoreMU = cell2mat(raw5(2:m1,3:n1));

```

```
% Constant
Pbar = 500;    %500mW/cm3
PFfactor = 1; %

% Draw out Pv plot vs B then interpolate
NoMat = m1-1;
Ball = 0.001:0.001:1;
MATcolorvector = rand(NoMat,3);
FreqFlag = zeros(size(1:1:NoMat));
for i = 1:1:NoMat
    DataSheetFreq = XCoreFreq(i,~isnan(XCoreFreq(i,:)));
    NoFreq = length(DataSheetFreq)/2;
    colorvector = rand(NoFreq,3);
    for j = 1:1:NoFreq
        %Pv = ConstantA*Bfield+ConstantB
        ConstantA(i,j) = (log10(XCorePloss(i,2*j)) - log10(XCorePloss(i,2*j-1)))/(
            log10(XCoreBfield(i,2*j)) - log10(XCoreBfield(i,2*j-1)));
        ConstantB(i,j) = log10(XCorePloss(i,2*j)) - ConstantA(i,j)*log10(XCoreBfield(
            i,2*j));
        B_atPv_500(i,j) = 10^((log10(Pbar) - ConstantB(i,j))/ConstantA(i,j)); % in T
        F_atPv_500(i,j) = DataSheetFreq(2*j-1); % in Hz
        PF_atPv_500(i,j) = B_atPv_500(i,j)*F_atPv_500(i,j)^PFfactor;

        if (abs(fs_range - F_atPv_500(i,j))./fs_range <= 0.4)
            FreqFlag(i) = 1;
        end
        %Steinmetz
        if (j > 1)
            beta_range(i,j) = log10(XCorePloss(i,2*j)/XCorePloss(i,2*j-1))/log10(
                XCoreBfield(i,2*j)/XCoreBfield(i,2*j-1));
            %Third point
            XCorePloss_3rd(i,j) = 10.^(ConstantA(i,j-1)*log10(XCoreBfield(i,2*j)) +
                ConstantB(i,j-1));
            alpha_range(i,j) = log10(XCorePloss_3rd(i,j)/XCorePloss(i,2*j))/log10(
                DataSheetFreq(2*j-3)/DataSheetFreq(2*j-1)); %(f2/f1)^alpha = P2/P1;
            K1_range(i,j) = XCorePloss(i,2*j)/(XCoreBfield(i,2*j)^beta_range(i,j))/(
                DataSheetFreq(2*j-1)^alpha_range(i,j)); %mW/cm3
            %Repeat frequency 2's steinmetz parameter for frequency 1
            if (j == 2)
                beta_range(i,j-1) = beta_range(i,j);
                alpha_range(i,j-1) = alpha_range(i,j);
                K1_range(i,j-1) = XCorePloss(i,2*j-2)/(XCoreBfield(i,2*j-2)^
                    beta_range(i,j-1))/(DataSheetFreq(2*j-3)^alpha_range(i,j-1));
            end
        end
    end
end
% Core size
[m1,n1] = size(raw);
TransformerCoreIndex = cell2mat(raw(3:m1,1));
XcoreVe = cell2mat(raw(3:m1,3))/(1000^3); % in m
XcoreAe = cell2mat(raw(3:m1,4))/(1000^2);
XcoreLe = cell2mat(raw(3:m1,5))/1000;
XcoreCoreShapeIndex = cell2mat(raw(3:m1,6));
XcorePriW = cell2mat(raw(3:m1,8))/1000;
XcorePriH = cell2mat(raw(3:m1,9))/1000;
XcoreSecW = cell2mat(raw(3:m1,10))/1000;
XcoreSecH = cell2mat(raw(3:m1,11))/1000;
XcoreWindowW = cell2mat(raw(3:m1,12))/1000;
XcoreWindowH = 2*cell2mat(raw(3:m1,13))/1000;
ShuffleIndex = 1:1:length(TransformerCoreIndex);
%-----------------------------------------------------------------------
% DESIGN STARTS FROM HERE

% Limit to core materials based on frequency
CoreMatIndexSweep = find(FreqFlag);

% Vectorize the design space
```

```
[Po, fs, Vppeak, Vspeak, Vinsulation_max, matno_record, ShuffleXcoreIndex, Np, Mlp, Mls] =
    ndgrid(Po_range, fs_range, Vppeak_range, ...
    Vspeak_range, Vinsulation_max_range, CoreMatIndexSweep, ShuffleIndex, ...
    MinPriWinding:IncreNp:MaxPriWinding, 1:IncreMlp:MaxMlp, 1:IncreMls:MaxMls);

Po = reshape(Po,[],1);
fs = reshape(fs,[],1);
Vppeak = reshape(Vppeak,[],1);
Vspeak = reshape(Vspeak,[],1);
Vinsulation_max = reshape(Vinsulation_max,[],1);
matno_record = reshape(matno_record,[],1);
Np = reshape(Np,[],1);
Mlp = reshape(Mlp,[],1);
Mls = reshape(Mls,[],1);
ui = XCoreMU(matno_record);
BSAT = XCoreBSAT(matno_record);
ShuffleXcoreIndex = reshape(ShuffleXcoreIndex,[],1);

% Map XcoreSize to actual size
Ve = XcoreVe(ShuffleXcoreIndex);
Ac = XcoreAe(ShuffleXcoreIndex);
W = XcoreWindowW(ShuffleXcoreIndex);
H = XcoreWindowH(ShuffleXcoreIndex);
Le = XcoreLe(ShuffleXcoreIndex);
PriW = XcorePriW(ShuffleXcoreIndex);
PriH = XcorePriH(ShuffleXcoreIndex);
SecW = XcoreSecW(ShuffleXcoreIndex);
SecH = XcoreSecH(ShuffleXcoreIndex);
XcoreIndex = TransformerCoreIndex(ShuffleXcoreIndex);
XcoreCoreShapeIndex = XcoreCoreShapeIndex(ShuffleXcoreIndex);

% Eliminate some elements based on dimension rule and BSAT rule
Bm_dummy = Vppeak/pi./fs./(2*Np.*Ac);
Keep_Bmindex = find(Bm_dummy < BSAT*BSAT_discount);
KeepIndex = Keep_Bmindex;

Po = Po(KeepIndex);
fs = fs(KeepIndex);
Vppeak = Vppeak(KeepIndex);
Vspeak = Vspeak(KeepIndex);
Vinsulation_max = Vinsulation_max(KeepIndex);
matno_record = matno_record(KeepIndex);
ui = ui(KeepIndex);
BSAT = BSAT(KeepIndex);
H = H(KeepIndex);
W = W(KeepIndex);
Ve = Ve(KeepIndex);
Ac = Ac(KeepIndex);
Le = Le(KeepIndex);
PriW = PriW(KeepIndex);
PriH = PriH(KeepIndex);
SecW = SecW(KeepIndex);
SecH = SecH(KeepIndex);
XcoreIndex = XcoreIndex(KeepIndex);
XcoreCoreShapeIndex = XcoreCoreShapeIndex(KeepIndex);

Np = Np(KeepIndex);
Mlp = Mlp(KeepIndex);
Mls = Mls(KeepIndex);

% Find core loss property that's none zero around the required frequency for each
    design group
FsnoNonzero = F_atPv_500(matno_record,:) > 0;
FsnoIndex = abs(fs - F_atPv_500(matno_record,:))./fs <= 0.4;
matfsIndex = FsnoNonzero.*FsnoIndex;
matfs = F_atPv_500(matno_record,:).*matfsIndex;
K1 = K1_range(matno_record,:).*matfsIndex*1000; %convert from mW/cm3 to W/m3
alpha = alpha_range(matno_record,:).*matfsIndex;
```

```
beta = beta_range(matno_record,:).*matfsIndex;
[rowIdcs, colIdcs] = find(matfs > 0);

% So far, each row of the above represent one DESIGN POINT (that has one
% set of electrical requirements, one core size, one core material, one Np, Mlp and
    Mls);
% Each row of matfs, K1, alpha and beta also correspond to each DESIGN POINT
% However, they have more than one non-zero columns because each material
% may have more than one loss data points in their datasheets around the required
    frequency

% We need to expand the design point to incorporate different loss data
% points for one material.

% Find the indices of unique values in rowIdcs
[UniqueRowIdcs, ind] = unique(rowIdcs,'rows');
ColDuplicate = sum(matfs(UniqueRowIdcs,:)~=0,2);

% Repeat by the number of loss data of each design point
Po = repelem(Po(UniqueRowIdcs),ColDuplicate);
fs = repelem(fs(UniqueRowIdcs),ColDuplicate);
Vppeak = repelem(Vppeak(UniqueRowIdcs),ColDuplicate);
Vspeak = repelem(Vspeak(UniqueRowIdcs),ColDuplicate);
Vinsulation_max = repelem(Vinsulation_max(UniqueRowIdcs),ColDuplicate);
matno_record = repelem(matno_record(UniqueRowIdcs),ColDuplicate);
ui = repelem(ui(UniqueRowIdcs),ColDuplicate);
BSAT = repelem(BSAT(UniqueRowIdcs),ColDuplicate);
H = repelem(H(UniqueRowIdcs),ColDuplicate);
W = repelem(W(UniqueRowIdcs),ColDuplicate);
Ve = repelem(Ve(UniqueRowIdcs),ColDuplicate);
Ac = repelem(Ac(UniqueRowIdcs),ColDuplicate);
Le = repelem(Le(UniqueRowIdcs),ColDuplicate);
XcoreIndex = repelem(XcoreIndex(UniqueRowIdcs),ColDuplicate);
PriW = repelem(PriW(UniqueRowIdcs),ColDuplicate);
PriH = repelem(PriH(UniqueRowIdcs),ColDuplicate);
SecW = repelem(SecW(UniqueRowIdcs),ColDuplicate);
SecH = repelem(SecH(UniqueRowIdcs),ColDuplicate);
XcoreCoreShapeIndex = repelem(XcoreCoreShapeIndex(UniqueRowIdcs),ColDuplicate);

Np = repelem(Np(UniqueRowIdcs),ColDuplicate);
Mlp = repelem(Mlp(UniqueRowIdcs),ColDuplicate);
Mls = repelem(Mls(UniqueRowIdcs),ColDuplicate);
% Reformat loss data into one non-zero vector
matfs = nonzeros(reshape(matfs(UniqueRowIdcs,:)',[],1));
K1 = nonzeros(reshape(K1(UniqueRowIdcs,:)',[],1));
beta = nonzeros(reshape(beta(UniqueRowIdcs,:)',[],1));
alpha = nonzeros(reshape(alpha(UniqueRowIdcs,:)',[],1));

if (isempty(Po))
    y = 0;
else
    %Repeat elements by Primary Wire Number of Strands
    skindepth = 1./sqrt(pi*fs*u0/rou);
    %ds = max(skindepth,MinLitzDia*ones(size(skindepth))); % take the skin depth litz
    ds = MinLitzDia*ones(size(skindepth));
    MinPriNstrands = floor((Po*2/etaXfmer./Vppeak/Jwmax)./(pi*ds.^2/4)) + 1;
    MaxPriNstrands = floor((Po*2/etaXfmer./Vppeak/Jwmax*1.0)./(pi*ds.^2/4)) + 1;

    Po = repelem(Po,[MaxPriNstrands - MinPriNstrands + 1]);
    fs = repelem(fs,[MaxPriNstrands - MinPriNstrands + 1]);
    Vppeak = repelem(Vppeak,[MaxPriNstrands - MinPriNstrands + 1]);
    Vspeak = repelem(Vspeak,[MaxPriNstrands - MinPriNstrands + 1]);
    Vinsulation_max = repelem(Vinsulation_max,[MaxPriNstrands - MinPriNstrands + 1]);
    matno_record = repelem(matno_record,[MaxPriNstrands - MinPriNstrands + 1]);
    ui = repelem(ui,[MaxPriNstrands - MinPriNstrands + 1]);
    BSAT = repelem(BSAT,[MaxPriNstrands - MinPriNstrands + 1]);
    H = repelem(H,[MaxPriNstrands - MinPriNstrands + 1]);
    W = repelem(W,[MaxPriNstrands - MinPriNstrands + 1]);
```

```
279     Ve = repelem(Ve,[MaxPriNstrands - MinPriNstrands + 1]);
280     Ac = repelem(Ac,[MaxPriNstrands - MinPriNstrands + 1]);
281     Le = repelem(Le,[MaxPriNstrands - MinPriNstrands + 1]);
282     XcoreIndex = repelem(XcoreIndex,[MaxPriNstrands - MinPriNstrands + 1]);
283     PriW = repelem(PriW,[MaxPriNstrands - MinPriNstrands + 1]);
284     PriH = repelem(PriH,[MaxPriNstrands - MinPriNstrands + 1]);
285     SecW = repelem(SecW,[MaxPriNstrands - MinPriNstrands + 1]);
286     SecH = repelem(SecH,[MaxPriNstrands - MinPriNstrands + 1]);
287     XcoreCoreShapeIndex = repelem(XcoreCoreShapeIndex,[MaxPriNstrands -
            MinPriNstrands + 1]);
288
289     Np = repelem(Np,[MaxPriNstrands - MinPriNstrands + 1]);
290     Mlp = repelem(Mlp,[MaxPriNstrands - MinPriNstrands + 1]);
291     Mls = repelem(Mls,[MaxPriNstrands - MinPriNstrands + 1]);
292     matfs = repelem(matfs,[MaxPriNstrands - MinPriNstrands + 1]);
293     K1 = repelem(K1,[MaxPriNstrands - MinPriNstrands + 1]);
294     beta = repelem(beta,[MaxPriNstrands - MinPriNstrands + 1]);
295     alpha = repelem(alpha,[MaxPriNstrands - MinPriNstrands + 1]);
296     Pri_Nstrands = repmat((MinPriNstrands(1):1:MaxPriNstrands(1))',length(
            MaxPriNstrands),1);
297
298     %Repeat elements by Secondary Wire Number of Strands
299     skindepth = 1./sqrt(pi*fs*u0/rou);
300     ds = MinLitzDia*ones(size(skindepth));
301     MinSecNstrands = 19*ones(size(skindepth));%178-5790 has 19 strands.
302     MaxSecNstrands = 19*ones(size(skindepth));%178-5790 has 19 strands.
303
304     Po = repelem(Po,[MaxSecNstrands - MinSecNstrands + 1]);
305     fs = repelem(fs,[MaxSecNstrands - MinSecNstrands + 1]);
306     Vppeak = repelem(Vppeak,[MaxSecNstrands - MinSecNstrands + 1]);
307     Vspeak = repelem(Vspeak,[MaxSecNstrands - MinSecNstrands + 1]);
308     Vinsulation_max = repelem(Vinsulation_max,[MaxSecNstrands - MinSecNstrands + 1]);
309     matno_record = repelem(matno_record,[MaxSecNstrands - MinSecNstrands + 1]);
310     ui = repelem(ui,[MaxSecNstrands - MinSecNstrands + 1]);
311     BSAT = repelem(BSAT,[MaxSecNstrands - MinSecNstrands + 1]);
312     H = repelem(H,[MaxSecNstrands - MinSecNstrands + 1]);
313     W = repelem(W,[MaxSecNstrands - MinSecNstrands + 1]);
314     Ve = repelem(Ve,[MaxSecNstrands - MinSecNstrands + 1]);
315     Ac = repelem(Ac,[MaxSecNstrands - MinSecNstrands + 1]);
316     Le = repelem(Le,[MaxSecNstrands - MinSecNstrands + 1]);
317     XcoreIndex = repelem(XcoreIndex,[MaxSecNstrands - MinSecNstrands + 1]);
318     PriW = repelem(PriW,[MaxSecNstrands - MinSecNstrands + 1]);
319     PriH = repelem(PriH,[MaxSecNstrands - MinSecNstrands + 1]);
320     SecW = repelem(SecW,[MaxSecNstrands - MinSecNstrands + 1]);
321     SecH = repelem(SecH,[MaxSecNstrands - MinSecNstrands + 1]);
322     XcoreCoreShapeIndex = repelem(XcoreCoreShapeIndex,[MaxSecNstrands -
            MinSecNstrands + 1]);
323
324     Np = repelem(Np,[MaxSecNstrands - MinSecNstrands + 1]);
325     Mlp = repelem(Mlp,[MaxSecNstrands - MinSecNstrands + 1]);
326     Mls = repelem(Mls,[MaxSecNstrands - MinSecNstrands + 1]);
327     matfs = repelem(matfs,[MaxSecNstrands - MinSecNstrands + 1]);
328     K1 = repelem(K1,[MaxSecNstrands - MinSecNstrands + 1]);
329     beta = repelem(beta,[MaxSecNstrands - MinSecNstrands + 1]);
330     alpha = repelem(alpha,[MaxSecNstrands - MinSecNstrands + 1]);
331     Pri_Nstrands = repelem(Pri_Nstrands,[MaxSecNstrands - MinSecNstrands + 1]);
332     Sec_Nstrands = repmat((MinSecNstrands(1):1:MaxSecNstrands(1))',length(
            MaxSecNstrands),1);
333
334     % Recalculate several parameters
335     k = Vspeak./Vppeak;
336     Ns = round(Np.*k)+1;
337     % Primary current (A)
338     Iprms = Po/etaXfmer./(Vppeak/sqrt(2));
339     Ippeak = Iprms*sqrt(2);
340     % Secondary current (A)
341     Isrms = Po./(Vspeak/sqrt(2));
342     Ispeak = Isrms*sqrt(2);
```

```
343     skindepth = 1./sqrt(pi*fs*u0/rou);
344     ds = MinLitzDia*ones(size(skindepth));
345
346     % Calculate core loss (W)
347     % ------------------------------------------------------------------
348     % Peak flux, this corresponds to peak to peak flux density
349     lamda = Vppeak./pi./fs;
350     % Equivalent load resistor
351     Rload = Vspeak.*Vspeak./2./Po;
352     % Input power (W)
353     Pin = Po./etaXfmer;
354     % Maximum total loss allowed (W)
355     Ploss_est = Pin - Po;
356     % Window area (m)
357     Wa = H.*W;
358     % Core volume (m3)
359     Vcore = Ve;
360     % Core weight (g)
361     Wcore = Vcore.*CoreDensity;
362     % Calculate Bmax (T)
363     Bm = lamda./(2.*Np.*Ac);
364     % Calculate core loss (W)
365     Pcore = CoreLossMultiple.*Vcore.*K1.*fs.^alpha.*Bm.^beta;
366
367     % Wire
368     % ------------------------------------------------------------------
369     % Primary wire diameter (m)
370     Pri_WireSize = sqrt(Pri_Nstrands.*pi.*ds.^2./4./LitzFactor./pi).*2;
371     % Primary wire diameter (m) including the insulation layer
372     Pri_FullWireSize = Pri_WireSize + (Vppeak./dielectricstrength_insulation).*2;
373     % Secondary wire diameter (m)
374     Sec_WireSize = sqrt(Sec_Nstrands.*pi.*ds.^2./4./LitzFactor./pi).*2;
375     % Secondary wire diameter (m) including the insulation layer
376     Sec_FullWireSize = Sec_WireSize + (Vspeak./dielectricstrength_insulation/2).*2; %
            100% dielectric strength, similar with Rubadue data
377     % For 178-5790 only
378     Sec_FullWireSize = 1.016./1000*ones(size(Sec_WireSize));
379     CopperPacking = (pi.*Pri_WireSize.^2.*Np./4 + pi.*Sec_WireSize.^2.*Ns/2./4)./(H.*
            W);
380     OverallPacking = (pi.*Pri_FullWireSize.^2.*Np./4 + pi.*Sec_FullWireSize.^2.*Ns
            /2./4)./(H.*W);
381
382     % Winding structures of each windings
383     % ------------------------------------------------------------------
384     % Core insulation thickness needed
385     CoreInsulationThickness = Vinsulation_max./dielectricstrength_insulation;
386     % Total length of first layer of winding
387     % Primary turns per layer
388     Pri_PerLayer = floor(Np./Mlp);
389     % Secondary turns per layer
390     Sec_PerLayer = floor(Ns./Mls); %start with E core
391
392     % Winding pattern of secondary
393     % For ER, only allow center leg winding
394     switch Winding_Pattern
395         case 1 %center leg
396             % Secondary turns per layer
397             Sec_PerLayer = floor(Ns./Mls);
398             % Number of rows in section 1, co-center with primary
399             Ns_group1 = floor((H - 2*CoreInsulationThickness)./Sec_FullWireSize);
400             Ns_group2 = zeros(size(Ns_group1));
401             Ns_group3 = zeros(size(Ns_group1));
402             Ns_group4 = zeros(size(Ns_group1));
403             % Supposed secondary winding number if wind as mentioned above
404             SupposeNs = Ns_group1.*Mls;
405             %% Total length of windings
406             TLp = Np.*2.*(PriW + PriH + 4*CoreInsulationThickness + 2.*Mlp.*
                    Pri_FullWireSize);
```

```
407             TLs = Ns.*2.*(PriW + PriH + 4*Mlp.*Pri_FullWireSize + 8*
                    CoreInsulationThickness + 2.*Mls.*Sec_FullWireSize);
408             % Recalculate XcoreCoreShapeIndex == 2, ER cores
409             SelecIndex = find(XcoreCoreShapeIndex == 2);
410             TLp(SelecIndex) = 2.*pi.*Np(SelecIndex).*(PriW(SelecIndex)./2 +
                    CoreInsulationThickness(SelecIndex) + 0.5.*Mlp(SelecIndex).*
                    Pri_FullWireSize(SelecIndex));
411             TLs(SelecIndex) = 2.*pi.*Ns(SelecIndex).*(PriW(SelecIndex)./2 + Mlp(
                    SelecIndex).*Pri_FullWireSize(SelecIndex) + 2*CoreInsulationThickness
                    (SelecIndex) + 0.5.*Mls(SelecIndex).*Sec_FullWireSize(SelecIndex));
412         case 2 %double leg
413             %% Winding pattern
414             % Only consider half because symmetric
415             Sec_PerLayer = floor(Ns./2./Mls);
416             % Winding on double leg
417             Ns_group1 = zeros(size(Sec_PerLayer)); % does not wind on center leg
418             Ns_group2 = floor((W - 3*CoreInsulationThickness - Mlp.*Pri_FullWireSize)
                    ./Sec_FullWireSize);
419             Ns_group3 = floor((H - 2*CoreInsulationThickness - 2*Mls.*
                    Sec_FullWireSize)./Sec_FullWireSize);
420             Ns_group4 = Ns_group2;
421             SupposeNs = Ns_group1.*Mls + Ns_group2.*Mls + Ns_group3.*Mls + Ns_group4
                    .*Mls;
422             %% Total length of windings
423             TLp = Np.*2.*(PriW + PriH + 4*CoreInsulationThickness + 2.*Mlp.*
                    Pri_FullWireSize);
424             TLs = Ns.*2.*(SecW + SecH + 4*CoreInsulationThickness + 2.*Mls.*
                    Sec_FullWireSize);
425         otherwise
426             disp('Wrong winding pattern');
427     end
428
429     % Calculate leakage inductance (not verified or used in this code)
430     Lg = u0.*(W - Mls.*Sec_FullWireSize - Mlp.*Pri_FullWireSize).*SecH./H;    %in
            Henry
431     Xg = 2.*pi.*fs.*Lg;
432     R_pri = Rload./Ns.^2;
433     Lg_Lc_ratio = (W - 2.*CoreInsulationThickness - Mls.*Sec_FullWireSize - Mlp.*
            Pri_FullWireSize).*Le./ui./SecH./H;
434     real_ratio = 1../(1 + Lg_Lc_ratio + Xg./R_pri);
435
436     % Calculate Copper Loss
437     %-------------------------------------------------------------
438     PriKlayer = sqrt(pi.*Pri_Nstrands).*ds./2./(Pri_WireSize);
439     Pri_xp = ds./2./skindepth.*sqrt(pi.*PriKlayer);
440     SecKlayer = sqrt(pi.*Sec_Nstrands).*ds./2./(Sec_WireSize);
441     Sec_xp = ds./2./skindepth.*sqrt(pi.*SecKlayer);
442     Pri_Rdc = rou.*TLp./(pi.*Pri_WireSize.^2./4);
443     Sec_Rdc = rou.*TLs./(pi.*Sec_WireSize.^2./4);
444     Pri_Fr = Pri_xp.*((sinh(2.*Pri_xp) + sin(2.*Pri_xp))./(cosh(2.*Pri_xp) - cos(2.*
            Pri_xp)) + 2.*(Mlp.^2.*Pri_Nstrands - 1)./3.*(sinh(Pri_xp) - sin(Pri_xp))./(
            cosh(Pri_xp) + cos(Pri_xp)));
445     Pri_Rac = Pri_Rdc.*Pri_Fr;
446     Sec_Fr = Sec_xp.*((sinh(2.*Sec_xp) + sin(2.*Sec_xp))./(cosh(2.*Sec_xp) - cos(2.*
            Sec_xp)) + 2.*(Mls.^2.*Sec_Nstrands - 1)./3.*(sinh(Sec_xp) - sin(Sec_xp))./(
            cosh(Sec_xp) + cos(Sec_xp)));
447     Sec_Rac = Sec_Rdc.*Sec_Fr;
448     Pcopper = (Iprms.^2.*Pri_Rac + Isrms.^2.*Sec_Rac);
449
450     % Calculate temperature rise
451     %-------------------------------------------------------------
452     Rth = 16.31.*1e-3.*(Ac.*Wa).^(-0.405);
453     Tafterloss = Rth.*(Pcopper + Pcore) + 25;
454
455     % Calculate the weight
456     %-------------------------------------------------------------
457     WeightPri_copper = pi.*Pri_WireSize.^2./4.*TLp.*CopperDensity;
458     WeightPri_Insu = pi.*(Pri_FullWireSize.^2 - Pri_WireSize.^2)./4.*TLp.*
```

```
        WireInsulationDensity;
459     WeightSec_copper = pi.*Sec_WireSize.^2./4.*TLs.*CopperDensity;
460     WeightSec_Insu = pi.*(Sec_FullWireSize.^2 - Sec_WireSize.^2)./4.*TLs.*
            WireInsulationDensity;
461     WeightCore_Insu = (2.*H.*(PriW + 2*PriH) + 4.*W.*(PriW + 2*PriH) + H.*(2*PriW +
            2*PriH)).*CoreInsulationThickness.*CoreInsulationDensity;
462     % Recalculate XcoreCoreShapeIndex == 2, ER cores
463     SelecIndex = find(XcoreCoreShapeIndex == 2);
464     WeightCore_Insu(SelecIndex) = (sqrt(2)*pi*H(SelecIndex).*PriW(SelecIndex) + ...
465         sqrt(2)*pi*2*W(SelecIndex).*PriW(SelecIndex) + H(SelecIndex)*pi.*PriW(
                SelecIndex)).*CoreInsulationThickness(SelecIndex).*CoreInsulationDensity;
466     TotalWeight = Wcore + WeightPri_copper + WeightSec_copper + WeightPri_Insu + ...
467         WeightSec_Insu + WeightCore_Insu;
468
469     % Filter good designs
470     %-----------------------------------------------------------------
471     B_index = find(Bm < BSAT*BSAT_discount);
472     P_loss_index = find(Pcopper + Pcore <= Ploss_est);
473     Tafterloss_index = find(Tafterloss <= Tmax);
474     Tmin_index = find(Tafterloss >= Tmin);
475     TotalWeight_index = find(TotalWeight < MaxWeight);
476
477     OverallPackingmin_index = find(OverallPacking >= minpackingfactor);
478     OverallPackingmax_index = find(OverallPacking <= maxpackingfactor);
479
480     Mlp_index = find(Mlp.*Pri_FullWireSize <= W - 3*CoreInsulationThickness);
481     Pri_PerLayer_index = find(Pri_PerLayer.*Pri_FullWireSize < H - 2*
            CoreInsulationThickness);
482     % make sure pri and sec has enough insulation in between
483     switch Winding_Pattern
484         case 1 %center leg
485             Mls_index = find(Mls.*Sec_FullWireSize + Mlp.*Pri_FullWireSize <= W - 3*
                    CoreInsulationThickness);
486         case 2 % double leg, Ns2 or Ns4 together with primary fits in the window
                width, Ns3 and primary also fits in the window width
487             Mls_index = intersect(find(Ns_group2.*Sec_FullWireSize + Mlp.*
                        Pri_FullWireSize <= W - 3*CoreInsulationThickness),...
488                     find(Ns_group3.*Sec_FullWireSize + Mlp.*Pri_FullWireSize <= W - 3*
                            CoreInsulationThickness));
489         otherwise
490             disp('Winding pattern does not meet Mls requirement');
491     end
492
493     % Secondary winding index
494     Ns_group1_index = find(Ns_group1 >= 0);
495     Ns_group2_index = find(Ns_group2 >= 0);
496     Ns_group3_index = find(Ns_group3 >= 0);
497     Ns_group4_index = find(Ns_group4 >= 0);
498     SupposeNs_index = find(SupposeNs >= Ns);
499
500     Index_Meet_All = intersect(B_index, P_loss_index);
501     Index_Meet_All = intersect(Index_Meet_All, Tafterloss_index);
502     Index_Meet_All = intersect(Index_Meet_All, Tmin_index);
503     Index_Meet_All = intersect(Index_Meet_All, TotalWeight_index);
504     Index_Meet_All = intersect(Index_Meet_All, OverallPackingmin_index);
505     Index_Meet_All = intersect(Index_Meet_All, OverallPackingmax_index);
506     Index_Meet_All = intersect(Index_Meet_All, Mlp_index);
507     Index_Meet_All = intersect(Index_Meet_All, Pri_PerLayer_index);
508     Index_Meet_All = intersect(Index_Meet_All, Mls_index);
509     Index_Meet_All = intersect(Index_Meet_All, Ns_group1_index);
510     Index_Meet_All = intersect(Index_Meet_All, Ns_group2_index);
511     Index_Meet_All = intersect(Index_Meet_All, Ns_group3_index);
512     Index_Meet_All = intersect(Index_Meet_All, Ns_group4_index);
513     Index_Meet_All = intersect(Index_Meet_All, SupposeNs_index);
514
515     % Sort by total weight and keep only the lightest one
516     %-----------------------------------------------------------------
517     [WeightSort, SortIndex] = sort(TotalWeight(Index_Meet_All));
```

```
518     if (length(SortIndex) >= 1)
519         TotalWeightSortIndex = Index_Meet_All(SortIndex(1:1));
520
521         Design(:,1) = Po(TotalWeightSortIndex);
522         Design(:,2) = Vppeak(TotalWeightSortIndex);
523         Design(:,3) = Vspeak(TotalWeightSortIndex);
524         Design(:,4) = Vinsulation_max(TotalWeightSortIndex);
525         Design(:,5) = fs(TotalWeightSortIndex);
526         Design(:,6) = matno_record(TotalWeightSortIndex);
527         Design(:,7) = matfs(TotalWeightSortIndex);
528
529         Design(:,8) = Ac(TotalWeightSortIndex);
530         Design(:,9) = H(TotalWeightSortIndex);
531         Design(:,10) = W(TotalWeightSortIndex);
532         Design(:,11) = Np(TotalWeightSortIndex);
533         Design(:,12) = Ns(TotalWeightSortIndex);
534         Design(:,13) = real_ratio(TotalWeightSortIndex);
535         Design(:,14) = Bm(TotalWeightSortIndex);
536
537         Design(:,15) = Pri_WireSize(TotalWeightSortIndex);
538         Design(:,16) = Pri_FullWireSize(TotalWeightSortIndex);
539         Design(:,17) = Sec_WireSize(TotalWeightSortIndex);
540         Design(:,18) = Sec_FullWireSize(TotalWeightSortIndex);
541         Design(:,19) = Ippeak(TotalWeightSortIndex)./(pi*Pri_Nstrands(
                TotalWeightSortIndex).*ds(TotalWeightSortIndex).^2/4);
542         Design(:,20) = Ispeak(TotalWeightSortIndex)./(pi*Sec_Nstrands(
                TotalWeightSortIndex).*ds(TotalWeightSortIndex).^2/4);
543
544         Design(:,21) = Pri_Nstrands(TotalWeightSortIndex);
545         Design(:,22) = Sec_Nstrands(TotalWeightSortIndex);
546         Design(:,23) = Pri_PerLayer(TotalWeightSortIndex);
547         Design(:,24) = Mlp(TotalWeightSortIndex);
548         Design(:,25) = Sec_PerLayer(TotalWeightSortIndex);
549         Design(:,26) = Mls(TotalWeightSortIndex);
550         Design(:,27) = Ns_group1(TotalWeightSortIndex);
551         Design(:,28) = Ns_group2(TotalWeightSortIndex);
552         Design(:,29) = Ns_group3(TotalWeightSortIndex);
553         Design(:,30) = Ns_group4(TotalWeightSortIndex);
554
555         Design(:,31) = CopperPacking(TotalWeightSortIndex);
556         Design(:,32) = OverallPacking(TotalWeightSortIndex);
557         Design(:,33) = Pcore(TotalWeightSortIndex);
558         Design(:,34) = Pcopper(TotalWeightSortIndex);
559         Design(:,35) = Wcore(TotalWeightSortIndex);
560         Design(:,36) = WeightPri_copper(TotalWeightSortIndex);
561         Design(:,37) = WeightPri_Insu(TotalWeightSortIndex);
562         Design(:,38) = WeightSec_copper(TotalWeightSortIndex);
563         Design(:,39) = WeightSec_Insu(TotalWeightSortIndex);
564         Design(:,40) = WeightCore_Insu(TotalWeightSortIndex);
565         Design(:,41) = TotalWeight(TotalWeightSortIndex);
566         Design(:,42) = Tafterloss(TotalWeightSortIndex);
567         Design(:,43) = XcoreIndex(TotalWeightSortIndex);
568         y = Design;
569     else
570         y = zeros(1,43);
571     end
572 end
573 end
```

Listing J.6: Code to simulate the weight of the resonant inductor (called in List J.4)

```
1 % This code is to design inductor based on off the shelf cores
2 % for certain sets of electrical requirements.
3 % Assumptions:
4 % . Sine wave on the input and output
5 % . Model core loss using standard steimetz equation
```

```
% . Model copper loss with full Dowell equations

function y = Ecore_actual_EEER_inductor_LCC(raw,raw1,raw2,raw3,raw4,raw5,...
    Vin_range, G_range, Po_range, fs_range, Ls_range, Imax_range, Winding_Pattern,...
    LCC_Q, LCC_f0, LCC_A, LCC_K, LCC_RT, LCC_Ls, LCC_Cs, LCC_Cp, LCC_GT)

% Lowest allowed transformer efficiency
etaInductor = 0.98;
% Max allowable temperature (C)
Tmax = 90;
% Min allowable temperature (C)
Tmin = 25;
% Max allowable current density in the wire (A/m^2)
Jwmax = 500*100*100;
% Minimal litz diameter one can get (m)
MinLitzDia = 0.05024/1000; %AWG44, 0.0316 is AWG48, %0.03983 is AWG46
% Dielectric strength of the insulation material (V/m), discount 50%
dielectricstrength_insulation = 0.5*200*1000*100; %TEFLON
% minimal air gap (m)
mingap = 10e-6;

% Minimum allowable core cross section radius (m)
MinWinding = 1;
% Maximum turns
MaxWinding = 100;
% Incremental winding
IncreN = 1;
% Maximum layer of winding
MaxMl = 5;
% Incremental layers
IncreMl = 1;
% Minimal wire diameter (m)
MinWireSize = 0.079/1000; %AWG28, 0.35 mm is AWG29, 0.079 is AWG40
% Maximum allowable weight (g)
MaxWeight = 1000;
% g/m3, density of the core
CoreDensity = 4.8*1000*1000;
% g/m3, density of copper
CopperDensity = 8.96*1000*1000;
% g/m3, density of core insulation materials
CoreInsulationDensity = 2.2*1000*1000; %TEFLON
% g/m3, density of wire insulation materials
WireInsulationDensity = 2.2*1000*1000; %TEFLON

% all discount factors
% Bmax discount factor
BSAT_discount = 0.75;
% Actual core loss is always higher than the calculated.
CoreLossMultiple = 1.0;
% Maximum packing factor (copper area compared with total window area)
maxpackingfactor = 0.7;
% Minimum packing factor
minpackingfactor = 0.01;
% Winding factor of litz wire, assuming only 80% of wire size is copper
LitzFactor = 0.8;
% Weight of bobbin as a faction of the core insulation
BobbinWeightFactor = 0.5;

% Save design results
Design_inductor = zeros(1,42);
% Electrical constants. Normally there is no need to change
% ohm*m, resistivity of copper at 100C
rou = 2.3*1e-8;
% /(ohm*m), conductivity of copper
sigma = 1/rou;
% HA/m2, permeability of freespace
u0 = 4*pi*10^(-7);
% F/m, permittivity of freespace
```

```
ebs10 = 8.854*1e-12;
%% MAIN BODY OF THE CODE STARTS FROM HERE
% ------------------------------------------------------------
% Read the material properties to get the P at different B and F map from
% the CoreLossData.xlsx file
% This map will be used to calculate core loss later on
[m1,n1] = size(raw1);
XCoreMAT = raw1(2:m1,2);
XCoreFreq = cell2mat(raw1(2:m1,3:n1));
[m1,n1] = size(raw2);
XCoreBfield = cell2mat(raw2(2:m1,3:n1));
[m1,n1] = size(raw3);
XCorePloss = cell2mat(raw3(2:m1,3:n1));
[m1,n1] = size(raw4);
XCoreBSAT = cell2mat(raw4(2:m1,3:n1));
[m1,n1] = size(raw5);
XCoreMU = cell2mat(raw5(2:m1,3:n1));

% Constant
Pbar = 500;    %500mW/cm3
PFfactor = 1; %

% Draw out Pv plot vs B then interpolate
NoMat = m1-1;
Ball = 0.001:0.001:1;
MATcolorvector = rand(NoMat,3);
FreqFlag = zeros(size(1:1:NoMat));
for i = 1:1:NoMat
    DataSheetFreq = XCoreFreq(i,~isnan(XCoreFreq(i,:)));
    NoFreq = length(DataSheetFreq)/2;
    colorvector = rand(NoFreq,3);
    for j = 1:1:NoFreq
        %Pv = ConstantA*Bfield+ConstantB
        ConstantA(i,j) = (log10(XCorePloss(i,2*j)) - log10(XCorePloss(i,2*j-1)))/(
            log10(XCoreBfield(i,2*j)) - log10(XCoreBfield(i,2*j-1)));
        ConstantB(i,j) = log10(XCorePloss(i,2*j)) - ConstantA(i,j)*log10(XCoreBfield(
            i,2*j));
        B_atPv_500(i,j) = 10^((log10(Pbar) - ConstantB(i,j))/ConstantA(i,j)); % in T
        F_atPv_500(i,j) = DataSheetFreq(2*j-1); % in Hz
        PF_atPv_500(i,j) = B_atPv_500(i,j)*F_atPv_500(i,j)^PFfactor;

        if (abs(fs_range - F_atPv_500(i,j))./fs_range <= 0.4)
            FreqFlag(i) = 1;
        end
        %Steinmetz
        if (j > 1)
            beta_range(i,j) = log10(XCorePloss(i,2*j)/XCorePloss(i,2*j-1))/log10(
                XCoreBfield(i,2*j)/XCoreBfield(i,2*j-1));
            %Third point
            XCorePloss_3rd(i,j) = 10.^(ConstantA(i,j-1)*log10(XCoreBfield(i,2*j)) +
                ConstantB(i,j-1));
            alpha_range(i,j) = log10(XCorePloss_3rd(i,j)/XCorePloss(i,2*j))/log10(
                DataSheetFreq(2*j-3)/DataSheetFreq(2*j-1)); %(f2/f1)^alpha = P2/P1;
            K1_range(i,j) = XCorePloss(i,2*j)/(XCoreBfield(i,2*j)^beta_range(i,j))/(
                DataSheetFreq(2*j-1)^alpha_range(i,j)); %mW/cm3
            %Repeat frequency 2's steinmetz parameter for frequency 1
            if (j == 2)
                beta_range(i,j-1) = beta_range(i,j);
                alpha_range(i,j-1) = alpha_range(i,j);
                K1_range(i,j-1) = XCorePloss(i,2*j-2)/(XCoreBfield(i,2*j-2)^
                    beta_range(i,j-1))/(DataSheetFreq(2*j-3)^alpha_range(i,j-1));
            end
        end
    end
end
% Core size
[m1,n1] = size(raw);
TransformerCoreIndex = cell2mat(raw(3:m1,1));
```

```
135 XcoreVe = cell2mat(raw(3:m1,3))/(1000^3); % in m
136 XcoreAe = cell2mat(raw(3:m1,4))/(1000^2);
137 XcoreLe = cell2mat(raw(3:m1,5))/1000;
138 XcoreCoreShapeIndex = cell2mat(raw(3:m1,6));
139 XcorePriW = cell2mat(raw(3:m1,8))/1000;
140 XcorePriH = cell2mat(raw(3:m1,9))/1000;
141 XcoreWindowW = cell2mat(raw(3:m1,12))/1000;
142 XcoreWindowH = 2*cell2mat(raw(3:m1,13))/1000;
143 ShuffleIndex = 1:1:length(TransformerCoreIndex);
144 %-----------------------------------------------------------------
145 % DESIGN STARTS FROM HERE
146
147 CoreMatIndexSweep = find(FreqFlag); % Limit to core materials based on frequency
148
149 % Vectorize the design space
150 [Po, fs, Vin, G, Ls, Imax, matno_record, ShuffleXcoreIndex, Np, Mlp] = ndgrid(Po_range,
        fs_range, Vin_range, ...
151         G_range, Ls_range, Imax_range, CoreMatIndexSweep, ShuffleIndex, MinWinding:IncreN:
              MaxWinding, 1:IncreMl:MaxMl);
152
153 Po = reshape(Po,[],1);
154 fs = reshape(fs,[],1);
155 Vin = reshape(Vin,[],1);
156 G = reshape(G,[],1);
157 Ls = reshape(Ls,[],1);
158 Imax = reshape(Imax,[],1);
159 Vinsulation_max = Vin.*G;
160 matno_record = reshape(matno_record,[],1);
161 ShuffleXcoreIndex = reshape(ShuffleXcoreIndex,[],1);
162 Np = reshape(Np,[],1);
163 Mlp = reshape(Mlp,[],1);
164 ui = XCoreMU(matno_record);
165 BSAT = XCoreBSAT(matno_record);
166
167 Ve = XcoreVe(ShuffleXcoreIndex); % in cm
168 Ac = XcoreAe(ShuffleXcoreIndex);
169 W = XcoreWindowW(ShuffleXcoreIndex);
170 H = XcoreWindowH(ShuffleXcoreIndex);
171 Le = XcoreLe(ShuffleXcoreIndex);
172 PriW = XcorePriW(ShuffleXcoreIndex);
173 PriH = XcorePriH(ShuffleXcoreIndex);
174 XcoreIndex = TransformerCoreIndex(ShuffleXcoreIndex);
175 XcoreCoreShapeIndex = XcoreCoreShapeIndex(ShuffleXcoreIndex);
176
177 % Inductance and air gap
178 Vpri = Vin.*G;
179 L = Ls;
180 airgap = u0.*Ac.*Np.^2./L - Le./ui;
181
182 %  Eliminate some elements based on dimension rule and BSAT rule
183 KeepAirGap = intersect(find(airgap >= mingap),find(airgap <= 0.2*Le));
184 ue = ui./(1+ui.*airgap./Le);
185 Bm_dummy = u0.*Np.*Imax./Le.*ue; %T
186 Keep_Bmindex = find(Bm_dummy < BSAT*BSAT_discount);
187 KeepIndex = intersect(KeepAirGap,Keep_Bmindex);
188
189 Po = Po(KeepIndex);
190 fs = fs(KeepIndex);
191 Vin = Vin(KeepIndex);
192 Vpri = Vpri(KeepIndex);
193 Imax = Imax(KeepIndex);
194 Vinsulation_max = Vinsulation_max(KeepIndex);
195 matno_record = matno_record(KeepIndex);
196 ui = ui(KeepIndex);
197 BSAT = BSAT(KeepIndex);
198
199 PriW = PriW(KeepIndex);
200 PriH = PriH(KeepIndex);
```

```
H = H(KeepIndex);
W = W(KeepIndex);
Ac = Ac(KeepIndex);
Le = Le(KeepIndex);
Ve = Ve(KeepIndex);
Np = Np(KeepIndex);
Mlp = Mlp(KeepIndex);
L = L(KeepIndex);
airgap = airgap(KeepIndex);
XcoreIndex = XcoreIndex(KeepIndex);
XcoreCoreShapeIndex = XcoreCoreShapeIndex(KeepIndex);

% Find core loss property that's none zero around the required frequency for each
    design group
FsnoNonzero = F_atPv_500(matno_record,:) > 0;
FsnoIndex = abs(fs - F_atPv_500(matno_record,:))./fs <= 0.4;
matfsIndex = FsnoNonzero.*FsnoIndex;
matfs = F_atPv_500(matno_record,:).*matfsIndex;
K1 = K1_range(matno_record,:).*matfsIndex*1000; %convert from mW/cm3 to W/m3
alpha = alpha_range(matno_record,:).*matfsIndex;
beta = beta_range(matno_record,:).*matfsIndex;
[rowIdcs, colIdcs] = find(matfs > 0);

% Find the indices of unique values in rowIdcs
[UniqueRowIdcs, ind] = unique(rowIdcs,'rows');
ColDuplicate = sum(matfs(UniqueRowIdcs,:)~=0,2);

% Repeat by the number of loss data of each design point
Po = repelem(Po(UniqueRowIdcs),ColDuplicate);
fs = repelem(fs(UniqueRowIdcs),ColDuplicate);
Vin = repelem(Vin(UniqueRowIdcs),ColDuplicate);
Vpri = repelem(Vpri(UniqueRowIdcs),ColDuplicate);
Imax = repelem(Imax(UniqueRowIdcs),ColDuplicate);
Vinsulation_max = repelem(Vinsulation_max(UniqueRowIdcs),ColDuplicate);
matno_record = repelem(matno_record(UniqueRowIdcs),ColDuplicate);
ui = repelem(ui(UniqueRowIdcs),ColDuplicate);
BSAT = repelem(BSAT(UniqueRowIdcs),ColDuplicate);
PriH = repelem(PriH(UniqueRowIdcs),ColDuplicate);
PriW = repelem(PriW(UniqueRowIdcs),ColDuplicate);
H = repelem(H(UniqueRowIdcs),ColDuplicate);
W = repelem(W(UniqueRowIdcs),ColDuplicate);
Ac = repelem(Ac(UniqueRowIdcs),ColDuplicate);
Le = repelem(Le(UniqueRowIdcs),ColDuplicate);
Ve = repelem(Ve(UniqueRowIdcs),ColDuplicate);
Np = repelem(Np(UniqueRowIdcs),ColDuplicate);
Mlp = repelem(Mlp(UniqueRowIdcs),ColDuplicate);
L = repelem(L(UniqueRowIdcs),ColDuplicate);
airgap = repelem(airgap(UniqueRowIdcs),ColDuplicate);
XcoreIndex = repelem(XcoreIndex(UniqueRowIdcs),ColDuplicate);
XcoreCoreShapeIndex = repelem(XcoreCoreShapeIndex(UniqueRowIdcs),ColDuplicate);
% Reformat loss data into one non-zero vector
matfs = nonzeros(reshape(matfs(UniqueRowIdcs,:)',[],1));
K1 = nonzeros(reshape(K1(UniqueRowIdcs,:)',[],1));
beta = nonzeros(reshape(beta(UniqueRowIdcs,:)',[],1));
alpha = nonzeros(reshape(alpha(UniqueRowIdcs,:)',[],1));

%size(Po)
if (isempty(Po))
    y = 0;
else
    %Repeat elements by Primary Wire Number of Strands
    skindepth = 1./sqrt(pi*fs*u0/rou);
    ds = max(skindepth,MinLitzDia*ones(size(skindepth))); % take the skin depth litz
    ds = MinLitzDia*ones(size(skindepth));
    MinPriNstrands = floor((Imax./Jwmax)./(pi*ds.^2/4)) + 1;
    MaxPriNstrands = floor((Imax./Jwmax*1.0)./(pi*ds.^2/4)) + 1;

    Po = repelem(Po,[MaxPriNstrands - MinPriNstrands + 1]);
```

```
268     fs = repelem(fs,[MaxPriNstrands - MinPriNstrands + 1]);
269     Vin = repelem(Vin,[MaxPriNstrands - MinPriNstrands + 1]);
270     Vpri = repelem(Vpri,[MaxPriNstrands - MinPriNstrands + 1]);
271     Imax = repelem(Imax,[MaxPriNstrands - MinPriNstrands + 1]);
272     Vinsulation_max = repelem(Vinsulation_max,[MaxPriNstrands - MinPriNstrands + 1]);
273     matno_record = repelem(matno_record,[MaxPriNstrands - MinPriNstrands + 1]);
274     ui = repelem(ui,[MaxPriNstrands - MinPriNstrands + 1]);
275     BSAT = repelem(BSAT,[MaxPriNstrands - MinPriNstrands + 1]);
276     PriH = repelem(PriH,[MaxPriNstrands - MinPriNstrands + 1]);
277     PriW = repelem(PriW,[MaxPriNstrands - MinPriNstrands + 1]);
278     H = repelem(H,[MaxPriNstrands - MinPriNstrands + 1]);
279     W = repelem(W,[MaxPriNstrands - MinPriNstrands + 1]);
280     Ac = repelem(Ac,[MaxPriNstrands - MinPriNstrands + 1]);
281     Le = repelem(Le,[MaxPriNstrands - MinPriNstrands + 1]);
282     Ve = repelem(Ve,[MaxPriNstrands - MinPriNstrands + 1]);
283     Np = repelem(Np,[MaxPriNstrands - MinPriNstrands + 1]);
284     Mlp = repelem(Mlp,[MaxPriNstrands - MinPriNstrands + 1]);
285     matfs = repelem(matfs,[MaxPriNstrands - MinPriNstrands + 1]);
286     K1 = repelem(K1,[MaxPriNstrands - MinPriNstrands + 1]);
287     beta = repelem(beta,[MaxPriNstrands - MinPriNstrands + 1]);
288     alpha = repelem(alpha,[MaxPriNstrands - MinPriNstrands + 1]);
289     L = repelem(L,[MaxPriNstrands - MinPriNstrands + 1]);
290     airgap = repelem(airgap,[MaxPriNstrands - MinPriNstrands + 1]);
291     XcoreIndex = repelem(XcoreIndex,[MaxPriNstrands - MinPriNstrands + 1]);
292     XcoreCoreShapeIndex = repelem(XcoreCoreShapeIndex,[MaxPriNstrands -
            MinPriNstrands + 1]);
293     Pri_Nstrands = repmat((MinPriNstrands(1):1:MaxPriNstrands(1))',length(
            MaxPriNstrands),1);
294
295     % Calculate core loss (W)
296     %-------------------------------------------------------------------
297     Iprms = Imax./sqrt(2);
298     ue = ui./(1+ui.*airgap./Le);
299     Bm = u0.*Np.*Imax./Le.*ue; %T
300     % Window area (m)
301     Wa = H.*W;
302     % Core volume (m3)
303     Vcore = Ve;
304     % Core weight (g)
305     Wcore = Vcore.*CoreDensity;
306     % Check core loss (W)
307     Pcore = CoreLossMultiple.*Vcore.*K1.*fs.^alpha.*Bm.^beta;
308
309     % Wire
310     %-------------------------------------------------------------------
311     % Recalculate ds
312     skindepth = 1./sqrt(pi*fs*u0/rou);
313     ds = max(skindepth,MinLitzDia*ones(size(skindepth))); % take the skin depth litz
314     ds = MinLitzDia*ones(size(skindepth)); %take the smallest litz
315     % Primary wire diameter (m)
316     Pri_WireSize = sqrt(Pri_Nstrands.*pi.*ds.^2./4./LitzFactor./pi).*2;
317     % Primary wire diameter (m) including the insulation layer
318     Pri_FullWireSize = Pri_WireSize + (Vin./dielectricstrength_insulation).*2;
319     CopperPacking = (pi.*Pri_WireSize.^2.*Np./4)./(H.*W);
320     OverallPacking = (pi.*Pri_FullWireSize.^2.*Np./4)./(H.*W);
321
322     % Winding structures
323     %-------------------------------------------------------------------
324     % Core insulation thickness needed
325     CoreInsulationThickness = Vinsulation_max./dielectricstrength_insulation;
326     % Turns per layer
327     Pri_PerLayer = floor(Np./Mlp);
328     % Total length of windings
329     % For XcoreCoreShapeIndex == 1, EE cores
330     TLp = Np.*2.*(PriW + PriH + 4*CoreInsulationThickness + 2.*Mlp.*Pri_FullWireSize)
            ;
331     % Recalculate XcoreCoreShapeIndex == 2, ER cores
332     SelecIndex = find(XcoreCoreShapeIndex == 2);
```

```
333     TLp(SelecIndex) = 2.*pi.*Np(SelecIndex).*(PriW(SelecIndex)./2 + ...
334         CoreInsulationThickness(SelecIndex) + 0.5.*Mlp(SelecIndex).*Pri_FullWireSize(
                SelecIndex));
335
336     %Copper Loss
337     %-----------------------------------------------------------------
338     PriKlayer = sqrt(pi.*Pri_Nstrands).*ds./2./(Pri_WireSize);
339     Pri_xp = ds./2./skindepth.*sqrt(pi.*PriKlayer);
340     Pri_Rdc = rou.*TLp./(pi.*Pri_WireSize.^2./4);
341     Pri_Fr = Pri_xp.*((sinh(2.*Pri_xp) + sin(2.*Pri_xp))./(cosh(2.*Pri_xp) - cos(2.*
            Pri_xp)) + 2.*(Mlp.^2.*Pri_Nstrands - 1)./3.*(sinh(Pri_xp) - sin(Pri_xp))./(
            cosh(Pri_xp) + cos(Pri_xp)));
342     Pri_Rac = Pri_Rdc.*Pri_Fr;
343     Pcopper = (Iprms.^2.*Pri_Rac);
344
345     % Calculate temperature rise
346     %-----------------------------------------------------------------
347     Rth = 16.31.*1e-3.*(Ac.*Wa).^(-0.405);
348     Tafterloss = Rth.*(Pcopper + Pcore) + 25;
349
350     % Calcualte the weight
351     %-----------------------------------------------------------------
352     WeightPri_copper = pi.*Pri_WireSize.^2./4.*TLp.*CopperDensity;
353     WeightPri_Insu = pi.*(Pri_FullWireSize.^2 - Pri_WireSize.^2)./4.*TLp.*
            WireInsulationDensity;
354     % For XcoreCoreShapeIndex == 1, EE cores
355     WeightCore_Insu = (2.*H.*(PriW + 2*PriH) + 4.*W.*(PriW + 2*PriH) + H.*(2.*PriW +
            2*PriH)).*CoreInsulationThickness.*CoreInsulationDensity;
356     % Recalculate XcoreCoreShapeIndex == 2, ER cores
357     SelecIndex = find(XcoreCoreShapeIndex == 2);
358     WeightCore_Insu(SelecIndex) = (sqrt(2)*pi*H(SelecIndex).*PriW(SelecIndex) + ...
359         sqrt(2)*pi*2*W(SelecIndex).*PriW(SelecIndex) + H(SelecIndex)*pi.*PriW(
                SelecIndex)).*CoreInsulationThickness(SelecIndex).*CoreInsulationDensity;
360
361     TotalWeight = Wcore + WeightPri_copper + WeightCore_Insu;
362
363     % Filter the designs
364     %-----------------------------------------------------------------
365     B_index = find(Bm < BSAT*BSAT_discount);
366     P_loss_index = find(Pcopper + Pcore <= Po*(1 - etaInductor));
367     Tafterloss_index = find(Tafterloss <= Tmax);
368     Tmin_index = find(Tafterloss >= Tmin);
369     TotalWeight_index = find(TotalWeight < MaxWeight);
370
371     OverallPackingmin_index = find(OverallPacking >= minpackingfactor);
372     OverallPackingmax_index = find(OverallPacking <= maxpackingfactor);
373     Mlp_index = find(Mlp.*Pri_FullWireSize <= W - 2*CoreInsulationThickness);
374     Pri_PerLayer_index = find(Pri_PerLayer.*Pri_FullWireSize < H - 2*
            CoreInsulationThickness);
375
376     Index_Meet_All = intersect(B_index,P_loss_index);
377     Index_Meet_All = intersect(Index_Meet_All,Tafterloss_index);
378     Index_Meet_All = intersect(Index_Meet_All,Tmin_index);
379     Index_Meet_All = intersect(Index_Meet_All,TotalWeight_index);
380     Index_Meet_All = intersect(Index_Meet_All,OverallPackingmin_index);
381     Index_Meet_All = intersect(Index_Meet_All,OverallPackingmax_index);
382     Index_Meet_All = intersect(Index_Meet_All,Mlp_index);
383     Index_Meet_All = intersect(Index_Meet_All,Pri_PerLayer_index);
384
385     % Sort by total weight and keep only the lightest one
386     %-----------------------------------------------------------------
387     [WeightSort,SortIndex] = sort(TotalWeight(Index_Meet_All));
388     if (length(SortIndex) >= 1)
389         TotalWeightSortIndex = Index_Meet_All(SortIndex(1:1));
390
391         Design_inductor(:,1) = Po(TotalWeightSortIndex);
392         Design_inductor(:,2) = Vin(TotalWeightSortIndex);
393         Design_inductor(:,3) = Vpri(TotalWeightSortIndex);
```

```
394             Design_inductor(:,4) = Vinsulation_max(TotalWeightSortIndex);
395             Design_inductor(:,5) = fs(TotalWeightSortIndex);
396             Design_inductor(:,6) = matno_record(TotalWeightSortIndex);
397             Design_inductor(:,7) = matfs(TotalWeightSortIndex);
398
399             Design_inductor(:,8) = PriW(TotalWeightSortIndex);
400             Design_inductor(:,9) = PriH(TotalWeightSortIndex);
401             Design_inductor(:,10) = Ac(TotalWeightSortIndex);
402             Design_inductor(:,11) = H(TotalWeightSortIndex);
403             Design_inductor(:,12) = W(TotalWeightSortIndex);
404             Design_inductor(:,13) = Np(TotalWeightSortIndex);
405             Design_inductor(:,14) = Bm(TotalWeightSortIndex);
406
407             Design_inductor(:,15) = Pri_WireSize(TotalWeightSortIndex);
408             Design_inductor(:,16) = Pri_FullWireSize(TotalWeightSortIndex);
409             Design_inductor(:,17) = Imax(TotalWeightSortIndex)./(pi*Pri_Nstrands(
                    TotalWeightSortIndex).*ds(TotalWeightSortIndex).^2/4);
410
411             Design_inductor(:,18) = Pri_Nstrands(TotalWeightSortIndex);
412             Design_inductor(:,19) = Pri_PerLayer(TotalWeightSortIndex);
413             Design_inductor(:,20) = Mlp(TotalWeightSortIndex);
414
415             Design_inductor(:,21) = CopperPacking(TotalWeightSortIndex);
416             Design_inductor(:,22) = OverallPacking(TotalWeightSortIndex);
417             Design_inductor(:,23) = Pcore(TotalWeightSortIndex);
418             Design_inductor(:,24) = Pcopper(TotalWeightSortIndex);
419             Design_inductor(:,25) = Wcore(TotalWeightSortIndex);
420             Design_inductor(:,26) = WeightPri_copper(TotalWeightSortIndex);
421             Design_inductor(:,27) = WeightPri_Insu(TotalWeightSortIndex);
422             Design_inductor(:,28) = WeightCore_Insu(TotalWeightSortIndex);
423             Design_inductor(:,29) = TotalWeight(TotalWeightSortIndex);
424             Design_inductor(:,30) = Tafterloss(TotalWeightSortIndex);
425             Design_inductor(:,31) = L(TotalWeightSortIndex);
426             Design_inductor(:,32) = airgap(TotalWeightSortIndex);
427             Design_inductor(:,33) = XcoreIndex(TotalWeightSortIndex);
428             Design_inductor(:,34) = LCC_Q.*ones(size(TotalWeightSortIndex));
429             Design_inductor(:,35) = LCC_f0.*ones(size(TotalWeightSortIndex));
430             Design_inductor(:,36) = LCC_A.*ones(size(TotalWeightSortIndex));
431             Design_inductor(:,37) = LCC_K.*ones(size(TotalWeightSortIndex));
432             Design_inductor(:,38) = LCC_RT.*ones(size(TotalWeightSortIndex));
433             Design_inductor(:,39) = LCC_Ls.*ones(size(TotalWeightSortIndex));
434             Design_inductor(:,40) = LCC_Cs.*ones(size(TotalWeightSortIndex));
435             Design_inductor(:,41) = LCC_Cp.*ones(size(TotalWeightSortIndex));
436             Design_inductor(:,42) = LCC_GT.*ones(size(TotalWeightSortIndex));
437             y = Design_inductor;
438         else
439             y = zeros(1,42);
440         end
441 end
442 %toc
443 end
```

J.1.3 Microcontroller

Listing J.7: Main microcontroller c code for the flight test

```
1 /*
2  * File:    main_PWMoutput.c
3  * Author: Yiou He
4  * Company: Massachusetts Institute of Technology, Power Electronics Research Group
5  * Date: June 22, 2016
6  * File Version:  0.1
7  * Other Files Required: p33FJ64GS606.h
```

```
 * Tools Used: MPLAB ICD3
 * Devices Supported by this file: dsPIC 33FJ64GS606
 */

//The HVPC can be started/stopped either by the RC controller or through the UART
//Through UART: send 'a' to precharge the input cap; send 'b' to start the HV; send 'c' to stop the HV
//All the parameters (desired output voltage, ADC calibration, etc) are set in main_PWMoutputDefinitions.h file
//This file records inflight data to FRAM through SPI;
//the "xxx_readclearSPI" program reads the data and save it in a txt file;
//the "xxx_clearSPI" program clears the FRAM on board, prep for a new run.

/* File Description: */
// <editor-fold defaultstate="collapsed" desc="File Description">
/*****************************************************************************
 * This program is for the high voltage power supply version 2 PCB board, it realizes the following functionalities:
 *  - Feedback control and PWM generation:
 *    Measure the output voltage, input voltage and input current to adjust operating frequency, the controller goal is to fix the output voltage at 40 kV.
 *  - Emergency shutdown when:
 *    Battery under voltage;
 *    Battery over temperature;
 *    RC control signal;
 *    Timer is up;
 *  - Storage data:
 *    Input voltage, current, output voltage data;
 *    Battery temperature data;
 *    Accelerometer data;
 * Requires to use the following function blocks:
 * - UART
 * - ADC
 * - PWM
 * - SPI
*****************************************************************************
 * Referenced files:
 * - Microchip example CE159-PWM_PushPull
 * - Microchip example CE160_StdPWM
 * - Microchip example CE166_Dual_Trig_ADC
 * - Dave Otten's assembly file ICNCmain_DaveOtten.s
 * - Microchip dsPIC33FJ64GS606 datasheet
 * - Microchip MPLABICD3 User's Guide for MPLAB X IDE
*****************************************************************************/
// </editor-fold>

#include "xc.h"
#include "p33FJ64GS606.h"
#include "stdio.h"
#include "string.h"
#include "math.h"
#include "dsPIC33FJ64GS606UART.h"
#include "dsPIC33FJ64GS606ADC.h"
#include "dsPIC33FJ64GS606SPI.h"
#include "dsPIC33FJ64GS606PWM.h"
#include "dsPIC33FJ64GS606CLK.h"
#include "dsPIC33FJ64GS606TIMER.h"
#include "dsPIC33FJ64GS606IO.h"
#include "main_PWMoutputDefinitions.h"
/* Configuration Bit Settings */
// <editor-fold defaultstate="collapsed" desc="Configuration Bits Setup">
#pragma config BWRP = WRPROTECT_OFF
/* ------ FBS (0xf80000) ------------------------------------------------------
 *   Boot Segment Write Protect:
 *       BWRP_WRPROTECT_ON     Boot Segment is write protected
 *       BWRP_WRPROTECT_OFF    Boot Segment may be written
 * */
#pragma config GWRP = OFF
```

```
72 /* ------ FGS (0xf80004) ------------------------------------------------------
73  *   General Code Segment Write Protect:
74  *     GWRP_ON                 General Segment is write protected
75  *     GWRP_OFF                General Segment may be written
76  * */
77 #pragma config FNOSC = FRCPLL
78 #pragma config IESO = OFF
79 /* ------ FOSCSEL (0xf80006) -------------------------------------------------
80 ;   Oscillator Source Selection:
81 ;     FNOSC_FRC               Internal Fast RC (FRC), 7.37 MHz
82 ;     FNOSC_FRCPLL            Internal Fast RC with PLL (FRCPLL)
83 ;     FNOSC_PRI               Primary Oscillator (XT, HS, EC)
84 ;     FNOSC_PRIPLL            Primary Oscillator (XT, HS, EC) with PLL
85 ;     FNOSC_SOSC              Secondary Oscillator (SOSC)
86 ;     FNOSC_LPRC              Low-Power RC Oscillator (LPRC)
87 ;     FNOSC_FRCDIV16          Internal Fast RC (FRC) Oscillator with divide-by-16
88 ;     FNOSC_FRCDIVN           Internal Fast RC (FRC) Oscillator with postscaler
89 ;
90 ;   Internal External Switch Over Mode:
91 ;     IESO_OFF                Start up with user-selected oscillator source
92 ;     IESO_ON                 Start up device with FRC, then switch to user-selected
       oscillator source
93 */
94 #pragma config POSCMD = NONE
95 #pragma config OSCIOFNC = OFF
96 #pragma config FCKSM = CSECME
97 /* ------ FOSC (0xf80008) ----------------------------------------------------
98 ;
99 ;   Primary Oscillator Source:
100 ;     POSCMD_EC               EC (External Clock) Mode
101 ;     POSCMD_XT               XT Crystal Oscillator Mode
102 ;     POSCMD_HS               HS Crystal Oscillator Mode
103 ;     POSCMD_NONE             Primary Oscillator disabled
104 ;
105 ;   OSC2 Pin Function:
106 ;     OSCIOFNC_ON             OSC2 is general purpose digital I/O pin
107 ;     OSCIOFNC_OFF            OSC2 is clock output, it will output Fcy but not function
       as REFCLKO.
108 ;
109 ;   Clock Switching Mode bits:
110 ;     FCKSM_CSECME            Both Clock switching and Fail-safe Clock Monitor are
       enabled
111 ;     FCKSM_CSECMD            Clock switching is enabled,Fail-safe Clock Monitor is
       disabled
112 ;     FCKSM_CSDCMD            Both Clock switching and Fail-safe Clock Monitor are
       disabled
113 */
114 #pragma config FWDTEN = OFF
115 /*;   Watchdog Timer Enable:
116 ;     FWDTEN_OFF              Watchdog timer enabled/disabled by user software
117 ;     FWDTEN_ON               Watchdog timer always enabled
118 */
119 #pragma config FPWRT = PWR128
120 /*;------ FPOR (0xf8000c) ----------------------------------------------------
121 ;
122 ;   POR Timer Value:
123 ;     FPWRT_PWR1              Disabled
124 ;     FPWRT_PWR2              2ms
125 ;     FPWRT_PWR4              4ms
126 ;     FPWRT_PWR8              8ms
127 ;     FPWRT_PWR16             16ms
128 ;     FPWRT_PWR32             32ms
129 ;     FPWRT_PWR64             64ms
130 ;     FPWRT_PWR128            128ms
131 ;
132 ;   Enable Alternate SS1 pin bit:
133 ;     ALTSS1_OFF              SS1 is selected as the I/O pin for SPI1
134 ;     ALTSS1_ON               SS1A is selected as the I/O pin for SPI1
```

```
135 ;
136 ;    Enable Alternate QEI1 pin bit:
137 ;      ALTQIO_ON              QEA1A, QEB1A, and INDX1A are selected as inputs to QEI1
138 ;      ALTQIO_OFF             QEA1, QEB1, INDX1 are selected as inputs to QEI1
139  * */
140 #pragma config ICS = PGD2
141 #pragma config JTAGEN = OFF
142 /*;------ FICD (0xf8000e) ------------------------------------------------------
143 ;
144 ;    Comm Channel Select:
145 ;      ICS_NONE               Reserved, do not use
146 ;      ICS_PGD3               Communicate on PGC3/EMUC3 and PGD3/EMUD3
147 ;      ICS_PGD2               Communicate on PGC2/EMUC2 and PGD2/EMUD2
148 ;      ICS_PGD1               Communicate on PGC1/EMUC1 and PGD1/EMUD1
149 ;
150 ;    JTAG Port Enable:
151 ;      JTAGEN_OFF             JTAG is disabled
152 ;      JTAGEN_ON              JTAG is enabled
153  */
154 #pragma config HYST0 = HYST0
155 #pragma config HYST1 = HYST0
156 /*;------ FCMP (0xf80010) ------------------------------------------------------
157 ;
158 ;    Even Comparator Hysteresis Select:
159 ;      HYST0_HYST0            No Hysteresis
160 ;      HYST0_HYST15           15 mV Hysteresis
161 ;      HYST0_HYST30           30 mV Hysteresis
162 ;      HYST0_HYST45           45 mV Hysteresis
163 ;
164 ;    Comparator Hysteresis Polarity (for even numbered comparators):
165 ;      CMPPOL0_POL_RISE       Hysteresis is applied to rising edge
166 ;      CMPPOL0_POL_FALL       Hysteresis is applied to falling edge
167 ;
168 ;    Odd Comparator Hysteresis Select:
169 ;      HYST1_HYST0            No Hysteresis
170 ;      HYST1_HYST15           15 mV Hysteresis
171 ;      HYST1_HYST30           30 mV Hysteresis
172 ;      HYST1_HYST45           45 mV Hysteresis
173 ;
174 ;    Comparator Hysteresis Polarity (for odd numbered comparators):
175 ;      CMPPOL1_POL_RISE       Hysteresis is applied to rising edge
176 ;      CMPPOL1_POL_FALL       Hysteresis is applied to falling edge
177 */
178 // </editor-fold>
179
180 //Definitions
181 int CheckElectrical(double,double,double,double,double);  //Check to see if all
        values are OK
182 //int CheckMechamical(double,double,double,double);  //Check to see if all values are
        OK
183 void AdjustPWM(double,double,double,double);
184 //Operation functions
185 void Prepare(); //200V on, precharge capacitors
186 void Charge(); //charge
187 void Connect();  //200V on, connect converter with 200V
188 void HVOperation(); //200V on, HV on
189 void EndOperation(); //turn off everything
190 //define look up table
191 const double LookUpInputV[7] = {40.0,60.0,80.0,100.0,120.0,140.0,160.0};
192 const double LookUpOutputV[20] = {DesiredOutputV/20.0*10.0,DesiredOutputV/20.0*11.0,
        DesiredOutputV/20.0*12,
193 DesiredOutputV/20.0*13.0,DesiredOutputV/20.0*14,DesiredOutputV/20.0*14.5,
        DesiredOutputV/20.0*15.0,DesiredOutputV/20.0*15.4,DesiredOutputV/20.0*15.8,
194 DesiredOutputV/20.0*16.2,DesiredOutputV/20.0*16.6,DesiredOutputV/20.0*17.0,
        DesiredOutputV/20.0*17.4,DesiredOutputV/20.0*17.8,DesiredOutputV/20.0*18.2,
195 DesiredOutputV/20.0*18.6,DesiredOutputV/20.0*19.0,DesiredOutputV/20.0*19.4,
        DesiredOutputV/20.0*19.8,DesiredOutputV};
196
```

```
/*
const double LookUpOutputV[20] = {DesiredOutputV/20.0*17.5,DesiredOutputV/20.0*17.5,
    DesiredOutputV/20.0*17.5,
DesiredOutputV/20.0*18.0,DesiredOutputV/20.0*18.0,DesiredOutputV/20.0*18.0,
    DesiredOutputV/20.0*18.0,DesiredOutputV/20.0*18.5,DesiredOutputV/20.0*18.5,
DesiredOutputV/20.0*18.5,DesiredOutputV/20.0*18.5,DesiredOutputV/20.0*19.0,
    DesiredOutputV/20.0*19.0,DesiredOutputV/20.0*19.0,DesiredOutputV/20.0*19.0,
DesiredOutputV/20.0*19.5,DesiredOutputV/20.0*19.5,DesiredOutputV/20.0*19.5,
    DesiredOutputV/20.0*19.5,DesiredOutputV};
*/
const double LookUpFreq[10] = {0.0,0.0,0.0,0.0,0.0,0.0,0.0};
int counter = 0;
const int maxcounter = 100;  //150 is 1.5 seconds
int IndexOutput = 0;
const int MaxIndexOutput = 19;
//Define PWM parameters
const int initPWMperiod = (int)((1000000/initPWMTimerFreq - 2000)/1.04) + 1880;
const int initPWMduty = (int)((((1000000/initPWMTimerFreq - 2000)/1.04) + 1880)/2.0);
int PWMperiod = (int)((1000000/initPWMTimerFreq - 2000)/1.04) + 1880; //normal
    operation
int MaxPWMperiod = (int)((1000000/MinPWMTimerFreq - 2000)/1.04) + 1880;
int MinPWMperiod = (int)((1000000/MaxPWMTimerFreq - 2000)/1.04) + 1880;
int PWMduty = (int)((((1000000/initPWMTimerFreq - 2000)/1.04) + 1880)/2.0); //normal
    operation
int MaxPWMduty = (int)((((1000000/MinPWMTimerFreq - 2000)/1.04) + 1880)/2.0);
int MinPWMduty = (int)((((1000000/MaxPWMTimerFreq - 2000)/1.04) + 1880)/2.0);
int PWMdeadtime = (int) initPWMdeadtime; //normal operation
//Define SPI and UART parameters
int long loc = 0;
unsigned int SPIdata = 0;
int SPIdataCounter = 0;
int SPIdataRecorder = 1;
char buf[30];
//Define ADC parameters
int ADCperiod = ADCtimerPeriod*Timer12Freq;  //ADC sample and conversion once in
    ADCperiod/460.5 ms
int ADCcounter = 0;
int ADCsampletime = 0;
double ADCFloat[5] = {0.0,0.0,0.0,0.0,0.0};
double InputVoltage = 0;
double InputCurrent = 0;
double Temperature = 0;
double OutputVoltage = 0;
double LogicBV = 0;
double AccX = 0;
double AccY = 0;
double AccZ = 0;
//Define flag for error code
int FlagE = 0; //Electrical value check error code
//int FlagM = 0; //Mechanical value check error code
int IC1cnt = 0;
unsigned int IC1timeAve = 0;
unsigned int IC1timeTotal = 0;
int FlagINCON = 0; //input capture interrupt switch ON
//int FlagINCOFF = 0; //input capture interrupt switch OFF
int FlagTimerEnd = 0; //timer end, then ignore RC control
//Define timer end interrupt
int EndTimeMSB = 0xD2;  //End time in sec, 0xD2 for 29.49 MHz (115.1953*1000*120), 0
    x1A5 is for 29.49*2 MHz (230.3906*1000*120 = 27646872)
int EndTimeLSB = 0xCA80;  //End time in sec, 0xCA80 for 29.49 MHz, 0xDB98 for 29.49*2
     MHz

int main()
{
    //Initialization
    initIO();
    DischargeCaps();
    initCLK();
```

```
256     initPWM(initPWMperiod, 0, initPWMdeadtime); //initiate with 0% duty cycle for
            PWM1, 100% for PWM2
257     initUART1();
258     //initUART2();
259     initSPI2();
260     //initial ADC
261     initTimer1(ADCperiod);
262     initADC(initPWMperiod);
263     //initial timer counter for 2 mins
264     initTimer45(EndTimeMSB,EndTimeLSB);
265     //initial input interrupt for RC signal
266     initTimer2();
267     initIC1();
268     EnableTimer1();
269     EnableTimer2();
270     EnableTimer45();
271     //EnableADC();
272     EnablePWM();
273     EnableSPI2();
274     EnableUART1();
275     WriteScreen("HelloWorld");
276     sprintf(buf,"MSB is %d , LSB is %u ",EndTimeMSB,EndTimeLSB);
277     WriteScreen(buf);
278     WriteScreen("\n\r");
279     while(1)
280     {
281         if (ADCsampletime == 10)
282         {
283             //LATFbits.LATF6 = 1;
284             InputVoltage = ADCFloat[0];
285             InputCurrent = ADCFloat[3];///ADCsampletime;
286             OutputVoltage = ADCFloat[2];///ADCsampletime;
287             Temperature = ADCFloat[1];///ADCsampletime;
288             LogicBV = ADCFloat[4];///ADCsampletime;
289             ADCsampletime = 0;
290
291             FlagE = CheckElectrical(InputVoltage,InputCurrent,OutputVoltage,LogicBV,
                    Temperature);  //Check to see if all values are OK
292             //Noticed that when start up, the input current is always big, so can we
                    bypass it?
293             if (FlagE == 0)
294             {
295                 if (counter == maxcounter)
296                 {
297                     counter = 0;
298                     IndexOutput = IndexOutput + 1;
299                 }
300                 else counter = counter + 1;
301                 if (IndexOutput >= MaxIndexOutput) IndexOutput = MaxIndexOutput;
302                 AdjustPWM(InputVoltage,InputCurrent,OutputVoltage,LookUpOutputV[
                        IndexOutput]);
303             }
304             else
305             {
306                 EndOperation();
307                 DisableTimer45();
308             }
309             if (SPIdataCounter == 50)  //every 10*50*ADCtiming, SPI
310             {
311                 SPIdataCounter = 0;
312                 SPIdataRecorder ++;
313             }
314             loc = SendThroughSPI(SPIdataRecorder,InputVoltage,InputCurrent,
                    OutputVoltage,LogicBV,loc);
315             //WriteScreenADCdata(FlagE,InputVoltage,InputCurrent,OutputVoltage,
                    Temperature,LogicBV,AccX,AccY,AccZ);
316             SPIdataCounter ++;
317
```

```
318                 //Reset ADC
319                 ADCFloat[0]=0.0;
320                 ADCFloat[1]=0.0;
321                 ADCFloat[2]=0.0;
322                 ADCFloat[3]=0.0;
323                 ADCFloat[4]=0.0;
324                 //LATFbits.LATF6 = 0;
325             }
326         }
327 }
328
329 // Capture Interrupt Service Routine
330 void __attribute__((__interrupt__, no_auto_psv)) _IC1Interrupt(void)
331 {
332     unsigned int t1,t2;
333     unsigned int IC1timePeriod;
334     //LATDbits.LATD4 = 1;
335     t1 = IC1BUF;
336     t2 = IC1BUF;
337     IFS0bits.IC1IF=0;
338     if(t2 > t1)
339         IC1timePeriod = t2 - t1;
340     else
341         IC1timePeriod = (PR2 - t1) + t2;
342     if (IC1timePeriod <= HVOFFminperiod) return;
343     if (IC1timePeriod >= HVONmaxperiod) return;
344     //Take Average
345     if (IC1cnt == 5)
346     {
347         IC1timeAve = floor(((float)(IC1timeTotal))/5.0);
348         IC1timeTotal = 0;
349         IC1cnt = 0;
350     }
351     else
352     {
353         IC1cnt = IC1cnt + 1;
354         IC1timeTotal = IC1timeTotal + IC1timePeriod;
355     }
356     //calculate see whether is turn-on signal or turn-off signal
357     if (IC1timeAve >= HVONminperiod)
358     {
359         if (IC1timeAve <= HVONmaxperiod)
360         {
361             if (FlagTimerEnd == 0)
362             {
363             switch(FlagINCON)
364             {
365                 case 0:
366                     Prepare();
367                     FlagINCON = 1;
368                     //WriteScreen("Pre-charge Caps\n\r");
369                     //PreparePWM();
370                     //Connect();
371                     //HVOperation();
372                     break;
373                 case 1:
374                     FlagINCON = FlagINCON + 1;
375                     //PreparePWM();
376                     break;
377                 case 10:  //50
378                     FlagINCON = FlagINCON + 1;
379                     //Connect();
380                     break;
381                 case 60:
382                     FlagINCON = FlagINCON + 1;
383                     PreparePWM();
384                     Connect();
385                     HVOperation();
```

```
                    break;
                default:
                    FlagINCON = FlagINCON + 1;
            }
            }
        }
    }
    //Following section is correct, does not cause current overshoot
    if (IC1timeAve >= HVOFFminperiod)
    {
        if (IC1timeAve <= HVOFFmaxperiod)
        {
            FlagINCON = 0;
            FlagTimerEnd = 0;
            EndOperation();
            DisableTimer45();
        }
    }
    if (FlagTimerEnd == 1)
    {
        FlagINCON = 0;
        EndOperation();
        DisableTimer45();
    }
}

//Timer 5 interrupt
void __attribute__((__interrupt__, no_auto_psv)) _T5Interrupt(void)
{
    //U1TXREG = 0x55; // Transmit one character
    FlagTimerEnd = 1;
    EndOperation(); //timer is up
    //DisableTimer45();
    IFS1bits.T5IF = 0; // clear TIMER5 interrupt flag
    //if (LATDbits.LATD4 == 0) LATDbits.LATD4 = 1;
    //else if (LATDbits.LATD4 == 1) LATDbits.LATD4 = 0;
}

void __attribute__((__interrupt__, no_auto_psv)) _U1RXInterrupt(void) {

    char receive = 0;
    receive = U1RXREG; // Receive one character
    //U1TXREG = receive;

    switch (receive)
    {
        case 'a':
            U1TXREG = 'a'; //Letter 'a'
            WriteScreen("Pre-charge Caps\n\r");
            Prepare();
            break;
        case 'b':
            U1TXREG = 'b';
            WriteScreen("Normal Operation\n\r");
            PreparePWM();
            Connect();
            HVOperation();
            break;
        case 'c':
            EndOperation();
            U1TXREG = 'c';
            WriteScreen("Converter stopped\n\r");
            break;
        case 'd':
            U1TXREG = 'd';
            WriteScreen("Converter running\n\r");
            break;
        case '=':
```

```
454                 PWMperiod = PWMperiod + 2;
455                 PWMduty = PWMduty + 1;
456                 ChangePD(PWMperiod, PWMduty, initPWMdeadtime);
457                 WriteScreen("Increase period\n\r");
458                 break;
459             case '-':
460                 PWMperiod = PWMperiod - 2;
461                 PWMduty = PWMduty - 1;
462                 ChangePD(PWMperiod, PWMduty, initPWMdeadtime);
463                 WriteScreen("Decrease period\n\r");
464                 break;
465             case 'w':
466                 PWMdeadtime = PWMdeadtime + 2;
467                 ChangePD(PWMperiod, PWMduty, PWMdeadtime);
468                 WriteScreen("Increase deadtime\n\r");
469                 break;
470             case 'e':
471                 PWMdeadtime = PWMdeadtime - 2;
472                 ChangePD(PWMperiod, PWMduty, PWMdeadtime);
473                 WriteScreen("Decrease deadtime\n\r");
474                 break;
475             default:
476                 break;
477         }
478         char buf[50];
479         sprintf(buf,"Period is %d, duty is %d, dtime is %d    ",PWMperiod, PWMduty,
                PWMdeadtime);
480         WriteScreen(buf);
481         WriteScreen("\n\r");
482         IFS0bits.U1RXIF = 0; // clear RX interrupt flag
483     }
484
485     //UART transmitter interrupt, worked.
486     void __attribute__((__interrupt__, no_auto_psv)) _U1TXInterrupt(void)
487     {
488         IFS0bits.U1TXIF = 0; // clear TX interrupt flag
489         //U1TXREG = 0x55; // Transmit one character
490     }
491
492     //UART transmitter interrupt, worked.
493     void __attribute__((__interrupt__, no_auto_psv)) _U2TXInterrupt(void)
494     {
495         IFS1bits.U2TXIF = 0; // clear TX interrupt flag
496         //U2TXREG = 0x55; // Transmit one character
497     }
498
499     //ADC interrupt
500
501     void __attribute__((__interrupt__, no_auto_psv)) _ADCP0Interrupt(void) {
502         IFS6bits.ADCP0IF = 0;
503         //LATFbits.LATF6 = 1;
504         ADCFloat[0] = (double)((unsigned int)(7.0*ADCFloat[0] + (double)ADCBUF0)>>3);//((
                double) ADCBUF0) * (double) (3.3/1023);
505         ADCFloat[1] = (double)((unsigned int)(7.0*ADCFloat[1] + (double)ADCBUF1)>>3);//((
                double) ADCBUF1) * (double) (3.3/1023);
506         //LATFbits.LATF6 = 0;
507     }
508
509     void __attribute__((__interrupt__, no_auto_psv)) _ADCP1Interrupt(void) {
510         IFS6bits.ADCP1IF = 0;
511         ADCFloat[2] = (double)((unsigned int)(7.0*ADCFloat[2] + (double)ADCBUF2)>>3);
512         ADCFloat[3] = (double)((unsigned int)(7.0*ADCFloat[3] + (double)ADCBUF3)>>3);
513     }
514
515     void __attribute__((__interrupt__, no_auto_psv)) _ADCP2Interrupt(void) {
516         IFS7bits.ADCP2IF = 0;
517         ADCFloat[4] = (double)((unsigned int)(7.0*ADCFloat[4] + (double)ADCBUF4)>>3);
518         //ADCFloat[5] = (double) ADCBUF5 + ADCFloat[5];
```

```
519     ADCsampletime = ADCsampletime + 1;
520 }
521 /*void __attribute__((__interrupt__, no_auto_psv)) _ADCP3Interrupt(void) {
522     IFS7bits.ADCP3IF = 0;
523     ADCFloat[6] = (double) ADCBUF6 + ADCFloat[6];
524     ADCFloat[7] = (double) ADCBUF7 + ADCFloat[7];
525     //LATFbits.LATF6 = 0;
526     ADCsampletime = ADCsampletime + 1;
527 }
528 */
529 //SPI transmit interrupt
530 void __attribute__((__interrupt__, no_auto_psv)) _SPI2Interrupt(void)
531 {
532     //U2TXREG = SPIdata; // Transmit the received SPIdata
533     //if (LATFbits.LATF6 == 1)
534     //    LATFbits.LATF6 = 0;
535     //else LATFbits.LATF6 = 1;
536     IFS2bits.SPI2IF = 0; // clear SPI2 interrupt flag
537 }
538
539 int CheckElectrical(double InputVoltage,double InputCurrent,double OutputVoltage,
        double LogicBV, double Temperature)  //Check to see if all values are OK
540 {
541     if (IndexOutput == 0)
542         return 0;
543     else
544     {
545         if (((InputVoltage*InputVScale + InputVOffset) < MinInputV) || ((InputVoltage
                *InputVScale + InputVOffset) > MaxInputV)) return 1;
546         else if ((InputCurrent*InputIScale + InputIOffset) > MaxInputI) return 2;
547         //else if ((OutputVoltage*OutputVScale + OutputVOffset) > MaxOutputV) return
                3;
548         //else if (((LogicBV*LogicBVScale + LogicBVOffset) < MinLogicBV) || ((LogicBV
                *LogicBVScale + LogicBVOffset) > MaxLogicBV)) return 4;
549         //else if (Temperature*TempScale + TempOffset > MaxTemp) return 5;
550         return 0;
551     }
552 }
553
554 void AdjustPWM(double InputVoltage,double InputCurrent,double OutputVoltage,double
        SetOutputV)
555 {
556     if ((OutputVoltage*OutputVScale + OutputVOffset) < SetOutputV)
557     {
558         PWMperiod = PWMperiod + 2;
559         PWMduty = PWMduty + 1;
560     }
561     else if ((OutputVoltage*OutputVScale + OutputVOffset) > SetOutputV)
562     {
563         PWMperiod = PWMperiod - 2;
564         PWMduty = PWMduty - 1;
565     }
566     if (PWMperiod > MaxPWMperiod) PWMperiod = MaxPWMperiod;
567     if (PWMperiod < MinPWMperiod) PWMperiod = MinPWMperiod;
568     if (PWMduty > MaxPWMduty) PWMduty = MaxPWMduty;
569     if (PWMduty < MinPWMduty) PWMduty = MinPWMduty;
570     ChangePD(PWMperiod, PWMduty, initPWMdeadtime);
571     //Check with look up table
572 }
573
574 void Prepare() //200V on, precharge capacitors
575 {
576     //clear timer45 flag
577     FlagTimerEnd = 0;
578     DisablePWM();
579     DisableTimer45();
580     //Change PWM to initial states
581     initChangePD(initPWMperiod, 0, initPWMdeadtime);
```

```
582     PWMperiod = initPWMperiod;
583     PWMduty = initPWMduty;
584     PWMdeadtime = initPWMdeadtime;
585     //restart output voltage profile and create delays
586     counter = 0;
587     IndexOutput = 0;
588     //PrechargePWM();
589     //PreparePWM();
590     Precharge();
591 }
592
593 void Connect()  //200V on, connect converter with 200V
594 {
595     EnablePWM();
596     //Precharge();
597 }
598 void HVOperation() //200V on, HV on
599 {
600     ChangePD(initPWMperiod, initPWMduty, initPWMdeadtime);
601     NormalOperation();
602     HVon();
603     //EnablePWM();
604     EnableTimer45(); //start timer 45 to detect 2 mins.
605     EnableADC();
606     EnableSPI2();
607 }
608 void EndOperation()
609 {
610     //clear timer flag
611     //FlagTimerEnd = 0;
612     DischargeCaps();
613     //Reinitiate PWM
614     DisablePWM();
615     //PrechargePWM();
616     DisableADC();
617     DisableSPI2();
618     counter = 0;
619     IndexOutput = 0;
620 }
```

Listing J.8: Main microcontroller header code for the flight test

```
1  /*
2   * File:   dsPIC33FJ64GS606TIMER.h
3   * Author: Yiou He
4   * Comments: header file of the definitions in the main file
5   * Revision history: v1
6   */
7
8  // This is a guard condition so that contents of this file are not included
9  // more than once.
10 #ifndef XC_HEADER_mainDefinition_H
11 #define XC_HEADER_mainDefinition_H
12
13 #include <xc.h> // include processor files - each processor file is guarded.
14 #include "p33FJ64GS606.h"
15 #include "stdio.h"
16 #include "string.h"
17
18 //define constants
19 #define initPWMTimerFreq 700.0 //unit in kHz
20 #define MinPWMTimerFreq 480.0 //unit in kHz
21 #define MaxPWMTimerFreq 700.0 //unit in kHz
22 #define initPWMdeadtime 45.0   //unit in ns
23 #define Timer12Freq 29.49/64.0*1000.0 //Timer 1 and 2's frequency in terms of 1 ms,
       times 2.0 adjusted for the 58 MHz
```

```
#define ADCtimerPeriod 1  //unit in ms, the period of ADC sampling is 1 ms
#define IC1timer2Period 2.5*Timer12Freq  //unit in ms, the period of the timer for RC signal
#define HVOFFminperiod 0.7*Timer12Freq    //0.7,unit in ms, minimum pulse width of RC on signal
#define HVOFFmaxperiod 1.1*Timer12Freq    //1.1,unit in ms, max pulse width of RC on signal
#define HVONminperiod 1.7*Timer12Freq    //1.7, unit in ms, minimum pulse width of RC off signal
#define HVONmaxperiod 2.2*Timer12Freq    //2.2,unit in ms, max pulse width of RC off signal
#define ADCScale 3.3/1023.0  //ADC scale
#define CalibratedScale 0.7  //calibrated input and output voltage scale factor
#define InputVScale 0.4327//0.4338//0.4596//0.4598 //0.3197   //,Calibrated on 06102017 //0.324    //Calibrated on March 2017
#define InputVOffset 2.0681//1.8397//1.0663//2.5139 //-0.0686  //,Calibrated on 06102017   //0.5296  //Calibrated on March 2017
#define InputIScale 0.0197//0.0213//0.021//0.0143    //,Calibrated on 06102017//0.0323 Calibrated on March 2017
#define InputIOffset -9.3941//-9.6692//-9.4371//-7.8522  //,Calibrated on 06102017//-17.031 Calibrated on March 2017
#define OutputVScale 76.574//81.363//82.66//82.936 //58.082  //,Calibrated on 06102017//56.577     //Calibrated on March 2017
#define OutputVOffset 534.23//367.65//225.48//-266.63 //342.97  //,Calibrated on 06102017//132.27    //Calibrated on March 2017
#define TempScale 1.0/(0.005*(100.0/24.9+1.0))*ADCScale
#define TempOffset 15.0  //change to 0 on June 3   //15 degree offset
#define AccScale 1.0/(100.0/24.9+1.0)*ADCScale/CalibratedScale
#define AccOffset 0.0
#define LogicBVScale 0.0059   //0.0065, Calibrated on Dec 04, 2016
#define LogicBVOffset -0.3132  //1053, Calibrated on Dec 05, 2016
//Sanity check value
#define MaxTemp 130.0
#define MaxInputV 250.0 //*CalibratedScale
#define MinInputV 150.0 //*CalibratedScale //145
#define MaxInputI 4.8 //*CalibratedScale  //if set as 4 A, can't even start
#define MaxOutputV 45000.0 //*CalibratedScale
#define MinOutputV 0 //30000.0 //
#define MinLogicBV 2.9 //*CalibratedScale
#define MaxLogicBV 4.5 //*CalibratedScale
#define ScaleFrom10To8 255.0/1023.0
#define MaxLoc 524287   //2^19 - 1, for FRAM address
//define desired control point
#define DesiredOutputV 40500.0 //*CalibratedScale //unit in Volts, the full desired output voltage,0.7 discount
//define timer
//#define EndTime 120 //unit in second

#endif  /* XC_HEADER_maindefinition_H */
```

Listing J.9: Microcontroller c code (ADC module)

```
/*
 * File:   dsPIC33FJ64GS606ADC.c
 * Author: Yiou
 *
 * Created on July 7, 2016, 9:41 AM
 */

#include "dsPIC33FJ64GS606ADC.h"

void initADC(int period)
{
    //We will use AN 0 -6, pair 0 - 3
    ADCONbits.SLOWCLK = 1;    //ADC is clocked by auxiliary PLL.
    ADCONbits.FORM = 0;       //Integer data format
```

```
    ADCONbits.EIE = 0;       //Interrupt generated after the first conversion is
        completed
    ADCONbits.ORDER = 0;     //Convert even channel first
    ADCONbits.SEQSAMP = 0;    //Shared S&H circuit and dedicated simultaneous sampling
    ADCONbits.ADCS = 5;      //ADC clock = FADC/8 = 120MHz / 8 = 15MHz

    //Set PWM as the trigger source of ADC (changed to Timer 1)
    ADCPC0bits.TRGSRC0 = 12;     //ADC Pair 0 triggered by Timer 1
    ADCPC0bits.TRGSRC1 = 12;     //ADC Pair 1 triggered by Timer 1
    ADCPC1bits.TRGSRC2 = 12;     //ADC Pair 2 triggered by Timer 1
    //ADCPC1bits.TRGSRC3 = 12;     //ADC Pair 3 triggered by Timer 1

    //Clear pair ready bit
    ADSTATbits.P0RDY = 0;        //Clear all pairs data ready bit
    ADSTATbits.P1RDY = 0;        //Clear all pairs data ready bit
    ADSTATbits.P2RDY = 0;        //Clear all pairs data ready bit
    //ADSTATbits.P3RDY = 0;        //Clear all pairs data ready bit

    //Set interrupt
    //ADCPC0bits.IRQEN0 = 1;         //Enable ADC Interrupt pair 0
    IFS6bits.ADCP0IF = 0;      //Clear ADC Pair 0 interrupt flag
    IEC6bits.ADCP0IE = 1;      //Enable the ADC Pair 0 interrupt
    IFS6bits.ADCP1IF = 0;      //Clear ADC Pair 1 interrupt flag
    IEC6bits.ADCP1IE = 1;      //Enable the ADC Pair 1 interrupt
    IFS7bits.ADCP2IF = 0;      //Clear ADC Pair 2 interrupt flag
    IEC7bits.ADCP2IE = 1;      //Enable the ADC Pair 2 interrupt
    //IFS7bits.ADCP3IF = 0;      //Clear ADC Pair 3 interrupt flag
    //IEC7bits.ADCP3IE = 1;      //Enable the ADC Pair 3 interrupt

    //Set the PWM trigger
    //TRGCON1bits.TRGDIV = 15;  //Set the trigger event to divide by 16
  //TRGCON1bits.TRGSTRT = 0;  // enable Trigger generated after 0 PWM cycles
    //TRIG1 = period; //Trigger every time when it reaches to the period.
}

void EnableADC()
{
    ADCONbits.ADON = 1;
}

void DisableADC()
{
    ADCONbits.ADON = 0;
}
```

Listing J.10: Microcontroller header code (ADC module)

```
/*
 * File:   dsPIC33FJ64GS606ADC.h
 * Author: Yiou He
 * Comments: header file of the dsPIC33FJ64GS606 ADC unit
 * Revision history: v1
 */

// This is a guard condition so that contents of this file are not included
// more than once.
#ifndef XC_HEADER_ADC_H
#define XC_HEADER_ADC_H

#include <xc.h> // include processor files - each processor file is guarded.
#include "p33FJ64GS606.h"
#include "stdio.h"
#include "string.h"

void initADC(int period);
void EnableADC();
```

```
20 void DisableADC();
21
22 #endif  /* XC_HEADER_ADC_H*/
```

Listing J.11: Microcontroller c code (Clock module)

```
1  /*
2   * File:   dsPIC33FJ64GS606CLK.c
3   * Author: Yiou
4   *
5   * Created on July 7, 2016, 9:55 AM
6   */
7
8  #include "dsPIC33FJ64GS606CLK.h"
9
10 void initCLK() //working, tested on 7/5/2016
11 {
12     //Tune the OSC
13     OSCTUNbits.TUN = 0b111011; //Tune the frequency to lower
14     /* Configure Oscillator to operate the device at 29.84 Mhz
15      Fosc= Fin*M/(N1*N2), Fcy=Fosc/2
16      Fosc= 7.37*(64)/(4*2) = Mhz for Fosc, Fcy = 29.84 Mhz
17        Under this condition, Icc = 61 mA) */
18   /* Configure PLL prescaler, PLL postscaler, PLL divisor */
19
20     PLLFBD = 62;          /* M = PLLFBD + 2, working */
21   CLKDIVbits.PLLPOST = 1;    /* N1 = 4, working, if PLLPOST = 0, N1 = 2*/
22   CLKDIVbits.PLLPRE = 0;     /* N2 = 2, working */
23     //Check FRCDIV, working CLKDIVbits.FRCDIV = 1;  /* Divide FRC with 2*/
24     while(OSCCONbits.LOCK != 1);       /* Wait for Pll to Lock */
25     //OSCCONbits.NOSC =
26     //Reference CLK output (OSC2 should be set as general IO to enable this function,
           working)
27     //REFOCONbits.ROSEL = 0;  // Reference Clock Source Select System Clock
28     //REFOCONbits.RODIV = 15;  //Divide the main clock by 32768, Fosc is 80MHz,
           Reference CLK should be 2.41 kHz
29     //REFOCONbits.ROON = 1;    //Reference Oscillator is enabled at pin 40
30
31     /* Now setup the ADC and PWM clock for 120MHz
32      ((FRC * 16) / APSTSCLR ) = (7.37 * 16) / 1 = ~ 120MHz*/
33   ACLKCONbits.FRCSEL = 1;         /* FRC provides input for Auxiliary PLL (x16) */
34   ACLKCONbits.SELACLK = 1;          /* Auxiliary Oscillator provides clock source for
       PWM & ADC */
35   ACLKCONbits.APSTSCLR = 7;       /* Divide Auxiliary clock by 1 */
36   ACLKCONbits.ENAPLL = 1;         /* Enable Auxiliary PLL */
37     while(ACLKCONbits.APLLCK != 1);    /* Wait for Auxiliary Pll to Lock */
38 }
```

Listing J.12: Microcontroller header code (Clockmodule)

```
1  /*
2   * File:   dsPIC33FJ64GS606CLK.h
3   * Author: Yiou He
4   * Comments: header file of the dsPIC33FJ64GS606 CLK unit
5   * Revision history: v1
6   */
7
8  // This is a guard condition so that contents of this file are not included
9  // more than once.
10 #ifndef XC_HEADER_CLK_H
11 #define XC_HEADER_CLK_H
12
13 #include <xc.h> // include processor files - each processor file is guarded.
14 #include "p33FJ64GS606.h"
15 #include "stdio.h"
```

```
16 #include "string.h"
17
18 void initCLK();
19
20 #endif  /* XC_HEADER_CLK_H */
```

Listing J.13: Microcontroller c code (IO module)

```
1  /*
2   * File:   dsPIC33FJ64GS606IO.c
3   * Author: Yiou
4   *
5   * Created on July 7, 2016, 9:53 AM
6   */
7
8  #include "dsPIC33FJ64GS606IO.h"
9
10 void initIO()  //working, tested on 7/4/2016
11 {
12     //Initialize the IO port
13     //Use PORT to read, use LAT to write
14     //PortB (Pin 0-4 (ANALOG), 6-7 (Enables), 8 (BT_DSR), 9-13, 15 as output, 14 (
           BT_DTR) as input)
15     LATB = 0x0000;     //Set the latch to zeros for all
16     TRISB = 0x401F; //0b0100000000011111;
17     //PORTC all output (RC12 & 14 as PGED and C)
18     LATC = 0x0000;
19     TRISC = 0x0000;
20     //PORTD all output (NOT USED)
21     LATD = 0x0000;  //RD4 - 7: 200VON, TBD, HV, Logic
22     TRISD = 0x0000;
23     //PORTE all output (RE0 - 3 as PWM output)
24     LATE = 0x0000;
25     TRISE = 0x0000;
26     //PORTF (RF4 - 5 are RX and TX, RF2 - 3 are RX and TX, RF6 is RCStop input)
27     TRISF = 0x0014; //0b0000000000010100
28     LATF = 0x0000;
29     //PORTG (RG6-9 are SCK, SI, SO, CS, SI (RG7) is input)
30     LATG = 0x0000;
31     TRISG = 0x0080;  //0b0000000010000000
32     //Analog and comparator input setting
33     //All analog and comparator pins are default as analog input, need to be set to 1
           when it's used as digital pins
34     //Using AN0 - 4 as analog and comparator input, using AN 6-8, 10, 11, 14 as
           digital IO, not using AN5, 9, 15
35     ADPCFG = 0xFFE0;
36     //Disable comparator pairs
37 }
38
39 void DischargeCaps() //Start to discharge the input caps
40 {
41     //LOGIC IS ON
42     LATBbits.LATB6 = 0;
43     LATBbits.LATB7 = 0;
44     LATDbits.LATD4 = 0;
45     LATDbits.LATD5 = 0;
46     LATDbits.LATD6 = 0;
47     LATDbits.LATD7 = 1;
48 }
49
50 void Precharge()       //Precharge the input caps
51 {
52     //200V is On
53     LATBbits.LATB6 = 1;
54     LATBbits.LATB7 = 0;
55     LATDbits.LATD4 = 1;
```

```
    LATDbits.LATD5 = 0;
    LATDbits.LATD6 = 0;
    LATDbits.LATD7 = 0;
}

void NormalOperation()  //Connect 200V to the switches
{
    //200V is on
    LATBbits.LATB6 = 0;
    LATBbits.LATB7 = 1;
    LATDbits.LATD4 = 1;
    LATDbits.LATD5 = 0;
    LATDbits.LATD6 = 0;
    LATDbits.LATD7 = 0;
}

void HVon()
{
    //HV is on
    LATDbits.LATD4 = 0;
    LATDbits.LATD5 = 0;
    LATDbits.LATD6 = 1;
    LATDbits.LATD7 = 0;
}
```

Listing J.14: Microcontroller header code (IO module)

```
/*
 * File:   dsPIC33FJ64GS606IO.h
 * Author: Yiou He
 * Comments: header file of dsPIC33FJ64GS606 IO file
 * Revision history: v1
 */

// This is a guard condition so that contents of this file are not included
// more than once.
#ifndef XC_HEADER_IO_H
#define XC_HEADER_IO_H

#include <xc.h> // include processor files - each processor file is guarded.
#include "p33FJ64GS606.h"
#include "stdio.h"
#include "string.h"

void initIO();
void DischargeCaps();     //Start to discharge the input caps
void Precharge();          //Precharge the input caps
void NormalOperation();  //Connect 200V to the switches
void HVon(); //HV on, LED light on.
#endif  /* XC_HEADER_IO_H */
```

Listing J.15: Microcontroller c code (PWM module)

```
/*
 * File:   dsPIC33FJ64GS606PWM.c
 * Author: Yiou
 *
 * Created on July 7, 2016, 9:48 AM
 */


#include "dsPIC33FJ64GS606PWM.h"

void initPWM(int period, int duty, int deadtime)
{
```

```
13      PTCON = 0;      //Disable PWM module
14      PTCON2 = 0;     //Set the PWM resolution to max 1.04 ns
15      PTPER = period;  //Set the primary time base (PWM period) to 500 kHz,
            1/500000/1.04ns)
16      MDC = duty;      //Set the PWM duty cycle to 50%
17      //Initiate PWM1
18      PWMCON1 = 0x0000; //Individual PDC control duty cycle, positive dead time
19      PDC1 = duty;        //Set the secondary PWM duty cycle
20      PHASE1 = 0;
21      DTR1 = deadtime;          //PWMH deadtime is DTR1*1.04 ns
22      ALTDTR1 = deadtime;       //PWML deadtime is ALTDTR1*1.04 ns
23      IOCON1 = 0x0341;         //Override PWM, not controlled by PWM module
24      //Initiate PWM2
25      PWMCON2 = 0x0000;       //Individual PDC control duty cycle
26      PDC2 = period;
27      PHASE2 = 0;
28      DTR2 = deadtime;        //PWMH deadtime is DTR2*1.04 ns
29      ALTDTR2 = deadtime;     //PWML deadtime is ALTDTR2*1.04 ns
30      IOCON2 = 0x0341;        //Override PWM, not controlled by PWM module
31      /*
32        ;GPIO module controls PWMxH pin
33      ;GPIO module controls PWMxL pin
34      ;complementary PWM output mode
35      ;overide enable for PWMxH
36      ;overide enable for PWMxL
37        ;override date 01
38      ;overide syncronized to PWM time base
39        */
40  }
41  void EnablePWM()
42  {
43      /*
44      TRISEbits.TRISE1 = 1; // Configure PWM1H/RE1 as digital input
45      TRISEbits.TRISE0 = 1; // Configure PWM1L/RE0 as digital input
46      TRISEbits.TRISE3 = 1; // Configure PWM2H/RE3 as digital input
47      TRISEbits.TRISE2 = 1; // Configure PWM2L/RE2 as digital input
48      // Ensure output is in safe state using pull-up or pull-down resistors
49      // Did not add pull-down resistors in the version, seems fine?
50
51      IOCON1bits.PENH = 0; // Assign pin ownership of PWM1H/RE1 to GPIO module
52      IOCON1bits.PENL = 0; // Assign pin ownership of PWM1L/RE0 to GPIO module
53      IOCON1bits.OVRDAT = 1; // Configure override state of the PWM outputs to
54      IOCON2bits.PENH = 0; // Assign pin ownership of PWM1H/RE1 to GPIO module
55      IOCON2bits.PENL = 0; // Assign pin ownership of PWM1L/RE0 to GPIO module
56      IOCON2bits.OVRDAT = 1; // Configure override state of the PWM outputs to
57      // desired safe state.
58      IOCON1bits.OVRENH = 1; // Override PWM1H output
59      IOCON1bits.OVRENL = 1; // Override PWM1L output
60      IOCON2bits.OVRENH = 1; // Override PWM1H output
61      IOCON2bits.OVRENL = 1; // Override PWM1L output
62      PTCONbits.PTEN = 1; // Enable PWM module
63      */
64
65      //Remove override
66      IOCON1bits.OVRENH = 0; // Remove override for PWM1H output
67      IOCON1bits.OVRENL = 0; // Remove override for PWM1L output
68      IOCON2bits.OVRENH = 0; // Remove override for PWM1H output
69      IOCON2bits.OVRENL = 0; // Remove override for PWM1L output
70
71      //delay(100); //for(int i = 0;i<= 10; i++); // Introduce a delay greater than one
            full PWM cycle
72      IOCON1bits.PENH = 1; // Assign pin ownership of PWM1H/RE1 to PWM module
73      IOCON1bits.PENL = 1; // Assign pin ownership of PWM1L/RE0 to PWM module
74      IOCON2bits.PENH = 1; // Assign pin ownership of PWM1H/RE3 to PWM module
75      IOCON2bits.PENL = 1; // Assign pin ownership of PWM1L/RE2 to PWM module
76
77  }
78
```

```
79  void DisablePWM()
80  {
81      //Disable PWM
82      PTCONbits.PTEN = 0;
83      // Have to add the similar procedure to make sure the switches are turned off to
            the correct states.
84      TRISEbits.TRISE1 = 0; // Configure PWM1H/RE1 as digital output
85      TRISEbits.TRISE0 = 0; // Configure PWM1L/RE0 as digital output
86      TRISEbits.TRISE3 = 0; // Configure PWM2H/RE3 as digital output
87      TRISEbits.TRISE2 = 0; // Configure PWM2L/RE2 as digital output
88
89      LATEbits.LATE1 = 0; //PWM1H = 0
90      LATEbits.LATE0 = 1; //PWM1L = 1
91      LATEbits.LATE3 = 1; //PWM2H = 0
92      LATEbits.LATE2 = 0; //PWM2L = 1
93      /*
94      TRISEbits.TRISE1 = 0; // Configure PWM1H/RE1 as digital input
95      TRISEbits.TRISE0 = 0; // Configure PWM1L/RE0 as digital input
96      TRISEbits.TRISE3 = 0; // Configure PWM2H/RE3 as digital input
97      TRISEbits.TRISE2 = 0; // Configure PWM2L/RE2 as digital input
98      // Ensure output is in safe state using pull-up or pull-down resistors
99      // Did not add pull-down resistors in the version, seems fine?
100
101     IOCON1bits.PENH = 0; // Assign pin ownership of PWM1H/RE1 to GPIO module
102     IOCON1bits.PENL = 0; // Assign pin ownership of PWM1L/RE0 to GPIO module
103     IOCON1bits.OVRDAT = 1; // Configure override state of the PWM outputs to
104     IOCON2bits.PENH = 0; // Assign pin ownership of PWM2H/RE1 to GPIO module
105     IOCON2bits.PENL = 0; // Assign pin ownership of PWM2L/RE0 to GPIO module
106     IOCON2bits.OVRDAT = 2; // Configure override state of the PWM outputs to
107
108     PTCONbits.PTEN = 0; // Disable PWM module
109     */
110 }
111
112 /*void PrechargePWM()
113 {
114     TRISEbits.TRISE1 = 0; // Configure PWM1H/RE1 as digital input
115     TRISEbits.TRISE0 = 0; // Configure PWM1L/RE0 as digital input
116     TRISEbits.TRISE3 = 0; // Configure PWM2H/RE3 as digital input
117     TRISEbits.TRISE2 = 0; // Configure PWM2L/RE2 as digital input
118
119     //Control PWM output with GPIO
120     LATEbits.LATE1 = 0; //PWM1H = 0
121     LATEbits.LATE0 = 1; //PWM1L = 1
122     LATEbits.LATE3 = 1; //PWM2H = 0
123     LATEbits.LATE2 = 0; //PWM2L = 1
124 }*/
125
126 void PreparePWM()
127 {
128     TRISEbits.TRISE1 = 0; // Configure PWM1H/RE1 as digital input
129     TRISEbits.TRISE0 = 0; // Configure PWM1L/RE0 as digital input
130     TRISEbits.TRISE3 = 0; // Configure PWM2H/RE3 as digital input
131     TRISEbits.TRISE2 = 0; // Configure PWM2L/RE2 as digital input
132     // Ensure output is in safe state using pull-up or pull-down resistors
133     // Did not add pull-down resistors in the version, seems fine?
134
135     IOCON1bits.PENH = 0; // Assign pin ownership of PWM1H/RE1 to GPIO module
136     IOCON1bits.PENL = 0; // Assign pin ownership of PWM1L/RE0 to GPIO module
137     IOCON1bits.OVRDAT = 1; // Configure override state of the PWM outputs to
138     IOCON2bits.PENH = 0; // Assign pin ownership of PWM2H/RE1 to GPIO module
139     IOCON2bits.PENL = 0; // Assign pin ownership of PWM2L/RE0 to GPIO module
140     IOCON2bits.OVRDAT = 2; // Configure override state of the PWM outputs to
141     // desired safe state.
142     IOCON1bits.OVRENH = 1; // Override PWM1H output
143     IOCON1bits.OVRENL = 1; // Override PWM1L output
144     IOCON2bits.OVRENH = 1; // Override PWM1H output
145     IOCON2bits.OVRENL = 1; // Override PWM1L output
```

```
146
147     PTCONbits.PTEN = 1; // Enable PWM module
148 }
149
150 void ChangePD(int period, int duty, int deadtime)
151 {
152     PTPER = period;  //Set the primary time base
153     MDC = duty;      //Set the PWM duty cycle to 50%
154     PDC1 = duty;       //Set the secondary PWM duty cycle
155     PDC2 = duty;       //Set the secondary PWM duty cycle
156
157     DTR1 = deadtime;         //PWMH deadtime is DTR1*1.04 ns
158     ALTDTR1 = deadtime;      //PWML deadtime is ALTDTR1*1.04 ns
159     DTR2 = deadtime;       //PWMH deadtime is DTR2*1.04 ns
160     ALTDTR2 = deadtime;    //PWML deadtime is ALTDTR2*1.04 ns
161 }
162 //
163 void initChangePD(int period, int duty, int deadtime)
164 {
165     PTPER = period;  //Set the primary time base
166     MDC = duty;      //Set the PWM duty cycle to 50%
167     PDC1 = duty;       //Set the secondary PWM duty cycle
168     PDC2 = period;       //Set the secondary PWM duty cycle
169
170     DTR1 = deadtime;         //PWMH deadtime is DTR1*1.04 ns
171     ALTDTR1 = deadtime;      //PWML deadtime is ALTDTR1*1.04 ns
172     DTR2 = deadtime;       //PWMH deadtime is DTR2*1.04 ns
173     ALTDTR2 = deadtime;    //PWML deadtime is ALTDTR2*1.04 ns
174 }
```

Listing J.16: Microcontroller header code (ADC module)

```
1  /*
2   * File:   dsPIC33FJ64GS606PWM.h
3   * Author: Yiou He
4   * Comments: header file of dsPIC33FJ64GS606 PWM unit
5   * Revision history: v1
6   */
7
8  // This is a guard condition so that contents of this file are not included
9  // more than once.
10 #ifndef XC_HEADER_PWM_H
11 #define XC_HEADER_PWM_H
12
13 #include <xc.h> // include processor files - each processor file is guarded.
14 #include "p33FJ64GS606.h"
15 #include "stdio.h"
16 #include "string.h"
17 #include "math.h"
18 #include "main_PWMoutputDefinitions.h"
19
20 void initPWM(int period, int duty, int deadtime);
21 void EnablePWM();     //Start PWM in complement mode
22 void DisablePWM();     //Disable PWM
23 //void PrechargePWM();  //Precharge the high side 5V
24 void PreparePWM();  //Assign pin ownership to IO pins, precharge the highside 5V
25 void ChangePD(int period, int duty, int deadtime);   //Change period, duty, deadtime
26 void initChangePD(int period, int duty, int deadtime);
27
28 #endif  /* XC_HEADER_PWM_H */
```

Listing J.17: Microcontroller c code (SPI module)

```
1  /*
2   * File:   dsPIC33FJ64GS606SPI.c
```

```
 * Author: Yiou
 *
 * Created on July 7, 2016, 9:44 AM
 */

#include "dsPIC33FJ64GS606SPI.h"

//init SPI 2 Module for external nonvolatile RAM
void initSPI2()
{
    IFS2bits.SPI2IF = 0; // Clear the Interrupt flag
    IEC2bits.SPI2IE = 0; // Disable the interrupt

    SPI2STAT = 0; //Clear status register
    SPI2CON1 = 0; //Clear control register 1
    SPI2CON2 = 0; //Clear control register 2

    // SPI2CON1 Register Settings
    SPI2CON1bits.DISSCK = 0; // Internal serial clock is enabled
    SPI2CON1bits.DISSDO = 0; // SDOx pin is controlled by the module
    SPI2CON1bits.MODE16 = 0; // Communication is byte-wide (8 bits)
    SPI2CON1bits.MSTEN = 1; // Master mode enabled
    SPI2CON2bits.FRMEN = 0; //Frame mode
    SPI2CON2bits.FRMPOL = 0;
    SPI2CON1bits.SMP = 0; // Input data is sampled at the middle of data output time
    SPI2CON1bits.CKE = 1; // Serial output data changes on transition from
    SPI2CON1bits.PPRE = 3; //Postscale clock to 1:1
    SPI2CON1bits.SPRE = 5;  //Prescale clock to 1:1
    // Idle clock state to active clock state
    SPI2CON1bits.CKP = 0; // Idle state for clock is a low level;

    // Interrupt Controller Settings
    //C1FEN1bits.FLTEN11 = 0;
    IFS2bits.SPI2IF = 0;  // Clear the Interrupt flag
    IEC2bits.SPI2IE = 0;  // Disable the interrupt
}

void EnableSPI2()
{
    SPI2STATbits.SPIEN = 1;
}

void DisableSPI2()
{
    SPI2STATbits.SPIEN = 0;
}

//send one byte of data and receive one back at the same time
 void writeSPI2(unsigned int in)
 {
    int i = 0;
    SPI2STATbits.SPIROV = 0;
    SPI2BUF = in;          // write to buffer for TX
    while(SPI2STATbits.SPITBF); // wait for transfer to complete
    //in = SPI2BUF;            // avoid overflow when reading
    for (i = 0; i<= 1;i++);
 } // writeSPI

 void write_enable(void)
 {
     RAM_enable();
     writeSPI2(WR_ENABLE);
     RAM_disable();
 }

 void write_disable(void)
 {
    RAM_enable();
```

```
71      writeSPI2(WR_DISABLE);
72      RAM_disable();
73  }
74
75  void writeByte(unsigned int in,int long loc)
76  {
77      RAM_enable();
78      writeSPI2(WR_ENABLE);
79      RAM_disable();  //      write_enable();
80      RAM_enable();
81      writeSPI2(WRITE);
82      writeSPI2(loc >> 16);
83      writeSPI2(loc >> 8);
84      writeSPI2(loc);
85      writeSPI2(in);
86      RAM_disable();
87  }
88
89  unsigned int readByte(int long loc)
90  {
91      int i = 0;
92      unsigned int r;
93      RAM_enable();
94      writeSPI2(READ);
95      writeSPI2(loc >> 16);
96      writeSPI2(loc >> 8);
97      writeSPI2(loc);
98      r = readSPI2();
99      for (i = 0; i<= 1;i++);
100     RAM_disable();
101     return r;
102 }
103
104   unsigned int readSPI2()
105 {
106     //int i = 0;
107     unsigned int out = -1;
108     SPI2STATbits.SPIROV = 0;
109     SPI2BUF = 0x13;                    // initiate bus cycle
110     while(!SPI2STATbits.SPIRBF);
111     /*Check for Receive buffer full status bit of status register*/
112     if (SPI2STATbits.SPIRBF)
113     {
114         //SPI2STATbits.SPIROV = 0;
115         //for (i = 0; i<= 0;i++);
116         out = SPI2BUF;     /* return byte read */
117     }
118
119     return out;                        /* RBF bit is not set return error*/
120 }
121
122 int long ReadID()
123 {
124     int long r = 0;
125     RAM_enable();
126     writeSPI2(RDID);
127     r = readSPI2();
128     RAM_disable();
129     return r;
130 }
131
132 int long SendThroughSPI(int Recorder, double InputVoltage,double InputCurrent,double
        OutputVoltage,double Temperature,int long loc)
133 {
134     writeByte(Recorder,loc);
135     loc++;
136     writeByte(((unsigned int)InputVoltage) >> 2,loc);  //200 V corresponds to 626
137     loc++;
```

```
    writeByte(((unsigned int)InputCurrent) >> 2,loc);
    loc++;
    writeByte(((unsigned int)OutputVoltage) >> 2,loc); //40 kV corresponds to 682
    loc++;
    writeByte(((unsigned int)Temperature) >> 1,loc); //usually around 300, maximum
        with hot water is 375
    loc++;
    if (loc >= MaxLoc) loc = MaxLoc;
    return loc;
}
```

Listing J.18: Microcontroller header code (SPI module)

```
/*
 * File:   dsPIC33FJ64GS606SPI.h
 * Author: Yiou He
 * Comments: header file of dsPIC33FJ64GS606 SPI unit
 * Revision history: v1
 */

// This is a guard condition so that contents of this file are not included
// more than once.
#ifndef XC_HEADER_SPI_H
#define XC_HEADER_SPI_H

#include <xc.h> // include processor files - each processor file is guarded.
#include "p33FJ64GS606.h"
#include "stdio.h"
#include "string.h"
#include "main_PWMoutputDefinitions.h"

#define WR_ENABLE 6
#define WR_DISABLE 4
#define RD_STATUS 5
#define WR_STATUS 1
#define READ 3
#define WRITE 2
#define RDID 0x9F
#define RAMCS LATGbits.LATG9
#define RAM_enable() RAMCS = 0
#define RAM_disable() RAMCS = 1;

void initSPI2();
void EnableSPI2();
void DisableSPI2();
void writeSPI2 (unsigned int in);
unsigned int readSPI2();
void write_enable(void);
void write_disable(void);
void writeByte(unsigned int in,int long loc);
unsigned int readByte(int long loc);
int long ReadID();
int long SendThroughSPI(int Recorder,double InputVoltage,double InputCurrent,double
    OutputVoltage,double Temperature,int long loc);

#endif  /* XC_HEADER_SPI_H */
```

Listing J.19: Microcontroller c code (Timer module)

```
/*
 * File:   dsPIC33FJ64GS606TIMER.c
 * Author: Yiou
 *
 * Created on July 7, 2016, 9:55 AM
 */
```

```
7
8  #include "dsPIC33FJ64GS606TIMER.h"
9
10 void initTimer1(int ADCperiod) //working, tested on 7/5/2016
11 {
12     //Scale Timer 1
13     //If Fcy = 29.49 MHz, divided by 64, Timer is clocked by 460.78 kHz. Then 1ms is
           460;
14     T1CONbits.TCKPS = 2;
15     PR1 = ADCperiod;
16 }
17
18 void EnableTimer1()
19 {
20     T1CONbits.TON = 1;
21 }
22
23 void initTimer2()
24 {
25     //Scale Timer 2
26     //If Fcy = 29.49 MHz, divided by 64, Timer is clocked by 460k kHz. Then 1ms is
           460;
27     T2CONbits.TCKPS = 2;
28     PR2 = IC1timer2Period; //~3 ms
29 }
30
31 void EnableTimer2()
32 {
33     T2CONbits.TON = 1;
34 }
35
36 void initIC1()
37 {
38     IC1CONbits.ICTMR = 1; //select Timer 2 as the source
39     IC1CONbits.ICI = 1;   //Interrupt generate every second event (second rising edge
           )
40     IC1CONbits.ICM = 1;   //Mode is to detect every rising and falling edge.
41
42     // Enable Capture Interrupt And Timer2
43     IPC0bits.IC1IP = 1; // Setup IC1 interrupt priority level
44     IFS0bits.IC1IF = 0; // Clear IC1 Interrupt Status Flag
45     IEC0bits.IC1IE = 1; // Enable IC1 interrupt
46 }
47
48 void initTimer45(int EndTimeMSB,int EndTimeLSB) //working, tested on 7/5/2016
49 {
50     //If Fcy = 29.49 MHz, divided by 256, Timer is clocked by 115.195 kHz. Then 1ms
           is 115.195, 230.3906;
51     T4CONbits.T32 = 1;
52     T4CONbits.TCKPS = 3;
53     T5CONbits.TCKPS = 3;
54     TMR4 = 0;
55     TMR5 = 0;
56     PR4 = EndTimeLSB;
57     PR5 = EndTimeMSB;
58
59     //Set up interrupt
60     IFS1bits.T4IF = 0;
61     IFS1bits.T5IF = 0;
62     IEC1bits.T4IE = 0;  //should not set to 1
63     IEC1bits.T5IE = 1;
64 }
65
66 void EnableTimer45()
67 {
68     T4CONbits.TON = 1;
69     T5CONbits.TON = 1;
70 }
```

```
71
72 void DisableTimer45()
73 {
74     T4CONbits.TON = 0;
75     T5CONbits.TON = 0;
76     TMR4 = 0;
77     TMR5 = 0;
78 }
```

Listing J.20: Microcontroller header code (Timer module)

```
1  /*
2   * File:   dsPIC33FJ64GS606TIMER.h
3   * Author: Yiou He
4   * Comments: header file of the dsPIC33FJ64GS606 TIMER unit
5   * Revision history: v1
6   */
7
8  // This is a guard condition so that contents of this file are not included
9  // more than once.
10 #ifndef XC_HEADER_TIMER_H
11 #define XC_HEADER_TIMER_H
12
13 #include <xc.h> // include processor files - each processor file is guarded.
14 #include "p33FJ64GS606.h"
15 #include "stdio.h"
16 #include "string.h"
17 #include "main_PWMoutputDefinitions.h"
18
19 void initTimer1(int ADCperiod);
20 void EnableTimer1();
21 void initTimer2();
22 void EnableTimer2();
23 void initTimer45(int EndTimeMSB,int EndTimeLSB);
24 void EnableTimer45();
25 void DisableTimer45();
26 void initIC1();
27
28 #endif  /* XC_HEADER_TIMER_H */
```

Listing J.21: Microcontroller c code (UART module)

```
1  /*
2   * File:   dsPIC33FJ64GS606UART.c
3   * Author: Yiou
4   *
5   * Created on July 7, 2016, 9:34 AM
6   */
7
8  #include "dsPIC33FJ64GS606UART.h"
9
10 void initUART1()
11 {
12     U1MODEbits.STSEL = 0; // 1 Stop bit
13     U1MODEbits.PDSEL = 0; // No Parity, 8 data bits
14     U1MODEbits.ABAUD = 0; // Auto-Baud Disabled
15     U1MODEbits.BRGH = 0; // Low Speed mode
16
17     U1BRG = 1;
18     /*
19      *  ;29.49 MHz Fcy (64/16 x PLL with 7.37MHz FRC)
20     ;191 = 9600 (+0.00%)
21     ;95 = 19200 (+0.00%)
22     ;47 = 38400 (+0.00%)
23     ;31 = 56000 (+0.00%)
```

```
24      ;15 = 115200 (+0.00%)
25      ;7 = 230400 (+0.00)
26      ;3 = 460800 (+0.00%)
27      ;1 = 921600 (+0.00%)
28      */
29      /*
30       *  ;58.98 MHz Fcy (64/8 x PLL with 7.37MHz FRC
31      ;191 = 19200 (+0.00%)
32      ;95 = 38400 (+0.00%)
33      ;47 = 56000 (+0.00%)
34      ;31 = 115200 (+0.00%)
35      ;15 = 230400 (+0.00)
36      ;7 = 460800 (+0.00%)
37      ;3 = 921600 (+0.00%)
38      */
39      U1STA = 0; //init status and control register, interrupt after one TX Character
            is transmitted
40      U1TXREG = 0x0000;
41      //Bit 15-9: Unimplemented (0000000)
42      //Bit 8: Data bit 8 in 9-bit mode (0)
43      //Bit 7-0: Data bits 7-0 (00000000)
44
45      //Set interrupt
46      IFS0bits.U1RXIF = 0;
47      IFS0bits.U1TXIF = 0;
48      IEC0bits.U1RXIE = 1;
49      IEC0bits.U1TXIE = 1;
50      //IPC2bits.U1RXIP = 0b111;
51  }
52  void EnableUART1()
53  {
54      U1MODEbits.UARTEN = 1; //Enable UART
55      Nop();
56      U1STAbits.UTXEN = 1;    //Enable UART transmit
57      Nop();
58  }
59
60  void DisableUART1()
61  {
62      U1MODEbits.UARTEN = 0; //Enable UART
63      Nop();
64      U1STAbits.UTXEN = 0;    //Enable UART transmit
65      Nop();
66  }
67
68  //UART2 for the bluetooth
69  void initUART2()
70  {
71      U2MODEbits.STSEL = 0; // 1 Stop bit
72      U2MODEbits.PDSEL = 0; // No Parity, 8 data bits
73      U2MODEbits.ABAUD = 0; // Auto-Baud Disabled
74      U2MODEbits.BRGH = 0; // Low Speed mode
75
76      U2BRG = 15;
77      /*
78       *  ;29.49 MHz Fcy (64/16 x PLL with 7.37MHz FRC)
79      ;191 = 9600 (+0.00%)
80      ;95 = 19200 (+0.00%)
81      ;47 = 38400 (+0.00%)
82      ;31 = 56000 (+0.00%)
83      ;15 = 115200 (+0.00%)
84      ;7 = 230400 (+0.00)
85      ;3 = 460800 (+0.00%)
86      ;1 = 921600 (+0.00%)
87      */
88
89      U2STA = 0; //init status and control register, interrupt after one TX Character
            is transmitted
```

```
90      U2TXREG = 0x0000;
91      //Bit 15-9: Unimplemented (0000000)
92      //Bit 8: Data bit 8 in 9-bit mode (0)
93      //Bit 7-0: Data bits 7-0 (00000000)
94
95      //Set interrupt
96      IFS1bits.U2RXIF = 0;
97      IFS1bits.U2TXIF = 0;
98      IEC1bits.U2RXIE = 0;
99      IEC1bits.U2TXIE = 1;
100     //IPC2bits.U1RXIP = 0b111;
101 }
102
103 void EnableUART2()
104 {
105     U2MODEbits.UARTEN = 1; //Enable UART
106     Nop();
107     U2STAbits.UTXEN = 1;    //Enable UART transmit
108     Nop();
109     LATBbits.LATB8 = 1;     //Set DSR pin high
110 }
111 void WriteScreen(char s[50])
112 {
113     char *p;
114     p = s;
115     while (*p)
116     {
117         while (!(U1STAbits.TRMT)) {}
118         U1TXREG = *(p++);
119     }
120 }
121 void WriteBluetooth(char s[50])
122 {
123     char *p;
124     p = s;
125     while (*p)
126     {
127         while (!(U1STAbits.TRMT)) {}
128         U2TXREG = *(p++);
129     }
130 }
131
132 void WriteScreenADCdata(int FlagE, double InputVoltage,double InputCurrent,double
        OutputVoltage,double Temperature,double LogicBV,double AccX,double AccY,double
        AccZ)
133 {
134     char buf[3];
135     sprintf(buf,"%d",FlagE);
136     WriteScreen(buf);
137     WriteScreen("\r\n");
138     sprintf(buf,"%.2f",InputVoltage); //*InputVScale + InputVOffset
139     WriteScreen(buf);
140     WriteScreen("\r\n");
141     sprintf(buf,"%.2f",InputCurrent); //*InputIScale + InputIOffset
142     WriteScreen(buf);
143     WriteScreen("\r\n");
144     sprintf(buf,"%.2f",OutputVoltage); //*OutputVScale + OutputVOffset
145     WriteScreen(buf);
146     WriteScreen("\r\n");
147     sprintf(buf,"%.2f",LogicBV);//LogicBV*LogicBVScale + LogicBVOffset);
148     WriteScreen(buf);
149     WriteScreen("\r\n");
150     sprintf(buf,"%.2f",Temperature);//LogicBV*LogicBVScale + LogicBVOffset);
151     WriteScreen(buf);
152     WriteScreen("\r\n");
153 }
```

Listing J.22: Microcontroller header code (UART module)

```
/*
 * File: dsPIC33FJ64GS606UART.h
 * Author: Yiou He
 * Comments: header file for the UART function
 * Revision history: v1
 */

// This is a guard condition so that contents of this file are not included
#ifndef XC_HEADER_UART_H
#define XC_HEADER_UART_H

#include <xc.h> // include processor files - each processor file is guarded.
#include "p33FJ64GS606.h"
#include "stdio.h"
#include "string.h"
#include "main_PWMoutputDefinitions.h"

void initUART1();
void initUART2();
void EnableUART1();   //StartUART1
void EnableUART2();    //StartUART2
void DisableUART1();
void WriteScreen(char s[50]); //Write texts on the screen
void WriteBluetooth(char s[50]); //Write texts to the bluetooth
void WriteScreenADCdata(int,double,double,double,double,double,double,double,double);

#endif  /* XC_HEADER_UART_H */
```

J.2 HVAC

J.2.1 Non-resonant topologies

Listing J.23: Shell code to simulate the weight of the example converter in Fig. 5-7

```
clc,clear all

global Requirement Design raw1 raw2 raw3 raw4 raw5 raw

Date = 'xxx';
Vin_range = 100;
% Peak amplitude of the secondary voltage that one hope to achieve (V)
Vo_range = 1000:1000:10000;
% Output power desired (W)
Po_range = 200;
% Winding Pattern Index: 1 inidcates center leg winding, 2 indicates double
Winding_Pattern = 1;
% Hypothesis: record why you want to run the sim
Hypothesis = ['xxx'];
% Notes: record any changes you made to the code
Notes = 'xxx';

filename = strcat(Date,'_','xxx.xlsx');
SheetNumber = 1;
Infosheetname = strcat('SimInfo',num2str(SheetNumber));
ResultDatasheetname = strcat('ResultsData',num2str(SheetNumber));
FBinvertersheetname = strcat('FBData',num2str(SheetNumber));
% RunNumber always starts with 1
RunNumber = 1;
```

```
25
26 % Read the core loss xlsx
27 corelossfile = 'CoreLossData.xlsx';
28 [num,txt,raw1] = xlsread(corelossfile,'Freq');
29 [num,txt,raw2] = xlsread(corelossfile,'Bfield');
30 [num,txt,raw3] = xlsread(corelossfile,'Ploss');
31 [num,txt,raw4] = xlsread(corelossfile,'BSAT');
32 [num,txt,raw5] = xlsread(corelossfile,'MU');
33
34 % Read the core size xlsx
35 coresizefile = 'CoreSizeData.xlsx';
36 [num,txt,raw] = xlsread(coresizefile,'Ecore');
37
38 % Read the FET and CAP xlsx
39 FETCapfile = 'MOSFETs and Capacitor Masses.xlsx';
40 FETsheetname = 'Component Masses_FETs';
41 CAPsheetname = 'Component Masses_Capacitors';
42
43 [num,txt,rawFET] = xlsread(FETCapfile,FETsheetname);
44 [m1,n1] = size(rawFET);
45 ColumnName = rawFET(1,:);
46 Vsw_term = 'voltage rating'; %V
47 Isw_term = 'current rating'; %A
48 Wsw_term = 'avg. mass (g)'; %W
49 Asw_term = 'Area'; %mm2
50 Wsw = cell2mat(rawFET(2:end,find(ismember(ColumnName, Wsw_term))));
51 Isw = cell2mat(rawFET(2:end,find(ismember(ColumnName, Isw_term))));
52 Vsw = cell2mat(rawFET(2:end,find(ismember(ColumnName, Vsw_term))));
53 Asw = cell2mat(rawFET(2:end,find(ismember(ColumnName, Asw_term))));
54
55 [num,txt,rawCAP] = xlsread(FETCapfile,CAPsheetname);
56 [m1,n1] = size(rawCAP);
57 ColumnName = rawCAP(1,:);
58 VCAP_term = 'Voltage (kV)'; %kV
59 CAP_term = 'Capacitance (uF)'; %uF
60 WCAP_term = 'avg. mass'; %g
61 ACAP_term = 'Area'; %mm2
62 WCAP = cell2mat(rawCAP(2:end,find(ismember(ColumnName, WCAP_term))));
63 CAP = cell2mat(rawCAP(2:end,find(ismember(ColumnName, CAP_term))));
64 VCAP = cell2mat(rawCAP(2:end,find(ismember(ColumnName, VCAP_term))))*1000;
65 ACAP = cell2mat(rawCAP(2:end,find(ismember(ColumnName, Asw_term))));
66
67 PCBdensity = 0.0033; %g/mmm
68 TotalCap = 1; %uF
69
70 tic
71 for i = 1:1:length(Vo_range)
72     for Va = linspace(2*Vin_range,Vo_range(i),10)
73         NumberOfStage = Vo_range(i)/Va;
74         G = Va/Vin_range;
75         Pa = Po_range/NumberOfStage;
76
77         %Run the Ecore Design
78         Suceed = Ecore_actualcore_E_Vectorize_Function_RTC(Date, RunNumber,
               Hypothesis, Notes,...
79             Vin_range, G, Pa, Va, Winding_Pattern);
80         if (Suceed == 1)
81             NumberOfCopies(i) = NumberOfStage;
82
83             % Run FB inverter selection
84             VswIndex = find(Vsw >= 2*Va);
85             SWparallel = floor(4.*Pa/Va./Isw(VswIndex))+1;
86             SwitchWeight = 4*Wsw(VswIndex).*SWparallel;
87             [MinSwitchWeight(i),mi] = min(SwitchWeight);
88             SWarea(i) = 4*Asw(VswIndex(mi))*SWparallel(mi);
89             % Select Capacitors
90             CAPseries = floor(2.*Va./VCAP) + 1;
91             CAPparallel = floor(TotalCap./(CAP./CAPseries)) + 1;
```

```
92                CAPWeight = WCAP.*CAPseries.*CAPparallel;
93                [MinCapWeight(i),mi] = min(CAPWeight);
94                CAParea(i) = ACAP(mi).*CAPseries(mi).*CAPparallel(mi)/2; %assume each cap
                      space has 2 soldered on.
95                % PCB weight
96                PCBWeight(i) = 2*(SWarea(i) + CAParea(i))*PCBdensity;
97                FBinverterWeight(i) = MinSwitchWeight(i) + MinCapWeight(i) + PCBWeight(i)
                      ;
98
99                FBdata = [NumberOfCopies(i),MinSwitchWeight(i),MinCapWeight(i),PCBWeight(
                      i),FBinverterWeight(i),FBinverterWeight(i)*NumberOfCopies(i)];
100
101               % Save Inductor Results
102               Design_excel = squeeze(struct2cell(Design));
103               [row,col] = size(Design_excel(2,:));
104               Design_num = cell2mat(Design_excel(2,:));
105               if (length(Design_excel(1,:)) >= 26)
106                   CharName = strcat('A',char(64+length(Design_excel(1,:))-26));
107                   if (length(Design_excel(1,:)) >= 52)
108                       disp('Too Many Variables');
109                   end
110               else
111                   CharName = char(64+length(Design_excel(1,:))-26);
112               end
113               xlswrite(filename,Design_num,ResultDatasheetname,strcat('A',num2str(5*
                      RunNumber -3),':',CharName,num2str(5*RunNumber + 1)));
114               % Save FB results
115               xlswrite(filename,[FBdata;FBdata;FBdata;FBdata;FBdata],
                      FBinvertersheetname,strcat('A',num2str(5*RunNumber -3),':','F',
                      num2str(5*RunNumber + 1)));
116               RunNumber = RunNumber + 1;
117           end
118       end
119   end
120   %%
121   % Save Requirements
122   Requirement_excel = squeeze(struct2cell(Requirement))';
123   xlswrite(filename,Requirement_excel,Infosheetname);
124   % Format Excel for easy to read
125   xlswrite(filename,Design_excel(1,:),ResultDatasheetname);
126   exl = actxserver('excel.application');
127
128   savefile = 'xxx';
129   exlWkbk = exl.Workbooks.Open(strcat(savefile,filename));
130   Worksheet = exlWkbk.Sheets.Item(3);
131   Worksheet.Rows.Item(1).RowHeight = 60;
132   cells = Worksheet.Range(strcat('A1:',CharName,'1'));
133   cells.ColumnWidth = 6;
134   set(cells.Font, 'Bold', true);
135   exlWkbk.Save
136   exlWkbk.Close
137   exl.Quit
138   toc
```

Listing J.24: Code to simulate the weight of the inductor in a resonant-transition boost converter (called in List J.23)

```
1  function y = Ecore_actualcore_E_Vectorize_Function_RTC(Date, RunNumber, Hypothesis,
       Notes,...
2      Vin_range, G_range, Po_range, Vinsulation_max_range, Winding_Pattern)
3
4  CodeName = 'Ecore_actualcore_E_Vectorize_Function_RTC.m';
5
6  % Lowest allowed transformer efficiency
7  etaInductor = 0.95;
```

```
% Max allowable temperature (C)
Tmax = 90;
% Min allowable temperature (C)
Tmin = 25;
% Max allowable current density in the wire (A/m^2)
Jwmax = 500*100*100;
% Minimal litz diameter one can get (m)
MinLitzDia = 0.05024/1000; %AWG44, 0.0316 is AWG48, %0.03983 is AWG46
% Dielectric strength of the insulation material (V/m), discount 50%
dielectricstrength_insulation = 0.5*200*1000*100; %TEFLON
% minimal air gap (m)
mingap = 100e-6;

MinWinding = 1;
% Maximum turns
MaxWinding = 50;
% Incremental winding
IncreN = 1;
% Maximum layer of winding
MaxMl = 10;
% Incremental layers
IncreMl = 1;
% Minimal wire diameter (m)
MinWireSize = 0.079/1000; %AWG28, 0.35 mm is AWG29, 0.079 is AWG40
% Maximum allowable weight (g)
MaxWeight = 1000;
% g/m3, density of the core
CoreDensity = 4.8*1000*1000;
% g/m3, density of copper
CopperDensity = 8.96*1000*1000;
% g/m3, density of core insulation materials
CoreInsulationDensity = 2.2*1000*1000; %TEFLON
% g/m3, density of wire insulation materials
WireInsulationDensity = 2.2*1000*1000; %TEFLON

% all discount factors
% Bmax discount factor
BSAT_discount = 0.75;
% Actual core loss is always higher than the calculated.
CoreLossMultiple = 1;
% Maximum packing factor (copper area compared with total window area)
maxpackingfactor = 0.7;
% Minimum packing factor
minpackingfactor = 0.01;
% Winding factor of litz wire, assuming only 80% of wire size is copper
LitzFactor = 0.8;
% Weight of bobbin as a faction of the core insulation
BobbinWeightFactor = 0.5;
%--------------------------------------------------------------------------
% The variables and constants in this section are predefined. Recommend
% users not change them unless necessary

% Simulation output variable section:
% Requirement file output
field1 = 'name';
value1_req = {'Date','RunNumber','Hypothesis','Notes','CodeName',...
    'Vin_range(V)','G_range(V)','Po_range(W)',...
    'Vinsulation_max_range(V)','etaInductor','Tmin(C)','Tmax(C)','Jwmax(A/m2)',...
    'MinLitzDia(m)','dielectricstrength_insulation(V/m)','min air gap (m)',...
    'Winding Pattern',...
    'MinWireSize(m)',...
    'MinWindingTurns','MaxWindingTurns','MaxNumberOfLayer','MaxWeight(g)',...
    'CoreDensity(g/m2)','CopperDensity(g/m2)','CoreInsulationDensity(g/m2)',...
    'WireInsulationDensity(g/m2)','BSAT_discount','CoreLossMultiple'...
    'maxpackingfactor','minpackingfactor','LitzFactor','BobbinWeightFactor'};

value1_design = {'Po(W)','Vin(V)','Va(V)','Vinsulation_max(V)','fs(Hz)','matno',...
    'CoreMatFreq(Hz)','CenterL (m)','CenterT (m)','CoreAc(m2)','CoreWindowH(m)','
```

```
        CoreWindowW(m)','NumOfPri',...
    'BcoreDensity(T)','WirePriDia(m)','WirePriFullDia(m)',...
    'WirePri_Idensity(A/m2)',...
    'WirePriNstrands','WirePri_per_layer','WirePri_Nlayer',...
    'CopperPackingFactor','PackingFactor','LossCore(W)',...
    'LossCopper(W)','WeightCore(g)','WeightPri_copper(g)','WeightPri_Insu(g)',...
    'WeightCore_Insu(g)','TotalWeight(g)','TempAbsolute(C)','L','airgap(m)','
        CoreIndex'};

field2 = 'data';
value2_req = {Date,RunNumber,Hypothesis,Notes,CodeName,Vin_range,G_range,Po_range,...
    Vinsulation_max_range,etaInductor,Tmin,Tmax,Jwmax,...
    MinLitzDia,dielectricstrength_insulation,mingap,...
    Winding_Pattern,MinWireSize,...
    MinWinding,MaxWinding,MaxMl,MaxWeight,...
    CoreDensity,CopperDensity,CoreInsulationDensity,...
    WireInsulationDensity,BSAT_discount,CoreLossMultiple,...
    maxpackingfactor,minpackingfactor,LitzFactor,BobbinWeightFactor};
value2_design = {[],[],[],[],[],[],[],[],[],[],[],[],[],[],[],...
    [],[],[],[],[],[],[],[],[],[],...
    [],[],[],[],[],[],[],[]};
global Requirement Design raw1 raw2 raw3 raw4 raw5 raw

% Save requirements
Requirement = struct(field1,value1_req,field2,value2_req);
% Save design results
Design = struct(field1,value1_design,field2,value2_design);
% Electrical constants. Normally there is no need to change
% ohm*m, resistivity of copper at 100C
rou = 2.3*1e-8;
% /(ohm*m), conductivity of copper
sigma = 1/rou;
% HA/m2, permeability of freespace
u0 = 4*pi*10^(-7);
% F/m, permittivity of freespace
ebsl0 = 8.854*1e-12;
%% MAIN BODY OF THE CODE STARTS FROM HERE
% ----------------------------------------------------------------------
% Read the material properties to get the P at different B and F map from
% the CoreLossData.xlsx file
% This map will be used to calculate core loss later on
[m1,n1] = size(raw1);
XCoreMAT = raw1(2:m1,2);
XCoreFreq = cell2mat(raw1(2:m1,3:n1));
[m1,n1] = size(raw2);
XCoreBfield = cell2mat(raw2(2:m1,3:n1));
[m1,n1] = size(raw3);
XCorePloss = cell2mat(raw3(2:m1,3:n1));
[m1,n1] = size(raw4);
XCoreBSAT = cell2mat(raw4(2:m1,3:n1));
[m1,n1] = size(raw5);
XCoreMU = cell2mat(raw5(2:m1,3:n1));

% Constant
Pbar = 500;    %500mW/cm3
PFfactor = 1; %

% Draw out Pv plot vs B then interpolate
NoMat = m1-1;
Ball = 0.001:0.001:1;
MATcolorvector = rand(NoMat,3);
FreqFlag = zeros(size(1:1:NoMat));
for i = 1:1:NoMat
    DataSheetFreq = XCoreFreq(i,~isnan(XCoreFreq(i,:)));
    NoFreq = length(DataSheetFreq)/2;
    colorvector = rand(NoFreq,3);
    for j = 1:1:NoFreq
        %Pv = ConstantA*Bfield+ConstantB
```

```
142         ConstantA(i,j) = (log10(XCorePloss(i,2*j)) - log10(XCorePloss(i,2*j-1)))/(
                log10(XCoreBfield(i,2*j)) - log10(XCoreBfield(i,2*j-1)));
143         ConstantB(i,j) = log10(XCorePloss(i,2*j)) - ConstantA(i,j)*log10(XCoreBfield(
                i,2*j));
144         B_atPv_500(i,j) = 10^((log10(Pbar) - ConstantB(i,j))/ConstantA(i,j)); % in T
145         F_atPv_500(i,j) = DataSheetFreq(2*j-1); % in Hz
146         PF_atPv_500(i,j) = B_atPv_500(i,j)*F_atPv_500(i,j)^PFfactor;
147
148         % if (abs(fs_range - F_atPv_500(i,j))./fs_range <= 0.4)
149             FreqFlag(i) = 1;
150         % end
151         % Steinmetz
152         if (j > 1)
153             beta_range(i,j) = log10(XCorePloss(i,2*j)/XCorePloss(i,2*j-1))/log10(
                    XCoreBfield(i,2*j)/XCoreBfield(i,2*j-1));
154             %Third point
155             XCorePloss_3rd(i,j) = 10.^(ConstantA(i,j-1)*log10(XCoreBfield(i,2*j)) +
                    ConstantB(i,j-1));
156             alpha_range(i,j) = log10(XCorePloss_3rd(i,j)/XCorePloss(i,2*j))/log10(
                    DataSheetFreq(2*j-3)/DataSheetFreq(2*j-1)); %(f2/f1)^alpha = P2/P1;
157             K1_range(i,j) = XCorePloss(i,2*j)/(XCoreBfield(i,2*j)^beta_range(i,j))/(
                    DataSheetFreq(2*j-1)^alpha_range(i,j)); %mW/cm3
158             %Repeat frequency 2's steinmetz parameter for frequency 1
159             if (j == 2)
160                 beta_range(i,j-1) = beta_range(i,j);
161                 alpha_range(i,j-1) = alpha_range(i,j);
162                 K1_range(i,j-1) = XCorePloss(i,2*j-2)/(XCoreBfield(i,2*j-2)^
                        beta_range(i,j-1))/(DataSheetFreq(2*j-3)^alpha_range(i,j-1));
163             end
164         end
165     end
166 end
167
168 % Core size
169 [m1,n1] = size(raw);
170 % Column order:
171 % Ve(mm3), Ae (mm2), Le (mm), CoreShapeIndex, WindingPatternIndex, Window W (mm),
        Half Window H (mm), Core W (mm),
172 % Half Core H (mm), Core Thick (mm), Center Leg Diameter (mm), Total Window W (mm)
173 XCoreIndex = cell2mat(raw(3:m1,1));
174 XcoreVe = cell2mat(raw(3:m1,3))/(1000^3); % in m
175 XcoreAe = cell2mat(raw(3:m1,4))/(1000^2);
176 XcoreLe = cell2mat(raw(3:m1,5))/1000;
177 XcoreCoreShapeIndex = cell2mat(raw(3:m1,6));
178 XcorePriW = cell2mat(raw(3:m1,8))/1000;
179 XcorePriH = cell2mat(raw(3:m1,9))/1000;
180 XcoreSecW = cell2mat(raw(3:m1,10))/1000;
181 XcoreSecH = cell2mat(raw(3:m1,11))/1000;
182 XcoreWindowW = cell2mat(raw(3:m1,12))/1000;
183 XcoreWindowH = 2*cell2mat(raw(3:m1,13))/1000;
184
185 % ------------------------------------------------------------------------
186 % DESIGN STARTS FROM HERE
187 % This section lists all possible designs and prepare for the parfor loop
188 % in the next section
189
190 % Limit to core materials based on frequency
191 CoreMatIndexSweep = find(FreqFlag);
192
193 % Vectorize the design space
194 [Po,Vin,G,matno_record,CoreIndex,Np,Mlp,airgap] = ndgrid(Po_range,Vin_range,...
195     G_range,CoreMatIndexSweep,XCoreIndex,MinWinding:IncreN:MaxWinding,1:IncreMl:MaxMl
        ,mingap:mingap:100*mingap);
196
197 Po = reshape(Po,[],1);
198 Vin = reshape(Vin,[],1);
199 G = reshape(G,[],1);
200 matno_record = reshape(matno_record,[],1);
```

```
Np = reshape(Np,[],1);
Mlp = reshape(Mlp,[],1);
airgap = reshape(airgap,[],1);
CoreIndex = reshape(CoreIndex,[],1);

% Map CoreSize to actual size
Vcore = XcoreVe(CoreIndex); % in cm
Ac = XcoreAe(CoreIndex);
W = XcoreWindowW(CoreIndex);
H = XcoreWindowH(CoreIndex);
Le = XcoreLe(CoreIndex);
Center_L = XcorePriW(CoreIndex);
Center_T = XcorePriH(CoreIndex);

% Map material
ui = XCoreMU(matno_record);
BSAT = XCoreBSAT(matno_record);

% Inductance following RTC operating principles
Vo = Vin.*G;
Vinsulation_max = Vo;
L = u0*Ac.*Np.^2./(airgap + Le./ui);
% compute RTC boost timing and frequency
Ctot = 160e-12; % Assume using two GS66502T in parallel, 40 pF, two C3D1P7060 in
    parallel, 20 pF, with some room

for xx = 1:1:length(L)
    sigma=(Vo(xx)-2*Vin(xx))./(Vo(xx)-Vin(xx));
    theta=acos(1-sigma);
    tring(xx)=(pi-theta).*sqrt(L(xx).*Ctot);
    Ilpeak(xx)=-(Vo(xx)-Vin(xx)).*sqrt(L(xx).*Ctot)./L(xx).*sin(theta);
    tlrise(xx)=L(xx).*abs(Ilpeak(xx))./Vin(xx);
    a=L(xx).*Vo(xx)./(Vo(xx)-Vin(xx));
    b=-2.*Po(xx).*Vo(xx).*L(xx)./Vin(xx)./(Vo(xx)-Vin(xx));
    c=-2.*Po(xx).*tring(xx)-2.*Po(xx).*tlrise(xx)-L(xx).*Ilpeak(xx).*Ilpeak(xx);
    d=-2.*Ctot.*Vo(xx).*Po(xx);
    p=[a b c d];
    I=roots(p);
    Ipeak(xx)=I(1);
end
tring = reshape(tring,[],1);
Ilpeak = reshape(Ilpeak,[],1);
tlrise = reshape(tlrise,[],1);
Ipeak = reshape(Ipeak,[],1);

tfall = L.*Ipeak./(Vo-Vin);
trise = L.*Ipeak./Vin;
thold = Ctot.*Vo./Ipeak;
T=trise+thold+tfall+tring+tlrise;
fs=1./T;
ILave = (Ipeak.*(trise + thold + tfall)/2 + Ilpeak.*(tring + tlrise)/2)./T;

%  Eliminate some elements based on dimension rule and BSAT rule
KeepAirGap = intersect(find(airgap >= mingap),find(airgap <= 0.2*Le));
ue = ui./(1+ui.*airgap./Le);
Bm_dummy = u0.*Np.*Ipeak./Le.*ue; %T
Keep_Bmindex = find(Bm_dummy < BSAT*BSAT_discount);
Keep_fsindex = intersect(find(fs >= 1000000),find(fs <= 3000000));
KeepIndex = intersect(intersect(KeepAirGap,Keep_Bmindex),Keep_fsindex);

Po = Po(KeepIndex);
Vin = Vin(KeepIndex);
G = G(KeepIndex);
Vo = Vo(KeepIndex);
Vinsulation_max = Vo;
matno_record = matno_record(KeepIndex);
ui = ui(KeepIndex);
BSAT = BSAT(KeepIndex);
```

```
268
269 CoreIndex = CoreIndex(KeepIndex);
270 Center_L = Center_L(KeepIndex);
271 Center_T = Center_T(KeepIndex);
272 H = H(KeepIndex);
273 W = W(KeepIndex);
274 Ac = Ac(KeepIndex);
275 Le = Le(KeepIndex);
276 Vcore = Vcore(KeepIndex);
277 airgap = airgap(KeepIndex);
278
279 Np = Np(KeepIndex);
280 Mlp = Mlp(KeepIndex);
281 L = L(KeepIndex);
282 fs = fs(KeepIndex);
283 Ipeak = Ipeak(KeepIndex);
284 Ilpeak = Ilpeak(KeepIndex);
285 trise = trise(KeepIndex);
286 Bm = Bm_dummy(KeepIndex);
287
288 % Find core loss property that's none zero around the required frequency for each
      design group
289 FsnoNonzero = F_atPv_500(matno_record,:) > 0;
290 FsnoIndex = abs(fs - F_atPv_500(matno_record,:))./fs <= 0.4;
291 matfsIndex = FsnoNonzero.*FsnoIndex;
292 matfs = F_atPv_500(matno_record,:).*matfsIndex;
293 K1 = K1_range(matno_record,:).*matfsIndex*1000; %convert from mW/cm3 to W/m3
294 alpha = alpha_range(matno_record,:).*matfsIndex;
295 beta = beta_range(matno_record,:).*matfsIndex;
296 [rowIdcs, colIdcs] = find(matfs > 0);
297
298 % So far, each row of the above represent one DESIGN POINT (that has one
299 % set of electrical requirements, one core size, one core material, one Np, Mlp and
      Mls);
300 % Each row of matfs, K1, alpha and beta also correspond to each DESIGN POINT
301 % However, they have more than one non-zero columns because each material
302 % may have more than one loss data points in their datasheets around the required
      frequency
303
304 % We need to expand the design point to incorporate different loss data
305 % points for one material.
306
307 % Find the indices of unique values in rowIdcs
308 [UniqueRowIdcs, ind] = unique(rowIdcs,'rows');
309 ColDuplicate = sum(matfs(UniqueRowIdcs,:)~=0,2);
310
311 % Repeat by the number of loss data of each design point
312 Po = repelem(Po(UniqueRowIdcs),ColDuplicate);
313 fs = repelem(fs(UniqueRowIdcs),ColDuplicate);
314 Vin = repelem(Vin(UniqueRowIdcs),ColDuplicate);
315 Vo = repelem(Vo(UniqueRowIdcs),ColDuplicate);
316 Vinsulation_max = repelem(Vinsulation_max(UniqueRowIdcs),ColDuplicate);
317 matno_record = repelem(matno_record(UniqueRowIdcs),ColDuplicate);
318 ui = repelem(ui(UniqueRowIdcs),ColDuplicate);
319 BSAT = repelem(BSAT(UniqueRowIdcs),ColDuplicate);
320
321 CoreIndex = repelem(CoreIndex(UniqueRowIdcs),ColDuplicate);
322 Center_L = repelem(Center_L(UniqueRowIdcs),ColDuplicate);
323 Center_T = repelem(Center_T(UniqueRowIdcs),ColDuplicate);
324 H = repelem(H(UniqueRowIdcs),ColDuplicate);
325 W = repelem(W(UniqueRowIdcs),ColDuplicate);
326 Ac = repelem(Ac(UniqueRowIdcs),ColDuplicate);
327 Le = repelem(Le(UniqueRowIdcs),ColDuplicate);
328 Vcore = repelem(Vcore(UniqueRowIdcs),ColDuplicate);
329 airgap = repelem(airgap(UniqueRowIdcs),ColDuplicate);
330
331 Np = repelem(Np(UniqueRowIdcs),ColDuplicate);
332 Mlp = repelem(Mlp(UniqueRowIdcs),ColDuplicate);
```

```
L = repelem(L(UniqueRowIdcs),ColDuplicate);
Ipeak = repelem(Ipeak(UniqueRowIdcs),ColDuplicate);
Ilpeak = repelem(Ilpeak(UniqueRowIdcs),ColDuplicate);
trise = repelem(trise(UniqueRowIdcs),ColDuplicate);
Bm = repelem(Bm(UniqueRowIdcs),ColDuplicate);
% Reformat loss data into one non-zero vector
matfs = nonzeros(reshape(matfs(UniqueRowIdcs,:)',[],1));
K1 = nonzeros(reshape(K1(UniqueRowIdcs,:)',[],1));
beta = nonzeros(reshape(beta(UniqueRowIdcs,:)',[],1));
alpha = nonzeros(reshape(alpha(UniqueRowIdcs,:)',[],1));

%size(Po)
if (isempty(Po))
    y = 0;
else
    %Repeat elements by Primary Wire Number of Strands
    skindepth = 1./sqrt(pi*fs*u0/rou);
    ds = max(skindepth,MinLitzDia*ones(size(skindepth))); % take the skin depth litz
    Pri_Nstrands = floor((Po*2/etaInductor./Vin/Jwmax)./(pi*ds.^2/4)) + 1;

    % Window area (m)
    Wa = H.*W;
    % Core weight (g)
    Wcore = Vcore.*CoreDensity;

    % Winding
    % Primary wire diameter (m)
    Pri_WireSize = sqrt(Pri_Nstrands.*pi.*ds.^2./4./LitzFactor./pi).*2;
    % Primary wire diameter (m) including the insulation layer
    Pri_FullWireSize = Pri_WireSize + (Vin./dielectricstrength_insulation).*2;

    CopperPacking = (pi.*Pri_WireSize.^2.*Np./4)./(H.*W);
    OverallPacking = (pi.*Pri_FullWireSize.^2.*Np./4)./(H.*W);

    % Winding structures
    % Core insulation thickness needed
    CoreInsulationThickness = Vinsulation_max./dielectricstrength_insulation;
    % Primary turns per layer
    Pri_PerLayer = floor(Np./Mlp);
    % Total length of windings
    TLp = Np.*2.*(Center_L + Center_T + 4*CoreInsulationThickness + 2.*Mlp.*
        Pri_FullWireSize);

    % Copper Loss parameters (Dowell)
    PriKlayer = sqrt(pi.*Pri_Nstrands).*ds./2./(Pri_WireSize);
    Pri_xp = ds./2./skindepth.*sqrt(pi.*PriKlayer);
    Pri_Rdc = rou.*TLp./(pi.*Pri_WireSize.^2./4);
    Pri_Fr = Pri_xp.*((sinh(2.*Pri_xp) + sin(2.*Pri_xp))./(cosh(2.*Pri_xp) - cos(2.*
        Pri_xp)) + 2.*(Mlp.^2.*Pri_Nstrands - 1)./3.*(sinh(Pri_xp) - sin(Pri_xp))./(
        cosh(Pri_xp) + cos(Pri_xp)));
    Pri_Rac = Pri_Rdc.*Pri_Fr;

    % Core loss and copper loss
    % Standard Steinmetz core loss (W)
    Pcore = CoreLossMultiple.*Vcore.*K1.*fs.^alpha.*Bm.^beta;
    Pcopper = (Po./Vin).^2.*Pri_Rdc + (Ipeak - Ilpeak).^2/8.*Pri_Rac;

    % Calculate the temp rise
    Rth = 16.31.*1e-3.*(Ac.*Wa).^(-0.405);
    Tafterloss = Rth.*(Pcopper + Pcore) + 25;

    % Calcualte the weight
    WeightPri_copper = pi.*Pri_WireSize.^2./4.*TLp.*CopperDensity;
    WeightPri_Insu = pi.*(Pri_FullWireSize.^2 - Pri_WireSize.^2)./4.*TLp.*
        WireInsulationDensity;
    WeightCore_Insu = (2.*H.*(Center_L + 2*Center_T) + 4.*W.*(Center_L + 2*Center_T)
        + H.*(2.*Center_L + 2*Center_T)).*CoreInsulationThickness.*
        CoreInsulationDensity;
```

```
395     TotalWeight = Wcore + WeightPri_copper + WeightCore_Insu;
396
397     % Filter the good designs
398     B_index = find(Bm < BSAT*BSAT_discount);
399     P_loss_index = find(Pcopper + Pcore <= Po*(1 - etaInductor));
400     Tafterloss_index = find(Tafterloss <= Tmax);
401     Tmin_index = find(Tafterloss >= Tmin);
402     TotalWeight_index = find(TotalWeight < MaxWeight);
403
404     OverallPackingmin_index = find(OverallPacking >= minpackingfactor);
405     OverallPackingmax_index = find(OverallPacking <= maxpackingfactor);
406     Mlp_index = find(Mlp.*Pri_FullWireSize <= W - 2*CoreInsulationThickness);
407     Pri_PerLayer_index = find(Pri_PerLayer.*Pri_FullWireSize < H - 2*
            CoreInsulationThickness);
408
409     Index_Meet_All = intersect(B_index,P_loss_index);
410     Index_Meet_All = intersect(Index_Meet_All,Tafterloss_index);
411     Index_Meet_All = intersect(Index_Meet_All,Tmin_index);
412     Index_Meet_All = intersect(Index_Meet_All,TotalWeight_index);
413     Index_Meet_All = intersect(Index_Meet_All,OverallPackingmin_index);
414     Index_Meet_All = intersect(Index_Meet_All,OverallPackingmax_index);
415     Index_Meet_All = intersect(Index_Meet_All,Mlp_index);
416     Index_Meet_All = intersect(Index_Meet_All,Pri_PerLayer_index);
417
418     % Sort by total weight and keep only the lightest five
419     [WeightSort,SortIndex] = sort(TotalWeight(Index_Meet_All));
420     if (length(SortIndex) >= 5)
421         TotalWeightSortIndex = Index_Meet_All(SortIndex(1:5));
422
423         Design(1).data = Po(TotalWeightSortIndex);
424         Design(2).data = Vin(TotalWeightSortIndex);
425         Design(3).data = Vo(TotalWeightSortIndex);
426         Design(4).data = Vinsulation_max(TotalWeightSortIndex);
427         Design(5).data = fs(TotalWeightSortIndex);
428         Design(6).data = matno_record(TotalWeightSortIndex);
429         Design(7).data = matfs(TotalWeightSortIndex);
430         Design(8).data = Center_L(TotalWeightSortIndex);
431         Design(9).data = Center_T(TotalWeightSortIndex);
432         Design(10).data = Ac(TotalWeightSortIndex);
433         Design(11).data = H(TotalWeightSortIndex);
434         Design(12).data = W(TotalWeightSortIndex);
435         Design(13).data = Np(TotalWeightSortIndex);
436         Design(14).data = Bm(TotalWeightSortIndex);
437         Design(15).data = Pri_WireSize(TotalWeightSortIndex);
438         Design(16).data = Pri_FullWireSize(TotalWeightSortIndex);
439         Design(17).data = Ipeak(TotalWeightSortIndex)./(pi*Pri_Nstrands(
                TotalWeightSortIndex).*ds(TotalWeightSortIndex).^2/4);
440         Design(18).data = Pri_Nstrands(TotalWeightSortIndex);
441         Design(19).data = Pri_PerLayer(TotalWeightSortIndex);
442         Design(20).data = Mlp(TotalWeightSortIndex);
443         Design(21).data = CopperPacking(TotalWeightSortIndex);
444         Design(22).data = OverallPacking(TotalWeightSortIndex);
445         Design(23).data = Pcore(TotalWeightSortIndex);
446         Design(24).data = Pcopper(TotalWeightSortIndex);
447         Design(25).data = Wcore(TotalWeightSortIndex);
448         Design(26).data = WeightPri_copper(TotalWeightSortIndex);
449         Design(27).data = WeightPri_Insu(TotalWeightSortIndex);
450         Design(28).data = WeightCore_Insu(TotalWeightSortIndex);
451         Design(29).data = TotalWeight(TotalWeightSortIndex);
452         Design(30).data = Tafterloss(TotalWeightSortIndex);
453         Design(31).data = L(TotalWeightSortIndex);
454         Design(32).data = airgap(TotalWeightSortIndex);
455         Design(33).data = CoreIndex(TotalWeightSortIndex);
456         y = 1;
457     else
458         y = 0;
459     end
460 end
```

```
461 end
```

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