Using Defect Data to Characterize Assembly Process Capabilities and Constraints for Printed-Circuit-Board Design for Assembly

by
Eric Martin Soederberg

B.S. Electrical Engineering, Worcester Polytechnic Institute (1983)

Submitted to the Sloan School of Management
and the Department of Electrical Engineering
in Partial Fulfillment of the Requirements of the Degrees of

Master of Science in Management
and
Master of Science in Electrical Engineering

at the
Massachusetts Institute of Technology
June, 1992

© Massachusetts Institute of Technology, 1992. All rights reserved.

Signature of Author_______________________________

Certified by_______________________________
John G. Kassakian, Professor of Electrical Engineering

Certified by_______________________________
Anant Balakrishnan, Assoc. Professor of Management

Certified by_______________________________
Arthur C. Smith, Chair, Department Committee on Graduate Studies

ARCHIVES
MASSACHUSETTS INSTITUTE
OF TECHNOLOGY
JUL 10 1992
LIBRARIES

Using Defect Data to Characterize Assembly Process Capabilities and Constraints for Printed-Circuit-Board Design for Assembly

by
Eric Martin Soederberg

Submitted to the Sloan School of Management
and the Department of Electrical Engineering on May 10, 1992,
in Partial Fulfillment of the Requirements of the Degrees of
Master of Science in Management and
Master of Science in Electrical Engineering

Abstract

Printed circuit boards (PCBs), the heart of most electronic products, are built using highly automated assembly processes. Currently available Design for Manufacturability and Assembly (DFMA) tools focus on combining parts and enhancing ease of assembly relative to manual and dedicated automatic assembly processes. Lacking design tools that can predict PCB assembly problems, manufacturers often rely on the iterative fabrication of prototype hardware and the intuition of product engineers to design electronic products that are producible in large volumes. DFMA methods, capable of capturing manufacturer specific process and part-related design constraints, are needed to ensure that new products are compatible with existing assembly processes early in the design cycle.

This research demonstrates how PCB assembly defect data can be used to characterize assembly process capabilities and constraints and outlines a method for communicating these constraints the the approp iate design engineers.

Typically a PCB assembly operation is faced with continuously changing product requirements and likewise a continuously changing set of process technologies and capabilities. This thesis stresses the importance of a continuously updated system for documenting and communicating process constraints to PCB designers.

Thesis Advisors:

Dr. John G. Kassakian	Professor of Electrical Engineering
Dr. Anant Balakrishnan	Assoc. Professor of Management

Acknowledgements

The work presented in this thesis was sponsored by the MIT Leaders for Manufacturing Program, a partnership between the MIT School of Engineering, the MIT Sloan School of Management and several major U.S. manufacturing companies. I would like to gratefully acknowledge the backing of this program and the resources it has provided during my two years at MIT.

The research for this thesis was done at Delco Electronics in Kokomo, Indiana. I would like to thank Delco for their very generous sponsorship. I would especially like to thank my company supervisor, Klaus Gschwend, for his support and encouragement.

Finally I would like to thank my thesis advisors, Anant Balakrishnan and John Kassakian, for their help and guidance in pulling this project and thesis together.

Table of Contents

1. Motivation 7
2. Background....14
   2.1. Delco Electronics....14
   2.2. The PCB Assembly Process at Delco Powertrain....15
3. Method of Analysis....17
   3.1 Identification of Design Related Manufacturability Problems....18
   3.2. In-circuit Rework Data and Analysis 19
      3.2.1. Compilation of Rework Data 21
      3.2.2. Estimated Cost of Rework....23
      3.2.3. Pareto Problem Areas by Cost or Rework....27
      3.2.4. Perform a Causal Analysis on Top 30 Problem Areas....28
      3.2.5. Current Design Related Manufacturability Problems 30
      3.2.6 Examples of DFMA Problems....33
4. Evaluation of Available DFMA Tools....37
   4.1. The Boothroyd Dewhurst Inc. DFMA Toolkit 38
      4.1.1. Manual DFMA....40
      4.1.2. BDI Printed Circuit Board DFMA 41
   4.2. The Texas Instruments/BDI PCB DFMA Tool....42
   4.3. Rules-in-the-Tools....43
   4.4. Product Design Specifications and Checklists....43
   4.5. Comparison of Available Tools 45
5. A Dynamic Approach to DFMA for PCB Assemblies....47
   5.1. Design Decisions....50
   5.2. Making Design Tradeoffs....51
   5.3. General Types of Design Tools 52
   5.4. Proposed Dynamic DFMA Method....54
      5.4.1. Process Oriented Design Specifications....56
      5.4.2. Knowledge-based PCB DFMA 57
         5.4.2.1 Defining Metrics for Evaluating Design Tradeoffs....58
         5.4.2.2 Modeling First Pass Assembly Yield 62
      5.4.3 Rules in the CAD Tools....68
6. Conclusions 69
References....72
Appendix A. Analysis of Variance–Missing Bottom Side Chips....74

List of Figures and Tables

Figure 1.1. Design constraints on electronic assemblies. 8
Figure 1.2. Product designed to match manufacturing processes. 10
Figure 2.1. Assembly process flow 15
Figure 3.1. The DPP Matrix. 22
Figure 3.2. Relative performance of different process/part-type categories. 23
Figure 3.3a. Frequency distribution of the most important (rank 1) defects. 28
Figure 3.3b. Frequency distribution of defects for rank 6: Short/Heatrail/ECMC. 29
Figure 3.4. Hole sizes for crystal mounting. 33
Figure 3.5. Solder shorts on J3. 34
Figure 3.6. Solder thieves used to prevent solder shorts. 34
Figure 3.7. Standard serial communications circuit. 35
Figure 4.1. The Boothroyd Dewhurst manual assembly DFMA approach. 39
Figure 5.1. A typical design cycle and the design tools pertinent to each stage. 49
Figure 5.2. Gatenby's DFX concept 51
Figure 5.3. A dynamic tool for DFMA of printed circuit board assemblies. 55
Figure 5.4. Process oriented product design specification. 57
Figure 5.5. Knowledge-based PCB DFMA. 58
Figure 5.6. The distribution of defects per board. 62
Figure 5.7. The expected distribution of defects per board. 63
Figure 5.8. Comparison of calculated and actual first pass yields 66
Figure 6.1. Product performance data routed to design. 70
Figure A1. SMC location and orientation on the bottom side of the ECMC product. . 74
Figure A2. Boxplots of the raw "missing component" data. 76
Table 3.1. Part count comparison for the products under study 18
Table 3.2. The DPP Matrix in normalized defects per million parts placed. 24
Table 3.3. Estimated repair times. 25
Table 3.4. Estimated cost of replacement parts. 26
Table 3.5. The top 20 defect categories. 27
Table 3.6. Causal analysis results 31
Table 3.7. 10Ω resistor failure rate. 36
Table 4.1. DFMA tool comparison. 37
Table 4.2. DFMA tools ability to address the problems found at DE. 46
Table 5.1. Relative performance of assembly processes. 52
Table 5.2. Results of a 15 board multiple defect analysis. 64
Table A1. Missing chip data broken into 40 experiments 75
Table A2. Analysis of variance for all main effects and 2-way interactions. 77
Table A3. Analysis of variance for the seven most significant effects. 78

1. Motivation

A printed circuit board (PCB) is flat non-conducting substrate that has one or more conducting layers patterned to interconnect electronic devices that are mounted on the board. Electronic components are assembled onto PCBs with various automated part insertion and soldering techniques to form PCB assemblies which are the heart of most electronic products.

Printed circuit board (PCB) assembly can be thought of as an assortment of discrete assembly processes strung together to form a composite assembly process that suits a manufacturer's product requirements. Each assembly process, within the combined assembly process, constrains the product design. In other words, a PCB design is constrained by the summation of all of the constraints from a number of individual assembly processes. The individual processes typically range from manual part insertion to completely automated part placement and solder processes. The standard part packages that are assembled onto the PCB further constrain the design. Most designers of other products, with their ability to define the form and function of major assembly components, are challenged by the near infinite degrees of freedom at their disposal. The PCB designer, on the other hand, is challenged by the large number of standards and process constraints, both explicit and hidden, that must be met. Here are several examples: if two surface mount components are positioned too close together on the side of a PCB that is being wave soldered, the two components will likely be shorted with a bridge of solder; if a bypass capacitor is located too far from the power pins of the integrated circuit (IC) that it is buffering, it will not buffer the IC and the circuit could fail; if all nodes of a PCB circuit are not available for test on the bottom side of the board then the in-circuit tester cannot verify the presence of all of the circuit components; if the leaded component holes in the

PCB are too big, the parts will likely fall out before it is soldered down; if the holes are too small, the assembly operators will have to struggle to get them in. Fig. 1.1 shows some of the sources of constraints that PCB designers are faced with.

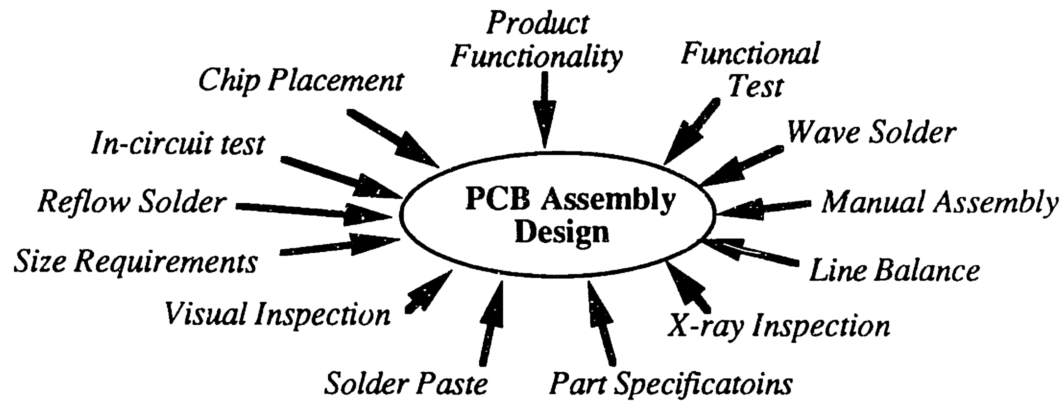


Figure 1.1. Design constraints on electronic assemblies.

The design constraints imposed by the processes and parts are not only numerous, they are also dynamic. The assembly processes and component packages used to build PCBs are changing rapidly as the electronics industry drives towards smaller more complex products. Brindley [6] points out that the package styles, dictated by the component manufacturers, once drove the assembly methods used to build electronic products. Now, however, the product manufacturers are driving the component package styles to fit their product requirements and assembly constraints. Recent examples include: fine-pitch surface mount technologies, flip-chip and tape bonding methods for securing integrated-circuit dies to PCBs, and soldering methods that do not require toxic solvents for cleaning. Hence, PCB design constraints are not only large in number, they are also changing rapidly.

It is no longer practical to rely on the intuition of the design engineers to develop PCB assemblies that take into account all pertinent design constraints. A DFMA tool that takes into account many individual and dynamic processes and part requirements is needed.

Shorter product life-cycles and market pressures to shorten time to market underline the need for design-process improvements in electronics.

Some argue that DFMA tools over-constrain designers and unduly inhibit their creativity. It should be pointed out that while design for assembly tools can require more effort in the early stages of product design, DFMA tools do not add design constraints--rather they attempt to illuminate *existing* constraints early in the design process. Highlighting the known constraints early in the design process allows more time to find creative solutions within the capability of the parts and the assembly processes.

DFMA tools are, by nature, specific to a particular assembly process. One cannot design a product for ease of assembly without defining an assembly method. For example, surface mount components are difficult to assembly by hand, even when using special tools. However, when a surface mount placement machine is available, these components can be assembled very quickly with ease. Various design tools are available for use in simplifying product designs that are built using manual assembly processes. However, PCB assembly requires many different automated assembly processes that are designed to handle many different part packages.

Most of the assembly processes and part packages used are standard throughout the industry [16]; however, very few manufacturers use the same combination of parts and processes. Even if two manufacturers do use the same processes and parts, they will likely have different levels of competence in using the processes and different process capacity constraints that would result in different product design criteria. The processes and the part packages, as well as the manufacturer's skill level, are constantly changing.

The most popular DFMA tools, such as the Boothroyd Dewhurst Inc. (BDI) DFMA toolkit [5], are based on the manual assembly process where there are many degrees of freedom in the part design and assembly process. These tools stress reduced part counts and ease of manual part insertion. Neither of these goals is applicable to PCB DFMA. Depending on one's process capabilities, a board with ten additional surface mount components (SMCs) may be easier to build than the same board with one additional leaded component. Designers need to know the specifics of their process capability and constraints in order to make intelligent design tradeoffs. For example, how much more should a designer be willing to pay for a surface mount component vs. a leaded version of the component given that it is easier to assemble the surface mount version? Design tools like the BDI DFMA tool allow designers to evaluate design tradeoffs while the design can still be changed easily. Design specifications are good for laying out the ground rules but they do not typically allow designers to evaluate tradeoffs, nor do they promote an active interchange between the designers and the manufacturers.

This thesis argues that the primary purpose of DFMA is to match products to process capabilities. (Fig. 1.2 shows this graphically) The following three steps are required to accomplish this:

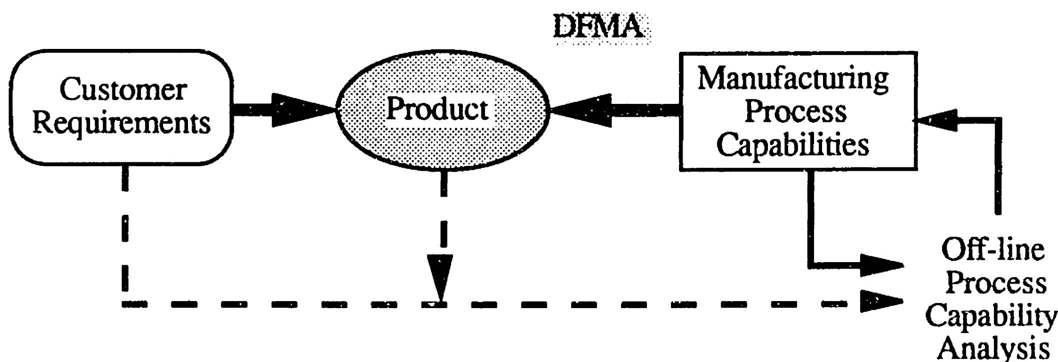


Figure 1.2. Product designed to match manufacturing processes.

- The first step in matching product and process is to define the process capabilities and constraints. For example, how close can surface mount components be mounted to each other to insure reliable wave soldering given a manufacturer's current wave solder capabilities or, how close to the edge of the board can a component be placed such that it is not knocked off when the board is moved from one assembly process to the next? Some general guidelines and industry standards are published [16] but the surface mount processes are still not mature and some assembly machines have different constraints than others. When these process constraints are documented, they are typically proprietary to the company that developed them.

- Once the process capabilities are well defined, they must be communicated to the designers in such a way that the designers are made aware of all process constraints while the design is still fluid and intelligent design tradeoffs can be made. For example, if a designer cannot satisfy all of the design constraints or guidelines, which constraint should be violated first, the distance to the edge of the board constraint or the component to component spacing? This constraint-communication scheme can take several forms including written manuals and design tools (e.g., computer aided PCB layout tools) with built in rule checking.

- Finally, new and improved process capabilities should be developed to support current and future product requirements. If new product designs are consistently constricted by one's ability to reliably place leaded components, then one should consider improving the leaded assembly process.

These three steps imply that all new products should be designed to match existing processes. While this is desirable, it is not always possible. For example, if you were to

design a wrist-watch television you would be seriously constrained by the available PCB assembly processes and available part packages. A new assembly method, perhaps a dedicated assembly machine would have to be developed simultaneously with the product development in order to meet the product's requirements. On the other hand, if you were designing the TV control circuitry for a 21 inch living room model, you would design the PCB assembly to be built with your existing assembly equipment. At any rate, a PCB assembly should not be designed without a specific set of assembly processes in mind.

It is tempting to minimize the importance of DFMA for electronic products since the assembly costs are generally a small fraction of total product cost. Assembly costs represent less than 6% of total production cost of products in the electronics industry. [21] Assembly cost reduction, however, is only one of the potential benefits that DFMA offers. Keith Brindley, in "Newnes Electronics Assembly Handbook" [6], estimates that 85 to 90% of all electronic assembly defects are a result of assembly problems. By facilitating a better match between product design and assembly process capabilities, production yields will increase and thus the likelihood of delivering defective products to the customer will decrease. Improved quality, less frustrated assembly workers or machine operators and fewer prototype revisions are all likely by-products of DFMA.

This thesis demonstrates how manufacturing defect data can be used to measure and characterize the match between assembly process and PCB design. This is done by comparing the relative production performance of three different PCB products that are built in the same assembly area using the same assembly processes. The effectiveness of some currently available DFMA tools is evaluated by first identifying the types of producibility problems that are experienced at a high volume board assembler, and then assessing the tools' ability to address these problems early in the design process. Learning from this comparison of available DFMA tools, the producibility problems isolated in the

defect data, and the types of decisions that designers make, a dynamic method for capturing and communicating process constraints to the designers is outlined.

Chapter 2 describes the setting in which this thesis research was conducted and a brief description of the PCB assembly process that was studied. Chapter 3 outlines the method used to uncover producibility problems, specifically those related to product design using assembly defect data. An evaluation of currently available DFMA tools is presented in Chapter 4 and a new DFMA approach is defined in response to these findings in Chapter 5. Conclusions are contained in Chapters 6.

2. Background

The analysis and results presented in this thesis is based on data collected and research conducted at Delco Electronics in Kokomo, Indiana.

2.1. Delco Electronics

Delco Electronics (DE) is a subsidiary of GM Hughes Electronics which is a wholly owned subsidiary of General Motors (GM). DE builds virtually all of General Motors' automotive electronics subassemblies (e.g. engine control modules, radios and air conditioning control units) and supplies electronic assemblies to several other automobile manufacturers as well. Seven business units operate production facilities in England, Singapore, Mexico, Wisconsin and Indiana. This thesis work was hosted by the Powertrain Electronics (PE) Business Unit in Kokomo, Indiana. PE designs and builds engine-control and transmission-control electronics.

An engine control module is typically built on a 5 by 8 inch PCB. The majority of the small components (resistors and capacitors) are surface mounted to the bottom side of the board and the larger components are surface mounted and through hole mounted on the top of the board. The newer Powertrain control modules combine electronic transmission control with engine control functions, and require two PCBs. Control modules that are mounted in the passenger compartment are packaged in aluminum sheet-metal boxes, while under-hood mounted modules are sealed in die-cast aluminum cases. PE builds roughly a dozen different engine controller board types in high volume (100,000 to 500,000 per year) and a dozen or so in low volumes (10,000 to 100,000 per year). GM car divisions purchase the majority of these controllers.

2.2. The PCB Assembly Process at Delco Powertrain

The individual assembly processes used at DE Powertrain are standard for the electronics industry. These include; surface mount components (SMC) onto solder paste; surface mount onto glue dots; manual component insertion; wave solder; in-circuit test; and so forth. The assembly process flow at DE, combining the individual assembly and test processes, is similar to the assembly process flow seen at other electronics manufactures, though the exact order of the assembly and test steps may be unique to DE. The following paragraphs describe the DE process flow. This process flow is described here as an example of the steps required to assemble a printed circuit board, and as a reference for the analysis presented in Chapter 3.

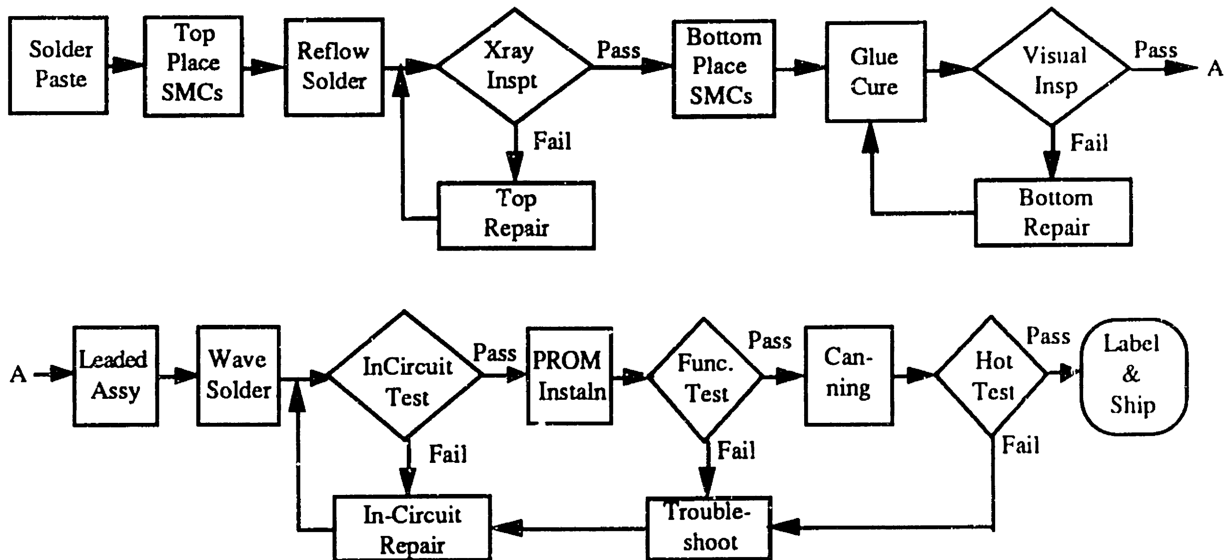


Figure 2.1. Assembly process flow.

The DE assembly process flow, shown in Fig. 2.1 above, begins with the automatic placement of the top SMCs onto a PCB that has been printed with solder paste. (Refer to Brindley [6] or Noble [19] for detailed descriptions of these assembly processes.) An infra-red oven then reflows the solder paste to secure these parts. An automated X-ray inspection machine then inspects the solder joints before the boards move to bottom-side

placement. Glue dots are applied to the bottom side of the board with an automated process that uses a product specific die with a glue pin positioned in the center of each chip location. The bottom surface mount parts (chips) are placed on the glue dots with a second automated placement machine, the glue is cured in an infra-red oven, and then the bottom side of the board is visually inspected by hand. Upon passing visual inspection, the boards are carried to the manual assembly area where the convector assembly (the heat-sink) and leaded components are inserted by hand. The bottom side of the board is then carried through a wave of molten solder to solder both the bottom surface mount parts and the leaded components in place. In-circuit and functional tests verify the proper installation and operation of the components through a "bed of nails" test fixture. Finally the PROM is installed, the unit is functionally tested, mounted in a case, tested again at an elevated temperature, and then shipped. Three different rework sites–top repair, bottom repair and in-circuit repair–rework the boards that fail the various inspections and tests shown in Fig. 2.1.

3. Method of Analysis

As argued in Chapter 1, designing products for assembly requires:

1. a clear understanding of the process capabilities and constraints, and
2. a method for communicating these constraints to the designers.

This thesis addresses both of these issues, process constraint identification and constraint communication.

Identifying Process Constraints:

In order to evaluate the type of constraint information that needs to be conveyed to PCB assembly designers, a list of current manufacturing problems that could be attributed to product design was compiled. This was done by measuring and comparing the manufacturing performance of three different products that are built using the same assembly line at DE. The relative performance of the various assembly methods employed at DE (e.g. reflow surface mount vs. wave soldered surface mount vs. manual insertion) was also compared.

Communicating Process Constraints:

Constraint communication was addressed by first evaluating available DFMA tools. The design-related manufacturing problems compiled in the constraint analysis were analyzed to determine which problems could have been avoided using which types of DFMA tools. A dynamic DFMA method is proposed that is capable of addressing all of the design problems found in the constraint analysis, and is maintainable as processes and a manufacturer's understanding of the processes change.

The next two sections (3.1 and 3.2) describe constraint identification analysis in more detail. Chapter 4 compares available DFMA tools and Chapter 5 describes the proposed dynamic DFMA method.

3.1 Identification of Design Related Manufacturability Problems

Manufacturability problems were found by measuring and contrasting the assembly performance of three different products that were currently in production.

Three engine control products–referred to here as ECMA, ECMB and ECMC–were selected for manufacturability analysis. They are all single-board designs and were built in the same focused factory. Table 3.1 lists the number of circuit board components used in each product as an indication of the products' relative complexities. Because the operators and assembly processes used to build these products are constant, differences in assembly performance can be attributed to differences in product design.

Part Category	Product		
	ECMA	ECMB	ECMC
Top SMC Integrated Circuits	6	9	13
Top SMC (w/o Integrated Circuits)	46	52	112
Bottom SMC (Chips)	162	223	223
Leaded Components	7	9	18
Heat-Rail Leaded Components	6	9	11
Total	**227**	**302**	**377**

Table 3.1. Part count comparison for the products under study.

It was not feasible to collect detailed manufacturing performance data (i.e. not only the aggregate yield at a given process, but the reason for and location of the defects that occur) at every assembly process step in the PCB assembly process with the resources available for this project. Aggregate total process yield data (the percentage of boards passed divided by the number of boards tested) was collected for all of the processes, but was not

sufficient for identifying and comparing the performance of specific product design attributes. Detailed data was, and is often, available at the in-circuit test operation (refer to the process flow in Fig. 2.1.). At DE, detailed defect data was entered into a computer database by the rework operators at in-circuit test. At the other test stations, only the aggregate test yields were recorded in note books, and they were not connected to the information system.

3.2. In-circuit Rework Data and Analysis

The cost of rework performed after the in-circuit test was selected as the primary manufacturing performance measure for several reasons including the following:

- The total rework represents the largest single cost in the production area under study. [24]
- Detailed data is often available at rework. Upon receiving boards rejected by in-circuit test, the rework operators enter a description of each part they replace and the presumed reason why it needed to be replaced; e.g. "no-solder," "missing" or "off-location." This is the only comprehensive failure data that is recorded in the PE focused factories.
- Rework cost is a reasonable metric for producibility. It provides an indication of how well a product design matches the process capabilities.
- The vast majority of assembled parts are verified at the in-circuit test. The major production processes, those responsible for nearly all of the assembly errors, are up-stream from this test and as such are verified, to some extent, at in-circuit test.

Because there are two test and rework stations up-stream (earlier in the process flow) of in-circuit rework, in-circuit rework data is not a comprehensive or fair picture of all product

performance or manufacturability issues. However, a wide cross-section of product design problems are captured in this data and offer a significant basis from which to measure the effectiveness of DFMA methods and tools.

Four steps were taken to extract the most prominent DFMA issues from the rework data.

1. *Compile Rework Data:* All post in-circuit defect data for the three products under investigation was collected over an eight week period (approximately 18,000 defect data records). Each data record represents rework performed on one component of the circuit board and included the time that the rework was performed, the part and the location of the part that was reworked or replaced, the type of problem that was fixed, and the serial number of the product that was repaired. This data was broken down and categorized by product, by assembly process/part-type (e.g., bottom surface mount is a process/part-type category, it defines both the type of part and the process(s) used to assemble and secure the part to the PCB) and by type of defect (e.g., missing or no-solder).
2. *Estimate Cost of Rework:* Cost of repair was estimated for the various defect types and part categories. This was done to illuminate the most significant design problems.
3. *Prioritize Problems by Cost of Rework:* The cost of rework for each defect area (classified by product, process and type of defect) was calculated on a cost per board basis and then listed in descending order of cost.
4. *Perform a Causal Analysis on Top 30 Problem Areas:* The top 30 problem areas were disaggregated to the individual PCB component level and the probable causes for each component defect were assigned. Causes were attributed to one of three activities: the assembly operations

(e.g.the assembly workers or the machine operators), the assembly process (e.g. the placement or solder machines) or the product design.

These four steps are now described in more detail.

3.2.1. Compilation of Rework Data

Eight weeks of in-circuit defect data, for all three products, was compiled on the host information system.

Each part that was replaced during this time period was recorded as one event. It is important to note that rework failures were not recorded for each opportunity of failure, e.g. 68 opportunities for "no solder" conditions on a 68 pin part package, but rather there was one defect entry per part that was reworked or replaced. Albin and Friedman [1] point out that using the number of defects, counted by the opportunities for failure method, to prioritize problem areas is misleading due to the clustering and high variability of these types of counts. They recommend using board yield loss measurements to quantify the relative impact of a class of assembly defects. Because more than one part is often reworked on one board, the number of parts reworked is not a true board yield loss measure. However, it is rare that a large number of parts are reworked on one board. Ninty-five percent of the boards built over the two month data collection period had three or fewer defects. Large differences between problem ranking by relative board yields and problem ranking by number of parts reworked per board are unlikely.

Process and defect categories were defined to be sufficient for both problem isolation and cost estimation purposes. Categories were defined on three dimensions:

- Product; (three categories: ECMA, ECMB or ECMC)

- Type of Part that needed rework, and thus the manufacturing Process used; (five categories: Top SMC Quad[1], Top SMC other, Bottom SMC, Leaded Component, Leaded Component Mounted to the Heatrail)
- Defect Reason, the reason rework was required; (fourteen categories including: Missing, Failed Part, Not Seated, Wrong Part, No Solder, Off Location, and Short)

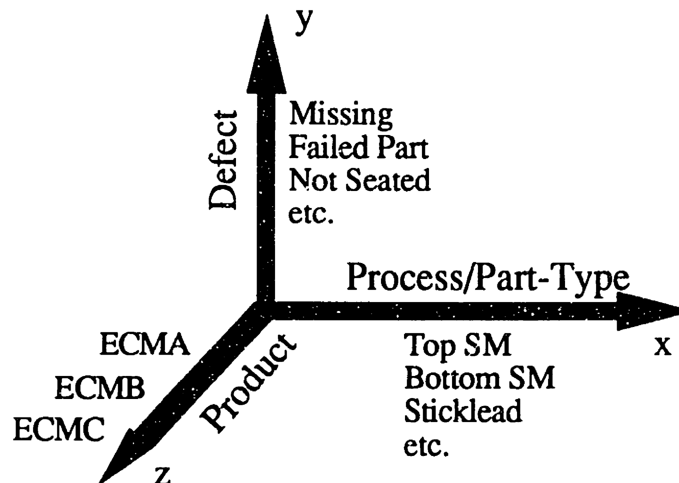


Figure 3.1. The DPP Matrix.

The Defect by Process by Product (DPP) Matrix, shown in Fig. 3.1, was created as the basis for most of the defect data analysis. The DPP Matrix is simply a three-dimensional array of defect data that allows defect data comparisons across three axes. Each cell of this array is calibrated in rework dollars per board and in defects per million parts placed. Looking down the product axis (the Z-axis) indicates whether a particular defect/process problem is product-related or process-related. Looking down the process categories (the X-axis) the relative capabilities of each process can be analyzed for each product. Looking down the defect description axis offers clues as to the root cause within the process

---

[1] A Quad is an integrated circuit packaged with leads on all four sides.

category in question. (e.g. a stuck glue pins would likely cause "missing" bottom SMCs, whereas a bad placement pipet might cause "off-location" defects)

Table 3.2 shows the DPP matrix that was derived form the eight week data sample. The data has been disguised for confidentiality such that the aggregate performance for ECMA is equal to 100. Fig. 3.2 compares the performance of the three products by part/process category.

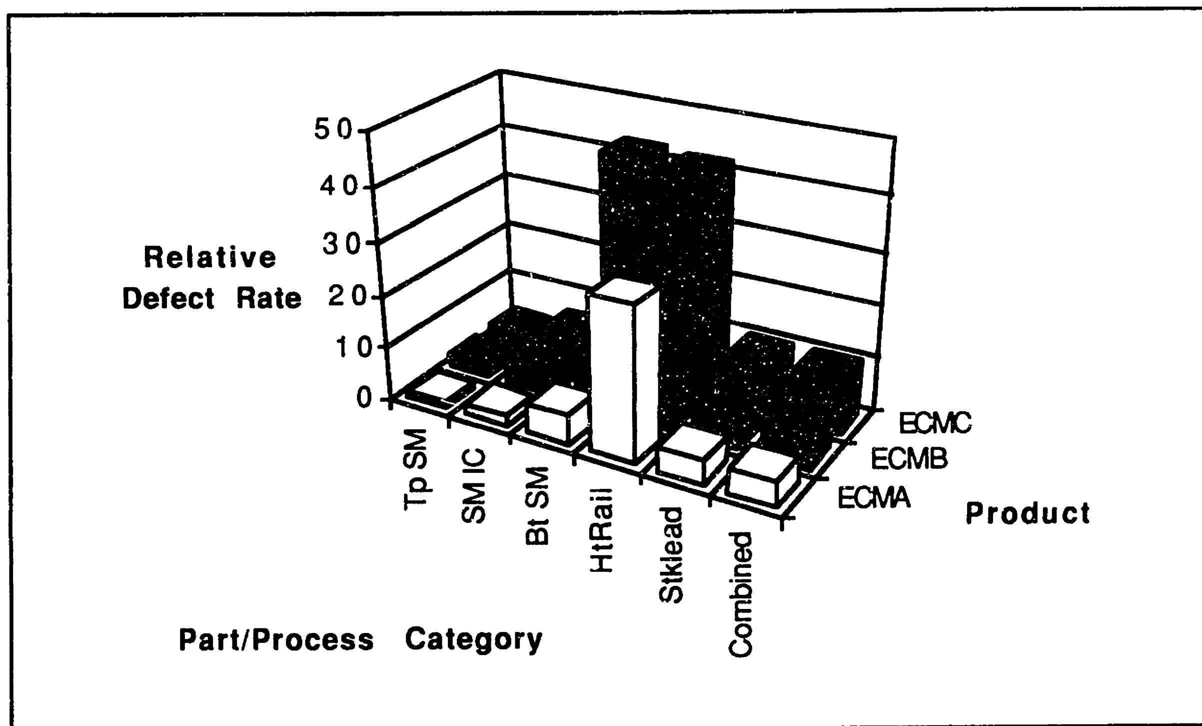


Figure 3.2. Relative performance of different process/part-type categories

3.2.2. Estimated Cost of Rework

As a means to weigh the significance of each problem area (i.e. each cell in the DPP matrix), the cost of rework labor and replacement parts was estimated for each defect-type and part category. The replacement part cost was added to the labor cost when a replacement part was required (e.g. for missing, failed part, or damaged part defect types).

DEFECTS PER x MILLION PARTS PLACED (8/27 to 10/23/91)*															
	ECMA Failures at Incircuit					ECMB Failures at Incircuit					ECMC Failures at Incircuit				
Defects	Tp SM	SM IC	HtRail	Stklead	Bt SM	Tp SM	SM IC	HtRail	Stklead	Bt SM	Tp SM	SM IC	HtRail	Stklead	Bt SM
Missing	0.9	0.6	14.2	315.4	19.1	8.6	2.1	68.6	269.0	36.2	2.8		112.7	327.1	48.9
Failed Part	13.8	32.3	11.6	18.8	15.9	26.3	71.7	23.2	20.0	22.9	28.4	75.3	67.3	52.7	37.0
No Solder	0.2		5.2		23.4	0.2		1.1	1.1	23.4	2.3	3.2	2.8	1.2	17.7
Short	0.3	3.2	48.4	1.7	8.2	0.4	23.2	26.4	2.1	1.7	1.7	11.2	595.9	2.9	30.4
Off Location	1.3				14.2	0.5				13.2	1.4	1.6	5.7	0.6	25.7
TroubleNotFound	3.8				4.5	7.3				7.3	24.1	4.0	0.9	21.4	28.0
Wrong Part	0.3		32.3	41.5	7.0	0.5	1.1	66.4	3.2	14.7	0.8		54.9	94.4	12.8
Not Seated	0.2		6.5	221.9	0.2	2.6		27.4	186.7	0.3	1.0	7.2	51.2	320.1	0.1
Excess Glue					6.3	0.4				6.9					8.6
Reversed		1.3	0.6	20.5		2.2			93.9		0.3	0.8	4.7	75.8	0.0
Damaged	0.7		2.6	3.3	1.9	1.6		10.5	3.2	1.5	1.7	0.8	17.1	1.7	3.6
Not Calibrated		3.2					1.1					18.4			
Too Much Solder					0.2	0.4			1.1	0.2	0.1		0.9	1.2	0.5
Extra Part		0.6		0.6	0.2				1.1	0.0			0.9		0.3
TOTAL	21.5	41.3	121.4	623.6	101.1	50.9	99.1	223.6	581.2	128.3	64.6	122.6	915.1	899.0	213.5
Defects/ x million parts placed/ product:					**100**					**130**					**219**

Table 3.2. Defect/Process/Product (DPP) Matrix, all numbers in normalized defects per million parts placed.

*This data has been disguised (normalized) so as not to divulge confidential performance data, the relative performance has been maintained.

The cost of labor includes both the rework operator's time and the in-circuit test operator's time for retest. No charge was included for equipment time or incidental rework supplies.

Because the rework operators in this factory record their repair operations on a computer database in real-time, it was possible to objectively measure the actual repair times of a large number of repairs without looking over the rework operators' shoulders with a stop-watch in hand. A stop-watch was used to corroborate the time values calculated from the database. Table 3.3 shows the results of the time study. Because the timed and calculated repair time measurements had large standard deviations, the estimated repair times were rounded to the nearest unit. Most repairs took the rework operators roughly 3 units of time to complete.

ESTIMATED REWORK TIMES, normalized*					
	Part/Process Category				
Defect Type	**Top SMC (non ICs)**	**Top SMC ICs**	**On Heatrail**	**Leaded**	**Bottom SMC**
Missing	3.00	7.00	3.00	3.00	3.00
Failed Part	3.00	7.00	3.00	3.00	3.00
No Solder	2.00	2.00	2.00	2.00	2.00
Short	2.00	2.00	2.00	2.00	2.00
Off Location	2.00	7.00	2.00	2.00	2.00
TroubleNotFound	2.00	2.00	2.00	2.00	2.00
Wrong Part	3.00	7.00	3.00	3.00	3.00
Not Seated			2.00	2.00	
Excess Glue					2.00
Reversed	2.00	7.00	2.00	2.00	
Damaged	3.00	7.00	3.00	3.00	3.00
Not Calibrated		7.00			
Too Much Solder	2.00	2.00	2.00	2.00	2.00
Extra Part	2.00				2.00

* *These times do not include time for retest; roughly one additional unit.*

Table 3.3. Estimated repair times.

Using the estimated repair times shown in Table 3.3 and the number of repairs performed over the eight week period, 78% of available rework time was accounted for. This is consistent with the rework operator idle time that was observed during this period.

The cost of replacement parts was estimated for each rework category by taking the weighted average of the actual part costs incurred over the eight week data collection period. See Table 3.4.

Estimated Replacement Parts Cost*	Product:			
Part Type Category	**ECMB**	**ECMA**	**ECMC**	**Combined**
Heat Rail				
Total Replaced (count)	*96*	*94*	*266*	*456*
Cost of Replaced ICs (dollars)	*148.50*	*169.77*	*232.17*	*550.44*
Est. Cost per Part (dollars)	1.55	1.81	0.87	**$1.21**
SM ICs				
Total Replaced (count)	*72*	*56*	*118*	*246*
Cost of Replaced ICs (dollars)	*443.24*	*292.47*	*618.69*	*1354.40*
Est. Cost per Part (dollars)	6.16	5.22	5.24	**$5.51**
Leaded				
Total Replaced (count)	*276*	*667*	*822*	*1765*
Cost of Replaced ICs (dollars)	*58.81*	*110.98*	*130.96*	*300.75*
Est. Cost per Part (dollars)	0.21	0.17	0.16	**$0.17**
SM Top and Bot				
Est. Cost per Part (dollars)		*Estimated*		**$0.01**

**The cost of each part replaced, over a given period of time, is summed and then divided by the total number of parts changed.*

Table 3.4. Estimated cost of replacement parts.

Using these time and part-cost estimates, the total cost of rework for each problem area in the DPP Matrix was calculated.

3.2.3. Pareto Problem Areas by Cost or Rework

The DPP Matrix entries are listed in descending order of rework cost per board in order to prioritize the defect categories. As implied by the DPP Matrix definition, each problem category is defined by a *defect* description, an assembly *process* and part-type, and a *product*; e.g. "missing, bottom SMCs on the ECMC product" tops the list. Each problem area is assigned a rank number that corresponds to its position on the list, "rank 1" being the most costly. Table 3.5 lists the top 20 defect categories.

Defect Category:			**Normalized Total Cost**	**Normalized Cost/Board**	
product	**part type**	**defect descptn**	**of Rework**		**rank**
ECMC	Bottom SMC	Missing	1.00	1.000	1
ECMC	Bottom SMC	Failed Part	0.76	0.756	2
ECMB	Bottom SMC	Missing	0.71	0.648	3
ECMC	Sticklead	Missing	0.57	0.575	4
ECMC	Bottom SMC	Short	0.46	0.464	5
ECMC	Heatrail	Short	0.45	0.449	6
ECMC	Bottom SMC	TroubleNotFound	0.43	0.430	7
ECMB	Bottom SMC	Failed Part	0.45	0.410	8
ECMC	Sticklead	Not Seated	0.39	0.395	9
ECMC	Bottom SMC	Off Location	0.39	0.392	10
ECMC	SMC IC	Failed Part	0.38	0.379	11
ECMB	Bottom SMC	No Solder	0.33	0.297	12
ECMC	Top SMC	Failed Part	0.29	0.291	13
ECMC	Bottom SMC	No Solder	0.27	0.270	14
ECMB	Bottom SMC	Wrong Part	0.29	0.263	15
ECMC	Bottom SMC	Wrong Part	0.26	0.262	16
ECMA	Bottom SMC	Missing	0.67	0.248	17
ECMB	SMC IC	Failed Part	0.27	0.242	18
ECMA	Bottom SMC	No Solder	0.58	0.216	19
ECMB	Sticklead	Missing	0.23	0.209	20

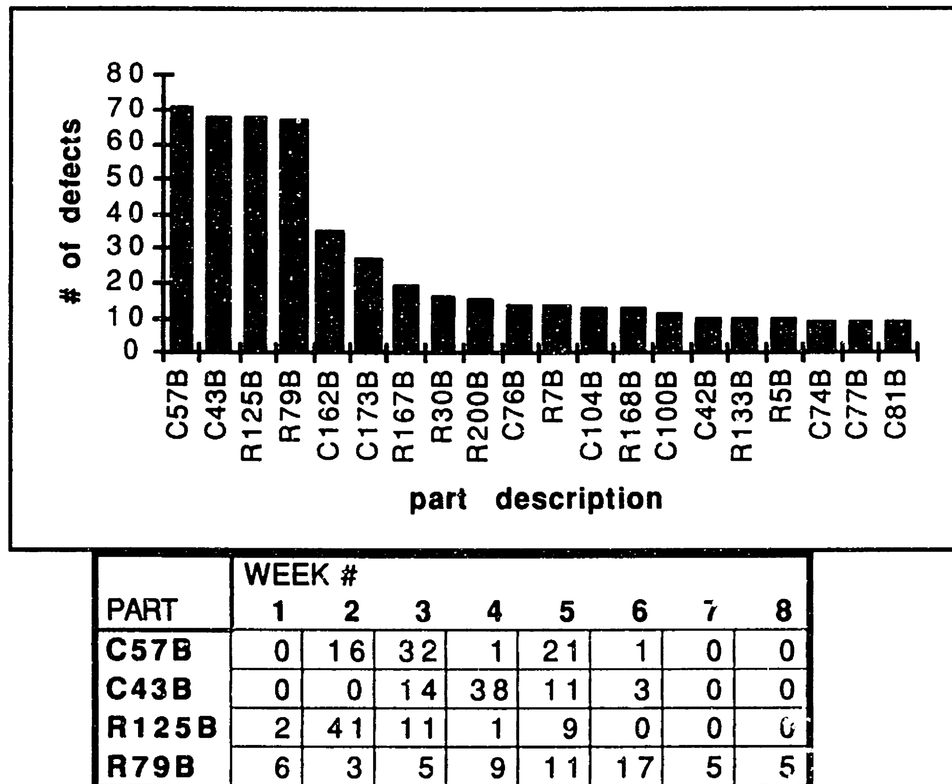
Table 3.5. The top 20 defect categories.

3.2.4. Perform a Causal Analysis on Top 30 Problem Areas

The top 30 (rank 1 through 30) problem areas were investigated in detail to determine the major cause(s) of failure. Each problem area (a cell in the DPP matrix) potentially has causes that can be attributed to any or all of the following:

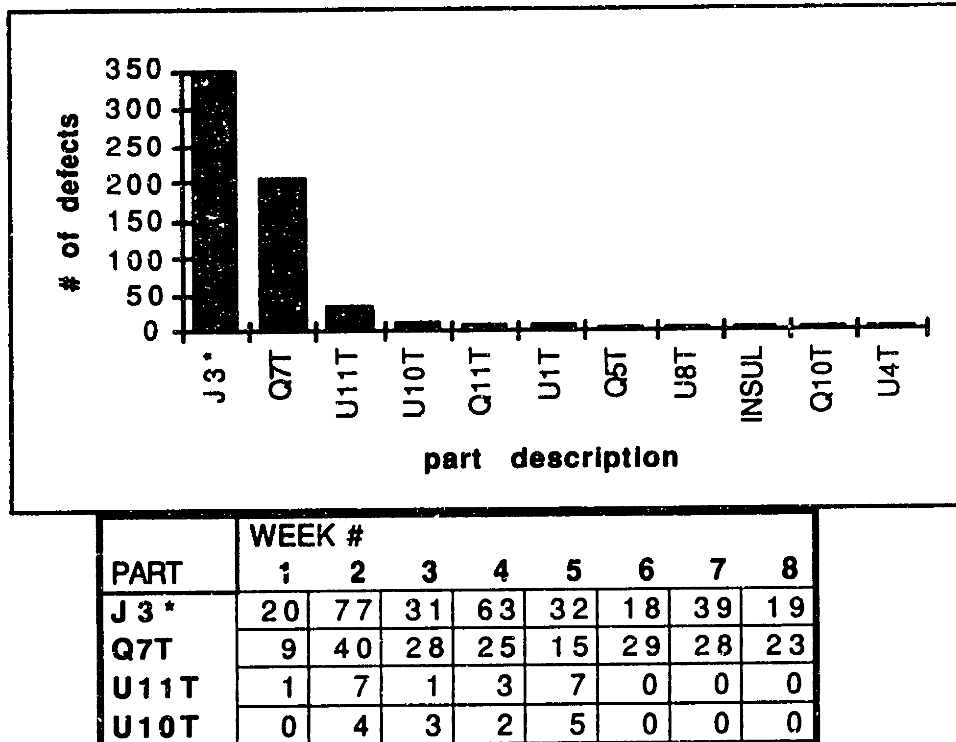
- an operations problem,
- a process problem, or,
- a product design problem.

This thesis concentrates on the design aspects of each production problem area.



PART	WEEK # 1	2	3	4	5	6	7	8
C57B	0	16	32	1	21	1	0	0
C43B	0	0	14	38	11	3	0	0
R125B	2	41	11	1	9	0	0	0
R79B	6	3	5	9	11	17	5	5

Figure 3.3a. Frequency distribution of the most important (rank 1) defects: Missing/Bottom SMC/ECMC.



PART	WEEK # 1	2	3	4	5	6	7	8
J3*	20	77	31	63	32	18	39	19
Q7T	9	40	28	25	15	29	28	23
U11T	1	7	1	3	7	0	0	0
U10T	0	4	3	2	5	0	0	0

Figure 3.3b. Frequency distribution of defects for rank 6: Short/Heatrail/ECMC.

The first step taken to isolate the defect causes was to disaggregate the individual defects within each problem area. Fig. 3.3 shows the frequency distribution of defects per individual PCB parts for the *rank 1* and *rank 6* problem areas. A week by week breakdown of the parts that fail most often provides evidence as to the nature of the cause, e.g., a one-time occurrence or a consistent problem. This specific part failure information was brought to the repair workers, the assembly machine operators and the manufacturing engineers to determine the most likely problem causes.

3.2.5. Current Design Related Manufacturability Problems

Table 3.6 lists the results of the causal analysis. Each problem area in the first column is the combination of problems found with all three products. The product distinctions were needed for the causal analysis, but are not needed for the tool analysis. Problem areas are now defined by defect description and process/part description (e.g. missing, bottom

surface mount), and the relative importance of each problem area is indicated by the rank numbers of each product problem area (determined by cost per board, see Table 3.5) from which each new problem area was derived.

The number of defects and total rework cost, in the second and third columns, give an absolute measure of the cost in this particular production area over the two month period studied. The forth column contains a normalized measure of problem severity in defects per million parts placed.

As mentioned earlier, the problem causes found could be assigned to one of three possible areas: operational, product design and process design. This table lists all three areas, though the design causes are of primary concern to this investigation.

In-Circuit Problem Area *Rank:(ECMA,B,C) by rework $/bd*	**Operational Cause**	**Product Design Cause**	**Process Design Cause**
Missing/Bottom SM *Rank: 1,3,17*	• Stuck Glue Pins • Visual missed it • Rough handling at stkld Assy • Boards stacked at visual insp	• Scattered chip layout • Empty pads near chips • Chip located near edge of board • Chips located near screw • High profile 0805s easy knock off • Transistor on bot. hard to inspect	• Glue pins unreliable • Visual inspection unreliable • Too much handling • 0805's easy to knock off
Failed Part/Bottom SM *Rank: 2,8,21*	• Pogo pins not working • "Failed" parts are not retested	• Tight tolerance (1%) parts used • Parallel capacitors hard to test • Extreme R&C values hard to test	• No pogo-pin continuity check • Tight Tolerances • Inconsistent test limits
Missing/Sticklead *Rank: 4,20,22*	• Conveyer jump knocks out part • Sticklead worker forgets part	• Unsecured parts fall out easily • Top heavy, loose parts fall out • Parts located in random locations • Holes too big • Difficult visual verification	• Time too tight for operator inspn
Short/BottomSM *Rank: 5,60,41*	• Solder wave out of tolerance	• Unmasked runner near chip pad • Exit pad too small for 1206 caps	• Solder wave requires tight specs
Short/Heatrail *Rank: 6,67,63*	• Solder wave out of tolerance	• Triangled wave exit. 65 pin heade (use solder thief) • Via hole close to sticklead pin • Long leads on heatrail IC	• Solder wave requires tight specs
TrblNotFnd/Bot SM *Rank: 7,33,48*	• Improper troubleshooting	• Tight tolerance (1%) parts used • Parallel capacitors hard to test • Extreme R&C values hard to test • Insufficient design for test	• No pogo-pin continuity check • Tight Tolerances • Inconsistent test limits • Poor test diagnostics

Table 3.6 Causal analysis results. Page 1 of 2

In-Circuit Problem Area	**Operational Cause**	**Product Design Cause**	**Process Design Cause**
Not Seated/Sticklead *Rank: 9,31,37*	• Conveyer jump knocks out parts	• Varistor on top of other parts • Unsecured parts fall out easily • Holes too big	• Time too tight for operator insptn
Off Location/Bot SM *Rank: 10,25,28*	• Pipet not working		• Pipets not reliable
Failed Part/SM IC *Rank: 11,18,44*	• Improper troubleshooting • "Failed" parts are not retested • Part not soldered	• Insufficient design for test	• Poor test diagnostics
Failed Part/Top SM *Rank: 13,29,46*	• "Failed" parts are not retested		• Tight Tolerances, pass E/C, Xray
No Solder/Bottom SM *Rank 14,12,19*	• Board not fully seated in pallet	• Chips in wake of screw head • No runner bottleneck to ground	• Pallets can be loaded improperly • Pallets out of spec
Wrong Part/Bot SM *Rank: 16,15,36*	• Wrong part loaded in MCMV • Bottom repair used wrong part	• Large number of part types used	• Bottom rework is required

Table 3.6 Causal analysis results. Page 2 of 2

3.2.6 Examples of DFMA Problems

Three examples of manufacturability problems found with this analysis are outlined here to illustrate the types of design problems that need to be addressed by DFMA methods.

Example 1. Missing Crystals

All three products use identical crystals for the microprocessor clock. The ECMC board has an order of magnitude fewer "Not-Seated" defects than the ECMB and ECMA products. As shown in Fig. 3.4, the ECMA and ECMB boards use a different hole pattern than the ECMC board.

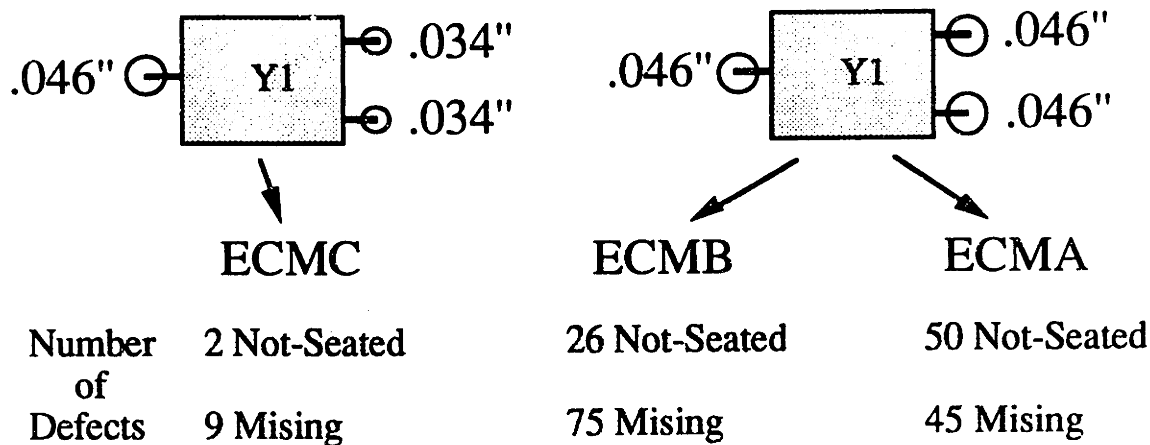


Figure 3.4. Hole sizes for crystal mounting.

Originally the hole pattern on the ECMC board was identical to that shown for the ECMB and ECMA boards. A manufacturing engineer recognized the missing crystal problem in an early version of the ECMC board and corrected it by using smaller holes for the active leads as shown in the ECMC configuration in Fig. 3.4. The ECMA board, the newest of

the three products, has not benefited from the ECMC experience due to a lack of communication between engineers.

Example 2. Wave Solder Shorts

The ECMC product consistently fails in-circuit test with solder shorts. The most common short occurs on a 65 pin connector (J3) shown in Fig. 3.5. This problem is likely much larger than the numbers suggest. The in-circuit test operator for this product typically removes the "J3" shorts before running the test. Solder bridges like these are a common at the end of a consecutive string of component leads. This effect is documented by Brindley [6] and Elliott [11].

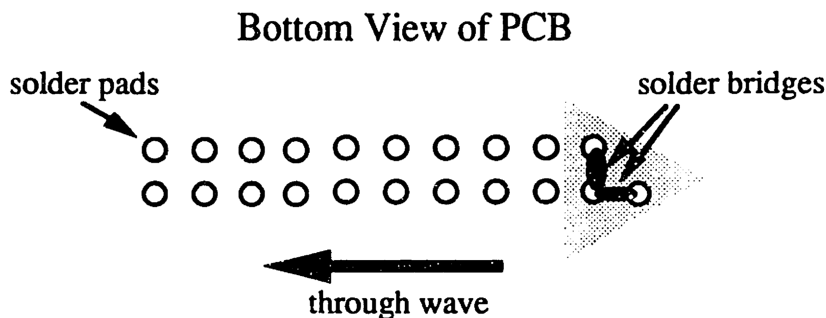


Figure 3.5. Solder shorts on J3.

Brindley and Elliott recommend the use of dummy pads, called solder thieves, at the end consecutive rows of solder pads such that the excess solder accumulation does not cause an undesired short. See Fig. 3.6.

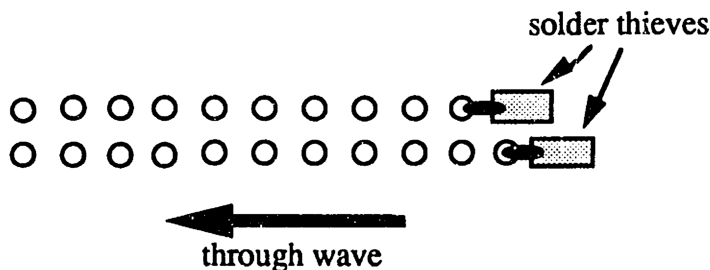


Figure 3.6. Solder thieves used to prevent solder shorts.

Example 3. Tight Part Tolerance on a current limit resistor

All three products use the same serial interface circuit which contains a 10Ω, 1% resistor in a DE standardized serial communications circuit. As shown in Fig. 3.7, the function of the 10Ω resistor is to protect the serial interface IC from an excess current condition. The serial interface circuit, with its required components, are considered a proven design and used in all recent engine controllers. As shown in Table 3.7, the ECMC and ECMB products have this part replaced for "failed part" failures 20 times more often than the ECMA product does. The rework operator enters a problem as "failed part" when there is no other apparent reason for failure, such as no-solder, off-location or missing problems. The removed parts are generally not retested.

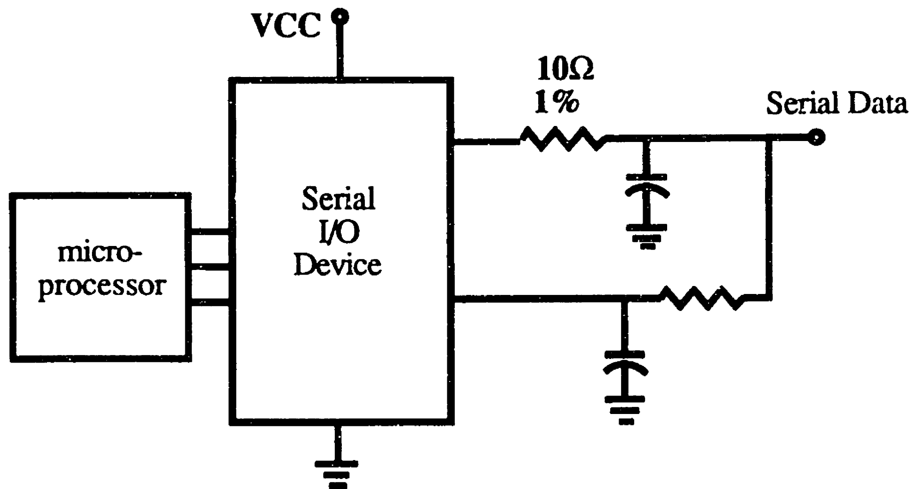


Figure 3.7. Standard serial communications circuit.

Product	Part Designator	# of "Failed-Part" Defects
ECMC	R23, Bottom SMC	49
ECMB	R79, Bottom SMC	40
ECMA	R49, Top SMC	5

Table 3.7. 10Ω resistor failure rate.

Small resistance values are difficult to test through the "pogo" or spring loaded test pins of the in-circuit "bed of nails" test interface because the contact resistance of the connection to the PCB is often larger than the allowed tolerance of the resistor.

On the ECMA product, this resistor is mounted on the reflow-solder side (top) of the PCB while the ECMB and ECMC products mount this resistor on the wave-solder side. Unfortunately, it is not clear whether the test limits; the part spec; or the assembly process; is the most significant cause of failure; however, the magnitude of the performance difference between the three products clearly indicates that some aspect of the problem is design-related and tight tolerances are difficult to measure at in-circuit test. Chevalier [8] has modeled the electronic testing problem and has derived equations for minimizing the total expected cost of quality based on where one inspects for defects and to what tolerance one accepts or rejects boards.

4. Evaluation of Available DFMA Tools

The object of this evaluation is to identify which types of available DFMA tools are capable of affecting the design decisions at the appropriate time in the design process of electronic products, i.e., before the design is frozen. An ideal DFMA system would be capable of evaluating the relative complexity of a design with a minimum amount of design information, be capable of predicting any and all downstream assembly difficulties, be easy to use, and be able to indicate clearly what steps need to be taken to improve the design under analysis. Of course, there are no ideal systems; however, it is important to have a clear goal for the ultimate tool.

DFMA tools and methods can be broken into two basic categories: those that use fixed experience databases to evaluate designs and those with user definable databases. As show in Table 4.1, the tools can be further broken down by those that are computer automated and those that are not.

DFMA Tools/Methods	Manual	Computer Automated
Fixed Database	GE/Hitachi/Westinghouse	BDI Toolkit
User Defined Database	Product Design Specs Checklists	Texas Instruments/BDI "Rules in the Tools"

Table 4.1. DFMA tool comparison.

The tools listed in Table 4.1 are discussed below in more detail. They are then evaluated relative to their ability to address the design problems identified in the causal analysis. The

following tools were selected to be representative of the DFA tools that are currently available to electronic product manufacturers:

- The Boothroyd Dewhurst Inc. Manual DFMA Tool (BDI Toolkit) [5]. This computer based tool is very similar to the manual General Electric/Hitachi/Westinghouse DFA method.
- The Texas Instruments/BDI PCB DFMA tool [4]. Originally developed for in-house use by Texas Instruments (TI), this product is being marketed jointly by TI and BDI.
- "Rules in the Tools". This is a Hewlett Packard expression [2] and [20] that refers to the concept of integrating design rules into the CAD tools that the engineers and draftsmen use to layout PCBs.
- Written Product Design Specifications (PDS) and Checklists. This is a written collection of design rules and guidelines used as a reference for designers and potentially as a design screening tool in product design reviews. The Institute for Interconnecting and Packaging Electronic Circuits (IPC) publishes a comprehensive PCB design specification [16].

The first two tools listed are commercially available personal computer programs. The remaining two tools are commonly used company-specific tools that are typically developed in-house.

4.1. The Boothroyd Dewhurst Inc. DFMA Toolkit

While this paper looks at the BDI Toolkit, it should be noted the manual assembly portion of the BDI Toolkit is very similar to the GE/Hitachi/Westinghouse (GE) method. Shina [21] has compared the methods by applying both the BDI and the GE manual assembly analyses to several different mechanical products. According to Shina's study, the two methods estimate assembly time to within 20% of each other and both methods are

repeatable to within 20% . The BDI manual assembly tool is used here to represent the entire class of tools that calculate assembly times and design efficiencies based on manual assembly time studies.

Written for an IBM compatible personal computer, the BDI DFMA software package[2] offers a number of tools to aid in the development of products that are easier to build. In general they guide the designers towards minimizing the number of parts and simplifying the required assembly operations.

The manual BDI assembly tool calculates measures of efficiency so that various design implementations can be compared for relative ease of assembly. The two primary measures of efficiency are the total estimated assembly time and the theoretical minimum number of parts required divided by the number of parts specified. The BDI DFMA tool was not designed to be a conceptual design aid, but rather a design analysis tool that can be applied to a design after the preliminary drawings are available. By encouraging part count reduction and ease of assembly, these tools minimize assembly costs by simplifying the assembly and part handling processes required to build a product.

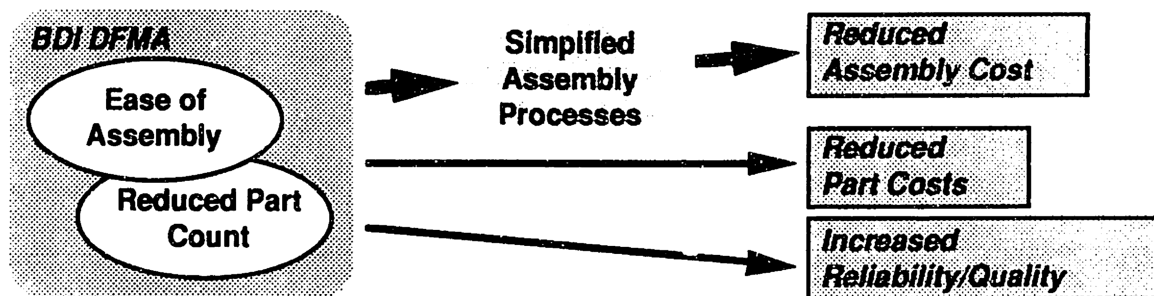


Figure 4.1. The Boothroyd Dewhurst manual assembly DFMA approach.

---

[2]Boothroyd Dewhurst Inc., "DFMA Toolkit", version 5.1a

The notion that BDI-like manual assembly tools are only good for analyzing mechanical products is not accurate. These tools are applicable to products that are built with manual assembly processes. In the case of PCBs, manual assembly is only a small part of the over-all assembly process and the BDI tool can be effective for this part of the assembly.

Two of the tools provided in the BDI DFMA Toolkit, the Manual Assembly DFMA Tool and the PCB DFMA Tool, are discused here. There are several other tools provided in this toolkit that are less pertinent to electronics assembly. [5].

4.1.1. Manual DFMA

The heart of the BDI Toolkit, the manual DFMA tool, systematically enforces the following set of rules [5]:

- Minimize the number of parts and part types.
- Eliminate adjustments.
- Design parts to be self-aligning and self-locating.
- Ensure adequate access and unrestricted vision.
- Ensure ease of handling from bulk.
- Minimize unneeded operations during assembly.
- Design parts that cannot be assembled incorrectly.
- Maximize part symmetry.

The manual analysis estimates the time and cost of assembling a given design by analyzing each part and each operation required to build a given assembly. The software penalizes (with additional assembly time) parts or operations that violate any of the above design rules. The assembly costs associated with each component are tabulated for reference during redesign.

Questions as to the fundamental necessity of a part lead the design team to reduce part count. Questions regarding the complex handling of individual parts lead the designer to part designs that are easy to assemble. The exercise of applying this analysis (i.e., answering the questions) leads a design team towards addressing the largest assembly cost areas in a systematic and insightful manner. The results of the analysis do not recommend specific design improvements; rather the exercise of applying this tool pushes the design team towards creative design improvements.

4.1.2. BDI Printed Circuit Board DFMA

The BDI Toolkit provides a printed circuit board tool to estimate the cost of assembling a PCB assembly. The theory behind this tool is that if you can estimate the cost of assembly up front, you can iterate on the design to come up with the least cost solution and thus the design that is easiest to build. However, this tool does very little to lead the designer to a better solution. Geoffrey Boothroyd describes it as an "after-the-fact" analysis tool that was added to the Toolkit for mechanical DFMA users who happened to have PCBs. The BDI PCB tool is described here for completeness, but is not considered in the tool evaluation section.

The PCB routine operates like a spreadsheet, calculating the cost of assembly by multiplying the number of parts inserted in a given part and process category by that category's cost per insertion and summing over all part categories. The cost of some process operations, such as wave solder, are simply added to the bottom line since the costs are considered fixed regardless of the number of parts on the board. All cost per insertion, time per insertion (for manually inserted components) and cost per operation data is stored in a database that can be modified by the user.

In summary, the BDI Manual DFMA tool has been proven to be effective in assessing ease of assembly relative to the manual-assembly process. It is most effective when a prototype is available to analyze. It is often argued that a good design for manual assembly is a good design for automated assembly and vice versa. This may be a convenient coincident for some automatic assembly processes, but the argument clearly does not hold for many of the automated PCB assembly processes which have no manual counterpart, such as surface mount and wave solder.

4.2. The Texas Instruments/BDI PCB DFMA Tool

This tool is a cleaned-up version of a program that TI has been using in-house for several years. It is based on a standard parts database that can be customized by the user. When fed a parts list, it calculates four PCB assembly metrics: PCB density, maximum board height, the ratio of auto-insert parts to manual insert parts, and the number of parts with special quality or handling requirements.

The heart of this tool is the parts database. Organized by part name, the part database is supplied with the most common electronic parts already entered and it can be modified and expanded by the user. The database contains information on the dimensions of each part, the assembly processes needed to assemble each part to the PCB, and a field for special-handling or quality-problem codes related to each part.

In addition to predicting possible board sizing conflicts, this tool has the ability to incorporate user specific lessons learned, indexed by part. This software tool was first released in October of 1991 without the ability to handle surface mount parts and processes. A surface mount version was due to be released in mid December of 1991.

4.3. Rules-in-the-Tools

Rules-in-the-tools [2, 20] refers to the incorporation of design constraints in computer aided design (CAD) tools. Whereas the TI tool aids the electrical design engineer in selecting components, CAD tools with built-in rule checking are used by draftsmen and engineers for PCB layout. For instance, a PCB layout CAD tool would not allow surface mount components to be mounted too close together or too close to the edge of a board. This is simply an automated implementation of the rules and specifications that most electronics manufacturers have written in design documents. With the proliferation of personal computers and workstations, there are literally hundreds of PCB design software packages on the market [15]. Most offer design rule verification (clearances and orientation) and schematic-to-layout checking. Some go far beyond the simple layout considerations and address complex and application specific issues, e.g. radio frequency and microwave simulations of microstrip and stripline designs.

When the design rules are written on paper, it is easy to accidentally violate them, or treat them as design guidelines instead of design rules. The rules-in-the-tools methodology effectively brings the specification information to the right place at the right time. By never granting the designer illegal degrees of freedom, complex design tasks can become less frustrating.

4.4. Product Design Specifications and Checklists

As mentioned above, design specifications are the written guidelines that every design engineer is expected to follow when developing a product. Most manufacturers have internal design specifications based on their own production experience as well as external standards such as part dimensions and material properties. For example, The Institute for Interconnecting and Packaging Electronic Circuits (IPC) publishes a widely accepted

standard, IPC-D-275, for the design of PCBs [16]. Adopted by the Department of Defense and the American National Standards Institute, IPC-D-275 addresses issues such as conductor spacing, land pattern design, laminate materials, component layout, and design for test. These guidelines are often violated in state of the art applications that push the process limits. In these instances a method for making tradeoffs among the different guidelines is needed, i.e., a list of guidelines is insufficient.

A checklist is a list of questions that verify conformance to design specifications and conformance to product development procedures. The lists allow a systematic review of the appropriate specification and procedures in a design review or audit. Examples of checklist questions for a circuit board layout audit include:[3]

Are all holes standard sizes?

Are all holes 1.5 times the laminate thickness from the board edge?

Have copper areas been waffled on the wave side? (so that the solder mask does not flake off)

Is the date code box in place?

Have the prints been given to Manufacturing Engineering?

Checklists are an effective means for verifying conformance to documented design specifications and design procedures. The major drawbacks with written design specifications and checklists are their lack of accessibility during the design task (right information at right time to right person) and the difficulty in keeping them current and therefore credible. They also lack the ability to aid a designer in making design tradeoffs in the event that all design constraints can not be met simultaneously.

---

[3]This list was taken from a DE circuit board layout review checklist, one of the nearly 100 design verification, manufacturability and reliability checklists used at DE.

4.5. Comparison of Available Tools

The tools described above are now evaluated using the list of design problems found in the rework-data analysis (Table 3.5.). Table 4.2. summarizes this evaluation. The question asked was whether each type of tool has the *potential* to flag each given DFMA problem in the list. This assumes that each problem was previously discovered and entered in the appropriate database or specification. The manufacturability problems are listed down the left-most column according to the assembly process that is responsible for the constraint.

The written PDS and Checklists are the only DFMA tools that are able to address all of the design-related assembly problems represented here. This is not a surprising result. The BDI Manual DFMA tool is capable of addressing design constraints related to the manual assembly process. The Texas Instruments PCB DFMA tools is capable of capturing part specific lessons learned and some very specific process specific design constraints (board density and maximum height). The rules-in-the-tools are useful only where CAD tools are used--typically only in board layout.

The design specifications and checklist are capable of capturing any and all of the design constraints, but they are incapable of presenting only the pertinent constraints for a particular product design and process configuration. This leaves the designers with the awesome task of reading through all of the design constraints and digging out the pertinent ones. These documents are typically large and difficult to maintain and, therefore, they are considered more as guidelines rather than meaningful and pertinent constraints. Product design specifications are typically read once during the first week a new engineer is on the job, and then referred to occasionally when a question comes up. Checklists are typically applied after the design is nearly complete in preparation for a design review. They provide

a systematic review of the design, but have weaknesses similar to the written design specifications. Specifically, checklists are hard to maintain and difficult to specialize to the specific product and process under analysis.

Product Design Cause	**Potentially addressed by:** BDI manl assy tool?	TI/BDI PCB tool?	Des specs &chklists?	Rules in the Tools?
(re: the visual inspection process)				
• Chip layout difficult too inspect	No	No	Yes	Maybe
• Empty pads near chips	No	No	Yes	Maybe
(re: the bottom surface mount assembly process)				
• Chip located near edge of board	No	No	Yes	Yes
• Chips located near screw	No	No	Yes	Yes
• High profile 0805s easy knock off	No	Yes	Yes	Maybe
• Transistor on bot. hard to inspect	No	Yes	Yes	Yes
• Large number of part types used	Maybe	No	Yes	Maybe
(re: the in-circuit test process)				
• Tight tolerance (1%) parts used	No	Yes	Yes	No
• Parallel capacitors hard to test	No	No	Yes	No
• Extreme R&C values hard to test	No	Yes	Yes	No
• Insufficient design for test	No	No	Yes	No
(re: the wave solder process)				
• Unmasked runner near chip pad	No	No	Yes	Yes
• Exit pad too small for 1206 caps	No	No	Yes	Yes
• 65 pin header, no solder thief	No	Yes	Yes	Yes
• Via hole close to sticklead pin	No	No	Yes	Yes
• Long leads on heatrail IC	No	Maybe	Yes	No
• Chips in wake of screw head	No	Maybe	Yes	Yes
• No runner bottleneck to ground	No	No	Yes	Yes
(re: the manual assembly process)				
• Unsecured parts fall out easily	Yes	No	Yes	No
• Top heavy, loose parts fall out	Yes	Yes	Yes	No
• Scattered leaded part layout	Yes	No	Yes	No
• Holes too big	Yes	No	Yes	Maybe
• Difficult visual verification	Yes	No	Yes	Maybe
• Varistor on top of other parts	Yes	Yes	Yes	Yes
TOTAL out of 24 Yes	6	7	24	10
Maybe	1	2	0	6

Table 4.2. DFMA tools ability to address the problems found at DE.

5. A Dynamic Approach to DFMA for PCB Assemblies

> "If we cannot analyze a design solution, then we cannot readily generate the *best* design since we cannot distinguish a good design from a bad design. In the absence of criterion for selecting good designs we cannot make good design decisions." – Nam Suh [23]

The primary purpose of a DFMA tool is to bring the right information to the product development team (PDT) at the right time. A good DFMA tool aids the design engineers in making decisions quickly so as to keep the momentum of the product development team going [21]. The question then becomes: How can we best capture assembly-related design constraints and feed them back to the appropriate design engineer at the appropriate time?

The right information. Of the many thousands of design constraints, the designers need to focus on those that are pertinent to the current design task. Up-to-date process performance data and part performance data are needed on each process and part that will be employed in building a new product. With the right information, the designers can make informed (data-driven) design decisions.

The right people. Many manufacturers, including DE, use cross-functional product design teams. The lead electrical engineer and the lead mechanical engineer are responsible for meeting the products' functional requirements, the manufacturing process engineer is responsible for meeting the manufacturing process constraints, the test engineer is responsible for meeting the test constraints and so forth. These are all the *right people* to target with the *right information*. A DFMA tool should aid the communications among the

members of the product development team by presenting them with the *right information* and challenging them to meet all of the pertinent design constraints simultaneously.

The right time. Design typically goes through a series of stages starting with a product concept and system design and ending with the release of a final production design. Fig. 5.1 shows the typical design stages and the design engineer responsible for each stage in the design. This thesis is primarily concerned with the electrical circuit design and the PCB layout that follow the system level design. There is no question that the concept and system level design stages are critical to building a successful product. However, it is difficult to perform a DFMA analysis on a system level design (e.g. a block diagram) since the parts and therefore the required assembly processes have not yet been determined. It is conceivable that a DFMA analysis, performed after a preliminary electrical and mechanical design, could lead to a modification of the system level or even conceptual design. In the context of this thesis, design for assembly tools address the detailed electrical and mechanical design tasks.

Before we can address how to get the right information to the right people at the right time it is first necessary to define what the right information is, who the right people are, and when is the right time. Stated differently; who is making what decisions when? Fig. 5.1 shows a typical design cycle, the decisions made at each stage, and the types of tools that are appropriate to each stage. This chapter will first discuss the design decisions that are crucial to PCB-assembly DFMA and then discuss design tradeoffs and the general types of tools that can be used to aid designers in making informed design decisions. Finally a new DFMA tool will be discussed.

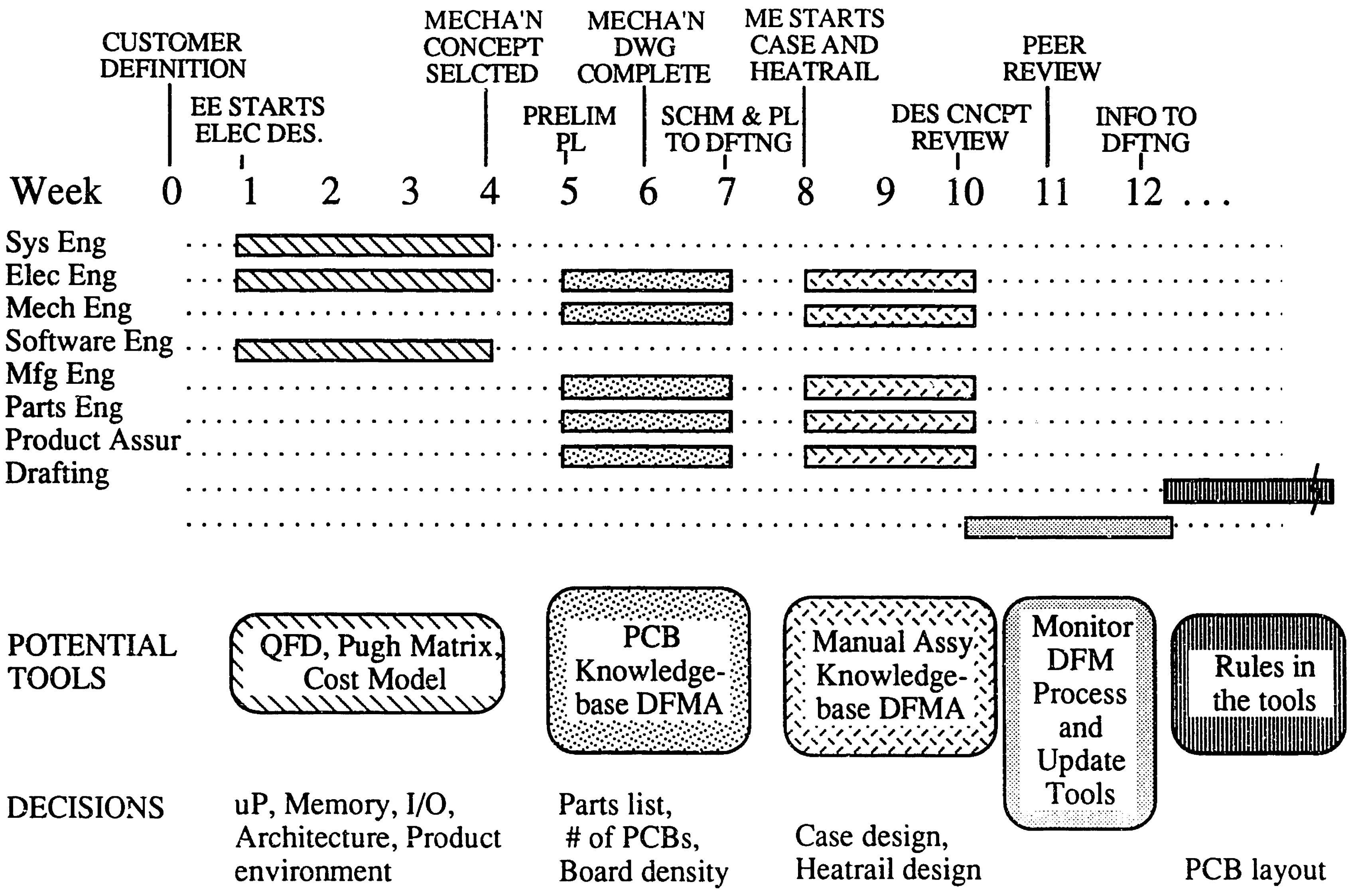


Figure 5.1. A typical design cycle and the design tools pertinent to each stage.

5.1. Design Decisions

The vast majority of the design-related assembly problems listed in Section 3.2 can be traced to two stages in the design process. These stages clearly have a direct impact on a PCB's ease of assembly. They are:

1. part specification and selection, and
2. circuit board layout.

Part specification includes the selection of the part packages and the tolerance of the components. As this task is closely related to the circuit design, these decisions are typically performed by the lead electrical engineer on the design team. The parts-procurement people supply the designers with a list of approved parts, and new parts are selected from part catalogs or through direct communications with the manufacturers of circuit components.

Circuit board layout is typically performed by draftsmen using some form of CAD package. This is the final step in the design as well as the most assembly process specific task. The location of all circuit board parts and runners are defined at this design stage. The CAD tool could be a simple drawing package or a sophisticated rule-based design aid.

Part specification must be performed before PCB layout. In fact the layout designers can be considered a customer of the electrical designers that produce the schematic and part list. The tools that support part specification will be used earlier in the design process, by different design team members, and they will support different types of decisions than the PCB layout tools.

5.2. Making Design Tradeoffs

David Gatenby [12] advocates his Design for "X" (DFX) concept as the key to efficient product design. Process-related design constraints, called *DFX linkages*, define the *design attributes* that, in turn, dictate the *design process activity*, e.g. component placement. (See Fig. 5.2.)

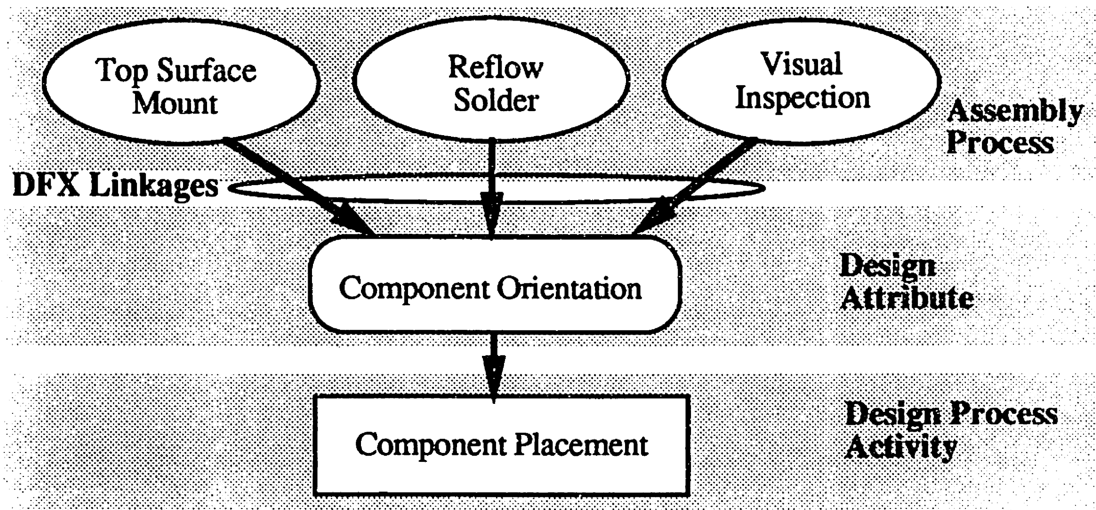


Figure 5.2. Gatenby's DFX concept.

Gatenby points out that the recognition and resolution of DFX trade-offs is one of the biggest challenges that product designers face. These DFX linkages are referred to in this paper as process specific design constraints.

Trade-offs are most easily evaluated when compared on a common scale or metric. The cost($), quality or cycle-time impact of a non-conformance to a design constraints can potentially be used as metrics to evaluate trade-offs that Gatenby refers to.

For example, history shows that boards using J3 connectors, shown in Fig. 3.6, will experience shorts at a rate fifteen times the average leaded component short rate with the standard pad design (shown in Fig. 3.6) and the current wave solder process. If solder thieves are designed into the product, this defect rate would likely be closer to the average

solder short rate for leaded components. From the rework cost estimate described in section 3.2, this corresponds to a cost of 6 cents per board versus 1 cent per board at in-circuit rework. Similarly, each process and part constraint can have an estimated cost of non-conformance based on production experience.

Product Performance in normalized defects per placement	Tp SM	SM IC	HtRail	Stklead	Bt SM	Combined
ECMA	1.0	1.9	5.7	29.0	4.7	4.7
ECMB	2.4	4.6	10.4	27.1	6.0	6.1
ECMC	3.0	5.7	42.6	41.9	9.9	10.2
Combined	2.0	3.9	17.9	33.6	6.3	6.6

Table 5.1. Relative performance of assembly processes.

As a minimum, designers should be aware of which processes (top surface mount versus bottom surface mount, versus leaded assembly) are the most reliable. Table 5.1 shows how the various part/process categories for each product perform relative to the top-surface-mount process for ECMA. Then they can consider assembling the most critical parts, or those invisible to automatic test, using the more reliable processes.

5.3. General Types of Design Tools

The knowledge-based tools referred to in Fig. 5.1 draw on past assembly experience, using similar processes, to aid the designers in predicting assembly performance while the design is still fluid. The BDI toolkit is an example of knowledge-based DFMA tool. It contains an assembly time database that allows it to estimate the the assembly time required to assemble parts with various different attributes. The automatic PCB assembly processes are not understood as well as the manual assembly process, and as a result the DFMA tools for PCB assembly are correspondingly less developed. A knowledge-based PCB tool is discussed later in this chapter.

As a design unfolds, the design decisions, and therefore the tools that support these decisions become more specific to the parts and processes that will be employed on the factory floor. Concept level product specification tools, such as Quality Function Deployment (QFD) [14] and the Pugh selection matrix, can be performed independent of the assembly processes that will ultimately be used to build the product. These tools do not address manufacturability. Knight and Kim [17] differentiate design tools as *domain-dependent* and *domain-independent*. QFD is a domain independent tool because it contains no knowledge of a particular class of problems. Domain independent tools are used to extract and integrate the knowledge and expertise of the group in order to solve the problem at hand. DFMA tools embody knowledge of the processes for which they are designed and, are therefore classified as *domain-dependent* design tools. It is interesting to note that as a design progresses through the design cycle, the appropriate design tool becomes more process specific, i.e., more dependent on the domain of the processes and parts.

As mentioned in Chapter 1, PCBs are built using several different assembly processes, and each process imposes a unique set of constraints on the product. It makes good sense for a DFMA tool to be capable of organizing design constraints by assembly process. For example, the constraint of laying out the bottom SMC chips in a fashion that is easy to inspect is driven by the visual inspection process. Whenever this visual process is used, the layout designer should be made aware of this constraint and how to layout parts for ease of inspection. When the visual inspection task is either automated or eliminated, this constraint should be dropped.

Some design constraints, on the other hand, are better classified by part number as opposed to process step. For example, the design constraint derived from the *missing-crystal* example (see Fig. 3.7) could be classified as a process constraint. Pertaining to the manual

assembly process, this constraint might read; "all leaded component holes should be as small as possible while allowing easy part insertion." This is a rather vague and common-sense constraint. A designer presented with this constraint might quickly confirm that she always does it that way and move on to the next constraint. In this case, much of the lesson learned from previous crystal assembly experience would be lost in a process-wide generalization. Referencing this constraint by the part number of the crystal, on the other hand, would be more useful. Whenever a design that specifies this crystal is presented to the DFMA tool, a flag saying: "use 0.034 inch holes for the active leads and 0.064 inch holes for the case lead" would be presented to the designer.

This part number classification scheme is used to some extent by the Texas Instruments tool. (i.e. a quality/handling flag letter is recorded in a part database and displayed whenever that part is specified in a design). Since most manufacturers use the same electronic and mechanical components across many different products, lessons learned in assembling specific parts are valuable.

5.4. Proposed Dynamic DFMA Method

The requirements, discussed above, for a new PCB DFMA tool are summarized below. A PCB DFMA method should have the capability to:

- capture process constraints as well as lessons-learned based on the specific parts and processes.
- provide pertinent process constraints and lessons-learned to the designers upon input of an initial parts list and process description.
- weight or rank-order design constraints, based on a metric that is important to the manufacture, to aid design tradeoff decisions in the event that all constraints cannot be met simultaneously.

• be updated frequently with most recent production data, part problems and process changes. The time horizon over which process performance data is updated would depend on the variability and the rate of change observed in the process performance.

An example of a tool that might satisfy these requirement is conceptualized in Fig. 5.3.

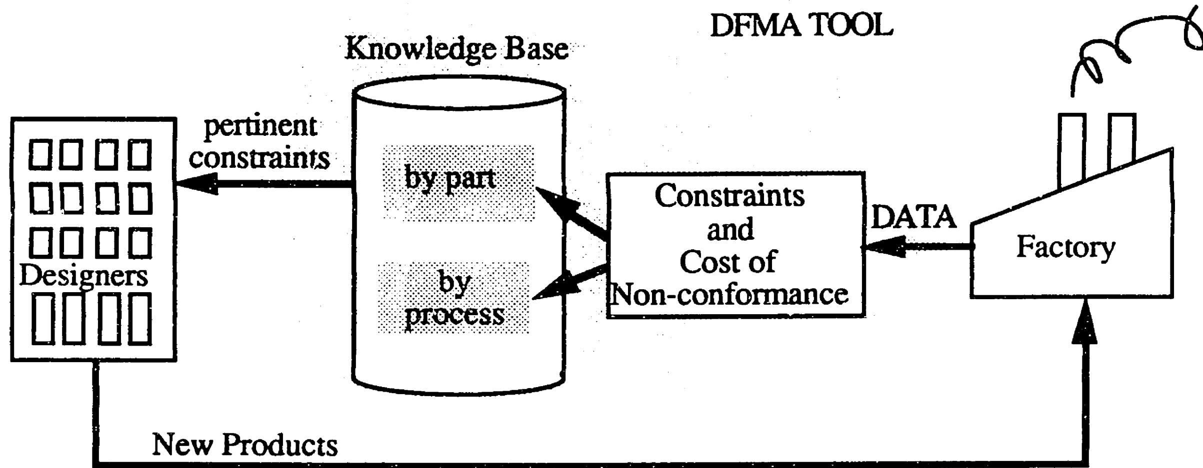


Figure 5.3. A dynamic tool for DFMA of printed circuit board assemblies.

In view of the requirements listed above and the key DFMA-related decisions that the design teams make, the following four pronged approach is recommended for dynamically collecting and communicating design constraints to the product designers:

1. A dynamic design specification organized by assembly process, presented by design activity and linked to the following design tools (items 2 and 4).
2. A knowledge based DFMA tool capable of capturing lessons learned (problem parts) and calculating design performance metrics based on an initial parts list.
3. Boothroyd Dewhurst manual DFMA or an equivalent manual assembly tool for heatrail design and an analysis of the manually inserted components.

4. Rules in the CAD layout tools (tied directly to the design specification of step 1) that flag rule violations and calculate predicted design performance metrics.

The tools listed as items 1, 3 and 4 are discussed briefly below. The knowledge based DFMA tool is the primary focus of this thesis and is discused below in considerably more depth.

5.4.1. Process Oriented Design Specifications

Design specifications are necessary to capture all known design constraints and lay the ground rules for all designers to reference. As shown in Fig. 5.4, the document should be organized by assembly process and present design rules to the designers according to the pertinent design activity. The specification should be updated each time there is an assembly process change or improvement. In addition, the process constraints contained in the design specification should be linked directly to the CAD layout and the part specification tools.

The relative performance of each assembly process and general guidelines for choosing which processes to use for which part types should also be included. For example, parts that are hard to test electrically (i.e., at in-circuit test) should be placed where another form of automatic part verification is performed (e.g., X-ray on top SMCs).

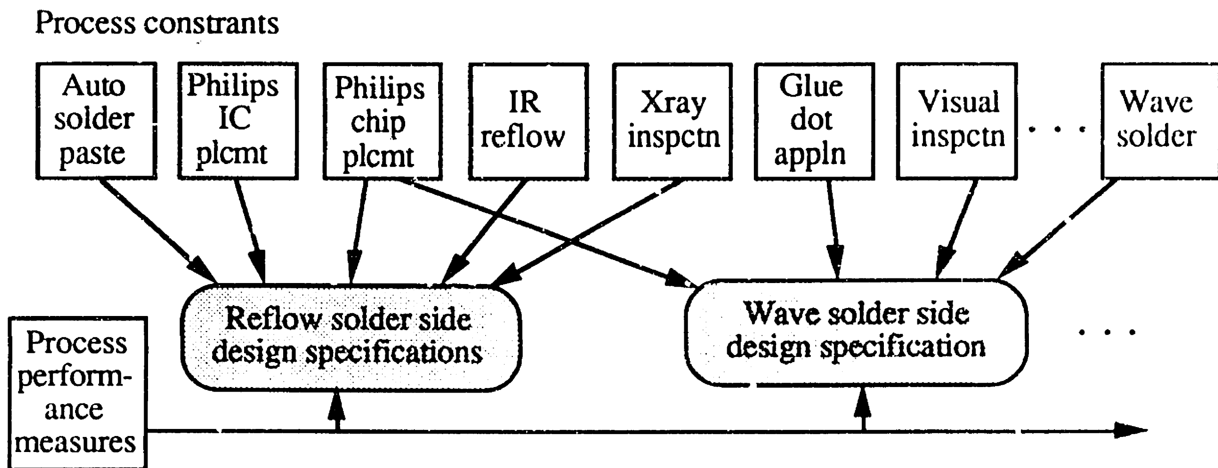


Figure 5.4. Process oriented product design specification.

5.4.2. Knowledge-based PCB DFMA

The goal of this tool is to assist the electrical design engineer in specifying parts and the assembly process used to assemble the parts of a new design. The tool will inform the engineer which components are difficult to assemble or test and allow the evaluation of design tradeoffs. The tool is based on a part and process database that contains lessons-learned and actual process capability measures derived from current PCB assembly operations. Lessons-learned can be captured in the database as numbered problem codes or as simple text records. The designer specifies which parts are to be assembled with which assembly process and the tool lists any problem parts and calculates a complexity metric to predict product performance for comparing different design tradeoffs.

Upon completing a preliminary circuit design (a schematic), the electrical designer would first determine which processes are available to build the product being designed, and then chose an initial list of parts, consistent with these assembly processes. This information would then be fed into the DFMA tool. The DFMA tool would query the design knowledge-base for the pertinent design constraints and lessons learned that have been gathered on these parts and processes and present these constraint to the designers. At this

point in time (when the initial parts list is generated), the circuit design is likely to be fluid enough that changes could be made in response to any problems highlighted by this parts-list DFMA. This process is outlined in Fig. 5.5.

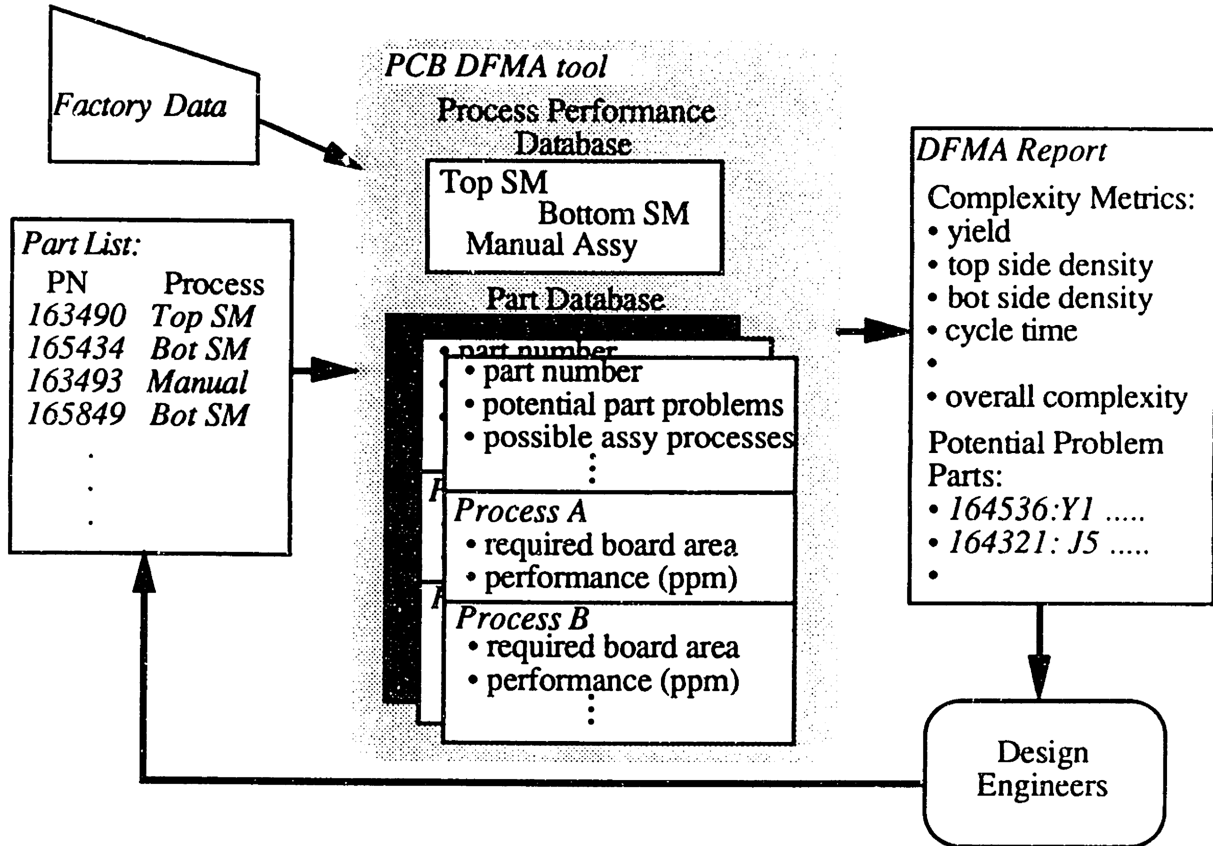


Figure 5.5. Knowledge-based PCB DFMA.

5.4.2.1 *Defining Metrics for Evaluating Design Tradeoffs*

The ultimate goal in designing a product for assembly is to minimize the level of complexity required to implement the desired functional requirements. At the stage in development when DFMA is an issue, product functionality is well defined and most likely no longer a variable. Therefore we can simplify our task to minimizing the manufacturing complexity.

Defining functionality would be valuable in that it would allow us to compare complexity per functionality (complexity normalized for functionality) from one product to the next. For the purposes of this thesis, we wish to optimize specific designs, and therefore, complexity normalization is not necessary. The metrics that we minimize will be relative to the design task at hand and not readily be compared to a standard.

Let us define complexity as the characteristics of a PCB design that make it difficult to assemble. More specifically, complexity refers to those qualities of a PCB design that add cost, increase production or design time, or degrade quality. In order to minimize complexity we must first define it explicitly. After defining complexity we can then attempt to model it as a function of a PCBs design attributes.

Three metrics are chosen for this discussion to capture the basic cost, time and quality elements of complexity:

- Assembly and part cost
- First pass assembly yield
- Production cycle-time

This list is by no means comprehensive. Some manufacturers will want to model other elements of complexity that they consider more important. For example, some manufacturers may assume high first pass yields and short production times and only concentrate on total cost. The BDI manual assembly tool uses total assembly cost, assembly time, the number of operations required and design efficiency (number of parts divided by a theoretical minimum number of parts) to measure complexity. We define complexity as a linear combination of cost, first-pass yield and cycle-time. The coefficients used in the linear combination capture the relative importance of each metric for a given project.

Next we consider which design attributes influence these elements of complexity. There are many potential drivers of complexity including the following:

- d_1– # of manual insertions
- d_2– # of surface mount components
- d_3– # of part types
- d_4– density of top side
- d_5– density of bottom side
- d_6– # of non-standard parts
- d_7– # of parts difficult to test electrically
- d_8– # of parts near the edge of the board

.

.

- d_n–

Then modeling complexity as a function of these drivers might take the form:

$$\begin{bmatrix} w_{11} & w_{12} & \cdots & w_{1n} \\ w_{21} & w_{22} & \cdots & w_{2n} \\ w_{31} & w_{32} & \cdots & w_{3n} \end{bmatrix} \begin{bmatrix} d_1 \\ d_2 \\ \vdots \\ d_n \end{bmatrix} = \begin{bmatrix} \text{cost} \\ \text{1st pass yield} \\ \text{cycle-time} \end{bmatrix}$$

The W matrix is comprised of weighting factors that capture each driver's influence on each complexity metric. Then we would tradeoff cost drivers d_1–d_n to minimize complexity (the linear combination of cost, 1st pass yield and cycle-time) such that all functional design parameters and design constraints are met.

Of course this simple model assumes a linear relationship between complexity and its drivers. Because we are not trying to solve a model for the optimum combination of complexity drivers it is not essential that these functions are linear in form. The complexity drivers are constrained first and foremost by the design requirements. The complexity model is used to compare one design alternative against another; i.e., evaluate tradeoffs.

A well known manufacturer of PCB electronic equipment uses regional surface mount centers to build PCBs for several product development operations. Their most cost competitive surface mount center uses one very simple complexity metric to communicate its process constraints to the product developers at remote sites. The metric is assembly cost, and it is equal to the assembly cost that they charge the product groups for the PCBs they assemble. The equation is very simple: Complexity = Assembly Cost = $0.03(# of SMCs)+$0.50(# of hand insertions)+$2.50(# of hand insertions after wave solder). This cost model sends a clear message to the designers that hand placed components should be avoided unless absolutely necessary. More accurately stated, hand placed components should not be used unless the surface mount alternative part(s) costs more than 50 cents (or $2.50 more if the part cannot be wave soldered). This allows the designers to make an intelligent tradeoff based on the capabilities of the surface mount center.

At DE Powertrain the engineers and management are more concerned with the quality of their PCB assemblies than incrementally reducing cost. Ultimately DE would like to minimize the number of defects found in the field. Modeling field failure rates is beyond the scope of this paper; however, first pass production yield may serve as a reasonable substitute. Given the imperfect nature of production testing, we can argue that if the PCBs are assembled with fewer defects, then fewer assembly defects will be found in the field. Of course assembly defects are only one variety of potential field failures.

First pass assembly yield is the ratio of PCBs that are built with no assembly defects divided by the number of boards built. Because the defect data used to calibrate this yield model was gathered at in-circuit test, this specific model refers to *in-circuit* first pass yield. The model itself can be easily modified to capture other test steps providing that part level defect data is available.

5.4.2.2 Modeling First Pass Assembly Yield

For the purposes of building a yield prediction model, we assume that defects occur independently of each other. It is argued by some that defects in electronic assembly operations tend to be clustered, i.e. not independent.[1] To address this concern we looked at the number of part defects found on each board that failed in-circuit test. Fig. 5.6 shows the frequency distribution of the number of defects found on each board that had at least one defect. Notice that 72% of the boards with defects had only one defect, 95% had 3 or fewer defects. This does not prove independence, however, it does show that there is not a great deal of defect clustering within each PCB.

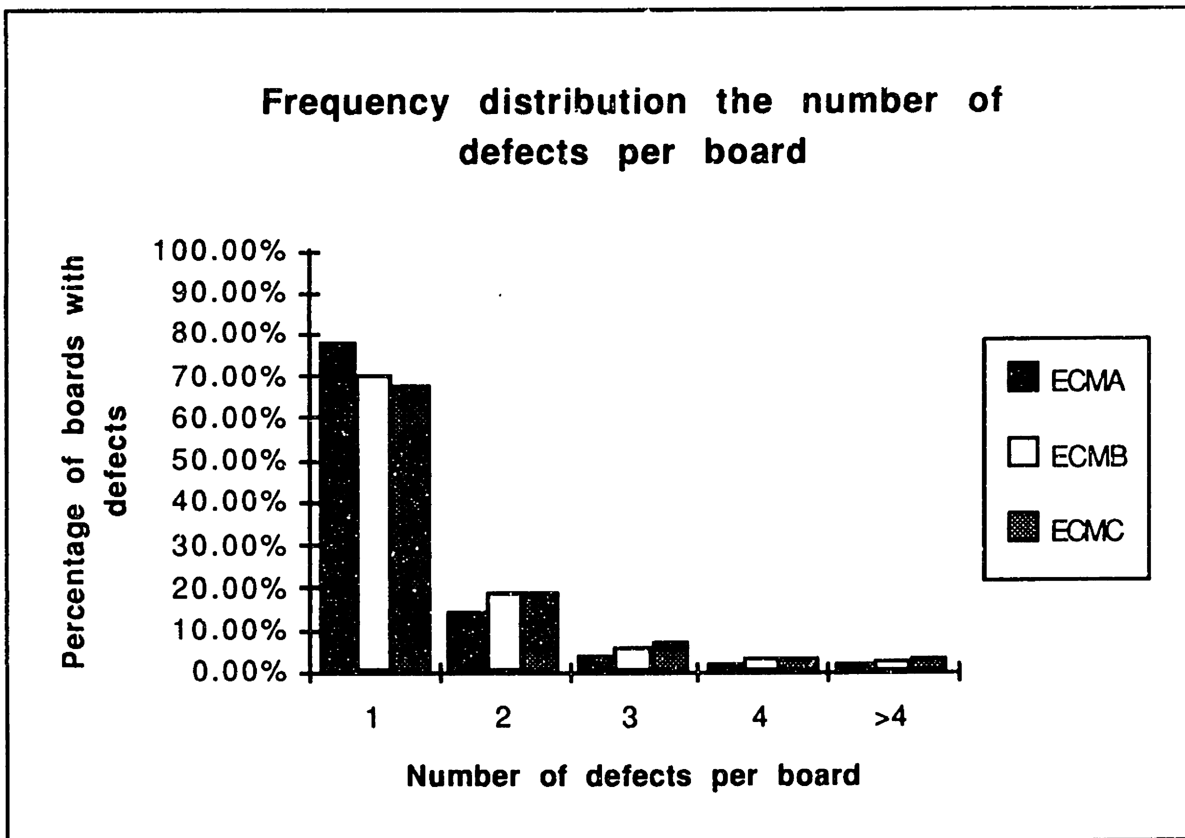


Figure 5.6. The distribution of defects per board for those boards with at least one defect. This graph represents 12,000 repaired boards from the three different PCB assemblies studied.

Using the probability of defect , P, for each product (calculated in the DPP matrix, Table 3.2) and the number of parts on each product, n, (from Table 3.1) we can calculate the expected distribution of defects per board assuming that defects are statistically independent. Table 5.2 was calculated using the binomial probability mass function:

$$p_k(k_0) = \binom{n}{k_0} P^{k_0}(1 - P)^{n-k_0} \quad \text{for } k_0=0,1,2,\cdots,n$$

the probability of k_0 successes in n independent trials. [10]

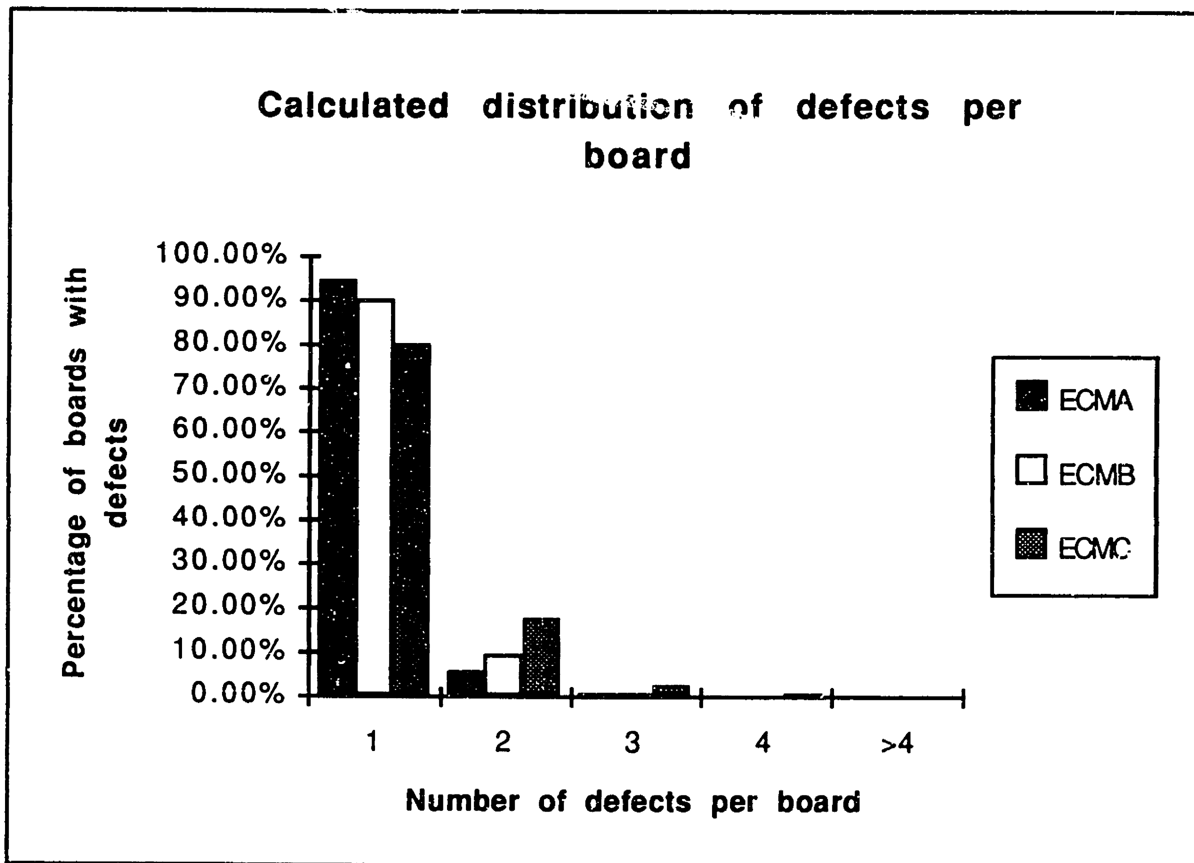


Figure 5.7. The expected distribution of defects per board assuming defects are independent events.

If the actual defects were completely independent of each other, we would expect the distribution in Fig. 5.6 to look more like the steeply falling distributions shown here in Fig. 5.7. Evidently there is some dependence among defect occurrences within each board.

To investigate the notion of independent defects further, we looked at 15 individual PCB assemblies (selected at random, 5 per product type) that had more than 5 defects to see if there was any evidence of clustering among the defects. Table 5.2 shows the results of this analysis. A third of the boards sampled showed no evidence of clustering.

Characterization of the defects found	# of boards
Defects clustered, wave solder problem	3
Defects clustered, missing sticklead parts	3
Defects clustered, bottom placement problem	4
Defects not clustered	5
TOTAL	15

Table 5.2. Results of a 15 board multiple defect analysis.

While the defect events may not be completely independent, we argue that the assumption of independence is not far off base and it greatly simplifies the yield model.

The defect data analysis counted the number of failures in each part/process category and scaled those counts by the number of parts placed, resulting in a defects per million parts placed figure for each part/process category. This is used in the yield model as the probability of a defect occurrence in each part/process category. This assumes that the past performance of one's products and processes are a good estimate of the future performance. Providing that the organization is continually improving its processes and products, past performance data will provide a conservative, or pessimistic estimate of future product yields. Let Ptp, Pic, Phr, Psl and Pbt be the probability of a component defect for the part process categories, top surface-mount, surface mount IC's, heatrail, sticklead and bottom surface-mount respectively.

Assuming independence, the probability of a successful part assembly for a top surface mount part would be: $(1-p_{tp})$, and the probability of successfully placing n top surface mount components is: $(1-p_{tp})^n$. The basic yield model looks like this:

$$\text{Yield} = (1-p_{tp})^{n_{tp}}(1-p_{ic})^{n_{ic}}(1-p_{hr})^{n_{hr}}(1-p_{sl})^{n_{sl}}(1-p_{bt})^{n_{bt}}$$

where:

n_{tp} = the number of top side SCMs specified,
n_{ic} = the number of surface mount integrated circuits specified,
n_{hr} = the number of heatrail components specified,
n_{sl} = the number of sticklead components specified,
n_{bt} = the number of bottom side SMCs specified.

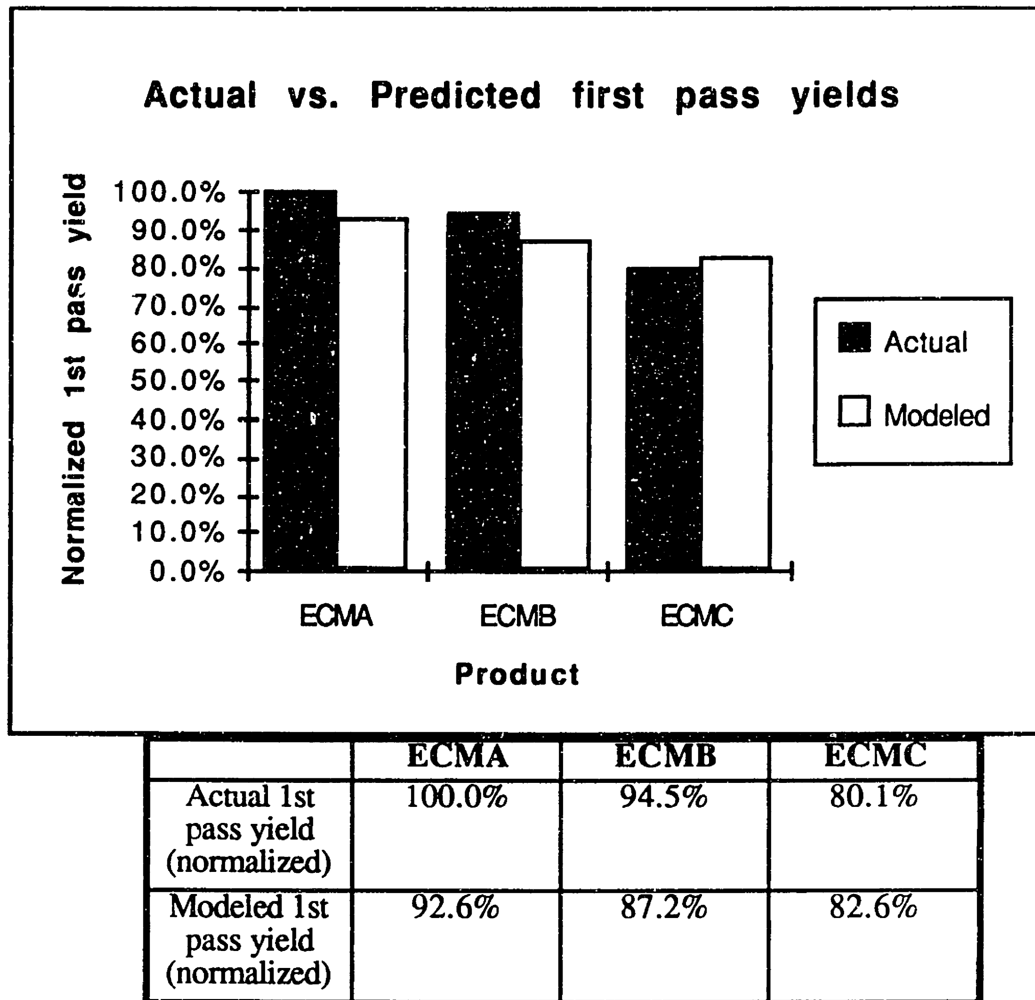
This basic model is useful for making tradeoffs between sticklead and surface mount alternatives. For instance, since p_{sl} is roughly 9 times p_{bt}, it becomes clear to the designer that nine bottom side surface mount components will have a less negative effect on the yield than one sticklead component. Fewer total part count is not always better for the manufacture of PCB assemblies.

Figure 5.8 shows the results of using this basic model on the three products studied and compares the model results to the actual first pass yields. The numbers have been normalized by setting the highest actual yield to 100%.

Because the probability values (p_{tp}, p_{ic}, p_{hr}, p_{sl} and p_{bt}) used in the model were derived from the aggregate defects rates of all three products, we would expect the predicted first pass yields to be pessimistic for the better performing products (ECMA and ECMB) and optimistic for the lower performing product (ECMC). Fig. 5.8 confirms this.

This basic yield model does not take into account the impact of using parts that are difficult to assemble or test and thus does not allow the designer to tradeoff the types and tolerance of the parts that are used. For instance, if this yield model was embedded in the CAD

layout tools, it would be nice to have the capability of modeling the effect of placing chips near the edge of the board or near a screw versus placing them in the middle of the board.



	ECMA	ECMB	ECMC
Actual 1st pass yield (normalized)	100.0%	94.5%	80.1%
Modeled 1st pass yield (normalized)	92.6%	87.2%	82.6%

Figure 5.8. Comparison of calculated and actual first pass yields.

By looking at the past performance of parts that are determined to be harder to assemble we can characterize problem parts or placements and then incorporate them into the model. For example, an analysis of variance on the SMC components on the bottom side of the ECMC product showed that the "0805" chips were 5 times more likely to be missing than the larger "1210" chips. If this were found to be true across several products it might be

worthwhile to break the p_{bt} term into two categories, one for "0805" chips and one for "1210" chips. The

$(1-p_{bt})^{n_{bt}}$ term in the basic yield model would be replaced with the dual term $(1-p_{0805})^{n_{0805}}(1-p_{1210})^{n_{1210}}$. The same analysis of variance showed that parts located near the edge of the board are twice as likely to be missing. If this phenomenon were proven to be true for all defects (not just missing defects) across several products, then it could be incorporated into the yield model used in the PCB layout stage.

By expanding this model to capture all of the major factors that determine the likelihood of a defect, this model should become quite accurate. However, accuracy is not our goal. The goal is to minimize product complexity while satisfying all functional requirements. It is important not to count the same component more than once. The sum of all n's $\left(\sum_i n_i\right)$ must equal the number of parts on the board. This basic model does not allow for inter-related problems such as an 0805 chip located near the edge.

The process of calibrating this model, that is, determining the major drivers of yield loss, teaches us a lot about how to design more robust PCBs. It is conceivable that a $(1-p_f)$ term for each part, based on the history of that part in one's factory, can be maintained in the part database. This part by part data would be very useful in finding trouble parts (e.g., those that received bad from the vendor) and in finding process problems (e.g., unrealistic test limits or part handling problems) as well as predicting first pass yield. However, as part groupings are subdivided into very small groups, the data available for each set of parts becomes smaller and thus the estimate of the defect probability becomes less accurate. The general design guidelines also become harder for the designers to understand as the number of part groupings increase.

When adding terms to the model it is important to consider the behavior you are encouraging. Changing the yield model to favor the bigger 1210s should encourage designers to use more large chips. This may not appear to be a good thing to do even though it does have a positive impact on first pass yield. Adding this term would allow the designer to trade off board area for yield. This assumes that board area constraints are captured in the other complexity metrics. If space is at a premium, then the use of 1210 chips will have a negative effect on the PCB density which may drive the design to two PCBs instead of one and thus add significant cost. Ultimately the cost metric is calculated and displayed in the same DFMA report. It is important that the the designers are aware of the rules that are being used to evaluate their designs and that the report is explicit as to were the big yield and cost liabilities are located.

5.4.3 Rules in the CAD Tools

To address the second major design task, PCB layout, the "rules in the tools" concept is recommended. The main idea of the rules in the tools is that it is easier to design a PCB layout if you are never given undesirable degrees of freedom. When the rules are not embedded in the layout tools, a designer can unknowingly violate a constraint and build on that mistake in his subsequent design choice leading him to a point where either a large part of the design must be redone or a constraint left compromised.

In addition to disallowing constraint violations, the layout tools should be capable of calculating complexity metrics to assist the designer in making design tradeoffs. For example yield is still an important measure of the design complexity. The model for first pass yield would have to modified for the different complexity drivers that the layout designer control. The defect causal analysis performed in Chapter 3 and summarized in Table 3.6 clearly shows that the location of parts on the PCB has a large impact on the likelihood that parts will make it to in-circuit test without defects.

The method defined here is an information system. Implementing this type of system comes with all of the issues and challenges that face any information system implementation. The specific software packages used are less important than the system framework and the organizational changes required to support the system.

6. Conclusions

This thesis has demonstrated that data from current manufacturing operations is valuable in improving the PCB assembly design. It has also described and demonstrated methods for gathering manufacturing defect data and communicating its lessons to the product designers in such a way that new products can benefit more fully from previous product experience.

Design tools capable of matching product designs to any of the vast array of possible process configurations used at an arbitrary manufacturer are not available. It is not clear that these tools, if they did exist, could keep pace with the rapid changes taking place in electronic packaging. With product/process mixes unique to each manufacturer, turnkey tools are unlikely to offer much help. Even solutions that seem to be generic, such as the use of solder thieves for the wave solder process, may be redundant if the wave solder machine is equipped with an air knife, a seemingly subtle change in process capability.

A practical alternative is for each manufacturer to understand its own process capabilities to the extent that new products can be designed to match them. DFMA tools of this nature would have to be capable of capturing and continually updating design constraints and process performance data from several different assembly processes and presenting data pertinent to a particular product design early in the design process.

In order to present this up to date and relevant process constraint data to the designer, one must first learn from the performance of ones own processes and products. Figure 6.1 shows how manufacturing data can be used on three levels.

This DFMA approach is consistent with the General Motors DFM philosophy [13]:

1. Define the envelope of your current process capabilities.
2. Design products within this process envelope.
3. Expand the process envelope through process improvements.

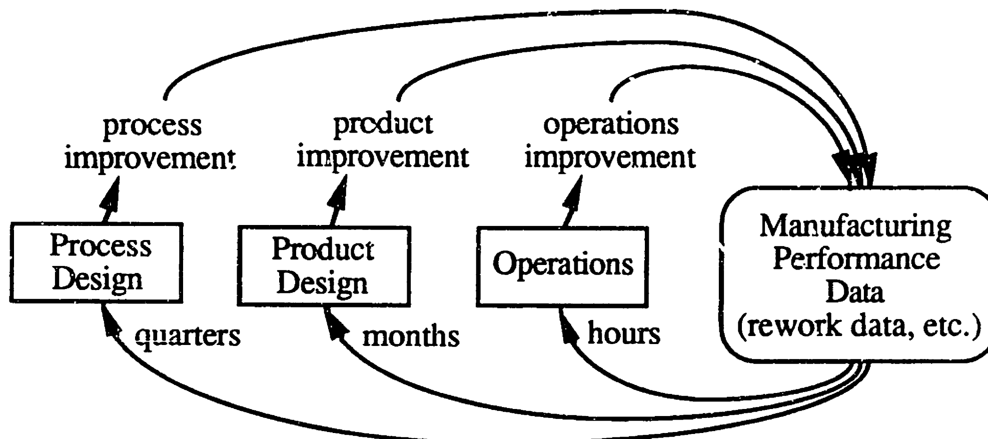


Figure 6.1. Product performance data routed to design.

Fact-based tools like the new tool discussed in this thesis ease negotiations among design team members. As one engineer at DE pointed out, the facts remove all of the emotion and egos from the equation, and allow quick decisions. When presented with the four current assembly problems described in Chapter 3, the DE engineers were quick to respond by establishing a list of lessons learned to be reviewed in the early stages of new product design. Factual data facilitates quick and accurate design decisions.

At some point we stop talking about *DFMA tools*, as such. Once systems are in place to measure and monitor the assembly process performance and feed that information to the new product designers, then a DFMA tool is merely the interface that presents the data to

the designers. The concept of a DFMA tool becomes less important than the implementation of a design process that incorporates DFMA. Designing products that match ones assembly processes is just good design practice and the whole design process is designed with this in mind.

References

[1] Albin, S. and Friedman, D. *Off-line Quality Control in Electronics Assembly: Selecting the Critical Problem*, Rutgers University, June 1991.

[2] Alstott, M. Hewlett Packard, LFM symposium on DFM, MIT, Cambridge MA, October 15, 1991.

[3] Battenberg, J.T. presentation to: The Manufacturing Technology Conference, Warren MI, May 1989.

[4] Boothroyd Dewhurst Inc. and Texas Instruments, Product Design for Manufacturability and Assembly Conference, Newport RI, October 29-39 1991.

[5] Boothroyd, G. and Dewhurst, P. *Product Design for Assembly*, Boothroyd Dewhurst Inc., Wakefield RI, 1989.

[6] Brindley, K. *Newnes Electronic Assembly Handbook*, Oxford:Heinemann Newnes, 1990, p 215.

[7] Carter, M. General Motors DFM Knowledge Center, Warren MI, 1991.

[8] Chevalier, P.B. Optimal Inspection for Circuit Board Assembly, Operations Research Center, MIT, 1991.

[9] Delco Electronics "Automotive Electronics Systems AES Hardware Design Standards", Kokomo IN, 1989.

[10] Drake, A.W. *Fundamentals of Applied Probability Theory*, McGraw-Hill: NY, 1967.

[11] Elliott, D. "How to Avoid Problems with Wave Soldering and IR Reflow," *Surface Mount Technology*, Oct. 1989 p47.

[12] Gatenby, D. "Design for X: Key to Efficient, Profitable Product Realization," *Productivity and Quality Improvement in Electronics Assembly*, Edosomwan and Ballakur, McGraw-Hill, 1988.

[13] General Motors DFM Knowledge Center, *DFM Process Reference Guide,* Warren MI. July 31, 1991.

[14] Hauser, J. and Clausing, D. "The House of Quality," *Harvard Business Review*, Vol 66, Num 3, May-June 1988 pp63-73.

[15] IEEE Staff, "Board Tools Proliferate," *IEEE Spectrum*, Nov. 1990, p82.

[16] Institute for Interconnecting and Packaging Electronic Circuits, IPC-D-275, *Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies*, IPC, Lincolnwood IL, 1991.

[17] Knight T.P. and Kim, S.H. "A Knowledge System for Integrated Product Design," *Journal of Intelligent Manufacturing*, 2, 1991, pp17-25.

[18] Nikkel, R. and Tarr, L. *Comprehensive Producibility Analysis for Printed Wiring Boards*, Hughes Aircraft Corp., El Segundo CA, 1991.

[19] Noble, P.J.W. *Printed Circuit Board Assembly - the complete works*, Open University Press, 1989.

[20] Sharp, B. "Zen Masters", *HP Professional*, Nov. 1991, p28.

[21] Shina, S.G. *Concurrent Engineering and Design for Manufacture of Electronic Products*, New York: Van Nostrand Reinhold, 1991.

[22] Soederberg, E.M. *Boothroyd Dewhurst DFMA at Delco Electronic*, Delco Electronics, Kokomo IN, 1991.

[23] Suh, Nam P. *The Principles of Design*, Oxford University Press, New York, 1990.

[24] Wagner, J. and Young, J. *Activity Based Costing Analysis*, Delco Electronics, Kokomo IN, 1990.

Appendix A. Analysis of Variance–Missing Bottom Side Chips

The "missing component" defect data for the ECMC product was categorized by four attributes:

- Orientation–whether the SMC was placed on the board in the same direction in which it was fed to the placement machine, or it is turned 90 degrees.
- Size–three different SMC chip package sizes are placed on the bottom side of the printed circuit boards (in increasing order of size: 0805, 1206, and 1210).
- Type–resistor of capacitor (R or C respectively).
- Location–broken into four zones as shown in Fig. A1.

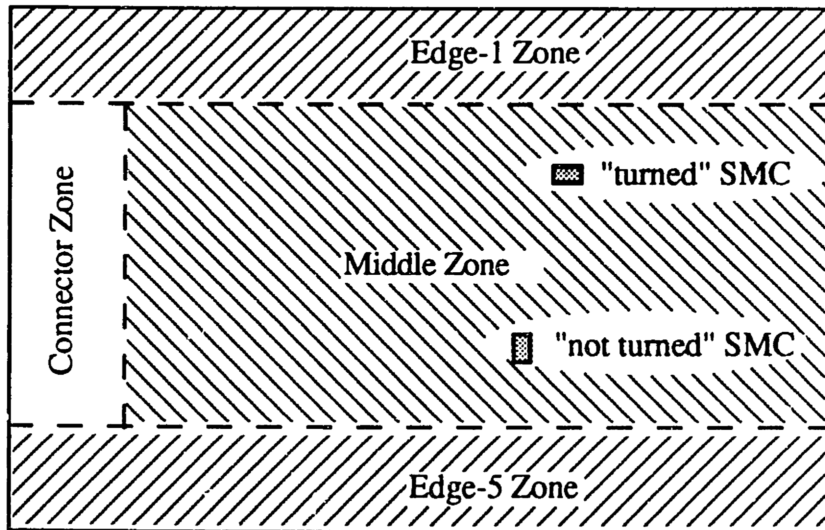


Figure A1. SMC location and orientation on the bottom side of the ECMC product.

The response variable "missing-chip ratio" is simply the number of chips reported missing during the two month data collection period divided by the number of chips of the particular orientation, size, type, and location (the number of failure opportunities). The data used for this analysis is presented in Table A1. Thirteen of the forty possible data points had no opportunities for failure, e.g. there are no 0805, turned, resistors in the connector zone.

Orientation	Size	Type	Location *(see fig. A1)*	Missing-Chip Ratio
Turned	"0805"	Resistor	Middle	3.36
Turned	"0805"	Resistor	EdgeFive	9.57
Turned	"0805"	Resistor	Connector	no data
Turned	"0805"	Resistor	EdgeOne	6.5
Turned	"0805"	Capacitor	Middle	2.11
Turned	"0805"	Capacitor	EdgeFive	6.75
Turned	"0805"	Capacitor	Connector	4.57
Turned	"0805"	Capacitor	EdgeOne	1.5
Turned	"1206"	Resistor	Middle	2.25
Turned	"1206"	Resistor	EdgeFive	no data
Turned	"1206"	Resistor	Connector	2.25
Turned	"1206"	Resistor	EdgeOne	no data
Turned	"1206"	Capacitor	Middle	1.43
Turned	"1206"	Capacitor	EdgeFive	3
Turned	"1206"	Capacitor	Connector	1.33
Turned	"1206"	Capacitor	EdgeOne	no data
Turned	"1210"	Resistor	Middle	0.67
Turned	"1210"	Resistor	EdgeFive	0
Turned	"1210"	Resistor	Connector	no data
Turned	"1210"	Resistor	EdgeOne	no data
NotTurned	"0805"	Resistor	Middle	3.6
NotTurned	"0805"	Resistor	EdgeFive	13.3
NotTurned	"0805"	Resistor	Connector	no data
NotTurned	"0805"	Resistor	EdgeOne	7.31
NotTurned	"0805"	Capacitor	Middle	7.35
NotTurned	"0805"	Capacitor	EdgeFive	no data
NotTurned	"0805"	Capacitor	Connector	no data
NotTurned	"0805"	Capacitor	EdgeOne	6.82
NotTurned	"1206"	Resistor	Middle	0.5
NotTurned	"1206"	Resistor	EdgeFive	no data
NotTurned	"1206"	Resistor	Connector	no data
NotTurned	"1206"	Resistor	EdgeOne	3
NotTurned	"1206"	Capacitor	Middle	1
NotTurned	"1206"	Capacitor	EdgeFive	5
NotTurned	"1206"	Capacitor	Connector	no data
NotTurned	"1206"	Capacitor	EdgeOne	0
NotTurned	"1210"	Resistor	Middle	0.29
NotTurned	"1210"	Resistor	EdgeFive	1.33
NotTurned	"1210"	Resistor	Connector	no data
NotTurned	"1210"	Resistor	EdgeOne	1

Table A1. Missing chip data broken into 40 experiments.

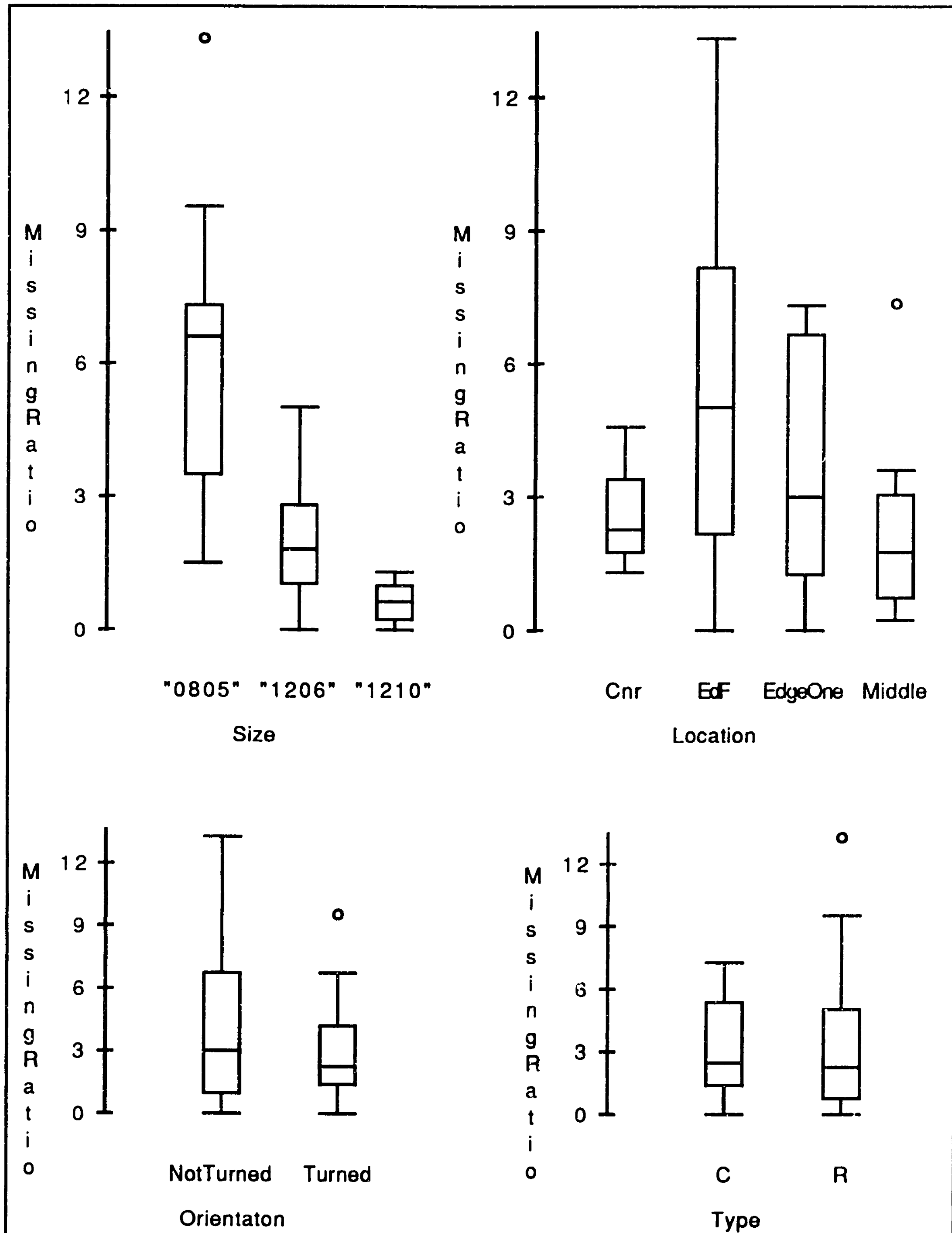


Figure A2. Boxplots of the raw "missing component" data.

The raw data, shown in Fig. A2, suggests that both size and location play a significant role in the missing-chip ratio. However these plots do not take into account the potential interaction between the four control variables; size, location orientation and type. An Analysis of Variance (ANOVA) showing all main effects and two-way interactions was calculated and is shown below in Table A2.

Analysis of Variance For Missing-Chip Ratio:
40 total cases of which 13 are missing

Source	df	Sum of Squares	Mean Square	F-ratio	Prob
Orn	*1*	*0.637159*	*0.637159*	*0.53607*	*0.5402*
Siz	2	45.0883	22.5441	18.968	0.0501
Orn*Siz	2	12.3497	6.17486	5.1952	0.1614
Typ	1	3.15544	3.15544	2.6548	0.2448
Orn*Typ	1	10.4151	10.4151	8.7627	0.0977
*Siz*Typ*	*2*	*2.07379*	*1.03690*	*0.87239*	*0.5341*
Lcn	3	38.6588	12.8863	10.842	0.0856
*Orn*Lcn*	*3*	*3.66539*	*1.22180*	*1.0280*	*0.5276*
Siz*Lcn	6	33.1953	5.53254	4.6548	0.1874
Typ*Lcn	3	15.7539	5.25129	4.4182	0.1901
Error	2	2.37713	1.18857		
Total	26	283.744			

Table A2. Analysis of variance for all main effects and 2-way interactions.

The three effects least likely to impact the Missing Ratio (shown in *italic* above) were removed and the analysis was repeated. This allows more degrees of freedom to estimate error and thus more accurate results.

Analysis of Variance For Missing-Chip Ratio:
40 total cases of which 13 are missing

Source	df	Sum of Squares	Mean Square	F-ratio	Prob
Siz	2	49.7419	24.8709	10.941	0.0051
Orn*Siz	2	19.6186	9.80929	4.3151	0.0536
Typ	1	5.91683	5.91683	2.6028	0.1453
Orn*Typ	1	4.71098	4.71098	2.0724	0.1879
Lcn	3	29.8397	9 94656	4.3755	0.0422
Siz*Lcn	6	31.9613	5.32689	2.3433	0.1316
Typ*Lcn	3	14.5265	4.84215	2.1301	0.1746
Error	8	18.1858	2.27322		
Total	26	283.744			

Table A3. Analysis of variance for the seven most significant effects.

Here we can say with 99% confidence that the missing-chip ratio for different size chips are different. In other words the *size* of a SMC part has an effect on the likelihood of it being found missing from the bottom side of the ECMC product at in-circuit test.

Similarly, we can say with 95% confidence that the missing-chip ratio for chips located on different parts of the board are different.

Just as importantly, the orientation and the type (resistor vs. capacitor) of SMC do not have a strong impact on the missing-chip ratio.