GERMANIUM-ON-SILICON VIRTUAL SUBSTRATE FOR LATERAL MULTIJUNCTION PHOTOVOLTAICS

By

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ABSTRACT

Lateral multijunction photovoltaics based on III-V direct band gap semiconductors enable efficient energy conversion. However, lattice matching between cell and substrate requires the use of expensive Ge or III-V substrates, which limits widespread application of III-V solar cells. Cost reduction can be achieved by using Ge-on-Si virtual substrate where a thin layer of Ge is grown on relatively inexpensive Si substrates, thanks to the greater material abundance and larger wafer diameters of Si. However, the lattice mismatch between Si and Ge can bring about threading dislocations that can significantly impair the efficiency of solar cells. This thesis presents patterned epitaxial growth of pure Ge on Si wafer through ultra-high vacuum chemical vapor deposition that achieves low threading dislocation density. This unlocks the potential for growing lattice-matched III-V photovoltaics of high quality on top of the virtual substrate. In addition, this thesis seeks to understand the mechanisms behind trapping of dislocations. The dislocation studies in this thesis not only shed light on dislocation motion in the Ge-on-Si epitaxy, but can be applied to other lattice mismatched materials systems as well. Lastly, the potential of lateral multijunction photovoltaics is demonstrated through simulation approaches.

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LIST OF SYMBOLS AND ABBREVIATIONS

Ge	germanium
Si	silicon
GaAs	gallium arsenide
InGaP	indium gallium phosphide
TD	threading dislocation
TDD	threading dislocation density
SiO_2	silicon dioxide
TEM	transmission electron microscopy
EPD	etch pit density
CVD	chemical vapor deposition
CTE or α	coefficient of thermal expansion
CMP	chemical mechanical polishing
FCC	face-centered cubic
G	shear modulus
V_P	Peierls potential
CDN	confined dislocation network
F_I	image force
F_L	line tension
UHVCVD	ultra-high vacuum chemical vapor deposition
SEM	scanning electron microscopy
PV	photovoltaics
InGaAs	indium gallium arsenide
InP	indium phosphide

SE	spectral efficiency
EQE	external quantum efficiency
CPV	concentrator photovoltaics
EA	electroabsorption

CHAPTER 1

INTRODUCTION

Despite their high performance and wide usage in space applications, III-V solar cells are far from penetrating mainstream photovoltaic markets, as a result of their high costs. The largest single cost in manufacturing lattice-matched InGaP/GaAs/Ge triple junction solar cells comes from the Ge substrate,[1] as shown in Figure 1.1. Heteroepitaxial growth of Ge film on Si wafers offers a promising path to reduce manufacturing costs of photovoltaic devices by providing a virtual substrate that is lattice matched to III-V semiconductors, thanks to Si's greater material abundance and larger wafer diameter. Besides photovoltaics, Ge has become an interesting candidate for electroabsorption (EA) modulator devices and laser diodes due to its pseudo-direct gap behavior and ease of integration into standard Si CMOS processing.[2–6] The main challenge for Ge growth on Si wafers is the ~4% lattice mismatch. For heteroepitaxial layers grown beyond a critical thickness, lattice mismatch leads to misfit dislocations at the film/substrate interface. Threading dislocations accompany the formation of misfit dislocations due to the constraint that dislocations can only terminate at free surfaces or other defects. Threading dislocations in the Ge epilayer can find their way into the device active region, thereby degrading device performance.[7,8] The threading dislocation density (TDD) in blanket Ge-on-Si film is on the order of 10^8 cm^{-2} or higher. TDD was found to be insignificant for device performance at a magnitude of 10^6 cm^{-2} or lower.[7–9] To address this problem, various paths have been explored for reducing TDD, including compositional grading,[10] cyclic annealing,[11] selective area epitaxy,[12,13] 3D heteroepitaxy,[14] self-assembling nanovoids,[15] etc. These approaches will be discussed in Chapter 2.

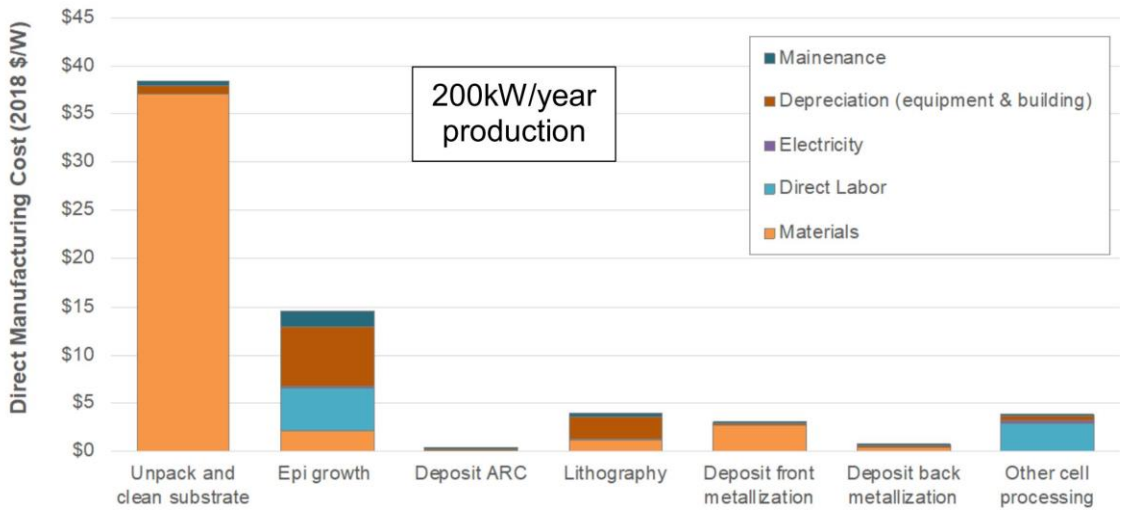

Figure 1.1: Manufacturing cost breakdown for InGaP/GaAs/Ge solar cell[1]

The motivation of this thesis is to lower the costs of III-V photovoltaics, focusing on the semiconductor substrate used to grow the solar cells. **This thesis is organized as follows:**

- Chapter 2 reviews epitaxy and dislocations as well as previous efforts from literature to reduce the TDD in Ge-on-Si epitaxial films.

- Chapter 3 explores two leading thesis questions:

1) Is there an interface between high and low temperature Ge?

2) Does the trench in Si have an influence on dislocations?

In an effort to answer these questions, a process flow that achieved significant TDD reduction as well as transmission electron microscopy (TEM) studies of dislocations are demonstrated. A fishbone diagram to track down the mechanisms behind TDD reduction is given in Figure 1.2.

- Chapter 4 introduces the concept of lateral multijunction photovoltaics and presents projection of their performance using simulation approaches.

- The thesis concludes in Chapter 5 with a summary of the work presented and discussion of future work on Ge-on-Si heteroepitaxy to elucidate the dislocation trapping mechanism and achieve cost-effective Ge-on-Si virtual substrate of low TDD for photonic devices.

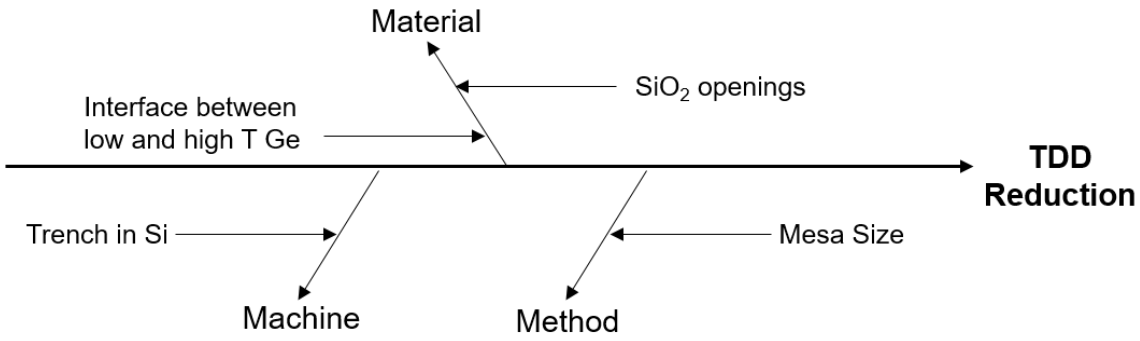

Figure 1.2: Fishbone diagram to track down the mechanisms behind TDD reduction

CHAPTER 2

BACKGROUND

Developing inexpensive, high performance epitaxial devices provides an attractive solution for a wide range of applications, including communications, electronics, energy, photonics, etc. The last decade has witnessed substantial improvement in various technologies based on mismatched heteroepitaxial materials. For example, heteroepitaxy of Ge on Si is a critical research topic to photodetectors,[16] lasers,[2] EA modulators,[6] etc. Additionally, heteroepitaxy of Ge on Si can provide a virtual substrate for III-V photovoltaics, thanks to very similar lattice constants of Ge, GaAs and InGaP, as shown in Figure 2.1.

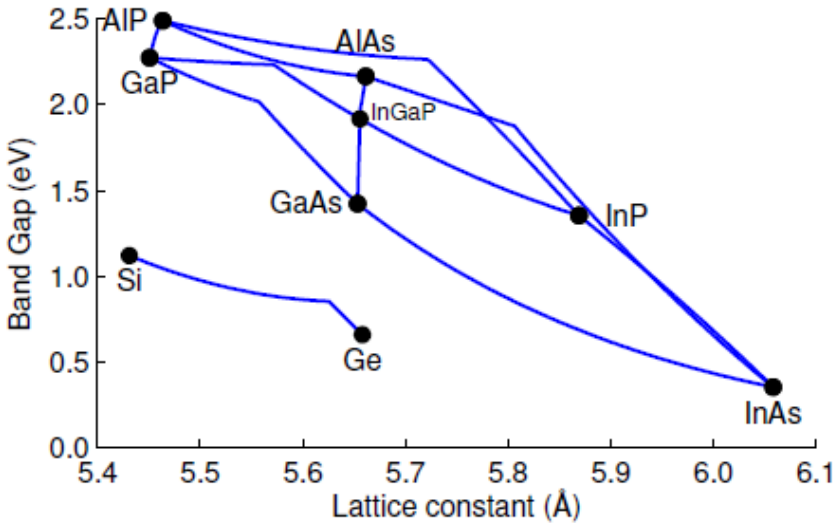

Figure 2.1: Band gap vs. lattice constant for Ge_xSi_{1-x} and III-V compounds. After Albert et al.[17]

2.1 Epitaxy and Dislocations

Epitaxy refers to deposition or growth of one crystal atop another forming a common interface. Homoepitaxy involves only one material, namely to deposit the same

material that the substrate is made of. In heteroepitaxy, a crystal grows on a substrate that is made of a distinct material. In homoepitaxy or heteroepitaxy where the materials have the same crystal structure and similar lattice constants, it is not difficult to register one-to-one lattice correspondence across the interface, as shown in Figure 2.2a. In most cases, however, different materials have different lattice constants. The orientation of the new crystalline layer is defined by the substrate. Initially, the new crystalline layer tries to maintain the one-to-one lattice registry across the interface. As the film continues to adopt the substrate's horizontal lattice with its lattice constant in the vertical direction being relaxed, it will remain biaxially strained by the substrate, as shown in Figure 2.2b. When the system accumulates enough strain energy (the film reaches the critical thickness), growth of defect-free epitaxial film can no longer be sustained. The film will relieve this energy through the formation of misfit dislocations at the interface. The misfit strain (ε_{misfit}) is defined in the following, where a is the lattice constant:

$$\varepsilon_{misfit} = \frac{a_{substrate} - a_{film}}{a_{substrate}}$$

Dislocations are line defects that can be characterized by two quantities: line direction and Burgers vector. Since dislocations need not be straight and can meander through a crystal, the line direction can vary continuously with position and is always tangent to the dislocation. The Burgers vector describes the lattice displacement from an ideal crystal. If line direction and Burgers vector are perpendicular, the dislocation has edge character. If line direction and Burgers vector are parallel, the dislocation has screw character. If line direction and Burgers vector are neither perpendicular nor parallel, the dislocation is part edge and part screw. The cross product of the line direction and Burgers vector defines the normal direction of a dislocation's glide plane (or slip plane). When a dislocation moves in this plane, it is said to *glide*. If a dislocation moves out of the glide plane, it is said to *climb*. The glide plane is not defined for perfect screw dislocations, which means they can glide on any plane and there is no such thing as climb of pure screw

dislocations. In order for them to move to other glide planes, they *cross slip*. Glide and cross slip are conservative because movement occurs by local adjustment of atom positions and reconstruction of bonds, hence no atoms are added or subtracted. Climb is non-conservative and can only take place if atoms are carried to or away from the dislocation, which requires diffusion of point defects. The principal role of climb is to provide a mechanism for dislocations to bypass microstructural barriers by changing slip planes.[18]

Dislocations cannot end abruptly inside a crystal without joining another defect. They can terminate at free surfaces, grain boundaries or on other dislocations (including themselves, thereby forming dislocation loops). Therefore for each misfit dislocation, unless it extends across the entire length of the substrate/film interface, there will be two threading dislocations at the ends of the misfit that extend to the surface or the ends of the two threading dislocations join and form a loop. As byproduct of misfit dislocations, threading dislocations have deleterious effects on electronic devices because they impair carrier mobility, carrier lifetime and device reliability. It is critical to keep the threading dislocation density (TDD) in the surface layer at a low level. The acceptable TDD depends on the application.

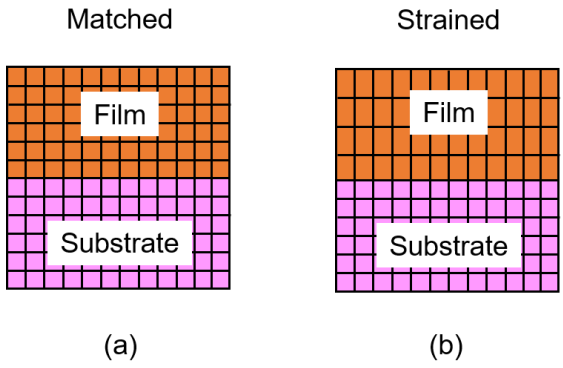

Figure 2.2: Perfect lattice registry between film and substrate in (a) lattice matched system and (b) lattice mismatched system

Dislocation density can be measured in various ways. One of the earliest approaches is to count the number of dislocation lines crossing unit area. Dislocations can

be revealed by chemical etching as etch pits because the spot where a dislocation emerges onto a free surface etches more easily than an area of perfect crystal structure. This method is called etch pit density (EPD) measurement.

2.2 Epitaxial Growth of Ge on Si

Normally there are three modes in epitaxial growth: 2D layer-by-layer growth, 3D island growth and layer-by-layer plus island growth (also called Stranski–Krastanov growth), as shown in Figure 2.3. In lattice-matched systems, the epitaxial film grows in either layer-by-layer mode or island growth mode. The layer will wet the surface if the substrate surface energy is lower than the sum of the surface and interface energy; in the opposite case, islands will form. In systems with significant lattice mismatch and a small interface energy, the growth mode may transit from layer-to-layer to island growth. Growth can occur layer-by-layer early on due to the small interface energy. As the epitaxial film grows thicker, strain energy builds up, triggering island formation to lower the energy. Island growth is not ideal because it results in a rough surface. One of the most important deposition techniques for epitaxial growth of Ge on Si is chemical vapor deposition (CVD). The CVD technique uses gas sources such as GeH_4, SiH_4, Si_2H_6 or $SiCl_2H_2$ for pyrolysis of the precursor gases at elevated temperatures.[19]

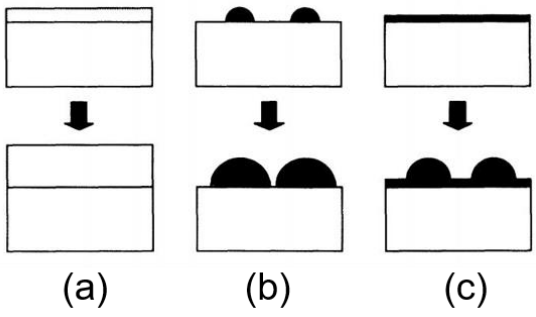

Figure 2.3: Schematic diagram of three growth modes: (a) 2D layer-by-layer growth (b) 3D island growth (c) layer-by-layer plus island growth. After Eaglesham and Cerullo.[20]

Ge is an elemental semiconductor with a lattice constant of 5.6579 Å, approximately 4.2% larger than that of Si. Additionally, Ge has a 10% lower surface energy than Si. By virtue of Ge's larger lattice constant and lower surface energy, the epitaxial growth of Ge on Si can be described as the Stranski–Krastanov growth mode: the epitaxial film initially grows layer by layer and island formation occurs after the film reaches the critical thickness which is estimated to be only a few atomic layers.[21] In order to avoid surface roughness, island formation can be suppressed by reducing atomic surface migration length. The shortened diffusion length can hinder the mass transport that is essential to form islands. The diffusion length of Ge atoms can be reduced by using a low growth temperature. Low temperature and high temperature *two-step growth* of Ge on Si is a practical approach to achieve high quality Ge films. In this method, the first step is growing a thin (30-50 nm) pure Ge buffer layer in the low temperature regime (300-400℃) to avoid island growth by limiting the mobility of Ge adatoms.[19] The second step is growing a thick film in the high temperature regime (600-800℃) for faster deposition rate and lower point defect concentrations.

Normally the two-step growth is combined with *post-growth cyclic annealing* to realize low TDD. Cyclic annealing provides a resolved shear stress on dislocations as a result of the mismatch in coefficient of thermal expansion (CTE) between Ge ($\alpha \approx 5.9\times10^{-6}$/K) and Si ($\alpha \approx 2.6\times10^{-6}$/K). In response to the thermal stress, dislocations can potentially react with each other, leading to TDD reduction. The mechanism will be discussed in detail in Chapter 2.3.2. Luan et al.[12] reported their results from the Ge epilayer deposited using the two-step growth technique followed by cyclic annealing. After deposition of 30 nm of Ge buffer layer, the furnace temperature was increased to 600℃ and 1 μm of Ge was deposited atop the buffer layer. Finally, the samples were cyclic annealed between 900℃ and 780℃ for 10 cycles, which was the optimized annealing condition that led to a TDD of 2.3×10^{7} cm^{-2}.

Compositional grading is another growth technique to realize high quality Ge films. In this approach, the Ge concentration is increased at a certain rate to gradually introduce the 4.2% lattice mismatch between pure Si and pure Ge. As the first lattice-mismatched layer is deposited and relaxed, new dislocations need not be introduced for subsequent layers to relax the strain because the threading segments in the precedent layer are available to continue as misfits at the newest film interface, as shown in Figure 2.4.[22] Starting with pure Si and grading at a rate of 10% Ge per micron to the final composition of pure Ge, TDD of 2.1×10^{6} cm^{-2} is achieved through reuse of dislocations in each layer and hence suppression of additional dislocation nucleation. The drawback of this approach is a total epitaxial thickness beyond 10 microns and a chemical mechanical polishing (CMP) step to remove surface crosshatch which originates from inhomogeneous strain fields in the epilayer.[23]

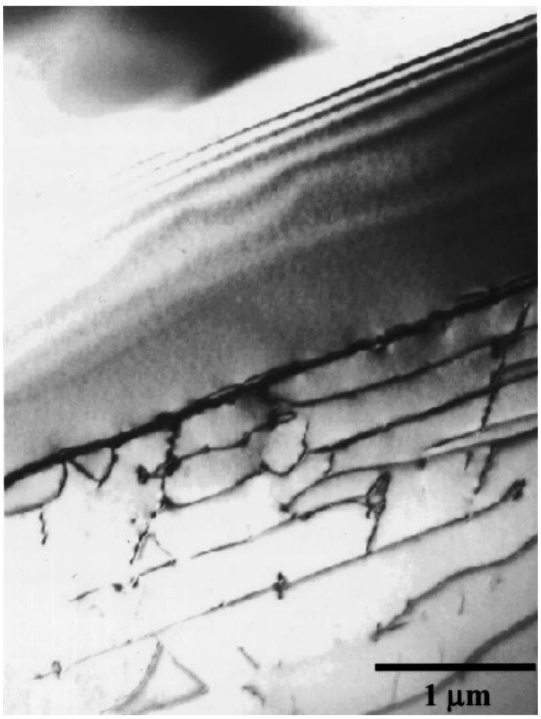

Figure 2.4: Cross-sectional TEM of SiGe layer at a grading rate of 10% Ge per micron from 0 to 100% Ge. Misfit dislocations are vertically distributed throughout the structure, reducing TDD to 2.1×10^{6} cm^{-2}. After Currie et al.[24]

The aforementioned approaches focus on Ge deposition on unmasked or unpatterned Si wafers. In the last decade, photolithography has spurred substantial progress in defect control by suitable pattern design, which will be discussed in Chapter 2.3 after review of dislocations and their reaction mechanisms in diamond cubic crystals.

2.3 Threading Dislocation Density Reduction

2.3.1 Dislocations in Diamond Cubic Crystals

Si and Ge crystallize in the diamond cubic structure that consists of two interwoven face-centered cubic (FCC) lattices. As expected from their FCC translation symmetry, diamond cubic crystals slip on {111} planes in <110> directions. Figure 2.5 shows the crystallography of the {111} <110> slip system in the diamond cubic structure, where basic dislocation types include:[25]

(a) Edge dislocation with line direction $\overrightarrow{BD} = [\bar{1}\bar{1}2]$ and Burgers vector $\overrightarrow{EB} = \frac{1}{2}[\bar{1}10]$

(b) Screw dislocation with line direction $\overrightarrow{FE} = [1\bar{1}0]$ and Burgers vector $\overrightarrow{AG} = \frac{1}{2}[1\bar{1}0]$

(c) 60° dislocation, where line direction $\overrightarrow{FE} = [1\bar{1}0]$ and Burgers vector $\overrightarrow{FA} = \frac{1}{2}[0\bar{1}1]$ make a 60° angle.

According to Kvam et al.,[26] at >2% lattice mismatch, misfit dislocations are observed to be predominantly of pure edge character.

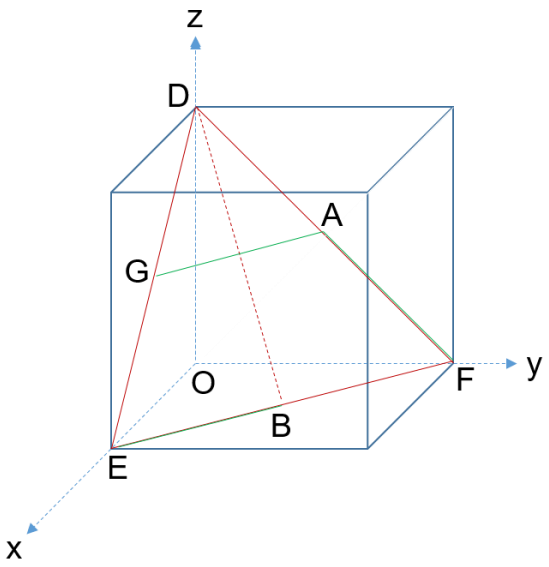

Figure 2.5: Schematic showing different types of dislocation in a diamond cubic crystal. DEF is the (111) slip plane.

A minimum shear stress must be applied to a dislocation before it begins to move, which is called the Peierls stress. The magnitude of the Peierls stress measures the ability of the lattice to resist dislocation motion and is determined by the bonding of the crystal. In covalently bonded solids such as Si and Ge, the Peierls stress ranges from 0.1 to 1G (G is the shear modulus), compared to 10^{-5}G in FCC metals.[27] Due to the crystal periodicity, the Peierls stress can be described as a series of potential energy barriers separated by valleys, as shown in Figure 2.6.[28] In diamond cubic crystals where the Peierls stress is high, the motion of dislocations is controlled by both the direction and magnitude of the applied stress as well as by the rate of nucleation and propagation of kinks.[29] A kink is a short break in the dislocation line which lies in the slip plane. Under thermal fluctuations, part of the dislocation can bulge over the Peierls potential, creating a kink pair. Kinks allow dislocations to move from one energy valley to the next one in small segments, instead of moving the entire line at once. In bulk materials and buried epilayers, kink nucleation must happen in pairs to maintain the continuity of the dislocation line (Figure 2.7a).[30] In the case of thin uncapped epilayers, however, single-kink nucleation is possible

at the epilayer/free surface interface, with a nucleation energy approximately half that of the kink pair (Figure 2.7b). As the epilayer gets thicker, conventional kink pair nucleation will increasingly dominate.[31]

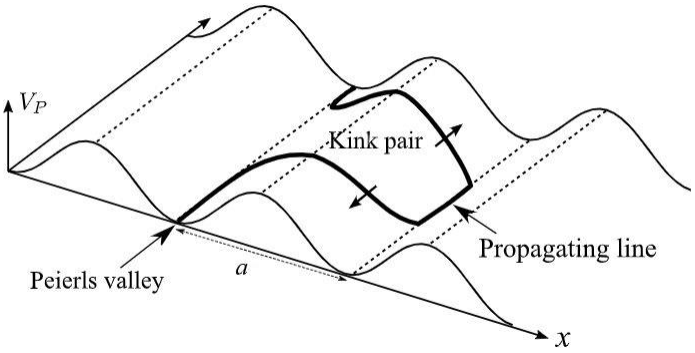

Figure 2.6: Schematic of a dislocation overcoming the Peierls potential (V_P) via propagation of a kink pair. a is lattice constant. After Kraych et al.[28]

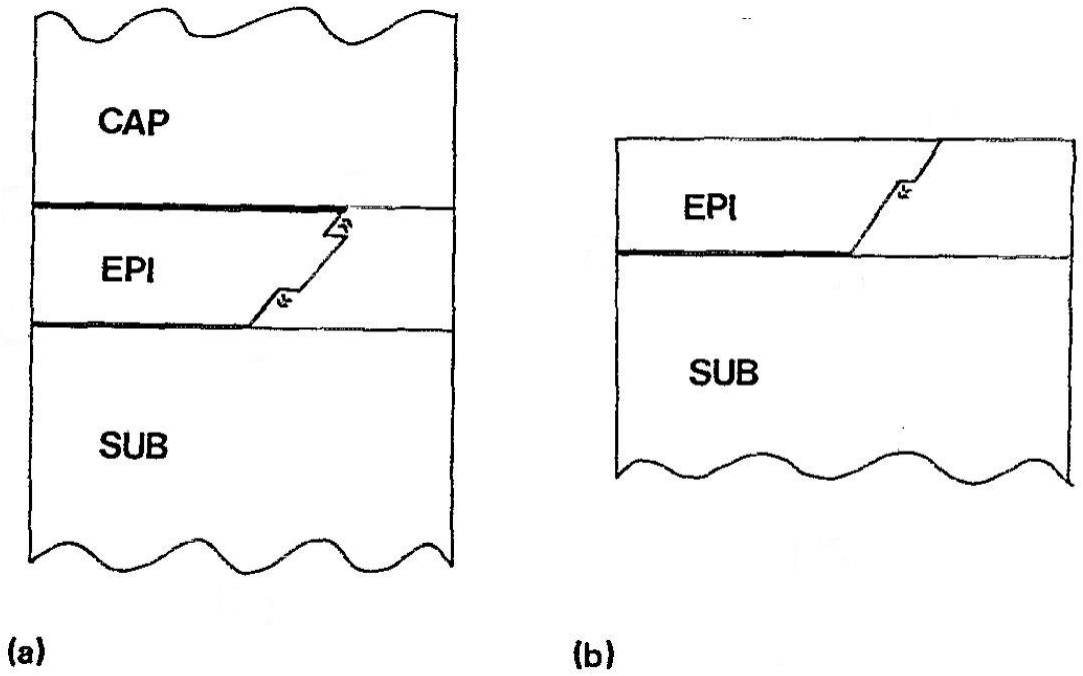

Figure 2.7: (a) For buried epilayers, kink pair mode must operate (b) for thin uncapped epilayers, single kinks may nucleate at the free surface. After Hull et al.[31]

2.3.2 Reaction Mechanisms behind TDD Reduction

The potential reactions between threading dislocations that lead to TDD reduction include annihilation and fusion.[32] In an annihilation reaction, threading dislocations with antiparallel Burgers vectors react and stop the propagation of both threading dislocations to the film surface. In a fusion reaction, two threading dislocations combine into one dislocation with a Burgers vector that is the sum of the Burgers vectors of the reacting dislocations. Annihilation or fusion can occur in the following ways (shown schematically in Figure 2.8):[32]

(a) Threading segments from distinct dislocation sources on the same slip plane may annihilate or fuse by glide.

(b) Threading segments from distinct dislocation sources on parallel slip systems can annihilate or fuse. Since threading segments are moving to a different glide plane, this can be achieved by glide, cross slip or climb.

(c) Threading segments from distinct dislocation sources on intersecting slip systems can annihilate or fuse by glide and/or climb.

Since dislocations can meander through a crystal, annihilation and fusion may happen in only part of the threading dislocations, as shown in Figure 2.9.[33]

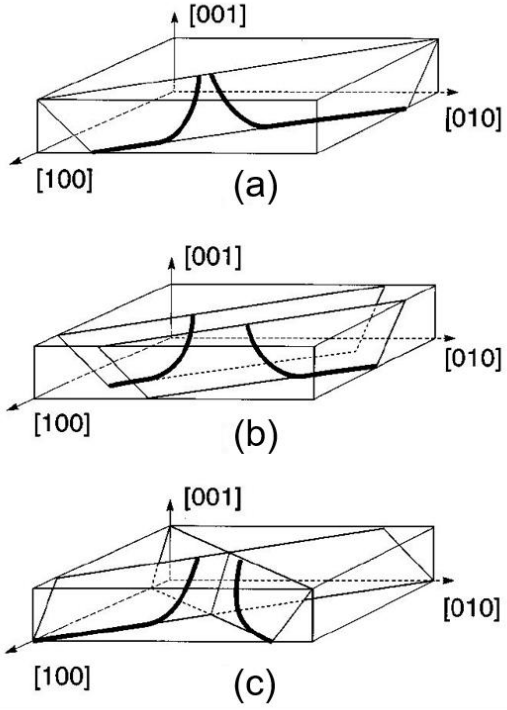

Figure 2.8: Potential reduction mechanisms between two threading segments: (a) Threading segments from distinct dislocation sources on the same slip plane may annihilate or fuse by glide (b) Threading segments from distinct dislocation sources on parallel slip systems can annihilate or fuse, via cross slip or climb (c) Threading segments from distinct dislocation sources on intersecting slip systems can annihilate or fuse by glide and/or climb. After Speck et al.[32]

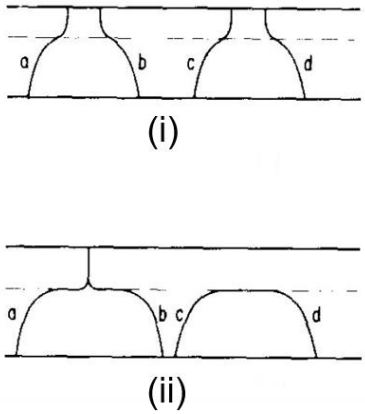

Figure 2.9: Dislocations a and b combine and form a new dislocation; dislocations c and d annihilate each other. After Matthews and Blakeslee.[33]

As two threading dislocations move and annihilate each other, their corresponding misfit dislocations will join. However, the misfit dislocations will not join at the Ge/Si interface

and instead they are observed to join ~50 nm above the Ge/Si interface, forming a confined dislocation network (CDN) as shown in Figure 2.10.[34]

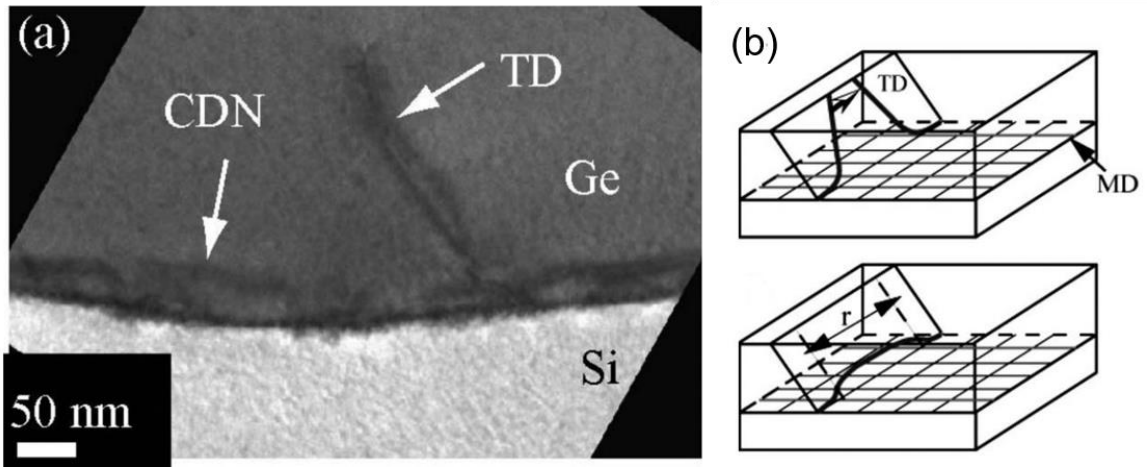

Figure 2.10: (a) Cross-sectional TEM image showing the confined dislocations at about 50 nm above the Ge/Si interface (b) Up: Schematic of threading dislocation (TD) glide in one plane; Down: after TD annihilation, a CDN is left above the Ge/Si interface. After Loo et al.[34]

According to Speck et al,[32] the essence of TDD reduction is to enhance the effective lateral motion of threading dislocations such that threading dislocations will fall within an annihilation or fusion radius of one another. Cyclic annealing, discussed in Chapter 2.2, produces a thermal stress that enhances the lateral motion of threading dislocations. This approach alone leads to a saturated TDD on the order of 10^7 cm^{-2}. In order to further reduce TDD, image forces are introduced in conjunction with the thermal stress to enhance the lateral motion of threading dislocations.

2.3.3 Image Force by SiO_2 Sidewalls, Facets and Nanovoids

Image force is an attractive force a dislocation feels toward a free surface. Classical studies show that an image dislocation needs to be imposed to satisfy the boundary condition that the normal and shear stress at a free surface are zero.[29,35] The image dislocation has the same magnitude but opposite direction of the Burgers vector of the original dislocation.

In order to enhance the lateral motion of dislocations by using the image force, free surfaces need to be introduced. Extensive studies have incorporated vertical SiO_2 sidewalls into the Ge epilayer, thanks to a wealth of semiconductor patterning techniques.[12,36,37] Additionally, Ge or GeH_4 reacts with SiO_2 and forms GeO_2, which is volatile and unstable at the growth temperature, so Ge growth does not occur on the sidewall. The image force due to the presence of vertical oxide sidewalls is equivalent to an attractive glide force that cause dislocations to glide to the sidewalls. Zhang et al.[37] developed a quantitative model that predicts the spacing between oxide sidewalls for effective removal of dislocations by glide toward the sidewall (without considering annihilation or fusion). The image force (F_I) is approximated as:

$$F_I = \frac{Gb^2h}{4r\pi cos\varphi}(cos\theta + \frac{sin\theta}{1-\nu})$$

where G is the shear modulus of Ge, r is the distance between a dislocation and a sidewall, b is the magnitude of the Burgers vector, θ is the angle between the line direction and the Burgers vector, h is the Ge layer thickness, ν is the Poisson's ratio of Ge and φ is the angle between the dislocation and the interface. Zhang et al.[37] neglected the Peierls force and only considered the line tension (F_L) as the opposing force:

$$F_L = \frac{Gb^2}{4\pi}(cos^2\theta + \frac{sin^2\theta}{4(1-\nu)})\ln\frac{sin\theta}{4f}$$

where f is the lattice mismatch. A dislocation at the mesa center is the most difficult to remove because it experiences the least image force and it has to travel the longest distance before reaching the sidewall. In this case, r = 0.5L where L is the side length of the square Ge mesa (spacing between sidewalls) and hence:

$$F_I = \frac{Gb^2h}{2L\pi cos\varphi}(cos\theta + \frac{sin\theta}{1-\nu})$$

The dislocation will be removed by glide to a sidewall if $F_I > F_L$. Consider the case where h = 1 μm, ν = 0.3, f = 4.2% and 60° threading dislocations, L < 10.9 μm. This states that

there is a maximum L for the mesa to be dislocation-free. As opposed to blanket film, local growth of the epilayer in between oxide sidewalls on a substrate is called *selective area epitaxy*. Combining selective area epitaxy and cyclic annealing, Luan et al.[12] demonstrated small mesas ($10\mu m \times 10\mu m$) of Ge on Si with no threading dislocations and an average TDD of 2.3×10^6 cm^{-2}.

Besides oxide sidewalls, facets can also provide image forces. The faceting behavior of Ge has been extensively studied.[6,17,38,39] It is commonly recognized that (001) is a fast growing plane and slow-growing {113} facets dominate with {111} facets expanding as the layer grows thicker. Studies have shown that the presence of facets plays a dominant role in directing dislocations because dislocations are observed to follow the facet normal.[14,38–41] When they encounter a second facet of different orientation, they redirect to follow the normal to the second facet (Figure 2.11). This inspired the emergence of *3D heteroepitaxy*.

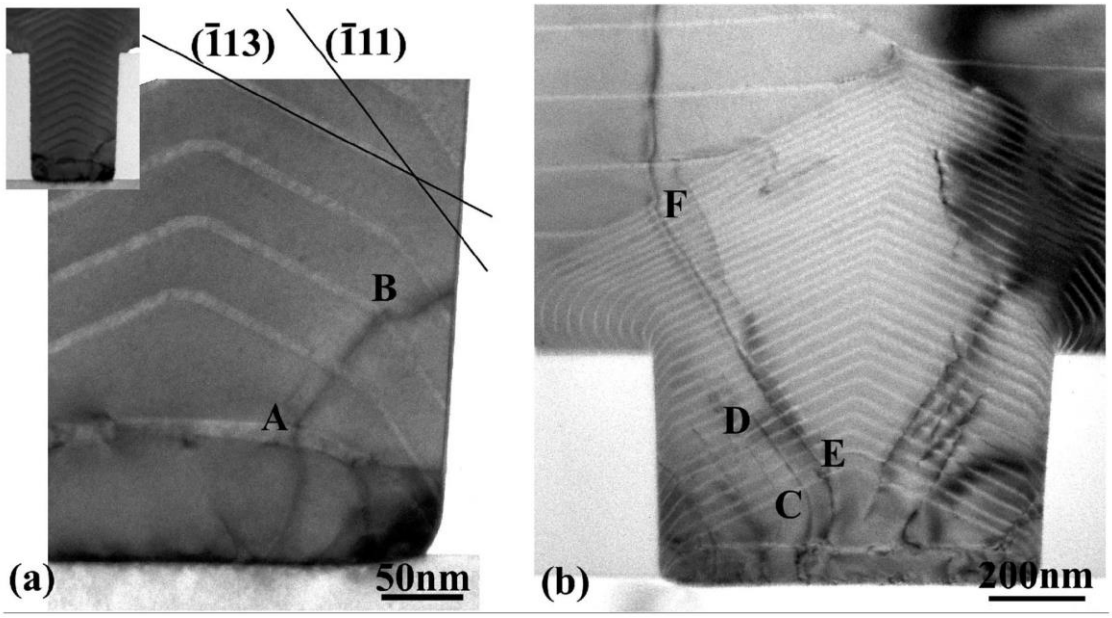

Figure 2.11: Cross-sectional TEM images showing the redirection of dislocations under the influence of faceting. The linear white contrast features correspond to the inserted SiGe growth marker layers. The film was overgrown beyond the sidewall. (a) Trench of 300 nm wide. The inset shows the overview of the Ge film deposited in the trench. (b) Trench of 800 nm wide. After Bai et al.[38]

In 3D heteroepitaxy, the Si substrate is patterned into arrays of micron-tall pillars by photolithography and deep reactive ion etching (the Bosch process). The Bosch process is based on repeated cycles of isotropic SF_6 plasma etching, followed by deposition of a protective C_4F_8 layer on the sidewalls, resulting in highly anisotropic vertical etching. Ge crystals are epitaxially deposited atop the Si pillars by CVD. Initially, the Ge crystals also grow in the lateral dimension and the spacing between adjacent crystals decreases as a result. When the spacing shrinks to a critical distance of about 50 nm, the local adatom density is diminished due to geometric shielding by neighboring crystals, which obstructs sizable material transfer and quenches the lateral growth. Finally, growth purely occurs in the vertical direction, achieving Ge crystals up to tens of microns tall on Si pillars. This is similar to selective area epitaxy which uses SiO_2 to confine Ge growth to the vertical direction.

As mentioned earlier, (001) is a fast growing plane. Ge adatoms preferentially deposit on the (001) plane, leading to a net flux of adatoms to the (001) plane from other facets.[17,40] At low growth temperature, the Ge crystals exhibit a central (001) facet bounded by slanted {113} and {111} facets, as shown in Figure 2.12a. As the growth temperature is raised, material transfer from {113} to (001) is enhanced and the (001) flat top eventually disappear (Figure 2.12b). At low growth temperature where the Ge crystals exhibit a central (001) facet, vertical dislocations (VD) extend straight up to the surface. At high growth temperature where the (001) top facet is consumed, dislocations are redirected to follow the normal to {113} and {111} facets and eventually they terminate at the sidewalls of Ge crystals, eliminating dislocations that extend to the top. While this approach realized thick Ge crystals on Si with no wafer bowing, no cracks and reduced TDD, a conspicuous drawback of 3D heteroepitaxy is the rugged top surface. For a large number of applications that require a flat surface, planarization of the top part of the Ge crystal array by chemical mechanical polishing can rupture the Si pillars.

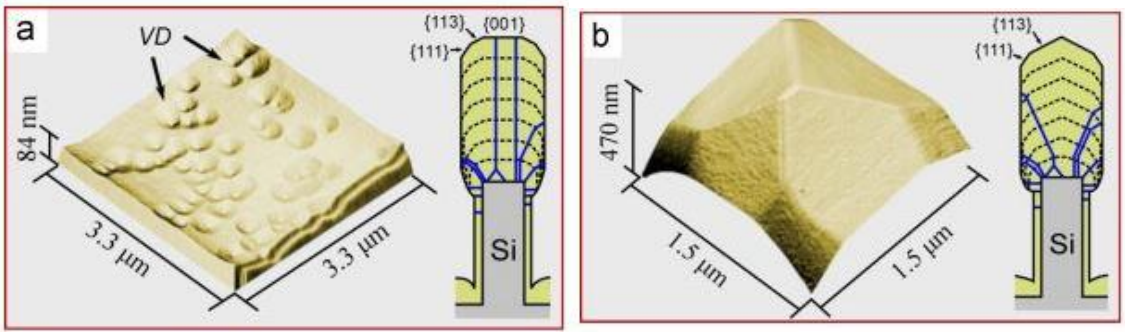

Figure 2.12: Atomic force microscopy scan of the crystal top surface after chemical etching and schematics of dislocation morphology for (a) flat (001) and (b) {113} fully facetted top morphology. After Bergamaschini et al.[40]

Another more recent method employs *nanovoids* as free surfaces that provide image forces.[15] This approach involves electrochemical etching and thermal annealing to form a porous nanostructure from the blanket Ge film. Similar to EPD measurement, electrochemical etching on blanket Ge film preferentially attacks dislocations and leads to a porous structure. Subsequent thermal annealing induces structural reorganization of the porous Ge and brings about nanovoids that attract dislocations, enhancing the probability of annihilation or fusion of dislocations. Wen et al.[42] also studied thermally induced geometric reconfiguration of Ge and they observed that the voids are actually defined by facets. Comparable to 3D heteroepitaxy, the nanovoids approach traps dislocations through facets. While this is a cost-effective and highly scalable strategy to achieve Ge-on-Si virtual substrate of low TDD, the porous structure of the Si substrate poses challenges in Si photonics.

2.4 Summary

This chapter focused on the crystallography of dislocations in the diamond cubic structure, the reaction mechanisms behind TDD reduction and strategies that introduce free surfaces and image forces into the Ge epilayer. The image forces attract dislocations and thus enhance the effective lateral motion of threading dislocations such that threading

dislocations will fall within an annihilation or fusion radius of one another. While 3D heteroepitaxy and the nanovoids approach use the same material (Ge) to introduce image forces, selective area epitaxy incorporates an additional material (SiO_2) for image forces. The balance between image force and line tension is a simplified calculation to predict if dislocations can be removed by glide to the oxide sidewall. Chapter 3 will unfold by discussing the complications when thermal mismatch between Ge and SiO_2 is taken into consideration.

CHAPTER 3

GERMANIUM-ON-SILICON VIRTUAL SUBSTRATE

The previous chapter discussed three approaches to introduce image forces. 3D heteroepitaxy and the nanovoids approach use facets to trap dislocations, which do not involve additional materials. Selective area epitaxy, however, relies on SiO_2. The thermal mismatch between Ge and SiO_2 compromises the thermal stress at the mesa edge, which repels dislocations back to the Ge mesa and hinders TDD reduction.[17] In this chapter, process flows are developed and optimized to address this challenge.

3.1 Thermal Mismatch

While the thermal mismatch between Si and Ge (approximately 2.7×10^{-6}/K in the temperature range of interest) is instrumental in TDD reduction during cyclic annealing by providing a thermal stress, SiO_2 has a similar mismatch but of opposite sign relative to Si of approximately 2.0×10^{-6}/K ($\alpha_{SiO_2} = 5.6 \times 10^{-7}/K$). As temperature is reduced, Ge mesas contract while SiO_2 sidewalls expand relative to the Si substrate. The thermal stress near the mesa edge is thus undermined, which can prevent dislocations from gliding further once they approach the mesa edge. During the next annealing half cycle where the temperature variation is reversed in sign, the dislocations will experience a thermal stress in the opposite direction that moves them away from the mesa edge and back into the mesa center.[17] To overcome this problem of thermal expansion compensation between Ge mesa and SiO_2 sidewall, a new process is designed that replaces the SiO_2 sidewalls with Ge

deposited at a different temperature. The hypothesis is to introduce an interface without thermal mismatch by depositing Ge at different temperatures and the interface should provide an image force that attracts dislocations in the mesa.

3.2 Process with Two UHVCVD Growths to Introduce an Interface

Six-inch Si (100) wafers were wet cleaned prior to Ge deposition by an "RCA standard clean"[43] with an additional HF dip to H-terminate the Si surface:[17]

1) Organic and particle clean: $NH_4OH:H_2O_2:H_2O$ = 1:1:5 at 80℃ for 10 min

2) Oxide strip: $HF:H_2O$ = 1:50 for 1 min

3) Ionic clean: $HCl:H_2O_2:H_2O$ = 1:1:6 at 80℃ for 15 min

4) Oxide strip and passivation: $HF:H_2O$ = 1:50 for 1 min

Ge was deposited on Si substrates using a two-step process in an ultra-high vacuum chemical vapor deposition (UHVCVD) system. In the two-step process, the low-temperature thin Ge buffer layer was deposited at 350°C to avoid island formation by limiting the mobility of Ge adatoms at lower temperatures. The high-temperature thick layer was deposited at 730°C for faster growth rate and higher crystal quality. Since typical photovoltaic concentrator cell sizes are on the order of 0.1 to 1 cm^2,[17] Ge mesa structures were therefore arrayed to fill 2mm x 2mm areas and patterning was performed through photolithography and subsequent reactive ion etching using the chlorine gas. The patterned epilayer was cleaned in $3H_2O:1H_2O_2$ for 30s, $5H_2O_2:1H_2SO_4$ for 10 min, followed by 30s $50H_2O$:1HF dip. Subsequently, the empty trenches were filled by Ge deposited at 450°C in a UHVCVD tool, followed by cyclic annealing and chemical mechanical polishing. CMP was performed using a low pH silica slurry (Cabot Microelectronics W2000) which

is suitable for blanket Ge films or Ge films with high pattern density.[44] A schematic of the process flow is outlined in Figure 3.1.

SiO_2 was deposited to allow selective growth of Ge in trenches while protecting the Ge layer from touching photoresist (as shown in Figure 3.1c). Scanning electron microscopy (SEM) was used to monitor the process flow, as shown in Figure 3.2a to Figure 3.2c. The cross section and top view of the epitaxy after trench filling are given in Figure 3.2a and 3.2b. As shown in Figure 3.2a, dry etching left behind an overetch in Si, which served as a landmark to locate the patterns. The trench was overfilled through selective growth of Ge at 450℃, which exhibited facets above the SiO_2 layer. To understand the growth mechanism of selective growth of Ge inside the trench, it is important to relate to the orientations with a local maximum or minimum in growth rate.[6] It has been reported that {111} and {113} are the two slowest growth facets in selective growth of Ge between SiO_2 sidewalls.[38] Since SiO_2 sidewalls were replaced with Ge at 450℃ which was aligned to <110> directions and Ge was grown on (001) substrate, the growth rate of {110} and (001) facets should be taken into account as well. According to Bergamaschini et al.[40], the growth rates of different facets with respect to the (001) facet are listed in Table 1. Since the growth rate of the (001) facet is much faster than the growth rate of the {110} facets, Ge growth from sidewalls must be slow and hence Ge growth at 450℃ occurred from bottom up. The (001) facet eventually disappeared and exhibited the slanted facets {113} and {111}. As shown in Figure 3.2b, the trenches were filled with Ge at 450°C, while the rest was Ge deposited at 730°C. As shown in Figure 3.2c, CMP removed the facets above the trenches. After the CMP, SiO_2 was chemically removed.

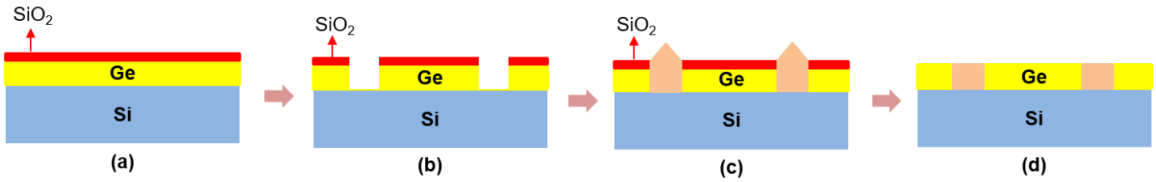

Figure 3.1: (a) Ge growth on Si at 730°C, followed by deposition of SiO_2. (b) Patterning of Ge through photolithography and dry etching. (c) Ge growth at 450°C to fill the trenches, followed by cyclic annealing. (d) Chemical-mechanical planarization and removal of SiO_2 by diluted HF.

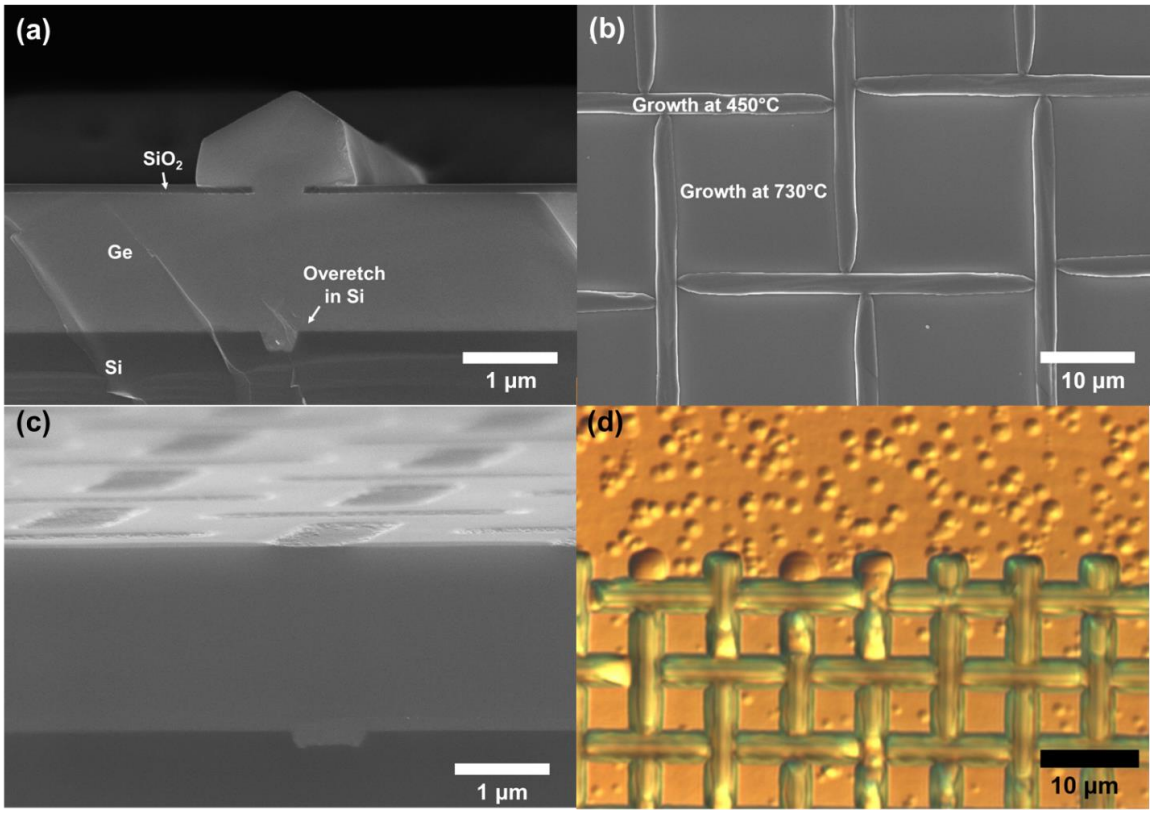

Figure 3.2: (a) Cross-sectional SEM after trench filling. (b) Top view SEM after trench filling: thin trenches are filled by Ge deposition at 450°C, while the mesas enclosed by the trenches are Ge deposited at 730°C. (c) CMP smoothed out the surface with some side effects of dishing above the patterns where SiO_2 is absent. (d) An optical micrograph of EPD results: the top half is blanket Ge-on-Si film deposited at 730°C; the bottom half has regular gridded arrays where the pattern is alternating between high and low temperature Ge.

Table 1: Growth rates of different facets with respect to the (001) facet. After Bergamaschini et al.[40]

Facet	v/v(001)
(001)	1
{113}	0.91
{111}	0.65
{110}	0.28

EPD measurements were performed by using a mixture of CH_3COOH (335mL), HNO_3 (100mL), HF (50mL) and I_2 (150mg) to preferentially etch threading dislocations on the Ge surface. An optical microscope was used to observe the etch pits. As shown in Figure 3.2d, there are significantly fewer etch pits in areas with patterns, compared to blanket Ge-on-Si film. From Figure 3.3a to Figure 3.3c, the grid size increased from 5μm x 5μm to 15μm x 15μm. As shown in Figure 3.3d, TDD increases with increase in side length of the grid. For grids larger than 10μm x 10μm, TDD is on the order of 10^7 cm^{-2}. For smaller grids, TDD is below 10^7 cm^{-2}. This dependence is in agreement with the results reported by Luan et al.[12] where TDD in Ge can be reduced below 10^7 cm^{-2} by combining cyclic annealing and patterned growth of 10 μm × 10 μm Ge mesas.

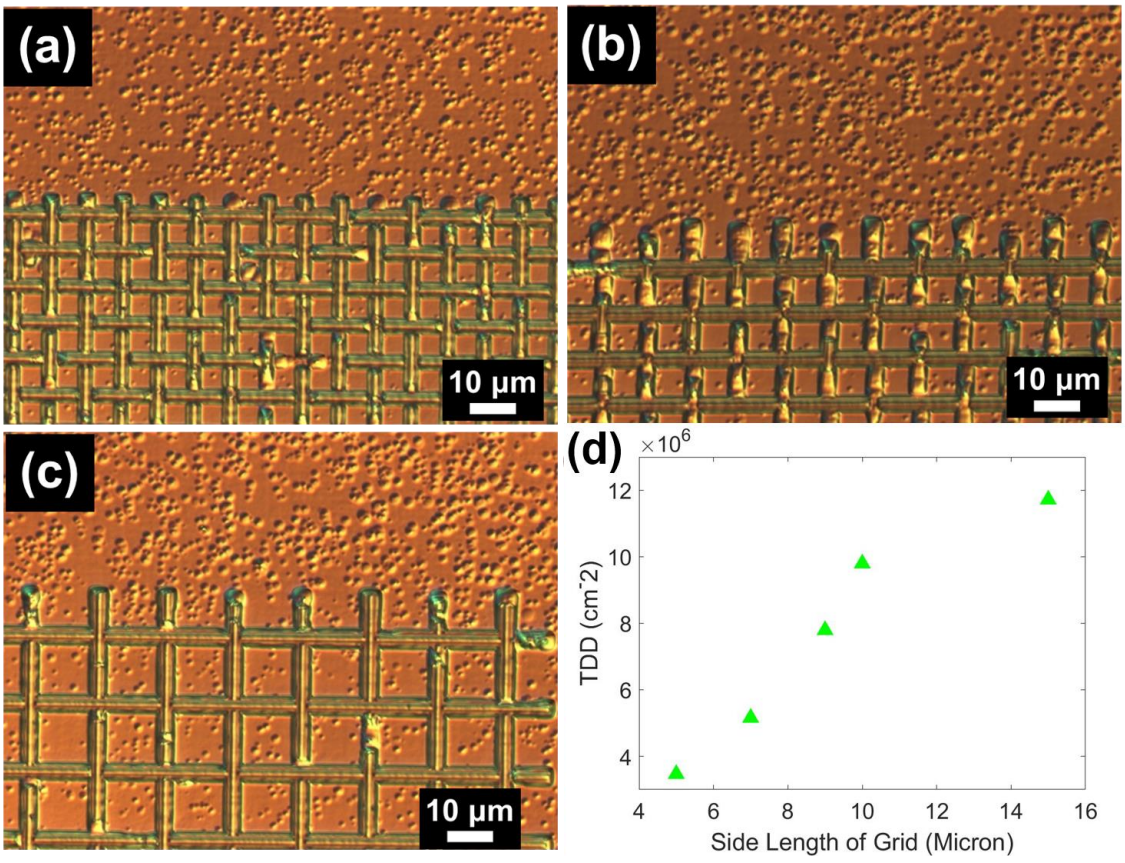

Figure 3.3: Optical micrographs of EPD results for regular gridded arrays of various sizes: (a) 5μm × 5μm grids. (b) 10μm × 10μm grids. (c) 15μm × 15μm grids. The grids show different color from

high temperature Ge because dishing occurred above the patterns as a side effect of CMP, which led to faster removal of the material during the EPD process (d) Threading dislocation densities measured by etch pit density counting in patterned Ge films on Si with various grid sizes.

A subsequent lateral overgrowth of Ge is necessary in order to achieve a continuous film of low TDD. Despite the promising TDD reduction as shown in Figure 3.2d, Albert[17] reported incomplete coalescence at mesa corners in regular gridded arrays due to slow growing facets. In order to eliminate this effect and achieve complete coalescence, a structure with isolated trenches was adopted to avoid crossings but also hinder dislocation movement, as shown in Figure 3.4a. The corresponding EPD results are given in Figure 3.4b. Most etch pits were observed at the trench edge in two rows, indicating an appreciable dislocation sink. The EPD in high temperature Ge mesas is on the order of 10^6 cm^{-2}. The remarkable TDD reduction leads to the first thesis question: **is there an interface between high and low temperature Ge?**

In order to answer this question, the morphology of dislocations was examined using cross-sectional TEM. Samples were prepared by focused ion beam ablation and TEM images were taken on an FEI Tecnai microscope operating at 120 kV. As shown in Figure 3.4d, the Ge epitaxial layer is about 1 micron thick and it appears continuous with no contrast that indicates a distinction between high and low temperature Ge. However, dry etching of Ge left behind a trench in Si which marks the transition between high and low temperature Ge. Dislocations at the trench edges extend to the film surface, which is in agreement with the two rows of etch pits observed under the optical microscope (Figure 3.4b). Dislocations outside the trench are mostly confined within 600 nm from the Ge/Si interface, indicating annihilation of dislocations in the upper half of the Ge epilayer as described by Matthews and Blakeslee.[33] Quantitative analysis was performed on dislocations outside the trench by segmenting the Ge epilayer into 10 sublayers of 100 nm

and calculating the dislocation length in each sublayer. As shown in Figure 3.4c, the dislocation length is greater than 1 micron in the first sublayer and begins to decrease as the sublayer moves away from the Ge/Si interface along the *z* axis.

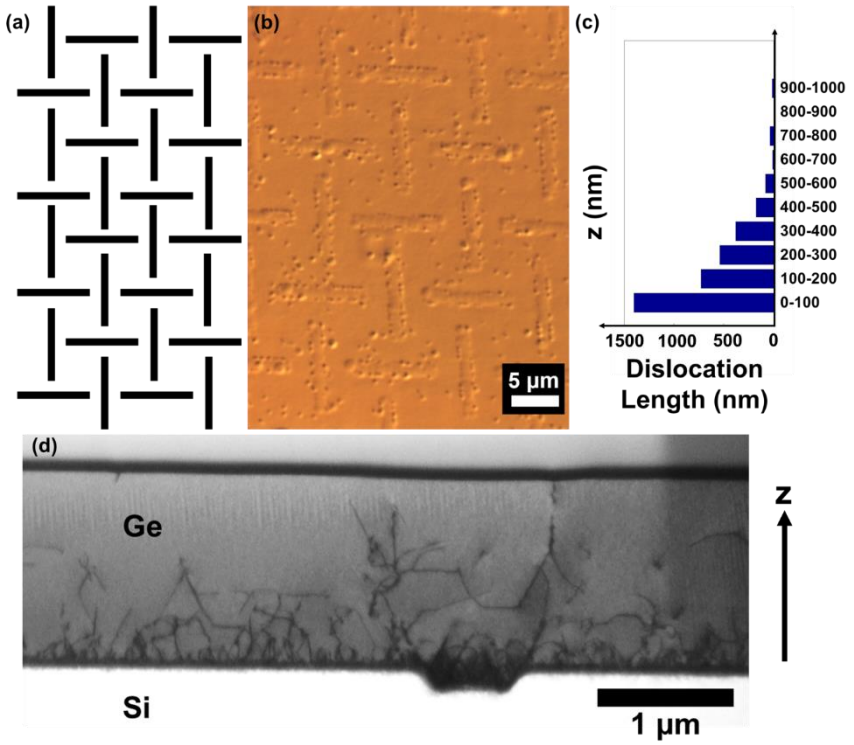

Figure 3.4: (a) Schematic of isolated trenches (b) EPD results of pattern design with isolated trenches (c) Dislocation length outside the trench in 10 sublayers of 100 nm (d) Cross-sectional TEM of Ge-on-Si in pattern of isolated trenches in two beam bright field conditions.

Selected area diffraction was performed on Ge inside the trench (low temperature) and Ge away from the trench (high temperature). Figure 3.5 shows the same set of diffraction spots, which confirms the TEM observation that **there is not an interface between high and low temperature Ge**. Therefore, the interface between high and low temperature Ge is ruled out in contributing to the dislocation sink at the trench edge. Since the overetch in Si is an unintended result of the process flow, this leads to the second thesis question: **does the trench in Si have an influence on dislocations?** In order to answer this question, a simplified process with only one UHVCVD growth is designed.

Additionally, two UHVCVD growths account for >50% of the cost in production scale, as shown in Figure 3.6. A simplified process can also help facilitate large-scale manufacturing.

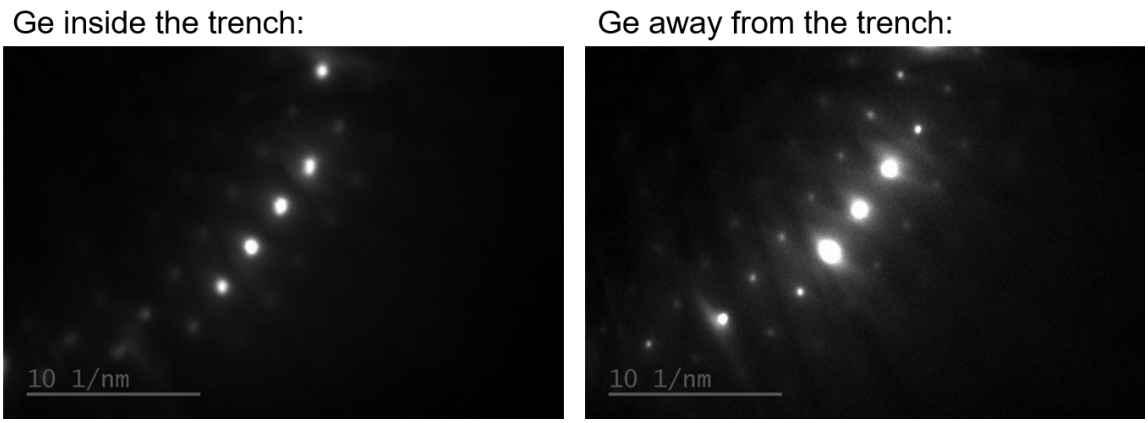

Figure 3.5: Selected area diffraction shows the same set of diffraction spots.

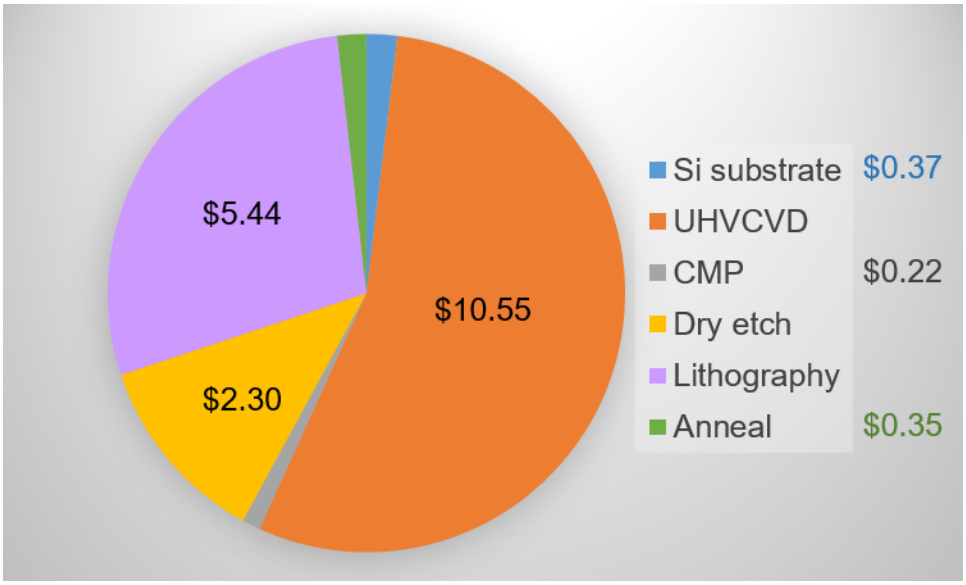

Figure 3.6: Cost breakdown in production scale of Ge-on-Si virtual substrate

3.3 Simplified Process: Ge Growth on Trenched Si Substrate

After 6-inch Si (100) wafers were wet cleaned by an "RCA standard clean" described in Chapter 3.2, they were spun dry in N_2, placed vertically onto a boat and loaded

into a tube furnace for wet oxidation. Trenches were etched into the Si wafers through photolithography and reactive ion etching. After removal of the oxide, the wafers were exposed to an RF generated, magnetically coupled plasma using chlorine gas. The patterned Si wafers were cleaned in a Piranha solution which is a mixture of sulfuric acid, water and hydrogen peroxide to remove organic residues. After the oxide layer was removed by wet etching, the patterned Si wafers were wet cleaned again by RCA with an additional HF dip to H-terminate the Si surface before Ge deposition. Ge was deposited using the same two-step process in an UHVCVD system as described in Chapter 3.2: the low-temperature thin Ge buffer layer was deposited at 350°C and the high-temperature thick layer was deposited at 730°C. The complete process flow is given in Table 2 and its schematic is outlined in Figure 3.7.

Table 2: Process flow of Ge growth on trenched Si substrate

1	RCA clean, HF dip, rinse	rca-ICL
2	Thermal oxide growth	5D-ThickOx
3	Coat photoresist	pTrack
4	Expose	i-stepper
5	Develop	pTrack
6	Oxide dry etch	AME5000
7	Si dry etch-chlorine gas	AME5000
8	Ash photoresist	asher-ICL
9	Si piranha clean	Premetal-Piranha
10	Buffered oxide etch	oxEtch-BOE
11	RCA clean, HF dip, rinse	rca-ICL
12	Ge growth and cyclic annealing	UHVCVD in SEL

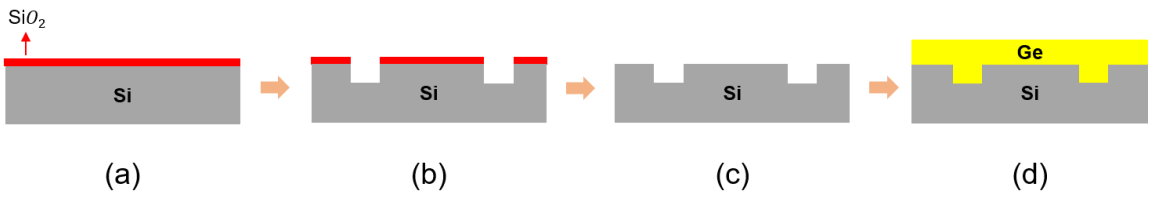

Figure 3.7: (a) RCA clean of Si substrate and wet oxidation (b) Patterning of Si substrate through photolithography and dry etching (c) Piranha clean and oxide removal (d) Ge deposition

SEM was used to examine the trench profile after dry etching of Si and Figure 3.8a shows sloped sidewalls with the trench bottom being narrower. EPD measurements were performed by using a mixture of CH_3COOH (335mL), HNO_3 (100mL), HF (50mL) and I_2 (150mg). As shown in Figure 3.8b, the distribution of etch pits does not seem to be affected by the patterns. The TDD in the Ge mesa is on the order of 10^7 cm^{-2}, which suggests no profound reduction in TDD. The morphology of dislocations was examined using cross-sectional TEM. Samples were prepared by focused ion beam ablation and TEM images were taken on an FEI Tecnai microscope operating at 120 kV. As shown in Figure 3.9a, a carbon layer was deposited on the area of interest to protect the top part of the specimen and to mark the position of the target area. There are two trenches in the area of interest and the dislocations are shown in Figure 3.9b. The Ge epilayer is approximately 1.3 μm thick and the trench depth is approximately 150 nm. For both trenches, dislocations do not appear to trace along the trench edge and they are mostly confined near the Si/Ge interface. A TEM image of a deeper trench (approximately 300 nm deep) is given in Figure 3.10. The morphology of dislocations is similar to Figure 3.9b. Before we rule out the influence of trenches on dislocations, the process flow is optimized to achieve more vertical trench sidewalls. This also leads to thesis question 2.1: **does the trench sidewall angle have an influence on dislocations** and thesis question 2.2: **does the trench depth have an influence on dislocations**?

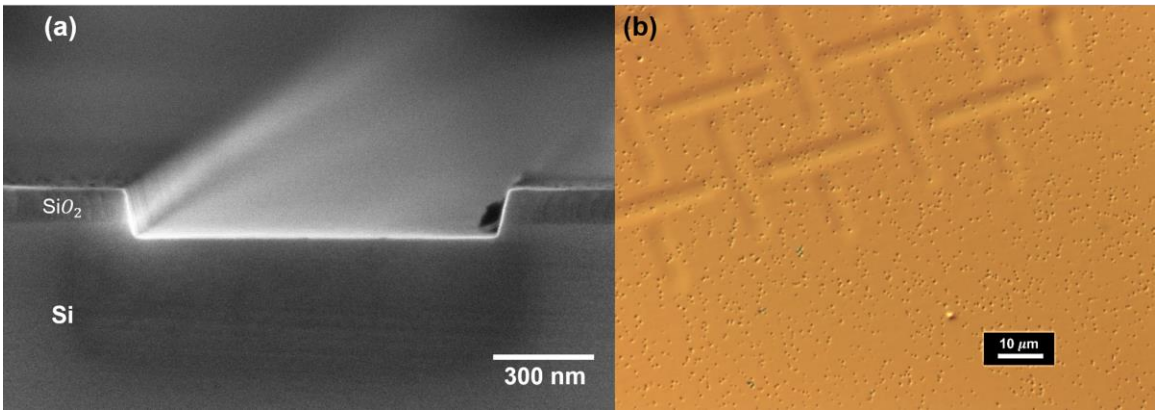

Figure 3.8: (a) Cross-sectional SEM after dry etching (b) EPD result of the simplified process

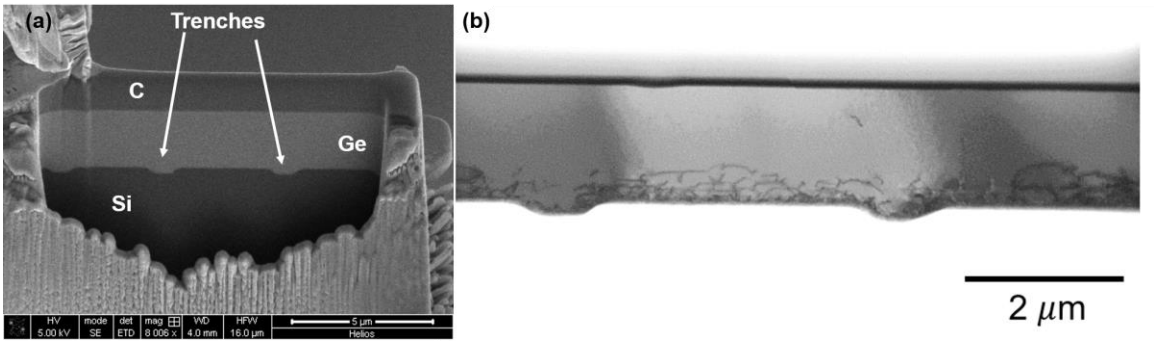

Figure 3.9: (a) Cross-section of Ge-on-Si epitaxy: there are two trenches in the area of interest and a carbon layer was deposited to protect the top portion of the sample (b) Cross-sectional TEM of Ge-on-Si in two beam bright field conditions.

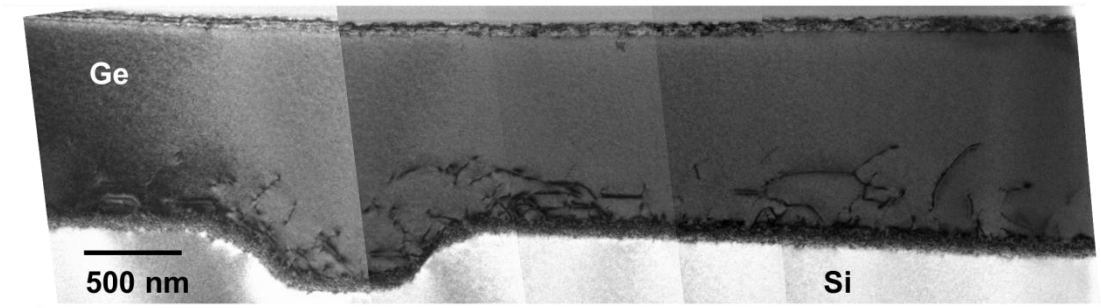

Figure 3.10: Cross-sectional TEM of Ge-on-Si in two beam bright field conditions. Trench depth is approximately 300 nm.

3.4 Modified Process to Avoid Sloped Sidewalls

Two notable changes are made to the process flow. In the old process flow, a soft mask was used to pattern the Si substrate; in the new process flow, a hard oxide mask will

be used instead. In the old process flow, chlorine gas was used for dry etching; in the new process flow, the Bosch process (introduced in Chapter 2) will be used for dry etching. The new process flow is given in Table 3.

Table 3: Modified process flow of Ge growth on trenched Si substrate

1	RCA clean, HF dip, rinse	rca-ICL
2	Thermal oxide growth	5D-ThickOx
3	Coat photoresist	pTrack
4	Expose	i-stepper
5	Develop	pTrack
6	Buffered oxide etch	oxEtch-BOE
7	Ash photoresist	asher-ICL
8	Si dry etch-Bosch process	sts2
9	Si piranha clean	TRL acid-hood
10	Buffered oxide etch	TRL acid-hood
11	RCA clean, HF dip, rinse	rca-TRL
12	Ge growth and cyclic annealing	UHVCVD in SEL

SEM was used to examine the trench profile after dry etching of Si and Figure 3.11a shows almost vertical sidewalls. EPD measurements were performed by using a mixture of CH_3COOH (335mL), HNO_3 (100mL), HF (50mL) and I_2 (150mg). The morphology of dislocations was examined using cross-sectional TEM. Samples were prepared by focused ion beam ablation and TEM images were taken on an FEI Tecnai microscope operating at 120 kV. As shown in Figure 3.11c, the Ge epilayer is approximately 600nm thick and the trench depth is approximately 500 nm. Dislocations are observed to trace along the trench edge, indicating dislocation trapping. As shown in Figure 3.11b, there are fewer etch pits in areas with patterns, compared to blanket Ge-on-Si film. Both TEM and EPD results show TDD reduction in Ge-on-Si virtual substrate with deep trenches and vertical trench sidewalls.

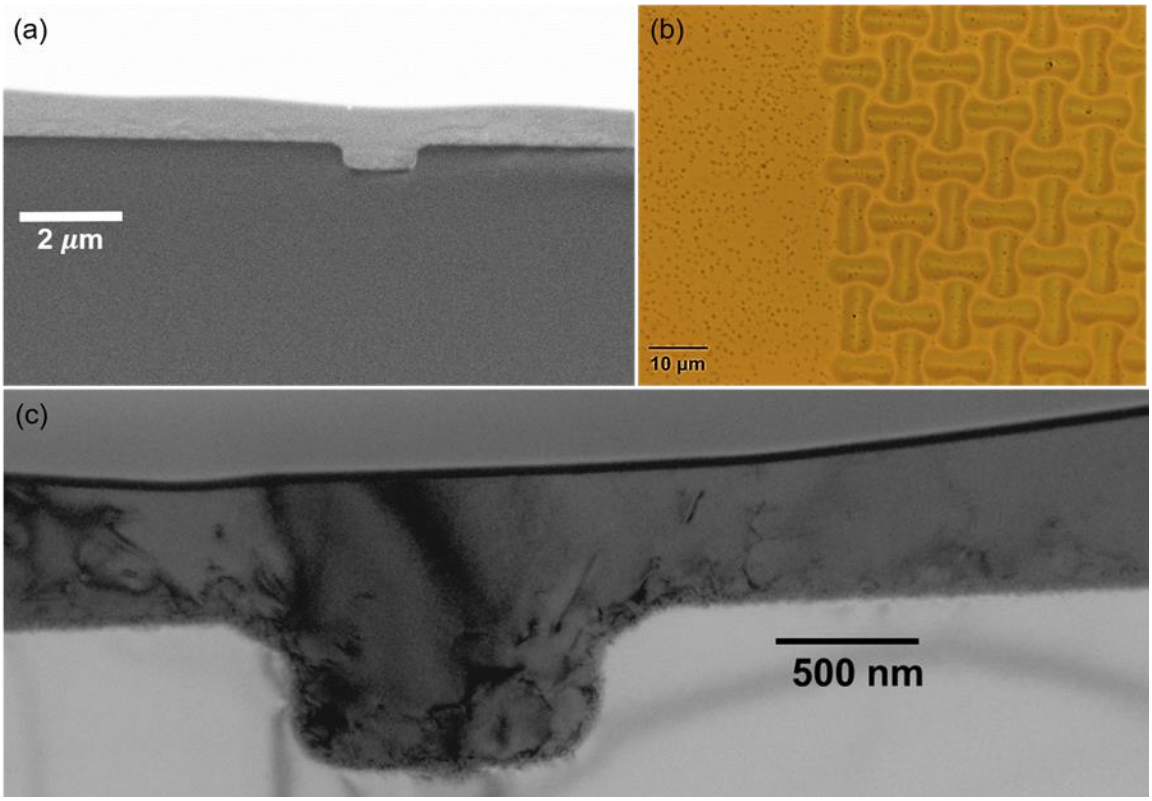

Figure 3.11: (a) Cross-sectional SEM after dry etching (b) EPD result of the modified process (c) Cross-sectional TEM of Ge-on-Si in two beam bright field conditions.

From Figure 3.12a to Figure 3.12c, the grid size increased from 12 μm × 12 μm to 20 μm × 20 μm. As shown in Figure 3.12d, TDD is reduced to the lower range of 10^7 cm^{-2} and it increases with increase in side length of the mesa. Since the wafers were not polished, there were variations in the film thickness, which brought about challenges in measuring TDD in smaller mesas.

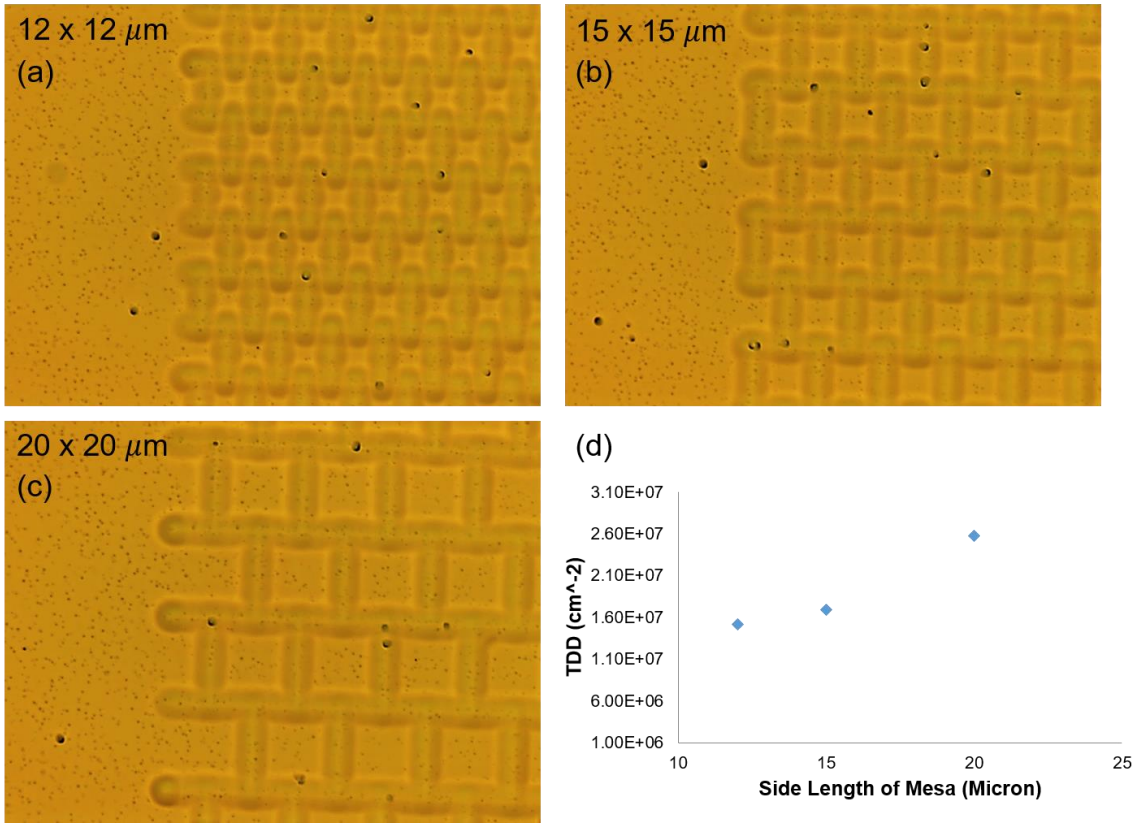

Figure 3.12: Optical micrographs of EPD results for Ge mesas of various sizes: (a) 12μm × 12μm grids. (b) 15μm × 15μm grids. (c) 20μm × 20μm grids. (d) Threading dislocation densities measured by etch pit density counting in patterned Ge films on Si with various mesa sizes.

To smooth out the variation in film thickness, CMP was performed on wafers from the same batch using the slurry introduced in Chapter 3.2. EPD measurements were performed after CMP, as shown in Figure 3.13. The patterns become less obvious after polishing and there are quite many etch pits in the Ge mesa. However, rows of etch pits are observed along the trench edge. The morphology of dislocations was examined using cross-sectional TEM. Samples were prepared by focused ion beam ablation and TEM images were taken on a JEOL 2010 microscope operating at 200 kV. As shown in Figure 3.14, dislocations are observed to trace along the trench edge. Both EPD and TEM results show dislocation trapping at the trench edge. In addition, the Ge epilayer is thinned down to only ~500nm thick, which explains why we see quite many etch pits in the mesa.

According to Tachikawa and Yamaguchi,[45] for films of thickness <10 μm the dislocation density is inversely proportional to the film thickness, which agrees with our observation that there are more dislocations in sublayers closer to the Si/Ge interface (Figure 3.4). This implies that when the epilayer is thinned down to half its original thickness, there will be more dislocations that extend to the surface. As shown in Figure 2.9, after dislocations c and d annihilate each other, the top half of the epilayer is dislocation free. However, if the epilayer thickness is reduced by half, dislocations c and d will extend to the surface and leave behind etch pits after etching.

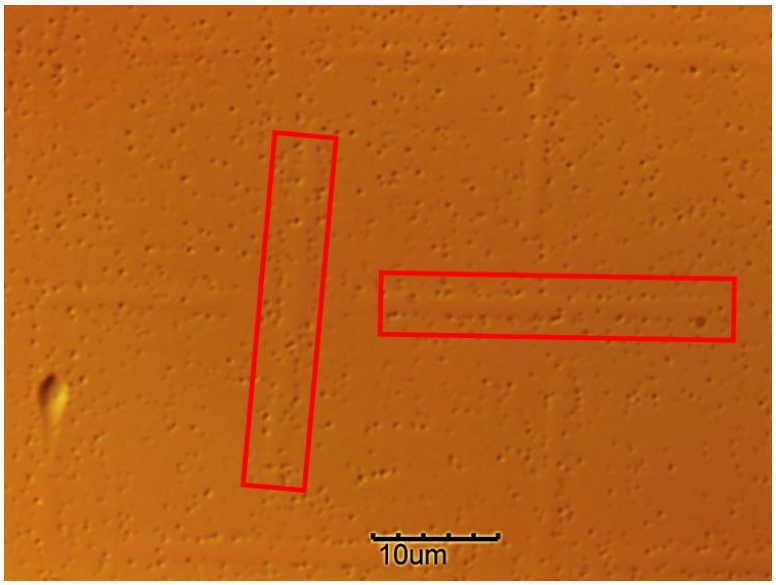

Figure 3.13: Optical micrograph of EPD results after polishing. The areas in the red boxes show rows of etch pits along the trench edge.

Figure 3.14: Cross-sectional TEM of Ge-on-Si after polishing in two beam bright field conditions.

Figure 3.15 and Table 4 compare the process with two UHVCVD growths and the process with only one UHVCVD growth. While both processes show TDD reduction, the

reduction is more pronounced in the process with two growths. Additionally, the simplified process requires deeper trenches and extended growth time in order to show TDD reduction. Although the simplified process only involves one UHVCVD growth, the extended growth time might not necessarily lead to significant cost savings. Moreover, dry etching is the third major cost contributor to the process flow. Deeper trenches require longer etching time, which will also add to the cost. The different trench sidewall angles between the two processes further indicates that TDD reduction in both processes is governed by different mechanisms. To answer thesis questions 2.1 and 2.2, **the trench sidewall angle has no influence on TDD reduction**; **TDD reduction and dislocation trapping are observed for deep trenches**.

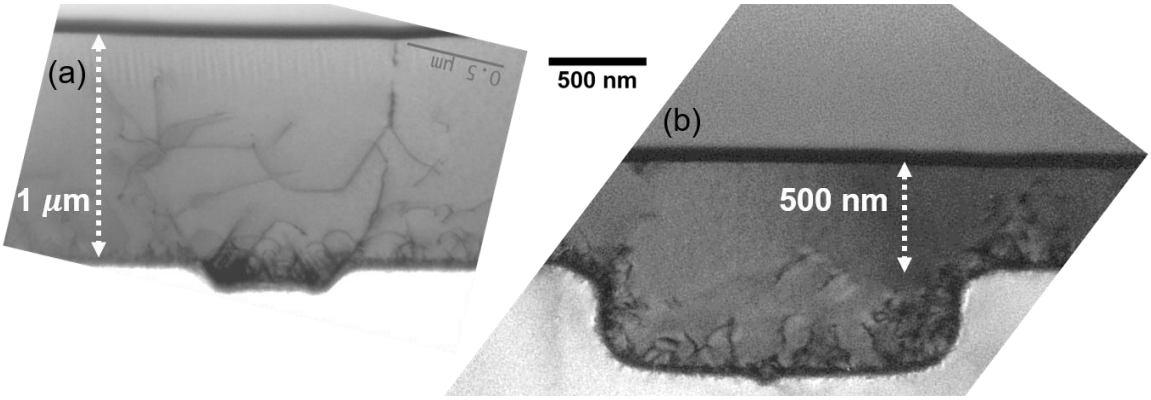

Figure 3.15: TEM comparison between (a) process with two growths and (b) process with one growth. Both micrographs are set to the same scale, with the Si/Ge interface aligned. (a) shows a shallow trench, sloped sidewalls and thicker film. (b) shows a deep trench, vertical sidewalls and film only half as thick.

Table 4: Comparison between the process with two growths and the process with one growth

	Process with 2 growths	**Process with 1 growth**
TDD reduction	Significant	Not as significant
Trench depth	150-200 nm	~500 nm
Trench sidewall angle	Sloped	Vertical

3.5 Revisiting the Process Flow with Two UHVCVD Growths

In Chapter 3.2, we disprove the hypothesis that the interface between high and low temperature Ge provides an image force for TDD reduction; in Chapters 3.3 and 3.4, we find that the trench sidewall angle and trench depth do not contribute to TDD reduction in the process with two UHVCVD growths. Then what leads to TDD reduction in that process? To answer this question, let us re-examine the processing steps and electron microscopy results. Some of the overlooked facts are listed below:

- The low temperature Ge deposited into trenches exhibits facets (Figure 3.2a)
- Cyclic annealing was performed in the presence of Ge facets and SiO_2
- TEM was performed after polishing which removed facets
- Parallel dislocations are observed in the trenches for the process with two growths (Figure 3.15a and Figure 3.16). The angle between the parallel dislocations and the Si/Ge interface is measured to be 54-60°.
- Neither parallel dislocations nor facets are observed in the trenches for the simplified process (Figure 3.15b and Figure 3.17)

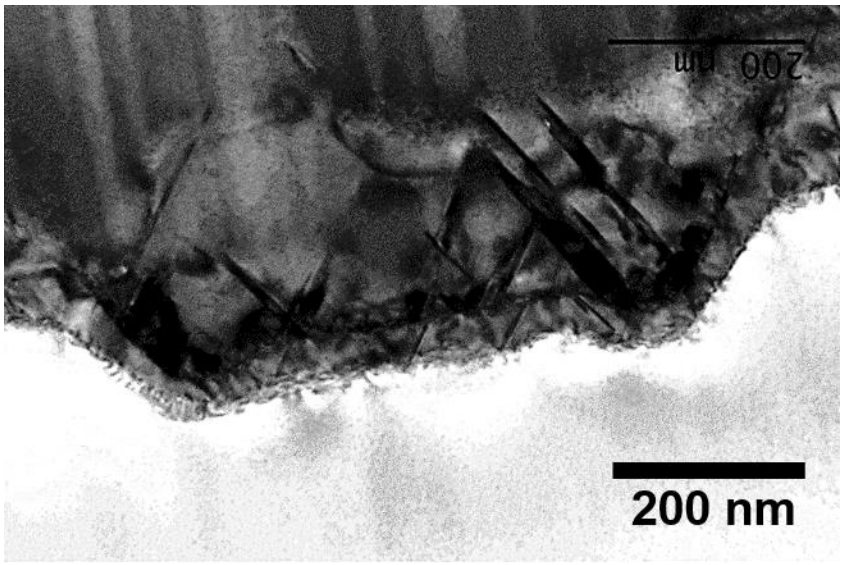

Figure 3.16: Cross-sectional TEM showing dislocations in the trench for the process with two growths. Despite the curtaining effect as a result of the milling process, parallel dislocations are observed in the trench.

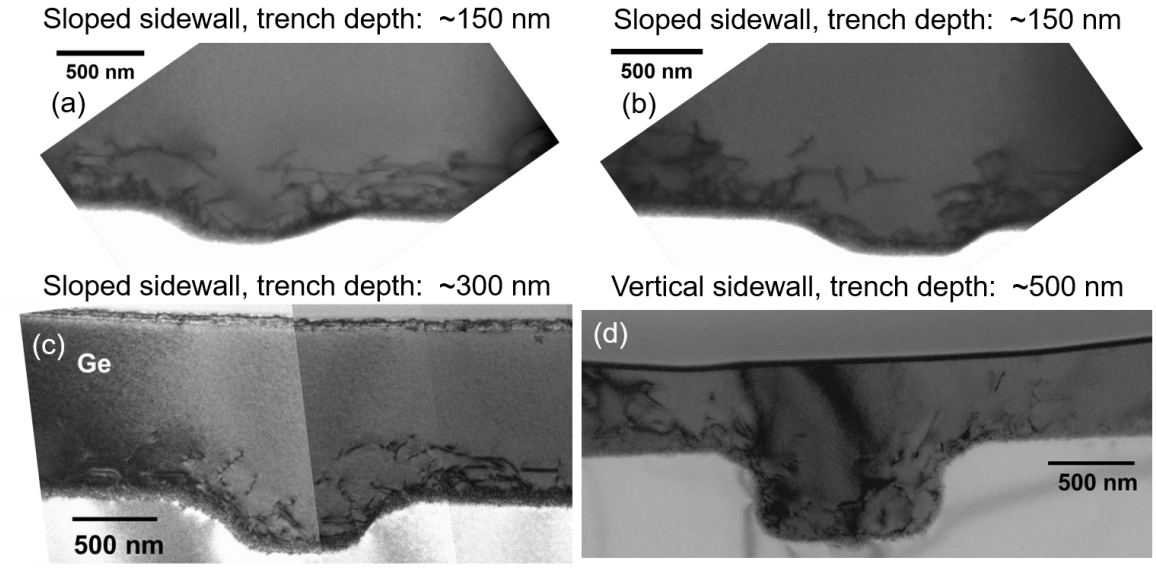

Figure 3.17: Morphologies of dislocations in different trenches for the simplified process. Samples are not polished.

As discussed in Chapter 2, Bai et al.[38] reported facets in Ge selectively deposited in trenches on Si. Their TEM images show parallel dislocations that follow the local facet normal (Figure 2.11b). The angle between these parallel dislocations and the Si/Ge

interface is also measured to be 54-60°. Therefore, it is probable that the parallel dislocations in the trench formed during the growth of low temperature Ge and were trapped by the facets due to image forces. As a result, these dislocations might have limited ability to glide during cyclic annealing.

Now consider a dislocation in the Ge mesa that started gliding to the trench in response to the thermal stress during cyclic annealing (Figure 3.18a). When the dislocation reached the end of the SiO_2 layer, it would be pinned there because there was little strain in the overgrown facet and dislocations cannot terminate inside a crystal. Therefore, dislocations would be trapped at the surface right above the trench edge, which was consistent with the fact that etch pits were observed at the trench edge. The other end of the dislocation at the Ge/Si interface, however, can be mobile before it reconfigures into a more energetically favorable position. While the presence of trenches might affect if and how the dislocation will reconfigure itself at the Ge/Si interface, it is dislocation trapping at the surface of the Ge epilayer that makes a difference on TDD in the Ge mesa. Since TEM studies were performed after removal of SiO_2, direct evidence of dislocation trapping at the end of the SiO_2 layer is lacking. However, we can measure the width of the SiO_2 opening from SEM studies (Figure 3.19a) and compare it with the distance between the two dislocation ends from TEM studies (Figure 3.19b). Since the trench width differs, it is reasonable to normalize both distances with respect to the trench width. As shown in Figure 3.19, the ratio of the width of oxide opening to the trench width is around 2 and the ratio of the distance between two dislocation ends to the trench width is also around 2, which adds credibility to the hypothesis that dislocations get pinned at the end of the SiO_2 layer.

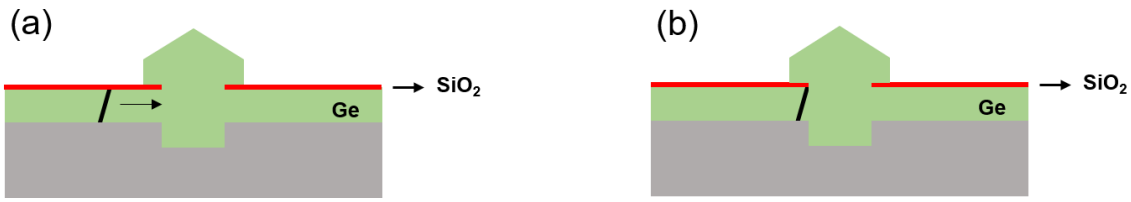

Figure 3.18: Schematic illustration for the mechanism of dislocation trapping: (a) a dislocation in the Ge mesa starts gliding to the trench in response to the thermal stress during cyclic annealing (b) the dislocation gets pinned at the end of the SiO_2 layer

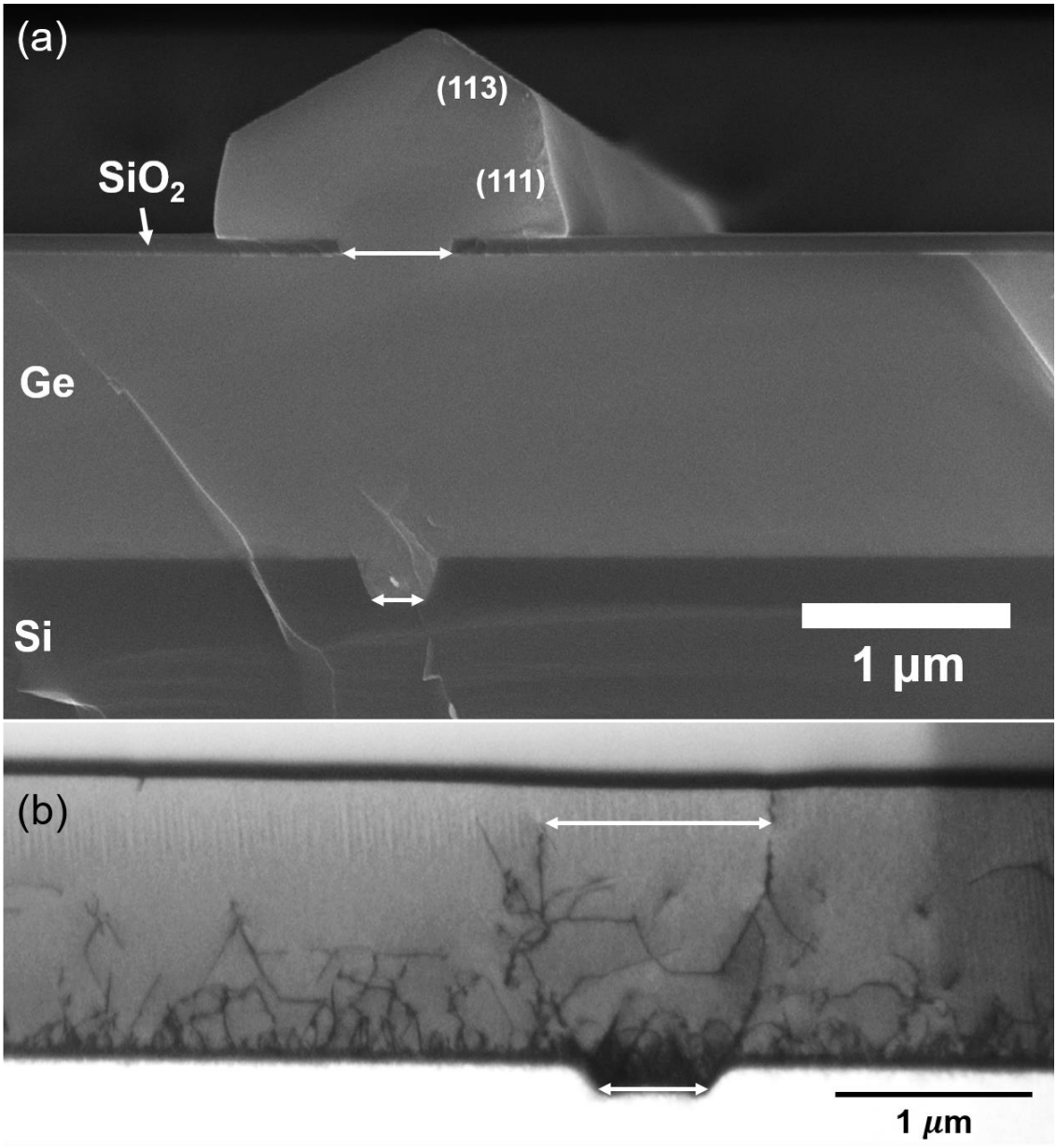

Figure 3.19: (a) The ratio of the width of oxide opening to the trench width is around 2. (b) The ratio of the distance between two dislocation ends to the trench width is also around 2.

Stach et al.[46] reported an increase in dislocation velocities during annealing when an oxide layer was added to the surface of SiGe epilayer. At 600℃, the dislocation velocity increases by a factor of two. Additionally, their experiments have shown that in the presence of an oxide layer atop the SiGe epilayer, the temperature range where dislocations can move is expanded. Dislocations can move at a temperature as low as 450℃. They attribute the increased dislocation velocities to enhanced kink nucleation at the oxide/epilayer interface,[30] which is a promising reason why TDD reduction is more effective in the process flow where cyclic annealing was performed in the presence of SiO_2 layer atop the Ge epilayer.

Despite the increase in dislocation velocities during annealing in the presence of SiO_2 on top, etch pits were observed in Ge mesas as small as 5 μm by 5 μm (Figure 3.3). While local weakening in thermal stress at mesa edges or sidewalls was reported to prevent dislocations from reaching the mesa edges,[17,47] it does not apply to this system because the Ge epilayer is continuous with no interface between high and low temperature Ge. Assume there is no significant nonuniformity in thermal stress in the Ge epilayer, Monte Carlo simulations are conducted in Matlab to evaluate the effect of dislocation pinning on dislocation glide. The code is given in Appendix A. In the simulation, the Ge epilayer is treated as a blanket film and the high temperature Ge mesa with SiO_2 on top is considered as a "virtual mesa". Dislocation reactions are considered separately from dislocation pinning by using an initial TDD based on experimental data of TDD in blanket Ge-on-Si films after cyclic annealing. The average glide distance per dislocation (l) to completely relieve the thermal strain is:

$$l = \frac{\int_{T_L}^{T_H} [\alpha_{Ge}(T) - \alpha_{Si}(T)]dT}{b_{eff}\rho_{TD}}$$

Where T_L and T_H are the lowest and highest temperature during cyclic annealing; α_{Ge} and α_{Si} are the thermal expansion coefficients of Ge[48] and Si[17] and they are given by:

$$\alpha_{Ge}(T) = 10^{-6}(5.04 + 3.79 \times 10^{-3}T - 3.5 \times 10^{-7}T^2)$$

$$\alpha_{Si}(T) = 3.725 \times 10^{-6}\left(1 - \exp\left(-5.88 \times 10^{-3}(T - 124)\right)\right) + 5.84 \times 10^{-10}T$$

Albert[17] included a factor of 2 in his equation to calculate l because his simulations are based on Ge mesas selectively grown between oxide sidewalls where the two threading arms of the same misfit are in the same mesa, which does not necessarily hold for virtual mesas. For ρ_{TD}= 2.5×10^7 cm^{-2}, $b_{eff} = 2$Å, T_L = 650℃ and T_H = 850℃, $l \approx 10.5\mu m$.

Threading dislocations are randomly placed in a single mesa. For each dislocation, an initial <110> glide direction is assigned which can only change in sign (no cross-slip is allowed). A threading dislocation is allowed to glide until it either gets pinned by a misfit dislocation or glides to the mesa edge. Once a threading dislocation arrives at a mesa edge, it will stop gliding. The pinned dislocations that have not reached the mesa edge are allowed to glide in the opposite direction in the next annealing half cycle. Figure 3.20 shows examples of the model's results for mesas of side length of 5 μm, 7 μm and 10 μm, with an initial TDD of 2.5×10^7 cm^{-2}. The average TDD values for various mesa sizes are given in Figure 3.20d, roughly corresponding with trends observed experimentally (Figure 3.3d). As the mesa side length is increased, the average required distance for a threading dislocation to glide to the mesa edge as well as the linear density of misfits increase, favoring the probability of dislocation pinning.

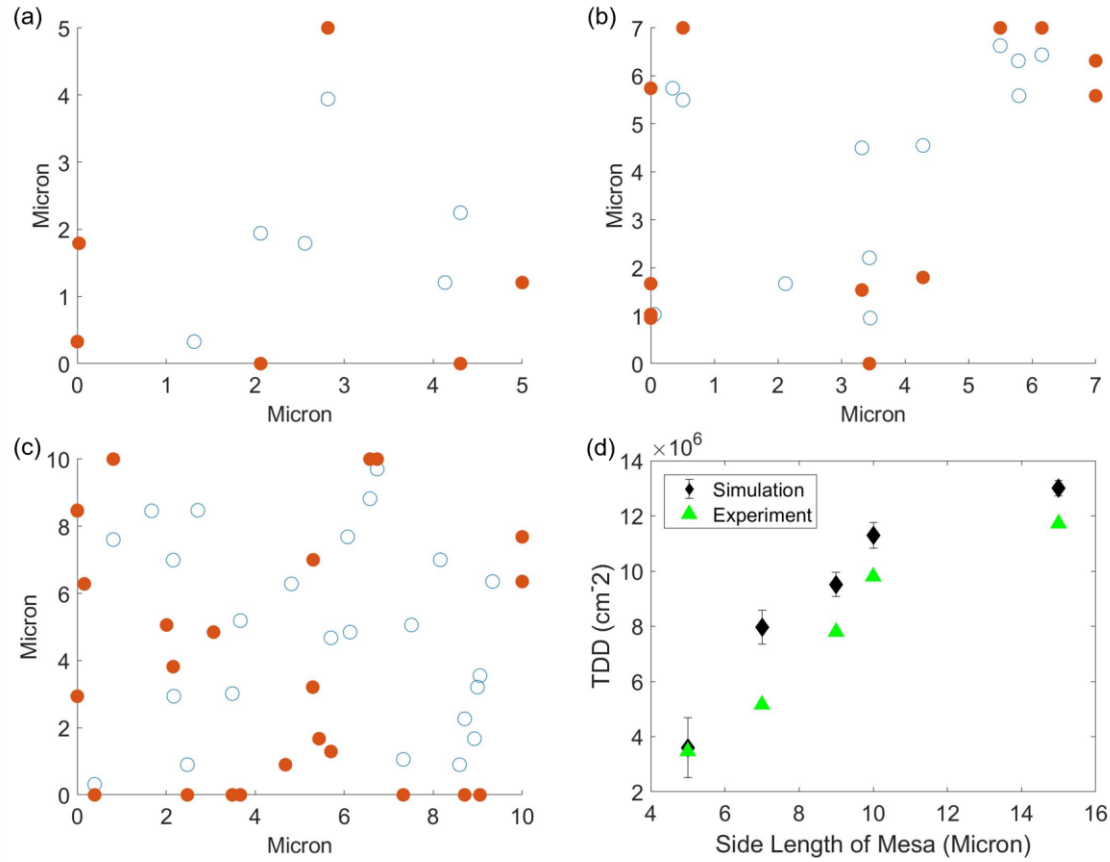

Figure 3.20: Results of dislocation pinning model for (a) 5 µm by 5 µm mesa (b) 7 µm by 7 µm mesa (c) 10 µm by 10 µm mesa and (d) average TDD for different mesa sizes. Unfilled circles are initial locations of threading dislocations and red circles are final locations of threading dislocations.

3.6 Summary and Outlook

In this chapter, a process flow was developed that achieved significant TDD reduction. Multiple possible causes of TDD reduction were explored: interface between high and low temperature Ge, mesa size, trench sidewall angle and trench depth. TEM results negated the existence of an interface between high and low temperature Ge. Dislocation trapping was observed along deep trenches and sidewall angle had no influence on TDD reduction. TDD was observed to increase with increase in side length of the mesa, which provides promises for small devices of high performance on Ge-on-Si virtual substrates.

While this chapter proposes a promising cause of TDD reduction (dislocations are pinned at the end of the SiO_2 layer), this hypothesis has not yet been experimentally confirmed. To confirm the hypothesis, a new process flow needs to be developed. Since the trench sidewall angle and trench depth are not major contributors to TDD reduction, dry etching can be excluded from the new process flow to reduce cost. A potential process flow is given in Table 5. The Ge overgrowth time should be varied to investigate the optimal thickness for effective TDD reduction and cost savings. TEM studies need to be performed on unpolished samples to confirm dislocation trapping.

Table 5: A potential process flow to confirm dislocation trapping mechanism

1	RCA clean, HF dip, rinse
2	Ge growth
3	SiO_2 deposition
4	Pattern SiO_2
5	Ge overgrowth
6	Cyclic annealing

CHAPTER 4

LATERAL MULTIJUNCTION PHOTOVOLTAICS

The previous chapter discusses the Ge-on-Si virtual substrate, which allows epitaxial growth of lattice matched III-V photovoltaics (PV) on top. Chapter 4.2 presents simulation results of the efficiency of lateral multijunction III-V photovoltaics based on a model developed by Broderick et al.[49] that assumes perfect spectrum splitting. Chapter 4.3 provides a more realistic projection of the performance of the lateral multijunction system with concentrator when overlapping of spots is taken into consideration. The standard spectrum for space applications is referred to as AM0. The AM1.5D spectrum is used for solar concentrator work in terrestrial applications.

4.1 From Tandem to Lateral Multijunction Solar Cells

Solar cells are composed of semiconductor materials that have a band gap between the valence band and conduction band. If an incoming photon has energy smaller than the band gap, it will transmit through. If the photon has energy greater than the band gap, it can promote an electron from the valence band to the conduction band, leaving a hole in the valence band. Photon energy in excess of the band gap will be lost as heat, which is called thermalization loss. In order to reduce thermalization loss, multijunction solar cells have been developed to split the incoming spectrum such that photons can be absorbed by the largest band gap subcell that can absorb it. Multijunction solar cells have primarily been realized in a tandem architecture where individual junctions are stacked on top of

each other. The material with the largest band gap is placed at the top of the structure to absorb photons of higher energy, while photons of energy smaller than the band gap will transmit through the first cell to the next cell with a smaller band gap. Since individual junctions are electrically connected in series, operation of tandem cells imposes a current matching restriction between junctions, which is limited by the smallest photocurrent generated in the subcell. The excess photocurrent generated in other subcells will be lost via recombination. Another constraint in tandem cells is lattice matching between each subcell, which limits materials selection and band gap combinations.[49] Research into tandem multijunction solar cells therefore leverages semiconductors of similar lattice constants: Ge, GaAs and InGaP.

In pursuit of higher efficiency, an alternative multijunction configuration where the subcells are connected in parallel has stimulated research interest in recent years.[50–52] The current matching constraint is eliminated because the subcells are connected in parallel. The lattice matching constraint is reduced because the subcells need not be lattice matched to each other. The choice of materials is hence increased, by allowing each subcell to be optimized independently of others. The lateral multijunction configuration uses spectrum splitting optics to direct photons of different wavelengths to subcells according to their band gaps. For decades, III-V materials have been commercially available and have achieved high efficiency in solar cell technology. III-Vs are a class of materials comprised of elements from group III and group V of the periodic table. In addition to having outstanding electronic and optical properties, thanks to the direct band gap, III-Vs can be grown in multijunction structures that allow for reduced thermalization losses and a resulting increase in efficiency. III-V solar cells have been used in space applications due

to their excellent radiation resistance and ability to perform well despite extreme temperatures, compared to crystalline silicon solar cells.[53]

To explore the benefits of lateral multijunction photovoltaics, we start by calculating the spectral efficiency of a three-junction system. The band gap combination is chosen based on lattice matching with commercially available substrates. As shown in Table 6, the InGaAs composition lattice matched to InP substrate has a band gap of 0.76 eV; GaAs lattice matched to Ge substrate has a band gap of 1.42 eV; the InGaP composition lattice matched to Ge substrate has a band gap of 1.88 eV. Spectral efficiency (SE) is defined as:

$$SE = \frac{\sum_{Egi} \int_{Egi}^{Egi+1} Egi \cdot \frac{dn}{dE} \cdot dE}{\int_0^{\infty} AM0(E)dE},$$

where dn/dE is the spectral flux density of AM0 standard spectrum in photons/cm^2·s·eV and E_{gi} is the band gap of the ith solar cell in the system.[54] This model predicts spectral efficiency of 68.5% for the three-junction system.

Table 6: Band gap and materials composition of III-V solar cells in the three-junction system

Band Gap (eV)	III-V
0.76	$In_{0.52}Ga_{0.48}As$
1.42	GaAs
1.88	$In_{0.51}Ga_{0.49}P$

For lateral junctions, each subcell receives a certain part of the solar spectrum directed to it by spectrum splitting optics. The efficiency of each subcell in the lateral junction under a certain solar spectrum is calculated using Matlab based on a model developed by Broderick et al.[49] The single-diode model is used to compute the current-voltage relation:

$$J = J_{ph} - J_0 \left[\exp\left(\frac{q(V+JR_S)}{nkT}\right) - 1\right] - \frac{V+JR_S}{R_{sh}} \quad (1)$$

Where V is the applied bias, J_0 is the reverse bias saturation current density, n is the diode ideality factor, q is the electronic charge, k is the Boltzmann constant, T is solar cell temperature, R_S and R_{sh} are the area normalized series and shunt resistance.[49]

First, the absorption spectrum A(λ) is obtained using the transfer matrix method for optical waves in multilayer structures.[55,56] Next, assuming perfect carrier collection and deducting 6% shadowing: the external quantum efficiency (EQE) spectrum is obtained from: EQE(λ) = A(λ) (1-6%), as shown in Figure 4.1.

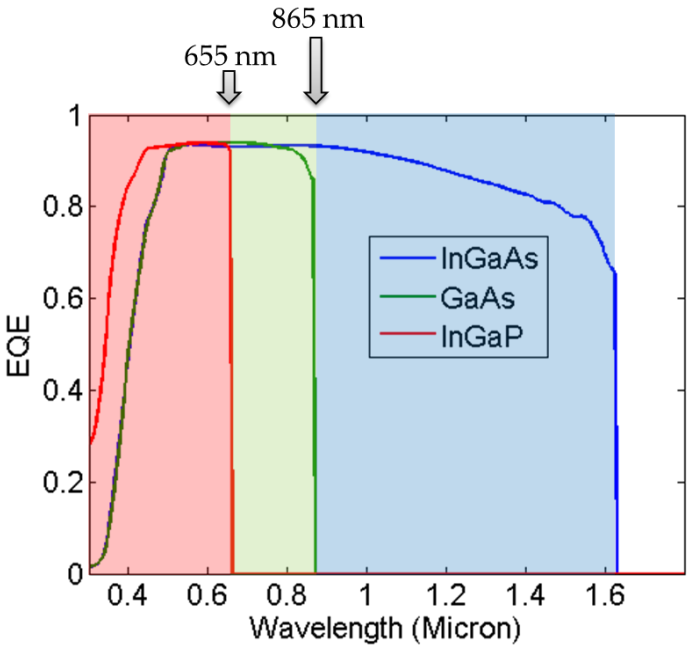

Figure 4.1: EQE spectrum of the lateral three-junction system. 6% shadowing is considered.

The subcell short circuit current density J_{ph} is calculated as: $J_{ph} = qC\int_{\lambda 1}^{\lambda 2} s(\lambda)\mathrm{EQE}(\lambda)\mathrm{d}\lambda$, where q is the electronic charge, C is the concentration factor, s(λ) is the incident photon flux at wavelength λ, λ_1 and λ_2 define the wavelength range allocated to that subcell.[49] At a certain current density J, the voltage V is calculated from Equation

1 and the power output P_{out} is $P_{out} = JV$. The optimal current density J_m and voltage V_m are found by scanning J to maximize P_{out}. The subcell efficiency η is: $\eta = \frac{J_m V_m}{C P_{in}}$, where P_{in} is the incident power under one sun. The total efficiency of the lateral junction is the sum of the efficiencies of each subcell. The optimal spectrum splitting wavelengths are found by searching for the values leading to the highest lateral junction efficiency. As shown in Figure 4.1, InGaP will absorb wavelength from 300 to 655 nm; GaAs will absorb wavelengths from 655 to 865 nm; InGaAs will absorb wavelengths from 865 to 1630 nm. Table 7 shows the band gap (E_g), open circuit voltage (V_{OC}), efficiency (η), fill factor (FF) and short circuit current density (J_{SC}) of each subcell of the three-junction system under AM0 spectrum 1 sun. The input subcell parameters are presented in Table 8.

Table 7: Output parameters for efficiency calculation of the three-junction system

	InGaP	GaAs	InGaAs	
E_g (eV)	1.88	1.42	0.76	
V_{OC} (V)	1.43	1.04	0.39	
η (%)	21.0	10.8	6.8	Sum: 38.6
FF	0.91	0.89	0.77	
J_{SC} (A/m^2)	201	146	280	

Table 8: Input subcell parameters for efficiency calculation of lateral multijunction solar cells

Parameter	InGaP	GaAs	InGaAs
J_0 (A/m^2)	1.4×10^{-22}	3.9×10^{-16}	6.6×10^{-5}
R_{sh} ($\Omega\ m^2$)	1600	450	142

4.2 Modeling Lateral Multijunction Photovoltaics with Concentrator

Another approach to boost the efficiency of solar cells is to raise the incident power by using concentrating optical elements. This technology is called concentrator photovoltaics (CPV). The solar cell area in CPV is comparatively small, thus saving expensive semiconductor materials.[57] Because of high current densities in CPV, solar cell cooling is an integral part of the design. The electrical performance of solar cells is

dependent on the operating temperature. When the temperature rises, the power output decreases due to a temperature dependent change in the band gap and therefore a drop in voltage with increasing temperature. In addition to the ongoing efforts in developing innovative cooling methods,[58] thermal management can be eased by miniaturization of the solar cell. If the surface area to volume ratio of the solar cell is high enough to allow efficient heat dissipation, the operating temperature will be essentially the same as that under the one-sun condition.[59] In this case, only passive or even no heat dissipation design is required, which simplifies the system integration and reduces costs. Therefore, the dimensions of the solar cells used in the simulation are scaled down, as shown in Table 9. InGaP, GaAs and InGaAs have the same width, which is 2.2 mm. InGaP is 2.5 mm in length; InGaAs is 1.2 mm in length; the length of GaAs is varied to optimize the efficiency. Typical photovoltaic concentrator cell sizes are on the order of 10 to 100 mm^2,[17] whereas the cell sizes used in the simulation are between 0.88 and 5.5 mm^2.

Table 9: Cell dimensions and concentration factors used in the simulation

	InGaP	GaAs	InGaAs
Cell Width (mm)	2.2	2.2	2.2
Cell Length (mm)	2.5	Varied	1.2
Concentration Factor	18	114 if cell length is 0.4 mm	38

In addition to shrinking the cell dimensions and incorporating the concentration factor into the simulation, Chapter 4.2 presents results based on a more realistic model than Chapter 4.1 that assumes an ideal spectrum splitting scenario where the spectrum is split perfectly according to the cell band gaps. It shall be noted that spectrum splitting is not perfect in reality due to solar beam divergence and optics aberration, which brings about overlapping of spots.[60] As shown in Figure 4.2a, when the cell length of GaAs is 0.9 mm, the crossover between the incident spectral intensities of InGaP and GaAs is around 500

nm, whereas the band gap of InGaP is at 655 nm. Changing the length of the GaAs subcell can optimize solar beam divergence. As shown in Figure 4.2b, when GaAs is reduced to 0.3 mm in length, the crossover between the incident spectral intensities of InGaP and GaAs is very close to the band gap of InGaP. Instead of a sharp drop at 655 nm as shown in Figure 4.1, the more realistic model in Figure 4.2 shows an overlap between the spectral intensities of InGaP and GaAs. Some photons of wavelengths longer than 655 nm fall into InGaP, but they do not have enough energies to promote electrons from the valence band to the conduction band. Some photons of wavelengths shorter than 655 nm are absorbed by GaAs, leading to higher thermalization loss than if they are absorbed by InGaP. Although loss due to overlapping of spots is inevitable, the efficiency of the three-junction system can be optimized by tuning the length of GaAs subcell, as shown in Figure 4.3.

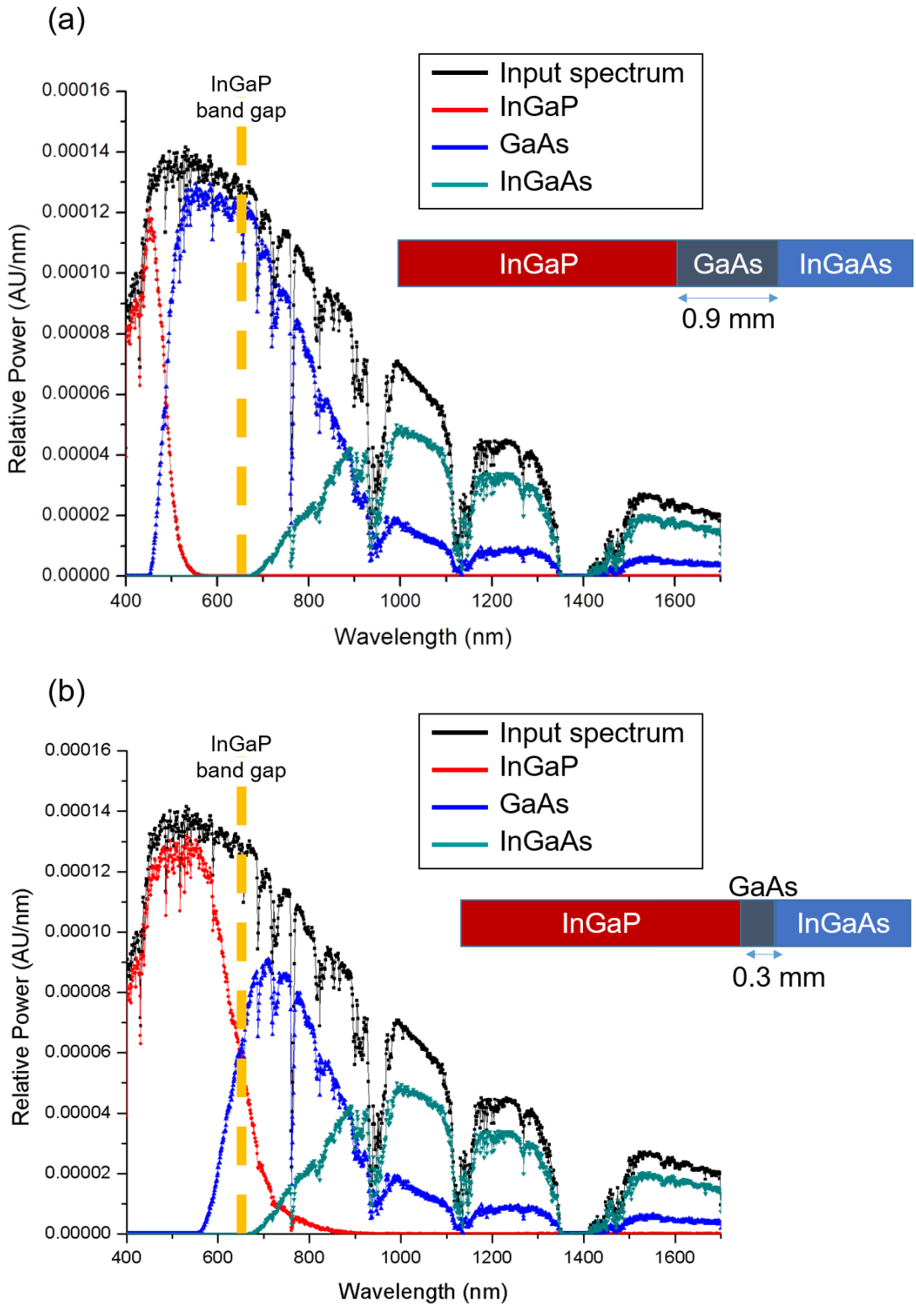

Figure 4.2: The incident spectral intensities of the three-junction system (a) GaAs is 0.9 mm in length (b) GaAs is 0.3 mm in length

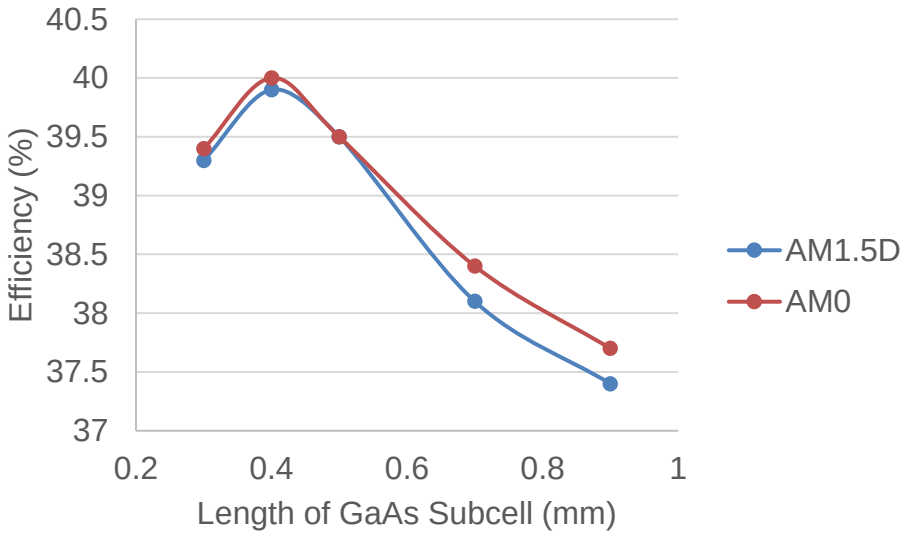

Figure 4.3: Efficiency of the three-junction system as a function of the length of GaAs subcell. The incident wavelengths range from 400 to 1700 nm. The concentration factor is given in Table 8.

-This work was done in collaboration with Dr. Duanhui Li and Dr. Tian Gu.

4.3 More Junctions = Higher Efficiency?

While single junction flat plate terrestrial solar cells are limited to about 30% efficiency, multiple junctions and concentrated light render higher efficiencies achievable. A recent study demonstrated a world record efficiency of 47.1% using a six-junction solar cell at 143 suns concentration.[61] Despite the general trend in PV technology to increase the number of junctions for higher efficiency, Li[60] reported that the lateral system will not gain substantial efficiency improvement by introducing more junctions, due to the reliance on optical elements for spectrum splitting.

In addition to overlapping of spots, another deviation from ideality comes from nonlinear spectrum splitting. As shown in Figure 4.4, the incoming spectrum is better split at shorter wavelengths than longer wavelengths. For instance, InGaP can only absorb

wavelengths from 400 to 655 nm. This part of the spectrum, however, is split across over half of the entire length of the three subcells.

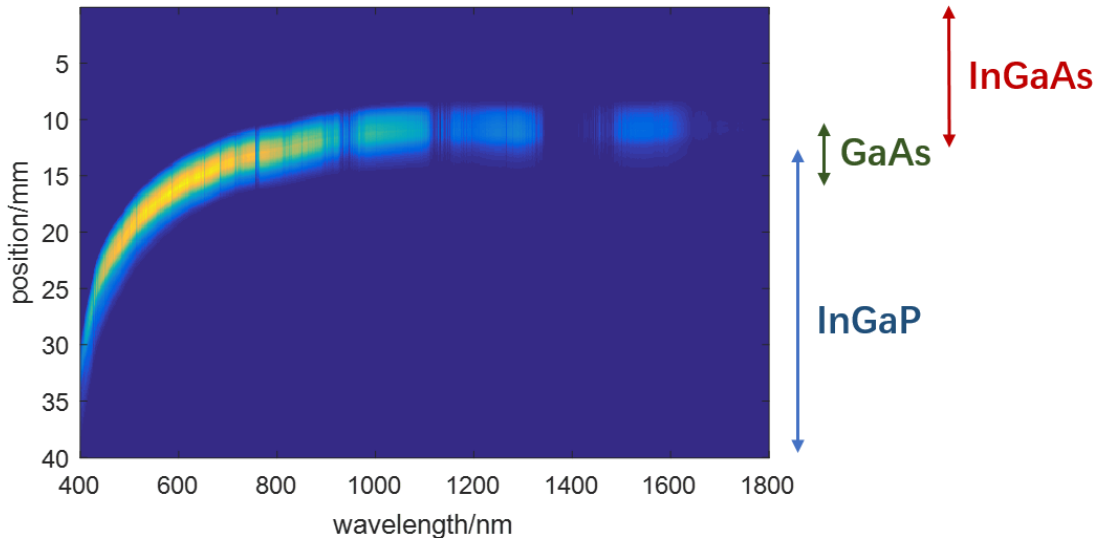

Figure 4.4: Nonlinear spectrum splitting of the optical element. The incoming spectrum is better split at shorter wavelengths.

To examine how nonlinear spectrum splitting affects solar cell efficiency, simulation was performed on a five-junction lateral system. The band gap combination, materials composition, and cell length are given in Table 10 and the spectra are given in Figure 4.5. The five-junction system shows a predicted efficiency of 47.9%, which is higher than that of the three-junction system.

Table 10: Band gap, materials composition and cell length of III-V solar cells in the five-junction system

Band Gap (eV)	III-V	Cell Length (mm)
0.76	$In_{0.52}Ga_{0.48}As$	4.1
1.42	GaAs	2.4
1.67	AlGaAs	1.5
1.88	$In_{0.51}Ga_{0.49}P$	2.3
2.19	$In_{0.25}Ga_{0.75}P$	18.3
Efficiency (%)	**47.9**	

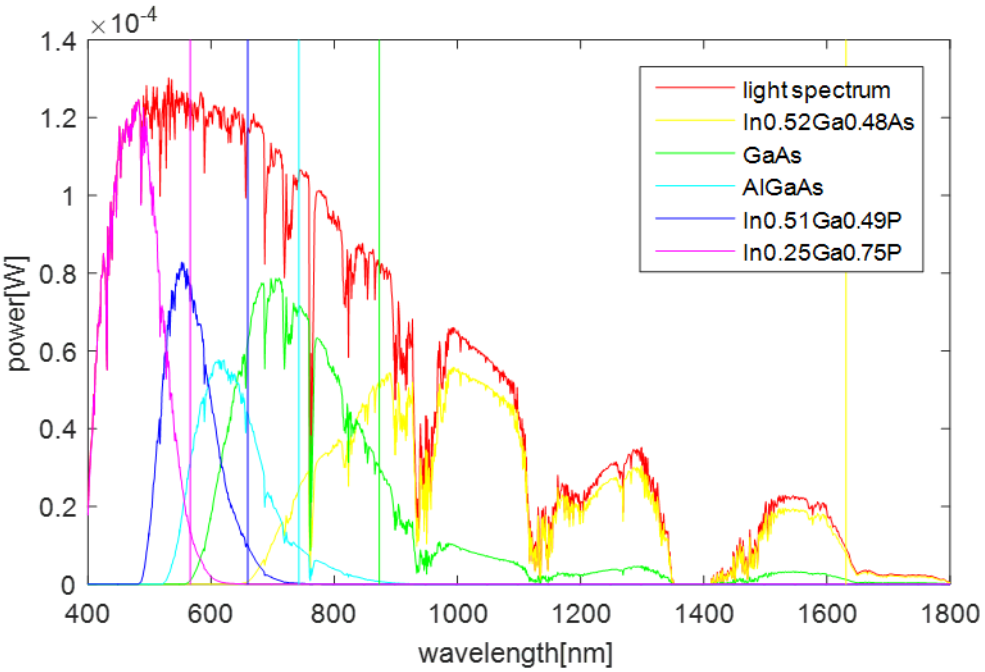

Figure 4.5: Spectra of the lateral five-junction system with defined materials. The red curve is the incoming spectrum. Curves of other colors are spectra that go to each subcell. The vertical lines correspond to the band gap combination.

Assume there is no constraint on materials selection, the band gap combination and cell length are optimized to achieve higher efficiency of 49.3% (Table 11). The spectra are shown in Figure 4.6. Nonlinear spectrum splitting and overlapping of spots due to the optical elements prevent the five-junction system from achieving higher efficiency.

Table 11: Optimized band gap combination and cell length of the five-junction system

Band Gap (eV)	Cell Length (mm)
0.93	4.1
1.37	2.4
1.73	2.4
2.04	3.6
2.42	16.7
Efficiency (%)	**49.3**

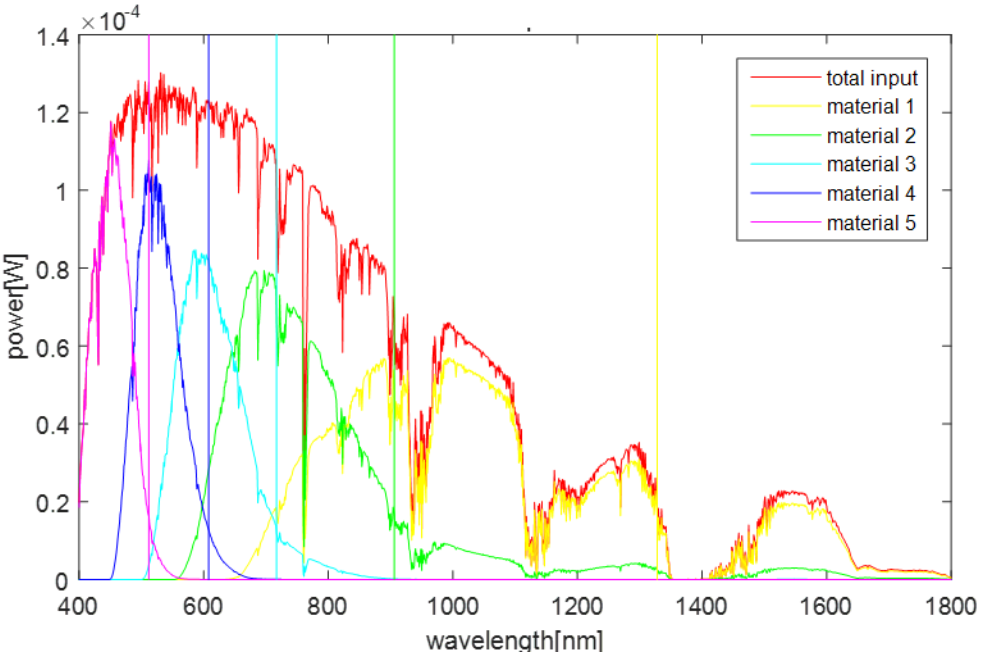

Figure 4.6: Spectra of the lateral five-junction system with optimized band gaps. The red curve is the incoming spectrum. Curves of other colors are spectra that go to each subcell. The vertical lines correspond to the band gap combination.

To overcome this limitation, we performed simulation on a hybrid four-junction system that consists of both lateral and tandem junctions. Tandem junctions do not count on optical elements for spectrum splitting and hence should be able to ease the loss due to dispersion. Lattice-matched GaAs/Ge tandem junction is incorporated into the lateral system for the simulation. As shown in Table 12, materials 1 and 2 are hypothetical semiconductors that have band gaps of 2.42 and 2.04 eV. Assume 100% absorption for Ge, the hybrid four-junction system shows a predicted efficiency of 49.1%, which is very close to the five-junction system with optimized band gaps. The spectra are shown in Figure 4.7.

Table 12: Band gap combination of the hybrid four-junction system

Band Gap (eV)	Material
2.42	1
2.04	2
1.42/0.66	GaAs/Ge

Efficiency (%)	49.1 (assume 100% absorption for Ge)

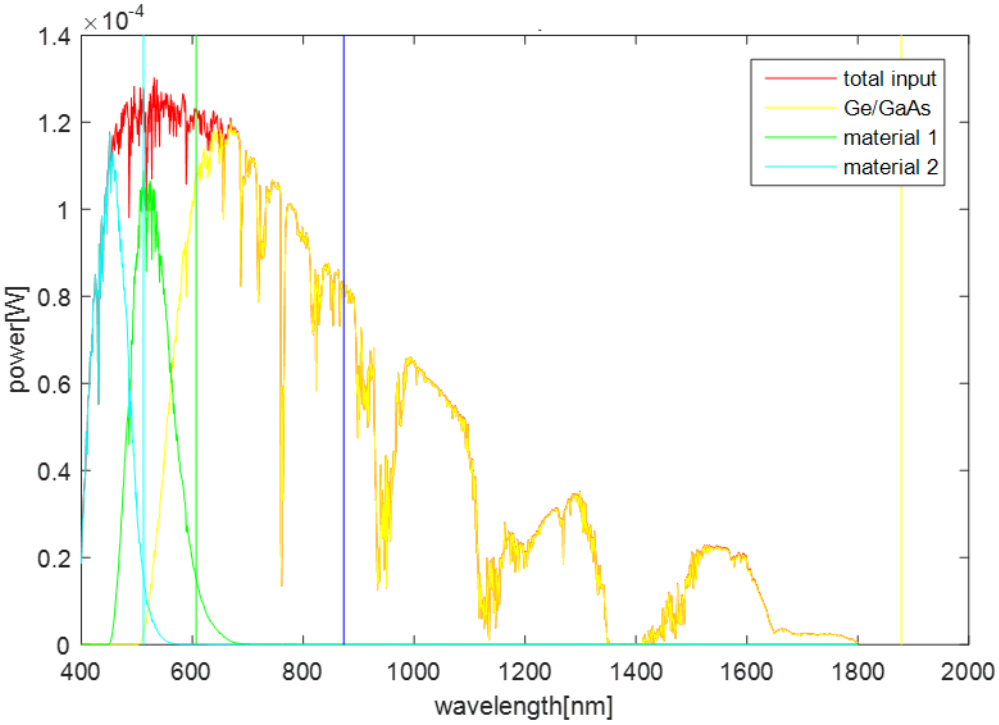

Figure 4.7: Spectra of the hybrid four-junction system. The red curve is the incoming spectrum. Curves of other colors are spectra that go to each subcell. The vertical lines correspond to the band gap combination (blue: GaAs, yellow: Ge).

-This work was done in collaboration with Ruihan Chen.

While tandem and lateral junctions have their advantages and drawbacks, our simulation results show that using a hybrid system has the potential to capture the best of both worlds. In addition to increasing the number of junctions and upgrading the optical elements for more efficient spectrum splitting, developing hybrid systems may evolve as a new avenue for boosting solar cell efficiency.

CONCLUSIONS AND FUTURE WORK

The focus of this thesis revolved primarily around identifying solutions to reduce the TDD in Ge-on-Si epitaxial films. Chapter 3 shows that Ge epilayers on Si substrates with trenches filled by Ge at a different temperature have very low TDD compared to blanket Ge epilayers on Si substrates. In order to unravel the causes of TDD reduction, two leading thesis questions were explored:

1) Is there an interface between high and low temperature Ge?

2) Do the trench sidewall angle and trench depth have an influence on dislocations?

Selected area diffraction and cross sectional TEM results did not show an interface between high and low temperature Ge. Trench sidewall angle had no influence on TDD reduction and dislocation trapping was observed along deep trenches. Since deep trenches require long etching time and extended growth duration, it is not a cost-effective approach. As mesa side length increases, the average required distance for a threading dislocation to glide to the mesa edge increases and hence TDD reduction becomes less significant. This enables small devices of low TDD. To create a large area, thin Ge film on Si of low TDD, SiO_2 should be deposited on Ge where dislocations are trapped. Since Ge does not grow on SiO_2, a subsequent lateral overgrowth of Ge will avoid the area where dislocations are trapped. According to Wen et al.[42], no dislocations were generated during coalescence and subsequent annealing in the Ge layer above the oxide. This should give us an almost perfect Ge top layer of large area. While Chapter 3 suggested a promising source of dislocation sink where dislocations were pinned at the SiO_2 openings, this hypothesis needs experimental substantiation. TEM studies should be performed on unpolished samples to confirm dislocation trapping. The Ge overgrowth time should be varied to investigate the optimal thickness for effective TDD reduction and cost savings. Cost analysis is critical because it serves as a roadmap for optimizing the process flow.

Chapter 4 compares the concepts of tandem and lateral multijunction photovoltaics. In a tandem multijunction system, the number of subcells is limited by the number of materials that are lattice matched to each other. Whereas in a lateral multijunction system, lattice matching is only needed between the subcell and its virtual substrate. The potential of lateral multijunction photovoltaics is demonstrated through simulation approaches.

Despite the room left for optimization in the process flow developed in Chapter 3, this thesis demonstrates high quality Ge-on-Si virtual substrate with low TDD. This renders Ge_xSi_{1-x}-on-Si virtual substrates possible, since the lattice mismatch between Ge_xSi_{1-x} alloys and Si is smaller than that between pure Ge and Si. The 4.2% lattice mismatch enables access to virtual substrates of various lattice constants and hence unlocks the potential for growing solar cells of various band gaps. If these solar cells are arrayed in a lateral configuration where each subcell has its own virtual substrate, researchers will be able to push the limit of the number of junctions and hence realize more efficient spectrum splitting.

APPENDIX A

PROCESS RECIPE AND MATLAB CODE

This appendix includes detailed process recipe as described in Figure 3.1 and Matlab code of the Monte Carlo simulations in Chapter 3.5. The notes relate to the specific tools at MIT's Microsystems Technology Laboratory (MTL) and MIT.nano fabrication facilities.

The process recipe for Figure 3.1 is as follows and the starting material is a 150 mm silicon wafer:

1. rca clean + HF dip: rca-ICL

2. Germanium growth at 730℃: UHVCVD in SEL

3. Oxide deposition: DCVD

4. Backside oxide deposition: DCVD

5. Coat SPR700: pTrack

6. Expose: i-stepper

7. Develop wafer: pTrack

8. Oxide dry etch: AME5000

(a) Recipe: BA_OX_TRENCH

(b) Etch time: 40 sec

9. Germanium dry etch: AME5000

(a) Recipe: BA_SI,GE

(b) Etch time: 100-200 sec

(c) Etching is not selective between silicon and germanium, which explains the overetch in silicon

10. Ash photoresist: asher-ICL

(a) 3 minutes plasma

11. Germanium sidewall clean: premetal-Piranha

(a) 30 sec 1:3 H_2O_2:H_2O

(b) Rinse

(c) 10 min 1:5 H_2SO_4:H_2O

(d) Rinse

(e) 30 sec 1:50 HF:H_2O

(f) Rinse

12. Germanium growth at 450℃: UHVCVD in SEL

13. CMP: GnP in MIT.nano

(a) Slurry: W2000. 1:3 slurry:DI water + 1 wt% H_2O_2

14. Post-CMP clean and oxide strip: premetal-Piranha

(a) 10 min 1:5 H_2SO_4:H_2O

(b) 4 min 1:50 HF:H_2O

The Matlab code of the Monte Carlo simulations in Chapter 3.5 is as follows:

```
function DislPinn(s,n)
% s is side length of mesa in micron
% n is the number of dislocations in the mesa
xi = rand(n,1)*s;
yi = rand(n,1)*s;
% The rand function creates a 1D array of random numbers
between 0 and 1
% (xi,yi) is the initial location of each threading
dislocation
```

```
T=linspace(1123.15,923.15);
% cyclic annealing between 650C and 850C
a_Si=3.725*10^-6*(1-exp(-5.88*10^-3*(T-124))+5.84*10^-4*T);
% thermal expansion coefficient of Si
a_Ge=(5.04+3.79*10^-3*T-3.5*10^-7*T.^2)*10^-6;
% thermal expansion coefficient of Ge

% calculate thermal strain
et=0;
for i=2:100
det=(a_Ge(i)-a_Si(i))*(T(i-1)-T(i));
et=et+det;
end

% calculate average glide distance per dislocation to
completely relieve the thermal strain
b=2e-8;% in cm
N=2.5e7;% cm^-2
l_ave=et/b/N*10^4;% in micron
mu=-0.035*s^2+0.45*s+1.6;

% assume the glide distance of each threading dislocation
follows a normal distribution
l1=linspace(0,l_ave);
p1=normpdf(l1,mu);
P1=round(p1*n/2);
l2=linspace(-l_ave,0);
p2=normpdf(l2,-mu);
P2=round(p2*n/2);

% Half of the dislocations glide in the x direction
% Half of the dislocations glide in the y direction
vx=xi(1:n/2);
vy=yi(1:n/2);
hx=xi(n/2+1:n);
hy=yi(n/2+1:n);

c=ones(n/2,1);
d=ones(n/2,1);

k=1;
for i=1:100
if k<=n/2
if P1(i)>0
for j=k:k+P1(i)-1
if j<=n/2
```

```
vy(j)=vy(j)+l1(i);
end
end
k=k+1;
end
end
end

k=1;
for i=1:100
if k<=n/2
if P1(i)>0
for j=k:k+P1(i)-1
if j<=n/2
hx(j)=hx(j)+l1(i);
end
end
k=k+1;
end
end
end

vx2=[];
vy2=[];
hx2=[];
hy2=[];

for i=1:n/2
if vy(i)>s
vy(i)=s;
else
vy2=[vy2 vy(i)];
vx2=[vx2 vx(i)];
c(i)=0;
end
if hx(i)>s
hx(i)=s;
else
hx2=[hx2 hx(i)];
hy2=[hy2 hy(i)];
d(i)=0;
end
end

% 2nd anneal half cycle
k=1;
for i=1:100
```

```
if k<=length(vy2)
if P2(i)>0
for j=k:k+P2(i)-1
if j<=length(vy2)
vy2(j)=vy2(j)+l2(i);
end
end
k=k+1;
end
end
end

k=1;
for i=1:100
if k<=length(hx2)
if P2(i)>0
for j=k:k+P2(i)-1
if j<=length(hx2)
hx2(j)=hx2(j)+l2(i);
end
end
k=k+1;
end
end
end

j=1;
for i=1:n/2
if c(i)<1
vy(i)=vy2(j);
if vy(i)<0
vy(i)=0;
end
j=j+1;
end
end

j=1;
for i=1:n/2
if d(i)<1
hx(i)=hx2(j);
if hx(i)<0
hx(i)=0;
end
j=j+1;
end
end
```

```
xf=[vx;hx];
yf=[vy;hy];
% (xf,yf) is the final location of each threading dislocation

scatter(xi,yi,100)
hold on
scatter(xf,yf,100,'fill')
axis([0 s 0 s])
ax = gca;
ax.FontSize = 16;
xlabel('Micron','FontSize',16)
ylabel('Micron','FontSize',16)
hold off
```

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