

Design of a Phi-2 and a Class E Inverter for Underwater Systems

by

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B.Sc., Massachusetts Institute of Technology (2018)

Submitted to the Department of Electrical Engineering and Computer Science

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Abstract

In Autonomous Underwater Vehicles (AUVs), many potential failure modes exist due to pressure housing and the need for connections between different pressure housings. Waterproof connectors do exist but drive up the price and weight of underwater systems, a costly disadvantage as mass and volume are at a premium for an underwater system. If we can remove the necessity for physical connectors, we can design cheaper, more robust submarines. This can be done with wireless power transfer (WPT), which can transmit power efficiently across mediums within the submarine, therefore eliminating the need for physical connections and making underwater systems more compact and light-weight.

The thesis presents two WPT systems for an AUV with two different inverters that convert DC power to AC power that drive the WPT system. The first system presented uses a Class E Inverter, a common topology for DC-AC conversion, and the second system utilizes a Phi-2 Inverter, a topology that uses the inherent parasitic capacitances to substitute for physical components. The WPT system utilizes magnetic resonance coupling to transmit power from transmitter coils attached to the inverters to receiver coils attached to a load through a rectifier. Simulations show that, when correctly tuned, the two designs can give comparable performance in power transfer efficiency and range. The choice of design is likely to be decided by a combination of the size and weight of the finished system, along with the ease of design.

Thesis Supervisor: James Bales
Title: Instructor

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Chapter 1

Introduction

The development of electronics for underwater environments is limited because of its price and weight. Connectors between pressure housings introduce many failure modes and increase the price and weight of the system, leading to the need for more power. In addition, an efficient method of inverting the DC power source to AC power is necessary. This thesis explores two different inverters combined with the wireless power transfer (WPT) coils and a rectifier. The system block diagram is shown in Figure 1-1.

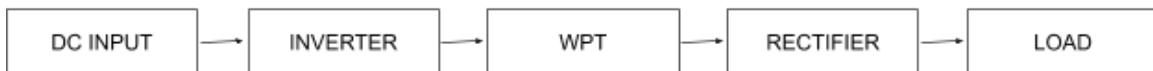


Figure 1-1: System Block Diagram.

Using a simulation based comparison of two systems, this thesis explores two major issues: the elimination of connectors using WPT, and the development of complementary inverters for the WPT systems.

1.1 Wireless Power Transfer

Most of the papers surveyed in this introduction revolved around magnetically resonant coupling (MRC), which is generally agreed on to be the most efficient type

of wireless charging for power transfer in the range where the transmission distance between the power source and the load is greater than the dimensions of the coil resonators [1].

This introduction will first provide a background on non-radiative power transfer via MRC, then explain some of the other types of wireless charging, and review current papers in the field. Then, this introduction will illustrate a model used for WPT and explain the derivation of efficiency of the WPT module.

1.1.1 Background

[1], [2], and [3] provide a summary of magnetic resonance, which works by oscillating energy between the parasitic capacitance and inductive elements of the coil. The transmitting and receiving coils are tuned to operate in the same resonance mode by using the parasitic capacitance of the coil's windings. MRC systems typically require a high frequency operation region (usually in the low MHzs), but can range from 10kHz to 200MHz through the use of low winding resistance (usually involving Litz wires that reduce the skin effect and proximity effects), and high Q. The most common MRC WPT configuration is a four coil system made up of a Power Driving Coil attached to the power source, a Sending Resonator, a Receiving Resonator, and a Load coil attached to the load. These coils are current-carrying copper coils. The transmitter emits a non-radiative magnetic field resonating at a specific frequency and the receiver receives this field. The first self-resonant frequency of the coil is the lowest frequency at which the inductor resonates with its self capacitance. For this thesis, a two coil system was selected because the requisite impedance matching could be accomplished with a two coil system.

There are two fundamental metrics of power transfer: Maximum Power Transfer (MPT) and Maximum Energy Efficiency (MEE). These two metrics for WPT have different operating points.

MPT transfers the maximum amount of power between the transmitting and receiving coil at the expense of system energy efficiency. It should be used in applications where system energy efficiency is not the main concern. Much recent mid-range

WPT research revolves around this concept. MPT maximizes transmission distance but energy efficiency can not exceed 50%. This is because the impedance of the source must be matched with the impedance of the load for maximum power transfer; therefore, at least half the power is lost to the fixed source impedance. While MPT maximizes transmission distance, it was not studied in this thesis because of its limited efficiency.

MEE, on the other hand, can achieve a very high efficiency by using a power source with a very small source impedance. The only type of losses are conduction losses due to AC resistances of the coil and power losses due to the source resistance. MEE relies on high magnetic coupling coefficients between the transmitting and receiving coils, which increase with the quality factor, Q , and decrease with the transmission distance. For MEE, the reactance of the parasitic capacitance cancels the positive reactance of the leakage inductance, which reduces the impedance of the power flow path from the power source to the output.

1.1.2 Basic Review of other WPT Technologies

The two most common techniques are MRC power transfer, which is used for mid range transfer and has freedom of position, and inductive power transfer (IPT), which can be used to charge low power devices at a very short range only. IPT is not flexible with misalignment and can not simultaneously transmit power to multiple devices, unlike MRC [4].

IPT is used for near field transfer, where the radius of the coil is much smaller than the wavelength. The efficiency falls off from the transmitter at a distance proportional to $1/d^3$, where d is the distance from the transmitter. Therefore, IPT is extremely efficient at close distances. With mid range and far range power transfer, the electromagnetic field is constantly drawing energy whether the energy is immediately received or not [5].

IPT has been popularized by the Wireless Power Consortium (WPC), an organization made up of over 200 companies that established the Qi standard. Qi supports wireless power transfer of up to 5 W over distances up to 5 mm, but is being quickly

extended to deliver up to 15 W, and after, to 120 W over much larger distances. The Power Matters Alliance (PMA) standard is very similar to the Qi standard; it also relies on inductive power transfer, but uses a different communication method and a different frequency range. Alliance for Wireless Power (A4WP) was developed as a competitor to WPC. Its standard, Rezence, relies on magnetic resonance and consists of a single power transmitter unit and one or more power receiver units. A4WP and PMA merged together to create the Airfuel Alliance, which allows up to 50W of power using magnetic resonance with loose coupling, tightly tuned coils, and a high Q [6].

1.1.3 Basic Review of Current WPT Papers

In [7], Marin Soljagic and his team of researchers transmitted 60W of power across 2m using MRC, showing a greater efficiency of transfer with a longer distance. They used self-resonant coils in the strongly coupled regime, showing power transfer 8x the distance of the radius of the coils. Self resonant coils rely on distributed inductance and distributed capacitance to achieve resonance. Two resonant objects of the same resonant frequency tend to exchange energy efficiently while dissipating little energy in other objects, irrespective of the geometry of the surrounding space. It is essential for the coils to be on resonance for WPT to be practical; some materials between the transmitting and receiving coils may shift the resonant frequency.

Soljagic achieved 40% transmission efficiency, but 15% source to load efficiency. This research spun out into a company called Wittricity, which delivers power at distances. Their setup is shown in Figure 1-2.

In [8], design considerations for an asymmetrical 4 coil MRC setup were defined for either a target efficiency or a target range. A method to optimize coil parameters, including Q and various different coupling coefficients, was provided. In this paper, the authors showed that there is an overcoupled region for which the efficiency is constant for a range of distances between the transmitting and receiving coils. As the region extends, a tradeoff between the efficiency and range starts to exist. This paper showed that many different coil geometries can achieve the same Q and that a

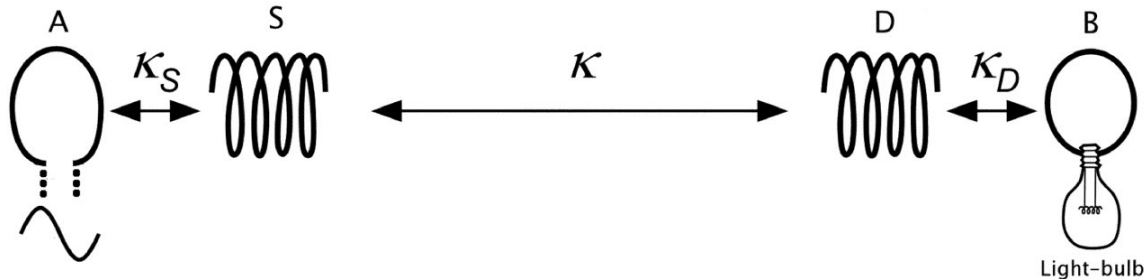


Figure 1-2: Experimental Setup. A and S and D and B are inductively coupled together, while S and D are magnetically coupled together with resonance.

broad range of coil parameters and angular misalignments can have the same coupling characteristics. The general behavior for any set of MRC systems can be modeled by characterizing the Q and coupling characteristics.

[9] analytically derived equations that the geometry of helices must satisfy in order to maximize efficiency for MRC systems. This paper reiterated much of the background explained already and mentioned how the transmitting and receiving coil exhibit a resonant frequency that coincides with the frequency where the Q factor is at its maximum.

In order for high efficiency to be reached, the transmitting and receiving coils must be designed so that they resonate at the desired operating frequency, which must be the same as the frequency where the transmitting and receiving coils have maximum Q. Resonant objects exchange energy efficiently while non resonant objects have weak interactions.

MCR elements can deliver power efficiently over large distances because of the maximum Q factor at the self resonant frequency, which is achieved through distributive capacitances and inductances.

1.1.4 WPT Model

For this thesis, we model the magnetic resonance coupling systems using a basic two-port impedance matrix based off of [10]. Capacitances are used to resonate out the inductances in the model. Below is the two-port impedance model, where M is the

mutual inductance between the two coils which occurs when the flux generated by the first, or transmitting, coil affects the second, or receiving, coil. Each coil has an inherent resistance, capacitance, and inductance. On the left in Figure 1-3 is the transmitting coil and on the right is the receiving coil. L_1 and L_2 represent physical inductances associated with each coil in isolation– these values are what would be measured if no current flows in the other coil. R_1 and R_2 are the parasitic resistances of the coils.

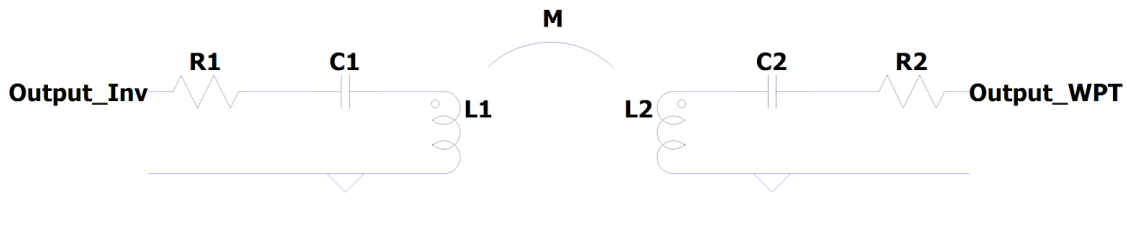


Figure 1-3: Two-port impedance model for WPT.

The coupling coefficient, k , is related to M and can be used interchangeably to characterize the degree of coupling. The coupling coefficient is characterized as "the closeness with which the magnetic fields of the two circuits are interlinked. If there were no magnetic leakage, the coefficient of coupling k would be unity, which is its greatest possible value" [11].

$$k = \frac{M}{\sqrt{L_1 L_2}} \quad (1.1)$$

Based on Figure 1-3, the following impedances can be derived:

$$Z_{11} = R_1 + j\omega L_1 - \frac{j}{\omega C_1}, \quad (1.2)$$

$$Z_{22} = R_2 + j\omega L_2 - \frac{j}{\omega C_2}, \quad (1.3)$$

$$Z_{12} = j\omega M. \quad (1.4)$$

The input impedance can be computed with a load resistance R_L on the output

of the WPT module.

$$Z_{\text{in}} = Z_{11} - \frac{Z_{12}^2}{Z_{22} + R_L}. \quad (1.5)$$

Setting C_1 to resonate out L_1 and setting C_2 to resonate out L_2 , we arrive at the following:

$$Z_{11} = R_1, \quad (1.6)$$

$$Z_{22} = R_2, \quad (1.7)$$

$$Z_{12} = j\omega M. \quad (1.8)$$

After some rearranging, the input impedance Z_{in} becomes

$$Z_{\text{in}} = R_1 - \frac{(j\omega M)^2}{R_2 + R_L} = R_1 + \frac{(\omega M)^2}{R_2 + R_L}. \quad (1.9)$$

Assuming ideal components with no parasitic resistance, $R_1 = R_2 = 0$ and so

$$Z_{\text{in}} = \frac{(\omega M)^2}{R_L}. \quad (1.10)$$

With some manipulation:

$$M = \frac{\sqrt{Z_{\text{in}} R_L}}{\omega}. \quad (1.11)$$

Substituting into (1.1),

$$k\sqrt{L_1 L_2} = \frac{\sqrt{Z_{\text{in}} R_L}}{\omega}. \quad (1.12)$$

Finally, we arrive at

$$L_1 L_2 = \frac{Z_{\text{in}} R_L}{(\omega k)^2}. \quad (1.13)$$

Additionally, the relationship between k and the distance between the coils, d , is illustrated below:

$$|k| = \frac{1}{\left(1 + \frac{2^{2/3} d^2}{a_1 a_2}\right)^{3/2}} \quad (1.14)$$

1.1.5 Efficiency of Coils

In order to find the efficiency of the WPT, the resistance and Q factors of the coils must be calculated. The resistance is the sum of the AC resistance and the DC resistance and can be calculated using the following equation [12]:

$$R = \frac{L\rho}{\pi D\delta}, \quad (1.15)$$

where R is the resistance, L is the length of the wire, ρ is the resistivity, D is the diameter, and δ is the thickness of the skin effect. This equation can be used with the assumption that the diameter is large compared to the thickness of the skin effect. The effective resistance due to a current at the surface of a large conductor can be calculated assuming direct current flows uniformly through a conductor with a thickness δ .

For the equations below, ω is $2\pi Fs$, L_1 is the inductance of the transmitting coil, R_1 is the resistance of the transmitting coil, and R_s is the source resistance, which is assumed to be 0Ω . L_2 is the inductance of the receiving coil, R_L is the load resistance of the rectifier, and R_2 is the resistance of the receiving coil.

The Q-factor of the first coil can be found with the following equation:

$$Q_1 = \frac{\omega L_1}{R_1 + R_s}. \quad (1.16)$$

The Q-factor of the second coil can be found with the following equation:

$$Q_2 = \frac{\omega L_2}{R_L + R_2}. \quad (1.17)$$

The efficiency of the WPT module can be found with:

$$\eta = \frac{R_L}{R_2 + R_L} \left(\frac{1}{1 + \frac{1}{k^2 Q_1 Q_2}} \right). \quad (1.18)$$

1.2 Inverter Topology Design

1.2.1 Class E

The Class E Amplifier is known for its high efficiency, especially at high frequencies, straightforward, simple design, and reduced sensitivity to active-device characteristics [13]. It is designed to have a transient response that maximizes efficiency, even if the duty cycle is very high. However, conventional Class E Inverters are very load-dependent—only able to maintain zero voltage switching (ZVS), critical for maximum power efficiency, over a small range of load resistances. The traditional single-switch Class E inverter is commonly used for frequencies above 10Mhz [14]. This traditional inverter can be seen below, in Figure 1-4.

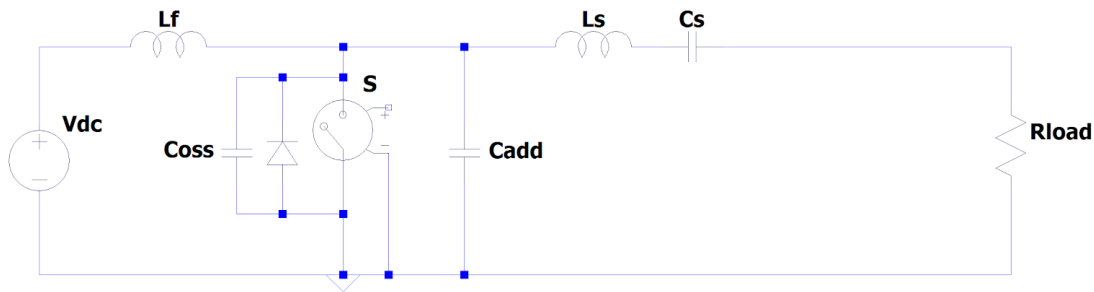


Figure 1-4: Traditional Class E inverter topology.

Here, the input inductor L_f serves as a choke and the tuned load network, composed of components C_f , L_s , C_s , and R , is chosen to deliver power to the load resistor, shape the drain to source voltage to provide ZVS, and achieve zero dv/dt across the switch to maximize efficiency. C_f is the sum of C_{oss} and C_{add} shown in the figure. The traditional inverter is extremely load dependent because of the load resistor's wave shaping property; the efficiency drops off when the resistance varies as the inverter strays from ZVS [15] [16].

While some applications do not require a wide range of resistive loads, many inverters require load sensitivity to maintain high efficiencies. Techniques such as resistance compression networks compensate these variations but increase loss and price. Applications that require a wide range of load resistance include outphasing

inverter systems and DC-DC converters. Outphasing inverter systems control power by utilizing phase-shift control of multiple inverters. The effective impedance, and therefore the output power, seen by the output of the inverter can be varied with control angle, a control scheme called load modulation [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28]. Class E inverters for these applications with wide ranges of load resistances are difficult to design.

For this thesis, a methodology that allows straightforward design of a load-independent Class E inverter introduced by Roslaniec and Perreault was utilized. This load-modulation methodology requires a fixed frequency and maintains ZVS switching and a constant duty cycle. However, to allow for flexibility, this design procedure does not maintain zero dv/dt switch turn off as the load changes.

This topology is shown in Figure 1-5. It includes a single switch and a parallel-tuned output filter network composed of C_p and L_p , which is used to shape the output waveform.

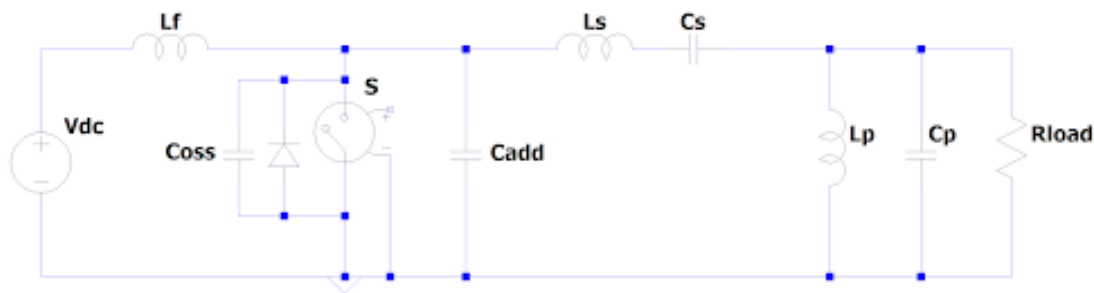


Figure 1-5: Class E topology with added parallel network.

The goal of this design is to select the input network parameters, L_f and C_f , and the output network parameters, L_s , C_s , L_p , and C_p . C_f , the total input capacitance, is composed of the switch's output capacitance, C_{oss} , and any additional capacitance. All components are assumed to be linear—the switch's capacitance does not vary with voltage with this assumption [29], [30]. To perform well with load modulation, the load network impedance, Z_L , (the impedance of the output network plus the load), also known as the input impedance of the load network, should stay resistive as the load resistance changes [14]. This means that in a plot of impedance versus frequency,

the impedance of the load network should resemble a fairly flat line with a slope near 0.

Theory of Class E

The Class E inverter implemented for this thesis was designed following the steps below in [14]:

1. Pick the switching frequency F_s , rated output power P_{or} , and a load resistance range from minimum rated load resistance to maximum rated load resistance.
2. Calculate the RMS output voltage amplitude, the RMS output current amplitude, and the DC input voltage.

$$\frac{P_{or}R}{V_{dc}^2} = 1.32 \quad (1.19)$$

$$V_{or} = \sqrt{P_{or}R_{or}} \quad (1.20)$$

$$I_{or} = \frac{P_{or}}{R_{or}} \quad (1.21)$$

$$V_{dc} = \frac{V_{or}}{1.15} \quad (1.22)$$

3. Select Q factors for sufficient filtering for both the parallel and series network. For example, the parallel network, L_p and C_p , provides high filtering for the maximum resistance load, while the series network, L_s and C_s , highly filters out for the minimum resistance, or rated resistance. The mid range of the load modulation, near the geometric mean of the largest and smallest resistive loads, will rely on a combination of both filtering schemes. Use the following equation with $Q_{fil} = 5$ to for sufficient filtering:

$$\frac{\sqrt{L_s/C_s}}{R_{min}} = \frac{R_{max}}{\sqrt{L_p/C_p}} = Q_{fil} \quad (1.23)$$

4. Choose the parallel and series components of the output network to be resonant at the switching frequency. Choose these impedances such that the output

voltage is filtered across the entire load modulation range.

$$\frac{1}{\sqrt{L_p C_p}} = \frac{1}{\sqrt{L_s C_s}} = 2\pi F_s \quad (1.24)$$

$$C_s = \frac{1}{2\pi F_s Q_s R_{or}} \quad (1.25)$$

$$L_s = Q_s^2 R_{or}^2 C_s \quad (1.26)$$

$$L_p = \frac{10 R_{or}}{2\pi F_s Q_p} \quad (1.27)$$

$$C_p = \frac{Q^2 L_p}{R_{or}^2} \quad (1.28)$$

5. Tune the input network, L_f and C_f , to slightly below $1.5\times$ the switching frequency. Start by tuning it at $1.5\times$ exactly. Increase C_f if switching conditions are not sufficient.

$$\frac{1}{\sqrt{L_f C_f}} = 3\pi F_s \quad (1.29)$$

$$F_f = 1.5 F_s \quad (1.30)$$

6. Select the characteristic impedance of L_f and C_f using the rated or minimum load resistance. Here, k_f is typically between 0.5 and 1.5. Use higher values of k_f to increase the characteristic impedance and reduce the input network's resonating losses. Use lower values of k_f to allow for higher C_f values and therefore higher value of C_{oss} . This allows more flexibility when choosing switches. Lower k_f values are useful in lowering the value of L_f , allowing the inverter to respond faster to operation changes. Approach this by starting with the smallest value of k_f and increase it until ZVS is no longer maintained across the load range. This will allow for the smallest amount of capacitance and sufficient response

time.

$$\sqrt{\frac{L_f}{C_f}} = k_f R_{\min} \quad (1.31)$$

$$Z_{\text{char}} = 0.7 R_{or} \quad (1.32)$$

$$C_f = \frac{1}{2\pi F_f Z_{\text{char}}} \quad (1.33)$$

$$L_f = C_f Z_{\text{char}}^2 \quad (1.34)$$

1.2.2 Phi-2

The second inverter explored in this thesis is the Phi-2 Inverter, a switched mode resonant inverter that operates most efficiently at very high frequencies (VHF). This inverter is known for its rapid turn on and turn off time, low switch voltage stress, and small energy storage requirements for its passive components. The Phi-2 also has a quick dynamic response and flexibility in its design [31]. It achieves these characteristics using a tuned resonant network that achieves ZVS.

Resonant inverters that switch at very high frequencies can be used for numerous applications, such as high-efficiency DC to DC converters [32], [33], [34], [35], RF power amplifiers [36], [13], [37], and induction heating and plasma generation [38], [39]. The Phi-2's small passives, ZVS, and low voltage stress make it an excellent candidate for applications that require high frequency operation at a fixed frequency and duty cycle. The use of smaller components is particularly suitable for underwater applications, with limits the size and weights of its systems.

Class E, E/F, and Phi inverters fall under the category of tuned switch mode inverters. These inverters operate by exciting resonant networks at very high frequencies. The Class E, for example, switches a resonant network at a very high frequency [15] to achieve ZVS and achieve a slow gating waveform using one ground-referenced switch. Device parasitics are built into the Class E's operation. These benefits make the Class E inverter a popular choice for various applications such as RF DC converters [31].

The Phi-2 inverter has certain advantages over the Class E Inverter and other existing designs. Fast transient response is critical in applications requiring fast dynamic response and on/off control [35] [40] [41]. The Class E Inverter is limited by its large input inductor, which stores a large amount of energy, increasing the time for the converter to respond to changes in the operating conditions. While some topologies, such as the “second harmonic Class E” [34] [42] [43] seen in Figure 1-6, reduce the size of the input inductor and the energy storage requirements, they do not reduce device voltage stress, which will be mentioned later on in this thesis.

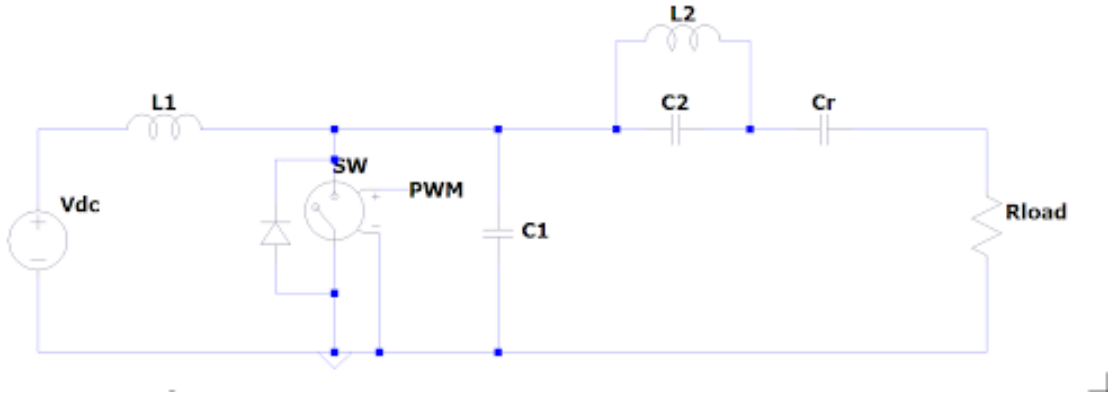


Figure 1-6: Second Harmonic Class E.

Further limitations of the Class E and the second harmonic Class E include the connection between the switch’s drain to source capacitance and the output power. For example, the power of the Class E and the second harmonic Class E inverter is shown in (1.35) and (1.36), respectively. Here, P_{out} is the output power of the inverter, V_{in} is the input voltage, F_s is the switching frequency, and C is the net capacitance parallel to the switch.

$$P_{out} = 2\pi^2 F_s V_{in}^2 C \quad (1.35)$$

$$P_{out} = \frac{1}{2}\pi^2 F_s V_{in}^2 C \quad (1.36)$$

These equations show that the minimum output power, and therefore, the efficiency, of these topologies is bound to the capacitance of the switches. This minimum output power may be higher than the desired output power, which reduces efficiency

considerably.

In addition, the Class E inverter's switch has a high voltage stress; the peak switch voltage in an ideal Class E is about 3.6 times the input voltage [13], [15] assuming ideal components and 50% duty cycle. In addition, the capacitance parallel to the switch of the Class E is usually made up of only the device's drain-to-source capacitance. Since capacitance varies under voltage, the device capacitance with drain voltage can increase the semiconductor's voltage stress up to almost 4.4 times the input voltage [44]. These high voltages can lead to power loss and over-spec'ing switches, which leads to more expensive, larger components.

To reduce the peak voltage on the switch, some RF power amplifiers under class F use resonant harmonic peaking of the input and output network [36], [45], [46], [47], [48], [49], [50], [51]. This leads to overlap of device voltage and current; as a result, the inverter is no longer in switched mode and the efficiency drops to unacceptable levels.

The Phi converter, a switched mode version of the Class F inverter, can become highly efficient [37], [52], [53], by adding a transmission line network or a lumped simulating network at the input. This shapes the waveform, reduces peak voltage stress, and removes the need for a large choke inductor. By operating entirely in switched mode at duty cycles below 50%, the inverter reaches high efficiency with low device stress and energy storage requirements. The Phi inverter, however, is limited by its large amount of energy storage elements and its complexity.

To summarize, the necessity of a large input inductor and the resulting large quantity and size of energy storage components which increase response time, the close tie between capacitance, output power, and efficiency, and the high voltage stress and peak voltage on the switch are important constraints of tuned switch mode inverters [31].

The Phi-2 was introduced because of these limitations. This improved topology allows for very high frequency (VHF) operation with low device voltage stress. Its reduced energy storage requirements leads to a small passive component count and therefore, a fast transient response. Based on a simplified version of the Class-Phi in-

verter, the Phi-2 creates symmetric drain to source waveforms by reducing the second harmonic voltage. It incorporates device capacitance into waveshaping, breaking the connection between capacitance and efficiency and allowing for flexible designs over a wider range of frequencies and power [31]. This Phi-2 inverter is shown in Figure 1-7.

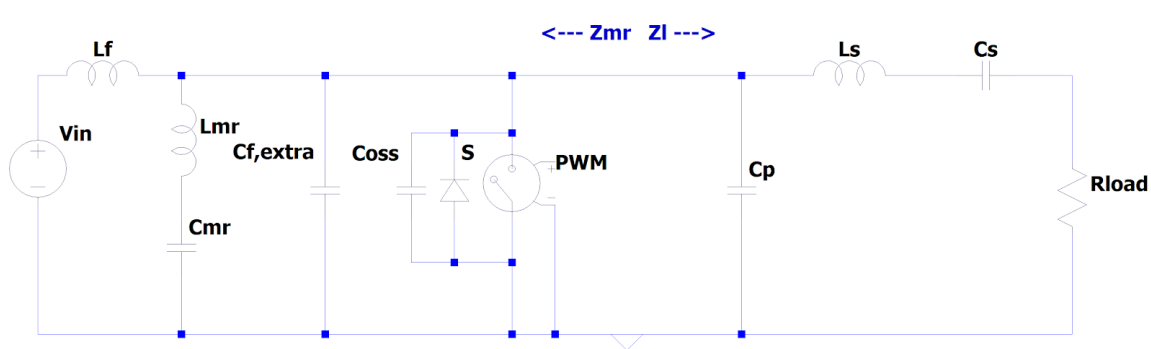


Figure 1-7: Topology of Phi-2 Inverter.

Theory of Phi-2

The Phi-2 is divided into two sections: a low-order lumped network and a load network. The Phi-2 inverter resembles the Class Phi inverter mentioned previously in [37], [53]. Instead of the high order transmission line at the input of the inverter, the Phi-2 has a low order resonant network, related to the Class E. This resonant network, shown in Figure 1-8, is connected to the DC input and is tuned to shape the switch's drain to source waveform by imposing half-wave voltage symmetry.

The network provides an output impedance of Z_{mr} when the switch is off. The inverter is tuned for switched-mode operation at a set frequency and duty cycle, low loss near ZVS, and zero dv/dt at turn on. Tuning is referred to choosing the impedances of components seen by the switch at the fundamental switching frequency and at the next few harmonics. In this network, C_f is the sum of the output capacitance of the switch, C_{oss} , and an additional capacitance component, $C_{f,extra}$, that may be added to improve wave shaping properties. The result is a semi-trapezoidal drain to source waveform with a lower peak amplitude in the middle of the waveform relative to the edges [31]. This waveform is shown in Figure 1-9.

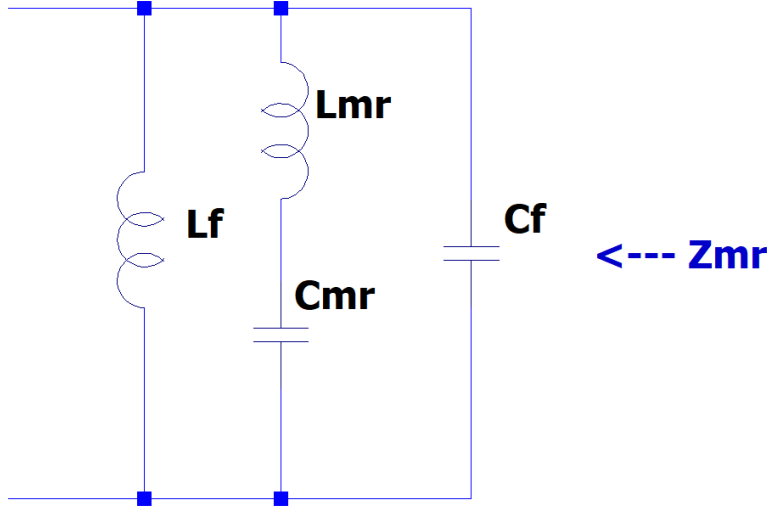


Figure 1-8: Low order lumped network.

The second half of the Phi-2 inverter is a load network made up of the load network, R_{load} , a shunt capacitance, C_p , and a reactive interconnect, X_s , made up of a capacitor C_s and an inductor L_s in series. This half of the inverter is shown in Figure 1-10.

L_s and C_s connect the drain of the switch to the load resistor. X_s blocks DC from the load and controls output AC power. This part of the inverter contributes an impedance of Z_L . The total impedance looking into the drain to source port of the switching device is Z_{ds} , the parallel combination of Z_L and Z_{mr} when the switch is off. It's important to note that the only physical capacitance requirement is that the actual switch capacitance plus any intrinsic parasitic capacitance must be less than or equal to the sum of all the capacitances parallel to the drain to source port of the switch, which is mathematically represented by $C_{oss} + C_{f,extra} + C_p$. The separation detailed here is only to simplify analysis and design of the inverter [31].

The Phi-2 inverter can be analyzed by splitting its operation into two states. In the first stage, the switch is on. The DC input provides energy that is stored in the input inductor, L_f . In addition, energy circulates in the resonant loop composed of L_{mr} and C_{mr} . In the second stage, the switch is off. The drain to source voltage in Figure 1-9 is the semi-trapezoidal waveform determined by the impedance of the

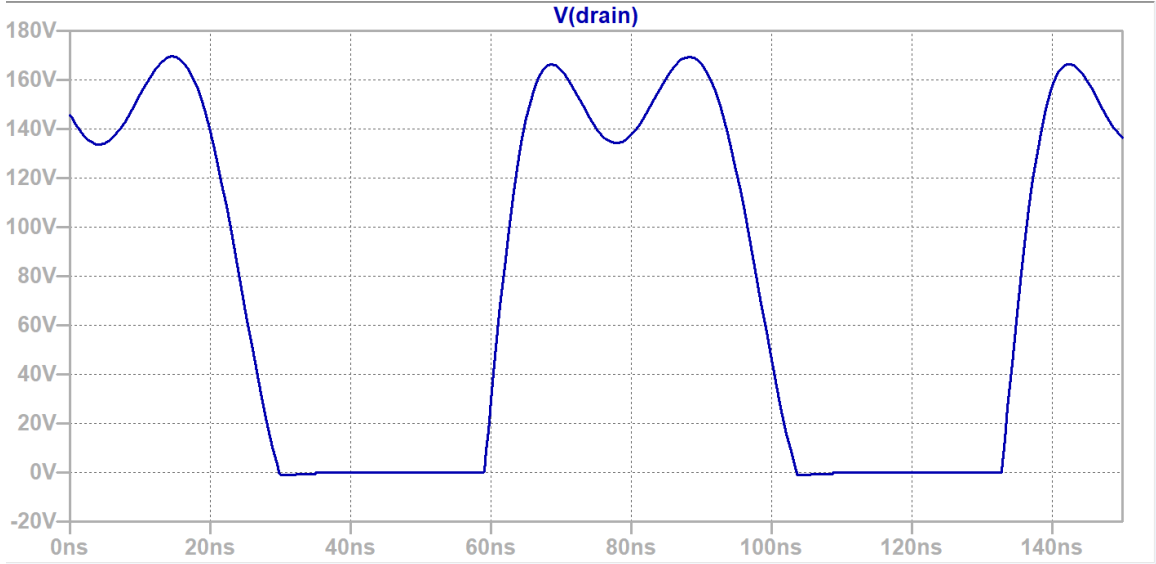


Figure 1-9: Semi-trapezoidal drain-to-source waveform

circuit.

The Phi-2 inverter implemented for this thesis was designed following the steps below in [31]. These steps allow for increased design flexibility not available in other inverters, such as the Class E inverter. This allows the Phi-2 inverter to be run at much higher frequencies than the Class E inverter. In addition, no bulk RF choke is required, allowing for rapid dynamic response. Also, the Phi-2 inverter has lower device stresses than traditional inverters. When designing this inverter, it is critical to remember that the component impedances at the switch drain to source port will change the waveform shape.

1. Select L_s and C_s of the output tank X_s and R_{load} to achieve the desired power transfer.
 - (a) V_{ds} , the drain to source voltage of the switch, is a semi-trapezoidal waveform. For simplicity, assume V_{ds} is a square wave with a 50% duty cycle and an average voltage equal to V_{in} with swings between 0 and $2V_{\text{in}}$.
 - (b) Assume that the AC power that is received by the load is at the fundamental of the switching frequency. This allows us to represent the reactive interconnect with the circuit shown in Figure 1-10. $V_{ds,1}$ is the fundamental

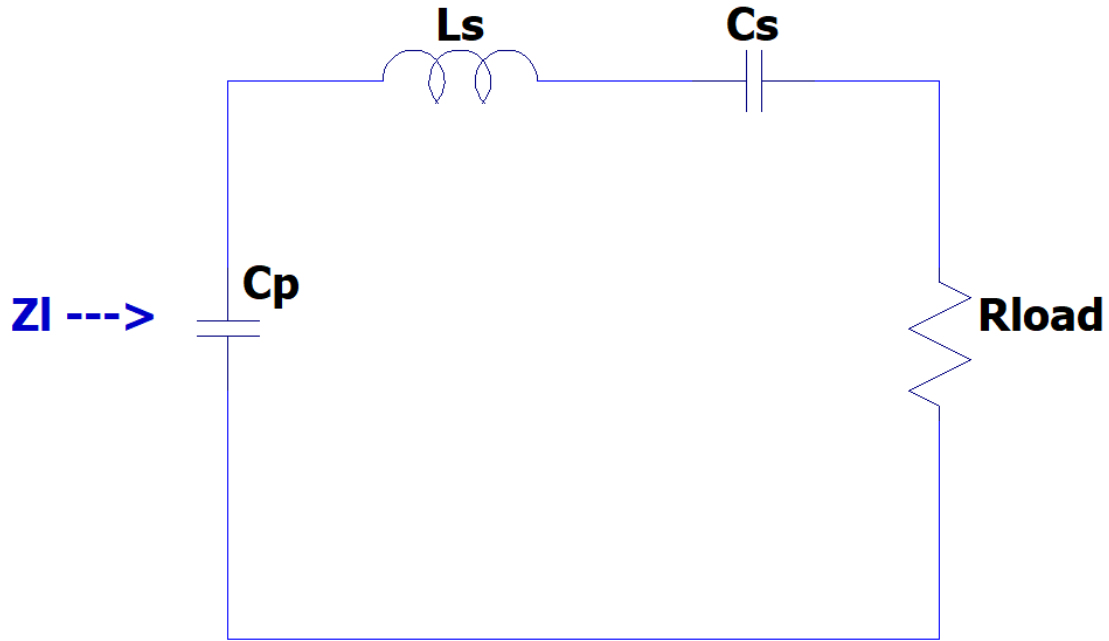


Figure 1-10: Load network.

of V_{ds} .

$$V_{ds,1} = \frac{4}{\pi} V_{in} X_s \quad (1.37)$$

- (c) The desired reactance X_s can be determined by finding the RMS voltage of the fundamental of the voltage across the the load at a given power (1.38) and the effective value of the fundamental component of the square wave approximation of V_{ds} (1.39).

$$V_{load,1,RMS} = \sqrt{P_{out} R_{load}} \quad (1.38)$$

$$V_{ds,1,RMS} = \frac{4}{\pi} \frac{V_{in}}{\sqrt{2}} \quad (1.39)$$

$$X_s = R_{load} \sqrt{\left(\frac{V_{ds,1,RMS}}{V_{load,1,RMS}} \right)^2 - 1} \quad (1.40)$$

- (d) Select L_s and C_s to arrive at the desired magnitude of X_s with either inductive or capacitive phase. Select C_s to have a low impedance compared

to the series combination of L_s and R_{load} and then solve for L_s . Too large of a value for C_s will increase transient response.

$$X_s = 2\pi F_s L_s \quad (1.41)$$

2. Size the elements of Z_{mr} . This includes L_f , L_{mr} , C_{mr} , and C_f .
 - (a) These elements make up the low order lumped network of Figure 1-8 and are critical to the wave shaping process.
 - (b) Initially, ensure Z_{mr} will peak at the fundamental and the third harmonic of the switching frequency and will have a null impedance at the second harmonic. This can be done by selecting a fixed value for C_f and using the equations below. To arrive at the correct waveform, tune L_{mr} and C_{mr} to be series resonant near the second harmonic of the switching frequency, $2F_s$.
 - i. C_f is the sum of C_{oss} from the switch and $C_{f,\text{extra}}$, an external capacitance. The value of C_f used in the equations below is a design parameter that can be the switch capacitance or a smaller or greater value.

$$L_f = \frac{1}{9\pi^2 F_s^2 C_f} \quad (1.42)$$

$$L_{mr} = \frac{1}{15\pi^2 F_s^2 C_f} \quad (1.43)$$

$$C_{mr} = \frac{15C_f}{16} \quad (1.44)$$

- (c) Model the impedance magnitude of Z_{mr} with respect to the frequency. An example can be seen in the next chapter.
 - i. Larger values of C_f will shift the magnitude of the impedance down, while smaller values of C_f will increase the impedance and reduce circulating currents. Too large or too small values of C_f will result in unreasonable values for the rest of the components.

3. Select the elements of Z_{ds}
 - (a) Final tuning of impedance characteristics to reach the following three goals. This is important to establish half-wave symmetry at the switch node.
 - (b) Z_{ds} at the third harmonic should be capacitive in phase with its magnitude between 4-8 decibels below the impedance magnitude at the fundamental.
 - i. The relative magnitude (ratio) between these impedances has a direct impact on the maximum voltage across the switch.
 - ii. Select C_p , which includes any of the capacitance not used in the previous tuning. If X_s is positive, and as a result, inductive, C_p dominates the high frequency portion of Z_L ; therefore, Z_L is capacitive at lower frequencies, inductive near the fundamental, and capacitive between the fundamental and third harmonic. An increase in C_p will cause the impedance at the third harmonic to decrease.
 - (c) Z_{ds} at the fundamental of the switching frequency should be $30^\circ - 60^\circ$ inductive to result in ZVS.
 - i. The phase angle can be increased by reducing L_f , which will increase the frequency where Z_{mr} peaks, making Z_{ds} look more inductive, and reducing the transient response of the converter. Reducing L_f too much will increase circulating currents and lower efficiency.
 - ii. Tune L_f to change the shape of the switch's drain to source waveform. Aim for ZVS and zero dv/dt across the switch at turn on. L_f acts as a resonant inverter but has a very small value and low energy storage compared to the RF choke in the Class E inverter.
 - (d) Z_{ds} at the second harmonic should be small, tuned to be series resonant at the second harmonic of the switching frequency.
 - (e) It is critical to establish half-wave symmetry at the switch's drain-to-source node of the switch. As mentioned previously, in periodic steady state, the average drain voltage must be the same as the input voltage. During

part of the cycle, the drain voltage is shunted to zero. For the other part of the cycle, the switch voltage rises, resembling a trapezoid. Z_{ds} , the parallel of Z_L and Z_{mr} , controls the exact shape of the wave. Selecting the components of Z_{ds} to achieve ZVS results in high-frequency switched mode operation. The Phi-2 works most efficiently at a fixed frequency, load, and duty cycle because of this specific tuning.

1.2.3 Comparison

Both inverters operate by exciting resonant networks at very high frequencies and rely on device parasitics for their operation. The Class E is particularly useful for its load modulation features. In addition, it has a straightforward design, unlike the Phi-2, a very complex system. The duty cycle can range for the Class E and still maintain high efficiencies, while the Phi-2 is not versatile with changes. The Phi-2 is designed for a specific duty cycle, frequency, and load.

The Phi-2 inverter has certain advantages over the Class E Inverter and other existing designs. The Class E Inverter is limited by its large input inductor, which stores a large amount of energy, increasing the time for the converter to respond to changes in the operating conditions. The Phi-2, however, is known for its rapid turn on and turn off time, low switch voltage stress, and small energy storage requirements for its passive components. The Phi-2 also has a quick dynamic response and flexibility in its design. It can be run at much higher frequencies than the Class E. It achieves these characteristics using a tuned resonant network that achieves zero voltage switching. In addition, the Phi-2's small passives, ZVS, and low voltage stress are formidable benefits.

Chapter 2

Design For Simulation

The topologies studied for this thesis are the Phi-2 Inverter and the Class E Inverter. For these inverters, the input and output power specifications, the load, and the frequency were equal.

2.1 Phi-2

The first step in designing a Phi-2 inverter is to select the load, output power, input voltage, and switching frequency. The output power was assumed to be the same as the input power. Table (2.1) summarizes parameters chosen for this thesis and their definitions. The duty cycle was selected to be 0.3 based off of the original design shown in [31]. This section illustrates how the methodology of the previous section can be applied.

Table 2.1: Design Procedure Input Data.

Parameter	Value
Input Power, P_{in}	150 W
Output Power, P_{out}	150 W
R_{load}	50 Ω
Input Voltage, V_{in}	100 V
Switching Frequency, F_s	13.6 MHz
Duty Cycle	0.3

Using the steps outlined earlier, the fundamental drain to source voltage, the fundamental RMS voltage across the load, and the fundamental RMS drain to source voltage are calculated.

$$V_{\text{load},1,\text{RMS}} = \sqrt{P_{\text{out}} R_{\text{load}}} = 86.6 \text{ V} \quad (2.1)$$

$$V_{ds,1,\text{RMS}} = \frac{4}{\pi} \frac{V_{\text{in}}}{\sqrt{2}} = 90.0 \text{ V} \quad (2.2)$$

$$X_s = R_{\text{load}} \sqrt{\left(\frac{V_{ds,1,\text{RMS}}}{V_{\text{load},1,\text{RMS}}}\right)^2 - 1} = 14.2 \Omega \quad (2.3)$$

Using the reactance calculated above, we can select C_s and then use the following to find L_s . For this design, C_s was set to be 4 nF so that there exists DC blocking to the load and so that the capacitor poses a low impedance compared to the series combination of L_s and R_{load} .

$$C_s = 4 \text{ nF} \quad (2.4)$$

$$L_s = \frac{X_s}{2\pi F_s} = 0.167 \mu\text{H} \quad (2.5)$$

To size the elements of the Phi-2 inverter that form the impedance Z_{mr} , we first select a value C_f and used the selected value to find L_f , L_{mr} , and C_{mr} .

$$C_f = 45 \text{ pF} \quad (2.6)$$

$$L_f = \frac{1}{9\pi^2 F_s^2 C_f} = 1.36 \mu\text{H} \quad (2.7)$$

$$L_{mr} = \frac{1}{15\pi^2 F_s^2 C_f} = 0.816 \mu\text{H} \quad (2.8)$$

$$C_{mr} = \frac{15C_f}{16} = 42.2 \text{ pF} \quad (2.9)$$

These values are summarized in Table (2.2).

Using the values above, the impedance versus frequency graph of the Z_{mr} elements

Table 2.2: Summary of Initial Values for Phi-2 Inverter.

Parameter	Value
C_s	4 nF
L_s	0.167 μ H
C_f	45 pF
L_f	1.36 μ H
L_{mr}	0.816 μ H
C_{mr}	42.2 pF

is generated. These values ensure that Z_{mr} will peak at the fundamental and third harmonic of the switching frequency and will have a null impedance at the second harmonic. The frequencies are outlined in the table below.

Table 2.3: Important Frequencies in Phi-2 Inverter Driven by the Chosen Switching Frequency.

Parameter	Value
Switching Frequency (F_s)	13.56 MHz
Second Harmonic ($2F_s$)	27.12 MHz
Third Harmonic ($3F_s$)	40.68 MHz

This is a good starting point for tuning, but the three goals that should be met with the Z_{mr} impedance plot at the end of the design are as follows:

1. The impedance at the switching frequency must look inductive.
2. The impedance at the second harmonic must look like a short.
3. The impedance at the third harmonic must look capacitive.

As seen in Figure 2-1, the impedance peaks at the fundamental frequency and at the third harmonic. A null exists at the second harmonic.

At this point, the circuit must be tuned and any additional capacitance must be added. C_p is selected and the impedance versus frequency graph of Z_{ds} is plotted. The goal of C_p is to lower the impedance of Z_{ds} at the third harmonic so that it

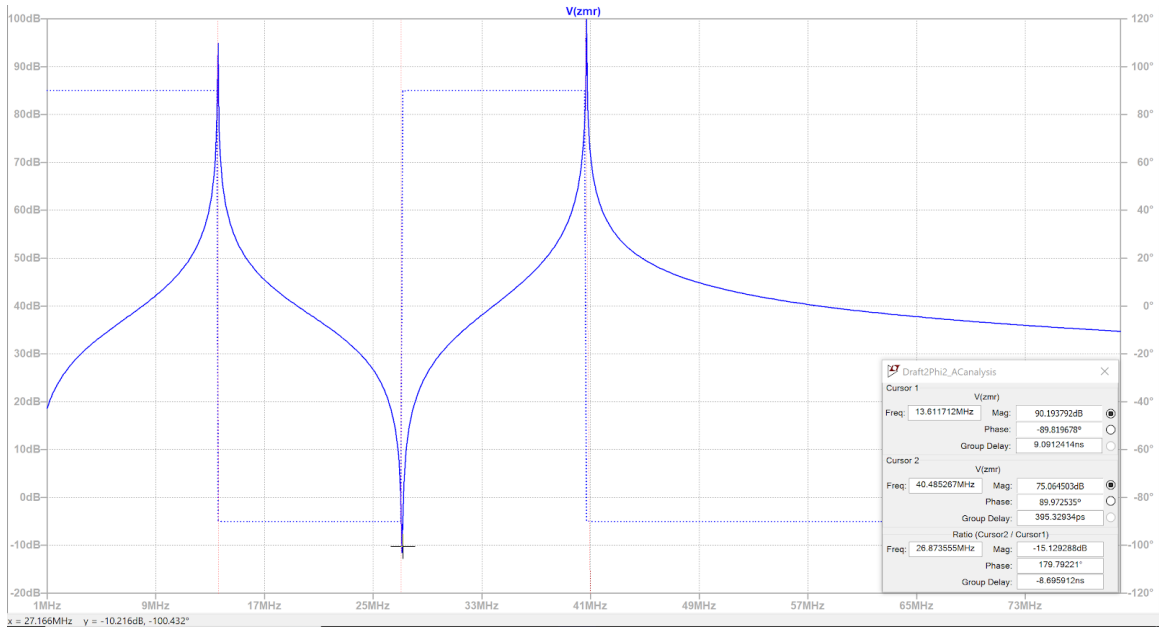


Figure 2-1: Plot of Z_{mr} versus Frequency. Note the bottom left of the screen, which displays the coordinates of the second harmonic. The chart on the right displays cursors at the fundamental frequency and the third harmonic. A red dashed line marks the fundamental frequency and the second and third harmonic.

remains capacitive in phase but is 4 – 8dB below the impedance magnitude at the fundamental.

Without C_p , Z_{ds} looks like Figure 2-2. Z_{ds} at the third harmonic does not look harmonic and the magnitude is not 4 – 8dB below the impedance magnitude at the fundamental. As a result, C_p is added.

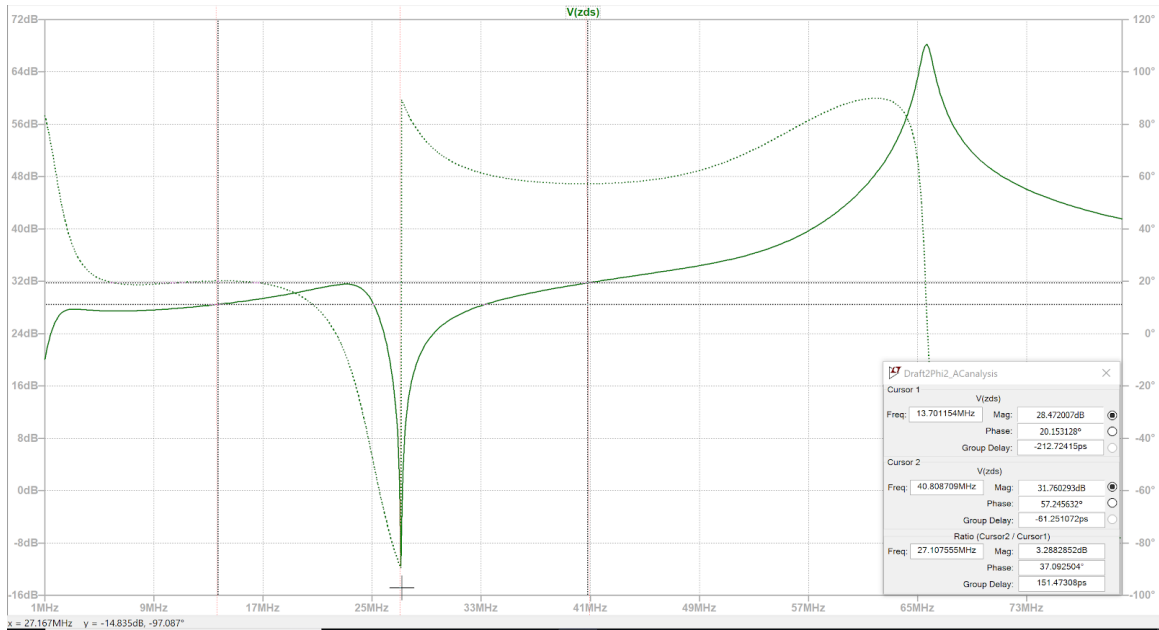


Figure 2-2: Plot of Z_{ds} vs Frequency Without C_p . The bottom left of the screen displays the second harmonic, while the box on the right displays the cursors at the fundamental and third harmonic. The magnitude here is not between 4 – 8dB and the phase of the fundamental is not between $30^\circ - 60^\circ$, so further tuning is required.

After adding C_p with a value of 40 pF, Z_{ds} looks like Figure 2-3. While Z_{ds} at the third harmonic still does not look capacitive, the magnitude between the fundamental and the third harmonic is between 4 – 8dB.

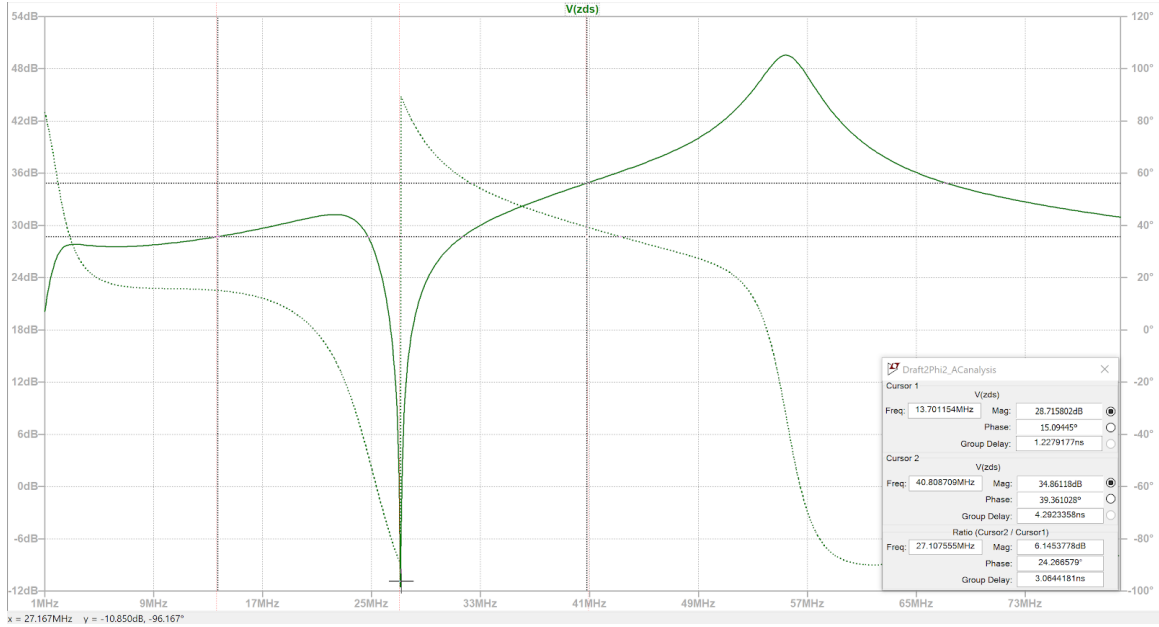


Figure 2-3: Plot of Z_{ds} versus Frequency with Addition of C_p .

The magnitude between the fundamental and third harmonic is 6.14 dB, as seen in the box on the right. The phase of the fundamental must be between $30^\circ - 60^\circ$.

Now, C_f is added to the Z_{mr} section of the inverter. A value of 100 pF was added in parallel to C_f , as seen in Figure 2-4 and Figure 2-5. One can see from the first plot that the magnitude between the fundamental and third harmonic decreases, but still in range. The phase drops substantially.

At this point, the requirements for Z_{ds} are somewhat met: the third harmonic is capacitive with its magnitude between 4 – 8dB below the impedance magnitude at the fundamental. However, the phase at the fundamental is not between $30^\circ - 60^\circ$. The requirements for Z_{mr} are somewhat met as well: the impedance at the second harmonic resembles a short and the impedance at the third harmonic is capacitive. However, the impedance at the switching frequency should look inductive, not capacitive. The drain to source waveform with the parameters above is shown in Figure 2-6. The drain to source voltage is asymmetrical. Further tuning is required.

The parameters used up to this point are listed in Table 2.4. Bolded values represent parameters added in the tuning process up to this point.

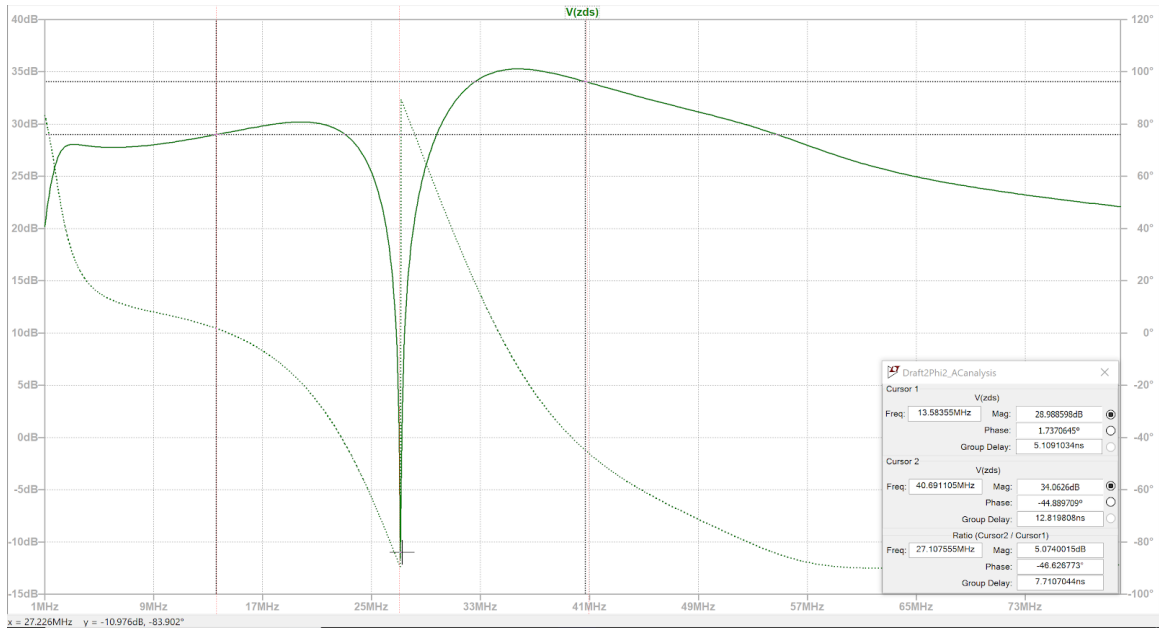


Figure 2-4: Plot of Z_{ds} versus Frequency with addition of $C_{f,extra}$ and C_p .

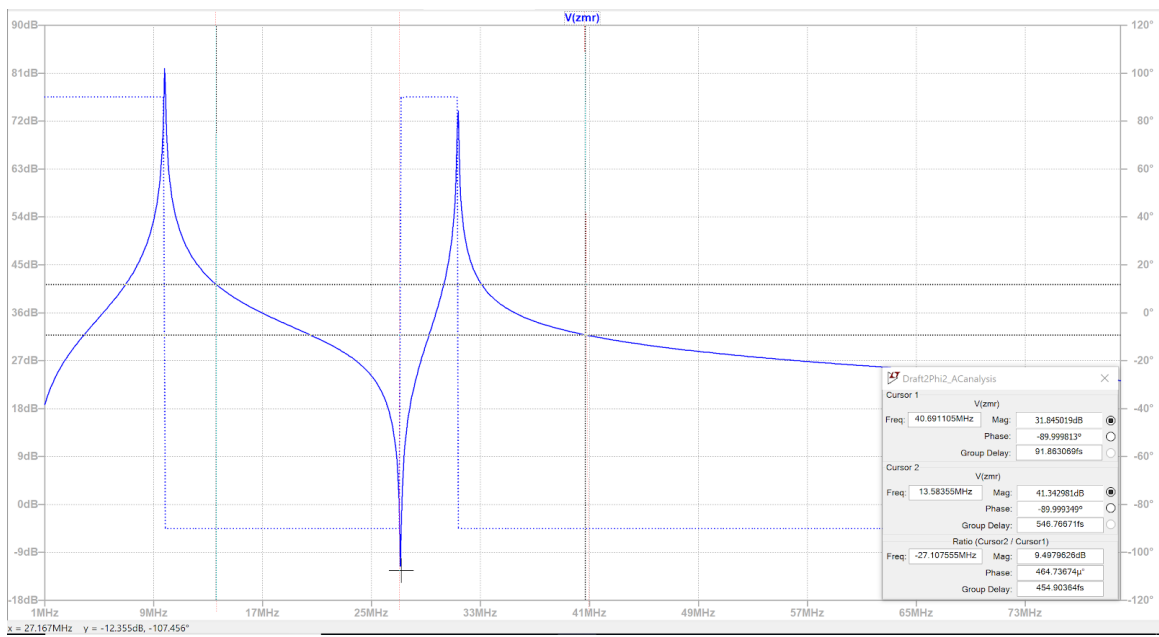


Figure 2-5: Plot of Z_{mr} versus Frequency with addition of $C_{f,extra}$ and C_p .

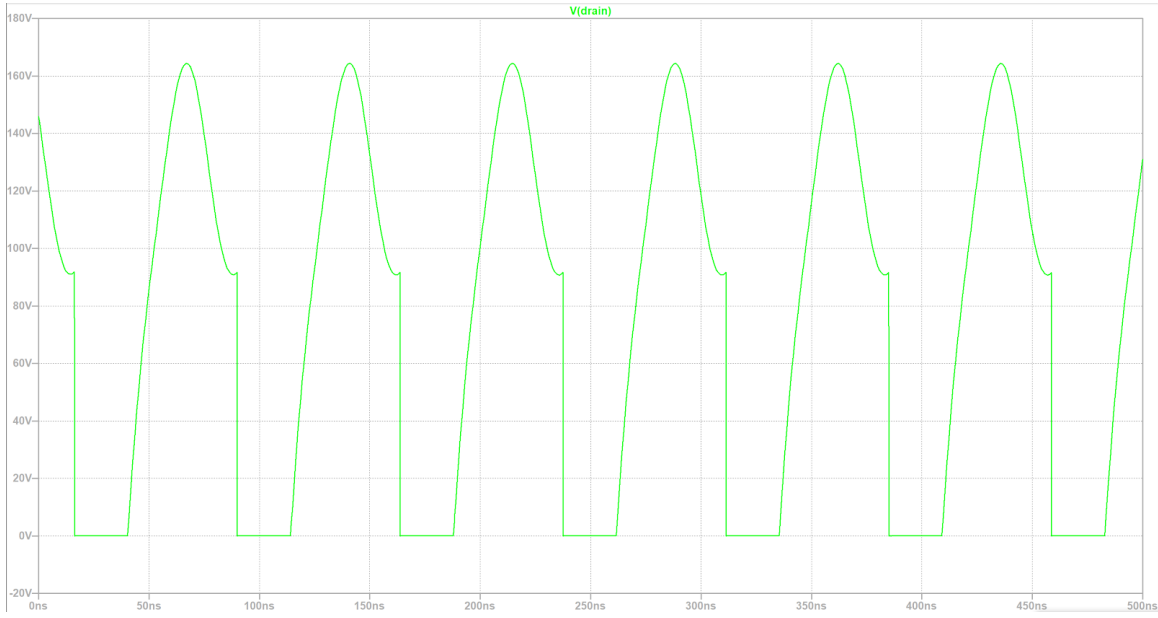


Figure 2-6: Asymmetrical Plot of Drain to Source Voltage versus Time with $L_f = 1.36 \mu\text{H}$.

Table 2.4: Summary of Values for Phi-2 Inverter After Some Tuning.

Parameter	Value
C_s	4 nF
L_s	0.167 μH
C_f	45 pF
L_f	1.36 μH
L_{mr}	0.816 μH
C_{mr}	42.2 pF
C_p	40 pF
$C_{f,\text{extra}}$	100 pF

Now, L_f is reduced from $1.36 \mu\text{H}$ to $0.5 \mu\text{H}$ in order to meet the remaining requirements for Z_{mr} and Z_{ds} and obtain a more symmetrical voltage.

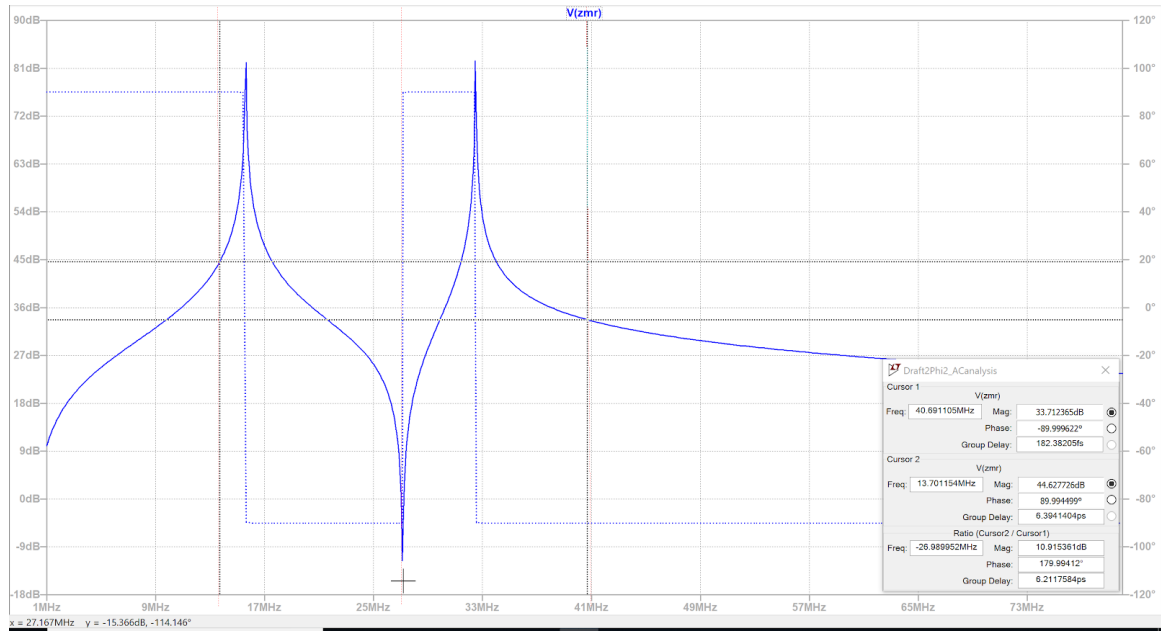


Figure 2-7: Plot of Z_{mr} versus Frequency with Reduction of L_f to $0.5 \mu\text{H}$.

Figure 2-7 meets more requirements than before. The requirements for Z_{mr} have been met: the impedance at the second harmonic resembles a short, the impedance at the third harmonic is capacitive, and the impedance at the switching frequency looks inductive.

Next we analyze the impedance graph of Z_{ds} with the reduction of L_f , shown in Figure 2-8. The requirements for Z_{ds} have been satisfied as well: the third harmonic is capacitive with its magnitude between $4 - 8\text{dB}$ below the impedance magnitude at the fundamental and the phase at fundamental is between $30^\circ - 60^\circ$.

The AC analysis requirements have been satisfied. Switching to the time domain, the drain to source waveform with $L_f = 0.5 \mu\text{H}$ is plotted in Figure 2-9:

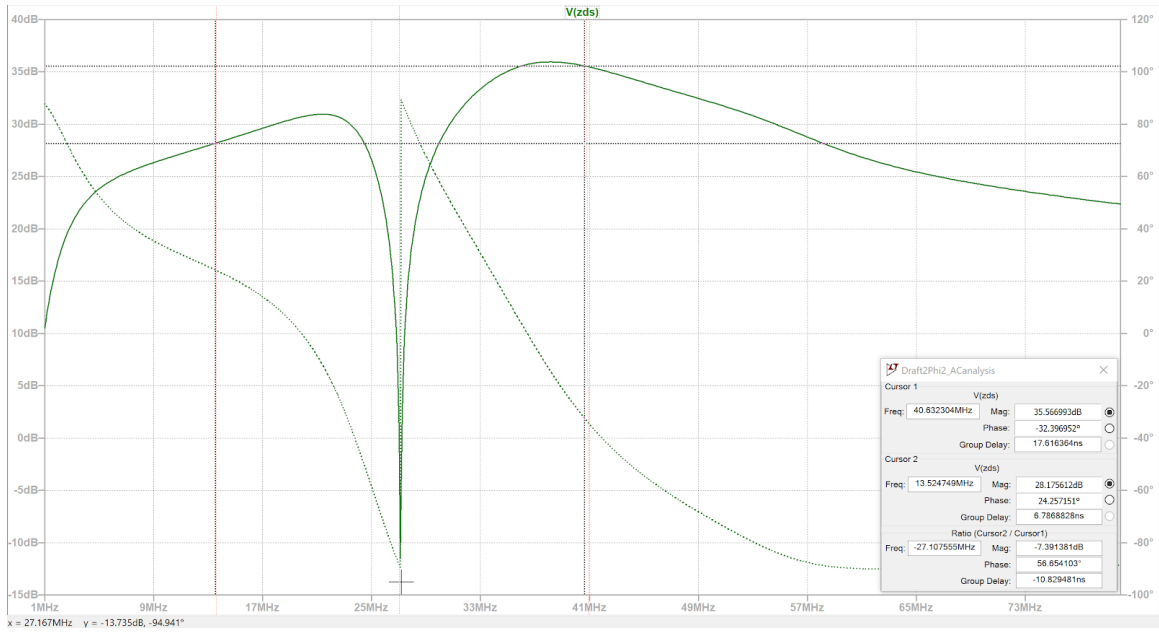


Figure 2-8: Plot of Z_{ds} versus Frequency with Reduction of L_f to $0.5 \mu\text{H}$.

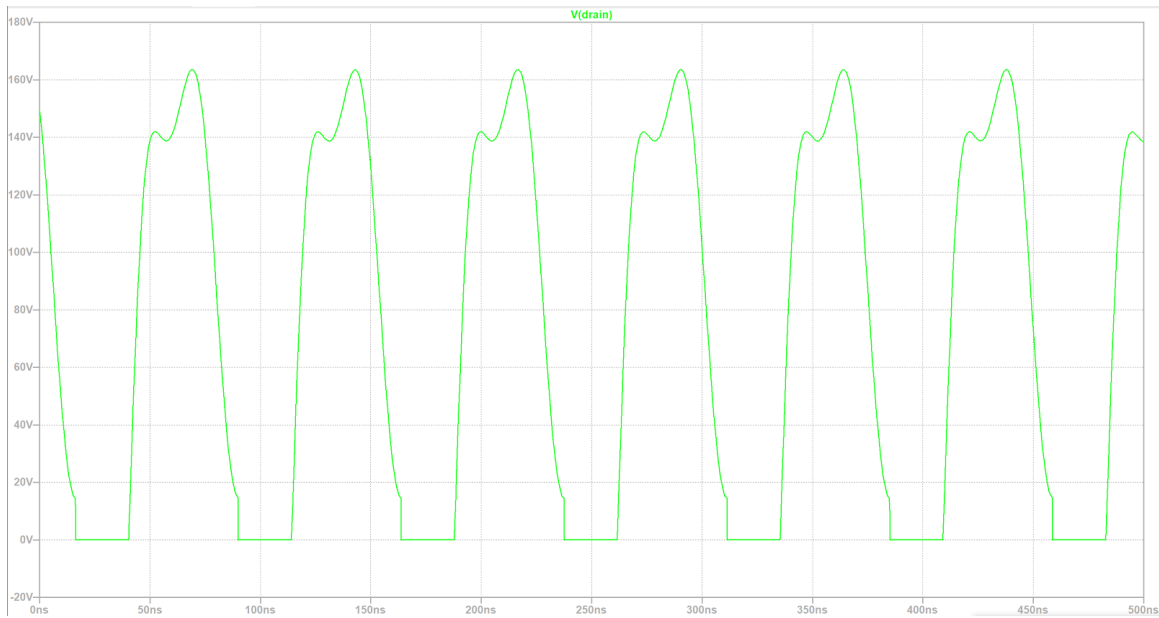


Figure 2-9: Plot of Drain to Source Voltage versus Time with $L_f = 0.5 \mu\text{H}$.

The waveform is not fully symmetrical, so L_f is further reduced to $0.44\mu\text{H}$. Figure 2-10 and Figure 2-11 show the inverter's impedance response with the reduction in L_f to $0.44\mu\text{H}$.

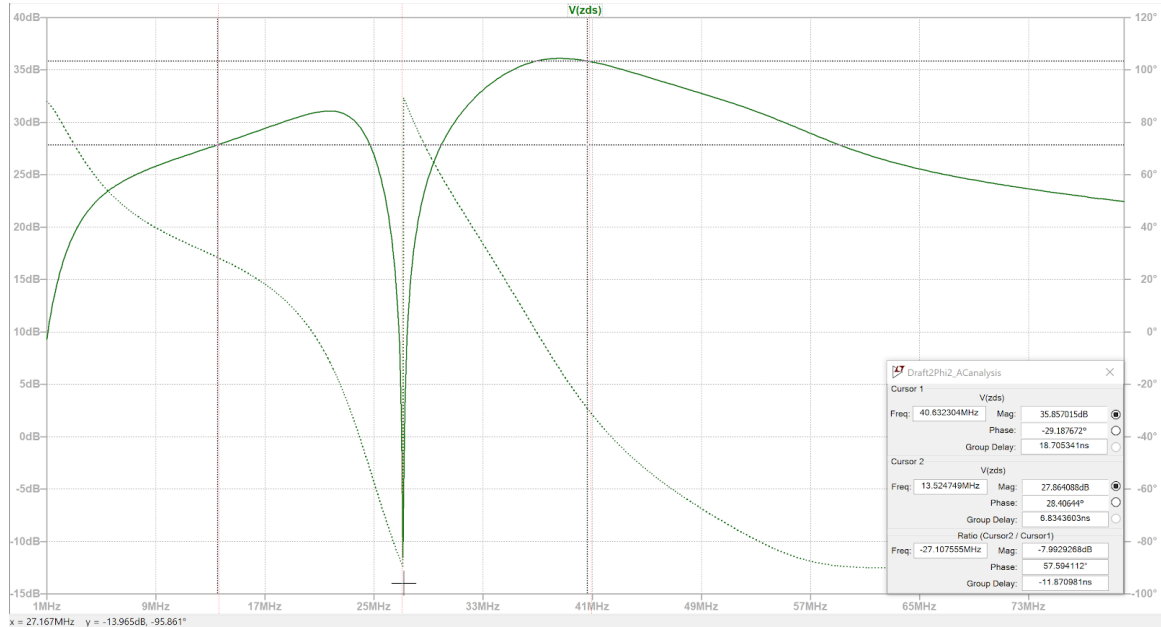


Figure 2-10: Plot of Z_{ds} versus Frequency with Reduction of L_f to $0.44\mu\text{H}$.

Note how close the magnitude of Z_{ds} and the phase are to their limits of 8 dB and 60° , respectively.

All three requirements for the Z_{mr} plot are still satisfied with the reduced value of L_f .

The AC analysis requirements have been met. Switching to the time domain, the drain to source waveform with $L_f = 0.44\mu\text{H}$ is plotted in Figure 2-12.

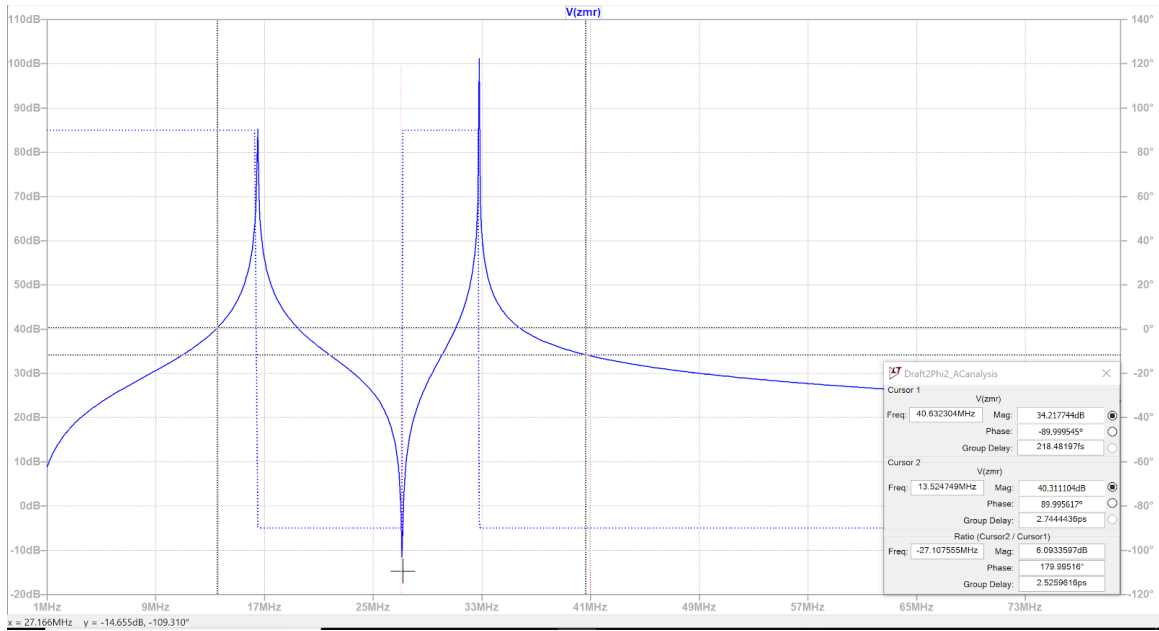


Figure 2-11: Plot of Z_{mr} versus Frequency with Reduction of L_f to $0.44 \mu\text{H}$.

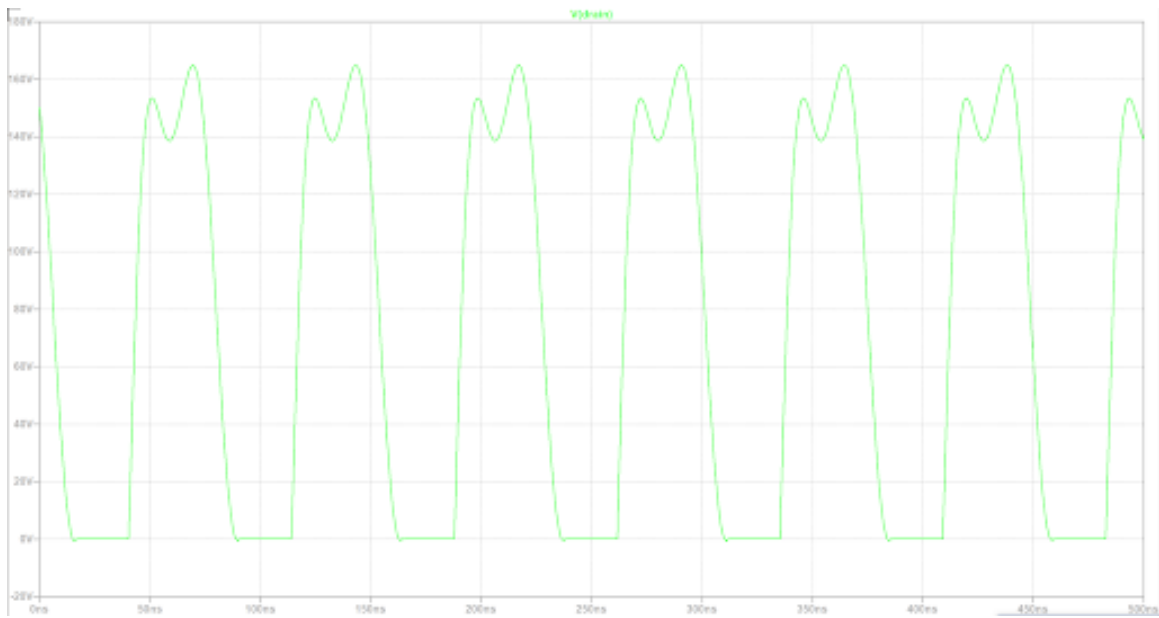


Figure 2-12: Plot of Drain to Source Voltage versus Time with $L_f = 0.44 \mu\text{H}$.

The waveform is still not symmetrical, so L_f is further reduced to a value of $0.38 \mu\text{H}$. We can see in the figure below that the drain to source voltage looks much more symmetrical. However, this comes at the cost of deviating from the requirements of Z_{ds} .

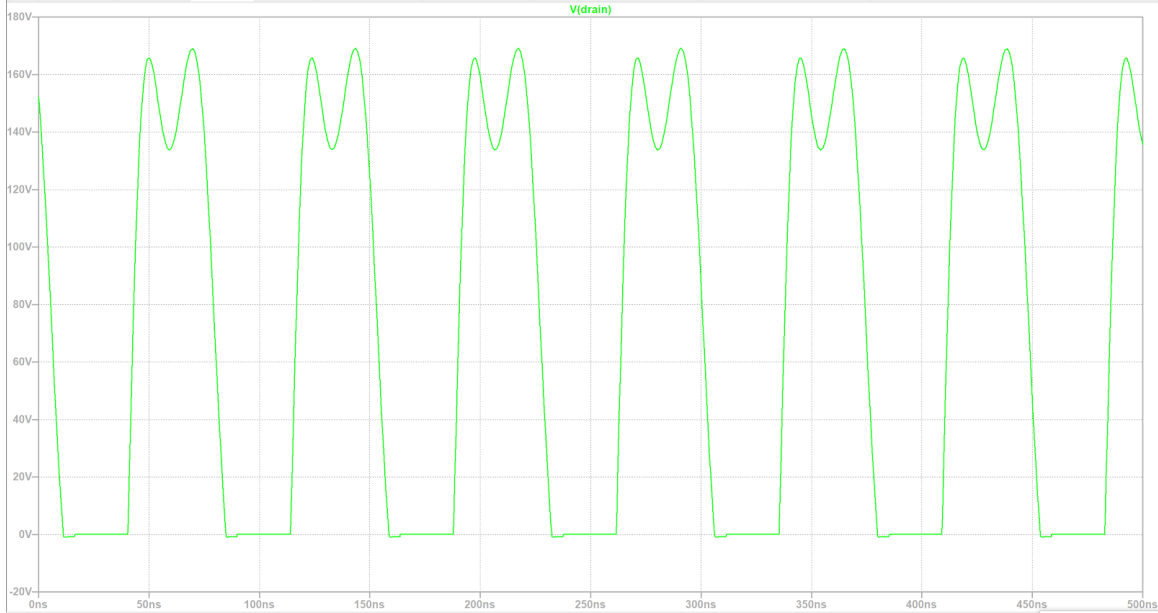


Figure 2-13: Plot of Drain to Source Voltage versus Time with $L_f = 0.38 \mu\text{H}$.

As shown in Figure 2-14, the Z_{mr} requirements are still met. The impedance at the fundamental looks inductive, the impedance at the second harmonic looks like a short, and the impedance at the third harmonic looks capacitive.

We can see in the bottom right of Figure 2-15 that the ratio between the impedance at the fundamental frequency and the impedance at the third harmonic is slightly above 8 dB.

Since the waveform looks symmetrical and the requirements stated above are to guide waveshaping, the final L_f value for the inverter is $0.38 \mu\text{H}$. Table 2.5 summarizes parameters chosen for this thesis and their definitions. Note that the only physical requirement is that the total capacitance selected for use at the drain to source node be greater than or equal to the actual switch capacitance plus any unavoidable parasitic capacitance. The total capacitance at the node is the sum of the output capacitance of the switch, C_{oss} , an optional additional capacitance, $C_{f,extra}$, and C_p [31].

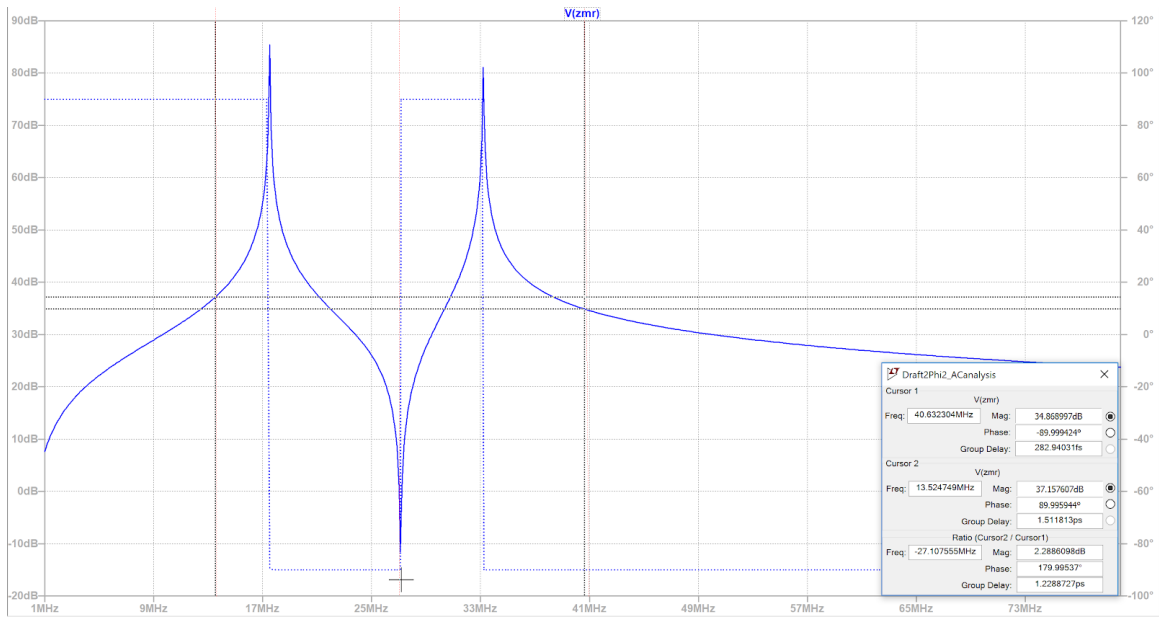


Figure 2-14: Plot of Z_{mr} versus Frequency with Reduction of L_f to $0.38 \mu\text{H}$.

Figure 2-16, Figure 2-17, and Figure 2-18 show the completed simulated inverter, the AC simulations, the drain to source voltage waveform, and the voltage waveform on the load. The AC Simulations were run with 1000 points with a starting frequency of 1Mhz and an ending frequency of 80Mhz.

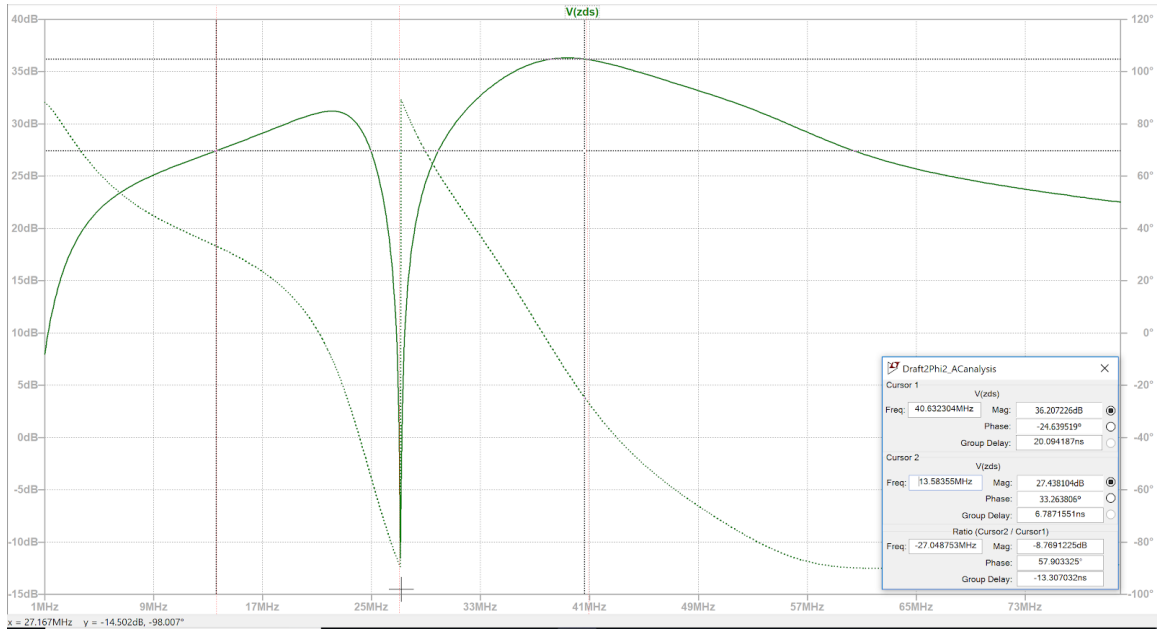


Figure 2-15: Plot of Z_{ds} versus Frequency with Reduction of L_f to $0.38 \mu\text{H}$.

Table 2.5: Summary of Final Values for Phi-2 Inverter.

Parameter	Definition	Value
C_s	Reactive interconnect capacitor	4 nF
L_s	Reactive interconnect inductor	0.167 μH
C_f	Output capacitance of switch plus additional capacitance of component	45 pF
L_f	Input inductor	0.38 μH
L_{mr}	Resonant inductor	0.816 μH
C_{mr}	Resonant capacitor	42.2 pF
C_p	Shunt capacitance	40 pF
$C_{f,extra}$	Additional capacitance component	100 pF
R_{load}	Resistive load	50 Ω

Phi-2 Inverter

Ensuring PowerIn = PowerOut

```
.meas PowerOut AVG I(Rload)*V(Output_Inv) FROM 80u TO 90u
.meas PowerIn AVG I(V2)*V(Vin) FROM 80u TO 90u
```

Creating Ideal Components and Running Simulation

```
.model Didl D(Ron=0.0001 Roff=100G Vfwd=0)
.model SW1 SW(Ron=1u Roff=10Meg Vt=.1)
.tran 0 100000ns 9000ns .74n
```

Setting Parameters

```
.param FREQ=13.56e6
.param PERIOD 1/{FREQ}
.param D=0.3
```

PWM Input

```
PULSE(0 5 0 1n 1n {D*PERIOD} {PERIOD})
```

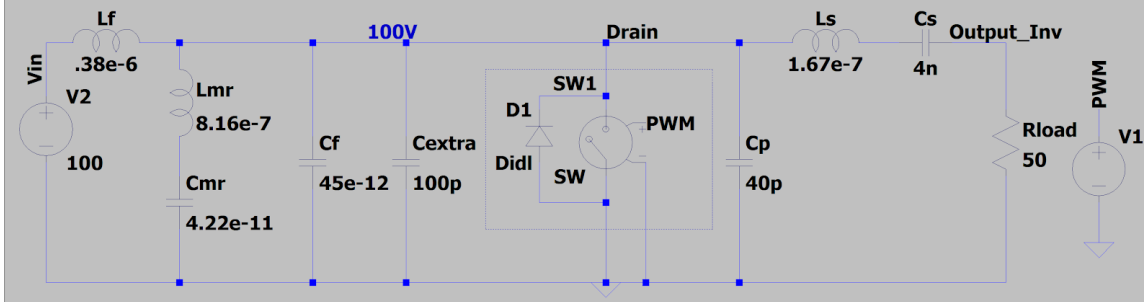
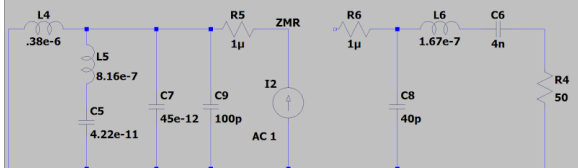


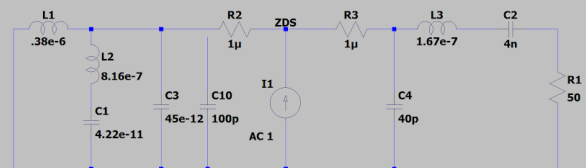
Figure 2-16: Phi-2 Simulation with a 50 Ω Load.

Phi-2 AC Simulations

Zmr Impedance Circuit



Zds Impedance Circuit



Lf,max = 1.36E-06

Fs = 13.56Mhz

2*Fs = 27.12Mhz

3*Fs = 40.68Mhz

Runs AC Sim

.ac lin 1000 1e6 80e6

For Zmr: Fundamental is inductive, 2nd harmonic is null, 3rd harmonic is capacitive

For Zds: Ratio btwn fund and 3rd harmonic of Zds is around 6dB, Phase angle of Zds at fundamental is 30 degrees

Figure 2-17: Phi-2 AC Simulations Used to find Impedance Response.

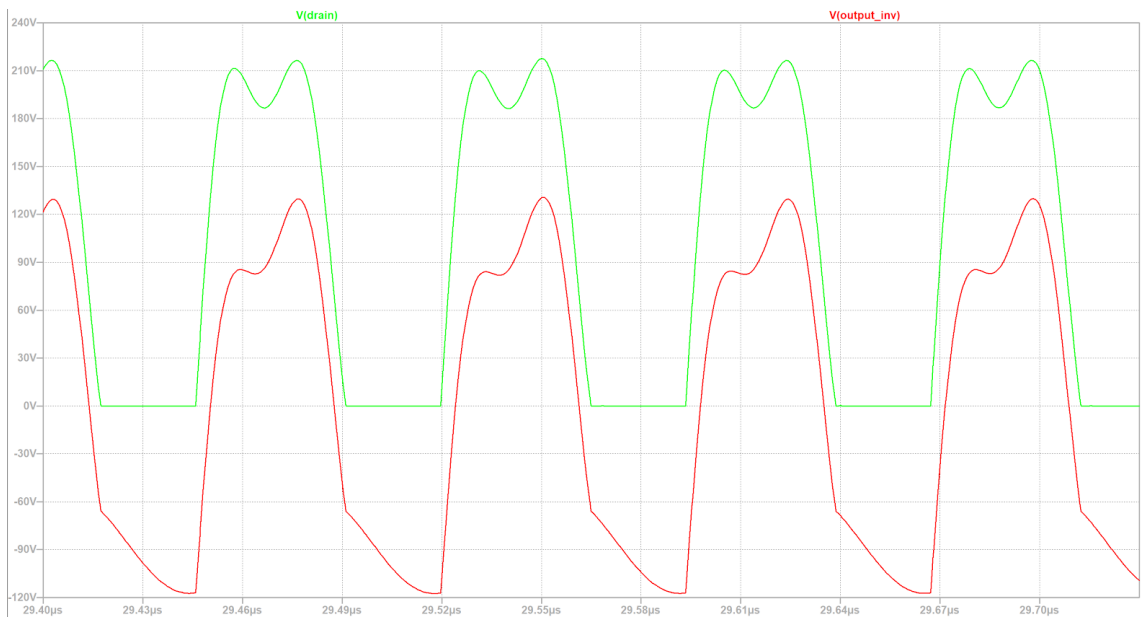


Figure 2-18: Drain to Source Voltage and Output Voltage of Phi-2 with 50 Ω Load.

2.2 Class E

Table 2.6 summarizes parameters chosen for this thesis and their definitions. This section illustrates how the methodology of the previous chapter was applied.

First, the rated load resistance, rated output power, and switching frequency were selected. For this thesis, both the maximum and minimum resistance were set at $50\ \Omega$ to better compare with the Phi-2, which does not have load modulation properties. We assumed the input power is equivalent to the output power.

Table 2.6: Design Procedure Input Data.

Parameter	Value
Input Power, P_{in}	150 W
Output Power, P_{or}	150 W
R_{load}, R_{or}	$50\ \Omega$
Output Voltage, V_{out}	86.6 V
Switching Frequency, F_s	13.6 MHz

Using the steps outlined earlier, the RMS value of the output voltage, the rated output RMS current, and the DC supply voltage were calculated. These values can be seen in Table 2.7

$$V_{or} = \sqrt{P_{or}R_{or}} = 86.6\ \text{V} \quad (2.10)$$

$$I_{or} = \frac{P_{or}}{R_{or}} = 3\ \text{A} \quad (2.11)$$

$$V_{dc} = \frac{V_{or}}{1.15} = 75.3\ \text{V} \quad (2.12)$$

Table 2.7: Design Procedure Initial Calculations.

Parameter	Value
RMS value of output voltage, V_{or}	86.6 V
Rated output RMS current, I_{or}	3 A
DC Supply voltage, V_{dc}	75.3 V

Then, set $Q_{\text{fil}} = Q_s = 5$ for sufficient filtering for both the parallel and series network. For the series network, we have:

$$\frac{\sqrt{L_s/C_s}}{R_{\text{or}}} = 5 \quad (2.13)$$

Solving this equation, we arrive at:

$$C_s = \frac{1}{2\pi F_s Q_s R_{\text{or}}} = 46.9 \text{ pF} \quad (2.14)$$

$$L_s = Q_s^2 R_{\text{or}}^2 C_s = 2.93 \text{ }\mu\text{H} \quad (2.15)$$

A similar approach is required for the parallel series:

$$\frac{R_{\text{or}}}{\sqrt{L_p/C_p}} = 5. \quad (2.16)$$

Leading to

$$L_p = \frac{R_{\text{or}}}{2\pi F_s Q_p} = 0.117 \text{ }\mu\text{H} \quad (2.17)$$

$$C_p = \frac{Q_p^2 L_p}{R_{\text{or}}^2} = 1.17 \text{ nF} \quad (2.18)$$

Now we must tune the input network, L_f and C_f , to slightly below $1.5\times$ the switching frequency to achieve optimal switching conditions. We can do this by finding the resonant frequency, F_f , as follows

$$F_f = 1.5F_s = 20.3 \text{ MHz}. \quad (2.19)$$

We then set k_f to 0.7 to find the characteristic impedance of the switching input network.

$$Z_{\text{char}} = k_f R_{\text{or}} = 35 \text{ }\Omega \quad (2.20)$$

Using Z_{char} , we find the L_f and C_f of the input network.

$$C_f = \frac{1}{2\pi F_f Z_{\text{char}}} = 0.225 \text{ nF} \quad (2.21)$$

$$L_f = C_f Z_{\text{char}}^2 = 0.274 \text{ }\mu\text{H} \quad (2.22)$$

Parameters used for the design of the Class E are included in the Tables below.

Table 2.8: Miscellaneous Parameters for Class E Inverter.

Parameter	Definition	Value
k_f	Tuning Coefficient	0.7
Z_{char}	Characteristic impedance	35Ω
$Q_{fil} = Q_s$	Q factor	5
Duty Cycle	Fraction of operation	0.5
F_f	Resonant frequency	20.3 MHz

Table 2.9: Component Values for Class E Inverter.

Parameter	Definition	Value
C_s	Tuned load network capacitor	46.9 pF
L_s	Tuned load network inductor	2.93 μH
C_f	Input capacitor including transistor output capacitance	0.224 nF
L_f	Input inductor	0.274 μH
L_p	Shunt output inductor	0.117 μH
C_p	Shunt output capacitor	1.17 nF

Below shows the completed simulated inverter, the drain to source voltage waveform, and the voltage waveform on the 50Ω load.

Class E Inverter

Ensuring PowerIn = PowerOut

```
.meas PowerOut AVG I(R4)*V(Output_Inv) FROM 80u TO 90u
.meas PowerIn AVG I(V4)*V(Vin) FROM 80u TO 90u
```

Creating Ideal Components and Running Simulation

```
.model Didl D(Ron=0.0001 Roff=100G Vfwd=0)
.model SW1 SW(Ron=1u Roff=10Meg Vt=.1)
.tran 0 100000ns 9000ns
```

Setting Parameters

```
.param FREQ=13.56e6
.param PERIOD 1/{FREQ}
.param Kf .7
.param Zcharf = {Kf*50}
.param Cf = {1/(2*3.14*(2.03E+07)*Zcharf)}
.param Lf = {Cf*Zcharf**2}
```

PWM Input

```
PULSE(0 5 0 0.5n 0.5n {0.5*PERIOD} {PERIOD})
```

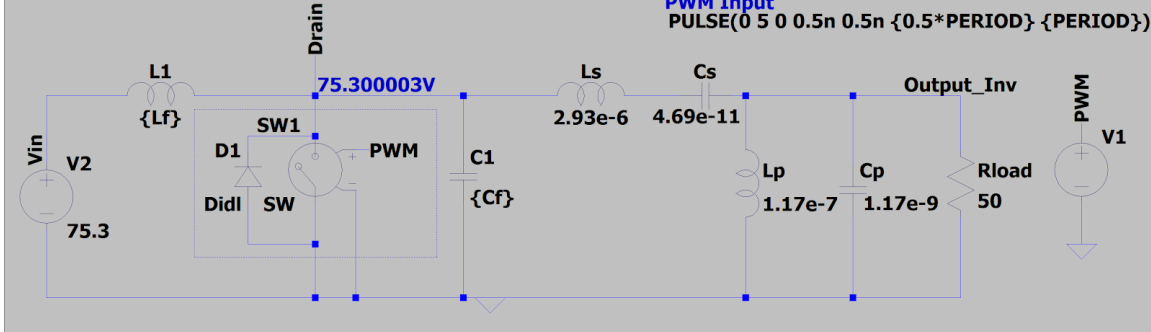


Figure 2-19: Simulated Class E Inverter.

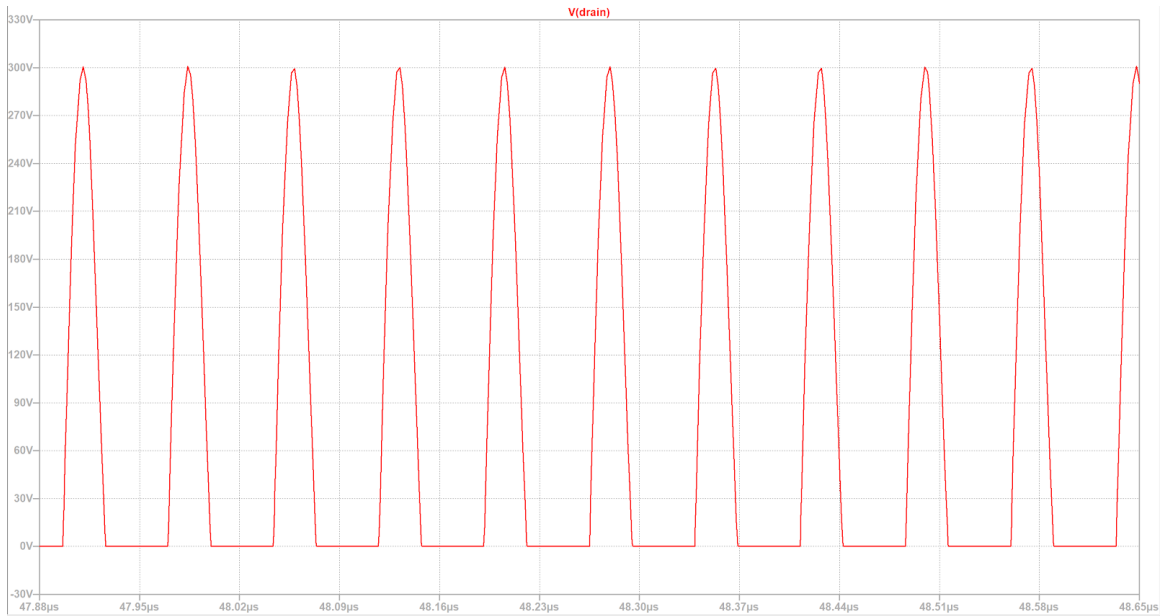


Figure 2-20: Drain to Source Voltage of Class E Inverter.

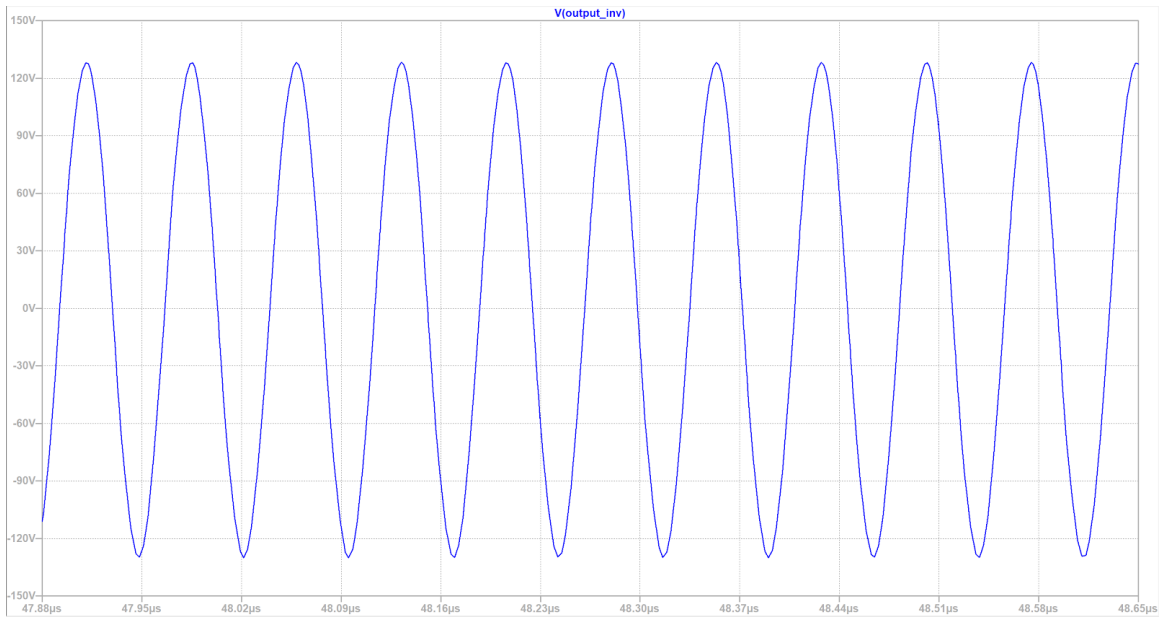


Figure 2-21: Output Voltage of Class E Inverter.

2.3 Rectifier

The inverters were designed for a 50Ω load. However, to explore the elimination of connectors in underwater systems, a WPT module and a rectifier were added and matched to look like the original 50Ω load. A rectifier is needed because AC current from the WPT module cannot charge a DC bus.

The wireless power transfer subsystem and the rectifier can cause the impedance seen at the output of the inverter to be different from the actual impedance of the load. This means that the WPT system and rectifier must be carefully considered to ensure that the load can be matched to 50Ω at the output of the inverter.

For this thesis, two different types of loads were considered.

2.3.1 Resistive Load

The output for this type of underwater system would ideally be a battery, but a resistive load would also be representative. For this design, two 12 V, 22 A Deep Cycle batteries were selected. The resistance that models the power draw of this load is:

$$P_{\text{out}} = 150 \text{ W} = \frac{24^2}{R} = \frac{V^2}{R}. \quad (2.23)$$

Yielding a resistance of $R = 3.84\Omega$. The full-wave rectifier topology selected is shown in Figure 2-22. The input is a sinusoidal voltage wave representing the voltage on the receiving coil of the WPT system.

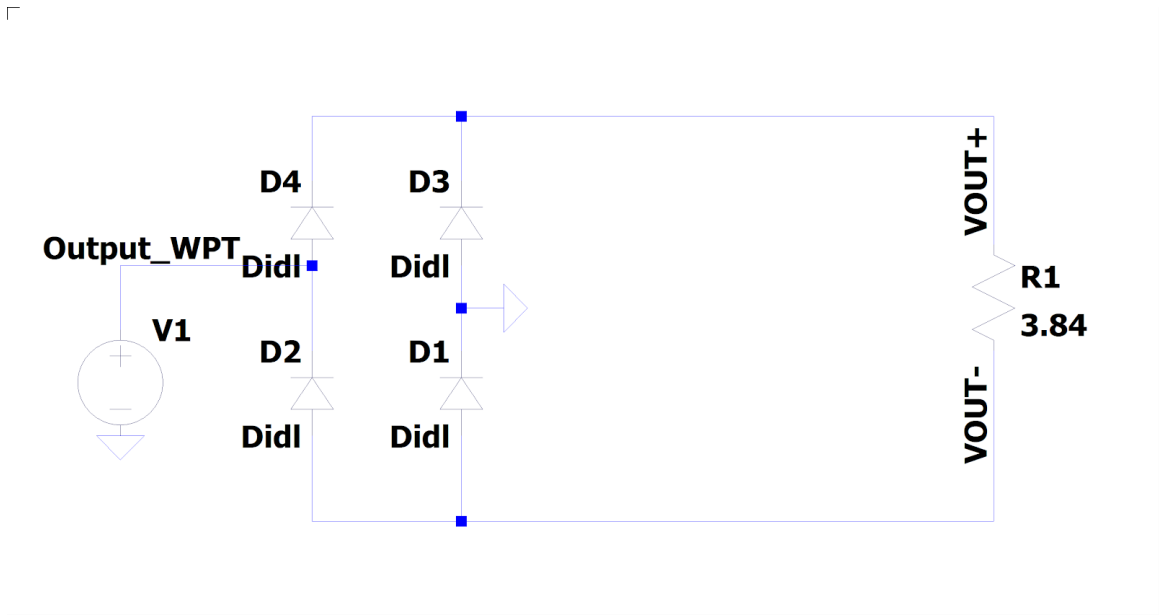


Figure 2-22: Model of Rectifier with Resistive Load.

These diodes are almost ideal, with an on-resistance of $0.1 \text{ m}\Omega$ and an off resistance of $10 \text{ G}\Omega$. There is no forward voltage drop. This topology takes a sinusoidal input, such as the blue signal below and rectifies the negative parts of the signal to obtain the red signal.

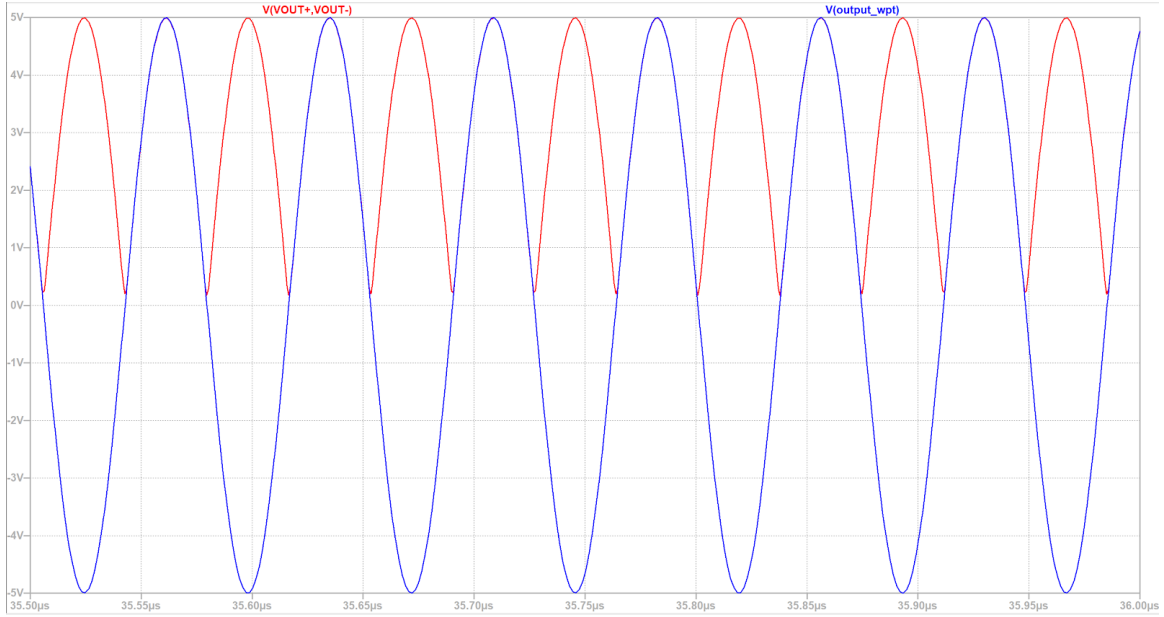


Figure 2-23: Input and Output of Rectifier with Resistive Load.

For the resistor model with a sinusoidal voltage input, we can use the theorem of power conservation to derive the equivalent resistance seen at the input of the inverter, $P_{\text{out}} = P_{\text{in}}$.

□

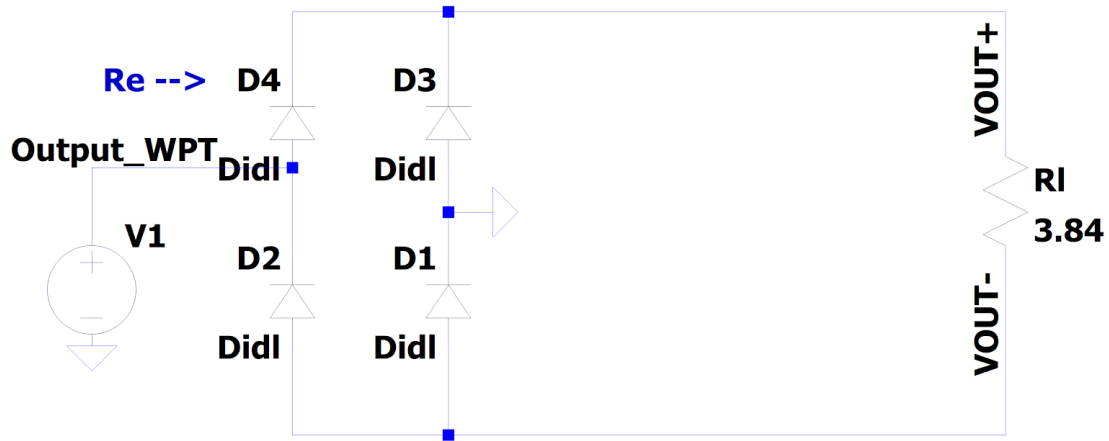


Figure 2-24: Model of Rectifier with Resistive Load, R_l , and Effective Resistance, R_e .

Taking the RMS value of the input and output voltages gives the following:

$$V_{in,RMS} = \frac{V_{pk}}{\sqrt{2}} \quad (2.24)$$

$$V_{out,RMS} = \frac{V_{pk}}{\sqrt{2}} \quad (2.25)$$

R_e is the effective resistance looking into the rectifier. R_{load} is R_l on the figure above. Using the power conservation equation above,

$$\frac{\left(\frac{V_{pk}}{\sqrt{2}}\right)^2}{R_e} = \frac{\left(\frac{V_{pk}}{\sqrt{2}}\right)^2}{R_{load}}. \quad (2.26)$$

Therefore, $R_e = R_{load}$.

2.3.2 Source Load

A battery can be modeled as a resistor and a capacitor in parallel, as shown in the figure below. R_2 in this figure models inherent resistive parasitics of the capacitor, C_1 . This is to model a high performance, meaning small ESR, low energy storage battery, suitable for underwater systems.

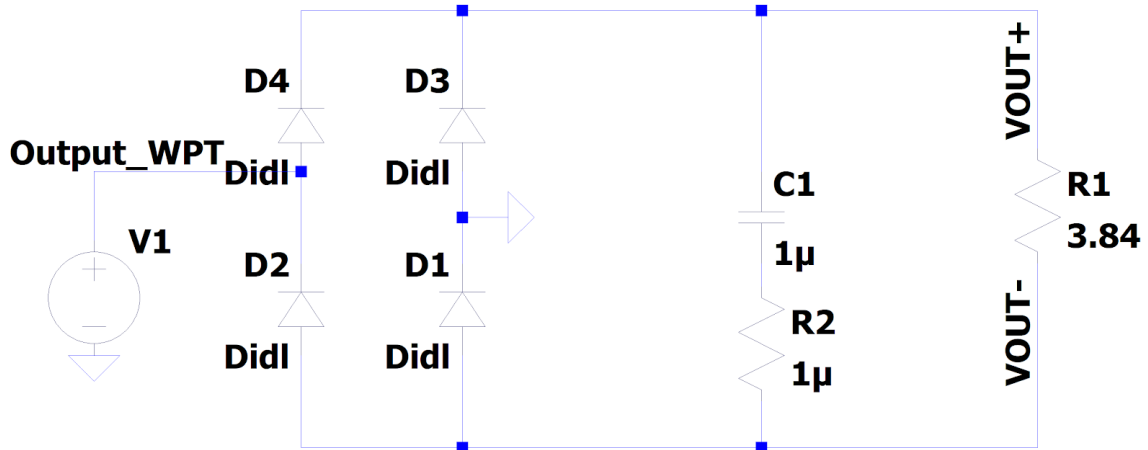


Figure 2-25: Model of Rectifier with Source as the Load.

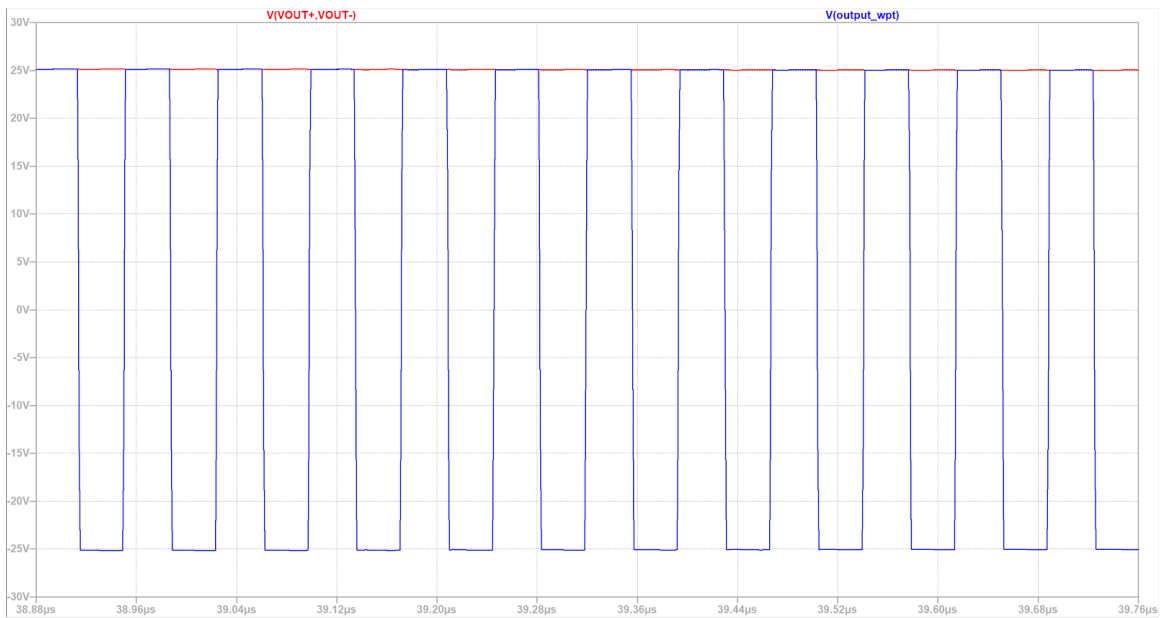


Figure 2-26: Input and Output of Rectifier with Source as Load.

The red voltage across the output resistor in Figure 2-26 resembles a DC voltage source because the capacitor filters out the AC current. The red waveform is the output voltage of the system, while the blue voltage is the input into the rectifier. This topology takes in a pulse input, such as the blue signal above. These diodes are almost ideal, with an on resistance of $0.1\text{ m}\Omega$ and an off resistance of $10\text{ G}\Omega$. There is no forward voltage drop.

□

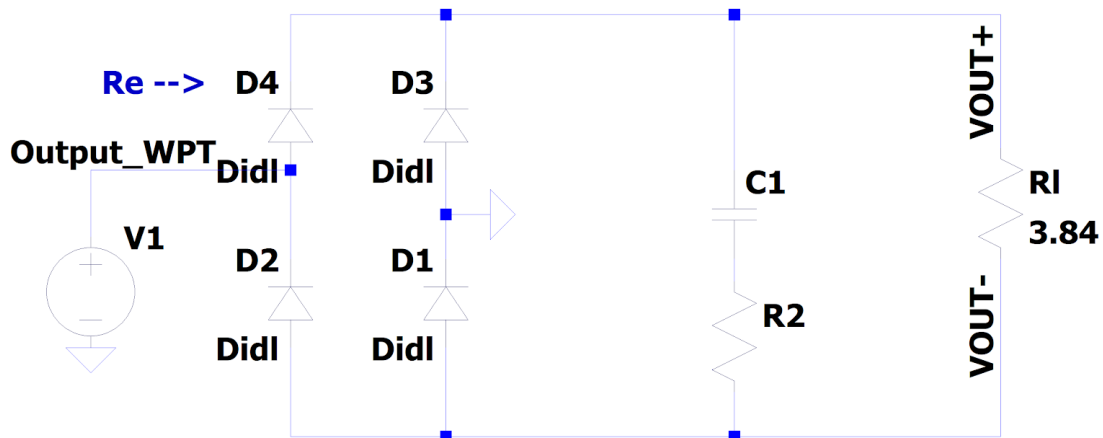


Figure 2-27: Equivalent Resistances with Source Model.

The theorem of power conservation, $P_{\text{in}} = P_{\text{out}}$, is used to derive the equivalent resistance seen at the input of the inverter. The voltage at the input of the rectifier is a square wave with a peak value, V_{pk} . The output is a DC voltage with value of V_{pk} . The RMS value of the input waveform is below:

$$V_{\text{in,RMS}} = \frac{4}{\pi} \frac{V_{pk}}{\sqrt{2}}. \quad (2.27)$$

Since power is conserved:

$$\frac{\left(\frac{4}{\pi} \frac{V_{pk}}{\sqrt{2}}\right)^2}{R_e} = \frac{V_{pk}^2}{R_l}. \quad (2.28)$$

Solving for R_e , we arrive at

$$R_e = \frac{8R_l}{\pi^2}. \quad (2.29)$$

These relationships between the output of the rectifier and the load seen at the input of the rectifier are necessary in order to match the output of the inverter to $50\ \Omega$. With these equations, an output load can be selected and then the rectifier and wireless power transfer modules can be designed so that the output of the inverter sees $50\ \Omega$.

2.4 Wireless Power Transfer

The process for determining the parameters for wireless power transfer can be divided into three steps.

The first step is to determine the inductance of the solenoid. This can be done by following the steps outlined in [54].

2.4.1 Derivation of Coil Inductance

First, the mean radius of winding (a), diameter of the wire over insulation (D), total number of turns in the winding (N), and the frequency of alternating current in cycles per second is selected (f). The rest of the parameters can be determined from these initial selections. In the table below are the list of the parameters are their descriptions.

Table 2.10: Parameters needed to Derive Inductance of a Coil.

Parameter	Description
a	Mean radius of winding
b	Axial length of the coil
c	Thickness of the winding
r	Inner radius of the winding
R	Outer radius of the winding
D	Diameter of the wire over insulation
C_m	Length of the conductor (cm)
N	Total number of turns in the winding
f	Frequency of alternating current (Hz)

The skin depth of copper at 13.56 MHz is 17.76 μm . Researchers typically use copper tubes rather than wires for these type of high frequency coils. However, copper tubes at the thickness of the skin depth do not exist. The thinnest types of copper tubes available are known as Model M. A Model M copper tube with a 1.5875 cm outside diameter (D), a 1.27 cm inside diameter, and a thickness of 0.071 12 cm was selected. Initially, the mean radius of the winding (a) was selected as 4 cm and the total number of turns in the winding was set at 5 (N).

The following equations were derived using Figure 2-28. This figure is similar to the coil design of [55].

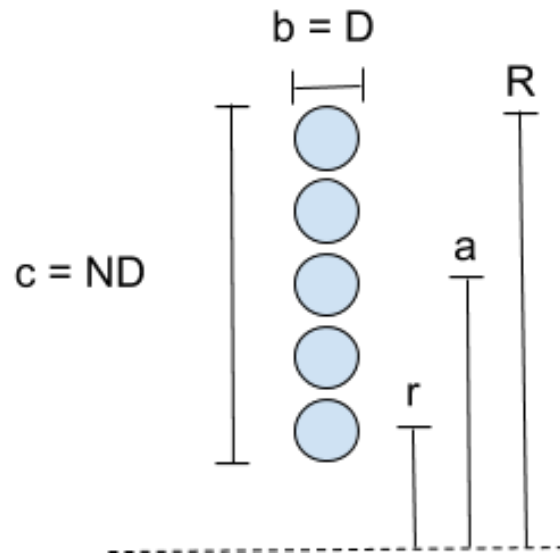


Figure 2-28: Cross sectional View of One Side of Winding .

The axial length of the coil, b , is equal to the diameter of the wire over insulation, D . The thickness of the winding, c , is equal to the product of the total number of turns in the winding, N , and the diameter of the wire over insulation: $c = ND$. The outer radius of the winding is equal to the following:

$$R = a + \frac{c}{2} \quad (2.30)$$

The inner radius of the winding, r , is the thickness of the winding, c , subtracted

from the outer radius of the winding, R .

$$r = R - c \quad (2.31)$$

The length of the conductor is the circumference multiplied by the total number of turns in the winding.

$$C_m = 2\pi aN \quad (2.32)$$

The table below shows the parameters derived using the equations above to calculate the inductance of the wireless power transfer coils.

Table 2.11: Parameters Used for Derivation of Coil Inductance.

Parameter	Value
a	4 cm
b	1.588 cm
c	7.938 cm
r	0.031 25 cm
R	7.969 cm
D	1.588 cm
C_m	125.7 cm
N	5
f	13.56 MHz

F' and F'' are empirical coil-shape factors depending on the dimensions of the windings, as seen in the equations below.

$$F' = \frac{10b + 12c + 2R}{10b + 10c + 1.4R} \quad (2.33)$$

$$F'' = 0.5 \log_{10} \left(100 + \frac{14R}{2b + 3c} \right) \quad (2.34)$$

The values are substituted in to arrive at the following:

$$F' = \frac{10b + 12c + 2R}{10b + 10c + 1.4R} = 1.194 \quad (2.35)$$

$$F'' = 0.5 \log_{10} \left(100 + \frac{14R}{2b + 3c} \right) = 1.01 \quad (2.36)$$

The inductance is calculated using these coil shape factors.

$$L = \frac{C_m^2}{b + c + R} \frac{F' F''}{10^9} = 1.09 \mu\text{H} \quad (2.37)$$

The system contains two identical coils with the same dimensions and therefore, the same inductance.

An external capacitor is added to the coils to allow resonance. The value of this capacitor, $C = 0.127 \text{ nF}$, can be calculated using the resonant formula:

$$f = \frac{1}{2\pi\sqrt{LC}}. \quad (2.38)$$

2.4.2 WPT Design

The next step after determining the inductance of the coils is to find the coupling coefficient, k , which is tied into the distance between the coils. The equation below can be manipulated to arrive at k . Here, L_1 and L_2 are the inductances of the coil, Z_{in} is the desired impedance, 50Ω , and R_l is the impedance at the output of the WPT module, which is equal to the impedance at the input of the rectifier. From the previous section, we know

$$L_1 L_2 = \frac{Z_{\text{in}} R_l}{(\omega k)^2}. \quad (2.39)$$

For the source model, R_l is 3.11Ω . For the resistor model, R_l is 3.84Ω . For the design in this thesis, $L_1 = L_2 = 1.09 \mu\text{H}$ and $\omega = 8.52 \cdot 10^7 \text{ rad s}^{-1}$. With these parameters, k is 0.135 for the source model and 0.150 for the resistor model.

Additionally, the relationship between k and the distance between the coils, d , is illustrated below

$$|k| = \frac{1}{\left(1 + \frac{2^{2/3} d^2}{a_1 a_2}\right)^{3/2}} \quad (2.40)$$

For the resistor model with a k of 0.150, d is approximately 5 cm. For the source model with a k of 0.135, d is approximately 5.3 cm.

From the previous chapter, R can be found with the following equation:

$$R = \frac{L\rho}{\pi D\delta}. \quad (2.41)$$

Where R is the resistance, L is the length of the wire, or C_m in the previous section, 1.257 m, ρ is the resistivity 1.72×10^{-8} , D is the diameter, 0.0159 m, and δ is the thickness of the skin effect, 17.7 μm . With these parameters, $R = 24.5 \text{ m}\Omega$.

Using the resistive model, with $R_l = 3.84 \Omega$, the Q-factor of the first coil can be found with the following equation, where L_1 is 1.09 μH , ω is 8.52×10^7 , R_1 is the resistance of the first coil, 24.5 $\text{m}\Omega$, and R_s is 0:

$$Q_1 = \frac{\omega L_1}{R_1 + R_s} = 3780 \quad (2.42)$$

Continuing with the resistive model, the Q-factor of the second coil can be found with the following equation, where L_2 is 1.09 μH , ω is 8.52×10^7 , R_2 is the resistance of the second coil, 24.5 $\text{m}\Omega$, and R_l is 3.84 Ω :

$$Q_2 = \frac{\omega L_2}{R_L + R_2} = 24 \quad (2.43)$$

In Figure 3-2, we can see the output voltage of the system across the resistive load, $V(V_{out+} - V_{out-})$, and the voltage at the output of the WPT module that is inputted into the input of the rectifier.



Figure 3-2: Output Voltage of System and Output Voltage of WPT of Phi-2 With Resistive Model as Load.

In the figure below, we see that the drain to source voltage of the Phi-2 with the WPT and rectifier modules and the resistive load is very similar to the drain to source voltage of the Phi-2 with just the $50\ \Omega$ load.



Figure 3-3: Drain to Source Voltage of Phi-2 With Resistive Model as Load.

Source Model

In the figure below is the completed simulation of the Phi-2 with the WPT and rectifier modules. The source model at the very end of the system results in a k of 0.135, a change of 0.015 from the resistive model .

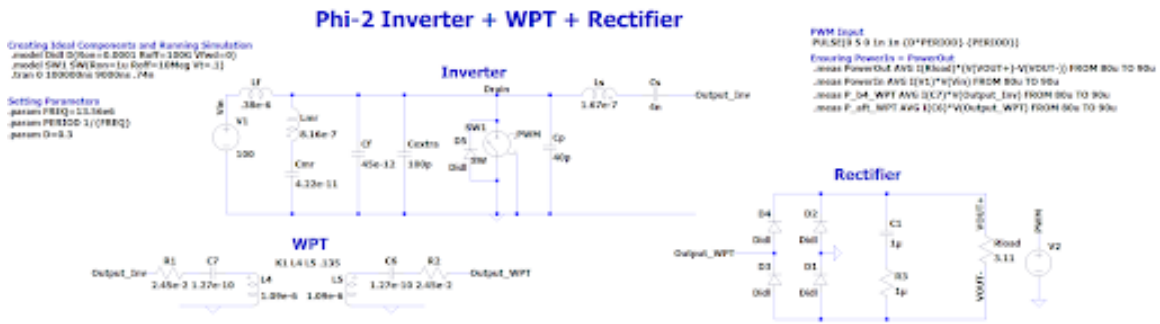


Figure 3-4: Phi-2 With WPT and Rectifier With Source Model as Load .

Figure 3-5 shows the output voltage of the system across the source load, $V(V_{out+} - V_{out-})$, and the voltage at the output of the WPT module that is inputted into the input of the rectifier.



Figure 3-5: Output Voltage of System and Output Voltage of WPT of Phi-2 With Source Model as Load.

In the figure below, we see that the drain to source voltage of the Phi-2 with the WPT and rectifier modules and the source load is very similar to the drain to source voltage of the Phi-2 with just the $50\ \Omega$ load.



Figure 3-6: Drain to Source Voltage of Phi-2 With Source Model as Load .

3.1.2 Class E

Resistive Model

Moving on to the Class E, below is the completed simulation of the Class E with the WPT and rectifier modules. The resistive model at the very end of the system results in a k of 0.150.

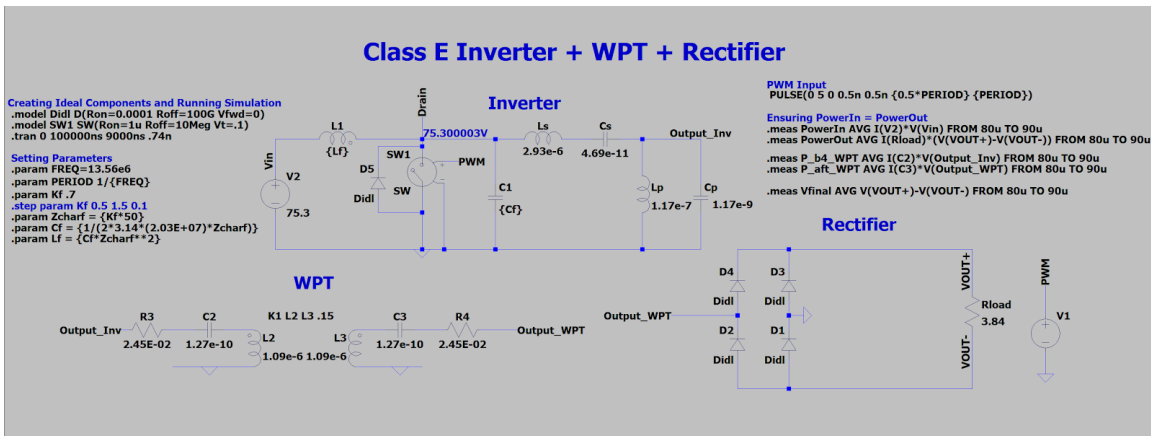


Figure 3-7: Class E With WPT and Rectifier With Resistive Model as Load.

In Figure 3-8, we can see the output voltage of the system across the resistive load, $V(Vout+ - Vout-)$, and the voltage at the output of the WPT module that is

inputted into the input of the rectifier.

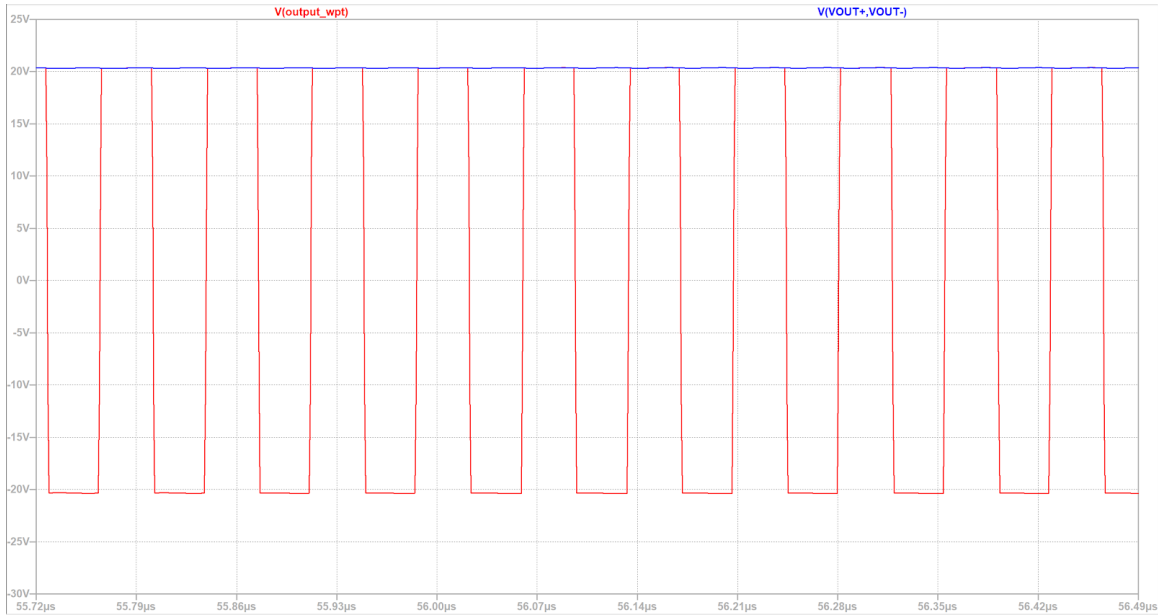


Figure 3-8: Output Voltage of System and Output Voltage of WPT of Class E With Resistive Model as Load .

In the figure below, we see that the drain to source voltage of the Class E with the WPT and rectifier modules and the resistive load is very similar to the drain to source voltage of the Class E with just the $50\ \Omega$ load.

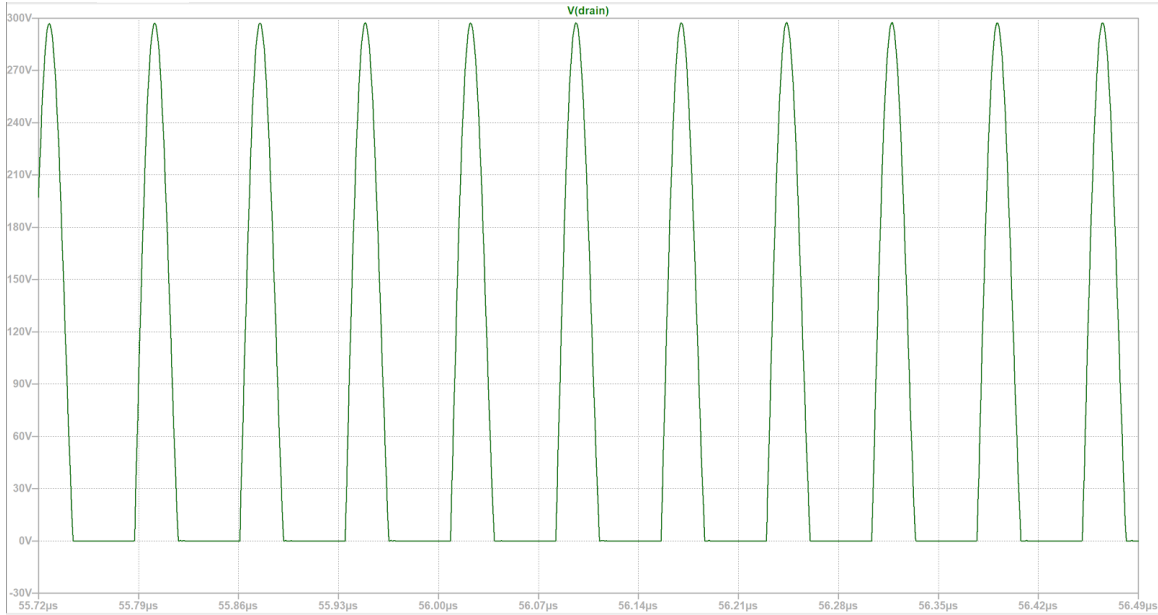


Figure 3-9: Drain to Source Voltage of Class E With Resistive Model as Load .

Source Model

Now we see the completed simulation of the Class E inverter with the source model below. Note how the k changes to 0.135.

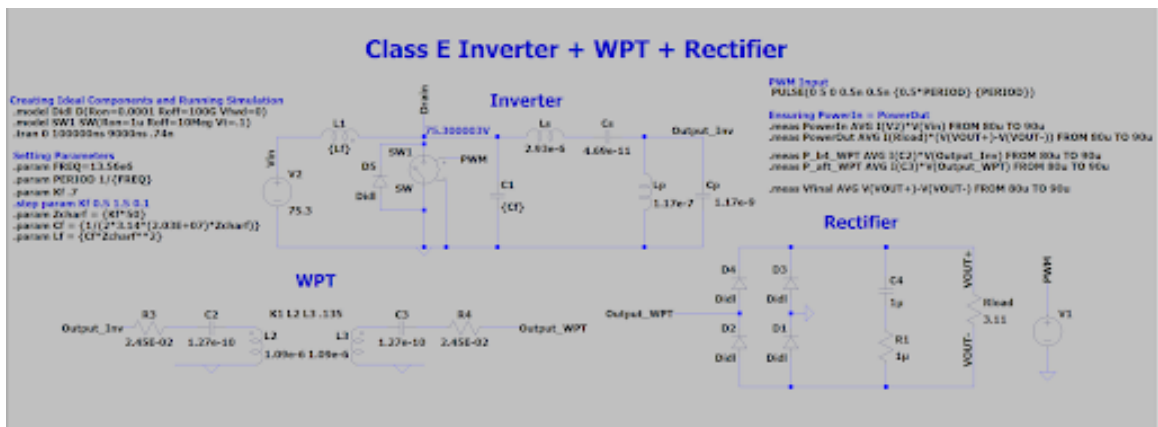


Figure 3-10: Class E With WPT and Rectifier With Source Model as Load.

Figure 3-11 shows the output voltage of the system across the source load, $V(Vout+ - Vout-)$, and the voltage at the output of the WPT module that is inputted into the input of the rectifier.

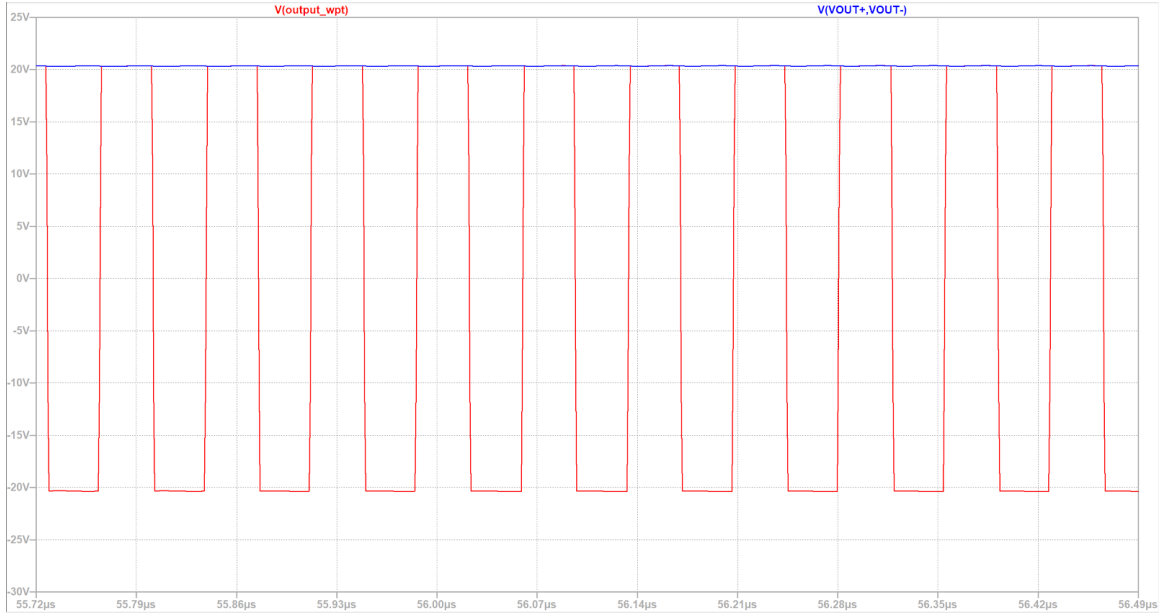


Figure 3-11: Output Voltage of System and Output Voltage of WPT of Class E With Source Model as Load.

Note how the waveform in the figure below resembles the drain to source waveform of the Class E inverter with only the $50\ \Omega$ load.

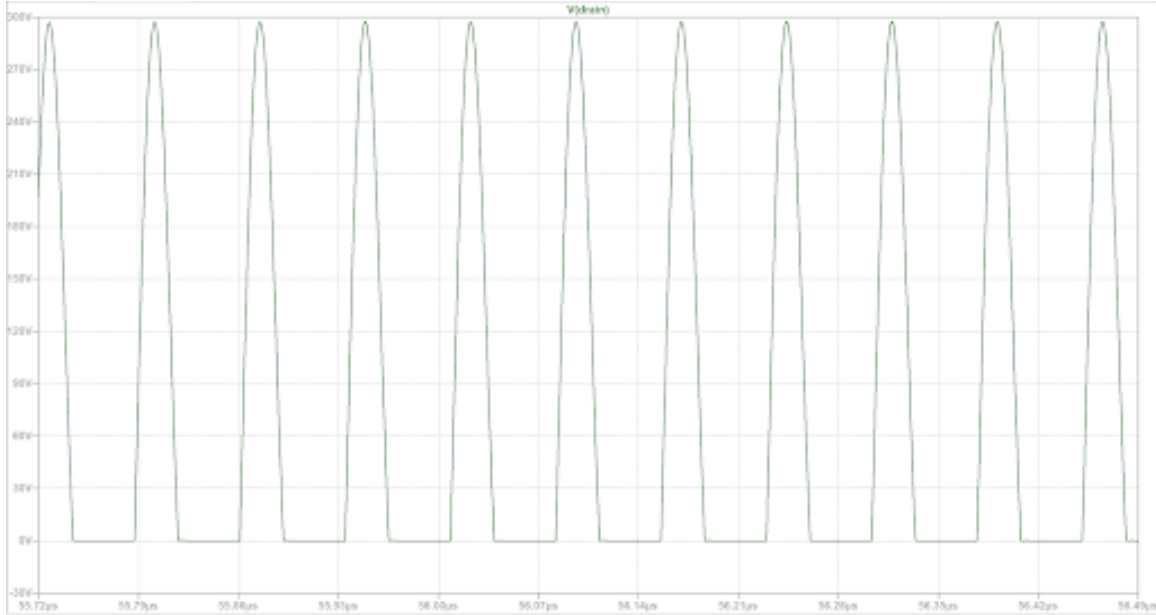


Figure 3-12: Drain to Source Voltage of Class E With Source Model as Load .

3.2 Assumptions

A few assumptions were made for the simulations included in this thesis. The first is that the power electronics are efficient with very little loss. The only loss within this system is within the WPT module. In order to calculate efficiency, the parasitic resistance of the coils needed to be calculated, as shown in one of the previous chapters.

These diodes are almost ideal, with an on-resistance of $0.1 \text{ m}\Omega$ and an off resistance of $10 \text{ G}\Omega$. There is no forward voltage drop. The switches used for these simulations had an on resistance of $1 \text{ }\mu\Omega$, an off resistance of $10 \text{ M}\Omega$, and a voltage threshold of 0.1 V . These assumptions were made because power converters are conventionally analyzed with ideal components so that loss can be lumped in later. If components cause sufficient loss that changes the operation of the converter, then these components are not worth using.

The simulations were run with a maximum time step of 0.74 ns to increase accuracy. The time scales may vary from figure to figure, but comparisons can be made since operation is in periodic steady state.

To ensure that the finished system with the three modules was properly matched

to a $50\ \Omega$ load, the output and input power of the inverters with a $50\ \Omega$ load was compared to the output and input power of the inverters with the WPT module and with the rectifier. The output and input power had a difference of $< 2\ \text{W}$ for each system, which is to be expected with ideal components. This power was calculated using LTspice measure statements after steady state to avoid any transients and with the accurate coupling coefficient for each system. For comparison, the systems with the WPT and rectifier modules used the resistive load.

Table 3.1: Differences in Power Between Simulations.

Simulation	Input Power (W)	Output Power (W)
Class E with $50\ \Omega$ Load	169.094	168.772
Class E with WPT and Rectifier	165.895	164.321
Phi-2 with $50\ \Omega$ Load	161.67	160.947
Phi-2 with WPT and Rectifier	155.841	154.093

The power difference between the Class E with $50\ \Omega$ load and the Class E with WPT and Rectifier is less than 3%. This power difference is because of the parasitic resistance of the coils. The power difference between the Phi-2 with $50\ \Omega$ load and the Phi-2 with WPT and Rectifier is less than 4.5%. This difference is because of the parasitic resistance of the coils and because the trapezoidal output waveform of the Phi-2 relies on harmonics, while the output of the Class E is purely sinusoidal.

3.3 Results

In this section, we will show the results of changing the coupling coefficient and the distance on efficiency. The efficiency was calculated using (1.18).

The graph below shows how the coupling coefficient falls off steeply as distance increases.

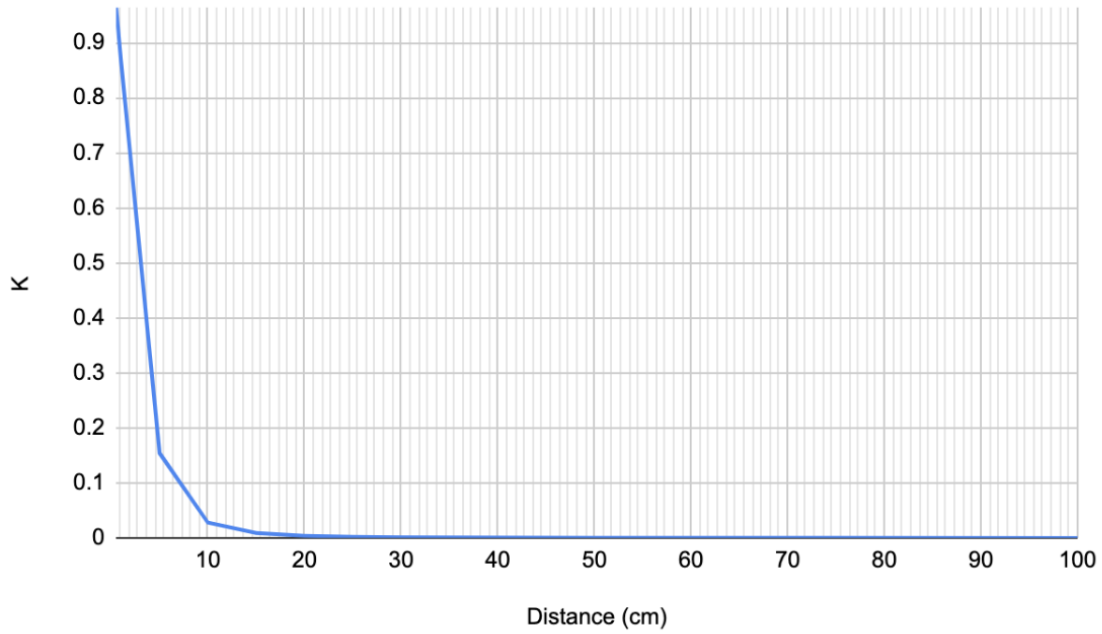


Figure 3-13: Effect of Distance on Coupling Coefficient.

Below are some graphs with both the resistive model and the source model that show how the efficiency of the WPT module responds as the coupling coefficient changes and as the distance between the coils increases. $R_l = 3.84 \Omega$ for the resistive model and $R_l = 3.811 \Omega$ for the source model.

As seen in the figures below, as the coupling coefficient increases for both models, the efficiency increases.

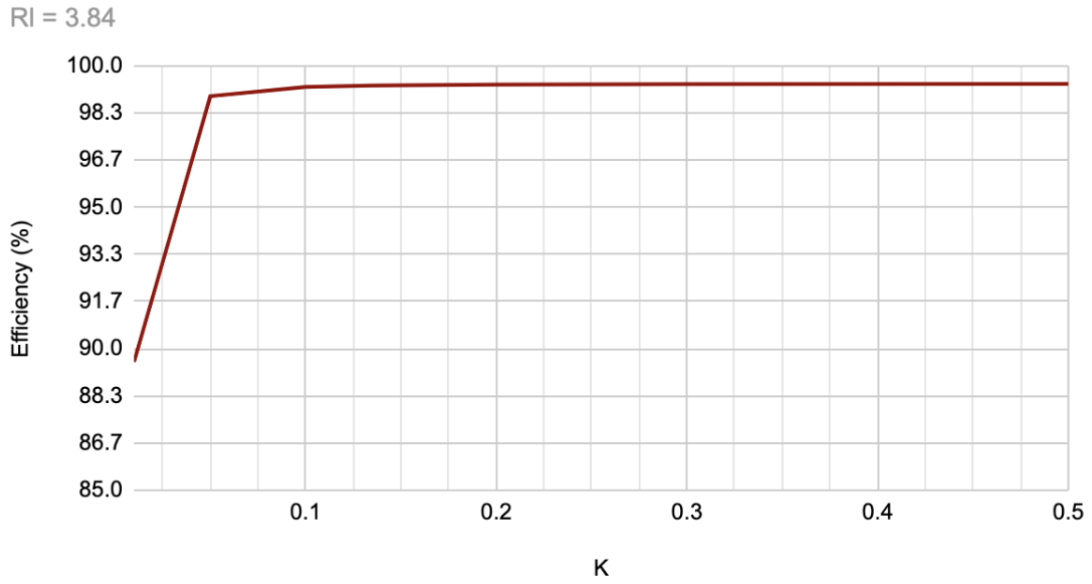


Figure 3-14: Effect of Coupling Coefficient on Efficiency for Resistive Model.

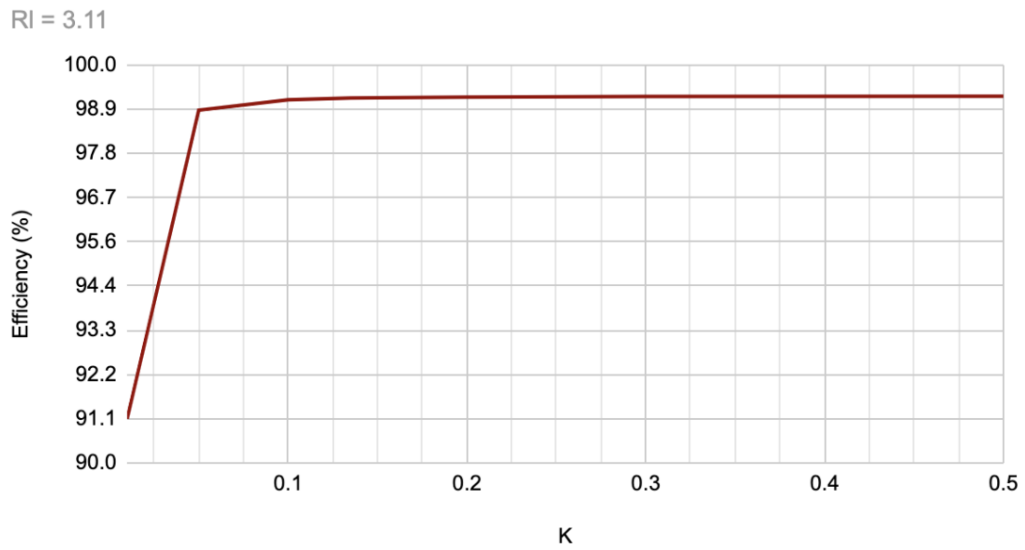


Figure 3-15: Effect of Coupling Coefficient on Efficiency for Source Model.

The next two figures are plots of the effect of distance on the efficiency. As the distance increases, the efficiency drastically decreases. With these coil parameters, in order to keep efficiency above 80%, the coils must be separated by at most 20 cm. Note that this is the upper bound on the efficiency at 20% since this is an ideal simulation.

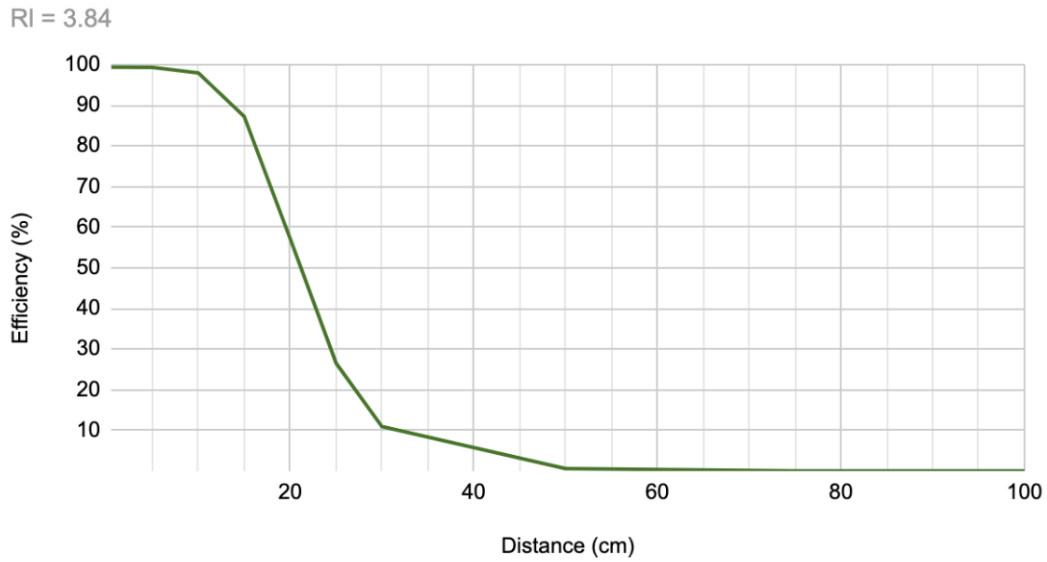


Figure 3-16: Effect of Distance on Efficiency for Resistive Model.

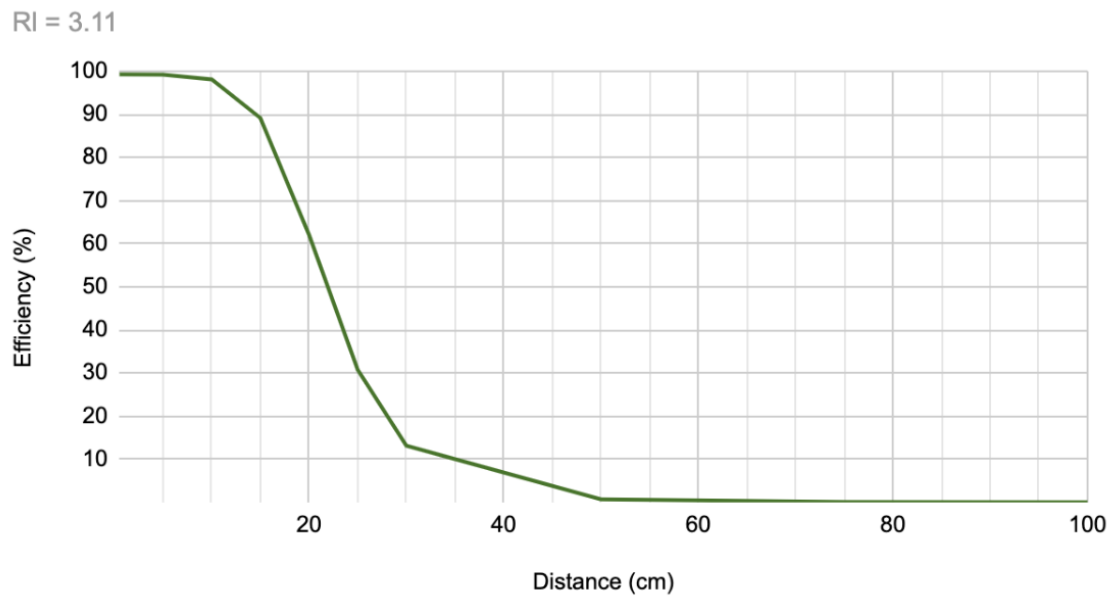


Figure 3-17: Effect of Distance on Efficiency for Source Model.

Chapter 4

Discussion and Future Work

4.1 Discussion

The main contribution of this thesis is a clear, concise framework for the development of two complicated inverters, a WPT system, and a rectifier. This thesis provides a step by step outline on the derivation of values and operation of each inverter. It also outlines how coil geometry affects inductance and how the distance between the coils changes the efficiency. This thesis gathers valuable information on how to use the WPT module and the rectifier as matching networks.

A few takeaways from the results of this thesis:

The efficiency shown in the plots above is the efficiency of the WPT module. With these coil parameters, in order to keep efficiency above 80%, the coils must be separated by at most 20cm. Different parameters will change these efficiency curves. Coils with a greater diameter will allow for power to be transferred at greater distances while maintaining suitable efficiencies.

Some underwater systems, such as submarines, have many different pressure housings with connectors and wires or cables between them that transfer power and data from one pressure housing to the next. To minimize the cost and size of these connectors and cables, pressure housings are usually close to each other. 80% efficiency at 20cm is suitable for these applications.

From the plots shown above, we can make a highly efficient system if the impedance

of the WPT and rectifier modules can be made to look like a $50\ \Omega$ load. This happens if the matching network made by the WPT and rectifier is perfectly tuned to $50\ \Omega$.

Based on the power calculations earlier, the Class E is mildly more efficient than the Phi-2. However, note that the inverters were designed to be 100% efficient in the simulation. The Class E also has a smaller input inductor, leading to faster transient response. The Class E's sinusoidal output waveform is simpler to connect to other modules than the Phi-2's.

4.2 Future Work

The next steps for this thesis include collecting more data to find parameters where both coil diameter and efficiency are maximized.

After this data is collected, future work includes replacing the PWM gate signal with discrete implementations of the gate drivers and selecting components that fit the calculated values. The ideal diode, ideal switch, and the rest of the components in the simulation would be replaced with non-ideal, physical versions. In addition, the simulations would include other non-idealities and some of the assumptions used earlier would no longer hold.

The simulations displayed in this thesis would be repeated with the non-ideal, physical components. Similar data will be gathered and contrasted to the ideal data in this thesis. Now that non-idealities are introduced, further questions to investigate include the effect of frequency on the overall system design and efficiency.

After these simulations, the next steps are to use electronic design software, such as Altium, to capture the schematic simulated in LTSpice with the selected physical components. Since the inverter operation is at such high frequency, the placement, layout, and stackup of the printed circuit board (PCB) will be carefully designed. It's important to follow PCB design guidelines, such as avoiding cross talk, minimizing ground loops, adding ground vias and teardrops to reduce mechanical and thermal stress. It's also valuable to take into consideration the series inductance of each trace and the fact that every trace has capacitance between the trace and the return path of

the signal on the trace. This is especially true at the high frequencies of the systems in this thesis.

It would be valuable to compare the weight of components, the power density, the and board space of the two inverters. Optimizing for high power density, low component count, minimal weight, integration of passives into trace structures, and high efficiency would be ideal for harsh underwater environments.

Bibliography

- [1] S. Y. R. Hui, Wenxing Zhong, and C. K. Lee. A Critical Review of Recent Progress in Mid-Range Wireless Power Transfer. *IEEE Transactions on Power Electronics*, 29(9):4500–4511, September 2014.
- [2] S. Y. R. Hui. Magnetic resonance for wireless power transfer. <https://spiral.imperial.ac.uk/bitstream/10044/1/38935/2/Magnetic%20Resonance%20and%20Wireless%20Power%20Transfer-5-final.pdf>.
- [3] Zhang Bin and Hao Xiao-hong. Modeling and analysis of wireless power transmission system via strongly coupled magnetic resonances. In *2014 International Conference on Mechatronics and Control (ICMC)*, pages 70–75, July 2014.
- [4] Seong-Min Kim, Jung-Ick Moon, In-Kui Cho, Jae-Hoon Yoon, and Woo-Jin Byun. 130w power transmitter for wireless power charging using magnetic resonance. In *2014 IEEE 36th International Telecommunications Energy Conference*, pages 1–5, September 2014. ISSN: 2158-5210.
- [5] Rohan Bhutkar and Sahil Sapre. Wireless energy transfer using magnetic resonance. In *2009 Second International Conference on Computer and Electrical Engineering*, volume 1, pages 512–515, December 2009.
- [6] Introduction to wireless battery charging | renesas. <https://www.idt.com/us/en/products/power-management/wireless-power/introduction-to-wireless-battery-charging>.
- [7] André Kurs, Aristeidis Karalis, Robert Moffatt, J. D. Joannopoulos, Peter Fisher, and Marin Soljačić. Wireless Power Transfer via Strongly Coupled Magnetic Resonances. *Science*, 317(5834):83–86, July 2007.
- [8] Gunbok Lee, Benjamin H. Waters, Chen Shi, Wee Sang Park, and Joshua R. Smith. Design considerations for asymmetric magnetically coupled resonators used in wireless power transfer applications. In *2013 IEEE Topical Conference on Wireless Sensors and Sensor Networks (WiSNet)*, pages 124–126, January 2013.
- [9] Olutola Jonah and Stavros V. Georgakopoulos. Optimal helices for wireless power transfer via magnetic resonance. In *WAMICON 2012 IEEE Wireless Microwave Technology Conference*, pages 1–4, April 2012.

- [10] Mike Ranjram. The evolution, trade-offs, and potential of wireless power transfer. Final Project for Massachusetts Institute of Technology Course 6.332, December 2018.
- [11] *Magnetic Circuits and Transformers: A First Course for Power and Communication Engineers*. Cambridge, Mass. : MIT-Press, 1943., 1943.
- [12] Frederick Emmons Terman. *Radio engineer's handbook*. McGraw-Hill Book Company, inc, 1st ed edition, 1943.
- [13] N.O. Sokal and A.D. Sokal. Class e-a new class of high-efficiency tuned single-ended switching power amplifiers. *IEEE Journal of Solid-State Circuits*, 10(3):168–176, June 1975.
- [14] L. Roslaniec and D. J. Perreault. Design of variable-resistance class e inverters for load modulation. In *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 3226–3232, Sep. 2012.
- [15] N.O. Sokal. Class-E RF power amplifiers. In *Proc. QEX*, pages 9–20, February 2001.
- [16] Yehui Han, Olivia Leitermann, David A. Jackson, Juan M. Rivas, and David J. Perreault. Resistance compression networks for radio-frequency power conversion. *IEEE Transactions on Power Electronics*, 22(1):41–53, January 2007.
- [17] H. Chireix. High Power Outphasing Modulation. *Proceedings of the Institute of Radio Engineers*, 23(11):1370–1392, November 1935.
- [18] F. Raab. Efficiency of Outphasing RF Power-Amplifier Systems. *IEEE Transactions on Communications*, 33(10):1094–1099, October 1985.
- [19] A. Birafane and A.B. Kouki. On the linearity and efficiency of outphasing microwave amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 52(7):1702–1708, July 2004.
- [20] Frederick H Raab, Peter Asbeck, Steve Cripps, Peter B Kenington, Zoya B Popovich, Nick Pothecary, John F Sevic, and Nathan O Sokal. RF and Microwave Power Amplifier and Transmitter Technologies — Part 3. *High-Frequency Electronics*, pages 34–48, September 2003.
- [21] I. Hakala, D.K. Choi, L. Gharavi, N. Kajakine, J. Koskela, and R. Kaunisto. A 2.14-GHz Chireix outphasing transmitter. *IEEE Transactions on Microwave Theory and Techniques*, 53(6):2129–2138, June 2005.
- [22] David J. Perreault. A New Power Combining and Outphasing Modulation System for High-Efficiency Power Amplification. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 58(8):1713–1726, August 2011.

- [23] Tao Ni and Falin Liu. A new impedance match method in serial chireix combiner. In *2008 Asia-Pacific Microwave Conference*, pages 1–4, December 2008. ISSN: 2165-4743.
- [24] Walter Gerhard and Reinhard Knoechel. Improved Design of Outphasing Power Amplifier Combiners. In *2009 German Microwave Conference*, pages 1–4, March 2009. ISSN: 2167-8030.
- [25] Ramon Beltran, Frederick H. Raab, and Arturo Velazquez. HF outphasing transmitter using class-E power amplifiers. In *2009 IEEE MTT-S International Microwave Symposium Digest*, pages 757–760, June 2009. ISSN: 0149-645X.
- [26] Mark P. van der Heijden, Mustafa Acar, Jan S. Vromans, and David A. Calvillo-Cortes. A 19W high-efficiency wide-band CMOS-GaN class-E Chireix RF outphasing power amplifier. In *2011 IEEE MTT-S International Microwave Symposium*, pages 1–4, June 2011. ISSN: 0149-645X.
- [27] Alexander S. Jurkov and David J. Perreault. Design and control of lossless multi-way power combining and outphasing systems. In *2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 1–4, August 2011. ISSN: 1548-3746.
- [28] Alexander S. Jurkov, Lukasz Roslaniec, and David J. Perreault. Lossless multi-way power combining and outphasing for high-frequency resonant inverters. In *Proceedings of The 7th International Power Electronics and Motion Control Conference*, volume 2, pages 910–917, June 2012.
- [29] M.J. Chudobiak. The use of parasitic nonlinear capacitors in class E amplifiers. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, 41(12):941–944, December 1994.
- [30] Xiuqin Wei, Hiroo Sekiya, Shingo Kuroiwa, Tadashi Suetsugu, and Marian K. Kazimierczuk. Design of Class-E Amplifier With MOSFET Linear Gate-to-Drain and Nonlinear Drain-to-Source Capacitances. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 58(10):2556–2565, October 2011.
- [31] J. M. Rivas, Y. Han, O. Leitermann, A. D. Sagneri, and D. J. Perreault. A high-frequency resonant inverter topology with low-voltage stress. *IEEE Transactions on Power Electronics*, 23(4):1759–1771, July 2008.
- [32] W.C. Bowman, F.T. Balicki, F.T. Dickens, R.M. Honeycutt, W.A. Nitz, W. Strauss, W.B. Suiter, and N.G. Ziesse. A resonant DC-to-DC converter operating at 22 megahertz. In *APEC '88 Third Annual IEEE Applied Power Electronics Conference and Exposition*, pages 3–11, February 1988.
- [33] Richard Redl, Bela Molnar, and Nathan O. Sokal. Class E Resonant Regulated DC/DC Power Converters: Analysis of Operations, and Experimental Results at 1.5 MHz. *IEEE Transactions on Power Electronics*, PE-1(2):111–120, April 1986.

- [34] H. Koizumi, M. Iwadare, and S. Mori. Class e2 DC/DC converter with second harmonic resonant class E inverter and Class E rectifier. In *Proceedings of 1994 IEEE Applied Power Electronics Conference and Exposition - ASPEC'94*, pages 1012–1018 vol.2, February 1994.
- [35] Juan M. Rivas, David Jackson, Olivia Leitermann, Anthony D. Sagneri, Yehui Han, and David J. Perreault. Design considerations for very high frequency dc-dc converters. In *2006 37th IEEE Power Electronics Specialists Conference*, pages 1–11, June 2006. ISSN: 2377-6617.
- [36] V. Tyler. A new high-efficiency high-power amplifier. *The Marconi Review*, 21(130):96–109, 1958.
- [37] Joshua W. Phinney, David J. Perreault, and Jeffrey H. Lang. Radio-frequency inverters with transmission-line input networks. In *2006 37th IEEE Power Electronics Specialists Conference*, pages 1–9, June 2006. ISSN: 2377-6617.
- [38] Daniel Goodman, Andrzej Bortkiewicz, Gary D. Alley, Stephen F. Horne, and William M. Holber. Rf power supply with integrated matching network, May 2005. US Patent 6,887,339.
- [39] R. Frey. 500 W, Class E 27.12 MHz Amplifier Using A Single Plastic MOSFET, 1999. Advanced Power Technology Application Note APT9903.
- [40] J.M. Rivas, R.S. Wahby, J.S. Shafran, and D.J. Perreault. New Architectures for Radio-Frequency DC–DC Power Conversion. *IEEE Transactions on Power Electronics*, 21(2):380–393, March 2006.
- [41] Y.S. Lee and Y.C. Cheng. A 580 kHz switching regulator using on-off control. *Journal of the Institution of Electronic and Radio Engineers*, 57(5):221–226, September 1987.
- [42] Minoru Iwadare, Shinsaku Mori, and Kazunaga Ikeda. Even harmonic resonant class E tuned power amplifier without RF choke. *Electronics and Communications in Japan (Part I: Communications)*, 79(1):23–30, 1996.
- [43] Andrei Grebennikov. Load Network Design Techniques for Class E RF and Microwave Amplifiers. *High-Frequency Electronics*, pages 18–32, July 2004.
- [44] M.J. Chudobiak. The use of parasitic nonlinear capacitors in class E amplifiers. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, 41(12):941–944, December 1994.
- [45] S.D. Kee, I. Aoki, A. Hajimiri, and D. Rutledge. The class-E/F family of ZVS switching amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 51(6):1677–1690, June 2003.

- [46] F.H. Raab. Class-F power amplifiers with maximally flat waveforms. *IEEE Transactions on Microwave Theory and Techniques*, 45(11):2007–2012, November 1997.
- [47] Kazuhiko Honjo. A simple circuit synthesis method for microwave class-F ultra-high-efficiency amplifiers with reactance-compensation circuits. *Solid-State Electronics*, 44(8):1477–1482, August 2000.
- [48] F.H. Raab. Maximum efficiency and output of class-F power amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 49(6):1162–1166, June 2001.
- [49] Andrei Grebennikov. Effective Circuit Design Techniques to Increase MOSFET Power Amplifier Efficiency. *Microwave Journal*, pages 64–72, July 2000.
- [50] A.V. Grebennikov. Circuit design technique for high efficiency Class F amplifiers. In *2000 IEEE MTT-S International Microwave Symposium Digest (Cat. No.00CH37017)*, volume 2, pages 771–774 vol.2, June 2000. ISSN: 0149-645X.
- [51] Andrei Grebennikov. *RF and Microwave Power Amplifier Design*. McGraw Hill Professional, September 2004.
- [52] J. Phinney, J.H. Lang, and D.J. Perreault. Multi-resonant microfabricated inductors and transformers. In *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, volume 6, pages 4527–4536 Vol.6, June 2004. ISSN: 0275-9306.
- [53] Joshua W. Phinney. *Multi-Resonant Passive Components for Power Conversion*. PhD dissertation, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, June 2005.
- [54] Morgan Brooks and H.M. Turner. *Inductance of Coils*, chapter 1. University of Illinois, 1912.
- [55] Jungwon Choi, Wei Liang, Luke Raymond, and Juan Rivas. A High-Frequency Resonant Converter Based on the Class Phi2 Inverter for Wireless Power Transfer. In *2014 IEEE 79th Vehicular Technology Conference (VTC Spring)*, pages 1–5, May 2014. ISSN: 1550-2252.