Millivolt Silicon Photonic Modulators for Cryogenic Applications

by

Marc de Cea Falco

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Author..
Department of Electrical Engineering and Computer Science
May 15, 2020

Certified by ....
Rajeev J. Ram
Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Accepted by..
Leslie A. Kolodziejski
Professor of Electrical Engineering and Computer Science
Chair, Department Committee on Graduate Students

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Abstract

Cryogenic technologies promise to overcome existing bottlenecks in a range of science and engineering fields including quantum computing, high performance computing and single-photon communication systems. As these technologies mature and systems scale, a readout solution for high speed, low power data transfer between the cryogenic environment and room temperature becomes essential.

The use of optical links for such data transfer - in what is known as cryogenic optical readout - is appealing due to the low heat conduction of optical fiber and the possibility to exploit wavelength division multiplexing architectures. However, existing demonstrations suffer from large power dissipation associated with amplifying the millivolt signals generated by the cryogenic systems.

This thesis deals with the development of silicon photonic modulators operating at cryogenic temperatures and capable of modulating an optical carrier with millivolt-level driving signals. We show cryogenic operation of CMOS photonic resonant modulators in the forward bias regime with high modulation efficiency and reduced power dissipation, and demonstrate cryogenic optical readout of a superconducting single photon detector. We also present a new operation mode for optical modulators that leverages parasitic photocurrent to achieve electrical gain and reduce power dissipation. Modulation with signal levels down to 4 mVpp and electrical power dissipation in the zJ/bit range is demonstrated.

This thesis sets the foundation for silicon photonics to realize scalable, low power, high throughput cryogenic readout, addressing one of the key remaining challenges for the wide adoption of cryogenic technologies.

Thesis Supervisor: Rajeev J. Ram
Title: Professor of Electrical Engineering and Computer Science

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Chapter 1

Introduction

1.1 Integrated optics

Ever since the first laser source was developed around 1960, the use of optical beams to perform a wide variety of operations has increased to the point where it is hard to imagine modern life without it: medicine, biology, communications, imaging, defense, basic science, space exploration, navigation, consumer products... all these and many others are fields where optical beams are routinely used.

Most of these applications require not only the generation of an optical beam, but also its manipulation to adapt it to some specific requirements. Traditionally, the components necessary to perform these manipulations (prisms, mirrors, collimators, electro-optic modulators, photodetectors, beam combiners, optical isolators...) are bulky, to the point where a dedicated table several meters long is necessary to implement any useful optical system.

As a response, Stewart Miller proposed the integration of all these components in a single, planar chip in his seminal paper published in 1969 [1] which initiated

the field of integrated optics. By exploiting the large index of refraction contrast between a 'core' and a 'cladding' material, nano- and micro-meter size structures that could guide and manipulate light were proposed and soon after experimentally demonstrated. This enabled the miniaturization of complex optical systems and a decrease in manufacturing costs, which ultimately resulted in such systems accessing the consumer market. Since then, an impressive range of integrated optical devices and systems have been proposed, realized and commercialized.

Different material platforms have been used over the years to realize integrated optical systems. Significant work has been done on platforms based on III-V semiconductors such as gallium arsenide (GaAs) [2] or indium phosphide (InP) [3], mainly because of their efficient electro-optic mechanisms and direct bandgap, which allows for the realization of on-chip lasers.

III-V materials have, nevertheless, several drawbacks [4]. Their maximum available wafer size to date is limited to about 200 mm (8") - with the typical size being 4" -, which raises concerns about its scalability and increases manufacturing costs. Its relatively low index contrast makes the devices large compared to other material platforms. Most importantly, the realization of complex electrical circuits in the same chip is challenging due to a limited transistor yield. This prevents monolithic integration of electronic and optical devices, which is highly desirable since nearly all modern photonic systems require control electronics.

A very attractive alternative to III-V material platforms is the use of silicon (Si), in what is know as Silicon Photonics.

1.1.1 Silicon photonics

The potential to use Si as a material for integrated optics has been recognized since the 1980s [5,6]. Because of the wide adoption of silicon in electronic systems manufacturing, there is a strong case towards its use in integrated optics: all the knowledge, research, fabrication and manufacturing processes, infrastructure and technologies developed over the last century by the microelectronics industry can be readily exploited to realize silicon photonic systems. Not only this, but using silicon allows for the fabrication of complex, high performance electronic circuits in the same chip ('monolithically'), alongside the photonic components. Therefore, complex control circuitry, as well as functionality requiring both electrical and optical operations, can be implemented without the need of co-packaging multiple chips.

Furthermore, silicon is an inexpensive, extremely well understood material with a high quality native oxide. The high index contrast between this oxide and the silicon allows for the realization of high optical confinement structures in standard Silicon on Insulator (SOI) platforms [7], enabling the realization of low loss optical waveguides and very compact photonic devices.

Once these advantages were recognized both by industry and academia, rapid development of a great variety of high performance optical and electro-optical devices and systems in silicon platforms followed [8, 9]. While most of the early development was directed towards the telecom and datacom spaces (as will be discussed in the next section), a range of optical systems for a variety of applications have been demonstrated in silicon photonics platforms. Examples include sensing [10], nonlinear optics [11], quantum optics [12] and computation [13].

1.2 Short reach optical interconnects

It is well known that optical communication is the standard solution for long-haul data communication due to its low loss, high speed and low sensitivity to interference compared to copper-based cables. While these advantages still hold for short and medium reach interconnects (mm - 1 km), the use of optical communication for these distances has traditionally been hindered by the ability of copper-based interconnects to deliver the necessary performance at a much lower cost.

Nevertheless, as the requirements for higher data rates and lower power consumption increase, copper is reaching its performance limits due to increased attenuation (Fig. 1-1), crosstalk and dispersion, making optical links a promising alternative [14, 15]. The need to offer high performance short reach optical interconnects at a competitive cost level makes the use of a photonic integrated platform a natural choice [16, 17], and silicon photonics postulates as a highly desirable platform.

As a result, significant effort has been applied by both academia and industry to realize efficient, low power, high performance optical interconnects in a silicon photonics platform through different approaches ([18–22] amongst others).

1.2.1 Zero-change CMOS silicon photonic optical interconnects

To enhance device and system performance, most silicon photonic platforms incorporate additional materials not present in traditional Si manufacturing processes in what is know as hybrid silicon photonics [24]. This is due to silicon's indirect bandgap, which prevents the possibility of fabricating native, high efficiency light sources [25], and the fact that second order nonlinearities (which are typically used
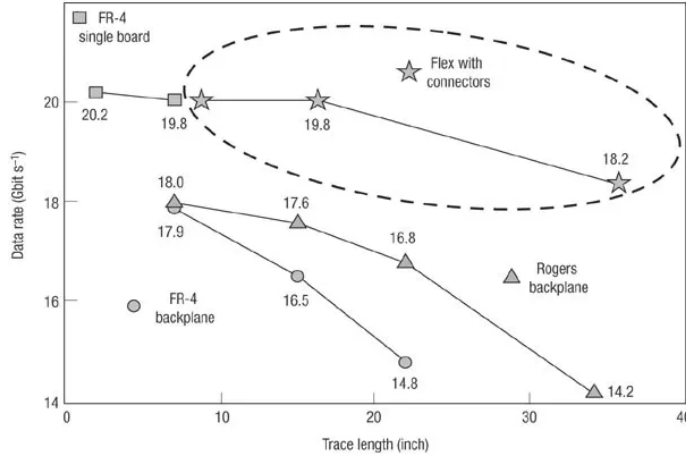
Figure 1-1: Measured electrical data rates as a function of link distance for various copper-based material systems including standard FR4, Rogers and Flex. Measurements are based on forwarded clock transceiver, fabricated using 90 nm CMOS technology. Reproduced from [23].

to implement active optical devices) are non-existent or very weak in Si [11]. Although this approach allows for optimized photonic devices, the need to use a modified CMOS process increases manufacturing costs and, more importantly, reduces transistor yield, preventing the successful integration of optics and electronics in the same chip.

On the contrary, the zero-change CMOS approach [27, 28] implements photonic devices and systems in commercial, unmodified CMOS fabrication processes. Using the exact same processes as an industry that manufactures billions of devices and chips per month (more than 20 trillion transistors are fabricated every second!) allows for reduced cost, the potential to scale production and close to 100% transistor yield, enabling seamless integration of photonics and electronics in the same chip. These come at a cost to the performance of the photonic components, not only because additional materials cannot be added, but also because flexibility and control over the fabrication process is lost.

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The zero-change CMOS approach has proved successful. A complete toolbox of high performance photonic components has been realized in a commercial, unmodified 45 nm SOI process, and a working chip integrating over 70 million transistors and 850 photonic components was demonstrated in 2015 [26] (Fig. 1-2). More recently (2018), a transceiver chip with a bandwidth density close to 1 Tbps/mm^2 and an overall power consumption of 0.83 pJ/bit was demonstrated in the same process [29].

Clearly, zero-change CMOS enables electro-optic integration of complex systems in a single chip, allowing for the implementation of high speed, low cost and low power consumption photonic interconnects. As a result, the application and commercialization of these interconnects in the chip-to-chip and data center communication spaces is already a reality [19].
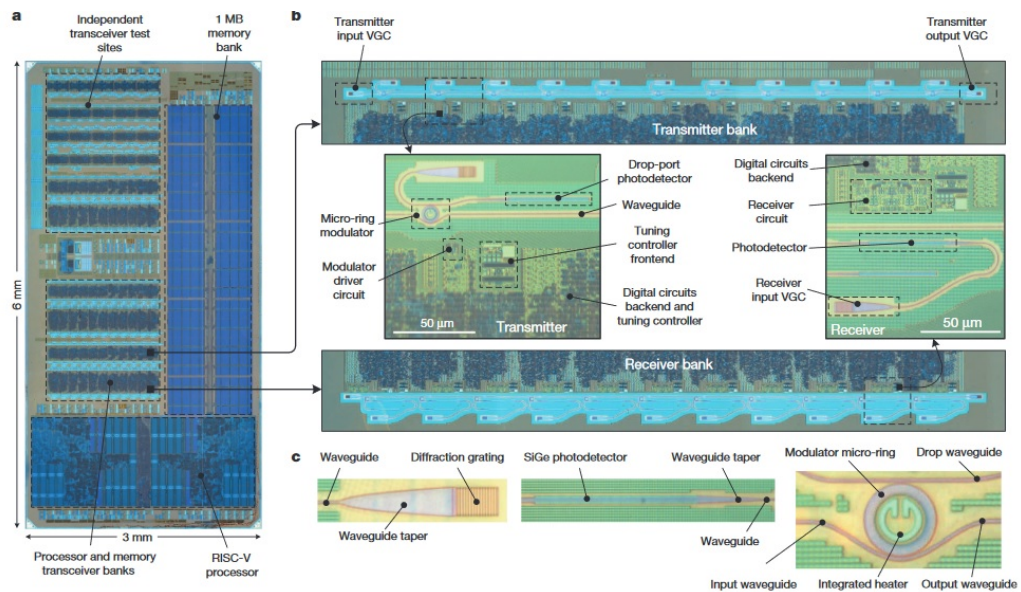
Figure 1-2: Silicon photonic transceiver on a zero-change CMOS platform [26]. (a) Micrograph of the chip, with 70 million transistors and 850 photonic components. (b) Transmitter and receiver banks. (c) Photonic components. From left to right, micrographs of the grating coupler, photodetector and optical modulator.

The advantages of this approach can be exploited in other application spaces requiring low power, high speed data communication. In this thesis we will explore the suitability of silicon photonic interconnects for the cryogenic readout problem, which will be discussed in depth in the next section.

1.3   The cryogenic readout problem

Operation at cryogenic temperatures ($<$77 K) allows us to leverage physical phenomena that are not dominant at higher temperatures, as well as to realize devices and systems with unmatched performance. Because of this, a range of cryogenic technologies are being pursued to solve current bottlenecks in sensing, computation and communications. Examples include quantum computing [30, 31], quantum metrology [32], superconducting electronics [33, 34], single photon imaging [35] and space-based communications [36, 37].

All the above mentioned technologies need a way to communicate to the outside of the cryogenic environment for feedback and control, further processing or communication to room temperature networks and systems. Due to the limited cooling power of the cryogenic environment, a high speed readout architecture that can sustain the needs in latency and throughput with minimal power dissipation is required.

1.3.1   Cryogenic applications from a readout perspective

Before introducing different cryogenic readout architectures and analyzing their advantages, limitations and challenges, it is of interest to briefly discuss representative cryogenic applications and their requirements from the point of view of readout to room temperature. As we will show, different cryogenic technologies, while present-

ing common requirements, have a different set of critical performance metrics which are mainly dictated by its application space. This is of critical importance when evaluating different device designs and system architectures.

Superconducting nanowire single photon detectors

Superconducting Nanowire Single Photon Detectors (SNSPDs) are the highest performing detectors for time-sensitive single-photon counting available from the ultraviolet to the mid-infrared thanks to its high detection efficiency, low dark counts and excellent timing resolution [38]. Due to their unrivalled low timing jitter -the uncertainty in the time it takes for an output voltage pulse to be generated after the absorption of a photon-, SNSPDs are used in a wide range of applications requiring very high timing resolution, such as optical communications [39], quantum optics, quantum computing and quantum communications [40] and lidar [41].

An SNSPD consists of a narrow wire patterned from a thin superconducting film that behaves as a switch that is activated by the detection of a single photon [42,43]. Typical cross-sectional dimensions for these nanowires are 1 nm - 10 nm thick and 80 nm - 200 nm wide. When a photon is absorbed, the superconducting wire develops a local resistive region, or hotspot, with a resistance on the order of kΩ. By detecting this resistance change through a readout circuit, a single photon detector can be realized.

It is of interest to collect a set of representative characteristics and requirements for SNSPD readout, which we will use in later sections to derive specifications for a suitable cryogenic readout architecture. These are summarized in Table 1.1:

- The voltage signals generated by an SNSPD are in the order of 0.1 mV to 0.5 mV into a 50 Ω load, limited by the maximum current that can be applied

Output Voltage	0.1-0.5 mV into a 50 Ω load
Escape bandwidth	1 Gcps (current) ; 100 - 1,000 Gcps (future)
Timing jitter	< 100 ps
Operating temperature	< 4 K, typical $\approx$ 100 mK

Table 1.1: SNSPD readout characteristics.

to the detectors without biasing them in the non-superconducting state (the 'critical current'). Depending on their size, intended operating wavelength and timing specifications, typical SNSPD critical currents range between 1 μA and 10 μA.

- Since the majority of SNSPD applications exploit their excellent timing resolution, a suitable readout architecture needs to conserve a low timing jitter (< 100 ps).

- The maximum number of counts from a single SNSPD is usually limited to 10-100 Mcps due to the large kinetic inductance (the inductance of the superconducting wire associated with the time needed to accelerate its cooper pairs when a voltage is applied) of the devices, which result in a large reset time [44]. In most applications, the ability to fabricate and interface with large arrays of SNSPDs is critical, and as such a suitable cryogenic readout architecture needs to support the aggregated number of counts generated by this array. Arrays with 100-1,000 pixels and < 1 Gcps have been demonstrated [45], but future requirements for imaging, lidar and quantum applications will likely require readout of 100-1,000 Gcps.

Single flux quantum logic

Without a change in the technology used for the realization of High Performance Computing (HPC), exascale computing systems (with more than 1 EFLOP/s) will face tremendous challenges because of power (> 100 MW), cooling and space requirements. With an unrivalled energy consumption and switching speed, digital circuits based on Single Flux Quantum (SFQ) logic are a promising technology to overcome the limitations of current CMOS circuits [33, 34].

The magnetic flux in a current-carrying superconducting ring is quantized, and the flux quantum is given by $\Phi_0 = h/(2e)$, where h is Planck's constant and e is the electron charge. SFQ circuits are based on the manipulation of such single magnetic flux quanta in Josephson Junctions [46]. Since $\Phi_0 \approx 2$ mV·ps, very low power dissipation (in the order of 10^{-19} J) and fast switching speeds (in the order of ps) are achieved. This represents a 1,000x lower power consumption than state-of-the art CMOS logic, which makes SFQ a viable technology to meet the requirements for exascale computing. It is worth noting that SFQ is not yet a mature technology, and outstanding challenges need to be addressed in order to make HPC SFQ systems a reality [34].

One of these challenges is the readout to room temperature. The high switching speed of SFQ circuits allows for the generation of enormous amounts of data, and thus require the readout architecture to sustain a very large escape bandwidth. Assuming a readout rate of 10^{-4} bytes/FLOP, a total bandwidth of 1 Tbps (1,000 Tbps) is needed for a 1 PFLOP/s (EFLOP/s) HPC system [34].

The requirements for a cryogenic readout architecture for SFQ systems are summarized in Table 1.2.

Output Voltage	0.1-0.4 mV into a 50 Ω load, 3-5 mV into a 50 Ω load after a SQUID amplifier
Escape bandwidth	1 Tbps - 1,000 Tbps
Operating temperature	4 K

Table 1.2: SFQ readout characteristics. SQUID = Superconducting Quantum Interference Device.

Quantum computing

Quantum computing and quantum information processing [47] promise to revolutionize the world and transform a wide range of disciplines including chemistry, medicine, biology, cryptography and communications. A range of technologies are being pursued to make quantum computing a reality, but the most promising are those based on trapped ions (where the electronic states of the ions are used as qubit logic levels [48–50]) and superconducting circuits based on Josephson Junctions (where a quantized magnitude such as magnetic flux or electric charge is used as the qubit [30, 51]). Both technologies operate at cryogenic temperatures, and as such require readout to room temperature. The discussion of these technologies is beyond the scope of this thesis, and the interested reader is pointed to the above references.

Typically, trapped ion readout involves the detection of fluorescent photons to discriminate between the ion being in a fluorescent or non-fluorescent state [52]. Currently, this is done via photomultiplier tubes (PMTs) sitting outside of the cryostat, which results in a bulky, expensive readout architecture that cannot be scaled beyond a few qubits (tenths of thousands to a million qubits are required for a useful quantum system with error correction). Approaches that perform the readout through the use of integrated, on chip SNSPDs and Avalanche Photodiodes (APDs) have been proposed but, to the best of the author's knowledge, not experimentally

demonstrated. The challenge in trapped ion readout mainly lies in the design and fabrication of fast, high detection efficiency and ultra low noise (integrated) photodetectors. Readout of the signals generated by these detectors is analogous to the SNSPD readout discussed earlier, and as such we will not consider trapped ion readout for the remainder of this thesis.

On the other hand, superconducting quantum computing is based on dispersive readout, where each qubit is coupled to a resonator whose resonance frequency shifts depending on the qubit state [51, 53]. The qubit state is inferred by measuring such a shift, which is read out to room temperature using a coherent detection scheme. Typically, the resonator frequency is around 5 GHz, which is detuned from the natural resonance frequency of the qubit. While this provides improved coherence time (as it minimizes the effect of the resonator on the qubit state), it also limits the strength of the readout signal to a few (< 10) microwave photons, which at 5 GHz translates into a signal power of -130 dBm. To maximize Signal to Noise Ratio (SNR), and thus readout fidelity, a near-quantum limited parametric amplifier is required to amplify the signal by close to 20 dB.

The low readout signal strength makes the focus of any cryogenic readout architecture for quantum applications be twofold: (1) maximize the SNR while (2) preventing the readout system from decreasing the coherence time of the qubit. These two are arguably more important than minimizing the power dissipation of the readout, at least in the current state of technology development. Likewise, the requirements on readout speed are low (< 100 MHz), although centered at a frequency of about 5 GHz, requiring a suitable readout architecture to sustain such frequencies.

We can derive a representative requirement for the equivalent noise temperature of a cryogenic readout suitable for quantum readout. Assuming 10 signal photons at

the readout resonator, and a desired SNR of 3 dB (6 dB), the necessary equivalent noise temperature of the readout is 1.2 K (1 K). The equivalent noise temperature T of the readout system is given by:

$$T = T_1 + \frac{T_2}{G_1} + \frac{T_3}{G_1 G_2} + ... \tag{1.1}$$

Above, T_i (G_i) is the noise temperature (gain) of the amplifier in stage i. As mentioned above, the first stage of amplification is realized through a quantum-limited parametric amplifier, with a typical gain $G_1 = 20$ dB and a noise temperature $T_1 = 700$ mK [54]. This translates into a required noise temperature of 60 K (40 K) for the readout circuit following the parametric amplifier for a total SNR of 3 dB (6 dB).

The requirements for a cryogenic readout architecture suitable for superconducting quantum computing systems are summarized in Table 1.3. It is worth pointing out that practical systems for quantum computing and signal processing are far from being a reality, and that daunting theoretical and practical challenges need to be overcome in order for quantum processing to be a reality.

Output Voltage	20-50 μV into a 50 Ω load after parametric amplifier
Escape bandwidth	100 MHz, centered at 5 GHz
Equivalent noise temperature	< 60 K after parametric amplifier
Operating temperature	< 1 K, typical ≈ 100 mK

Table 1.3: Quantum readout characteristics.

Figure 1-3: Cryogenic readout architectures. (a) Electrical readout. The signal is transported out of the cryostat through the use of high speed electrical cables, requiring amplification and large cable lengths for heat sinking. (b) A dilution cryostat with electrical readout (image from Google). (c) Optical readout. Electro-optical (EO) devices encode the electrical data into an optical carrier transported out of the cryostat through optical fibers. WDM can be exploited to readout multiple data streams with a single optical fiber. (d) A depiction of how optical readout could look like in a dilution cryostat. By reducing the thermal loads and anchoring requirements and exploiting WDM, optical readout can provide a scalable cryogenic readout solution.

1.3.2 Cryogenic electrical readout

In the previous section we have briefly discussed the readout requirements for a range of representative cryogenic technologies. The typical approach to realize such cryogenic readout is through the use of electrical cables (see Fig. 1-3(a)). While simple and well established, this architecture has several limitations:

- The high thermal conduction of the metal wires presents a high heat load to the cryostat, limiting the maximum number of readout lines. For example, a 1 meter long SMA copper cable carries 100 mW of heat between 290 K and 4.2 K, and 40 mW between 80 K and 4.2 K [55]. Figure 1-4(a,b) shows the thermal conductivity of typical materials used in cryogenic environments.

- Electrical cables have non-negligible losses at microwave frequencies (Fig. 1-4(c)). To compensate for this effect it is necessary to use higher signal levels, increasing the power dissipation inside the cryostat.

- To reduce the impact of the high thermal loads on the lower temperature stages (which have a lower cooling power due to efficiency limits [55]), each electrical connection is thermally anchored at multiple intermediate temperature stages (Fig. 1-3(a, b)), increasing the cost and complexity of the system [56, 57]. Perhaps more importantly, the long cable lengths required for efficient thermal anchoring increase the latency of the readout, which could severely constrain applications in quantum computing [58] or high performance computing [34].

- Electrical cables are sensitive to electromagnetic interference and crosstalk, which makes the realization of readout with high signal fidelity challenging.

- The maximum achievable bandwidth density (a measure of how much data can

be escaped per unit area of the cryostat, measured in Gbps/mm^2) is limited by the physical size of the cryostat, since a single electrical line can in general carry only a single data stream.

- Due to the low signal levels generated by the cryogenic systems (usually in the μV and mV range) an amplification stage inside the cryostat is typically required to achieve a sufficiently high SNR for processing at room temperature. The power consumption of the cryogenic amplifier is in the mW range, which severely increases the heat load to the cryostat and limits the maximum number of readout lines that can be supported.

All the limitations mentioned above make it clear that conventional electrical readout is not a suitable solution for future, large scale cryogenic systems requiring a high number of readout lines with high throughput communication to room temperature (see Fig. 1-3(b)). This is a well-known problem to the different communities working in these cryogenic systems [34, 59, 60].

Substantial efforts have been put into designing devices and alternative architectures to enable a scalable, low power, high throughput solution to the cryogenic problem, but the success to date has been limited (see Table 1.4). For instance, multiple low power electrical amplifier devices and architectures have been reported in the literature [64–70], but the per-channel power consumption is still above the mW level. To eliminate the need for a readout with high bandwidth and high channel count, architectures where a great part of the data processing (which would otherwise happen at room temperature) is done inside the cryostat have also been proposed [71–73]. It is nevertheless unclear if all the necessary computations can be done with low enough power dissipation to not result in heating of the cryogenic environment.
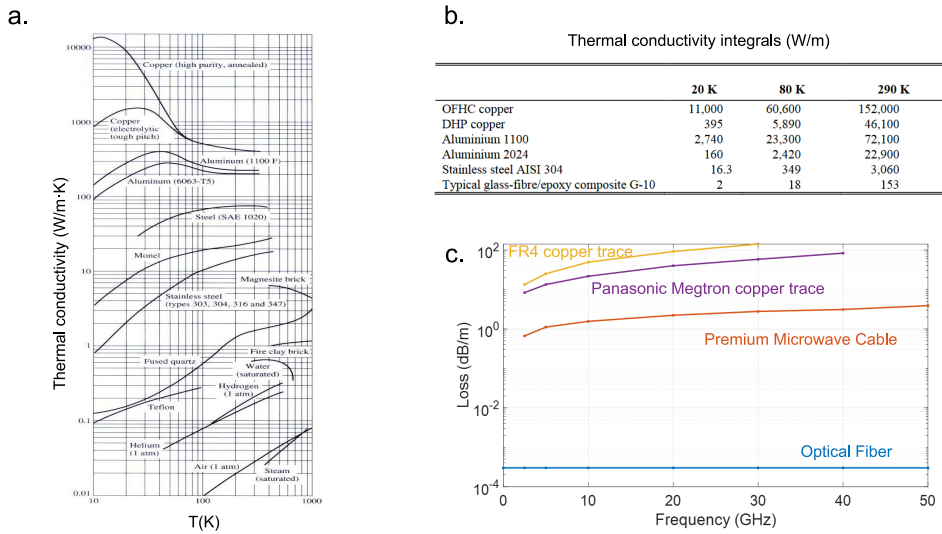
Figure 1-4: Heat conduction and loss in typical materials. (a) Thermal conductivity as a function of temperature. (b) Thermal conductivity integrals between indicated temperatures and 4.2 K [55]. The total heat load is obtained by multiplying the integral by the ratio of cross sectional area and length of the conductor (A/L). The reader is pointed to reference [61] for a compendium of thermal conductivity data of relevant materials. (c) Signal power loss as a function of frequency for optical fiber (blue), high speed microwave cables (orange, [62]), and copper traces in FR4 (yellow) and Megtron substrates (violet) [63].

Regardless, all the above mentioned solutions are based on the use of electrical cables, which have additional drawbacks aside from power consumption. An alternative approach that could overcome most of the limitations of electrical readout is the use of optical fiber communication, which we will discuss in detail in the next section.

1.3.3 Cryogenic optical readout

As we have already discussed, optical communications offer significant advantages when compared to copper in high performance, high speed room temperature in-

Experimental demonstrations of electrical readout of classical (not quantum) technologies

Ref., Year	Brief description	Power [*]	Bandwidth	Energy per bit [†]
[64] 2013	SiGe amplifiers at 3 temp stages (4K - 18K - 50K) for RSFQ readout	300 μW at 4K 2 mW at 18K 20 mW at 50K	Sim. 30 GHz Dem. 400 kHz	Sim. 10 fJ/bit Dem. 750 pJ/bit (4K stage only)
[65] 2009	Commercial p-HEMT transistors for RSFQ readout	4 mW at 4.2K	3 GHz	1.3 pJ/bit
[66] 2018	Commercial GaAs amplifier for SNSPD readout	3 mW at 4K	1.5 GHz	2 pJ/bit
[67] 2003	Hybrid amplifier using JJ and CMOS transistors for RSFQ	500 μW at 4K	Not reported	—
[70] 2017	Hybrid amplifier using an nTron and a commercial HEMT for SFQ readout	12 mW at 4 K	0.5 GHz	24,000 pJ/bit

Experimental demonstrations of electrical readout of quantum technologies

Ref., Year	Brief description	Power [*]	Bandwidth	Energy per bit [†]
[74] 2013	Readout of superconducting transmon qubits	LNA at 3K: 24 mW	20 GHz	1.2 pJ/bit
[75] 2015	Readout of superconducting transmon qubits	LNA at 3K: 4.8 mW	8 GHz	600 pJ/bit
[76] [72] 2017, 2018	Perform data processing and control at 4 K to greatly relax readout requirements	FPGA: 228 mW idle + 21 μW per LUT LNA: 54.9 mW	NA	NA

[*] The only power dissipation considered is that of the cryogenic amplifier. The passive heat load of the bias and high speed microwave lines is not accounted for.
[†] Estimated from power consumption and bandwidth.

Table 1.4: Demonstrations of conventional cryogenic electrical readout. No experimental electrical readout demonstration is below 1 pJ/bit, even when disregarding the passive heat load of the DC and microwave electrical cables between the cryostat and room temperature. RSFQ = Rapid Single Flux Quantum. HEMT = High Electron Mobility Transistor. SNSPD = Superconducting Nanowire Single Photon Detector. JJ = Josephson Junction. LNA = Low Noise Amplifier. FPGA = Field Programmable Gate Array.

terconnects. Since cryogenic readout has a similar set of requirements, it is natural to ask ourselves if optical communications could address the limitations of current cryogenic readout architectures.

Figure 1-3(c) shows a schematic of an architecture to realize cryogenic optical readout. An input optical fiber carries multiple, continuous wave (CW) optical carriers generated by an ensemble of lasers operating at room temperature. An array of electro-optical devices, each associated with a different data stream generated by the cryogenic system and each tuned to a specific optical carrier wavelength, encodes the different electrical signals into the optical domain. The resulting modulated optical signals are read out to room temperature through a different optical fiber.

Compared to electrical readout, this architecture offers several advantages:

- Optical fiber has a 10,000-100x lower thermal conduction than typical electrical cables (Fig. 1-4), considerably reducing the heat load associated to adding data channels between the cryostat and room temperature. For instance, a 1 meter long optical fiber carries 7 μW of heat between 290 K and 4.2 K, and 0.8 μW between 80 K and 4.2 K (compared to 100 mW and 40 mW, respectively, for a copper SMA cable).

- Optical fiber has negligible signal losses at the length scales needed for cryogenic readout (typically 0.2-0.5 dB/km), which are also frequency independent. As a reference, the typical losses of commercial, high quality electrical cables at microwave frequencies are around 3 dB/m for a 40 GHz signal and 2.5 dB/m for a 26 GHz signal (Fig. 1-4(c)).

- The lower thermal conduction of optical fiber relaxes the requirements in thermal anchoring and isolation. This reduces the complexity of the system and

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results in shorter fiber lengths, which can significantly decrease the latency of the system.

- Optical fiber is robust to electronic interference and crosstalk, allowing for high signal fidelity in environments with a high density of readout lines.

- The possibility of exploiting Wavelength Division Multiplexing (WDM) allows the escape of multiple readout signals through the same physical fiber [77, 78] as depicted in Fig. 1-3(c). Thus, a much higher bandwidth density can be achieved in optical readout.

By exploiting optical fiber communications one can envision a low latency, low power, high throughput readout architecture requiring a minimal number of connections between the cryogenic and room temperature environments (Fig. 1-3(d)).

The use of optical communications for cryogenic readout was first proposed in the early 1960s [83], and since then several demonstrations of optical readout through the use of directly modulated laser diodes [79–81, 84] have been reported in the literature. The above mentioned demonstrations suffered either from a low escape bandwidth or from a high heat load due to the use of a driver to amplify and impedance match the signals generated by the cryogenic system (see Table 1.5). Thus, to the best of the author's knowledge, a scalable, low power, high speed cryogenic optical readout architecture is yet to be demonstrated. We will delve into the challenges for the realization of efficient optical readout in a later section.

An alternative to the use of directly modulated laser diodes is the use of optical modulators, an idea that has been proposed in the literature [85], but has not yet been experimentally demonstrated.

The use of optical modulators for cryogenic readout has several advantages when compared to directly modulated lasers. First, it allows for the laser to be operated

at ambient temperature, where control and feedback is easier. It is well known that lasers are more prone to failure than optical modulators, and having the laser at room temperature allows for easy replacement without the need to warm up the cryogenic environment. More importantly, the maximum bandwidth of directly modulated lasers depends strongly on its relaxation oscillation frequency, which increases as the operating current increases [86]. Thus, optical readout based on directly modulated lasers has a strong bandwidth-power tradeoff, increasing the heat load to the cryostat and limiting the maximum number of readout lines.

We have argued that the use of optical modulators could be advantageous for the realization of cryogenic optical readout, and outlined the advantages of integrated optics in general, and silicon photonics in particular. It is thus clear that realizing a

Optical readout demonstrations

Ref., Year	Brief description	Electrical Power [*]	Bandwidth	Energy per bit [†]
[79] [80] 1994, 1997	Directly modulated InGaAsP laser for RSFQ readout	400 μW at 4.2K	200 MHz	2 pJ/bit
[81] 1996	GaAs-AlGaAs VCSEL for cryogenic focal plane array readout	35 mW at 77K	2 GHz	17.5 pJ/bit
[82] 2019	Thermal switch to drive an LED for SNSPD readout	100 μW at 1K	100 MHz	1 pJ/bit

[*] Only electrical power is accounted for. Optical power consumption is not included.
[†] Estimated from power consumption and bandwidth.

Table 1.5: Demonstrations of cryogenic optical readout. No demonstration is below 1 pJ/bit, even when not accounting for optical power consumption. RSFQ = Rapid Single FLux Quantum. VCSEL = Vertical Cavity Surface Emitting Laser. SNSPD = Superconducting Nanowire Single Photon Detector.

high speed, low power cryogenic modulator in an integrated silicon photonic platform could solve the cryogenic readout problem. In the next section we will review the operating principle of silicon optical modulators and analyze in detail the challenges and performance metrics for cryogenic optical modulators.

1.4 Silicon photonic modulators for cryogenic optical readout

Optical modulators are, along with photodetectors, the main building block of any optical communication system. By modifying a physical property of the medium where the light propagates (the 'optical waveguide') due to an applied electric field, optical modulators are electro-optical devices that encode an electrical signal into an optical signal. High modulation bandwidth (a measure of the maximum data rate at which the modulator can operate), high optical bandwidth (the wavelength range at which the modulator works), high extinction ratio (the ratio between the output optical power of a '1' bit and a '0' bit), low optical loss and low power consumption are the desired characteristics of any optical modulator.

Optical modulators have been implemented in a variety of material platforms. Lithium Niobate (LiNbO$_3$, LN) has been the preferred option for decades [87], but the difficulties associated with its on-chip integration have generated a lot of interest in other alternatives. Silicon [88], InP [89], polymer [90], graphene [91] and plasmonic structures [92] have all been used to demonstrate high speed optical modulators, each with a different set of advantages and limitations.

Here, we will only discuss optical modulators in silicon, as they are the focus of this thesis. In the interest of brevity, a rapid overview of the physical phenomena
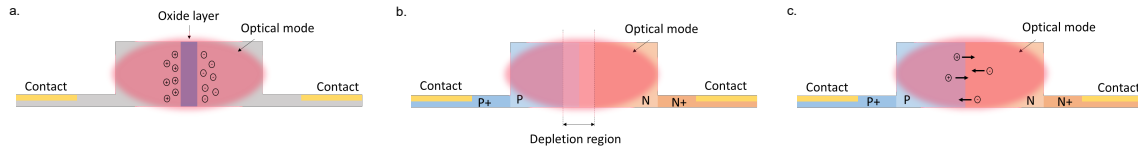
Figure 1-5: Inducing free carrier concentration changes in an optical waveguide. (a) Carrier accumulation through the use of a capacitive structure. (b) Depletion region width modulation in a reverse biased p-n junction. (c) Carrier injection into a forward biased p-n or p-i-n junction.

and device structures used in silicon modulators is to follow. The reader is pointed to references [88, 93–95] for a more in-depth discussion of these topics.

1.4.1 Silicon photonic modulators

Modulation mechanism

Typical electro-optic modulators exploit linear electro-optic effects (such as the Pockels, Kerr or Franz-Keldysh effects [7]), in which the application of an electric field generates a linearly proportional change in the real or imaginary part of the refractive index of the optical waveguide. Silicon is a centro-symmetric material and, as such, it does not exhibit these effects unless subject to a stress that breaks the lattice symmetry [96]. The use of the thermo-optic effect, in which a refractive index change is induced through a change in the temperature of the waveguide, is possible since silicon has a high thermooptic coefficient. Nevertheless, its limited speed prevents its use in applications requiring a bandwidth above a few MHz [97].

Alternatively, one can exploit the plasma dispersion effect, in which a change in the concentration of free carriers in the optical waveguide generates a change in its refractive index. Through this effect, efficient silicon modulators with bandwidths above 30 GHz have been realized [98, 99]. The plasma dispersion effect can be ex-

plained and approximated using the Drude model [7], but empirical expressions for the generated refractive index change at room temperature exist at 1550 nm and 1300 nm wavelengths, in what is commonly referred as the Soref's equations [100].

At 1550 nm wavelength:

$$\Delta n = -(8.8 \times 10^{-22} \times \Delta N_e + 8.5 \times 10^{-18} \times \Delta N_h^{0.8}) \tag{1.2}$$

$$\Delta \alpha = 8.5 \times 10^{-18} \times \Delta N_e + 6 \times 10^{-18} \times \Delta N_h \tag{1.3}$$

And at 1300 nm wavelength:

$$\Delta n = -(6.2 \times 10^{-22} \times \Delta N_e + 6 \times 10^{-18} \times \Delta N_h^{0.8}) \tag{1.4}$$

$$\Delta \alpha = 6 \times 10^{-18} \times \Delta N_e + 4 \times 10^{-18} \times \Delta N_h \tag{1.5}$$

Where Δn is the change in the refractive index, $\Delta \alpha$ is the change in the absorption coefficient in cm^{-1} and ΔN_e (ΔN_h) is the change in the density of free electrons (holes) in cm^{-3}. As an example, a change in the carrier density of 5×10^{17} cm^{-3} results in a change in refractive index $\Delta n = -1.66 \times 10^{-3}$ at 1550 nm and $\Delta n = -1.18 \times 10^{-3}$ at 1300 nm. It is worth mentioning that these relations are likely to be different at cryogenic temperatures due to changes in the material parameters of Si.

Different approaches can be used to generate the necessary changes in the free carrier density (ΔN_e and ΔN_h), which are schematically depicted in Fig. 1-5. Carrier accumulation (Fig. 1-5(a)) uses a capacitor structure and modifies the charge stored in it. Carrier depletion (Fig. 1-5(b)) uses a reversed biased p-n junction, and changes in the carrier density are achieved by modulating the width of the depletion region.

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Carrier injection (Fig. 1-5(c)) uses a forward biased p-n or p-i-n junction to control the amount of carriers injected into the optical waveguide.

Each operation mode features a different set of advantages and drawbacks. Carrier injection has the highest modulation efficiency (the change in refractive index per unit voltage applied), but has a high power consumption and a limited speed unless pre-emphasis driving signals are used [101]. Carrier accumulation has both good modulation efficiency and speed characteristics, but the need to include a capacitor-like structure in the optical waveguide makes its design and fabrication challenging [102]. Carrier depletion, while having a low modulation efficiency, has a very high speed and low power consumption [98], which makes it the preferred operation mode for silicon modulators.

Device structures

We have discussed how, through the plasma dispersion effect, we can achieve a change in the refractive index of the optical waveguide where the light propagates. A change in the real part of the index of refraction Δn generates a pure phase change in the light. While this is enough to achieve phase modulation, the preferred modulation format for short reach optical interconnects is On-Off keying (OOK) [1], in which the bits are encoded in the intensity of the light: a '1' is signaled by the presence of light and a '0' by the absence of it.

We thus need a device structure that can obtain intensity modulation from the phase change generated by the plasma dispersion effect. To do so, we can interfere two different light beams: when the two beams have a π phase difference, there is

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[1]The use of higher order modulation formats is possible [103], but its added complexity, signal processing requirements and extra power consumption make it unappealing for most short reach interconnects.
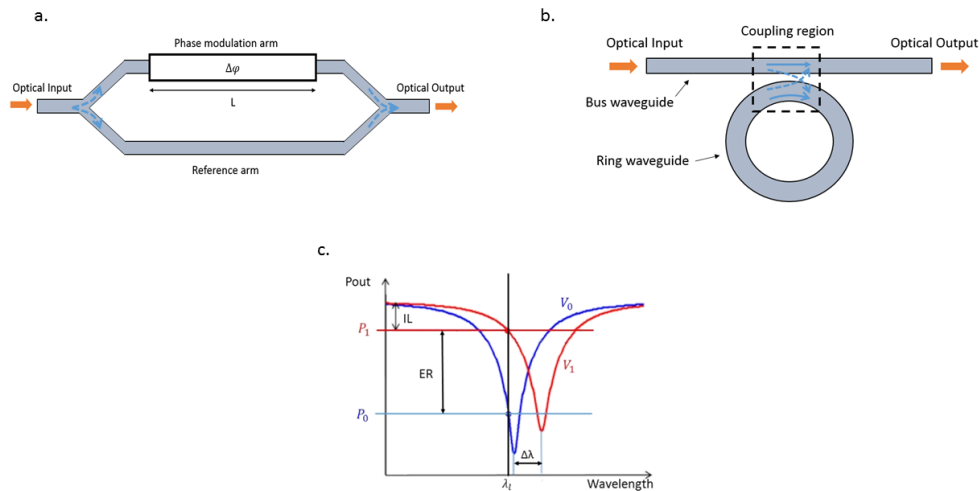
Figure 1-6: Integrated optical modulator configurations and working principle. (a) Mach Zehnder interferometer (MZI) structure. The incoming light is split in two branches. By controlling the phase difference between the two paths, constructive or destructive interference can be achieved. (b) Microring resonator (MRR) structure. By modifying the phase that the light acquires in a round trip through the ring, the resonance wavelength of the ring can be modified. (c) Modulation working principle. By generating a change in the resonance wavelength of the ring (in the MRR case) or a change in the phase difference between the two branches (in the MZI case) through an applied voltage, the transmission of the CW input light changes, achieving optical modulation.

destructive interference and no light is present at the output ('0' bit); when the two beams have a 2π phase difference, constructive interference occurs and there is light at the output ('1' bit).

The two main device configurations to achieve such beam interference in an integrated platform are show in Fig. 1-6. Figure 1-6(a) shows a Mach-Zehnder interferometer (MZI), where an incoming CW beam is split between two branches, and one of them is phase modulated through the plasma dispersion effect. Figure 1-6(b)

shows a microring resonator (MRR) configuration, in which the interference happens between the light propagating through the bus waveguide and the light coupled back from the ring waveguide. As depicted in Fig. 1-6(c), an applied voltage generates a refractive index change, which shifts the wavelengths at which there is destructive and constructive interference (in the MZI case) or the resonance wavelength of the resonator (in the MRR case). As a consequence, the transmission of a CW laser at a wavelength λ_l changes from P_0 to P_1 when the applied voltage is switched between V_0 and V_1. The relevant characteristics of a modulation format, mainly Insertion Loss (IL) and Extinction Ratio (ER), are also shown.

MZIs are highly linear, feature a higher optical bandwidth and are less sensitive to temperature and fabrication variations, but are large (in the order of mm) and require high voltages to achieve enough optical modulation. On the other hand, microring modulators have a much smaller footprint (tenths of μm diameter), lowering cost and, more importantly, requiring lower voltages to achieve modulation. Additionally, microring modulators function inherently as narrowband wavelength filters, which makes it possible to build WDM architectures without the need of a wavelength demultiplexer [78, 104]. It is for these reasons that microring modulators are seen as a more suitable choice for optical interconnect applications.

In this thesis we will exclusively deal with silicon photonic microring resonators. A deep understanding of microring resonator theory is not required, but the interested reader is pointed to references [105, 106] for a detailed theoretical study of the properties of general ring resonators. Reference [94] discusses ring resonators with a focus on modulator applications.

Cryogenic optical modulators

Ref., Year	Brief description	Physical effect for modulation	Integrated?	Packaged fiber?	DC Input impedance	Vpp	Electrical power [*]	Bandwidth	Energy per bit
[107] 2016	SiN resonant modulator	Thermo-optic	Yes	No	Low	NA	20 mW for 20 pm shift	Not reported	NA
[108] 2017	Si resonant modulator	Plasma dispersion	Yes	No	High (MΩ)	1.8V	NA	18GHz (4.3K)	45 fJ/bit
[109] 2019	$BaTiO_3$ Mach Zehnder and racetrack modulator	Pockels effect	Yes	No	High (MΩ)	1.7V	NA	18GHz (4.8K)	Estimated 40 fJ/bit[†]
[110] 2001	EuSe Mach Zehnder modulator (theoretical, not demonstrated)	Magneto-optical	-	-	Low	-	-	-	-
[111] 1994	Mach Zehnder $LiNb0_3$ modulator	Pockels effect	No	Yes	50 Ω	$V_\pi = 3V$	Not reported	Not reported	-
[112] 2019	SiN piezo-optomechanical ring modulator	Piezo-optomechanical	Yes	No	20 TΩ	8V	Not reported	200MHz	Estimated 650 fJ/bit[†]

Table 1.6: Demonstrations of cryogenic optical modulators reported in the literature. SiN = Silicon Nitride. $BaTiO_3$ = Barium Titanate. EuSe = Europium Selenide. $LiNb0_3$ = Lithium Niobate.

* Only electrical power is accounted for. Optical power consumption is not included.
† Estimated using a device input capacitance $C = 20$ fF.

1.4.2 Challenges and performance metrics for cryogenic optical modulators

We have mentioned earlier that, while advantageous when compared to directly modulated cryogenic lasers, the use of optical modulators operating at cryogenic temperatures to realize optical readout has never been experimentally demonstrated.

This is mainly due to the additional performance requirements that cryogenic readout applications pose. In this section we will analyze such requirements and describe the challenges associated with the cryogenic operation of silicon photonic modulators. We will also define a set of performance metrics for the use of optical modulators in efficient, high speed cryogenic readout based on the requirements we derived in Section 1.3.1.

Several optical modulators operating at cryogenic temperatures have been reported in the literature, covering a range of material platforms and device designs. Table 1.6 summarizes the main characteristics of these demonstrations. We will refer to it throughout the ensuing discussion.

Low temperature effects

Operation at cryogenic temperatures has important effects on material and device properties. These have been well characterized for silicon in the context of electrical devices (see for example [113]),and several models for CMOS devices have been proposed [114, 115]. Substantial work on the study of lasers at cryogenic temperatures exists [116, 117] but, to the best of the author's knowledge, the effects of low temperatures on the performance of optical modulators have not been extensively studied.

One of the effects that has a higher impact on silicon photonic modulators is

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carrier freezeout [118]. The lower thermal energy at cryogenic temperatures reduces the number of ionized dopants and thus the number of free carriers in the material. As a consequence, a large increase in device resistance and a decrease in junction capacitance is observed (see Appendix A for a theoretical discussion).

These impact the performance of an optical modulator in two different ways: (1) there is an increase in the RC time constant, which results in a lower bandwidth at cryogenic temperatures; and (2) there is a decrease in the capacitance density of the device, which lowers its modulation efficiency (lower junction capacitance means a lower change in free carrier density for the same applied voltage, and therefore lower refractive index change). This effect has been experimentally observed in silicon photonic modulators [108]: a bandwidth drop from more than 20 GHz at ambient temperature to 300 MHz at 4.8 K for a device with $1 \cdot 10^{18}$ cm^{-3} doping concentration was measured.

Techniques to eliminate carrier freezeout exist. Doping concentrations above a certain threshold allow for the dopants to generate an impurity band in which the carriers are free to move. Since this impurity band does not depend on the number of ionized carriers, but only on the distance between impurities, the semiconductor does not suffer from freezeout. This is know as the Mott metal insulator transition [119, 120]. As an example, the Mott transition happens for doping concentrations above $6 \cdot 10^{18}$ cm^{-3} for As-doped Si. This approach was used in [108] to increase the bandwidth a silicon resonant modulator at 4.8 K from 300 MHz for $1 \cdot 10^{18}$ cm^{-3} doping concentration to 4.5 GHz for $5 \cdot 10^{18}$ cm^{-3}. Another approach to unfreeze the carriers is to use field ionization: the application of a large enough electric field can free the impurities from their potential well either through tunneling or Poole-Frenkel ionization [118].

Carrier lifetime τ and mobility μ are other parameters that greatly affect the

performance of silicon modulators. Substantial work has been done to characterize these parameters at cryogenic temperatures, but its dependence on geometry, doping densities and material quality make the generalization of the results challenging. A decrease in carrier lifetime at cryogenic temperatures is expected due to (1) an increase in the defect capture cross section, which makes Shockley-Read-Hall (SRH) recombination faster [121] and (2) an increase in the radiative recombination rate [122]. Reference [123] studied the free carrier lifetime in undoped silicon resonators and measured a 20x decrease, from 1.9 ns at ambient temperature to a 100 ps below 10 K. A decrease in carrier lifetime is advantageous as it would increase modulator bandwidth (given a small enough RC time constant).

An increase in carrier mobility at cryogenic temperatures is expected due to the decrease in phonon scattering, which is the dominant mechanism at ambient temperature. For low doping concentrations, the dominant mechanism at cryogenic temperatures becomes neutral impurity scattering, whereas for higher dopings it is ionized impurity scattering [124, 125]. Figure 1-7(a) shows the carrier mobility in Si as a function of temperature for different doping concentrations.

The thermal properties of the device are also of the utmost importance for the correct operation of optical modulators. Since silicon has a high thermo-optic coefficient, temperature variations in the optical waveguide (due to optical absorption or free carrier absorption, for example) affect its index of refraction, which generate unwanted changes in the optical transmission through the modulator. Bulk thermal properties of silicon are well characterized, and reproduced in Fig. 1-7(b,c). A 5 orders of magnitude decrease in specific heat is observed, as well as a sharp decrease in the thermo-optic coefficient. This data suggests that operation at cryogenic temperatures could be beneficial to avoid unwanted thermo-optical modulation: to have the same refractive index change, a 1,000x larger temperature change is needed at

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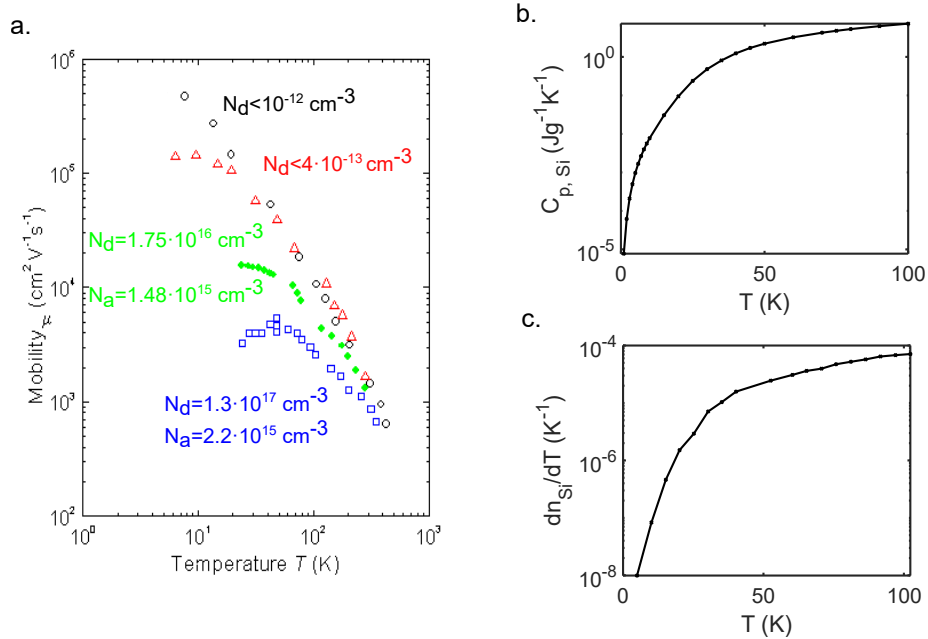
Figure 1-7: Temperature dependent properties of Si. (a) Carrier mobility for different doping concentrations [126]. (b) Specific heat [126]. (c) Thermo-optic coefficient [127].

4 K compared to 300 K. Nevertheless, larger temperature changes could occur at cryogenic temperatures due to the reduced specific heat.

In summary, most of the material properties dictating the performance of silicon photonic modulators change substantially when operated at cryogenic temperatures. Carrier freezeout is detrimental since it increases series resistance and decreases the RC bandwidth of the system. For systems limited by carrier lifetime, operation at cryogenic temperatures could be beneficial since a decrease in τ is expected. Finally, a sharp decrease in thermo-optic coefficient is accompanied by an even stronger decrease in heat capacity, which makes the prediction of the strength of thermal effects at low temperatures challenging.

Electrical signals in cryogenic environments

Cryogenic modulators need to function with the electrical driving signals generated by the cryogenic technologies we want to read out. Table 1.7 summarizes the typical signal levels and bandwidth requirements for the representative cryogenic technologies we discussed in Section 1.3.1.

While bandwidth requirements are lower or similar to those of room temperature modulators, cryogenic signal levels are in the order of mV, whereas driving signals for room temperature modulators are > 500 mV. This constitutes one of the main challenges for cryogenic modulators: to be suitable for cryogenic readout, they need to achieve modulation with 100x lower voltage signals. Clearly, the previous demonstrations of cryogenic modulators, which require > 1.5V (see Table 1.6), would not be able to function with such low voltages.

To compensate for the difference between the mV-level cryogenic signal and the V-level signal required by the modulator, demonstrations of optical readout rely on the use of an electrical amplifier. Nevertheless, the high power consumption of the cryogenic amplifier makes these demonstrations suffer from similar heat loads as conventional readout technologies.

An alternative approach yet to be demonstrated is the design of ultra-efficient modulators that are capable of achieving optical modulation directly with the mV

Typical signals generated by cryogenic technologies

Technology	Voltage level	Speed
SFQ	3-5 mV into 50 Ω load	20 - 40 Gbps
SNSPD	0.1-0.5 mV into 50 Ω load	< 1 GHz
Qubit readout	20-50 μV into 50 Ω load	4 - 8 GHz

Table 1.7: Typical requirements for signals generated by cryogenic technologies.

level signals generated by the cryogenic circuit.

It is of interest to derive an approximate expression for the minimum optical transmission change that a modulator should achieve for successful readout. While the definition of the figure of merit dictating what is "good enough" modulation could differ depending on the application, a natural choice is to use the bit error rate (BER) of the communication link established between the cryogenic and room temperature environments. In the case of OOK modulation, the bit error rate is defined as:

$$BER = \frac{1}{2}p(e|1) + \frac{1}{2}p(e|0) \qquad (1.6)$$

$p(e|1)$ $[p(e|0)]$ is the probability of error when a bit 1 [bit 0] is transmitted. We will use the definitions in Fig. 1-8(a). The optical power received for bit '1' is P_1, and the optical power for bit '0' is $P_0 = (1-t)P_1$. Here, t is the transmission change between the '1' and '0' bits. The current generated at the photodetector is given by $I_i = RP_i$, where R is the responsivity of the photodetector. Wit this, we can write:

$$p(e|1) = p(RP_1 + n < A) \qquad (1.7)$$

$$p(e|0) = p(R(1-t)P_1 + n > A) \qquad (1.8)$$

In the equations above, n is the noise present in the system and A is the decision threshold. A lower bound for the noise is the assumption of a shot noise limited system, which is equivalent to assuming that the thermal noise at the photodetector and receiving electronics is negligible. In this case, and making use of the central limit theorem, we can assume that the noise has a gaussian distribution with 0 mean

and variance $\sigma^2 = 2qRP\Delta f$ [128], with Δf being the bandwidth of the transmitted signal. It follows that:

$$p(e|1) = \frac{1}{2}\left[1 + erf\left(\frac{A - RP_1}{\sigma\sqrt{2}}\right)\right] = \frac{1}{2}\left[1 - erf\left(\frac{RP_1 - A}{\sigma\sqrt{2}}\right)\right] \quad (1.9)$$

$$p(e|0) = \frac{1}{2}\left[1 + erf\left(\frac{A - RP_0}{\sigma\sqrt{2}}\right)\right] = \frac{1}{2}\left[1 - erf\left(\frac{A - R(1-t)P_1}{\sigma\sqrt{2}}\right)\right] \quad (1.10)$$

It is left to find the optimal decision threshold A to minimize the error probability. Since the shot noise power is dependent on the power of the received bit, the optimal decision threshold will in general depend on the value of the transmission t. Nevertheless, for small values of t, we can approximate $\sigma_1 \approx \sigma_0$, and then the optimal threshold is just the average of the two currents $A = R(P_1 + P_0)/2$.

Putting all together, we arrive to the following expression (valid only for small values of t):

$$BER = \frac{1}{4}\left[2 - erf\left(\frac{t}{4}\sqrt{\frac{RP_1}{q\Delta f}}\right) - erf\left(\frac{t}{4}\sqrt{\frac{RP_1}{q(1-t)\Delta f}}\right)\right] \quad (1.11)$$

Clearly, the BER is dependent on the transmission change t, but also on the signal bandwidth Δf and the absolute power arriving at the photodetector. Figure 1-8(b) shows the BER as a function of the percentage transmission change for a 1 GHz bandwidth signal and several received powers P_1. If we set the threshold of acceptable BER to 10^{-9}, the minimum necessary transmission change varies from around 6.7% (equivalent to a 0.3 dB extinction ratio) for a received power of 10 μW to about 21% (1 dB ER) for 1 μW. In applications where Forward Error Correction (FEC) is possible (those with relaxed latency and complexity requirements), the

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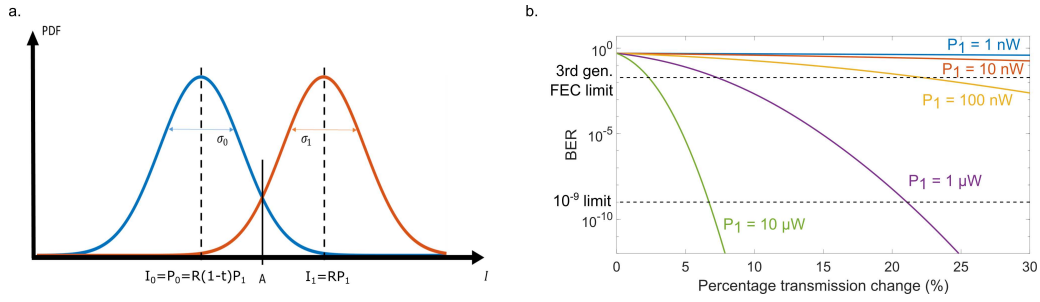
Figure 1-8: BER for a shot noise limited system. (a) Probabability density function (PDF) of the '1' and '0' bits assuming gaussian distribution. Bit '1' has an average current RP_1, while bit '0' has an average $R(1-t)P_1$. A, the optimal decision threshold between the '1' and '0' bits, is also shown. (b) BER as a function of the transmission change between the '1' and '0' bits (t) for a 1 GHz bandwidth signal. A responsivity R = 1 A/W is assumed.

minimum necessary transmission change is 2.3% (0.1 dB ER) for a 10 μW power and 22% (1 dB ER) for 100 nW, assuming 3rd generation FEC with 23% redundancy.

For a 10 GHz signal, the requirements increase to a 21% (66%) change or 1 dB (4.7 dB) ER for a 10 μW (1 μW) power and 10^{-9} BER. A 47% change (2.7 dB ER) is necessary at 50 GHz and 10 μW for a 10^{-9} BER, while very high extinction ratios > 20 dB are needed for a 1 μW signal.

It is important to note how these are lower bounds for the minimum necessary transmission change, since we have not considered the presence of thermal noise in the system.

In summary, the low voltage levels generated by the cryogenic circuits constitute a great challenge for cryogenic modulators. The development of ultra high efficiency optical modulators capable of achieving ER above 1 dB with mV-level driving voltages is thus essential.

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Impedance matching

The need to provide impedance matching between the cryogenic circuit and the modulator to avoid signal reflections and maximize power delivery is also challenging. Most cryogenic technologies are based on superconductors, therefore its output is typically a current signal delivered by a low output impedance stage. On the other hand, optical modulators are usually voltage driven and have very high input impedances in the order of $M\Omega$ or larger at DC frequencies (see Table 1.6), and are usually a few kΩ at GHz frequencies.

Clearly, the direct delivery of current signals from a low output impedance stage to a high input impedance stage is challenging, and an impedance matching technique is necessary to enable the cryogenic circuit to drive the optical modulator.

The most straightforward approach is the addition of a resistor R_{par} in parallel to the modulator, with a resistance low enough to be successfully driven by the cryogenic circuit (usually $R_{par} = 50$ Ω). While simple, this approach intrinsically limits the maximum driving voltage at the modulator to a value $R_{par}I_{cryo}$, where I_{cryo} is the output current generated by the cryogenic circuit. As shown in Table 1.7, these driving voltages are limited to < 5 mV, which are orders of magnitude smaller than typical modulator driving voltages. Another option is to use resonant matching networks, but these are usually narrowband and lossy at high frequencies. The use of impedance matching tapers to break the limit of $V_{mod} = R_{par}I_{cryo}$ while providing impedance matching has been reported [129], but at the cost of a significant decrease in the device speed (a 3x decrease in the maximum count rate of a superconducting detector was measured in [129]).

An alternative approach yet to be demonstrated is the use of current-driven optical modulators, which would allow for the direct delivery of signals from the

cryogenic circuits.

Heat load and power consumption

The strict power dissipation requirements in cryogenic environments are probably the biggest challenge for cryogenic modulators (and any other technology for cryogenic readout). Due to the Carnot efficiency limit, available cooling powers at the coldest temperature stages of a cryostat are usually very low [55], making the minimization of the overall power dissipation at these coldest temperature stages of the utmost importance.

Several heat sources exist in a cryogenic environment: heat conduction through the DC and RF cables coming from higher temperature stages, power dissipated in the cryogenic circuit itself and power dissipated by any other passive or active components needed for signal conditioning (such as filters, attenuators, amplifiers...) are the dominant heat sources.

As we have mentioned, optical readout eliminates the power dissipation associated with DC and RF electrical cables, and could potentially reduce the amplification requirements if efficient modulators can be realized. On the other hand, optical readout contributes to power dissipation in two ways: (1) The electrical power associated with the driving of the modulator; and (2) the optical power dissipation due to optical losses (through radiation, absorption, scattering...) in the modulator.

It is useful to find a figure of merit for the maximum power consumption (electrical + optical) for a cryogenic modulator (or any other cryogenic readout architecture) to be an attractive solution for cryogenic readout. The cooling powers of a representative, commercial dilution refrigerator used for quantum computing experiments are shown in Table 1.8. It is worth noting that higher cooling powers are available

Available cooling powers for a commercial dilution refrigerator

Stage Temperature	Cooling power	Cable length	$\mathbf{F}_{1.2K}$	$\mathbf{F}_{20mK}$
45 K	30 W	200 mm	110	70
4.2 K	1.5 W	290 mm	3,000	950
1.2 K	40 mW	250 mm	-	160
140 mK	200 μW	170 mm	-	180
20 mK	19 μW	140 mm	-	-

Table 1.8: Cooling powers for different temperature stages of a Bluefors XLD400 DR dilution refrigerator [130]. Coaxial cable lengths towards the specified stage are also shown. F_i = *cooling power/(heat load to i stage * attenuation to i stage)* is a figure of merit that quantifies the compromise between available cooling power and the cost associated with running an electrical signal from the specified stage to the ith stage. Attenuation is considered to be directly proportional to the necessary cable length to connect both stages. Operation at 4 K is optimal.

in commercial cryostats, but their cost is prohibitive [2].

We will consider that the optical modulator operates at the 4 K stage. This is a good compromise between the cooling power available at that stage and the heat load and electrical loss associated with connecting electrical cables to lower temperature stages. In fact, we can define a figure of merit to find the optimal operation stage:

$$
\begin{aligned}
F_i = \ &cooling\ power/(heat\ load\ to\ i\ stage\ *\ attenuation\ to\ i\ stage) \\
&\propto cooling\ power/(cable\ length\ to\ i\ stage)^2
\end{aligned}
\tag{1.12}
$$

As shown in Table 1.8, the 4 K stage is optimal.

1.5 W of cooling power are available at the 4 K stage. Of course, not all of it can be used for readout since there are other sources of power dissipation (memory, actual computation, signal conditioning...). Allocating 30% of the cooling power for readout

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[2]A refrigerator with 100 W of cooling power at the 4 K stage costs around $2 million, and one with 1 kW at 4 K around $6 million [34].

seems a safe assumption, which allows for a total power consumption of 450 mW. Of course, in a large cryogenic system multiple modulators would be operated in parallel, and the acceptable power consumption per device would depend on the number of readout channels. A more convenient metric to use instead of power consumption per device is the total energy consumed per bit of information read out. This way, our metric is independent of the number of modulators (or readout channels) needed: in terms of heat dissipation, it is the same to have a single modulator that can escape 50 Gbps with a 1 mW power dissipation than having 5 different modulators each operating at 10 Gbps and dissipating 0.2 mW - both consume an energy of 20 fJ/bit.

We need thus a bound for the necessary aggregate escape data rate out of a cryogenic circuit. Of all the applications we reviewed in Section 1.3.1, the most demanding in terms of escape data rate is SFQ high performance computing, which requires about 1 Tbps (1,000 Tbps) for a 1 PFLOP/s (1 EFLOP/s) supercomputing system. For a 450 mW total power allocated for readout, this allows for a maximum energy dissipation of 450 fJ/bit for a moderately demanding system, and 450 aJ/bit for future high performance systems. The bandwidth requirements for large SNSPD array readout are about 10x lower, resulting in an energy dissipation limit of 4.50 pJ/count. As a reminder, these energy consumption requirements include both electrical and optical power dissipation.

The requirements for quantum computing are probably best conveyed in terms of power dissipation per qubit. Since the data rate is low and readout is not performed continuously (usually, certain amount of time is allocated for logic operations, which are then followed by readout), energy consumption per bit is not a suitable performance metric. Assuming a mid-scale (large-scale) quantum system with a 1,000 (1 million) qubits, the power consumption per qubit should be < 0.45 mW ($< 0.45\ \mu$W) per qubit.

It is worth noting that even an ideal optical modulator with no insertion loss has an associated optical power consumption, since in the '0' state the input light is lost through scattering or absorption. This is shown in Fig. 1-9(b): not accounting for any electrical power consumption, an ideal optical modulator operating at 1 Gbps with 1 μW input optical power would dissipate 500 aJ/bit, which is already larger than the target power consumption for the 1 EFLOP/s HPC system. These losses are, nevertheless, not fundamental: by adding a second output port to the modulator (a 'drop' port in a ring configuration, and an additional port at the output 3 dB coupler in a Mach-Zehnder configuration) we could potentially recover the input light that is not used whenever a '0' is transmitted.

We can derive a lower bound for the minimum optical power consumption that is needed to achieve successful data communication based on the ER requirements we derived above. The optical energy per bit dissipated by a modulator is given by:

$$ E = \left(\frac{1}{2} E_1 + \frac{1}{2} E_0 \right) / f = \left(\frac{1}{2} P_{in}(1 - IL) + \frac{1}{2} P_{in}(1 - \frac{IL}{ER}) \right) / f \quad [J/bit] \quad (1.13) $$

Above, E_1 (E_0) is the energy per bit dissipated in the '1' ('0') bit. $ER = P_1/P_0$ is the extinction ratio and $IL = P_1/P_{in}$ is the insertion loss (Fig. 1-9(a)). f is the data rate at which the modulator is operating.

The optical energy dissipation for the minimum necessary ER to achieve successful data communication with a BER of 10^{-9} (calculated using Eq. 1.11) is shown in Fig. 1-9(c). For data rates above 10 MHz, the optical energy dissipation is below the limit for high performance systems. It is important to point out a few things: (1) Fig. 1-9(c) accounts only for optical power dissipation. (2) Fig. 1-9(c) assumes the minimum ER to achieve 10^{-9} BER in a shot noise limited system. Higher ER (and

61
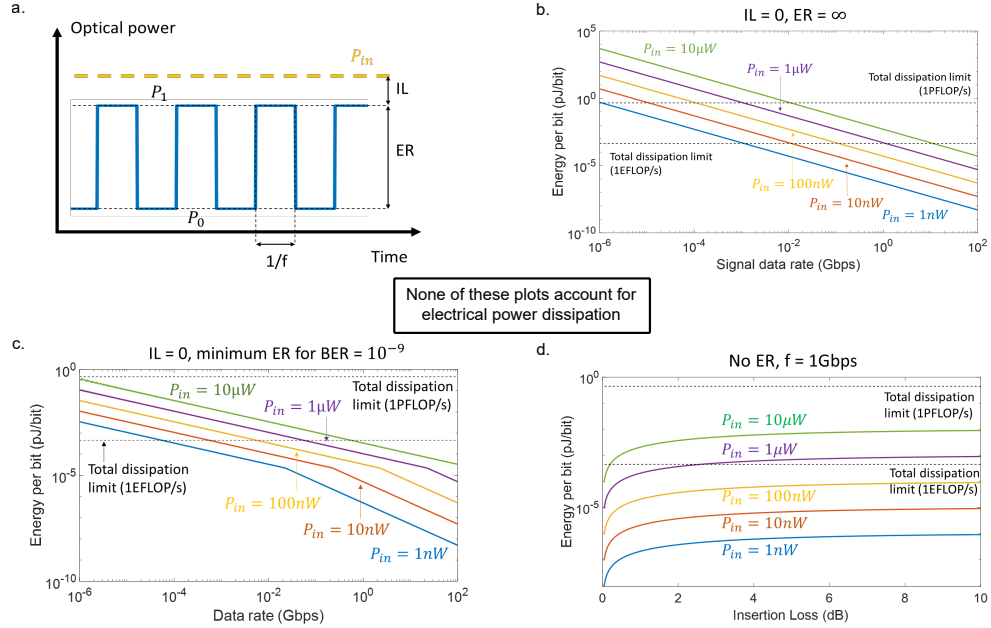
Figure 1-9: Optical energy dissipation in optical modulators. (a) Depiction of the relevant parameters of an optically modulated signal. (b) Optical energy dissipation in an ideal modulator (IL=0 and ER=∞) as a function of data rate for different input optical powers. Dashed lines show the readout power dissipation limits we derived. (c) Optical energy dissipation in a modulator with IL=0 and the minimum ER needed to achieve a BER of 10^{-9}, assuming a shot noise limited system. (d) Optical energy dissipation as a function of IL for different input optical powers. The energy cost of ER is not accounted for.

therefore higher power consumption) will be needed in a system with other noise sources. (3) Fig. 1-9(c) assumes no IL. The energy dissipation associated with finite IL is shown in Fig. 1-9(d) for a 1 Gbps signal. As can be seen, IL higher than 3 dB have a large associated energy dissipation.

In summary, the maximum energy that a cryogenic optical modulator can dissipate to be suitable for cryogenic readout is set by the (low) cooling power of the cryostat. Including both electrical and optical energy dissipation, we derived a 450 fJ/bit limit for moderately demanding systems, which decreases to 450 aJ/bit for

future high performance systems. To minimize optical power dissipation it is necessary to minimize input optical power and insertion loss, as well as to operate the modulator at the highest data rate possible.

Fiber packaging

An outstanding problem in the silicon photonics community is the need to provide a reliable and robust connection between the optical fibers carrying input and output light beams and the silicon chip, in what is commonly know as fiber packaging [131]. Fiber packaging is challenging because precise micro-meter precision alignment and attachment is needed, which usually requires active feedback. As a consequence, fiber packaging of integrated optics is expensive and time consuming, and constitutes a significant bottleneck to the wide commercialization of silicon photonic technologies.

The challenges of fiber packaging become worse in cryogenic applications due to the additional stress caused by the repeated thermal cycling associated with the cool down and warm up of the cryostat for setup modifications. As a consequence, most demonstrations of cryogenic modulators have been done in a cryogenic probe station with micromanipulated fiber probes, without the need of fiber packaging (see Table 1.6). While sufficient for device testing and proof-of-principle demonstrations, a high yield, robust cryogenic fiber packaging technique is absolutely necessary to make optical readout a viable solution to the cryogenic readout problem.

A few demonstrations of cryogenic fiber packaging have been reported in the literature [132]. In [133], patterned SU8 structures combined with a macroscopic support assembly were used to constrain the movement of the fiber. While successful, this approach requires extra processing steps and results in a bulky system, increasing costs and preventing its scalability. A packaging technique with very low loss tailored

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for single photon detectors has also been reported [134], but it is not applicable to other integrated optical chips. Finally, an approach based on the use of angle polished fibers glued to the chip surface has been recently reported [135]. While promising, the robustness and scalability of this technique is unclear.

Cryogenic optical readout won't reach wide adoption without a robust and scalable cryogenic fiber packaging technique. While several promising demonstrations have been reported, substantial work is yet to be done.

1.5 Summary

In this chapter we have reviewed how silicon photonics can provide compact, low power and high performance devices and systems in a scalable and low cost platform. We have argued how these make silicon photonics a promising solution for the cryogenic readout problem: cryogenic technologies need a means to communicate to ambient temperature, and current approaches based on electrical readout dissipate too much power to be suitable for future, large scale cryogenic systems (Table 1.4 and Fig. 1-10(a)).

We have introduced cryogenic optical readout and discussed how it can overcome many of the limitations of electrical readout, but we have also shown that previous demonstrations suffer from the same large power dissipation problem (Table 1.5 and Fig. 1-10(a)).

In this sense, we have reviewed the outstanding challenges for cryogenic optical modulators and derived several requirements that a cryogenic modulator should fulfil to make optical readout a viable solution. We have discussed how operation at low temperatures profoundly impacts material and device properties. We have also described the need for highly efficient modulators capable of **working with** $<$

a.

b.

* Heat load of bias and high speed microwave lines not accounted for.

+ Optical power dissipation not accounted for.
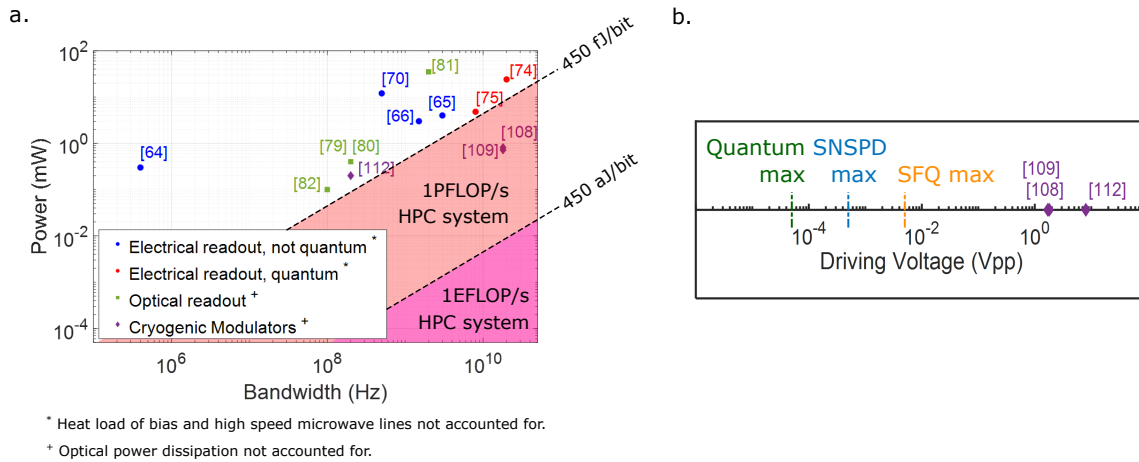
Figure 1-10: The cryogenic readout problem. (a) Bandwidth and electrical power consumption of previous demonstrations of cryogenic readout. Blue circles show electrical readout demonstrations for non-quantum technologies and red circles show electrical readout of quantum technologies. Green squares depict previous demonstrations of optical readout and purple diamonds previously reported cryogenic modulators. The shaded areas show the requirements for 1 PFLOP/s (red) and 1 EFLOP/s (violet) high performance computing systems as derived in the text. Most readout architectures reported to date, both optical and electrical, are far from meeting the requirements. (b) Peak to peak voltages for cryogenic modulator demonstrations along with the output voltages generated by representative cryogenic technologies. A more than 2 orders of magnitude decrease in driving voltage is needed for these modulators to be suitable for cryogenic readout.

5 mV electrical signal levels and generating > 1 dB ER, as well as the need to provide an impedance matching mechanism to make delivery of the signals from the cryogenic circuit possible. We have discussed the stringent limitations in energy dissipation inside a cryostat, and concluded that the modulator needs to dissipate, including both electrical and optical energy, < **450 fJ/bit for a moderately demanding system, and 450 aJ/bit for future high performance systems**. While cryogenic modulators with electrical power consumption and bandwidth compatible with such requirements have been reported in the literature (Fig. 1-10(a)),

its direct application to cryogenic readout is challenging due to the need for voltage levels more than 1,000x larger than those generated by the cryogenic system (Fig. 1-10(b)).

The purpose of this thesis is to propose, analyze, characterize and test silicon photonic modulators capable of fulfilling the requirements to make optical readout a scalable, low power, high speed solution for the cryogenic readout problem.

1.6   Thesis outline

The rest of this thesis is organized in 5 chapters, each describing a self-contained project with a specific set of goals.

- Chapter 2 deals with the characterization of silicon photonic resonant modulators at 4 K. We evaluate the feasibility of using silicon photonic devices in cryogenic environments, and propose device designs and operation modes specifically tailored for low temperature operation.

- Chapter 3 discusses the experimental demonstration of cryogenic optical readout of a Superconducting Nanowire Single Photon Detector (SNSPD). This work constitutes the first demonstration of the use of an optical modulator to realize cryogenic optical readout, and could open up a new application space for silicon photonics.

- Chapter 4 proposes and characterizes a new operational mode for resonant optical modulators based on the photovoltaic effect. By exploiting the optical absorption occurring in resonant modulators, modulation with ultra low electrical power consumption in the zJ/bit regime is achieved.

- Chapter 5 analyzes, both theoretically and experimentally, the effect of non-linearities due to high input optical powers on the operation and performance of silicon resonant modulators. This work will help set boundaries to the maximum optical power that a silicon photonic transmitter can output, which can be used in link design and planning.

Chapter 2

Cryogenic Operation of Silicon Photonic Modulators

The first step towards realizing cryogenic optical readout is to analyze the performance of standalone silicon photonic modulators at cryogenic temperatures, which is the purpose of this chapter.

This will help us identify the main physical processes affecting the performance of silicon photonic modulators when operated at cryogenic temperatures, and propose design and operation techniques targeting the unique characteristics of cryogenic operation.

2.1   Device designs

As discussed in Chapter 1, in this thesis we will exclusively deal with silicon photonic resonant modulators due to their compactness, ability to act as wavelength demultiplexers and, most importantly, their lower power dissipation compared to Mach

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Zehnder modulators.

We will study 2 different device geometries, which are shown in Fig. 2-1:

1. Design C is a resonant modulator designed for operation on the C band ($\approx$ 1550 nm operating wavelength). Both the design and room temperature performance of this device have been reported in [136], showing a 14 GHz bandwidth and a modulation efficiency of 20 pm/V in reverse bias. We will characterize the performance of this exact same modulator at cryogenic temperatures.

2. Design O is a resonant modulator designed for the O band ($\approx$ 1270 nm operating wavelength). The main difference with design C, besides its smaller size, is the addition of a 300 nm wide silicon germanium (SiGe) band to increase absorption and carrier recombination (for reasons that will be discussed later). Also, this design has 3 variants, each with different doping implants:

   - Variant C-Z (where Z stands for *zero-change*) uses the same doping implants as design C, which are the standard implants used for the realization of transistors.

   - Variant C-B (where B stands for *balanced*) uses doping implants with a better balance between p and n doping.

   - Variant C-H (where H stands for *high-doping*) uses doping implants with 2x higher impurity concentration compared to variant 1.

The ring modulators are realized in the crystalline silicon layer that is used to make the standard transistors offered in the CMOS process, which is a commercial microelectronics Silicon on Insulator (SOI) process offered by GlobalFoundries (45RF SOI). The silicon thickness is less than 100 nm, and the buried oxide (BOX) is about
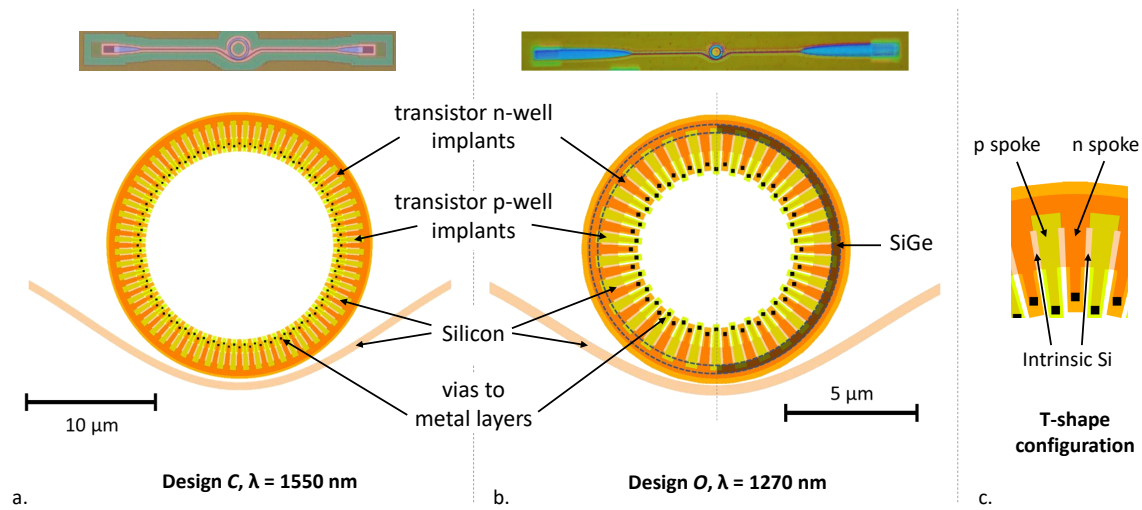
Figure 2-1: Cryogenic ring resonant modulator designs. (a) Design for 1550 nm operating wavelength. The ring has a 20 μm outer diameter and is 1.7 μm wide. A micrograph of the device is shown on top. (b) Design for 1270 nm operating wavelength. The ring has a 10 μm outer diameter and is 1.2 μm wide. A 300 nm wide SiGe band is present in this device. A micrograph of the device is shown on top. (c) Closeup showing the T-shape configuration of the interleaved p-n junctions.

200 nm thick. To avoid leaking of the optical mode into the silicon substrate, a post-processing step where the silicon substrate is removed using a xenon difluoride (XeF$_2$) etch is performed. The interested reader is pointed to references [27, 137] for more information on the fabrication process.

2.1.1 Device geometry

The modulator designs characterized here are based on spoked ring resonators with whispering gallery modes (WGM). By concentrating the optical mode at the outer side of the ring, metal contacts at the inner side can be added to provide electrical access and not incur in substantial optical losses (Fig. 2-1). Waveguide widths and bend radius are optimized for the specific operating wavelength to minimize radiation

and sidewall scattering losses, and the gap between the ring and the bus waveguide is adjusted to achieve critical coupling [137, 138].

Active control of the free carrier density is achieved through interleaved p-n junctions, which are made using standard doping layers normally used to realize the source and drain of the transistors in the CMOS process. The SiGe implant in design O (Fig. 2-1(b)) is also a standard layer in such processes, as it is used to strain the channel of p-FETs to improve transistor speed.

The p-n junctions in the ring are layed out in a T-shaped configuration (Fig. 2-1(c)). This configuration is optimized to provide high capacitance density, and thus high modulation efficiency, in the region where the optical mode is concentrated. At the same time, it minimizes the parasitic capacitance in the access regions (where there is no optical mode) to reduce the RC time constant and increase device bandwidth. Detailed information on the geometry optimization for these devices can be found in [139, 140].

Optical coupling into and out of the chip is achieved through the use of vertical grating couplers (visible in the micrographs in Fig. 2-1). These are structures which, by introducing periodic perturbations into the optical waveguide, produce scattered light which constructively interferes at a specific angle [138, 141].

2.2   Cryogenic probe station

All the experimental results presented in this chapter were taken in a Lakeshore (formerly Desert Cryogenics) TTP4-1.5K cryogenic probe station (Fig. 2-2). This is a Helium flow system with high cooling power and a base temperature of 4.2 K.

Optical coupling in and out of the chip is achieved through micromanipulated probe arms holding an optical fiber (Fig. 2-2(b,c)). The position of the optical fibers

can be controlled with 100 nm resolution in x, y and z, which is enough to achieve good optical coupling to the grating couplers in the CMOS chip. The angle at which the fiber is held with respect to the stage can also be precisely controlled by means of a custom-made fiber holder (shown in Fig. 2-2(c)).

Electrical access is achieved through the use of another micromanipulated arm holding a microwave probe with two contacts (ground and signal), as shown in Fig. 2-2(c). Electrical losses below 1.7 dB are achieved for frequencies up to 40 GHz, enabling high speed testing of our devices.

A large working distance microscope allows for the visualization and alignment of the devices and optical and electrical probes. As shown in Fig. 2-2(a), a variety of optical (lasers, power meters, photodetectors...) and electrical (oscilloscopes, vector network analyzers...) instrumentation is used to characterize the different devices.

2.3   DC characterization

The first step to evaluate the suitability of our modulators for cryogenic readout is to characterize its DC performance at low temperatures. This will allow us to confirm that the devices still function at such temperatures and will help us identify the main effects that low temperature operation has on our devices.

2.3.1   Electrical characterization - IV curves and differential resistance

A large amount of information about the dominant physical current transport processes occurring in a device can be obtained from its IV characteristics. Since from an electrical point of view our device is a simple p-n junction diode, we expect it to

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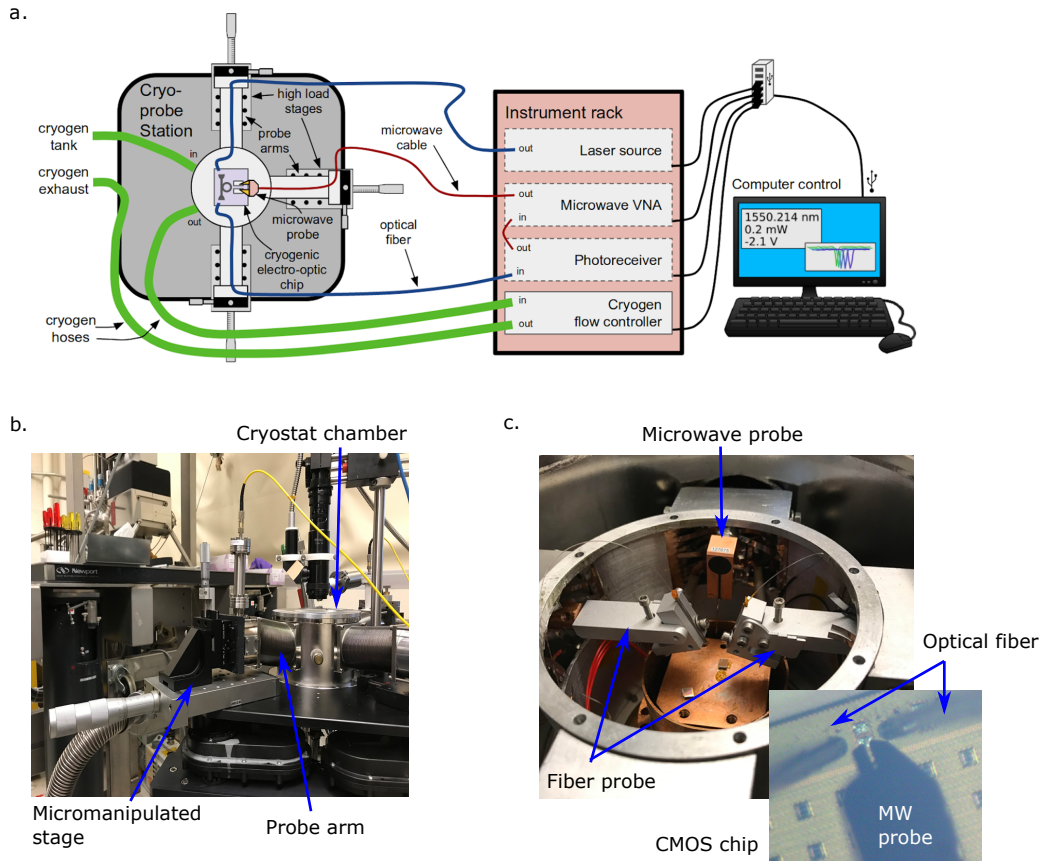
Figure 2-2: Probe station for cryogenic testing. (a) Schematic of the cryogenic testing system. The cryogenic probe station allows for optical and electrical access to the device under test through micromanipulated probe arms, and a variety of optical and electrical instrumentation is used to characterize the device. Image courtesy of Dodd J. Gray. (b) Probe arm closeup. 3 axis micromanipulated stages allow for alignment of the optical fibers and microwave probe with 100 nm resolution. (c) Cryostat chamber closeup. The two optical fiber probes, as well as the microwave probe, are visible. The inset shows a microscope image of the two fibers and the microwave probe aligned for testing of a device.
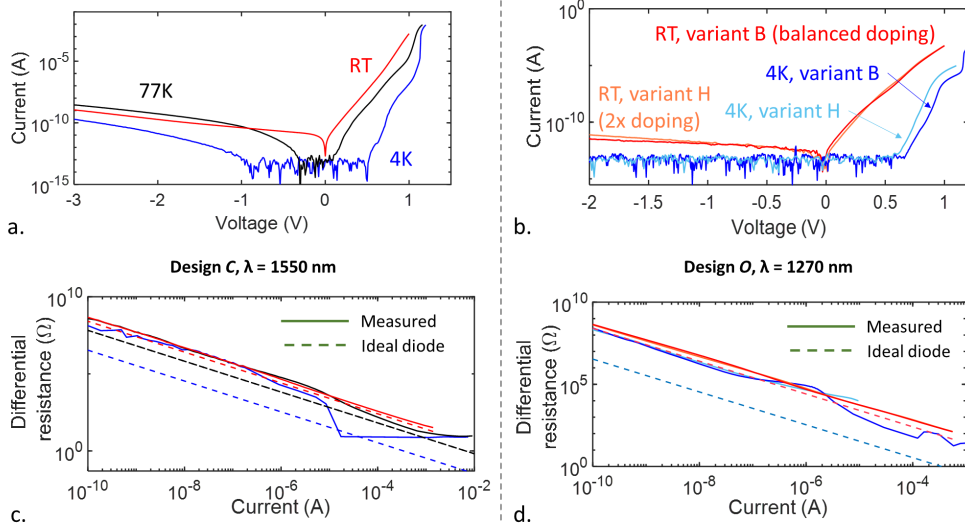
Figure 2-3: DC electrical characterization of modulators at ambient and cryogenic temperatures. (a) IV curves for design C - the modulator for 1550 nm. (b) IV curves for design O - the modulator for 1270 nm. Two of the design variants are shown. (c) Differential resistance for design C. The curves follow the same coloring as (a). (d) Differential resistance for design O. The curves follow the same coloring as (b). In (c) and (d), solid lines show measured values, and dashed lines the value for an ideal diode at the same temperature. While at room temperature the behavior of the devices approaches that of an ideal diode, operation at cryogenic temperatures shows large deviations from the characteristic diode curve.

show the characteristic rectifying characteristic [142]:

$$I = I_s \left(e^{q\frac{V - IR_s}{nkT}} - 1 \right) \tag{2.1}$$

Above, I is the current flowing through the modulator when a voltage V is applied. I_s is the reverse saturation current of the diode, which depends on several material and design parameters. R_s is the series resistance of the diode, and n is the ideality factor, which accounts for non idealities in the diode behavior.

Figure 2-3(a,b) show the IV characteristics of our designs at several temperatures.

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Even at 4 K all the modulators show a rectifying IV curve, which indicates that our devices are still electrically operational at cryogenic temperatures.

Nonetheless, it is clear by looking at Fig. 2-3 that the electrical behavior of the devices changes substantially as temperature decreases. The first visible change is on the turn-on voltage of the device, which increases as temperature goes down for all the designs. This is due to an increase in the junction built-in voltage caused by the Fermi levels in the p and n regions getting closer to the conduction and valence band edges (see Appendix A.1 for a comparison between the increase predicted by the theory and the measured values).

Another noticeable effect is the decrease in the current in reverse bias (V<0) as temperature decreases, which indicates a reduction in the reverse saturation current I_s. This is a direct result of the increase in the built-in voltage of the junction: since saturation current is due to minority carrier diffusion through the junction, the number of carriers with enough energy to overcome such barrier depends exponentially on its height. In see Appendix A.2 we calculate the decrease in I_s predicted by theory and compare it to the experimental values.

It is also apparent that, at low temperatures and forward bias ($V > 0$), the IV curve deviates considerably from the typical diode behavior. Several regimes can be identified for different applied voltage ranges, each with a characteristic slope. This is better visualized by plotting the differential resistance of the diodes, $r_d = dV/dI$. The differential resistance is a measure of how big of a voltage change is needed to achieve a given change in the current flowing through the diode. r_d is one of the basic parameters for the modeling of a diode in the small signal regime, and, as we will analyze in detail in a later section, directly determines the strength of optical modulation achievable in a forward biased modulator.

The measured differential resistance extracted from the IV curves is shown for

our devices in Fig. 2-3(c,d). The same plots also show the differential resistance for an ideal diode at a temperature T in dashed lines, which is given by the expression $r_d = dV/dI = kT/qI$, where I is the current flowing though the diode and we assume $R_s = 0$ and $n = 1$ (see Eq. 2.1). While at room temperature the differential resistance follows closely that of an ideal diode, large deviations are observed at low temperatures.

The study of the IV characteristics of diodes at cryogenic temperatures was an active field about 30 years ago, but not much work has been done since then. This makes it hard to compare our results with previously reported data, since device behavior is largely affected by material and fabrication quality and, without much room for debate, such quality is higher nowadays. Nevertheless, we will attempt to propose and discuss the main physical processes that cause the deviations from typical diode behavior we have observed. A detailed study of these processes does not exist in the literature (to the best of the author's knowledge) and, while much needed, is not the focus of this thesis [1].

We can qualitatively describe both the IV curve and the differential resistance at room temperature and cryogenic temperatures as sketched in Fig. 2-4. At ambient temperature, the IV curve follows closely that of an ideal diode (with an ideality factor n not necessarily equal to 1), until at high forward currents the series resistance R_s limits how fast the current can rise. Consequently, the dynamic resistance at low forward currents is given by $r_d = kT/nqI$, and it saturates at a value $r_d = R_s$ at high forward bias. From our experimental curves, both designs C and O have $R_s < 100 \ \Omega$ and n $\approx$ 2 at room temperature.

At cryogenic temperatures, the IV curve shows an increase in the current at low

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[1]If the reader is a PhD student interested in device modeling and simulation, he/she is encouraged to work on it. If the reader is a professor, consider hiring a PhD student to do so.

forward bias (label "1" in Fig. 2-4), followed by a "shoulder" where the current rises very slowly (label "2" in Fig. 2-4). For increased forward biases, a very steep increase in current follows (label "3" in Fig. 2-4), until the current becomes limited again by the series resistance R_s (label "4" in Fig. 2-4).

Such behavior has been observed previously in p-n junction at low temperatures [143–146], and is usually explained by electric field assisted effects. At low currents (low forward bias voltages), trap-assisted tunneling dominates the current, which shows large characteristic ideality factors in the order of $n \approx 10 - 20$ [147] (label "1" in Fig. 2-4). Trap assisted tunneling can only occur for a given electric field range (which is set by the trap energy and material parameters [145]), so at higher forward voltages the growth in current is greatly diminished (label "2" in Fig. 2-4). At sufficiently high forward bias, the electric field in the quasi neutral regions is high enough for field assisted impact ionization to take place, causing a steep rise in current (label "3" in Fig. 2-4). Finally, voltage levels close to the junction built-in voltage lower the potential barrier enough for carrier injection (which is the dominant transport process in forward bias diodes at room temperature) to take place. At such high currents, the IV curve is limited by the diode series resistance R_s (label "4" in Fig. 2-4).

Another plausible explanation for the IV curve evolution at cryogenic temperatures accounts for the effects of temperature fluctuations arising from ohmic heating for moderate currents flowing through the device [144, 148]. The increase in the junction temperature is accompanied by a change in carrier density and mobility, which generates changes in the IV curve of the device and can also generate large dynamic oscillations when the device is current driven [149].

Most likely, an accurate explanation of the IV characteristics of p-n junctions at cryogenic temperatures involves both field-assisted and heating effects. To the best of

RT

① IV curve follows closely diode characteristic: $I = I_s * e^{qV/nkT}$ $\quad r_d = \frac{kT}{nqI}$

② IV limited by series resistance: $I = I_s * e^{qV-IR_s/nkT}$ $\quad r_d = R_s$

Cryo T

① Current due to trap assisted tunneling. $\quad r_d = \frac{kT}{nqI}$ $\quad$ n ≈ 10-20

② Trap assisted tunneling suppressed. Very slow rise in current, r_d high.

③ Field assisted impact ionization in quasi-neutral regions. Steep rise in current.

④ Carrier injection with IV limited by series resistance. $\quad r_d = R_s$

Figure 2-4: Qualitative description of the main physical processes affecting the diode IV characteristics at ambient temperature (red) and cryogenic temperatures (blue).

the author's knowledge, no work accounting for both phenomena has been reported in the literature. Independent of the underlying physical mechanism, it is worth noting that achievable dynamic resistances at cryogenic technologies are always at least an order of magnitude larger than one would expect for an ideal diode. This is because at moderate voltages the increase in current is NOT due to carrier injection (as is the case at room temperature), but instead it is due either to tunneling and recombination or to heating effects, which show large ideality factors ($n > 10$).

Summarizing, we have confirmed that our devices do not suffer fatal effects when cooled down to cryogenic temperatures: the characteristic rectifying behavior of p-n junctions is observed for all devices at temperatures down to 4 K, which suggest that our modulators will be functional at cryogenic temperatures. Nevertheless, we observe large deviations from a conventional diode behavior at low temperatures, likely due to both field assisted and heating effects.

2.3.2 Optical characterization - Q factor and ER

In the previous section we have electrically characterized our devices at low temperatures, but we also need to characterize its optical behavior to confirm that the optical resonance of our modulators is not negatively affected when cooled down to cryogenic temperatures.

The results we obtained are summarized in Fig. 2-5. Figure 2-5(a,b) show transmission spectra for the different designs, both at room temperature and 4 K. Clearly, all devices maintain their characteristic resonant behavior. This is expected, since the existence of an optical resonance in our ring structures is guaranteed as long as the waveguides are capable of guiding light. The existence of a relatively sharp optical resonance indicates then that the device is not destroyed at cryogenic temperatures: the thin silicon layer where the waveguides are realized does not crack due to thermal stress or any other effect.

We did nevertheless observe a significant change in the resonance wavelength λ_0 of all the devices (Fig. 2-5(c)): it blue-shifted around 12 nm for design C and 9 nm for all variants of design O when cooled down to 4 K. This is expected, since silicon shows a strong thermo-optic effect - the change in refractive index with temperature (see Fig. 1-7). The thermo-optic coefficient dn/dT in Si is positive for all temperatures, and thus a decrease in temperature is accompanied by a decrease in the refractive index of the optical waveguides. Since $\lambda_0 \propto n_{eff}L$ (where L is the ring length), a decrease in the refractive index generates a blue shift in the resonance wavelength [135]. The differences in the magnitude of the resonance shift between design C and O are due to the different operating wavelengths and effective indexes. Good agreement between the measured resonance shift and that predicted by theory is found (see Appendix A.4).
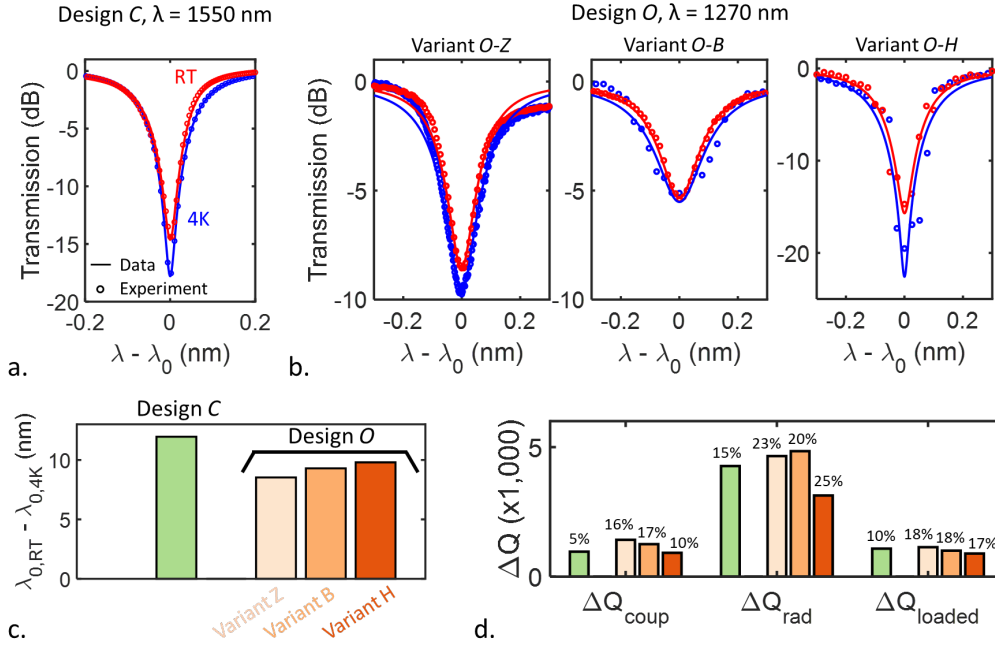
Figure 2-5: Characterization of the optical resonance at room temperature (red) and 4 K (blue) for the different device designs and variants. (a) Resonance for design C - the modulator for 1550 nm - at 4K and room temperature. (b) Resonance for the 3 variants of design O - the modulator for 1270 nm with SiGe - at 4K and room temperature. (c) Change in resonance wavelength when cooling down to 4 K. A decrease in resonance wavelength is measured. (d) Change in the resonance quality factors ($Q_{RT} - Q_{4K}$) when cooling down to 4 K. The percentage change ($\Delta Q/Q_{RT}$) is also shown. Changes lower than 20% are observed for all designs.

It is also interesting to analyze how the resonance shape changes with temperature. Resonance width is usually quantified though the quality factor Q, which is related to the number of round trips made by the energy in the ring before being lost, either due to internal loss mechanisms (such as radiation or absorption) or due to the coupling from the ring to the output bus waveguide [106]. The quality factor can be experimentally obtained using the relation $Q = \lambda_0/\Delta\lambda_{3dB}$, where $\Delta\lambda_{3dB}$ is the full width half maximum of the resonance. Since in our ring modulator there

are two sources of losses, the total Q factor of the resonance, usually called loaded Q (Q_{loaded}), is the inverse sum of the Q factors associated with each loss mechanism: $Q_{loaded}^{-1} = Q_{coup}^{-1} + Q_{rad}^{-1}$. Q_{coup} is associated with the optical loss due to the coupling of light from the ring to the output bus waveguide, and Q_{rad} with the internal loss mechanisms in the ring, which are mainly radiation, scattering and absorption. The optical transmission through the ring has a Lorentzian shape, and is given by [105]:

$$T = \frac{\left(1 - \frac{\lambda_0}{\lambda_l}\right)^2 + \frac{1}{4Q_{coup}^2} + \frac{1}{4Q_{rad}^2} - \frac{1}{2Q_{coup}Q_{rad}}}{\left(1 - \frac{\lambda_0}{\lambda_l}\right)^2 + \frac{1}{4Q_{coup}^2} + \frac{1}{4Q_{rad}^2} + \frac{1}{2Q_{coup}Q_{rad}}} \tag{2.2}$$

Above, λ_0 is the resonance wavelength of the ring and λ_l is the laser wavelength. When $Q_{coup} = Q_{rad}$, the ring is said to be in the critical coupling condition, and the transmission is $T = 0$ on resonance ($\lambda_l = \lambda_0$).

We fit the experimental transmission spectra for the different devices (shown in Fig. 2-5(a,b)) to Eq. 2.2, and the results are summarized in Table 2.1 and Fig. 2-5(d). Some interesting observations should be noted:

- The Q factor for design C is close to 2x higher that that of design O both at room temperature and 4 K. This is expected, since design O incorporates the SiGe band, which adds optical absorption and reduces the Q factor.

- No significant change in the resonance Q factors ($< 20\%$ for all the devices) is observed when cooling the devices down to 4 K. This is surprising, since we would expect an increase in the internal Q factor of the ring Q_{rad} at cryogenic temperatures due to decreased free carrier losses caused by freezeout. Two plausible arguments exist to explain the observed behavior:

  1. Free carrier absorption is not the main loss mechanism in our resonant

structures, even at room temperature. We do not expect scattering or defect absorption to depend strongly on temperature, so if these are the dominant loss mechanisms we would not expect a large change in Q factor as we cool the devices.

Nevertheless, the data at room temperature seems to contradict this argument: we observe significant changes in the internal Q factor of the different variants of design O which are correlated with doping density: the higher doped O-H variant has a lower Q factor than the lower doped variants (Table 2.1), which is a strong indicator of free-carrier absorption dominating internal loss in the ring.

2. A change in the main internal loss mechanism occurs as we cool the devices: from free carrier absorption at room temperature to photo-excitation of the frozen impurities at 4 K. In other words, at 4 K the main optical loss mechanism is the absorption of photons to excite the impurity electrons and holes from their impurity energy to the conduction and valence band edges. Notice how in this case we would expect higher doped devices to show lower internal Q factors, since the larger impurity density would translate into larger optical absorption. This is indeed what we observed for our devices: we can see how at 4 K the higher doped O-H variant also shows a lower internal Q factor compared to lighter doped variants O-Z and O-B (Table 2.1). Such behavior has been previously reported in silicon with varying impurity concentration [150–152].

Our observations are also in agreement with the results reported in [108] for a similar silicon resonant modulator as ours. There, a 5% increase in the Q factor of the resonator was observed at 4 K.

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Design	Q_{loaded}, RT	Q_{coup}, RT	Q_{rad}, RT	Q_{loaded}, 4 K	Q_{coup}, 4 K	Q_{rad}, 4 K
Design C	11,353	19,191	27,796	10,270	18,227	23,528
Design O **Variant** Z	6,205	9,041	19,788	5,068	7,619	15,134
Design O **Variant** B	5,602	7,288	24,219	4,599	6,031	19,376
Design O **Variant** H	5,170	8,884	12,370	4,275	7,960	9,236

Table 2.1: Extracted quality factors for the different device designs at room temperature and 4 K.

Summarizing, we have shown how our devices are still optically operational at cryogenic temperatures, and how temperature does not seem to have much influence on the optical properties beyond a blue shift in the resonance wavelength due to the change in refractive index.

2.3.3 Electro-optical characterization - Modulation efficiency

Now that we have confirmed that our devices are optically and electrically operational at cryogenic temperatures, it is time to characterize their electro-optical properties. We will do this by measuring the modulation efficiency of the modulators. Modulation efficiency is a measure of how much shift in resonance wavelength is achieved per differential of voltage applied:

$$\text{Modulation efficiency [pm/V]} = \frac{\Delta \lambda_0}{\Delta V} \tag{2.3}$$

As indicated, it is usually measured in pm/V. Clearly, we want our modulators to have as large a modulation efficiency as possible, since this means that a small applied voltage generates a large change in resonance wavelength, and thus a large

change in the optical transmission though the device and a large ER modulation.

Fig. 2-6 shows the results for design C (the modulator for 1550 nm operating wavelength). The other designs show similar characteristics, so the curves are not reproduced here. Fig 2-6(a) shows transmission spectra at different bias voltages at ambient temperature (top) and 4 K (bottom). The evolution is as expected: an increase in the bias voltage blue shifts the resonance of the device due to the increase in carrier density, which through the plasma dispersion effect (Eqs. 1.2, 1.3) decreases the refractive index of the Si waveguide. Note how for strong forward bias the resonance becomes wider. This is due to an increase in free carrier absorption caused by the injection of carriers, which decreases the internal quality factor Q_{rad}.

Fig. 2-6(b) shows the evolution of the resonance wavelength with applied voltage, and Fig. 2-6(c) shows the corresponding modulation efficiency, which is obtained by taking the derivative of the data in Fig. 2-6(b). We can see how in reverse bias (V < 0) the change in resonance wavelength is almost linear with voltage, which translates into an almost constant modulation efficiency. In this operation regime, we measure a modulation efficiency of about 12 pm/V at ambient temperature and 15 pm/V at 4 K. In forward bias (V > 0) we see how the shift in resonance wavelength is exponential with the applied voltage, which translates into an also exponential evolution of the modulation efficiency. In this regime, we measure modulation efficiencies higher than 1,000 pm/V both at 4 K and room temperature.

It is of interest to explain the observed behavior from the physics of the device. We will start by describing the evolution with voltage at a fixed temperature, and afterwards we will explain the differences between ambient and cryogenic temperature operation.

We have identified how in reverse bias the modulation efficiency is almost constant with applied voltage, while in forward bias we see an exponential increase with
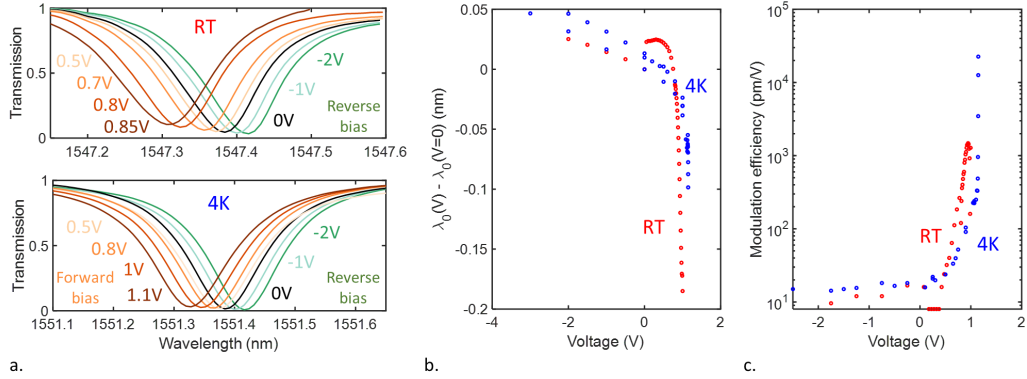
Figure 2-6: Electro-optical characteristics of design C (1550 nm modulator) at room temperature and 4 K. (a) Transmission spectra at different bias voltages at room temperature (top) and 4 K (bottom). (b) Resonance wavelength as a function of bias voltage at room temperature (red) and 4 K (blue). (c) Modulation efficiency as a function of bias voltage at room temperature (red) and 4 K (blue).

increasing voltage. This is due to the different physical mechanism generating the carrier density change in both operation regimes. In reverse bias, the change in carrier density comes from the modulation of the depletion region width with voltage. In a 1D diode, this dependence is relatively weak and proportional to $\sqrt{\phi_{bi} - V}$ [142], where ϕ_{bi} is the junction built-in voltage. While our junction is not a simple 1D diode, we expect the dependence of the depletion region width modulation to be similar. When operating in forward bias, the mechanism that generates the change in carrier density is carrier injection. Carrier injection is limited by the diffusion of carriers through the potential barrier in the p-n junction, which depends exponentially on that barrier and, as a consequence, depends exponentially on the applied voltage [142]. Thus, a much stronger dependence $e^{qV/kT}$ on applied voltage is obtained in forward bias compared to reverse bias, which explains why we observe much larger modulation efficiencies in forward bias operation (Fig. 2-6(c)).

We can also observe differences between the behavior at 4 K and ambient tem-

perature. The most apparent difference is the increased "turn on" voltage of the modulation efficiency in forward bias at 4 K. This is expected, and is tightly related to the IV curve characteristics we studied in Section 2.3.1. There, we explained that the turn-on voltage of the diode at cryogenic temperatures is higher due to an increase in the built-in voltage. Since the modulation efficiency in forward bias is due to carrier injection, we expect it to show a similar behavior to the IV curve.

We can go further than this and try to derive an approximate expression for the evolution of the modulation efficiency in forward bias. As we have mentioned, the modulation mechanism in this regime is carrier injection, which results in added charge stored in the quasi-neutral regions (QNR) of the diode. In an ideal 1D p-n junction, the charge stored in the QNR (Q_d) is given by [142]:

$$Q_d = Q_s \left(e^{\frac{qV}{kT} - 1} \right) \tag{2.4}$$

$$Q_s = \tau_e I_{s,p} + \tau_h I_{s,n} \tag{2.5}$$

Above, Q_s is the charge stored in the QNR in reverse bias, τ_e (τ_h) is the carrier lifetime of electrons (holes) in the region where they are minority carriers, and $I_{s,n}$ ($I_{s,p}$) is the contribution of the n (p) region to the reverse saturation current ($I_s = I_{s,n} + I_{s,p}$).

If we assume that $I_{s,n} = I_{s,p} = I_s/2$ (an assumption that is in general not correct, but that we will do for the sake of simplicity), we get:

$$Q_d = \frac{\tau_e + \tau_h}{2} I_d \tag{2.6}$$

Where $I_d = I_s e^{qV/kT}$ is the current flowing through the diode. The change in the

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total number of carriers is of course Q_d/q, and it should be divided by the total ring volume to obtain the change in carrier concentration ΔN.

We know that, through Soref's equations (Eq. 1.2) we can directly relate ΔN to the change in refractive index Δn, which is directly proportional to the shift in resonance wavelength. Thus, we can write:

$$\text{Modulation efficiency} \quad \propto \frac{dn}{dV} \propto \frac{dN}{dV} \propto \frac{dQ_d}{dV} = \frac{d}{dV}\left(\frac{\tau_e + \tau_h}{2}I_d\right) \qquad (2.7)$$

Assuming that the minority carrier lifetime does not depend on the applied voltage, we conclude:

$$\text{Modulation efficiency} \quad \propto \left(\frac{\tau_e + \tau_h}{2}\right)\frac{dI_d}{dV} = \frac{\tau_e + \tau_h}{2r_d} \qquad (2.8)$$

Where r_d is the differential resistance, which we studied in Section 2.3.1. [2]. We can see how the modulation efficiency in forward bias is tightly related to the IV characteristics of our devices.

It is worth exploring the relation we derived in Eq. 2.8. Note how, if our devices behaved as an ideal diode, the modulation efficiency at 4 K would be 75x larger compared to that of room temperature at the same bias current (since $r_d = kT/qnI$)

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[2]The reader should note that we have not considered any spatial effects in this derivation, which is a very strong simplification. The shift in resonance wavelength of the ring will depend on the change in refractive index only in areas where the optical mode is concentrated. Thus, to get an accurate number for the modulation efficiency from the change in refractive index we should account for the spatial distribution of the optical mode ($E_{opt}(x,y)$) and the refractive index change, which would look something like this:

$$\text{Modulation efficiency} \quad \propto \iint_{ring} \frac{dn(x,y)}{dV}|E_{opt}(x,y)|^2 dxdy \qquad (2.9)$$

This would require the calculation of the change in carrier density as a function of position in the ring, which is complicated and requires the consideration of all the geometry, design and material parameters.

assuming no change in carrier lifetime. This would allow for very high modulation efficiencies at lower bias currents compared to room temperature operation.

The experimental results for design C are shown in Fig. 2-7. The modulation efficiency at 4 K is indeed larger for the same current flowing through the diode (Fig. 2-7(a)), but the measured ratio between the modulation efficiencies at 4 K and room temperature is about 10 (orange dots in Fig. 2-7(b)). This value is much lower than what we would get assuming ideal diode behavior (gray dashed line in Fig. 2-7(b)). This is expected, and is due to the non-ideal evolution of our devices at cryogenic temperatures, which results in increased ideality factors n (Section 2.3.1).

Interestingly, for small bias currents ($I < 1\mu A$), the ratios of measured modulation efficiencies do not coincide with the ratio of dynamic resistances. This suggests that at these bias conditions, the relevant carrier lifetimes τ_e and τ_h are larger at 4 K than at room temperature. For larger bias currents ($I > 1\mu A$) there is a pretty good agreement between the dynamic resistance and the modulation efficiency ratios, which suggests that the carrier lifetimes are more or less the same at 4 K and room temperature. This fact supports the analysis we made in Section 2.3.1: for low bias currents (moderate forward bias), the dominant physical process at cryo temperatures is trap assisted tunneling, with a characteristic 'carrier lifetime' [3]. At larger bias currents, the dominant process becomes carrier injection, which has a faster characteristic carrier lifetime [4]. We will come back to this discussion in the next section, when we analyze the high speed characteristics of our devices.

To conclude, it is worth discussing why, for an ideal diode, we expect a larger

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[3]Note how the term 'carrier lifetime' is technically not correct in this situation, since in trap assisted tunneling the relevant time constant τ is set by the trap physics (mainly its energy and density). Therefore, talking about a 'trap lifetime' might be more accurate.

[4]Now the term carrier lifetime is accurate, since the current mechanism is either impact ionization or diffusion through the p-n junction.
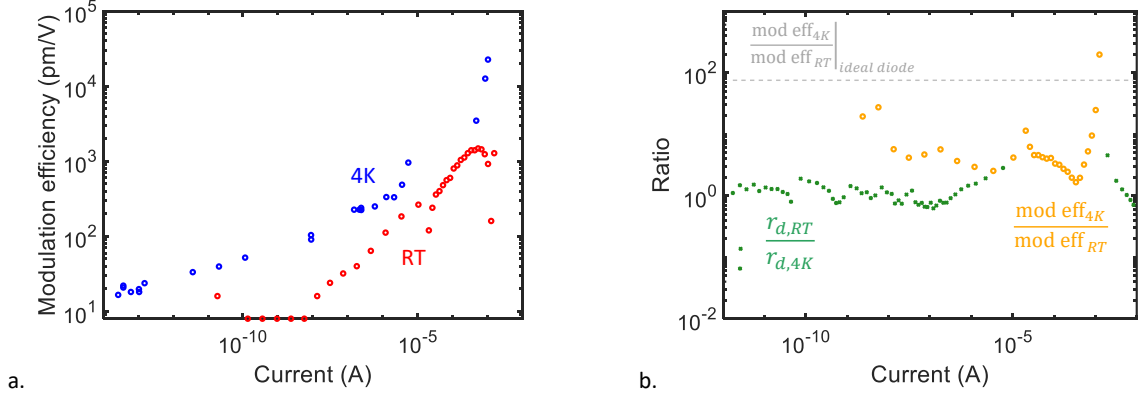
Figure 2-7: Relation between modulation efficiency and IV characteristics. (a) Modulation efficiency as a function of the current flowing through the diode at room temperature (red) and 4K (blue). (b) 4K vs room temperature ratios for relevant parameters as a function of the current flowing through the diode. Green corresponds to the ratio of differential resistance, orange to that of modulation efficiency, and gray shows the theoretical limit for the modulation efficiency ratio of an ideal diode, assuming that carrier lifetimes are temperature independent.

modulation efficiency at 4 K. At cryogenic temperatures the carriers are distributed over a much narrow range of energy states within the conduction and valence bands due to the fact that the occupation probability (which is given by the well-know Fermi-Dirac distribution) is much steeper. As a consequence, the same change in the potential barrier height ΔV results in a larger current increase ΔI at cryogenic temperatures, since the increase in the number of carriers with enough energy to overcome the potential barrier is larger. This is schematically depicted in Fig. 2-8. Since ΔI is larger at cryogenic temperatures, $r_d = \Delta V / \Delta I$ is lower, which translates into a higher modulation efficiency (eq. 2.8).

Summarizing, we have shown how very large modulation efficiencies can be achieved in our devices by operating in the forward bias regime, both at ambient and cryogenic technologies. We have also observed that, for the same current flowing through the
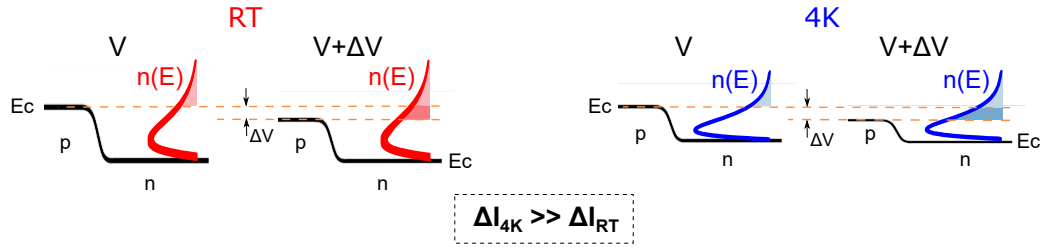
Figure 2-8: Physics of modulation efficiency in an ideal diode at 4 K and room temperature. At low temperatures (blue, right), the energy distribution of the free carriers is more tightly distributed than at room temperature (red, left). As a consequence, the same decrease in the junction's potential barrier ΔV results in a stronger current injection at 4 K, since a larger number of carriers are now energetic enough to overcome the barrier.

device, the modulation efficiency is larger at cryogenic temperatures, and we have discussed why this is the case based on the physics of the device.

2.4 High speed characterization

In the previous sections we have characterized the DC behavior of our devices at cryogenic temperatures. We have confirmed that our devices are still operational and shown that cryogenic operation is advantageous in the forward bias regime, as a larger modulation efficiency is obtained compared to room temperature. The picture is, nevertheless, incomplete, since we still need to characterize the high speed behavior of our devices at low temperature: if the devices are functional but their bandwidth is very low, its attractiveness for cryogenic readout would be greatly reduced.

We characterized the bandwidth for all the different designs both at 4 K and room temperature, and relevant results are shown in Fig. 2-9 and Fig. 2-10. Figure 2-9 shows the bandwidth measured at different bias voltages both at room temperature and 4K, while Fig. 2-10 shows measured frequency responses at selected bias points.

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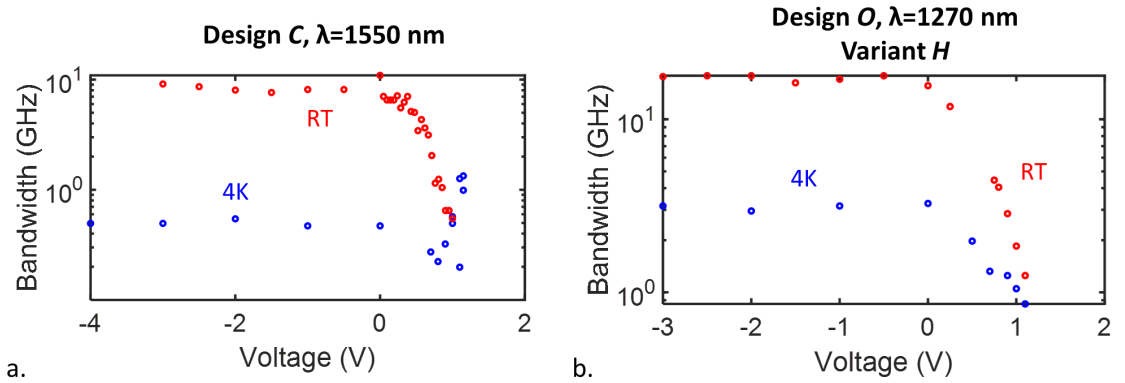
Figure 2-9: 3 dB bandwidth as a function of voltage for design C (a) and design O-H (b) at room temperature (red) and 4 K (blue). In all cases, a transition from an RC limited bandwidth in reverse bias to a carrier lifetime limited bandwidth in forward bias is observed. The bandwidth in reverse bias at 4 K is greatly reduced compared to that at ambient temperature due to carrier freezeout.

These two figures contain a lot of information, which we will go through on the next paragraphs.

(1) Let's start by looking at the 3 dB bandwidth dependence with voltage at room temperature (red curves in Fig. 2-9). The first thing to notice is how, in reverse bias, design O-H has a larger bandwidth than design C (17 GHz compared to 9 GHz, respectively). This is expected, since design O-H uses implants with 2x larger doping concentrations than design C. As a consequence, the access resistance of the spokes is lower, resulting in a shorter RC time constant and a larger bandwidth.

A second important observation is that, for both designs, a sharp decrease in bandwidth is observed as the devices are driven more into the forward bias regime. For design C, we measure a decrease in bandwidth from 9 GHz at -3 V to 1 GHz at 0.8 V, and for design O-H the bandwidth drops from 17 GHz to 4 GHz at these same bias points (the frequency response at these two conditions is shown in Fig. 2-10). This is because our devices switch from being limited by the RC time constant (in

reverse bias) to being limited by the minority carrier lifetime (in forward bias). In forward bias, the excess minority carriers stored in the QNRs need to recombine to reset the device, something which happens on the scale of the carrier recombination lifetime (which for our devices is on the order of ns at room temperature). This is not the case in reverse bias, where the carriers are swept by the strong electric field present in the junction.

An additional interesting observation regarding the frequency response at room temperature is that device *O-H* shows a larger 3 dB bandwidth at forward bias compared to device 1 (4 GHz vs 1 GHz at 0.8 V bias). Two reasons are probably contributing to this difference. The first one is the fact that minority carrier lifetime decreases as doping density increases [153], and the second one is that the SiGe band present in design *O* does likely contribute to the reduction of carrier lifetime due to the addition of recombination sites at defect states.

(2) Let's now look at the differences in the bandwidth at 4 K and room temperature in reverse bias conditions. It is apparent that a large reduction in bandwidth occurs when the devices are cooled down. We measure a 18x reduction in bandwidth from 9 GHz to 500 MHz for design *C*, and a 6x reduction for design *O-H*, from 17 GHz to 3 GHz (see left column in Fig. 2-10). This effect has been observed previously in similar devices [108], and is due to the increase in the device resistance due to the carrier freezeout (less ionized carriers means that less carriers can participate in conduction, resulting in higher resistivity), which increases the RC time constant of the system. In Appendix A.3 we derive the predicted drop in bandwidth from basic theory and compare it to our experimental results.

Notice how the reduction in bandwidth is considerably lower for design *O-H*, which is more highly doped than design *C*. This is expected, since the extent of carrier freezeout is lower for higher doping concentrations. This is because as one

increases the doping concentration an impurity band is formed that allows for movement of the free carriers. In fact, above a threshold impurity concentration (which depends on the material, and is about $6 \cdot 10^{18}$ cm^{-3} for Si) no carrier freezeout is observed at any temperature [120]. This is because the impurity band depends on the average distance between dopants, but is independent of the number of ionized carriers and, as a consequence, independent of temperature. In Appendix A.3.1 we present the theoretical framework for the Mott effect and study the matching between experimental and theoretical results.

(3) Finally, let's analyze the differences between the bandwidth at 4 K and room temperature in forward bias. As can be seen in the right column of Fig. 2-10, each design shows a different behavior: design C shows improved 3 dB frequency at 4 K (1.5 GHz vs 0.8 GHz at 20 μA bias current), whereas design O-H shows a decrease in bandwidth (1 GHz vs 4.5 GHz). This is most likely due to the dependence of carrier lifetime in the doping characteristics of the device and the possible effect of the SiGe band in design O. To the best of the author's knowledge there is not a substantial body of research on the carrier lifetime in Si at temperatures below liquid nitrogen (77 K), so comparing our results to previous lifetime measurements is challenging. The data available at liquid nitrogen and higher temperatures seems to indicate that there is a decrease in the radiative recombination lifetime as temperature goes down [154]. As for Shockley-Read-Hall (SRH) recombination, contradicting results showing a decrease [155] and an increase [156] in SRH rate as temperature decreases have been reported in the literature.

It is worth noting how the bandwidth dependence on bias voltage at 4 K for design C is consistent with our observations on the relevant time constants affecting the modulation efficiency (Fig. 2-7). There, we argued how for weak forward bias the dominant time constant of the system was the 'trap lifetime', which was slower

than the minority carrier lifetime, which dominates at larger forward bias. This is consistent with our frequency response measurements (Fig. 2-9(a)), where a dip in the bandwidth for forward bias voltages < 0.7 V (where the slower 'trap lifetime' dominates) is observed compared to larger bias voltages (where the faster minority carrier lifetime is dominant). This might indicate that a larger bandwidth could be obtained at 4 K for design *O-H* at stronger forward bias voltages than the studied in Fig. 2-9(b).

While the evolution of the forward bias bandwidth with temperature might be dependent on geometry and doping, it is true that this temperature dependence
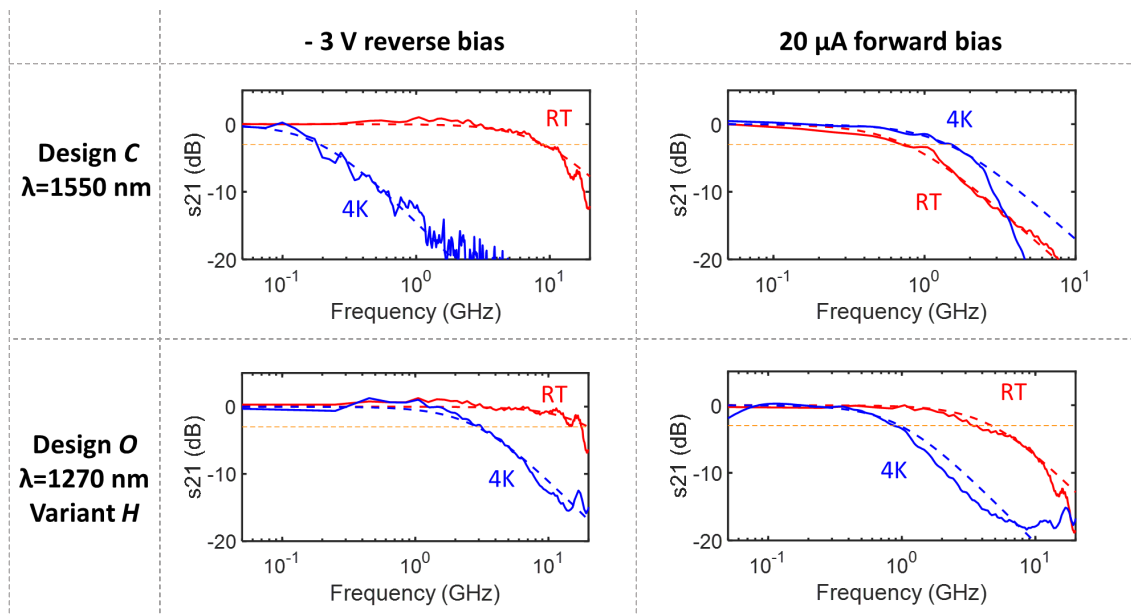
Figure 2-10: Frequency response of design *C* (first row) and design *O-H* (second row) at -3 V reverse bias (left column) and 20 μA forward bias (right column). Spectra at 4 K (blue) and room temperature (red) are shown for each case. The yellow dashed line shows the -3 dB level. For both designs, a bandwidth decrease in reverse bias is observed at 4 K compared to room temperature due to freeze out effects. In forward bias, the bandwidth increases at 4 K for design *C*, but it decreases for design *O-H*.

is much weaker than in reverse bias. This is expected, since carrier lifetime does not change significantly with temperature, but carrier freeze-out can change the resistance (and as a consequence the RC time constant) by orders of magnitude. Additionally, the ohmic heating occurring in forward bias as a consequence of the current flow most likely reduces the impact of carrier freeze-out, which contributes to the bandwidths at 4 K and room temperature being more similar in the forward regime.

Summarizing, we have studied the frequency response of our devices at 4 K and room temperature. We have observed a significant decrease in the reverse bias bandwidth at 4 K due to carrier freezeout, and measured a smaller decrease in devices with higher doping concentrations. Due to the relatively large carrier lifetime in Si, the bandwidth in forward bias is significantly lower than in reverse bias. Nevertheless, the temperature dependence of the forward bias bandwidth is much lower than that in reverse bias, which is explained by the fact that carrier lifetime does not depend strongly on temperature.

2.4.1 The lack of eye diagrams

Eye diagrams with Pseudo Random Binary Signals (PRBS) are the quintessential tool to demonstrate the correct performance of a modulator, so the reader might be wondering why no eye diagrams have been shown for our devices at 4 K. We attempted the acquisition of eye diagrams at cryogenic temperatures, but the low SNR of our output optical signal prevented us from succeeding. The main cause for this low SNR is the high loss of the vertical grating couplers used to couple light in and out of the chip, which is between 10 and 15 dB. This represents a total in-out loss close to 25 dB, which translates in a 25 dB loss in SNR. These losses are not

20 ns

5 mV

$f = 1\ Gbps\ ;\ V_{bias} = -4\ V$
$V_{pp} = 5\ V\ ;\ P_{in} = 5\ mW$

500 ps

2 mV

PRBS signal: pattern dependent effects

Clock signal: no pattern dependent effects

a.

b.
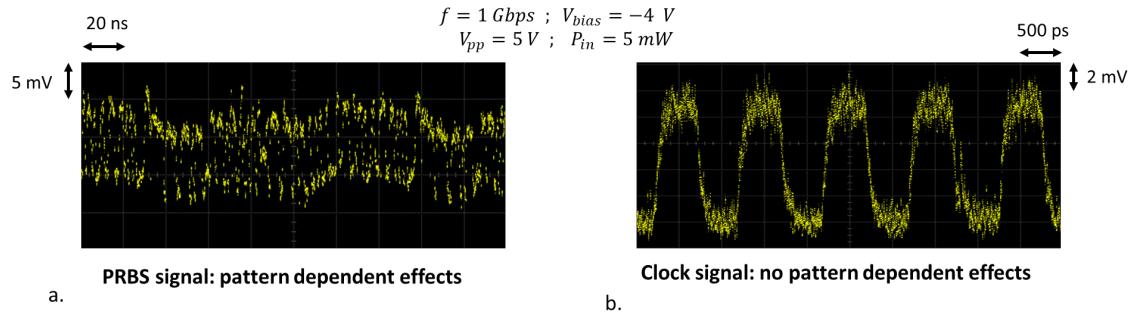
Figure 2-11: Heating effects in modulation waveforms. (a) When a PRBS driving signal is used, the locally varying ratio of '1' and '0' results in a "wander" of the DC value of the output signal. (b) When a clock signal is used, the effects disappear due to the fact that there is a balanced number of '1' and '0'.

fundamental to the coupler themself or to the CMOS platform: grating couplers with > 90% efficiency have been demonstrated in the same CMOS platform we are using [141].

This large hit in SNR made it necessary to either increase the input power to the device (so as to have a stronger optical signal at the output of the modulator) or increase the amplitude of the electrical driving signal (to increase the modulation depth and have a larger '1' to '0' ratio). While possible, we observed pattern dependent effects in both cases (Fig. 2-11(a)) when driving the device with a PRBS signal. We attribute this behavior to unwanted heating caused either by the high circulating optical power in the resonator or by the large ohmic heating due to the high power of the electrical driving signals. As we will discuss in Chapter 5, these effects become more important at cryogenic temperatures compared to room temperature because of the change in the thermal properties of Si and SiO_2.

Due to the fact that PRBS patterns have a locally unbalanced number of '1' and '0' bits, the strength of these thermal effects is pattern dependent, which causes the DC value of the output signal to "wander" as the device resonance shifts due

to the thermo-optic effect (Fig. 2-11(a)). This is more easily understood with an example: imagine a pattern with a long stream of consecutive '0' bits (pattern 1), and a different pattern with a long stream of '1' bits (pattern 2). Pattern 1 will result in an overall heating of the device (since in '0' bits all the light is circulating in the resonator), whereas pattern 2 will result in an overall cooling of the device (since in '1' bits the light does not get into the ring). Temperature changes affect device performance in two ways: (1) they will affect the electrical behavior of the p-n junction; and (2) through the thermo-optic effect, changes in the local temperature of the device cause changes in the resonance wavelength of the ring, and thus change the transmission through the modulator. As a consequence, the output optical signal does not only depend on the driving electrical signal, but also on the temperature changes that the driving electrical signal produces. Since these temperature changes depend on the ratio of '1' and '0' being transmitted, pattern dependent effects arise. If we use a driving signal with a balanced number of '1' and '0', such as a clock signal, the pattern dependent effects disappear (Fig. 2-11(b)).

Having a larger SNR would allows us to decrease both the input optical and electrical powers, which would strongly reduce the heating effects (as these effects are roughly quadratic with input power). Thus, we believe that by improving the grating coupler loss we could eliminate the observed pattern dependence.

Chapter 5 is entirely devoted to the study of these non-linear effects and its impact on modulator performance, so the reader is pointed there for a more in-depth analysis.

2.5 Considerations for cryogenic optical readout

Throughout this chapter we have experimentally characterized the performance of our modulators but we have not discussed in detail where do these results leave our CMOS modulators in terms of applicability to cryogenic readout.

Almost every room temperature application that requires the use of a silicon optical modulator operates in reverse bias. This is because its speed can be much larger than in forward bias and its power consumption is lower since there is no DC current flowing through the device. It is natural to ask ourselves if the use of reverse biased modulators for cryogenic optical readout is possible, something that has been studied before [108]. Three main concerns arise: (1) We have seen how carrier freeze-out profoundly impacts the bandwidth in reverse bias, limiting it to below 3 GHz. While still larger than what we measured in forward bias (about 1.5 GHz), the difference is greatly reduced. (2) The modulation efficiency for reverse biased modulators is low, which means that large peak to peak voltages need to be applied. We already discussed in Chapter 1 how a good modulator for cryogenic readout should be able to operate with electrical signals in the order of μV and mV, since these are the signal levels generated by typical cryogenic circuits. (3) The input impedance of a reverse biased modulator is very large at DC frequencies ($>$ MΩ) and on the order of a few kΩ at frequencies around 10 GHz. As we discussed in Chapter 1, this raises a question about how to perform impedance matching to ensure the correct delivery of signals from the low impedance cryogenic circuits to the high impedance modulator.

While solutions exist for these three concerns, they come at a cost in complexity, performance and, most importantly, power consumption. For example, problem (1) could be solved by increasing doping concentrations, but this increases the optical

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losses in the ring and reduces the quality factor of the resonator, resulting in decreased modulation strength. Problems (2) and (3) could be addressed by the use of an electrical amplifier but, as we reviewed in Chapter 1, these tend to have high power consumption. Thus, the use of reverse biased modulators for cryogenic readout seems challenging.

Nevertheless, the use of forward biased modulators for cryogenic readout could be appealing. In room temperature applications the use of forward biased devices is usually dismissed because its larger power consumption (due to the fact that the diode is turned on, so there is a DC power consumption $P_{DC} = I_{DC}V_{DC}$) and its slower speed compared to reverse bias. Nevertheless, we have seen how cryogenic operation fundamentally changes these performance trade-offs. At 4 K and forward bias we measured a 1.5 GHz bandwidth, which is only 2x lower than that measured for a reverse biased modulator. Also, we have seen how forward bias operation at cryogenic temperatures is beneficial in terms of power consumption compared to room temperature: the same modulation efficiency can be achieved with a lower bias current at 4 K (Fig. 2-7(a)), resulting in decreased power consumption. This is depicted in Fig. 2-12(a), which shows how the same DC power yields a much larger transmission change at 4 K than at room temperature for the same 2 mV differential signal.

But the most important advantage of forward bias operation is its exceptionally large modulation efficiency, which can reach 1,000 pm/V - 10,000 pm/V. This means that a 50-500x smaller electrical signal compared to reverse bias operation (with a measured modulation efficiency around 20 pm/V) can be used to achieve the same optical modulation strength. Thus, while reverse biased modulators cannot generate optical modulation with the typical mV-level voltage signals generated by cryogenic technologies, forward biased modulators could (Fig. 2-12(b)). Additionally, forward
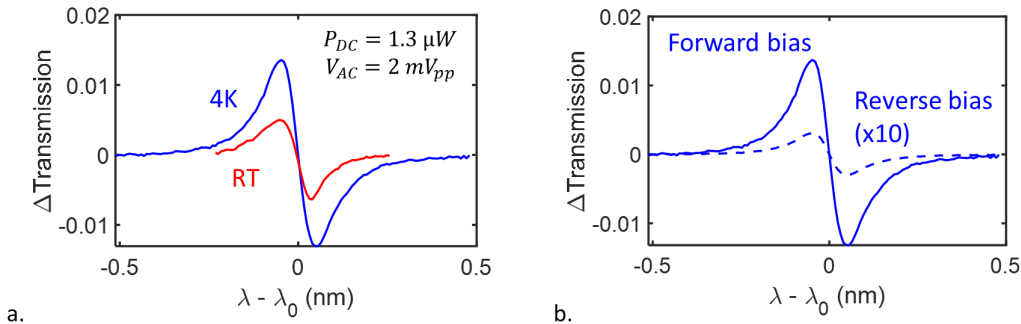
Figure 2-12: The advantages of forward bias operation at 4 K. (a) The same DC power consumption results in a larger modulation strength at 4 K (blue) compared to room temperature (red) due to the smaller differential resistance at low temperatures. (b) Forward bias operation (solid line) at 4 K results in a stronger modulation compared to reverse (dashed line) bias due to the much larger modulation efficiency. The transmission change in reverse bias is enlarged by 10x.

bias modulators have low input impedances below 500 Ω (Fig. 2-3(c,d)), making the direct delivery of signals from cryogenic circuits to the modulator possible.

It seems then that forward bias modulators could be an appealing solution for cryogenic readout. It is worth mentioning that forward bias operation at 4 K has some limitations, mainly a bandwidth limited to about 1-2 GHz and a DC power consumption that could be too high for cryogenic environments with very constrained heat load budgets. In the next chapter we will explore the use of our resonant modulators in the forward biased regime for the readout of SNSPDs.

2.6 Conclusion

In this chapter we have analyzed the behavior of our CMOS resonant modulators at 4 K and compared their performance to that at room temperature. We have shown that these devices are still operational at such low temperatures, but we have

also identified significant differences in its behavior. The IV curves seem to indicate that the main carrier transport mechanism switches from carrier injection (at room temperature) to field-assisted effects (at 4 K) at moderate bias voltages, whereas we have not observed large differences in the shape of the optical resonance when the devices are cooled down. We have seen how modulation efficiency is not largely affected by temperature in reverse bias, but how it increases by about 10x in forward bias at 4 K, which we explained because of the smaller differential resistance at these temperatures. We have also discussed how carrier freezeout causes a much slower frequency response at 4 K in reverse bias, but how this frequency response is not largely affected by temperature in forward bias.

Finally, we have identified the operation of our modulators in forward bias as a promising approach to realize optical readout, since it features a very large modulation efficiency (> 1000 pm/V) and a low input impedance (< 500 Ω). While this operation regime has an associated DC electrical power consumption, it is much lower than at room temperature. The main drawback of forward bias operation is its relatively low bandwidth, which we measured to be between 1 and 2 GHz.

Chapter 3

Cryogenic Optical Readout Through Forward Biased Silicon Modulators

In the previous chapter we have shown how our CMOS photonic modulators are still operational at cryogenic temperatures. In particular, we have seen how forward bias operation could be suitable to realize cryogenic optical readout: (1) very high modulation efficiencies can be reached in this operation regime, which means that the small electrical driving signals coming from the cryogenic device can result in modulation of the optical carrier; and (2) small input impedances in the order of 100 Ω can be obtained, making the direct delivery of the electrical signal coming from the cryogenic device to the modulator possible.

The purpose of this chapter is to demonstrate cryogenic optical readout of a superconducting single photon detector (a Superconducting Nanowire Single Photon Detector - SNSPD) through the use of a silicon modulator biased in the forward regime. This constitutes, to the best of our knowledge, the first demonstration of cryogenic optical readout without the use of an amplifier inside the cryostat. With

orders of magnitude lower power consumption than conventional readout techniques, this work opens up the path for the realization of scalable, low power and high speed cryogenic readout, which could help achieve the full potential of cryogenic technologies.

3.1   Amplifier-less optical readout architecture

As described in Chapter 1, cryogenic optical readout achieves data transfer between the cryogenic and room temperature environments through the use of optical fibers. The cryogenic device generates an electrical signal, which then drives an electro-optical modulator that imprints the signal into an optical carrier, which is transported out of the cryostat through optical fibers.

As we also saw in Chapter 1 (see Table 1.5), the only previous demonstration of cryogenic optical readout reported in the literature used a semiconductor electrical amplifier operating inside the cryostat to amplify the signal generated by a superconducting analog-to-digital converter and drive a laser diode. The scalability of this pre-amplified scheme is hindered by the amplifier's mW-scale power consumption, which makes this approach have a thermal load that exceeds that of conventional electrical readout.

Instead, we propose a scheme where the superconducting device (which in our case is an SNSPD) directly drives the electro-optical modulator, without the need of any cryogenic amplification or impedance matching network. This is possible because we bias the modulator in the forward bias regime. As we have learned in Chapter 2, forward bias modulators make the direct delivery of signals coming from superconducting devices possible:
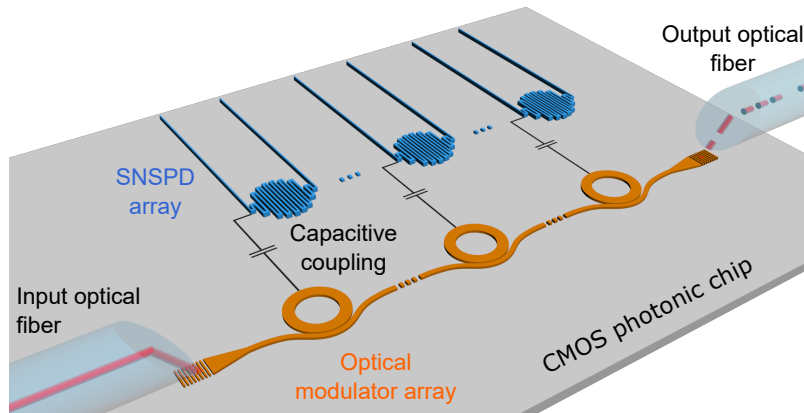
Figure 3-1: Amplifier-less cryogenic optical readout of an SNSPD array. Forward biased optical modulators allow for the direct delivery of the signal generated by the SNSPD to the modulator, which encodes the data into the optical carrier.

1. Very high modulation efficiencies in the range of 1,000-10,000 pm/V can be reached with relatively low power dissipation. This makes it possible to achieve noticeable modulation of the optical carrier with the small electrical signals generated by the SNSPD. With a modulation efficiency of 5,000 pm/V, a 5 mV signal is enough to obtain the same modulation that we would achieve with a 20 pm/V modulation efficiency (a typical number for reverse bias operation) and a 1,250 mV signal.

2. Low input impedances in the order of 100 Ω can be reached. As we will discuss in Section 3.3, this makes the delivery of the signal from the superconducting device to the modulator possible.

By eliminating the high power consumption of the electrical amplifier (which is the main bottleneck for scalable electrical readout) and exploiting WDM, such an amplifier-less scheme (Fig. 3-1) could feature orders of magnitude lower power consumption and thus provide a path to realize scalable, high speed cryogenic readout.

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The optical modulator we used is our zero change CMOS resonant modulator designed for an operating wavelength of 1550 nm, which we have characterized at room temperature in [136] and at cryogenic temperatures in Chapter 2 (design C). As a reminder, at 4 K and in forward bias we measured a 1.5 GHz bandwidth and a loaded Q factor close to 10,000. Modulation efficiencies larger than 10,000 pm/V could be reached.

3.2   SNSPD

The superconducting device we used for our optical readout demonstration is an SNSPD, which as we discussed in Section 1.3.1 is the highest performing detector for time-correlated single-photon counting. For our demonstration we use a Molybdenum Silicide (MoSi) SNSPD optimized for UV photon detection [157]. As shown in Fig. 3-2, the detector has a 10 nm×110 nm cross-section, a 180 nm pitch with a 56 μm diameter active area and shows a detection efficiency of about 70% at 373 nm. This device has a high inductance of $\sim$ 12.8 μH, allowing it to develop a large hotspot resistance during photodetection events. Fits to the rising edge of a typical pulse from the device give a hotspot resistance of approximately 12 kΩ. Compared to typical near-IR SNSPDs with smaller active-areas (with a hotspot resistance $\approx$ 1 kΩ), this high impedance allows the detector to drive a larger load resistance and therefore produce a larger voltage signal at the modulator. The UV detector also has over 60 dB of rejection at 1550 nm, making it less sensitive to any scattering of the light used for the readout. The detector has a higher operating temperature compared to typical near-IR SNSPDs, with a switching current above 10 μA at temperatures
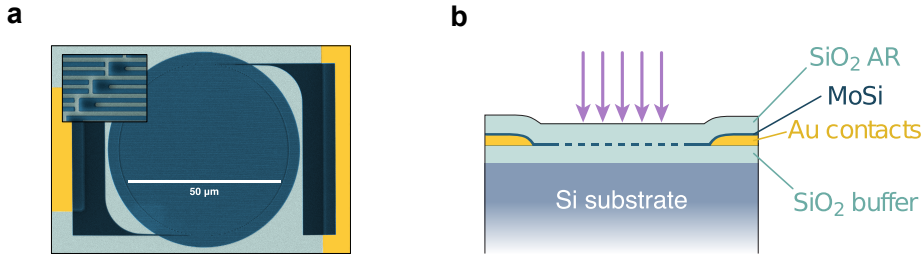
Figure 3-2: UV superconducting nanowire single photon detector. (a) False-color SEM images of the nanowire pattern. The inset shows a closeup on the nanowire meanders. (b) Optical stack cross-section.

below 3.8 K [1].

3.3   Readout circuit

As already mentioned, our amplifier-less readout architecture allows for the SNSPD to directly drive the optical modulator. A passive circuit is needed for two purposes: (1) allow for different DC bias points for the SNSPD and the modulator; and (2) provide a reset branch to avoid the SNSPD from "latching" into its normal state (a situation in which the SNSPD cannot thermally relax to the superconducting state [158]).

A simplified schematic of the readout circuit and its operation is shown in Fig. 3-3. The decoupling capacitor ($C_{\mathrm{DECOUPLING}} = 100\ pF$) allows for separate DC biases to each device while coupling the AC signal generated by the SNSPD into the modulator. When the SNSPD is superconducting, it provides a low impedance path to ground so all the bias current flows through it (Fig.3-3(a)). After the SNSPD absorbs a photon, the developed hotspot resistance (~ 12 kΩ) diverts most of the current into the readout, producing a voltage pulse that drives the modulator and

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[1]Typical switching currents for near-IR SNSPDs are around 4 μA at operating temperatures $<$ 1 K.

shifts its resonance, changing the intensity of the transmitted light (Fig.3-3(b)). A reset circuit ($L_{\text{RESET}} = 8\ \mu H$, $R_{\text{RESET}} = 50\ \Omega$) provides a low-impedance path to ground, diverting any leftover current from the nanowire, allowing for the hotspot to thermally relax and for the SNSPD to return to its superconducting state (Fig.3-3(c)). The values for L_{RESET} and R_{RESET} were optimized to (1) ensure that any leftover current flowing through the nanowire is eventually sunk into the passive reset branch (with $R_{\text{RESET}} = 50\ \Omega$, 99.6% of the residual current is redirected to the reset) and (2) ensure the time constant of the reset branch is slow enough to allow for a voltage signal to develop at the modulator, but fast enough to not be limiting the speed of the readout.

Notice that the key working principle for this readout configuration is the fact that, when the SNSPD becomes resistive, most of the current flowing through it is diverted into the modulator, generating a resonance shift. Of course, the amount of current delivered to the modulator (and therefore the modulation strength) will depend on its input resistance, since we essentially have a current divider between the SNSPD and the modulator: $I_{mod} = I_{bias,SNSPD} R_{SNSPD}/(R_{SNSPD} + R_{mod})$. Clearly, to maximize the current delivered it is necessary to minimize the resistance of the modulator, which makes operation in forward bias very appealing. With the input resistance $R_{mod} \approx 100\ \Omega$ we measured for our device (Section 2.3), 99% of the SNSPD bias current is delivered to the modulator.

3.3.1 Readout simulation

It is very useful to derive an equivalent circuit model of our readout system for simulation and analysis. Since our CMOS modulator is essentially a p-n junction, its equivalent circuit model is just that, a diode. Several equivalent circuit models
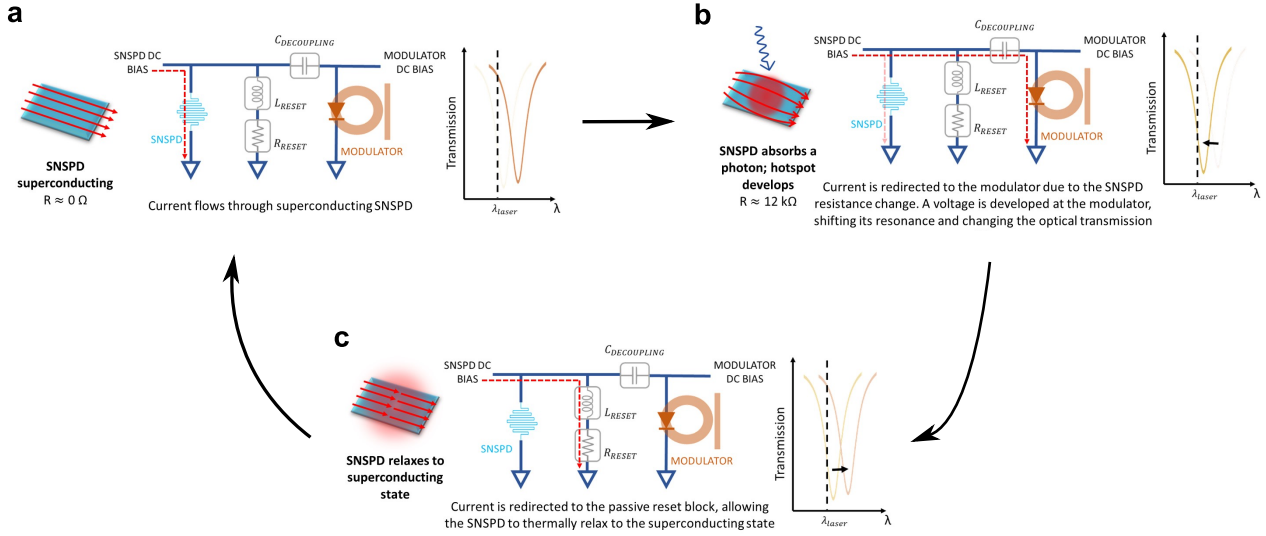
Figure 3-3: Working principle of the SNSPD optical readout. (a) The superconducting SNSPD provides a low impedance path to ground so all the bias current flows through it. (b) When the SNSPD absorbs a photon, the developed hotspot resistance diverts the current into the readout, producing a voltage pulse that drives the modulator and shifts its resonance, therefore changing the transmitted light. (c) The passive reset circuit provides a low-impedance path to ground, allowing for the hotspot to thermally relax and for the SNSPD to go back to its superconducting state. $C_{\text{DECOUPLING}} = 100 \ pF$, $L_{\text{RESET}} = 8 \ \mu H$, $R_{\text{RESET}} = 50 \ \Omega$.

for SNSPDs with varying complexity have been used and proposed in the literature [159, 160]. Here, we use one of the simplest, in which the SNSPD is modeled as a fixed inductor (whose value corresponds to the kinetic inductance of the nanowire) in series with a resistor. The resistor value switches from $R_{SNSPD} = 0 \ \Omega$ in the superconducting state to $R_{SNSPD} = R_{normal}$ in the normal state (whose exact value depends on the type of SNSPD). The switching time τ_{sw} between the superconducting and normal states also depends on the device and is usually obtained by fitting to experimental data.

Figure 3-4 shows the equivalent circuit model we used to simulate our readout
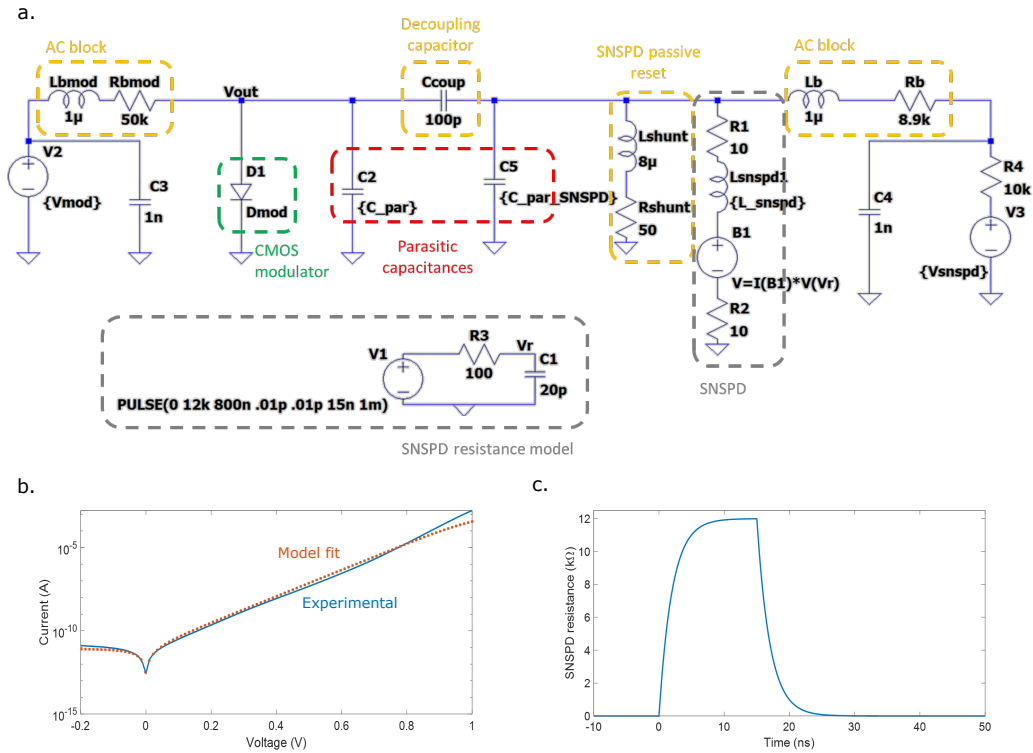
Figure 3-4: Readout system equivalent circuit. (a) Equivalent spice model. Relevant blocks are highlighted. (b) The IV curve of the modulator. Orange dots show the simulated IV curve, and the blue line shows experimental data. (c) Modeled SNSPD resistance as a function of time.

system. Notice how inductive AC blocks are used for DC biasing the SNSPD and modulator. Two parallel capacitors (C_{PAR}, $C_{PAR,SNSPD}$) are added at either side of the decoupling capacitor to account for any parasitic capacitance present in the system (due to device packaging, the PCB, the diffusion capacitance of the modulator...). Figure 3-4(b) shows the simulated IV curve of the modulator, and Figure 3-4(c) shows the resistance change of the SNSPD. The UV SNSPD we used has an $R_{normal} = 12 \ k\Omega$ and a switching time $\tau_{sw} = 2$ ns, which were obtained by fitting to experimental data on the SNSPD alone.

By simulating this equivalent circuit model using LTSpice we can study how

Parameter	Value	Parameter	Value
C_{par}	3 pF	$C_{par,SNSPD}$	50 pF
V_{mod}	3.15 V	V_{SNSPD}	0.17 V
L_{SNSPD}	12.8 μH	D_{mod}	Standard spice diode model: D (IS=1E-11, N=2.8, CJO=0f, VJ=1, m=0.4, RS = 100)

Table 3.1: Default parameters used for the simulation of the readout circuit.

different circuit parameters affect the readout performance. Table 3.1 shows the default parameters used in the circuit simulation. Unless otherwise stated, these are the values that were used to obtain the simulation results we are going to discuss below.

Let's start by analyzing the effect of parasitic capacitance. Fig. 3-5 shows the simulated voltage at the modulator terminals for different parasitic capacitance values. Fig. 3-5(a) shows different parasitic capacitances at the SNSPD side ($C_{par,SNSPD}$), while Fig. 3-5(b) corresponds to varying parasitic capacitance at the modulator side (C_{par}).

Several important conclusions can be drawn from these results. Clearly, having large parasitic capacitance is detrimental for circuit performance: not only the circuit response becomes slower (the rate of oscillation damping slows down as parasitic capacitance increases), but the amplitude of the modulator driving signal also decreases, which translates into a weaker modulation and a readout signal with decreased SNR. The reason why a slower response is obtained for larger parasitic capacitance values is simple: larger C values result in an increase in the RC time constant of the system. At the same time, larger values of capacitance translate into lower impedance values at AC frequencies ($Z_C = 1/jCw$). This means that as parasitic capacitance increases, a larger part of the current coming from the SNSPD

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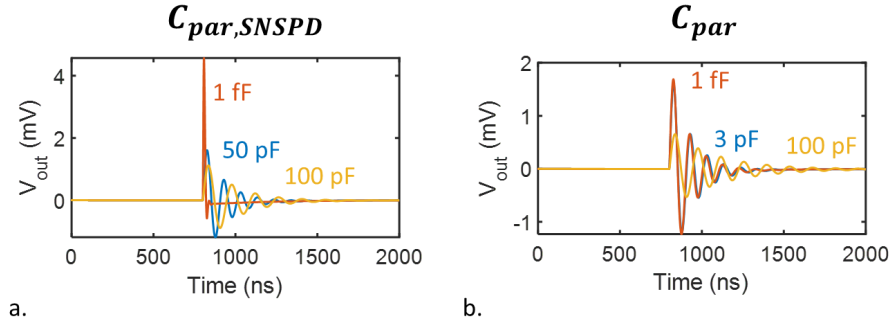
Figure 3-5: Effect of parasitic capacitances on the system response. (a) Voltage signal at the modulator terminals for different values of parasitic capacitance at the SNSPD side ($C_{par,SNSPD}$). (b) Voltage signal at the modulator terminals for different values of parasitic capacitance at the modulator side (C_{par}). In both cases, larger parasitic capacitance results in a slower response and a lower voltage amplitude.

sinks into these capacitors and does not get into the modulator, thus decreasing the driving signal.

Interestingly, we can see how the parasitic capacitance at the SNSPD side has a larger effect on the response that that at the modulator side. This is because at the SNSPD side, the current splitting happens between the parasitic capacitance of the SNSPD $C_{par,SNSPD}$ and the decoupling capacitor. These have similar impedances and, as such, small impedance variations can cause large changes in the current splitting. On the contrary, at the modulator side the splitting occurs between the diode and the parasitic capacitance C_{par}. At the bias currents we are simulating, the diode has a resistance close to its series resistance ($\approx 100 \ \Omega$), but the decoupling capacitor has impedance at least an order of magnitude larger at frequencies around 1 MHz. Since the impedances are so different, the current splitting is not as sensitive to variations in C_{par}.

We can conclude that minimizing parasitic capacitance is paramount for our readout circuit to have a fast response and generate as large an optical signal as pos-

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sible. Since $C_{par,SNSPD}$ has a larger impact on the overall response, ensuring that the SNSPD packaging has low parasitics would ensure a faster response. Unfortunately, this requires the redesign of the SNSPD chip packaging, which was not possible for us to do.

It is also interesting to analyze the effects of different bias points on the circuit performance. The results are shown in Fig. 3-6. Fig. 3-6(a) shows the effect of varying the bias current for the SNSPD. As expected, increasing the bias current increases the amplitude of the driving signal at the modulator terminals. This is because a larger bias current at the SNSPD means that a larger current is diverted into the modulator when a photon is absorbed, therefore producing a larger voltage. Nevertheless, we should note that the SNSPD bias current cannot be arbitrarily high, as there is a threshold current above which the devices become non-superconductive - the critical current. For our SNSPDs, this critical current is around 10 μA.

Fig 3-6(b) show the effects of varying the modulator bias current. We can see how increasing the DC bias current results in a larger differential current signal at the modulator terminals. A larger differential current does of course result in a stronger optical modulation, since $\Delta\lambda_0 \propto \Delta V/r_d = \Delta I$, as we saw in Chapter 2.

Interestingly, the amplitude of the current signal saturates at large bias points. Disregarding parasitic capacitance effects, the value of the current at the modulator is given by $I_{mod} = I_{bias,SNSPD}R_{SNSPD}/(R_{SNSPD} + R_{mod})$, which reaches a maximum when the modulator resistance R_{mod} is the lowest. Since the minimum possible R_{mod} corresponds to the series resistance of the diode R_s, the maximum differential signal at the modulator is $I_{mod,MAX} = I_{bias,SNSPD}R_{SNSPD}/(R_{SNSPD} + R_S)$. $I_{mod,MAX}$ is shown in the dashed gray line in Fig. 3-6(b) for our modulator with $R_s = 100\Omega$. We can see how the simulated points never reach this limit, and this is because part of the current is also diverted into the parasitic capacitances.

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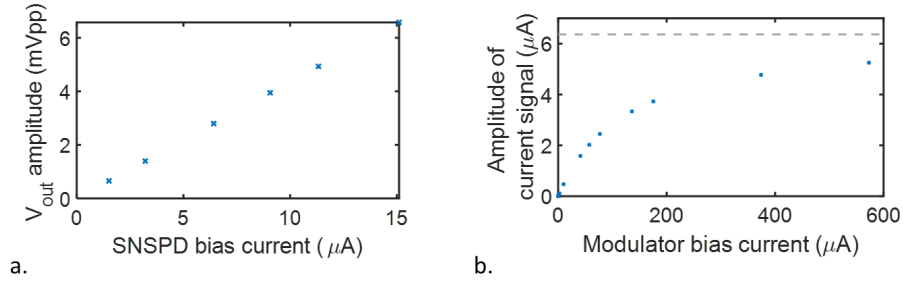
Figure 3-6: Effect of bias points on the system response. (a) Amplitude of the voltage signal at the modulator terminals for different values of the SNSPD bias current. (b) Amplitude of the current signal at the modulator terminals for different values of the modulator bias current. The dashed gray line shows the maximum possible amplitude assuming no parasitic capacitance effects.

This is, nevertheless, not the whole picture. Even if the current signal does not increase, a larger modulator bias current will be beneficial since it results in a larger modulation efficiency (Chapter 2, Fig. 2-6). We cannot, nevertheless, make the bias current arbitrarily high, since this will increase the power dissipation and eventually result in a heating of the cryogenic environment (as we will experimentally characterize in a later section).

We can thus conclude that increasing the bias current at the modulator is beneficial to achieve a stronger optical signal. Nevertheless, we need to be careful, as larger bias currents result in increased power dissipation, which is to be minimized if we want our approach to be appealing for scalable cryogenic readout.

In summary, we discussed how minimizing parasitic capacitance (especially at the SNSPD side) is very important to ensure a system with a fast response and stronger modulation. Increasing the bias current at the SNSPD also results in larger modulation, but this is intrinsically limited by the critical current of the nanowires. Finally, increasing the modulator bias current also results in stronger modulation because of two reasons: more current is diverted into the device due to a decrease in

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its resistance, and a larger modulation efficiency is obtained.

3.4   Readout system packaging

The realization of the proposed readout scheme requires a substantial packaging effort. On the first place, a PCB is needed to implement the readout circuit we described in the previous section. Second, we need a fiber packaging approach, since the system will be operating in a cryostat without optical fiber probes that can be aligned in real time or optical windows that can be used to couple light from the outside of the cryostat. Finally, we also need a means to launch light into the SNSPD.

3.4.1   PCB design

Figure 3-7(a) shows the layout of the designed PCB, which implements the circuit shown in Fig. 3-4(a). Several considerations affected the PCB design:

- The bottom layer of the PCB is completely gold plated to maximize thermal contact to the cold head and ensure correct thermalization of the whole system.

- As we analyzed in the previous section, minimizing parasitic capacitance is critical to the performance of the system. To this end, we use the maximum available FR-4 dielectric thickness of 3.2 mm, and the thinnest possible metal traces.

- We need to ensure that the passive components used in the PCB (inductors, capacitors and resistors) are still operational at cryogenic temperatures and that its values are still close to the room temperature nominal values. Air-coil

inductors, silicon capacitors and thin film resistors were used since they show very low temperature dependence.

- Bond pads are included to allow connection of the SNSPD and modulator chips through wirebonds. Aluminum wirebonds were used for the SNSPD, whereas gold wirebonds were used used for the modulator (see Fig. 3-7(b)).

It is worth mentioning that, while we used an external PCB, we could have implemented the passives in the CMOS chip itself using integrated resistors, inductors and capacitors. This way we could have directly connected the modulator and SNSPD chips through wirebonds without the need of the PCB, resulting in decreased parasitics.

3.4.2 Cryogenic fiber attach

As we discussed in Chapter 1, developing a robust, reliable and repeatable cryogenic fiber packaging technique capable of surviving the thermal stresses associated with the cooling from room temperature is essential for the wide adoption of cryogenic optical readout.

We put a substantial amount of effort into developing a cryogenic fiber packaging suitable to our needs. Our CMOS chip uses vertical grating couplers designed for a 5 μm mode field diameter (MFD) to couple light into and out of the chip at angle of about 16 degrees with respect to the chip normal. These structures have stringent misalignment tolerances of about 1 μm. Thus, the fiber attach mechanism has to maintain the fiber tip position within 1 μm throughout the whole process of placing the system into the cryostat and cooling it down to 3.6 K.

A first approach we tried was to glue single cleaved fibers at the optimal incidence angle, as shown in Fig. 3-8(a). This approach was not mechanically stable due to
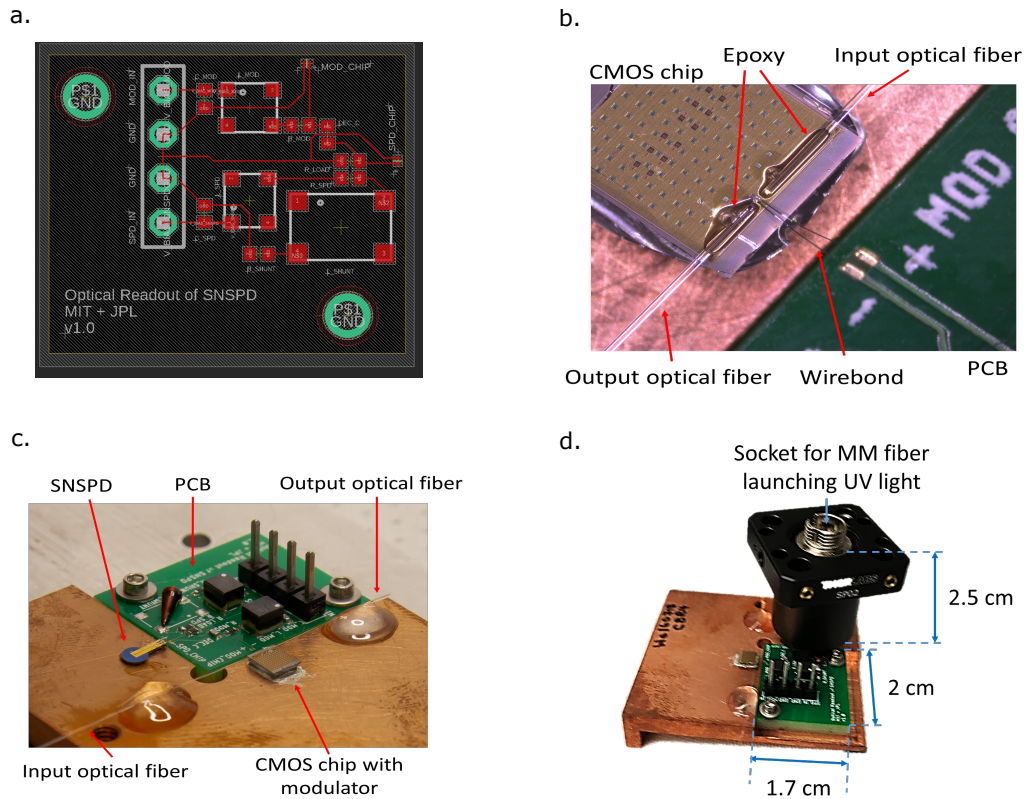
Figure 3-7: Optical readout system packaging. (a) PCB layout. (b) Packaged CMOS chip. The epoxied fibers are visible, as well as the wirebonds to the PCB. (c) Full packaged system. The SNSPD, the CMOS chip, the PCB and the attached optical fibers are all sitting in a copper chuck which attaches to the cryostat. (d) Full system ready for placing in the cryostat. A lens tube is used to launch UV light into the SNSPD and provide optical isolation between the UV and the infrared light. Representative dimensions are shown.

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the high stress the fiber tip was subject to. To provide stress relief we also tried using fibers held by quartz v-grooves, as shown in Fig. 3-8(b). While the mechanical stability was greatly improved, the large amounts of epoxy needed to glue the v-groove to the chip resulted in substantial creep of the epoxy when cooled down to cryogenic temperatures, causing the alignment to move and even crack.

In the end we used a very similar approach to the one described by McKenna et al. [135]. Angle-polished fibers matched to the design angle of the grating couplers were glued to the chip after optimization of the alignment with micropositioners using Norland Optical Adhesive 88 (NOA 88). A 1.1 W, 365 nm UV LED was used to cure the NOA, and the attach was left sitting at ambient temperature for 24 hours to ensure optimal adhesion. Two different gluing steps were performed. First, a small amount of NOA was deposited and cured at the fiber tip to ensure it is correctly held in place. Second, a large amount of NOA was deposited away from the tip to serve as stress relief and ensure that any movement of the rest of the fiber does not affect the highly sensitive fiber tip attach. For each step, the total curing time was about 3 minutes, distributed in short, 30 second intervals.

This approach proved to be mechanically robust due to the fact that the fibers are laying horizontally on the chip, and did not suffer from substantial misalignment when cooled down to cryogenic temperatures because of the small amount of epoxy used at the fiber tip, where the alignment is most sensitive. The resulting fiber attach is shown in Fig. 3-7(b,c).

Optimal alignment of SMF-28 fibers with a 10 μm MFD to the grating couplers in the CMOS chip resulted in 10 dB insertion loss per grating coupler. Due to tolerances in the polish angle and non-perfect alignment, we incurred in around 3.5 dB of extra loss after curing of the epoxy at room temperature. During the cooldown from room temperature to 3.6 K, 1.5 dB was lost due to thermal contraction of the epoxy. These
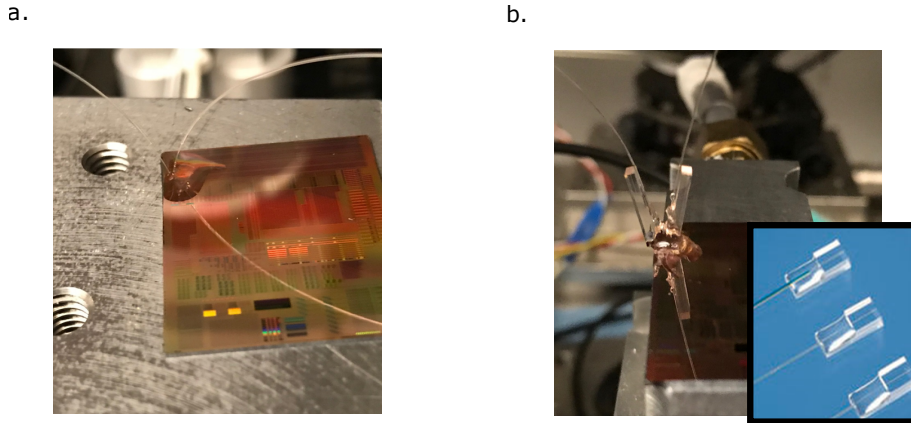
Figure 3-8: Fiber packaging trials. (a) Cleaved fibers at the optimal angle are directly attached to the chip with epoxy, This approach was not mechanically stable due to the high stress at the fiber tip. (b) Fibers in a v-groove are attached to the chip. The larger surface area and smaller stress make this attach mechanically robust, but the large amounts of epoxy needed resulted in a misalignment when cooled down to cryogenic temperatures. The inset shows the optical fibers in the v-grooves. The final packaging with horizontal, angle cleaved fibers is shown in Fig. 3-7.

result in a total loss of about 15 dB per attached fiber, which translates into a 30 dB total optical insertion loss between the input and output of the cryostat.

It is important to mention that these high losses are not intrinsic to the technology. Grating couplers with > 90% efficiency have been demonstrated in our CMOS photonic platform [141]. With the use of optimized grating couplers and a better polish angle control, total insertion losses could be reduced to about 3-5 dB after cooling down to cryogenic temperatures. As will be analyzed in a later section, such a reduction would allow for a much better system performance.

3.4.3   Launching light into the SNSPD

Our packaging system also needs to provide a means to flood illuminate the SNSPD to generate photodetection events. As shown in Fig. 3-7(d), we used a tube lens to

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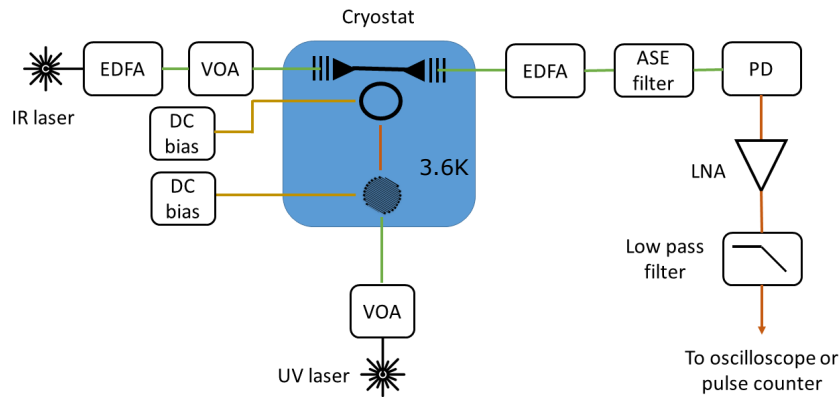
Figure 3-9: Experimental setup for the characterization of the readout system. EDFA = Erbium Doped Fiber Amplifier. VOA = Variable Optical Attenuator. ASE = Amplified Spontaneous Emission. PD = Photodetector. LNA = Low Noise Amplifier.

provide an easy way to attach the fiber carrying the UV light and at the same time ensures optical isolation between the SNSPD and the readout light (infrared light at 1550 nm). This way we guarantee that no scattered infrared photons from the readout light cause the SNSPD to generate a photodetection event [2].

3.5 Readout system: experimental characterization

3.5.1 Experimental setup

Fig. 3-9 shows the experimental setup used to characterize the readout system. The packaged optical readout system was operated on the 2nd stage of a two-stage Gifford-McMahon (GM) cryocooler. The output optical signal from the cryostat was

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[2]As specified earlier, the UV SNSPD has a 60 dB supression at 1550 nm, so even without the tube lens, 10^6 more infrared photons would be needed to generate a detection event compared to UV photons.

connected to a high speed photodetector (New Focus 1544B), and the resulting electrical signal was amplified using a Low Noise Amplifier (Mini Circuits ZKL 1R5+). A low pass filter was then used to remove high frequency noise, and its output connected either to a high speed oscilloscope (Agilent DSO81204A) or a pulse counter (Agilent 53131A).

To overcome the high, 30 dB optical insertion loss coming from the non optimized grating couplers, an EDFA (JDSU Erfa 1215) was used at the input of the cryostat to amplify the light coming from a C band tunable laser (New Focus TLB-6600), and a variable optical attenuator (Ando AQ8201-31) was used to control the optical power getting into the cryostat. For the same reason, an additional EDFA followed by a narrowband filter (Agiltron FOTF) to eliminate ASE noise was used at the output of the cryostat before going into the photodetector.

A UV laser (PicoQuant LDH-P-C-375) followed by a chain of optical filters was used to control the UV power incident on the SNSPD.

3.5.2 Optical readout heat load

One of the main concerns of operating the CMOS modulator at the same temperature stage as the SNSPD is the possibility of thermal crosstalk between the two devices. It is very likely that the modulator is locally at a temperature higher than that of the cryogenic environment (which is around 3.6 K) for two reasons: (1) Ohmic heating resulting from the forward bias operation of the modulator and (2) free carrier absorption. Additionally, high input optical powers could also result in an increase in the temperature of the cryogenic environment. Excessive heating could be fatal for the operation of the SNSPD since its switching current depends strongly on its temperature.

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We recorded the SNSPD switching current for different modulator bias points and different input optical powers to the cryostat. The results are shown in Fig. 3-10. Increasing the modulator bias current or the optical power results in a decrease in the SNSPD switching current caused by an increase in its temperature. This has a direct effect in the quality of the optical readout: a lower switching current results in a lower driving signal at the modulator, which translates into a lower wavelength shift and shallower modulation.

If we set the boundary of acceptable heating to a 20% decrease in the switching current (from 9 μA without any heat load to 7 μA), modulator bias currents up to 70 μA and input optical powers up to 2 mW are acceptable. The operating conditions for the experimental results presented in the following sections are 25 - 40 μA of modulator bias current and 1 mW of input optical power, which are within the acceptable bounds.

Based on measurements of the switching current as a function of temperature on a standalone SNSPD, switching currents above 7 μA are obtained for temperatures <3.8 K. This means that our forward biased CMOS modulator results in a minimal increase in the SNSPD temperature of <200 mK. Moreover, as will be discussed in a later section, simple improvements to the optical coupling to the CMOS chip could decrease the heat load by 2 orders of magnitude, which would eliminate any detrimental effects to the SNSPD operation caused by the optical readout.

3.5.3 Optical readout pulses

As explained earlier, every photon incident on the SNSPD generates a driving signal at the modulator, which imprints it into the intensity of the readout optical signal. Figure 3-11(a) shows a typical readout waveform recorded using a high speed os-
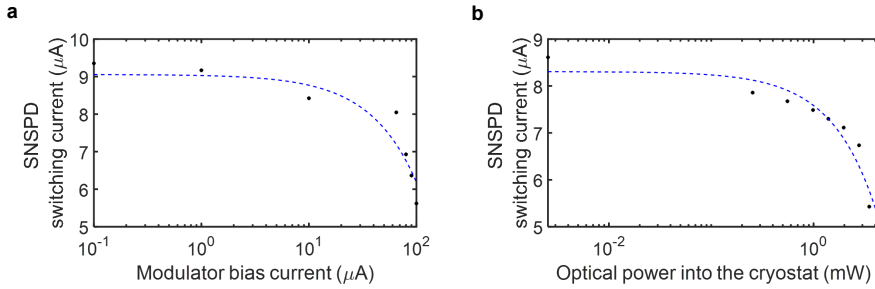
Figure 3-10: SNSPD switching current as a function of the modulator bias current (a) and as a function of the input optical power into the cryostat (b). Dots are measured values, and dashed lines are a linear fit as a guide to the eye. Modulator bias currents up to 70 μA and optical powers up to 2 mW result in switching currents above 7 μA. The switching current without any extra heat load is about 9 μA.

cilloscope. 1 mW of input 1550 nm light was used for readout of the modulator, corresponding to 30 μW on chip after the input grating coupler (which as we discussed has a 15 dB optical loss). The SNSPD bias was 6 μA, while the modulator was biased at 40 μA, corresponding to a modulation efficiency of 10,000 pm/V, 45 μW of electrical power dissipation and an input resistance of $\approx$ 100 Ω.

Figure 3-11(b) shows the readout pulse generated by a single photon detection event. The effects of the high parasitic capacitance are clearly visible: the signal differs from typical SNSPD pulses and shows slowly decaying oscillations. The parasitics come mainly from the SNSPD chip, which is not optimized to minimize stray capacitance. The peak to peak amplitude of the driving electrical signal (obtained by simulating our equivalent circuit model presented in Section 3.3.1 [3]) is only 2 mV. Clearly, this amplitude would not be enough to generate a signal for a reverse biased modulator, but the very high modulation efficiencies we can attain in forward bias make such small voltages enough to achieve modulation.

Figure 3-11(c) shows a single readout pulse for a lower modulator bias current

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[3]We fit the experimental response in Fig. 3-11(b) to our circuit simulation, and we obtained parasitic capacitance values $C_{par} = 70$ pF and $C_{par,SNSPD} = 80$ pF.
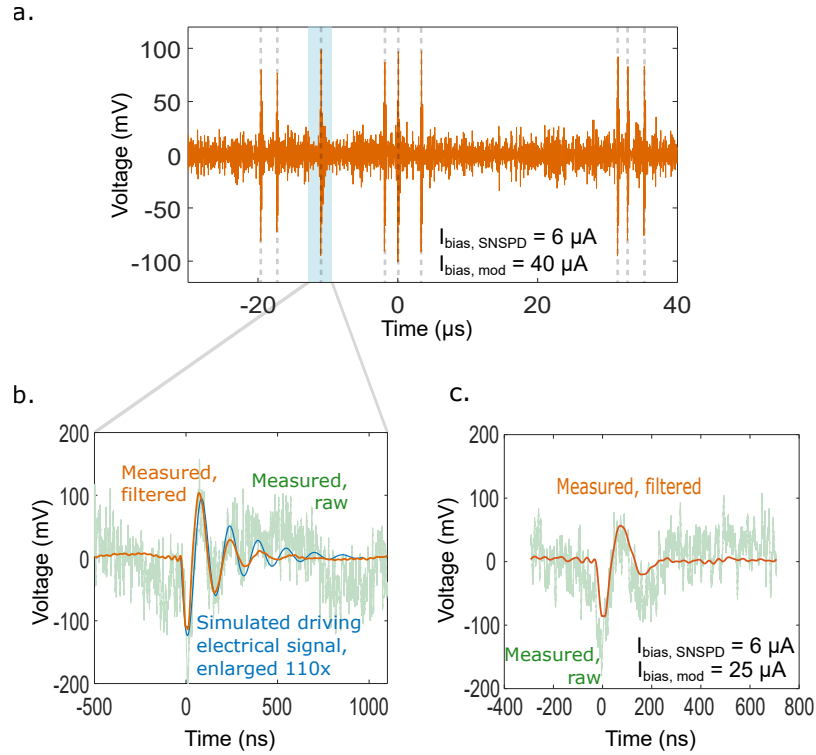
Figure 3-11: Output pulses generated by the optical readout system. (a) Filtered optical readout signal obtained for a 6 μA SNSPD bias current and 40 μA modulator bias current. SNSPD triggering events are highlighted. (b) Readout pulse generated by a single photon for a 6 μA SNSPD bias current and 40 μA modulator bias current. Orange shows the filtered signal, light green a single readout pulse and blue depicts the simulated electrical driving signal. (c) Readout pulse for a modulator bias current of 25 μA and an SNSPD bias of 6 μA. As expected, the amplitude of the output pulse in (c) is lower than in (b) due to the decreased modulation efficiency at lower bias currents.

of 25 μA. As expected, a decrease in the bias current of the modulator results in a smaller amplitude pulse due to a reduced modulation efficiency, but has also a lower electrical power dissipation. A 25 μA bias current corresponds to a modulation efficiency close to 4000 pm/V, which reduces the peak to peak amplitude to around 150 mV and the power dissipation to about 28 μW.

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Data treatment for optical readout pulses

Due to the 30 dB optical coupling losses and the use of Erbium Doped Fiber Amplifiers (EDFAs) both at the input and output of the cryostat, our optical readout demonstration suffered from a low SNR. We applied some digital filtering to the readout waveforms to compensate for this low SNR. Figure 3-12 depicts the data treatment process:

- A single optical readout pulse, which as discussed has a low SNR, is shown in green in Fig. 3-12(a).

- To reduce the noise, we configured the oscilloscope to take an average of 500 pulses, shown in red in Fig. 3-12 (a).

- As shown in Fig. 3-12(b), after the averaging a low frequency sinusoidal component at 1 MHz is present. To remove it, we calculated the Fast Fourier Transform (FFT) of the readout signal and substituted the frequency component at 1 MHz by the interpolation of its two nearest neighbors. We also applied a low pass digital filter to remove high frequency noise above 30 MHz. The FFT of the signal before and after the filtering step is shown in Fig. 3-12 (b). The resulting waveform is shown in black in Fig. 3-12 (a).

3.5.4   Pulse counting

We also characterized the number of counts registered by the optical readout system by connecting the output signal to a pulse counter. Figure 3-13(a) shows the number of counts for different UV powers and different SNSPD bias currents. The modulator bias current was kept at 40 μA and the readout input optical power to the cryostat

125
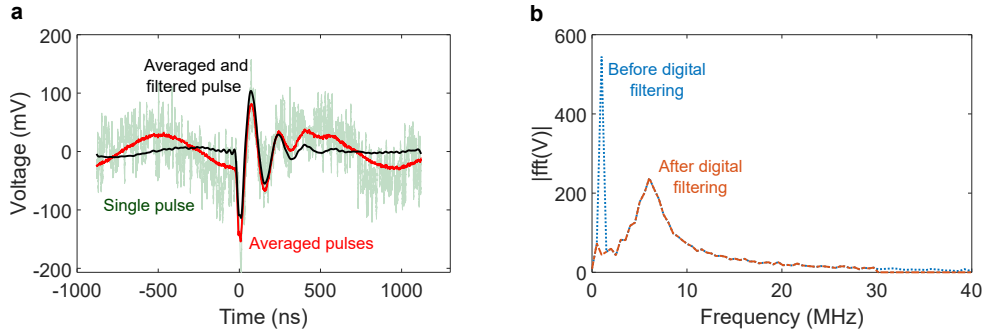
Figure 3-12: Filtering of optical readout pulses. (a) Optical readout signal in the time domain. Light green shows a single optical readout pulse, red corresponds to an average of 500 pulses, and black shows the averaged and digitally filtered readout. (b) Magnitude of the FFT of the readout signal before (blue) and after (orange) the digital filtering step. A low pass filter with 30 MHz cutoff is applied, and the frequency component at 1 MHz is interpolated using the nearest neighbors. The shown pulse corresponds to a modulator bias current of 40 μA and and SNSPD bias of 6 μA.

was 1 mW. Above 6.6 μA bias current the SNSPD undergoes relaxation oscillations [161] and is not photosensitive anymore. As expected, and shown in Fig. 3-13(b), the number of generated pulses depends linearly on the UV optical power hitting the SNSPD [4]. The internal efficiency of the SNSPD decreases for decreasing bias currents [157], which explains why the number of recorded counts in Fig. 3-11(b) is smaller for lower bias currents.

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[4] The solid lines in Fig. 3-13(b) showing the expected number of counts for each incident laser power are obtained by using the number of counts recorded experimentally for the lowest UV laser power, and assuming a perfectly linear detector, such that:

$$counts_{expected}(P_{in}) = P_{in}\frac{counts_{measured}(P_{min})}{P_{min}} \tag{3.1}$$

In our case, P_{min}=25 nW.

Pulse counting efficiency

It is of interest to estimate the pulse counting efficiency of our readout. We begin by estimating the number of counts per second we would expect from the number of photons hitting the SNSPD:

$$cps = \eta_{snspd} * \eta_{misalignment} * \frac{P_{int}(r_{snspd})}{P_{int}(r \to \infty)} * \phi_{TOT} \tag{3.2}$$

ϕ_{TOT} is the total flux of photons, which for a power of 360 nW (the power used for the waveforms shown in Fig. 3-11) and a wavelength of 373 nm is 7×10^{11} photons per second. $\eta_{snspd} = 0.7$ and $r_{snspd} = 28$ μm are the SNSPD internal efficiency and radius, respectively.

$P_{int}(r)$ is the power contained in a circular aperture of radius r by a gaussian beam centered in the aperture, which is given by:

$$P_{int}(r) = P_{TOT} * (1 - e^{\frac{-2r^2}{w^2}}) \tag{3.3}$$
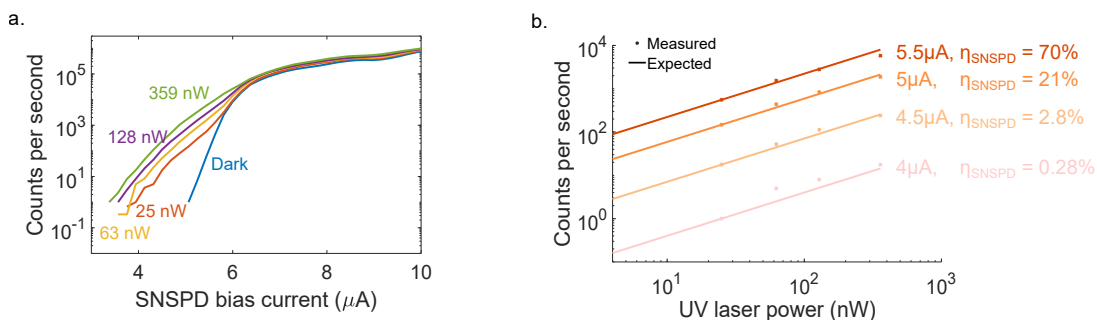
Figure 3-13: Optical readout counts. (a) Counts per second as a function of SNSPD bias and UV power hitting the SNSPD. Above 6.6 μA the SNSPD undergoes relaxation oscillations. (b) Counts per second as a function of the UV optical power hitting the SNSPD for 4 different bias currents. Dots show measured values, and lines show the expected value assuming a linear detector. Less counts are measured for lower bias currents due to a decrease in the SNSPD internal efficiency.

P_{TOT} is the total power of the gaussian beam, and w is the beam waist radius, which can be approximated as $w(d) = NA * d$. NA is the numerical aperture of the multimode fiber used to launch the UV light and d is the distance between the tip of the fiber and the SNSPD surface. In our case, NA=0.22 and $d \approx 2.5$ cm (see Fig. 3-7(d)).

$\eta_{misalignment}$ accounts for the misalignment between the center of the SNSPD and the center of the UV gaussian beam, which decreases the number of photons incident on the SNSPD. It is easy to show that $\eta_{misalignment}$ is given by:

$$\eta_{misalignment} = \frac{e^{\frac{-2r_0^2}{w^2}} \int_0^{r_{snspd}} \int_0^{2\pi} r \; exp(-2r^2/w^2)exp(4 \; r_0 \; r \; cos(\theta)/w^2) \, d\theta \, dr}{(\pi/2)w^2(1 - e^{\frac{-2r^2}{w^2}})} \qquad (3.4)$$

r_0 is the distance between the center of the gaussian beam and the center of the SNSPD.

Figure 3-14 plots Eq. 3.2 as a function of the misalignment between the UV beam and the SNSPD for the parameters corresponding to our experimental demonstration. If the SNSPD and the UV fiber were perfectly aligned, we would expect around 2.5×10^7 cps, or one count every 50 ns. It is clear by observing Fig. 3-11(a) that this is not the case for us. This is expected, since our assembly did not have a mechanism to optimize the alignment between the UV beam and the center of the SNSPD.

We can use the time traces recorded with the oscilloscope to estimate the number of photons impinging on the SNSPD, in which case we get about 10 counts every 60 μs, or about 2×10^5 cps (Fig. 3-11(a)). If we assume this is the number of photons hitting the SNSPD, we conclude that the UV laser beam and the SNSPD were misaligned by approximately 8 mm, which is plausible given our coarse relative

128
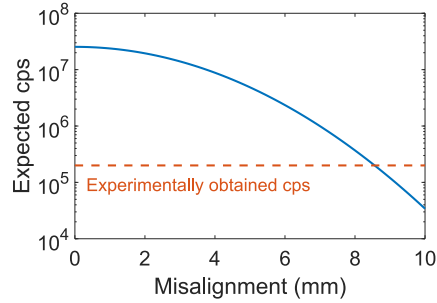
Figure 3-14: Counts per second of the optical readout system. Blue: Expected number of counts as a function of the misalignment between the center of the UV beam and the center of the SNSPD for an input UV power of 360 nW. Orange: inferred cps from the recorded oscilloscope traces.

positioning between the SNSPD and the lens tube.

Since we have an estimate for the number of photons incident on the SNSPD, we can easily calculate the pulse counting efficiency we obtained experimentally: a bias current of 5 μA gave around 2×10^3 cps (Fig. 3-13), which translates into an efficiency $\eta \approx 1\%$ for 2×10^5 photons per second incident on the SNSPD.

It is important to note that this is the counting efficiency for a given voltage threshold used at the pulse counter. The low SNR of the output signal (caused mainly by the 30 dB loss in the input-output optical coupling to the CMOS chip) made it necessary to set a higher voltage threshold for the pulse counter in order to avoid noise events to be counted as readout pulses, which causes certain fraction of real pulses (pulses corresponding to a photon detection event) to be missed and thus decreases the pulse counting efficiency. As will be discussed in a later section, improving the optical coupling would allow for a lower pulse counter threshold and thus a larger counting efficiency.

3.5.5 Comparison to state of the art

Power dissipation

The electrical power dissipation of our demonstration is dominated by the DC electrical power consumption, which was between 20 and 40 μW.

We can estimate the AC electrical power dissipation, since we know from our equivalent circuit simulations that the generated electrical driving signal is about 2 mV at the modulator terminals. The total AC power dissipation is given by:

$$P_{AC} = C * V_{AC}^2 * f + \frac{V_{AC,rms}^2}{r_{diode}} \tag{3.5}$$

The first term in the above equation is the power consumption associated with the charging and discharging of the modulator capacitance, and the second term that associated with the current flowing through the equivalent resistance of the diode. C corresponds to the input capacitance of the modulator, which is <200 pF from fitting to the experimental readout waveforms using our equivalent circuit model. V_{AC} ($V_{AC,rms}$) is the peak to peak (root mean square) amplitude of the AC signal, which is < 2 mV (< 1.4 mV$_{rms}$) in our case. f is the frequency at which readout pulses are generated, and r_{diode} is the equivalent resistance of the diode, which we know is around 100 Ω.

For a frequency $f = 1 \times 10^9$ readout pulses per second, the total AC power dissipation is < 0.8 μW, which is dominated by the energy needed to charge the capacitance (first term in Eq. 3.5). Thus, AC power consumption is two orders of magnitude lower than the DC power, which is 20-40 μW.

Unfortunately, estimating the optical power consumption of our readout is challenging due to the difficulty of accurately obtaining optical insertion losses. We can,

nevertheless, calculate an upper bound by assuming that all the input optical power is dissipated inside the cryostat (which, of course, is not true since there is an output signal!). With this, we can estimate the upper bound for optical power dissipation to be 1 mW.

Comparison to previous cryogenic readout demonstrations

Our readout approach presents two main differences compared to previous cryogenic readout demonstrations:

1. Due to the low input impedance of our modulator, no impedance matching technique is necessary, so direct delivery of the cryogenic electrical signal to the modulator is possible.

2. The high modulation efficiency obtained in forward bias eliminates the need for cryogenic amplification.

These key changes result in our readout demonstration, with a total electrical power consumption of 20-40 μW, to have at least an order of magnitude lower electrical power dissipation than any previous optical readout demonstration in the literature (Table 1.5).

With a 40 μW electrical power dissipation and a 1.5 GHz bandwidth, our readout energy dissipation is close to 25 fJ/bit, which is 100x smaller than any previous demonstration of cryogenic readout (Tables 1.4 and 1.5, and Fig. 3-16).

Comparison to previous cryogenic modulator demonstrations

The same key changes that make our optical readout better than any previous demonstrations apply when comparing to previous cryogenic modulators reported in the literature.

Our device could realize optical modulation with a 2 mV electrical signal, which is 1,000x lower than the voltage signals used to demonstrate cryogenic modulators reported in the literature (Table 1.6 and Fig. 3-16). While the bandwidth of our modulator is significantly lower due to the carrier lifetime limitation, our achieved electrical energy dissipation of 25 fJ/bit is the lowest amongst all cryogenic modulator reported to date.

Finally, unlike any other cryogenic modulator demonstration, our system was fiber packaged, eliminating the need for optical fiber alignment and manipulation in the cryogenic environment.

Summary

The work presented in this chapter is, to the best of the author's knowledge, the first demonstration of cryogenic optical readout through the use of an optical modulator. This work constitutes also a demonstration of the important advantages that forward biased operation of silicon modulators at cryogenic temperatures can provide for the realization of cryogenic optical readout.

With a bandwidth of 1.5 GHz (as we measured in Chapter 2), the modulator is fast enough to respond to the SNSPD signal, and faster than the 500 MHz bandwidth electrical amplifiers typically used in SNSPD readout [162, 163]. With a 40 μW electrical power dissipation and a 25 fJ/bit energy dissipation, our scheme presents 100x lower heat loads than typical cryogenic readout schemes.

Including optical (650 fJ/bit) and electrical (25 fJ/bit) energy, our readout has a total energy dissipation of 675 fJ/bit. This is close to the target we derived in Section 1.4.2 for a moderately demanding system, which was 450 fJ/bit. Clearly, the energy dissipation is dominated by the large input optical power needed to overcome

the high optical coupling losses, which as we will discuss in the next section, can be solved by using optimized grating couplers.

3.6 Potential for improved performance

Simple improvements in the optical coupling to the chip would allow for a substantial decrease in the optical power that was needed for this demonstration. As has been mentioned previously, the readout is limited by a low SNR, which is mainly due to the 30 dB insertion loss introduced by the optical coupling in and out of the CMOS chip.

These high losses are not intrinsic to the technology: grating couplers with $> 90\%$ efficiency have been demonstrated in zero change CMOS [141]. Thus, the use of optimized grating couplers would reduce insertion losses to about 3-5 dB after cooling down to cryogenic temperatures.

Energy dissipation

Reducing the optical loss by 25 dB would allow us to obtain the same output signal with 25 dB lower input optical power, from 1 mW to about 5 μW, which would decrease the optical energy dissipation from 650 fJ/bit to 3 fJ/bit. With this, the total energy dissipation of our readout would be close to 30 fJ/bit, enough to beat the 450 fJ/bit target for a moderately demanding cryogenic system.

Pulse counting efficiency

A decrease in the grating coupler loss would improve the readout in additional ways. First, it would decrease the heat load to the cryostat, reducing the operating temperature of the SNSPD and increasing its switching current from ≈ 7.5 μA to ≈ 9

μA (Fig. 3-10). Assuming a linear dependence between electrical signal and modulation depth, which is a good approximation given the small amplitude signals that develop in our system, the generated readout signal would increase by 20%. Second, a decrease in the optical coupling loss would eliminate the need for an input EDFA, which would increase the SNR of the readout signal by a factor equal to the Noise Figure of the amplifier, which in our case is specified to be > 6 dB.

Thus, the improvement in the optical coupling loss would result in a ≈ 7 dB increase in the SNR of the readout signal, which would allow for a much higher pulse counting efficiency of our optical readout. Because of the low SNR, our demonstration was mainly limited by the need to set the threshold for the pulse counter at a level far enough from the noise floor so as not to get any false count from noise events. As a consequence, a great part of the pulses corresponding to detected photons were actually not counted because they didn't overcome the pulse counter threshold.

Using measured data, we fit the noise to a gaussian distribution to estimate its variance and obtained the signal power by integrating a single readout pulse, which resulted in an SNR=1.83. Figure 3-15 shows the readout waveform we would obtain if there was no noise (orange), for the experimental SNR=1.83 (green) and for the SNR=10 we would obtain with improved optical coupling (purple). Clearly, an increase in the SNR would allow for a lower threshold for the pulse counter, which would increase the number of pulses detected and would result in a detection efficiency approaching that of the SNSPD, which is close to 70% for our detector.

Input impedance

As discussed previously, superconducting devices are not capable of driving high input impedance loads. For instance, SNSPDs typically drive an amplifier with a
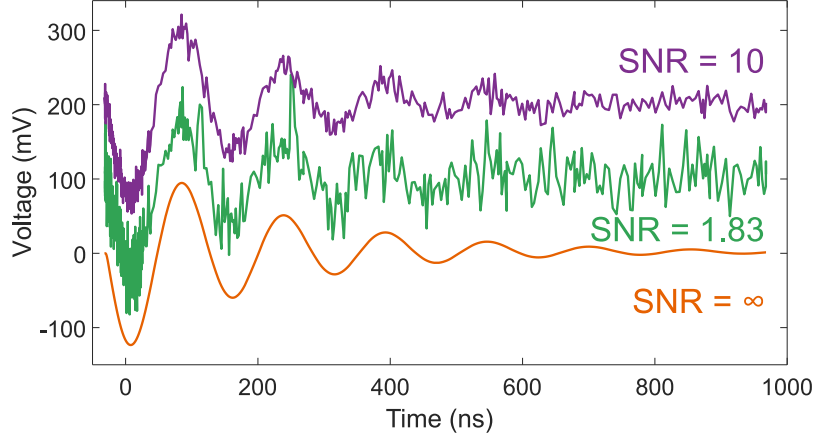
Figure 3-15: Readout waveforms for different SNR. Orange corresponds to SNR $=$ ∞, green to the experimentally obtained SNR of 1.83, and purple to the SNR of 10 attainable with improved optical coupling. Each waveform is offset 100 mV for ease of visualization.

50 Ω input impedance, but our modulator showed and input impedance of around 100 Ω. As a consequence, we added a passive reset branch to sink all the current still flowing through the SNSPD when in its normal state because of the impedance mismatch. This allowed the SNSPD to recover to the superconducting state, but at the expense of increased complexity and added parasitics, which reduced the speed of the optical readout system.

Nevertheless, the differential resistance of an ideal diode at 4 K biased with 40 μA is $r_d = kT/qI = 10$ Ω. Clearly, our demonstration is limited by the series resistance of the modulator, which comes mainly from the resistance of the quasi-neutral regions of the p-n junctions in the ring (we estimate the metal layers used for signal routing to have $R = 12$ Ω). Several techniques exist to reduce R_s in our device. For instance, we could reduce the width of the intrinsic regions in the T-junction design, or we could increase the doping of the p and n regions to compensate for the partial ionization at low operating temperatures.

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a.

b.
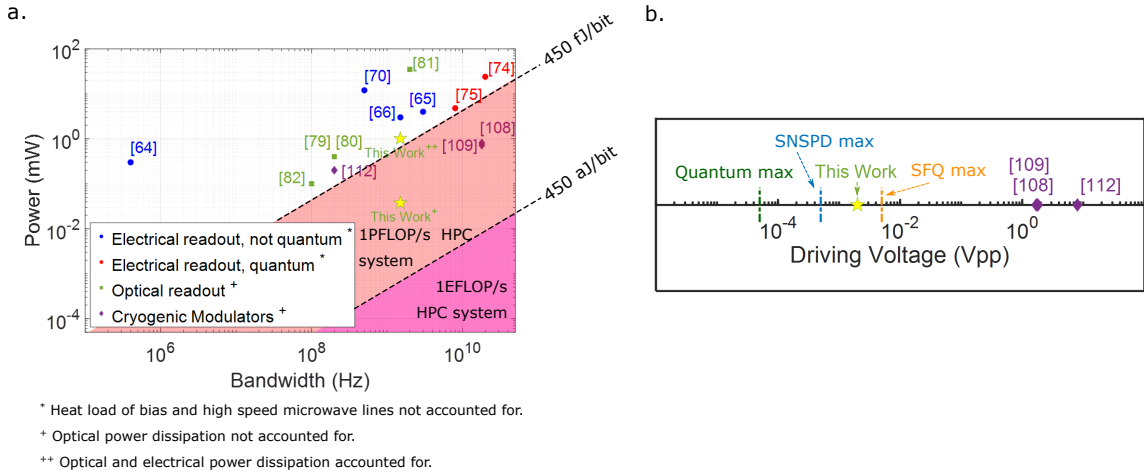
Figure 3-16: Comparison of the optical readout solution presented in this chapter with previously demonstrated cryogenic readout schemes. (a) Bandwidth and electrical power consumption. Our readout solution has the lowest power consumption of all cryogenic readout demonstrations reported in the literature. (b) Peak to peak voltage. Our modulator works with 2 orders of magnitude lower peak to peak voltages.

Notice how reducing the series resistance would not have a detrimental effect in the modulation depth, since the voltage drop through the p-n junction (which is the voltage that modulates the output signal) is still $V_{pn} \sim I_{SNSPD} \times r_d$, independent of the series resistance. On the other hand, reducing R_s would allow the modulator to present a much lower input impedance to the superconducting device, reducing the impedance mismatch and eliminating the need for a passive reset branch.

Thus, we can conclude that by optimizing the modulator to have negligible series resistance at cryogenic temperatures we could have achieved an input impedance of about 10 Ω ($\sim$ 20-30 Ω if accounting for the resistance of the metal lines) for the 40 μA bias current we demonstrated experimentally. This would have allowed us to eliminate the passive reset branch, reducing both parasitic effects and the system footprint. Furthermore, having a modulator with such low input impedance

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would allow for direct readout of superconducting devices with lower impedance than SNSPDs, such as SFQ circuits.

3.7 Conclusion

In this chapter we have demonstrated for the first time cryogenic optical readout through an optical modulator. By exploiting the advantages of forward bias operation that we described in Chapter 2, direct delivery of the signal generated by an SNSPD to the modulator was possible, and optical modulation was achieved with only 2 mV of electrical driving signal.

The total (electrical and optical) energy dissipation of 700 fJ/bit is the lowest ever demonstrated for cryogenic optical readout. The 25 fJ/bit electrical power dissipation of this demonstration is also 100x lower than typical cryogenic readout schemes, both electrical and optical. Figure 3-16 shows how our solution compares to the previous demonstrations of cryogenic readout and optical modulators presented in Chapter 1. Simple improvements to the optical coupling could result in a total (electrical and optical) power dissipation of 30 fJ/bit, which would be enough to fulfill the requirements for a 1PFLOP/s cryogenic system.

Chapter 4

Photovoltaic Operation of Optical Modulators

Throughout the last two chapters we have demonstrated how silicon photonic modulators operated in forward bias are a suitable candidate to realize scalable, low power cryogenic readout. Modulation efficiencies 50x-500x larger that these achievable in reverse bias are obtained, but at the cost of increased power dissipation due to the presence of a DC current flowing through the device ($P_{DC} = I_{DC}V_{DC}$).

In this section, we propose and characterize a modulation technique that eliminates this DC power dissipation, but simultaneously achieves large modulation efficiencies on the order of 10-20x larger than reverse bias operation. This is accomplished by leveraging the parasitic photocurrent present in optical modulators to achieve electrical gain.

While such operation does not feature as high a modulation efficiency as a forward biased modulator and has a limited bandwidth, it can reach electrical energy dissipations in the zJ/bit range, which makes it attractive for ultra-low power applications

such as cryogenic readout.

Most of the experimental characterization presented in this chapter was performed at room temperature, but we will also show preliminary results at cryogenic temperatures and argue why performance should be similar if not better.

4.1 Energy dissipation in optical modulators

Throughout the previous chapters we have briefly discussed the sources of energy dissipation in optical modulators. The purpose of this section is to formally introduce the different mechanisms that contribute to energy dissipation in these devices, which will prove useful in later sections. The reader is pointed to reference [164] for a more detailed discussion on this topic.

4.1.1 Electrical energy consumption

There are 2 sources of electrical power dissipation in optical modulators:

1. The energy associated with the charging and discharging of the device input capacitance C_{in}. Such energy is due to the dissipation coming from the flow of current through the series resistance in the circuit, and is given by:

$$E_C = \frac{1}{2}C_{in}V_{ac,pp}^2 \tag{4.1}$$

In the equation above, $V_{ac,pp}$ is the peak to peak voltage applied to the modulator terminals. Strictly speaking, capacitive charging has an additional energy dissipation associated with the bias voltage $E_{C,bias} = C_{in}V_{ac,pp}V_{bias}$, but it can

be easily recovered through the use of decoupling capacitors [164], so it won't be considered here.

Nevertheless, E_C is not the average energy dissipation per bit due to capacitive charging, since a real digital data pattern does not have a transition from '1' to '0' bit or viceversa at every bit time.

We can calculate the average energy consumption by noting that there are 4 possible 2-bit transitions in a digital pattern: 1 - 1, 0 - 0, 1 - 0, 0 - 1, and that these transitions are to a good approximation equally likely. The 1 - 1 and 0 - 0 transitions do not have an associated energy dissipation, while the 1 - 0 and 0 - 1 transitions incur in $E_C = \frac{1}{2}C_{in}V_{ac,pp}^2$. Since the probability of each transition is $1/4$, we conclude that the average energy dissipation is $E = 1/4 * 0 + 1/4 * 0 + 1/4 * E_C + 1/4 * E_C = \frac{1}{4}C_{in}V_{ac,pp}^2$ $[J/bit]$.

2. The energy associated with any DC bias current flowing through the device. The power dissipation associated with the bias point is given by $P_{DC} = I_{DC}V_{bias}$, and can be converted to energy per bit simply dividing by the signal data rate: $E_{DC} = I_{DC}V_{bias}/f_{data}$ $[J/bit]$.

   Notice how a reverse biased modulator has, in principle, a very low DC power dissipation since the DC current is close to 0. On the contrary, forward biased p-n and p-i-n junction modulators can have a significant DC current and, as a consequence, large DC energy dissipation.

   An important source of DC current that is usually overlooked in optical modulators is that associated with the photogenerated charges. The majority of optical modulators generate a photocurrent I_{PC} when light is input to the device due to desired (in the case of electroabsoprtion modulators) or parasitic (in

the case of electrorefraction modulators) absorption taking place in the device. Such photocurrent has an associated power dissipation due to the work done by the bias field on the photogenerated carriers $P_{PC} = I_{PC}V_{bias}$.

Since $I_{PC} < 0$, we can see how the application of a reverse bias voltage $V_{bias} < 0$ increases the energy dissipation. Interestingly, for a forward bias $V_{bias} > 0$ the power dissipation is negative, which means that the photogenerated charges do work on the system.

We can see how, essentially, a modulator with photogenerated current acts as a photovoltaic cell: if biased correctly, it can generate electrical energy. This is the basis of our photovoltaic modulation scheme, and we will come back to it and analyze it in detail in a later section. For now, the reader should have in mind that there is a mechanism for a modulator to generate energy, which is equivalent to energy harvesting in a photovoltaic cell.

Gathering all the terms presented above, we can write the total electrical energy dissipation for a generic optical modulator:

$$E_{el} = E_C + E_{DC} = \frac{1}{4}C_{in}V_{ac,pp}^2 + \frac{(I_{DC,op} + I_{PC})V_{bias}}{f_{data}} \ [J/bit] \qquad (4.2)$$

Where we have explicitly indicated the two contributions to the DC current flowing through the device: that associated with the bias of the device at a specific operating point ($I_{DC,op}$) and that associated with the photogenerated current (I_{PC}).

Clearly, our goal is to make the electrical energy dissipation as small as possible. In typical reverse biased modulators the main source of energy dissipation is capacitive charging, for which we want to minimize both the input capacitance of the device C_{in} and the necessary driving voltage $V_{ac,pp}$. For forward biased devices,

the presence of a current $I_{DC,op}$ makes operating at a bias point with low DC current critical. Photocurrent power dissipation can become important for electroabsoprtion modulators or devices with large reverse bias voltages.

4.1.2 Optical energy consumption

Optical modulators also have optical power dissipation associated with any optical losses occurring in the device. We discussed this in Section 1.4.2, and arrived at an optical power dissipation given by:

$$E_{opt} = \frac{\frac{1}{2}E_1 + \frac{1}{2}E_0}{f_{data}} = \left(\frac{1}{2}P_{in}(1 - IL) + \frac{1}{2}P_{in}(1 - \frac{IL}{ER})\right)/f_{data} \quad [J/bit] \qquad (4.3)$$

Above, E_1 (E_0) is the optical energy consumption for bit '1' (bit '0'), P_{in} is the input optical power to the modulator, and ER and IL are the extinction ratio and insertion loss of the modulation, respectively.

It is technically possible to recover the optical energy associated with the ER by adding a second output to the optical modulator: a 'drop' port in a ring configuration or an additional port at the output 3 dB coupler in a Mach-Zehnder configuration. While possible, this is not commonly done in practical systems, since there is no efficient way of reusing the recovered optical energy. We will, nonetheless, consider that such a scheme is possible and compute the total optical power dissipation in a modulator as:

$$E_{opt} = \frac{P_{in}(1 - IL)}{f_{data}} \quad [J/bit] \qquad (4.4)$$

It is obvious that minimizing optical power dissipation requires lowering both the

necessary input optical power to the device and the insertion loss introduced by the modulator.

4.1.3   State of the art

It is of interest to examine the power consumption in state of the art modulators (Tables 4.1 and 4.2). We can see how the majority of optical modulators demonstrated to date, both in silicon and in other material platforms, have associated electrical energy dissipations in the order of 1 fJ/bit. The exception are LiNbO$_3$ and plasmonic-organic hybrid modulators, which can achieve very low driving voltages due to the large electro-optic coefficients of the materials and consequently reduce the capacitive charging energy dissipation ($\propto V_{pp}^2$). Nevertheless, both material platforms suffer from scalability issues due to challenging fabrication and, in the case of organic modulators, material stability concerns.

On the contrary, and as we have discussed extensively in Chapter 1, optical modulators fabricated on a silicon platform offer excellent scalability and ease of integration with electronics, and are therefore highly desirable for low cost, large scale systems for the consumer market.

Nevertheless, and as shown in Table 4.1, Si modulators have not overcome the barrier of 1 fJ/bit electrical energy dissipation, and this is mainly because plasma dispersion, which as discussed is the physical effect used for modulation in Si, is relatively weak compared to other electro-optic effects (such as the Pockels effect used in LiNb or polymer based modulators). This results in the need of comparatively large driving signals on the order of 0.5 V, which set a lower bound on the electrical energy dissipation in these devices:

1. A high speed, state of the art traveling wave Mach-Zehnder modulator termi-

nated with a 50 Ω resistor and a 0.5 V_{pp} electrical signal already dissipates 10 fJ/bit at a 100 Gbps.

2. For resonant modulators, the fact that there is a minimum bent radius below which radiation losses are too large and result in poor performance sets a limit to how compact the device can be. Since device capacitance is closely related to device size, a limit in the minimum input capacitance exists. Practical devices are $> 10\ \mu\mathrm{m}^2$, which translates into input capacitances $C_{in} > 20$ fF.

   Disregarding any other source for electrical energy dissipation, a resonant modulator with $C_{in} = 20$ fF and $V_{pp} = 0.5$ V already dissipates 1.25 fJ/bit.

In this chapter, we present a Si modulator that is capable of breaking the 1 fJ/bit energy dissipation barrier. As we will discuss in detail below, we achieve this through (1) the addition of a nano-scale electrical switch at the input of the device, which lowers the input capacitance to $C_{in} < 1$fF; and (2) the achievement of electrical gain in the device, which allows us to decrease the necessary driving voltage to $V_{pp} < 50$ mV.

Silicon Modulators

Ref., Year	Structure	Electrical energy	Bandwidth	Eye diagram demonstrations				Input optical power on chip	Optical energy
				Speed	V_{pp}, V_{bias}	ER	IL*		
[99] 2014	MRR, reverse biased vertical p-n junction	0.9 fJ/bit	21 GHz	25 Gbps	0.5 V_{pp} V_{bias} NR	6.1 dB	1 dB	-1.75 dBm	5.5 fJ/bit
[165] 2016	MZM, reverse biased lateral p-n junction	30 fJ/bit	21 GHz	25 Gbps	0.1 V_{pp} -0.8 V_{bias}	6 dB	5 dB	12 dBm	433 fJ/bit
[166] 2009	MRR, forward biased lateral p-i-n junction	86 fJ/bit	NR	3 Gbps	0.5 V_{pp} 1.4 V_{bias}	NR	NR	-2.2 dBm	74 fJ/bit †
[167] 2014	MZM, vertical MOS capacitor	2 pJ/bit	NR	40 Gbps	1 V_{pp} 1.7 V_{bias}	8 dB	NR	NR	NR

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* Does not account for the losses associated with coupling the light into the chip.
† Assuming 2 dB IL.

Table 4.1: Lowest power silicon modulators of its kind reported in the literature, ordered from lowest to highest electrical energy dissipation. NR = Not reported. MRR = Micro-ring resonator. MZM = Mach-Zehnder Modulator.

Non-silicon Modulators

Ref., Year	Structure	Electrical energy	Bandwidth	Eye diagram demonstrations				Input Optical power on chip	Optical energy
				Speed	V_{pp}, V_{bias}	ER	IL*		
[168] 2018	LiNbO$_3$	37 aJ/bit	45 GHz	70 Gbps	60 mV$_{pp}$ V_{bias} NR	3.4e-3 BER	0.4 dB	8 dBm	200 aJ/bit
[169] 2019	Plasmonic Organic hybrid	70 aJ/bit	NR	50 Gbps	145 mV$_{pp}$ V_{bias} NR	2e-3 BER	11.2 dB	8 dBm	116 fJ/bit
[90] 2015	Electro-optic polymer	12 fJ/bit	NR	12.5 Gbps	300 mV$_{pp}$ V_{bias} NR	NR	6 dB	-0.25 dBm	56 fJ/bit
[92] 2018	Plasmonic	12 fJ/bit	> 100 GHz	72 Gbps	3.3 V_{pp} V_{bias} NR	1e-3 BER	2.5 dB	-3 dBm	3 fJ/bit
[170] 2012	InP	43 fJ/bit	NR	10 Gbps	1.62 V_{pp} -1.6 V_{bias}	2.2 dB	NR	-10 dBm	3.7 fJ/bit [†]
[171] 2012	SiGe	240 fJ/bit	40 GHz	28 Gbps	2.8 V_{pp} 1.4 V_{bias}	5.9 dB	4 dB	NR	NR
[172] 2012	graphene	350 fJ/bit	5.9 GHz	10 Gbps	2.5 V_{pp} 1.75 V_{bias}	2.3 dB	3.8 dB	NR	NR

* Does not account for the losses associated with coupling the light into the chip.
† Assuming 2 dB IL.

Table 4.2: Lowest power non-silicon modulators of its kind reported in the literature, ordered from lowest to highest electrical energy dissipation. NR = Not reported.

4.2 Photovoltaic modulator: Operational principle

The operational principle of the photovoltaic (PV) modulator is best understood when compared to that of a typical modulator (Fig. 4-1).

In a typical modulator (left column in Fig. 4-1), a driver delivers the electrical signal to the modulator input. As we discussed in Section 4.1, and assuming a modulator with no DC operating current ($I_{DC,op}=0$), such scheme has two main energy dissipation sources: (1) that associated with the capacitive charging of the modulator input capacitance C_{MOD}; and (2) that associated with the photocurrent generated in the device. Thus, the average electrical energy dissipation is given by:

$$E_{typ} = \frac{1}{4}C_{MOD}V_{pp,typ}^2 + \frac{I_{PC}V_{bias}}{f_{data}} \tag{4.5}$$

In a PV modulator (right column in Fig. 4-1), a voltage controlled switch is added before the optical modulator. Turning on and off the switch allows us to change the voltage at the modulator terminals: when the switch is in the open circuit state (Fig. 4-1(b)), the voltage at the modulator becomes the open circuit voltage of the photovoltaic cell [1], while when the switch is in the short circuit state, the voltage at the modulator terminals is 0 (Fig. 4-1(d)).

Notice how, in this configuration, the external source only needs to provide the energy necessary to charge and discharge the input capacitance of the switch C_{SW}. The modulator capacitance C_{MOD} is self-charged through the photocurrent generated in the device (Fig. 4-1(b)), and the bias source does not need to provide energy to the photogenerated charges (as happens in conventional modulators).

The reader might be wondering how do we realize this voltage controlled switch.

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[1]The photovoltaic cell which we are referring to is the optical modulator itself. As we will discuss in great detail later, optical modulators generate a photocurrent when light is input to the device.
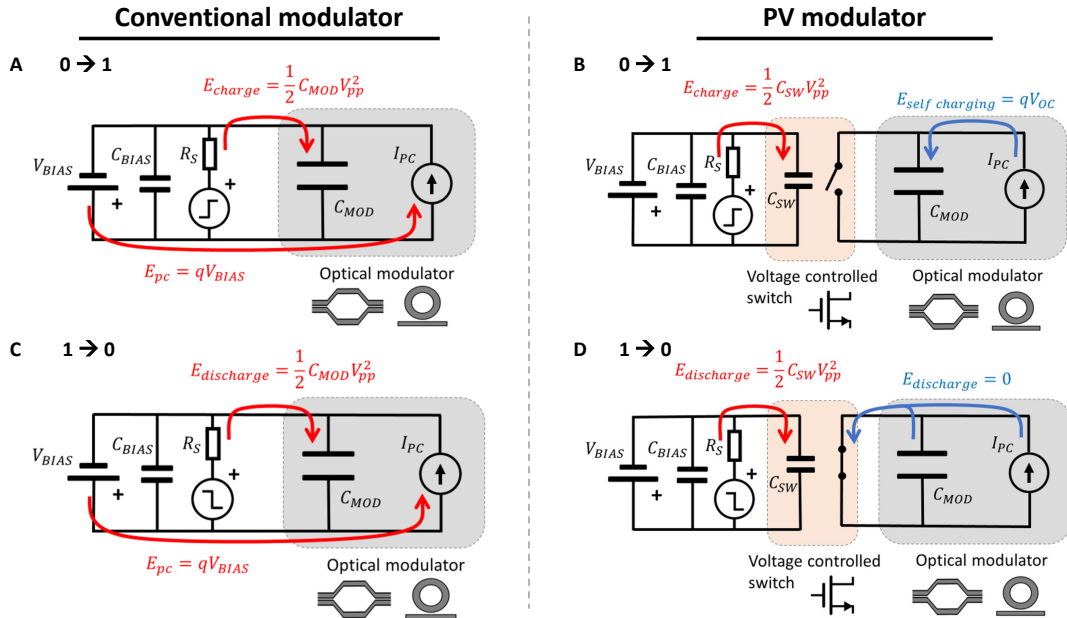
Figure 4-1: Energy dissipation in the charging and discharging of typical (left) and photovoltaic (right) modulators. (a, c) When charging (discharging) a conventional modulator, the driving source dissipates the energy needed to charge (discharge) the modulator capacitance and that associated with the photocurrent generated in the device. (b) When the PV modulator is charged, the source provides the energy needed to charge the switch capacitance. The modulator capacitance is self-charged to the open circuit voltage V_{oc} via the photocurrent. (d) When the PV modulator is discharged, the source provides the energy needed to discharge the switch capacitance. The charge stored in the modulator is shunted through the switch.

The answer is simple: a transistor. By applying a voltage to the transistor gate, we can control the current flowing between the source and drain. The first advantage of the PV modulator should now become apparent: the voltage controlled switch is a transistor, which is a nano-scale device, and as such has a much smaller input capacitance than the micron-scale modulator. Consequently, in the PV modulator the external source has to drive the gate capacitance of a transistor (typical gate capacitances of modern transistors are in the range of $C_{SW} \approx 0.1$ - 1 fF), whereas in

a conventional modulator it needs to drive the modulator capacitance itself ($C_{MOD} \approx$ 20 fF for typical reverse biased silicon modulators).

The average energy dissipation in a PV modulator is then given by:

$$E_{PV} = \frac{1}{4} C_{SW} V_{pp,PV}^2 \qquad (4.6)$$

Comparing the equation above to Eq. 4.5 for a conventional modulator, we achieve a 20-100x reduction in energy dissipation due to the smaller C_{SW}.

It is worth noting how the ability to monolithically integrate electronic and photonic components - which is immediate in our zero-change CMOS photonic platform - is essential to realize a PV modulator. It allows us to place the transistor very close to the optical modulator, avoiding electrical losses and parasitic effects that would be present in a non-monolithic approach [28].

The reduction in input capacitance is not the only advantage of our scheme. The PV modulator configuration allows us to achieve voltage gain, that is, the voltage swing at the modulator terminals can be larger than that applied at the input of the transistor. This means that a PV modulator needs lower input driving voltages than a conventional modulator ($V_{pp,PV} < V_{pp,typ}$), which translates into a further reduction in electrical energy dissipation. To understand how voltage gain is achieved, it is useful to look at the small signal model of the PV modulator, which we will discuss in the next section.

4.2.1 Small signal picture

In the previous section we have discussed the operational principle of the PV modulator from a large signal picture (Fig. 4-2(a)): by switching the current flowing through the source and drain of the transistor I_{SW} between 0 and I_{pc}, we can change

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Large signal model   **Small signal model**

a.   b.
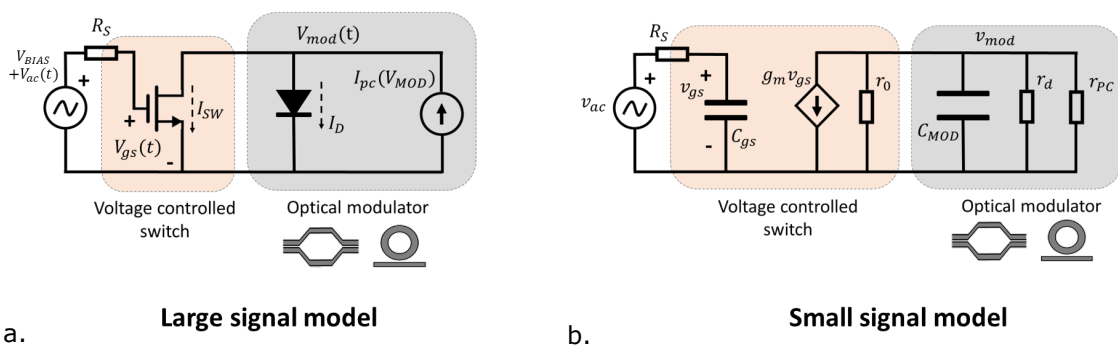
Figure 4-2: PV modulator equivalent circuit models. (a) Large signal model. (b) Small signal model. The small signal model corresponds to that of an amplifier with the load resistance being the dynamic resistance of the modulator r_d.

the voltage at the modulator terminals V_{mod} between V_{OC} and 0, respectively. Nevertheless, switching the transistor on and off requires a relatively large voltage swing in the range of the transistor threshold voltage $V_{th} \approx 0.6$ V.

As we have discussed previously, cryogenic technologies can't generate such large driving signals, so we need to explore the behavior of the PV modulator for small input voltage signals in the order of mV or lower. We can do this by looking at the small signal equivalent model, shown in Fig. 4-2(b). All the circuit components correspond to the standard equivalent circuit model for a transistor and a diode [2] with the exception of $r_{pc} = (dI_{pc}/dV_{mod})^{-1}$, which accounts for the change in the generated photocurrent with the voltage applied to the modulator. This can become important in resonant modulators, where a change in the voltage at the modulator terminals changes its resonance frequency and as a consequence the amount of light coupled into the ring, which in turn affects the generated photocurrent (see Appendix C).

The reader might recognize the resulting circuit, since it corresponds to the small signal model of a simple common source amplifier [173] with the diode as the load.

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[2]The reader is pointed to reference [142] for the derivation and discussion of the small signal equivalent model for a transistor and a diode.

Analysis of the circuit at low frequencies yields the following expression for the signal gain:

$$A_{vd} = \frac{v_{mod}}{v_{gs}} = g_m \left(r_0||r_d||r_{pc}\right) \tag{4.7}$$

Assuming $r_0 \ll r_d, r_{pc}$, which we will see later is a valid assumption, we can simplify the above expression to $A_{vd} = g_m r_0$. This is know as the intrinsic gain of a transistor [173], and while it depends strongly on the technology node and the bias point, it is on the order of 10 for modern transistors.

We can see how the PV modulator configuration acts essentially as a common source amplifier that amplifies the input electrical driving signal, resulting in a larger driving signal at the modulator terminals. What is interesting from such a configuration is that this amplifier is self-powered: the energy needed to bias the transistor at a point where gain is achieved is given by the photocurrent generated in the modulator. On the contrary, in a conventional common source amplifier the bias current is provided by an external voltage source at a voltage V_{DD} [173], which has an associated power dissipation $V_{DD}I_{bias}$.

The second source of reduction in energy dissipation in PV modulators should now become clear: the necessary peak to peak voltage that needs to be provided by the driver is A_{vd} times lower than in typical modulation schemes, since in the PV scheme $V_{mod,pp} = A_{vd}V_{in,pp}$. Assuming a gain of 10 (which we will see later is achievable experimentally), we need $V_{pp,PV} \approx V_{pp,typ}/10$ to achieve the same modulation strength, which yields a 100x reduction in power dissipation (since $E \propto V_{pp}^2$).

Thus, combining the 10-100x reduction in power dissipation coming from a decrease in input capacitance and the 100x reduction due to the decrease in driving voltage, the PV modulator offers a 1,000-10,000x reduction in electrical energy dissi-

pation compared to conventional modulators. Such a gain is obtained by leveraging the photogenerated current in the optical modulator due to parasitic absorption, which provides the energy needed to achieve gain in the transistor.

4.2.2   Is photogenerated current universal?

Notice how in our analysis we have not made any assumption about the optical modulator being used. This is because the PV modulator concept applies to any optical modulator (regardless of material platform, structure, operational principle) that can act as a photovoltaic cell, i.e, that generates a photocurrent and develops a photovoltage when light is input to the device. The source of this photocurrent, either intentional or due to parasitic effects, is irrelevant for the operation of the device.

Thus, to study the applicability of our PV modulator scheme it is necessary to study how universal is the generation of photocurrent in modern optical modulators in general, and in modern silicon modulators in particular.

The presence of photocurrent in electroabsorption modulators is obvious, since these achieve modulation by the absorption of the input optical power when a '0' bit is transmitted, which generates electron-hole pairs in the device and a current as a result.

On the contrary, there is in principle no reason why electro-refraction modulators should generate a photocurrent, since they rely on the change in refractive index with applied voltage and not on absorption mechanisms. In particular, Si modulators typically operate at wavelengths well below its bandgap (1300 nm and 1550 nm are the most common operating wavelengths), therefore linear optical absorption resulting in photogenerated current should be almost non existent.

IR absorption in silicon waveguides

There exist, nevertheless, several physical mechanisms in Si allowing for absorption of light with energy below the bandgap resulting in significant photocurrents [174]. In fact, several approaches exploiting these effects for power monitoring [175, 176], stabilization of microring resonators [177] and realization of photodetectors [178] have been reported in the literature.

Three different mechanisms contribute to photocurrent generation in Si optical waveguides:

1. Defect Mid-Bandgap Absorption (DMBA), which is due to the presence of crystalline defects or foreign atoms in the bulk of the Si waveguide, which break the crystal periodicity and generate states with energy levels within the bandgap. By intentionally adding defects into a silicon waveguide through ion implantation, mid-IR photodetectors with responsivities as high as 0.8 A/W over a wavelength range from 1270 nm to 1700 nm have been realized [179].

2. Surface State Absorption (SSA). The termination of the crystal structure at the surface of a semiconductor distorts its band structure and creates intra-gap states [180], which can then result in sub-bandgap light absorption. Such effect has been reported, characterized and exploited in standard silicon photonic waveguides [181–183].

3. Two photon Absorption (TPA), where the simultaneous absorption of two photons results in the generation of an electron-hole pair. Being a nonlinear effect, TPA becomes important at high input optical powers or in resonant structures, as we will discuss in detail in Chapter 5.
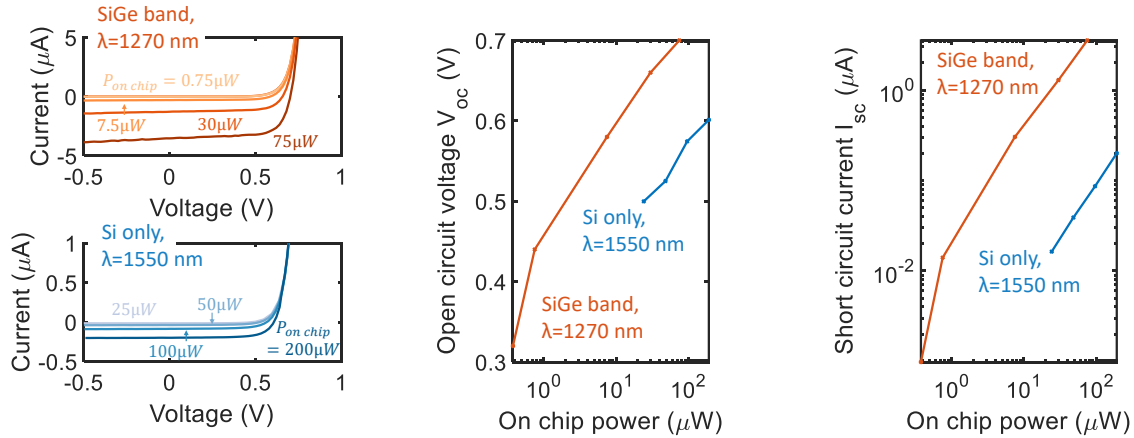
Figure 4-3: Photocurrent in Si optical modulators. (a) IV curves, (b) open circuit voltage and (c) short circuit current under different on-chip input optical powers. Blue shaded curves correspond to a Si-only modulator operating at 1550 nm (design *C* in Chapter 2) and orange curves to a modulator with a SiGe band operating at 1270 nm (design *O-Z* in Chapter 2).

At moderate input optical powers, SSA is believed to be the dominant photocurrent generation mechanism in modern silicon photonic waveguides over DMBA. This is because the high quality of the fabrication process results in a low density of defects in the bulk of the Si waveguide, and thus reduced DMBA. Two main factors dominate the strength of SSA in optical waveguides: (1) The overlap of the optical mode with the silicon surface, and (2) the quality of the surface passivation [184]. SSA does not show a strong wavelength dependence in the wavelength ranges of interest [185, 186].

Besides absorption mechanisms intrinsic to the silicon waveguide, another approach for photocurrent generation is the addition of other materials with a smaller bandgap such as germanium (Ge), which usually requires the use of modified silicon photonic processes since pure Ge is not a standard layer in CMOS foundries. Nonetheless, SiGe is used in standard CMOS to strain the channel of pFET tran-

sistors, which can be used to increase optical absorption in our zero change CMOS platform [187]. It is important to note that this is only possible for O band wavelengths and below, since the absorption edge of SiGe alloys is near 1300 nm [188].

Figure 4-3 shows measured photovoltaic responses (IV curves, open circuit voltages and short circuit currents) as a function of input optical power in the waveguide for two of our CMOS resonant modulator. Blue curves correspond to a Si only device (design C in Chapter 2) where photocurrent generation is primarily due to SSA. Orange curves show the response for the silicon resonator incorporating a SiGe band (design O-Z in Chapter 2). As expected, the addition of SiGe increases the generated photocurrent for a given input power, resulting in open circuit voltages above 0.5 V and photogenerated currents on the order of 1 μA for small input optical powers on the order of 10 μW.

We expect, then, photogenerated current to be present in most modern optical modulators in general, and in Si modulators in particular.

Estimating photocurrent generation in state of the art silicon modulators due to SSA

As mentioned above, several approaches exploiting SSA for optical power monitoring in integrated silicon devices have been reported in the literature. We can use these works to estimate the SSA-generated photocurrent in the high performance Si modulators in Table 4.1.

We selected the publications employing the most similar fabrication techniques and device geometries as the modulators in Table 4.1, and derived an approximate value for the photocurrent generating SSA absorption parameter α_{SSA} using the same approach as in Appendix B. These are shown in Table 4.3, where we can see

Ref.	Structure	R	η	α_{SSA}
[189]	Straight Si waveguide with air cladding, 500 x 100 nm cross section	36 mA/W (low input power)	2.8 %	19 m^{-1}
		1.5 mA/W (high input power)	0.12 %	0.8 m^{-1}
[183]	Straight SOI waveguide, 450 x 220 nm cross section	—	—	1.9 m^{-1}
[190]	MRR, lateral p-n junction in SOI waveguide, 500 x 200 nm cross section	1 mA/W	0.08 %	2.22 m^{-1}

Table 4.3: Estimated Surface State Absorption (SSA) coefficient α_{SSA} in silicon photonic waveguides from published works. MRR = Micro-ring resonator.

how values for α_{SSA} are reasonably consistent over published works. A conservative estimate seems to be $\alpha_{SSA} = 1$ m^{-1}, which translates into a loss of 0.04 dB/cm.

Using this value for α_{SSA}, we can get an estimate for the responsivity of the modulators in Table 4.1 from the reported device geometries and Q factors (in the case of resonant devices) using the same approach as in Appendix B [3]. The extracted responsivity values are shown in Table 4.4, along with the photocurrent and associated DC energy dissipation for the input optical powers that were used to experimentally characterize the devices. Responsivities around 1 mA/W and photocurrents close to 1 μA are reached. As shown, the energy dissipation associated with the photocurrent is on the order of a few percent of the total electrical power consumption.

It is worth noting that the value of R $\approx$ 1 mA/W we derived from literature values is consistent with the responsivity we measured for our Si-only, zero-change CMOS modulator for 1550 nm operation (design C in Chapter 2), which is 0.85 mA/W (see Fig. 4-3(c)).

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[3]Basically, we can estimate the quantum efficiency as $\eta = 1 - exp(-\alpha_{SSA}L_{eff})$. For Mach-Zehnder modulators, L_{eff} corresponds to the device length L. In the case of resonant devices, $L_{eff} = F * L/2\pi$, where F is the Finnesse of the resonance.

Ref., Year	Structure	Responsivity	$P_{in,opt}$	I_{PC}	V_{bias}	E_{DC} @ f	$E_{DC}/E_{el,TOT}$
[99] 2014	MRR, reverse biased vertical p-n junction	1 mA/W	-1.75 dBm	0.66 μA	- 1 V [*]	25 aJ/bit @ 25 Gbps	2.25 %
[165] 2016	MZM, reverse biased lateral p-n junction	3.75 mA/W	12 dBm	60 μA	- 0.8 V	2 fJ/bit @ 25 Gbps	6.25 %
[166] 2009	MRR, forward biased lateral p-i-n junction	1 mA/W	-2.2 dBm	0.6 μA	1.4 V	- 280 aJ/bit @ 3 Gbps	0.32 %

[*] Estimated.

Table 4.4: Surface State Absorption (SSA) photocurrent generation in state of the art silicon modulators. The last column shows the percentage of the total electrical power consumption that is due to photocurrent. More information on these modualtors is shown in Table 4.1. MRR = Micro-ring resonator. MZM = Mach-Zehnder modulator.

4.2.3 Recap

In the sections above we have presented a new scheme for optical modulation, which we call a PV modulator, that relies on the photocurrent generated in the optical modulator to self-power a transistor acting as an amplifier.

We have discussed how such a scheme allows for a $> 1,000x$ reduction in electrical power dissipation compared to conventional modulation, coming from (1) a decrease in the input capacitance of the device, which is now that of the gate of a transistor and (2) the achievement of electrical gain by using the transistor in a common source configuration and biasing it with the photogenerated current.

Our PV modulation approach only relies on the presence of a photocurrent, which we have shown is ubiquitous in most modern silicon optical modulators.

It is important to note that the existence of an operating regime in optical modulators that could allow for power generation by exploiting the photovoltaic effect has been previously recognized [164, 191]. Nevertheless, an efficient method to harvest the generated power was not proposed nor realized. In contrast, our PV modulation is able to use the photogenerated current to achieve voltage gain in the transistor.

4.3 Device simulation

Understanding the different performance tradeoffs in the PV modulator architecture is essential for the design and optimization of the device. With this purpose, we simulated the equivalent circuit model shown in Fig. 4-2(a) using Cadence [192].

The SPICE model for the transistor was provided in the Process Design Kit (PDK) of the CMOS process we use to fabricate our devices (GlobalFoundries 45 nm RF SOI). For the modulator we used the standard SPICE diode model [193],

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Parameter	Description	Value	Extracted from
I_s	Reverse saturation current	$1.81 \cdot 10^{-12}$ A	Fit to IV curve
R_s	Series resistance	0.5 Ω	Fit to IV curve
n	Ideality factor	1.92	IV curve
C_{j0}	Zero bias junction capacitance	20 fF	Parasitic extraction from layout
V_j	Junction potential	0.95 V	Estimated from doping concentrations of p and n regions
m	Grading coefficient	0.4	—
TT	Transit time	45 ns	Fit to falling edge of modulation waveform in forward bias conditions
R [†]	Responsivity	0.034 A/W	Photocurrent vs input power (Fig. 4-3(c))

[†] This is not a SPICE diode model parameter.

Table 4.5: Spice diode model parameters used to describe the modulator electrical behavior.

and the corresponding parameters were obtained from fitting to experimental data taken on the SiGe band modulator for 1270 nm operating wavelength (design *O-Z* in Chapter 2). Table 4.5 shows the model parameters used in the simulation, along with a brief note on how they were obtained. Default values were used for the parameters not specified in Table 4.5.

To model the generated photocurrent in the modulator as a function of input optical power we extracted the modulator responsivity using the data in Fig. 4-3(c), which yields R = 0.034 A/W. As mentioned earlier, this is higher than the 0.001 A/W we estimated for Si-only modulators because the addition of SiGe increases optical absorption at wavelengths around 1280 nm due to phonon-assisted indirect electronic transitions [188].

4.3.1 DC characterization

Figure 4-4 shows the DC operating point characterization of the device. Figure 4-4(a) shows the voltage at the modulator terminals V_{mod} as a function of the bias voltage at the transistor gate V_{gs} [4] for different generated photocurrents I_{pc}, i.e, different input optical powers. Figure 4-4(b) shows the currents flowing through the modulator (solid lines) and the transistor (dashed lines) for the same photocurrents as in Fig. 4-4(a).

Clearly, a change in the voltage applied to the gate of the transistor is accompanied by a change in the voltage at the modulator terminals. Specifically, we see how the voltage at the modulator switches from the open circuit voltage of the PV cell V_{oc} for low V_{gs}, to 0 as we increase the gate voltage. The reason for this is easily visualized when looking at Fig. 4-4(b). For low gate voltages, the transistor is turned off ($V_{gs} < V_{th}$, where V_{th} is the transistor threshold voltage), so there is no current flowing through the switch, $I_{sw} \approx 0$ (gray shaded area in Fig. 4-4(b)). As a consequence, all the photocurrent I_{pc} flows through the diode, which develops a voltage corresponding to the open circuit voltage V_{oc} (gray shaded area in Fig. 4-4(a)). When the gate voltage is above the transistor threshold voltage ($V_{gs} > V_{th}$), the transistor turns on and becomes essentially a short circuit, so all the photocurrent flows through the switch and none through the modulator diode (blue shaded area in Fig. 4-4(b)). Since the transistor becomes a short circuit, the voltage at the modulator terminals is close to 0 (blue shaded area in Fig. 4-4(a)).

From figure 4-4(a), it is clear that the PV modulator has a maximum achievable voltage swing at the modulator terminals which corresponds to the open circuit voltage of the modulator V_{oc}: no matter how large is the voltage swing at the

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[4] We follow the terminology show in Fig. 4-2 for the different node voltages.
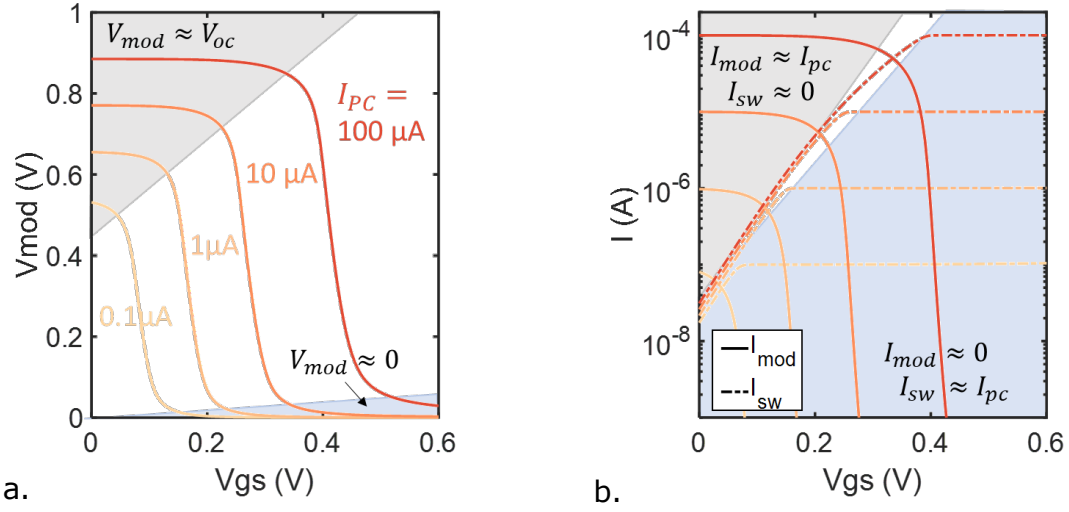
Figure 4-4: PV modulator operating point. (a) Voltage at the modulator terminals as a function of the gate voltage for different generated photocurrents. (b) Currents flowing through the modulator (solid lines) and the transistor (dashed lines) for the same photocurrents as in (a). The transistion between open circuit and short circuit conditions as the gate voltage increases is clearly visible.

transistor gate ΔV_{gs}, the maximum voltage swing at the modulator will be that corresponding to the difference between the open circuit and short circuit conditions $\Delta V_{mod,max} = V_{oc} - V_{sc} = V_{oc} - 0 = V_{oc}$. This is important, because it means that there is a maximum resonance shift we can achieve in a PV modulator which depends mainly on the generated photocurrent (as I_{pc} sets the value of V_{oc}, Fig. 4-4(a)).

Small signal gain

As we discussed in Section 4.2.1, the PV modulator configuration can achieve electrical gain for certain bias conditions. This is readily observable in Fig. 4-4(a): in the transition between the open circuit and short circuit conditions (non-shaded region in Fig. 4-4(a)), a change in V_{gs} results in a larger magnitude change in V_{mod}, resulting in electrical gain.

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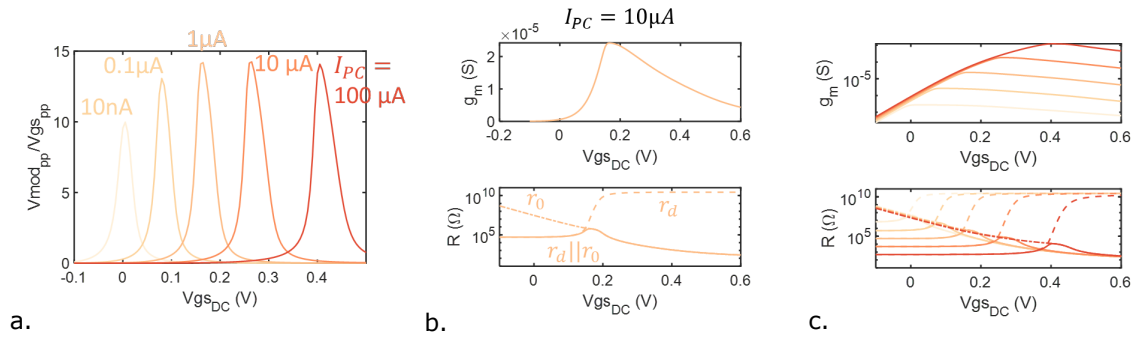
Figure 4-5: PV modulator DC gain. (a) Gain as a function of the bias applied to the transistor gate for different generated photocurrents. (b) Evolution of the transistor g_m (top) and the relevant resistances in the circuit (bottom) as a function of gate bias for a 1 μA photocurrent. (c) Evolution of the transistor g_m (top) and the relevant resistances in the circuit (bottom) as a function of gate bias for the same generated photocurrents as in (a). As photocurrent increases, g_m increases and r_0 decreases, resulting in a similar small signal gain $g_m r_0$.

We obtained the small signal gain of the PV modulator configuration simulating the equivalent circuit model, and the results are shown in Fig. 4-5. Fig. 4-5(a) shows the small signal gain as a function of the bias applied to the transistor gate for different photocurrents. Interestingly, small signals gains above 10 can be obtained regardless of photocurrent when the device is correctly biased.

As we discussed in Section 4.2.1, the small signal gain of the PV configuration is given by $A_{vd} = g_m(r_0||r_d||r_{pc}) \approx g_m(r_0||r_d)$, where we have approximated $r_{pc} = dV_{mod}/dI_{pc} \approx \infty$, i.e, the generated photocurrent does not depend strongly on the modulator bias voltage (see Appendix C for a discussion on the effects of r_{pc}). It is therefore of interest to study the evolution of g_m (the transistor transconductance $g_m = dI_{ds}/dV_{gs}$) , r_0 (the output resistance of the transistor $r_0 = dV_{ds}/dI_{ds}$) and r_d (the dynamic resistance of the diode $r_d = dV_{mod}/dI_{mod}$) with bias voltage.

This is shown in Fig. 4-5(b) for a fixed photocurrent $I_{PC} = 1$ μA. $g_m \propto I_{DS} = I_{sw}$ [173], so an increase in g_m is observed as V_{gs} rises due to the fact that a larger current

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is flowing though the transistor (Fig. 4-4(b)). For large values of V_{gs}, channel length modulation (CLM) effects (the dependence of the transistor channel length on the drain-source voltage $V_{DS} = V_{mod}$ in our circuit) become important and g_m decreases as a consequence. Since $r_0 \propto I_{DS} = I_{sw}$, a decrease is observed with increasing V_{gs} because of the rise in the current flowing through the transistor. The diode resistance $r_d \propto 1/I_{mod}$ follows the opposite trend: an increase in r_d is observed with increasing V_{gs}, which is explained because the current flowing through the diode decreases as V_{gs} rises (Fig. 4-4(b)). As a consequence, the equivalent resistance at the modulator terminals $r_d||r_0$ is dominated by r_d at low values of V_{gs}, and by r_0 for large V_{gs}, as can be seen in the bottom plot of Fig. 4-5(b).

It is also important to note that $r_d||r_0 \approx r_0$ at the bias point which yields the larger small signal gain. Therefore, the maximum achievable gain is $A_{vd,max} \approx g_m r_0$, which depends solely on the transistor parameters and is usually referred to as the intrinsic gain of a transistor [173].

Fig. 4-5(c) shows the evolution of g_m and the resistances for different generated photocurrents. A general trend can be observed: as photocurrent increases, the peak g_m increases and the resistance at the maximum transconductance point $r_0||r_d \approx r_0$ decreases, such that $A_{vd,max} \approx g_m r_0$ is approximately independent of photocurrent. This explains why the small signal gain is not strongly dependent on I_{pc} (as observed in Fig. 4-5(c)).

Summarizing, we have confirmed that the PV modulator can generate electrical gain when appropriately biased. At the optimal bias, the gain corresponds to the intrinsic gain of the transistor $A_{vd} \approx g_m r_0$, which can be as high as 14 for our technology node. Moreover, we have observed how the small signal gain is independent of I_{PC}, which means that large gains can be obtained even for low photocurrents.

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4.3.2 RF characterization

The characterization of the device performance is not complete without analyzing its frequency response. Figure 4-6(a) shows the frequency response for different generated photocurrents when the device is biased at the voltage that gives the maximum electrical gain $V_{mod,pp}/V_{gs,pp}$.

Interestingly, a faster response is obtained for larger photocurrents. By looking at Fig. 4-2(b), it is clear that the device speed is limited by the RC time constant at the modulator terminals, which is simply $\tau = (C_{mod} + C_{ds})(r_0||r_d||r_{pc})$. From the PDK model, the transistor output capacitance C_{ds} is on the order of 10^{-18} F, so we can approximate $C_{mod} + C_{ds} \approx C_{mod}$, and as we already discussed, $r_0||r_d||r_{pc} \approx r_0||r_d$. Therefore, we are left with $\tau = C_{mod}(r_0||r_d)$.

The evolution of τ, C_{mod}, r_0 and r_d with photocurrent is shown in Fig. 4-6(b). We can see how τ decreases as photocurrent increases, which explains why we get a faster frequency response with a larger photocurrent. Clearly, the decrease in τ comes from the decrease in the node resistance, which is dominated by r_0 [5]. The decrease in r_0 is due to the rise in the transistor current at the maximum gain point with increasing photocurrent ($I_{PC} \uparrow \rightarrow I_{sw,max\_gain} \uparrow$, and $r_0 \propto 1/I_{sw}$).

Independent of the value of I_{pc}, the device has a limited speed with a 3 dB bandwidth lower than 200 MHz, mainly caused by the large r_0 of the transistor, which is in the order of MΩ.

It is of interest to explore the possibility to decrease the output resistance r_0 to improve the frequency response of the device. The output resistance of the transistor is given by:

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[5]Note this is expected, since in the previous section we observed that at the maximum gain point, $r_0||r_d \approx r_0$.
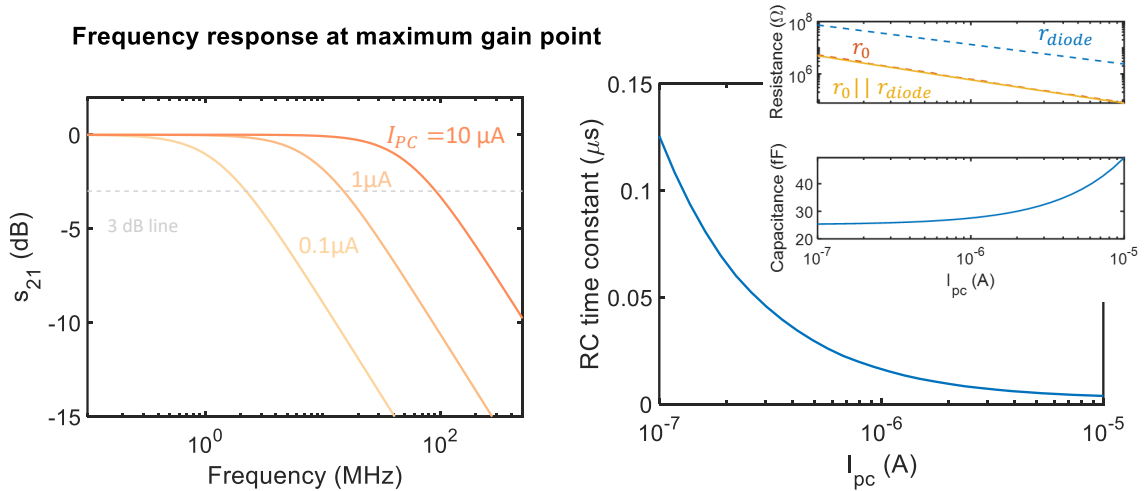
Figure 4-6: PV modulator frequency response at the maximum gain point. (a) Frequency response for different generated photocurrents. (b) RC time constant of the system as a function of photocurrent. The inset shows the evolution of the device resistance (top) and capacitance (bottom) with photocurrent. For both (a) and (b), the values correspond to the the device being biased at the point where the maximum electrical gain is obtained.

$$r_0 = \frac{1}{\lambda I_{DS}} \tag{4.8}$$

Above, I_{DS} is the current flowing through the transistor (which corresponds to I_{sw} in our schematic), and λ is know as the channel length modulation parameter, which depends mostly on intrinsic technology parameters [6]. This means that, unfortunately, there is no design approach that can reduce the value of r_0 for a given I_{sw}, which points to the conclusion that the bandwidth limitation is intrinsic to the PV modulator.

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[6] $\lambda \propto \sqrt{t_{ox}X_j}/L$, where t_{ox} is the gate oxide thickness, L is the gate length and X_j is the drain junction depth. [173]

Gain-bandwidth tradeoff

While the bandwidth at the maximum gain point is limited, there is a clear gain-bandwidth tradeoff in the PV modulator: a larger r_0 will yield a larger small signal gain ($A_{vd} \approx g_m r_0$), but will result in a decreased bandwidth ($f_{3dB} \approx 1/(2\pi r_0 C_{diode})$).

We can thus bias the modulator at a point with a smaller electrical gain, but larger bandwidth. It follows, then, that we can tradeoff a faster device for an increase in electrical energy dissipation.

Figure 4-7 illustrates such tradeoff. The gain and bandwidth as a function of gate bias for different photocurrents is shown in Fig. 4-7(a). Larger gate bias voltages result in lower electrical gains and larger bandwidths due to a decrease in r_0, which is caused by an increase in the current flowing through the transistor I_{sw}.

The gain-bandwidth product is shown in Fig. 4-7(b) for different generated photocurrents. Two main trends are observed: (1) the gain-bandwidth product increases as gate bias increases until it saturates at a certain value; and (2) the gain-bandwidth product is larger for larger generated photocurrents.

Both observations can be explained by noting that the gain-bandwidth product is simply given by:

$$A_{vd} f_{3dB} = g_m(r_0||r_d)\frac{1}{2\pi(r_0||r_d)C_{mod}} = \frac{g_m}{2\pi C_{mod}} \tag{4.9}$$

As we saw in Fig. 4-5(b), g_m increases as the gate bias voltage increases for a fixed photocurrent, which explains observation (1) above. We also saw how larger photocurrents result in larger g_m values (Fig. 4-5(c)), which explains observation (2).

Clearly, the PV modulator can be biased at a point with a smaller gain but a faster frequency response, which can be desirable in applications requiring high

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data rate communication. As mentioned earlier, lowering the gain comes at a cost of increased power dissipation, because a larger input voltage swing is needed to achieve the same modulation strength.

In fact, we can characterize the energy gain that the PV modulator can achieve compared to a typical modulator:

$$\frac{E_{PV}}{E_{typ}} = \frac{\frac{1}{4}C_{sw}V_{pp,PV}^2}{\frac{1}{4}C_{mod}V_{pp,typ}^2} = \frac{C_{sw}}{C_{mod}}\frac{1}{g^2} \tag{4.10}$$

Where we have used $V_{pp,typ} = gV_{pp,PV}$, and g is the electrical gain of the PV modulator [7].

Figure 4-7(c) shows the 3 dB bandwidth of the PV modulator as a function of the energy gain compared to a typical modulator calculated using Eq. 4.10 and assuming $C_{mod}/C_{sw} = 20$. We can see how energy gains > 1,000x are achievable, but with limited bandwidths in the order of 1-10 MHz. Lower energy gains in the order of 100x can result in bandwidths above 1 GHz.

Figures 4-7(b,c) illustrate the importance of the photocurrent in the PV modulator performance. Clearly, large photocurrents are desirable to achieve energy savings at bandwidths above 1 GHz (as well as to achieve large open circuit voltages, see Fig. 4-4(a)).

4.3.3 Optical performance

All the analysis we have done up to this point has dealt with the electrical performance of the PV modulator. As a consequence, we have not made any strong assumptions about the optical modulator:

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[7]Since the voltage swing at the modulator terminals in the PV modulator is $V_{mod,pp} = gV_{pp,PV}$, and in a typical modulator is $V_{mod,pp} = V_{pp,typ}$.
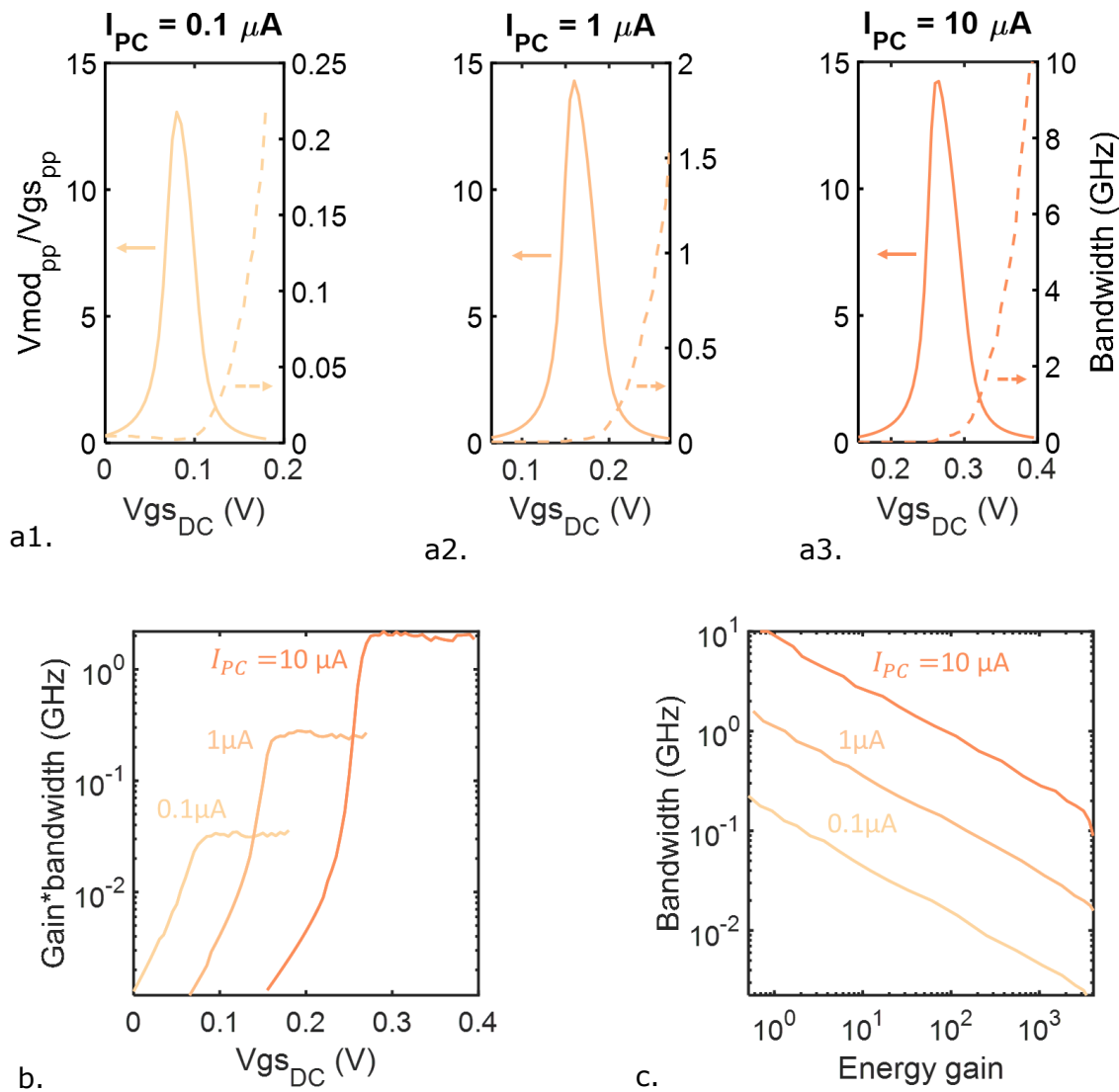
Figure 4-7: Gain-bandwidth tradeoff in a PV modulator. (a) Gain (solid line, left axis) and 3 dB bandwidth (dashed line, right axis) as a function of gate bias for 0.1 μA (a1), 1 μA (a2) and 10 μA (a3) generated photocurrent. (b) Gain-bandwidth product as a function of bias voltage for the same photocurrents as in (a). (c) Bandwidth as a function of energy gain compared to a conventional modulator for the same photocurrents as in (a). $C_{mod}/C_{sw} = 20$ is assumed.

1. We have assumed the modulator acts as a photovotlaic cell, i.e, it generates a photocurrent and develops a photovoltage when light is input to the device. We have already seen that photocurrent generation is ubiquitous in modern optical modulators, and any such device using p-n or p-i-n junctions will develop a photovoltage as a response.

2. We have used the diode model parameters corresponding to one of our CMOS resonant devices (Table 4.5), but any optical modulator based on p-n junctions will show similar characteristics. Of all the model parameters, the one which can vary the most is the zero bias junction capacitance C_{j0}, which as we have seen plays an important role in the device bandwidth.

Clearly, these assumptions apply to most optical modulators based on p-n junctions [8], which makes the analysis we have done up to this point quite general.

Nevertheless, we ultimately care about the optical performance of the device, so in this section we will make some assumptions about the optical characteristics of the modulator. This will allow us to derive performance parameters describing the modulation quality (ER, IL) of our PV modulator, and study how different parameters affect such quality. We will assume here that we are dealing with resonant modulators since it has been the core of this thesis, but a similar analysis could be made for Mach-Zehnder configurations.

Resonance wavelength shift

The first step to derive the optical modulation characteristics of the PV modulator is to translate the input voltage swing ΔV_{gs} to a shift in the resonance wavelength $\Delta\lambda_0$ of the modulator. We can do this by recognizing:

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[8]Most modulators are based on p-n or p-i-n junctions, especially in Si.
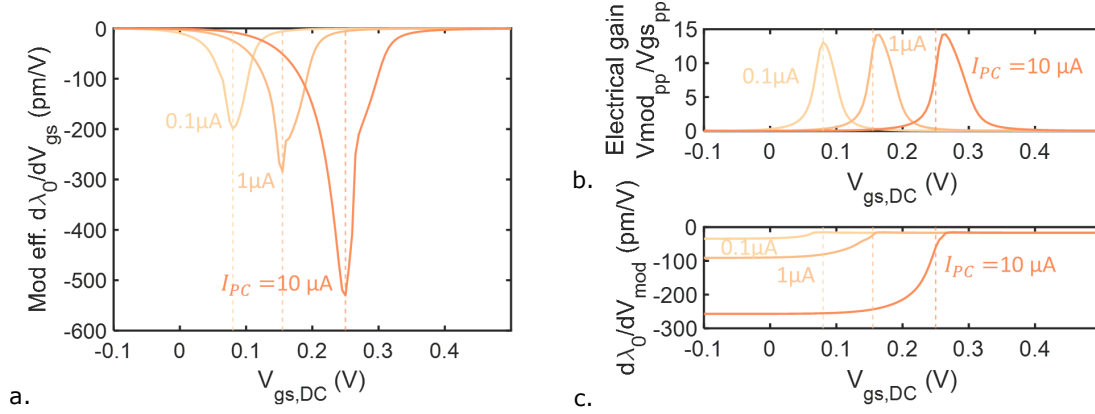
Figure 4-8: Modulation efficiency of the PV modulator. (a) Modulation efficiency from the PV modulator input terminals ($d\lambda_0/dV_{gs}$) as a function of gate bias voltage for different photocurrents. (b) Electrical gain g as a function of gate bias voltage for different photocurrents (same as Fig. 4-5). (c) Intrinsic modulation efficiency ($d\lambda_0/dV_{mod}$) as a function of gate bias voltage for different photocurrents. For (a), (b) and (c), the dashed lines denote the point of maximum modulation efficiency.

$$d\lambda_0 = \frac{d\lambda_0}{dV_{mod}}\frac{dV_{mod}}{dV_{gs}}dV_{gs} = \frac{d\lambda_0}{dV_{mod}}\bigg|_{V_{mod,bias}(V_{gs,bias})}g(V_{gs,bias})dV_{gs} \qquad (4.11)$$

In the equation above, $d\lambda_0/dV_{mod}$ is the modulation efficiency of the optical modulator (which we will call *intrinsic modulation efficiency*), and g is the electrical gain of the PV modulator configuration. Note we have explicitly indicated that both the intrinsic modulation efficiency and the gain depend on the bias point.

To evaluate the above expression we need the small signal electrical gain of the PV modulator $g(V_{gs})$, which we have already obtained with the electrical model simulations (Fig. 4-5). The intrinsic modulation efficiency $d\lambda_0/dV_{mod}$ is also required, and for this we will use the experimentally characterized values for our CMOS resonant modulators presented in Chapter 2 (Fig. 2-6).

Figure 4-8(a) shows the results of evaluating Eq. 4.11. Clearly, larger photo-

generated currents result in larger peak modulation efficiencies. This is due to the fact that, while the maximum electrical gain g is independent of photocurrent (Fig. 4-8(b)), larger intrinsic modulation efficiencies $d\lambda_0/dV_{mod}$ are achieved with larger photocurrents (Fig. 4-8(c)).

Note how the point of maximum modulation efficiency does not coincide with the bias that gives a larger electrical gain (dashed lines in Fig. 4-8) due to the fact that larger intrinsic modulation efficiencies can be achieved for bias voltages that do not yield optimal electrical gain.

It is important to note how, even for small photocurrents, the achievable peak modulation efficiencies are > 200 pm/V. This is > 10x larger than the modulation efficiency we can get with the modulator operated in a conventional configuration (≈ 20 pm/V).

From Eq. 4.11, the total wavelength shift for a voltage swing at the input of the PV modulator between $V_{gs,min}$ and $V_{gs,max}$ is then given by:

$$\Delta\lambda_0 = \int_{V_{gs,min}}^{V_{gs,max}} \left.\frac{d\lambda_0}{dV_{mod}}\right|_{V_{mod}(V_{gs})} g(V_{gs})dV_{gs} \qquad (4.12)$$

Note how, in general, $\Delta\lambda_0$ will depend not only on the amplitude of the applied voltage $V_{gs,pp} = V_{gs,max} - V_{gs,min}$, but also on the DC voltage $V_{gs,DC} = (V_{gs,max} + V_{gs,min})/2$. Fig. 4-9(a) shows the maximum achievable $\Delta\lambda_0$ as a function of $V_{gs,pp}$, assuming that the optimal $V_{gs,DC}$ is chosen. As expected, larger photocurrents result in larger resonance shifts for the same $V_{gs,pp}$ due to the fact that larger modulation efficiencies can be achieved (Fig. 4-8(a)).

It is also important to note how $\Delta\lambda_0$ saturates at large voltage amplitudes. As discussed in Section 4.3.1, this is because the maximum voltage swing at the modulator terminals is limited to V_{oc}, and therefore the maximum achievable resonance

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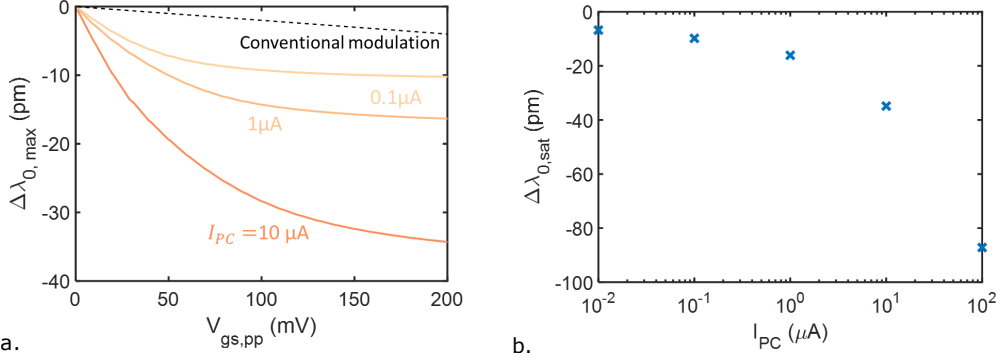
Figure 4-9: Resonance shift in the PV modulator. (a) Maximum achievable resonance shift for the PV modulator as a function of input peak to peak voltage. Different colors correspond to different generated photocurrents. The dashed black line shows the resonance shift achievable with conventional modulation. (b) Saturation wavelength shift as a function of photocurrent. Regardless of input peak to peak voltage, this is the maximum wavelength shift achievable in a PV modulator.

shift in the PV modulator is given by:

$$\Delta\lambda_{0,sat} = \int_0^{V_{oc}} \frac{d\lambda_0}{dV_{mod}}\bigg|_{V_{mod}} dV_{mod} \tag{4.13}$$

This is shown in Fig. 4-9(b) as a function of photocurrent. An increase in $\Delta\lambda_{0,sat}$ is observed with increasing photocurrent due to an increase in the open circuit voltage.

Modulation characteristics

Since we can obtain the wavelength shift for a given input voltage, the only thing we need to calculate the achievable ER and IL in our PV modulators is the resonance shape $T(\lambda)$.

With this, the ER and IL for a given wavelength shift $\Delta\lambda_0$ with the laser operating

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at a wavelength λ_l is given by [9]:

$$ER = |T(\lambda_l) - T(\lambda_l - \Delta\lambda_0)| \tag{4.14}$$

$$IL = max(T(\lambda_l), T(\lambda_l - \Delta\lambda_0)) \tag{4.15}$$

Of course, ER and IL will depend on λ_l, but they will also depend on the resonance characteristics, which are described by the quality factors Q_{rad} and Q_{coup} (see Eq. 2.2).

Figure 4-10 illustrates some of these dependences. Plots on the left correspond to a ring that is close to critical coupling ($Q_{rad} \approx Q_{coup}$), while those on the right correspond to rings far from the critical coupling condition, but with the same loaded Q factor. Several conclusions can be drawn from these results:

1. Critical coupling allows us to achieve better ER for the same electrical energy per bit, but at a higher IL point (compare Figs. 4-10(a2,a4) to Fig. 4-10(b2,b4)). This is expected, since a critically coupled ring has a much larger extinction ($\approx$ 20 dB - Fig. 4-10(a1)) at the resonance wavelength than a non-critically coupled ring ($\approx$ 10 dB - Fig. 4-10(b1)).

2. Lager Q factors result in better performance characteristics, both in terms of ER and IL (compare solid lines - smaller Q factor - to dashed lines - larger Q factor - in Fig. 4-10). This is because the same resonance wavelength shift $\Delta\lambda_0$ results in a larger transmission change (therefore larger ER) for a narrower resonance (i.e, for a larger Q factor resonance).

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[9]Notice how we are making the assumption that the only change to the resonance when applying a voltage is on its resonance wavelength. No changes in the resonance shape itself are considered.

3. Larger generated photocurrents result in better modulation performance, which is expected since we have previously seen how they result in larger resonance wavelength shifts $\Delta\lambda_0$.

While modulation performance is strongly dependent on the resonance shape, Fig. 4-10 shows how the PV modulator can achieve ER > 3 dB for energies per bit $\approx$ 1 aJ/bit with limited IL on the order of 3 dB. Noticeable modulation with ER $\approx$ 1 dB can be achieved for energies on the order of tenths of zJ/bit, although at larger IL.

4.3.4   PV modulator design principles

Throughout the last sections we have done a thorough analysis of the PV modulator working principle and studied how different variables affect its performance. We are now in a good position to summarize all the findings and derive a series of design principles to achieve the best overall performance.

On the transistor side, we want:

- A small gate capacitance C_{sw} to reduce electrical energy dissipation. This is equivalent to minimizing transistor size.

- A large intrinsic gain $g_m r_0$ to increase the small signal gain A_{vd}.

- A small output resistance r_0 to enhance the device bandwidth.

Besides using minimum size transistors, there is not much we can do in a PV modulator with regard to the transistor, since these are already fully optimized by the microelectronics foundry [10].

On the optical modulator side, we want:

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[10]Technically, a better performance could be achieved by switching technology node.
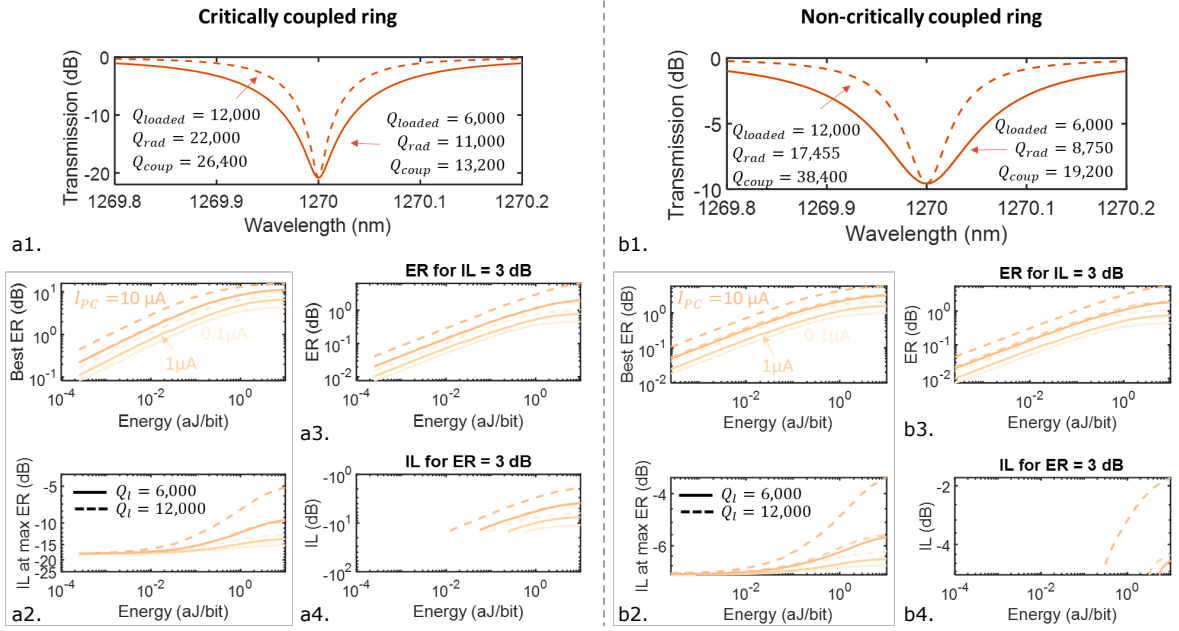
Figure 4-10: Achievable modulation characteristics for a PV modulator. (a) plots correspond to a critically coupled ring ($Q_{rad} \approx Q_{coup}$) and (b) plots to a non-critically coupled ring with the same loaded Q factors as in (a). (1) Resonance shapes considered. (2) Maximum achievable ER (top) and IL at that point (bottom) as a function of electrical energy per bit. (3) Achievable ER when the IL is limited to 3 dB as a function of electrical energy per bit. (4) IL necessary to achieve a 3 dB ER as a function of electrical energy per bit. If blank, it means that a 3 dB ER can't be achieved. For (2), (3), and (4), different colors correspond to different generated photocurrents. Solid lines correspond to the resonance with $Q_{loaded} = 6,000$, and dashed lines correspond to the resonance with $Q_{loaded} = 12,000$. The electrical energy per bit is calculated as $E = (1/4)C_{sw}V_{pp}^2$, with $C_{sw} = 1$ fF.

- Large generated photocurrents I_{pc}, which are essential to achieve:

  1. Large open circuit voltages, which increase the maximum achievable wavelength shift $\Delta\lambda_{0,sat}$.

  2. Larger peak modulation efficiencies $d\lambda_0/dV_{gs}$ and therefore larger wavelength shifts for the same applied input voltage. This translates into better ER and IL modulation for the same electrical energy consumption.

  3. Larger bandwidth, as larger photocurrents result in a larger transistor g_m.

- Large quality factor resonances and close to critical coupling condition.

Essentially, we want a critically coupled, high Q factor modulator with a large responsivity (i.e, a large generated photocurrent when light is input to the device).

At first sight, having a large Q factor resonance might seem incompatible with a large responsivity device, since large responsivities translate into large absorption coefficients, and therefore large ring internal loss and low Q factors. We argue in Appendix B how this is not the case for sufficiently compact resonant devices. Large Q factors > 20,000 with responsivities on the order of 0.2 A/W could potentially be achieved in Si resonators, which would result in improved PV modulator performance.

4.4 Experimental characterization at room temperature

The simulations we have performed seem to indicate that the PV modulator allows for ultra-low electrical energy dissipation < 1 aJ/bit with moderate ER > 1 dB. To confirm these results, we designed and fabricated a PV modulator in the 45 nm

CMOS SOI process from GlobalFoundries (the same commercial foundry process we used to fabricate all the devices in this thesis) and characterized its performance.

4.4.1 Device structure

Figure 4-11 depicts the fabricated device. The resonant modulator is the same as design *O-Z* presented in Chapter 2: a 5 μm radius ring designed for a 1270 nm operating wavelength incorporating a SiGe band to increase photocurrent generation in the ring.

We used a body-contacted NMOS transistor offered as a standard cell in the
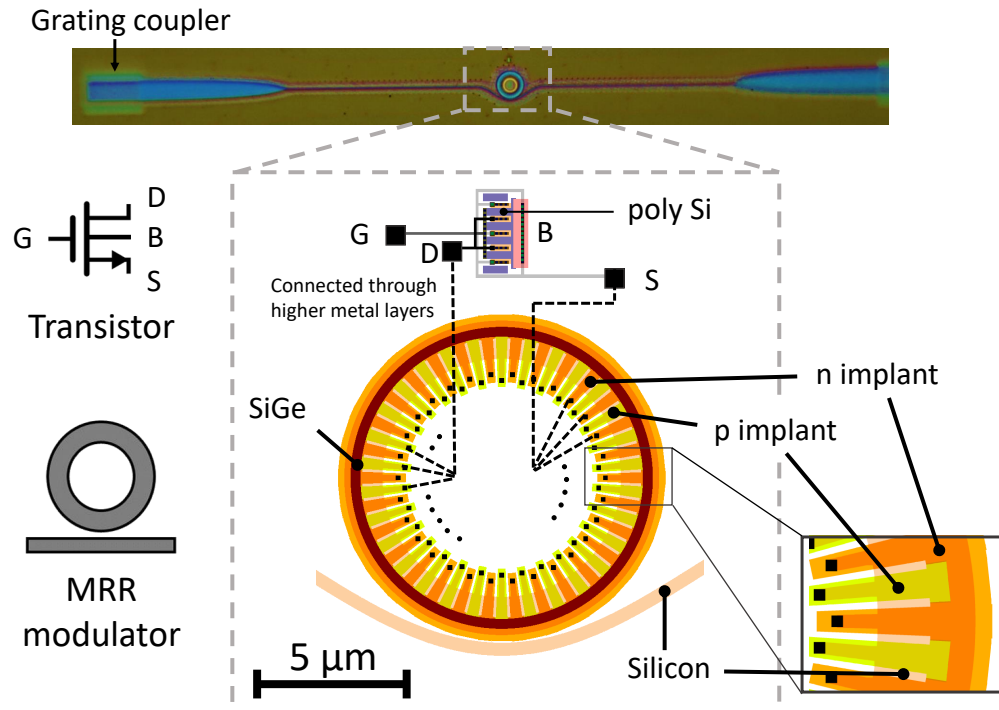
Figure 4-11: Fabricated PV modulator. (a) Micrograph of the device. Both the ring resonator and the transistor are visible. The grating couplers offering optical access to the chip are also shown. (b) Device layout. (c) Closeup on the T junction design for the modulator spokes.

microelectronics process. The nominal gate length is 56 nm, and the device width is 2.4 μm. From the electrical model given by the PDK, the input gate capacitance is $C_{sw} \approx 1$ fF. Smaller input capacitances on the order of 0.2 fF can be achieved in the same process using minimum width transistors.

4.4.2   DC characterization

We first measured the DC characteristics of the fabricated device and compared them to simulation results. Fig. 4-12(a) shows the measured DC voltage at the modulator terminals for a given gate bias voltage, and Fig. 4-12(b) shows the extracted small signal electrical gain.

Good agreement between experimental and simulation results is obtained, although we measured a lower small signal electrical gain than that predicted by simulation. Experimental data characterizing the fabricated transistors seems to suggest that this is due to the fact that the g_m is about 25% lower experimentally. We observed a stronger dependence of g_m on drain source voltage (V_{mod} in our configuration) than that predicted by simulations, which explains why larger deviations are obtained for lower generated photocurrents.

We also measured the resonance wavelength shift as we varied the gate bias voltage, and the results are shown in Fig. 4-13. Clearly, the device resonance shifts towards longer wavelengths as the gate source voltage increases as predicted by simulation.

While the simulation predicts very well the total resonance wavelength shift between open circuit ($Vgs = 0V$) and short circuit conditions ($V_{gs} > V_{th} \approx 0.6V$), a slower variation with gate bias is measured experimentally compared to what is predicted by simulation (Fig. 4-13(b)). As a consequence, the measured modulation

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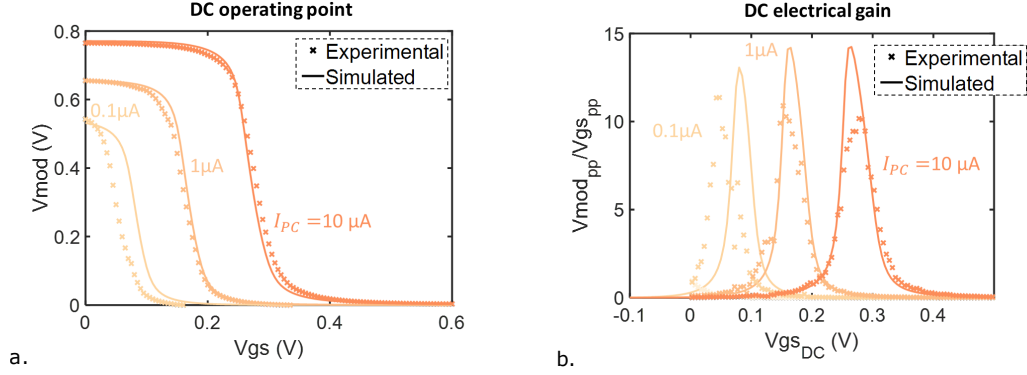
Figure 4-12: PV modulator experimental DC operating point characteristics. (a) Voltage at the modulator terminals as a function of gate bias voltage. (b) DC electrical gain as a function of gate bias voltage. For both (a) and (b), different colors correspond to different generated photocurrents. Crosses correspond to experimentally measured values, while solid lines are simulation results.

efficiencies are lower than those predicted by simulation (Fig. 4-13(c)). This is again due to the lower g_m values of the transistor, which result in a smaller electrical gain and therefore a smaller modulation efficiency. We experimentally measure peak modulation efficiencies > 100 pm/V, which are 5x larger than the $\approx$ 20 pm/V achievable with conventional modulation.

4.4.3   RF characterization

The measured frequency response of the PV modulator at the maximum gain point for different generated photocurrents is shown in Fig. 4-14. As we already discussed in previous sections, we observe an increase in the 3 dB bandwidth for increasing photocurrent: from 4.6 MHz for $I_{pc} = 0.22$ μA to 35 MHz for $I_{pc} = 3.2$ μA. Agreement between experimental and simulation results is excellent.
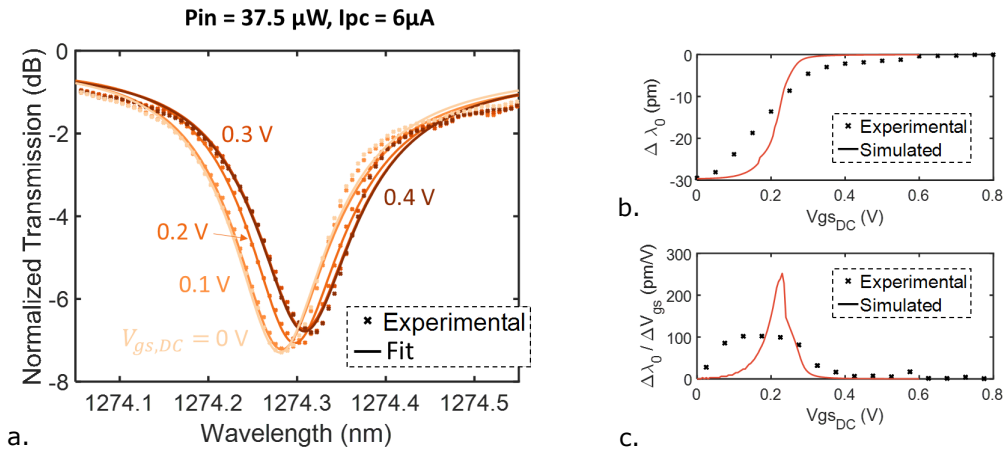
Figure 4-13: PV modulator experimental resonance wavelength shift. (a) DC transmission spectra for different gate bias voltages. (b) Resonance wavelength shift as a function of gate bias voltage. (c) Modulation efficiency as a function of gate bias voltage. For (b) and (c), crosses show experimentally measured values, and solid lines values predicted by simulation. The generated photocurrent was 6 μA.
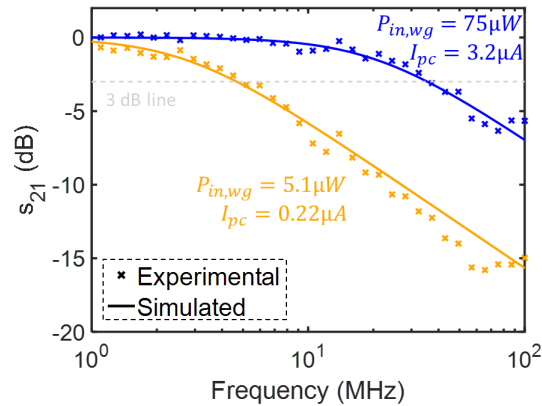
Figure 4-14: PV modulator experimental frequency response for 0.22 μA (yellow) and 3.2 μA (blue) generated photocurrents. Crosses correspond to experimentally measured values, while solid lines are simulation results.

4.4.4 Modulation characteristics

We also recorded modulation waveforms at 1 Mbps data rate for different input voltage signals and a 7.5 μW on chip input optical power, shown in Fig. 4-15. We can see how noticeable modulation can be achieved with input peak to peak voltages as low as 4 mVpp, corresponding to a 4 zJ/bit electrical energy dissipation. Such an electrical energy dissipation approaches the Landauer limit for the minimum energy necessary for binary switching [194], which is given by $kTln(2) = 3$ zJ at 300 K. Of course, the total energy dissipation in the PV modulator is not only that provided by the external electrical driver, but includes also the energy generated by the photovoltaic effect. An on chip optical power of 7.5 μW generates a 0.25 μA photocurrent and an open circuit voltage of about 0.6 V,corresponding to a 0.15 μW power and an additional 150 fJ/bit energy dissipation at 1 Mbps.

For all the waveforms shown in Fig. 4-15 the IL is lower than 3 dB, which is comparable to the IL of most modern optical modulators (see Tables 4.1 and 4.2). At 1 MHz data rate, such IL corresponds to an optical energy dissipation of 3.75 pJ/bit. While this is larger than the optical energy dissipation in state of the art modulators, significant improvements could be obtained by operating the modulator at faster data rates and improving the responsivity of the device (with a measured responsivity of 0.034 A/W, only 7% of the internal loss in the ring generates photocurrent, Appendix B).

Figure 4-16 compares the results obtained experimentally (black crosses) with the predictions made using the simulations described in Section 4.3 for a 0.25 μA generated photocurrent and the resonance shape measured experimentally (inset in Fig. 4-16). Very good agreement is obtained when we limit the maximum achievable IL to 3.5 dB in the simulations (solid line in Fig. 4-16). Clearly, better ER could

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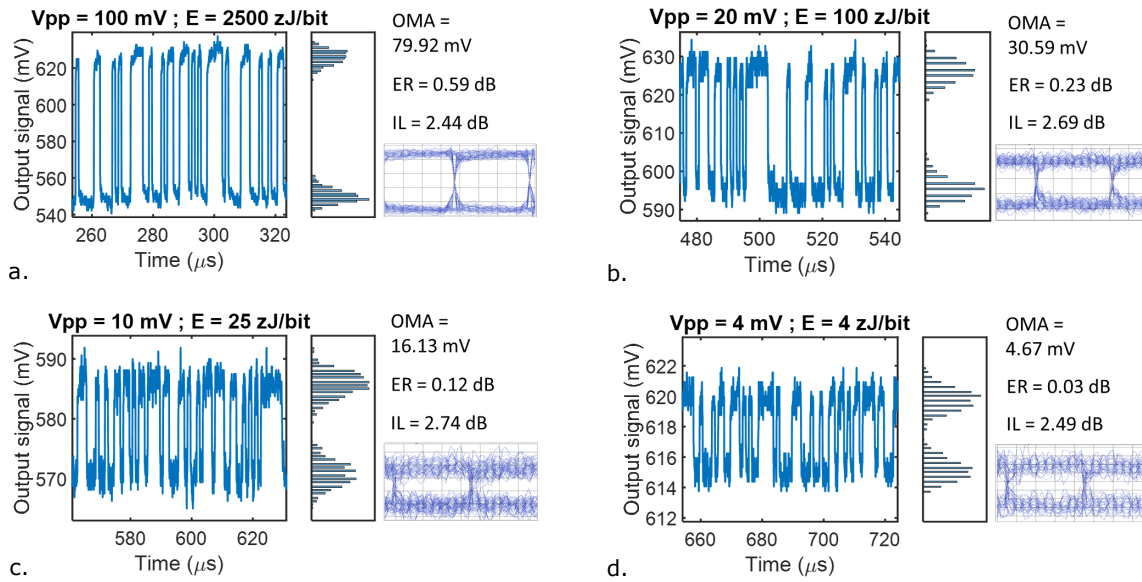
Figure 4-15: PV modulator experimental modulation signals. Each subfigure shows the resulting output optical signal for a different input peak to peak voltage, along with the histogram of the detected '1' and '0' bit values, its corresponding eye diagram and the modulation characteristics. The signal data rate is 1 Mbps, and the on chip input optical power is 7.5 μW, which corresponds to 0.25 μA of generated photocurrent.
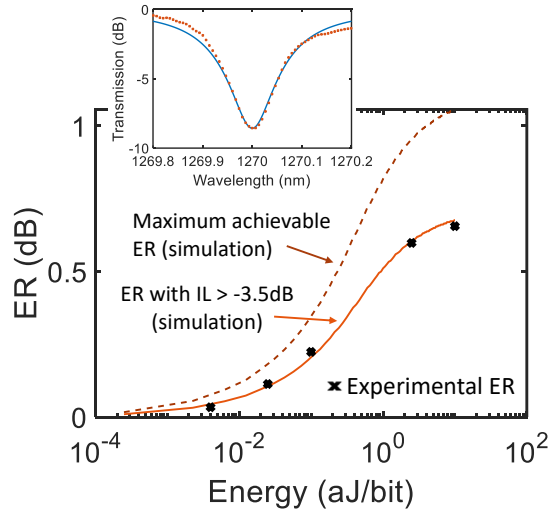
Figure 4-16: Comparison between measured and simulated PV modulator performance. Crosses show experimental results, the solid line simulation results limiting IL to less than 3.5 dB, and the dashed line the maximum achievable ER predicted by simulation. The inset shows the modulator's experimentally measured transmission spectrum (crosses) and the resonance considered in the simulations (solid line). A 0.25 μA photogenerated current is assumed for the simulations.

have been achieved at larger IL points, as shown by the dashed line in Fig. 4-16.

4.5 Cryogenic operation

Up to this point, in this chapter we have described and characterized the operation of PV modulators at room temperature. While interesting by its own, the focus of this thesis is the design of modulators for cryogenic readout applications. It is pertinent then to ask ourselves if the operational principle of the PV modulator is still valid at cryogenic temperatures, and how will its performance be affected.

To this end, we performed some preliminary testing to check how do photocurrent and open circuit voltage change at cryogenic temperatures. The results are shown in
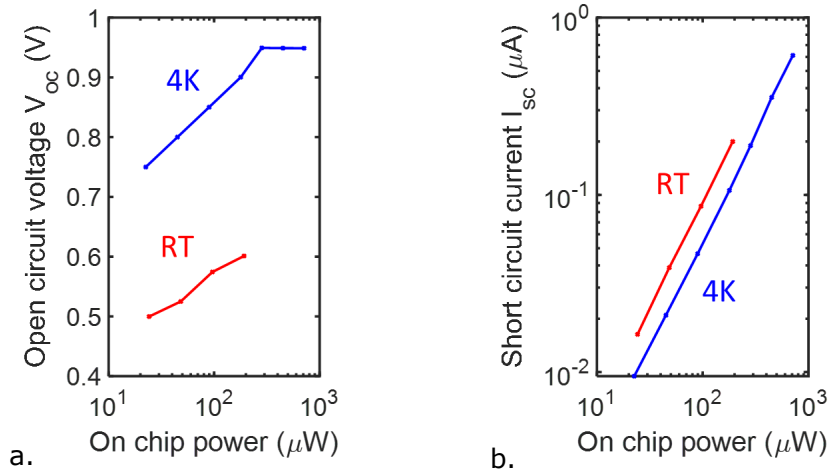
Figure 4-17: Photovoltaic effect at 4 K. Open circuit voltage (a) and short circuit current (b) as a function of on chip input optical power at 4 K (blue) and room temperature (red) for the Si only modulator for 1550 nm operating wavelength (design C in Chapter 2).

Fig. 4-17 for the modulator for a 1550 nm operation wavelength (design C in Chapter 2). We can see how the open circuit voltage increases at cryogenic temperatures, while a ≈ 3 dB decrease in photogenerated current is observed compared to room temperature. These results confirm that the basic principle of operation of the PV modulator - the existence of a generated photocurrent in the modulator when light is input to the device - can still be leveraged at cryogenic temperatures.

It is also important to consider how do the transistor characteristics change when operating at low temperatures. We are particularly interested in the evolution of the transconductance g_m and the output resistance r_0, since we have seen how these dominate the gain and bandwidth of the PV modulator. Previous work characterizing the performance of 40 nm technology transistors at 4K measured a 3x increase in g_m (attributed mainly to the mobility increase at cryogenic temperatures) and a similar intrinsic gain $g_m r_0$ [195].

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Such temperature dependence is highly beneficial for the low temperature operation of PV modulators: maintaining the same $g_m r_0$ with a larger g_m (therefore smaller r_0) means that we can achieve the same small signal electrical gain but with a faster frequency response compared to room temperature.

We can thus say that preliminary results point to an increased performance of the PV modulator at cryogenic temperatures. Particularly, a faster frequency response should be obtained due to a decrease in the output resistance of the transistor r_0. Of course, the confirmation of these predictions through testing and characterization of PV modulator devices at cryogenic temperatures is needed.

4.6   Conclusion

In this chapter we have presented, simulated and experimentally characterized a new operational regime for optical modulators, which we call the photovoltaic regime. We leverage the parasitic photocurrent generated by most optical modulators when light is input to the device to bias a transistor at a point where voltage amplification is achieved, therefore reducing the necessary driving electrical signal and the electrical energy dissipation in the device. Further energy reduction is obtained because the input capacitance that the external source has to drive is now that of a nanoscale transistor, which is 20-100x that the capacitance of the micrometer scale modulator.

We experimentally demonstrated optical modulation with electrical energies down to 4 zJ/bit at 1 MHz data rate. Figure 4-18 shows how our solution compares to the previous demonstrations of cryogenic readout and optical modulators presented in Chapter 1. It is important to remember that we have only tested the PV modulator at room temperature, but preliminary results point to an improved performance at cryogenic temperatures.

a.

b.

* Heat load of bias and high speed microwave lines not accounted for.

+ Optical power dissipation not accounted for.

++ Optical and electrical power dissipation accounted for.
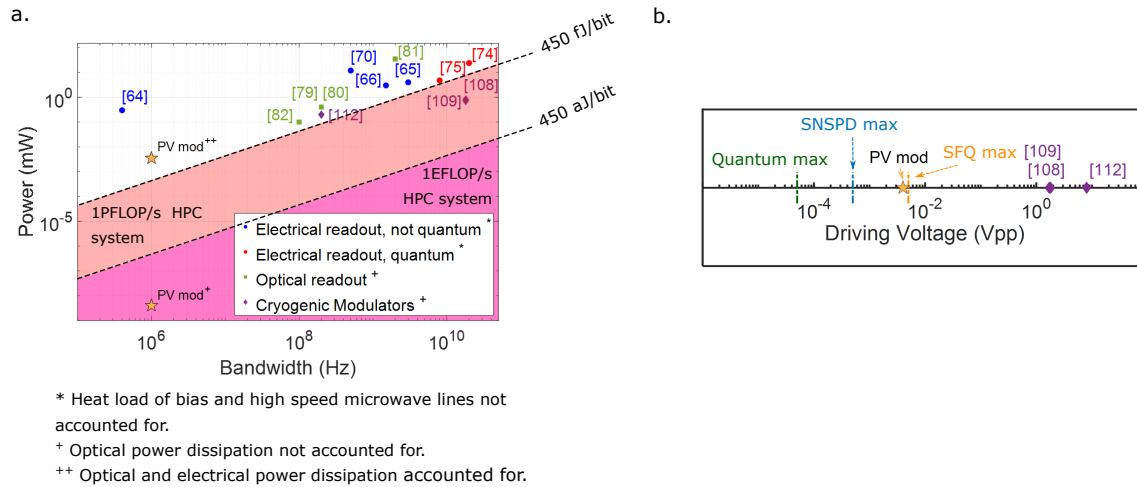
Figure 4-18: Comparison of the PV modulator with previously demonstrated cryogenic readout schemes. (a) Bandwidth and electrical power consumption. While it has a low bandwidth, our PV modulator has close to 7 orders of magnitude lower electrical energy dissipation than previously demonstrated cryogenic modulators. (b) Peak to peak voltage. Our modulator works with 2 orders of magnitude lower peak to peak voltages. Caveat: our PV modulator has only been experimentally characterized at room temperature.

While the experimentally achieved data rates are low for most modern communication systems, we have also demonstrated how larger 3 dB bandwidths on the order of 1 GHz can be achieved at the expense of a larger electrical energy dissipation (but still lower than that of conventional modulators). We have also discussed how a better performance in terms of extinction ratio and optical power dissipation could be achieved by increasing the responsivity of the device and its Q factor.

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Chapter 5

Nonlinear Effects in Resonant Modulators

All throughout this thesis we have been dealing with resonant modulators. As mentioned in Chapter 1, resonant modulators are attractive for high speed optical communication systems because of their compactness and narrow wavelength selectivity, which makes them a natural choice for DWDM systems where wavelength multiplexing and demultiplexing is necessary [78, 104]. Most importantly, such modulators have reduced power consumption, which as we discussed is essential for cryogenic applications.

While the resonant nature of these devices allows for such reduced power consumption, it also has some associated drawbacks. For instance, changes in the resonance wavelength of the device occur due to fabrication variations and environmental fluctuations such as substrate temperature. More importantly, the strong light confinement and electric field enhancement that microring modulators achieve due to their resonant nature gives rise to high power densities, which combined with the

fact that silicon exhibits high third-order nonlinearity [196], generate nonlinear effects that can cause unexpected behaviors even for low input powers.

As a consequence, practical communication systems using ring modulators need to limit their working input optical power and require active locking of the device resonance to the laser light. Such locking is possible and well established [197], but comes at the cost of increased power consumption (about 1 mW per modulator). While such power consumption might be tolerable for typical room temperature applications, it is in general not acceptable in applications with limited power budgets such as cryogenic readout.

It becomes necessary, then, to develop a tool to study the nonlinear effects that arise in resonant modulators. The goal is to understand their effects on device performance, analyze when do these effects become relevant and identifying the most relevant device parameters affecting such behaviors.

In this chapter we present a theoretical time domain model for externally modulated, reverse biased silicon resonators which accounts for the main nonlinear effects that affect the performance of a modulator – free carrier dispersion, free carrier absorption (FCA), two photon absorption (TPA) and thermal effects. We will use this model to study how increasing input optical powers affect resonant modulators, and we will compare modeling results with experimental data taken on our CMOS photonic modulators. While the bulk of this chapter will assume room temperature operation, we will also discuss the extension of the model to cryogenic temperatures.

5.1 Theoretical model

5.1.1 Relevant nonlinear effects in silicon resonant modulators

While silicon shows a wealth of nonlinear effects [11], here we will only discuss the dominant nonlinearities affecting operation of resonators as optical modulators. The interested reader is pointed to references [11,198] for an in-depth review of nonlinear effects in silicon and its applications [1].

The main nonlinear effects that dominate the behavior of silicon resonant modulators are depicted in Fig. 5-1(a): TPA, FCA and thermal effects. TPA is the process by which an electron-hole pair is generated by the simultaneous absorption of two photons, and it has a quadratic dependence with the energy stored in the microring. Through TPA, additional free carriers are generated in the waveguide, which change the resonance wavelength of the ring modulator through the plasma dispersion effect. Additionally, TPA results in a local heating of the waveguide due to increased FCA - the process in which a carrier is excited from an already-excited state to another through the absorption of a photon. The non-radiative relaxation of these excited carriers generates phonons, which translates into a self-heating of the waveguide. Such temperature changes are accompanied by a change in the refractive index of the optical waveguide (because of thermo-optic dispersion), and thus also generate shits in the resonance wavelength of the device.

The strong coupling between self-heating and TPA makes the evolution of the resonance wavelength of the resonator with time non trivial (Fig. 5-1(b)) given

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[1]Although nonlinear behavior is generally not desired in resonant modulators, which is the focus of this thesis, a lot of interesting applications have been reported in the literature that exploit nonlinearities in silicon waveguides. Examples include amplification [199], cross-phase and cross-amplitude modulation [200], switching [201] and wavelength conversion [202].
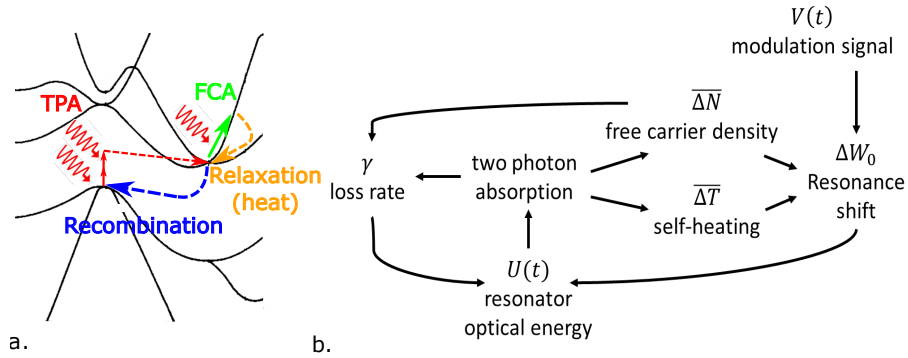
Figure 5-1: Dominant nonlinear effects in silicon resonant modulators. (a) Diagram of the physical phenomena occurring in a silicon optical device in the presence of two photon absorption (TPA). (b) Diagram of nonlinear effects in a silicon ring modulator and their inter-dependence. The modulation signal $V(t)$ changes the resonance frequency ΔW_0 of the device, affecting the total stored energy in the resonator and setting the strength of TPA. TPA, in turn, modifies the resonance through two effects: free-carrier dispersion and self-heating. These two phenomena compete in opposite directions: free carrier dispersion shifts the resonance to shorter wavelengths, while heating pushes it to longer wavelengths.

that the generated dispersion moves the resonance in opposite directions: a larger free carrier density generated by TPA blue shifts the resonance (i.e, decreases the resonance wavelength), but it generates an increase in waveguide temperature, which has an associated red-shift (i.e, increase in the resonance wavelength). The fact that the time scales of these two effects are also very different (TPA is an instantaneous process, but heating has a time constant in the order of μs) adds more complexity to the nonlinear behavior of silicon resonant modulators.

Such nonlinear interactions are important: effects such as thermal [203] and carrier [204] induced optical bistabilities, as well as self-pulsation due to the competition between these processes [205], have been reported in silicon microring or microdisk resonators.

It is important to note how the change in the resonance wavelength generated

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by these two effects is not desired when operating a resonant device as an optical modulator. This is because we want the externally applied voltage to be the only variable controlling the resonance wavelength and setting the output '0' and '1' power levels and the transition between them. The resonance shifts caused by nonlinear effects generates changes in optical transmission that do not correspond to changes in the data being transmitted, and as such should be minimized.

5.1.2 Theoretical model formulation

Several time domain models to study nonlinear effects in silicon resonators have been reported in the literature. In [205], Johnson et al. presented a model accounting for the effects of two photon absorption (TPA), free carrier absorption (FCA) and self-heating on passive resonators. A similar model focusing on carrier effects was also presented in [206]. These models are developed for passive structures, in which no active external modulation of the device resonance is possible.

Here, we will use a model based on [205], but we will extend it to actively modulated, reverse biased silicon resonators. In the interest of brevity, here we will reproduce only the most relevant equations. The full coupled system of differential equations is discussed in Appendix D.

Three modifications are included to the model by Johnson et al. [205] to extend it to actively modulated devices. First, the splitting between clockwise and counter-clockwise modes of the ring (which is included in [205]) is not considered, since this effect is only observable in high quality factor (Q > 100, 000) resonators that are not attractive for fast modulation due to their limited bandwidth [207] (optimal Q for high-speed modulation are in the 10,000-20,000 range). Second, the definitions of effective mode volumes for TPA (V_{TPA}) and FCA (V_{FCA}), and of the field confinement

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factor (Γ_{ring}) have been modified by normalizing the electric field to the Poynting vector rather than the E-field energy for better accuracy in high-index-contrast silicon photonic structures [208]. Third, the effect of external modulation voltage on the resonance frequency of the microring ($\Delta W_{0_{mod}}$) is included as an additive term next to the thermal and plasma dispersion terms:

$$\frac{\Delta W_0(t)}{W_0} = -\frac{1}{n_{Si}} \left(\frac{dn_{Si}}{dT}\overline{\Delta T(t)} + \left(\frac{dn_{Si}}{dN_p} + \frac{dn_{Si}}{dN_n} \right) \overline{N(t)} \right) + \frac{\Delta W_{0_{mod}}(t)}{W_0} \qquad (5.1)$$

Above, $\overline{\Delta T(t)}$ is the difference between the local ring temperature and the ambient temperature weighed by the overlap with the optical mode (see Appendix D), and is given by:

$$\frac{d\overline{\Delta T(t)}}{dt} = -\gamma_{th}\overline{\Delta T(t)} + \frac{\Gamma_{disk}}{\rho_{Si}c_{p,Si}V_{ring}}P_{abs}(t) \qquad (5.2)$$

P_{abs} is the instantaneous power absorbed in the ring: $P_{abs}(t) = (\gamma_{lin} + \gamma_{TPA} + \gamma_{FCA})U(t)$, where $U(t)$ is the energy stored in the ring (see Appendix D).

In Eq. 5.1, $\overline{N(t)}$ is the free carrier concentration in the ring weighed by the overlap with the optical mode, with a dynamic evolution given by:

$$\frac{d\overline{N(t)}}{dt} = -\gamma_{fc}\overline{N(t)} + \frac{\Gamma_{FCA}\beta_{Si}c^2}{2\hbar W_l n_g^2 V_{FCA}^2}U(t)^2 \qquad (5.3)$$

Above, the second term accounts for the free carriers generated through two photon absorption.

We assume that the resonance frequency changes linearly with the p-n junction voltage through a constant factor dW_0/dV_{pn} - the modulation efficiency. While in general the term dW_0/dV_{pn} will depend on the voltage at the modulator terminals

$V_{pn}(t)$, assuming this term does not change is valid in reverse bias due to the fact that the changes in the depletion region width are small compared to the optical mode size [2]:

$$\Delta W_{0_{mod}}(t) = \frac{dW_0}{dV_{pn}} V_{pn}(t) \tag{5.4}$$

The voltage across the p-n junction (V_{pn}) whose depletion region is modulated through $V(t)$ is modeled as a first order system with time constant τ:

$$\frac{dV_{pn}(t)}{dt} = \frac{-V_{pn}(t)}{\tau} + \frac{V(t)}{\tau} \tag{5.5}$$

τ corresponds to the dominant time constant of the system, which as we have previously discussed corresponds to the RC limit in reverse bias. Due to the dependence of the depletion capacitance $C(t)$ and series resistance $R(t)$ of the device on the applied voltage, the time constant τ is time dependent. Nevertheless, this dependence is generally small due, again, to the small changes in depletion region width with applied voltage. As a consequence, we will consider τ to be voltage (and time) independent.

The model results in a system of coupled, nonlinear differential equations. We use a variable order Adams-Bashforth-Moulton predictor-corrector method [209] to solve it. The model allows us to obtain the time evolution of the optical signal at the output of the modulator, as well as that of the resonator variables (resonance wavelength, stored energy, temperature, etc.) as an electrical voltage signal is applied

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[2]Note how, experimentally, we did not measure large changes in the modulation efficiency with voltage in reverse bias (Chapter 2). It is also worth mentioning how this assumption is not valid for forward biased devices, as modulation efficiency depends exponentially on voltage as experimentally measured in Chapter 2. The only instance where this could be valid in forward bias would be for very small driving voltage amplitudes, where a linearization of the modulation efficiency would be a good approximation.

to the modulator.

The reader interested in a more in-depth discussion of the model derivation is pointed to Appendix D and reference [205].

5.2   Device under study

To confirm the validity of our theoretical model, we will compare the obtained results with experimental measurements in our CMOS photonic resonant modulators. In particular, we will use design C presented in Chapter 2 (see Fig. 2-1(a)). As a reminder, this device is designed for a 1550 nm operating wavelength, has an outer radius of 10 μm and is 1.7 μm wide. For this device, we measured a 14 GHz bandwidth and a modulation efficiency of 20 pm/V in reverse bias at room temperature.

In the time-domain nonlinear model, different physical parameters capture linear and nonlinear effects in the resonator. These parameters are listed in Table 5.1 for our modulator, along with a brief description for their derivation. A detailed description of the process to obtain such parameters is available in [95]. An important parameter in our model is the free-carrier lifetime, which is estimated to be on the order of 0.1 ns in our device [212]. This magnitude is consistent with the estimated lifetime from operation of the device in the forward bias regime, and lifetime variations on the order of 0.5-5x do not cause significant differences in the qualitative behavior of the model. We derived the thermal time constant γ_{th} using estimates for the thermal impedance (through self-heating resonance shift measurements) and heat capacitance of the device. It is also worth noting that linear optical absorption, which as we discussed in Chapter 4 is important in silicon photonic structures due to surface state absorption, is accounted for through the parameter γ_{lin}.

Parameter	Value	Ref.
β_{Si}	$8.4 \times 10^{-12}\ m \cdot W^{-1}$	[196]
n_{Si}	3.485	[210]
dn_{Si}/dT	$1.86 \times 10^{-4}\ K^{-1}$	[97]
dn_{Si}/dN_n	$-8.8 \times 10^{-22}\ cm^3$	[100]
dn_{Si}/dN_p	$-8.5 \times 10^{-18}\ cm^3$	[100]
α_p	$6 \times 10^{-22}\ m^2$	[100]
α_n	$8.5 \times 10^{-22}\ m^2$	[100]
Γ_{TPA}	0.90967	FEM
Γ_{FCA}	0.9621118	FEM
Γ_{ring}	0.6515	FEM
V_{FCA}	$8.67 \times 10^{-18}\ m^3$	FEM
V_{TPA}	$10.63 \times 10^{-18}\ m^3$	FEM
γ_0	$30\ GHz$	DC transmission
γ_{rad}	$11\ GHz$	DC transmission vs power [211]
κ	$1.73 \times 10^5\ \sqrt{Hz}$	DC transmission
n_g	2.73	Free spectral range
dW_0/dV_{pn}	$1.57 \times 10^{10}\ rad/(s \cdot V)$	DC transmission vs voltage
γ_{th}	$2.4\ MHz$	DC transmission vs power
τ	$10\ ps$	Bandwidth measurements [136]
γ_{lin}	$19\ GHz$	DC transmission vs power [211]
γ_{fc}	$10\ GHz$	[212]
λ_0	$1545.2\ nm$	DC transmission
$V(t)$ signal	$2^7 - 1$ PRBS square	Arbitrary
$V(t)$ data rate	$0.5\ Gbps$	Arbitrary
$V(t)$ bias voltage	$-2.5\ V$	Arbitrary
$V(t)$ amplitude	$4\ V_{pp}$	Arbitrary

Table 5.1: Model parameters corresponding to the 1550 nm silicon microring modulator (design C in Chapter 2). FEM = Finite Elements Method.

5.3 Modulator initialization in the nonlinear regime

The presence of bistabilities under high optical powers makes it important to bring the resonator into a stable point before starting the modulation. Figure 5-2(a) shows the bistability curve of the device for a 0.45 mW optical power launched in the input waveguide, simulated using the method outlined in [197]. The red shift of the resonance (λ_0) in states A and B is observed due to thermal effects: the closer the laser wavelength is to the ring resonance, the larger circulating power is present in the ring, which generates local heating due to linear and free carrier absorption and pushes the resonance towards longer wavelengths.

From looking at Fig. 5-2(a), it is clear that if we want to get close to the resonance wavelength of the device we need to be able to track the resonance along the A+B branch. Getting close to the resonance wavelength is essential to achieve low output powers for the '0' bit, and therefore achieve large ER modulation [3].

A simple way to track the A+B branch is to sweep the laser from shorter wavelengths, which allows us to place the laser on any arbitrary point on the blue side of the Lorentzian curve of the resonator and as such achieve arbitrarily low '0' output powers. This is shown in the blue curve in Fig. 5-2(b), which shows the '0' bit transmission value simulated with our time domain model as wavelength is swept from the blue side of the resonance toward longer wavelengths. The consequence of this initialization approach is that it allows us to achieve an arbitrary small value for the transmitted zero bit, and therefore high ER and high optical modulation amplitude (OMA) modulation.

If instead of sweeping the laser we were to abruptly turn it on at a given wavelength, the ability to track the resonance is lost, which causes a transition from

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[3]Note that, if $P_{out,0} \to 0$, then $ER \to \infty$ no matter the value of $P_{out,1}$.
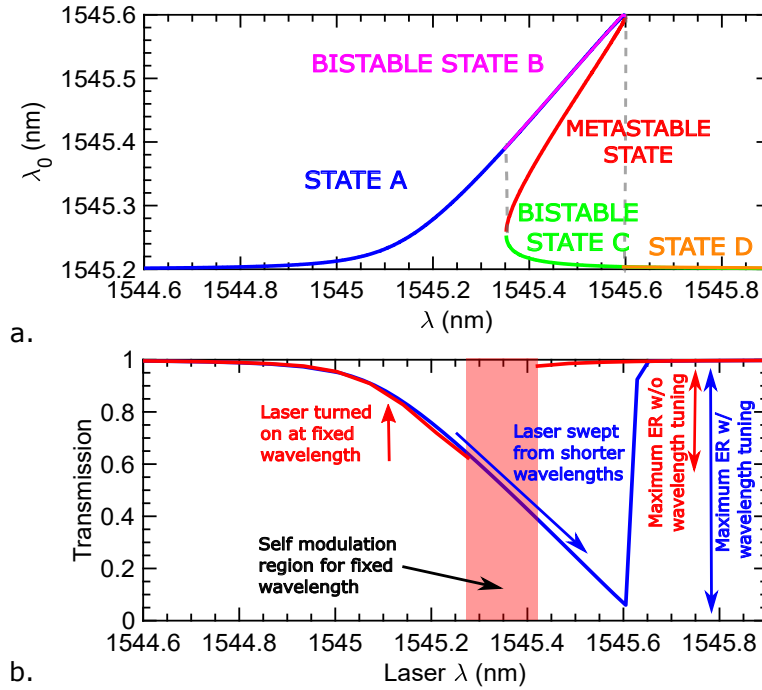
Figure 5-2: Resonant modulator initialization in the nonlinear regime. (a) Bistability curve of the microring extracted using the model in [197] for a 0.45 mW input power. λ_0 is the resonance wavelength of the ring and λ is the laser wavelength. (b) Transmission as a function of wavelength for a 0.45 mW input optical power obtained with our nonlinear model. The red curve corresponds to the laser being abruptly turned on at a fixed wavelength, and the blue curve corresponds to the laser being swept from the blue side of the resonance and stopped at the target wavelength. The ER achievable when the laser is swept is significantly higher.

branch A in the blue side of the resonance to branch C in the red side. This is shown by the red curve in Fig. 5-2(b), which we also obtained by solving our nonlinear model. It is clear that, as opposed to the swept initialization case (blue curve), when the laser is directly turned on at the target wavelength the transmission values cannot approach zero, resulting in a low ER and OMA modulation, and therefore high BER. Furthermore, when the laser is turned on abruptly, self-modulation due

to competing heating (moving the resonance to longer wavelengths) and free-carrier (moving the resonance to shorter wavelengths) dispersion can occur (shaded band in Fig. 5-2(b)), preventing successful data modulation.

We have therefore identified one important effect of nonlinearities and the need of proper device initialization to overcome such effect. Note that the same initialization (tracking down the A+B branch) is used for most nonlinear experiments with high-Q resonators, as the goal in those experiments is to achieve maximum power drop in the resonator for maximizing the nonlinearity [213], which overlaps with our goal to achieve low '0' bit values (strong power drop) for modulation.

Of course, these nonlinear effects become more important as the input optical power is increased. For our device, input optical powers below 500 μW in the waveguide did not result in noticeable initialization effects (i.e, the same '0' optical power could be achieved using laser sweeping or abrupt initialization). For optical powers above 1.5 mW, we observe a close to 70% improvement in the achievable '0' value when wavelength sweeping is used.

5.4 Modulator operation in the nonlinear regime: power handling

The theoretical model described gives the time domain optical waveform at the output of the modulator device $s_{out}(t)$, which allows for direct comparison between modulation results under different operational conditions. We will use OMA as a measure of the quality of the modulation, as it can be directly related to the bit error rate (BER) in a communication link [128]. The OMA is defined as the difference between the mean value of the output power corresponding to the '1' (μ_1) and '0' (μ_0)

bits, and can be rewritten as $\mu_1 - \mu_0 = \frac{P_{in}}{IL}\left(1 - \frac{1}{ER}\right)$, where P_{in} is the input optical power, and ER and IL are the extinction ratio and insertion loss of the modulator, respectively.

Using our time-domain nonlinear solver, we explored power handing capabilities of the microring modulator as the device is driven by a pseudo-random bit sequence with the characteristics specified in Table 5.1. Different input optical powers and optical carrier (laser) wavelengths (swept from the blue side of the resonance as mentioned in the previous section) were considered, and the modulation performance metrics (ER, IL, OMA) were extracted by analyzing the obtained time-domain transmission waveforms.

As we have already mentioned, we also performed experimental measurements on our 1550 nm CMOS resonant optical modulator, under the same operational conditions as the simulation to evaluate the validity of the model. The modulator's output optical signal for different input optical powers and laser wavelengths was recorded using a photodetector connected to a high speed oscilloscope and analyzed to extract modulation performance metrics. To reach high input optical powers an Erbium Doped Fiber Amplifier (EDFA) was used to amplify the light coming out of a tunable laser, and a second EDFA was used at the output of the modulator device to increase the strength of the signal going into the photodetector. A narrowband filter was used to reduce the Amplified Spontaneous Emission (ASE) noise at the output of the second amplifer.

Figures 5-3(a) and 5-3(b) show the evolution of ER, IL and OMA with wavelength for a fixed input optical power of 0.45 mW and a 4 V_{pp} driving voltage derived with the model (Fig. 5-3(a)) and obtained experimentally (Fig. 5-3(b)). OMA results are normalized to its maximum to allow for a direct comparison between experimental OMA (measured in mV at the output of the photoreceiver) and simulated OMA

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(given in mW at the output of the microring).

The results given by the model are in good agreement with the experimental curves. The existence of two distinct peaks (corresponding to modulation in the blue (peak at lower wavelengths) and red (peak at higher wavelengths) sides of the ring resonance) for OMA and ER is correctly modeled, as well as the fact that the maximum IL occurs between these two peaks (due to modulation happening
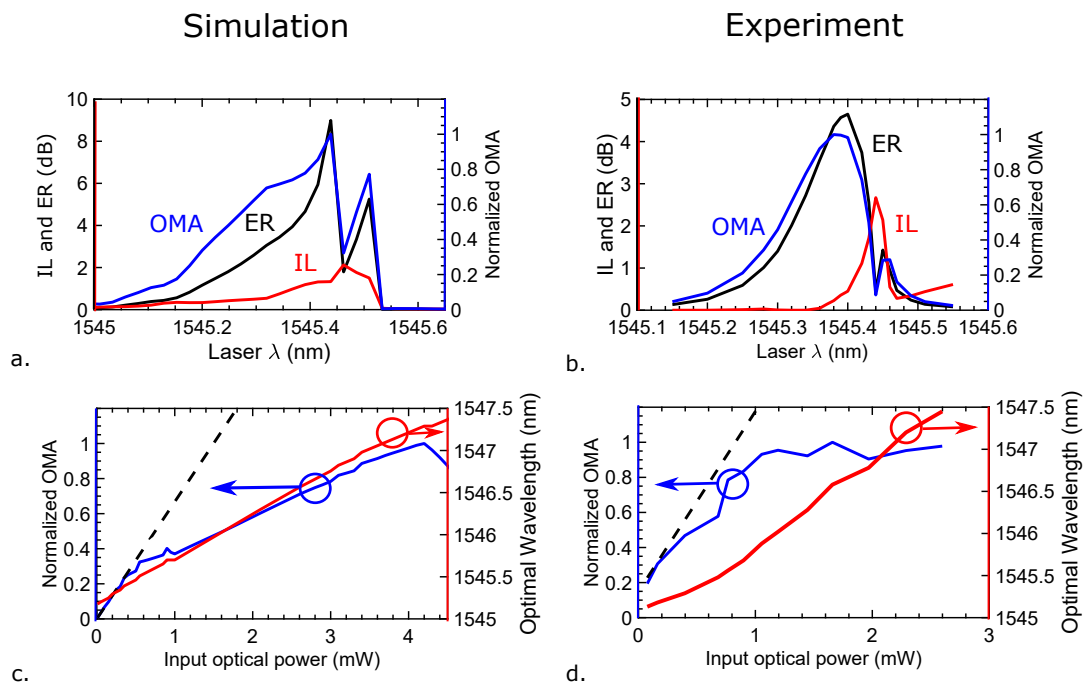
Figure 5-3: Device optimum operational point. Theoretical (a) and experimental (b) evolution of the ER (black), IL (red) and normalized OMA (blue) as a function of laser wavelength for a 0.45 mW input power. Theoretical (c) and experimental (d) maximum attainable OMA (blue, left axis) and wavelength at which this value is reached (red, right axis) as a function of input power. The dashed line shows the expected evolution of OMA if no nonlinearities were present. Reported experimental powers are at the center laser wavelength and do not account for the extra input power due to unfiltered ASE optical power coming from the EDFA. The data rate used is 0.5 Gbps.

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right at the resonance dip). The model also correctly captures the fact that better OMA is obtained when modulation is performed at the blue side of the resonance, and that the maximum OMA is obtained when the ER is maximum. Due to the theoretical model not accounting for noise, experimental ER (IL) values are lower (higher) than theoretical values. For the same reason, experimental curves show a smoother dependence with wavelength.

Both experiment and theory show that there is a well-defined wavelength where the best performance is achieved for a specific input optical power. As expected, the IL is near zero when the laser is far from the 'hot' resonance of the device (the resonance under nonlinear effects), and increases and reaches a peak as it approaches the transmission dip (where the modulation swing is not enough to move the device out of the resonance line-shape). The ER increases as the laser approaches the resonance dip from the blue side, and reaches a maximum when the system is able to reach the critical coupling condition and close to zero transmission for bit '0'. As the laser moves slightly to longer wavelengths, ER drops dramatically as the modulation now happens between the two sides of the resonance lineshape, resulting in a return-to-zero (RZ) like pattern with a high '0' output power. ER increases and reaches a second peak as modulation moves completely to the red side of the resonance, but the value of ER is low due to the resonance returning quickly to its cold state (state D in Fig. 5-2(a)).

Figures 5-3(c) and 5-3(d) show the highest achieved OMA (blue curve; normalized to its maximum to allow for comparison of experimental and theoretical results) along with the wavelength (red curve) at which it is achieved derived with the model (Fig. 5-3(c)) and obtained experimentally (Fig. 5-3(d)). Again, good qualitative agreement between experimental and theoretical results is achieved: (1) the experimental optimal operational wavelengths are very closely reproduced by our model,

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Simulation

a.

Experiment

b.

Output power   Thermal dispersion   Free carrier dispersion

c.

d.
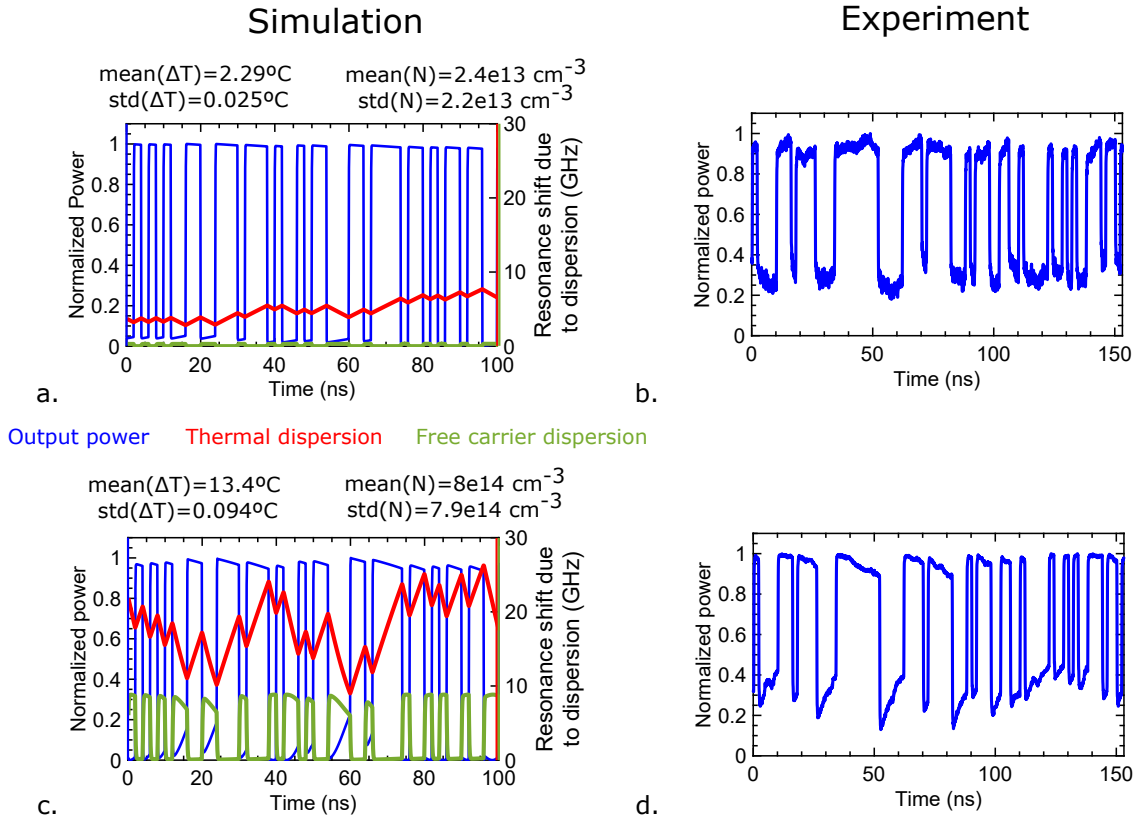
Figure 5-4: Effects of nonlinearities in time domain. Simulated normalized output optical power as a function of time (blue, left axis) and resonance frequency shift due to temperature (red, right axis) and carrier density (green, right axis) fluctuations for 0.3 mW input optical power (a) and for 2 mW input optical power (c). Resonance shifts are referenced to the minimum shift for the operational condition being considered, so that the shown curves are $\Delta W_X(t) - min\{\Delta W_X(t)\}$, where X refers to either temperature or carrier dispersion. Experimental normalized output optical power as a function of time for 0.1 mW input optical power (b) and for the experimental optimal input optical power of 1.65 mW (d). Reported experimental powers are at the center laser wavelength and do not account for extra input power due to unfiltered ASE optical power coming from the EDFA. The data rate is 0.5 Gbps. Reported temperature and carrier averages and standard deviations are calculated over a 2 μs time series.

and (2) the saturation and eventual decrease in the maximum attainable OMA as input optical power increases, which is predicted by the theoretical model, is also observed experimentally, although not as clearly.

While simulated data shows a peak in OMA followed by a saturation (see Fig. 5-5(a)), experimental data only shows the saturation of OMA. Notice how, in simulation, the difference between the peak OMA and its saturated value is roughly 20%, or 1dB. We believe that we probably missed this relatively small peak due to our coarse choice of wavelengths in the experiment. Nevertheless, both the theory and experiment point to presence of an optimum input optical power: if the maximum attainable OMA has plateaued, there is no need to increase the power as this will only increase energy dissipation but won't improve modulation quality.

Clearly, the existence of nonlinear effects results in an optimal input optical power for modulation quality: an increase in the power beyond this limit will deteriorate the performance due to the enhancement of nonlinear effects. Note that, if nonlinearities were not present in the system, OMA would linearly increase with input power (dashed black curves in Fig. 5-3(c) and 5-3(d)) as ER and IL would be independent of the optical power (resulting in OMA being only dependent on P_{in}). In the presence of nonlinearities, there is a power above which the negative effects of increased thermal and carrier dispersion (which cause a fluctuation in the output power values for bits '1' and '0', see Fig. 5-4) overcome the gain of using a high input power that would otherwise result in a higher '1' output power and an improvement in OMA.

As can be observed, the theoretical optimal input power ($\approx$ 4.2 mW) is around 2.5x higher than the experimentally measured optimum ($\approx$ 1.65 mW). This difference is due to the fact that the experimental powers measured and reported correspond to the power at the center wavelength of the laser, but the effective power entering the cavity is higher due to the presence of unfiltered ASE optical power. By studying the

shift in resonance wavelength as a function of input optical power with and without an input EDFA, we observed that the total effective power driving nonlinearities was approximately 2-3 dB higher than the center wavelength input power. Additionally, uncertainties in the input grating coupler loss (which translate into uncertainties in the power launched into the ring) and the difficulty of experimentally reaching the exact optimum operational point also contribute to this difference.

Due to the use of non-optimized grating couplers (with an insertion loss of around 10 dB) and a limited gain EDFA, the maximum input optical power that could be experimentally reached at the input waveguide of the modulator was around 2.6 mW. As we will discuss later, at high modulation speeds (a few Gbps) this amount of optical power does not result in significant nonlinear effects due to the slow thermal response of the device, which translates in lower thermal nonlinearities at the same level of input power. Therefore, in order to experimentally observe nonlinear phenomena at lower powers we reduced the data to 0.5 Gbps.

Figure 5-4 shows simulated and experimental transmission waveforms for low power (Fig. 5-4(a) - theoretical, Fig. 5-4(b) - experimental) and at the optimal input power (Fig. 5-4(c) - theoretical, Fig. 5-4(d) - experimental). The theoretical waveforms also show the thermal (red curve) and free carrier dispersion (green curve) temporal evolution (first and second terms in Eq. (5.1)). Again, good agreement between theoretical and experimental waveforms is obtained.

For low input powers (Figs. 5-4(a) and 5-4(b)) nonlinearities are weak, so resonance fluctuations due to unwanted thermal and carrier dispersion effects are minimal, and thus stable output power values for the '0' and '1' bits are achieved. At the optimal input power (Figs. 5-4(c) and 5-4(d)) the increase in temperature and carrier density variations generates visible fluctuations in the output power for bits '0' and '1'. Notice how our model correctly predicts the time evolution of the '0' and '1' lev-

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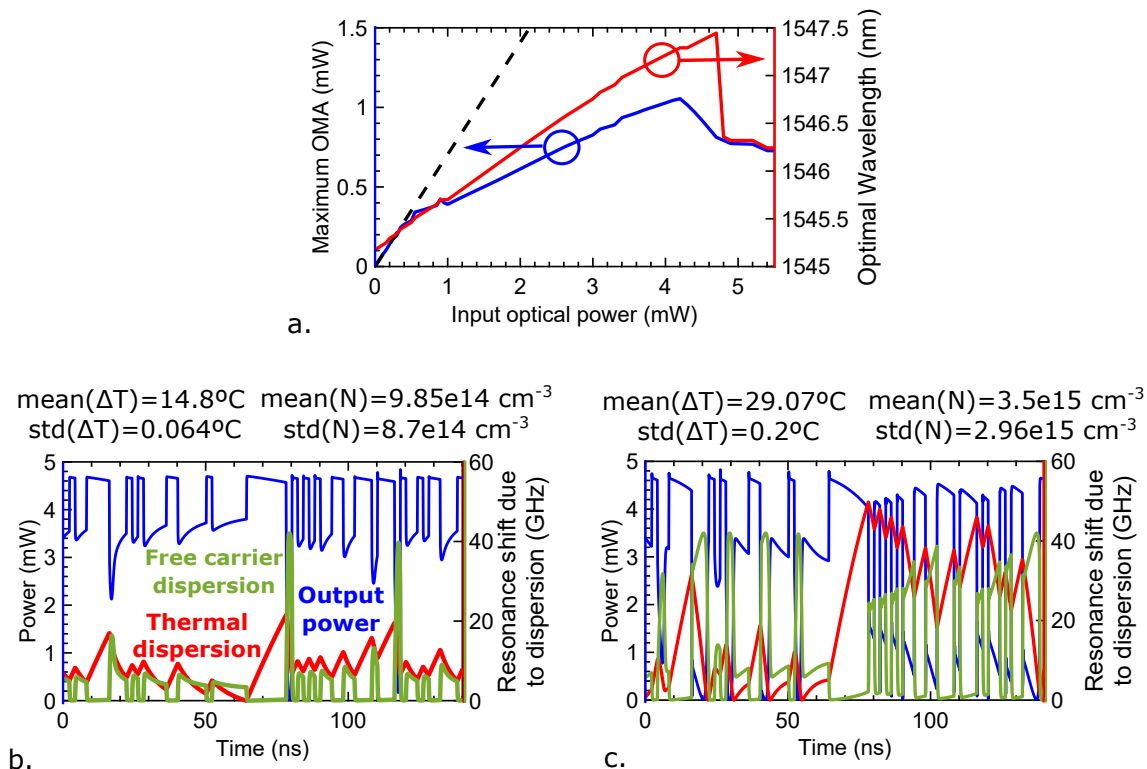
Figure 5-5: Optimal operation point for high input optical powers. (a) Maximum attainable OMA (blue, left axis) and wavelength at which this value is reached (red, right axis) as a function of input power derived with the model. The dashed line shows the expected performance if no nonlinearities were present. (b)(c) Output optical power as a function of time (blue, left axis) and resonance frequency shift due to temperature (red, right axis) and carrier density (green, right axis) fluctuations for 5 mW of input optical power at the optimal operation wavelength of 1546.32 nm (b) and with a wavelength of 1547.52 nm, closer to the resonance (c). Resonance shifts are referenced to the minimum shift for the operational condition being considered, so that the shown curves are $\Delta W_X(t) - min\{\Delta W_X(t)\}$, where X refers to either temperature or carrier dispersion. Reported temperature and carrier averages and standard deviations are calculated over a 2 μs time series.

els observed experimentally: '1' output powers show a negative slope with time due to a temperature decrease (which moves the resonance towards shorter wavelengths and thus closer to the laser wavelength, as we concluded that optimal modulation is obtained with the laser on the blue side of the resonance), while '0' output powers show a positive slope with time due to the complementary effect (as we are closer to the resonance, there is a temperature increase which moves the resonance towards longer wavelengths and away from the operating laser wavelength). Notice how experimental '0' values do not reach close to zero transmission (as shown by simulation) due to the presence of noise. As power is increased beyond the optimal point, the enhancement in thermal and carrier dispersion and corresponding '0' and '1' output power fluctuations is so high that the modulation performance decreases. To further explore the effects of high input powers over device performance, simulations were performed for input powers well above the optimum. The results are summarized in Fig. 5-5. As could be inferred from Fig. 5-3(c), the existence of an optimum input power beyond which modulation quality decreases is confirmed (Fig. 5-5(a)).

As power is increased beyond the maximum OMA point to 4.75 mW, an interesting trend is observed: the optimal operation results in bit 0 backing off from close to zero transmission (Fig. 5-5(b) for a 5 mW input power), showing that at such high powers it is necessary to keep the laser away from critical coupling in order to reduce the energy stored in the resonator and thus lower optical nonlinearities. This is also seen in Fig. 5-5(a), where the optimal wavelength moves toward shorter wavelengths for input powers above 4.75 mW (see the distinct knee in the red curve of Fig. 5-5(a)) . Figure 5-5(c) shows the resulting waveform at 5 mW input power if the laser is tuned closer to the resonance ($\lambda' = \lambda_{opt} + 800 \ pm$) and critical coupling: thermal and free carrier dispersion effects are increased to a level that leads to very strong fluctuations in the '0' and '1' bits, and degradation of the modulation quality.

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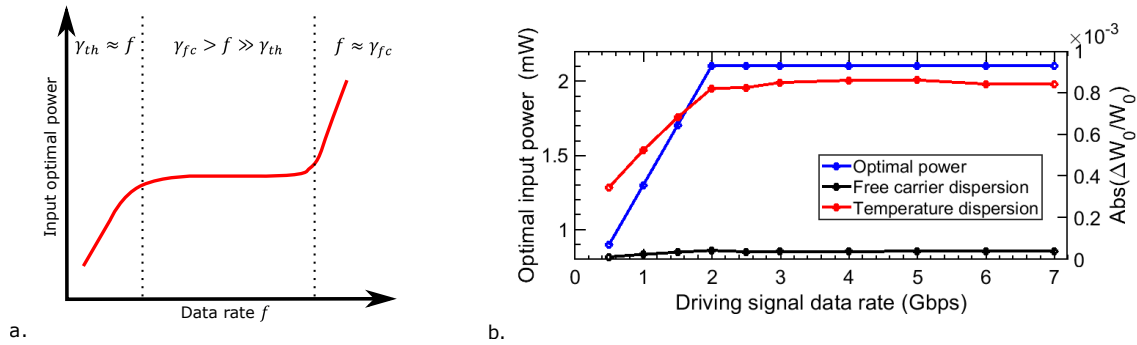
Figure 5-6: Dependence of optimal input power on data rate. (a) Qualitative behavior. An increase in power handling is expected as bit time becomes shorter than the thermal time constant and the free carrier lifetime. (b) Modeling results (blue curve). As reasoned, an increase in power handling followed by a plateau is observed. The plateau occurs when the bit time becomes much faster than the thermal response of the device, which limits the extent of thermal effects (red curve).

5.4.1 Data rate dependence

The agreement with experimental results at the modest data rates considered suggests that our theoretical model correctly captures the effects of both free carrier and thermal nonlinearities. Since modern data transmission devices work at speeds at least an order of magnitude higher than the 0.5 Gbps data rate considered in this work, it is pertinent to ask ourselves how does the behavior described here, and in particular the optimum input power, change as the data rate of the modulating signal is increased.

Figure 5-6(a) depicts the qualitative behavior we expect for the input optical power as a function of data rate. As bit time decreases well below the thermal time constant of the device ($\tau_{th} \approx 0.5\mu s$), the extent of thermal fluctuations (and thus its penalty on modulation efficiency) will decrease for the same input power due to the system's temperature not responding rapidly enough to the changes in the absorbed optical power. For the same reason, these thermal effects will become pattern

dependent, that is, temperature changes will depend on how many consecutive '0' ('1') bits does the transmitting signal have, since this will set the maximum time the system has to increase (decrease) its temperature. Thus, for the same data pattern, an increase in the input optimal power with data rate is expected as it transitions from a bit time longer or comparable to the thermal time constant ($T_b >\approx \tau_{th}$) to a much shorter bit period ($T_b \ll \tau_{th}$). The increase in optimum power will stop when the decrease in bit time does not have a significant effect in the relative magnitude of T_b with respect to τ_{th}.

At data rates in which ($\tau_{th} \gg T_b > \tau_{fc}$), only free carrier effects will limit the maximum power that the device can handle. While the bit time is smaller than the free carrier lifetime, no change in the optimum power is expected, since the free carrier response won't be limited by the time the device stays on or off resonance. But if we keep increasing the data rate to a point in which T_b becomes comparable to τ_{fc},the extent of carrier dispersion fluctuations (and thus its penalty on modulation efficiency) will decrease due to the free carrier population not being able to respond to changes in the bits being transmitted. At this point, both free carrier and thermal dispersion effects will become pattern dependent, and it is expected that for the same pattern there will be an increase in the optimum power as data rate increases.

Figure 5-6(b) shows representative results obtained with our theoretical model. As discussed, we see an increase in optimal input power with increasing data rate for low speeds, but this increase stops at data rates above 2 GHz, when changes in the bit time do not represent a significant change in the relative magnitude of T_b with respect to τ_{th} (at 2 GHz, $\tau_{th}/T_b \approx 1,000$). At such data rates, an increase in input power generates such an enhancement of the nonlinear effects that the use of shorter bit periods is not enough to compensate for this increase. This can be explained due to the much stronger dependence of nonlinear effects on input power compared

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to its dependence on bit time. Also notice how, as expected, an increase in input power is accompanied by a higher associated dispersion due to nonlinear effects at the optimal operational point (red and black curves in Figure 5-6(b)).

5.4.2 Summary

Throughout the sections above we have presented a time-domain model that describes nonlinear effects arising in silicon ring modulators under moderately high input optical powers and analyzed their effects on modulation quality. Furthermore, by comparing modeling results to experimental data we have been able to confirm the validity of the model.

We have seen how, for sufficiently high input powers, nonlinearities have a relevant impact on the resonance wavelength of the device and, as a consequence, on the output optical signal generated by the modulator. In fact, we have showed the existence of an optimal input optical power at which the best modulation performance (in terms of OMA) is achieved. Increasing the power beyond this point will degrade modulation by closing the eye diagram due to strong fluctuation in the resonance wavelength caused by thermal and free-carrier dispersion effects.

For our device, optimal powers of around 3-5 mW were obtained. Nevertheless, even for lower powers nonlinearities are relevant. For instance, we observed how fluctuations of as much as 20% in the '0' output power can occur for an input power of 2 mW (Fig. 5-4(c,d)). While the range of input optical powers used in practical systems with ring modulators is broad, powers in the range of a few mW are not rare. This model is thus useful to inform the design of practical microring modulator devices and systems needed for optical communication systems, from inter and intra-chip systems to data-center optical interconnects and telecommunications systems.

5.5 Nonlinear effects at cryogenic temperatures

So far, our analysis has dealt with typical modulation formats: large signal modulation ($\approx 4\ V_{pp}$), reverse bias and room temperature operation. Of course, it is of interest to extend the presented model to the operating conditions we have focused on in this thesis: cryogenic temperatures, small signal modulation and forward bias. This goal of this section is to study how these affect the nonlinear behavior of the devices.

5.5.1 Extending the model to low temperature operation

The derivation of the nonlinear model we have presented in this chapter is independent of the operating temperature, which makes all the equations we have used in the sections above still valid at cryogenic temperatures.

Nonetheless, most of the material and device parameters that the model uses have different values at low temperatures. Not only this, but some of these parameters are strongly sensitive to small temperature fluctuations around 4 K. For instance, the thermo-optic coefficient of silicon varies almost 3 orders of magnitude in the temperature range between 4 K and 50 K [127]. A similar effect is observed with the heat capacity of silicon [214] or silica's thermal conductivity [215]. As a consequence, our model needs to incorporate such temperature dependence when solving the system of coupled nonlinear differential equations, something that was not necessary at 300 K, where all the parameters are insensitive to small temperature fluctuations.

Table 5.2 shows the different model parameters at RT (same as in Table 5.1) and at 4 K for reverse bias operation, where we have explicitly indicated the values that are strongly susceptible to thermal fluctuations in cryogenic conditions. It is worth noting several points:

1. We have considered the plasma dispersion effect parameters (α_n, α_p, dn_{Si}/dN_n, dn_{Si}/dN_p) to be independent of temperature. Using the Drude model approximation [7], these parameters will vary with temperature since they depend on the carrier effective masses, which are themselves temperature dependent [216]. Nevertheless, such dependence is weak (< 10 % variation between 4 K and 300 K), so it has not been considered.

2. We have assumed that the resonance shape (given by γ_0, γ_{rad} and κ) does not change with temperature, which is in agreement with what we observed experimentally in Chapter 2. In accordance with our experimental results, we have also assumed no change in the modulation efficiency dW_0/dV_{pn} in reverse bias.

3. As measured in Chapter 2, we have accounted for the bandwidth decrease at 4 K through the parameters γ_{fc} and τ.

It is also important to mention the assumptions we have made for the thermal behavior of the device at cryogenic temperatures. Since the heat capacity and thermal conductivity of Si and SiO$_2$ decrease by several orders of magnitude between 300 K and 4 K [214, 215], it is hard to predict the thermal properties of our device, which in our model are captured by the thermal time constant γ_{th}. As done in [205], we will assume that $\gamma_{th} \propto k_{SiO_2}/C_{p,Si}$, where k_{SiO_2} is the thermal conductivity of the oxide surrounding the silicon layer and $C_{p,Si}$ is the heat capacity of the silicon. With this, we will assume:

$$\gamma_{th}(T) = \gamma_{th}(T = 300K)\frac{C_{p,Si}(T = 300K)}{C_{p,Si}(T)}\frac{k_{SiO_2}(T)}{k_{SiO_2}(T = 300K)} \tag{5.6}$$

Where we experimentally characterized $\gamma_{th}(T = 300K) = 2.4$ MHz. Using this

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Parameter	Units	300 K value	4 K value	Strong T dependence?	Ref.
β_{Si}	$m \cdot W^{-1}$	8.4×10^{-12}	4.25×10^{-12}	No	[217]
n_{Si}	—	3.485	3.453	No	[127]
dn_{Si}/dT	K^{-1}	1.86×10^{-4}	1×10^{-8} @ 4 K 1.5×10^{-6} @ 20 K	Yes	[127]
dn_{Si}/dN_n	cm^3	-8.8×10^{-22}	-8.8×10^{-22}	No	[100]
dn_{Si}/dN_p	cm^3	-8.5×10^{-18}	-8.5×10^{-18}	No	[100]
α_p	m^2	6×10^{-22}	6×10^{-22}	No	[100]
α_n	m^2	8.5×10^{-22}	8.5×10^{-22}	No	[100]
Γ_{TPA}	—	0.90967	0.90967	No	FEM
Γ_{FCA}	—	0.9621118	0.9621118	No	FEM
Γ_{ring}	—	0.6515	0.6515	No	FEM
V_{FCA}	m^3	8.67×10^{-18}	8.67×10^{-18}	No	FEM
V_{TPA}	m^3	10.63×10^{-18}	10.63×10^{-18}	No	FEM
γ_0	GHz	30	30	No	DC transm
γ_{rad}	GHz	11	11	No	DC transm vs power [211]
κ	$\sqrt{Hz}$	1.73×10^5	1.73×10^5	No	DC transm
n_g	—	2.73	2.73	No	FSR
dW_0/dV_{pn}	$rad/(s \cdot V)$	1.57×10^{10}	1.57×10^{10}	No	DC transm vs voltage
$C_{p,Si}$	$J/(g \cdot K)$	0.7145	1.75×10^{-5} @ 4 K 3.4×10^{-3} @ 20 K	Yes	[214]
k_{SiO_2}	$W/(cm \cdot K)$	1.1×10^{-2}	7.98×10^{-4} @ 4 K 1.37×10^{-3} @ 20 K	Yes	[215]
τ	ps	10	50	No	Bandwidth measurements
γ_{lin}	GHz	19	19	No	DC transm vs power [211]
γ_{fc}	GHz	10	3	No	Bandwidth measurements
λ_0	nm	1545.2	1550	No	Arbitrary

Table 5.2: Model parameters at 300 K and 4 K corresponding to the reverse bias operation of the 1550 nm silicon microring modulator (design C in Chapter 2). FEM = Finite Elements Method. FSR = Free Spectral Range.

approximation, $\gamma_{th}(T = 4K) = 7.3$ GHz and $\gamma_{th}(T = 30K) = 15$ MHz, i.e, a much faster thermal response is obtained at cryogenic temperatures. The reader should be aware that this is a strong assumption which, as we will discuss in detail in a later section, is most likely not accurate given the large change in the thermal properties of both Si and SiO$_2$. Heat transport simulations using Finite Element Methods along with experimental studies are necessary to develop an accurate thermal model for photonic SOI systems at cryogenic temperatures [218].

With these changes we can use our nonlinear time domain model to solve for the behavior of resonant modulators at cryogenic temperatures in reverse bias. When solving the coupled system of differential equations, we need to compute the model parameters at every single time step based on the ring state at the previous time step, since some of these (dn_{Si}/dT and γ_{th}) depend very strongly on small changes to the ring temperature.

5.5.2   Extending the model to forward bias operation

We need to include two main changes to extend the model to forward bias operation:

1. In reverse bias it is a good approximation to consider the modulation efficiency dW_0/dV_{pn} independent of the voltage applied. This is not the case in forward bias, where we experimentally saw how there is an exponential dependence between the applied voltage and the modulation efficiency (Fig. 2-6). We thus need to compute the modulation efficiency at every time step based on the voltage at the p-n junction V_{pn}:

$$\Delta W_{0_{mod}}(t_{i+1}) = \frac{dW_0}{dV_{pn}}\bigg|_{V_{pn,t_i}} (V_{pn,t_{i+1}} - V_{pn,t_i}) + \Delta W_{0_{mod}}(t_i) \qquad (5.7)$$

Where t_i is the previously computed time step, and $t_{i+1} = t_i + \Delta t$ is the time step being computed.

2. In forward bias, the presence of a current flowing through the diode results in ohmic heating, which contributes to changes in the internal temperature of the ring and to changes in the resonance wavelength of the device through the thermo-optic effect. We will add this effect as an additive term in the total power absorbed in the ring:

$$P_{abs}(t) = (\gamma_{lin} + \gamma_{TPA} + \gamma_{FCA})U(t) + V_{pn}(t)I_{pn}(t) \qquad (5.8)$$

The time dependence of the ohmic heating is likely not trivial, since changes in the internal temperature of the ring generate changes in the electrical characteristics of the diode, and as such modify V_{pn} and I_{pn}. This affects the extent of ohmic heating in the ring and, as a consequence, its temperature.

5.5.3   Steady state

The modifications outlined above allow us to extend the model to operation at 4 K and forward bias. Before analyzing how these affect the dynamic behavior of the devices, it is informative to study how do they impact the steady state conditions, i.e, the ring state when no modulation signal is applied.

Reverse bias operation at 4 K

We will first consider operation at 4 K in reverse bias, where ohmic heating is negligible since the current flowing through the diode is close to 0. Fig. 5-7 shows the results obtained when solving for the equilibrium point of the system of coupled dif-

ferential equations (i.e, finding the ring state that makes all time derivatives equal to 0).

Figures 5-7(a,c) show the evolution of the temperature rise in the device $\Delta T = T_{ring} - T_{ambient}$ as a function of laser wavelength λ_l, both at 300 K (Fig. 5-7(a)) and 4 K (Fig. 5-7(c)) for different on chip input optical powers. Similarly, Figs. 5-7(b,d) show the increase in free carrier concentration due to two photon absorption in the ring for the same conditions. Abrupt (dashed lines) and swept (solid lines) wavelength initialization (as described in Section 5.3) are shown.

Several differences between 4 K and 300 K operation are observed:

1. The rise in temperature at 4 K is much larger than at 300 K: $\Delta T > 10$ K are reached at 4 K for powers on the order of a 100 μW, while at 300 K these powers results in $\Delta T \approx 1$ K. This is better visualized in Fig. 5-7(e), which shows the maximum temperature increase for a given input optical power, both at 4 K and 300 K. Such a difference is due to the reduced thermal conductivity of SiO$_2$ and heat capacity of Si at cryogenic temperatures, which increase γ_{th} and result in a larger rise in temperature for the same input optical power to the ring.

2. While ΔT is larger at 4 K, the accompanying shift in the resonance wavelength of the ring due to the thermo-optic effect is reduced (see Fig. 5-7(f)). This is expected, and is due to the much lower thermo-optic coefficient of silicon at cryogenic temperatures (see Fig 1-7(d)).

3. At 4 K there is no significant difference in the achieved steady state using abrupt and swept wavelength initialization, even for high input optical powers. This is due to the reduced impact of thermal dispersion at 4 K, which eliminates

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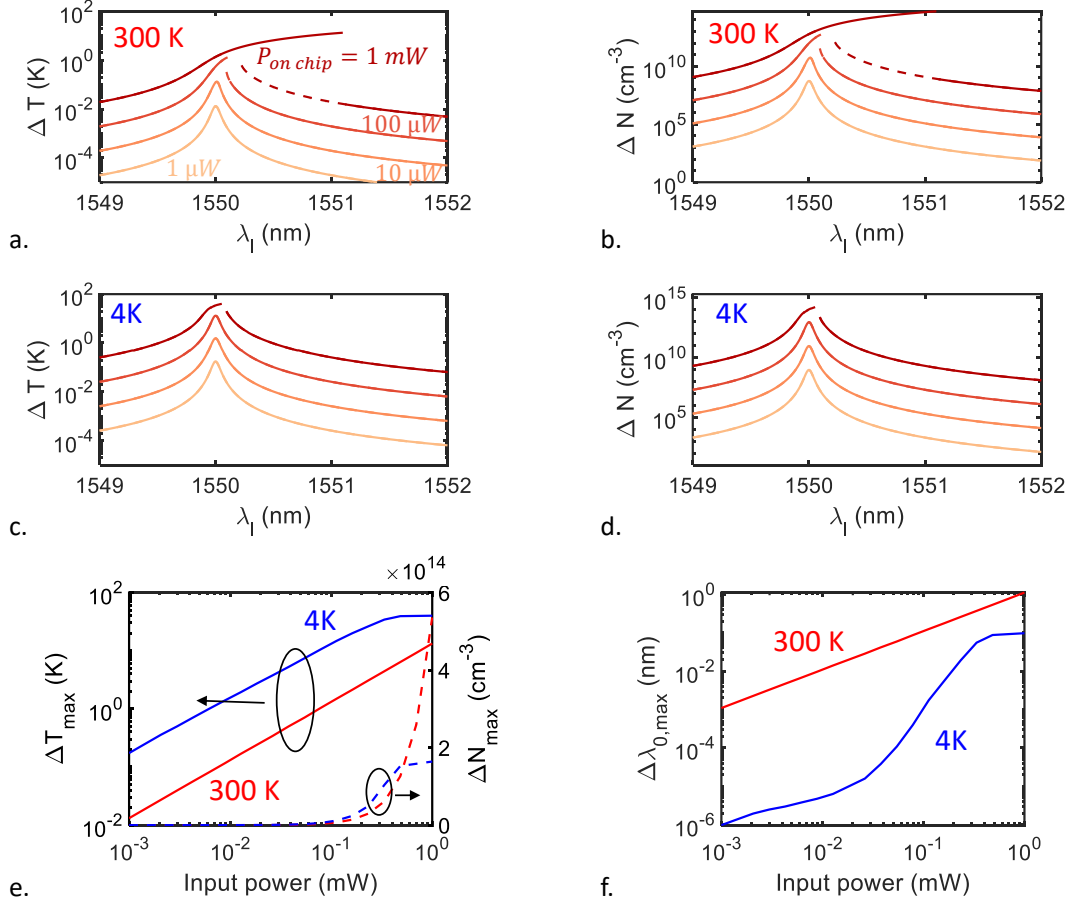
Figure 5-7: Equilibrium states for a reverse biased resonant modulator at 4 K and 300 K. (a) Temperature increase in the ring $\Delta T = T_{ring} - 300K$ as a function of laser wavelength λ_l for different on chip optical powers at room temperature. Dashed lines correspond to abrupt wavelength initialization, and solid lines to swept wavelength. (b) Free carrier density due to two photon absorption at 300 K. (c) Temperature increase in the ring $\Delta T = T_{ring} - 4K$ as a function of laser wavelength λ_l for different on chip optical powers at 4 K. Swept wavelength and abrupt initialization result in the same equilibrium state. (d) Free carrier density due to two photon absorption at 4 K. (e) Maximum increase in temperature (left axis) and free carrier density (right axis) as a function of on chip input optical power at 4 K (blue) and 300 K (red). Larger ΔT are obtained at 4 K due to decreased thermal conductivity and heat capacity. (f) Maximum resonance wavelength shift at the equilibrium point at 4 K (blue) and 300 K (red). Smaller shifts are obtained at 4 K due to the decrease in thermo-optic coefficient.

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the need of tracking the movement of the resonance (which is necessary at 300 K as discussed in Section 5.3).

These observations have important implications for the operation of resonant modulators at 4 K. First, we need to be aware of the fact that, although the cryostat is at 4 K, the modulator is locally at a temperature between 1 K and 30 K larger depending on the input optical power. This represents a 25% - 750% increase in temperature, which has significant effects on the material parameters and the electrical characteristics of our device. Second, we do not expect large shifts in the resonance wavelength of the modulator due to local heating, which eliminates the need for swept wavelength initialization.

Forward bias operation at 4 K

As discussed above, the main effect of forward bias operation (both at 4 K and 300 K) in the steady state of the system is the addition of an additional power dissipation term corresponding to ohmic heating $P_{ohm} = I_{pn}V_{pn}$.

This adds yet another degree of complexity to the system, since there is a feedback effect between the current flowing through the diode and its temperature: the application of a forward bias current generates ohmic heating, causing an increase in device temperature which in turn affects the current flowing through the diode (since I_{pn} is strongly temperature dependent: $I_{pn} = I_s(T)(exp(qV/kT) - 1)$).

It is thus interesting to analyze how the current through a diode depends on its temperature for a fixed bias voltage V_{bias}. This is shown in Fig. 5-8(a) at 300 K and in Fig. 5-8(c) at 4 K [4]. As is apparent, when the voltage is fixed, small changes in temperature generate very large changes in current, especially at 4 K (where an

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[4]We used the diode equation $I_{diode} = I_s(T)*(exp(qV/nkT)-1)$ with n = 2. $I_s(T)$ was calculated as outlined in Appendix A.2.

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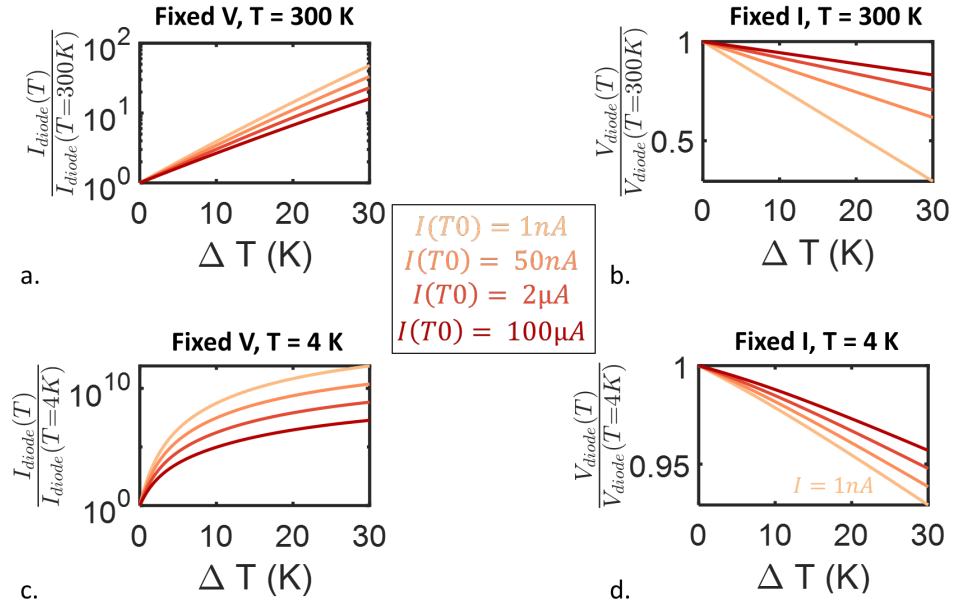
Figure 5-8: Fixed voltage versus fixed current operation of forward biased modulators. (a) Change in diode current for a fixed voltage at temperatures around T0 = 300 K. (b) Change in voltage for a fixed current at temperatures around T0 = 300 K. (c) Change in diode current for a fixed voltage at temperatures around T0 = 4 K. (d) Change in voltage for a fixed current at temperatures around T0 = 4 K. The current at fixed voltage operation is much more sensitive to small temperature fluctuations than the voltage at fixed current.

almost 5 order of magnitude increase in current occurs between 4 K and 8 K - Fig. 5-8(c)).

Since we expect changes in the local temperature of the device both due to ohmic heating and nonlinear effects, it is clear that fixed voltage operation is not suitable in forward bias conditions, as in this case we would observe very large current fluctuations that would compromise the stability and correct operation of the device.

On the contrary, fixed current operation should be used in forward bias. Figs. 5-8(c,d) show the fluctuations in the applied voltage to keep a fixed current at temperatures around 300 K and 4 K, respectively. We can see how changes smaller than

50% at 300 K and smaller than 10% at 4 K are needed to maintain a fixed current, which results in improved device stability.

It is of interest to check if the presence of ohmic heating in current driven forward biased diodes has a significant effect on the steady state of the device. The results are shown in Fig. 5-9, where two regimes can be identified:

1. For low input optical powers or wavelengths far from the resonance ohmic heating dominates, so the device temperature depends strongly on the bias current. This is apparent in Figs. 5-9(c,d), where for low input optical powers, ΔT and $\Delta \lambda_0$ only depend on bias current.

2. For high enough input optical powers and wavelengths close to the resonance, heating due to FCA, TPA and linear absorption dominate over ohmic heating, and therefore bias current does not significantly affect the temperature of the device. This is clearly visible in Figs. 5-9(c,d), where for high input optical powers all curves show the same ΔT and $\Delta \lambda_0$ independent of the bias current.

The existence of these two separate regimes indicates that there is not a strong interaction between the nonlinear effects (TPA and FCA) and the extent of ohmic heating, which allows us to treat both phenomena as nearly independent. This is because the heating associated with the bias current flowing through the device is almost independent of any temperature fluctuation generated by nonlinearities: when using constant current drive (as shown in Fig. 5-8), temperature changes generate small changes in the applied voltage V_{pn}, and thus small changes in $P_{ohm} = I_{bias}V_{pn}$ (a temperature change of 1 K generates $< 5\%$ change in V_{pn}, and thus a $< 5\%$ change in P_{ohm}). Since the feedback effect between temperature and ohmic heating is small, the stability of the ring state is not compromised.
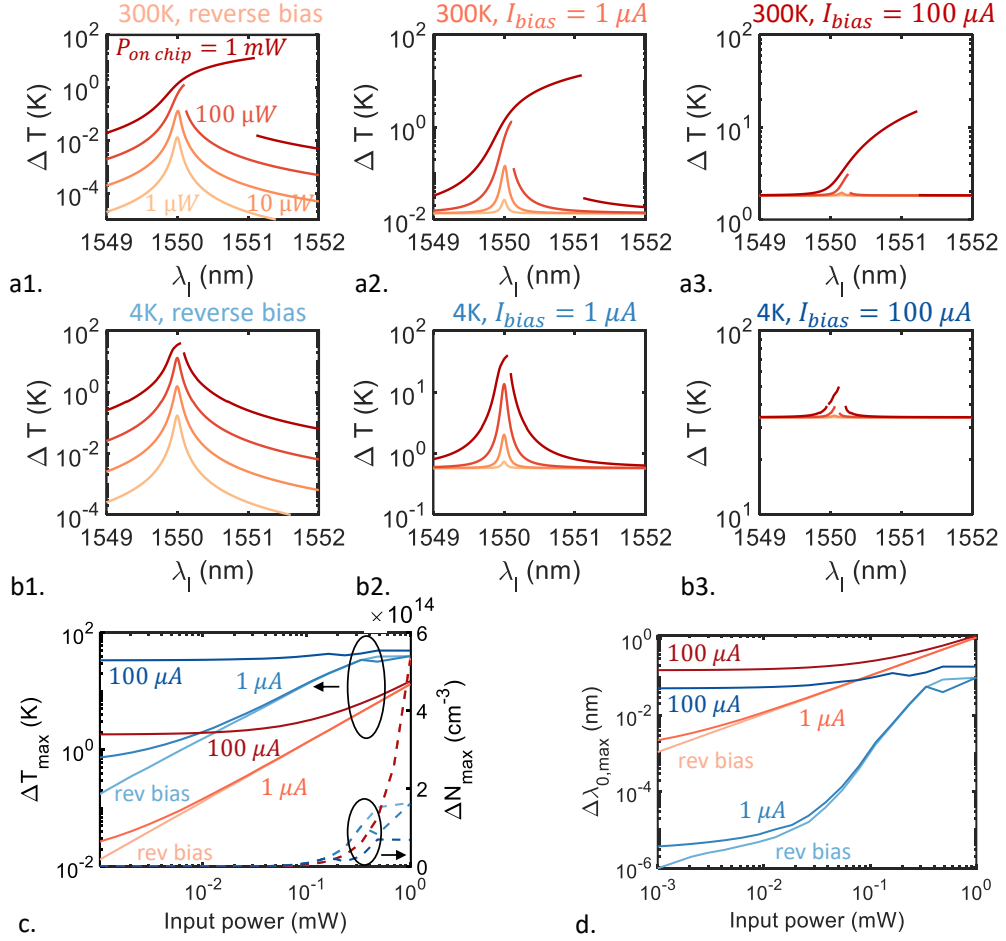
Figure 5-9: Equilibrium states for a forward biased resonant modulator at 4 K and 300 K. (a) and (b) show the temperature increase in the ring as a function of laser wavelength λ_l for different on chip optical powers at 300 K (a) and 4 K (b). '1' corresponds to reverse bias operation, '2' to a 1 μA forward bias current and '3' to a 100 μA forward bias current. (c) Maximum increase in temperature (left axis) and free carrier density (right axis) as a function of on chip input optical power at 4 K (blue) and 300 K (red) for the same bias conditions as (a) and (b). (f) Maximum resonance wavelength shift as a function of on chip input optical power at 4 K (blue) and 300 K (red). Ohmic heating dominates at low input optical powers and wavelengths far from the resonance, but nonlinear heating due to FCA and TPA dominates at high input optical powers and wavelengths close to the resonance.

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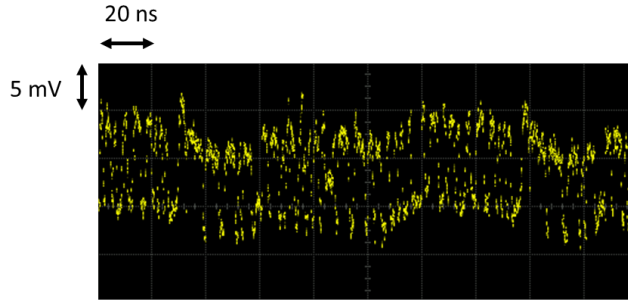
$$f = 1\ Gbps\ ;\ V_{bias} = -4\ V$$
$$V_{pp} = 5\ V\ ;\ P_{on\ chip} = 200\ \mu W$$

Figure 5-10: Nonlinear effects in experimental waveforms at 4 K. Very strong fluctuations in the '1' and '0' output levels are observed.

5.5.4 Dynamic evolution

Now that we have studied how the change in material parameters and the presence of nonlinearities affect the steady state of our resonant modulators at 4 K, it is time for us to study their dynamic evolution under the same conditions. Our goal is to reproduce the experimental observations we presented in Section 2.4.1. There, we discussed how we observed stronger fluctuations in the generated modulation signal compared to room temperature operation, which we attribute to an enhancement in the nonlinear effects occurring in the device.

Figure 5-10 shows an example experimental waveform corresponding to a 1 Gbps, 4 V_{pp} PRBS 7 signal at -4 V reverse bias and 200 μW of on chip input optical power. Very strong fluctuations on the '1' and '0' output power levels are observed, which are almost as large as the average OMA of the signal ($\Delta P_1 \approx \Delta P_0 \approx < P_1 - P_0 > \approx 5mV$).

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Back of the envelope calculations

Before jumping right into the simulations of the dynamic behaviour of our modulators at 4 K using the nonlinear model, it is of interest to do some back of the envelope calculations to get an estimate for the strength of the thermal fluctuations we should expect.

We can estimate the point at which nonlinearities will fatally affect modulation by calculating the temperature change ΔT needed to make the resonance shift due to the applied external voltage be the same as the resonance shift due to the the thermooptic effect (a situation close to what we observed in Fig. 5-10):

$$\frac{dW_0}{dV} V_{pp} = \frac{W_0}{n_{Si}} \int_{T0-\Delta T/2}^{T0+\Delta T/2} \frac{dn_{Si}}{dT} dT \tag{5.9}$$

Where the integral is necessary due to the strong temperature dependence of the thermooptic coefficient of silicon at cryogenic temperatures. At temperatures around 300 K the thermooptic coefficient is constant with temperature, and Eq. 5.9 reduces to:

$$\frac{dW_0}{dV} V_{pp} = \frac{W_0}{n_{Si}} \frac{dn_{Si}}{dT} \Delta T \tag{5.10}$$

Evaluating the equation above for our ring (see Table 5.1) and a $V_{pp} = 4$ V, we obtain $\Delta T = 0.97$ K. This means that, at ambient temperature, fluctuations of 1 K in the internal ring temperature due to nonlinear effects will generate as large a shift in its resonance wavelength as that generated by the driving voltage, severely affecting the OMA of the modulated signal. Of course, nonlinearities will affect modulation performance for temperature fluctuations much lower than this.

A more careful analysis of Eq. 5.9 is required at cryogenic temperatures. As we
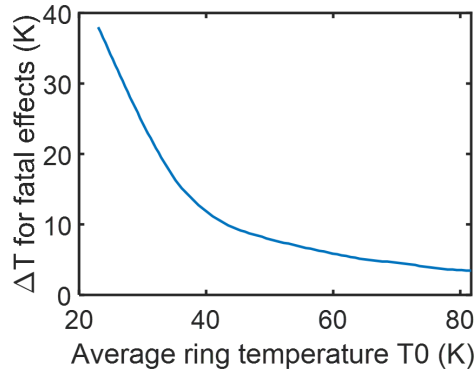
Figure 5-11: Necessary temperature fluctuation for fatal effects on modulation quality at cryogenic temperatures. This is the ΔT that makes the thermooptic resonance shift as large as the shift due to the external applied voltage. At temperatures around 300 K, the necessary temperature fluctuation is $\Delta T = 1$ K (see text).

have seen in the previous section, at 4 K the average temperature in the ring $T0$ is greatly dependent on the input optical power and operating wavelength, and can be as large as ≈ 50 K. Due to the large variation of dn_{Si}/dT at cryogenic temperatures, a different thermo-optic shift will be obtained for the same ΔT depending on the actual value of $T0$.

Therefore, at cryogenic temperatures we need to solve for ΔT in Eq. 5.9 as a function of the average operating temperature $T0$. This is shown in Fig. 5-11 for our ring parameters (see Table 5.2) and $V_{pp} = 4$ V. Because of the reduced thermo-optic coefficient of Si at cryogenic temperatures, much larger temperature fluctuations (on the order of 10 K) are needed compared to 300 K operation (where $\Delta T = 1$ K is enough) for the thermo-optic shift to become as large as that due to the external voltage. Nevertheless, we expect to observe larger temperature fluctuations at low temperatures due to the increase in γ_{th}. Thus, it is possible that, at 4 K, nonlinear effects impact modulator performance at lower input optical powers.

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Dynamic simulations: the need for an improved thermal model

Looking at the experimental waveforms we obtained experimentally (such as the one in Fig. 5-10) and the back of the envelope calculations we did above, we would expect our nonlinear model to predict temperature fluctuations on the order of 10 - 20 K and average temperatures around 30 K for low input optical powers on the order of 100 μW.

Figure 5-12 shows the simulation results corresponding to a 200 μW on chip input optical power and the same operational conditions as the experimental waveform in Fig. 5-10. The modulation OMA and the output '1' and '0' powers are shown as a function of laser wavelength in Fig. 5-12(a) and (b), respectively. Fig. 5-12(c) shows the average temperature (solid line) and the temperature fluctuations around it (shaded bands). The same is shown for the free carrier density in Fig. 5-12(d).

Figure 5-12(e) shows the maximum resonance shift ΔW_0 due to the external driving signal (black), thermal effects (red) and free carrier effects (blue). Both thermal and free carrier effects are more than an order of magnitude lower than the external applied signal, which indicates that nonlinear effects are not significant for this operational conditions. As we derived above, temperature fluctuations in the order of 10 - 20 K are necessary for thermal effects to become comparable to the effect of external modulation, but our model predicts fluctuations < 7 K for the 200 μW input power.

Clearly, these results are not consistent with our experimental observations, which show a large impact of nonlinear effects for a 200 μW input optical power. This suggests that our time domain model is not accurate at cryogenic temperatures. Several reasons could explain this:

1. The dominant physical effect generating the fluctuations of the '1' and '0'

$$P_{on\ chip} = 200\ \mu W, T_0 = 4\ K$$
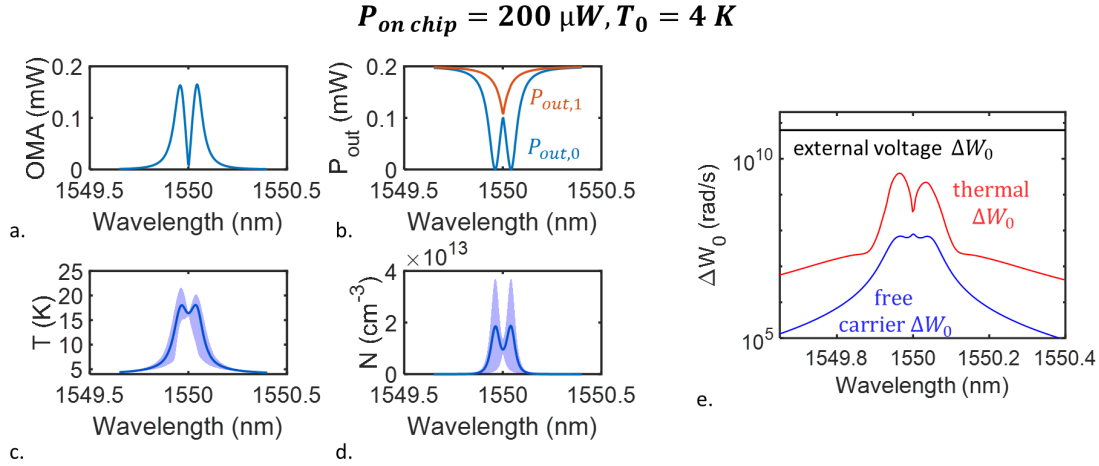
Figure 5-12: Dynamic simulation of modulator operating at 4 K with a 200 μW on chip input optical power as a function of laser wavelength. (a) OMA. (b) Output optical power for bit '1' (orange) and '0' (blue). (c) Average temperature (solid line) and temperature fluctuations (shaded bands). (d) Average free carrier density (solid line) and its fluctuations (shaded bands). (e) Maximum resonance wavelength shift due to the applied external voltage (black), thermal fluctuations (red) and free carrier variations (blue). At this input power, nonlinear effects do not have a significant impact in the performance of the modulator.

output powers at low temperatures is not included in the model. We have overlooked several phenomena in our model at cryogenic temperatures. For example, we have not accounted for the effect of temperature fluctuations in the diode characteristics or in the modulation efficiency, or how nonlinear effects can impact the extent of carrier freezeout in the devices.

Nevertheless, all these effects are likely to be significant in forward bias operation, but not in reverse bias, where the electrical behavior of the diode should not largely affect the optical modulation.

2. A more likely explanation for the inaccuracy of our model is that it does not correctly predict the thermal behavior of our system at cryogenic temperatures.

Several assumptions are implicit in the simple equation we use to describe the thermal dynamics in our system (Eq. 5.2).

Amongst them, the fact that the system can be described by a simple RC-like behavior with a single time constant, which is most likely not accurate even at room temperature [219]. Additionally, the definition of γ_{th} described in Eq. 5.6 assumes that the heat conduction is dominated by the thermal response in the SiO_2 and overlooks any effects of heat propagation in the Si, which could be inaccurate at cryogenic technologies due to its reduced thermal conductivity. Additionally, this model assumes that the temperature in the silicon is near uniform, which is most likely not true at cryogenic temperatures due to the very small heat capacity of Si. It is also important to mention that the thermal properties of the thin (< 100 nm) Si layer present in our devices are probably different than that of bulk Si [220], which we have used.

It thus seems highly likely that the simple thermal model used in our simulations is not correct at cryogenic temperatures, which explains why our model cannot reproduce our experimental observations. Thus, an accurate study of the thermal (and electro-thermal) behavior of silicon and SOI systems at cryogenic temperatures through modeling and experiment is needed. It is worth mentioning that at such low temperatures Fourier heat transfer (which is the standard model in commercial Finite Element software) is not valid, and more sophisticated heat transfer models such as the Two Temperature Model (TTM) equations are needed [221–223].

Being aware of how the model fails to capture the correct thermal behavior of the system at cryogenic temperatures, it is still interesting to study its predictions on how high input optical powers affect the extent of the nonlinearities in our device.

The results for 3 different input optical powers are shown in Fig. 5-13 for both
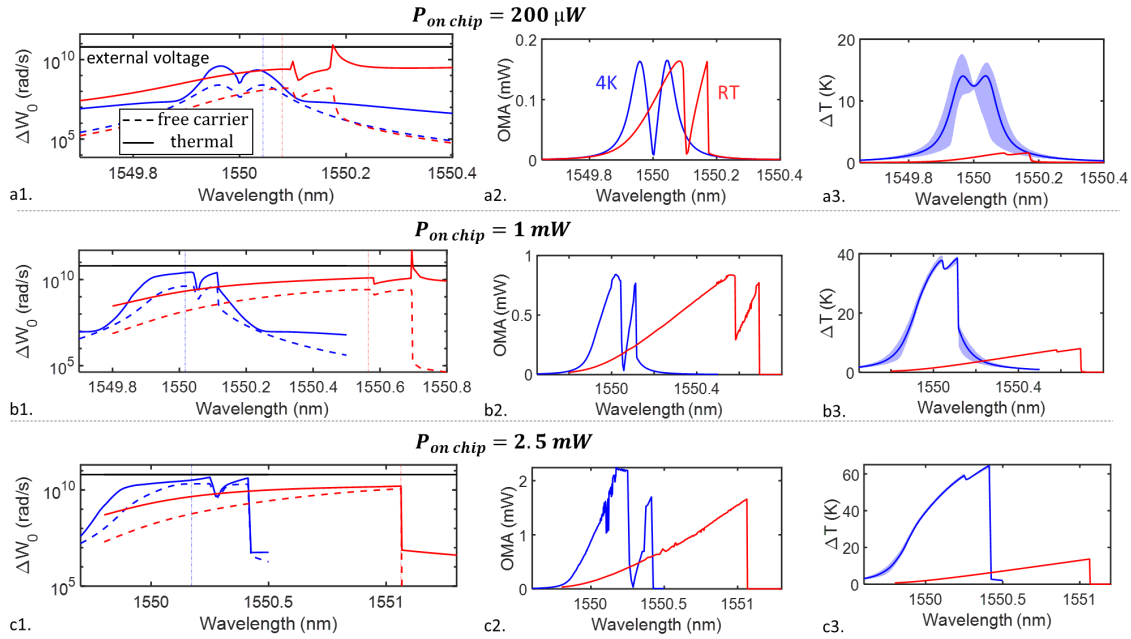
Figure 5-13: Optical power dependence of nonlinearities at 4 K and 300 K. Three different on chip input optical powers are shown: (a) 200 μW, (b) 1 mW and (c) 2.5 mW. For each power, (1) shows the resonance shift ΔW_0 due to the external voltage (black), thermal fluctuations (solid line) and free carrier fluctuations (dashed line). The vertical lines show the operation wavelength that gives maximum OMA. (2) shows the modulation OMA; and (3) the average temperature increase (solid line) and its fluctuations (shaded bands). For all plots, red corresponds to 300 K operation and blue to 4 K operation.

300 K (red) and 4 K (blue) operation. Several trends are observed:

1. As expected, both at 300 K and 4 K an increase in the input optical power is accompanied by an increase in the temperature fluctuations and the dispersion due to thermal and free carrier effects.

2. Much larger temperature fluctuations are observed at 4 K compared to 300 K operation. This is consistent with what we observed when analyzing the steady state solutions, and is due to the larger γ_{th} at cryogenic temperatures. As we

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discussed above, we expect the actual temperature fluctuations at 4 K to be larger than those shown in Fig. 5-13 due to the inaccurate thermal model we are using.

3. Interestingly, the resonance shift ΔW_0 due to nonlinear effects (Fig. 5-13, (1) plots) is larger at 4 K than at 300 K at the operating wavelength with maximum OMA. At first, we would expect this to mean that the maximum achievable OMA is reduced at 4 K, but we can see how it is actually the opposite (Fig. 5-13(c2)): for large input optical powers, larger OMA is achievable at 4 K compared to 300 K, even though the maximum shift due to thermal and free carrier effects is larger. This is due to the fact that the thermal response is 100x-10x faster (depending on the actual ring temperature $T = 4K + \Delta T$) at cryogenic temperatures compared to 300 K, which means that the compensation between free carrier and thermal effects is much faster [5]. As a consequence, at low temperatures thermal dispersion is quickly compensated by free carrier dispersion and viceversa, which reduces the overall effect of nonlinearities. This does not happen at 300 K due to the very different time scales of free carrier ($\approx$ ns) and thermal ($\approx \mu$s) effects.

While informative, these observations should be taken with care. As argued before, it is necessary to develop an accurate model to describe the thermal behavior of our system at cryogenic temperatures, since we were not able to recover our experimental observations with the model as is.

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[5]The reader should remember that thermal dispersion moves the resonance in the opposite direction that free carrier dispersion does. An increase in temperature red shifts the resonance, while an increase in free carrier density blue shifts it.

5.6 Conclusion

In this chapter we have presented a time domain model to describe the dynamics of resonant optical modulators subject to nonlinear effects, which can have a significant impact on modulation performance. Our model accounts for two photon absorption and free carrier absorption, and the thermal and free carrier dispersion effects arising as a consequence. These affect in a non-trivial manner the resonance wavelength of the modulator and, as a consequence, the output optical waveform and the quality of data communication.

In the first part of this chapter we have analyzed the effects of high input optical powers on resonant modulators in conventional operating conditions: 300 K , reverse bias and large signal modulation. We have demonstrated the existence of a limit in the maximum input optical power that a resonant modulator can handle: powers above such limit will result in decreased performance due to strong fluctuations in the device resonance wavelength cause by enhanced nonlinear effects. We have also compared our model to experimental results and shown good agreement.

In the second part of this chapter we have attempted to extend the model to describe operation at cryogenic temperatures and forward bias conditions. We described the necessary changes and implemented them, but we could not reproduce our experimental observations. We attribute this to the inaccuracy of the simple model we use to describe the thermal behavior of the system. We anticipate that our devices have complex thermal dynamics at cryogenic temperatures due to the very large change in the thermal parameters of the materials involved (Si and SiO_2) and its strong temperature dependence.

Nevertheless, several important observations were made. We recognized the importance of current biasing the device when operating modulators in forward bias,

and demonstrated how ohmic heating does not have a significant interaction with other thermal effects arising from free carrier and two photon absorption. Finally, we also recognized how at cryogenic temperatures the local temperature of the ring is most likely between 1 and 40 K larger than that of the cryostat, depending on the operating wavelength and the input optical power. This has important implications on the electrical behavior of the system, and needs to be considered for an accurate description of the modulator operation at cryogenic temperatures.

Chapter 6

Conclusions and Future Work

In this thesis we have performed a substantial amount of work to understand and characterize the operation of silicon optical modulators at low temperatures for its use in cryogenic readout.

- In Chapter 1 we have presented the cryogenic readout problem and argued why optical communications are a promising alternative to overcome the limitations of conventional electrical readout (mainly, a large power consumption and a limited escape bandwidth). In addition, we have identified the main challenges for cryogenic optical readout: the changes in material properties at low temperatures, which cause large deviations from the behavior of electro-optic devices at room temperature; the need of functioning with the mV and sub-mV electrical signals generated by the cryogenic circuits; and the need to minimize optical and electrical energy dissipation to the sub-fJ/bit level.

- In Chapter 2 we have experimentally characterized zero-change CMOS resonant modulators at cryogenic temperatures. We have confirmed that the devices are still operational, both electrically and optically, but we have identified

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important differences with respect to room temperature operation. Mainly, we have seen how the electrical behavior deviates from what one would expect for a close to ideal diode, and how carrier freezeout has a significant impact in the high speed response of the devices in reverse bias. In this chapter we have also identified forward bias operation as a promising regime for cryogenic readout, since it allows for large modulation efficiencies and low input impedances at reduced electrical power dissipation compared to 300 K.

- In Chapter 3 we have demonstrated for the first time cryogenic optical read-out of a superconducting device. By exploiting the advantages of forward bias operation of our CMOS resonant modulators, we achieved optical modulation with the 2 mV electrical driving signal generated by the superconducting detector. We demonstrated a 25 fJ/bit electrical energy dissipation, which is 100x lower than that of any cryogenic readout scheme demonstrated to date.

- In Chapter 4 we have introduced, simulated and experimentally characterized a new operational regime for optical modulators which we call photovoltaic operation. By leveraging the photocurrent generated in the modulator to bias a transistor at a point where it acts as a common source amplifier, we were able to demonstrate optical modulation with an electrical energy dissipation as low as 4 zJ/bit, close to 1,000x lower than any modulator demonstrated to date.

- In Chapter 5 we have developed a theoretical model to describe the dynamic behavior of silicon ring resonators under input optical powers that make non-linear effects significantly impact device behavior. We have used the model to show how resonant modulators have a power handling limitation due to

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nonlinear effects, and experimentally confirmed such observations.

We have also attempted to use the model for operation at cryogenic temperatures, but recognized its failure to capture the complex thermal dynamics of our system, caused by the large change in material parameters at such temperatures. Nevertheless, we have shown how the local temperature of the ring is likely between 1 and 40 K above the cryostat temperature, and recognized the importance of current biasing the device in forward bias to avoid large fluctuations in the operating point, which would otherwise occur if using voltage bias.

Figure 6-1 shows how the devices presented in this thesis compare to cryogenic readout devices and architectures reported in the literature. It is clear that substantial improvements have come out as a result of this thesis.

There is, nevertheless, a significant amount of work yet to be done, as well as several research directions worth pursuing, which we will discuss briefly in the following sections.

6.1 Characterization of silicon modulators at cryogenic temperatures

Chapter 2 of this thesis dealt with the electrical, optical and electro-optical characterization of our CMOS photonic modulators at cryogenic temperatures. We identified how operation at these temperatures has significant effects on device behavior, which deviates from that at room temperature or that expected from simple diode theory. While we proposed several explanations for such deviations, further experimental
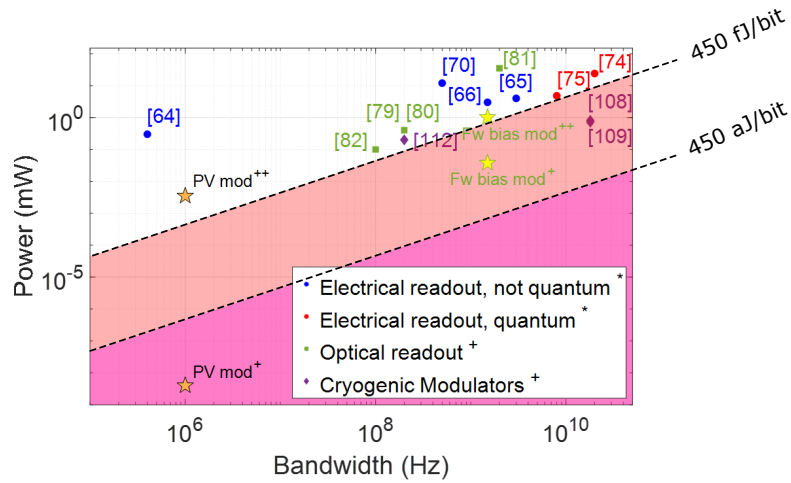
a.
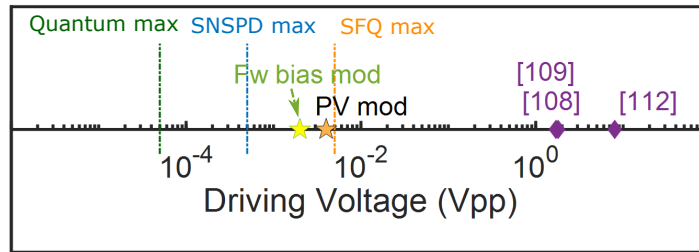
b.

Figure 6-1: Comparison of the cryogenic systems and devices presented in this thesis with previously demonstrated cryogenic modulators and readout schemes. (a) Bandwidth and electrical power consumption. Our readout through forward biased modulators has the lowest power consumption of all cryogenic readout demonstrations reported in the literature. While it has a low bandwidth, our PV modulator has close to 7 orders of magnitude lower electrical energy dissipation than previously demonstrated cryogenic modulators. (b) Peak to peak voltage. Both the forward biased modulator and the PV modulator can modulate an optical carrier with 2 orders of magnitude lower peak to peak voltages compared to devices reported in the literature. Caveat: our PV modulator has only been experimentally characterized at room temperature.

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work is needed to confirm such hypothesis and understand them better. Of particular importance are:

- Further characterizing the diode behavior at temperatures around 4 K, identifying the physical carrier transport mechanisms dominating the IV response at these temperatures and understanding the effects of local heating of the device.

- Characterizing how optical power and applied electric field affect impurity ionization and carrier freezeout, and relate it to device resistance and frequency response.

- Obtaining basic material parameters for our devices at cryogenic temperatures, such as carrier lifetime, mobility and diffusion coefficient. Additionally, given that our devices are made in a thin silicon layer with thickness < 100 nm, understanding how surfaces affect device behavior at low temperatures.

Parallel to the experimental characterization outlined above, it is of paramount importance to develop reliable models describing device behavior to inform device and system design.

6.2 Forward bias operation of silicon modulators at cryogenic temperatures

In Chapter 2 we identified the benefits of forward bias operation for cryogenic readout: very large modulation efficiencies and low input impedances at a relatively low electrical energy dissipation.

As we discussed, if the device behaved as an ideal diode, operation at 4 K should result in energy gains nearly 10x larger than what we measured experimentally.
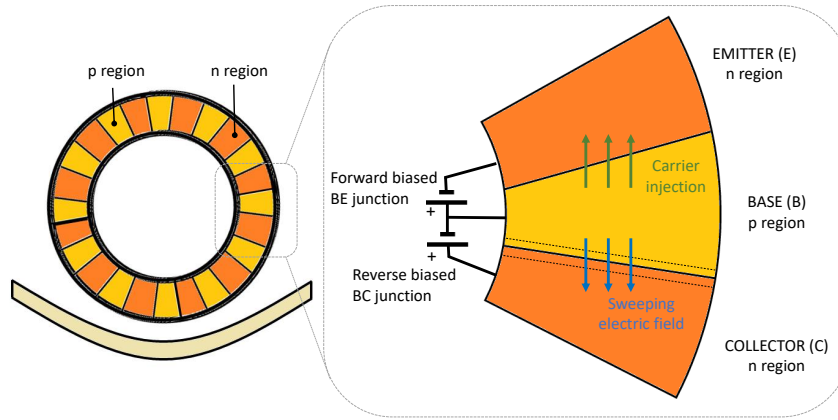
Figure 6-2: BJT modulator concept. The addition of the reversed biased base - collector junction creates a sweeping electric field that removes the carriers from the forward biased base - emitter junction. This way, a high modulation efficiency is achieved (through carrier injection in the B-E junction) where the speed of the device is only limited by the time it takes the B-C junction to sweep the carriers away from the base (as opposed to being limited by minority carrier recombination as is the case in a conventional forward biased modulator).

Understanding the reason for this difference (which is strongly related to the work described in Section 6.1) and proposing techniques and designs to approach the theoretical limit is the natural next step for improving the performance of forward biased cryogenic modulators.

On a different note, the main disadvantage of forward bias operation is its relatively low bandwidth, which is limited to the neighborhood of 1 GHz due to the relatively long minority carrier lifetime. Proposing new device concepts capable of overcoming this limitation is important to extend the use of forward biased modulators to applications where high speed is essential such as SFQ-based high performance computing.

A possibility to break the bandwidth limitation is to transform the device from

being carrier lifetime limited to being transit-time limited, i.e, to design a device where the carriers are swept away from the active area by, for example, an electric field. We have developed a device concept that could achieve such a behavior, that we call a BJT modulator (Fig. 6-2). The basic idea of this device is to achieve carrier injection (and therefore high modulation efficiency) through forward biasing the Emitter-Base (EB) junction. By simultaneously reverse biasing the Base-Collector (BC) junction, a high electric field is created that can sweep the carriers away from the base region. This way, the turn-off transient of the modulator is not dominated by the recombination time, but by the time it takes the carriers to be swept away from the base to the collector. In other words, the frequency response of the device is only limited by the transit time of carriers in the base, which is given by $\tau \approx W_B^2/2D_B$, where W_B is the base width and D_B is the diffusion coefficient of the minority carriers in the base. For a short enough base W_B, transit times < 0.1 ns can be achieved. While potentially faster, this device will have a smaller modulation efficiency compared to a conventional forward biased modulator, since only half of the p-n junctions (those corresponding to EB junctions) contribute to modulation. While promising, further work on device modeling and design is necessary to confirm the feasibility of this approach.

6.3 Cryogenic readout through silicon modulators

In Chapter 3 we demonstrated how cryogenic readout can be achieved through forward biased modulators. While our results serve as a proof of concept demonstration, substantial work is necessary to improve performance and obtain a better understanding of the tradeoffs, benefits and disadvantages of optical readout and how it compares to its electrical counterpart.

As discussed in Chapter 3, an improvement in system packaging would result in a significant performance improvement. First, minimizing the parasitic capacitance of the SNSPD package would result in a faster system. Second, and most importantly, minimizing optical coupling losses into and out of the chip through the optimization of the grating couplers and a refined fiber attach process would result in improved photon detection efficiency and a decrease in the necessary input optical power (and thus a decrease in the readout power dissipation).

From a system perspective, and discussed in Chapter 1, SNSPD readout requires very low timing jitter. It is thus of interest to study, both experimentally and through modeling, the timing characteristics of optical readout and how they compare to conventional electrical readout.

In the readout demonstration in Chapter 3 we used a UV SNSPD, which was advantageous because of its large hotspot resistance, large switching current, high critical temperature and insensitivity to 1550 nm light, which avoided scattered readout light to generate counts on the SNSPD. The extension of our readout architecture to infrared (IR) SNSPDs is of great interest, since these are more widely deployed and have a larger application space. Because the operating principle of an SNSPD is the same regardless of its operating wavelength, the readout architecture we presented in Chapter 3 can be extended to any SNSPD. Nevertheless, additional constraints arise when operating with an IR SNSPD:

1. Scattered readout light could generate counts on the SNSPD. Several approaches exist to minimize this crosstalk. For instance, the use of a lens tube (or some other physical barrier) to isolate the SNSPD from the readout light (as shown in Fig. 3-7) should prevent most of the readout photons from impinging on the SNSPD. Additionally, reducing optical coupling losses would

allow for an approximate three orders of magnitude reduction in the necessary input power for readout, further decreasing the number of scattered photons.

2. Typical IR SNSPDs have a lower switching current (≈ 4 μA) and a lower hotspot resistance (≈ 1 $k\Omega$) than UV SNSPDs, which would decrease the generated driving signal at the modulator to less than 1 mV. This could be compensated by an increase in the SNR of the readout signal, which would decrease the optical transmission change necessary for the detection of a pulse. Additionally, the modulator bias current could be increased so that a higher modulation efficiency is achieved, or the sensitivity of the receiver chain increased (for example, by using a coherent detection scheme).

3. Typical IR SNSPDs have a lower critical temperature than UV SNSPDs, and are usually operated at < 1 K, where the available cooling power is highly constrained. We believe our forward biased optical modulators could operate at 1 K due to the ionization generated by the DC bias currents and the input optical power, which decreases the impact of carrier freezeout. Nevertheless, additional work is necessary to ensure that the modulator power consumption is low enough to be compliant with the available cooling power at this temperature stage. Alternatively, the readout modulator could be operated at the 4 K stage and connected to the 1 K stage through a high speed microwave cable, which would present a minimal heat load due to the small temperature difference between the two stages.

It is also of interest to extend our readout architecture to other cryogenic technologies beyond SNSPDs. Extension to SFQ readout requires the development of faster cryogenic modulators (as outlined in Section 6.2) with bandwidths close to 10

GHz. For applications in quantum computing, where signal fidelity is paramount, a careful study of the noise characteristics of cryogenic optical readout is needed.

6.4 Photovoltaic modulators

In Chapter 4 we demonstrated a new modulator concept capable of achieving optical modulation with electrical power dissipation in the zJ/bit range. We experimentally characterized the device at 300 K and predicted its behavior at 4 K. It is of course necessary to experimentally test the PV modulator at cryogenic temperatures and study how its performance varies with respect to room temperature operation.

It is also of interest to explore if there exist variations on the PV modulator that can improve its frequency response to bandwidths beyond 1 GHz, even if it comes at a cost in power dissipation. At this time, such a variation is not obvious to the author. On a related note, testing the PV modulator concept with a different optical modulator (eg, an electro-absorption modulator) would be of interest to demonstrate the 'universality' of our concept and perhaps obtain a performance improvement.

On a broader perspective, the PV modulator is a demonstration of how tight integration and co-design of photonics and electronics can lead to new device concepts. A further exploration of such an approach could result in the development of new solutions to bottlenecks in a wide range of fields.

6.5 Modeling of nonlinear effects at cryogenic temperatures

In Chapter 5 we presented a theoretical time domain model to describe nonlinear effects in resonant modulators and its impact in modulation performance. We confirmed the accuracy of the model at ambient temperature through comparison with experiments, but we were not able to reproduce experimental observations when using the model at cryogenic temperatures.

Since we have experimentally observed a large effects of nonlinearities on the output waveforms generated by our modulators at 4 K, it is of paramount importance to develop an accurate nonlinear model at these temperatures. This involves the analysis of heat transport in the SOI platform at cryogenic technologies. The strong drop in heat capacity and thermal conductivity of both Si and SiO_2, and its large dependence on the instantaneous temperature (an almost 2 order of magnitude change in heat capacity for both silicon and silica takes place between 2 K and 10 K) makes this a complex problem which likely involves the use of finite element methods with non-standard heat transport equations (as we argued in Chapter 5, the standard Fourier heat transport is not accurate at cryogenic temperatures).

Appendix A

Prediction of Behavior at Cryogenic Temperatures Based on Theory

The purpose of this appendix is to predict, using simplified theory, several representative parameters for our devices when operated at cryogenic temperatures. We will also compare such predictions with the values obtained experimentally in Chapter 2 and analyze the matching between theory and experiment.

A.1   Built-in voltage

The built-in voltage ϕ_{bi} of our p-n junctions has an important effect in the electrical behavior of our devices, since it essentially determines the voltage at which the junction becomes forward biased. An increase in ϕ_{bi} will result in an increased turn-on voltage for our diode, which we observed experimentally as temperature is decreased (Figure 2-3).

The junction built-in voltage is defined as the potential difference between the

two quasi-neutral regions (QNR) of a p-n junction in equililbrium [142]:

$$\phi_{bi} = (E_c - E_F)|_{p,QNR} - (E_c - E_F)|_{n,QNR} \tag{A.1}$$

$$= E_g - (E_F - E_v)|_{p,QNR} - (E_c - E_F)|_{n,QNR} \tag{A.2}$$

Above, E_c (E_v) is the conduction (valence) band energy, E_F is the Fermi level and E_g is the bandgap of the material (Fig. A-1(a)).

Assuming that the doping levels are low enough so that the semiconductor is non degenerate allows us to use Maxwell-Boltzmann statistics, which yields the following expression for the equilibrium electron and hole concentration at a temperature T [1]:

$$n_0 = \frac{N_c}{2\beta_d} e^{\frac{-E_d}{kT}} \left(\sqrt{1 + 4\beta_d \frac{N_D}{N_c} e^{\frac{E_d}{kT}}} - 1 \right) \tag{A.3}$$

$$p_0 = \frac{N_v}{2\beta_a} e^{\frac{-E_a}{kT}} \left(\sqrt{1 + 4\beta_a \frac{N_A}{N_v} e^{\frac{E_a}{kT}}} - 1 \right) \tag{A.4}$$

In these equations, k is the Boltzmann constant and N_D (N_A) is the donor (acceptor) impurity concentration in the n (p) region of the diode. E_d (E_a) is the donor (acceptor) ionization energy (see Fig. A-1(a)), and β_d (β_a) the impurity degeneracy factor, which accounts for the fact that the additional electron (hole) given by the impurities can be bound to the donor (acceptor) atom in more than one way.

N_c (N_v) is the effective density of states of the conduction (valence) band, which is given by:

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[1] The reader is pointed to Chapter 2 in [142] for the details of this derivation, which is not reproduced here for the sake of brevity.

$$N_c = 2 \left(\frac{2\pi m_e^* kT}{h^2} \right) \tag{A.5}$$

$$N_v = 2 \left(\frac{2\pi m_h^* kT}{h^2} \right) \tag{A.6}$$

m_e^* (m_h^*) is the density of states effective mass for electrons (holes).

Assuming Maxwell-Boltzmann statistics, we can calculate the Fermi level from Eqs. A.3 - A.4 noting:

$$n_0 = N_c exp \left(-\frac{E_c - E_F|_{n,QNR}}{kT} \right) \tag{A.7}$$

$$p_0 = N_v exp \left(\frac{E_v - E_F|_{p,QNR}}{kT} \right) \tag{A.8}$$

Figure A-1(b) and (c) show the results of evaluating Eqs. A.3, A.4 and A.7 for a silicon p-n junction with doping densities $N_A = N_D = 1 \cdot 10^{18}$ cm^{-3}. Phosphor ($E_d = 45$ meV, $\beta_d = 2$) is assumed as the n dopant and Boron ($E_a = 45$ meV, $\beta_a = 4$) as the p dopant. While the effective masses are temperature dependent [216], such dependence is weak and here we have assumed fixed values $m_e^* = 1.08m_0$ and $m_h^* = 0.81m_0$. We have, nevertheless, accounted for the temperature dependence of the bandgap [142]:

$$E_g = E_{g0} - \frac{\alpha T^2}{T + \beta} \tag{A.9}$$

Where $\alpha = 3.83 \cdot 10^{-4}$ eV/K, $\beta = 453$ K and $E_{g0} = 1.17$ eV for Si.

As is observable in Fig. A-1(b), the Fermi energy approaches the conduction and valence band edges as temperature is lowered, which results in an increase in the
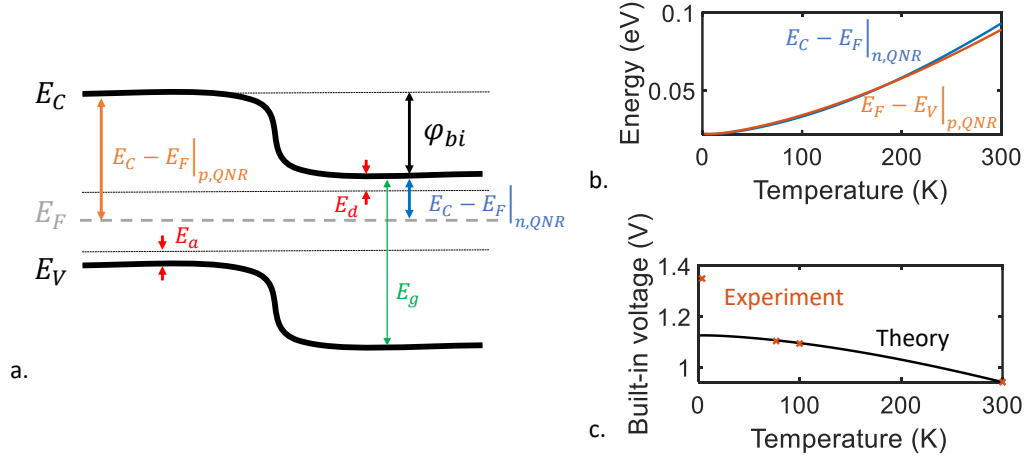
Figure A-1: Evolution of built-in voltage with temperature. (a) Band diagram of a p-n junction in equilibrium. Relevant metrics are indicated. (b) Evolution of the energy difference between the conduction band edge and the Fermi energy at the n side (blue) and between the valence band edge and the Fermi energy at the p side (orange). (c) Evolution of the built-in voltage with temperature. The black line shows the theory prediction, and the crosses show a rough estimation from the experimental IV curves. For (b) and (c), a doping density $N_A = N_D = 1 \cdot 10^{18}$ cm^{-3} is assumed. The p side is doped with Boron, while the n side is doped with Phosphor.

built-in voltage of the junction (Fig. A-1(c)) of almost 0.2 V.

We can make a rough estimation of the built-in voltage measured experimentally by looking at the increase in the voltage we have to apply to reach a given current as a function of temperature. The orange crosses show these for design C at a current of 1 μA, extracted from the results shown in Figure 2-3(a) [2]. Very good agreement between the theory and the experimental results is obtained for liquid nitrogen temperatures and above (T > 77 K), but the measured value at 4 K is considerably larger than that predicted by theory. This is most likely due to the fact

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[2]We assumed that at 300 K the experimental built-in voltage is that predicted by the theory, and computed the built-in voltage at temperature T as: $\phi_{bi}(T) = \phi_{bi}(300K) + V(T, I = 1\mu A) - V(T = 300K, I = 1\mu A)$.

that, as we discussed, the main carrier transport mechanism at this current level and 4 K is not carrier diffusion, but impact ionization. In this case, the simple method we used to estimate the built-in voltage from the IV curves is not valid.

A.2 Reverse saturation current

Another effect we observed in the experimental characterization of the electrical behavior of our devices was a steep decrease in the reverse saturation current I_s as temperature is lowered. As discussed in Chapter 2, this is expected and is tightly related to the increase in the built-in voltage of the junction we studied in the previous section, since I_s is due to the diffusion of carriers through the potential barrier. An increase in the potential barrier will result in an exponential decrease in the saturation current, as the fraction of carriers with enough energy to overcome such barrier decreases also exponentially.

In a simple 1 dimensional p-n junction, the reverse saturation current density $J_s = I_s/A$, with A the cross sectional area of the diode, can be written as [142]:

$$J_s = q\frac{n_i^2}{p_0}\frac{D_e}{L_e} + q\frac{n_i^2}{n_0}\frac{D_h}{L_h} \tag{A.10}$$

Above, n_0 (p_0) is the equilibrium carrier concentration of electrons (holes) in the n (p) region, which is given by Eqs. A.3 - A.4. D_e (D_h) and L_e (L_h) are the diffusion coefficient and diffusion length of electrons (holes) in the p (n) region, respectively. n_i is the intrinsic carrier concentration, and is given by:

$$n_i = \sqrt{N_c N_v}exp(-\frac{E_g}{2kT}) \tag{A.11}$$

Figure A-2 shows the results of evaluating Eq. A.10 for the same diode parameters
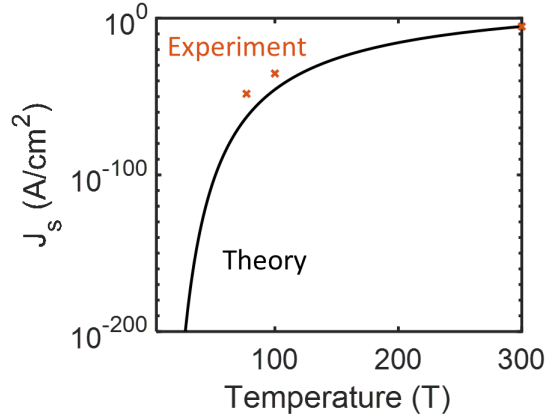
Figure A-2: Evolution of the reverse saturation current density with temperature. The black line shows the theory prediction, and the crosses show a rough estimation from the experimental IV curves. A doping density $N_A = N_D = 1 \cdot 10^{18}$ cm^{-3} is assumed. The p side is doped with Boron, while the n side is doped with Phosphor.

that we used in the last section. We approximated the drift velocity D_x/L_x to be independent of temperature and used typical values at room temperature ($D_e/L_e = 2.9 \cdot 10^3$ cm/s, $D_h/L_h = 3.1 \cdot 10^2$ cm/s). We can see how a very sharp decrease in the saturation current is predicted.

We can estimate the reverse saturation current experimentally from the IV curves in Figure 2-3(a) by looking at the voltage necessary to reach a specific current I:

$$I = I_s(T_1) * exp\left(\frac{qV(T_1)}{kT_1}\right) = I_s(T_2) * exp\left(\frac{qV(T_2)}{kT_2}\right) \tag{A.12}$$

$$\frac{I_s(T_1)}{I_s(T_2)} = exp\left(\frac{qV(T_1)}{kT_1} - \frac{qV(T_2)}{kT_2}\right) \tag{A.13}$$

The orange crosses in Fig. A-2 show the extracted saturation current density using this approach for design C and a current $I = 1$ μA. While the experimental data shows the same trend as the theory, 10 orders of magnitude larger values are

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obtained experimentally. Several factors are probably contributing to such difference:

1. We have not accounted for the temperature dependence of the drift velocity. The decrease in temperature reduces the phonon occupancy, which increases the carrier drift velocity and results in an increased saturation current compared to what we predicted.

2. Our diodes are complex 3D structures, so the assumption of a linear 1 dimensional diode has limited validity.

3. Most importantly, the presence of a current flowing through the diode generates ohmic heating, which increases the temperature of the device above the cryostat temperature. This, in turn, generates a significant change on the saturation current. For example, at temperatures around 77 K, a 1 K increase in temperature generates a 10x increase in the saturation current. Thus, an increase in the diode temperature due to ohmic heating would have an important contribution on the difference between theoretical and experimental values.

A.3 Reverse biased RC time constant

In Chapter 2 we observed a significant decrease in the reverse bias bandwidth of our devices at cryogenic temperatures. This is expected, and is due to carrier freezeout, which increases the access resistance to the diode and results in an increased RC time constant.

We can estimate the expected drop in bandwidth as a function of temperature using the theory we have layed out in the previous sections. We can estimate the resistivity of the quasi neutral regions of the diode to be:

$$\rho_n = \frac{1}{q(\mu_e n_0)} \tag{A.14}$$

$$\rho_p = \frac{1}{q(\mu_h p_0)} \tag{A.15}$$

Above, μ_e (μ_h) is the electron (hole) mobility in the n (p) region. The change in resistivity for the diode parameters we have used throughout this Appendix is shown in Fig. A-3(a). We assumed carrier mobility to be temperature independent and used Eqs. A.3 - A.4 to calculate n_0 and p_0. As expected, a huge increase in resistivity is predicted at low temperatures due to the low free carrier density.

We can also estimate the capacitance C of our system in reverse bias using:

$$C = A\frac{\epsilon}{x_{SCR}(V)} \tag{A.16}$$

Where ϵ is the permitivity of Si and x_{SCR} is the width of the depletion region of the diode. In a simple 1D diode x_{SCR} is given by [142]:

$$x_{SCR}(V) = \sqrt{\frac{2\epsilon(n_0 + p_0)(\phi_{bi} - V)}{qn_0 p_0}} \tag{A.17}$$

The capacitance C as a function of temperature for $V = 0$ is shown in Fig. A-3(b) assuming no temperature dependence of the silicon permitivity. A strong decrease with temperature is predicted due to the increase in the space charge region width.

Combining the calculations of the resistivity and capacitance allows us to easily obtain the evolution of the RC time constant τ_{RC} with temperature, which is shown in Fig. A-3(c). At 4K, a more than 20 orders of magnitude increase in τ_{RC} is predicted.
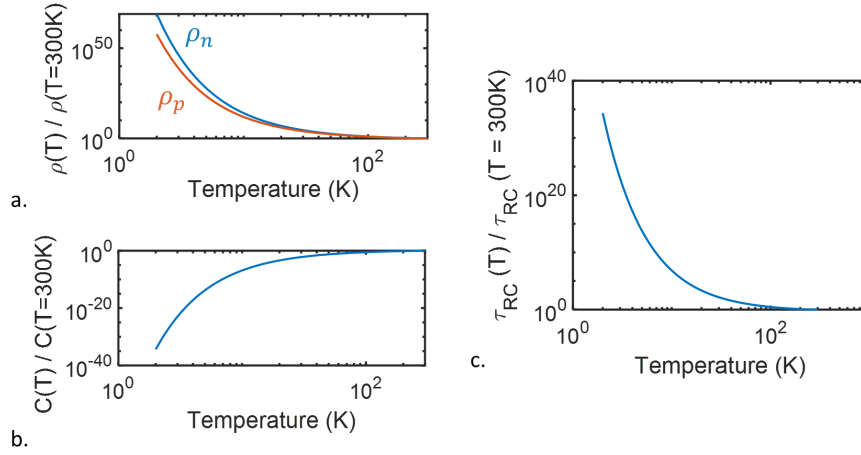
Figure A-3: Predicted evolution of RC time constant with temperature. (a) Resistivity of the n (blue) and p (orange) QNR as a function of temperature. (b) Junction capacitance as a function of temperature normalized to its value at 300 K. (c) RC time constant of the diode as a function of temperature normalized to its value at 300 K.

Clearly, the basic theory predictions are really far from what we observe experimentally, which is a decrease in bandwidth between 5 - 20x. Besides the simple assumptions we made to derive the theoretical formulas, two main factors contribute to such a difference, both related to ionization of carriers:

1. A significant electric field can be present in the device when a reverse bias voltage is applied. Such an electric field can result in the ionization of the impurities because there is a lowering in the energy barrier needed to do so [118].

   We can approximate the lowering of the ionization energy in the presence of an electric field $\mathcal{E}$ by $\Delta E = -2q\sqrt{q\mathcal{E}/\epsilon_{si}}$ [118]. For boron and phosphor, with E_{ion} = 45 meV, the application of a field $\mathcal{E} > 3.3$ kV/cm eliminates the potential well and allows the carriers to participate in conduction. In a 1 μm long resistor, an applied voltage as small as 0.33V can fully ionize the impurities.

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2. The presence of light in the device can also cause impurity ionization through the absorption of photons. In fact, we observed this effect experimentally when characterizing the optical resonance of our devices at 4 K (Section 2.3.2).

Both processes result in an increase in the number of free carriers n_0 and p_0 above what is predicted by simple thermal ionization considerations (Eqs. A.3 - A.4). Thus, a decreased resistivity resulting in a larger bandwidth is expected.

A.3.1   Doping dependence

In our experiments we also saw how doping density had an important effect on the bandwidth drop observed at cryogenic temperatures: our device with larger impurity concentration (design *O-H*) showed a 5x decrease in bandwidth, whereas lower doped devices showed a close to 20x decrease.

This behavior is expected, and is due to the fact that when larger doping concentrations are used the average distance between impurities decreases. This results in the formation of an impurity band that allows for the movement of free carriers. In fact, above a threshold impurity concentration (which depends on the material, and is about $4 \cdot 10^{18}$ cm^{-3} for Si) no carrier freezeout is observed at any temperature, an effect known as the Mott metal-insulator transition [120].

Mathematically, we can express the effect of the impurity band formation as a lowering of the impurity ionization energy [142]:

$$E_i = E_{i0} \left(1 - \left[\frac{N_i}{N_M} \right]^{1/3} \right) \tag{A.18}$$

Where E_{i0} is the ionization energy for low doping values, N_i is the doping density and N_M is the Mott concentration, which depends on the material and the impurity
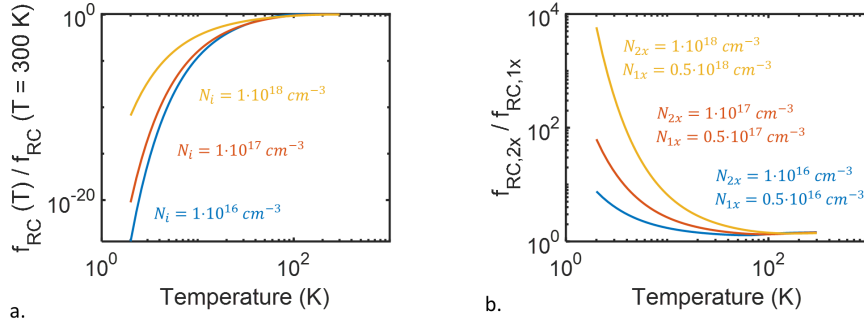
Figure A-4: Effect of impurity concentration on 3 dB bandwidth. (a) 3 dB bandwidth as a function of temperature normalized to the value at 300 K for different impurity concentrations. (b) Ratio between the bandwidth for samples doped with 2x and 1x impurity concentration as a function of temperature.

atom. For P-doped Si, $N_M = 3.5 \cdot 10^{18}$ cm^{-3}.

Figure A-4(a) shows the evolution of 3 dB bandwidth with temperature for varying impurity concentrations $N_A = N_D = N_i$. In accordance with our experimental observations, a lower bandwidth drop is expected for higher doping concentrations due to the lowering of the impurity ionization energy.

Figure A-4(b) shows the increase in bandwidth when doubling the doping concentration as a function of temperature. We can see how, depending on the base doping level, bandwidth increases between 4x and 80x are expected at 4 K. For our devices, we experimentally observed a 6x increase in the 4 K bandwidth - from 500 MHz to 3 GHz - when using a 2x higher impurity concentration.

A.4 Resonance shift at low temperature

Another effect of low temperature operation we observed experimentally was the blue shift in the resonance wavelength of the devices (Fig. 2-5(c)). This is due to the decrease in the refractive index of silicon as we lower the temperature (Fig.
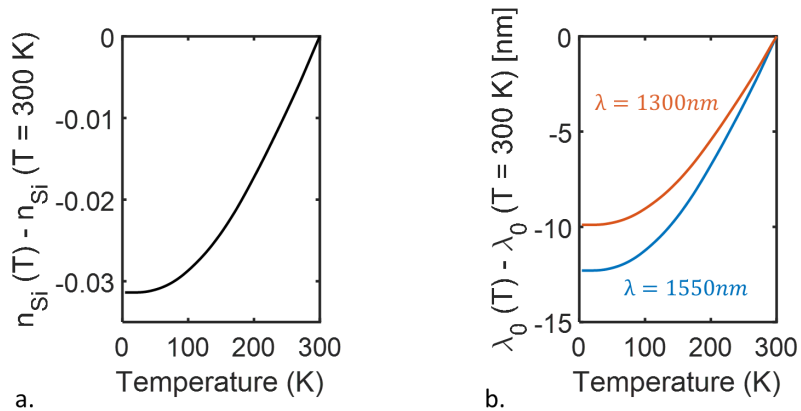
Figure A-5: Thermo-optic effect on resonance wavelength. (a) Change in the refractive index of silicon as a function of temperature. (b) Predicted resonance wavelength shift as a function of temperature for the 1550 nm ring (design C in Chapter 2, blue) and for the 1300 nm ring (design C in Chapter 2, orange).

A-5(a), [127]), which generates a resonance shift given by [135]:

$$\Delta\lambda_0 \approx \lambda_0 \frac{\Gamma\Delta n_{Si}}{n_g} \tag{A.19}$$

Above, n_g is the group index of the optical mode and Γ its confinement factor as defined in Chapter 5 [3]. Clearly, a decrease in index of refraction is accompanied by a decrease in the resonance wavelength of the device.

We computed the expected resonance shift for design C ($\lambda_0 = 1550$ nm, $n_g = 2.77$, $\Gamma = 0.7$) and O ($\lambda_0 = 1300$ nm, $n_g = 3.02$, $\Gamma = 0.75$), and the results are shown in Fig. A-5(b). Very good agreement between the expected values shown in Fig. A-5(b) and the experimental values we measured for our devices ($\Delta\lambda_{C,exp} = 11$ nm, $\Delta\lambda_{O,exp} = 9.2$ nm, see Fig. 2-5) is obtained.

---

[3]Note that in Eq. A.19 we are disregarding any change in the refractive index of the waveguide cladding (SiO_2 in our case). This is a valid approximation since the thermo-optic coefficient of SiO_2 is 2 orders of magnitude lower than that of Si at any temperature.

Appendix B

Q Factors in Resonant Modulators With Absorption

In Chapter 4 we have argued how having a large Q factor and a large generated photocurrent is essential to the performance of the PV modulator. At first sight, having a large Q factor resonance might seem incompatible with a large responsivity device, since large responsivities translate into large absorption coefficients, and therefore large ring internal loss and low Q factors.

In this appendix we analyze the tradeoffs between responsivity and Q factor, and show that for sufficiently small round trip, critically coupled resonators, device responsivity and Q factor are independent.

B.1   Deriving responsivity from Q factor

We will follow closely the notation used in [106]. The loaded quality factor Q_{loaded} of a resonator is given by:

$$Q_{loaded} = \frac{\pi n_g L \sqrt{ra}}{\lambda_0 (1 - ra)} \tag{B.1}$$

Above, L is the roundtrip length of the resonator, n_g is the group index of the mode and λ_0 the resonance wavelength. a is the single pass amplitude transmission $a^2 = e^{-\alpha L}$, where α is the power attenuation coefficient, and r is the self-coupling coefficient between the bus waveguide and the resonator. In a critically coupled ring $r = a$ [106].

The coupling quality factor of the ring is that associated with the losses due to coupling of the ring and the bus waveguide, and is given by:

$$Q_{coup} = \frac{\pi n_g L \sqrt{r}}{\lambda_0 (1 - r)} \tag{B.2}$$

Similarly, the internal quality factor of the ring is that associated with the losses in the ring itself due to absorption, scattering and radiation [1], and is given by:

$$Q_{int} = \frac{\pi n_g L \sqrt{a}}{\lambda_0 (1 - a)} \tag{B.3}$$

If we know Q_{int}, we can easily calculate a, and from it obtain the internal loss coefficient α. α includes a variety of optical loss mechanisms such as absorption resulting in photocurrent α_{pc}, free carrier absorption α_{fc}, and radiation and scattering losses α_{scat}:

$$\alpha = \alpha_{pc} + \alpha_{fc} + \alpha_{scat} \tag{B.4}$$

We will assume that a fraction f of the total losses is due to absorption that generates a photocurrent: $\alpha_{pc} = f\alpha$.

---

[1] Throughout this thesis, we have used the notation Q_{rad} to refer to the internal Q factor.

With this, we know that the power absorbed in the ring leading to photocurrent will be given by:

$$P_{abs,pc} = P_{in}(1 - e^{-\alpha_{pc}L_{eff}}) \tag{B.5}$$

L_{eff} is the effective length that the light travels around the resonator before being lost, and is given by $L_{eff} = FL/2\pi$ [106]. F is the resonator finesse, and is given by:

$$F = \frac{\pi\sqrt{ra}}{1 - ra} = \frac{\pi a}{1 - a^2} \tag{B.6}$$

Where the second equality is valid under critical coupling conditions $(r = a)$.

With this, we can calculate the quantum efficiency of the resonator:

$$\eta = \frac{P_{abs,pc}}{P_{in}} = 1 - e^{-\alpha_{pc}FL/2\pi} \tag{B.7}$$

Finally, the device responsivity is given by:

$$R = \frac{q\eta}{h\nu} = \frac{q}{h\nu}\left(1 - e^{-\alpha_{pc}FL/2\pi}\right) = \frac{q}{h\nu}\left[1 - exp\left(-f\alpha\frac{L}{2}\frac{a}{1 - a^2}\right)\right] \tag{B.8}$$

Above, q is the elementary charge, h is Planck's constant and ν is the frequency of the light.

Equation B.8 allows us to evaluate the responsivity of a resonant device based on its internal quality factor given the fraction f of internal losses due to absorption resulting in photocurrent.

B.2 Responsivity and Q factor tradeoff

Figure B-1 shows the responsivity of the resonator as a function of internal Q factor for a critically coupled ring, assuming a fixed f. We can see how, for Q factors above a certain threshold (which depends on the round trip length of the device), the responsivity becomes independent of the quality factor. As expected, larger f result in larger responsivities, since more of the internal loss generates photocurrent.

This leads us to an interesting conclusion: decreasing photocurrent generating absorption in the ring waveguide (and therefore achieving larger Q factors) does not lead to smaller device responsivities as long as the overall loss is also decreased (i.e, the fraction of photocurrent generating absorption to total loss f is kept constant).

Therefore, to achieve large Q factor resonators with decent responsivity, it might be advantageous to reduce the absorption coefficient α_{pc} in the ring if that leads to an overall reduction in the total internal loss α of at least the same relative magnitude $(\Delta\alpha_{pc}/\alpha_{pc} = \Delta\alpha/\alpha)$.
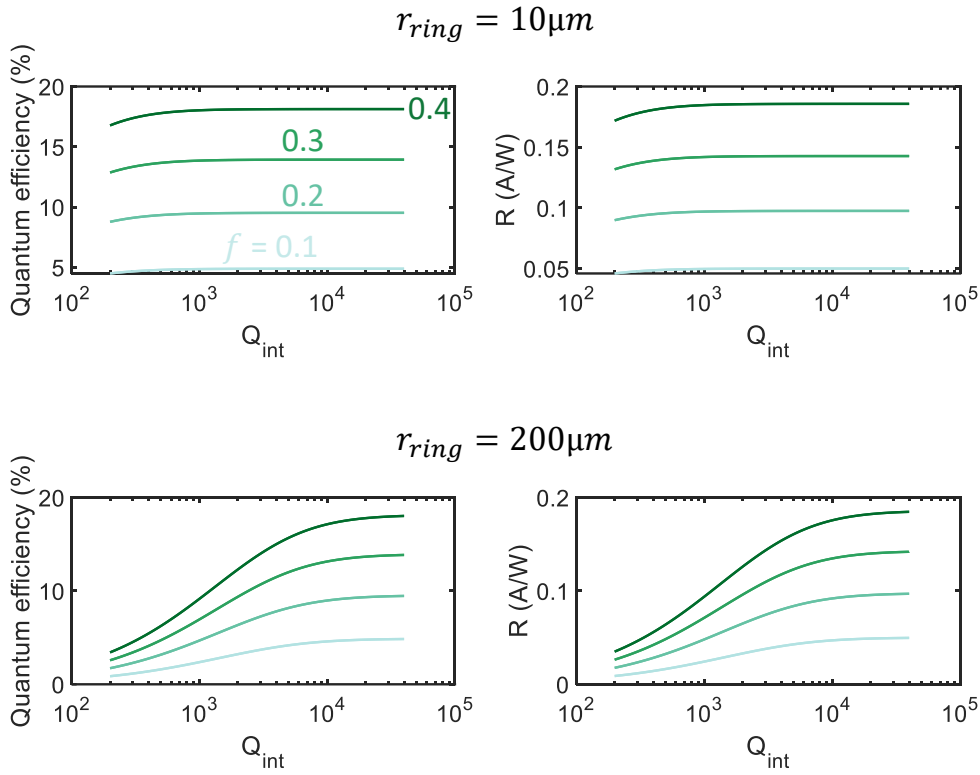
Figure B-1: Responsivity and quantum efficiency as a function of resonator internal Q factor. (a) Quantum efficiency and (b) responsivity for a 10 μm radius resonator as a function of internal Q factor. Q factors larger than 1,000 result in the same responsivity. Different lines correspond to a different fraction of loss due to photocurrent generating absorption $f = \alpha_{pc}/\alpha$. (c) Quantum efficiency and (d) responsivity for a 200 μm radius resonator as a function of internal Q factor. Q factors larger than 5,000 result in the same responsivity.

Appendix C

The Effect of r_{pc} on the Performance of PV Modulators

All throughout Chapter 4 we have assumed that the equivalent resistance associated to the change in photocurrent with the voltage at the modulator terminals $r_{pc} = dV_{mod}/dI_{pc}$ is much larger than the diode dynamic resistance r_d and the transistor output resistance r_0, so that we can say $r_d||r_0||r_{pc} \approx r_d||r_0$. In this appendix we will study the validity of this assumption and study how r_{pc} could affect PV modulator operation.

In any optical modulator we would use in our PV concept, a change in the voltage at the modulator terminals V_{mod} will be accompanied by a change in the photogenerated current I_{pc}. Take, for example, a resonant modulator as the one we used in our experiments. A change in V_{mod} will shift the resonance wavelength of the device, modifying the power absorbed in the ring and resulting in a change in I_{pc}. As a consequence, $r_{pc} = dV_{mod}/dI_{pc}$ has a finite value and can affect the performance of a PV modulator.

It is easy to derive an expression for the value of r_{pc}, recognizing that the generated photocurrent is given by $I_{pc} = RP_{abs}$, where R is the device responsivity and P_{abs} is the optical power absorbed in the modulator. We can then write:

$$\frac{dI_{pc}}{dV_{mod}} = R\frac{dP_{abs}}{dV_{mod}} = RP_{in}\frac{d(1-T)}{dV_{mod}} = -RP_{in}\frac{dT}{d\lambda}\frac{d\lambda}{dV_{mod}} \tag{C.1}$$

Where $T = P_{out}/P_{in}$ is the transmission through the ring. We can rewrite the term $d\lambda/dV_{mod} = -d\lambda_0/dV_{mod}$, which is the intrinsic modulation efficiency of our modulator.

We end up with the following expression for r_{pc}:

$$r_{pc} = \frac{1}{\frac{dI_{pc}}{dV_{mod}}} = \left(RP_{in}\frac{dT}{d\lambda}\frac{d\lambda_0}{dV_{mod}}\right)^{-1} \tag{C.2}$$

Fig. C-1 shows the calculated r_{pc} using Eq. C.2 for the modulator we experimentally characterized in Chapter 4 under different input optical powers, as a function of laser wavelength. We used a responsivity R = 0.034 A/W, assumed a modulation efficiency $d\lambda_0/dV_{mod} = 20$ pm/V and a Lorentzian resonance with $Q_{coup} = 20,000$, $Q_{rad} = 9,000$ and $\lambda_0 = 1270$ nm. Several important observations should be made:

1. For a given input optical power, the minimum achievable values of r_{pc} are about 10x larger than typical values for $r_0||r_d$ (see for example Fig. 4-6). This confirms that our assumption $r_d||r_0||r_{pc} \approx r_d||r_0$ is correct.

2. Negative r_{pc} values can be obtained when the laser wavelength is at the red side of the resonance $(\lambda_l > \lambda_0)$. This is because in a Lorentzian resonance, $dT/d\lambda > 0$ for $\lambda_l > \lambda_0$.

While in our experimental demonstration $r_{pc} \gg r_0||r_d$, a scenario where r_{pc} becomes comparable to r_0 and r_d (or even $r_{pc} \ll r_0||r_d$) is possible by, for example,
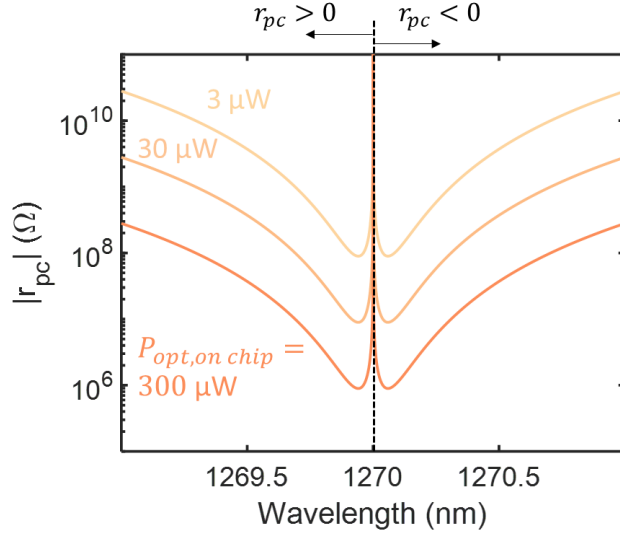
Figure C-1: r_{pc} values for design OZ in Chapter 2 (the device used for the experimental demonstration of the PV modulator in Chapter 4) for different input optical powers as a function of laser wavelength.

using a modulator with a larger modulation efficiency $d\lambda_0/dV_{mod}$ or a sharper resonance (and therefore larger $dT/d\lambda$). In this case, we would need to account for r_{pc} when computing the small signal gain and bandwidth. From Chapter 4, we can approximate:

$$A_{vd,DC} = gm(r_0||r_d||r_{pc}) \tag{C.3}$$

$$f_{3dB} = \frac{1}{2\pi C_{diode}(r_0||r_d||r_{pc})} \tag{C.4}$$

And of course:

$$r_0||r_d||r_{pc} = \frac{r_{pc}(r_0||r_d)}{r_{pc} + (r_0||r_d)} \tag{C.5}$$

Clearly, if we operate a device where $r_{pc} \ll r_0||r_d$, then $r_0||r_d||r_{pc} \approx r_{pc}$, which would reduce the small signal gain $A_{vd,DC}$, but increase the frequency response f_{3dB}

of the device.

A very interesting situation arises when we operate at a bias point where $r_{pc} \approx -r_0||r_d$. In this case, $r_0||r_d||r_{pc} \to \infty$, which makes $A_{vd,DC} \to \infty$ and $f_{3dB} \to 0$. The possibility of synthesizing negative resistances is interesting for other applications beyond modulation, such as the realization of on chip oscillators.

We can thus conclude that r_{pc} can have a significant effect in the PV modulator behavior if the photogenerated current depends strongly on the voltage applied at the modulator terminals. This was not the case for the device we experimentally demonstrated in Chapter 4, but it could be important in devices with increased modulation efficiency or higher Q factor.

Appendix D

Time Domain Nonlinear Model Equations

In this Appendix we will briefly present the derivation of the system of coupled nonlinear differential equations that we used in Chapter 5 to describe the dynamics of silicon microring resonators under nonlinear effects.

The reader is pointed to reference [205] for a more in-depth discussion of the model derivation for passive resonators. Likewise, a more detailed discussion of the extension to actively modulated devices is available in my undergraduate thesis [95]. Besides setting up the theoretical framework for the model, the reader will find a discussion about how device geometry plays a role in the strength of the nonlinear effects.

D.1 Model derivation

The amplitude of the optical mode travelling along a ring resonator coupled to an input waveguide can be derived using the coupling of modes in time formulism. Considering the ring as a lumped oscillator with resonance frequency W_0 and an amplitude decay constant $\gamma/2$ [224], we can write:

$$\frac{da}{dt} = \left(-\frac{\gamma}{2} + j\Delta W_0\right) a - j\kappa s_{in} \tag{D.1}$$

$$s_{out} = s_{in} - j\kappa^* a \tag{D.2}$$

Above, κ is the coefficient of coupling between the ring and the waveguide, $\Delta W_0 = W_0 - W_l$ is the detuning between the wavelength of the input light and the resonance wavelength of the modulator, $|s_{in}|^2$ is the input power into the modulator and $|s_{out}|^2$ is the power at the output of the modulator. The mode amplitude a is defined such that the energy stored in the ring is $U = |a|^2$.

Note that here, as opposed to [205], the splitting of the cosine- and sine-like degenerate modes is not considered, as this only occurs in very high-Q ($> 10^5$) resonant structures.

D.1.1 Loss rate

The loss rate γ defined above can be directly related to quality factor of a resonator. Since $\gamma = 1/\tau$ (where τ is the decay time constant of the power inside the resonator) and $Q = W_0\tau$, γ and Q can be directly related by $Q = W_0/\gamma$.

The mode's total loss rate γ can be separated in different terms corresponding to different loss mechanisms:

$$\gamma = \gamma_0 + \gamma_{rad} + \gamma_{lin} + \gamma_{TPA} + \gamma_{FCA} \tag{D.3}$$

γ_0 describes the losses due to the coupling between the ring and the bus waveguide, γ_{rad} those due to radiation and scattering in the ring and γ_{lin} those associated with linear absorption in the ring (which as discussed in Chapter 4 can be important in our silicon photonic structures). γ_{TPA} and γ_{FCA} are losses due to TPA and FCA, respectively. From power conservation, $\kappa = \sqrt{\gamma_0}$ [224]. Note here the assumption that there are no losses due to coupling to higher order modes of the ring.

While γ_0, γ_{rad} and γ_{lin} are independent of the ring state, γ_{TPA} and γ_{FCA} depend on the density of free carriers in the ring which, in turn, depend on the amount of energy stored in it.

It is necessary to account for the non-uniform distribution of the optical mode in the ring waveguide, which makes the different physical phenomena be, in general, position dependent (for example, TPA will be more intense in the waveguide regions where the optical mode is more concentrated). To do so we follow the approach in [225], which consists in introducing weighted averages of the local rates at each position in the waveguide for the specific propagating optical mode. With this, we can define [225]:

$$\gamma_{TPA}(t) = \Gamma_{TPA} \frac{\beta_{Si} c^2}{V_{TPA} n_g^2} U(t) \tag{D.4}$$

Where c is the speed of light in vacuum, n_g is the group index of the optical mode, β_{Si} is the intensity loss per unit length due to TPA and Γ_{TPA} and V_{TPA} account for the non uniformity of the mode and are defined as:

$$\Gamma_{TPA} = \frac{\int_{Si} |E(\mathbf{r})|^4 d\mathbf{r}}{\int n^4(\mathbf{r}) |E(\mathbf{r})|^4 d\mathbf{r}} \qquad (D.5)$$

$$V_{TPA} = \frac{\left(\frac{1}{n_{Si}\epsilon_0 c}\right)^2 \left(\int Re\{\mathbf{E}(\mathbf{r}) \wedge \mathbf{H}^*(\mathbf{r})\} \hat{e}_z d\mathbf{r}\right)^2}{\int n^4(\mathbf{r}) |E(\mathbf{r})|^4 d\mathbf{r}} \qquad (D.6)$$

Note that the definitions of the mode averaged parameters are different than the ones used in [205] to account for the high index contrast achieved in these type of devices [208].

As already discussed, the generation of carriers due to TPA generates additional optical losses due to FCA, which can be described by:

$$\gamma_{FCA}(t) = \frac{(\alpha_p + \alpha_n)c}{n_g} \overline{N(t)} \qquad (D.7)$$

α_p and α_n are the loss coefficients given by the Soref's equations presented in Chapter 1 (see Eq. 1.3). Note that we are not considering the free carrier population due to the ionized acceptors and donors. As this population is not time dependent (at least at room temperature, where all the impurities are ionized due to thermal energy), the associated optical losses are constant and can be considered as a background loss included in γ_{lin}.

In equation D.7, we again account for the non-uniformity of the electric field distribution by defining:

$$\overline{N(t)} = \frac{\int N(\mathbf{r}, t) n^2(\mathbf{r}) |E(\mathbf{r})|^2 d\mathbf{r}}{\int n^2(\mathbf{r}) |E(\mathbf{r})|^2 d\mathbf{r}} \qquad (D.8)$$

With the above definitions we can then obtain the total power absorbed in the ring at a given time:

$$P_{abs}(t) = (\gamma_{lin} + \gamma_{TPA} + \gamma_{FCA})U(t) \tag{D.9}$$

D.1.2 Microring resonance wavelength

Both the generated free carriers (through the plasma dispersion effect) and the induced self-heating of the waveguide (through thermal dispersion) induce a change in the resonance wavelength of the ring. The relation between a change in the refractive index of the waveguide Δn and the induced change in the resonance wavelength ΔW_0 is given by:

$$\frac{\Delta W_0(t)}{W_0} = -\frac{\overline{\Delta n(t)}}{n} \tag{D.10}$$

Where, again, we account for the non-uniformity of the field distribution through mode-averaging:

$$\frac{\overline{\Delta n(t)}}{n} = \frac{\int \frac{\Delta n(\mathbf{r},t)}{n(\mathbf{r})} n^2(\mathbf{r})|E(\mathbf{r})|^2 d\mathbf{r}}{\int n^2(\mathbf{r})|E(\mathbf{r})|^2 d\mathbf{r}} \tag{D.11}$$

Noticing that the change in the refractive index Δn is due to thermal and free carrier dispersion and also the externally appplied driving signal, we can write:

$$\frac{\Delta W_0(t)}{W_0} = -\frac{1}{n_{Si}} \left(\frac{dn_{Si}}{dT}\overline{\Delta T(t)} + \left(\frac{dn_{Si}}{dN_p} + \frac{dn_{Si}}{dN_n} \right) \overline{N(t)} \right) + \frac{\Delta W_{0_{mod}}(t)}{W_0} \tag{D.12}$$

Above, $\frac{dn_{Si}}{dT}$ is the thermo-optic coefficient of silicon, $\frac{dn_{Si}}{dN_n}$ and $\frac{dn_{Si}}{dN_p}$ are the free carrier dispersion coefficient for electrons and holes respectively (which can be directly obtained from Soref's equations - Eqs. 1.2 and 1.3) and n_{Si} is the refractive index of silicon. $\overline{\Delta T(t)}$ is the mode-averaged temperature difference between the sil-

icon waveguide and the environment and $\overline{N(t)}$ is the free carrier density (Eq. D.8). $\Delta W_{0_{mod}}$ accounts for the resonance shift due to the applied driving signal, which is of course dependent on the voltage applied to the modulator as well as the dynamics of the pn-junction.

Note the important simplifications made when adding external modulation. The modulation of the depletion region width generates a change in the mode-averaged free carrier density $\overline{N(t)}$, which translates into a change in the resonance wavelength and in the loss rates through the equations derived above. Adding such dependence to our model would add a lot of complexity, since the geometry and layout of the microring should be included, the depletion region width derived for each applied voltage and the mode averages recalculated at each time step. Instead, we reduce the effect of the modulation to an additional term affecting the resonance wavelength, and no effect in the loss rates is included.

D.1.3 Dynamic equations

To complete the model, the dependence of all the relevant variables of the system with time has to be introduced.

As discussed in Chapter 5, we model the voltage across the p-n junction (V_{pn}) as a first order system with time constant τ:

$$\frac{dV_{pn}(t)}{dt} = \frac{-V_{pn}(t)}{\tau} + \frac{V(t)}{\tau} \tag{D.13}$$

In reverse bias, τ corresponds to the RC limit of the device, which is in principle time dependent due to the dependence of the depletion capacitance $C(t)$ and series resistance $R(t)$ on the applied voltage. Nevertheless, this dependence is generally weak due to the small changes in the depletion region width with applied voltage.

As a consequence, we will consider τ to be voltage (and time) independent.

The voltage through the pn junction can be directly related to the shift in resonance frequency through the modulation efficiency dW_0/dV:

$$\Delta W_{0_{mod}}(t) = \frac{dW_0}{dV} V_{pn}(t) \tag{D.14}$$

The time evolution of the temperature can be also derived from energy conservation principles [226]:

$$\frac{d\overline{\Delta T(t)}}{dt} = -\gamma_{th} \overline{\Delta T(t)} + \frac{\Gamma_{disk}}{\rho_{Si} c_{p,Si} V_{ring}} P_{abs}(t) \tag{D.15}$$

Several assumptions are made here. First, radiation and convection are disregarded. Second, as silicon has a high thermal conductivity (at least at 300 K), we consider that the temperature is uniform all over the waveguide ($\Delta T(\mathbf{r}, t) = \Delta T(t)$). Finally, we assume that the power dissipation is instantaneous, that is, the heating at time t depends on the absorbed power P_{abs} at that same time t. As discussed in Chapter 5, this simple thermal model becomes inaccurate at cryogenic temperatures.

The non-uniformity of the mode profile is again considered by defining:

$$\Gamma_{disk} = \frac{\int_{Si} |E(\mathbf{r})|^2 d\mathbf{r}}{\left(\frac{1}{n_{Si}\epsilon_0 c}\right) \int Re\{\mathbf{E}(\mathbf{r}) \wedge \mathbf{H}^*(\mathbf{r})\} \hat{e}_z d\mathbf{r}} \tag{D.16}$$

Two mechanisms affect the free carrier population: recombination and TPA, which results in:

$$\frac{d\overline{N(t)}}{dt} = -\gamma_{fc} \overline{N(t)} + \overline{G(t)} \tag{D.17}$$

$\overline{G(t)}$ is the rate of free carrier generation due to TPA and γ_{fc} accounts for all

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the processes that reduce free carrier density in the regions where the optical mode is confined. These are mainly carrier recombination (which include a variety of processes such as non-radiative recombination, Auger recombination...), drift (due to the applied external voltage, which generates an electric field that sweeps the carriers) and diffusion due to carrier density gradients along the waveguide. Note how, in general, γ_{fc} is position dependent, but here we consider an average recombination rate that is uniform all over the waveguide.

Since every two photons absorbed one electron-hole pair is generated, the generation rate G can be written as:

$$\overline{G(t)} = \frac{\Gamma_{FCA}\beta_{Si}c^2}{2\hbar W_l n_g^2 V_{FCA}^2} U(t)^2 \tag{D.18}$$

where we define the mode averages:

$$\Gamma_{FCA} = \frac{\int_{Si} |E(\mathbf{r})|^6 d\mathbf{r}}{\int n^6(\mathbf{r})|E(\mathbf{r})|^6 d\mathbf{r}} \tag{D.19}$$

$$V_{FCA}^2 = \frac{\left(\frac{1}{n_{Si}\epsilon_0 c}\right)^3 \left(\int Re\{\mathbf{E}(\mathbf{r}) \wedge \mathbf{H}^*(\mathbf{r})\}\hat{e}_z d\mathbf{r}\right)^3}{\int_{Si} n^6(\mathbf{r})|E(\mathbf{r})|^6 d\mathbf{r}} \tag{D.20}$$

With this, the derivation of the model is complete.

Note that the model uses a number of parameters that need to be accurate if meaningful results are to be obtained. While some of these are material parameters well-known from the literature, some others are specific for the geometry or device to be tested (see Table 5.1). The derivation of these parameters (experimentally or through simulation) is described in [95].

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Bibliography

[1] S. E. Miller, "Integrated optics: An introduction," *The Bell System Technical Journal*, vol. 48, no. 7, pp. 2059–2069, Sep 1969.

[2] V. Evtuhov and A. Yariv, "GaAs and GaAlAs devices for integrated optics ." *IEEE Transactions on Microwave Theory and Techniques*, vol. 23, no. 1, pp. 44–57, Jan 1975.

[3] M. Smit, X. Leijtens, H. Ambrosius, E. Bente, J. van der Tol, B. Smalbrugge, T. de Vries, E.-J. Geluk, J. Bolk, R. van Veldhoven, L. Augustin, P. Thijs, D. D'Agostino, H. Rabbani, K. Lawniczuk, S. Stopinski, S. Tahvili, A. Corradi, E. Kleijn, D. Dzibrou, M. Felicetti, E. Bitincka, V. Moskalenko, J. Zhao, R. Santos, G. Gilardi, W. Yao, K. Williams, P. Stabile, P. Kuindersma, J. Pello, S. Bhat, Y. Jiao, D. Heiss, G. Roelkens, M. Wale, P. Firth, F. Soares, N. Grote, M. Schell, H. Debregeas, M. Achouche, J.-L. Gentner, A. Bakker, T. Korthorst, D. Gallagher, A. Dabbs, A. Melloni, F. Morichetti, D. Melati, A. Wonfor, R. Penty, R. Broeke, B. Musk, and D. Robbins, "An introduction to InP-based generic integration technology," *Semiconductor Science and Technology*, vol. 29, no. 8, p. 083001, Jun 2014.

[4] J. E. Bowers and A. Y. Liu, "A comparison of four approaches to photonic integration," in *2017 Optical Fiber Communications Conference and Exhibition (OFC)*, Mar 2017, pp. 1–3.

[5] R. A. Soref and J. P. Lorenzo, "Single-crystal silicon: a new material for 1.3 and 1.6 μm integrated-optical components," *Electronics Letters*, vol. 21, no. 21, pp. 953–954, Oct 1985.

[6] G. T. Reed, W. R. Headley, and C. E. J. Png, "Silicon photonics: the early years," in *Optoelectronic Integration on Silicon II*, J. A. Kubby and G. E. Jabbour, Eds., vol. 5730, International Society for Optics and Photonics. SPIE, 2005, pp. 1 – 18.

[7] G. T. Reed and A. P. Knights, *Silicon Photonics: An Introduction*, 1st ed. The Atrium, Southern Gate, Chichester, West Sussex PO19 8SQ, England: John Wiley & Sons Ltd, 2004.

[8] B. Jalali and S. Fathpour, "Silicon photonics," *Journal of Lightwave Technology*, vol. 24, no. 12, pp. 4600–4615, Dec 2006.

[9] R. Soref, "The past, present, and future of silicon photonics," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 12, no. 6, pp. 1678–1687, Nov 2006.

[10] A. L. Washburn, M. S. Luchansky, A. L. Bowman, and R. C. Bailey, "Quantitative, label-free detection of five protein biomarkers using multiplexed arrays of silicon photonic microring resonators," *Analytical Chemistry*, vol. 82, no. 1, pp. 69–72, Jan 2010.

[11] J. Leuthold, C. Koos, and W. Freude, "Nonlinear silicon photonics," *Nature Photonics*, vol. 4, no. 8, pp. 535–544, 2010.

[12] X. Qiang, X. Zhou, J. Wang, C. M. Wilkes, T. Loke, S. O'Gara, L. Kling, G. D. Marshall, R. Santagati, T. C. Ralph, J. B. Wang, J. L. O'Brien, M. G. Thompson, and J. C. F. Matthews, "Large-scale silicon quantum photonics implementing arbitrary two-qubit processing," *Nature Photonics*, vol. 12, no. 9, pp. 534–539, 2018.

[13] Y. Shen, N. C. Harris, S. Skirlo, M. Prabhu, T. Baehr-Jones, M. Hochberg, X. Sun, S. Zhao, H. Larochelle, D. Englund, and M. Soljacic, "Deep learning with coherent nanophotonic circuits," *Nature Photonics*, vol. 11, no. 7, pp. 441–446, 2017.

[14] C. Berger, M. A. Kossel, C. Menolfi, T. Morf, T. Toifl, and M. L. Schmatz, "High-density optical interconnects within large-scale systems," in *VCSELs and Optical Interconnects*, H. Thienpont and J. Danckaert, Eds., vol. 4942, International Society for Optics and Photonics. SPIE, 2003, pp. 222 – 235.

[15] A. Boletti, D. Giacomuzzi, G. Parladori, P. Boffi, M. Ferrario, and M. Martinelli, "Performance comparison between electrical copper-based and optical fiber-based backplanes," *Opt. Express*, vol. 21, no. 16, pp. 19 202–19 208, Aug 2013.

[16] D. A. B. Miller, "Rationale and challenges for optical interconnects to electronic chips," *Proceedings of the IEEE*, vol. 88, no. 6, pp. 728–749, Jun 2000.

[17] J. W. Goodman, F. J. Leonberger, S. Kung, and R. A. Athale, "Optical interconnections for VLSI systems," *Proceedings of the IEEE*, vol. 72, no. 7, pp. 850–866, Jul 1984.

[18] P. De Dobbelaere, A. Narasimha, A. Mekis, B. Welch, C. Bradbury, C. Sohn, D. Song, D. Foltz, D. Guckenberger, G. Masini, J. Schramm, J. White, J. Redman, K. Yokoyama, M. Harrison, M. Peterson, M. Mack, M. Sharp, R. LeBlanc, S. Abdalla, S. Gloeckner, S. Hovey, S. Jackson, S. Sahni, S. Yu, T. Pinguet, and Y. Liang, "Silicon photonics for high data rate optical interconnect," in *2012 Optical Interconnects Conference*, May 2012, pp. 113–114.

[19] R. Meade, S. Ardalan, M. Davenport, J. Fini, C. Sun, M. Wade, A. Wright-Gladstein, and C. Zhang, "TeraPHY: A high-density electronic-photonic chiplet for optical I/O from a multi-chip module," in *2019 Optical Fiber Communications Conference and Exhibition (OFC)*, Marc 2019, pp. 1–3.

[20] J. S. Orcutt, D. M. Gill, J. Proesel, J. Ellis-Monaghan, F. Horst, T. Barwicz, C. Xiong, F. G. Anderson, A. Agrawal, Y. Martin, C. W. Baks, M. Khater, J. C. Rosenberg, W. D. Sacher, J. Hofrichter, E. Kiewra, A. D. Stricker, F. Libsch, B. Offrein, M. Meghelli, N. B. Feilchenfeld, W. Haensch, and W. M. J. Green, "Monolithic silicon photonics at 25 Gb/s," in *Optical Fiber Communication Conference*.   Optical Society of America, 2016, p. Th4H.1.

[21] A. J. Zilkie, P. Srinivasan, A. Trita, T. Schrans, G. Yu, J. Byrd, D. A. Nelson, K. Muth, D. Lerose, M. Alalusi, K. Masuda, M. Ziebell, H. Abediasl, J. Drake, G. Miller, H. Nykanen, E. Kho, Y. Liu, H. Liang, H. Yang, F. H. Peters, A. S. Nagra, and A. G. Rickman, "Multi-micron silicon photonics platform for highly manufacturable and versatile photonic integrated circuits," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 25, no. 5, pp. 1–13, Sep 2019.

[22] M. Raj, Y. Frans, P. Chiang, S. L. Chaitanya Ambatipudi, D. Mahashin, P. De Heyn, S. Balakrishnan, J. Van Campenhout, J. Grayson, M. Epitaux, and K. Chang, "Design of a 50-Gb/s hybrid integrated si-photonic optical link in 16-nm FinFET," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 4, pp. 1086–1095, 2020.

[23] A. Alduino and M. Paniccia, "Wiring electronics with light," *Nature Photonics*, vol. 1, no. 3, pp. 153–155, 2007.

[24] M. J. R. Heck, H. W. Chen, A. W. Fang, B. R. Koch, D. Liang, H. Park, M. N. Sysak, and J. E. Bowers, "Hybrid silicon photonics for optical interconnects,"

277

IEEE Journal of Selected Topics in Quantum Electronics, vol. 17, no. 2, pp. 333–346, Marc 2011.

[25] D. Liang and J. E. Bowers, "Recent progress in lasers on silicon," *Nature Photonics*, vol. 4, pp. 511–517, Jul 2010.

[26] C. Sun, M. T. Wade, Y. Lee, J. S. Orcutt, L. Alloatti, M. S. Georgas, A. S. Waterman, J. M. Shainline, R. R. Avizienis, S. Lin, B. R. Moss, R. Kumar, F. Pavanello, A. H. Atabaki, H. M. Cook, A. J. Ou, J. C. Leu, Y. Chen, K. Asanovic, R. J. Ram, M. A. Popovic, and V. M. Stojanovic, "Single-chip microprocessor that communicates directly using light," *Nature*, vol. 528, pp. 534–538, 2015.

[27] J. S. Orcutt, B. Moss, C. Sun, J. Leu, M. Georgas, J. Shainline, E. Zgraggen, H. Li, J. Sun, M. Weaver, S. Urošević, M. Popović, R. J. Ram, and V. Stojanović, "Open foundry platform for high-performance electronic-photonic integration," *Opt. Express*, vol. 20, no. 11, pp. 12 222–12 232, May 2012.

[28] V. Stojanović, R. J. Ram, M. Popović, S. Lin, S. Moazeni, M. Wade, C. Sun, L. Alloatti, A. Atabaki, F. Pavanello, N. Mehta, and P. Bhargava, "Monolithic silicon-photonic platforms in state-of-the-art CMOS SOI processes," *Opt. Express*, vol. 26, no. 10, pp. 13 106–13 121, May 2018.

[29] M. Wade, M. Davenport, M. de Cea Falco, P. Bhargava, J. Fini, D. Van Orden, R. Meade, E. Yeung, R. Ram, M. Popović, V. Stojanović, and C. Sun, "A bandwidth-dense, low power electronic-photonic platform and architecture for multi-Tbps optical I/O," in *2018 European Conference on Optical Communication (ECOC)*, Sep 2018, pp. 1–3.

[30] J. Clarke and F. K. Wilhelm, "Superconducting quantum bits," *Nature*, vol. 453, p. 1031, Jun 2008.

[31] J. M. Gambetta, J. Chow, and M. Steffen, "Building logical qubits in a superconducting quantum computing system," *npj Quantum Information*, vol. 3, no. 2, 2017.

[32] V. Giovannetti, S. Lloyd, and L. Maccone, "Quantum metrology," *Phys. Rev. Lett.*, vol. 96, p. 010401, Jan 2006.

[33] M. L. Laboratory, "Forecasting superconductive electronics technology," *The Next Wave*, vol. 20, no. 3, 2014.

[34] D. S. Holmes, A. L. Ripple, and M. A. Manheimer, "Energy-efficient superconducting computing—power budgets and requirements," *IEEE Transactions on Applied Superconductivity*, vol. 23, no. 3, Jun 2013.

[35] Q. Y. Zhao, D. Zhu, N. Calandri, A. E. Dane, A. N. McCaughan, F. Bellei, H.-Z. H. Z. Wang, D. F. Santavicca, and K. K. Berggren, "Single-photon imager based on a superconducting nanowire delay line," *Nature Photonics*, vol. 11, p. 247, Mar 2017.

[36] D. M. Boroson, B. S. Robinson, D. V. Murphy, D. A. Burianek, F. Khatri, J. M. Kovalik, Z. Sodnik, and D. M. Cornwell, "Overview and results of the Lunar Laser Communication Demonstration," in *Free-Space Laser Communication and Atmospheric Propagation XXVI*, H. Hemmati and D. M. Boroson, Eds., vol. 8971, International Society for Optics and Photonics.   SPIE, 2014, pp. 213 – 223.

[37] B. S. Robinson, A. J. Kerman, E. A. Dauler, R. J. Barron, D. O. Caplan, M. L. Stevens, J. J. Carney, S. A. Hamilton, J. K. Yang, and K. K. Berggren, "781 Mbit/s photon-counting optical communications using a superconducting nanowire detector," *Opt. Lett.*, vol. 31, no. 4, pp. 444–446, Feb 2006.

[38] C. M. Natarajan, M. G. Tanner, and R. H. Hadfield, "Superconducting nanowire single-photon detectors: physics and applications," *Superconductor Science and Technology*, vol. 25, no. 6, p. 063001, apr 2012.

[39] A. Biswas, M. Srinivasan, R. Rogalin, S. Piazzolla, J. Liu, B. Schratz, A. Wong, E. Alerstam, M. Wright, W. T. Roberts, J. Kovalik, G. Ortiz, A. Na-Nakornpanom, M. Shaw, C. Okino, K. Andrews, M. Peng, D. Orozco, and W. Klipstein, "Status of NASA's deep space optical communication technology demonstration," in *2017 IEEE International Conference on Space Optical Systems and Applications (ICSOS)*, Nov 2017, pp. 23–27.

[40] H. Zhang, L. Xiao, B. Luo, J. Guo, L. Zhang, and J. Xie, "The potential and challenges of time-resolved single-photon detection based on current-carrying superconducting nanowires," *Journal of Physics D: Applied Physics*, vol. 53, no. 1, p. 013001, oct 2019.

[41] A. McCarthy, N. J. Krichel, N. R. Gemmell, X. Ren, M. G. Tanner, S. N. Dorenbos, V. Zwiller, R. H. Hadfield, and G. S. Buller, "Kilometer-range, high resolution depth imaging via 1560 nm wavelength single-photon detection," *Opt. Express*, vol. 21, no. 7, pp. 8904–8915, Apr 2013.

[42] G. N. Gol'tsman, O. Okunev, G. Chulkova, A. Lipatov, A. Semenov, K. Smirnov, B. Voronov, A. Dzardanov, C. Williams, and R. Sobolewski, "Picosecond superconducting single-photon optical detector," *Applied Physics Letters*, vol. 79, no. 6, pp. 705–707, 2001.

[43] J. K. W. Yang, A. J. Kerman, E. A. Dauler, V. Anant, K. M. Rosfjord, and K. K. Berggren, "Modeling the electrical and thermal response of superconducting nanowire single-photon detectors," *IEEE Transactions on Applied Superconductivity*, vol. 17, no. 2, pp. 581–585, Jun 2007.

[44] C. Lv, W. Zhang, L. You, P. Hu, H. Wang, H. Li, C. Zhang, J. Huang, Y. Wang, X. Yang, Z. Wang, and X. Xie, "Improving maximum count rate of superconducting nanowire single-photon detector with small active area using series attenuator," *AIP Advances*, vol. 8, no. 10, p. 105018, 2018.

[45] E. E. Wollman, V. B. Verma, A. E. Lita, W. H. Farr, M. D. Shaw, R. P. Mirin, and S. W. Nam, "Kilopixel array of superconducting nanowire single-photon detectors," *Opt. Express*, vol. 27, no. 24, pp. 35 279–35 289, Nov 2019.

[46] K. K. Likharev and V. K. Semenov, "RSFQ logic/memory family: a new josephson-junction technology for sub-terahertz-clock-frequency digital systems," *IEEE Transactions on Applied Superconductivity*, vol. 1, no. 1, pp. 3–28, Marc 1991.

[47] T. D. Ladd, F. Jelezko, R. Laflamme, Y. Nakamura, C. Monroe, and J. L. O'Brien, "Quantum computers," *Nature*, vol. 464, no. 7285, pp. 45–53, 2010.

[48] J. I. Cirac and P. Zoller, "Quantum computations with cold trapped ions," *Phys. Rev. Lett.*, vol. 74, pp. 4091–4094, May 1995.

[49] C. Monroe, "Quantum information processing with atoms and photons," *Nature*, vol. 416, no. 6877, pp. 238–246, 2002.

[50] C. D. Bruzewicz, J. Chiaverini, R. McConnell, and J. M. Sage, "Trapped-ion quantum computing: Progress and challenges," *Applied Physics Reviews*, vol. 6, no. 2, p. 021314, 2019.

[51] P. Krantz, M. Kjaergaard, F. Yan, T. P. Orlando, S. Gustavsson, and W. D. Oliver, "A quantum engineer's guide to superconducting qubits," *Applied Physics Reviews*, vol. 6, no. 2, p. 021318, 2019.

[52] A. H. Myerson, D. J. Szwer, S. C. Webster, D. T. C. Allcock, M. J. Curtis, G. Imreh, J. A. Sherman, D. N. Stacey, A. M. Steane, and D. M. Lucas, "High-fidelity readout of trapped-ion qubits," *Phys. Rev. Lett.*, vol. 100, p. 200502, May 2008.

[53] T. Walter, P. Kurpiers, S. Gasparinetti, P. Magnard, A. Potočnik, Y. Salathé, M. Pechal, M. Mondal, M. Oppliger, C. Eichler, and A. Wallraff, "Rapid high-fidelity single-shot dispersive readout of superconducting qubits," *Phys. Rev. Applied*, vol. 7, p. 054020, May 2017.

[54] C. Macklin, K. O'Brien, D. Hover, M. E. Schwartz, V. Bolkhovsky, X. Zhang, W. D. Oliver, and I. Siddiqi, "A near–quantum-limited josephson traveling-wave parametric amplifier," *Science*, 2015.

[55] V. Parma, "Cryostat Design," *arXiv e-prints*, p. arXiv:1501.07154, 2015.

[56] J. I. Colless and D. J. Reilly, "Modular cryogenic interconnects for multi-qubit devices," *Review of Scientific Instruments*, vol. 85, no. 11, p. 114706, 2014.

[57] F. Kuemmeth and C. M. Marcus, "Reducing noise and temperature during measurements in cryostats," Marc 2015, uS Patent App. 14/011,176.

[58] J. P. G. van Dijk, E. Charbon, and F. Sebastiano, "The electronic interface for quantum processors," *arXiv e-prints*, p. arXiv:1811.01693, 2018.

[59] D. J. Reilly, "Challenges in Scaling-up the Control Interface of a Quantum Computer," *arXiv e-prints*, p. arXiv:1912.05114, 2019.

[60] A. N. McCaughan, "Readout architectures for superconducting nanowire single photon detectors," *Superconductor Science and Technology*, vol. 31, no. 4, p. 040501, feb 2018.

[61] J. E. Jense, W. A. Tuttle, R. B. Stewart, H. Brechna, and A. G. Prodell, *Selected Cryogenic Data Notebook*. Brookhaven National Laboratory, 1980.

[62] "Thorlabs TMM36 premium microwave cable," 2020. [Online]. Available: https://www.thorlabs.com/newgrouppage9.cfm?objectgroup_id=9827

[63] W. Beyene, Y.-C. Hahm, J. Ren, D. Secker, D. Mullen, and Y. Shlepnev, "Lessons learned: How to make predictable PCB interconnects for data rates of 50 Gbps and beyond," 2017. [Online]. Available: https://www.signalintegrityjournal.com/articles/

581-lessons-learned-how-to-make-predictable-pcb-interconnects-for-data-rates\
-of-50-gbps-and-beyond

[64] D. Gupta, J. C. Bardin, A. Inamdar, A. Dayalu, S. Sarwana, P. Ravindran, S. Chang, A. H. Coskun, and M. Ghadiri Sadrabadi, "Low-power high-speed hybrid temperature heterogeneous technology digital data link," *IEEE Transactions on Applied Superconductivity*, vol. 23, no. 3, Jun 2013.

[65] S. Wuensch, T. Ortlepp, E. Crocoll, F. H. Uhlmann, and M. Siegel, "Cryogenic semiconductor amplifier for RSFQ-circuits with high data rates at 4.2 K," *IEEE Transactions on Applied Superconductivity*, vol. 19, no. 3, pp. 574–579, Jun 2009.

[66] C. Cahall, D. J. Gauthier, and J. Kim, "Scalable cryogenic readout circuit for a superconducting nanowire single-photon detector system," *Review of Scientific Instruments*, vol. 89, no. 6, 2018.

[67] Y. J. Feng, X. Meng, S. R. Whiteley, T. Van Duzer, K. Fujiwara, H. Miyakawa, and N. Yoshikawa, "Josephson-CMOS hybrid memory with ultra-high-speed interface circuit," *IEEE Transactions on Applied Superconductivity*, vol. 13, no. 2, pp. 467–470, Jun 2003.

[68] T. V. Duzer and S. Kumar, "Semiconductor-superconductor hybrid electronics," *Cryogenics*, vol. 30, no. 12, pp. 1014 – 1023, 1990.

[69] D. Wei, S. R. Whiteley, L. Zheng, H. Park, H. Kim, and T. Van Duzer, "New josephson-CMOS interface amplifier," *IEEE Transactions on Applied Superconductivity*, vol. 21, no. 3, pp. 805–808, Jun 2011.

[70] Q.-Y. Zhao, A. N. McCaughan, A. E. Dane, K. K. Berggren, and T. Ortlepp, "A nanocryotron comparator can connect single-flux-quantum circuits to conventional electronics," *Superconductor Science and Technology*, vol. 30, no. 4, p. 044002, Mar 2017.

[71] S. J. Pauka, K. Das, R. Kalra, A. Moini, Y. Yang, M. Trainer, A. Bousquet, C. Cantaloube, N. Dick, G. C. Gardner, M. J. Manfra, and D. J. Reilly, "A Cryogenic Interface for Controlling Many Qubits," *arXiv e-prints*, p. arXiv:1912.01299, 2019.

[72] B. Patra, R. M. Incandela, J. P. G. van Dijk, H. A. R. Homulle, L. Song, M. Shahmohammadi, R. B. Staszewski, A. Vladimirescu, M. Babaie, F. Sebastiano, and E. Charbon, "Cryo-CMOS circuits and systems for quantum

computing applications," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, Jan 2018.

[73] J. C. Bardin, P. Ravindran, S. Chang, R. Kumar, J. A. Stern, M. D. Shaw, D. S. Russell, and W. H. Farr, "A high-speed cryogenic SiGe channel combiner IC for large photon-starved SNSPD arrays," in *2013 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Sep 2013, pp. 215–218.

[74] D. Ristè, M. Dukalski, C. A. Watson, G. de Lange, M. J. Tiggelman, Y. M. Blanter, K. W. Lehnert, R. N. Schouten, and L. DiCarlo, "Deterministic entanglement of superconducting qubits by parity measurement and feedback," *Nature*, vol. 502, no. 7471, pp. 350–354, 2013.

[75] D. Ristè, S. Poletto, M.-Z. Huang, A. Bruno, V. Vesterinen, O.-P. Saira, and L. DiCarlo, "Detecting bit-flip errors in a logical qubit using stabilizer measurements," *Nature Communications*, vol. 6, no. 1, p. 6983, 2015.

[76] H. Homulle, S. Visser, B. Patra, G. Ferrari, E. Prati, F. Sebastiano, and E. Charbon, "A reconfigurable cryogenic platform for the classical control of quantum processors," *Review of Scientific Instruments*, vol. 88, no. 4, p. 045103, 2017.

[77] C. A. Brackett, "Dense wavelength division multiplexing networks: principles and applications," *IEEE Journal on Selected Areas in Communications*, vol. 8, no. 6, pp. 948–964, Aug 1990.

[78] K. Preston, N. Sherwood-Droz, J. S. Levy, and M. Lipson, "Performance guidelines for WDM interconnects based on silicon microring resonators," in *CLEO: 2011 - Laser Science to Photonic Applications*, May 2011, pp. 1–2.

[79] L. A. Bunz, S. V. Rylov, and E. K. Track, "Laser diodes for optical readout of cryo-electronics," in *Infrared Readout Electronics II*, E. R. Fossum, Ed., vol. 2226, International Society for Optics and Photonics. SPIE, 1994, pp. 50 – 59.

[80] L. A. Bunz, R. Robertazzi, and S. Rylov, "An optically coupled superconducting analog to digital converter," *IEEE Transactions on Applied Superconductivity*, vol. 7, no. 2, pp. 2972–2974, Jun 1997.

[81] Bo Lu, Yin-Chen Lu, J. Cheng, R. P. Schneider, J. C. Zolper, and G. Goncher, "Gigabit-per-second cryogenic optical link using optimized low-temperature

AlGaAs-GaAs vertical-cavity surface-emitting lasers," *IEEE Journal of Quantum Electronics*, vol. 32, no. 8, pp. 1347–1359, Aug 1996.

[82] A. N. McCaughan, V. B. Verma, S. M. Buckley, J. P. Allmaras, A. G. Kozorezov, A. N. Tait, S. W. Nam, and J. M. Shainline, "A superconducting thermal switch with ultrahigh impedance for interfacing superconductors to semiconductors," *Nature Electronics*, vol. 2, no. 10, pp. 451–456, 2019.

[83] B. Rabinovici, "Optical readout for cryogenic circuits," *Review of Scientific Instruments*, vol. 32, no. 6, pp. 747–748, 1961.

[84] T. Liu, D. Gong, S. Hou, C. Liu, D. S. Su, P. K. Teng, A. C. Xiang, and J. Ye, "Cryogenic digital data links for the liquid argon time projection chamber," *Journal of Instrumentation*, vol. 7, no. 01, pp. C01 091–C01 091, jan 2012.

[85] A. R. Johnston, D. T.-H. Liu, S. Forouhar, G. F. Lutes, J. L. Maserjian, and E. R. Fossum, "Optical links for cryogenic focal plane array readout," in *Infrared Detectors and Instrumentation*, A. M. Fowler, Ed., vol. 1946, International Society for Optics and Photonics. SPIE, 1993, pp. 375 – 383.

[86] L. A. Coldren and S. Corzine, *Diode Lasers and Photonic Integrated Circuits*. John Wiley & Sons, Ltd, 2012.

[87] E. L. Wooten, K. M. Kissa, A. Yi-Yan, E. J. Murphy, D. A. Lafaw, P. F. Hallemeier, D. Maack, D. V. Attanasio, D. J. Fritz, G. J. McBrien, and D. E. Bossi, "A review of lithium niobate modulators for fiber-optic communications systems," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 6, no. 1, pp. 69–82, Jan 2000.

[88] G. T. Reed, G. Mashanovich, F. Y. Gardes, and D. J. Thomson, "Silicon optical modulators," *Nature Photonics*, vol. 4, pp. 518–526, Jul 2010.

[89] R. A. Griffin and A. C. Carter, "Advances in InP optical modulators," in *Asia Optical Fiber Communication and Optoelectronic Exposition and Conference*. Optical Society of America, 2008, p. SuF6.

[90] S. Koeber, R. Palmer, M. Lauermann, W. Heni, D. L. Elder, D. Korn, M. Woessner, L. Alloatti, S. Koenig, P. C. Schindler, H. Yu, W. Bogaerts, L. R. Dalton, W. Freude, J. Leuthold, and C. Koos, "Femtojoule electro-optic modulation using a silicon-organic hybrid device," *Light: Science & Applications*, vol. 4, no. 2, pp. e255–e255, 2015.

[91] S. Luo, Y. Wang, X. Tong, and Z. Wang, "Graphene-based optical modulators," *Nanoscale Research Letters*, vol. 10, no. 1, p. 199, 2015.

[92] C. Haffner, D. Chelladurai, Y. Fedoryshyn, A. Josten, B. Baeuerle, W. Heni, T. Watanabe, T. Cui, B. Cheng, S. Saha, D. L. Elder, L. R. Dalton, A. Boltasseva, V. M. Shalaev, N. Kinsey, and J. Leuthold, "Low-loss plasmon-assisted electro-optic modulator," *Nature*, vol. 556, no. 7702, pp. 483–486, 2018.

[93] J. Witzens, "High-speed silicon photonics modulators," *Proceedings of the IEEE*, vol. 106, no. 12, pp. 2158–2182, Dec 2018.

[94] G. Li, A. V. Krishnamoorthy, I. Shubin, J. Yao, Y. Luo, H. Thacker, X. Zheng, K. Raj, and J. E. Cunningham, "Ring resonator modulators in silicon for interchip photonic links," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 19, no. 6, pp. 95–113, Nov 2013.

[95] M. de Cea, *Zero Change CMOS Microring Modulators at 1550 nm: Modeling and Characterization*, Universitat Politecnica de Catalunya, Jun. 2017.

[96] M. Berciano, G. Marcaud, P. Damas, X. Le Roux, P. Crozat, C. Alonso Ramos, D. Pérez Galacho, D. Benedikovic, D. Marris-Morini, E. Cassan, and L. Vivien, "Fast linear electro-optic effect in a centrosymmetric semiconductor," *Communications Physics*, vol. 1, no. 1, p. 64, 2018.

[97] G. Treyz, "Silicon Mach-Zehnder waveguide interferometers operating at 1.3 μm," *Electronic Letters*, vol. 27 (2), pp. 118–120, Jan 1991.

[98] L. Liao, A. Liu, D. Rubin, J. Basak, Y. Chetrit, H. Nguyen, R. Cohen, N. Izhaky, and M. Paniccia, "40 Gbit/s silicon optical modulator for high-speed applications," *Electronics Letters*, vol. 43, pp. 1196–1197(1), Oct 2007.

[99] E. Timurdogan, C. M. Sorace-Agaskar, J. Sun, E. S. Hosseini, A. Biberman, and M. R. Watts, "An ultralow power athermal silicon modulator," *Nature Communications*, vol. 5, Jun 2014.

[100] R. Soref and B. Benett, "Electrooptical effects in silicon," *IEEE J. Quantum Elect*, vol. QE-23, pp. 123–129, Jan 1987.

[101] Q. Xu, S. Manipatruni, B. Schmidt, J. Shakya, and M. Lipson, "12.5 Gbit/s carrier-injection-based silicon micro-ring silicon modulators," *Opt. Express*, vol. 15, no. 2, pp. 430–436, Jan 2007.

[102] K. Debnath, D. J. Thomson, W. Zhang, A. Z. Khokhar, C. Littlejohns, J. Byers, L. Mastronardi, M. K. Husain, F. Y. Gardes, G. T. Reed, and S. Saito, "20 Gbps silicon lateral MOS-capacitor electro-optic modulator," in *Conference on Lasers and Electro-Optics*. Optical Society of America, 2018, p. SM3B.5.

[103] K. Zhong, X. Zhou, J. Huo, C. Yu, C. Lu, and A. P. T. Lau, "Digital signal processing for short-reach optical communications: A review of current technologies and future trends," *Journal of Lightwave Technology*, vol. 36, no. 2, pp. 377–400, Jan 2018.

[104] A. Joshi, C. Batten, Y. J. Kwon, S. Beamer, I. Shamim, K. Asanovic, and V. Stojanovic, "Silicon-photonic clos networks for global on-chip communication," in *2009 3rd ACM/IEEE International Symposium on Networks-on-Chip*, May 2009, pp. 124–133.

[105] D. G. Rabus, *Ring Resonators: Theory and Modeling*. Berlin, Heidelberg: Springer Berlin Heidelberg, 2007, pp. 3–40.

[106] W. Bogaerts, P. De Heyn, T. Van Vaerenbergh, K. De Vos, S. Kumar Selvaraja, T. Claes, P. Dumon, P. Bienstman, D. Van Thourhout, and R. Baets, "Silicon microring resonators," *Laser & Photonics Reviews*, vol. 6, no. 1, pp. 47–73, 2012.

[107] A. W. Elshaari, I. E. Zadeh, K. D. Jöns, and V. Zwiller, "Thermo-optic characterization of silicon nitride resonators for cryogenic photonic circuits," *IEEE Photonics Journal*, vol. 8, no. 3, pp. 1–9, Jun 2016.

[108] M. Gehl, C. Long, D. Trotter, A. Starbuck, A. Pomerene, J. B. Wright, S. Melgaard, J. Siirola, A. L. Lentine, and C. DeRose, "Operation of high-speed silicon photonic micro-disk modulators at cryogenic temperatures," *Optica*, vol. 4, no. 3, pp. 374–382, Mar 2017.

[109] F. Eltes, J. Barreto, D. Caimi, S. Karg, A. A. Gentile, A. Hart, P. Stark, N. Meier, M. G. Thompson, J. Fompeyrine, and S. Abel, "An integrated cryogenic optical modulator," *arXiv e-prints*, p. arXiv:1904.10902, Apr 2019.

[110] R. Sobolewski and J. . Park, "Magneto-optical modulator for superconducting digital output interface," *IEEE Transactions on Applied Superconductivity*, vol. 11, no. 1, pp. 727–730, Marc 2001.

[111] J. D. Morse, K. G. McCammon, C. F. McConaghy, D. A. Masquelier, H. E. Garrett, and M. E. Lowry, "Characterization of lithium niobate electro-optic modulators at cryogenic temperatures," in *Design, Simulation, and Fabrication of Optoelectronic Devices and Circuits*, M. N. Armenise, Ed., vol. 2150, International Society for Optics and Photonics. SPIE, 1994, pp. 283 – 291.

[112] P. R. Stanfield, A. J. Leenheer, C. P. Michael, R. Sims, and M. Eichenfield, "CMOS-compatible, piezo-optomechanically tunable photonics for visible wavelengths and cryogenic temperatures," *Opt. Express*, vol. 27, no. 20, pp. 28 588–28 605, Sep 2019.

[113] E. A. Gutiérrez-D., M. J. Deen, and C. Claeys, *Low Temperature Electronics*. Academic Press, 2001.

[114] A. Beckers, F. Jazaeri, A. Ruffino, C. Bruschini, A. Baschirotto, and C. Enz, "Cryogenic characterization of 28 nm bulk CMOS technology for quantum computing," in *2017 47th European Solid-State Device Research Conference (ESS-DERC)*, Sep 2017, pp. 62–65.

[115] A. Beckers, F. Jazaeri, and C. Enz, "Cryogenic MOS transistor model," *IEEE Transactions on Electron Devices*, vol. 65, no. 9, pp. 3617–3625, Sep 2018.

[116] D. C. Brown, "The promise of cryogenic solid-state lasers," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 11, no. 3, pp. 587–599, May 2005.

[117] E. Goobar, G. Peters, G. Fish, and L. A. Coldren, "Highly efficient vertical-cavity surface-emitting lasers optimized for low-temperature operation," *IEEE Photonics Technology Letters*, vol. 7, no. 8, pp. 851–853, Aug 1995.

[118] D. P. Foty, "Impurity ionization in mosfets at very low temperatures," *Cryogenics*, vol. 30, no. 12, pp. 1056 – 1063, 1990.

[119] N. F. Mott, "Metal-insulator transition," *Rev. Mod. Phys.*, vol. 40, pp. 677–683, Oct 1968.

[120] P. W. Chapman, O. N. Tufte, J. D. Zook, and D. Long, "Electrical properties of heavily doped silicon," *Journal of Applied Physics*, vol. 34, no. 11, pp. 3291–3295, 1963.

[121] P. Norton, T. Braggins, and H. Levinstein, "Recombination of electrons at ionized donors in silicon at low temperatures," *Phys. Rev. Lett.*, vol. 30, pp. 488–489, Mar 1973.

[122] R. Brüggemann, M. Xu, J. Alvarez, M. Boutchich, and J.-P. Kleider, "Temperature dependence of the radiative recombination coefficient in crystalline silicon by spectral and modulated photoluminescence," *physica status solidi (RRL) – Rapid Research Letters*, vol. 11, no. 6, p. 1700066, 2017.

[123] W. H. P. Pernice, C. Schuck, M. Li, and H. X. Tang, "Carrier and thermal dynamics of silicon photonic resonators at cryogenic temperatures," *Opt. Express*, vol. 19, no. 4, pp. 3290–3296, Feb 2011.

[124] G. Swartz, "Low-temperature hall coefficient and conductivity in heavily doped silicon," *Journal of Physics and Chemistry of Solids*, vol. 12, no. 3, pp. 245 – 259, 1960.

[125] J. R. Meyer and F. J. Bartoli, "Phase-shift calculation of electron mobility in n-type silicon at low temperatures," *Phys. Rev. B*, vol. 24, pp. 2089–2100, Aug 1981.

[126] "Ioffe institute - Si material properties database," http://www.ioffe.ru/SVA/NSM/Semicond/Si/.

[127] J. Komma, C. Schwarz, G. Hofmann, D. Heinert, and R. Nawrodt, "Thermo-optic coefficient of silicon at 1550 nm and cryogenic temperatures," *Applied Physics Letters*, vol. 101, no. 4, p. 041905, 2012.

[128] G. P. Agrawal, *Fiber-Optic Communication Systems*, 4th ed. The Atrium, Southern Gate, Chichester, West Sussex PO19 8SQ, England: John Wiley & Sons Ltd, 2010.

[129] D. Zhu, M. Colangelo, B. A. Korzh, Q.-Y. Zhao, S. Frasca, A. E. Dane, A. E. Velasco, A. D. Beyer, J. P. Allmaras, E. Ramirez, W. J. Strickland, D. F. Santavicca, M. D. Shaw, and K. K. Berggren, "Superconducting nanowire single-photon detector with integrated impedance-matching taper," *Applied Physics Letters*, vol. 114, no. 4, p. 042601, 2019.

[130] S. Krinner, S. Storz, P. Kurpiers, P. Magnard, J. Heinsoo, R. Keller, J. Lütolf, C. Eichler, and A. Wallraff, "Engineering cryogenic setups for 100-qubit scale superconducting circuit systems," *EPJ Quantum Technology*, vol. 6, no. 1, p. 2, 2019.

[131] L. Carroll, J.-S. Lee, C. Scarcella, K. Gradkowski, M. Duperron, H. Lu, Y. Zhao, C. Eason, P. Morrissey, M. Rensing, S. Collins, H. Y. Hwang, and

P. O'Brien, "Photonic packaging: Transforming silicon photonic integrated circuits into photonic devices," *Applied Sciences*, vol. 6, no. 12, p. 426, 2016.

[132] E. Bardalen, M. N. Akram, H. Malmbekk, and P. Ohlckers, "Review of devices, packaging, and materials for cryogenic optoelectronics," *Journal of Microelectronics and Electronic Packaging*, vol. 12, no. 4, pp. 189–204, 2015.

[133] J. M. Shainline, S. M. Buckley, N. Nader, C. M. Gentry, K. C. Cossel, J. W. Cleary, M. Popović, N. R. Newbury, S. W. Nam, and R. P. Mirin, "Room-temperature-deposited dielectrics and superconductors for integrated photonics," *Opt. Express*, vol. 25, no. 9, pp. 10 322–10 334, May 2017.

[134] A. J. Miller, A. E. Lita, B. Calkins, I. Vayshenker, S. M. Gruber, and S. W. Nam, "Compact cryogenic self-aligning fiber-to-detector coupling with losses below one percent," *Opt. Express*, vol. 19, no. 10, pp. 9102–9110, May 2011.

[135] T. P. McKenna, R. N. Patel, J. D. Witmer, R. V. Laer, J. A. Valery, and A. H. Safavi-Naeini, "Cryogenic packaging of an optomechanical crystal," *Opt. Express*, vol. 27, no. 20, pp. 28 782–28 791, Sep 2019.

[136] M. de Cea, A. H. Atabaki, L. Alloatti, M. Wade, M. Popovic, and R. J. Ram, "A thin silicon photonic platform for telecommunication wavelengths," in *2017 European Conference on Optical Communication (ECOC)*, Sep 2017, pp. 1–3.

[137] J. S. Orcutt, "Monolithic electronic-photonic integration in state-of-the-art CMOS processes," Ph.D. dissertation, Massachusetts Institite of Technology, 2012.

[138] M. T. Wade, "Devices and systems-on-chip for photonic communication links in a microprocessor," Ph.D. dissertation, University of Colorado Boulder, 2015.

[139] L. Alloatti, D. Cheian, and R. J. Ram, "High-speed modulator with interleaved junctions in zero-change CMOS photonics," *Applied Physics Letters*, vol. 108, no. 13, p. 131101, 2016.

[140] D. Cheian, "T-junction resonant modulators and detectors in CMOS," Master's thesis, Massachusetts Institite of Technology, 2016.

[141] J. Notaros, F. Pavanello, M. T. Wade, C. M. Gentry, A. Atabaki, L. Alloatti, R. J. Ram, and M. A. Popović, "Ultra-efficient CMOS fiber-to-chip grating couplers," in *Optical Fiber Communication Conference*, 2016.

[142] J. del Alamo, *Integrated Microelectronic Devices: Physics and Modeling.* Pearson, 2017.

[143] A. K. Jonscher, "p-n junctions at very low temperatures," *British Journal of Applied Physics*, vol. 12, no. 8, pp. 363–371, aug 1961.

[144] S. Koenig and G. Gunther-Mohr, "The low temperature electrical conductivity of n-type germanium," *Journal of Physics and Chemistry of Solids*, vol. 2, no. 4, pp. 268 – 283, 1957.

[145] W. W. Anderson and H. J. Hoffman, "Field ionization of deep levels in semiconductors with applications to Hg(1-x)Cd(x)Te p-n junctions," *Journal of Applied Physics*, vol. 53, no. 12, pp. 9130–9145, 1982.

[146] J. C. S. Woo, J. D. Plummer, and J. M. C. Stork, "Non-ideal base current in bipolar transistors at low temperatures," *IEEE Transactions on Electron Devices*, vol. 34, no. 1, pp. 130–138, 1987.

[147] G. A. M. Hurkx, D. B. M. Klaassen, M. P. G. Knuvers, and F. G. O'Hara, "A new recombination model describing heavy-doping effects and low-temperature behaviour," in *International Technical Digest on Electron Devices Meeting*, 1989, pp. 307–310.

[148] B. P. Merz and R. A. Treumann, "Relaxation oscillation phenomena in cryogenic Si diodes," *Applied Physics Letters*, vol. 78, no. 13, pp. 1876–1878, 2001.

[149] V. Borblik, Y. Shwarts, M. Shwarts, and A. Fonkich, "Concerning the nature of relaxation oscillations in silicon diodes in the cryogenic temperature region," *Cryogenics*, vol. 50, no. 6, pp. 417 – 420, 2010.

[150] H. T. Nguyen, F. E. Rougieux, B. Mitchell, and D. Macdonald, "Temperature dependence of the band-band absorption coefficient in crystalline silicon from photoluminescence," *Journal of Applied Physics*, vol. 115, no. 4, p. 043710, 2014.

[151] W. Spitzer and H. Y. Fan, "Infrared absorption in *n*-type silicon," *Phys. Rev.*, vol. 108, pp. 268–271, Oct 1957.

[152] P. E. Schmid, "Optical absorption in heavily doped silicon," *Phys. Rev. B*, vol. 23, pp. 5531–5536, May 1981.

[153] D. K. Schroder, "Carrier lifetimes in silicon," *IEEE Transactions on Electron Devices*, vol. 44, no. 1, pp. 160–170, 1997.

[154] H. T. Nguyen, S. C. Baker-Finch, and D. Macdonald, "Temperature dependence of the radiative recombination coefficient in crystalline silicon from spectral photoluminescence," *Applied Physics Letters*, vol. 104, no. 11, p. 112105, 2014.

[155] S. W. Johnston and R. K. Ahrenkiel, "Measurement of the temperature-dependent recombination lifetimes in photovoltaic materials," *AIP Conference Proceedings*, vol. 462, no. 1, pp. 505–510, 1999.

[156] M. Ichimura, "Temperature dependence of carrier recombination lifetime in Si wafers," *Journal of The Electrochemical Society*, vol. 145, no. 9, p. 3265, 1998.

[157] E. E. Wollman, V. B. Verma, A. D. Beyer, R. M. Briggs, B. Korzh, J. P. Allmaras, F. Marsili, A. E. Lita, R. P. Mirin, S. W. Nam, and M. D. Shaw, "UV superconducting nanowire single-photon detectors with high efficiency, low noise, and 4 K operating temperature," *Optics Express*, vol. 25, no. 22, pp. 26 792–26 801, Oct 2017.

[158] A. J. Kerman, J. K. W. Yang, R. J. Molnar, E. A. Dauler, and K. K. Berggren, "Electrothermal feedback in superconducting nanowire single-photon detectors," *Phys. Rev. B*, vol. 79, p. 100509, Mar 2009.

[159] K. K. Berggren, Q.-Y. Zhao, N. Abebe, M. Chen, P. Ravindran, A. McCaughan, and J. C. Bardin, "A superconducting nanowire can be modeled by using SPICE," *Superconductor Science and Technology*, vol. 31, no. 5, p. 055010, apr 2018.

[160] J. K. W. Yang, A. J. Kerman, E. A. Dauler, V. Anant, K. M. Rosfjord, and K. K. Berggren, "Modeling the electrical and thermal response of superconducting nanowire single-photon detectors," *IEEE Transactions on Applied Superconductivity*, vol. 17, no. 2, pp. 581–585, Jun 2007.

[161] R. H. Hadfield, A. J. Miller, S. W. Nam, R. L. Kautz, and R. E. Schwall, "Low-frequency phase locking in high-inductance superconducting nanowires," *Applied Physics Letters*, vol. 87, no. 20, p. 203505, 2005.

[162] V. B. Verma, B. Korzh, F. Bussières, R. D. Horansky, S. D. Dyer, A. E. Lita, I. Vayshenker, F. Marsili, M. D. Shaw, H. Zbinden, R. P. Mirin, and S. W. Nam,

"High-efficiency superconducting nanowire single-photon detectors fabricated from MoSi thin-films," *Opt. Express*, vol. 23, no. 26, pp. 33 792–33 801, Dec 2015.

[163] B. E. Vyhnalek, S. A. Tedder, and J. M. Nappier, "Performance and characterization of a modular superconducting nanowire single photon detector system for space-to-Earth optical communications links," in *Free-Space Laser Communication and Atmospheric Propagation XXX*, H. Hemmati and D. M. Boroson, Eds., vol. 10524, International Society for Optics and Photonics. SPIE, 2018, pp. 369 – 377.

[164] D. A. B. Miller, "Energy consumption in optical modulators for interconnects," *Opt. Express*, vol. 20, no. S2, pp. A293–A308, Mar 2012.

[165] C. Xiong, D. M. Gill, J. E. Proesel, J. S. Orcutt, W. Haensch, and W. M. J. Green, "Monolithic 56 Gb/s silicon photonic pulse-amplitude modulation transmitter," *Optica*, vol. 3, no. 10, pp. 1060–1065, Oct 2016.

[166] L. Chen, K. Preston, S. Manipatruni, and M. Lipson, "Integrated GHz silicon photonic interconnect with micrometer-scale modulators and detectors," *Opt. Express*, vol. 17, no. 17, pp. 15 248–15 256, Aug 2009.

[167] M. Webster, P. Gothoskar, V. Patel, D. Piede, S. Anderson, R. Tummidi, D. Adams, C. Appel, P. Metz, S. Sunder, B. Dama, and K. Shastri, "An efficient MOS-capacitor based silicon modulator and CMOS drivers for optical transmitters," in *11th International Conference on Group IV Photonics (GFP)*, 2014, pp. 1–2.

[168] C. Wang, M. Zhang, X. Chen, M. Bertrand, A. Shams-Ansari, S. Chandrasekhar, P. Winzer, and M. Loncar, "Integrated lithium niobate electro-optic modulators operating at CMOS-compatible voltages," *Nature*, vol. 562, no. 7725, pp. 101–104, 2018.

[169] W. Heni, Y. Fedoryshyn, B. Baeuerle, A. Josten, C. B. Hoessbacher, A. Messner, C. Haffner, T. Watanabe, Y. Salamin, U. Koch, D. L. Elder, L. R. Dalton, and J. Leuthold, "Plasmonic IQ modulators with attojoule per bit electrical energy consumption," *Nature Communications*, vol. 10, no. 1, p. 1694, 2019.

[170] J. Hofrichter, O. Raz, A. L. Porta, T. Morf, P. Mechet, G. Morthier, T. D. Vries, H. J. S. Dorren, and B. J. Offrein, "A low–power high–speed InP microdisk modulator heterogeneously integrated on a SOI waveguide," *Opt. Express*, vol. 20, no. 9, pp. 9363–9370, Apr 2012.

[171] D. Feng, S. Liao, H. Liang, J. Fong, B. Bijlani, R. Shafiiha, B. J. Luff, Y. Luo, J. Cunningham, A. V. Krishnamoorthy, and M. Asghari, "High speed GeSi electro-absorption modulator at 1550 nm wavelength on SOI waveguide," *Opt. Express*, vol. 20, no. 20, pp. 22 224–22 232, Sep 2012.

[172] Y. Hu, M. Pantouvaki, J. Van Campenhout, S. Brems, I. Asselberghs, C. Huyghebaert, P. Absil, and D. Van Thourhout, "Broadband 10 Gb/s operation of graphene electro-absorption modulator on silicon," *Laser & Photonics Reviews*, vol. 10, no. 2, pp. 307–316, 2016.

[173] B. Razavi, *Design of Analog CMOS Integrated Circuits*.   McGraw Hill, 2017.

[174] M. Casalino, G. Coppola, M. Iodice, I. Rendina, and L. Sirleto, "Near-infrared sub-bandgap all-silicon photodetectors: state of the art and perspectives," *Sensors*, vol. 10, no. 12, pp. 10 571–10 600, 2010.

[175] F. Morichetti, S. Grillanda, M. Carminati, G. Ferrari, M. Sampietro, M. J. Strain, M. Sorel, and A. Melloni, "Non-invasive on-chip light observation by contactless waveguide conductivity monitoring," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 20, no. 4, pp. 292–301, 2014.

[176] H. Yu, D. Korn, M. Pantouvaki, J. V. Campenhout, K. Komorowska, P. Verheyen, G. Lepage, P. Absil, D. Hillerkuss, L. Alloatti, J. Leuthold, R. Baets, and W. Bogaerts, "Using carrier-depletion silicon modulators for optical power monitoring," *Opt. Lett.*, vol. 37, no. 22, pp. 4681–4683, Nov 2012.

[177] H. Jayatilleka, K. Murray, M. Ángel Guillén-Torres, M. Caverley, R. Hu, N. A. F. Jaeger, L. Chrostowski, and S. Shekhar, "Wavelength tuning and stabilization of microring-based filters using silicon in-resonator photoconductive heaters," *Opt. Express*, vol. 23, no. 19, pp. 25 084–25 097, Sep 2015.

[178] X. Li, Z. Li, X. Xiao, H. Xu, J. Yu, and Y. Yu, "40 Gb/s all-silicon photodetector based on microring resonators," *IEEE Photonics Technology Letters*, vol. 27, no. 7, pp. 729–732, 2015.

[179] M. W. Geis, S. J. Spector, M. E. Grein, R. T. Schulein, J. U. Yoon, D. M. Lennon, S. Deneault, F. Gan, F. X. Kaertner, and T. M. Lyszczarz, "CMOS-compatible all-Si high-speed waveguide photodiodes with high responsivity in near-infrared communication band," *IEEE Photonics Technology Letters*, vol. 19, no. 3, pp. 152–154, 2007.

[180] P. Zhang, E. Tevaarwerk, B.-N. Park, D. E. Savage, G. K. Celler, I. Knezevic, P. G. Evans, M. A. Eriksson, and M. G. Lagally, "Electronic transport in nanometre-scale silicon-on-insulator membranes," *Nature*, vol. 439, no. 7077, pp. 703–706, Feb 2006.

[181] S. Grillanda and F. Morichetti, "Light-induced metal-like surface of silicon photonic waveguides," *Nature Communications*, vol. 6, no. 1, p. 8182, 2015.

[182] Y. Li and A. W. Poon, "Characterization of surface-state absorption in foundry-fabricated silicon ridge waveguides at 1550 nm using photocurrents," in *2016 Conference on Lasers and Electro-Optics (CLEO)*, 2016, pp. 1–2.

[183] A. Gil-Molina, I. Aldaya, J. L. Pita, L. H. Gabrielli, H. L. Fragnito, and P. Dainese, "Optical free-carrier generation in silicon nano-waveguides at 1550 nm," *Applied Physics Letters*, vol. 112, no. 25, p. 251104, 2018.

[184] M. Borselli, T. J. Johnson, and O. Painter, "Measuring the role of surface chemistry in silicon microphotonics," *Applied Physics Letters*, vol. 88, no. 13, p. 131114, 2006.

[185] G. Chiarotti, S. Nannarone, R. Pastore, and P. Chiaradia, "Optical absorption of surface states in ultrahigh vacuum cleaved (111) surfaces of Ge and Si," *Phys. Rev. B*, vol. 4, pp. 3398–3402, Nov 1971.

[186] L. Tsakalakos, J. E. Balch, J. Fronheiser, M.-Y. Shih, S. F. LeBoeuf, M. Pietrzykowski, P. J. Codella, B. A. Korevaar, O. Sulima, J. Rand, A. Davu-luru, and U. D. Rapol, "Strong broadband optical absorption in silicon nanowire films," *Journal of Nanophotonics*, vol. 1, no. 1, pp. 1 – 10, 2007.

[187] L. Alloatti and R. J. Ram, "Resonance-enhanced waveguide-coupled silicon-germanium detector," *Applied Physics Letters*, vol. 108, no. 7, p. 071105, 2016.

[188] R. Braunstein, A. R. Moore, and F. Herman, "Intrinsic optical absorption in germanium-silicon alloys," *Phys. Rev.*, vol. 109, pp. 695–710, Feb 1958.

[189] T. Baehr-Jones, M. Hochberg, and A. Scherer, "Photodetection in silicon beyond the band edge with surface states," *Opt. Express*, vol. 16, no. 3, pp. 1659–1668, Feb 2008.

[190] Y. Li, S. Feng, Y. Zhang, and A. W. Poon, "Sub-bandgap linear-absorption-based photodetectors in avalanche mode in pn-diode-integrated silicon microring resonators," *Opt. Lett.*, vol. 38, no. 23, pp. 5200–5203, Dec 2013.

294

[191] S. Fathpour and B. Jalali, "Energy harvesting in silicon optical modulators," *Opt. Express*, vol. 14, no. 22, pp. 10 795–10 799, Oct 2006.

[192] Cadence design systems. [Online]. Available: https://www.cadence.com/

[193] Diode spice model parameters. [Online]. Available: http://ltwiki.org/LTspiceHelp/LTspiceHelp/D_Diode.htm

[194] J. D. Meindl and J. A. Davis, "The fundamental limit on binary switching energy for terascale integration (TSI)," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 10, pp. 1515–1516, 2000.

[195] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and compact modeling of nanometer CMOS transistors at deep-cryogenic temperatures," *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 996–1006, 2018.

[196] M. Dinu, F. Quochi, and H. Garcia, "Third-order nonlinearities in silicon at telecom wavelengths," *Applied Physics Letters*, vol. 82, no. 18, pp. 2954–2956, 2003.

[197] C. Sun, M. Wade, M. Georgas, S. Lin, L. Alloatti, B. Moss, R. Kumar, A. H. Atabaki, F. Pavanello, J. M. Shainline, J. S. Orcutt, R. J. Ram, M. Popović, and V. Stojanović, "A 45 nm CMOS-SOI monolithic photonics platform with bit-statistics-based resonant microring thermal tuning," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 4, pp. 893–907, 2016.

[198] Q. Lin, O. J. Painter, and G. P. Agrawal, "Nonlinear optical phenomena in silicon waveguides: Modeling and applications," *Opt. Express*, vol. 15, no. 25, pp. 16 604–16 644, Dec 2007.

[199] T. K. Liang and H. K. Tsang, "Efficient raman amplification in silicon-on-insulator waveguides," *Applied Physics Letters*, vol. 85, no. 16, pp. 3343–3345, 2004.

[200] D. J. Moss, L. Fu, I. Littler, and B. J. Eggleton, "Ultrafast all-optical modulation via two-photon absorption in silicon-on-insulator waveguides," *Electronics Letters*, vol. 41, no. 6, pp. 320–321, Marc 2005.

[201] H. K. Tsang, C. S. Wong, T. K. Liang, I. E. Day, S. W. Roberts, A. Harpin, J. Drake, and M. Asghari, "Optical dispersion, two-photon absorption and self-phase modulation in silicon waveguides at 1.5 μm wavelength," *Applied Physics Letters*, vol. 80, no. 3, pp. 416–418, 2002.

[202] S. F. Preble, Q. Xu, and M. Lipson, "Changing the colour of light in a silicon resonator," *Nature Photonics*, vol. 1, pp. 293–296, 2007.

[203] V. R. Almeida and M. Lipson, "Optical bistability on a silicon chip," *Opt. Lett.*, vol. 29, no. 20, pp. 2387–2389, Oct 2004.

[204] Q. Xu and M. Lipson, "Carrier-induced optical bistability in silicon ring resonators," *Opt. Lett.*, vol. 31, no. 3, pp. 341–343, Feb 2006.

[205] T. J. Johnson, M. Borselli, and O. Painter, "Self-induced optical modulation of the transmission through a high-Q silicon microdisk resonator," *Opt. Express*, vol. 14, no. 2, pp. 817–831, Jan 2006.

[206] M. Soltani, S. Yegnanarayanan, Q. Li, A. A. Eftekhar, and A. Adibi, "Self-sustained gigahertz electronic oscillations in ultrahigh-Q photonic microresonators," *Phys. Rev. A*, vol. 85, p. 053819, May 2012.

[207] G. Li, A. V. Krishnamoorthy, I. Shubin, J. Yao, Y. Luo, H. Thacker, X. Zheng, K. Raj, and J. E. Cunningham, "Ring resonator modulators in silicon for inter-chip photonic links," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 19, no. 6, pp. 95–113, Nov 2013.

[208] J. T. Robinson, K. Preston, O. Painter, and M. Lipson, "First-principle derivation of gain in high-index-contrast waveguides," *Opt. Express*, vol. 16, no. 21, pp. 16 659–16 669, Oct 2008.

[209] L. Shampine and M. Reichelt, "The MATLAB ODE suite," *SIAM J. Sci. Comput.*, vol. 18, no. 1, pp. 1–22, 1997.

[210] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. John Wiley & Sons Ltd., 2006.

[211] M. Borselli, T. J. Johnson, and O. Painter, "Accurate measurement of scattering and absorption loss in microphotonic devices," *Opt. Lett.*, vol. 32, no. 20, pp. 2954–2956, Oct 2007.

[212] D. Dimitropoulos, R. Jhaveri, R. Claps, J. C. S. Woo, and B. Jalali, "Lifetime of photogenerated carriers in silicon-on-insulator rib waveguides," *Appl. Phys. Lett.*, vol. 86, no. 7, p. 071115, 2005.

[213] T. Carmon, T. J. Kippenberg, L. Yang, H. Rokhsari, S. Spillane, and K. J. Vahala, "Feedback control of ultra-high-Q microcavities: application to micro-raman lasers and micro-parametric oscillators," *Opt. Express*, vol. 13, no. 9, pp. 3558–3566, May 2005.

[214] P. D. Desai, "Thermodynamic properties of iron and silicon," *Journal of Physical and Chemical Reference Data*, vol. 15, no. 3, pp. 967–983, 1986.

[215] R. C. Zeller and R. O. Pohl, "Thermal conductivity and specific heat of non-crystalline solids," *Phys. Rev. B*, vol. 4, pp. 2029–2041, Sep 1971.

[216] D. M. Riffe, "Temperature dependence of silicon carrier effective masses with application to femtosecond reflectivity measurements," *J. Opt. Soc. Am. B*, vol. 19, no. 5, pp. 1092–1100, May 2002.

[217] G. F. Sinclair, N. A. Tyler, D. Sahin, J. Barreto, and M. G. Thompson, "Temperature dependence of the kerr nonlinearity and two-photon absorption in a silicon waveguide at 1.55 μm," *Phys. Rev. Applied*, vol. 11, p. 044084, Apr 2019.

[218] M. Asheghi, M. N. Touzelbaev, K. E. Goodson, Y. K. Leung, and S. S. Wong, "Temperature-Dependent Thermal Conductivity of Single-Crystal Silicon Layers in SOI Substrates," *Journal of Heat Transfer*, vol. 120, no. 1, pp. 30–36, 02 1998.

[219] D. Gray and R. Hamerly, "Thermo-Optic Multi-Stability and Relaxation in Silicon Microring Resonators with Lateral Diodes," *arXiv e-prints*, p. arXiv:2003.09978, 2020.

[220] *Thermal Conductivity of Ultra Thin Single Crystal Silicon Layers: Part I — Experimental Measurements at Room and Cryogenic Temperatures*, ser. ASME International Mechanical Engineering Congress and Exposition, vol. Heat Transfer, Volume 2, 11 2004.

[221] J. Chen, D. Tzou, and J. Beraun, "A semiclassical two-temperature model for ultrafast laser heating," *International Journal of Heat and Mass Transfer*, vol. 49, no. 1, pp. 307 – 316, 2006.

[222] K. Zhukovsky, "Operational approach and solutions of hyperbolic heat conduction equations," *Axioms*, vol. 5, no. 4, 2016.

[223] T. J. Bright and Z. M. Zhang, "Common misperceptions of the hyperbolic heat equation," *Journal of Thermophysics and Heat Transfer*, vol. 23, no. 3, pp. 601–607, 2009.

[224] B. E. Little, S. T. Chu, H. A. Haus, J. Foresi, and J. P. Laine, "Microring resonator channel dropping filters," *Journal of Lightwave Technology*, vol. 15, no. 6, pp. 998–1005, June 1997.

[225] P. E. Barclay, K. Srinivasan, and O. Painter, "Nonlinear response of silicon photonic crystal microresonators excited via an integrated waveguide and fiber taper," *Opt. Express*, vol. 13, no. 3, pp. 801–820, February 2005.

[226] T. Carmon, L. Yang, and K. J. Vahala, "Dynamical thermal behavior and thermal self-stability of microcavities," *Opt. Express*, vol. 12, no. 20, pp. 4742–4750, October 2004.