Fabrication and Electrical Characterization of BESOI

by

Mousumi Bhat

B.Tech., Indian Institute of Technology(1988)
M.S., University of Maryland, College Park(1990)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Master of Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

September 1991

© Massachusetts Institute of Technology 1991. All rights reserved.

Author ....
Department of Electrical Engineering and Computer Science
September 5th, 1991

Certified by ....
Martin A. Schmidt
Assistant Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Accepted by ....
C.L.Searle
Chairman, Departmental Committee on Graduate Students

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

NOV 04 1991

LIBRARIES ARCHIVES

Fabrication and Electrical Characterization of BESOI

by

Mousumi Bhat

Submitted to the Department of Electrical Engineering and Computer Science
on September 5th, 1991, in partial fulfillment of the
requirements for the degree of
Master of Science

Abstract

The developement of a method for preparation of Silicon-On-Insulator by the Bond and Etch-back technique is reported in this thesis. Targets set for the project were good oxide quality and superior quality of device layer silicon.

Experiments were performed on SiGe, SiGeB and boron-doped layers as etch-stops and $KOH : H_2O$ and $NH_4OH : H_2O$ as etchants, to decide on the optimum combination of etch-stop and etchant. Etching conditions were varied to obtain the set of parameters which gave the best wafer surface and good stopping on the etch-stop.

Assessment of the quality of the BESOI substrate was done through electrical measurements and defect analysis. Leakage current measurements and breakdown measurem ents were performed to evaluate the oxide quality. Leakage currents of the order of picoamperes were obtained. The oxide did not degrade at voltages as high as 350V. IR inspection of the bonded interface showed good bonding. Thickness uniformity measurements across the wafer showed a thickness variation of $\pm 300\text{Å}$. Defect-etch studies and optical microscopy indicated good device layer quality.

Thesis Supervisor: Martin A. Schmidt
Title: Assistant Professor of Electrical Engineering and Computer Science

Acknowledgments

First of all I would like to thank my advisor Professor Martin Schmidt for all the help, guidance and constant encouragement he provided during the course of this research. In addition to his support, the independence he gave me in doing my research, helped me build confidence in my convictions. For this, I shall be ever grateful to him. His help in the timely editing of the thesis will not be forgotten.

I would also like to thank Professor R. Reif, Professor D.A. Antoniadis and Professor J. Chung for their helpful suggestions and guidance.

My team-mates Vince, Javad, Mike, Mark and Chris have contributed in a big way by providing me with various perspectives of graduate life at MIT. Conversations with them was always an eyeopener.

This work was fully funded by the Semiconductor Research Corporation, contract# 90-SP-080. Special thanks go to members of SRC for their participation in the project, to Pat for being an excellent secretary and to Octavio Hurtado, Tim Tyson and Rob Cuikay for their help and patience during processing.

Finally, I would like to express my gratitude to my husband, Naveen, who was with me through thick and thin and without whose constant love and support the completion of this thesis would have been difficult.

Contents

1 SILICON ON INSULATOR TECHNOLOGY 9
1.1 SOI Performance Advantages 10
1.2 SOI Technologies 11
1.3 Objective and Layout of Thesis 12

2 BESOI: SALIENT FEATURES 14
2.1 SOI by Wafer Bonding 14
2.1.1 Wafer Preparation 14
2.1.2 Wafer Bonding 16
2.1.3 Wafer Thinning 16
2.2 Significance of Etch-Back Process 17
2.3 Conventional Etch-Back Process 19
2.4 Etch-Stops and Etchants Used in Thesis 20
2.4.1 Etch-Stops 20
2.4.2 Etchants 22
2.5 Requirements for an Optimized Process 23

3 EXPERIMENTAL PROCEDURE 24
3.1 Etch-Stop Characterization 24
3.1.1 Procedure 26
3.1.2 Sample Description 27
3.2 Etchant Characterization 29
3.3 Material Characterization 31

3.4 Electrical Characterization 33
3.4.1 Fabrication Summary 33
3.4.2 Leakage Current Measurements 33
3.4.3 Breakdown Measurements 35
3.4.4 Capacitance-Voltage Measurements 35

4 FABRICATION RESULTS **36**
4.1 Etch-Stop Results 36
4.2 Etchant Results 39

5 BESOI: SUBSTRATE PROPERTIES **42**
5.1 Material Characteristics 42
5.1.1 SEM Inspection Results 42
5.1.2 Defect Etch Results 44
5.1.3 Uniformity of Wafer Thickness 44
5.2 Electrical Characterization 46
5.2.1 Interface Quality 46
5.2.2 Leakage Current Measurement Results 47
5.2.3 Breakdown Voltage Measurement Results 47
5.2.4 Capacitance-Voltage Measurement Results 47

6 CONCLUSIONS **51**

A Etch rates of Si and SiO_2 in KOH **53**

B REFLUX CONDENSER **55**
B.1 Part List 56

C PROCEDURE: Preparation of BESOI Substrate **62**

D Steps for Fabrication of Capacitors on BESOI **64**

List of Figures

1-1 An SOI CMOS circuit 9

2-1 Fabrication sequence for preparation of BESOI 15

2-2 Control of film uniformity by etch-back technique 18

3-1 Experimental sequence 25

3-2 Expected plot 26

3-3 Test samples 28

3-4 Schematic of Reflux Condenser 32

3-5 Fabrication of capacitors: starting material and final structure 34

4-1 Calibration etch 37

4-2 Comparison of etch-selectivities of Si_xGe_{1-x} and $Si_xGe_yB_{1-x-y}$ etch-stop layers 38

4-3 Comparison of etch-selectivity of AHW and KOH as etchants 40

5-1 SEM picture of BESOI wafer surface 43

5-2 SEM picture of magnified defect 43

5-3 Etch pits on BESOI wafer surface (linear magnification: 400) 44

5-4 Defect-etched surface of BESOI wafer surface (linear magnification: 400) 45

5-5 Defect-etched surface of prime wafer surface (linear magnification: 200) 45

5-6 Measure of thickness uniformity across the wafer 46

5-7 IR picture of bonded interface before and after anneal 47

5-8 Distribution of leakage current 48

5-9 Capacitor structure and connections for C-V measurements 49

5-10 High-frequency plot of capacitance against voltage 50

B-1 Schematic of reflux condenser setup 57
B-2 Detailed diagram of reflux condenser 58
B-3 Top view of bottom plate of teflon jig 59
B-4 Top view of top plate of teflon jig 60
B-5 Cross section of teflon jig 61

List of Tables

4.1 Summary of etch-selectivities of different etch-stop materials: Etch at 30^oC in 20% $KOH : H_2O$ 37

4.2 Effect of germanium concentration on etch-selectivity: Etch at 45^oC in 3.7% $NH_4OH : H_2O$ 39

A.1 < 100 > silicon etch rate in μm/hr 54

A.2 < 100 > silicon-dioxide etch rate in nm/hr 54

D.1 Silicon Plasma Etch (Recipe #10) 65

Chapter 1

SILICON ON INSULATOR TECHNOLOGY

There has been a growing interest in Silicon On Insulator (**SOI**) substrates over the past few years. The advantages of SOI devices over bulk devices have impact in markets such as military, high temperature and power electronics. The factors that make SOI subtrate attractive have been pointed out by several groups who are actively involved in SOI research [1, 2, 3]. The advantages of SOI material can be seen by comparing a bulk CMOS circuit against an SOI CMOS circuit: fig.(1-1). The following section highlights some of the obvious advantages of SOI over bulk CMOS.

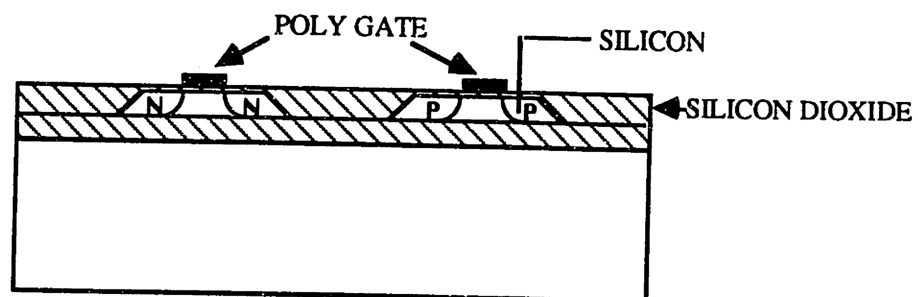


Figure 1-1: An SOI CMOS circuit

1.1 SOI Performance Advantages

There are many advantages of CMOS SOI circuitry over bulk CMOS circuits. As indicated in fig.(1-1):

1. Complete dielectric isolation: SOI technology allows for complete isolation of closely spaced components. This feature helps one to get around problems like latch-up in CMOS which limit the scaling of geometry. With the reduction in device size and separation, isolation between devices becomes difficult. For submicron structures, conventional bulk isolation no longer works. In the SOI structures, one can etch away the silicon between devices and fill it up with silicon dioxide. This kind of isolation technique allows the spacing between devices to be the minimum feature size. The overall effect of this is increased packing density.

2. Low capacitance: In thin film SOI structures, the source and drain regions extend all the way to the buried SiO_2 layer. Thus there is no junction at the bottom of the source/drain implants. In addition, the side walls can extend to an SiO_2 layer. All these features lead to a reduction in the junction area, hence the junction capacitance. The RC time constant is reduced providing for high operating speeds and low dynamic power consumption.

3. Radiation hardness: SOI devices first found their place in military applications due to the property of radiation hardness. Incident radiations such as protons, alpha particles, gamma rays and x-rays generate electron-hole pairs in the material. These charges collect at nodes in the circuit giving rise to "soft errors". In SOI structures, the dielectric layer protects the electrons and holes from collecting in the active devices.

4. Fully depleted MOSFETs: SOI technology allows for the fabrication of very thin film substrates thus creating a potential for the fabrication of fully depleted MOSFETs. Fully depleted MOSFETs exhibit many attractive properties such

as low electric fields, high transconductance, excellent short-channel behavior and a quasi-ideal subthreshold slope.

5. New technologies: SOI technology opens up the field for the fabrication of a whole new array of novel structures like power devices, transducers, and 3-D circuits.

1.2 SOI Technologies

Many technologies have been developed for producing a film of single-crystal silicon on top of an insulator (usually Silicon Dioxide). The four major techniques used for fabricating SOI substrates are: Zone Melting Recrystallization (ZMR), Full Isolation by Porous Oxidation (FIPOS), Separation by Implantation of Oxygen (SIMOX) and Direct Wafer Bonding (DWB) [1, 2, 3].

SOI generated by the ZMR technique involves scanning a focused laser beam/e-beam/graphite-strip-heater across the surface of a polysilicon layer deposited on an oxide surface. The polysilicon melts and recrystallizes as large grains of crystalline silicon. The limitation of the ZMR techniques lies in the fact that rapid cooling of the melted zone causes defects to be generated near the seed.

A technique for forming SOI using porous oxidized silicon has been developed and is called FIPOS. Phosphorus islands are first implanted in the p-type silicon wafer. An anodic reaction in HF is then used to transform the 'p' region surrounding the phosphorus implants to porous silicon. The porous silicon is then selectively oxidized. The final structure is obtained after annealing for oxide densification. FIPOS stands as inexpensive material which offers variable thickness of the insulator and good crystalline quality. Fabrication and material quality issues have limited the use of this material.

SIMOX is prepared by implanting high oxygen doses into a silicon wafer. Most of the residual defects in the device layer can be removed during a post-implant high temperature anneal. SIMOX material is a good candidate for VLSI and rad-hard applications because of its reproducibility. However, cost of fabrication is high due

to the need for a high current implanter.

An SOI wafer prepared by the DWB technique is produced by bonding together two wafers, a handle wafer and a device wafer, and then thinning the device wafer back to the required thickness. The process begins when a thermal oxide is grown on the handle wafer and/or the device wafer. After a surface hydration step, these ultraflat surfaces are brought in contact. The Van-der-waal forces hold the two smooth surfaces in contact. These wafers are then annealed at high temperature at which time the bonding of the two wafers occurs. The device wafer is then thinned back to produce the SOI material by the DWB technique.

The Bond and Etch-Back technique for making **SOI** material (BESOI) uses the DWB technique followed by a chemically selective etch to thin the device wafer. The device wafer is thinned by etching away the excess silicon with an anisotropic etchant. The etching stops at an etch-stop layer. The etch-stop layer is then removed with another selective etchant producing the SOI structure.

BESOI technique has advantages over other techniques for forming SOI since it produces a bulk quality single-crystal-silicon device layer and a thermal oxide quality insulator. The device layer does not have to undergo implantation damages as in the case of SIMOX and the insulator sandwiched between the silicon layers is thermally grown SiO_2 rather than SiO_x as in the case of SIMOX. The excellent quality of the device layer and the insulator obtained by the BESOI technique makes this technology potentially superior to the others. Hence, optimization of the BESOI process steps and evaluation of the substrate quality has been chosen as the goal of this thesis. The next chapter presents a detailed discussion of BESOI.

1.3 Objective and Layout of Thesis

The aim of this thesis is to illustrate the importance of the Bond and Etch Back technique for the fabrication of SOI substrate with particular focus on the formation of thin layers ($< 1\mu m$). The thesis presents methods of characterizing etch-stop materials and etchants that are used during the fabrication sequence. Finally, material

and electrical evaluation of the substrate is done to assess the quality of the material.

The body of the thesis is divided into five principal chapters.

- Chapter II is a review of SOI prepared by the Bond and Etch Back technique. This chapter discusses the significance of the bond and etch back method and throws light on the salient features of fabrication.
- Chapter III is an illustration of the experiments done for characterization of the etch-stop material and the etchant. It also includes the methods used for evaluation of the substrate quality.
- Chapter IV has experimental results and discussions of the observations made. It sets the milestones for the standardized procedure for fabrication of the BE-SOI substrate.
- Chapter V presents the electrical and material properties of the samples prepared at MIT.
- Finally, the main conclusions and suggestions for future work are summarized in Chapter VI.

Chapter 2

BESOI: SALIENT FEATURES

This chapter has two important objectives. The first is to present some of the conventional techniques used for the fabrication of BESOI. Each of the process steps involved in the fabrication are described and a summary of the popularly used process flow is presented. The second section of the chapter points out the advantages and disadvantages of individual processes or materials. Reasons that make BESOI a more attractive fabrication technique as compared to other popularly used techniques are also illustrated.

2.1 SOI by Wafer Bonding

SOI wafers are created in three basic steps: (i) preparation of the handle wafer and the device wafer, (ii) contacting the polished faces of the two wafers and bonding them, (iii) thinning the seed wafer back to the desired thickness fig(2-1).

2.1.1 Wafer Preparation

Two wafers, the handle wafer and the device wafer, are needed to produce a BESOI substrate. The handle wafer is usually n/p-type prime grade silicon. A layer of thermal SiO_2 is grown on the handle wafer, where this layer will form the insulator in the SOI structure.

Preparation of the device wafer is more complicated. Depending on the thin-

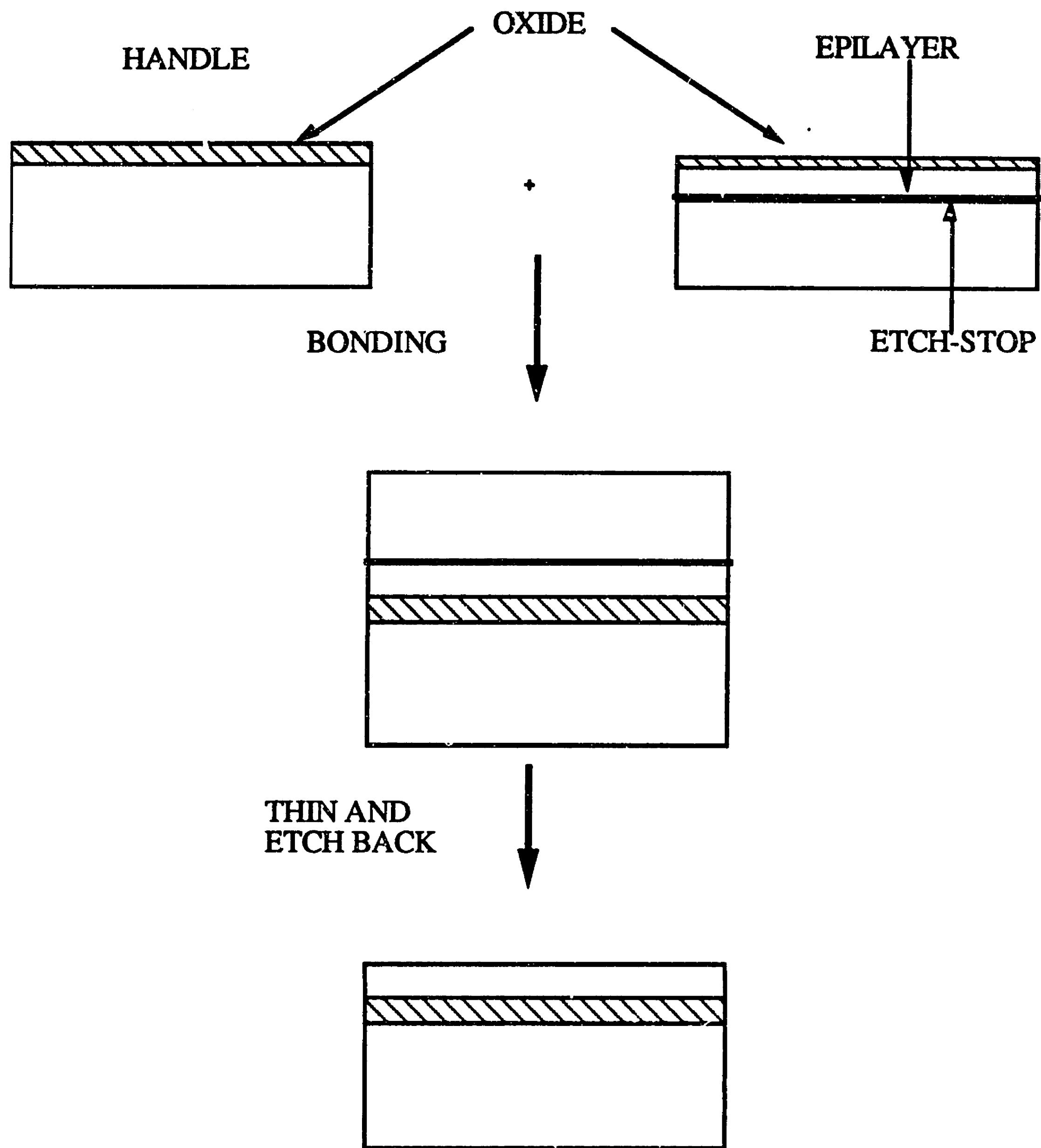
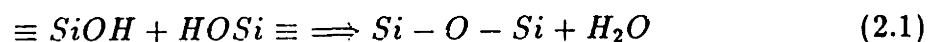


Figure 2-1: Fabrication sequence for preparation of BESOI

ning mechanism used, the device wafer goes through different kinds of preparation steps. Wafer-thinning may be done mechanically or chemically. Mechanical thinning involves the formation of a polish-stop in the device wafer [4]. The polish-stop is usually an imbeded grid of slow polishing material. In the case of chemical etch-back, an etch-stop layer has to be incorporated in the device wafer by epitaxy, implantation or diffusion. An epi-layer is then grown on top of the etch-stop layer. This is the layer which eventually forms the device layer.

2.1.2 Wafer Bonding

Two mirror polished wafers are hydrated to form hydrophillic surfaces, brought together at room temperature, and then annealed at high temperature when the oxide flows and forms a permanent bond. The handle wafer usually has a layer of thermally grown silicon dioxide which electrically isolates the handle wafer and the device wafer. When the ultraflat surfaces are brought in contact at room temperature, Van der Waals forces caused by the mutual interaction of all the induced dipoles on both wafers results in an attractive force that keeps the wafers in contact. The bond strength increases monotonically with temperature. The proposed reaction that occurs at the interface is as follows:



$$\equiv SiOH + HOSi \equiv \Longrightarrow Si - O - Si + H_2O \tag{2.1}$$

The viscous flow of oxide at higher temperatures leads to complete bonding [4, 7, 8])

2.1.3 Wafer Thinning

In the mechanical polishing technique, the bonded wafer pair is supported on a polishing machine, the exposed surface of the handle wafer is used as a reference and the device wafer is mechanically lapped. Since lapping causes sub-surface damage, the subsurface layer is removed by a chemomechanical polishing techniques. This is done by tribochemical polishing [7]. However, it is hard to obtain submicron thick layers with uniform thickness, since the reference surface (handle wafer) may itself

be non-uniform in thickness, causing the non-uniformity to propagate. In practice, manufacturers have been able to achieve $\pm 0.3\mu m$ thickness control by using a handle wafer with comparable total thickness variations.

Chemical etching helps to solve the problem of non-uniformity. The wafer is mechanically polished till very close to the etch-stop layer and then it is chemically etched in a solution which has a high etch-selectivity to the etch-stop material. The etching process can be summarized by the following reaction

$$Si + 2OH^- + 2H_2O \Longrightarrow SiO_2(OH)_2^{--} + 2H_2 \tag{2.2}$$

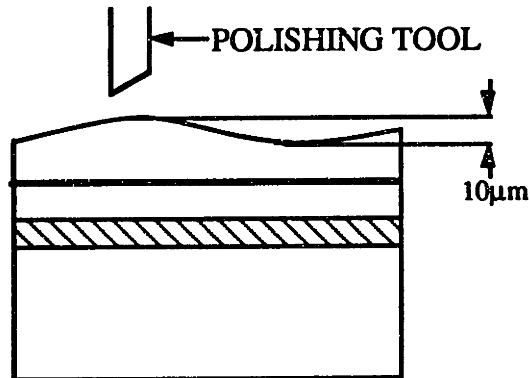
2.2 Significance of Etch-Back Process

Most of the methods used for producing SOI substrates have several drawbacks. The first category includes laser recrystallization and selective epitaxy. The quality of the silicon layer is inferior to that normally associated with bulk silicon processing. The second category is comprised of methods which form an oxide layer beneath an existing high quality silicon layer. Examples are FIPOS and SIMOX. These methods result in inferior quality of oxide and also degradation of the silicon top layer during oxide formation.

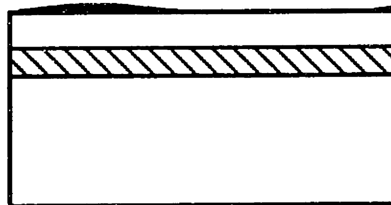
SOI formed by wafer bonding helps get around the drawbacks of the above methods. The oxide in the case of wafer bonded SOI is thermally grown and hence of better quality than implanted SiO_x. The device layer is epitaxially grown on bulk silicon and hence not degraded from its original quality. Another attractive feature of SOI prepared by the bond and etch-back technique is the fact that it allows for the fabrication of ultrathin device layers with excellent uniformity of thickness across the wafer.

The reason for the excellent controllability of film thickness and uniformity is demonstrated in fig(2-2). We start with a wafer that has a certain amount of non-uniformity and chemically etch it back. If, for example, the non-uniformity is $10\mu m$, and the selectivity of the etch-stop layer is 100:1, then over time as etching proceeds,

MECHANICALLY POLISHED WAFER



AFTER ETCHING IN ETCH SOLUTION



SELECTIVITY = 100:1

NON-UNIFORMITY = 0.1 µm

Figure 2-2: Control of film uniformity by etch-back technique

the non-uniformity gets reduced to 10/100= 0.1μm. If we now use another selective etchant of selectivity 10:1 to remove the etch-stop layer, then the non-uniformity can furthur be reduced to (.1/10)μm. Hence as is obvious from the above discussion, the higher the selectivity of the etch-stop, the higher is the degree of uniformity obtainable.

2.3 Conventional Etch-Back Process

The standard procedure used for the etch-back process is as follows.

- Thermal oxide is grown on the handle wafer.
- An etch-stop layer, usually a heavily doped boron layer with concentration higher than $10^{20} cm^{-3}$, is diffused, implanted, or epitaxially grown onto the device wafer, followed by the epitaxial growth of a lightly-doped layer.
- A thin oxide may or may not be grown on the device wafer.
- The wafers are brought together on their polished surfaces and bonded at $1000^o C$.
- The silicon on the device wafer end is mechanically polished to within a few microns of the etch-stop layer.
- The remaining silicon is removed with an anisotropic etchant like aqueous KOH, CsOH, Ethylene Diamine Pyrochatecol(EDP) or Hydrazine.
- The etch-stop layer is then removed using an 8:3:1 solution of acetic acid, nitric acid and hydrofluric acid giving us the final structure [5].
- Surface staining caused by the formation of SiO_x is removed in $HF - KMnO_4$ solution [7].

2.4 Etch-Stops and Etchants Used in Thesis

In this section the advantages and disadvantages of the etch-stop material and etchants investigated as a part of the thesis are discussed.

2.4.1 Etch-Stops

The etch-stop materials that we have investigated are (i) heavily boron-doped layers (concentrations $> 10^{20} cm^{-3}$), (ii) Strained Silicon-Germanium (Si_xGe_{1-x}) layers, (iii) Silicon-Germanium layers doped with boron ($Si_xGe_yB_{1-x-y}$).

Boron-Doped Layers:

Heavily boron-doped layers with concentrations higher than $10^{20} cm^{-3}$ form excellent etch-stops. Researchers have noted etch-selectivities of p^+ layer to silicon in excess of 100:1. These high doses of boron can be incorporated by implantation or by solid source diffusion of boron using BN or B_2O_3 dopant wafers at 1100° C. The solid solubility of boron in silicon being higher at elevated temperatures yields a surface concentration as high as $2 \times 10^{20} cm^{-3}$ [9]. Finally it is possible to grow the etch-stop layer epitaxially and successfully obtain concentrations in excess of $10^{20} cm^{-3}$ [6].

However, there are several problems associated with using such high boron concentrations. The first disadvantage arises from the tensile stresses in silicon introduced by the high concentration of boron. At boron concentrations higher than $8 \times 10^{19} cm^{-3}$, misfit dislocations start to form due to the stress, which is believed to be caused by the differing atomic radii of boron in comparison to silicon. Since the device layer is grown epitaxially on the p^+ layer, the epi-layer will have dislocations which are imprints of the heavily doped layer. A related problem arises when a secondary etchant is used to remove the etch-stop layer. The defects in the epi-layer get decorated and etch-pits begin to form on the surface of the epi-layer. Another major handicap of using heavily doped boron layer is the problem of out-diffusion of boron during high temperature processes like bonding and growth of the epi-layer. Out-diffusion of boron not only lowers the peak concentration and hence reducing etch-selectivity,

it also dopes the epi-layer. Furthermore, if the boron is implanted into the sample to create the etch-stop layer, then the device layer will have residual defects due to ion bombardment.

Silicon-Germanium Layers:

Silicon-germanium is found to form a good etch-stop [11, 12, 13]. The etch-stop layer consists of a strained $Si_{0.7}Ge_{0.3}$ layer. Using a selective etchant that attacks the silicon over the Si_xGe_{1-x} layer selectively, Godbey et.al. [12] have managed to produce BE-SOI films with silicon film thickness between 0.2 - 0.3 μm. Silicon-germanium layers were found to present etch-selectivity of 17:1. Thermal studies indicated that high temperature altered the selectivity only slightly. Advantages of silicon-germanium layers over boron doped layers are: silicon-germanium layers produce defect free device layers, thermal cycles do not alter etch rates [12] and problems of out-diffusion do not exist. However, silicon-germanium does not form as excellent an etch-stop as boron does. It has been observed that higher germanium concentrations form better etch-stops, however, incorporating doses as high as 30% germanium involves complicated processing.

Silicon-Germanium-Boron Layers:

Hunt et.al. [14] have shown that using boron doped silicon-germanium layers helps to form good etch-stops with reduced defect density in the epi-layer. Since boron induces tensile strains in silicon and germanium introduces compressive strains, presence of both species in the etch-stop layer compensates the strain. A Ge:B ratio of 3.5:1 was found to form stress compensated layers. Hence, it was possible to have stress compensated layers with high boron concentration and low germanium concentration (3%). These features make the Si-Ge-B layer particularly attractive because the high etch-selectivity due to high boron is retained and the germanium required is only 3%. However, the problem of boron out-diffusion at high temperatures still remains and the step taken by us to reduce this problem are discussed in the next chapter.

2.4.2 Etchants

The two etchants investigated in this thesis are aqueous potassium hydroxide and aqueous ammonium hydroxide (AHW) Listed here are their respective advantages and disadvantages. While a number of different etchants have been investigated for BESOI, we chose $KOH : H_2O$ and $NH_4OH : H_2O$ solutions because of their ease of handling and minimal safety risk.

Aqueous Potassium Hydroxide:

Potassium hydroxide has been extensively used as silicon etchant for micromachining [18, 19, 20, 21, 22, 23]. Advantages of aqueous potassium hydroxide as an etchant are: ease of handling, simple and established process, and it produces smooth etching surfaces. However, aqueous potassium hydroxide is not IC compatible because of the concern of alkali ion contamination. Potassium hydroxide also has a significant silicon dioxide etch rate, posing a problem when SiO_2 is used as an etching mask. Finally, as results presented in chapter 4 will also indicate, potassium hydroxide does not present as high selectivities with p^+ etch-stops as compared to certain other etchants.

Aqueous Ammonium Hydroxide:

Ammonium hydroxide not only yields excellent selectivity with p^+ layers [15], it also has the advantage of being IC compatible. Literature reflects that the etch rate of SiO_2 with ammonium hydroxide is very low. Etch rate ratio of SiO_2 to Si of 1:8400 has been reported by Benecke et. al. [15]. Despite all these attractive features of AHW, handling of AHW can be difficult. It is volatile and ammonia evaporates leaving the solution degraded and necessitating the need for a reflux condenser. AHW also has the problem of producing very rough etched surfaces [15, 16, 17]. Ways to get around these problems will be discussed in the following chapters.

2.5 Requirements for an Optimized Process

The above discussion can be summarized for the optimum etch-back process that would produce the best quality material.

- Etch-Stop Material:
  - The etch-stop material should be one that has very high etch-selectivity.
  - It should be easy to incorporate in the device wafer.
  - It should be one that produces defect free etch-stop layers and hence defect free epi-layers.
  - The material should not undergo thermal changes which will worsen its etch-selectivity ratios.
  - The etch-stop layer should not affect the epi-layer during subsequent processing steps.
- Device Layer:
  - The device layer essentially needs to be free of defects. Processing steps should be such that it is possible to control the defect count and contamination from etch-stop layer through the process steps.
  - It should be possible to produce very thin device layers with a high degree of thickness uniformity across the wafer.
- Etchants:
  - The combination of the etchant and the etch-stop material should produce excellent etch-selectivity.
  - Etchants should not cause chemical contamination of the substrate.
  - Etchant should be easy to handle.

Chapter 3

EXPERIMENTAL PROCEDURE

This thesis aims at investigating two major issues regarding SOI prepared by the bond and etch-back technique. The first issue involves characterization of the etch-stop and the etch-back step. The idea is to find the optimum combination of etch-stop materials, etchant and etching conditions. The second criterion is to evaluate the quality of BESOI prepared from the above conditions. Methods used to perform the material and electrical assessment are presented in this chapter. All detailed information about the apparatus and sample preparation are contained in the Appendices of this thesis.

3.1 Etch-Stop Characterization

The most important criterion for evaluation of the etch-stop material is to determine its etch-selectivity. To measure the etch-selectivity of the etch-stop material, we have performed experiments by which it is possible to determine the etch rates of the individual layers. The starting material for the experiment is a sample which has the etch-stop layer (Boron, Si_xGe_{1-x} or $Si_xGe_yB_{1-x-y}$), and an epi-layer of low doped silicon on top of the etch-stop layer fig(3-1a).

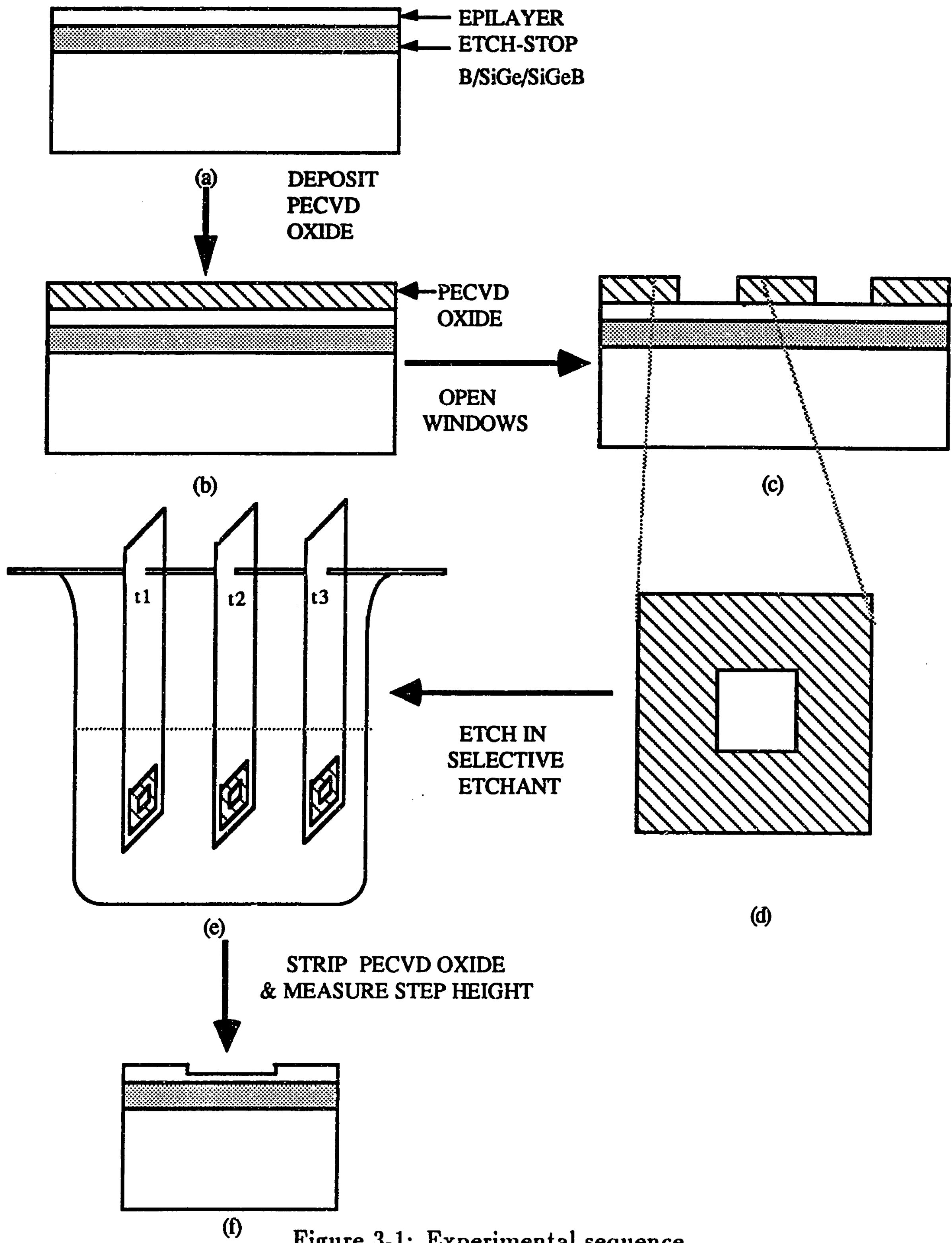


Figure 3-1: Experimental sequence

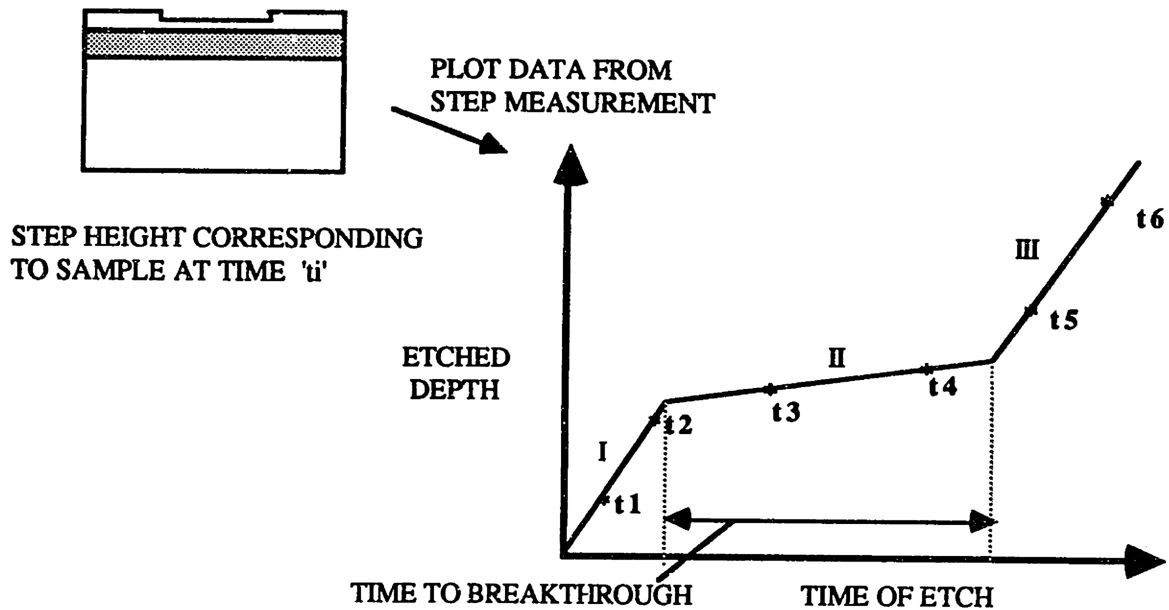


Figure 3-2: Expected plot

3.1.1 Procedure

A layer of PECVD oxide ($\sim 2.5\mu m$) which acts as an etch mask is deposited on the top of the sample as shown in fig(3-1b). PECVD oxide is used instead of thermal oxide because PECVD oxide can be deposited at 300° C as opposed to thermal oxide which has to be grown at elevated temperatures. It is important to avoid the thermal cycle so that one can preserve the peak of the etch-stop layer. The PECVD oxide mask is then patterned to open square windows (2mm $\times$ 2mm), exposing small areas of silicon fig(3-1c). The wafer is broken into small pieces such that each piece has an exposed area in the center surrounded by the oxide along all four sides fig(3-1d).

These pieces are then mounted on teflon strips that are suspended into the etching solution ($KOH : H_2O$ or AHW) after a brief 7:1 HF dip. The time of etching of each sample piece is monitored and each piece is pulled out after different time intervals fig(3-1e). The oxide layer is then stripped with 7:1 BOE. The etched depth from the unetched silicon surface to the etched silicon surface is then measured using a commercial surface profilometer fig(3-1f). The measured etch-depth is then plotted against time. The expected graph is shown in fig(3-2).

The plot can be explained as follows. Since the etchant sees the lightly doped

epitaxial layer first, it etches through this epi-layer relatively fast. When it hits the etch-stop layer, etching slows down drastically because the etch-rate of the etch-stop layer is expected to be greatly reduced. Finally, after the etchant has completely etched through the etch-stop layer, the etch rate should go up again since it starts etching the bulk silicon. The two important quantities here are the "*time to break-through*" and "*selectivity*". The "*time to breakthrough*" is the time required for the etchant to etch through the etch-stop layer. It can also be defined as the $\frac{Layer\ thickness}{etch\ rate}$. "*Selectivity*" is measured as the ratio of the slope of the silicon-etch-region (region III) to the slope of the etch-stop-etch-region (region II) fig(3-2). The bigger this number, the higher is the etch-selectivity of the etch-stop.

3.1.2 Sample Description

Two issues were studied as part of this experimentation. (i) Comparison of etch-selectivities of the three etch-stop materials and (ii) effect of increasing germanium concentration in the stop layer. The samples used for experiment (i) were as follows:

Sample 1: Etch-stop layer was a heavily doped layer of boron concentration $\sim 10^{20} cm^{-3}$ grown epitaxially. Thickness of the etch-stop layer was $1.5 \mu m$. Thickness of the p^- epi-layer was 0.6 μm. These samples were obtained from a commercial source [6], fig(3-3a).

Sample 2: Etch-stop layer was a silicon-germanium layer with Ge=3% to 12% grown by low temperature (625^oC) epitaxy. Thickness of the etch-stop layer was $500 \AA$. Thickness of the epi-layer was 0.4 μm. Grown by Prof. R. Reif's group at MIT, fig(3-3b).

Sample 3: Etch-stop layer was a silicon-germanium-boron layer with Ge=3% to 12%, $N_A = 2 \times 10^{19}$ to $2 \times 10^{20} cm^{-3}$ grown by low temperature (625^oC) epitaxy. Thickness of the etch-stop layer was $500 \AA$. Thickness of the epi-layer was 0.4 μm. Grown by

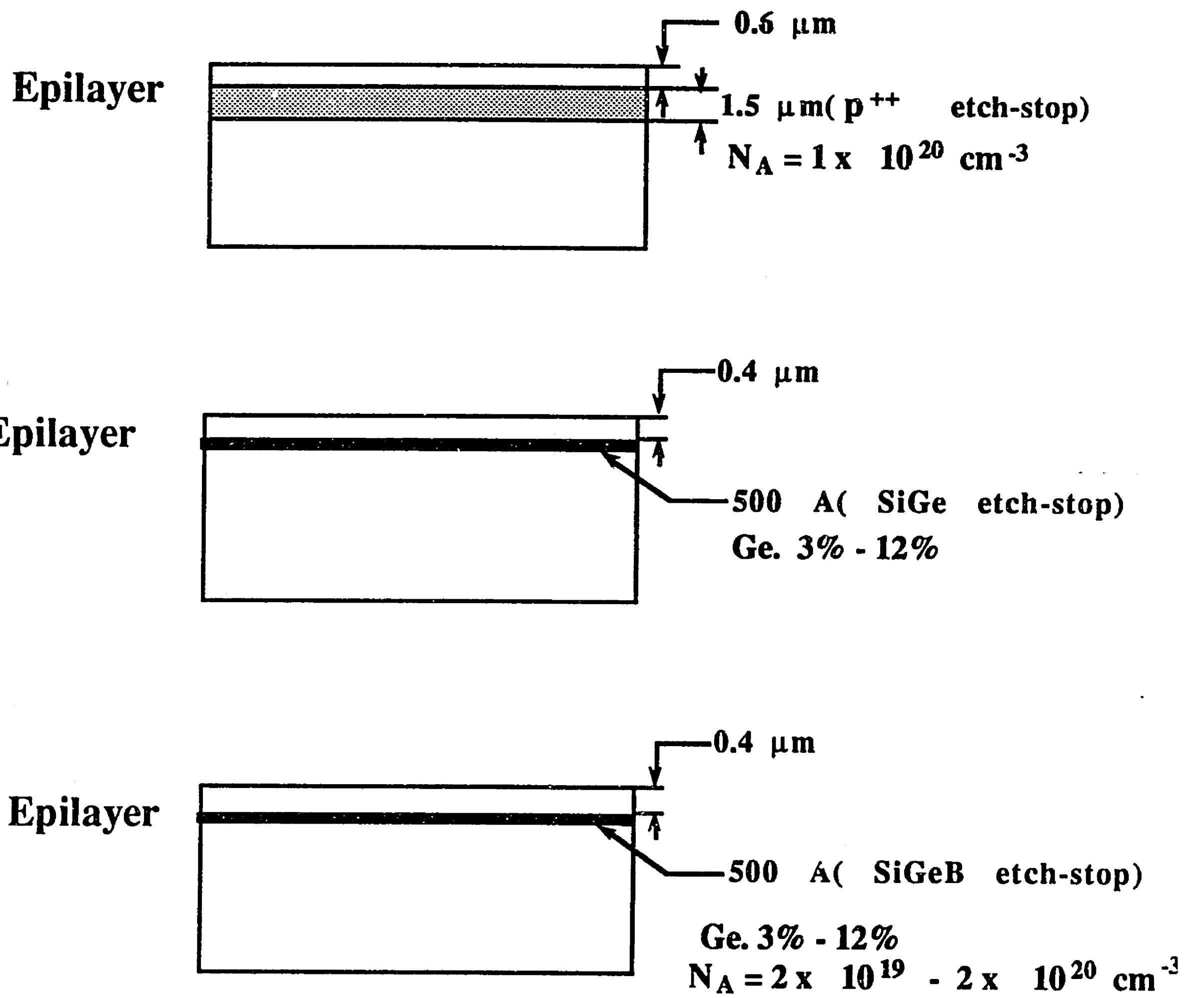


Figure 3-3: Test samples

Prof. R. Reif's group at MIT, fig(3-3c).

Etchant used was 20% aqueous Potassium hydroxide at 30°C.

The samples for the second experiment had silicon-germanium-boron etch-stop material. Thickness of the etch-stop layer was $500\AA$. Thickness of the epi-layer was $0.4\mu m$. Boron concentration on the three samples was fixed at $2 \times 10^{19} cm^{-3}$ and the germanium concentration was varied from 3% - 10%. The etchant used in this case was 3.7 % ammonium hydroxide at $45°C$.

The steps taken to limit the effect of the thermal cycles were: (i) low temperature epitaxy was used instead of regular epitaxy for growth of the etch-stop layer and the epilayer and (ii) these samples were successfully bonded at a lower bonding temperature of $800°C$ for 30 minutes. These growth and bonding conditions were estimated to significantly reduce the **Dt** involved in the out-diffusion of boron.

3.2 Etchant Characterization

Several issues had to be investigated while characterizing the etchant. Most of the results obtained were qualitative. The first issue was to determine which etchant had better selectivity properties.

Experiment 1: The sample with boron doped etch-stop layers were used in this experiment. They were broken into small pieces and prepared as outlined in the previous section. The experiment was performed on two sets of these samples. One set was etched in 20% $KOH : H_2O$ at $30°C$ and the other set was etched in 3.7% AHW at $45°C$. The etched depths were determined by using a commercial surface profilometer. The plots of the two etch experiments were superimposed and their selectivities compared.

Experiment 2: This experiment was aimed at studying the effect of stirring the solu-

tion during the etching process. As has been pointed out earlier, ammonium hydroxide etching was found to produce very rough etch surfaces. This has been described by Schnakenberg et.al. [16] as formation of pyramidal shaped hillocks. The formation of these pyramidal structures greatly reduce the etch rate of prime silicon. Prime grade silicon with thermal oxide protecting the back surface were etched in 3.7% AHW for half hour at 45°C with and without stirring. The wafers were placed vertically upright along the walls of the flask while a magnetic stirrer stirred the solution in the middle.

Experiment 3: Effects of changing temperature, time of etch and concentration of solution were studied.

- Keeping the temperature fixed at 45°C, the concentrations were varied from 8% to 12%. Published data on etch-rate of silicon in ammonium hydroxide indicates a peak etch-rate at AHW concentration of 10%, hence the range of AHW concentrations was chosen as above. Concentrations of 8%, 10% and 12% were used to etch prime silicon wafers at 45°C for 30 minutes.

- Keeping the concentration fixed at 8% and the temperature of etch at 45°C, the time of etch was varied. The etch was done on two samples for 30 minutes and for 1 hour.

- Keeping the concentration fixed at 8%, the temperature was varied. Samples were etched for 30 minutes at 45°C and 60°C.

- Effects of stirring the solution were also studied. Two samples, one with the etchant stirred during etching and the other without the etchant stirred, were etched for 30 minutes at 45°C in 3.7% AHW. Effects of temperature variation on the setup with stirred etchant was also studied.

Experiment 4: The effects of creating a positive overpressure of nitrogen were studied. The positive overpressure was expected to prevent the ammonia from vaporizing into the ambient above the solution. Two experiments, one with high nitrogen flow-rate

and the other with low flow-rate through the etching apparatus were conducted. The experiment was performed to ascertain the optimum nitrogen flow rate that would be required to create a positive overpressure and yet not be so strong as to aid evaporation of ammonia from solution.

The best conditions resulted when the etch was done in a reflux condenser with etchant stirred. The reflux condenser was placed in a temperature controlled bath filled with water. A submersible magnetic stirrer was used to stir the etchant. A schematic of this setup appears in fig(3-4). An alternate setup for the reflux condenser unit is shown in Appendix B in fig (B-1). The reflux condenser is housed in a heating jacket which has a stir mantle and a temperature control unit. A cooling tower that is 50 cm high, collects the vapors of ammonia and condenses it. A teflon jig was built to hold up four wafers vertically against the wall allowing for the stirrer to stir the solution in the center. Details of the reflux condenser and the teflon jig are contained in Appendix B.

3.3 Material Characterization

The quality of the epilayer was determined using some of the standard material evaluation techniques. The methods used by us to characterize the material were:

- Scanning Electron Microscopy (SEM) of the surface of BESOI substrate.
- Pictures taken with the help of the Nomarsky Microscope.
- Defect etch studies of the surface.
- Profilometer measurements of film thickness for uniformity.

Defect Etch:

The defect etch was done using the Schimmel Etch, which is a mixture of 49% HF & 0.3 mol. CrO_3 in the proportion of 4:5. The wafer was broken into pieces about $1cm \times 1cm$. The surface of these pieces were observed under the Nomarsky microscope

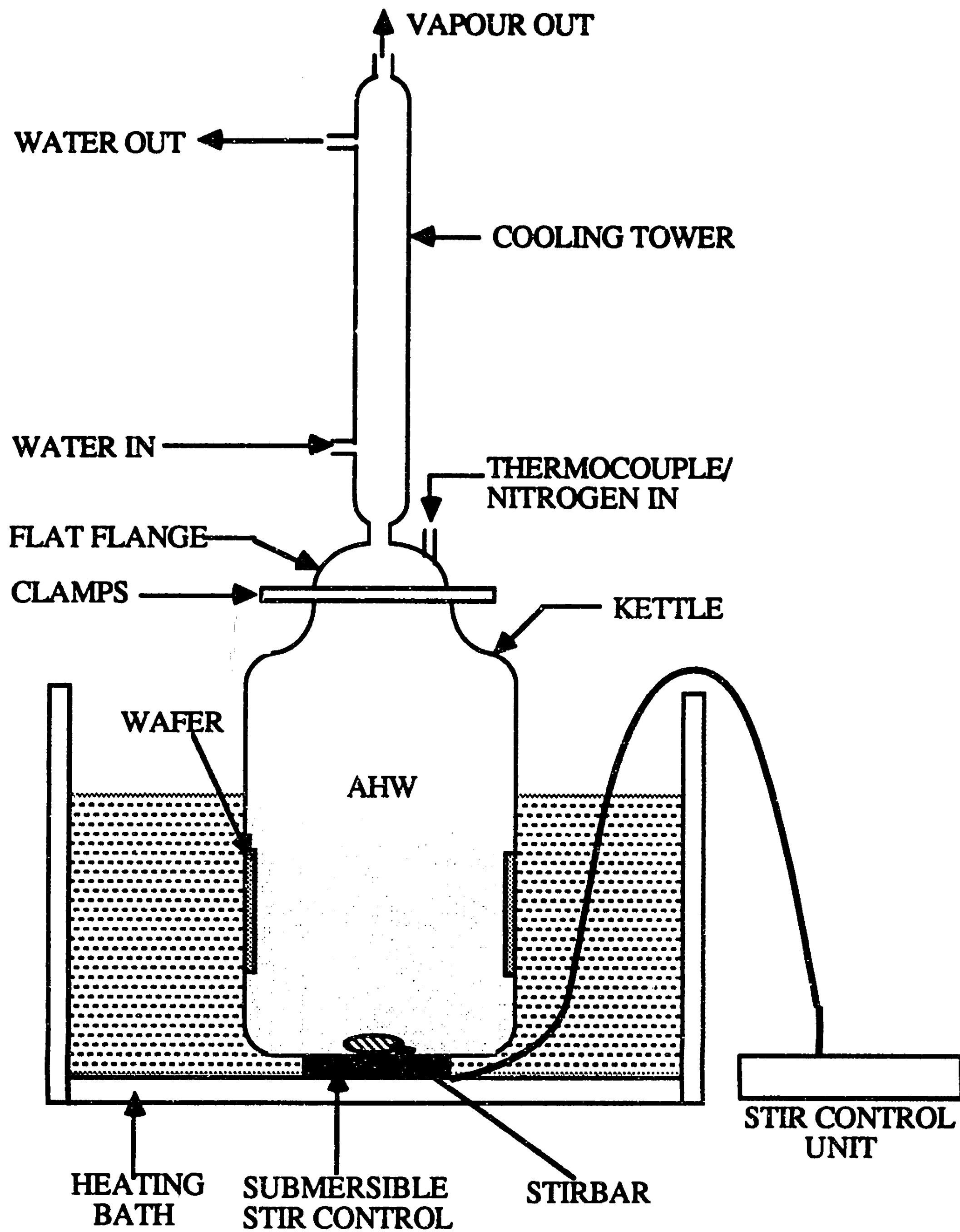


Figure 3-4: Schematic of Reflux Condenser

before the defect etch. The pieces were then put into the defect etch solution and they were allowed to etch for 1.5 minutes. Then they were washed in DI water and dried and then the surface was observed under the Nomarsky microscope.

Pictures of the defect etch studies and the SEM pictures are presented in the chapter V.

3.4 Electrical Characterization

The experiments were designed to inspect the bonded interface of the device layer and the handle wafer and the quality of the insulating oxide. This was done with the help of the IR camera (as mentioned before) and by fabricating capacitors on the BESOI substrate. The process flow for the capacitor structures appears in Appendix D.

3.4.1 Fabrication Summary

The starting material for the fabrication of the capacitors and the final structure of the capacitors is shown in fig(3-5). The first step is to degenerately dope the device layer with phosphorus. This is done by a shallow implant followed by an anneal. The wafer then goes through a lithography step that defines the 500 $\mu m \times 500$ μm capacitor pads. Isolation between devices is obtained by trench etching the silicon between devices.

3.4.2 Leakage Current Measurements

Leakage current measurements were performed on every capacitor structure on the wafer. The number of devices on the wafer were 13,104. The devices covered the entire wafer allowing for the entire wafer to be tested for leakage current. An automatic probe system was used to scan the wafer. The current measurements were done at +10V and -10V. These values were written into a data file and then charted to obtain an estimate of the leakage current distribution across the wafer.

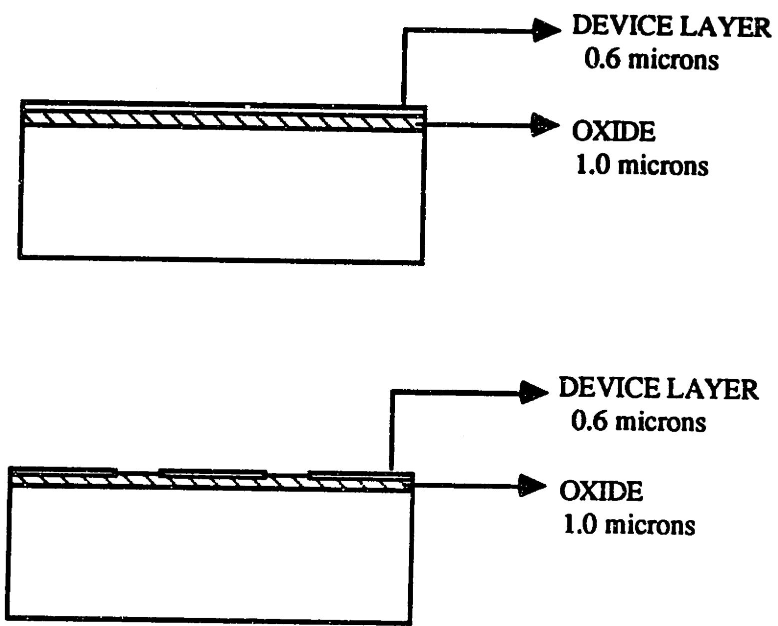


Figure 3-5: Fabrication of capacitors: starting material and final structure

3.4.3 Breakdown Measurements

The capacitors were stressed at 350 volts to determine the reliability of the bonded oxide. The setup used a 200KΩ resistor in series with the capacitor and a high voltage power supply. A measure of the current through the circuit was obtained by monitoring the voltage across the resistor. All the results obtained are presented in Chapter V.

3.4.4 Capacitance-Voltage Measurements

High frequency measurements (100KHz) were performed on the capacitor structures. The applied voltage was swept from -20V to 20V. From the high frequency curve, parameters like oxide thickness, doping concentration and oxide fixed charge were determined. Details of the measurement appear in Chapter V.

Chapter 4

FABRICATION RESULTS

This chapter presents the etch results from the experiments done for characterization of the etch-stop material and etchants. Discussions and comments which explain the trend of data follow the plots and tables that summarize the data.

4.1 Etch-Stop Results

The first experiment was a calibration run which was done to obtain etch-rate results on a prime wafer as control wafer. Results of the calibration run performed at $30°C$ in 20% aqueous KOH are presented in fig.(4-1). The measured etch-rate is 533 Å/min.

Two sets of results, one of which gives information about the different etch-stop materials and the other which illustrates the effect of increasing boron concentration are shown here.

Etch-stop material comparison:

The experimental conditions were as follows

a) Samples - p^+, Si_xGe_{1-x}, $Si_xGe_yB_{1-x-y}$ etch-stops.

b) Etchant - $KOH : H_2O$, 30%, $20°C$.

Fig(4-2) shows a comparison between Si_xGe_{1-x} and $Si_xGe_yB_{1-x-y}$ etch-stop layers. The plot reflects that Si_xGe_{1-x} doped with boron forms a better etch-stop that undoped Si_xGe_{1-x}. This agrees with the anticipated result which asserts that the etch

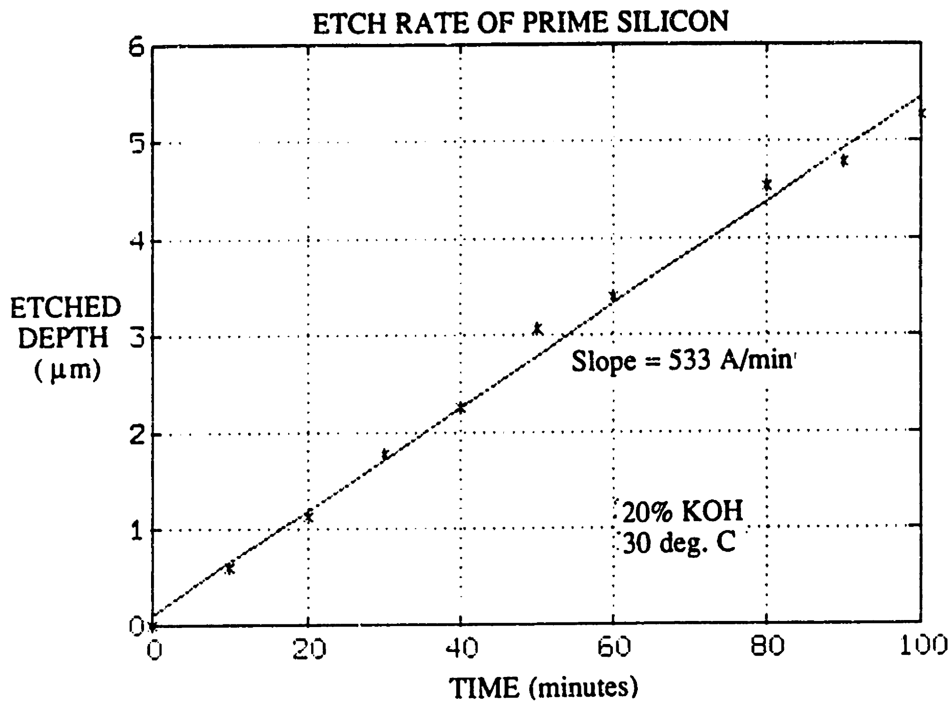


Figure 4-1: Calibration etch

characteristics of Si_xGe_{1-x} doped with boron is determined by the presence of both Si_xGe_{1-x} and boron. Since the concentration of boron is quite high ($5 \times 10^{19} cm^{-3}$) in this case, and boron at high concentrations forms good etch-stops, we expect the etch-stop doped with boron to have high selectivity.

Table(4.1) summarizes the selectivity results obtained for the three etch-stop materials.

ETCH-STOP MATERIAL	SELECTIVITY
p^{++} (1.5 μm) ($N_A = 1 \times 10^{20} cm^{-3}$)	2.5:1
Si_xGe_{1-x} (500 Å) (Germanium 12%)	12.5:1
$Si_xGe_yB_{1-x-y}$ (500 Å) (Germanium 12%, $N_A = 5 \times 10^{19} cm^{-3}$)	55:1

Table 4.1: Summary of etch-selectivities of different etch-stop materials: Etch at $30°C$ in 20% $KOH : H_2O$

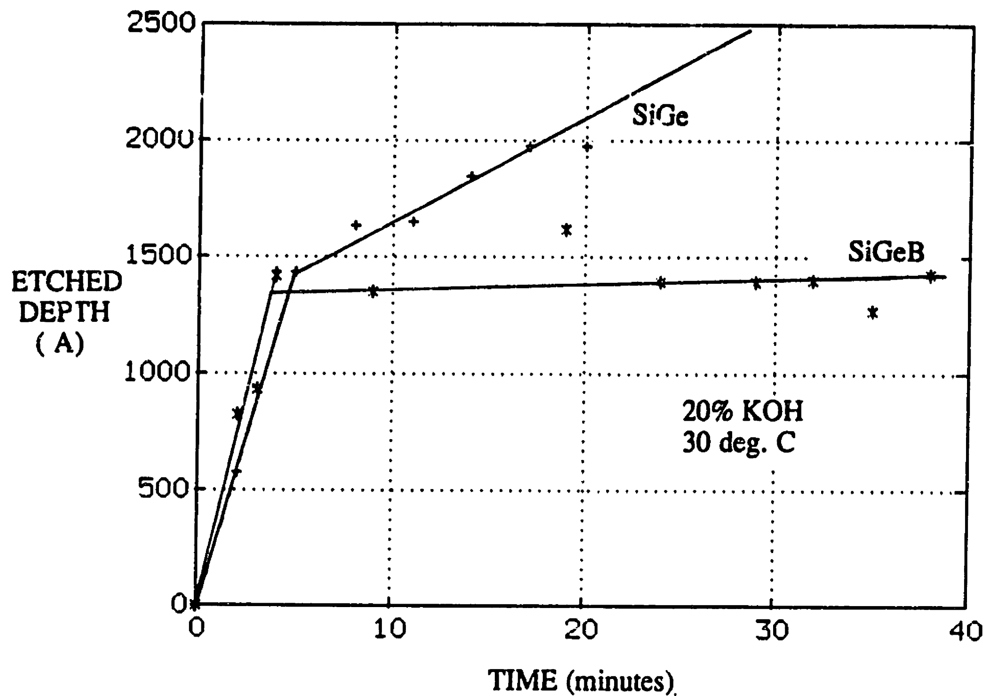


Figure 4-2: Comparison of etch-selectivities of Si_xGe_{1-x} and $Si_xGe_yB_{1-x-y}$ etch-stop layers

Varying germanium concentration:

The conditions for this experiment were

a) Sample - $Si_xGe_yB_{1-x-y}$, $N_A = 2 \times 10^{19} cm^{-3}$, $Ge : 3\%; 5\%; 10\%$.

b) Etchant - $NH_4OH : H_2O$ 3.7% 45°C.

Table(4.2) summarizes the results obtained from the experiment. The main conclusion that can be drawn from the experiment is that increasing the germanium concentration increased the etch-selectivity. At very low germanium concentrations, increasing germanium concentration from 3% to 5% did not seem to influence the etch-selectivity. The low etch rates of the etch-stop layers with low germanium concentration was probably due to boron alone. However, the interesting feature is that the selectivity of all the samples are very high. Selectivities observed with aqueous ammonium hydroxide are better than those obtained from using aqueous potassium hydroxide as etchant. This experiment is an indication to the fact that AHW is potentially a better etchant than aqueous KOH.

GERMANIUM CONCENTRATION	SELECTIVITY
Si_xGe_{1-x} (500Å) (Ge = 3%)	127:1
Si_xGe_{1-x} (500 Å) (Ge= 5%)	127:1
Si_xGe_{1-x} (500 Å) (Ge= 10%)	248:1

Table 4.2: Effect of germanium concentration on etch-selectivity: Etch at $45°C$ in 3.7% $NH_4OH : H_2O$

4.2 Etchant Results

Etchant comparison:

The experimental conditions were

a) Sample - p^+ etch-stop layer.

b) Etchant- AHW 3.7% 45°C; $KOH : H_2O$ 20% 30°C.

Fig(4-3) shows the etch-selectivities obtained by using two different etchants on the same etch-stop material. The etch-selectivities obtained with aqueous ammonium hydroxide is 60 times better than those obtained with aqueous potassium hydroxide. The etch surfaces obtained after the etch-stop had been reached were extremely smooth indicating that uniform layer thickness could be achieved by using aqueous ammonium hydroxide as etchant.

Characterization of AHW:

All the experiments for determination of optimum operating conditions were conducted on prime wafers. The surface topography of these wafers were inspected to determine the effect of varying certain parameters.

- The surface roughness was highest at 10% AHW concentration. As has been indicated earlier, the etch-rate of silicon on ammonium hydroxide is highest at a concentration of 10%. This implies that higher etch-rates cause higher surface

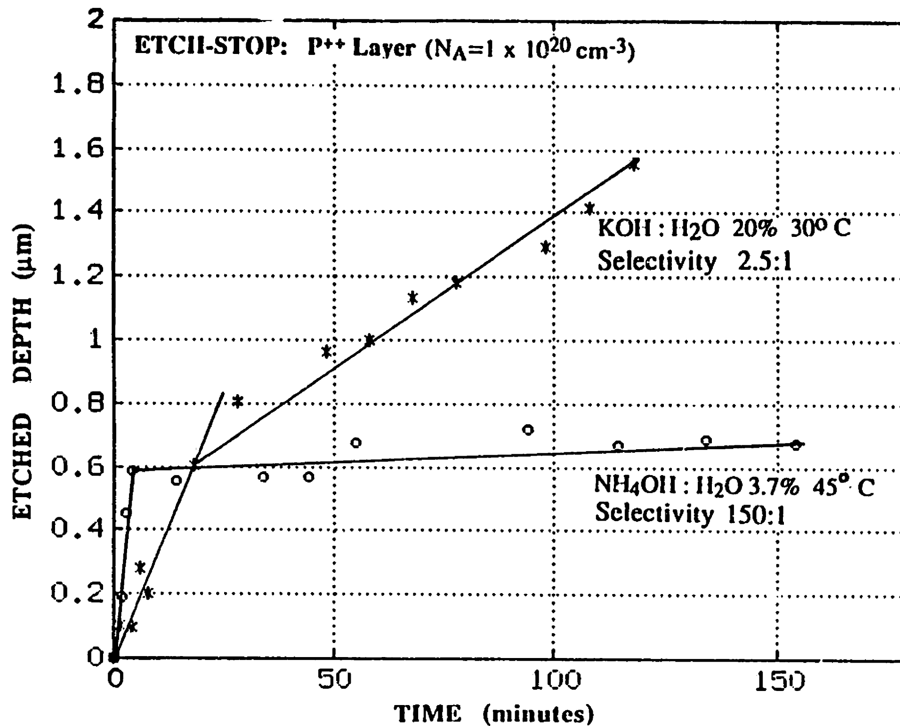


Figure 4-3: Comparison of etch-selectivity of AHW and KOH as etchants

roughness.

- Increasing etching time, increased surface roughness. The point to be noted here is that the experiments were conducted on prime silicon and the results would probably be different if the experimental wafers had etch-stop in them.
- Increasing temperature helped reduce the surface roughness to some extent.
- Stirring the solution during the etch made a noticeable difference on the surface topography of the wafer. While the sample etched without stirring had a rough surface, the sample etched with the solution stirred had an uniform surface with a hazy film on top indicating that the surface roughness had reduced by several orders of magnitude.

The above experimental results indicated that the optimum conditions for etching were higher temperatures and etching in stirred solutions. We decided to etch in 5% AHW at $70^{o}C$ with the solution stirred vigorously.

The phenomenon of surface roughness caused by anisotropic etching of silicon inNH_4OH : H_2O has also been observed by Benecke et.al. [15]. Surfaces etched in KOH : H_2O and EDP have also been found to present this structure and the cause for this kind of a surface topography has been discussed by Seidel et.al. in [18]. Etching fronts of a $<$ 100 $>$-oriented wafer are found to get covered with pyramidal structures which gives the surface a very rough surface topography. The degree of roughness was found to be a strong function of transport phenomenon. Hence, stirring the solution showed a significant reduction in the surface roughness. Surface roughness was also found to decrease the etch-rate significantly due to the strong crystallographic modification of the surface.

Study of the effect of varying N_2 flow-rate indicated that wafers etched under the influence of higher flow-rates had more non-uniform surfaces as compared to those etched with low N_2 flow-rates. The low N_2 flow-rates were enough to create the optimum overpressure and prevent evaporation of NH_3 from the solution. However, high flow-rates aided evaporation of NH_3 causing the AHW solution to deplete fast.

Chapter 5

BESOI: SUBSTRATE PROPERTIES

The BESOI substrates were successfully fabricated and their material properties were extracted. The substrates were prepared from p-type handle wafers which had $1\mu m$ thermal oxide grown on them and device wafers with p^+ etch-stop layers as shown in fig(3-3 a). The electrical characteristics were obtained after fabrication of capacitors on these subtrates. This chapter documents all the material and electrical evaluation results.

5.1 Material Characteristics

Assessment of the material quality was obtained from the SEM and defect-etch results.

5.1.1 SEM Inspection Results

SEM photcgraph of the surface of the BESOI substrate before defect-etch is shown in fig.(5-1). The photograph indicates that the BESOI wafer surface has an approximate defect density of 9×10^3 defects/cm^2. A magnified picture of a defect is also shown in fig.(5-2).

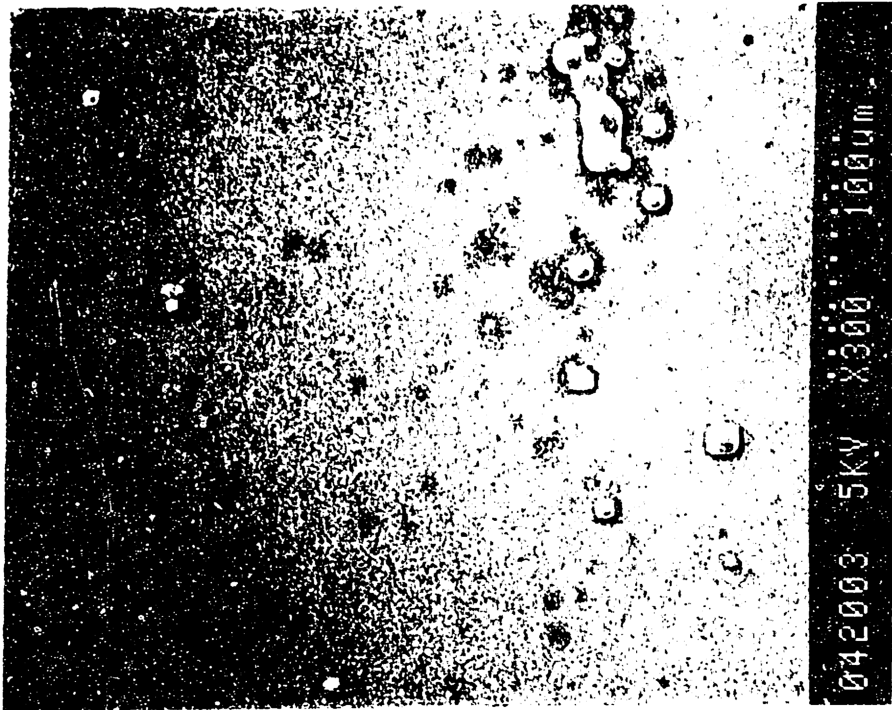


Figure 5-1: SEM picture of BESOI wafer surface

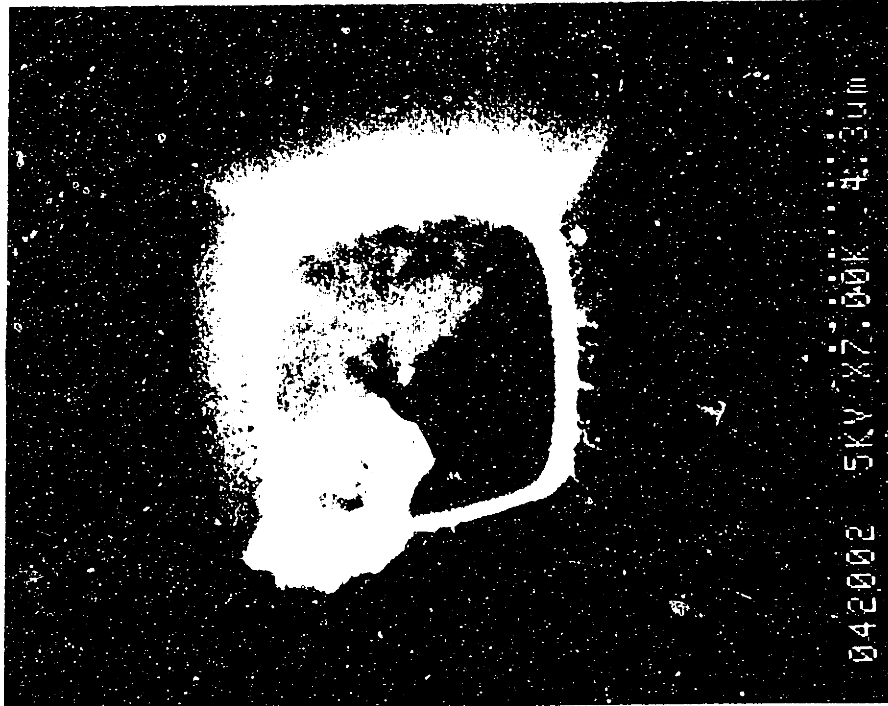


Figure 5-2: SEM picture of magnified defect

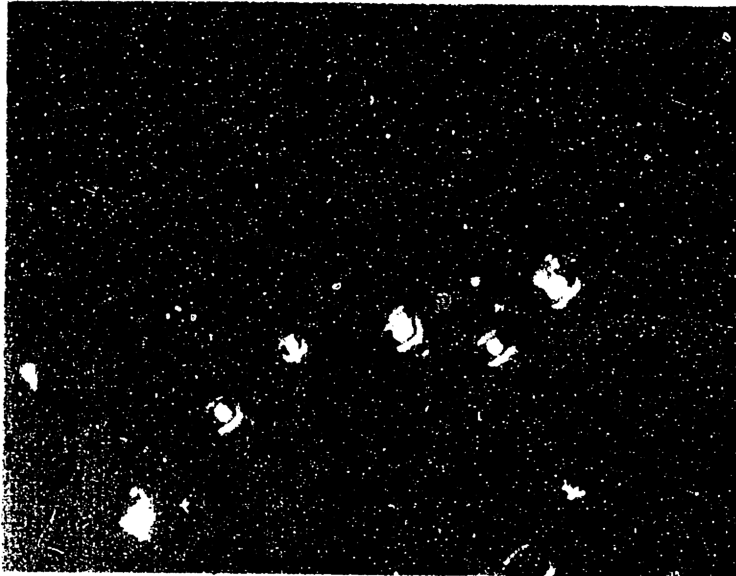


Figure 5-3: Etch pits on BESOI wafer surface (linear magnification: 400)

5.1.2 Defect Etch Results

Etch pits were seen to form on the surface of the BESOI substrate and fig.(5-3) demonstrates such pits. These pits are similar to those obtained by Kelly et. al. [10]. Fig.(5-4) gives an approximate count for defect density as 4.7×10^4 defects/cm^2. Prime wafers, similar to those on which the etch-stop epi-layers were grown, yielded a defect density of 0.6×10^4 defects/cm^2 after defect-etching. A pictures taken with a Nomarsky Microscope is shown in (fig.5-5).

5.1.3 Uniformity of Wafer Thickness

The thickness uniformity of the device layer was studied by measuring the step height from the device layer surface to the oxide below. The measurements were done using a commercial surface profilometer and readings were taken at several locations on the wafer surface. The measured thickness is $6060\mathring{A}$ with a standard deviation of $297\mathring{A}$. Fig.(5-6) gives a comprehensive picture of the device layer thickness at different points on the wafer. It should be noted that this measurement of layer thickness could include some non-uniformity due to the plasma etching of SiO_2 during formation of the Si islands. All measurements indicated on the wafer are in Angstroms.

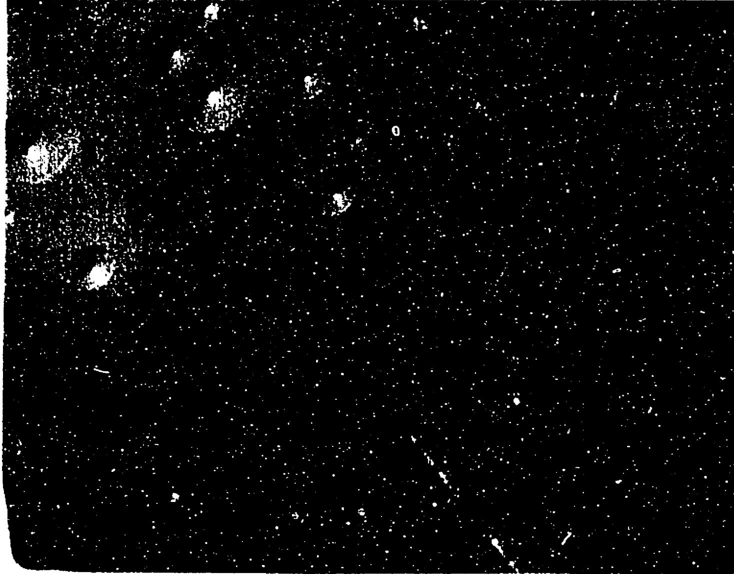


Figure 5-4: Defect-etched surface of BESOI wafer surface (linear magnification: 400)

Figure 5-5: Defect-etched surface of prime wafer surface (linear magnification: 200)

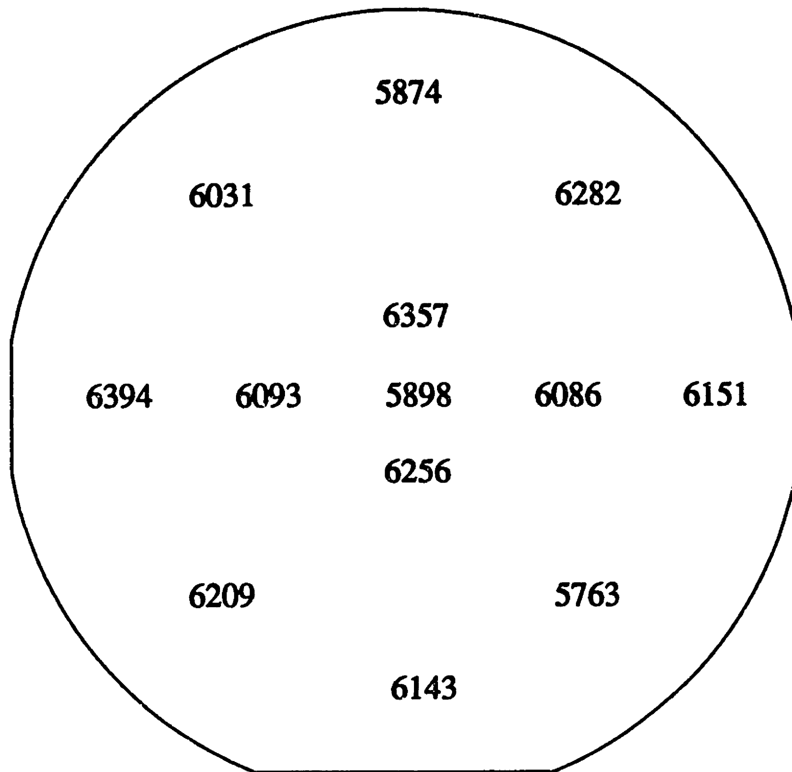


Figure 5-6: Measure of thickness uniformity across the wafer

5.2 Electrical Characterization

Before fabrication of capacitors, a commercial surface profilometer was used to measure the thickness of the device layer. The device layer was found to be 0.65 μm, which was the expected thickness. A sheet resistance mapping of the wafer surface indicated that the doping of the device layer was $5 \times 10^{15} cm^{-3}$. This value of surface doping demonstartes the fact that the device layer was free of any contamination due to out-diffusion of boron from the etch-stop layer. Thus we have successfully preserved the quality of the device layer and the peak of the etch-stop layer by chosing the bonding conditions to be 800°C and time to be 30 minutes.

5.2.1 Interface Quality

The bonded interface was inspected using an Infra-red transmission system. Pictures taken before and after the anneal are show in fig.(5-7). These pictures indicate that the bonded interface is free of macro voids. This shows that the bonding is good and

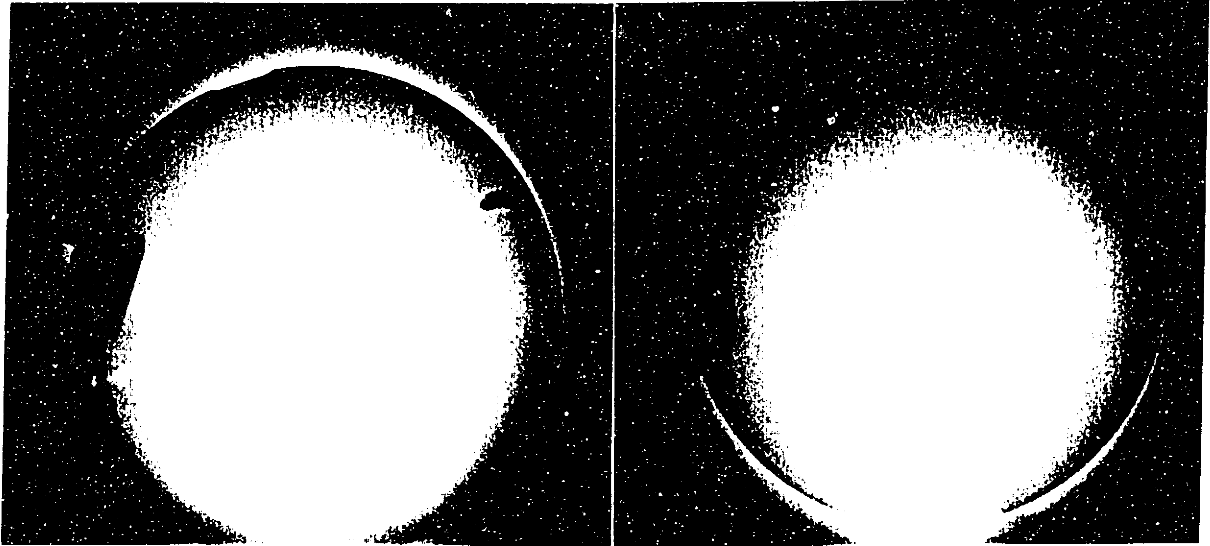


Figure 5-7: IR picture of bonded interface before and after anneal

will produce a high quality insulating layer.

5.2.2 Leakage Current Measurement Results

Leakage current distribution in fig.(5-8) shows that the peak of the distribution occurs at 100pA. This can be estimated as roughly the most probable value of leakage current across the insulating oxide. The maximum value of leakage current is 360pA. None of the devices in the entire wafer failed. These results are encouraging since they show that there is absolutely no leakage in any part of the wafer.

5.2.3 Breakdown Voltage Measurement Results

Breakdown measurements performed at various sites on the wafer showed that the oxide did not breakdown up to 350V which was the limit of the tester. For the 1μm oxide thickness, one would not expect to see breakdown of a thermal oxide. Thus to the limit of our resolution, this result indicates that the process did not compromise the quality of the oxide.

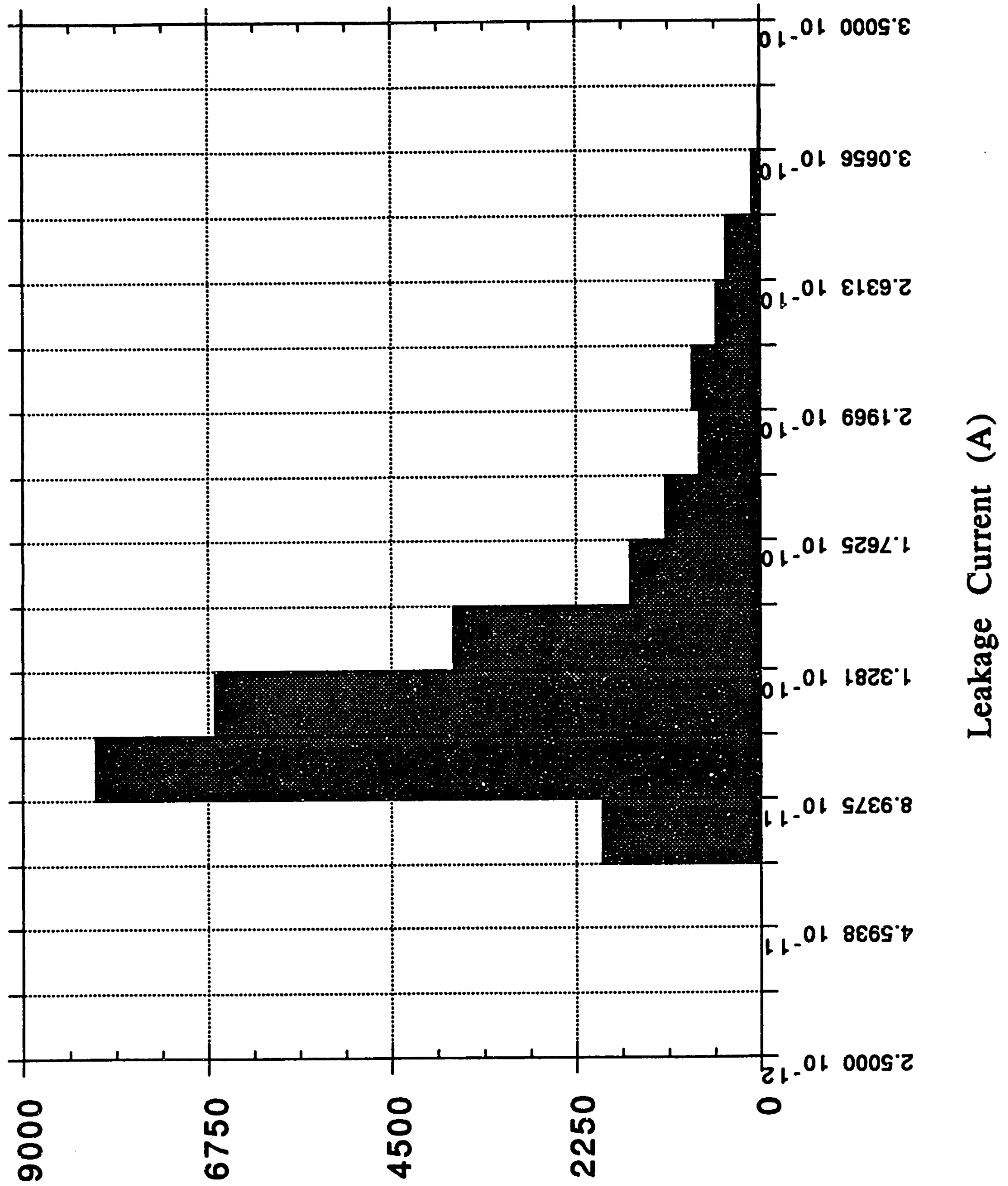


Figure 5-8: Distribution of leakage current

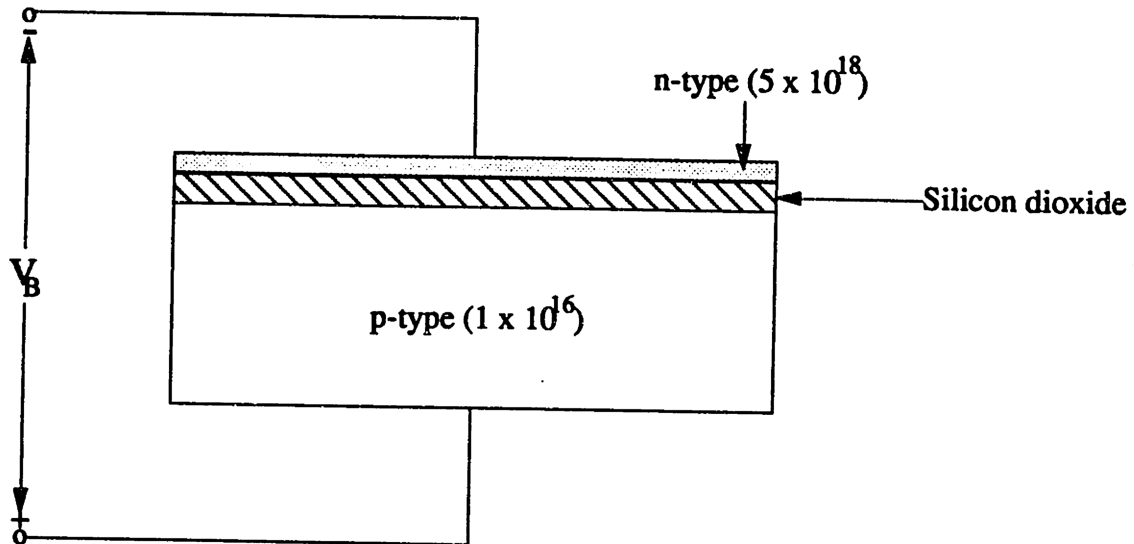


Figure 5-9: Capacitor structure and connections for C-V measurements

5.2.4 Capacitance-Voltage Measurement Results

High frequency measurements were performed on the capacitors at 100KHz. The structure of this Silicon-Oxide-Silicon structure is shown in fig(5-9). Since the upper electrode is heavily doped, it should contribute little to the total depletion capacitance, and we would therefore expect a C-V characteristics similar to a MOS p-type device. The high frequency characteristics are shown in fig.(5-10). The samples had to be dried by flushing with nitrogen for 72 hours. The high frequency plot obtained, had the characteristics as expected for an MOS device.

Parameters extracted from the high frequency measurements were: Oxide thickness, Doping density, Flat-band voltage and Oxide fixed charge.

- T_{ox} = 1.183 μm
- $N_A = 8.5 \times 10^{14} cm^{-3}$ to $1 \times 10^{15} cm^{-3}$
- V_{fb} = -6.5 V to -7.0 V
- $|Q_{ox}| = 1.1 \times 10^{11} cm^{-2}$

These values are found to be consistent across the wafer.

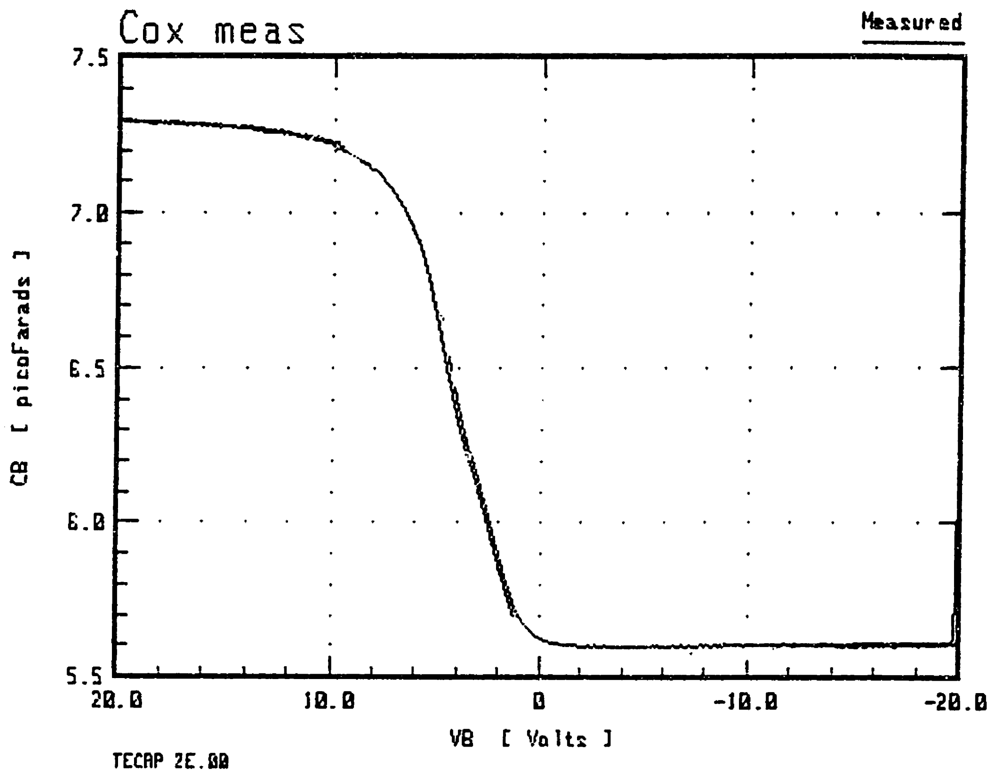


Figure 5-10: High-frequency plot of capacitance against voltage

Chapter 6

CONCLUSIONS

Several important objectives have been achieved in this thesis. Some of the obvious targets that have been met are:

Different etch-stop materials were investigated and it was demonstrated that Si_xGe_{1-x} and $Si_xGe_yB_{1-x-y}$ both form excellent etch-stop materials. However, $Si_xGe_yB_{1-x-y}$ layer exhibit higher selectivity compared to Si_xGe_{1-x} layers.

Aqueous ammonium hydroxide though not as convenient to handle as aqueous potassium hydroxide was demonstrated to have selectivities much higher than aqueous potassium hydroxide. The etchant was standardized and a reflux condenser was built to circumvent the problems involved with handling of ammonium hydroxide. Conditions that produce the best BESOI material were also determined through a series of experiments.

The material quality of the BESOI substrate was found to be comparable to bulk silicon. This was encouraging because it illustrated the fact that the processes seen by the wafer did not affect the quality of the water.

Leakage current measurements indicated very good oxide quality. Breakdown measurements showed that the oxide was reliable and did not breakdown at high voltages. Capacitance measurements indicated that proper isolation was important to obtain normal capacitor performance.

A further investigation into the electrical properties of the device layer is needed. Measurements for extraction of recombination lifetime, mobility and interface state

density need to be performed to obtain a closer assessment of the wafer quality.

Appendix A

Etch rates of Si and SiO_2 in KOH

The etch-rates of Si and SiO_2 as a function of concentration and temperature has been systematically studied by Seidel et.al. [18]. The results are tabulated in the following page.

% KOH	20°	30°	40°	50°	60°	70°	80°	90°	100°
10	1.49	3.2	6.7	13.3	25.2	46	82	140	233
15	1.56	3.4	7.0	14.0	26.5	49	86	147	245
20	1.57	3.4	7.1	14.0	26.7	49	86	148	246
25	1.53	3.3	6.9	13.6	25.9	47	84	144	239
30	1.44	3.1	6.5	12.8	24.4	45	79	135	225
35	1.32	2.9	5.9	11.8	22.3	41	72	124	206
40	1.17	2.5	5.3	10.5	19.9	36	64	110	184
45	1.01	2.2	4.6	9.0	17.1	31	55	85	158
50	0.84	1.8	3.8	7.5	14.2	26	46	79	131
55	0.66	1.4	3.0	5.9	11.2	21	36	62	104
60	0.70	1.6	3.4	6.7	13	24	42	72	78

Table A.1: < 100 > silicon etch rate in μm/hr

% KOH	20°	30°	40°	50°	60°	70°	80°	90°	100°
10	0.40	1.22	3.5	9.2	23	54	123	266	551
15	0.63	1.91	5.4	14.4	36	85	193	416	862
20	0.88	2.66	7.5	20.0	50	118	268	578	1200
25	1.14	3.46	9.8	26.0	65	154	348	752	1560
30	1.42	4.32	12.2	32.5	81	193	435	940	1950
35	1.44	4.37	12.4	32.8	82	195	440	949	1970
40	1.33	4.03	11.4	30.3	76	180	406	876	1820
45	1.21	3.67	10.4	27.5	69	163	369	797	1650
50	1.08	3.28	9.3	24.6	62	146	330	713	1480
55	0.95	2.87	8.1	21.6	54	128	289	624	1290
60	0.81	2.45	6.9	18.4	46	109	246	532	1100

Table A.2: < 100 > silicon-dioxide etch rate in nm/hr

Appendix B

REFLUX CONDENSER

Described here are the details of the reflux condenser used for $NH_4OH : H_2O$ etch. Fig.(B-1) shows the schematic of the reflux condenser and all other additional equipments required. The following page has the complete part list. A more detailed drawing of the kettle for the reflux condenser, is shown in the next page in fig.(B-2). The following three pages contains engineering drawings of the teflon jig that was made at MIT. Fig(B-3) is a top view of the bottom plate of the teflon jig, fig.(B-4) is a top view of the top plate of the teflon jig and fig.(B-5) is the cross-section of the assembled structure.

B.1 Part List

- Kettle: 5.5in. Flat Flange, 8.0in. Height, 200mm O.D. (LG-8082-S).
- Flat Flange Head: 5.5in., CN-24/40, SN-14/35. (LG-8086A-S).
- Clamps: 5.5in, McCarter. (LG-7316-108).
- Magnetic Teflon Stirbar.
- Condenser: Double Cool, Tube Top, 500mm. length 24/40. (LG-4810-108).
- Thermowell: 14/35 (LG-1950-100S).

  Vendor: Lab Glass Inc., P.O.Box 610. Vineland, N.J.-08360.

- Stirrer Mantle: 7.875in. x 6.5in. (LG-8883-S).
- Stir Control Unit: EMC-4. (LG-8810-100).
- Automatic Controller: Mantle Minder. (LG-8956-100).

  Vendor: Glas-col, 711 Hulman Street. Terrehaute, IN-47802.

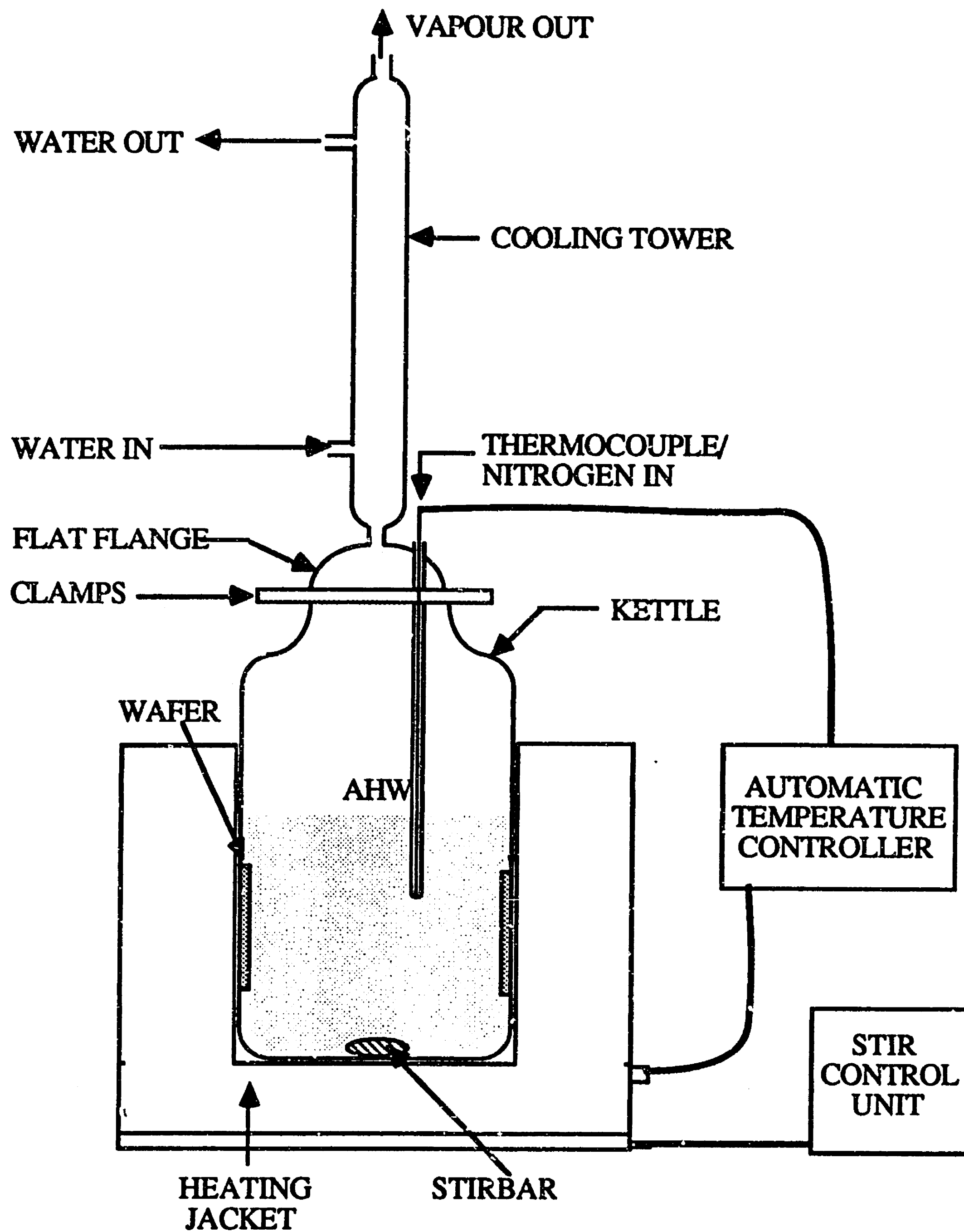


Figure B-1: Schematic of reflux condenser setup

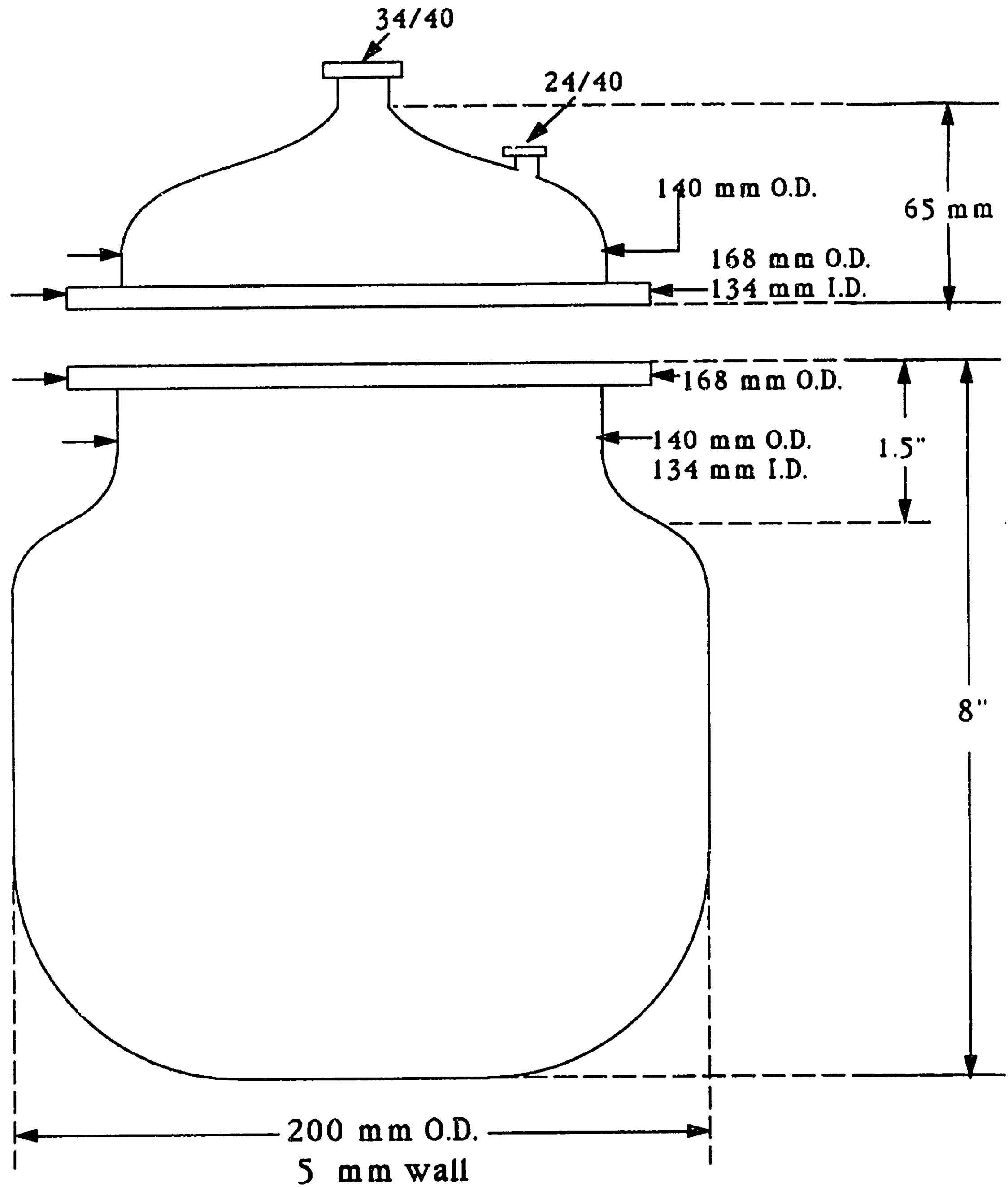
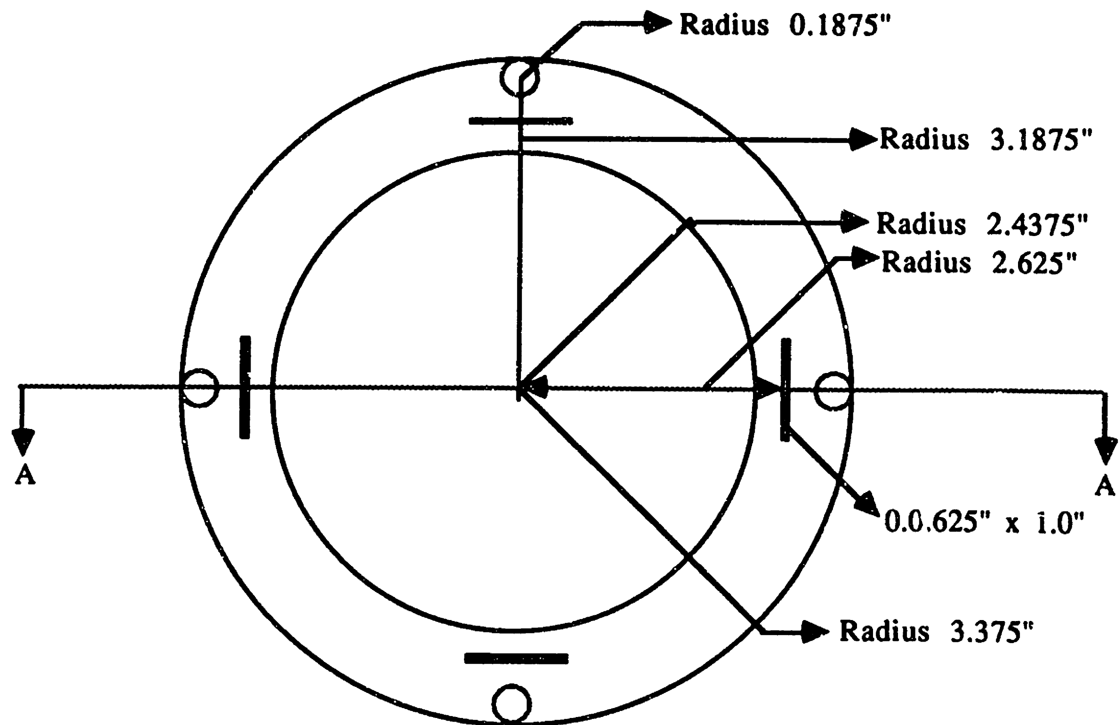
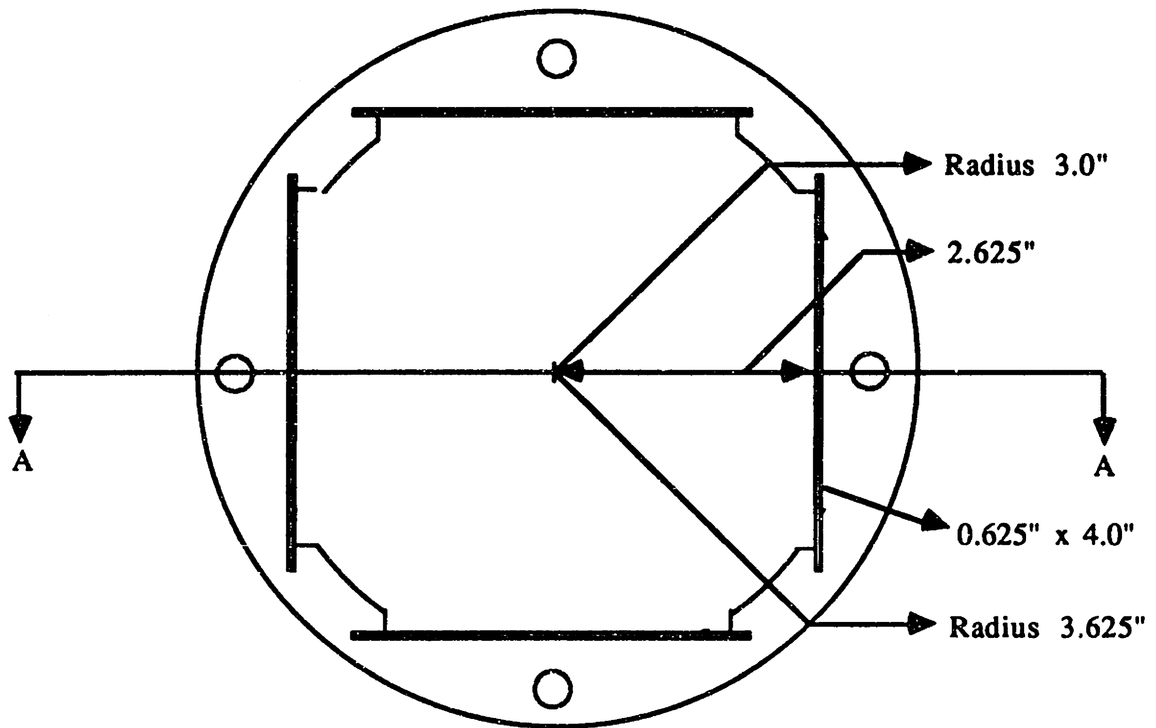


Figure B-2: Detailed diagram of reflux condenser



TITLE: Bottom Ring of Teflon Jig	
SCALE 2:1	PAGE 1 of 3
DATE August 27 1991	
SIGNATURE [signature]	

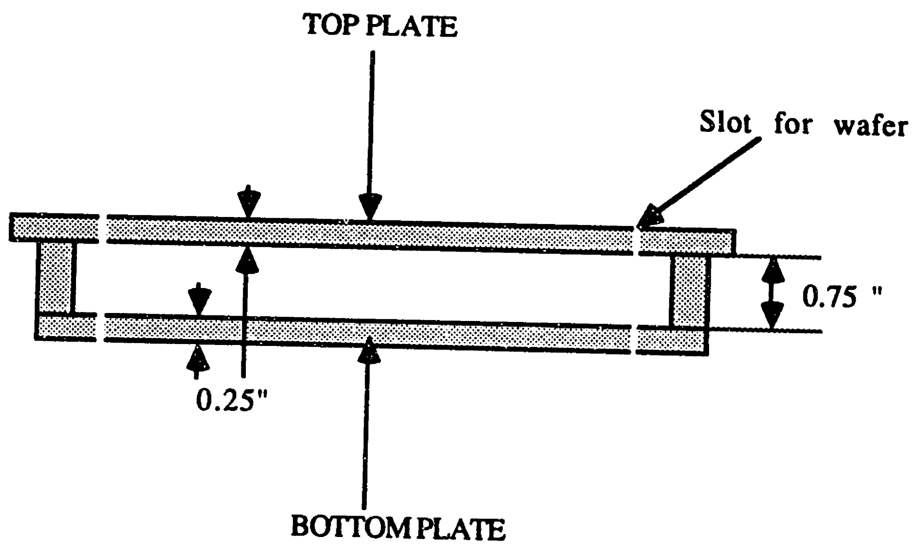
Figure B-3: Top view of bottom plate of teflon jig



TITLE: Top Ring of Teflon Jig	
SCALE 2:1	PAGE 2 of 3
DATE August 27 1991	
SIGNATURE	

Figure B-4: Top view of top plate of teflon jig

SECTION A-A Cross-Section



TITLE: Cross Section of Teflon Jig	
SCALE 2:1	PAGE 3 of 3
DATE August 27 1991	
SIGNATURE	

Figure B-5: Cross section of teflon jig

Appendix C

PROCEDURE: Preparation of BESOI Substrate

Starting Material: p-type handle wafer, resistivity 10-20Ω-cm. p-type device wafer with p^+-etch-stop and p^--epilayer.

Procedure:

- 1 μm of wet oxide is grown on the handle wafer. (Tube B1 or Tube B2).
- Very thin layer of thermal oxide may or may not be grown on the device wafer. (Tube A2).
- Measure thickness of oxide layers grown. (Ellipsometer or Nanospec).
- RCA clean (TRL or ICL).
- Piranha dip for 10 minutes.
- DI rinse and spin dry.
- Bring wafers in contact.
- Inspect using the IR inspection system. (TRL)
- Bond at $800°C$ for 30 minutes in a N_2 ambient. (TRL or ICL).
- Inspect using the IR inspection system. (TRL).

- Strip oxide from back of device wafer. Dip in 10:1 HF solutions.
- Etch away 500μm of silicon in 20% KOH at 60^oC for 16.8 hours and at 56^oC for 2.7 hours.
- Final Etch in AHW:
  - Prepare the etchant by first heating 2317ml of DI water in the reflux condenser placed in a heating bath set to 70^oC.
  - Check temperature of water inside the reflux condensor using the type-J thermocouple.
  - When temperature inside reaches 70^oC, remove thermowell and connect nitrogen jet to the top cap of the reflux condenser.
  - Pour in 483ml of 30% NH_4OH through the opening for the cooling tower. This prepares 2800ml of 5% $NH_4OH : H_2O$. Let this stand in the water bath for 15 minutes.
  - Strip native oxide from surface of wafer by dipping in 7:1 HF solution for 3 seconds.
  - Rinse off HF by immediately dipping in DI water.
  - Remove top cover of reflux condenser and insert the wafers into one of the slots.
  - Set stirrer to maximum rotary speed.
  - Replenish the AHW solution every 4 hours.
- The etch time is determined by the amount of silicon left after KOH etch.
- Strip p^+ layer with the 8:3:1 solution which is a mixture of CH_3COOH:HNO_3:HF. Add small amounts of H_2O_2 to the solution every 15 seconds to prevent the solution from depleting. The p^+-strip takes approximately 3 minutes.

Appendix D

Steps for Fabrication of Capacitors on BESOI

- The BESOI is first cleaned in TRL before it is taken through the processing steps in TRL or ICL. Cleaning is done in piranha for 10 minutes followed by a dip in 50:1 HF, followed by an RCA clean.
- The wafer is then implanted with phosphorus at 30KeV with a dose of $7 \times 10^{15} cm^{-2}$.
- Anneal at $950°C$ for 1 hour, nitrogen ambient.
- Lithography step using MOSCAP NP mask-set patterns $500\mu m \times 500\mu m$ capacitors.
- Plasma etch in etcher 1, using recipe #10 for 1 minute. Details of recipe #10 are given in table(D.1).
- Strip resist
- Remove back oxide with 7:1 BOE for 2 minutes.

%	Step #1	Step #2	Step #3	Step #4	Step #5
Pressure	500mTorr	500 mTorr	200 mTorr	200 mTorr	200 mTorr
RF Top	0 W	30 W	0 W	300 W	200 W
Gap	1.5 cm	1.5 cm	1.5 cm	1.5 cm	1.5 cm
CCL_4	0 sccm	0 sccm	130 sccm	130 sccm	130 sccm
O_2	200 sccm	200 sccm	20 sccm	20 sccm	20 sccm
He	100 sccm	100 sccm	70 sccm	70 sccm	130 sccm
Time	Stable	6 sec	Stable	Time	Overetch

Table D.1: Silicon Plasma Etch (Recipe #10)

Bibliography

[1] Colinge, J.P., "Silicon On Insulator Technology: Materials to VLSI", Kluwer Academic Publishers, Boston, 1991.

[2] Schmidt, D.N. (editor) *Proceedings of the Fourth International Symposium on Silicon-On-Insulator Technology and Devices* Vol.90, No.6, 1990.

[3] "SOI Technology, Part 1", *IEEE Circuits and Devices Magazine*, Vol.13, No.4, Jul. 1987.

[4] Maszara, W.P., "Silicon-On-Insulator by Wafer Bonding: A Review", *Journal of Electrochemical Society*, Vol.138, No.1, 341-347, Jan. 1991.

[5] Muraoka, H., T. Ohhashi and Y. Sumitomo, "Controlled Preferential Etching Technology", *The Electrochemical Society Softbound Proceedings Series*, Princeton, NJ. H.R. Huff and R.R. Burgess, Editors. 327-338, 1973.

[6] Lawrence Semiconductor Inc., Tempe, Arizona.

[7] Haisma, J., G.A.C.M. Spierings, U.K.P. Biermann and J.D.Pals, "Silicon-on-Insulator Wafer Bonding-Wafer Thinning Technological Evaluations", *Japanese Journal of Applied Physics*, Vol.28, No.8, 1426-1443, Aug. 1989.

[8] Lasky, J.B., S.R. Stiffler, F.R. White and J.R. Abernathey, "Silicon-On-Insulator (SOI) by Bonding and Etch-Back", *Digest of Technical Papers IEDM-85*, 684-687, 1985.

[9] Harendt, C., C.E. Hunt, W. Appel, H. Graf, B. Höfflinger and E. Penteker, "Silicon On Insulator Material By Wafer Bonding", *Submitted to Journal of Electronic Materials.*

[10] Kelly, M.J., T.R. Gulinger, J.W. Medernach, S.S. Tsao, H.D.T. Jones and J.O. Stevenson, "Identification of Defects in SOI Wafers", *Proceedings of the Fourth International Symposium on Silicon-On-Insulator Technology and Devices* Vol.90, No.6, 120-128, 1990.

[11] Herzog, H.-J., L. Csepregi and H. Seidel, "X-Ray Investigation of Boron- and Germanium-Doped Silicon Epitaxial Layers", *Journal of Electrochemical Society,* Vol.131, No.12, 2969-2974, Dec. 1984.

[12] Godbey, D.J., M.E. Twigg, H.L.Hughes, L.J.Palkuti, P.Leonov and J.J.Wang, "Fabrication of Bond and Etch Back silicon on Insulator Using a Strained $Si_{0.7}Ge_{0.3}$ layer as an Etch Stop", *Journal of Electrochemical society* 1990.

[13] Godbey, D., H. Hughes, F. Kub, M. Twigg, L. Palkuti, P. Leonov and J.Wang, "A $Si_{0.7}Ge_{0.3}$ strained-layer etch stop for the generation of thin layer undoped silicon, *Applied Physics Letters*, Vol.56(4), No.22, 373-375, Jan. 1990.

[14] Hunt, C.E., G.V. Rouse, C. Harendt and M.L. Green, "Highly Selective Etch Stop by Stress Compensation for Thin-Film BESOI", In *Proceedings of IEEE SOS/SOI Technology Conference*, Key West, 145-146, Oct 2-4, 1990.

[15] Schnakenberg, U., W. Benecke and B. Löchel, "NH_4OH-based Etchants for Silicon Miromachining", *Sensors and Actuators* A21-A23, 1031-1035, 1990.

[16] Schnakenberg, U., W.Benecke, B. Löchel, S. Ullerich and P. Lange,"NH_4OH-based Etchants for Silicon Miromachining: Influence of Additives and Stability of Passivation layers", *Sensors and Actuators* A25-A27, 1-7, 1991.

[17] Gould, G. and E.A. Irene, "An *In Situ* Ellipsometric Study of Aqueous NH_4OH Treatment of Silicon", *Journal of Electrochemical Society,* Vol.136, No.4, 1108-1112, Apr. 1989.

[18] Seidel, H., L. Csepregi, A. Heuberger and H. Baumgärtel, "Anisotropic Etching of Crystalline Silicon in Alkaline Solutions", *Journal of Electrochemical Society*, Vol.137, No.11, 3612-3626, No.1990.

[19] Seidel, H., "The mechanism of Anisotropic Silicon Etching and Its Relevance for Micromachining, In *Proceedings of 4th International Conference on Solid-State Sensors and Actuators- Transducers '87*, 120-125, Tokyo, Japan, 1987.

[20] McNeil, V.M., S.S. Wang, K.Y. Ng and M.A. Schmidt, "An Investigation of the Electrochemical Etching of (100) Silicon in CsOH and KOH", *Solid-State Sensors & Actuators Workshop*, 92-97, Hilton Head Island, South Carolina, June 1990.

[21] Jackson, T.N., M.A. Tischler and K.D. Wise, "An Electrochemical P-N Junction Etch-Stop for the Formation of Silicon Microstructures", *IEEE Electron Device Letters*, Vol.EDL-2, No.2, 44-45, Feb.1981.

[22] Heyboer, W.L.C.M., G.A.C.M. Spierings and J.E.A.M. van den Meerakker, "Chemomechanical Silicon Polishing: electrochemical *in situ* measurements", *Journal of Electrochemical Society*, Vol.138, No.3, 774-777, Mar.1991.

[23] Sarro, P.M. and A.W. van Herwaarden, "Silicon Cantilever Beams Fabricated by Electrochemically Controled Etching for Sensors Applications", *Journal of Electrochemical Society*, Vol.133, No.8, 1724-1729, Aug.1986.