Energy Efficient sub-Terahertz Electrical Interconnect

by

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Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

With the end of Moore's Law and Dennard scaling in silicon platforms, coupled with the increase in computational demand across applications, the semiconductor industry has seen a move towards high-density compute leveraging multiple dies in package. These types of products have been partially enabled by short-reach, energy-efficient, high-speed interconnect in package. Big data and AI/ML applications have pushed the development of longer-reach, high-capacity, and energy efficient interconnect enabling connectivity between racks across large data centers. This work investigates and demonstrates a new interconnect technology that fills a meter-class interconnect gap in these applications. By leveraging the wide transmission bandwidth and low-losses associated with dielectric waveguides in the sub-THz regime (100 GHz - 1 THz), large baseband data rates are aggregated across multiple channels, multiplexed on to a single electrical channel, efficiently coupled into a dielectric waveguide, and transmitted between chips.

In this work, enabling component technologies are developed and demonstrated, including planar broadband couplers and high-performance sub-THz multiplexers operating in the 220-330 GHz WR-3.4 band — both technologies designed to ease implementation and packaging costs. Lastly, an end-to-end link is realized in a 130nm Silicon Germanium BiCMOS process and is demonstrated utilizing a small cross-section polymer dielectric waveguide. The link achieves 105 Gbps in a 250×400 μm^2 waveguide cross section, demonstrating a state of the art 330 Gbps/mm figure of merit and better than 5 pJ/bit energy efficiency.

Thesis Supervisor: Ruonan Han
Title: Associate Professor of Electrical Engineering and Computer Science

Acknowledgments

The culmination of this research effort has been, to put it mildly, circuitous, covering a lot of organizations. This acknowledgement is a bit long, but I have been absolutely blessed to have had the support of too many amazing people to list. I have endeavored here, however, to list a small subset of people I will forever appreciate for their help along this journey.

I started my doctoral journey much earlier in life, in 2004, under the guidance of the late Professor David Staelin and Professor Joel Dawson. I was drawn into military service, or rather I was compelled by the events of September 11, 2001. I will be forever in debt to Professor Staelin and Professor Dawson for their kindness, understanding, and support in facilitating the pause in my doctoral pursuits and pivot to military service.

I was blessed to eventually find my way back to academic pursuits as military officer serving as a program manager at the Office of Naval Research. During the last 6 years I was lucky enough be supported (via funding, collaboration, and/or laboratory space/equipment) by ONR, the Naval Research Laboratory, MIT Lincoln Laboratories, Intel, and Raytheon Technologies.

At MIT, I'll be forever grateful to my thesis supervisor, Professor Ruonan Han, whose mentorship, understanding, and friendship have been an inspiration. I'm also indebted to my other committee members – Professors Duane Boning and Jacob White. A number of students in Professor Han's THz Electronics group provided much-needed support in the early days of this research. A special thank you to Professor Dave Perreault, who took a cold call from a student from the early 2000's that led to my introduction back into the MIT community.

At ONR, I would not have been able to pursue a PhD concurrently with military service had it not been for Dr. Larry Schuette, Mr. Lee Mastroianni, Dr. Peter Squire, Colonel William Zamagni (USMC, Ret.), Dr. John Pazik, Dr. Paul Zablocky, Dr. Reggie Williams, and Vice Adm. Mat Winter. They performed uncounted administrative miracles to allow me the flexibility to re-start the journey I had put

on pause years earlier.

At the Naval Research Laboratory, there are literally hundreds of people I need to acknowledge. Dr. Roger Cortesi, as an MIT alumnus and former Naval Officer, took an aspiring PhD student and found a niche within that enterprise where I would have the tools to successfully execute. Within NRL Code 6850, I enjoyed laboratory facilities and material budgets unmatched by what I would have had a MIT alone. Dr. Harvey Newmann, Dr. Colin Joye, Dr. Alan Cook, Dr. Baruch Levusch, Dr. Jeff Pond, Dr. Eric Naglich, Dr. John Rogers, Dr. Dave Abe, and Dr. David Meyer all provided immense support, guidance, and advocacy within NRL. I wouldn't have been able to perform some of the fabrication miracles required during this research without Mr. Spence Albright. I would like to extend a special thank you to Dr. Luciano Boglione, Mr. Joel Goodman, and Dr. Sanghoon Shin for their friendship, mentorship, and help along this journey.

At MIT Lincoln Laboratories, I was blessed to connect with Colonel John Kuconis (USAF, Ret.), the Executive Officer for the Lab Director. He administered the Military Fellow program that paid for the early years of my doctoral work. Dr. Tim Hancock took a chance on me over a lunch in the lab cafeteria, cementing initial funding for the concept – thank you Tim. Dr. Chris Galbraith shared an office in Division 8 at the lab with me when I was physically there. He provided a great sounding board and continues to tell me I'm "really a filter guy."

From Intel, I'd like to thank the entire team, who weighed in on the concept during monthly meetings, but specifically Dr. Georgios "George" Dogiamis, who was my primary contact. The organic packaging work and a lot of the system application and context work rose out of direct contact with George. He spent many nights and weekends working with me on manuscripts for papers and was always available to rush a shipment of materials to me to help in fabrication or testing.

When I transitioned out of active duty military and into the commercial sector, I will always be grateful to LtCol Dan Schmitt (USMC, Ret.) who continued to provide flexibility and autonomy – allowing me to do my "day" and my "night" jobs without onerous external stresses. I was blessed to have landed a research and development

job with Raytheon during transitioning out of the military, while continuing to work through my PhD. This would normally be a non-starter, had I not landed in Raytheon IDS's Advanced Technology Programs division under the leadership of Dr. Ellen Ferraro and Mr. Colin Whelan. The required flexibility, autonomy, tuition, and camaraderie the Raytheon AT team has shown me over the last two years has been simply without compare. Thank you, specifically, to Mr. John McElroy, Mr. Matt Tyhach, Mr. John Finkenaur, and Ms. Nina Caissie. I'd also like to provide a special acknowledgement to Dr. Andrew Marcum, (Raytheon BBN), Mr. Tom Markarian (Raytheon Intelligence and Space), and Dr. Tom Kazior (Raytheon Missiles and Defense, DARPA) who have been much needed close friends during the last two years in which I have led a dual-life with a full-time job and a full-time PhD.

When I found myself in Cambridge for a campus visit or a meeting with faculty, I was thankful to draw on old college friends still in the area. Thanks to Mr. Matt Humbert and Mr. Dan Schultz, in particular. I spent many a dinner with Drs. Beth and Brook Longmaid, sharing trials and tribulations.

All of this would not have been possible without the life lessons my parents provided: always provide the maximum effort in whatever it is you do and follow through. I leaned on them a lot over the years. Thank you to both of you for your support, but most importantly for instilling in me determination.

Last, but certainly not least, I have been blessed since I met my wife, Allison, more than a decade ago. She has comforted me in dark times and cheered me on through deployments, absences, *a lot* of moves, career changes, and during this PhD. Her parents, David and Nona, have also played a monumental role (thankfully) in our lives these last 6 years. Allison has given me two children, James and Adeline, that are the light of my life. I have made sacrifices in pursuit of this work, and, in many respects, my children had those sacrifices placed on them. It is only by her grace and sacrifice that my children didn't feel more of that burden. Thank you Allison, for everything.

This doctoral thesis has been examined by a Committee of the Department of Electrical Engineering and Computer Science as follows:

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Chairman, Thesis Committee
Clarence J. LeBel Professor in Electrical Engineering, and Professor of Electrical Engineering and Computer Science

Professor Jacob K. White .....
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Cecil H. Green Professor of Electrical Engineering and Computer Science

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Thesis Supervisor
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Chapter 1

Introduction

1.1 Terahertz Interconnect: A Potential Gap Filler Between Electrical and Optical Interconnect?

The continued increase in computing capability that has occurred through the technology scaling foretold by Moore [70] and Dennard [19] has led to a commensurate increase in the I/O requirements of computing systems. This phenomenon has been most significantly experienced in terms of the interconnect technologies in large data centers (DC) and high performance computing (HPC) applications. Historical data have shown 2∼3X increase in aggregate data rates every two years [80]. This space covers a variety of different interconnect length scales. In a comprehensive survey by Thraskias, et al. [94], high-speed interconnects are grouped according to the following taxonomy:

1. Rack-to-rack: Interconnects in this range, ranging from a few meters to hundreds of meters, are presently served through a variety of high-speed optical and mid-speed electrical (such as Ethernet and InfiniBand^{TM}) interconnect technologies.

2. Board-to-board: Within a given rack, shorter-range electrical interconnects are utilized. These technologies are designed to address efficient, high-speed transport from tens of centimeters to a few meters.

3. Module-to-module: Interconnects on the scale of several to tens of centimeters address high-speed connections across backplanes, cards, etc.

4. Chip-to-chip: Technologies in this group generally address communication across a backplane or within a larger multi-chip module. They are on the order of a few centimeters. Examples include DDR as well as ESIstream and JESD204 for high-speed parallel analog-to-digital interfaces.

5. Core-to-core: High speed signaling among individual processor cores and memory in a system-in-package or a multi-Chip Module is handled via interconnects across a short-range of a few to tens of millimeters. Examples include Intel Embedded Multi-die Interconnect Bridge (EMIB$^{\text{TM}}$).

All of the above applications are presently dominated by optical and electrical interconnects. As discussed in [34, 46, 94], the attenuation and dispersion associated with copper-based electrical interconnects lead to an ever-increasing challenge to achieve both higher data rates and longer reaches. One example can be observed from the roadmap for Ethernet over copper-based channels [1]: while the data rates are doubling every 3-4 years, the maximum reach is reduced by half, thus resulting in a relatively constant bandwidth-distance product. To some extent, the frequency-dependent loss can be addressed through the use of transmitter pre-emphasis, receiver equalization and forward error correction techniques, while larger waveguide or transmission line loss can be compensated by signaling with higher power. These, however, inevitably reduce link efficiency and increase latency, with equalization becoming increasingly difficult at higher signaling bandwidth. As a result, increasing the data rate per lane in electrical links gets increasingly difficult for long-reach applications. High-order pulse amplitude modulation (PAM) is being adopted to keep the signal bandwidth low. For short-reach applications, such as inter-chip/core and small backplane communications, copper interconnects with high parallelism and density (Tbps/mm) still serve well to provide high throughput, thanks to the low cost and small footprint of the links, as well as their full compatibility with silicon infrastructure.

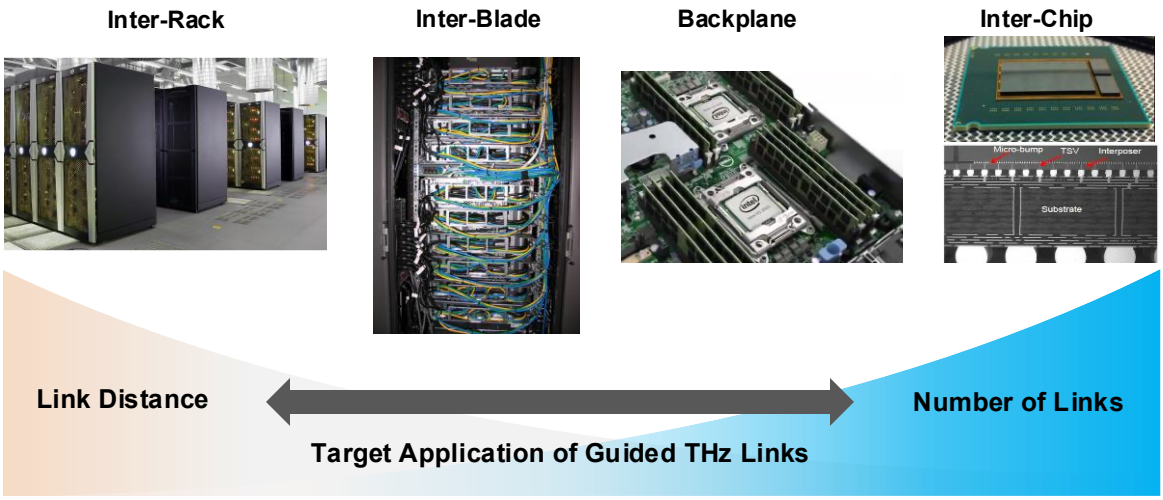


Figure 1-1: An opportunity for insertion of a high date-rate, efficient, and cost-effective guided terahertz interconnect into an existing ecosystem of optical and electrical interconnects. From [43]

In comparison to copper, optical channel media exhibits excellent loss characteristics and substantially more available channel bandwidth. These advantages have led to ubiquitous adoption of long-haul fiber links with tera-scale aggregate data rate. However, the use of various sources and electro-optical components fabricated with III-V semiconductors renders the integration with commodity silicon processes difficult and expensive. In addition, the reliance of the operation on stabilized environmental temperature and high-precision component alignment degrades the reliability and further increases maintenance cost. It should be noted that significant research and development efforts have been focused on improving the efficiency of optical links below a meter; and the associated link efficiency and bandwidth density with more efficient lasers and electro-optical modulation schemes start to make the links competitive with their electrical counterparts [94]. Nevertheless, due to the aforementioned problems, optical links are still better suited for low-density, inter-rack connections across tens to hundreds of meters in HPC and DC.

While both long (tens of meters and above) and short (tens of centimeter and below) links are being well-addressed, the gap between the two regimes provides an opportunity to investigate high-performance and low-cost alternatives. In this class of links, meter-level interconnects for neighboring server racks and backplanes are

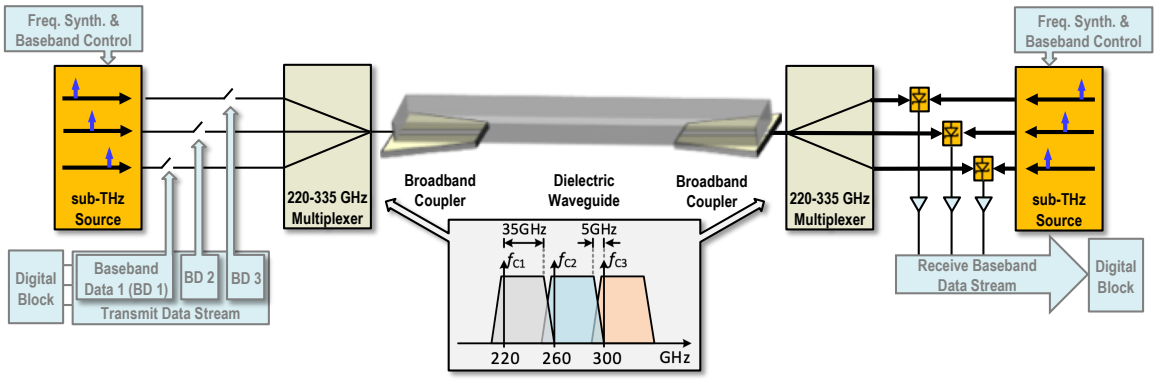


Figure 1-2: Generalized parallel architecture to realize high-data rate digital communication utilizing a rectangular dielectric THz waveguide.

required to transport data at hundreds of Gbps per lane and high link densities. This inter-blade and backplane regime is in critical needs of performance improvement and cost reduction (Fig. 1-1). That is where we believe *terahertz (i.e. 0.1∼1-THz) signals, generated and manipulated by electrical silicon chips, aggregated together to leverage the wide available waveguide bandwidth, and then transmitted over dielectric waveguides* (Fig. 1-2) may play a promising role.

Recently, there has been growing interest in research related to these types of concepts. Prof. Gu discussed the applications of waveguide-confined THz for communications, the concept's comparisons with all-electrical and optical interconnect, and enumerated a number of the challenges associated with realizing such a link utilizing a *single* RF channel per waveguide [34]. The overall architecture shown in Fig. 1-2 has a number of similarities to the Multiband RF Interconnect (MRFI) concept advanced by Prof. Chang at UCLA [60, 92] and others [12], in which multiple narrow-band data streams are multiplexed onto a *conductive* transmission medium. In comparison, this work showcases the very broad bandwidth, low losses, and smaller guide cross section associated with dielectric terahertz waveguides is utilized.

Previously, applications of THz components have centered around radio astronomy, non-invasive imaging, molecular structure studies, and wireless communications [29, 81, 87]. Over the past decade, developments of THz electronic components, especially those on commercial CMOS/BiCMOS chips have made significant progress

and are making guided-THz communication (Fig. 1-2) practical and affordable using existing silicon infrastructures. In addition, a variety of studies have been done to understand the material, waveguide, and supported modes' impact to transmission and dispersion, just as in the fiber optics community, in the THz and sub-THz regimes [4]. While there has been some work on designing THz waveguides for low loss *and low dispersion* [24, 66, 73, 113, 114], more work needs to be done to demonstrate achievable dispersion at the lower THz or sub-mmWave frequencies addressed by silicon circuits. Achieving lower dispersion has an important impact on overall link performance by significantly reducing the complexity, power, cost, and latency associated with equalization schemes.

Operating at lower frequencies than optical solutions also provides additional robustness to waveguide misalignment. Due to the difference in operating wavelength, one expects a THz interconnect to demonstrate a few orders of magnitude more misalignment tolerance than an optical scheme. This would allow low-cost, misalignment-tolerant cable connections, which is one key for the cost reduction of the overall system. Furthermore, the cable itself i.e, the THz waveguide, is targeted to be manufactured using similar low-cost techniques as those used for twinaxial cables, for example. Packaging required for the system is neither custom, nor out of exotic materials or processes. This is yet another aspect that would lead to further system cost reduction. Hence, this link technology offers the promise of an end-to-end solution that will keep costs low from every perspective, while enabling excellent data rate and efficiency performance.

1.2 Enabling Technologies

Recent developments in THz materials, components, active semiconductor devices, packaging processes, and circuit techniques are paving the way towards a high-speed-per-lane, energy-efficient interconnect in the meter range, based on modulated and waveguide-confined THz waves. In this section, a few enabling technologies are introduced and analyzed.

1.2.1 THz Dielectric Waveguides

Sub-THz and THz waveguides with waves confined in dielectrics, although more lossy ($\sim$1$\sim$10 dB/m) than fiber optic cables, provide significant attenuation improvements over electrical channels with similar bandwidth (>100 GHz) [26, 50, 51, 73, 74, 85]. Even at lower frequencies, there is a stark contrast in the loss characteristics of a dielectric waveguide and existing copper backplanes. In [89] a hollow-tube is examined at V-band and demonstrates $90 - 180$ dB less loss than a 1-meter copper backplane. These advantages increase with higher operating frequencies where copper conductor-associated losses continue to increase.

In addition, the employed dielectric materials, usually consisting of amorphous polymer dielectrics, are relatively low cost. These materials can be processed using low-cost manufacturing techniques, and are often compatible with existing printed circuit board technologies.

The published works to date have studied a variety of waveguide materials and geometries [26, 34, 50, 51, 73, 74, 85]. These include a number of different waveguide cross sections – hollow cylindrical, solid cylindrical, fiber bundles, and rectangular waveguides. Each of these geometries support a number of different spatial modes with varying single-mode operating frequencies. In addition, given the wavelength of operation in the THz regime (between 0.3-3 mm) and spatial constraints imposed by the platform architecture, one can consider the realization of both sub-wavelength and wavelength-scale cross sections. This decision can have significant impact on associated radiative and mode-coupler loss, as well as dispersion. The survey carried out by Atakaramians, et al. [4] is an excellent resource, which discusses the trade-offs associated with the design of waveguides (e.g. shapes, sizes and material properties). This is a very rich area offering a large number of different waveguide types that may be considered depending on the application requirements.

The discussion here will focus on sub-wavelength waveguides with rectangular cross sections, as it lowers the barrier to planar integration [20, 46] and can be readily manufactured either by laser-cutting existing sheets of bulk material or by direct

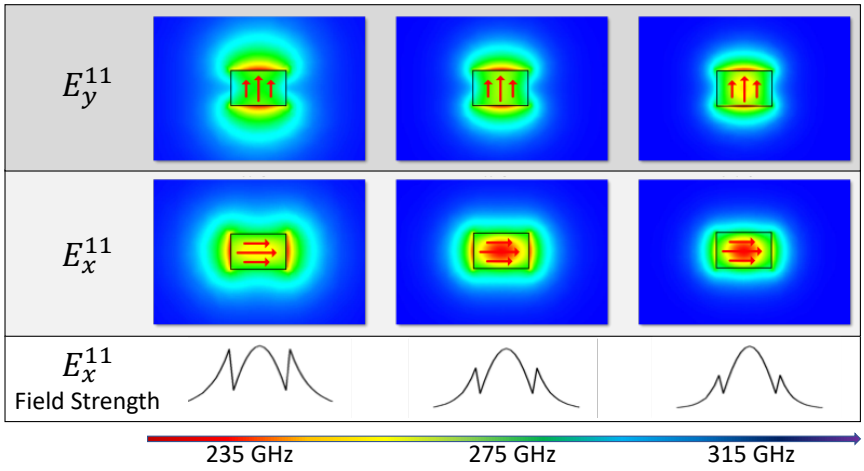


Figure 1-3: Simulated mode confinement in a rectangular dielectric waveguide at varying frequencies. This waveguide has a $250 \times 400\mu\text{m}^2$ cross section and is made from Rogers R3003$^{\text{TM}}$ dielectric material. The vertically- and horizontally-polarized quasi-TE modes are shown at various frequencies in H-Band in the top and middle rows, respectively. One can see the modal profile remains consistent. The bottom row demonstrates that a larger proportion of the modal energy is contained within the waveguide itself at higher frequencies (in this case, the horizontally-polarized mode). From [43].

polymer extrusion. Moreover, it provides (with the proper choice of material properties, operating band, and dimensions) separate quasi-horizontally and quasi-vertically polarized modes in the form of lower-order hybrid modes [3,23,46] (see Fig. 1-3). The choice of a sub-wavelength geometry itself means that the guided THz wave is contained both within and outside of the guide material. The extent of the energy distribution beyond the waveguide surface is largely a function of the waveguide material dielectric constant ϵ_r and the guide dimensions. Fig. 1-3 shows an example of this type of dielectric waveguide, which demonstrates the mode confinement around the guide. In addition, the inset illustrates the large bandwidth over which the guide demonstrates single-mode operation. In this case, more than 100 GHz of single-mode operating bandwidth is available from 220 to 330 GHz, covering the entire H-Band.

Due to the modal distribution exhibited by these types of guides, undesired guide-to-guide coupling can occur for parallel guide geometries. This could be particularly significant in the case of meter-range interconnects and have negative impact on the overall link performance. Undesired energy coupled from one waveguide into an ad-

jacent waveguide manifests itself as uncorrelated interference or noise, thus reducing effective SNR at the receiver. The isolation between two rectangular dielectric guides is illustrated in Fig. 1-4, following a parametric study in [113]. Tighter waveguide spacing s leads to larger amounts of undesired guide-to-guide coupling. Transmitted power P_{in} is launched in each of these waveguides, with similar spectral distribution (driven by channelization, modulation rate, and modulation type). The energy coupled from one guide into the other can be treated as uncorrelated interference by virtue of their data streams being uncorrelated. The undesired coupled power will decrease the receiver signal-to-noise plus interference ratio (SINR), reducing data rates and potentially making detection and demodulation impossible.

There are a number of strategies to ameliorate this effect if bandwidth density (i.e. bps/mm^2) is a critical metric for the application as is the case in many HPC and DC systems. For example, the use of higher dielectric constant waveguide material leads to tighter modal confinement and less guide-to-guide coupling. Another interesting strategy is to manufacture consecutive waveguides with slightly different propagation constants β for a designed operating mode. This so-called k-mismatch technique was pioneered in the integrated photonics community [71] to allow for smaller pitch between waveguides while reducing guide-to-guide coupling. It was also studied from a theoretical perspective in [40,53]. This mismatch can be achieved through a number of techniques, with the simplest being a choice of different guide cross section dimensions or different materials with slightly different dielectric constants. Another approach utilizing orthogonal modes, from $90 - 120$ GHz, has been studied in [23]. More recently, at higher frequencies, orthogonal modes were utilized in [114] to increase the usable bit rate in a rectangular dielectric waveguide.

1.2.2 Signal Sources

Historically, one of the most significant barriers to the use of THz waves for highly-scaled computing applications has been the lack of efficient high-power sources in silicon processes. In the past, efficient generation of power in this regime at the milliwatt level was relegated to III-V sources and tended to be integrated with large

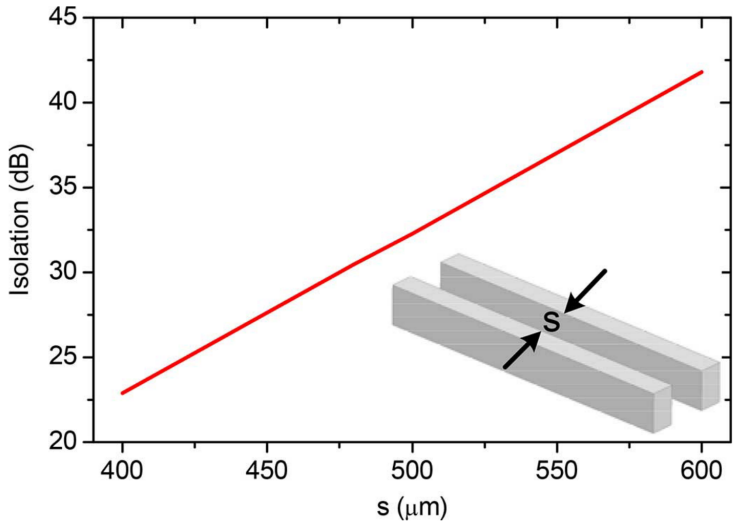


Figure 1-4: Isolation between parallel rectangular dielectric guides, with guide-to-guide spacing s, in a notional THz interconnect system (from [113]). This plot assumes a 6-mm parallel geometry with identical guide cross-sections and material. Each rectangular dielectric waveguide is modeled as a $300 \times 500\mu\text{m}^2$ guide constructed from silicon and operating around 200 GHz. From [43].

waveguide assemblies for power transport. With the increasing active device transition frequency f_T in integrated circuit technology, monolithic sources in the THz frequency range have begun to proliferate in the literature. Figure 1-5 shows a collection of recent power sources in the investigated frequency range. As one can see, there are a number of published results with milliwatt-class output powers in CMOS and SiGe processes in the $100 - 300$ GHz regime. These technologies are of particular interest as they lend themselves to direct and large scale integration with existing silicon design blocks. This provides a foundational capability to begin building progressively more complex and capable systems.

1.2.3 Wideband THz Channelization

Similar to optical fiber interconnect and the use of wavelength division multiplexing (WDM), the available single-mode bandwidth of these THz waveguides lend themselves to the use of spectrally-multiplexed data streams.

The use of novel and compact on-chip, on-interposer, or in-package filters can be

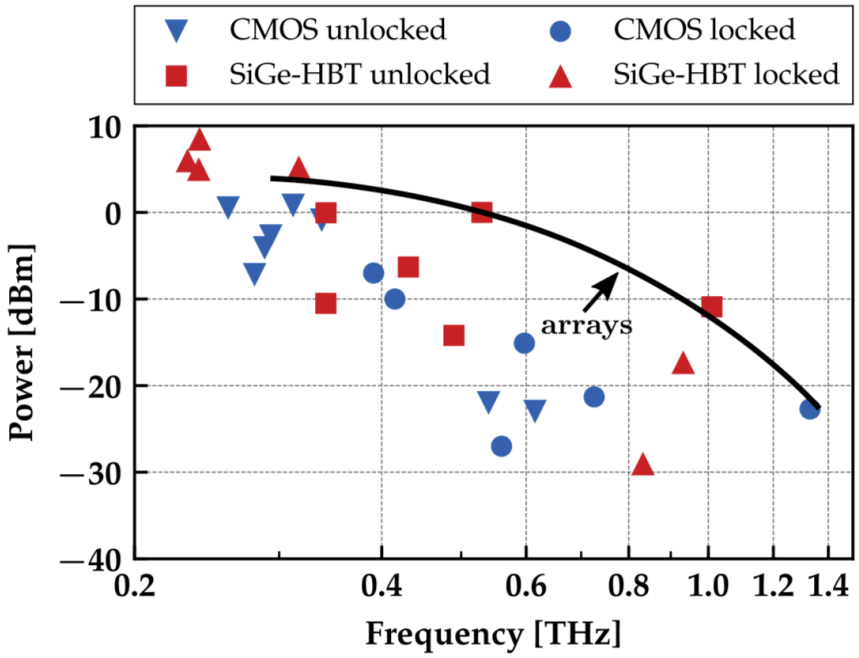


Figure 1-5: A survey of contemporary THz sources in silicon from Pfeiffer's group at the University of Wupertal [41].

considered for the implementation of physical broadband multiplexer devices. Careful performance and cost trade-offs must be considered. Realization of high channel-count microwave multiplexers is challenging [7], [64] and components with finite quality factor lead to rigid bandwidth/loss trade-offs.

Unfortunately, in the THz regime, on-chip and other planar structures suffer from poor quality factor associated with conductor, dielectric, and radiative losses. Fig. 1-6 shows an example of a compact folded quarter-wave resonator in the back-end metalization of the 130nm IHP SG13G2 BiCMOS process. Using HFSS, the resonator's first-order eigenmode can be tuned between 220 GHz and 330 GHz and realizes an unloaded quality factor Q_u of 20-30. This type of resonator is attractive because of the mixed electric and magnetic coupling that can be realized via various arrangements and is relatively compact, allowing for the efficient realization of higher-order filter [47]. Fig. 1-7 shows an implementation and the full-wave simulated response of a THz triplexer in this back-end process. In this case, quasi-elliptical channel filter responses are designed in HFSS and star-connected to form the overall channelizer

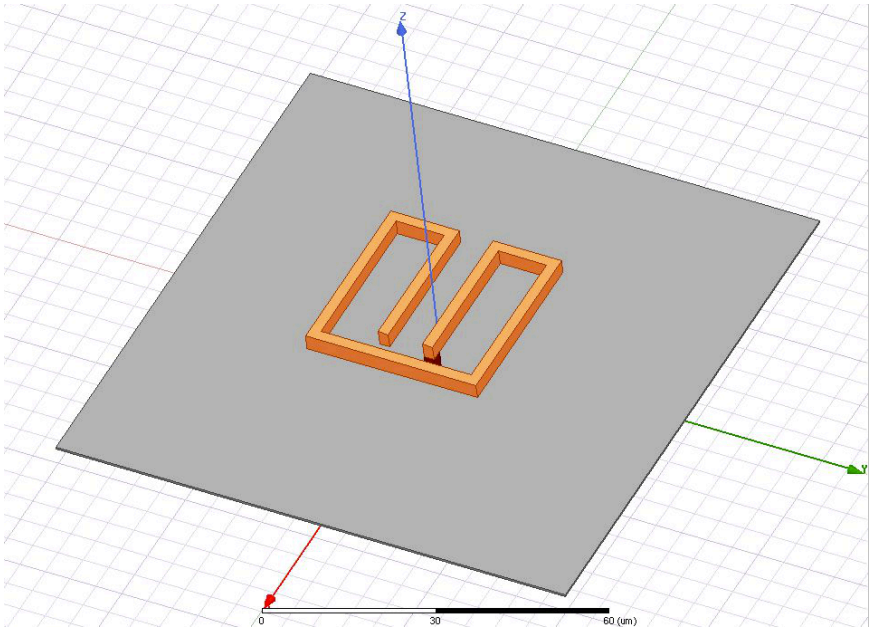


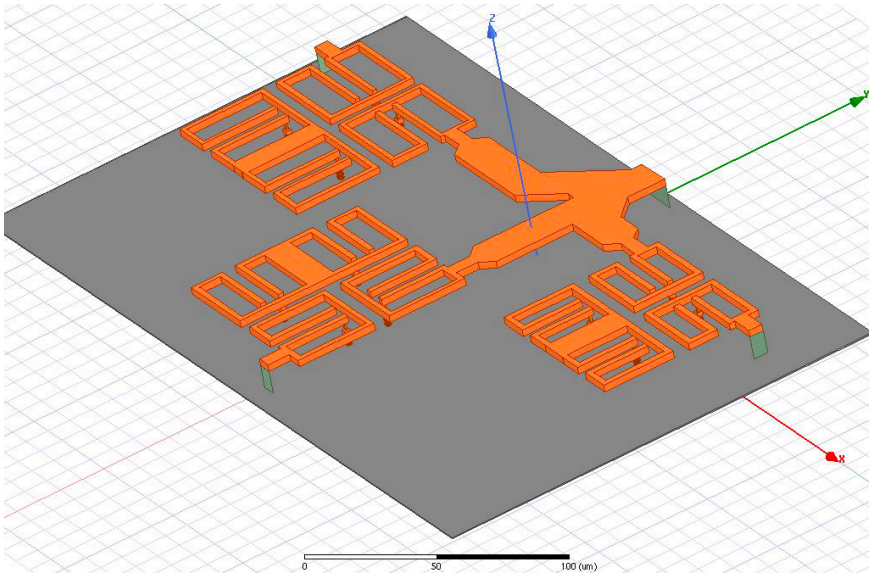
Figure 1-6: A folded microstrip quarter-wave resonator, implemented in a 130nm BiCMOS back-end of line processes provides simulated resonances from 220 GHz to 330 GHz with Q_u from 20-30. From [43].

response.

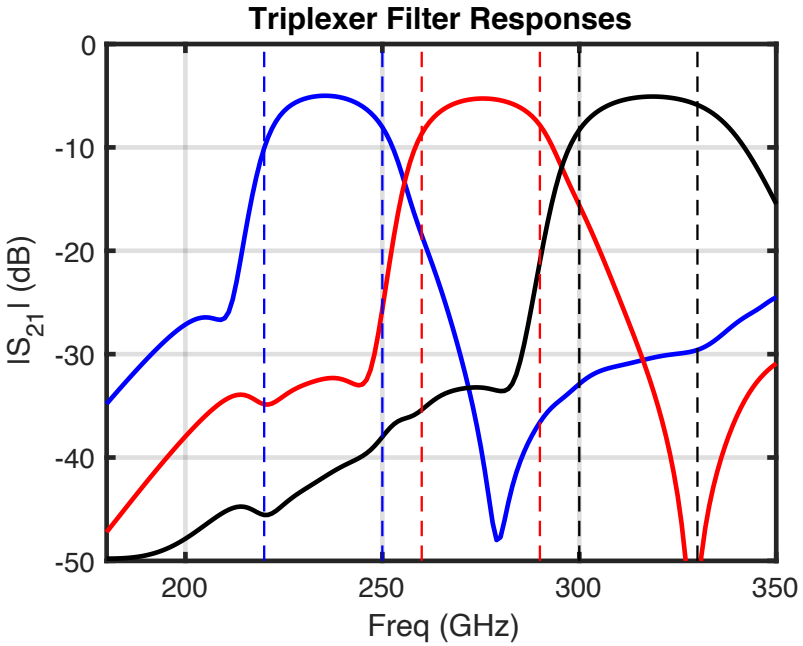
There have been a number of on-chip investigations of higher Q structures, such as substrate integrated waveguide (SIW) filters in the THz regime [93]. These structures generally produce better quality factor resonators than transmission-line based on-chip structures, but they are quite large. A number of different SIW geometries have been explored to reduce the structure's size, but they are limited by the process design rules and available metal layer thickness and spacing. In [65] a folded SIW was implemented in a 130nm CMOS process, realizing a 30% reduction in area for a TE10 waveguide.

Slow-wave structures have also been examined for the realization of on-chip THz filters. In [110], a V-Band filter was realized in a CMOS back-end, showing more than 30% size reduction over a conventional transmission-line based approach. Once again, design rules and metal fill density requirements are significant drivers of overall performance and achievable resonator and filter geometries.

The losses associated with on-chip SIW structures arising from low aspect-ratio

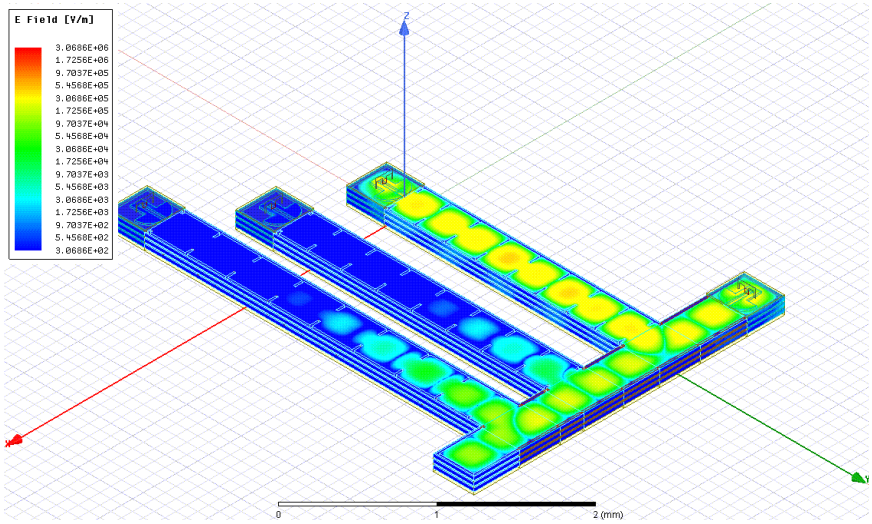


(a)



(b)

Figure 1-7: Realization of a THz triplexer operating over $220-330$ GHz, implemented in a silicon BiCMOS BEOL. (a) An HFSS model of a star-connected on-chip triplexer. (b) Full wave simulation of the overall triplexer response, assuming 50Ω source and load impedances. The dotted lines correspond to the design's desired channel filter bands. From [43].



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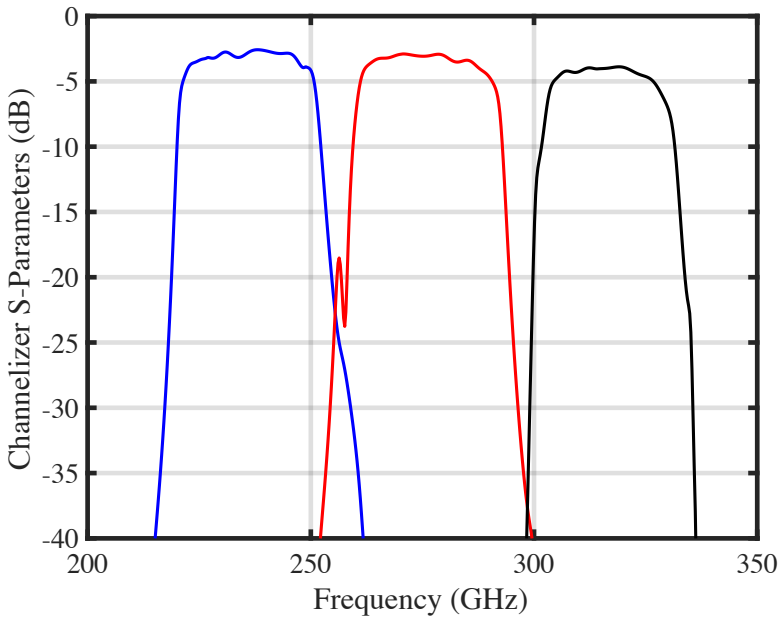


(b)

Figure 1-8: Full-wave EM simulation of a triplexer utilizing an interposer technology. The surface current density is shown at (a) the middle of the top band: 315 GHz. The triplexer transmission is shown from a broadband full-wave simulation (b). From [43].

and design rule considerations [93] tend to be higher than those realizable off-chip. Indeed, conventional off-chip, metallic waveguide-based approaches are well established and provide superior performance at these low power levels. A waveguide-based solution, however high-performance, is still quite bulky at these frequencies, where wavelengths are on the order of a millimeter. The integration of such waveguide filters into an HPC or DC application is a non-starter. Off-chip in-package filters may provide lower losses compared to their on-chip counterparts, however they suffer from the relatively large manufacturing tolerances associated with semiconductor packaging processes. In [91], a 300 GHz transition from microstrip to a low-temperature co-fired ceramic (LTCC) waveguide is demonstrated. THz filters in LTCC have been successfully demonstrated in [69] and [106]. Aside from single bandpass filters, SIW techniques have been successfully employed at lower frequencies to realize multiplexers [38]. Fig. 1-8(a) shows one potential realization of an SIW-based triplexer in the THz regime. This manifold multiplexer is implemented in an interposer technology with integrated ground-signal-ground pads. This channelizer is designed for three channels: 220-250 GHz, 260-290 GHz, and 300-330 GHz. The current density is shown for the mid-band point for the highest channel. The resultant simulated wideband S-parameters are plotted in Fig. 1-8(b). 40 dB (or better) of stop-band attenuation is achieved with less than 5 dB of mid-band insertion loss.

The trade-offs associated with realizable resonator quality factor, required structural size, designed stop-band attenuation, etc. all have direct impacts on the performance of a short-haul THz link. Section 2.1.2 discusses a number of design trade-offs associated with this critical component in the context of an on-chip channelizer and their impact on overall link performance.

1.2.4 On-Chip THz Power Couplers

The efficient coupling of power generated on-chip into and out of the THz waveguide at the transmitter and receiver respectively, is of critical importance. Unlike power couplers in the optical domain, where multi-wavelength adiabatic tapers can achieve sub-dB coupling efficiencies, THz-regime power couplers are required to be

Ref.	Freq. (GHz)	Guide Cross-Section	Coupling Geometry	Guide Loss (dB*)	Coupling Loss (dB)
[46]	220-300	Rectangular	Planar On-Chip	50	4.8
[114]	130-210	Rectangular	Orthogonal Off-Chip	40	6.5
[66]	90-220	Rectangular	Planar Off-Chip	<100	2.2-3.3
[113]	210	Rectangular	Orthogonal On-Chip	100.6	3.6
[20]	60, 100	Rectangular	Metallic Waveguide	8.7	-
[42]	100-600	Rectangular	Metallic Waveguide	<2-19	-
[112]	140-190	Rectangular with Taper	Planar Off-Chip	14	0.44-1.5
[25]	80-100	Rectangular	Planar On-Chip	65.8	0.46
[97]	120	Round Hollow	Orthogonal On-Chip	5.5	12
*The published results were normalized to a 1-meter link to include losses from waveguide bends associated with the coupling geometry.					

Table 1.1: A Survey of Measured THz waveguide Geometries and Coupling Schemes.

sub-wavelength in size. Larger, more efficient, coupling devices would require excessive chip or interposer area and become cost-prohibitive or complicate integration. As discussed in [46], traditionally on-chip power couplers at these frequencies have been forced into a number of design trade-offs associated with bandwidth and efficiency. Moving the coupling structures themselves off-chip alleviates this issue (Fig. 1-9(a) and (b)), but it comes at the cost of additional loss to route the THz wave on/off chip, as well as additional packaging complexity – itself tied to cost. Other approaches require the thinning of the high permittivity bulk silicon behind the coupling structure to reduce the undesired coupling of the modulated THz wave into bulk modes. This approach is also costly, requiring significant post-processing. A third approach is the use of very high permittivity waveguide materials, such as machined silicon [34], which has a number of advantages, in terms of tight mode confinement (Fig. 1-9(c)). This lends itself to efficient coupling with low cross talk between lanes, but the manufacturing required for large-scale integration is challenging. Additionally, significant

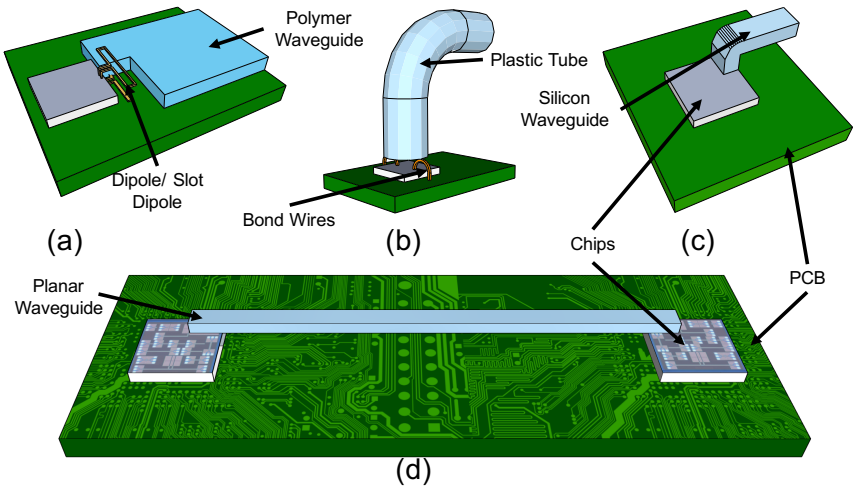


Figure 1-9: Several concepts for the physical interface between a THz waveguide and the on-chip transceiver (from [46]). An off-chip aperture excites the electromagnetic wave in (a). In (b), the on-chip radiation inefficiencies are addressed through the use of bond-wire antennas, radiating into a circular waveguide. A high-permittivity machined silicon waveguide and an on-chip aperture are shown in (c). An on-chip aperture launching a broadband wave into a rectangular THz waveguide is shown in (d).

challenges are associated with the packaging required to support a number of the existing schemes for physically interfacing the electromagnetic coupling structures with the waveguides themselves. These concepts are of the utmost importance when considering a scheme for large-scale integration into HPC, DC, and other planar applications (such as backplanes, etc.). Table 1.1 lists a number of different waveguide geometries, coupling approaches, and measured guide performance from a variety of sources above 100 GHz. The measured or estimated guide losses are normalized to 1-meter and the coupling losses listed are per coupler.

In [46] a broadband travelling wave structure is integrated in a BiCMOS back end of line (BEOL) to produce broadband, low-loss coupling into a rectangular polymer waveguide (Fig. 1-9(d)). An example of the measured structures and the waveguide placement, directly on the chip passivation layer, is shown in Fig. 1-11(a). In this case, a coupling loss of less than 5 dB per coupler, after de-embedding waveguide losses, was measured in H-Band (Fig. 1-11(b)). In addition, the transmission phase response, normalized to the waveguide length, is shown in Fig. 1-11(c).

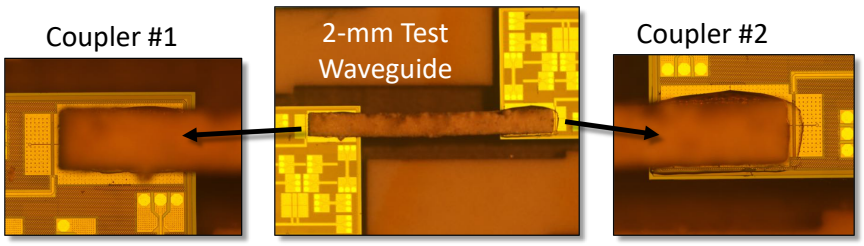
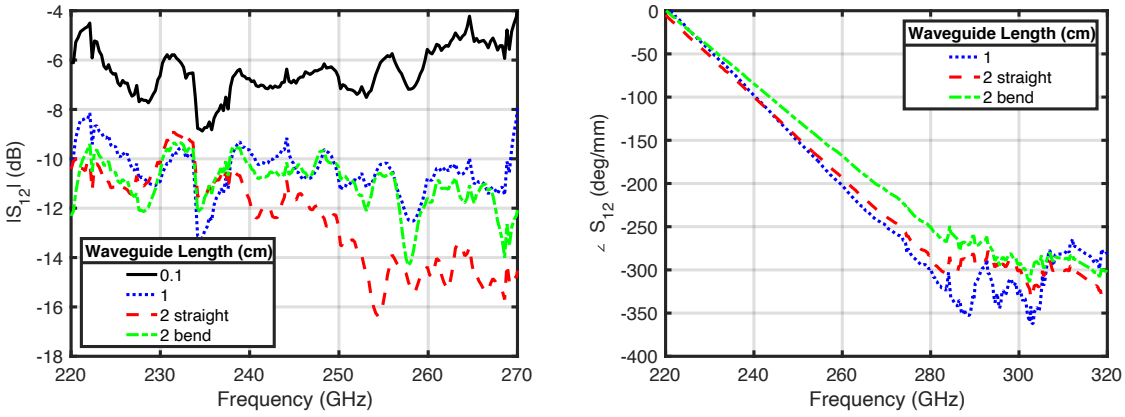


Figure 1-10: Chip and waveguide-placement photos in which the rectangular dielectric waveguide is directly bonded to the chip passivation layer above the coupler structure. From [46].



(a) (b)

Figure 1-11: (a) Measured transmission magnitude, and (b) phase response of a broadband on-chip THz power coupler and rectangular dielectric waveguide from [46].

Ref.	Freq. (GHz)	Aggregate Data Rate (Gb/s)	Link Len. (m)	Efficiency (pJ/b/m)	Notes
[97, 100]	120	12.7	1	1.8	
[99]	120	6.2	8	1.2	Full Duplex
[111]	165	9.4	0.023	29.56	

Table 1.2: Integrated THz Links Utilizing Dielectric Waveguides

These integration concepts have a variety of system-level impacts, from waveguide and coupling losses to packaging considerations. Ultimately, tradeoffs associated with system cost, performance, and application will have to be made to determine the appropriate solution. For example, the use of entirely planar coupling geometries with rectangular waveguides might be considered for meter-class THz backplanes. Board-to-board interfaces may be better served via orthogonal coupling interfaces utilize rectangular or circular waveguides. These choices will impact achievable lane data rates, data efficiency, lane-to-lane pitch (and associated aggregate data rates), and overall system cost.

1.3 Previous Full-Link Demonstrations

With the proliferation of available couplers and waveguides, as well as a variety of higher-frequency silicon sources and circuits, there have been a number of recent demonstrations of full end-to-end links (Table 1.2). These have focused on single-channel transmit/receive or full-duplex architectures. Independent channel aggregation has been demonstrated through the use of orthogonal guided modes. To date, the authors are unaware of any published integrated THz links making use of multiple-carrier RF channels aggregated and transmitted over a dielectric channel as depicted in Fig. 1-2. However, the links that have been demonstrated push critical metrics, such as energy efficiency and realizable link lengths at THz frequencies. These demonstrations serve to show the tenability of the concept.

1.4 Research Contributions

This link concept, in addition to architectural trades, was published in the following invited article:

- **J. W. Holloway**, G. C. Dogiamis, and R. Han, "Innovations in Terahertz Interconnects: High-Speed Data Transport Over Fully Electrical Terahertz Waveguide Links," *IEEE Microw. Mag.*, vol. 21, no. 1, pp. 35–50, Jan. 2020.

Initial designs, analysis, and measurements of the first broadband, planar sub-THz power coupler was published as:

- **J.W. Holloway**, L. Boglione, T.M. Hancock, and R. Han, "A Fully Integrated Broadband Sub-mmWave Chip-to-Chip Interconnect," *IEEE Transactions on Microwave Theory and Techniques*, 65(7), 2017.

Additional coupler information has been published in:

- A. Aleksov, G. Dogiamis, T. Kamgaing, A. Elsherbini, J. Swan, K. Darmawikarta, S. Boyapati and **J. Holloway**, R. Han, "Organic Package Substrates Using Lithographic Via Technology for RF to THz Applications," in *Technical Digest - International Electron Devices Meeting, IEDM,* 2020.

Wideband multiplexer work was published in:

- **J. W. Holloway**, G. C. Dogiamis, S. Shin, and R. Han, "220-to-330-GHz manifold triplexer with wide stopband utilizing ridged substrate integrated waveguides," *IEEE Trans. Microw. Theory Tech.*, vol. 68, no. 8, pp. 3428–3438, 2020.

A successful end-to-end link demonstrator and constituent components have been published in:

- **J. W. Holloway**, G. C. Dogiamis, and R. Han, "A 105Gb/s Dielectric-Waveguide Link in 130nm BiCMOS Using Channelized 220-to-335GHz Signal and Integrated Waveguide Coupler," in *IEEE International Solid-State Circuits Conference*, 2021, p. *Accepted.*

Portions of the presented work has also been published in the following:

- R. Han, **J. Holloway** et al., "On-chip terahertz electronics: From device-electromagnetic integration to energy-efficient, large-scale microsystems," in *Technical Digest - International Electron Devices Meeting, IEDM,* 2017.
- R. Han, **J. Holloway** et al., "Filling the Gap: Silicon Terahertz Integrated Circuits Offer Our Best Bet," *IEEE Microw. Mag.*, vol. 20, no. 4, pp. 80–93, Apr. 2019.

1.5 Thesis Organization

The remainder of this thesis is organized around an analysis of the proposed link architecture (Chapter 2); design, simulation, and measurements of key broadband power couplers (Chapter 3) and sub-THz multiplexers (Chapter 4); and an end-to-end link demonstrator (Chapter 5). Lastly, the document concludes (Chapter 6) with a review of research contributions and a discussion of follow-on research areas. Two appendices provide background on the employed wideband sub-THz electromagnetic modeling techniques (Appendix A) and techniques associated with physical assembly of the final link (Appendix B).

Chapter 2

Sub-THz Link Architecture

2.1 THz Interconnect Architectural Trade-Offs

2.1.1 Canonical Architectural Concept

Given the large single-mode waveguide bandwidths available in the THz regime and the achievable operating bandwidths available in modern silicon nodes, a parallel channelization scheme is considered as a candidate for aggregate high-data rate digital communication. Due to the large channel bandwidths and challenges associated with realizing gain at these frequencies in existing silicon processes, microwave multiplexers or channelizers are used to present constant impedances across the up-conversion modulators' output bands. The channelizer ensures out-of-channel suppression, and provide channel-to-channel isolation. This architecture also enables the choice of different modulation schemes, if appropriate, within each analog channel based on the channel's operating conditions. Various architectural trades can be made regarding the design and implementation of these channelizers. Subsections 2.1.2 and 2.1.3 focus on the impacts of various channelizer performance parameters on overall lane capacity as well as link efficiency. In this example, we assume N channels, each with a 3-dB bandwidth of Δf within the total available transmission channel bandwidth BW_{WG} (Fig. 2-1). The latter is determined by the transmission material properties, the modal characteristics of the waveguide, and the response of the structures used

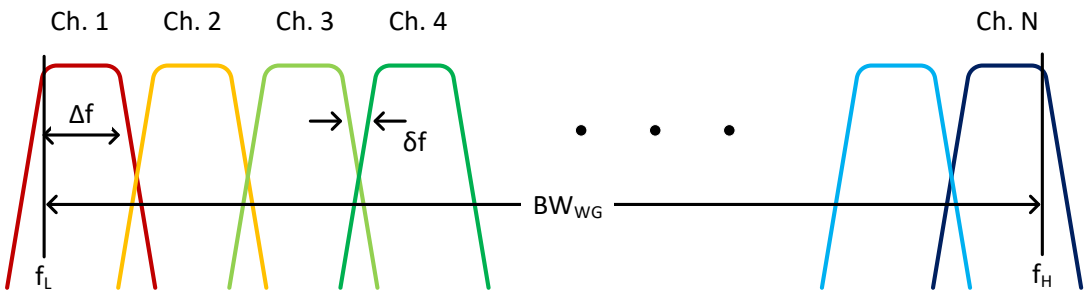


Figure 2-1: Generalized channel structure on a single waveguide. From [43].

to couple energy between the waveguide and the on-chip structures and circuits.

Quantifying the performance of such a system can be achieved by examining a number of metrics, such as consumed energy per transmitted bit, aggregated across all the channels on a given waveguide or lane. Other metrics of relevance include latency, a targeted bit-error-rate (BER), active area required to implement such a scheme, maximum achievable bit rate per lineal length, maximum achievable bit rate per waveguide cross-sectional area, or total cost per Gbps. Here, we concentrate on the energy per bit and aggregated data rate per waveguide required for this type of architecture given various component performance trades and current trends in silicon circuit performance.

2.1.2 Link Budget Calculation

Given the canonical multi-channel architecture, we begin by modeling the available signal-to-noise ratio at each channel receiver. In addition, due to the finite order of the multiplexer channel filters we define the channel separation, consisting of guard bands of width δf to ensure band-to-band isolation and ease of realization of the multiplexer design. Ideally, one would prefer to realize a channelizer that provides little insertion loss, has very high stop-band attenuation, and minimizes the channel separation to provide the highest utilization of available aggregate waveguide bandwidth BW_{WG}.

To quantify the overall system-level performance trade-offs associated with these parameters, we have modeled the impacts of Δf, δf, and desired channel filter stop-

band attenuation A_s on the overall system performance, as it relates to total aggregate channel capacity and estimated energy per bit. To do this, we first consider a potential channel filter response: a Type-II Chebyshev response since it provides excellent selectivity compared with other types of filter responses of a given order n and also provides a convenient set of closed-form expressions [68].

The design equations for estimating filter order based on these parameters is well known [78]. Utilizing an estimate of the filter order and the lumped filter prototype values (using [68]), and the assumed resonator Q_u, one can estimate the resultant channel filter insertion loss L_0 [13, 14].

To achieve a Type-I or Type-II Chebyshev response with desired minimum stopband attenuation A_s and passband ripple A_p, one can estimate the required order n of the filter [78]:

$$n = \left\lceil \frac{\cosh^{-1}\left\{\sqrt{10^{A_s/10}-1}/\sqrt{10^{A_p/10}-1}\right\}}{\cosh^{-1}\left(f_s/f_p\right)} \right\rceil , \tag{2.1}$$

where A_s and A_p are in dB and f_s and f_p are the bandpass filter stopband bandwidth and passband bandwidth, respectively. From the value of n, one can calculate the prototype filter parameters using analysis available in [68]. These formulas have been reproduced here for convenience.

$$\beta = \ln\left(\coth\left(\frac{A_p}{17.37}\right)\right),$$

$$\gamma = \sinh\left(\frac{\beta}{2n}\right),$$

$$a_k = \sin\left(\frac{(2k-1)\,\pi}{2n}\right),\ \mathrm{k} \in \{1, 2, \ldots n\},$$

and

$$b_k = \gamma^2 + \sin^2\left(\frac{k\pi}{n}\right),\ \mathrm{k} \in \{1, 2, \ldots n\}.$$

The expressions are used to recursively calculate the filter prototype values, g_i as

$$g_1 = \frac{2a_1}{\gamma}, \qquad g_k = \frac{4a_{k-1} \cdot a_k}{b_{k_1} \cdot g_{k-1}}, \ \mathrm{k} \in \ \{2, 3 \ ... \ n\}$$
$$g_{n+1} = 1.00, \text{for } n \text{ odd} \quad g_{n+1} = \coth^2\left(\frac{\beta}{4}\right), \text{ for } n \text{ even.}$$

Given the prototype filter values g_i for a given filter order n and the finite resonator unloaded quality factor Q_u available to realize individual channel filters, we can estimate the pass band filter loss L_0 [13, 14] as

$$L_0 \approx 4.343 \frac{f_1^{'}}{f} \sum_{i=1}^{n} \frac{g_i}{Q_{ui}} \text{ [dB]}. \tag{2.2}$$

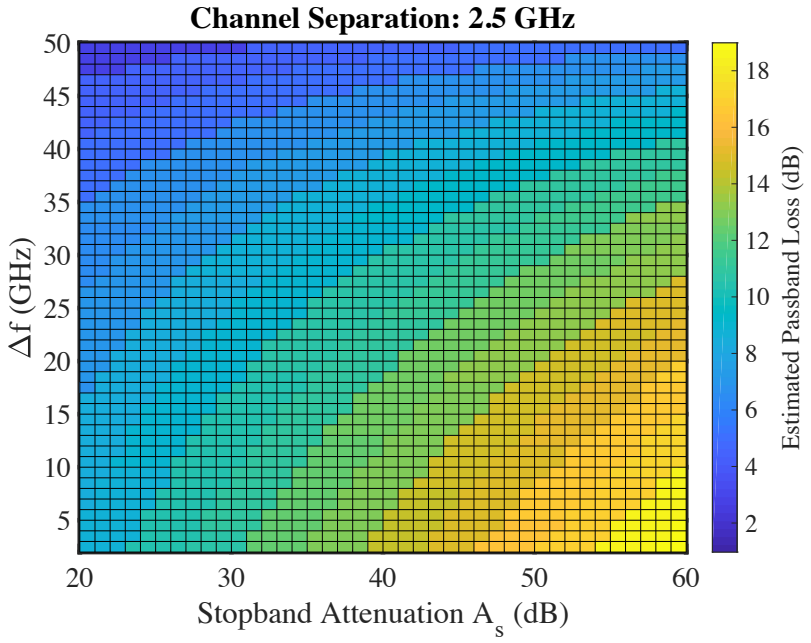
In this case we have made the assumption that the resonators' $Q_{ui} = Q_u$. The ratio $f_1^{'}/f$ is a frequency transform from a normalized low-pass filter prototype to a bandpass filter and vary based on the fractional bandwidth of the filter [13, 14].

Based on the H-band operating frequencies available in the polymer waveguide under investigation mid-band insertion loss of channel filter as a function of channel bandwidth Δf, desired stop-band attenuation A_s, and channel separation δf. Utilizing a nominal Q_u of 20, based on an electromagnetic study of available sub-wavelength resonators realized in the back-end of a commercially-available 130nm SiGe BiCMOS process (see Section 1.2.3), the varying levels of passband insertion loss can be seen in Fig. 2-2.

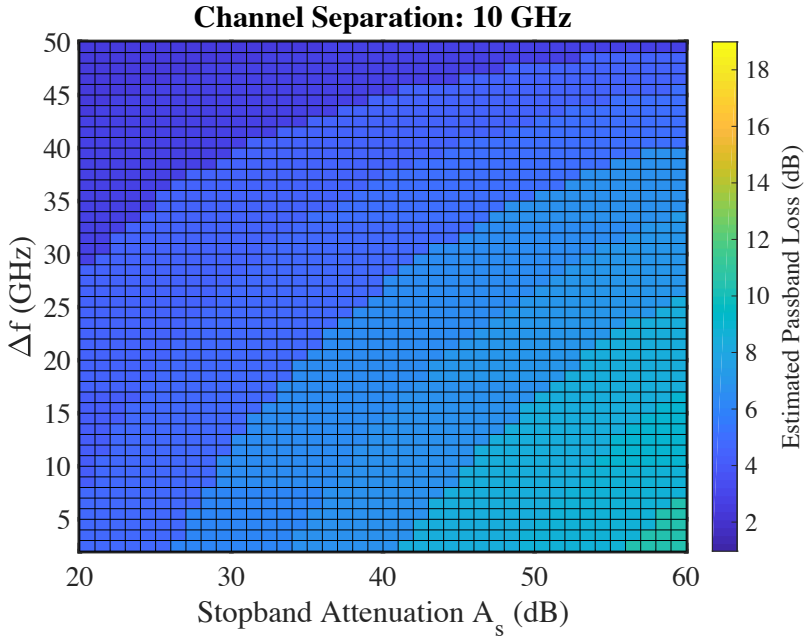
One can see that given a specified Δf and A_s, changes in the channel separation δf have significant impacts on the insertion loss through each channel filter. This will necessarily impact available signal-to-noise ratio at the receiver and thus impact that specific channel's available Shannon capacity

$$C \propto \Delta f \cdot \log_2\left(1 + \frac{S}{N}\right). \tag{2.3}$$

Decreasing the channel separation provides a larger total aggregate number of channels and use of the available transmission bandwidth BW_{WG}, but for a given filter order number n, this leads to an increase in channel filter loss or an undesired re-



(a)



(b)

Figure 2-2: Estimated passband insertion loss for two different channel separations; (a) $\delta f = 2.5$ GHz and (b) $\delta f = 10$ GHz . From [43].

duction in stopband attenuation for the same given passband insertion loss. This stopband attenuation is a concern as the adjacent channel energy is uncorrelated and will increase the in-band SINR, and thus reduce the channel capacity. Increasing the order of the filter is one option, assuming the increase in stopband attenuation is much larger than the associated passband insertion loss, but one would strive to reduce the order of a given channel filter if cost or size constraints were a concern. Alternatively, one might choose larger Δf channel sizes. This is an attractive solution, but a realistic implementation will suffer from the difficulty in realizing sufficiently wide-band components capable of modulating, demodulating, and amplifying such large baseband bandwidths.

We select a nominal digital modulation scheme to help in analyzing these trade-offs. In this case, we will carry out the following analysis utilizing a vestigial-sideband (VSB) BPSK modulation. This scheme is chosen for its simplicity and the relative ease of transmitter realization at these sub-mmWave frequencies, as well the format's spectral efficiency.

For a given modulation rate

$$\frac{1}{T} = \Delta f$$

and a given transmitter power P, we make use of the modulated signal power spectral density

$$S(f, f_{c,n}) \;=\; \frac{P \cdot T}{2} \left[\mathrm{sinc}^2\left(\left(f - f_{c,n}\right) T \cdot \pi\right) + \mathrm{sinc}^2\left(\left(f + f_{c,n}\right) T \cdot \pi\right)\right] \;\; [\mathrm{W/Hz}] \quad (2.4)$$

at some carrier $f_{c,n}$ for each independent channel n. It should be noted that other modulation schemes can just as easily be utilized by the insertion of the appropriate $S(f, f_{c_n})$.

Fig. 2-3 depicts a schematic of the spectral plan being analyzed in this paper based on the link architecture of Fig. 1-2. The parallel transmitter PSDs are shown, along with a representation of the idealized multiplexer response. In the upper-right corner, a graph illustrates the impact of finite filter roll-off and stop-band attenuation on in-band performance.

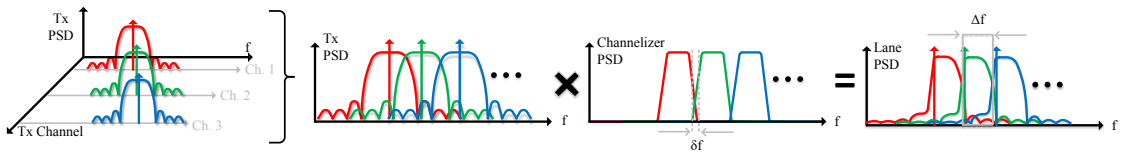


Figure 2-3: The VSB THz interconnect spectral plan being analyzed. Parallel double-sideband BPSK modulation occurs across N channels, undergoes filtering (via multiplexer channel filters) to suppress the modulated lower sideband, and multiplexes independent channels onto a single waveguide. From [43].

Assuming consistent modulation rates, modulation types, channel spacing, channel filter design specifications, and channel transmitter powers, using the PSD (2.4) we can estimate the in-band correlated signal power and the uncorrelated interference power from adjacent channels. A first-order approximation of the available desired signal power in the n-th passband can be written as

$$P_{signal} \approx 10^{-L_{pb}/10} \int_{f_{c,n}}^{f_{c,n}+\Delta f} S(f, f_{c,n}) df \text{ [W]}$$

for the total loss in the passband through the multiplexer and channel as

$$L_{pb} = 2A_P + L_{ch} \text{ [dB]}$$

with the coupler and channel loss combined in

$$L_{ch} = 2L_{cpl} + L_{WG} \text{ [dB]}.$$

Similarly, we approximate the uncorrelated interference power from the $(n-1)$ lower band present in the band of interest as

$$P_{intLB} \approx 10^{-L_{sb}/10} \int_{f_{c,n-1}+\Delta f+\delta f}^{f_{c,n-1}+2\Delta f+\delta f} S(f, f_{c,n-1}) df \text{ [W]}$$

with the out-of-band attenuation (assuming a symmetric channel filter response) of

$$L_{sb} = A_s + A_P + L_{ch} \text{ [dB]}.$$

Lastly, we account for the undesired lower or vestigial sideband energy present in the n-th band of interest from the $(n+1)$-th band as

$$P_{intUB} \approx 10^{-L_{sb}/10} \int_{f_{c,n+1}+\delta f}^{f_{c,n+1}+\Delta f+\delta f} S(f, f_{c,n+1}) df \text{ [W]}.$$

We note that no special treatment is given to the first and last channels; they will encounter less undesired out-of-band interference energy. This *improvement* in the signal-to-interference level is not modeled. As a result, we expect the link performance to perform slightly better, in aggregate, that this model predicts. The total interference in the n-th band can be approximated as

$$P_{int} \approx P_{intUP} + P_{intLB} \text{ [W]}.$$

In addition, the individual receiver implementation will exhibit a noise floor

$$P_{N-rx} = -204 \text{ dBW/Hz} + 10 \cdot \log_{10} \Delta f + NF_{rx} \text{ [dBW]}$$

due to the noise equivalent bandwidth and the receiver finite noise figure NF_{rx}. The signal-to-noise plus interference is written as

$$SINR = \frac{P_{signal}}{P_{int} + P_{N-rx}}. \tag{2.5}$$

Equation 2.5 can be used to perform a parametric analysis on the SINR impact of various channel filter performance metrics and guard band spacings. Similarly, this type of system-level model can used with any other type of modulation through a simple substitution for the appropriate PSD $S(f)$.

Fig. 2-4 shows the estimated SINR as parameterized over various values of A_s, Δf, and δf of a single channel, given a 1 mW source that encounters 10 dB of conversion loss through the THz modulators. The losses associated with the wideband coupler is 5 dB [46]. We assume 5 dB of total loss in the waveguide medium. The receiver performance is modeled with a 20 dB noise figure and a 10 dB conversion loss.

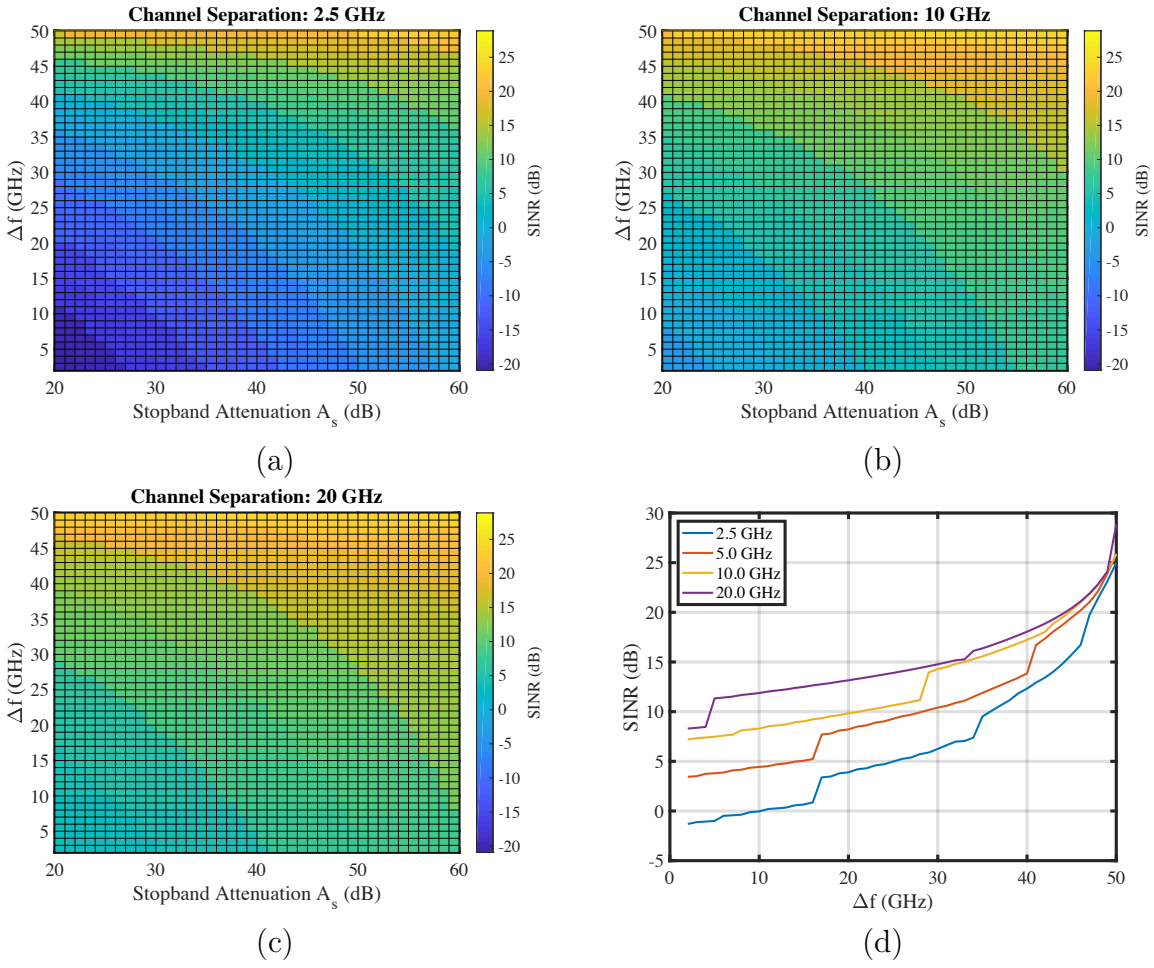


Figure 2-4: SINR estimates vs. channel bandwidth and channel filter stop-band attenuation for a VSB BPSK-modulated THz carrier with (a) 2.5 GHz, (b) 10 GHz, and (c) 20 GHz channel-channel separation. The best SINR estimate available for a given Δf for a variety of δf values is shown in (d). The discontinuities in (d) are associated with steps in the filter order n required to meet a given A_s specification. From [43].

One can see that the SINR improves, in general, for a given channel bandwidth Δf as the stop-band attenuation increases. Similarly, we see that larger channel-to-channel spacing also improves the channel SINR, but this comes at the cost of unused spectrum on a given waveguide. Similarly, an increase in the stop-band attenuation for a given δf and Δf is associated with an increase in the filter order, size, and cost. This growth in filter size could potentially limit the available number of lanes one could implement on a given area. Note that the size or resonators are on the order of the carrier wavelength (around 1 mm at these frequencies) and their number is proportional to filter order n.

Given the energy outside of the first Nyquist band for this type of modulation (Fig. 2-1), the idealized flat stop-band response, and the large equivalent noise bandwidth contribution to the overall receiver noise floor, we expect the noise floor to be dominated by the channel equivalent noise bandwidth. Given other types of modulation, other filter implementations, or even changes in available component quality factor, these trends can change.

2.1.3 Aggregate Lane Data Rate and Energy-per-Bit

Our ultimate goal is maximizing the bandwidth density, for a given waveguide, while minimizing the energy required to modulate, transport and demodulate the data. We build upon the SINR analysis presented in the previous section, which was illustrated in Fig. 2-4. For a given available lane bandwidth BW_{WG}, channel-to-channel guard bandwidth δf, and a channel bandwidth Δf the number of available channels per lane is

$$N = \left[\frac{BW_{WG} + \delta f}{\Delta f + \delta f} \right].$$

Given the available channel capacity (2.3), number of channels per lane N, and the channel SINR (2.5) we can calculate the total aggregate lane capacity

$$C_{WG} \propto N \cdot \Delta f \cdot \log_2 (1 + SINR), \tag{2.6}$$

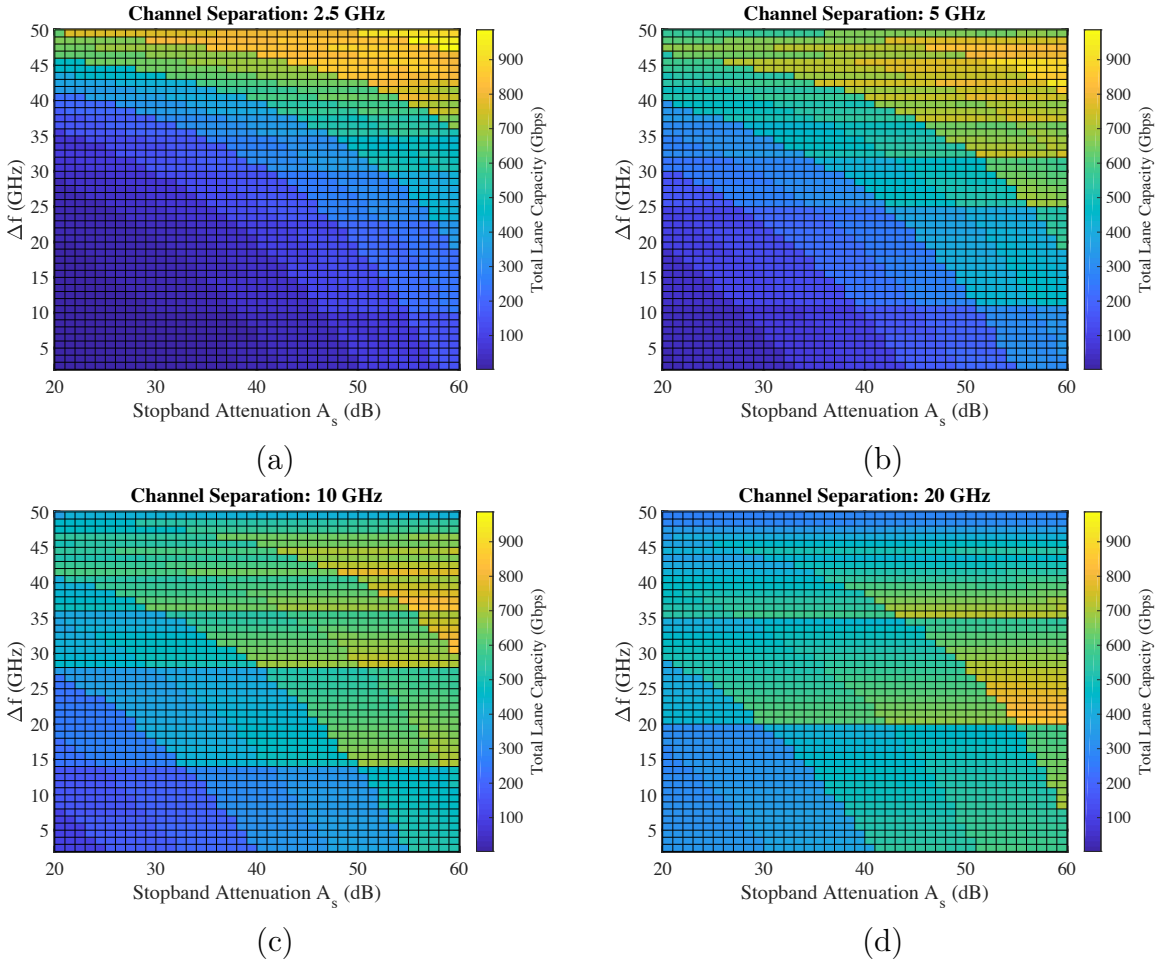


Figure 2-5: Aggregate Shannon channel capacity per waveguide for (a) 2.5 GHz, (b) 5 GHz, (c) 10 GHz, and (d) 20 GHz channel spacing. This analysis assume $BW_{WG} = 110$ GHz of contiguous, single-mode waveguide bandwidth. Some higher-order modulation schemes are assumed to approach the channel Shannon capacity, with total system DC-RF efficiency of 2.5%. From [43].

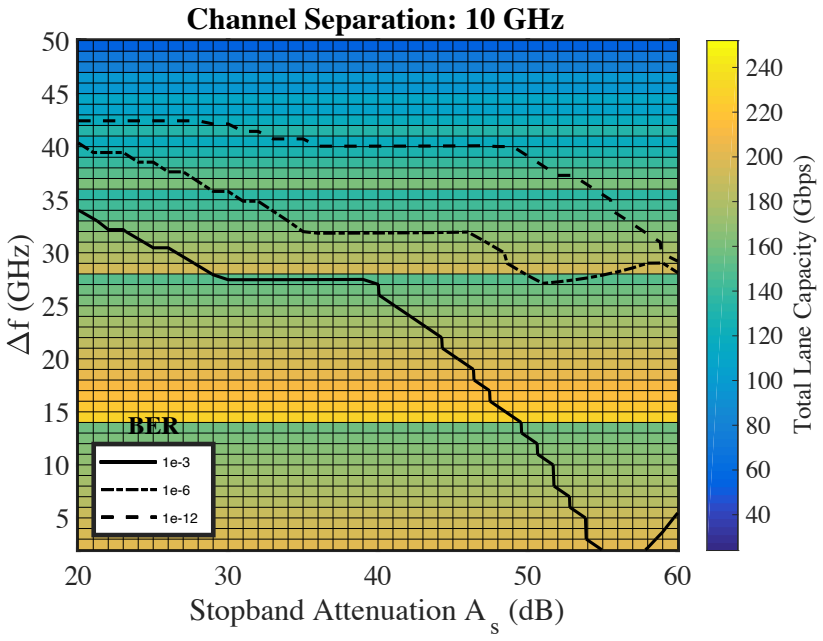
presented in Fig. 2-5. In this analysis, one might select an architecture that maximizes the available channel bandwidth Δf, utilizing a diplexer to provide the channelization with large stop-band attenuation. There is little published work on monolithically-integrated silicon-based modulators capable of achieving those types of modulation bandwidths ($>$ 50GHz) in the G- or H-Bands ($140 - 330$ GHz). In addition, selecting smaller channel separation (Fig. 2-5(a)) requires a more stringent out-of-band channel filter attenuation to reduce the in-band SINR. As discussed previously, this leads to an increase in system complexity, size, and cost.

Furthermore, scaling the baseband rate Δf comes with a commensurate increase

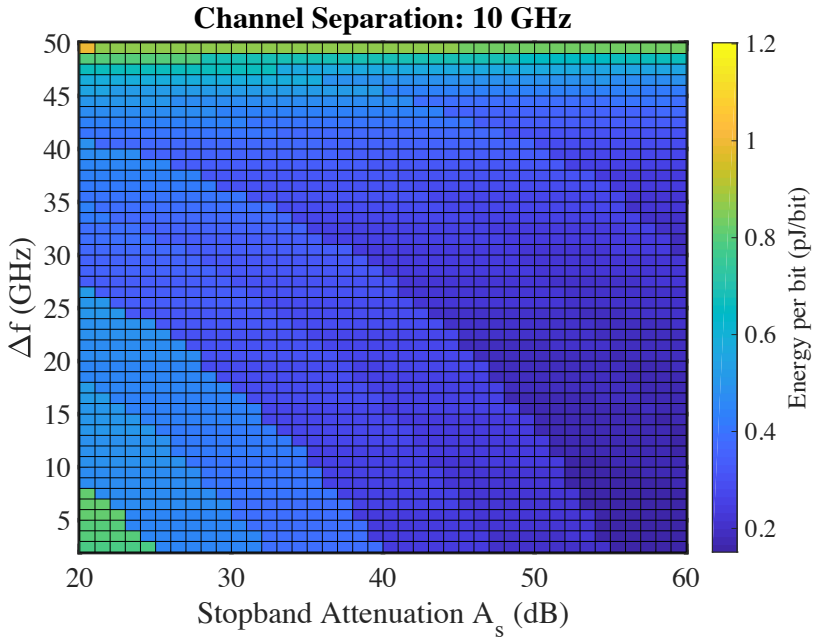
in the power requirements for a variety of baseband components (amplifiers, etc.). This bandwidth-power trade off in transmitter modulator and baseband circuitry is not included in this analysis. Given analytical models, one would see a diminishing advantage as the channel bandwidth increases. Similarly, the impacts of dispersion related to both the lane waveguide as well as the multiplexer filter shape and order, the subsequent equalization requirements, and the related power overhead is also not modeled here.

We again consider the specific case of the VSB BPSK modulation described in Section 2.1.2 and impose a specific BER requirement. The channel capacity can then be defined as above for a given SINR to provide that required BER. For the case of a 10 GHz channel separation, the aggregate channel capacity, given BPSK modulation, is shown in Fig. 2-6(a). Given this modulation, the modeled achievable lane capacity, assuming a minimum SINR, is primarily defined by the available channel bandwidth. Therefore, we expect relatively flat capacity dependence on the channel bandwidth Δf. In Fig. 2-6(a), the discrete steps corresponding to changes in lane capacity are due to changes in required filter order to meet the given fractional bandwidth requirements of a given Δf. The BER figures, however, are strongly tied to the in-channel SINR figures. One can see the relationship between an *increase in designed stop-band attenuation* at a given channel bandwidth and the subsequent *improvement in BER*. In this case, realizable on-chip or interposer-based multiplexers might drive one to stop-band attenuation specifications on the order of 40 dB. In this case, to meet the given BER rate, one would choose channel bandwidths on the order of 30 GHz to maximize the available aggregate lane data rate.

Recall that we are concerned with not only aggregate data rate per lane but also the energy per bit required to transmit and receive the data. Assuming a 2.5% DC-RF efficiency for baseband circuitry, carrier generation, modulation, and down-conversion (carrier generation being the largest contributor to overall link efficiency), we can estimate the energy per bit (Fig. 2-6(b)) for the maximum throughput case (assuming Shannon capacity). In this case, as well, one can see that the optimal energy per bit occurs at $\Delta f \approx 30$ GHz with around 40 dB of stop-band attenuation.



(a)



(b)

Figure 2-6: (a) Aggregate lane channel capacity for a VSB BPSK-modulated set of carriers with a 10 GHz channel separation. The three iso-contours correspond to bit error rates of 10^{-3}, 10^{-6}, and 10^{-12} (the bottom, middle, and top contours, respectively). Regions above these contours provide sufficient SINR to achieve BERs better than these values. Regions below these lines will generate higher BERs. In this case, a 5% DC-RF efficiency is assumed due to the simple nature of the modulation scheme. (b) Estimated energy-per-bit (Shannon capacity) with a 10 GHz channel separation. This estimate assume high-order modulation; with the added complexity, a 2.5% DC-RF efficiency is assumed. From [43].

2.2 Full-Link Simulation Results

Utilizing the analysis of the notional architecture in Fig. 1-2 discussed in Section 2.1, a simulation was carried out to verify the above analysis. A 10 cm rectangular dielectric waveguide made from Rogers R3003^{TM} PCB material and utilizing a broadband power coupler based on the work in [46] were utilized for the channel. A three channel architecture was chosen with Δf=30 GHz channel bandwidths and δf=10 GHz guard bands. A coherent VSB modulation scheme was utilized with baseband raised-root cosine ISI filtering. EM-circuit models, based on a commercially-available BiCMOS technology, of sub-harmonic mixers were used for phase modulation and heterodyne detection. Similarly, baseband circuitry and LO generation were simulated using EM-circuit models. The individual transmit chains were driven with independent (uncorrelated) 30 Gbps Pseudo-Random Bit Sequences (PRBS) of length 2^{15}. The simulation makes no use of additional receiver baseband amplification. In addition, the simulation utilizes neither baseband pre-emphasis nor receiver equalization. Cursory examination shows eye opening improvements with the use of simple single-tap baseband pre-emphasis or analog feed-forward equalization. As can be seen in Fig. 2-7, the eye opening is sufficient to close the link without the use of additional equalization techniques at an aggregate lane rate of 90 Gbps over the three indepdent channels. The middle channel, which one expects to be the most susceptible to interference from adjacent channel interference, is shown in the plot. Without equalization, eye openings larger than 2 mV can be seen.

2.3 Review of THz Interconnect Tradeoffs

It should be noted that this analysis is highly dependent on a number of application-specific factors and design choices. First, the waveguide (or channel) losses are largely a function of material properties and waveguide geometry. Cost, manufacturability, integration scheme, guide-to-guide coupling, and chromatic dispersion should all be considered. These considerations will drive the link attenuation as well as provide a

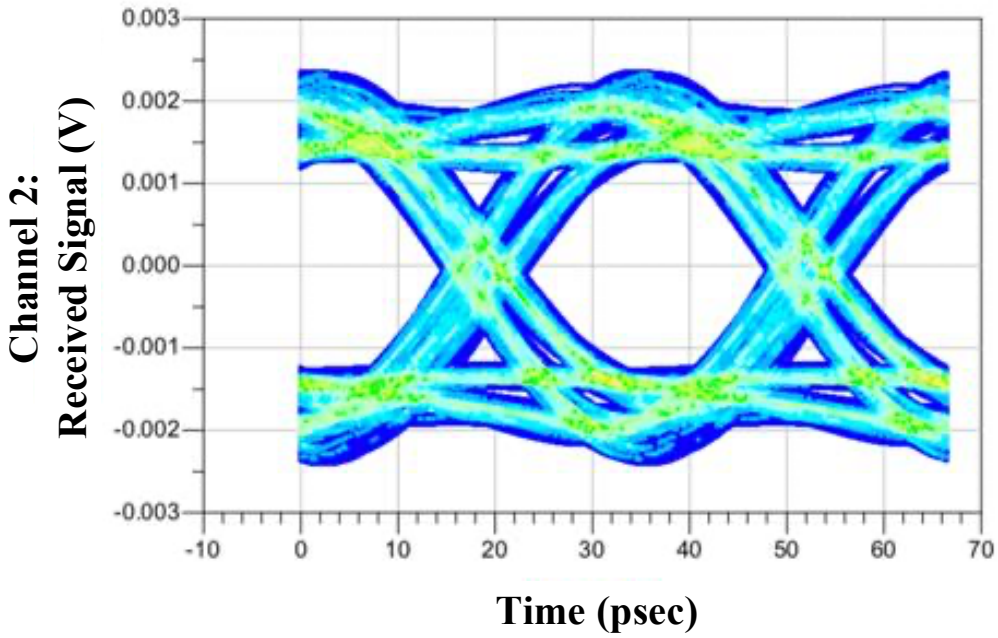


Figure 2-7: Simulated eye diagram of a 90 Gbps aggregate rate lane, carried over a THz waveguide. Baseband received voltage from a PRBS bit-stream for Channel 2 (260-290 GHz) is shown. From [43].

maximum for a given channel's signaling rate at a specific link length. In addition, guide-to-guide coupling will drive the maximum achievable bandwidth density at a given link length.

Once the waveguide configuration is chosen, a coupler that is capable of supporting the operating frequency and bandwidths of interest will have to trade off area (cost), ease of integration, efficiency, and bandwidth against each other. The performance of the waveguide and coupler will establish a baseline level of link loss, L_{ch}. Similarly to fiber optic interconnects, the loss mechanisms in these types of THz interconnects will exhibit fairly flat attenuation characteristics across the applicable link length scales [94].

As a result, focus should then shift to the THz channelization, carrier frequency generation and modulation, as well as baseband circuitry. Again, the overall link efficiency will largely depend on the efficiency of these components. As was discussed in Section 2.1.2, the choice of on- or off-chip multiplexers will have significant impacts on achievable spectral performance. This will, in-turn, have substantive impacts on the overall link performance.

Chapter 3

Wideband Planar THz Couplers

3.1 Introduction

Techniques utilizing off-chip radiators [3, 22, 23, 30, 34], illustrated in Fig. 1-9(a), aside from increasing system integration complexity, inherently trade the original bandwidth-distance constraint of copper interconnects in driving an off-chip coupler. This effect manifests itself as a decrease in coupling efficiency. In [3] a dual band coupler, utilizing mode orthogonality, was demonstrated with a bandwidth of 35 GHz and coupling loss of 5 dB. A number of efforts have utilized die-to-package bond wires or patch antennas as radiators, coupling energy into plastic tube waveguides [54, 96, 100, 101]. In [54] a coupler was demonstrated with a bandwidth of 6 GHz and a coupling loss of 6 dB utilizing air core plastic tube waveguides. This approach (and those used in [100,101]) is illustrated in Fig. 1-9(b). It presents a number of integration challenges in packaging, especially when high-density I/O integration is required. Lastly, work has been done on utilizing integrated on-chip antennas to couple modulated carriers into waveguides [34, 113], as shown in Fig 1-9(c). In [34] a coupler with a bandwidth of 8 GHz was implemented using a micro-machined silicon waveguide, exhibiting a coupling loss of 5.8 dB. While these efforts address the need for an on-chip coupler, they suffer from the well-known bandwidth-radiation efficiency tradeoffs associated with on-chip resonant antennas [36, 84]. This approach also requires the waveguide interface itself to be normal to the radiator surface to maximize

the coupling efficiency.

One of the key enabling technologies for such a THz link, a power coupler, is conceptually illustrated in Fig. 3-1. This structure, fully implemented in a silicon chip, requires neither wafer post-processing nor off-chip radiators, and presents a low-cost and readily-integrated solution for high-bandwidth short range chip-to-chip communication. The proposed structure is measured the frequency band. To the best of the authors' knowledge, these performance metrics represent the best reported to date.

The structure of the chapter is as follows: Section 3.2 covers the development of analytical models to approximate the electromagnetic behavior of the coupler structure, as well as the dielectric waveguide. Section 3.3 describes the parametric optimization, design, and implementation of the on-chip components, dielectric waveguide, and test fixtures. Section 3.4 discusses the measurement setup and procedures, he measurement results of the insertion loss associated with the coupler and various lengths of dielectric waveguide, as well as a comparison with data available in the literature. Section 3.5 concludes the chapter with a summary of achievements.

3.2 On-Chip Apertures

At sub-mmWave and THz frequencies, on-chip resonant radiators atop bulk silicon trade off bandwidth for radiation efficiency [36]. In the case of an unshielded radiator, a dipole or unbacked slot radiator, for example, the majority of the radiated energy preferentially couples into the bulk silicon. A silicon lens can be used to more efficiently radiate this power into free space [37] from the rear of the chip, but in doing so, one sacrifices integration cost and complexity. Backing a radiator with a ground plane may significantly improve the radiator efficiency. However, given the Back-End-of-Line (BEOL) interconnects available in modern silicon IC processes, the proximity of the ground plane and the radiator produces a high Q resonance dramatically lowering the radiation bandwidth [79].

A number of techniques can be used to increase on-chip antenna bandwidth. In [35]

parasitic reflectors were added to increase both the bandwidth and efficiency, as well as the directivity of the radiator. In [63, 109] extra resonances are designed into the aperture to extend antenna bandwidth. However, the antenna still radiates in the broad side which is incompatible with a planar coupling solution. Leaky Wave Antennas (LWA) have been used for efficient on-chip broad band radiation [79], and generally provide excellent directivity, as well as excellent beam width for use in a quasi-optical coupling scheme. These structures, however, require significant aperture lengths (on the order of several wavelengths) to maintain radiation efficiency [33, 52, 75, 76, 79]. This issue is of particular concern as related to on-chip integration. Any step taken to maintain or increase bandwidth and radiation efficiency, and decrease required physical size would make LWAs more attractive for on-chip integration. This work makes use of a modified LWA structure in which the coupler cross section is tapered to capitalize on the traveling wave structure's inherent bandwidth while decreasing the required structure length.

3.2.1 Differential Half-Mode Substrate Integrated Waveguide (HM-SIW) Leaky Wave Coupler

Single-sided HM-SIW antennas are traveling wave radiators that support the first microstrip higher-order mode (generally referred to as the EH_1 mode). Constant-cross section variants have been integrated on chip, and their single- and differentially-driven (Fig. 3-2(b)) variants have been demonstrated in arrays [11, 61, 79]. In [11], it was shown that the frequency at which a mode is said to be in the leaky wave region, defined as

$$\alpha < \beta < k_0\sqrt{\epsilon_{r-rad}}, \tag{3.1}$$

can be decreased if the structure is excited by the odd EH_1 mode. k_0 is the free space wave number. The longitudinal wave number is defined as

$$k_z = \beta - j\alpha, \tag{3.2}$$

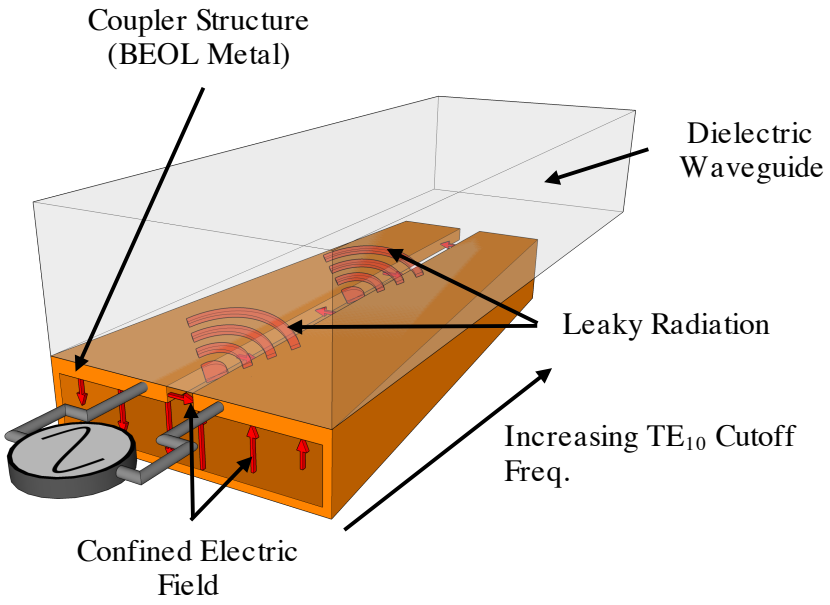


Figure 3-1: Conceptual illustration of a tapered Differential Half-Mode Substrate Integrated Waveguide (HMSIW) as presented in this work. From [46].

and the dielectric constant of the material where the leaky wave power radiates is denoted by ϵ_{r-rad} (Fig. 3-2). Here β is the propagation constant and α is the corresponding attenuation constant of a time-harmonic mode.

Consider a constant cross-section structure illustrated in Fig. 3-2(a)-(c). The inner dimension of the full HM-SIW width is denoted by $2d+a$, with the inner height dimension b, the slot width a and the top conductor thickness c. The HM-SIW coupler is filled with a material with dielectric constant ϵ_r. The entire structure couples to a infinite half-space with dielectric constant ϵ_{r-rad}.

This structure supports both even and odd EH_1 modes, Fig. 3-2(a) and (b), respectively. As was shown in [11], when supporting the odd EH_1 mode (as shown by the solid and dashed red arrows in Fig. 3-2(a)), the frequency at which leaky-wave behavior begins for a given structure width is decreased over that of a half-mode LWA or the same structure excited by the even EH_1 mode. In addition, using the odd EH_1 mode increases the power radiated due to leaky radiation (described by the attenuate constant α) at a given frequency over the even EH_1 mode or a traditional half-mode LWA. By utilizing the odd EH_1 mode, for a given cross section, the amount of energy

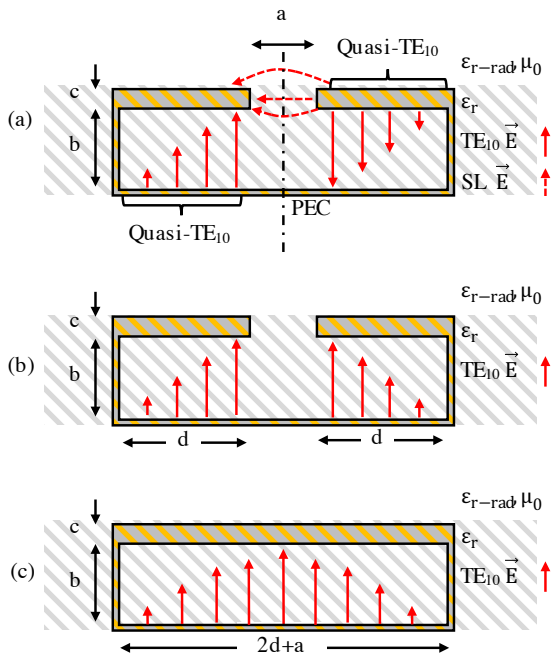


Figure 3-2: Three structures with the same cross section: (a) the presented structure supporting the odd EH_1; (b) the presented structure supporting the even EH_1 mode; and (c) a TE_{10} mode in the same size structure as the gap a goes to zero width. The solid lines correspond to the those portions of the mode that resembles a portion of a standard rectangular waveguide TE mode, while the dashed lines in the odd EH_1 mode resemble that portion of the field resembling a slot line mode. From [46].

coupled into a space-leaky mode can be enhanced and the overall required radiator length decreased while maintaining coupling efficiency compared with a structure excited by the even EH_1 mode or a half-mode LWA supporting a TE_{10} mode.

When excited with the odd EH_1 mode, a portion of the electric field contained within the structure and far from the central slot resembles half of a TE_{10} rectangular waveguide mode (Fig. 3-2(c)). In the following discussion, we will refer to this portion of the mode as the quasi-TE_{10} portion, and this portion of the field is denoted by the solid red lines in Fig. 3-2(a). Near the center slot, the increased electric field strength across the gap causes the electric field lines from the top conductor near the gap to terminate, not vertically onto the bottom conductor, but rather on the top conductor on the opposite side of the gap. These fields are similar to a conductor-backed slot-line mode. This portion of the mode is denoted by the dashed electric field lines.

It should be noted that, for a given guide width $2d + a$, which is approximated by $2d$, at frequencies above

$$f_{TE} \approx \frac{c_0\sqrt{\epsilon_r}}{4d}, \tag{3.3}$$

where c_0 is the free-space speed of light, the energy in the quasi-TE_{10} field is well-confined in those rectangular waveguide regimes on the structure to the left and right of the center slot. As the wavelength of the supported mode is increased, each rectangular guide section of length d can no longer fully support a quarter wave, and some portion of this energy is coupled into the electric field supported between the center slot and the bottom conductor. This portion of the mode is shown by the slot-line fields denoted by the dashed field lines in Fig. 3-2(a). Once this energy has been coupled into this regime, it will radiate away from the structure in a space leaky mode if the mode's propagation constant satisfies (3.1). In the slot and near field, this structure produces an electric field in which the major component is aligned horizontally (Fig. 3-3(a)), which is matched with the desired horizontally-polarized mode in the dielectric waveguide (Fig. 3-8). The similarity between the desired waveguide mode and coupler radiative modes aides in energy coupling. This is in contrast with the

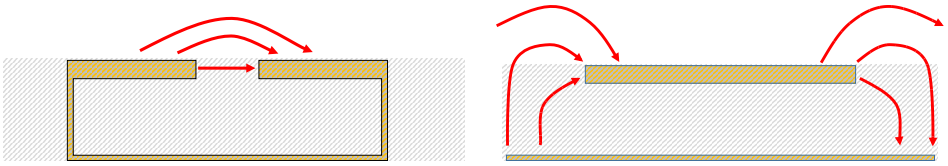


Figure 3-3: A comparison of the near-field electric field lines around (a) the presented coupler structure supporting the odd EH_1 mode and (b) a patch antenna. From [46].

field distribution created by a traditional patch antenna (Fig. 3-3(b)), as was used in [34,113]. The fringe fields at the edge of a patch form horizontally-polarized electric fields in the far-field, but the near-field modes have much more structure. Traditional patch antennas exhibit larger near-field electric field intensity at the edge with smaller field intensity in the center of the patch. The dissimilarity, in the near field, of this mode and the desired waveguide mode does not encourage energy coupling from the radiative mode into the waveguide mode.

By decreasing the structure width, $2d$, longitudinally (as illustrated in Fig. 3-1), such a structure produces regions in which energy in a previously-propagating quasi-TE_{10} portion of the mode impinges on a narrower cross section where that energy couples into the field supported across the center gap. By virtue of the differential excitation (the odd EH_1 mode), this same structure facilitates the lower-frequency onset of space-leakage, as defined in (3.1), and simultaneously increases the rate of leakage α over the leaky regime [11]. In this way, this structure is able to radiate with the same efficiency while requiring less length.

If implemented on chip, this structure provides a number of advantages over traditional on-chip antennas. It is noteworthy that the proposed coupler structure provides the following three advantages over the prior on-chip designs:

1. Its enclosed nature provides mode confinement away from the bulk silicon, thus decreasing unwanted energy coupling into the substrate.

2. The proposed structure is a traveling wave structure leading to a wider bandwidth than in resonant structures.

3. The coupler near-field mode is structurally similar to the desired mode of the

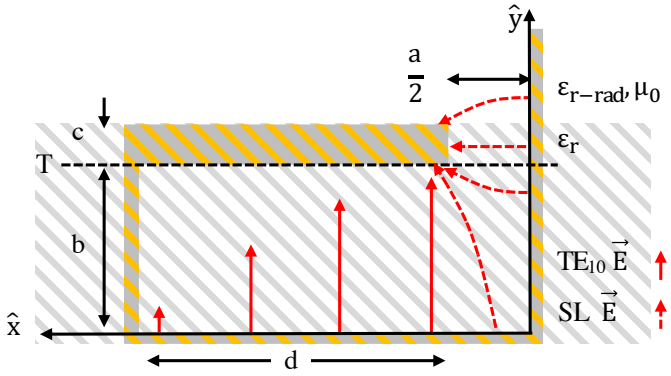
dielectric waveguide, improving coupling efficiency.

3.2.2 Analytical Transverse Resonance Model

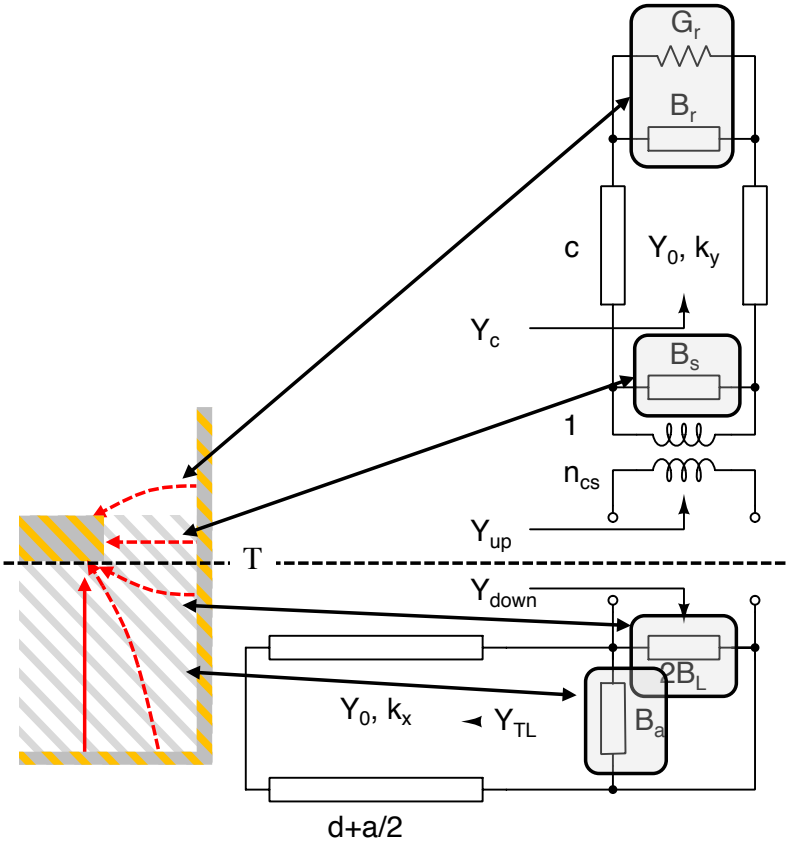
Structures similar to that presented in Fig. 3-2(b) have been studied using modal analysis in [115, 116], but these analyses assumed a zero-thickness top conductor. However, the integrated circuit process in which our structure is implemented makes use of a thick top metal of thickness c. The conductor-backed slot-line and its odd hybrid mode behavior have also been extensively modeled, utilizing both modal analysis and circuit approximations [56]. This analysis does not support modes constrained laterally in the bottom portion of the structure. The operation of the proposed structure relies on the vertical SIW walls to contain energy that might otherwise be dissipated into bulk silicon surface waves. In a comparison with full-wave analysis, both of the aforementioned analyses were found to deviate significantly.

An analytical model of the relationship of the odd EH_1 mode longitudinal propagation constant, k_z, as a function of guide dimensions, is desired. Such a model provides insight into the space leaky wave behavior, or the propagation constant β to be specific, as the cross section of the structure is modified. We first consider a uniform cross section HM-SIW leaky-wave coupler (Fig. 3-2(a) and (b)). We assume the conductors (physically realized by aluminum metallization and arrays of tungsten vias) are perfect electric conductors. Next, we note that the electric field distribution of the odd EH_1 mode (Fig. 3-2(a)) is differentially symmetric, and thus its transverse equivalent network can be represented by a half structure utilizing a perfect electric conductor (PEC) boundary condition (Fig. 3-4(a)).

The geometry in Fig. 3-4(a), using an approach modified from [57, 76] for the fields in and around the gap, can be analyzed by a closed-form transverse resonance expression. The resonance condition plane T, denoted by the dashed horizontal line in Fig. 3-4(b), provides a convenient reference with which to categorize the energy stored in various portions of the fringe fields near the center gap. Modifications to lumped element approximations for the energy storage and coupling mechanisms for an air filled rectangular guide based on E-plane tee junction models from [57, 76] are



(a)



(b)

Figure 3-4: (a) HM-SIW EH_1 equivalent half structure, and (b) equivalent transverse resonance circuit model. From [46].

reproduced here with appropriate modifications for different dielectric constants and differential energy storage not accounted for in the original analysis.

The susceptances $2B_L$and B_a account for the stored energy in the main guide (below the resonance plane T) underneath the slot (Fig. 3-4(b)). In the following analysis, each lumped element is normalized by the transverse guide characteristic admittance Y_0 of the rectangular waveguide portions of the structure in Fig. 3-2(b). Enhancing the analysis in [76] to account for dielectric fill and odd-mode symmetry, we write the susceptances for the slot-line-like fields as

$$\begin{aligned} \frac{B_L}{Y_0} &= \frac{\epsilon_r}{n_c^2}\left(\frac{k_x b}{\pi}\right)\left[\ln\left(1.43\frac{b}{a}\right)+\frac{1}{2}\left(\frac{k_x b}{\pi}\right)^2\right]\ldots \\ &+ \frac{\pi}{32}\frac{a}{b}\left(k_x\frac{a}{2}\right)J_0^2\left(k_x\frac{a}{2}\right) \end{aligned} \tag{3.4}$$

$$\frac{B_a}{Y_0} = -\frac{\pi}{16}\frac{a}{b}\left(k_x\frac{a}{2}\right)J_0^2\left(k_x\frac{a}{2}\right), \tag{3.5}$$

where J_0 is the Bessel function of the first kind, and

$$n_c = \frac{\sin\left(k_x\frac{a}{2}\right)}{k_x\frac{a}{2}}. \tag{3.6}$$

These expressions arise from the analysis of E-plane tee junctions and the integration of the electric modal functions across the gap above and below the resonance plane T when excited by a symmetric magnetic field [57, 72, 76]. The admittance looking into the left side of the shorted transmission line (Fig. 3-4) from the right, representing the half-width guide along the x-axis of length $d+\frac{a}{2}$, can be written as

$$\frac{Y_{TL}}{Y_0} = -j\cot\left(k_x\left(d+\frac{a}{2}\right)\right). \tag{3.7}$$

The wavenumber k_x, as driven by structure geometry, is used as the parameter to ultimately tune the leaky-wave behavior of the structure.

Above the resonance plane T, we assume that the gap is narrow enough such that only a transverse electric field is supported across the gap. In the gap between the

top conductors, from T to the ϵ_r - ϵ_{r-rad} dielectric interface, a horizontally-polarized TE_{10} mode (that is $E_x \neq 0$, $E_y = E_z = 0$), is supported in the vertical $\hat{y}$ direction. The equivalent susceptances of the energy stores in the field directly above T are written as,

$$\frac{B_s}{Y_0} = \frac{4b}{\lambda_g} \ln \csc \frac{\pi a}{2b}, \tag{3.8}$$

where the guide wavelength is

$$\lambda_g = \frac{\lambda_0}{\sqrt{\epsilon_r - \left(\frac{\lambda_0}{4d}\right)^2}}. \tag{3.9}$$

The coupling coefficient, modeled by the transformer in Fig. 3-4(b) with a turns ratio of,

$$n_{cs} = n_c \sqrt{\frac{a}{b}} \tag{3.10}$$

accounts for the difference in the modal voltages in the horizontal portion of the structures and those in the gap [75]. The short section of vertical parallel plate, of length c along $\hat{y}$, seen from reference plane T and up can be represented as a short transmission line of length c. We can write the admittance looking into this transmission line as

$$\frac{Y_c}{Y_0} = \frac{\frac{Y_r}{Y_0} + j \tan k_y c}{1 + j \frac{Y_r}{Y_0} \tan k_y c}. \tag{3.11}$$

The equivalent radiation admittance from a rectangular waveguide into a dielectric half-space is,

$$\frac{Y_r}{Y_0} = \frac{G_r + jB_r}{Y_0} = \frac{\sinh\left(\frac{k_y a}{2}\right) + j\sqrt{\epsilon_r} \sin A}{\cosh\left(\frac{k_y a}{2}\right) + \cos A} \tag{3.12}$$

for

$$\begin{aligned} A \;=\; & \frac{k_y a}{\pi} \ln\left(\frac{e}{\gamma} \frac{4\pi}{k_y a}\right) - \\ & 2\sum_{n=1}^{\infty} \left[\sin^{-1}\left(\frac{k_y a}{2\pi} \frac{1}{n}\right) - \left(\frac{k_y a}{2\pi} \frac{1}{n}\right)\right] \end{aligned} \tag{3.13}$$

where $\gamma \approx 1.781$ and Napier's constant, e, is 2.718 [72]. In addition, we have assumed

a single transverse electric mode above T in Fig. 3-4(a) and single TE mode operation in the horizontal portion of the structure to the left of the gap in Fig. 3-4(a). As this entire region is filled with the same dielectric, we assume k_x below the reference plane T and away from the slot is equal to k_y above T.

Considering the circuit model in Fig. 3-4(b), we can write the admittance looking down from the reference plane T as

$$Y_{down} = Y_{TL} + j\left(B_a + 2B_L\right), \tag{3.14}$$

and, similarly, the admittance looking up as

$$Y_{up} = \frac{1}{n_{cs}^2}\left(Y_c + jB_s\right). \tag{3.15}$$

In order for a transverse resonance to occur, we note that the phases of Y_{up} and Y_{down} at the resonance plane must cancel, from which we are able to solve for the transverse wavenumber in the horizontal portion of the coupler structure away from the slot

$$k_x = \sqrt{k_0^2\epsilon_r - k_z^2}, \tag{3.16}$$

which in turn yields the longitudinal wavenumber, k_z, and subsequently, the propagation β and attenuation α constants.

3.2.3 Analytical Model: Numerical Investigation

In comparison to the case of an un-tapered structure, this tapered structure provides a progressively higher cutoff frequency as the wave travels longitudinally down the structure. In addition, the traveling wave also exhibits a commensurate increase in the rate of leakage α in the leaky regime. While an un-tapered structure will certainly leak energy into the covering semi-infinite dielectric, the length required to achieve high levels of coupling is much longer. In this way, the tapered structure is capable of forcing energy otherwise confined in a quasi-rectangular waveguide mode into a space leaky wave mode in a longitudinally-shorter aperture while maintaining a large

bandwidth.

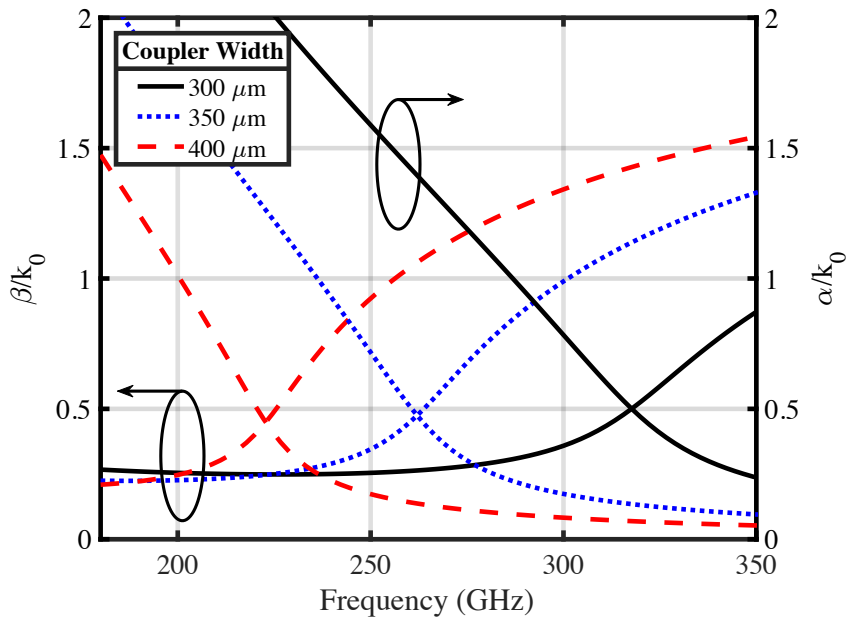


Figure 3-5: Propagation constant of a uniform cross section coupler for various coupler widths, $2d + a$, and gap width $a = 3.5$ μm from the analytical model. From [46].

Fig. 3-5 shows the dependence of the propagation constant β and attenuation constant α, as modeled in Subsection 3.2.2, as a function of frequency for changing coupler widths. In this model, the dielectric into which the leaky wave is propagating is chosen to be compatible with Rogers Corp. R3006 dielectric ($\epsilon_{r-rad} = 6.15$). From this plot, we can see that the analytical model predicts that, for a desired operating range of 220 GHz - 320 GHz, the total guide width ranges from approximately 300 μm to 400 μm to provide leaky operation across the entire band, while maximizing leakage, α, for a given length. These values are utilized in a subsequent full-wave optimization as a starting point to co-optimize the dielectric waveguide cross section and the coupler geometry to minimize insertion loss and coupler return loss.

3.2.4 Dielectric Waveguide

Utilizing Marcatili's method [67] for rectangular waveguides, we consider a cross section of a homogenous dielectric material, size dw x dh μm^2 with dielectric constant

ϵ_{r1} surrounded on each face, to ease analysis, by material, ϵ_{r2} (Fig. 3-6). This structure supports two quasi transverse-electric modes, the E^x_{mn} and E^y_{mn} modes, in which the bulk of the field is polarized in either the $\hat{x}$ or $\hat{y}$ direction, respectively. The $\hat{x}$

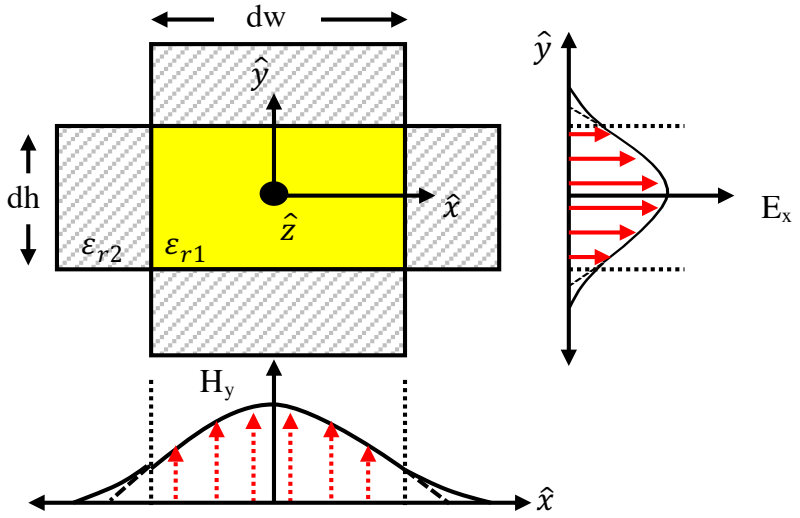


Figure 3-6: Setup for Marcatili's rectangular dielectric guide approximation, and quasi-transverse E^x_{11} modes of a rectangular dielectric waveguide. From [46].

polarized case, E^x_{11} is shown in Fig. 3-6. As in the case utilized in [30], we can set up the nonlinear relationships for the desired first order E^x_{11} mode, assuming the guide is surrounded by air ($\epsilon_{r2} = 1$) as

$$k_x dw = m\pi - 2\tan^{-1}\left(\frac{k_x}{\epsilon_{r1}\sqrt{k_0^2(\epsilon_{r1}-1)-k_x^2}}\right) \tag{3.17}$$

$$k_y dh = n\pi - 2\tan^{-1}\left(\frac{k_y}{\sqrt{k_0^2(\epsilon_{r1}-1)-k_y^2}}\right) \tag{3.18}$$

which can be solved for the transverse wavenumbers, k_x and k_y. From these, the dispersion relationship

$$k_z = \beta = \sqrt{\epsilon_{r1}k_0^2 - k_x^2 - k_y^2} \tag{3.19}$$

can be computed and used to determine the cutoff frequencies of a given mode. The cutoff frequencies of the first and second-order modes (E^x_{11} and E^x_{21}) are shown in Fig.

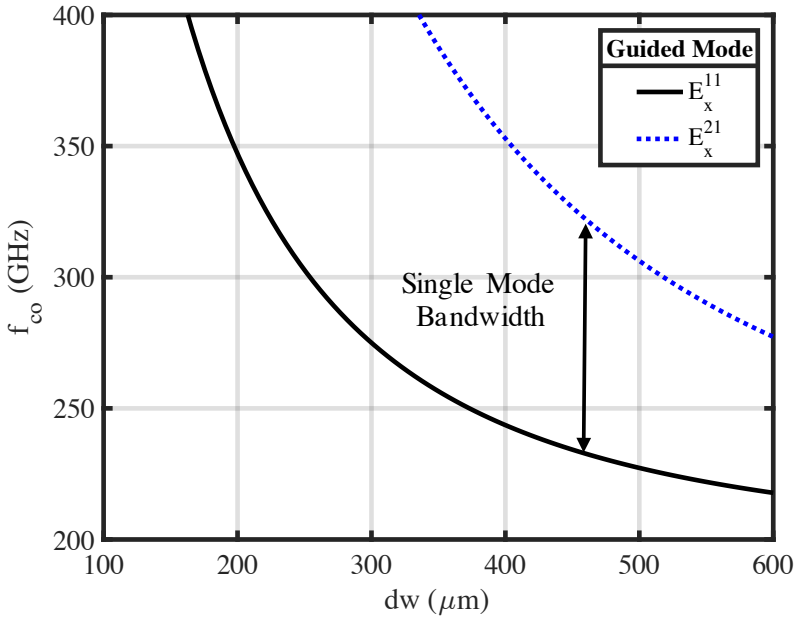
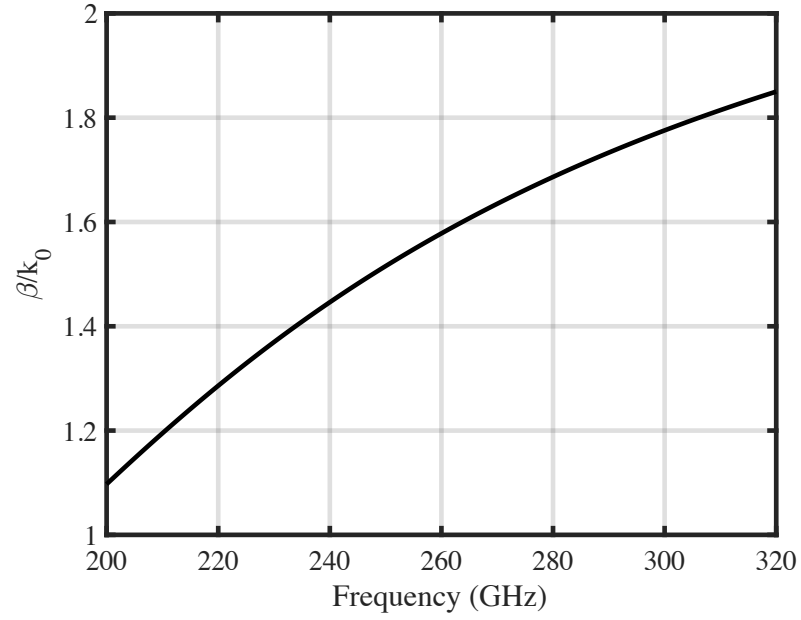


Figure 3-7: The predictions of the cutoff frequencies for the first and second order (E_{11}^x and E_{21}^x) modes of a 250 x dw μm^2 R3006 dielectric waveguide guide from Marcatili's method, used as a starting point for full-wave optimization. From [46].

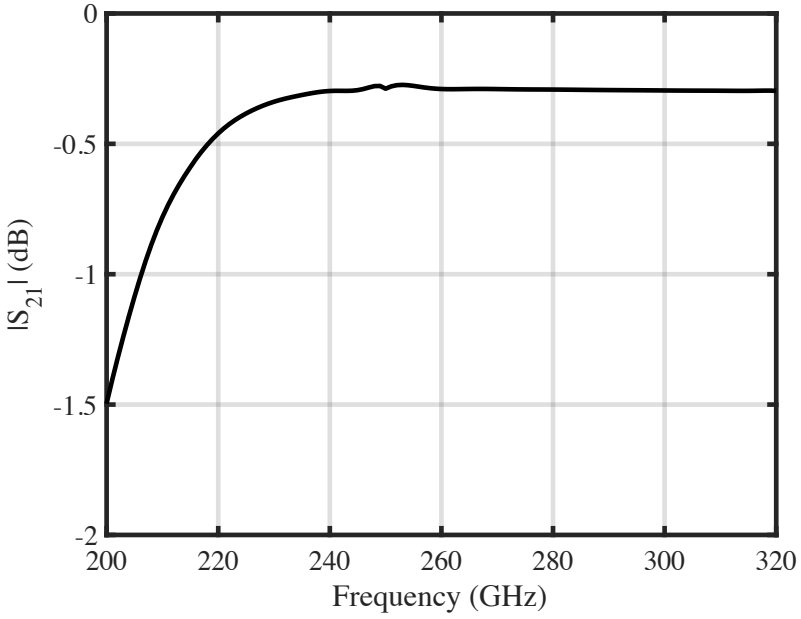
3-7 for a waveguide height, dh, of 250 μm thick bulk R3006 of different widths. In this case, an initial estimate of guide dimensions to preclude over-moding in the frequency band of choice can be made. This initial waveguide width, dw, of 500 μm was used in a full-wave simulation to co-optimize the coupler structure and the waveguide cross section. Following this optimization, a 400 μm waveguide width was chosen. As can be seen in Fig. 3-8(b) a 250 x 400 μm piece of Rogers Corp. R3006 with a dielectric constant of 6.15 provides a more than 100 GHz of bandwidth from 220 GHz to beyond 320 GHz. It should be noted that Marcatili's approximation provides a reasonable starting point for full-wave electromagnetic simulation from which optimization is used to converge to a guide cross section that is mode-matched to the tapered coupler structure, maximizing power transfer.

3.2.5 On-Chip Tapered Coupler

Using the coupler dimensions derived numerically in Section 3.2.3 and the waveguide cross section in Subsection 3.2.4 as a starting point, the coupler and waveguide di-



(a)



(b)

Figure 3-8: Full wave data demonstrating operation above cutoff of the E_{11}^x mode in a 250 x 400 μm^2 cross section R3006 waveguide of 500 mm in length. (a) Normalized longitudinal dispersion characteristics, and (b) transmission scattering parameters. From [46].

mensions ($L_{coupler}$, a, and $a+2d_w$ and $a+2d_n$ at the coupler's wide and narrow widths, respectively) were designed in the IHP SG13G2 SiGe BiCMOS BEOL process and optimized with the aid of full-wave simulation tools. This process offers a 3 μm thick top metal with a distance of 9.83 μm between the top of the bottom metal and the bottom of the top metal. The coupler is composed of the bottom metal (Metal 1) and the top thick metal (Top Metal 2) as the horizontal conductors and the intermediate metal interconnects and arrays of vias to produce the vertical walls (Fig. 3-9).

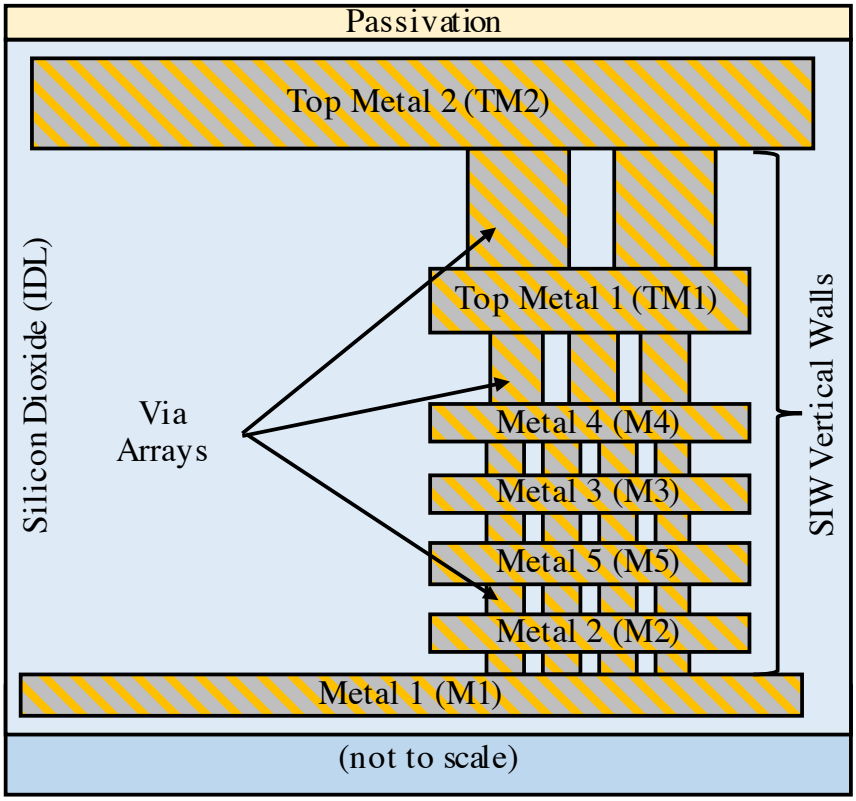


Figure 3-9: Schematic diagram of the IHP SG13G2 BEOL and Substrate Integrated Waveguide structure (not to scale). From [46].

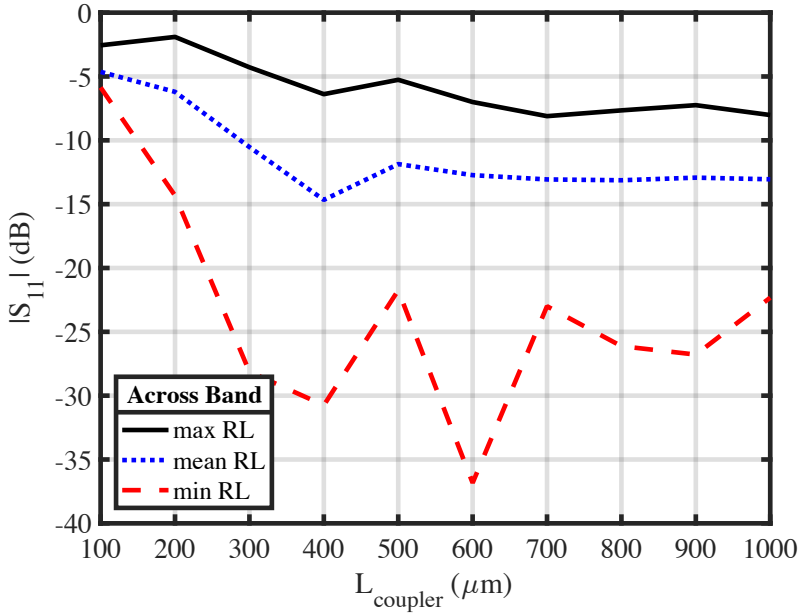
A simplified model was implemented in HFSS, a commercial full-wave electromagnetic simulation package. The coupler geometry was excited by a 50 Ω source across the structure's slot at the wider end of the coupler (Fig. 3-1). Immediately on top of this coupler topology, a rectangular fiber with a thickness, dh, of 250 μm (to account for commercially-available material thicknesses) rectangular cross section fiber completely overlays the coupler slot and extends 500 μm beyond the narrow end of the

structure. The second port of the model consists of a wave port at the end of this 500 μm protrusion. The coupler structure and waveguide dimensions were optimized with $a \approx 3.5$ μm, $d_w \approx 180$ μm at the widest end of the structure, and $d_n \approx 100$ μm for the narrowest end of the structure to minimize the structure return and insertion loss across the desired 220 GHz to 325 GHz operating band. From this point, full-wave simulations were executed to tune the coupler length, $L_{Coupler}$. The results of these simulations can be seen in Fig. 3-10. From these plots, one can readily see that the input match and insertion loss across the entire band improves with increasing coupler length. A coupler length, $L_{coupler}$, of 750 μm was chosen for fabrication to maintain an average insertion loss of approximately 4 dB with better than 8 dB of return loss across the band, while minimizing on-chip area.

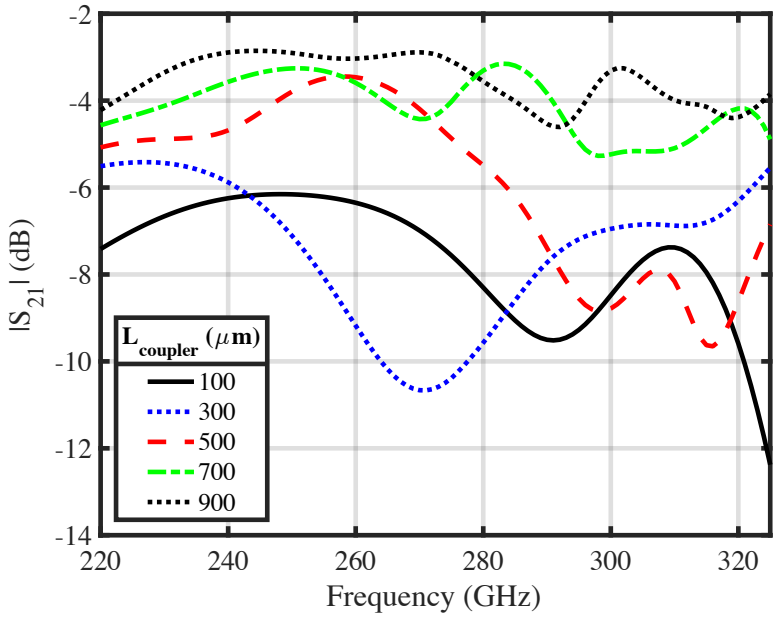
3.3 Implementation

3.3.1 On-Die Structures

In order to facilitate on-wafer testing of the coupler, a mode converter (Fig. 3-11) was designed to provide a broadband conversion of an on-wafer 50 Ω microstrip mode to a 50 Ω slot-line mode, driving the coupler structure (as shown schematically in Fig. 3-1). The microstrip feed line was implemented using the top and bottom metal layers, with a trace width of 17 μm. In addition, this mode-converter was used to compensate the slightly inductive input reactance of the coupler. By using Top Metal 1 (Fig. 3-9) under Top Metal 2 in the mode-converter feed structure, a capacitive waveguide E-plane iris is presented in parallel with the driving point of the coupler input [72], providing an improved input match. This section of the mode converter presents itself, essentially, as a grounded co-planar waveguide (GCPW) or half of a rectangular coaxial transmission line with a trace width of 4 μm, and a gap width of 20 μm. The distance between the bottom of the signal trace and the GCPW effective ground is 3 μm. The mode converter is approximately a quarter wave in length at the center of the operating band, comprised of a 170 μm long 3.5 μm wide slot and



(a)



(b)

Figure 3-10: Parametric full-wave analysis of the coupler structure radiating into a 250 x 400 μm^2 R3006 waveguide: (a) magnitude of S_{11} (characteristic impedance 50 Ω) and (b) magnitude of S_{21} for various coupler lengths. From [46].

a 20 μm diameter circular choke for broadband response. This mode converter is designed with the same cross section (width, height, gap width, etc.) as the coupler structure, enabling direct connection to the coupler structure. With the integration of on-chip electronics, this mode-converter may not be necessary, further decreasing the end-to-end insertion loss and reducing the overall coupler size.

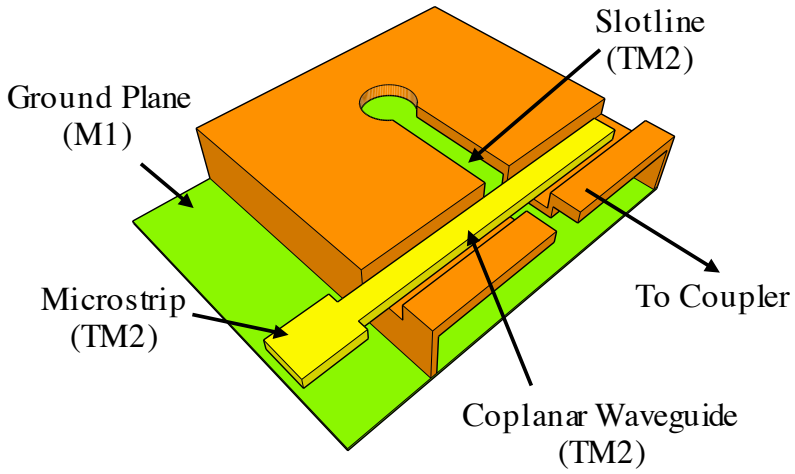


Figure 3-11: A model of the mode-converter (not to scale). The vertical walls are modeled as solid and connected to the structure top metal (TM2). A continuous ground plane (M1) underneath the structure is shown. The feeding structure is illustrated as a microstrip connected to a coplanar waveguide (TM2). From [46].

On-die calibration standards were designed and implemented, enabling multi-line transmission, reflection, and line (mTRL) calibration [105]. Microstrip lines of lengths commensurate with those driving the coupler and mode-converter structures were available on die to aid in de-embedding the microstrip loss. Lastly, a back-to-back mode-converter was implemented on die to enable de-embedding the response associated with the mode-conversion and subsequent additional dielectric and ohmic losses. A micro-photograph of the taped-out chip is presented in Fig. 3-12. The entire chip is 2.0 x 2.0 mm^2 and requires no post-processing or special handling.

3.3.2 Test Coupon and Dielectric Waveguide

A test coupon/holder was designed (Fig. 3-13) to provide a rigid substrate, maintaining relative position between two dies under test. This substrate provided a stable

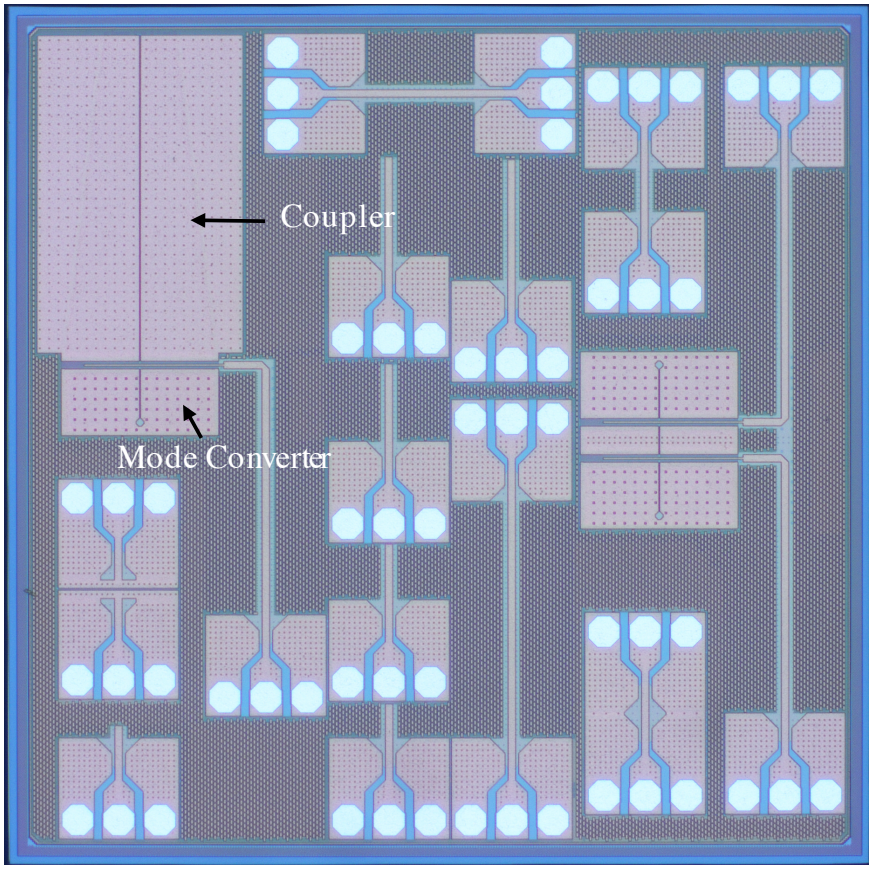


Figure 3-12: A die photo graph of the chip, including calibration standards, de-embedding structures, and the coupler. From [46].

Table 3.1: Test coupon positions and waveguide lengths.

Position in Fig. 3-13	Chip-to-Chip Distance	Notes
1	N/A	Calibration Positions
2	0.1 cm	Straight Waveguide
3	1.0 cm	Straight Waveguide
4	2.0 cm	Straight Waveguide
5	2.0 cm	2 x 90° Bends, 1.2 mm Rad. of Curve

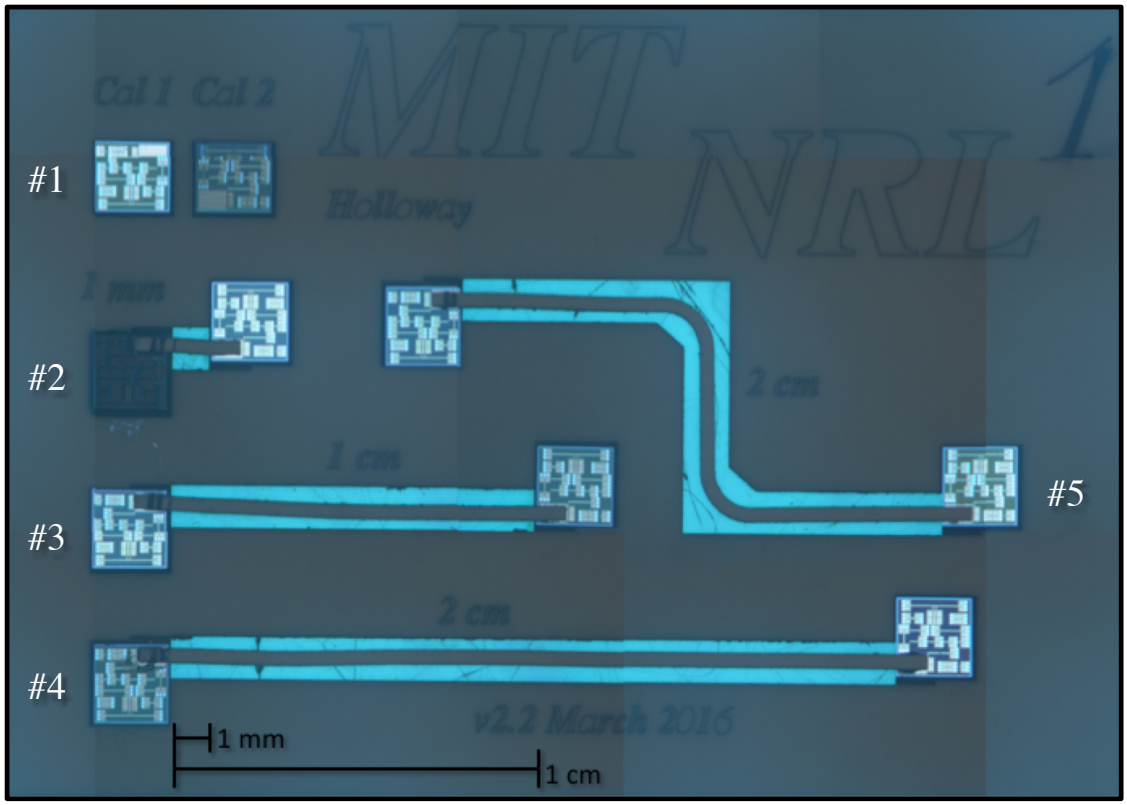


Figure 3-13: A photograph of a fully populated test coupon (the light blue areas are from back-side illumination on the micrograph station). From [46].

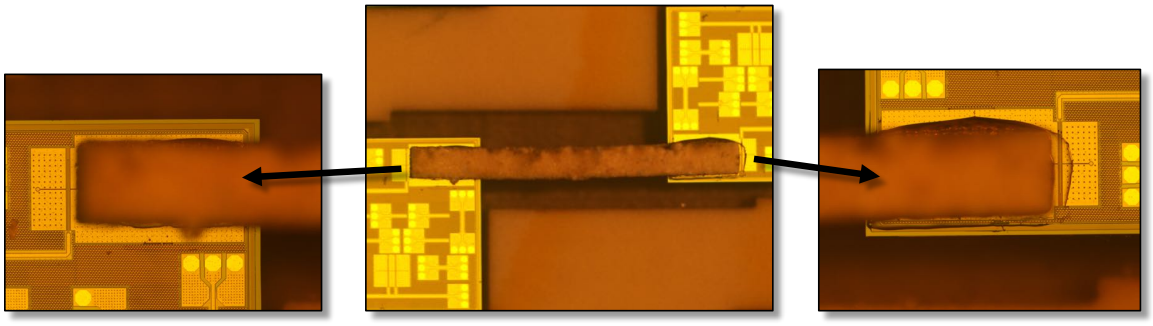


Figure 3-14: Bonding of the dielectric waveguide to coupler apertures. From [46].

platform onto which dies were bonded, and subsequently, the dielectric waveguides bonded to these dies. In order to minimize evanescent mode coupling into areas surrounding the dielectric waveguide a low dielectric constant Rogers TMM3 ceramic composite material ($\epsilon_r \approx 3.27$) was selected for the substrate. The material was laser ablated for individual die position, depressed 300 μm from the material surface. Areas underneath the desired dielectric waveguide routing were removed to reduce the waveguide's evanescent field interaction with the substrate. The final test coupon consists of three straight waveguide sections of different lengths and one section that has two 90° bends with a radius of 1.2 mm. Table 3.1 enumerates the waveguide lengths corresponding to those positions in Fig. 3-13.

Rogers R3006 was chosen for the dielectric waveguide interconnect for its specified dielectric constant, machinability, low loss, and wide availability. These waveguides were made from bulk 250 μm thick unclad R3006 that are laser cut to a width, dw, of 400$\pm$10 μm. A number of straight and curved waveguide pieces were cut to align with the individual die and coupler positions after bonding to the test coupon/substrate described in the next subsection.

After the individual dies were placed, aligned, and bonded to the substrate material, the dielectric waveguides were then individually bonded on top of the chips' passivation layers (Fig. 3-14) with EPOTEK 713 epoxy. Following the preparation of the test coupon substrate, die bonding, and waveguide bonding, the vertical relief of the bonds was investigated using a microscope profilometer. We were able to measure the distance between the top of the individual die passivation layer and the bottom of the dielectric waveguide (denoted as ΔH_{gap}) at each position. At positions #2, #3, and #5, we found that the bond was flush with the top of the passivation layer ($\Delta H_{gap} \approx 0$ μm), whereas the bonds for the 2 cm straight waveguide, position #4, had an average separation of approximately 17.5 μm above the two chip interfaces. Our inability to remove the epoxy and waveguide from these positions without damage and our limited number of dies precluded re-bonding these positions. As such, a full-wave characterization of the effects of this separation was carried out over the frequency range 220 - 320 GHz. The results of this simulation (Fig. 3-15) show that

approximately 2.5 dB increased loss, averaged across the band, is expected in the measurement of position #4.

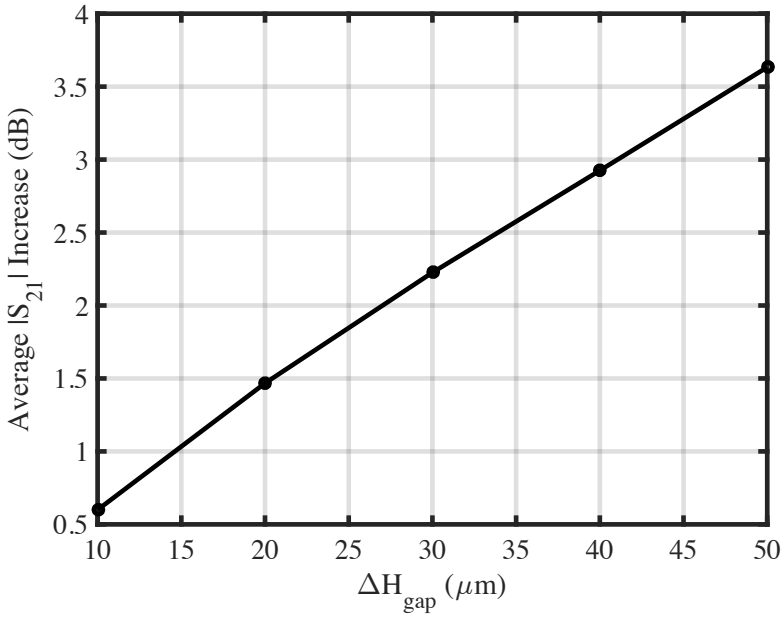


Figure 3-15: Full-wave simulation results of the increase in insertion loss, averaged over the frequency band, of a single coupler-waveguide transition as a function of ΔH_{gap}. From [46].

3.4 Measurement

3.4.1 Setup

Calibrations and measurements of these coupons were taken using a Suss micro probe station with micro positioners, an Agilent N5426 PNA-X network analyzer, a set of OML WR-3.4 220-325 GHz VNA extenders, and two Cascade Infinity Ground-Signal-Ground (GSG) probes (Fig. 3-16). A second set of measurements was taken to verify these measurements with Virginia Diodes, Inc. frequency extenders and Dominion Micro-Probe's T-Wave probes.

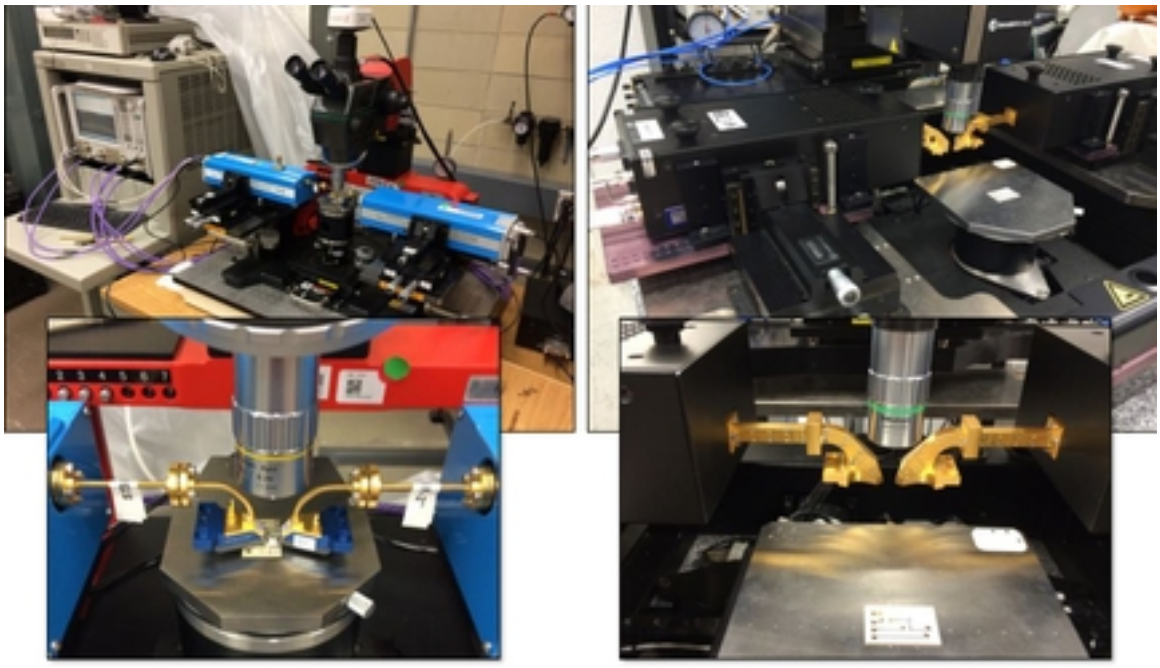


Figure 3-16: Measurement setup utilizing OML frequency extenders with Cascade Infinity probes (left), and VDI extenders with DMPI T-Wave probes (right). From [46].

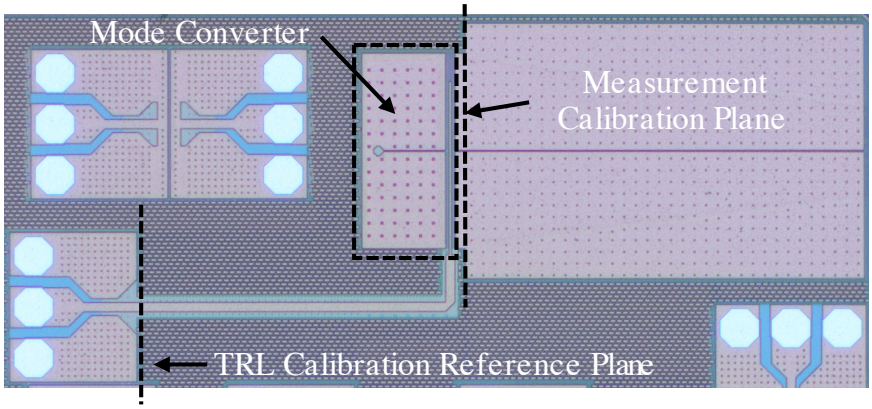


Figure 3-17: Calibration reference plane following mTRL calibration. From [46].

3.4.2 De-embedding

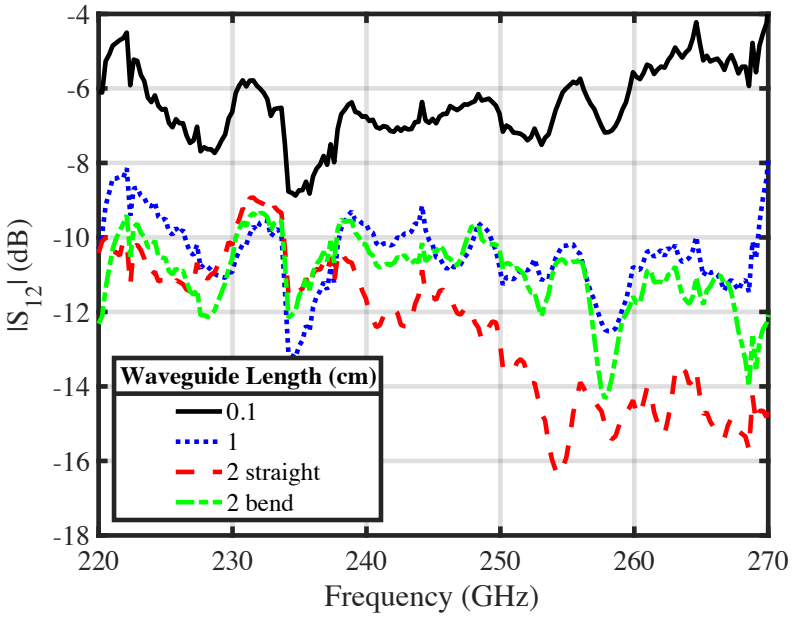
A multi-line Thru-Reflect-Line (mTRL) calibration [105], using on-chip calibration standards, was used to establish the calibration plane at the beginning of the microstrip transmission line shown in Fig. 3-17. Good calibrations were repeatably obtained from 220 GHz to 270 GHz. Above 270 GHz, an unanticipated resonance appeared, which is due to unpredicted coupling with the BEOL dummy metal fill around the pads and transmission lines added by the fab to adhere to minimum metal density rules. Post-calibration measurements of microstrip transmission lines and mode-converter de-embedding structures were taken to enable de-embedding of the coupler structure and waveguide response.

3.4.3 Results

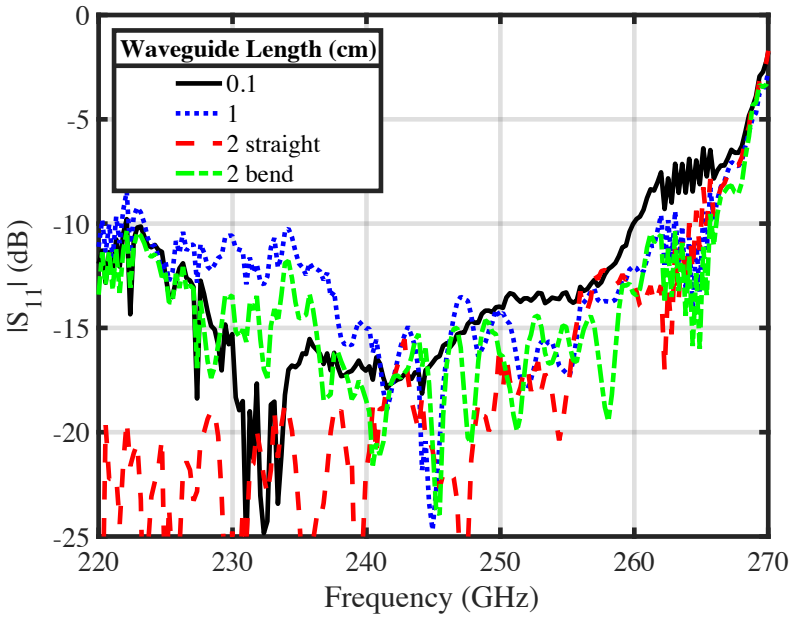
Utilizing the microstrip and mode-converter de-embedding structure responses, the back-to-back coupler-to-waveguide response was de-embedded from measurement. The resultant de-embedded data are presented in Fig. 3-18 and Fig. 3-19. The presented data are calibrated to the reference plane between the mode converter and the coupler structure (Fig. 3-17). The phase in Fig. 3-19(a) is not the absolute phase shift of each coupler-waveguide-coupler transmission, but rather is reduced by a multiple of 360° so that the phase at 220 GHz lies within 0° to 360°, as directly provided by the VNA in the measurement.

Compared to the 2.0 cm waveguide with bends, the 2.0 cm straight waveguide has an additional measured average insertion loss of 2.5 dB, partly due to the 17.5 μm ΔH_{gap}. The simulated loss increase corresponding to ΔH_{gap} is shown in Fig. 3-15. The significantly reduced insertion loss and increased phase delay of the 0.1 cm waveguide compared to the longer waveguides indicated that this length is short enough to support energy coupling into not only a traveling wave mode in the dielectric guide, but a radiative mode coupled into the opposite side of the link.

The close and linear relationship between the phase responses, normalized to the waveguide lengths, indicates that the guided waves do not encounter significant

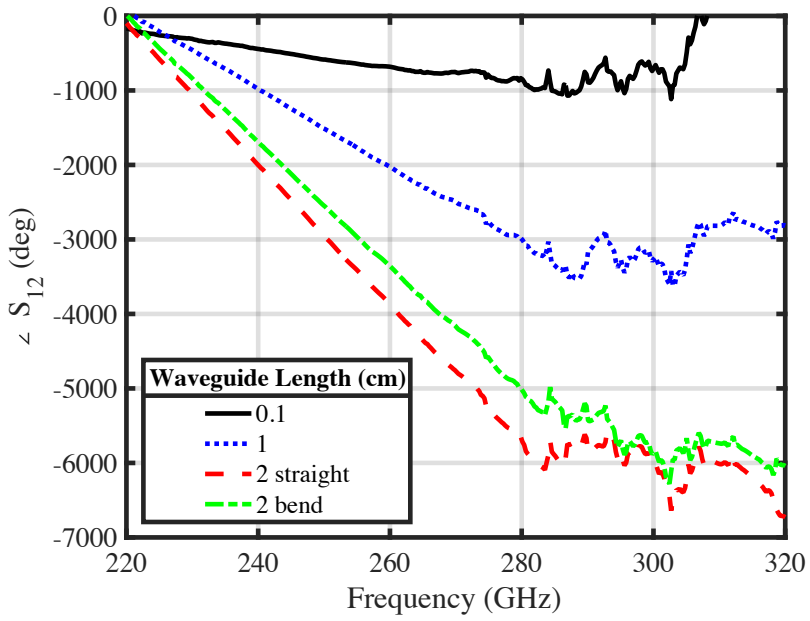


(a)



(b)

Figure 3-18: (a) Measured coupler-waveguide-coupler response, (b) S-parameter magnitude response. From [46].



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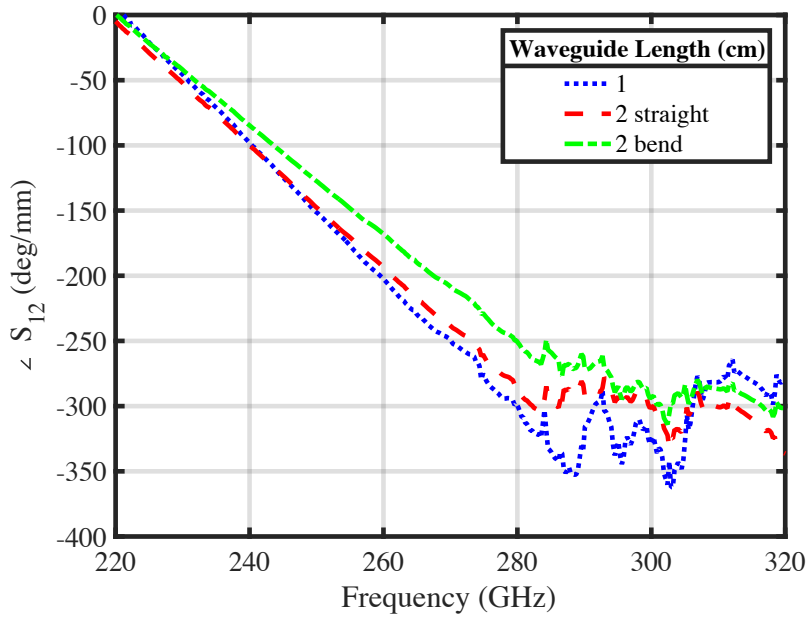
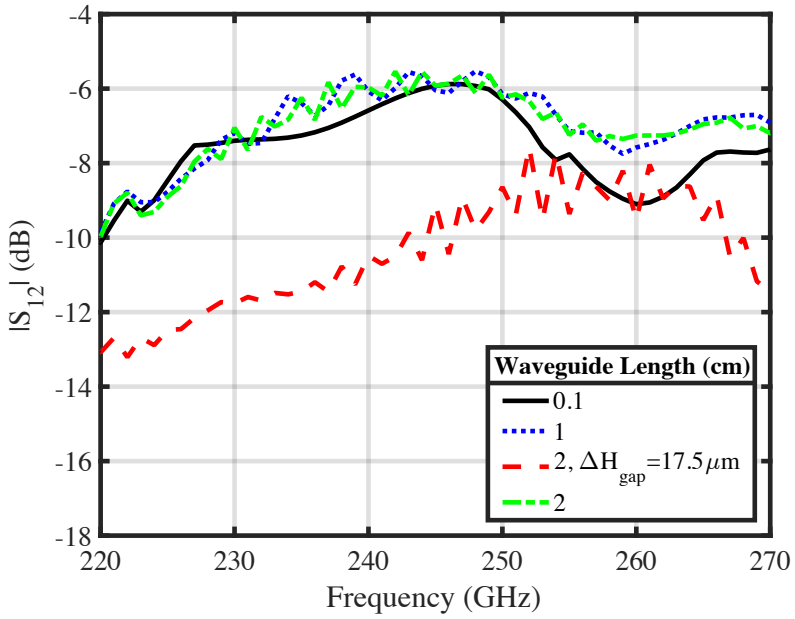


(b)

Figure 3-19: (a) Measured transmission phase response, (b) length-normalized phase response for measured waveguide lengths. From [46].



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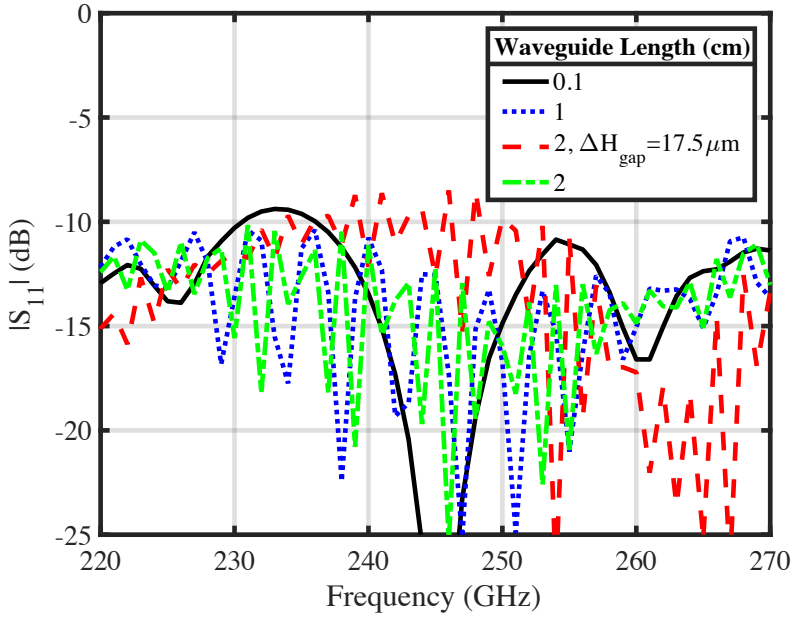


(b)

Figure 3-20: Full-wave simulated coupler-fiber-coupler response with straight 0.1 cm, 1.0 cm, and 2.0 cm waveguide lengths. The 2.0 cm guide is also simulated with gap between the waveguide and coupler surface, ΔH_{gap}, of 17.5 μm to compare with measured data. The simulated coupler and waveguide dimensions are identical to those used in the measurements. From [46].

Table 3.2: Summary of measured and simulated coupler responses.

Average Coupler-Waveguide-Coupler Loss		
Guide Length	Measured	Simulated
0.1 cm	6.2 dB	7.7 dB
1.0 cm	10.2 dB	7.4 dB
straight 2.0 cm	12.2 dB	11.4 dB
bent 2.0 cm	10.7 dB	7.5 dB

dispersion along the waveguide. A flat group delay of approximately 14 ps/mm was measured. For comparison, full-wave coupler-waveguide-coupler simulation results are provided in Fig. 3-20. The average measured and simulated coupler-waveguide loss is presented in Table 3.2. The discrepancy between simulated and measured data is attributed to additional waveguide dielectric loss at sub-mmWave frequencies, measurement inaccuracies, and imperfect waveguide-chip bonding. Lastly, it should be noted that, after accounting for the excess coupling loss present in the 2.0 cm straight guide sample bonds, the 1.0 cm and 2.0 cm average losses over the band are currently estimated at only 0.5 dB/cm. Given this waveguide loss, we estimate the insertion loss of a single coupler is approximately 4.8 dB which agrees well with the simulated data of approximately 3.8 dB per transition. The performance of this inter-chip link system exceeds that of the previous state-of-the-art results. A comparison of available "radio of fiber" coupler performance is provided in Table 3.3.

Table 3.3: Comparison of the presented work with published mm-wave/sub-mmWave radio over fiber couplers.

Ref.	This Work	[34]	[3]	[54]	[30]
Center Freqs.	275 GHz	195 GHz	77 GHz 75 GHz	60 GHz	57 GHz 80 GHZ
BW	50 GHz	8 GHz	35 GHz	6 GHz	6 GHz
Ins. Loss	4.8 dB	5.8 dB	5 dB	6 dB	7 dB (est)
Guide Cross Section	400 μm 250 μm	500 μm 300 μm	850 μm 850 μm	1.6 mm Radius	1.1 mm 8 mm
Notes	1	2	3	2	3

1 On-chip coupler with a planar chip-waveguide interface
2 On-chip coupler with the waveguide attached to the chip at a 90° angle
3 Off-chip coupler with a planar chip-waveguide interface

3.5 Conclusions

In this chapter, a fully-integrated on-chip traveling wave power coupler, based on a differentially-driven Half-Mode Substrate Integrated (HM-SIW) structure, co-designed with a low-cost planar rectangular dielectric waveguide is presented, analyzed, and measured. This structure achieves an insertion loss of 4.8 dB, which is the lowest among all published works in the millimeter-wave frequency band. The increased operating frequency provides the smallest waveguide cross section and the potential for a lower guide-to-guide pitch. A usable bandwidth of more than 50 GHz was measured, providing an opportunity for very high data rate transmission. Additional bandwidth – beyond 100 GHz – is shown available in full wave simulation. This structure provides the most straightforward path for on-chip integration. The proposed coupler structure also enables the simplest implementation of a planar interface between the chip and dielectric waveguide. This simple system-level planar integration makes use of low-cost commercially-available materials already in wide-spread use in the PCB industry.

This structure is demonstrated for the first time at these frequencies, providing smaller guide size, lower pitch, and more available bandwidth than demonstrated in previously-published works. Lastly, the small differences in losses between the 1.0 cm and 2.0 cm samples indicates low loss in this guide material at these frequencies, approximately 0.5 dB/cm. This in-guide loss makes this design viable for link lengths up to approximately one meter.

Chapter 4

Sub-THz Multiplexers for Carrier Aggregation

4.1 Introduction

In Chapter 1, a candidate link is described in which guided and modulated sub-THz (approximately 220-330 GHz) waves are used to transport high-rate data over backplane-scale distances. Such a scheme is attractive for a number of reasons, including broad available fractional bandwidth, compact system size (driven by smaller wavelengths compared to lower-frequency operations), relative robustness to misalignment during assembly versus optical systems, and lower transmission losses than those exhibited by copper lines for high-speed data transmission.

One of the challenges associated with the development of the above link system is the realization of compact, low-loss channelizers. The use of these components is a fundamental requirement to leverage the available waveguide bandwidths. While waveguide-based channelizers have been demonstrated at lower bands and waveguide components are available at higher operating frequencies, they are relatively large and require more expensive packaging and interface schemes. This type of scheme would require a planar integration approach to be economically feasible. On-chip implementation is one option: the use of transmission line-based structures in an integrated circuit (IC) back end of line (BEOL) can produce compact filters, but the loss as-

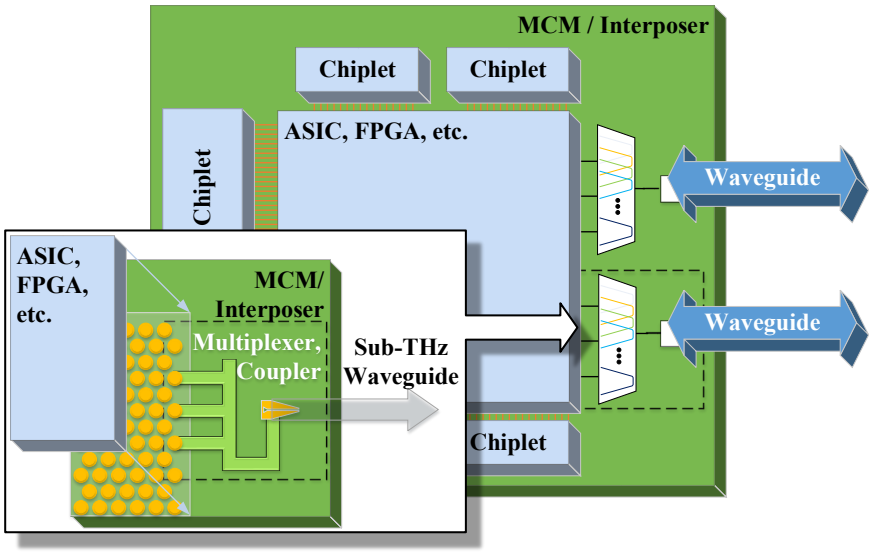


Figure 4-1: A concept of a multi-chip module (MCM) in which high-rate data are aggregated and transported across a wideband sub-THz dielectric waveguide. Inset: an exploded view of the concept with a broadband triplexer, directly-coupled to solder bumps, each driven by an electronic sub-THz transceiver. The combined energy is coupled into a sub-THz waveguide via a broadband coupler. The triplexer structure is outlined in the dotted black line within the inset. From [45].

sociated with radiation and conductor resistance is a disadvantage. SIW filters have been broadly investigated at lower frequencies [5, 8–10] for their superior performance over other planar approaches. There are some published results of BEOL-integrated SIW structures for radiators in the sub-THz regime [21, 46, 49, 104, 107, 108] and a smaller number related to transmission lines [93] and simple filters [82]. There are a few published SIW filter works utilizing LTCC or PCB materials at W-band [103, 106] and above [69]. In [90], a novel thick-film technology was used to demonstrate cavity filters at V-, W-, D-, and G-bands. In comparison to single filter topologies, the use of SIW topologies and techniques for RF multiplexers and channelizers has been relegated to lower frequencies [16, 39]. This may be attributed to the difficulty of designing both manifold [7] and star-junction [64] devices, as well as the design rules and tolerances in available processes.

This chapter discusses the design and measurement of a 220-330-GHz triplexer, for the integration into a high data rate meter-class I/O scheme illustrated in Fig. 4-1.

The concept is shown in further details in the figure inset in which a flip-chip bonded IC with sub-THz transceivers is directly connected to an in-package multiplexer to combine (on transmit) and channelize (on receive) the modulated sub-THz wave. The multi-channel sub-THz energy is coupled to/from the sub-THz waveguide via a wideband planar coupler [46]. To the best knowledge of the authors, there was previously no work utilizing SIW structures for channelizing sub-THz signals.

This triplexer is implemented in a new organic packaging process technology developed by Intel Corporation. This new process features thick copper layers, continuous via bars/trenches, and flexible design rules. The channelizer, based on a manifold topology [7, 32], uses ridged SIW structures for the individual channel filters, and includes broadband ground-signal-ground (GSG) transitions for direct wafer probing. The device is designed for three 30-GHz-wide passbands, with 10-GHz guard bands between channels.

4.2 Organic Packaging Process

The triplexer presented in this work is fabricated on an integrated circuit organic packaging process developed at Intel Corporation employing laminate panels of $\sim$500$\times$500 mm^2 area. The fabrication process is a modified semi-additive microelectronics packaging process (SAP) that allows the creation of continuous and arbitrary shape interlayer trench vias. A high-level fabrication flow of a semi-additive microelectronics packaging process is shown in Fig. 4-2a. The process starts with a patterned copper clad core (CCL) with through holes (step 1). Next, the dielectric build-up film is laminated (step 2). Laser via drilling, cleaning and seed deposition follows (step 3). Via and trace formation are performed via plating and etching (step 4). Steps 2 through 4 are repeated for N metal layers. Finally, solder-resist layer deposition and patterning is performed (step 5).

The stack-up developed features a total of eight metal layers and three build-up dielectric layers around each side of a thicker substrate core. The build-up layers feature low-loss organic based materials with inorganic fillers, while top and bottom sides

of the fabricated package are covered by a solder resist layer. The dielectric layer and the core layer thicknesses targeted are 30 μm and 200 μm, respectively. The targeted copper thickness is 15 μm. Continuous trench vias, favored for the implementation of low-loss SIW structures, are enabled through lithographic processes. These via layers target 30 μm in thickness. Fig. 4-2b shows a cross section of the metal layers (M1-M4) and inter-layer vias (V1-V3) utilized in this work. A ridge structure is also shown in the figure.

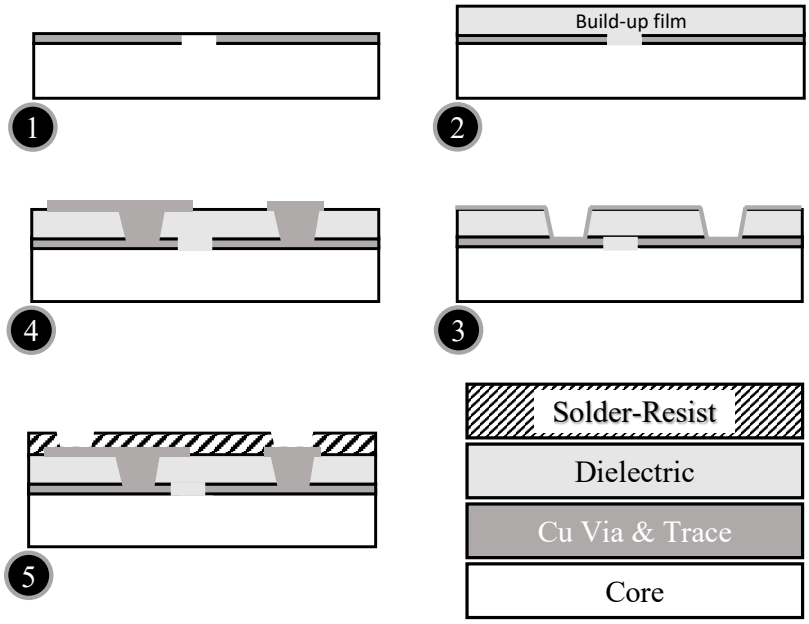
4.3 Triplexer Design

The triplexer is designed to match to 50 Ω at all ports, and has three 30-GHz-wide channels: 220-250 GHz (Channel 1), 260-290 GHz (Channel 2), and 300-330 GHz (Channel 3). For the application described in Fig. 4-1, less than 5 dB of passband insertion loss and better than 10 dB return loss are desired. To prevent cross-channel interference, more than 30 dB of stopband attenuation and better than 40 dB of inter-channel isolation are also required.

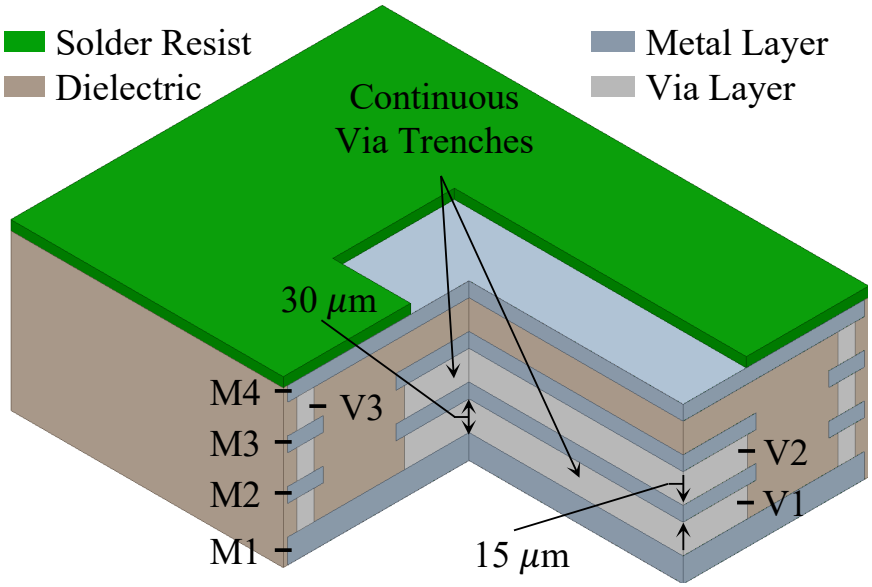
Fig. 4-3 shows a 3D model of the final triplexer design. The structure makes use of ridged SIW resonator sections, described in Section 4.3.1. The individual channel filters and the manifold (common) ports are excited with wideband transitions from GSG probes (Fig. 4-3, upper-right inset). This transition is described in Section 4.3.2. Lastly, a very fast circuit-EM co-design scheme is described in Section 4.3.3 to finalize the triplexer dimensional parameters.

4.3.1 SIW versus Ridged-SIW

Due to the large range of frequencies over which the triplexer must operate, consideration must be given to the spurious passband present in a bandpass filter utilizing a conventional SIW with a rectangular cross section [48, 83]. This leads to an unwanted interaction between Channels 1 and 3. In order to ameliorate this problem, a ridged-waveguide topology is adopted, which takes advantage of the wider frequency range over which only the lowest order mode is allowed to propagate [6, 59].



(a)



(b)

Figure 4-2: (a) A simplified semi-additive microelectronics packaging process flow for N build-up dielectric layers and (b) a graphic illustration of the cross section of the organic packaging process with an integrated ridge (implemented using layers M1-M3 and V1-V2). From [45].

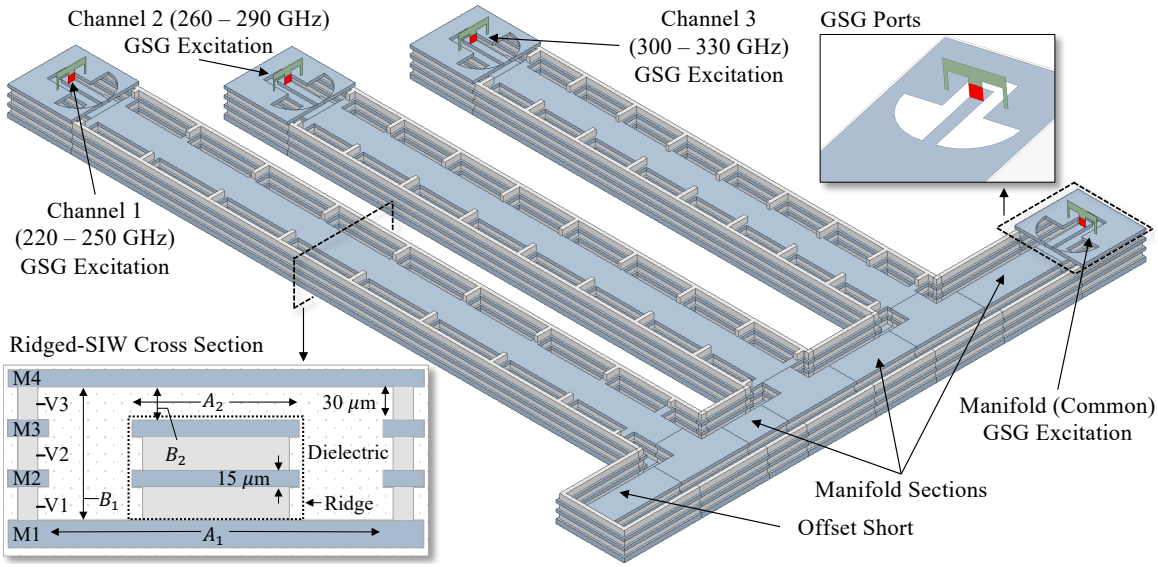


Figure 4-3: An isometric view of a model of the final 220-330 GHz triplexer design. The process' top metal layer, M4, and the dielectric fill material have been removed from the model to reveal the structural details of the channel filters, T-junctions, and connecting manifold. The three channel filter GSG ports are illustrated, along with the manifold GSG port. The lower-left inset shows a cross section of the ridged-SIW resonator sections. The upper-right inset shows a detail on the GSG ports used to simulate and measure the device. From [45].

A ridged-waveguide has a wider spurious-free passband region over the conventional rectangular waveguide. Since the cross-sectional circumference of a ridged waveguide is much longer than a rectangular waveguide (RWG) due to the additional ridge inside the waveguide, the associated cutoff frequency is much lower than that of the RWG with the same size. Due to an irregular shape of the inside of the ridged waveguide (Fig. 4-2b), the transverse resonance method can be used to analyze the structure. The cutoff frequency of a single ridged waveguide can be found by using [15]:

$$f_c = \frac{1}{2A_1\sqrt{\mu\epsilon}} \cdot \frac{2}{\pi}\sqrt{\frac{A_1}{A_2}\frac{B_2}{B_1}\frac{1}{1-\frac{A_2}{A_1}}}, \tag{4.1}$$

where μ and ϵ are the permeability and permittivity of the process dielectric material and A_1, A_2, B_1 and B_2 are the guide dimensions shown in the inset of Fig. 4-3. Additionally, the gap between the top surface of the ridge and the waveguide ground surface has a strong electric field; this capacitive loading increases the cutoff frequency

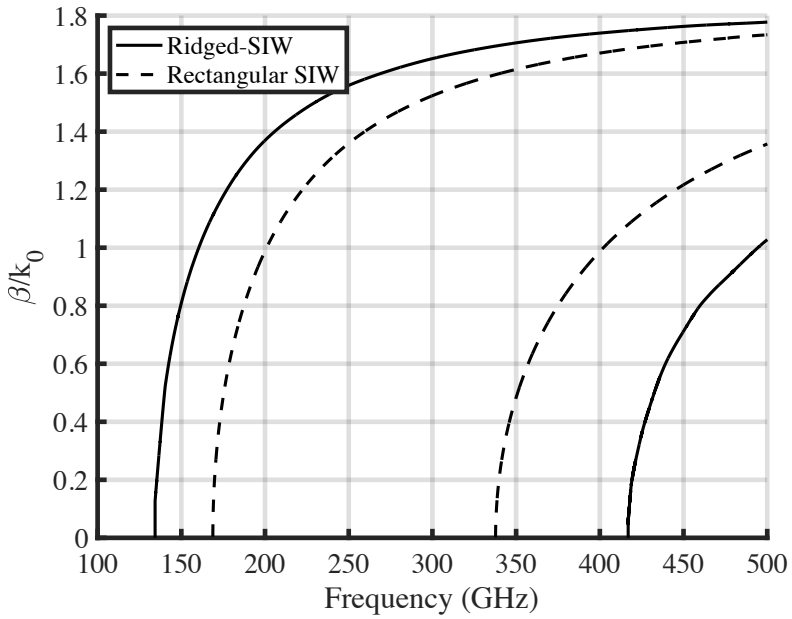
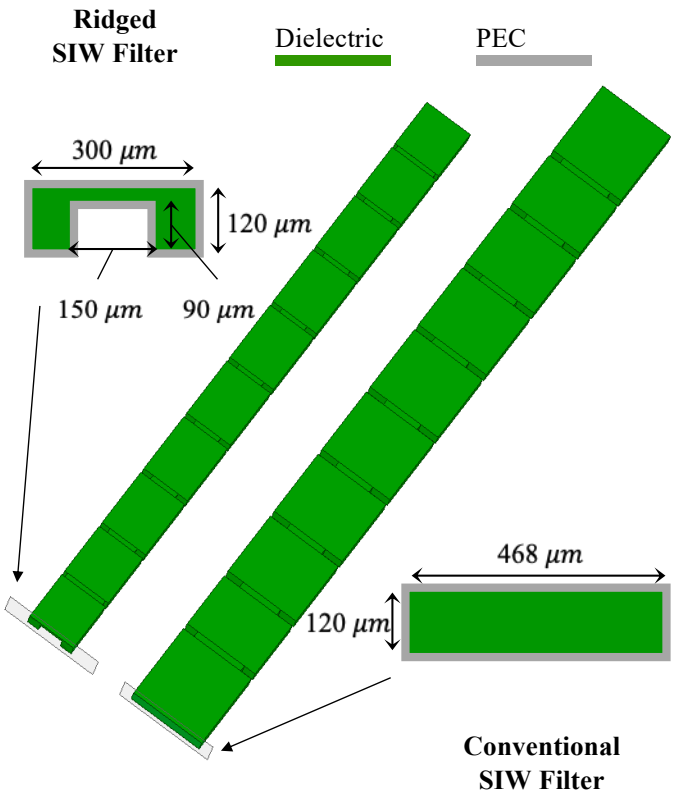


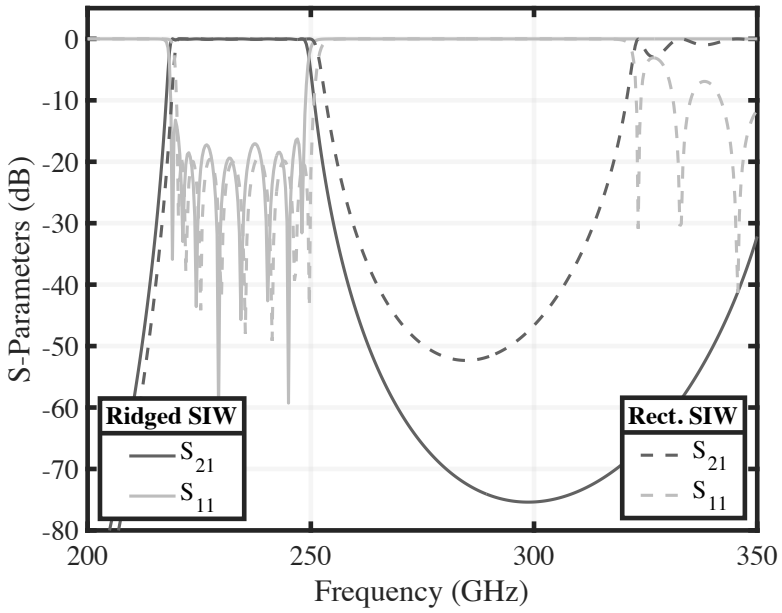
Figure 4-4: Eigenmode simulation of a ridged-SIW section versus a standard rectangular SIW section. From [45].

of the next higher mode operation, compared with the case of a RWG-based resonator. Such a cutoff frequency can be modified by the values of these dimensional parameters B_2 and A_2. By leveraging this wider fundamental-mode bandwidth provided by ridged-waveguide resonators, we realize higher spurious-free stopband suppression than with conventional rectangular waveguides (or SIWs). However, the structure does incur additional insertion loss over conventional RWG-based filters.

As the packaging process provides access to variable ridge heights by using different metal layers, a parametric eigenmode analysis using HFSS [2] is carried out to determine the optimal dimensions for the maximum quality factor Q of an idealized resonator geometry. An overall guide width of A_1=300 μm (Fig. 4-3, inset) and height of B_1=120 μm (utilizing the full process stack) are adopted. A ridge width of 50% of the overall waveguide width (to meet spurious passband requirements) and a ridge height of 90 μm (commensurate with the M3 metal layer) are found to provide the highest available Q: between 233 and 238 across the entire triplexer operating band – including dielectric and conductor losses. These dimensions were used on the subsequent channel filter and triplexer designs. Fig. 4-4 shows the waveguide dispersion



(a)



(b)

Figure 4-5: Full-wave EM simulation of idealized conventional SIW and ridged-SIW filter. (a) Isometric views of the two topologies along with the cross sections of the respective resonant sections; the PEC surrounding the filter structures is removed in the isometric views, revealing the internal dielectric material. (b) S-parameters demonstrating suppression of the unwanted spurious passband. From [45].

results of an eigenmode simulation in which the normalized propagation constants β/k_0 of the first two modes are plotted. As can be seen, *only* the lowest-order mode is supported from 130 GHz to 410 GHz using this ridged SIW cross section, providing 280 GHz of available single-mode bandwidth – far more than the 110 GHz required in this channelizer design. Rectangular SIW dispersion characteristics are also shown for comparison. In this case, the ridged cross section provides an 67% more single-mode bandwidth than the rectangular SIW.

For comparison, a conventional RWG-based SIW filter and a ridged-SIW-based filter, both having eight sections and eight passband poles, are designed using FEST3D [88]. Both filter designs maintain compatibility with the dimensions available in the organic packaging process described in Section 4.2, and they are optimized to meet the same passband bandwidth, insertion loss, match, and adjacent band suppression figures. Shown in Fig. 4-5a, the ridged SIW filter is ∼40% more compact. The resultant 3D structures are simulated using HFSS. The simulated S-parameters are shown in Fig. 4-5b and verify that the ridged-SIW topology indeed improves the spurious passband performance by >50 dB and increases the adjacent channel stopband suppression by ∼10-25 dB across the 260-to-290 GHz band.

4.3.2 Wideband Ridged-SIW to GSG Transition

In order to measure the triplexer in the WR-3.4 band, transitions to GSG pads for on-substrate probing had to be integrated. To facilitate rapid design, a single wideband transition was designed into the packaging process, simultaneously providing the pads for probing, waveguide mode conversion, and impedance matching. An approach based on the technique presented in [117] was used. In the previous work, a short section of slot line was used to produce the match between a GSG probe and a SIW at W-band. As the presented triplexer operates over a large fractional bandwidth (40%), a broader bandwidth match was required.

Fig. 4-6a shows the transition structure. The top metal layer was used to realize the pad landings. The pads are terminated with broadband opens realized as circular slots. The interposer process provides flexible conductor design rules, including curved

Table 4.1: Dimensions of the GSG-Pads to Ridged-SIW Transition

Parameter	**Dimension (μm)**	**Parameter**	**Dimension (μm)**
A_1	300	A_2	150
A_3	45.7	R	130
D_p	93.5	L_{match}	330
W_d	43.1	W_p	35
W_s	33.8	ΔP	113

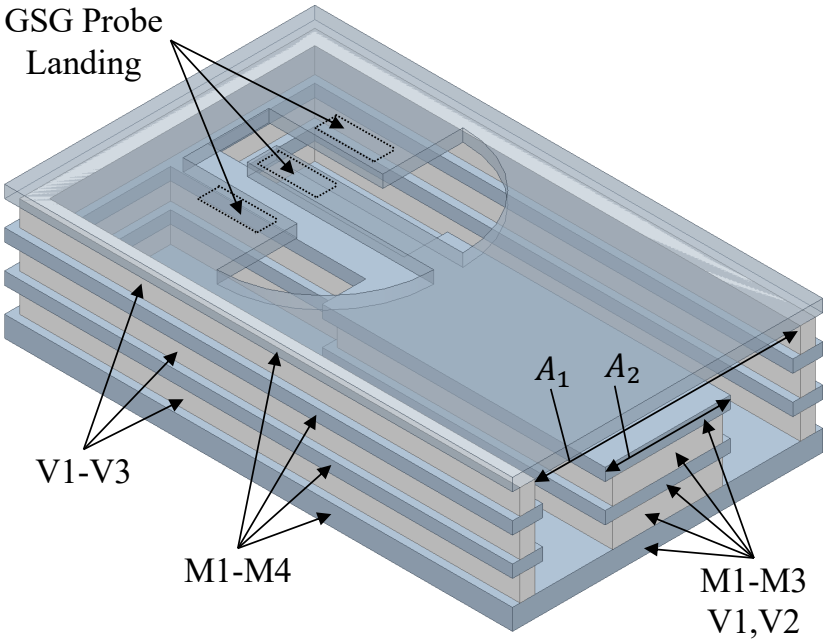
geometries. This flexibility allows for the design of this type of broadband open termination. A symmetric lumped port mimicking the wafer probe is used to excite the GSG pads. The values of the dimensional parameters (illustrated in Fig. 4-6b) of the transition are listed in Table 4.1.

Fig. 4-7 shows the simulated S-parameters of the transition. Across the entire 200-to-320 GHz band, the return loss is better than 8 dB and the insertion loss is better than 3 dB. The slight mismatch below 250 GHz and above 320 GHz was compensated in the final design by absorbing the transition response into the final triplexer end-to-end response.

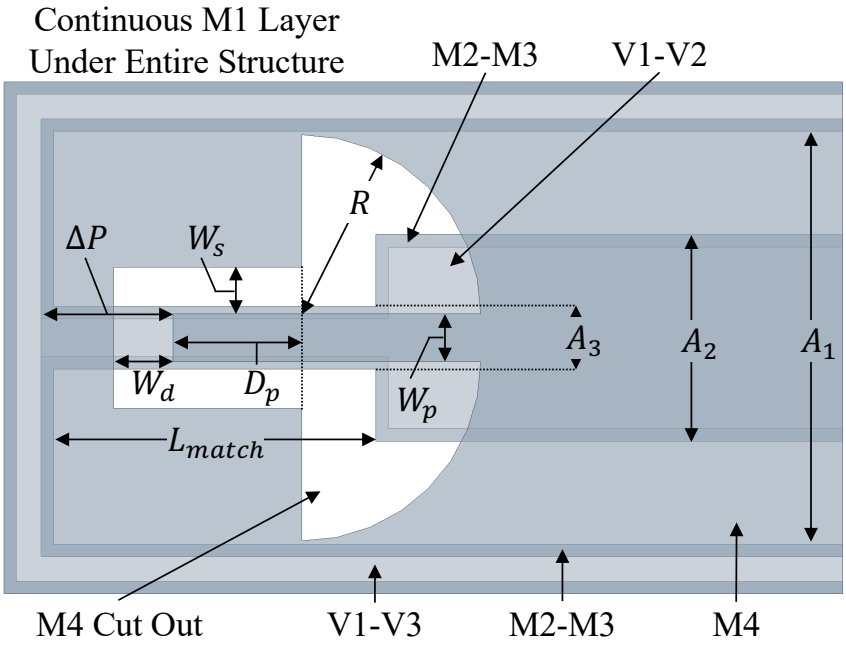
4.3.3 EM-Circuit Model Co-Design

Full-wave parametric design and optimization of complicated electromagnetic structures can be time consuming and expensive. Assuming a triplexer utilizing *asymmetric* eight-pole channel filters, the overall triplexer would require tuning over at least 61 parameters. This figure includes nine iris widths and ten waveguide lengths per channel filter, and four manifold spacing lengths between each of the channel filters.

Instead, a method, which is based on a EM-circuit co-design and similar to that presented in [38] and [95], was utilized to rapidly converge on a set of design parameters. In this case, a waveguide cross section was first set (A_1=300 μm and A_3=150 μm in Table 4.1), and a straight section of ridged SIW was modeled with an inductive iris. This iris width was varied and broadband full-wave simulations were performed in HFSS, with waveport de-embedding used to move the reference plane immediately adjacent to the iris (Fig. 4-8). In addition, a ridged SIW T-junction was modeled and de-embedded ($\mathbf{S_T}$) to remove the response of a feed waveguide with a finite length.



(a)



(b)

Figure 4-6: (a) An isometric view and (b) a top view of the broadband GSG to ridged-SIW transition. The dielectric filled in the structure is not shown. From [45].

The resultant parameterized S-parameter files are used in a circuit simulator to model the reactive response of the iris, $\mathbf{S_{Wi,k}}$ corresponding to the frequency response

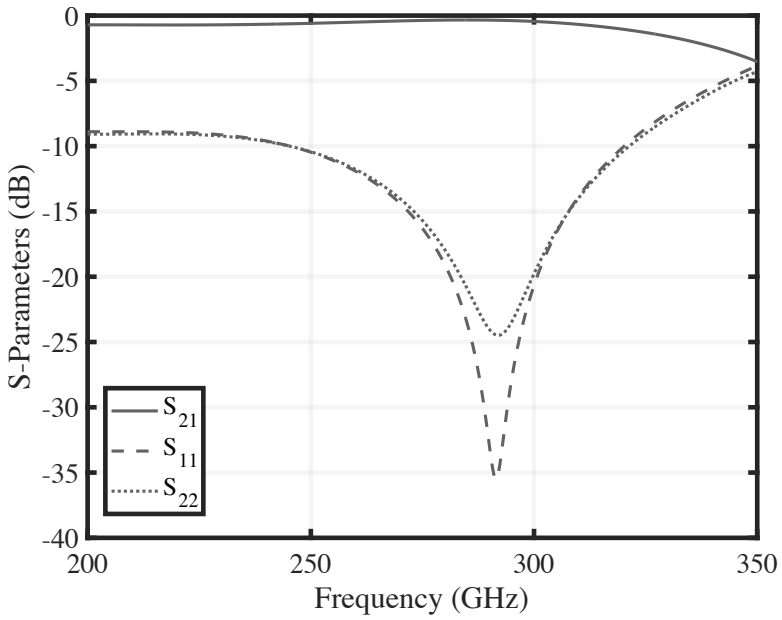


Figure 4-7: Full-wave simulated S-parameters of the wideband GSG-to-ridged-SIW transition, designed in the interposer process. Port 1 corresponds to the GSG probe port, and port 2 corresponds to the ridged SIW port. From [45].

of the k-th iris in the i-th filter with iris opening width $W_{i,k}$ (Fig. 4-9). The responses of lengths of ridged-SIW (corresponding to parameter $L_{i,k}$ in Figs. 4-9 and 4-10) is based on a ports-only full-wave solution for the guide cross section, with the propagation constant and attenuation (β and α, respectively) extracted. These transmission line responses are modeled in the same circuit simulator, parameterized by guide length. These parameterized iris responses were integrated into a full triplexer circuit model (Fig. 4-10) incorporating the wideband GSG probe transition $\mathbf{S_P}$, and the T-junction response $\mathbf{S_T}$. Full-wave parametric design and optimization of complicated electromagnetic structures can be time consuming and expensive. Assuming a triplexer utilizing *asymmetric* eight-pole channel filters, the overall triplexer would require tuning over at least 61 parameters. This figure includes nine iris widths and ten waveguide lengths per channel filter, and four manifold spacing lengths between each of the channel filters.

Each channel filter is connected through a certain length of single-ridge waveguide ($L_{i,1}$ in Fig. 4-10) to provide a proper phase compensation between channel filters.

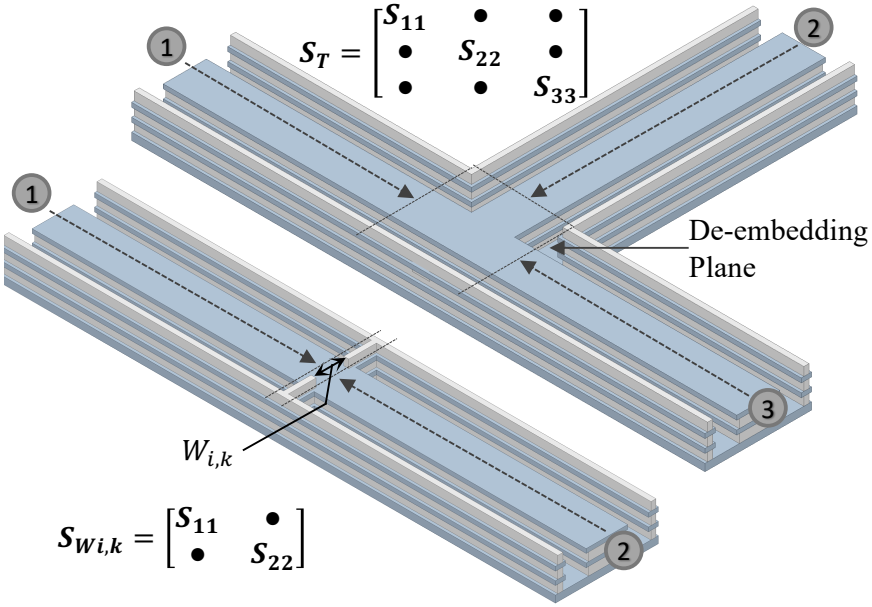


Figure 4-8: Full-wave models of ridged-SIW building blocks. Parameterically-varied inductive iris widths are used to model $\mathbf{S_{Wi,k}}$, and a ridged-SIW T-junction to model $\mathbf{S_T}$. The top copper layer is removed from the isometric images to reveal features within the structures. The arrows in the overhead views denote the full-wave de-embedding to the ultimate block reference planes. From [45].

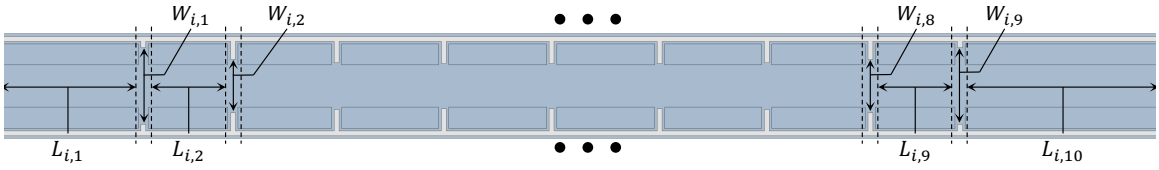


Figure 4-9: The top view of a full-wave model of a parameterized, asymmetric, 8-pole ridged-SIW bandpass filter utilizing inductive iris coupling. The structure's top copper layer is removed in this view to reveal structure within the filter. From [45].

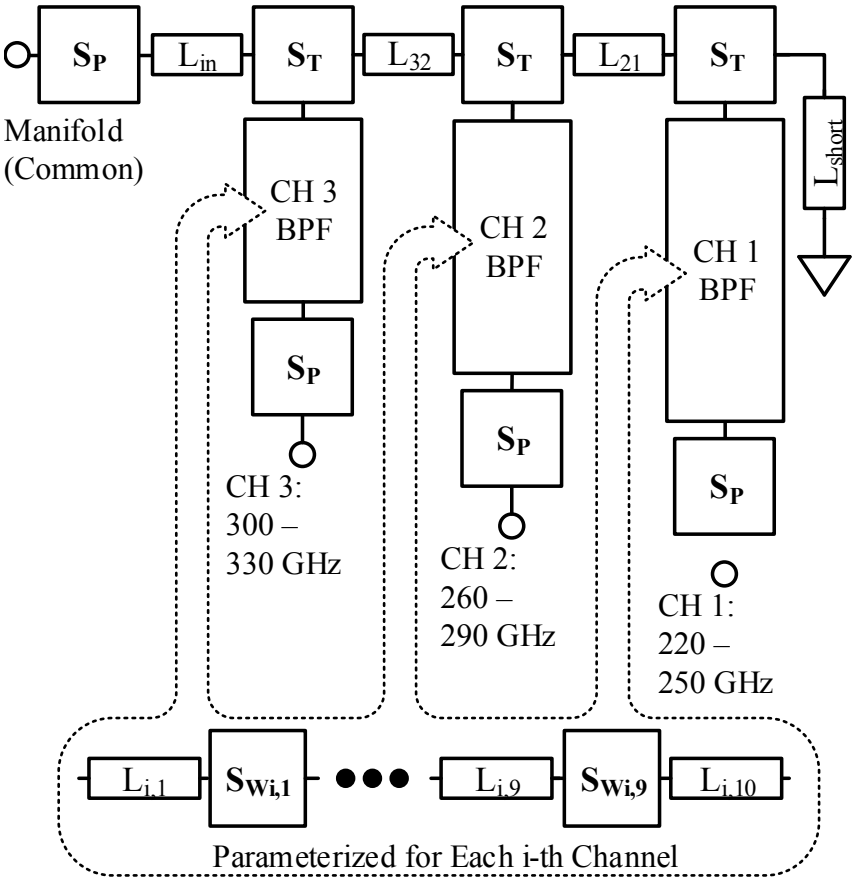


Figure 4-10: The circuit model used in the EM-circuit co-design of the presented triplexer. Each bandpass filter is composed of fully-parameterized lengths of waveguide and s-parameters, parameterized by width, representing the inductive irises. From [45].

The connecting manifold lengths (L_{32}, L_{21}, and L_{short}) are determined to provide an open-matching in the center frequency of the neighboring channels.

Interpolation of the previously-generated iris responses, $\mathbf{S_{Wi,k}}$, was utilized in the S-parameter circuit simulation to rapidly optimize the triplexer parameters *in the circuit domain*. The triplexer was optimized for a flat passband and return loss. A 10 GHz guard band was utilized between each channel, and the design was optimized for better than 10 dB return loss at the output of each channel filter. The resultant circuit simulator-generated dimensions were utilized in a fully-parameterized full-wave model of the overall design (shown previously, in Fig. 4-3). The results for both the circuit-EM model and the full-wave model are plotted in Fig. 4-11. It should be noted that *no post-circuit-design optimization was done utilizing the full-wave model.* As full-wave simulation of the entire triplexer structure required orders of magnitude more time (more than an hour compared to fractions of a minute when utilizing the circuit model), further full-wave optimization was not practical. The results show excellent agreement between the two simulated responses.

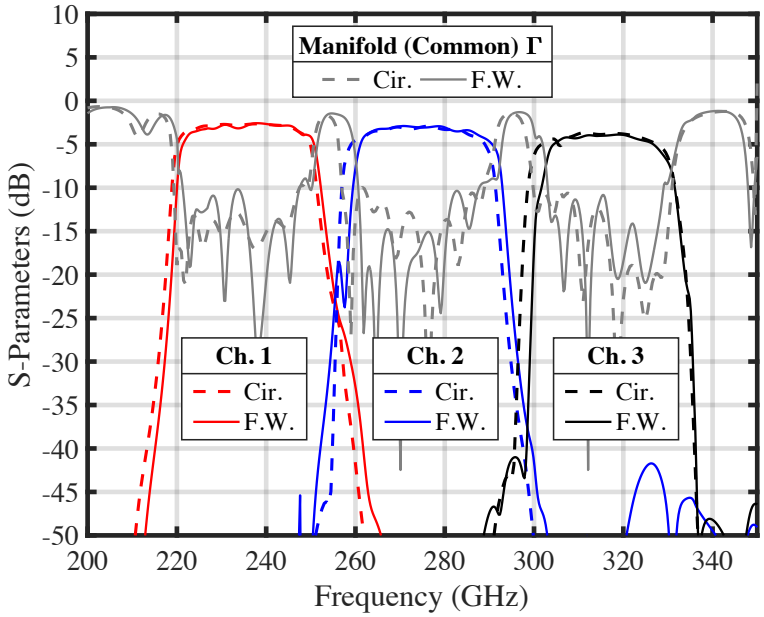
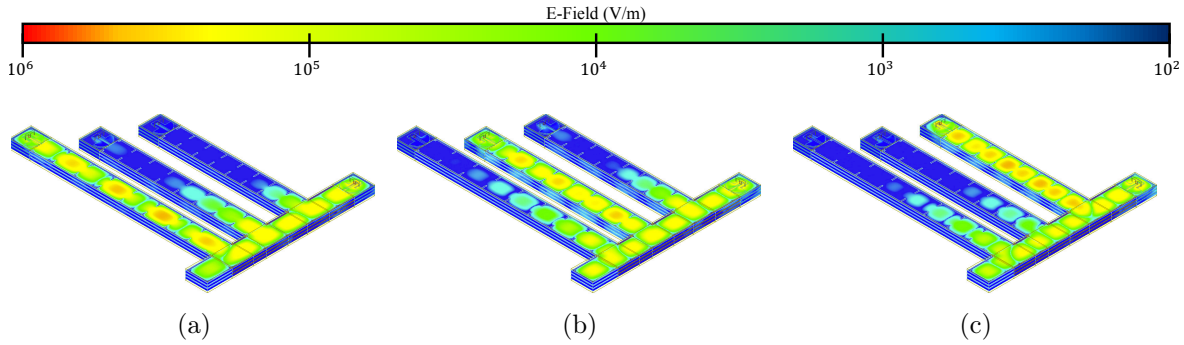


Figure 4-11: A comparison of the simulated responses of the circuit-EM co-design triplexer (dashed lines) and the full-wave triplexer response (solid lines). From [45].

The manifold reflection Γ, Fig. 4-11, shows a good match across all the designed



(a) (b) (c)

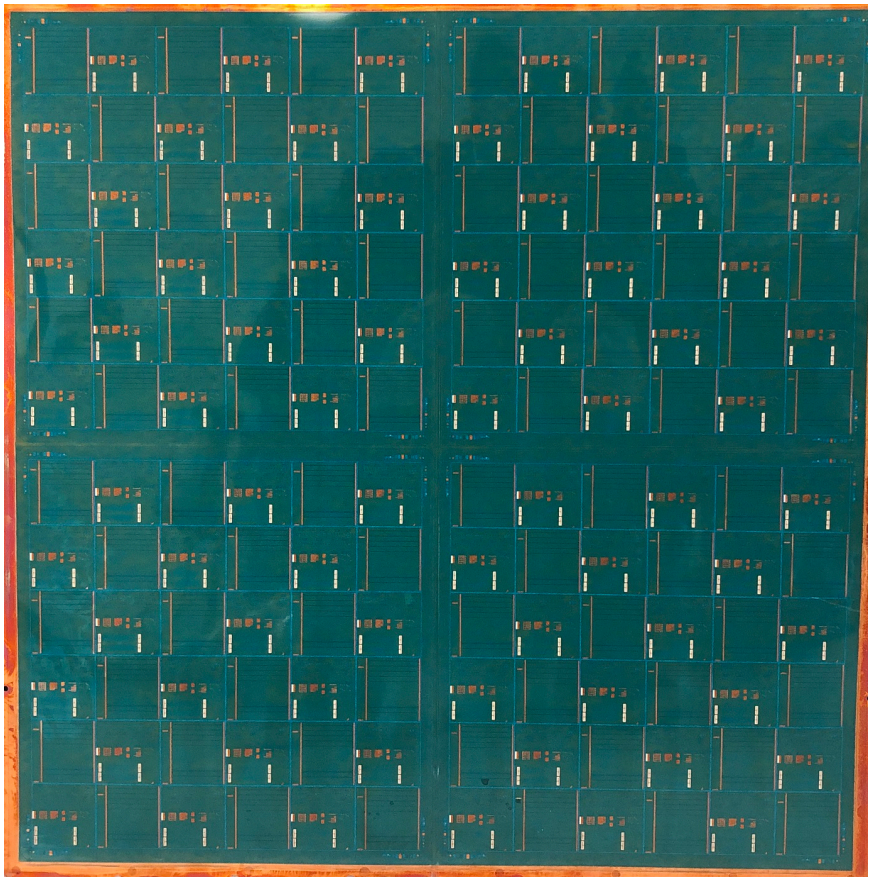
Figure 4-12: A plot of the E-field intensity on the triplexer conductor surfaces at (a) 235-GHz, (b) 275-GHz, and (c) 315-GHz. These frequencies correspond to the centers of the three passband channels. From [45].

passbands, with a reflection between the passbands. This is expected given the non-contiguous design. In addition, the full-wave model was used to generate plots of the magnitude of the E-field on all the device conductors in Fig. 4-12. The three plots demonstrate the passband characteristics of the device at the designed center frequencies of the three channels. The figure also demonstrate that the channel filters effectively suppress the out-of-band energy injected into the channelizer from the manifold or the other channel filters.

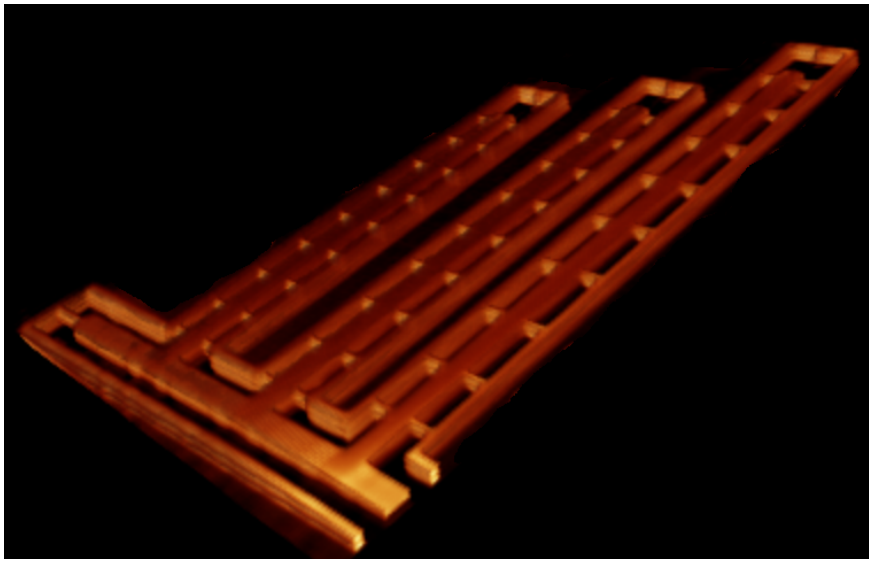
4.4 Experimental Results

4.4.1 Fabrication

All designs were fabricated at Intel Corporation, Chandler, AZ facility. The process provides a feasible means to realize highly-scalable, higher-performance electromagnetic structures. Fig. 4-13a shows a fabricated panel, sized 500 mm x 500 mm, made up of copies of designed test structures. A 3D X-ray view of the fabricated triplexer is shown in Fig. 4-13b. A photo of a portion of the fabricated devices, with the triplexer and individual channel filter locations denoted, is shown in Fig. 4-15. The GSG pads and the wideband ridged-SIW transitions implemented in the top copper layer are revealed through the solder resist layer openings.



(a)



(b)

Figure 4-13: (a) A fabricated 500 mm x 500 mm panel made up of repeated test designs, and (b) a 3D X-ray image of the fabricated triplexer on Intel's organic packaging process. Note that the top and bottom metal layers have been intentionally hidden to allow a view of the internal ridges and SIW resonator cavities. From [45].

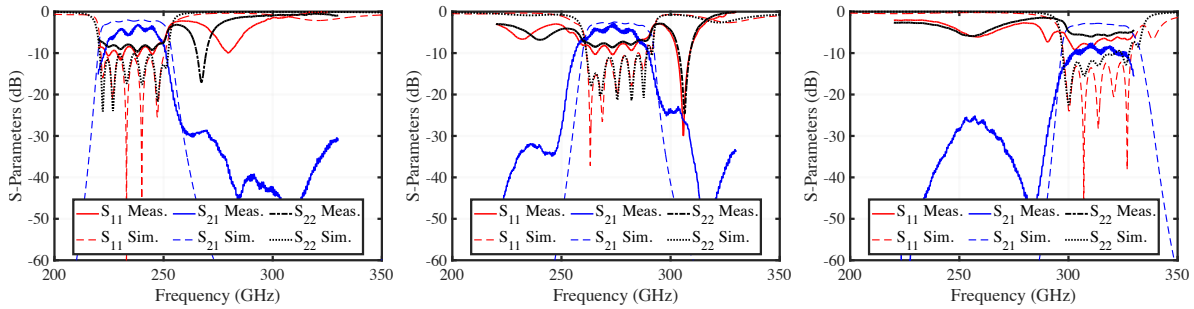


Figure 4-14: A comparison of three individual *channel filters*, with wideband GSG transitions at both ends of the filters. (a) Channel 1 (220-250 GHz). (b) Channel 2 (260-290 GHz). (c) Channel 3 (300-330 GHz). The measured data is depicted as the solid line, with the corresponding full-wave simulation results shown as dotted lines. The forward transmission (S_{21}) and both ports' reflection (S_{11} and S_{22}) are plotted. From [45].

4.4.2 Individual Channel Measurements

Three individual channel filters (Fig. 4-15, left), incorporating wideband GSG transitions on *both sides* of the filter structure were fabricated and measured. These filter designs are identical to the channel filters optimized for use in the triplexer. When measuring the individual channel filters the probes are co-linear. This co-linear geometry also allows the use of standard one-tier probe calibration using commercial available calibration standards. The measured and simulated data is plotted in Fig. 4-14. There is good agreement between the number and location of the passband poles, indicated by the location of the resonances in the input reflections (S_{11}, S_{22}) – especially in the lower two channels. The measured data is within 2-4 dB of the simulated passband S_{21} in the bottom two channels. The top channel (Fig. 4-14c) demonstrates a larger discrepancy between simulated and measured data of up to 7 dB in the mid-band.

Unanticipated out-of-band resonances can be seen in all three measurements (S_{11}, S_{22}, and S_{21}) outside of the individual channel passbands. For example, in Fig. 4-14a, we see a discrepancy due to a passband pole at approximately 260 GHz. Similarly, in Fig. 4-14b, unintended passband poles are placed outside the desired passband (260-290 GHz) at approximately 240 GHz and 305 GHz. We also see an unintended

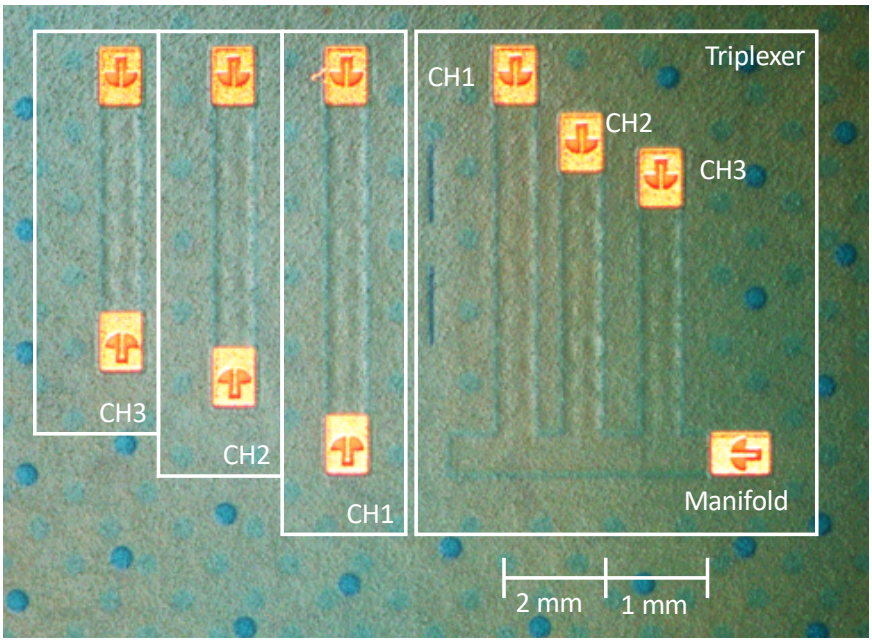


Figure 4-15: Micrograph of the standalone channel filters (left) and the complete triplexer (right). From [45].

transmission in channel 3 (Fig. 4-14c) at approximately 255 GHz. Given the exact number of resonators in each filter, we assess that these unanticipated portions of the responses are due to slightly misplaced passband poles. These effects are due to either small differences in the packaging dielectric properties, small perturbations in the fabricated devices (vertically or laterally), or both. These un-anticipated responses are responsible for the reduction in the measured passband bandwidths and the poorer input match compared to the simulated response.

4.4.3 Triplexer Measurement

The frequency of operation precludes performing measurements with more than two ports. Additionally, the design did not include resistors and the use of discrete resistors at these frequencies is impractical. These factors dictated two-port measurements with the remaining device ports un-terminated (open).

As can be seen in the photo in Fig. 4-15, the manifold and individual channel filters in the triplexer are not co-linear. The device testing is done via 100 μm-pitch wafer probes; at these frequencies, no commercially-available calibration substrates

are available that account for the 90° relative orientation between the channel filters and the triplexer manifold. Instead, a tiered calibration scheme was utilized to calibrate to the probe tips. As was described in Section 4.3, the response of the wideband GSG probe to ridged-SIW transition was *absorbed* into the overall triplexer response. This allows the full device response to be tested by simply calibrating to the wafer probe tips.

The test setup, pictured in Fig. 4-16, consists of a Keysight PNA-X four-port Vector Network Analyzer (VNA), two Virginia Diodes (VDI) WR-3.4 frequency extenders, and two Cascade Infinity WR-3.4 GSG probes. Several straight sections of WR-3.4 and H-plane bends are used to position the waveguide probes appropriately for testing the triplexer.

When measuring the triplexer design, a multi-tier calibration scheme (including an unknown-through calibration [28]) is used to deembed the measurement setup from the device measurement:

1. A small section of WR-3.4 bend is characterized ($\mathbf{S_{bend}}$) independently after performing a two-port flange-flange calibration on a separate setup. The phase response of this section will be used in the subsequent unknown-through calibration.

2. Each VNA extender calibrated to the waveguide flange using a vendor-supplied waveguide calibration kit.

3. Each probe ($\mathbf{S_{left}}$ and $\mathbf{S_{right}}$) is characterized using the previous flange calibration to a set of vendor-supplied short, open, and load (SOL) standards on a calibration substrate.

4. The waveguide sections are attached to the VNA extenders up to the probes; the probes are not connected. A two-port unknown through calibration is utilized to move the calibration plane *up to* the probe flanges.

5. Lastly, the probes are mounted and the measured $\mathbf{S_{left}}$ and $\mathbf{S_{right}}$ responses for the left and right probes are used in the VNA to performer the final layer of deembedding to the probe tips.

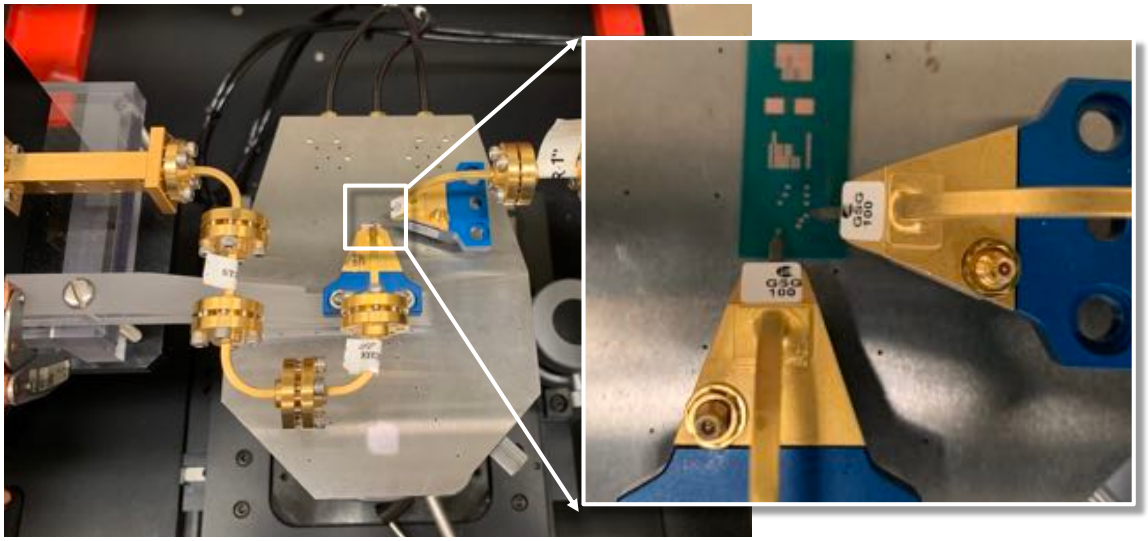


Figure 4-16: Wafer-probe characterization of the triplexer. From [45].

At this point, the measurement setup is calibrated to a reference plane at the probe tips. The two-port device measurements can be taken. To account for larger calibration errors that were observed for wideband calibrations (when compared to a test standard), this process was carried out for three sets of measurements. Each calibration and measurement covered 50 GHz of bandwidth: 220-270 GHz, 250-300 GHz, and 280-330 GHz. Each waveguide calibration was followed by the measurement of an offset short standard to ensure good calibration across the observation bandwidth. The plotted response includes averaging of those overlapping portions of the bands from each measurement (i.e. 250-270 GHz and 280-300 GHz).

The simulated full-wave response in Fig. 4-11 is based on 50 Ω ports connected to all four triplexer ports. This full-wave four-port was simulated in three separate situations in Keysight ADS® with the manifold (input) port connected and one of each of the channel filter ports connected. These simulated channel responses are plotted against the measured response in Fig. 4-17 and Fig. 4-18.

The frequency band is limited to no lower than 220 GHz due to the Virginia Diodes VNA extender and the available waveguide probes (WR-3.4) in the test setup. Fig. 4-17 shows the measured and simulated transmission of a two-port response of the triplexer structure; this represents a measurement (or simulation, shown with the

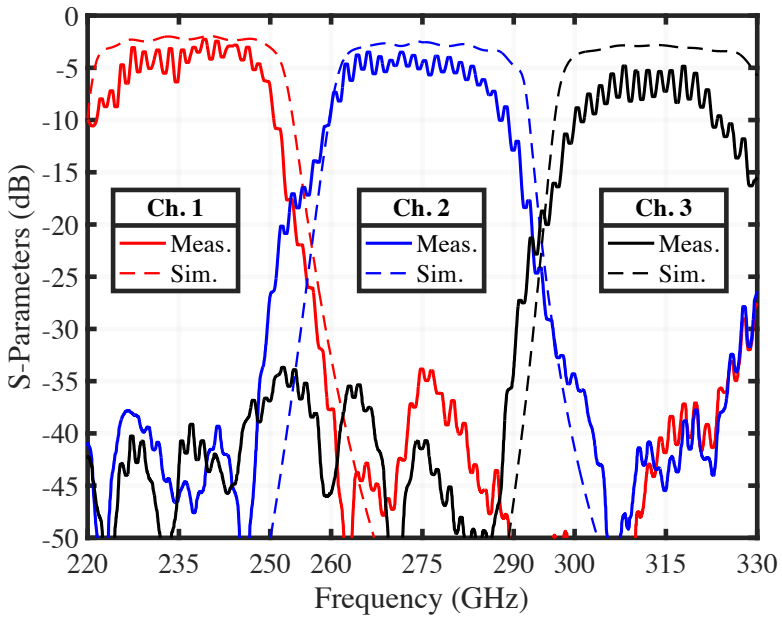


Figure 4-17: Measured triplexer (two-port) response (solid lines) and the simulated two-port triplexer response based on a full-wave four-port model (dashed lines). The plotted data depicts the forward transmission of the two-port measurements, from the manifold to individual channel filter output ports. From [45].

dashed line) between the manifold and the associated channel filter output port. The other ports are un-terminated. The measured data was smoothed with a 800 MHz wide Gaussian window. As can be seen in Fig. 4-14, the passband and stopband behaviors of the device correspond very well to the simulated response. The higher-frequency ripple seen on the measured data is associated with phase mismatch between the VNA and the VDI frequency extenders. During calibration, phase mismatch is compensated for, but during measurement any gross movement associated with the re-positioning of the on-platen micro-positioners, etc. manifests itself as this type of high-frequency ripple.

Fig. 4-18 shows the measured and simulated channel filter reflection of the same scenarios. In this case, a 2 GHz wide Gaussian window was used to smooth the data in order to resolve the structure in the channel filter reflections in channels 2 and 3. Again, the in-band response corresponds to the channel filter. The match in bands 2 and 3 from 220-250 GHz demonstrate an imperfect out-of-band reflection for those

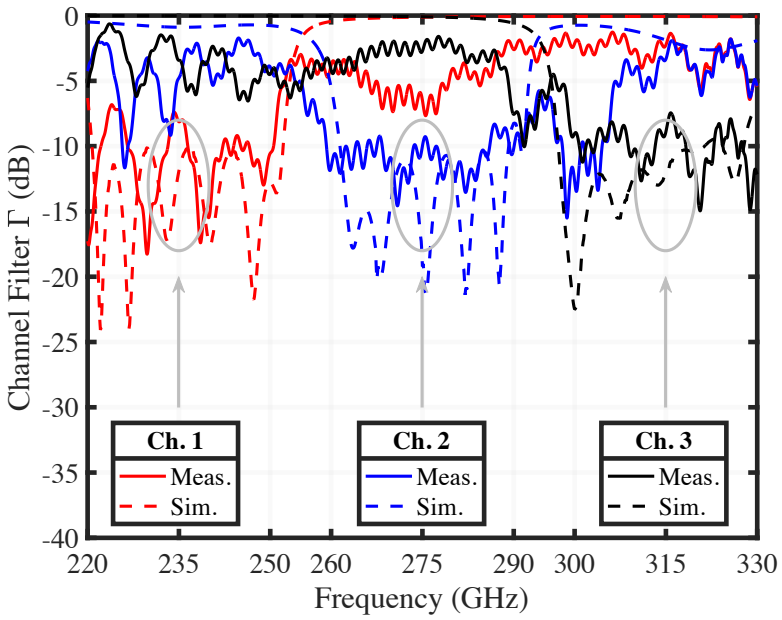


Figure 4-18: The measured channel filter reflection of the triplexer (solid lines) and the simulated reflection based on a full-wave four-port model (dashed lines). This data corresponds to the S_{22} measurement of a set of simulated and measured two-port tests. From [45].

channels that will likely degrade the channel-to-channel isolation.

The mid-band insertion loss is approximately 2-4 dB larger than the simulated data. This may be attributed to losses associated with calibration and wafer probing and un-modelled copper roughness. There is some undesired spurious stop-band transmission, which also may be attributed to imperfect calibration – especially at the lower signal to noise ratios physically present at the VNA extenders in the stopbands. Lastly, one can see the channel bandwidths are more narrow than the device design. This is likely a function of small perturbations in resonator frequency and inter-resonator coupling. These could arise from small changes in fabricated dimensions or differences between modeled and fabricated material dielectric properties. Probe landing locations can also be a source of inconsistency in the measurements. However, large changes in the measured responses were not observed with different positioning of the probes relative the wideband transition pad openings. This may be attributed to the highly confined nature of these ridged-SIW structures and well-designed port

matching.

4.5 Conclusion

The measured channel filters and triplexer responses demonstrate the efficacy of the presented device and design methodology. This represents the first published instance of a ridged-SIW multiplexer implemented at these frequencies and operating over the demonstrated bandwidth. Furthermore, this work represents the first measured devices on an organic packaging process featuring continuous trench vias. Lastly, this work also represents the best performance at these frequencies for these types of devices implemented in organic packaging technologies.

Table 4.2: Performance Comparison With Published Work

Work	**Oper. Band (GHz)**	**MUX FBW**	**Ch. FBW**	**IL (dB)**	**Size (λ_0^2)**	**Res. Type**
This Work	220–330	40%	∼10%	∼3-7*	0.7-1.1*	Ridged SIW
[58]	525–625	17%	∼3%	∼0.5	199	Photonic Crystal
[55]	675–700	18.5%#	3.6%	∼2.1	-	RWG
[102]	305–357	-	15.4%	1.5	2.0	SIW
[118]	330–349	-	5.3%	0.6	1.9/542$^{\$}$	RWG

* - Per channel filter, incl. GSG transition. # - Estimated. $ - Packaged size.

While we are unaware of any comparable published multiplexer implementation for this sub-THz application, the closest comparison in Table 4.2 is that shown in [58], though that work does not include any measurement results. It is a three-band channelizer over 525-625 GHz. However, the multiplexer bandwidth is 17% (compared to the 40% in the presented work) due to the narrow channel filter bandwidth. As was discussed in Section 4.1, the device operating band is of the utmost importance. As such, fractional bandwidth of the multiplexer is an important figure of merit. The remaining comparisons [55, 102, 118] are sub-THz band single-channel filters and are listed to compare the fractional bandwidth of the single filter with our channel filter

design. We note [102], in particular. This work compares favorably from a channel-filter perspective. However, as described in Section 4.3.1, the spurious passband performance precludes the realization of wide operating band triplexers.

The device performance can, in the future, be improved by carefully characterizing the process material properties in the designed band, along with the achievable fabrication tolerances and variations. These factors can be used to future improve the design of the channel filter and overall triplexer response by ensuring the location of the passband zeros. We expect that this will not only improve passband insertion loss and channel-to-channel isolation, but also improvement manifold and channel filter matching.

The presented devices along with Intel's organic packaging process provide an attractive option for new, low-cost, high-performance, in-package filters and multiplexers, that can be readily integrated with existing IC infrastructure. The availability of these components can enable the realization of new millimeter wave and THz systems.

Chapter 5

End-to-End Link Demonstrator

5.1 Introduction

An end-to-end link demonstrator was pursued to realize and validate the concept and architecture outlined in Chapters 1 and 2. In order to demonstrate a prototypical link, the high-order multiplexer and ultra-broadband waveguide coupler developments previously discussed are applied. The link demonstrator, shown in Fig. 5-1, is im-

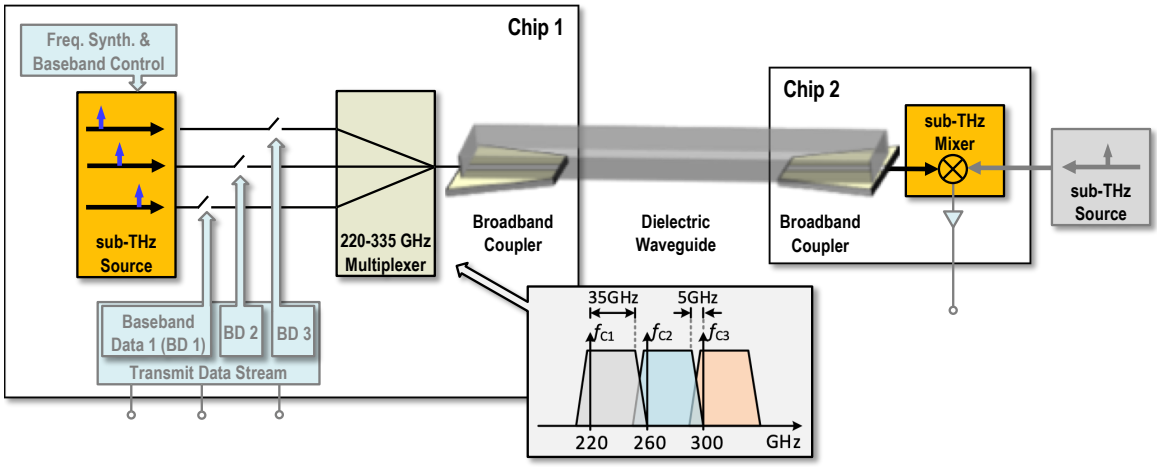


Figure 5-1: A high-level block diagram of the implemented prototype link.

plemented in IHP 130nm SiGe BiCMOS technology. Two chips are implemented, realizing a three-channel transmitter and a single-channel receiver. The transmitter chip incorporates a multiplexer, and both the transmitter and receiver include

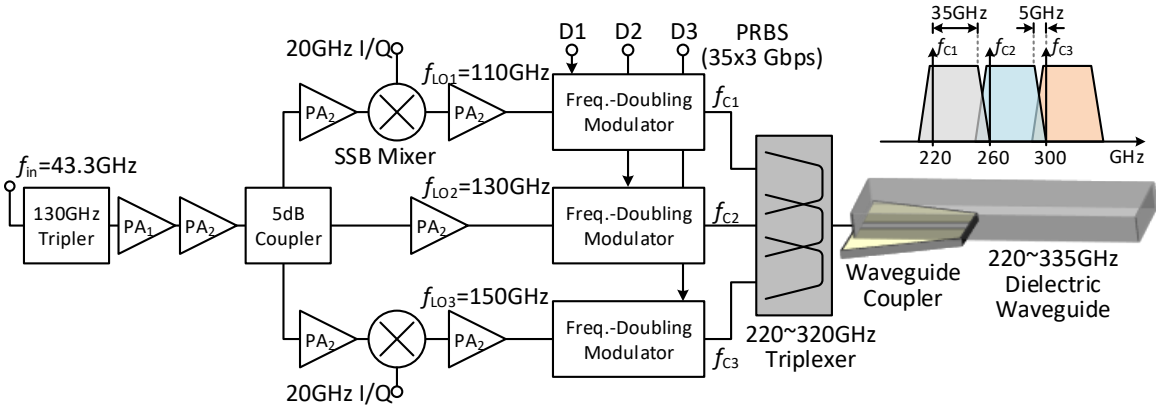


Figure 5-2: The block diagram of the transmitter chip. From [44].

monolithically-integrated waveguide couplers. The demonstrator is shown to achieve 105 Gbps (3x35 Gbps channels). To demodulate each channel, the 35 Gbps coupler-integrated receiver coherently down-converts and demodulates the data. The link, including the chipset and a 0.4 mm-wide, 30 cm-long dielectric ribbon, experimentally demonstrates the potential speed, efficiency, size and cost advantages of sub-THz fiber links in high-speed inter-server and backplane fabrics.

5.2 Architecture

5.2.1 Three-Channel Transmitter

The transmitter chip block diagram is shown in Fig. 5-2. It divides a waveguide single-mode operating band ranging from 220 GHz to 340 GHz into three 35 GHz-wide channels. Two guard bands, each approximately 5 GHz wide, are inserted to ensure isolation between adjacent channels. The transmitter consists of three sub-harmonic LO paths generating signals at f_{LO}=110, 130 and 150 GHz.

130 GHz Amplifier Multiplier Chain

The 130 GHz signal is obtained from a frequency tripler with a 43.3 GHz input (Fig. 5-3a), composed of a conventional tripler followed by a common base buffer for interstage matching. This 130 GHz signal is then amplified by cascode power

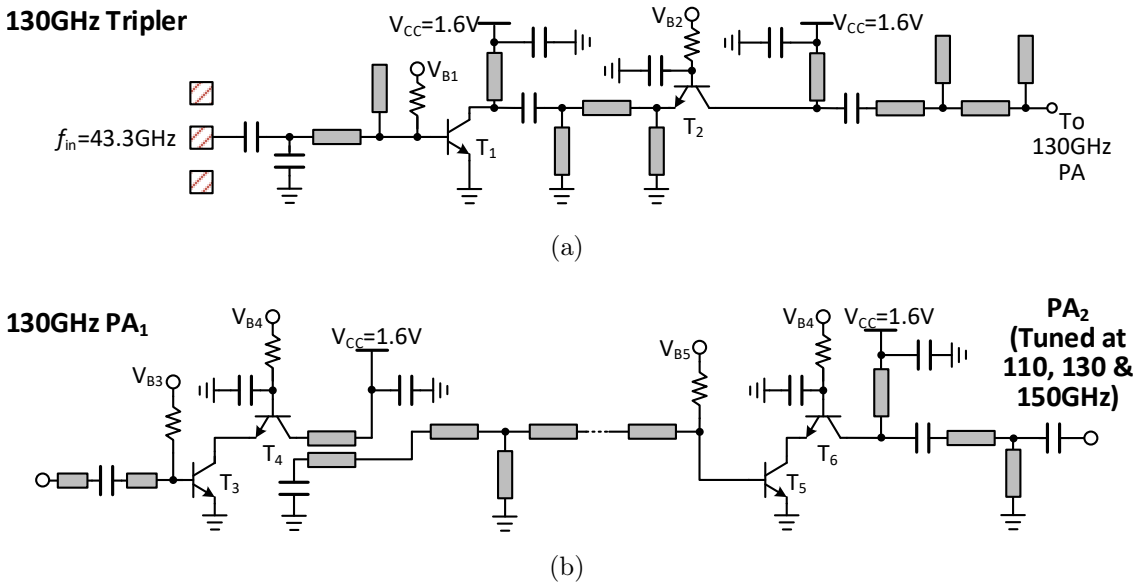


Figure 5-3: Schematics of the local oscillator seed frequency tripler (a) and the cascaded cascode amplifiers (b) use to generate transmit subharmonic carriers. From [44].

amplifier stages, shown in Fig. 5-3b. PA1 is utilizes a broad-side coupled microstrip resonator that acts as an impedance transformer, optimizing the impedance match with the input of the following PA2 stage. The transmission line resonators and matching networks in PA2 are tuned for each of the three subhamonic frequencies – 110 GHz, 130 GHz, and 150 GHz – and are utilized later in the signal chains to compensate for loss.

This amplifier multiplier chain (AMC), made up of the tripler and PA1/PA2 amplifiers, was designed to provide approximately 3.2 dBm of output power at 130 GHz. Thee simulated performance of the amplifier multiplier chain – including all post-layout BEOL full-wave and parasitics is provided in Fig. 5-4. In modelling, we expect to provide approximately 0 dBm of input 43.3 GHz LO power to the AMC. On the left, one can see the third harmonic output power, swept over input power. At 0 dBm input power, the the simulated out spectrum is shown in the right inset, with -45 dBc of spurious performance. The spurious performance of the system is further improved via narrow-band match of subsequent stages.

In order to provide full transmitter characterization, some level of AMC tunability is desired. Specifically, the ability to tune the output transmitter carrier across of

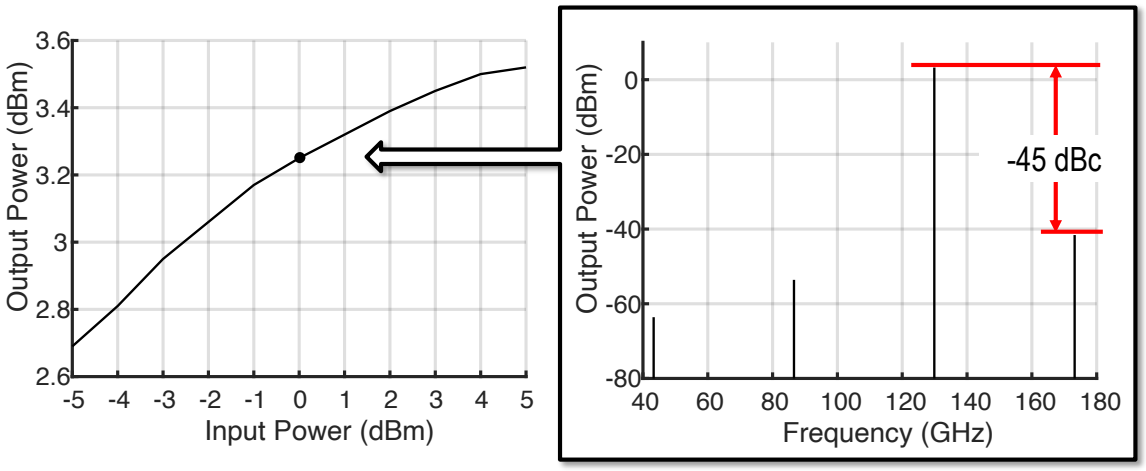


Figure 5-4: Simulated AMC input/output power and output power spectrum.

the final channel filter bands is desired for transmitter power characterization. The resonant loads and matching networks utilized in the AMC (Figs. 5-3a and 5-3b) are chosen to provide sufficiently wide bandwidth to accommodate this. Fig. 5-5 shows the results of a simulation of the complete AMC circuit in which a 0 dBm pump LO is swept over 38 GHz to 48 GHz and the third-harmonic power is measured in harmonic balance. The AMC demonstrates approximately 8 GHz of 3-dB bandwidth, with respect to the input LO. This corresponds to 24 GHz around the circuits nominal 130 GHz operating point, which in turn corresponds to 48 GHz at the final operating frequency (220, 260, or 300 GHz).

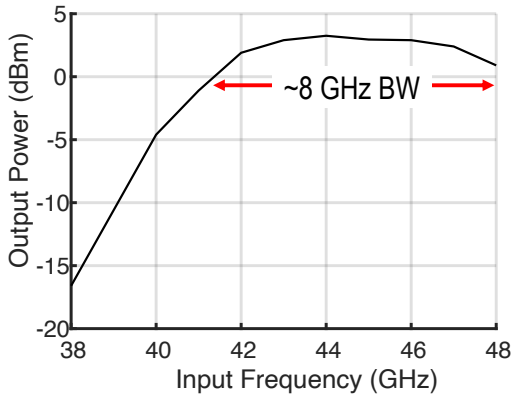


Figure 5-5: Simulated AMC bandwidth.

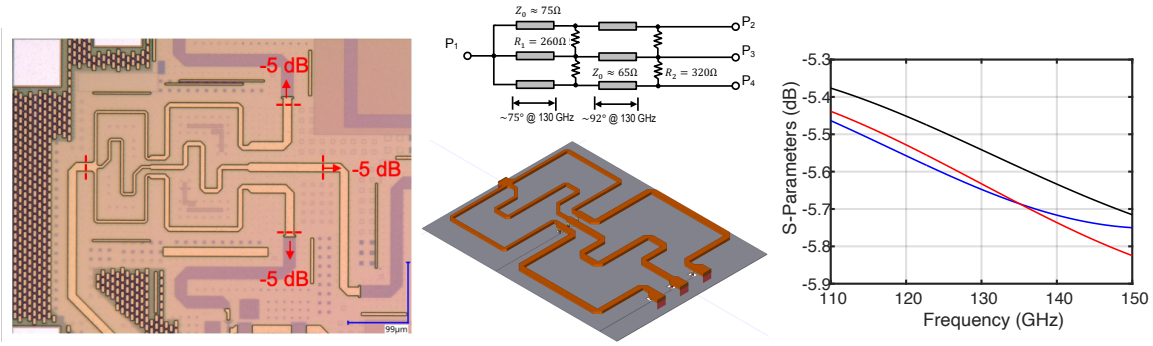


Figure 5-6: 3-way power divider.

5-dB Coupler

Part of the 130 GHz power is diverted to the other two LO paths via a 3-way power divider, shown in Fig. 5-6 (right-most pane). The entire coupler occupies 0.07 mm^2. Cascaded Wilkinson 3-way dividers are realized using microstrip transmission lines and resistive loads to minimize amplitude imbalance, provide 50 Ω matches at each port, and widen the bandwidth response of the component. The transmission line model, utilizing achievable microstrip characteristic impedances utilize the process' top metal layer, is shown in the center of Fig. 5-6. Following transmission line model tuning, a full-parameterized full wave model (also shown in center of the figure), which incorporates all vertical via interconnects, is leveraged for final dimensional tuning. The average coupling across the three outputs at 110 GHz is 5.4 dB. At 150 GHz, this figure is 5.8 dB. The entire 110-150 GHz coupling band exhibits less than a tenth of a dB of coupling difference between the outputs (Fig. 5-6, right).

Upper- and Lower-Sideband Mixers

These single-ended 130 GHz signals are again amplified (using PA2 in Fig. 5-3b) before being mixed in single-sideband mixers to shift the input tones by ±20 GHz, generating signals at $f_{c1} = 110$ GHz and $f_{c2} = 150$ GHz. The schematic for the single-sideband mixers is shown in Fig. 5-7. Tail NNMOS devices, driven by quadrature 20 GHz voltages supplied from off-chip, are utilized to reduce required circuit rail voltage and DC power consumption. A high impedance stub resonator is implemented to provide

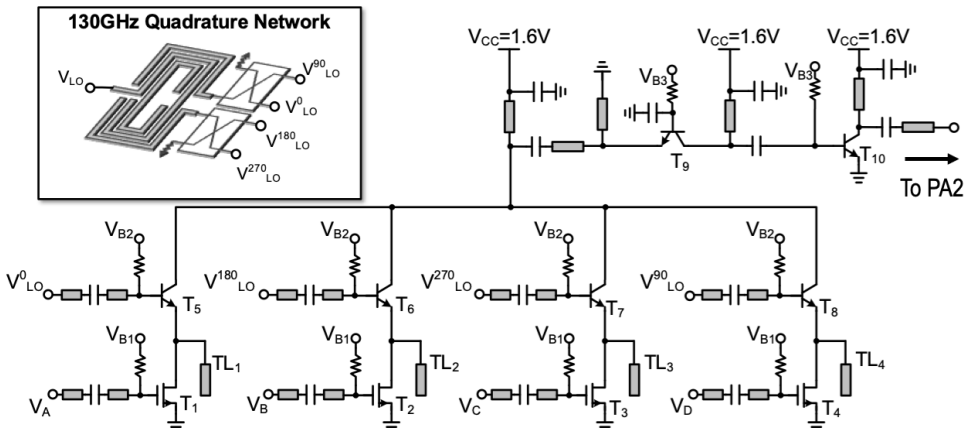


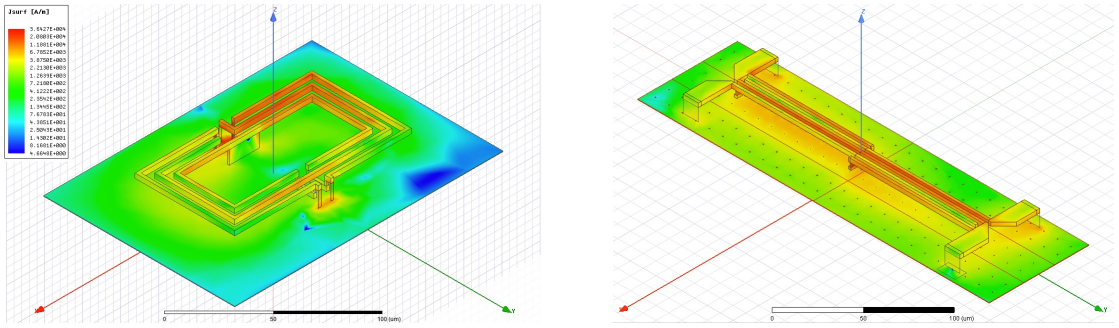
Figure 5-7: Transmitter single-sideband mixer schematic.

a low-impedance node at 130 GHz at the top HBT emitters. The same mixer core performs upper- and lower- single sideband mixing by simply changing the phases of the 20 GHz quadrature signals, $V_A - V_D$. These 20 GHz quadrature signals are produced via a carefully-tuned off-chip quadrature generation network to minimize phase and amplitude errors.

The mixer core is made up of NMOS devices T1–T4 and HBTs T5-T8. The NMOS devices are driven by the off-chip 20 GHz quadrature voltages $V_A - V_D$ and reduce the required voltage headroom for the circuit and thus the dissipated DC power. The core's HBTs (T5-T8) are driven in quadrature via the on-chip 130 GHz quadrature network, made up of a folded Marchand balun and two Lange couplers, all parametrically tuned in full-wave simulation to minimize phase and amplitude offsets in these mixers. HFSS simulations showing current density while operating in band are shown in Fig. 5-8.

Transmission line resonators, TL1-TL4, are each approximately a quarter wave at the nominal LO pump frequency of 130 GHz. They are placed in shunt with the mixer core's HBTs emitters to provide a low-impedance AC-coupled node at the nominal LO pump frequency of 130 GHz.

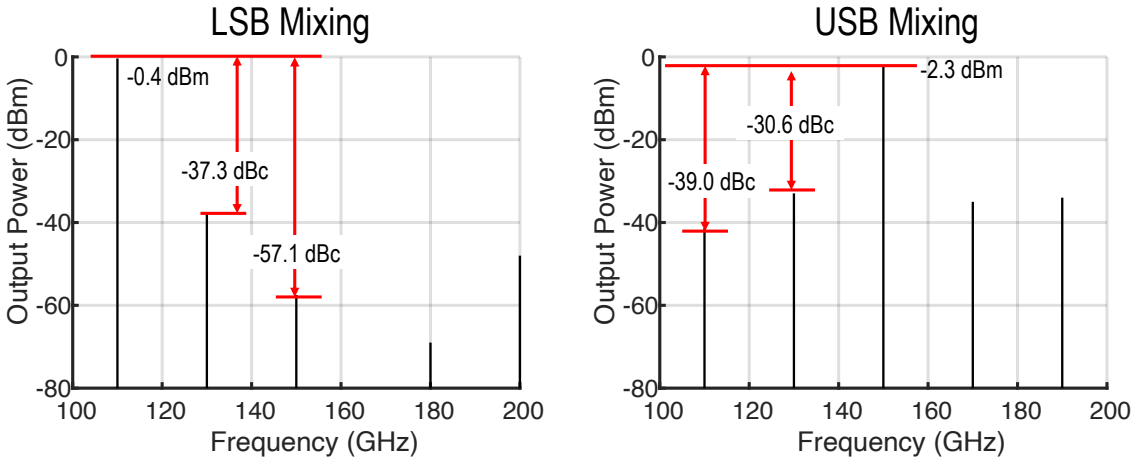
Following the common mixer core, a common base and common emitter buffer-amplifier stage, made up on HBTs T9 and T10, is utilized to further reduce undesired



(a) (b)

Figure 5-8: Full wave simulations of a (a) Marchand balun and (b) Lange Coupler used to drive the 130 GHz single-sideband mixer.

sidebands in addition to improving output power. PA2 amplifiers, tuned to 110 and 150 GHz, follow these mixers to provide additional gain and sideband suppression.



(a) (b)

Figure 5-9: Simulated output power spectrum of the (a) lower sideband and (b) upper sideband mixer performance.

After the tuned PA2 stages, the simulated 110 GHz and 150 GHz carriers are -0.4 dBm and -2.3 dBm, respectively. In both cases, the mixers and PAs achieve better than -30 dBc of carrier suppression and better than -39 dBc of undesired sideband suppression in harmonic balance simulation (including all full-wave interconnect modeling). Fig. 5-9a illustrates the final simulated output spectrum for the

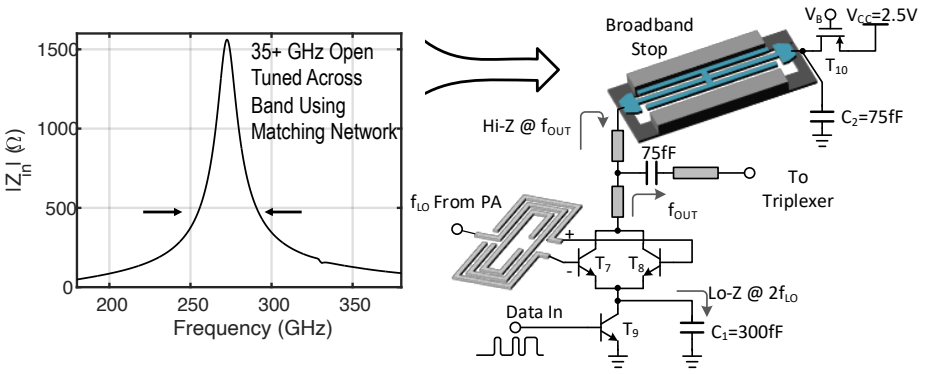


Figure 5-10: Transmitter combined doubler-modulator schematic.

lower sideband (LSB) mixer-PA block, that generated the final 110 GHz sub-harmonic carrier. Fig. 5-9b shows the output spectrum for the 150 GHz sub-harmonic carrier generation.

Doubler-Modulator

A single circuit combines the function of modulation and frequency doubling, acting as the final output stage before channelization via the on-chip multiplexer. This scheme reduces overall system losses, required circuit area, and overall power dissipation compared to a more conventional doubler followed by a modulator circuit. The schematic is shown in Fig. 5-10. The core emitter coupled pair, T7 and T8, sized with 5 emitter fingers each, provide frequency doubling via push-push operation. The tail HBT, T9, modulates the baseband bit steam via an on-chip AC-coupled buffer. The capacitor C1 is chosen to be sufficiently large so that when T7 and T8 are active, it acts as a current path at $2f_{LO}$ (between 220 GHz and 300 GHz) in order to increase the frequency conversion efficiency. Simultaneously, C_1 is small enough to still allow for up to 35 GHz modulation of the tail current.

The NPN devices T7 T9 are biased by a PMOS T10 through the dumbbell broadband stop structure, which isolates the large parasitic capacitance of T10 from the THz output path. This structure, implemented to the top metal layer, provides bet-

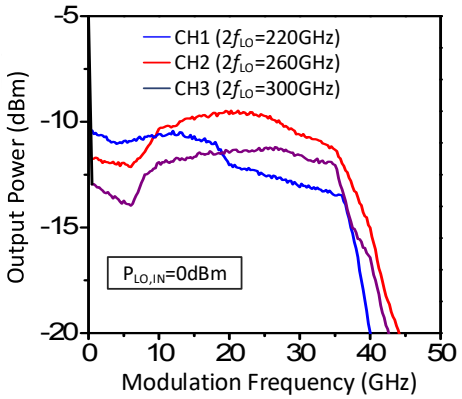


Figure 5-11: Transmitter combined doubler-modulator simulated output power. From [44].

ter than 1 dB of return loss from 200 GHz to 400 GHz, acting as a common load for all operating bands. The input impedance of this choke, extracted from full wave simulation, is plotted on the left of Fig. 5-10, demonstrating more than 35 GHz of modulation bandwidth. The matching transmission lines are tuned to optimize extraction of upper sideband power from 200-225 GHz, 260-295 GHz, and 300-335 GHz for channel 1,2, and 3, respectively. The doubler-modulator module consumes 22mW of power, and with ∼0 dBm input LO, its output power is around -12 dBm with ∼3 dB fluctuation across the 35 GHz modulation frequency range. The simulated upper sideband power from each channel's modulator is shown in Fig. 5-11.

On-Chip Triplexer

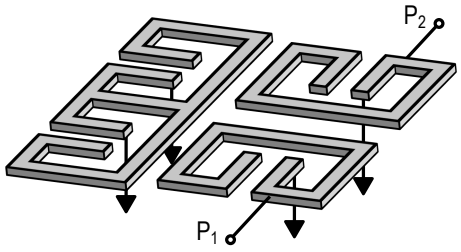


Figure 5-12: Isometric model of the asymmetric quarter-wave hairpin resonator-based filter comprising the on-chip triplexer.

An on-chip channelizer makes use of three channel filters to provide lower-sideband suppression, channel aggregation, and prevents undesired sub-THz power injection

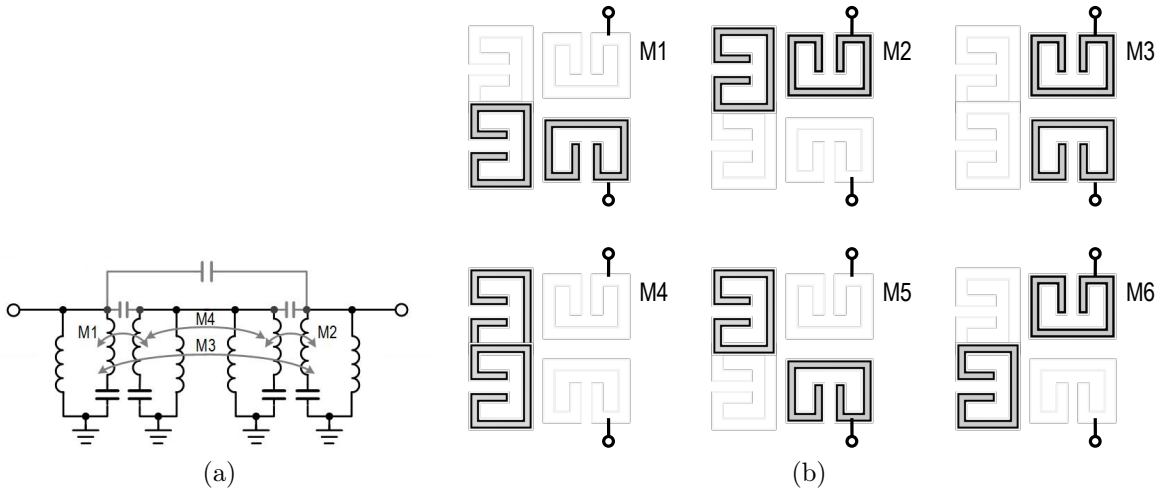
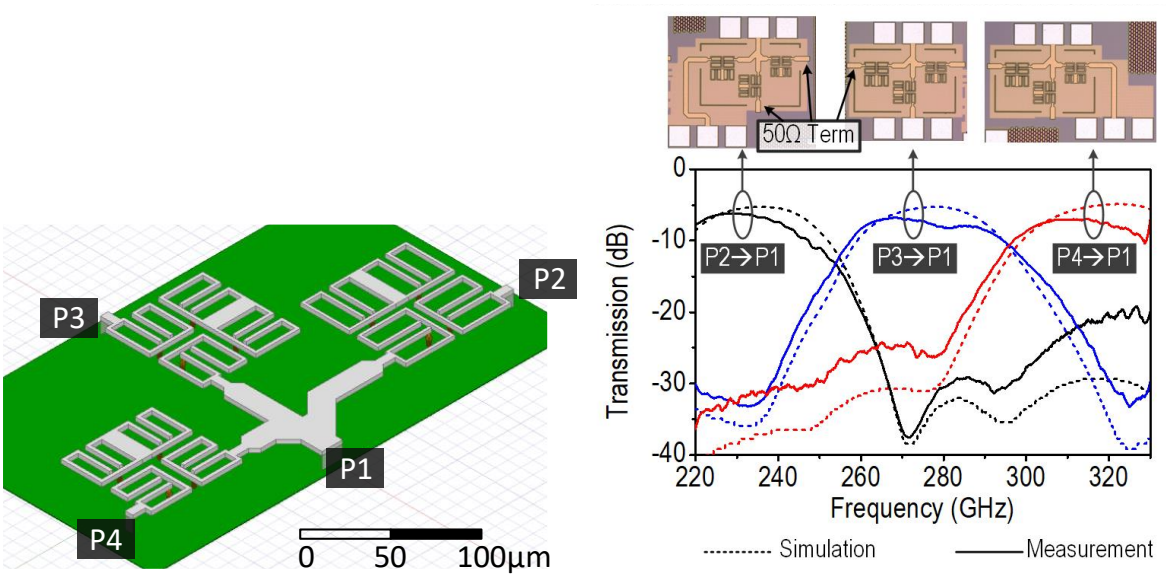


Figure 5-13: On-chip channelizer filter (a) circuit model with coupling (from [44]) (b) resonator orientation for each set of coupling coefficients.

between adjacent channels. Traditional filter topologies with rapid roll-off adopt cascaded resonators, which causes excessive loss at sub-THz frequencies. To manage losses and stopband performance, the channel filters are realized using four resonators, physically arranged with mixed electric and magnetic coupling. A high-level illustration of the physical layout of a single filter is shown in Fig. 5-12. To reduce overall size, these resonators are designed as quarter wave structures, instead of conventional half-wave structures. Each channel filter's resonator dimensions are parametrically tuned in electromagnetic eigenmode simulations to maximize quality factor. Each filter is tuned in full-wave simulation to achieve the desired quasi-elliptical filter response with three passband poles and four stopband zeros (Fig. 5-13a). Due to the asymmetric fields around these quarter wave resonators, not only are the individual resonator-resonator spacings important to determine coupling, but the relative orientation of each resonator is varied to achieve the desired coupling and filter response (Fig. 5-13b).

Each channel filter provides a high impedance in the stop bands, allowing us to connect all three filters to a common node, forming a star-topology triplexer, minimizing filter-to-filter interaction. Final triplexer optimization is carried out in full-wave simulation to meet channel-channel isolation, input matching, and insertion loss design requirements. A full-wave model is shown in Fig. 5-14a.



(a) (b)

Figure 5-14: Full wave model of the hairpin filter-based on-chip triplexer (a) and (b) the comparison between measured and simulated results. From [44].

For verification, three standalone triplexer test structures are fabricated, allowing for separate tests of the three channel filters via on-chip termination of the remaining ports. Photos of test structures are shown in Fig. 5-14b, denoting the location of the on-chip terminations. Following standard wafer-probe calibration, on-chip measurement results agree well with the simulation, showing a 3-dB pass bandwidth of 30∼35GHz and 10∼30dB stop-band rejection (Fig. 5-14b).

Of note, the degraded channel 1-to-3 isolation, while not ideal, has less of an impact than the adjacent channel stop-band performance. In the case of channel 1-to-3 interference, for example, the integrated channel 1 transmit power spectral density, well beyond the second spectral null, is further attenuated by more than 20 dB via the triplexer response. This integrated power is still significantly smaller than the adjacent channel vestigial lower sideband integrated power.

On-Chip Waveguide Coupler

A broadband planar sub-THz power coupler of the same design as described in Chapter 3 is implemented on-chip. It is used to launch the 220-to-335 GHz multiplexed channels into the wideband dielectric waveguide. The structure, illustrated in the cen-

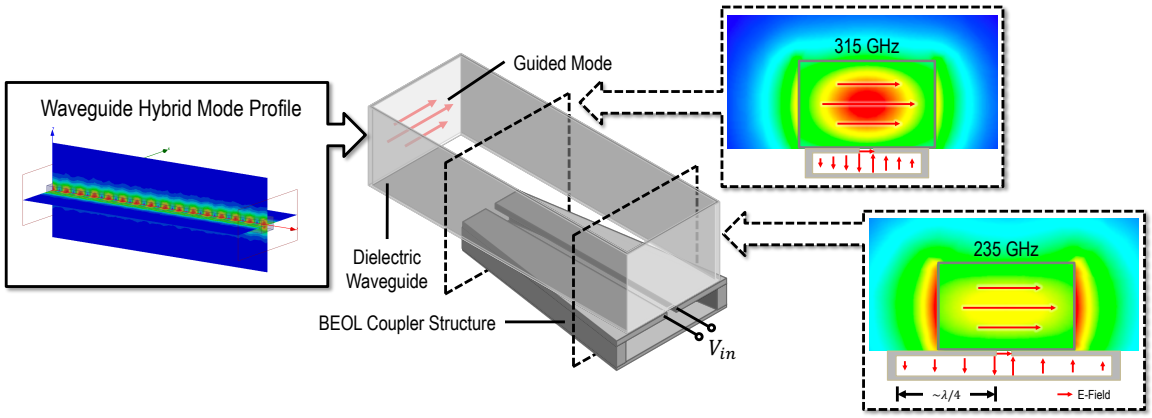


Figure 5-15: On-chip dielectric waveguide coupler core operation.

ter of Fig. 5-15, is integrated using the back-end-of-line metal in the implementation process.

The dielectric waveguide is bonded directly on top of the structure. The coupler is enclosed, relative to the bulk silicon, reducing undesired substrate coupling and thus losses. The width is tapered along the longitudinal axis, forcing the travelling wave energy out of the enclosed metal structure and into the waveguide. This behavior illustrated in insets to the right in Fig. 5-15, with representative field profiles near the beginning and end of the structure.

The coupler geometry and the waveguide material and cross section are carefully co-designed in full wave simulation to mode-match the radiated mode with the guided mode. In this work, we target the horizontally-polarized hybrid mode, shown in the inset to the left of the figure. The final dielectric waveguide cross section dimensions, built from Rogers R3006 material, are 0.4x0.25 mm^2. This waveguide material and cross section is sized to operate in a single-mode regime in the excited horizontal hybrid mode polarization.

Fig. 5-16 shows additional details of this coupler. The coupler core is, in essence, a differentially-excited substrate integrated waveguide structure (SIW), in which the cross section is tapered from WC1=364μm to WC2=204μm. This present an increasing characteristic impedance, forcing the travelling wave energy out of the structure and into the dielectric waveguide. This longitudinal taper further boosts the cou-

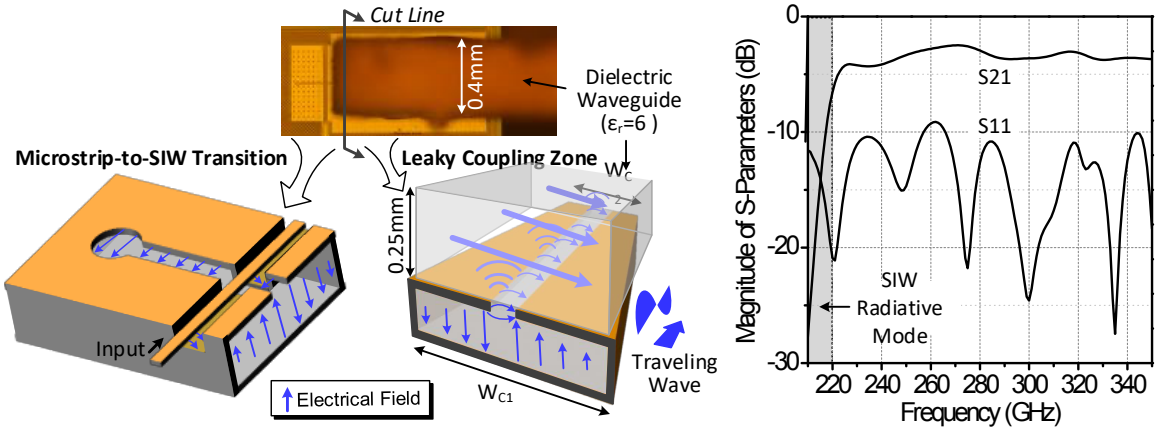


Figure 5-16: On-chip dielectric waveguide coupler and deembedded simulated wideband response. From [44].

pling and decreases the length of the coupler to 750μm. A wideband single-ended microstrip to slotline transition both performs the mode conversion over a wideband and compensates the slightly inductive response of the core coupler travelling wave structure. This improves efficiency and bandwidth. A photo of a waveguide, directly bonded to the passivation on top of the chip, immediately above the coupler, is shown in Fig. 5-16. Here one can see the metal slotting required to satisfy process metal density requirements.

Additional full-wave simulation is performed to de-embed the performance of a single microstrip-to-coupler-to-waveguide response, with the waveguide mode reference plane placed *just past the end of the coupler structure*. The fields near the coupler structure are relatively complex, with poor mode confinement. As such, conventional modeling techniques provide incorrect scattering parameter response. More information is provided in Appendix A. In the resultant de-embedded simulation, the coupler exhibits a low insertion loss of 2.5$\sim$6dB across the entire 220$\sim$340GHz band.

Compared to prior works discussed in Chapter 3, this coupling scheme eliminates the lossy THz-signal routing to off-chip couplers/radiators, and enables a planar waveguide placement with a direct contact to the chip edge.

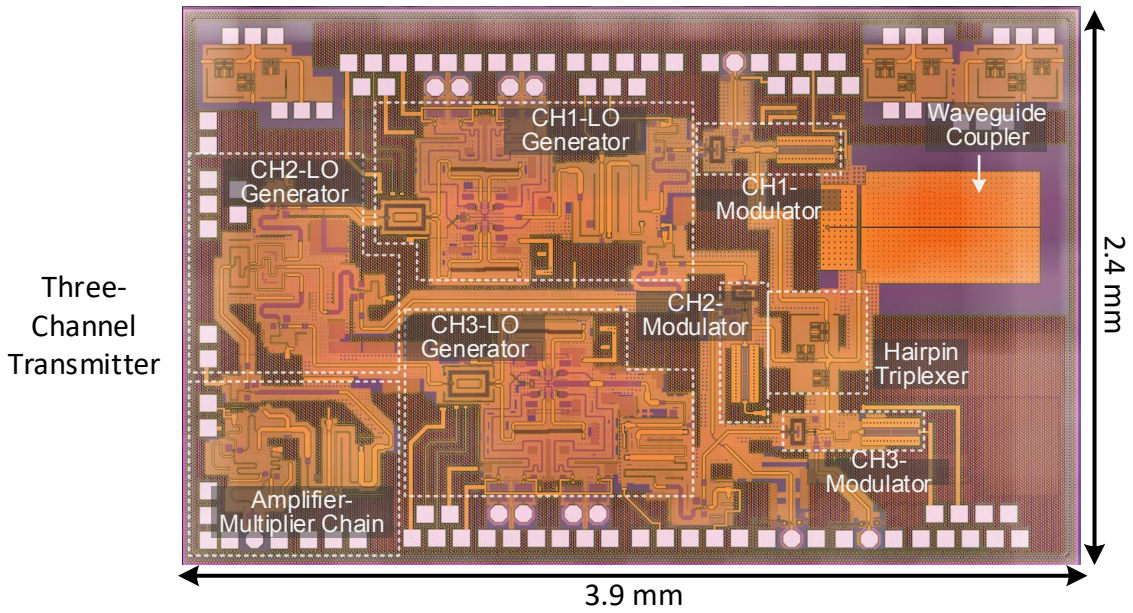


Figure 5-17: Fabricated transmitter die photo. From [44].

Fabricated Transmitter Chip

The fabricated transmitter chip is 2.4x3.9mm^2. It is shown in Fig. 5-17, supplied with off-chip seed 43.3 GHz LO, 20 GHz LOs and baseband PRBS modulation waveforms via ground-signal-ground pads around the periphery. Pads are supplied for individual sub-block power and bias voltages to enable DC power characterization of various blocks within the transmitter.

5.2.2 Single-Channel Receiver

To form a complete all-silicon link with the transmitter, a single-channel receiver, integrated with the same waveguide coupler, is implemented using the same IHP 130nm BiCMOS process. Shown in Fig. 5-18, T15∼T17 form an active balun, with full band matching, that converts the single-ended THz input from the coupler into a pair of differential currents. To down convert the sub-THz energy to baseband, these currents are injected into four resistive-loaded switching transistors T11∼T14, which are driven by an externally-applied LO signal. An on-chip Marchand balun, covering the entire 220-330 GHz band provides the differential on-chip LO signals to the top

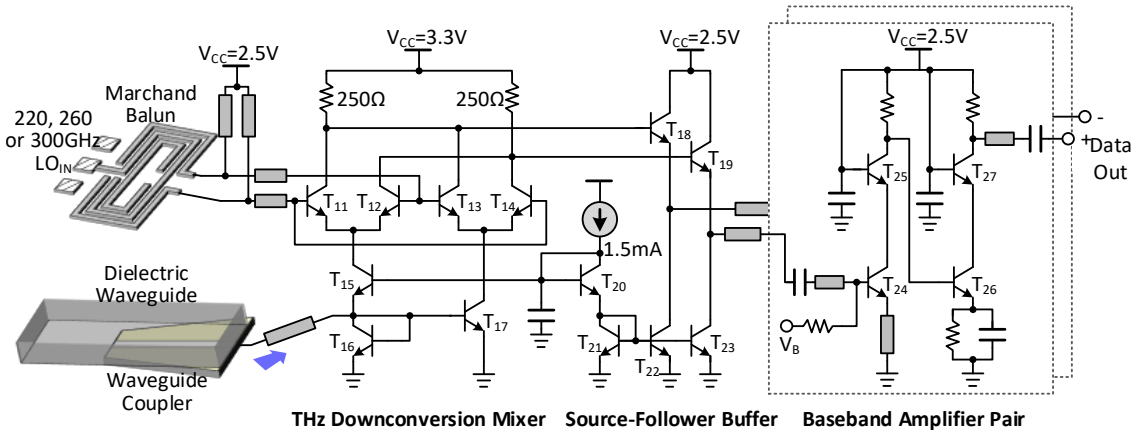


Figure 5-18: Single-channel link receiver chip schematic. From [44].

switching quad. T11∼T14 are minimally sized and T15∼T17 are biased to maximize f_t (approximately 1.5mA per emitter finger).

Followers buffers T18, T19, T22, and T23 are used to step-down the baseband signal (reducing DC power consumption), and aid in inter-stage matching. Lastly, a pair of baseband amplifier-drivers are utilized to drive pads for subsequent off-chip measurements. The cascode amplifiers' emitter degeneration is carefully chosen to provide peaking to compensate for modelled bond wire parasitics, with approximately 30 GHz of 3-dB bandwidth in simulation. The recovered data are amplified and extracted at the output.

Fig. 5-19 shows the simulated single-sideband conversion gain of the receiver, utilizing a 0 dBm sub-THz LO source, injected into the probe's waveguide flanges. The harmonic balance simulation includes all the post-layout interconnect full-wave responses, to include the wafer probe response and the probe-pad transitions.

The simulations show more than 30 GHz of bandwidth in each channel, which is driven primarily by the baseband amplifier bandwidth. The increased conversion gain from Channel 1 to Channel 2 (Fig. 5-19d)is primarily due to the LO Marchand balun's phase and amplitude mismatch away from its center operating frequency of 275 GHz. The simulated DC power consumption is 65 mW: 20 mW in the mixer core and 45 mW consumed in the baseband cascode amplifier-drivers. The THz mixer operates across a broad band; in measurement, the applied LO frequency is

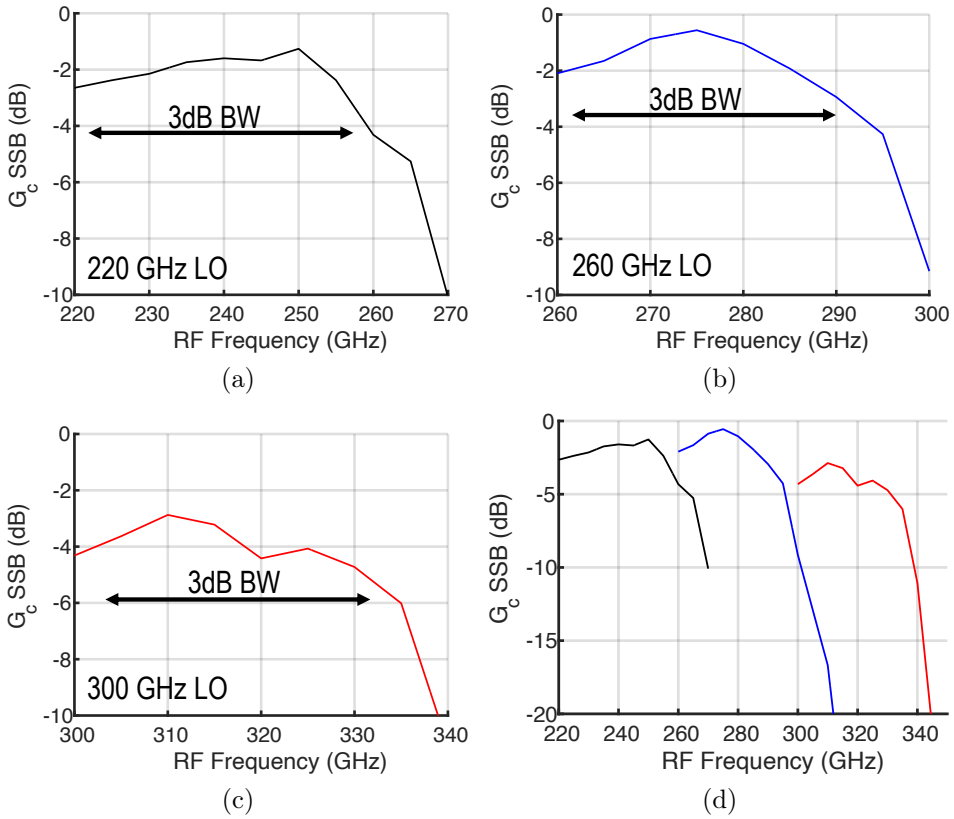


Figure 5-19: Harmonic balance simulation results of single-sideband (SSB) conversion gain (G_c) of the receiver for (a) Channel 1, (b) Channel 2, (c) Channel 3, and (d) the combined three-channel responses.

selected to be 220, 260 and 300 GHz and manually tuned for phase coherence with the transmitter, so that each transmitted channel is tested. Future multi-channel receivers could include the same triplexer in the receiver and separate receiver circuits to enable simultaneous down conversion/demodulation. Furthermore, if this scheme were monolithically implemented within a larger digital fabric, the baseband amplifier performance requirements would be significantly reduced without the need to drive off-chip measurement equipment. As such, one would expect this block's power consumption to be significantly reduced. The fabricated receiver chip, shown in Fig. 5-20, is 0.9x0.9mm^2 in size.

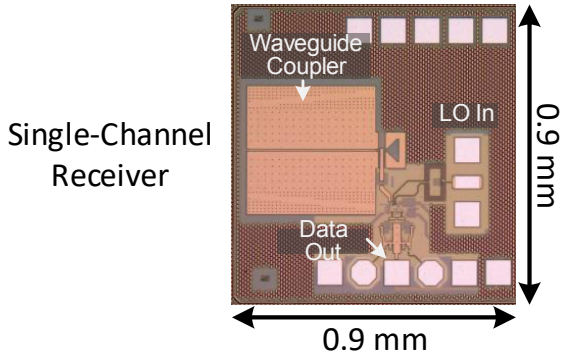


Figure 5-20: Fabricated receiver die photo. From [44].

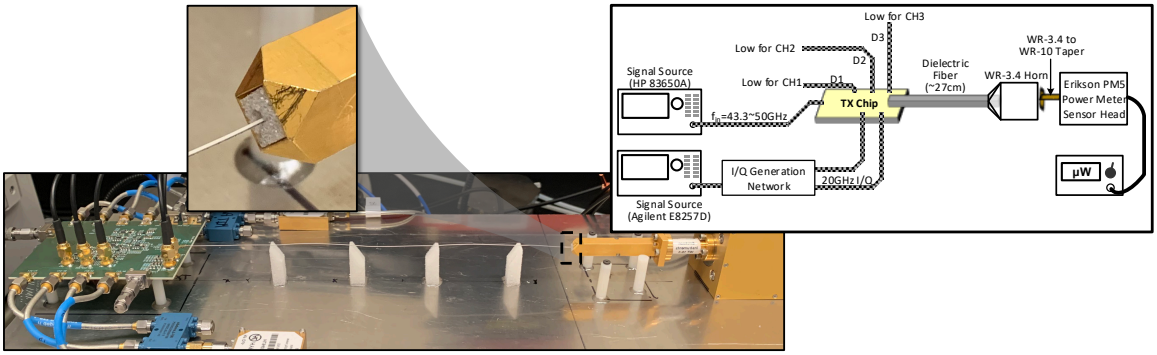
5.3 Full Link Assembly, Test, and Measurement

5.3.1 Transmitter Characterization

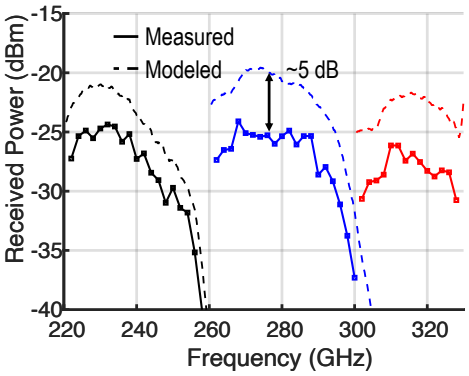
In order to verify transmitter operation, the output power of each transmitter channel is characterized. The receiver-end of the waveguide is directly inserted into a WR-3.4 horn connected, via a taper, to to an Erikson power meter. A piece of polystyrene foam, with a small central hole, is used to mechanically support the waveguide. A single channel carrier is generated, unmodulated, and swept over the channel bandwidth by changing the TX seed LO from a lab source. The setup is shown in Fig. 5-21a.

Fig. 5-21b shows the results of these measurements (solid lines). This figure also shows the theoretical received power utilizing the the simulated transmit power, accounting for the measured triplexer and coupler losses (dashed lines).The difference between measured and modelled power ($\sim$5 dB) can be largely attributed to the unmodelled mode-conversion or mode coupling losses between the abrupt end of the waveguide and the horn's supported modes. The peak output power of the transmitter channels is measured to be -24 dBm. The roll-off associated with the on-chip transmitter channelizer response and finite doubler-modulator bandwidth can be clearly seen in this plot.

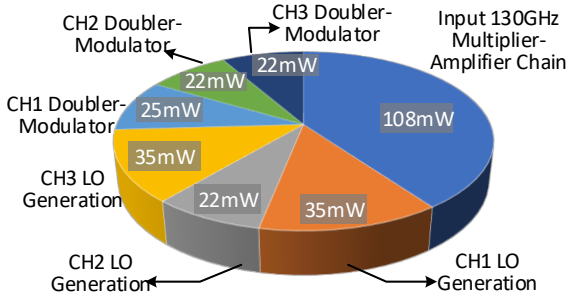
The DC power of the transmitter is measured at 256mW with all three channels operating. A breakdown of the transmitter system power consumption is provided in Fig. 5-21c. The preponderance of the DC power consumption is in the 130 GHz



(a)



(b)



(c)

Figure 5-21: (a) Transmitter power measurement setup and (b) comparison of measured and modelled responses for each channel. (c) Breakdown of transmitter power consumption. From [44].

tripler chain to generate the internal, high-power seed LO, from which all the channel carriers are generated. In future implementations, this can be dramatically reduced to lower the overall power consumption.

5.3.2 Link Testing

Fig. 5-22 shows a photo of the test setup for a 30 cm dielectric waveguide connecting the transmitter and receiver on a probe-station. An additional, functional, 5 cm link was also built and successfully measured. In this photo, the transmitter (on the left) is connected to the receiver (on the right in the photo) via a 30 cm-long waveguide. The waveguide is mechanically supported by small posts machined from low-density polystyrene foam. This material has a dielectric constant very close to air and a low loss tangent, even in the 200∼300 GHz regime. As such, it does not significantly

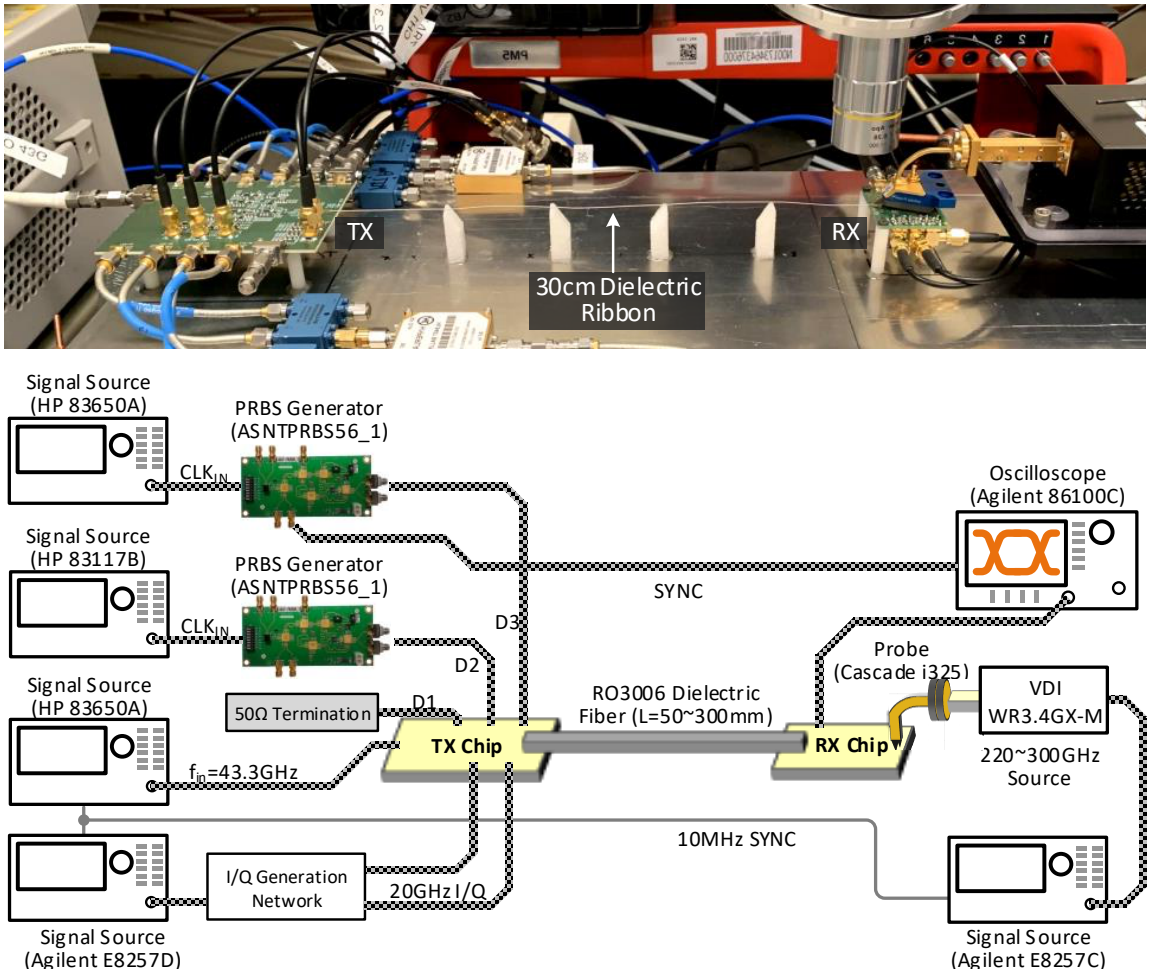


Figure 5-22: Completed dielectric link demonstrator setup. From [44].

perturb the waveguide's modal profile or introduce significant loss.

The number of successful links is limited by available transmitter test boards, the fragility of the waveguides themselves, the yield of these boards (to include the yield of the hand-bonded) waveguide-couplers, and the availability of bulk waveguide material. The end-to-end link SNR was not a limiting factor in testing. Specifically, a probe station platen with precision micro-positioners is required to position and land a wafer probe to provide the required down-conversion LO on the receiver side. The bulk material – an 8.5" x 11" sheet of Rogers R3006 material – constrained the maximum available straight waveguide that could be fabricated. Both factors drove the fabrication of several links at the same lengths to ensure successful test at those links, but constrained the ultimate number of different link lengths.

The lower portion of Fig. 5-22 demonstrates the overall link testing setup schematic. The 20 GHz quadrature signals are generated using bench top signal generators and off-board quadrature generation networks made up on high-frequency baluns and hybrid couplers. Phase-stabilized coaxial cables are characterized via a VNA and selected to minimize the phase variations across nominally-quadrature signals. A 0 dBm 43.3 GHz LO source is provided via a bench top signal generator and connected via 2.4 mm coax. Two high-speed pseudo-random bit sequence (PRBS) generators supply single-ended modulation waveforms to the transmit chip via phase stabilized 2.4mm coax cables. To include the impact of inter-channel interference, the PRBS-7 generators simultaneously drive both the channel under test and an adjacent channel of the transmit chip.

The receiver (right side of the photo in Fig. 5-22) receives LO power at 220, 260, and 300 GHz via a WR-3.4 waveguide wafer probe from Cascade. A Virginia Diodes spectrum analyser source provides a clean LO tone around 0 dBm to pump the receive down conversion mixer. The receive chip features a *differential* baseband output. The single-ended sampling oscilloscope requires that only a single end of the receiver output stage is received, via phase stabilized 2.4 mm coax, while the opposite polarity is terminated with a matched load. As a result, the measured results are expected to exhibit $\sim$3dB lower signal-to-noise ratio that is available in the system.

The system is manually phase-aligned at each PRBS rate to ensure coherent down-conversion/demodulation prior to a given measurement. A single sync reference from one of the PRBS generators is used to trigger a sampling oscilloscope to measure eye diagrams and estimate bit-error rate performance.

Fig. 5-23 provides a view of complete waveguide bonded to a transmitter chip. The dielectric ribbon is directly-bonded by hand with low permittivity epoxy on top of the two chips. No precise ribbon-chip alignment is required. The waveguide is laser cut from bulk unclad Rogers R3000-series materials, manufactured to be 250 μm thick. More information of waveguide fabrication and bonding techniques is available in Appendix B.

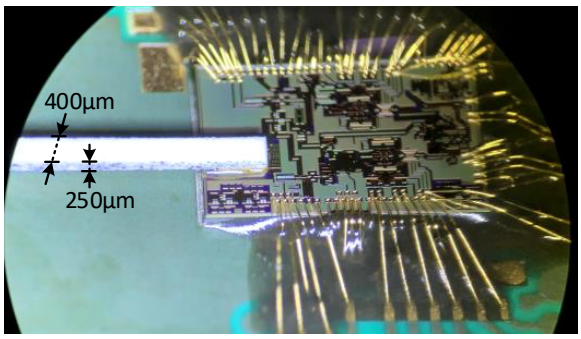


Figure 5-23: Microscope photo of a complete transmitter chip-waveguide bond. From [44].

Single-Channel Characterization

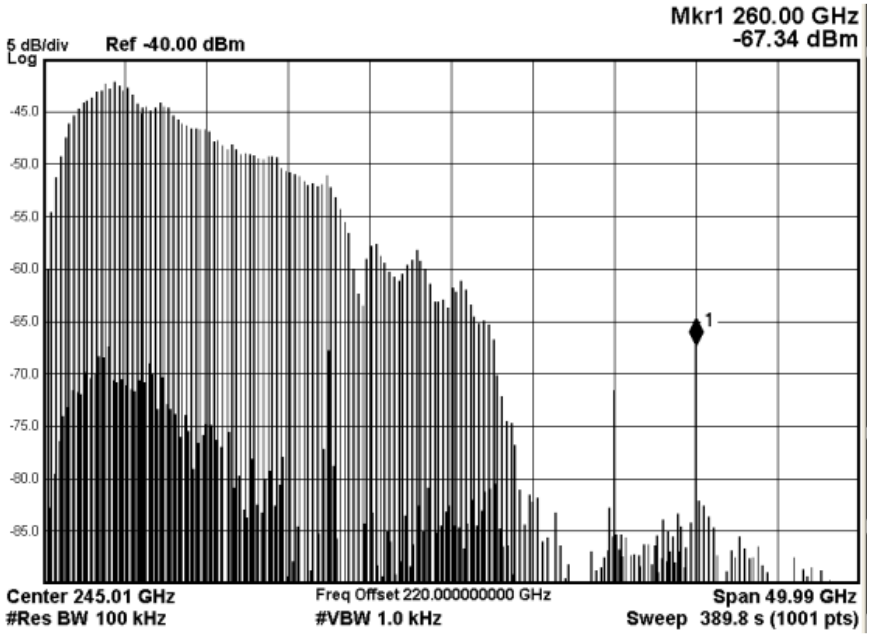


Figure 5-24: Channel 1 received baseband spectrum. From [44].

The baseband received spectrum is characterized, subject to a single-channel PRBS transmission. In this case, only one channel is modulated with baseband data and the adjacent channel is powered, transmitting a lone carrier tone. In Fig. 5-24 one can see the results of this test. Here, a screen shot of a the *baseband* spectrum from channel 1 (220-255 GHz) is shown. The spectrum analyzer is manually setup with a frequency offset to help the reader recall the sub-THz channel which is being measured. In this figure, we see the characteristic spectrum of the upper sideband of

a conventional PRBS signal with the expected null in the power spectral density near the modulation rate. The instrument's marker is setup to measure the power from the f_{c2} carrier in the adjacent channel 2 (260-295 GHz). The power of this carrier, and any data modulated on to it's upper side band, is attenuated considerably by the ∼35 GHz bandwidth presented by the receiver chip's down-conversion mixer and baseband amplifiers. Furthermore, the losses associated with the off-chip baseband data signal path's parasitics further attenuates energy beyond this ∼35 GHz baseband bandwidth. The receiver chip DC power consumption, under this test, was measured to by 73 mW.

Multi-Channel Bit Error Rate Characterization

Next, a set of measurements are undertaken to verify successful PRBS data transport over the link in Fig. 5-22. The test setup is limited to two high-speed baseband PRBS generators for equipment availability. The eye openings for each channel, along with the sub-THz channels being modulated are shown in Fig. 5-25 - Fig. 5-27. In all three cases, the link was successfully measured up to 35 Gbps using PRBS-7 transmitter data across the 30 cm link. For each measurement, the receiver is manually phase aligned to the transmitter to maximize the baseband eye amplitude before commencing a measurement. The eye openings shown are at the limit of what the instrument can reliably resolve and on which it can automatically trigger. However, slightly higher data rates can be observed by the oscilloscope if manually triggered.

As we expect, given the higher channelizer and circuit losses at higher frequency, we do observe an overall reduction in eye amplitude from channel 1 to channel 3. In the channel 1 measurement, Fig. 5-25, PRBS data is transmitted in both channel 1 and channel 3. In the case of channel 2 measurements, Fig. 5-26, the presented results show the *lowest measured eye SNR of the available measurement configurations* - in this case, using the adjacent channel 3 to inject unwanted interference. Lastly, the channel 3 measurement (Fig. 5-27) includes interference from the adjacent channel 2 transmission. It should be noted that in all three cases, the system includes no

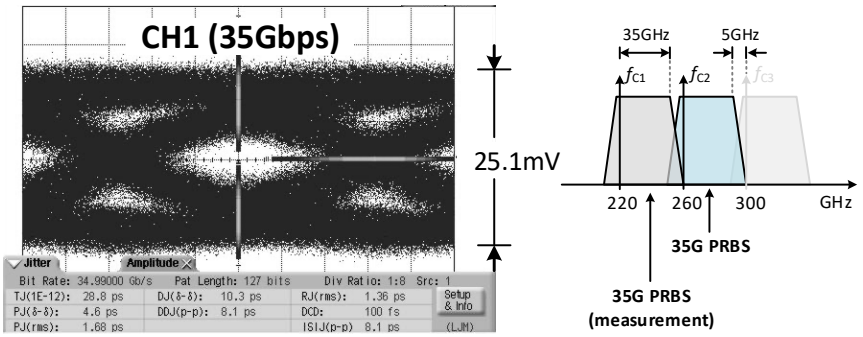


Figure 5-25: Measured channel 1 eye opening.

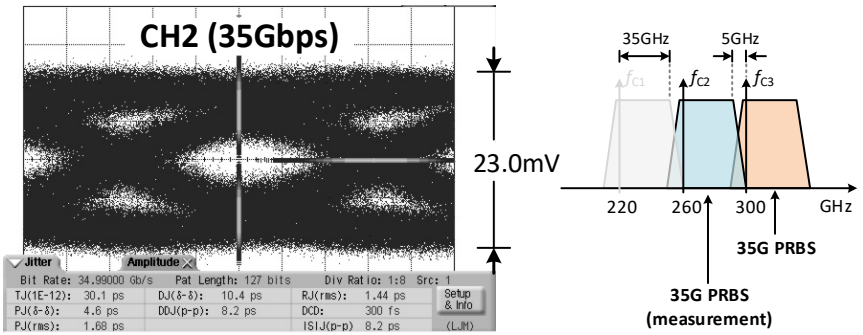


Figure 5-26: Measured channel 2 eye opening.

equalization, which is one of the advantages of this scheme over conventional copper wireline channels.

Overall, these measurements verify operation of the link up to 105 Gbps, aggregate rate. With the measured transmitter and receiver DC power consumption and the demonstrated link rates, we can calculate the transmitter energy efficiency of 2.4 pJ/bit and receiver energy efficiency of 2.1 pJ/bit. The total link efficiency is, therefore, 4.5 pJ/bit.

As discussed earlier, in addition to the 30 cm long link, a shorter 5 cm link was built and successfully tested. A complete set of measurements were carried out to generate the bit error rate (BER) bath tub curves (estimated from the eye SNR), in which both the timing and jitter-induced eye closure, as well as SNR-induced eye closure are quantified. As can be seen in Fig. 5-28, the link demonstrations are able to achieve $\leq 10^{-12}$ for the 5 cm distance (and 30 Gbps), and $\leq 5 \times 10^{-8}$ for the 30 cm

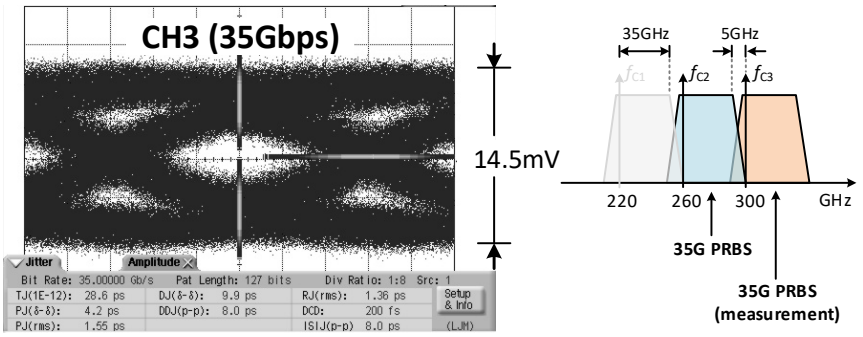


Figure 5-27: Measured channel 3 eye opening.

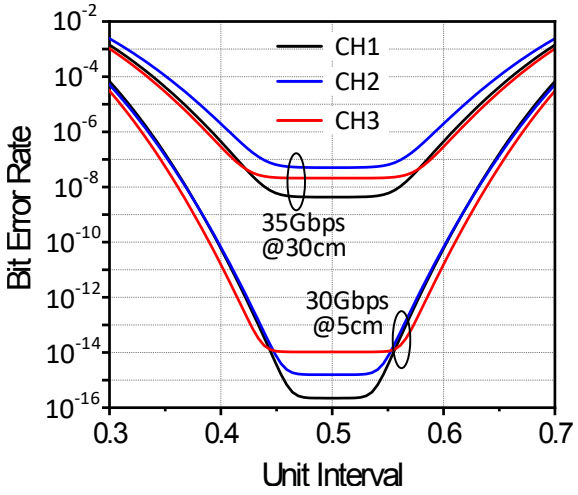


Figure 5-28: Complete set of measured BER bathtub curves. From [44].

distance (at 35 Gbps).

Impact of Additional Link Waveguide Length

Next, cursory characterization of the relative performance of the 5-cm and 30-cm links at maximum data rates is performed to understand guide-length losses. Shown in Fig. 5-29, a reduced BER at a longer link length with the same aggregate signaling rate is plotted. In these measurements, the BER degradation measured with the longer length corresponds to ∼2 dB of additional loss. One should note that this cursory test is insufficient to draw definitive conclusions regarding guide losses given only two measurements. Given the link performance variability induced from the hand-bonding of the waveguide and coupler, we expect lower incremental waveguide losses

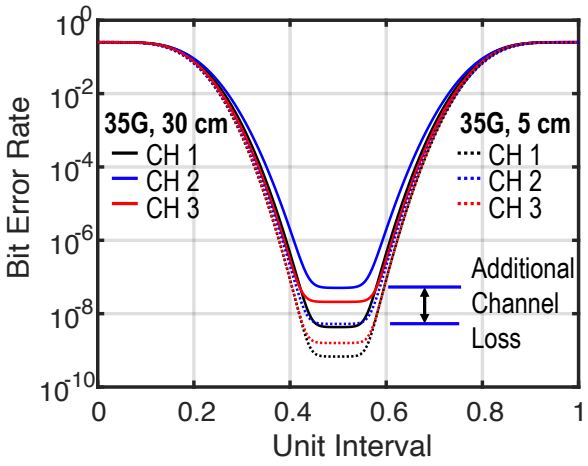


Figure 5-29: BER impacts from additional link guide lengths.

based on full-wave simulation and prior published THz dielectric waveguide characterization. Additional measurements using additional physical links are required to draw statistically-meaningful conclusions.

Impact of Adjacent Channel Interference

In this measurement, the impact of adjacent channel interference to the link's BER is investigated. In this measurement the 5 cm link is utilized to ensure maximum receiver SNR. A single channel is characterized at maximum rate (35 Gbps) with and without adjacent channel energy present.

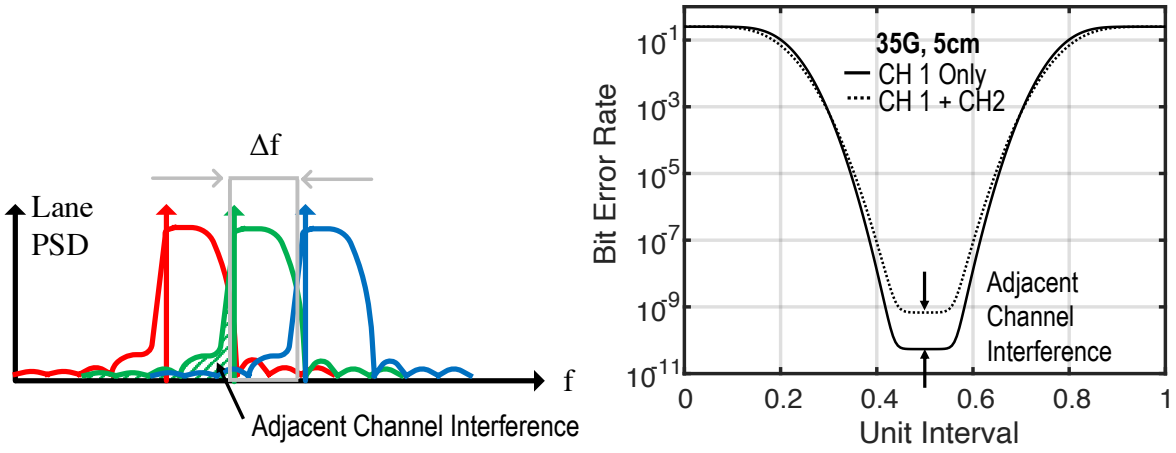


Figure 5-30: (a) Impact of lower sideband adjacent channel interference, and (b) comparison of measured BER with and without adjacent channel interference.

As shown in Fig. 5-30a, one expects that the *undesired* lower sideband energy, in this case injected from channel 2 into channel 1, will manifest itself as uncorrelated noise, decreasing the measured channel 1 SINR. This is indeed the case, as demonstrated in Fig. 5-30b, in which a single channel, without adjacent channel modulation, is measured. The adjacent channel 2 is then modulated with a separate 35 Gbps PRBS data stream (dotted line). This incremental change in BER at the center of the bathtub curve corresponds to approximately 2 dB change in SNR from the adjacent channel interference. Given this measurement, we expect that the majority of the noise contribution in the system is not adjacent channel interference, but rather the transmitter and receiver noise. Additional measurements of multiple links and variable adjacent channel data rates are required to further de-embed and estimate those transmitter and receiver noise figures.

5.4 Summary and Comparison with State of the Art

Comparison with existing dielectric links is somewhat challenging given the relatively small numbers of end-to-end link that are available in the literature. Shown in Table 5.1, this link has 3x higher data rate than the prior arts and the smallest interconnect size due to its integrated coupler and the small dimension of the THz dielectric waveguide. The link achieves an aggregate rate of 105 Gbps compared to

Table 5.1: Link Performance Comparison With Best-in-Class Published Works

	Technology	**Carrier Frequency (GHz)**	**Data Rate (Gbps)**	**BER**	**Waveguide Coupler**	**Fiber Size (W×H, mm)**	**Demo Link Length (cm)**	**TX DC Power & Efficiency**	**RX DC Power & Efficiency**	**Density FOM (Gbps/mm)**
JSSC 2011 [31]	40nm CMOS	57, 80	12.5+12.5†	$<10^{-12}$	Quasi Yagi (Off-Chip)	8×1.1	120	56mW 2.2pJ/bit	87mW 3.5pJ/bit	8.4
SSC-L 2018 [86]	55nm SiGe	130	36	$<10^{-8}$ @ 25Gbps	Vivaldi (Off-Chip)	1.3×1.3	100	216mW†† 6pJ/bit	No RX	27.7
ESSCIRC 2016 [98]	40nm CMOS	120	17.7	$<10^{-12}$	Tapered Slot (Off-Chip)	2 (Circular)	100	11.1mW 0.63pJ/bit	59.6mW 3.4pJ/bit	8.9
JSSC 2019 [18]	28nm CMOS	140	12	$<10^{-12}$	CPW-WG Transition (Off-Chip)	1.9×1.0	100	65mW 5.4pJ/bit	165mW 13.8pJ/bit	8.7
This Work	**130nm BiCMOS**	**220, 260, & 300**	**35×3‡ 30×3‡**	**5×10^{-8} ≤ 10^{-12}**	**Leaky SIW (Integrated)**	**0.4×0.25**	**30**	**256mW†† 2.4pJ/bit**	**73mW‡‡ 2.1pJ/bit**	**332.0**

† Full-duplex transmission (12.5 Gbps each direction)
†† Input signal sources (16.25 GHz in [86], 43.3, and 20 GHz in this work) not included
‡ The link is demonstrated with a three-channel TX and one-channel RX
‡‡ RX LO source (220∼300 GHz) not included

the previous record of 36 Gbps [86] at a similar BER of approximately 10^{-8}. The presented work is also the only published to date that include a fully-monolithic coupling scheme. Furthermore, this work has a significantly smaller waveguide cross section.

The demonstrated total link efficiency is competitive; the aggregate efficiency is 4.5 pJ/bit, which is higher than (though, competitive with) the record of 4.1 pJ/bit [98]. Compared to prior works, the demonstrated data rate density figure of merit is significantly higher – almost 12 times higher than previously-published work. This can be attributed to the use of single-mode waveguides and higher carrier frequencies, along with the efficient use of the available waveguide bandwidth through wideband coupling and muti-channel aggregation.

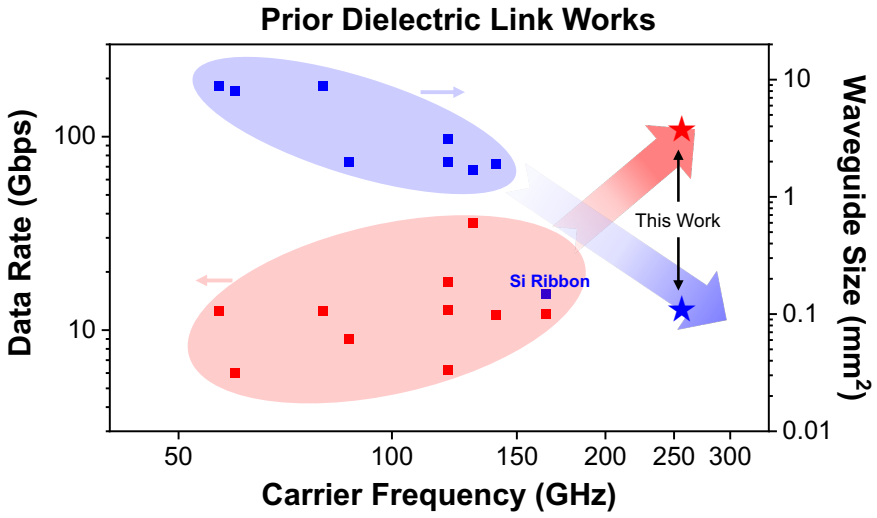


Figure 5-31: Current published dielectric link work comparison.

In conclusion, Fig. 5-31 show a plot demonstrating contemporary current dielectric waveguide works, with their demonstrated data rates and waveguide sizes, as a function of operating frequency and how this work compares. As one can see, this link has advanced the state of the art in both aggregate rate and in the wave guide size.

As the first end-to-end THz dielectric link, implemented entirely monolithically utilizing multi-channel aggregation, this work has shown competitive energy efficiency in a BiCMOS process. This can certainly be improved through the use of other processes and the use of more complex modulation formats; for example, moving to

quadrature modulation would improve data rate and potentially efficiency.

Movement to a higher operating frequency and multi-channel aggregation improves the total data rate by a factor of 3 over the state of the art and the reduce the waveguide size, improving the lane capacity density figure of merit by a factor of almost 12.

Chapter 6

Conclusion

6.1 Summary

This dissertation investigated the context in which an intermediate range interconnect, encompassing chip-to-chip, module-to-module, and board-board ranges, based on guided modulated THz carriers would fit in applications such as data centers and high performance computing. The comparison to existing electrical copper-based and short-range optical interconnects was presented. A number of components and technology developments that directly enable THz interconnect were discussed. This discussion included trade-offs associated with various component choices and historical data on active device performance.

In addition, this work presented a notional link architecture based on a set of independent channels, frequency multiplexed together on a single waveguide. A detailed analysis was carried out to understand the critical trade-offs associated with the multiplexer specifications. A vestigial sideband (VSB) modulation scheme using representative circuit performance figures of metric was utilized to quantify performance in terms of aggregate data rate and lane efficiency employing a rectangular dielectric waveguide.

Simulation results were presented to validate the link analysis. These results demonstrate that the concept is tenable and achieves high aggregate lane rates. Lastly, a discussion of future component/system research pursuits were enumerated

that would make this concept more attractive.

Individual component enablers were developed, to include novel design approaches and closed-form analytical models based on first-principle electromagnetics. Sub-THz passives were build/fabricated and thoroughly characterized to validate models. In the case of both the wideband power coupler presented in Chapter 3 and the sub-THz in-package triplexer in Chapter 4, the fabricated devices represent the state of the art in performance.

Lastly, fully-integrated transmitter and receiver chips were fabricated, links were assembled, and tested. The results, in Chapter 5 represent a significant improvement over the state of the art in this field in both data rates and data rate densities while maintaining competitive power efficiency compared to more modern silicon process implementations.

6.2 Areas of Future Investigation

Following the survey of prior work in all the constituent components in Section 1.2, it is clear that there are a variety of areas where continued exploration will provide significant improvements in performance and cost associated with the implementation of these types of links.

The continued development and characterization of materials for use as THz guides is important. This will, in turn, inform the achievable performance for a variety of different types of guide geometries – beyond the simple rectangular dielectric waveguide presented here. Taking cues from the integrated photonics community may prove useful in increasing achievable lane densities in the context of longer interconnects that might be found in board-to-board applications.

The solid-state circuits community has, and continues to, pursued aggressively pursue increased THz signal source power and efficiency. The community continues to leverage device feature scaling – and more importantly, device speed scaling. A focus on lowering phase noise will become more important as this type of interconnect becomes a more feasible alternative to higher-loss electrical copper-based intercon-

nects or more expensive optical interconnects. In addition, the circuit community continues to pursue increasing signaling rates and efficiencies in baseband circuitry to address optical interconnect/communication. THz interconnect technologies can directly leverage these efforts towards more efficient baseband technologies.

The use of multiple parallel transceivers, just as in optical WDM schemes, requires continued work on efficient and high-performance channelization/multiplexing schemes. There is a wealth of information and experience in this area as it relates to the software defined radio (SDR) community for access to lower-frequency bands and smaller bandwidths. This is an area where research could contribute substantially to improve the overall receiver SINR – and thus leading to improvements in channel and lane rates, as well as potentially significant improvements on lane efficiency.

Realizing high-performance analog multiplexers will be important to the successful demonstration of these types of links. The choice of on- or off-chip multiplexer has a number of packaging, cost, and performance implications. These implications require co-design of the associated transceiver circuitry, the wideband power coupler, and the waveguide itself.

Lastly, the development of efficient and broadband power couplers for THz interconnects is another area for further work. The choice of waveguide/package/coupler integration concept, waveguide material, waveguide geometry, operating bandwidth, and the decision to utilize on- or off-chip coupling structures all play pivotal roles in realizable performance. This is a rich area in which a number of new and different concepts could be pursued. Achieving sub-dB coupling loss would contribute almost an order of magnitude improvement in current state of the art SINR and efficiency figures in these types of links. Just as in the multiplexer discussion, this would have significant impacts on lane rates and efficiency. The use of new topologies and materials in MCM or SIP technologies are interesting and may provide an attractive path forward.

Appendix A

Dielectric Waveguide and Coupler Modeling Techniques

This section describes some of the high level trade offs associated with modeling the coupler-waveguide interface. This dicsussion will focus on techniques using both the Ansys HFSS [2] and the MEEP [77] computational electromagnetic packages.

As mentioned earlier in this thesis, this interface, by its sub-wavelength design, produces an inherently complex field profile around the structure. Furthermore, given the large variation in characteristic feature scales within the coupler structure and subsequent waveguide modes, electromagnetic modeling can be challenging.

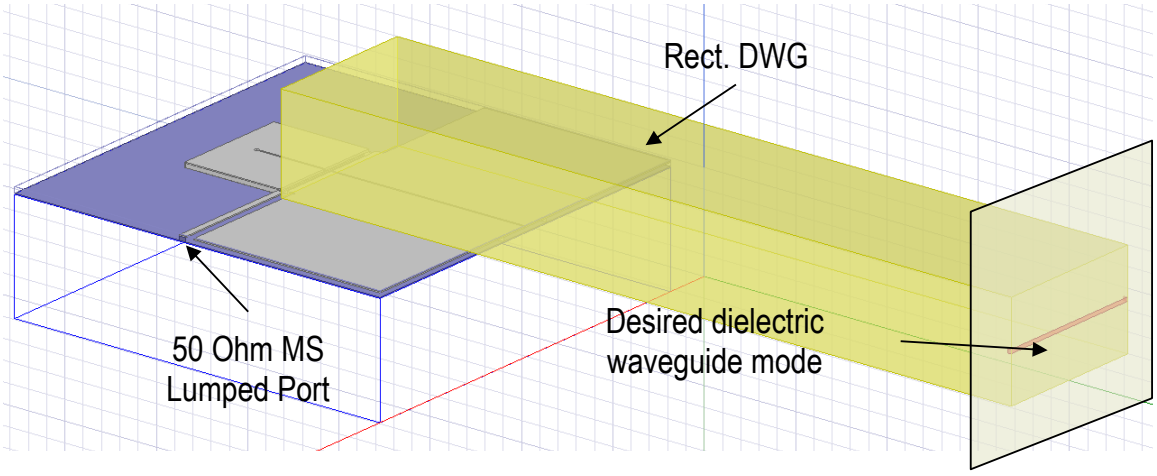


Figure A-1: Naive coupler-waveguide modeling scenario.

Ideally, modeling and design of this structure would be as simple as what is shown in Fig. A-1, in which a lumped port, compatible with an on-chip excitation, is used to excite the coupler structure. A small section of waveguide, at the end of which, a waveport is used to measure the resultant dielectric waveguide (DWG) mode. Unfortunately, there are a number of challenges associated with this type of approach. At a high level, one can categorize these issues as either related to waveguide mode degeneration and near-/far-field interactions. Both of these challenges force one into a situation that requires larger/longer models and precludes the use of conventional techniques used to reduce electromagnetic model size.

A.1 Near-/Far-Field Interactions

The first significant modeling concern is that of coupler-coupler near field effects. Given the permittivity of the materials one might consider for this scheme (ϵ_r between $5 \sim 12$), we can *estimate the guided mode's wavelength lower bound*

$$\lambda_g \approx \frac{\lambda_0}{\sqrt{\epsilon_r}}, \tag{A.1}$$

in which we assume a homogeneous and infinite guide material. This isn't strictly true for a sub-wavelength cross-section dielectric waveguide, but this approximation is helpful for this discussion. In practice, the guide wavelength is between λ_g and λ_0, as a portion of the mode at a given frequency lies outside of the guide material (see Fig. A-2 for example mode profiles).

If we adopt the view that this coupler-waveguide interface is, in essence, an antenna with a physical size $D \sim \lambda_0$, we can estimate those regimes in which we expect the field behavior to be large reactive (near-field) versus radiative (far-field). The defining point between these behaviors is the Fraunhofer distance [27]

$$d_F = \frac{2D^2}{\lambda}. \tag{A.2}$$

Antenna theory provides that the far-field regime occurs for $d_f \gg \lambda$ and $d_F \gg D$

[27]. In the case of this coupler-waveguide structure, the radiative regime corresponds to a situation in which a stable mode profile is providing constant guided travelling wave power flow through a cross-section of the DWG. In order to ensure that the waveguide mode profile is *not reactive*, the electromagnetic model in Fig. A-1 must be longer than $2\lambda_0$ (at the shortest), and possibly longer than $2\lambda_0\sqrt{\epsilon_r}$. Furthermore, given perfect electric conductor (PEC) boundary conditions generally applied to waveports within a tool like HFSS [2], shorter coupler-waveguide models run the risk of further skewing the results via unanticipated interactions between these boundary conditions and the fields in and around the structure in this intermediate Fraunhofer regime. This, again, leads one to a much longer model, in which one would seek to de-embed a "radiative" mode (read: travelling wave within the DWG) from this waveport, back towards the coupler. These dynamics alone, in the $220 \sim 335$ GHz regime, call for models, like that shown in Fig. A-1, in which the waveguide extends significantly further than $3 \sim 10$ mm *beyond the end of the coupler.* Given the range of coupler dimensions' (many of which are on the order of single microns), a full parametric optimization becomes onerous with convergence issues requiring very fine mesh sizes.

A.2 Waveguide Mode Degeneration/Mode Coupling

Beyond the undesired near-/far field interactions, the second challenge is that of waveguide mode degeneration. Due to the loosely-confined nature of the waveguide modes utilized in this scheme, horizontal and vertically "polarized" hybrid modes can existing with similar propagation constants β. In the presence of any scatterers near or within the waveguide material (to include slight variations in the material permittivity ϵ_r), these modes can couple. It should be noted that hybrid modes cannot be strictly defined as either horizontally- or vertically-polarized, but the nomenclature is adopted here for the sake of brevity. Fig. A-2 demonstrate the two modes in

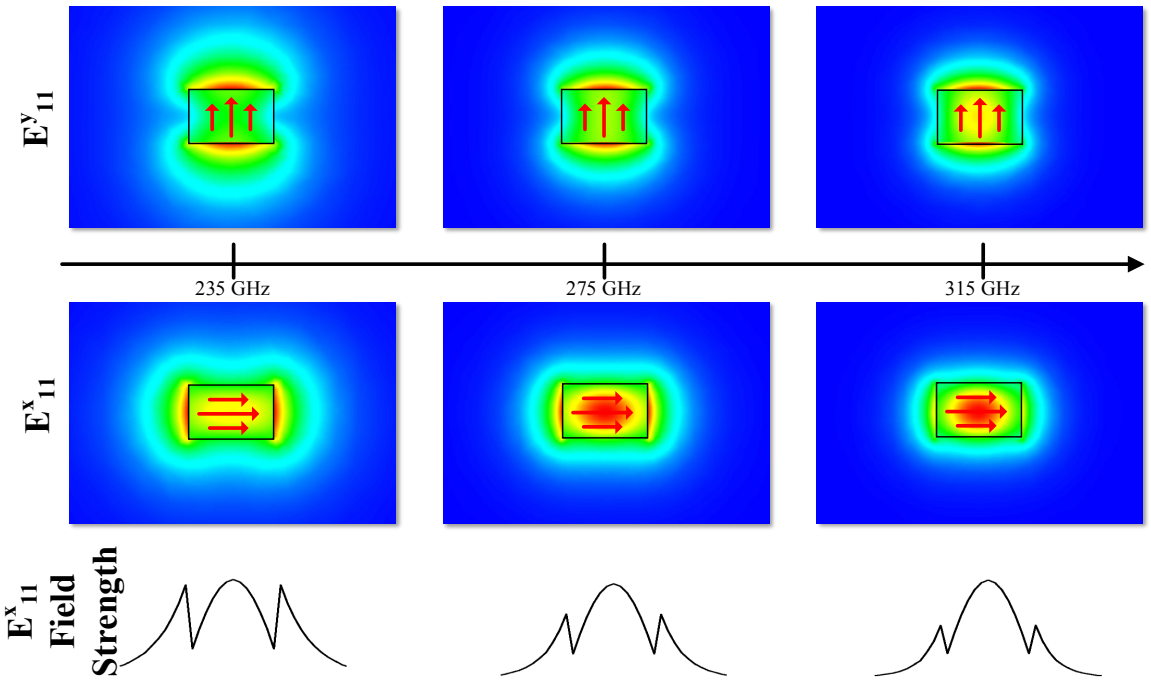


Figure A-2: The lowest-order hybrid modes supported by a rectangular cross-section dielectric waveguide. From [43].

question; this is not an exhaustive list of the modes present – many other higher-order modes existing within this structure, but they generally have dramatically different propagation constants, so mode coupling isn't a significant concern.

To further complicate modeling, as mentioned in the previous section, full-wave tools generally enforce PEC boundary conditions at the edges of waveports. This is consistent with interfacing with metal waveguides, which is the conventional use; indeed, Ansys recommends a conventional 2:1 aspect ratio for the waveports, in keeping with conventional metal waveguides [2]. However, tools like HFSS leverage the waveport geometry and computed eigenmodes, utilizing the 2D waveport and co-incident conductors and dielectrics, to assign an ordered priority to those modes which are supported at a given frequency (meshed and modeled). These artificial waveport PEC boundary conditions (even with a waveport size significantly larger that the DWG cross section) and aspect ratios can lead to different modal priorities as a function of frequency. This can be problematic when performing parametric dimensional optimization using resultant scattering parameters. One can often see an otherwise

smooth plot of S_{21} $[dB]$ with a highly-nonphysical discontinuities. This behavior corresponds, at that frequency, to a re-ordering of the modal priority within the solver. An exhaustive plotting of all other models modes will demonstrate that this power is indeed still carried through the structure, now in one (or more) other mode(s).

This effect can be ameliorated by forcing a preferred integration line or placing additional boundary conditions in the modal. For example, the use of a PEC plane to enforce horizontally-polarized symmetry (i.e. enforcing the E_{11}^{x} mode in Fig. A-2). When one chooses to do this, however, one is artificially precluding the existence of the other physical and *supported* modes that one would like to eliminate by DWG material choice and cross section design. In simple terms, utilizing this approach (forcing modal priority using non-physical and/or artificial boundary conditions) can likely lead to a final design in which undesired mode coupling exists, leading to poor guide dispersion and/or a reduction in overall response bandwidth.

Instead, a more expedient modeling technique, in which one first parametrically identifies DWG ranges of material ϵ_r and cross section dimensions without a coupler structure, was developed during this thesis work. Following this baseline material and guide cross section range determination, end-to-end simulation is used to fine-tune the DWG parameters and coupler dimensions to maximize bandwidth and reduce overall loss. In the future, a similar process could be leveraged to also optimize dispersion, should much larger signalling bandwidths be desired.

A.3 Initial DWG ϵ_r and Cross Section Selection

The hybrid modes utilized in the reported scheme don't allow for a separation of variables within Maxwell's equation [67]. Therefore, we cannot derive analytical expressions for each mode. Unfortunately, this precludes an analytical approach to the design of material properties and dimensions to control DWG bandwidth and operating band. Instead, we are forced to perform full-wave analysis in the pursuit of a given guide operating frequency, loss, and bandwidth.

Over the course of this research work, it was found that while Ansys HFSS is a

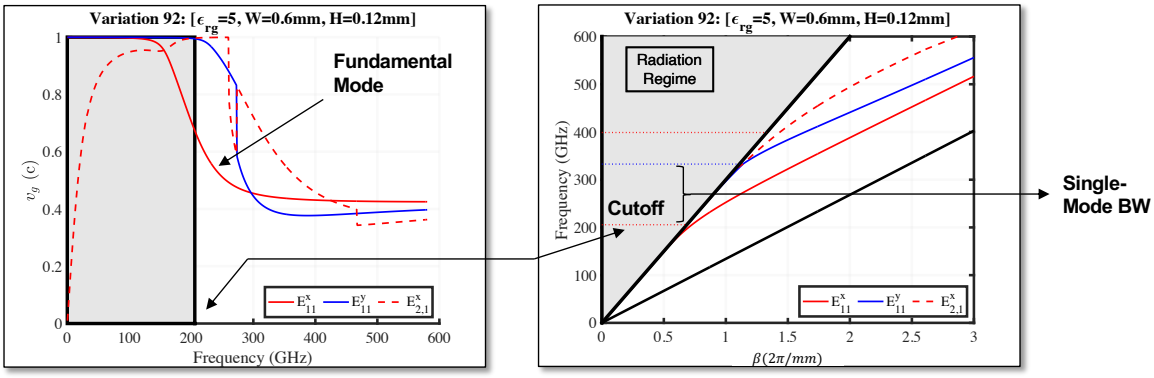


Figure A-3: Example of the utilized definition of DWG cutoff and single-mode bandwidth.

very powerful tool and extremely user friendly, the potentially large parametric variations and instability of these tools on our Linux deployment made their universal use impractical. Instead, we leveraged the MIT-developed MEEP [77] package with massively parallel compute resources at MIT and MIT Lincoln Laboratories to perform rapid parametric tuning of the waveguide materials and cross section. Specifically, we make use of the eigenmode solver within the larger MEEP distribution (MPB) to rapidly and scalably determine *initial* DWG cross section dimensions.

Because the DWG in question does not exhibit the same type of cutoff behavior one sees in conventional waveguides, we define a new cutoff frequency for the n-th mode f_{co_n} that corresponds to

$$v_{g_n}(f_{co_n}) = \sqrt{v_{g_{\epsilon_0,n}}(f_{co_n}) \times v_{g_{\epsilon_r,n}}(f_{co_n})}. \tag{A.3}$$

Here, $v_{g_n}(f)$ is the group velocity of the n-th mode, derived from the MEEP eigenmode solution. $v_{g_{\epsilon_0,n}}(f)$ corresponds to the group velocity in free space. Similarly, $\mathrm{v}_{g_{\epsilon_r,n}}(f)$ is the mode's group velocity in the waveguide bulk material ($\epsilon = \epsilon_r$).

In contrast to HFSS, the MEEP eigenmode solver provides very reliably modal order/priority, which allows one to extract the corresponding mode from the solver output without explicit inspection of the field profile in all cases. This allows for very rapid parametric search.

Fig. A-3 shows the frequency regime associated with this cutoff definition (shaded

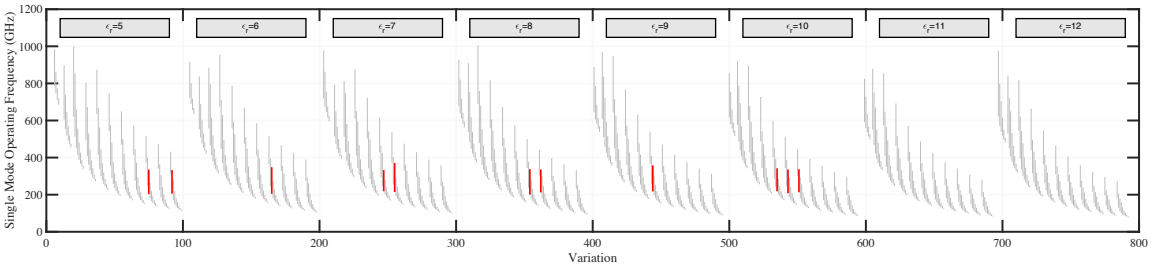


Figure A-4: Exhaustive parametric modeling of guide materials and cross sections.

gray area). The desired mode E_{11}^{x} is plotted in red. The vertically-polarized E_{11}^{y} mode is plotted in blue. A single-mode bandwidth is defined, utilizing our definition of cutoff,

$$\Delta f = f_{co_2} - f_{co_1}, \tag{A.4}$$

and is diagrammed in the right plot of Fig. A-3.

Using this definition of cutoff f_{co_1} and single-mode bandwidth Δf, an exhaustive search is performed across $\epsilon_r \in \{5, 6, ..., 12\}$, guide width $w = 100\mu m - 500\mu m$, and aspect ratio $A = 0.1 - 0.9$. Fig. A-4 demonstrates a sparse subset of those simulated parametric variations (only one out of every ten variations is plotted to allow for a more readable plot). In this plot, those variations in which

$$200\ GHz < f_{co_1} \leq 220\ GHz \tag{A.5}$$

and

$$\Delta f \geq 125\ GHz \tag{A.6}$$

are satisfied are colored red.

Further investigation was undertaken around those variations where both the cut-off and bandwidth conditions are satisfied to understand the impacts of variations in material properties. An example of this analysis is shown in Fig. A-5. Here, we show that a 10% variation in the material permittivity, *for these dimensional variations* has little impact on the guide cutoff f_{co_1}, but will naturally impact the guide propagation constant β. This analysis is helpful in determining which guide width and aspect ratios, w and A, respectively, are brittle to minor material variations.

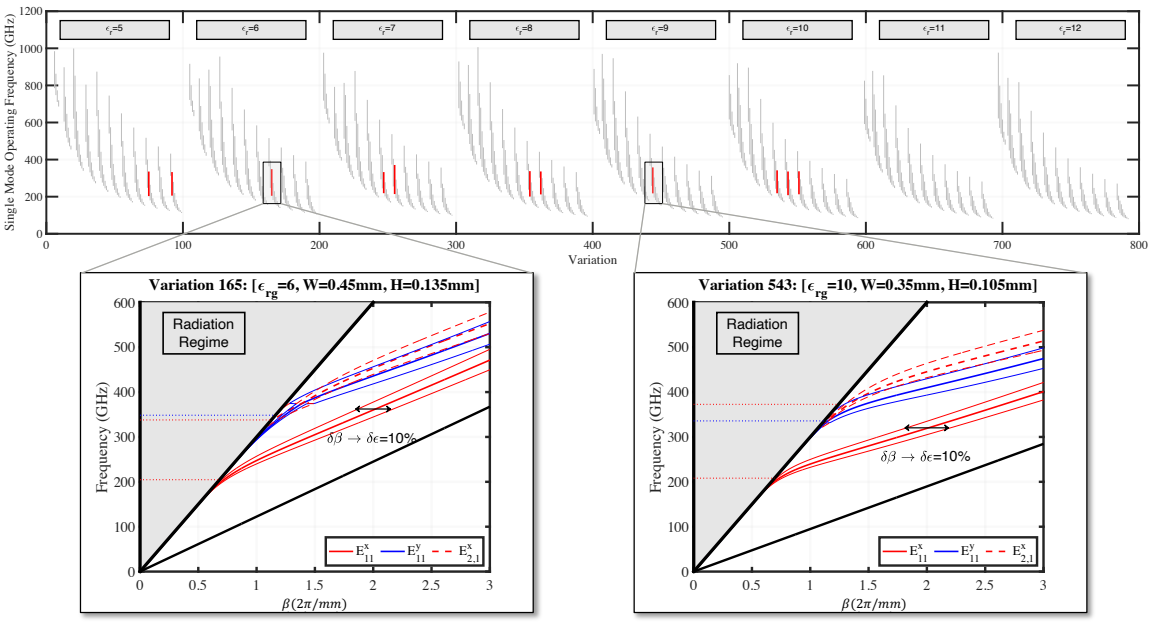


Figure A-5: 10% ϵ_r variation around a given DWG cross section and impact to Δf.

A.3.1 Impacts of DWG ϵ_r on Guide Dielectric Losses

Given these results and the intuition that associates stronger mode confinement with higher DWG ϵ_r, one may be tempted to design a DWG with a material with the highest available ϵ_r. There are obvious bandwidth and cutoff constraints at higher permittivity (as illustrated by the lack of red solutions at $\epsilon_r \geq 11$ in Fig. A-4 and A-5). Higher mode confinement also directly impacts realized guide dielectric losses.

While the MEEP package does not natively support lossy dielectric materials, the package provides direct access to the full complex electromagnetic vector field at each frequency, and can be used to estimate the losses in the DWG.

The time-averaged power carried by the n-th mode along the guide at position z is written

$$\left\langle P^{(n)}(z)\right\rangle = \left\langle P_0^{(n)}\right\rangle \times e^{-2\alpha_d^{(n)} z}. \tag{A.7}$$

We can then write the dialectic loss per unit length as

$$-\frac{\partial\left\langle P^{(n)}(z)\right\rangle}{\partial z} = 2\alpha_d^{(n)} \times \left\langle P^{(n)}(z)\right\rangle.$$

We define a mode confinement factor that characterizes the ratio of the power in

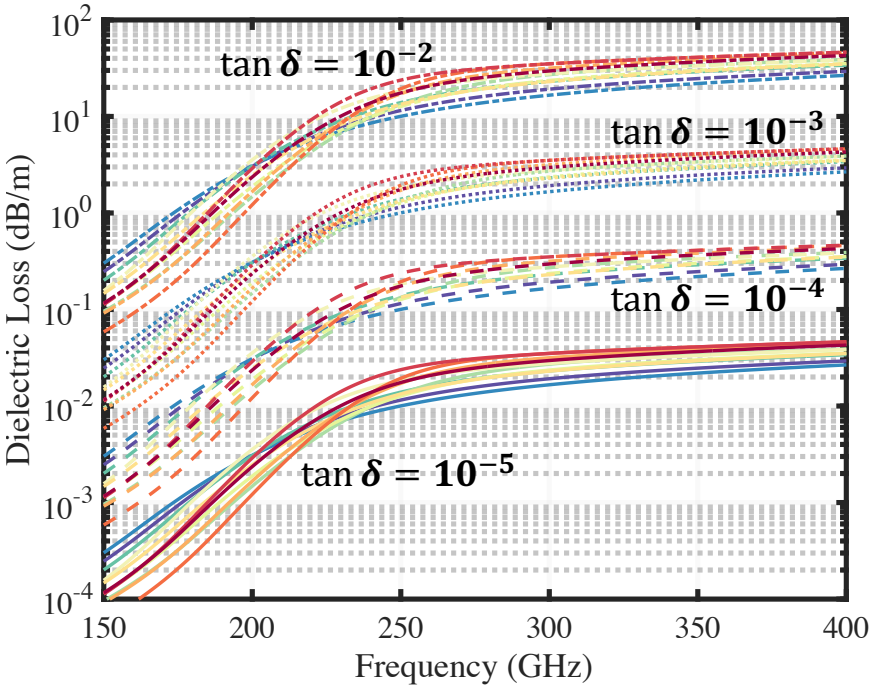


Figure A-6: Impacts to guide ϵ_r on dielectric losses.

the guide Γ_g and surrounding the guide cross section Γ_c, with $\Gamma_g + \Gamma_c = 1$. Both of these quantities can be supplied directly from the MEEP suite at each parametric variation, across frequency. We approximate the dielectric loss

$$\alpha_d \approx \frac{\omega}{2v_g(f)}[\tan\delta \times \Gamma_g(f)], \tag{A.8}$$

and plot the loss per meter length in Fig. A-6.

As one would intuit, higher mode confinement at the same material loss ($\tan\delta$) leads to increased losses in the guided mode. A higher percentage of the mode is interacting with the lossy dielectric material. This higher mode confinement comes from higher ϵ_r and/or higher frequency (smaller λ).

For a given loss tangent, selection of a different guide cross section (a single color in Fig. A-6), *can chance the estimated dielectric loss by as much as a factor of five.*

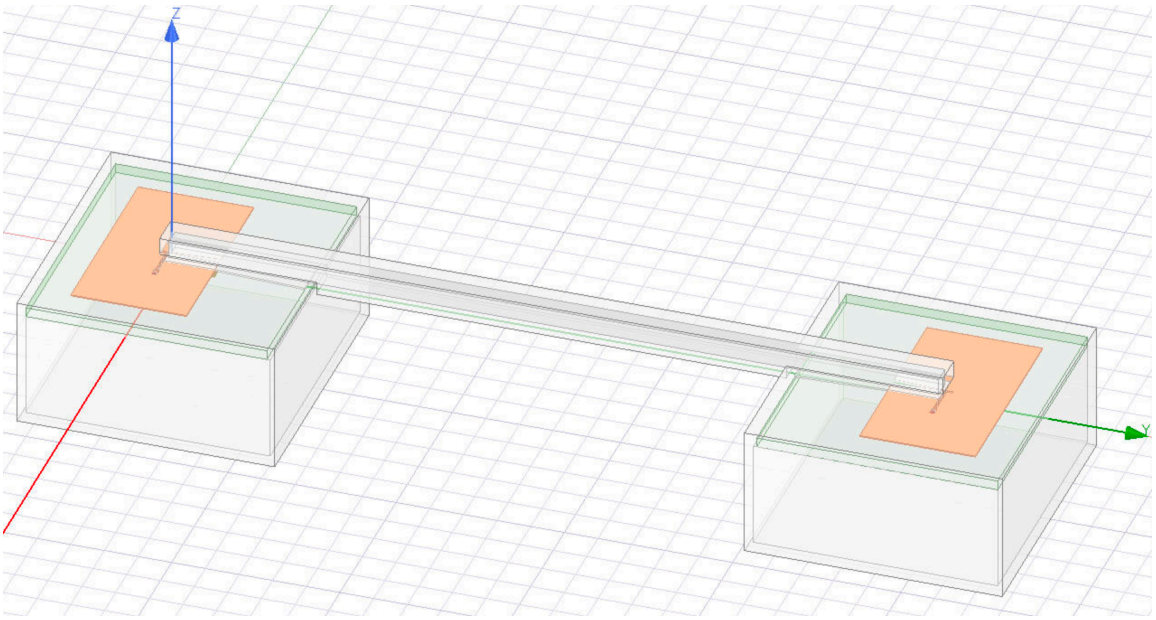


Figure A-7: End-to-end simulation to tune coupler dimensions and waveguide cross section.

A.4 Coupler-Waveguide Tuning

Once candidate cross sections *ranges* and materials have been determined via the techniques outlined earlier, one can then begin the task of co-optimizing the final coupler and waveguide dimensions. Of note – as this research focused on the use of existing low-cost materials, the material permittivity is limited to those available materials. In this case, we had access to various Rogers R3000-series materials that had permittivities from $\epsilon_r \approx 6.15 \sim 10.2$.

In addition, while the simulation setup in Fig. A-1 might be ideal from a model size perspective, as discussed in the previous sections of this appendix, the use of waveports can artificially alter the coupler-waveguide response. As such, final coupler-waveguide tuning is carried out using back-to-back coupler-waveguide-coupler models. This allows for the unambiguous excitation of the overall structure at both ends.

Fig. A-7 shown an isometric 3D model of a fully-parameterized coupler-waveguide-coupler model in Ansys HFSS. 50Ω lumped (circuit) ports are located within the 3D model, realizing a two-port channel.

As was discussed earlier in the appendix, one may desire a shorted waveguide in

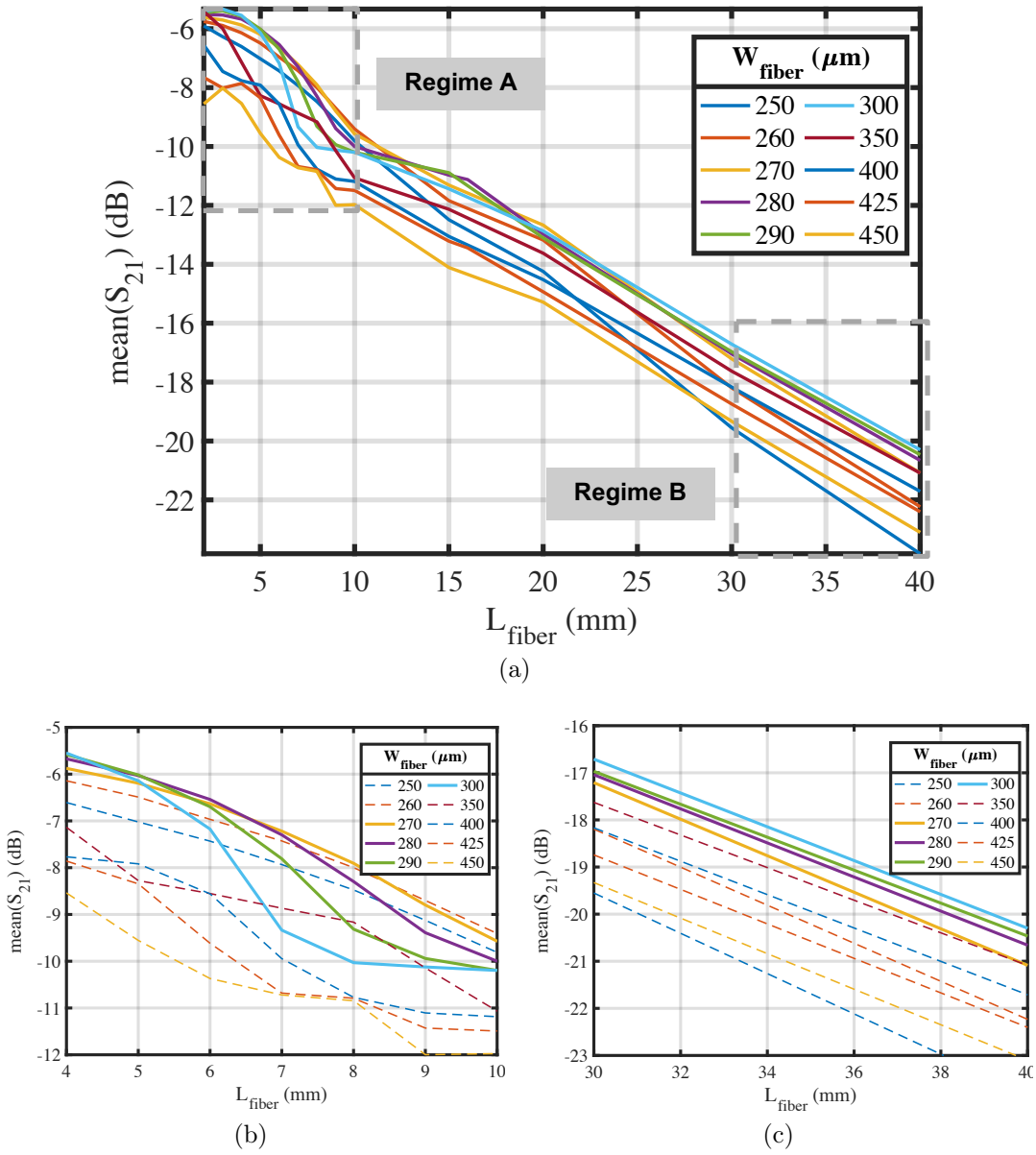


Figure A-8: (a) The impact of waveguide length in DWG cross section tuning. (b) Regime A: shorter DWG lengths, and (c) Regime B: longer DWG lengths.

order to reduce the overall model size, the required mesh size, and subsequent memory and solve time. It was found that, per the discussion in Section A.1, near-field/far-field effects can play a role in the solution. Fig. A-8a shows the results of a series of full-wave simulations of a coupler-waveguide-coupler model, similar to that shown in Fig. A-7. Here, the average loss across the passband is reported over guide length for various guide widths (L_{fiber} and W_{fiber}, respectively). The DWG material and guide height are held constant throughout the parametric variations. Furthermore,

we denote two areas, in dotted grey lines, Regime A and Regime B, corresponding to the extreme near-field and far-field coupler-coupler interactions. Fig. A-8b and A-8c show zoomed-in plots of these two regimes.

If one attempts to reduce the overall 3D model size by reducing the DWG length to something near the $2\times d_F$ (from Eq. A.2), optimization of the average transmission loss across the band of interest will likely arrive at a guide width of $W_{fiber} \approx 260 \sim 280\mu m$. However, as one can see from the larger model (Fig. A-8c), a higher-performance solution would required a wider DGW width ($W_{fiber} \approx 300\mu m$).

This discussion is designed to be illustrative of the disadvantages of reducing the model size to manage computation complexity. While this discussion focused on one set of dimensional parameters over just the waveguide width, this same behavior can be seen over other parameters. Unfortunately, model complexity reduction via reduced waveguide size is not a tenable approach, and can lead to non-optimal solutions.

A.4.1 Techniques to Reduce Model Complexity

As was discussed in Section A.2, large scale parametric waveguide variational analysis is leveraged to converge on a range of material properties and cross sections. This is allows us to constrain the parameter space in subsequent full-wave modal (driven) analysis. One can use other techniques to further speed up model meshing and solving to accelerate parametric tuning.

One obvious approach is to utilize PEC for all metals. While ohmic losses within the chip BEOL can be significant, it was found that these losses are secondary to radiative losses. Likewise, dielectric losses, though they can be significant, tend be secondary compared to radiative and mode-coupling losses in these types of coupler-waveguide-coupler structures. As such, one should consider utilizing totally lossless dielectrics during initial optimization to speed up processing.

Additional techniques that can be leveraged include the use of mixed-domain solvers. For example, a Finite Element-Integral Equation (FE-IE) solver was utilized for the model in Fig. A-7 and the results in Fig. A-8a. Compared to a conventional

all-FE solver, with it's requirement for a convex radiation boundary, an FE-IE solver (and associated *conformal* air box boundary) can dramatically reduce the overall volume and thus required mesh size.

Other techniques that have proven helpful include leveraging mixed-order basis functions and iterative solvers. Both require careful trial and error to show reliable performance advantages. Lastly, one may attempt to accelerate adaptive meshing by segmenting coupler and waveguide geometries to provide discrete volumes that are highly meshed prior to the first adaptive meshing. For example, the BEOL metal, oxide, and passivation layers in and around the coupler slot. The waveguide materials directly above the coupler slot, as well, is an appropriate volume to a priori mesh at a characteristic length on the order of the coupler slot width ($\sim 10\mu m$). This will generally allow for much more rapid adaptive mesh convergence across parametrically-varied geometry.

Appendix B

Waveguide Fabrication and Link Assembly Techniques

B.1 Dielectric Waveguide Fabrication

Through out this work, we utilized bulk sheets of Rogers RO3000-series printed circuit board laminates [17]. These materials are used for high-frequency circuit boards and are widely available. The bulk materials are ceramic-filled Polytetrafluoroethylene (PTFE) composites; the ratio of PTFE and ceramic is changed to engineer the dielectric constant. They were available from Rogers as 8" x 11" sheets with thicknesses of 130, 250, 640, and 1280 μm. All the bulk materials obtained from Rogers had full copper cladding – either 35 μm or 70 μm thickness. Following the full-wave analysis detailed in Appendix A, a final thickness of 250 μm was chosen to meet guide bandwidth and operating frequencies.

Copper cladding was removed from all the bulk materials using a bath of $FeCl_3$ (Ferric Chloride), followed by an ultrasonic bath of distilled water, and a final rinse with acetone to remove final copper particulate. A visual inspection was undertaken using a microscope to verify the material was free of copper particulate or residue.

Guide designs were designed in any CAD package capable of export to a DXF file format (HFSS, Solidworks, ADS, were all utilized during this work). The waveguide design is simply the top silhouette as the material is cut from a flat sheet. Material

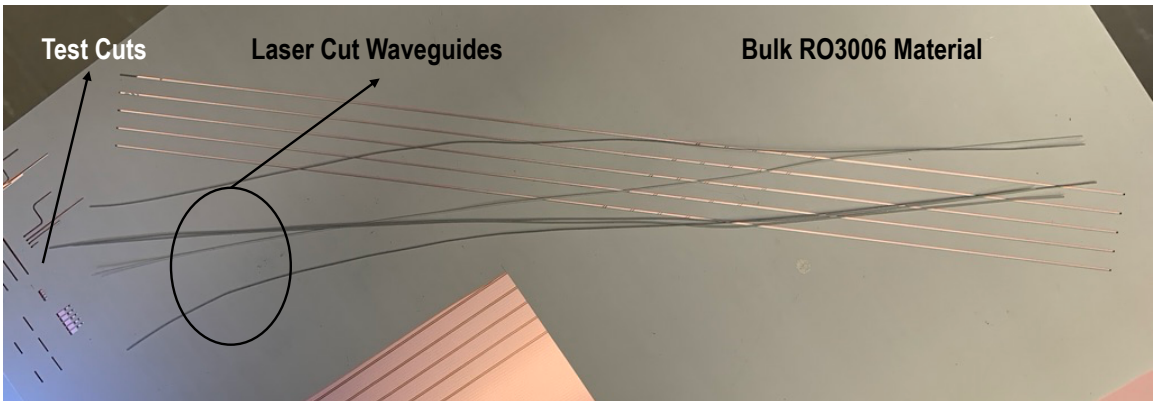


Figure B-1: Cut waveguides, bulk material, and test cuts.

is cut using an LPKF ProtoLaser U4 laser mill [62]. This tool provides a variable power and pulse-repetition frequency (PRF) 335 nm laser, focused to a 20 μm beam. When calibrated, this laser mill is capable of providing better than 2 μm of accuracy, though one must be careful as this accuracy drifts over time as the mill comes out of calibration.

Prior to each set of waveguides being cut, a series of test cuts with different laser powers, PRFs, and numbers of sweeps are performed on a sacrificial area of the bulk waveguide material sheet. Wide variability in these parameters were observed in order to make consistent cuts all the way through the materials while avoiding scorching.

Due to the way in which the laser is both grossly mechanically positioned as well as finely electrically steered, longer waveguide cuts required special attention to avoid excessive laser parallax-induced errors in the length of the guide. For waveguides on the order of 5-10 cm, this was not observed to be an issues. Longer cuts than this, however, required several waveguide designs be placed in parallel and cut, each ~ 5 μm shorter or longer than the desired (nominal) length. Furthermore, due to the variability in required laser power, PRF, etc. several *identical* waveguides, whose designs were closely placed in parallel on the bulk sheet, were cut for a single assembly. This generally yielded approximately 50%, providing several viable waveguides after cutting, prior to preparation and assembly.

After cutting, in order to separate the bulk material sheet from the waveguides without tearing, twisting, or otherwise destroying the waveguides, it was found that

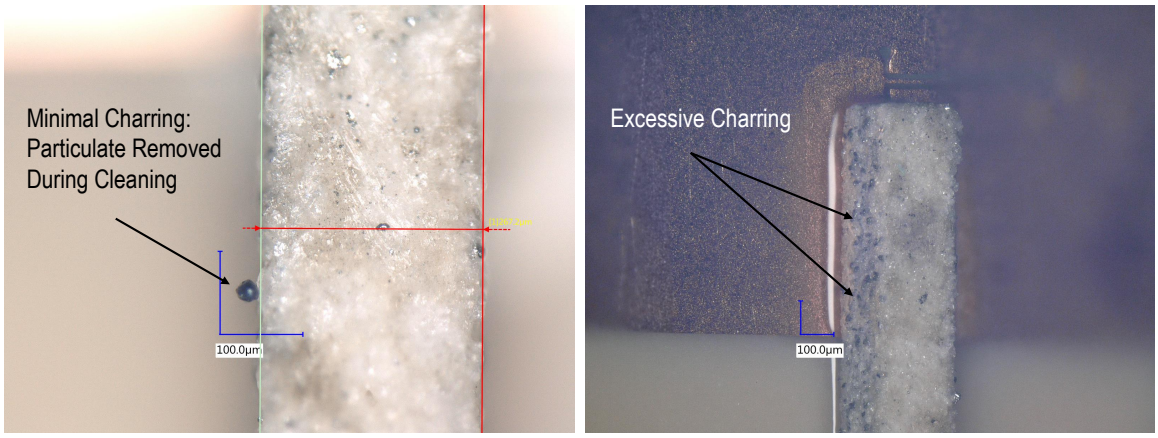


Figure B-2: Examples of charring in cut waveguide materials.

keeping the laser mill vacuum chuck engaged while gently lifting the remaining bulk material at a corner and peeling the material off of the vacuum chuck provided the best results. The vacuum chuck was then disengaged and the freshly cut waveguides were picked up using tweezers and placed onto a static-free Gel-Pak.During the early stages of this research, it was discovered that attempting to grasp the waveguides and peel them away from the bulk material caused significant damage to the waveguides and/or caused the waveguides to become twisted, causing subsequent bonding to become impossible. Fig. B-1 shows some 30 cm long waveguides, cut from a piece of bulk material.

During laser cutting, the waveguides (and bulk material) build up an electrostatic charge. It was found that allowing the waveguides to rest for some time ($\sim$1 hour) in a static-free bag or Gel-Pak dramatically reduced this electrostatic charge, allowing more freedom to maneuver the waveguide on the chip passivation during bonding.

Next, a visual inspection of the waveguides is performed under a microscope. Samples are measured to ensure they are the correct width and length, as well as remove any waveguides with any undesired twisting and/or curve. While the material is very flexible, any undesired curve – however slight – in the waveguide can prove very difficult to correct during the bonding process. They they are also examined for excessive charring (Fig. B-2). Those waveguides with incorrect dimensions and those with excessive charring are discarded. The remaining waveguides are cleaned,

in preparation for bonding, with an ultrasonic bath of distilled water and detergent, followed by a rinse using acetone, and a final ultrasonic bath using distilled water. The waveguides are allowed to dry in a positive-pressure, clean and dry nitrogen environment.

B.2 Waveguide-Chip Bonding

The waveguides, once cleaned, are ready for bonding. The chip passivation is similarly cleaned of any debris found under a microscopic inspection. A low-loss epoxy from EpoTek is used to realize the bond. While low loss and lower dielectric constant are important, post-fabrication forensic analysis indicates that even with hand-assembly, one can achieve a very intimate waveguide-coupler bond, with epoxy layers less than 10 μm thick. As such, the losses though this layer are minimal. In practice, it was found that the viscosity of the bonding epoxy played a much more significant role in achieving successful bonding than the specific dielectric proprieties of the epoxy.

Ultimately, one wants a fairly low viscosity epoxy, that presents the lowest self-adhesion possible, but sets within $\sim$ 15 minutes, allowing the flexibility for re-work without require extremely long setup time. A variety of epoxies were used and some experimentation was done with varying the epoxy heat and even introducing small amounts of acetone into the mixture to reduce the viscosity. Additional work needs to be done in this area to refine the process, ultimately increasing yield.

Fig. B-3 shows some of the details surrounding the tooling used to facilitate the bonding. A modified pick-and-place (the micro-positioner tool with a Teflon-tipped vacuum tool) and tweezers are used to first position the waveguide near the chips and ensure that the waveguide is rotated such that the bond will be done with the top or bottom face of the waveguide and not the left or right face. This is important as these waveguides have a rectangular cross section and determining aspect ratio through a microscope can be challenging. One technique is the make a small mark on the bulk material sheets using a permanent marker. This will indelibly mark the top and/or bottom face of the waveguide, making it easier to identify orientation through

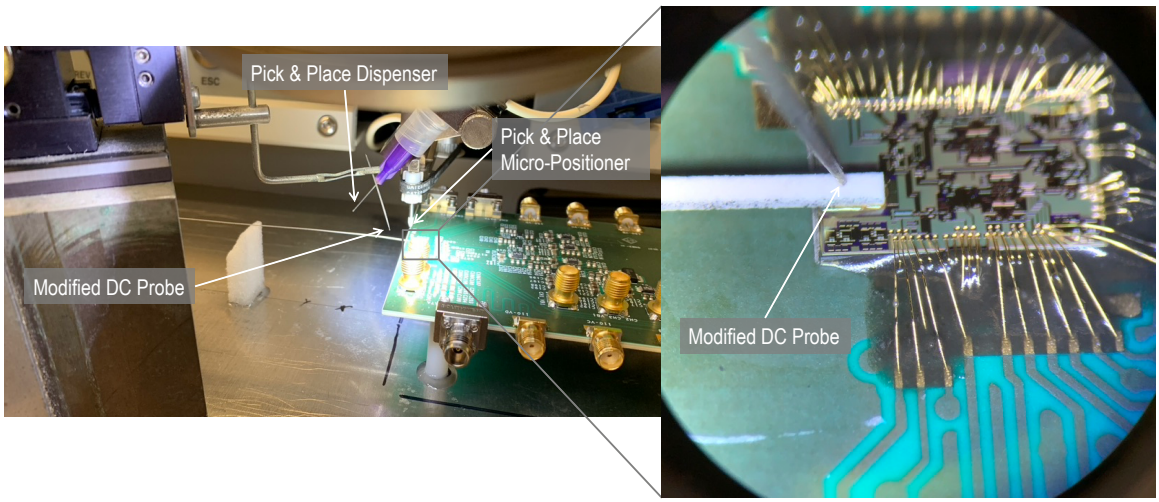


Figure B-3: Waveguide-chip bonding flow.

a microscope one the waveguide is in place.

Next, a modified DC probe is placed into position near the tool with sufficient x-, y-, and z-travel to land the probe tip on top of the chip's coupler. This DC probe will act as an ersatz clamp to both hold the waveguide in position (to ensure good setup of the epoxy) and provide downward pressure (to ensure a thin bond).

The epoxy material itself is then prepared, in a small quantity. A small needle is used to capture the smallest single drop of epoxy and subsequently transfer this to the tip of the pick-and-place dispenser needle (itself *not connected to any forced air*). This double-transfer of the material further reduces the total amount of material available for deposition on the chip's passivation. This is critical because of the smooth nature of the passivation layer; the surface tension of the material will cause it, if heavily deposited, to spread our significantly. In some cases, the epoxy may spread as far as nearby wire bond or probe pads, causing subsequent issues with testing, etc.

Using the small amount of epoxy on the pick-and-place dispenser needle, very carefully position the dispenser needle above the center of the coupler. Very gently touch the small droplet of epoxy to the passivation surface. One will see the epoxy immediately adhere to the surface and begin to spread out. It is not uncommon to require the droplet to be gently landed in a few locations on the coupler to ensure good coverage.

Next, the pick-and-place tool is rotated from the dispenser needle to the Teflon-tipped vacuum micro-positioner. This tool is used to pickup the waveguide, which should already by placed nearby, within the microscope field of view. The rotation of this tool, coupled with the vacuum chuck, should be sufficient to make minor alignment changes and land the waveguide on the passivation. One should see a noticeable movement of the previously-deposited epoxy. While maintaining downward pressure and stable positioning of the waveguide using this Teflon-tipped tool using one hand, the other hand should then begin moving the DC probe into position to maintain the waveguide's position and provide downward pressure (Fig. B-3, right inset). Once the waveguide is in position and the DC probe tip is providing stabilization and downward pressure, one should not disturb the setup until the bond epoxy is set up, and preferably until it is fairly hard. This is a function of the amount of epoxy, type of epoxy, ratio of compounds, material heat, etc. The most successful bonds during the final link assembly each required approximately one hour of stable time before moving on to the next bond. Additional experimentation is required to refine this process flow, as well.

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